

MODEL NAME : *RANGER 17*
 PCB NO : *LA-9331P*
 BOM P/N : *4619KL31L01*

Compal Confidential

RANGER 17

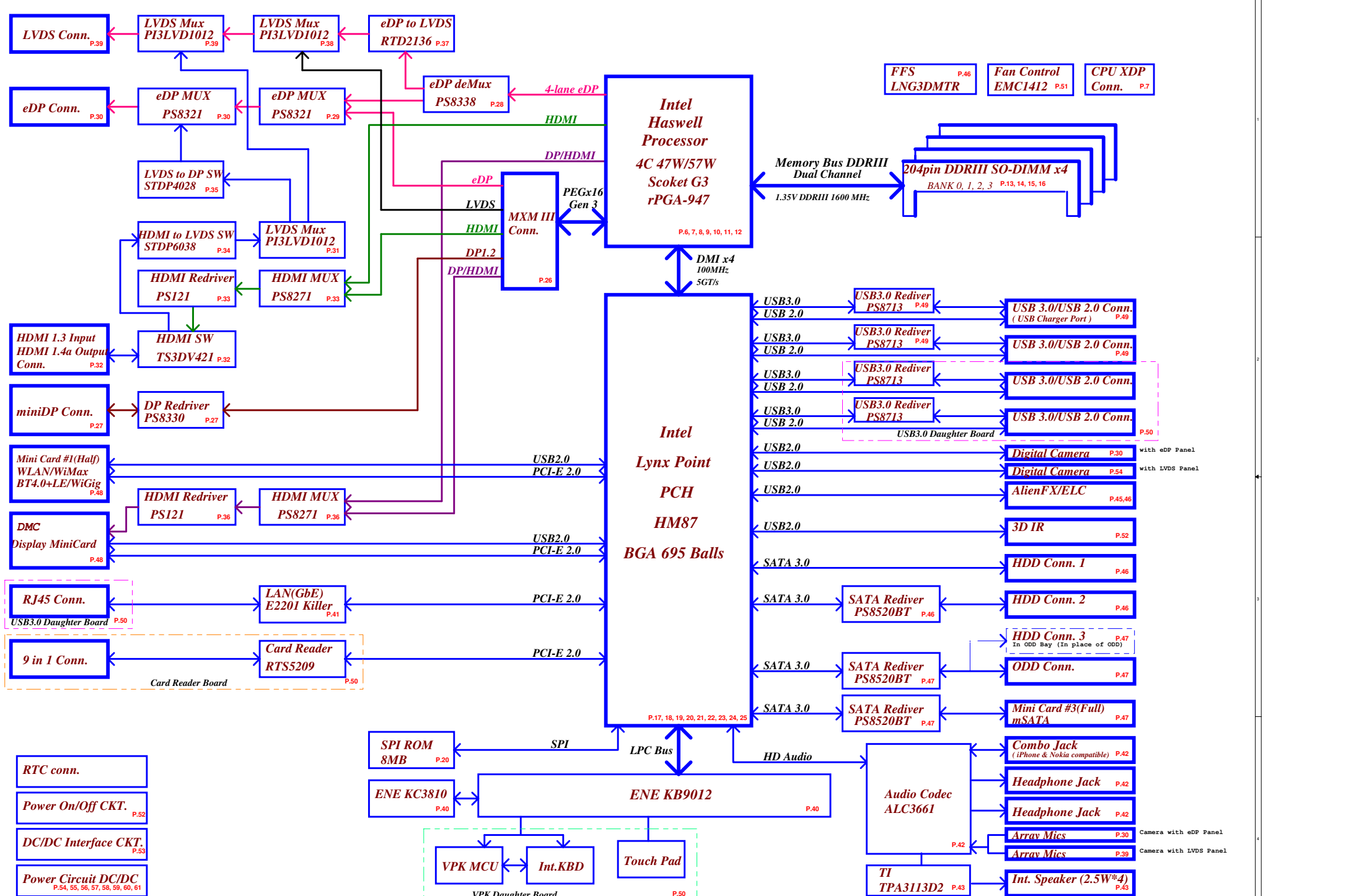
Schematic Document

Rev: X00

2012-06-22

@ : Nopop Component

Security Classification	Compal Secret Data			Title <i>Compal Electronics, Inc.</i>	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title <i>Cover Sheet</i>	
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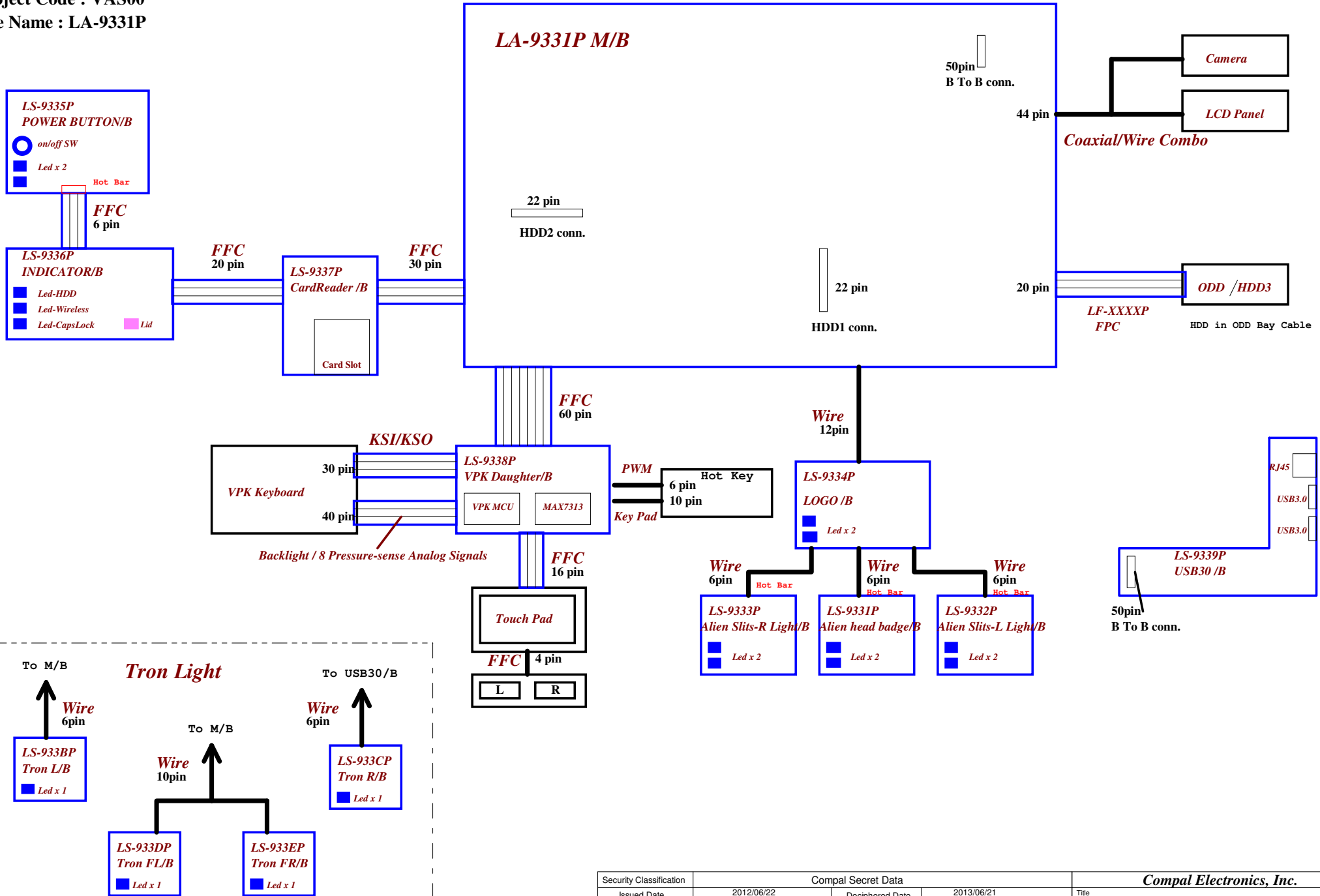


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Project Code : VAS00

File Name : LA-9331P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (OT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connction
1	JUSB1 (Left side)
2	JUSB2 (Left side)
3	NA
4	NA
5	JUSB3 (Right side)
6	JUSB4 (Right side)

USB PORT#	DESTINATION
0	JUSB1(USB3.0 P1)
1	JUSB2(USB3.0 P2)
2	JUSB3(USB3.0 P5)
3	JUSB4(USB3.0 P6)
4	JMINI1 (WLAN)
5	JMINI2 (DMC)
6	AlienFX/ELC
7	IR SENSOR
8	None
9	None
10	None
11	eDP CAMERA
12	LVDS CAMERA
13	VPK K/B

POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State	power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0		ON	ON	ON
S3		ON	ON	OFF
S5 S4/AC		ON	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF

Symbol Note :



CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_A	MXM			

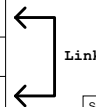
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

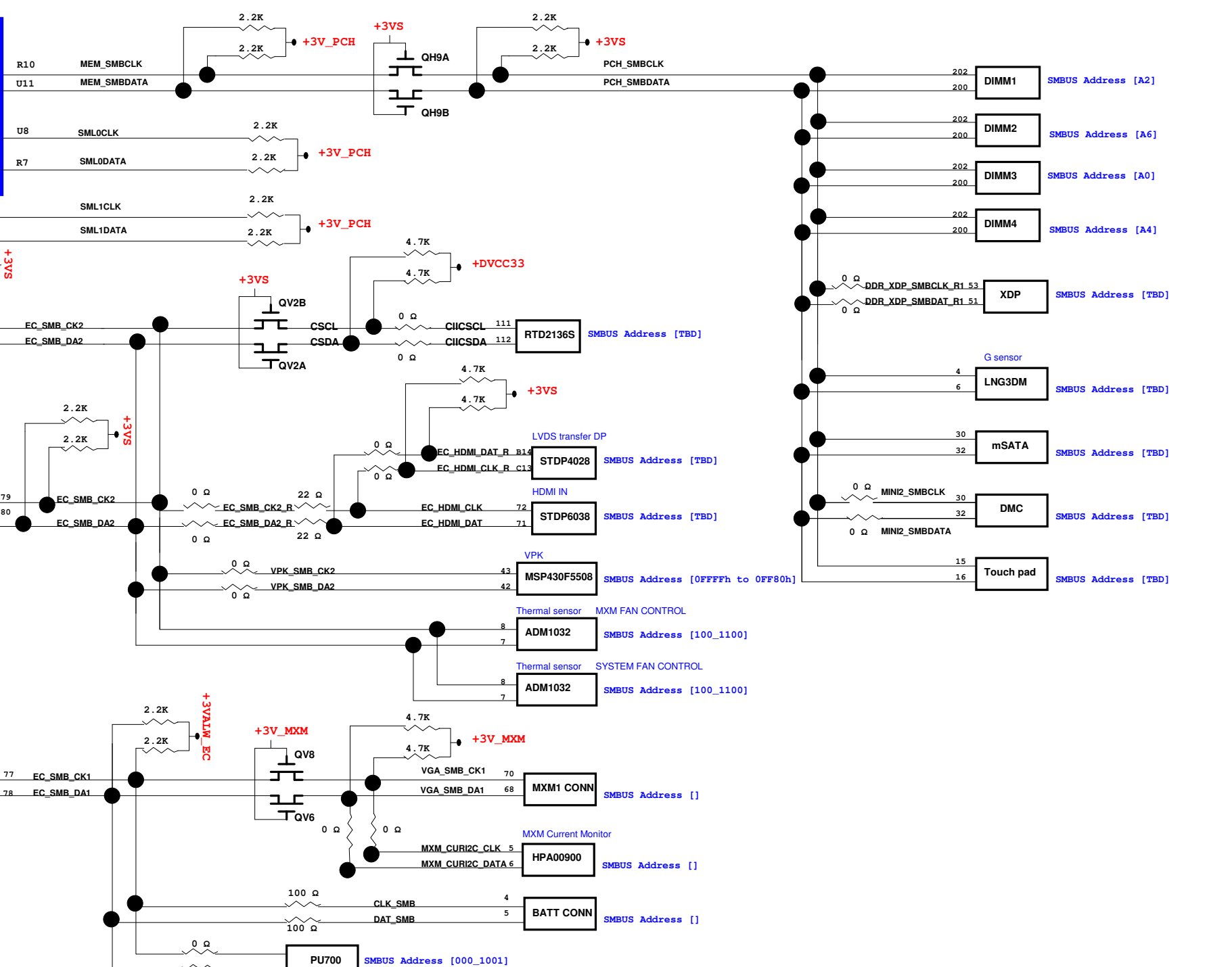
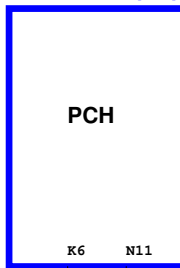
SMBUS Control Table

	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			✓								✓		✓		
EC_SMB_CK2 EC_SMB_DA2	KB9012				✓	✓	✓			✓	✓					
PCH_SML0CLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		✓		✓				✓				✓	✓	✓	✓

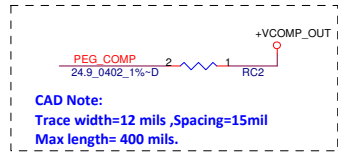


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SMBUS Address [TBD]

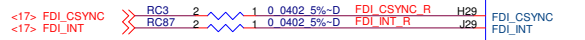
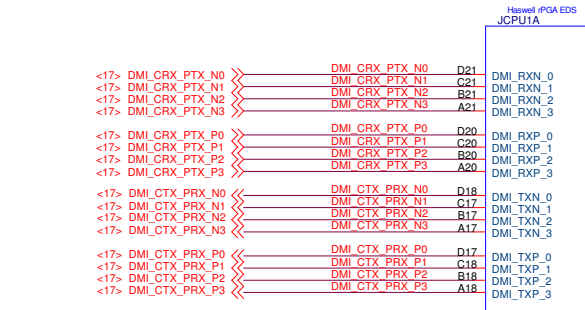


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CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

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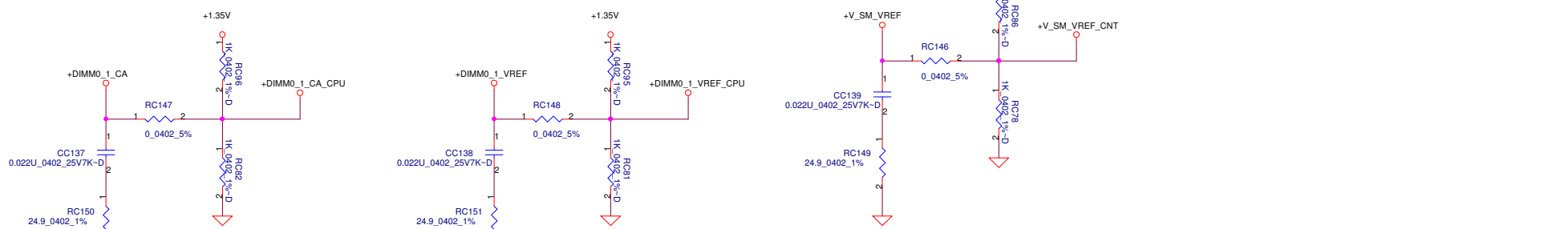


Signal	Value	Part	Value	Part	Signal
PEG_RCOMP	E23	PEG_COMP			
PEG_RXN_0	M29	PEG GTX C HRX N0	CC1	1	2 0.22U 0402 16V7K-D PEG GTX HRX N0
PEG_RXN_1	K28	PEG GTX C HRX N1	CC2	1	2 0.22U 0402 16V7K-D PEG GTX HRX N1
PEG_RXN_2	M31	PEG GTX C HRX N2	CC3	1	2 0.22U 0402 16V7K-D PEG GTX HRX N2
PEG_RXN_3	L30	PEG GTX C HRX N3	CC4	1	2 0.22U 0402 16V7K-D PEG GTX HRX N3
PEG_RXN_4	M33	PEG GTX C HRX N4	CC5	1	2 0.22U 0402 16V7K-D PEG GTX HRX N4
PEG_RXN_5	L32	PEG GTX C HRX N5	CC13	1	2 0.22U 0402 16V7K-D PEG GTX HRX N5
PEG_RXN_6	M35	PEG GTX C HRX N6	CC6	1	2 0.22U 0402 16V7K-D PEG GTX HRX N6
PEG_RXN_7	L34	PEG GTX C HRX N7	CC7	1	2 0.22U 0402 16V7K-D PEG GTX HRX N7
PEG_RXN_8	E29	PEG GTX C HRX N8	CC8	1	2 0.22U 0402 16V7K-D PEG GTX HRX N8
PEG_RXN_9	D28	PEG GTX C HRX N9	CC9	1	2 0.22U 0402 16V7K-D PEG GTX HRX N9
PEG_RXN_10	E31	PEG GTX C HRX N10	CC10	1	2 0.22U 0402 16V7K-D PEG GTX HRX N10
PEG_RXN_11	D31	PEG GTX C HRX N11	CC11	1	2 0.22U 0402 16V7K-D PEG GTX HRX N11
PEG_RXN_12	E35	PEG GTX C HRX N12	CC12	1	2 0.22U 0402 16V7K-D PEG GTX HRX N12
PEG_RXN_13	D34	PEG GTX C HRX N13	CC14	1	2 0.22U 0402 16V7K-D PEG GTX HRX N13
PEG_RXN_14	E33	PEG GTX C HRX N14	CC15	1	2 0.22U 0402 16V7K-D PEG GTX HRX N14
PEG_RXN_15	E32	PEG GTX C HRX N15	CC16	1	2 0.22U 0402 16V7K-D PEG GTX HRX N15
PEG_RXP_0	L29	PEG GTX C HRX P0	CC17	1	2 0.22U 0402 16V7K-D PEG GTX HRX P0
PEG_RXP_1	L28	PEG GTX C HRX P1	CC18	1	2 0.22U 0402 16V7K-D PEG GTX HRX P1
PEG_RXP_2	L31	PEG GTX C HRX P2	CC19	1	2 0.22U 0402 16V7K-D PEG GTX HRX P2
PEG_RXP_3	K30	PEG GTX C HRX P3	CC20	1	2 0.22U 0402 16V7K-D PEG GTX HRX P3
PEG_RXP_4	L33	PEG GTX C HRX P4	CC21	1	2 0.22U 0402 16V7K-D PEG GTX HRX P4
PEG_RXP_5	K32	PEG GTX C HRX P5	CC22	1	2 0.22U 0402 16V7K-D PEG GTX HRX P5
PEG_RXP_6	L35	PEG GTX C HRX P6	CC23	1	2 0.22U 0402 16V7K-D PEG GTX HRX P6
PEG_RXP_7	K34	PEG GTX C HRX P7	CC24	1	2 0.22U 0402 16V7K-D PEG GTX HRX P7
PEG_RXP_8	F29	PEG GTX C HRX P8	CC25	1	2 0.22U 0402 16V7K-D PEG GTX HRX P8
PEG_RXP_9	E28	PEG GTX C HRX P9	CC26	1	2 0.22U 0402 16V7K-D PEG GTX HRX P9
PEG_RXP_10	F31	PEG GTX C HRX P10	CC27	1	2 0.22U 0402 16V7K-D PEG GTX HRX P10
PEG_RXP_11	E30	PEG GTX C HRX P11	CC28	1	2 0.22U 0402 16V7K-D PEG GTX HRX P11
PEG_RXP_12	F35	PEG GTX C HRX P12	CC29	1	2 0.22U 0402 16V7K-D PEG GTX HRX P12
PEG_RXP_13	E34	PEG GTX C HRX P13	CC30	1	2 0.22U 0402 16V7K-D PEG GTX HRX P13
PEG_RXP_14	F33	PEG GTX C HRX P14	CC31	1	2 0.22U 0402 16V7K-D PEG GTX HRX P14
PEG_RXP_15	D32	PEG GTX C HRX P15	CC32	1	2 0.22U 0402 16V7K-D PEG GTX HRX P15
PEG_TXN_0	H35	PEG HTX GRX N0	CC33	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N0
PEG_TXN_1	H34	PEG HTX GRX N1	CC34	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N1
PEG_TXN_2	I33	PEG HTX GRX N2	CC35	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N2
PEG_TXN_3	H32	PEG HTX GRX N3	CC36	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N3
PEG_TXN_4	J31	PEG HTX GRX N4	CC37	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N4
PEG_TXN_5	C30	PEG HTX GRX N5	CC38	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N5
PEG_TXN_6	C33	PEG HTX GRX N6	CC39	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N6
PEG_TXN_7	B32	PEG HTX GRX N7	CC40	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N7
PEG_TXN_8	B31	PEG HTX GRX N8	CC41	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N8
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PEG_TXN_11	A28	PEG HTX GRX N11	CC44	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N11
PEG_TXN_12	B27	PEG HTX GRX N12	CC45	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N12
PEG_TXN_13	A26	PEG HTX GRX N13	CC46	1	2 0.22U 0402 16V7K-D PEG HTX C GRX N13
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PEG_TXP_3	G32	PEG HTX GRX P3	CC52	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P3
PEG_TXP_4	H31	PEG HTX GRX P4	CC53	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P4
PEG_TXP_5	H30	PEG HTX GRX P5	CC54	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P5
PEG_TXP_6	B33	PEG HTX GRX P6	CC55	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P6
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PEG_TXP_8	C31	PEG HTX GRX P8	CC57	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P8
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PEG_TXP_11	B28	PEG HTX GRX P11	CC60	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P11
PEG_TXP_12	C27	PEG HTX GRX P12	CC61	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P12
PEG_TXP_13	B26	PEG HTX GRX P13	CC62	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P13
PEG_TXP_14	C25	PEG HTX GRX P14	CC63	1	2 0.22U 0402 16V7K-D PEG HTX C GRX P14
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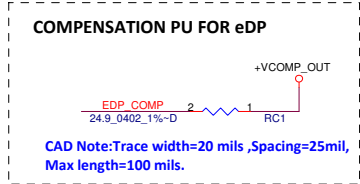
Near MXM Connector

INTEL_HASWELL_HASWELL

CONN@

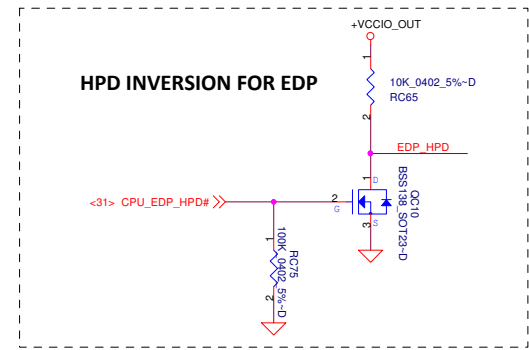
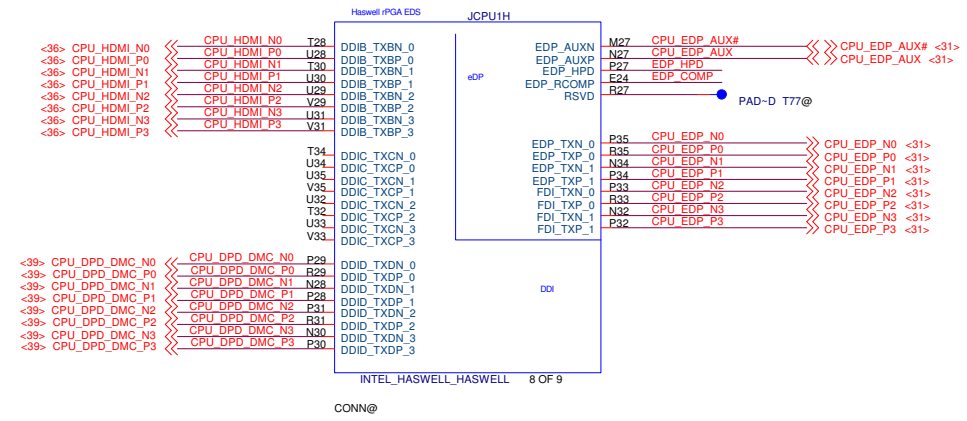


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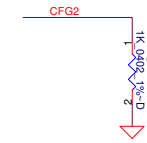
HDMI

DMC

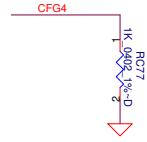


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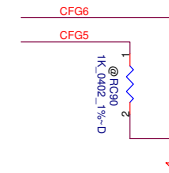
CFG STRAPS for CPU



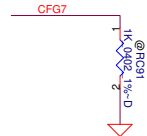
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



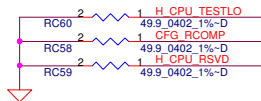
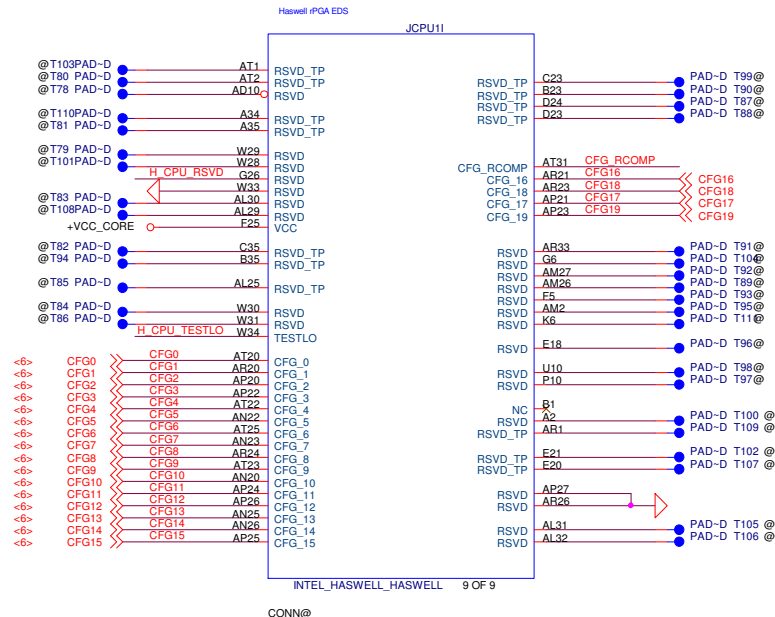
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

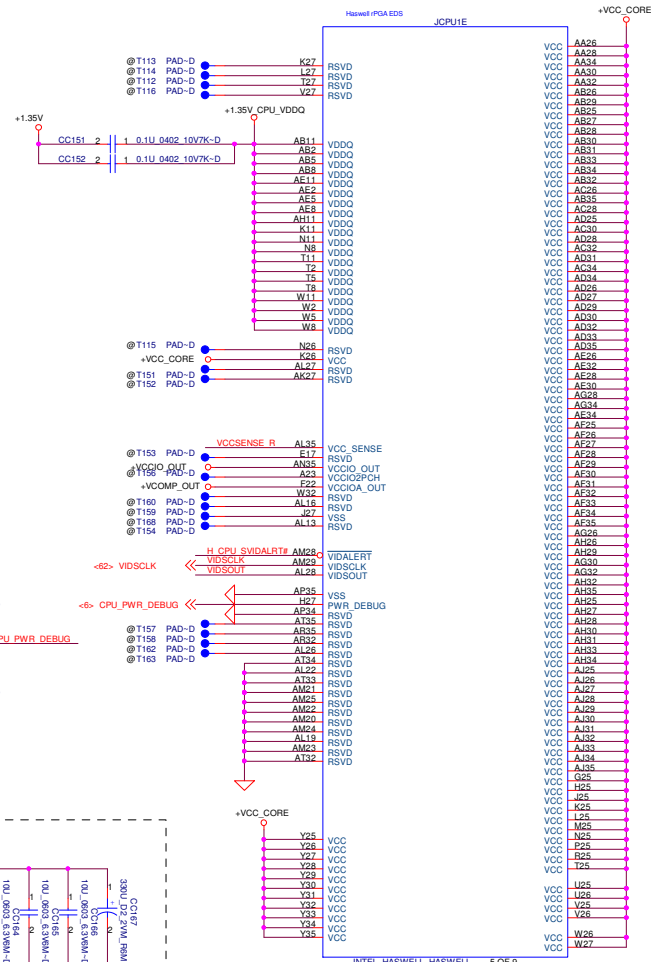
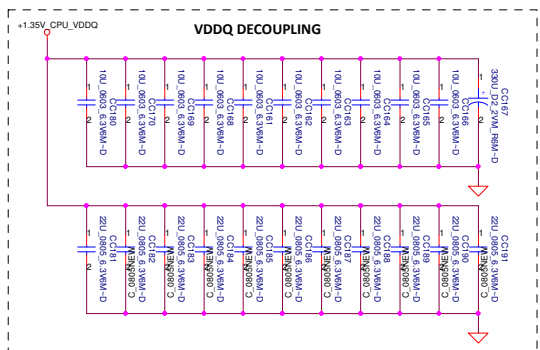
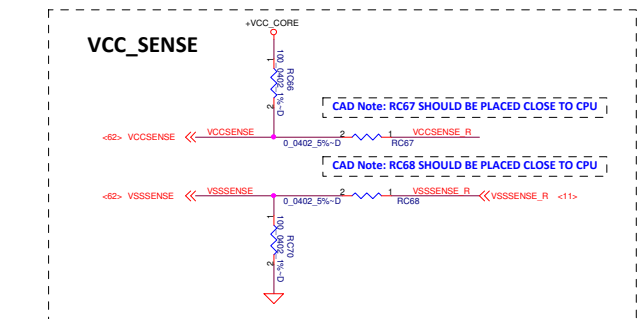
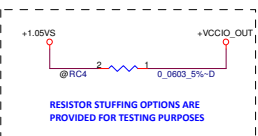
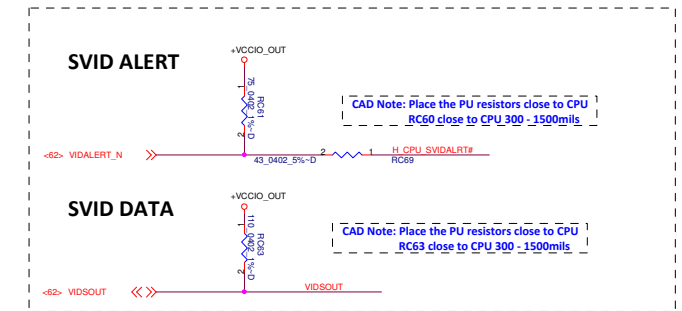
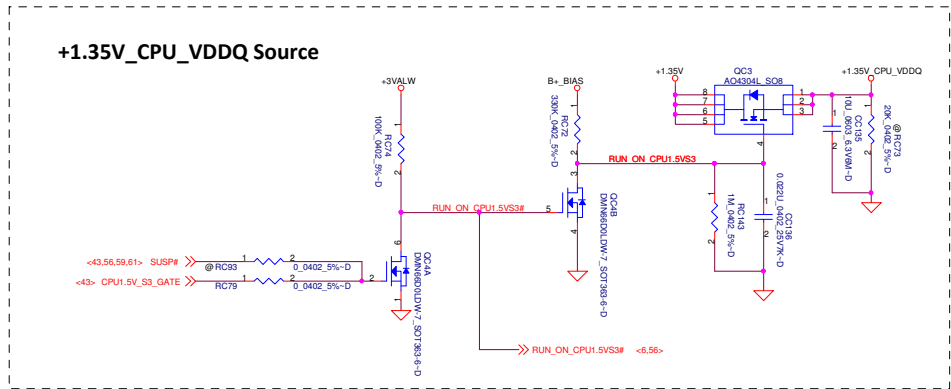


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





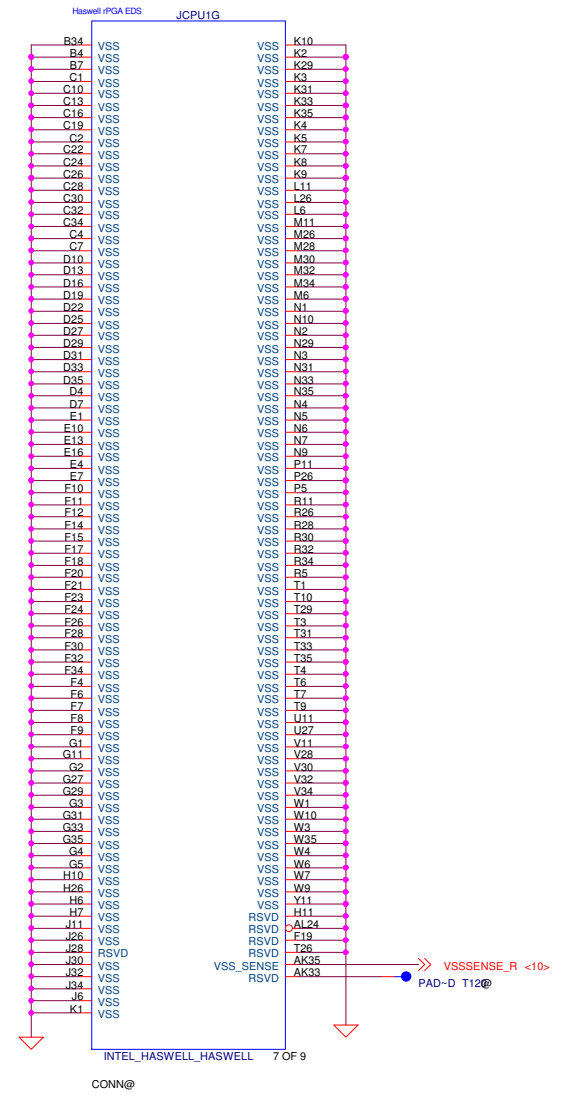
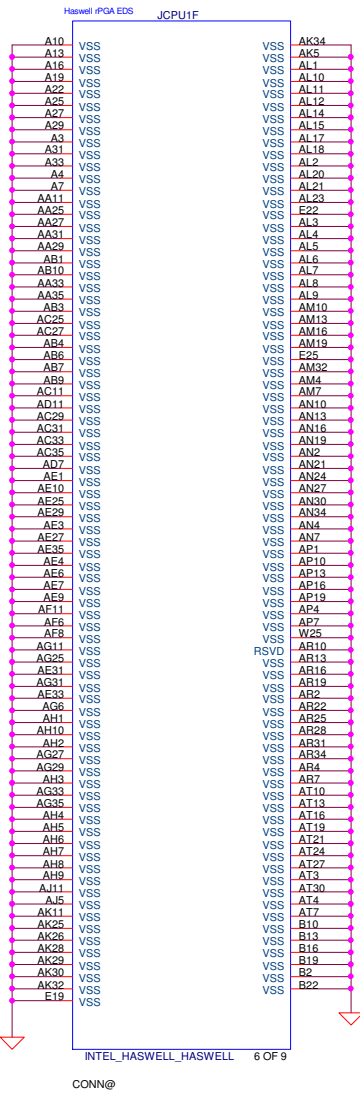
Security Classification	Compal Secret Data		Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Document Number
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				LA-931P
				11 of 61

Compal Electronics, Inc.

CPU (67) PWR

LA-931P

Friday, June 22, 2012



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				Rev 0.1
				Sheet 12 of 61

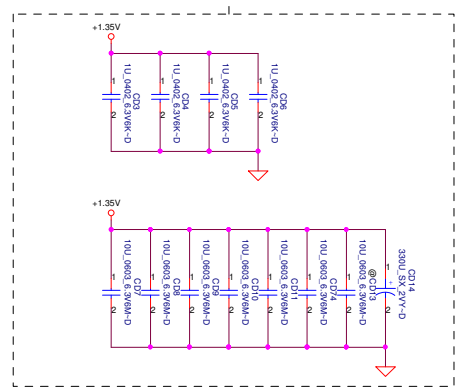
JDIMMA H=4mm



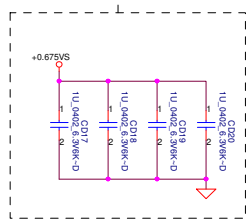
All VREF traces should have 20 mil trace width

- <7.14> DDR_A_DQS#(0..7) <<>
- <7.14> DDR_A_D(0..63) <<>
- <7.14> DDR_A_DQS(0..7) <<>
- <7.14> DDR_A_MA(0..15) <<>

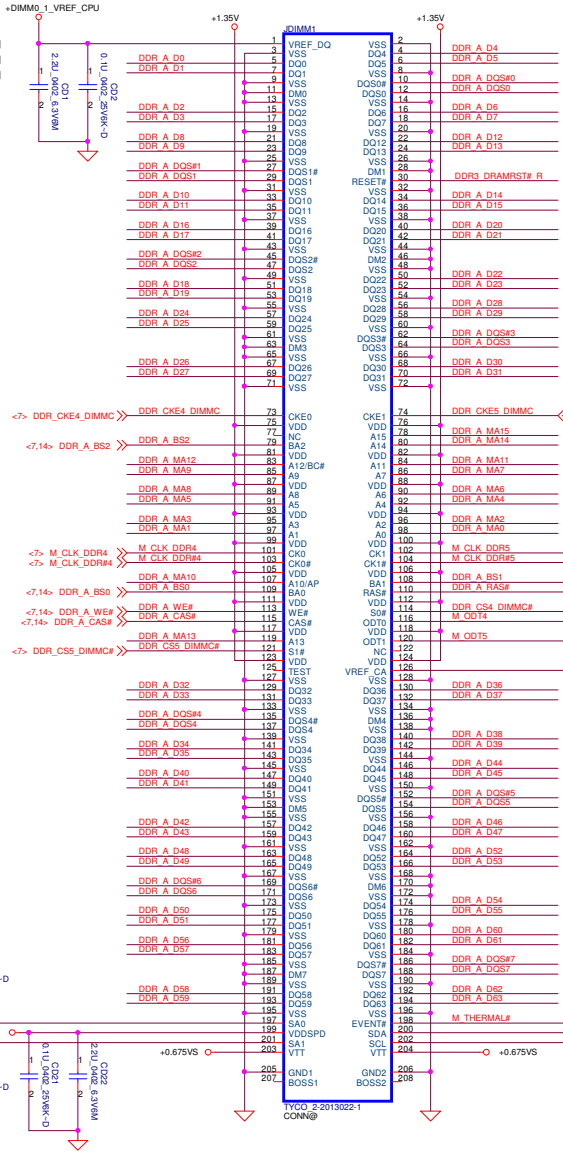
Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA.203,204

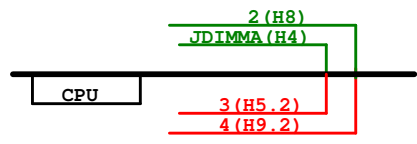


SA0	SA1	
1	0	DIMMIA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD

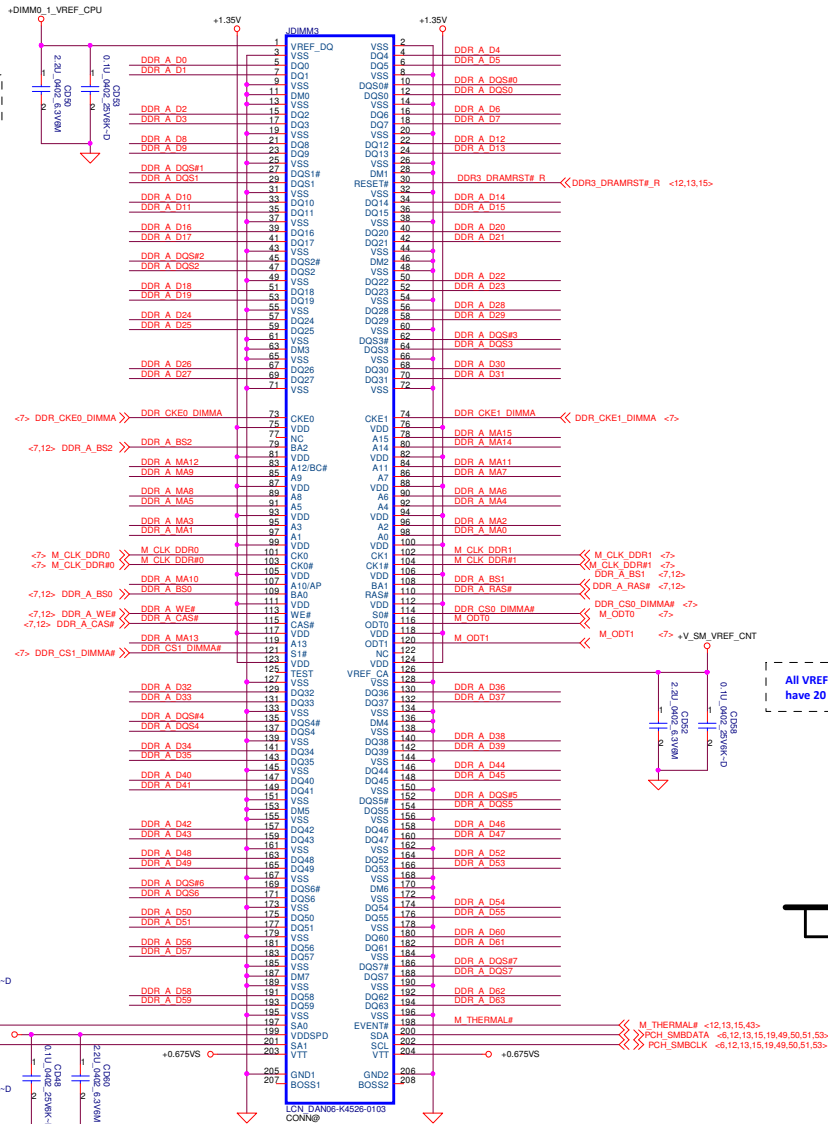


<-13.14.15> DDR3_DRAMRST#_R <<< DDR3_DRAMRST#_R RD29 1K_0402_5%-D >>> DDR3_DRAMRST#_CPU <->

All VREF traces should have 20 mil trace width



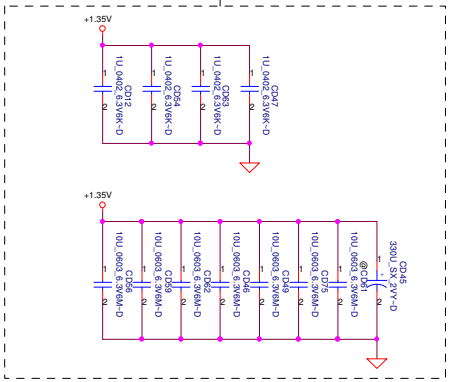
JDIMMC H=5.2mm



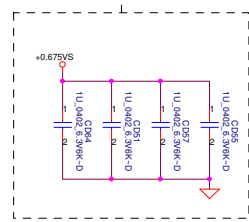
All VREF traces should have 20 mil trace width

- <-7.12> DDR_A_DQS[0..7] <<>
- <-7.12> DDR_A_D[0..63] <<>
- <-7.12> DDR_A_DQS[0..7] <<>
- <-7.12> DDR_A_MA[0..15] <<>

Layout Note:
Place near JDIMMC

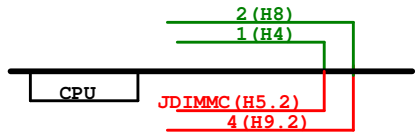


Layout Note:
Place near JDIMMC.203,204

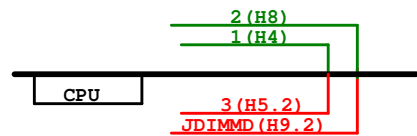
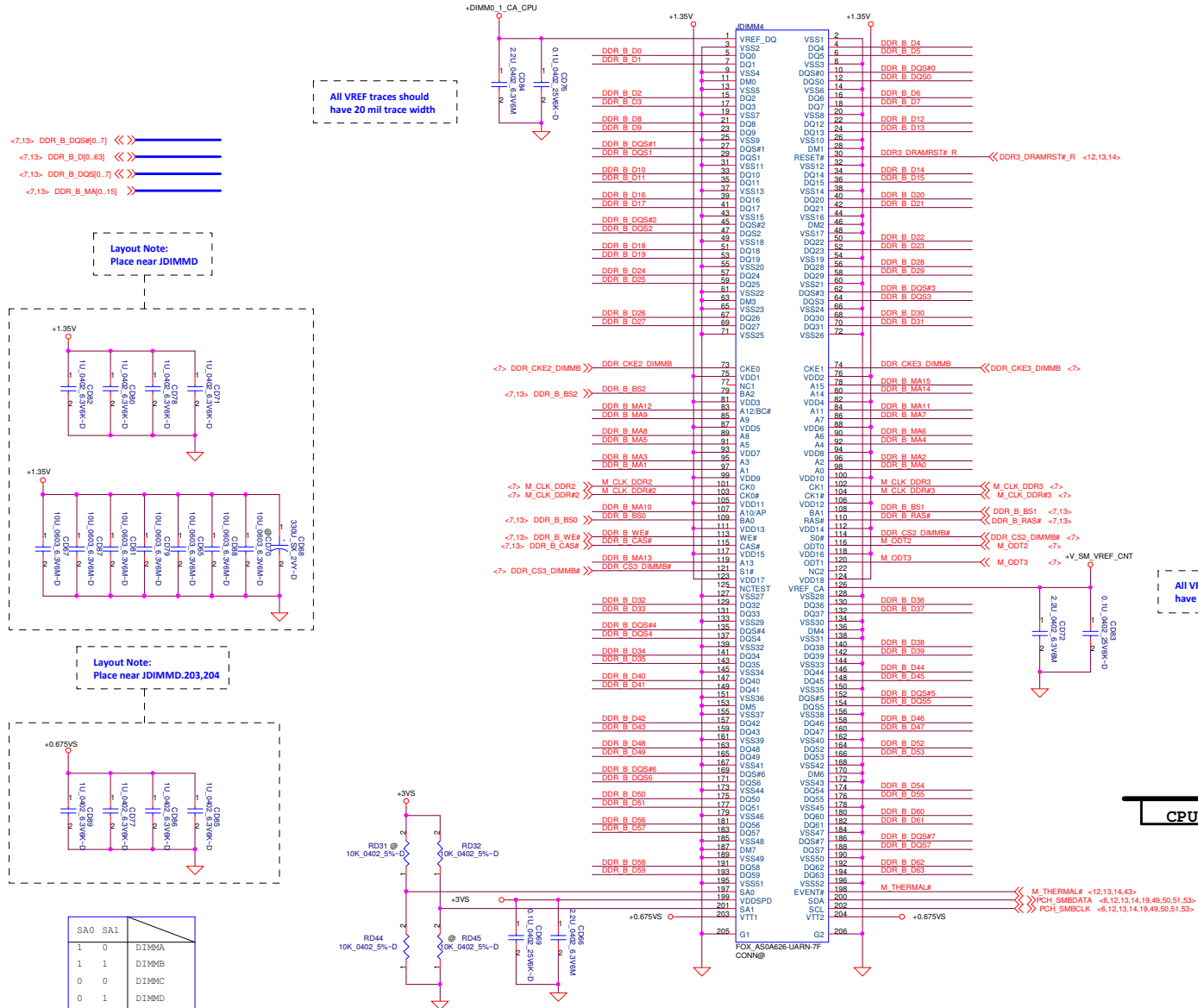


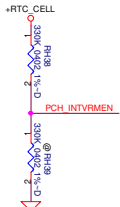
SA0	SA1	
1	0	DIMMA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD

All VREF traces should have 20 mil trace width



JDIMMD H=9.2mm



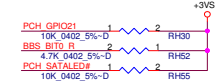
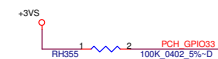


INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
 High - Enable Internal VRs
 Low - Enable External VRs



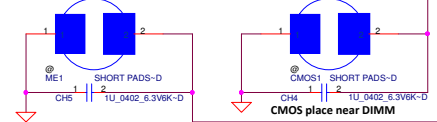
NO REBOOT STRAP
 DISABLED WHEN LOW (DEFAULT)
 ENABLED WHEN HIGH

FLASH DESCRIPTOR SECURITY OVERRIDE
 LOW = DESABLED (DEFAULT)
 HIGH = ENABLED

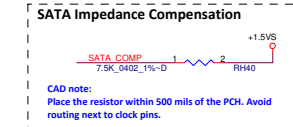
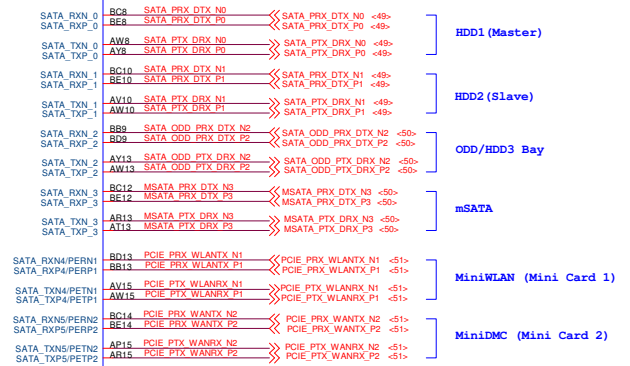
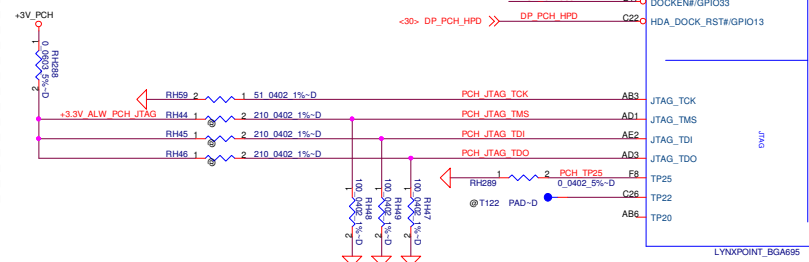
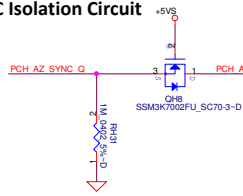


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

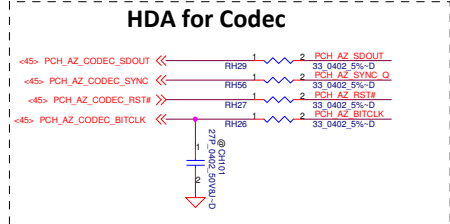
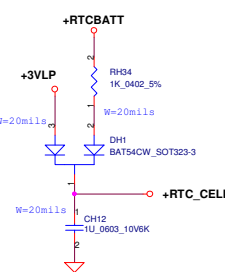
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

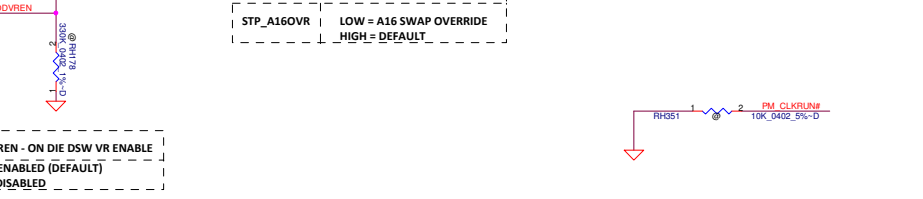
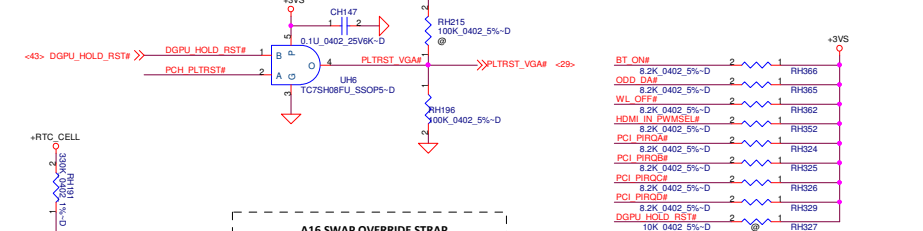
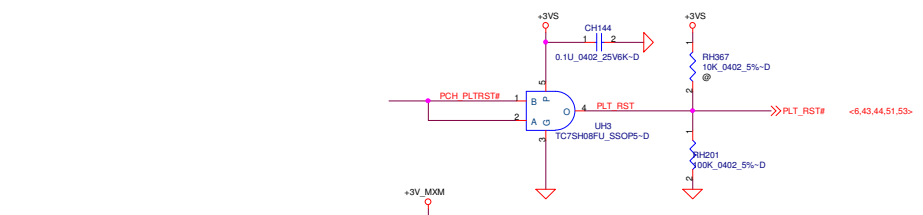
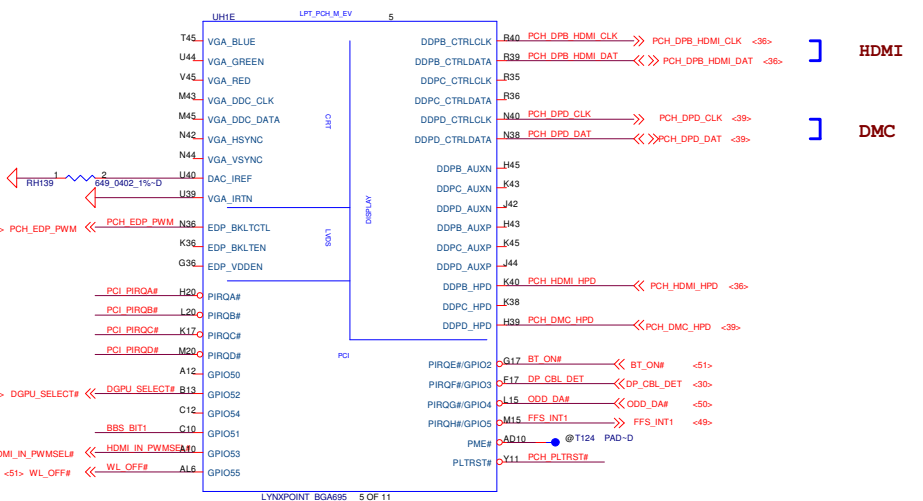
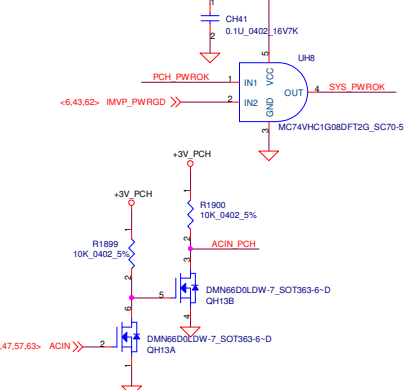
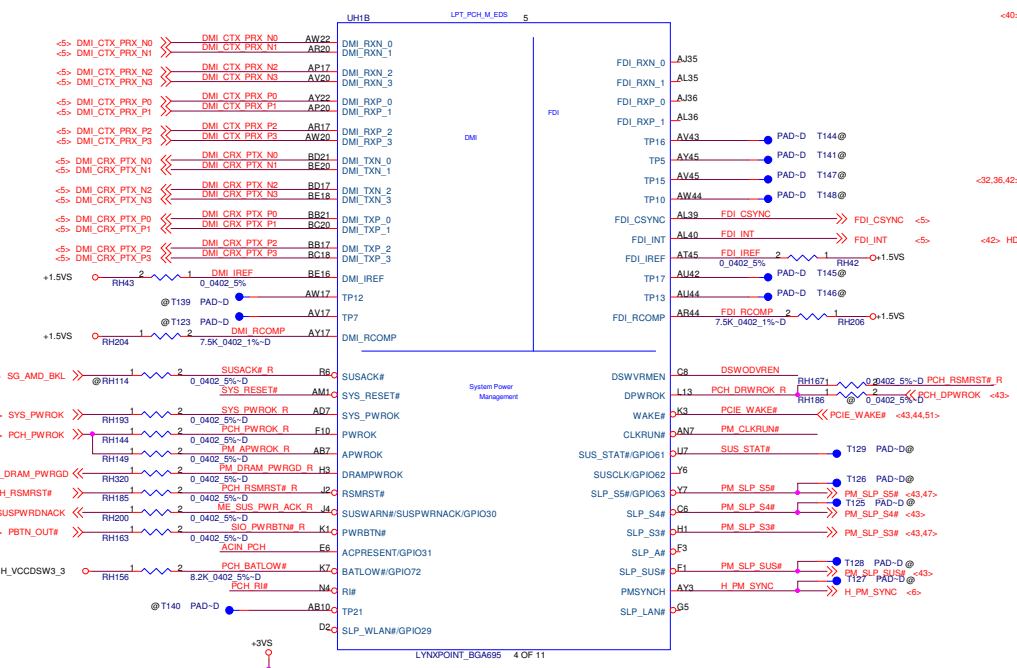
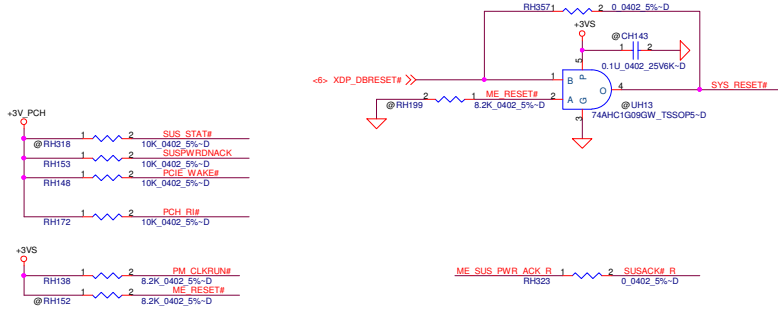


HDA_SYNC Isolation Circuit



RTC Battery





GNT1#/GPIO1 (BBS_BIT1)	SATA1GP/GPIO19 (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DSWVDREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

A16 SWAP OVERRIDE STRAP
STP_A16OVR LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT

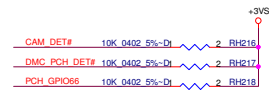
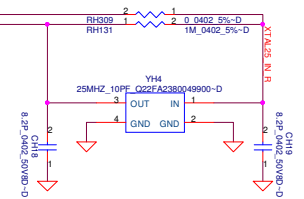
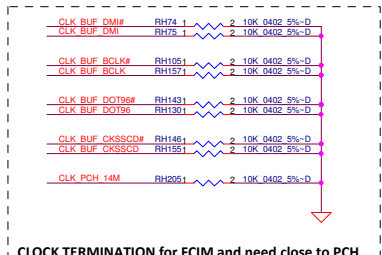
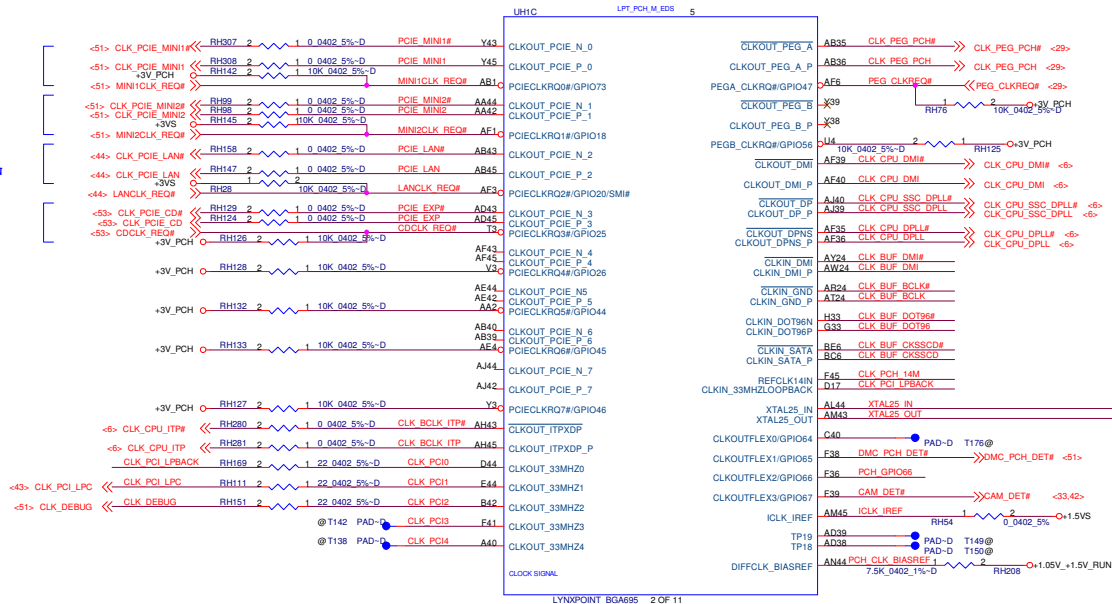
GPIO15 has internal pull up.

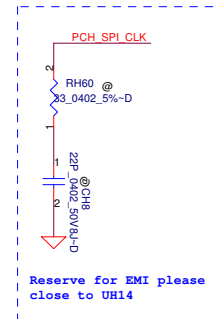
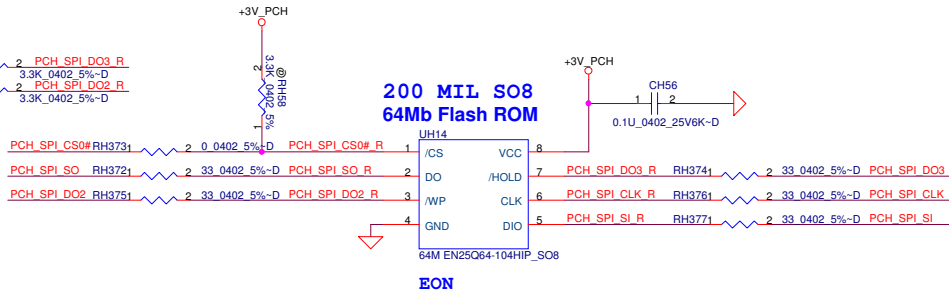
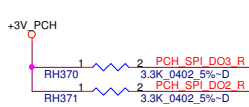
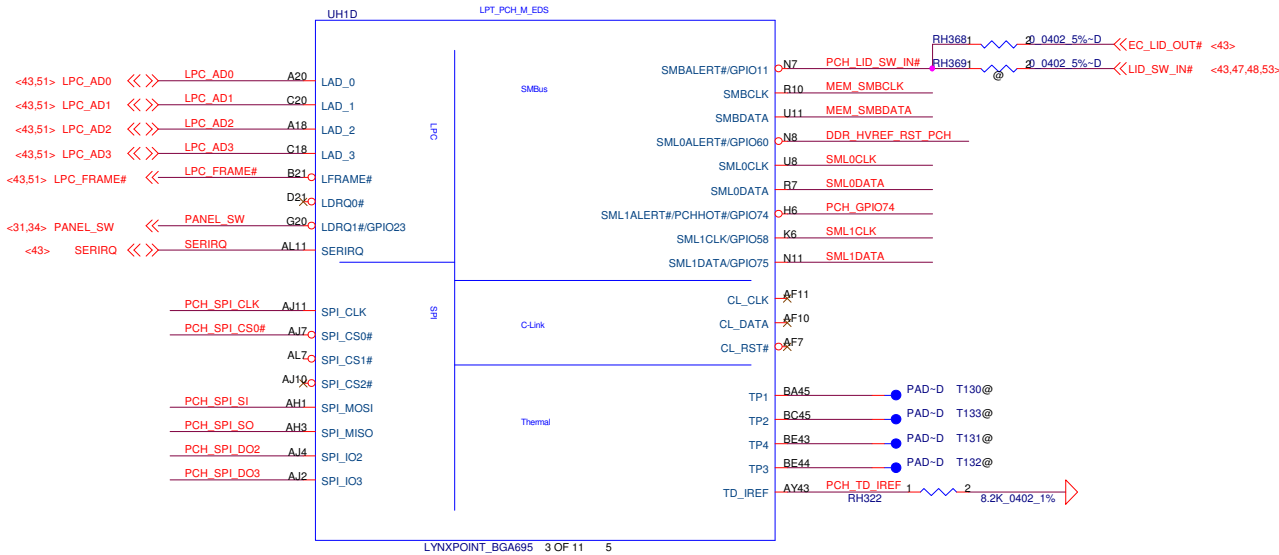
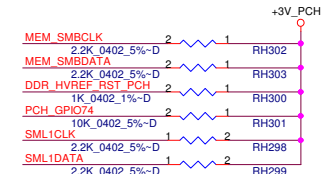
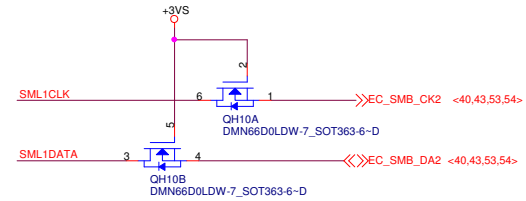
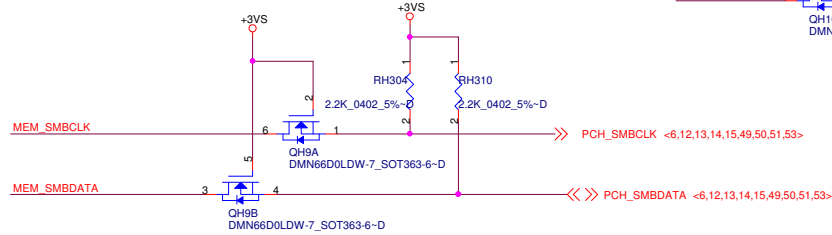
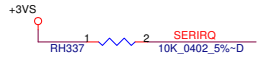
MiniWLAN (Mini Card 1)

DMC (Mini Card 2)

10/100/1G LAN

Card Reader

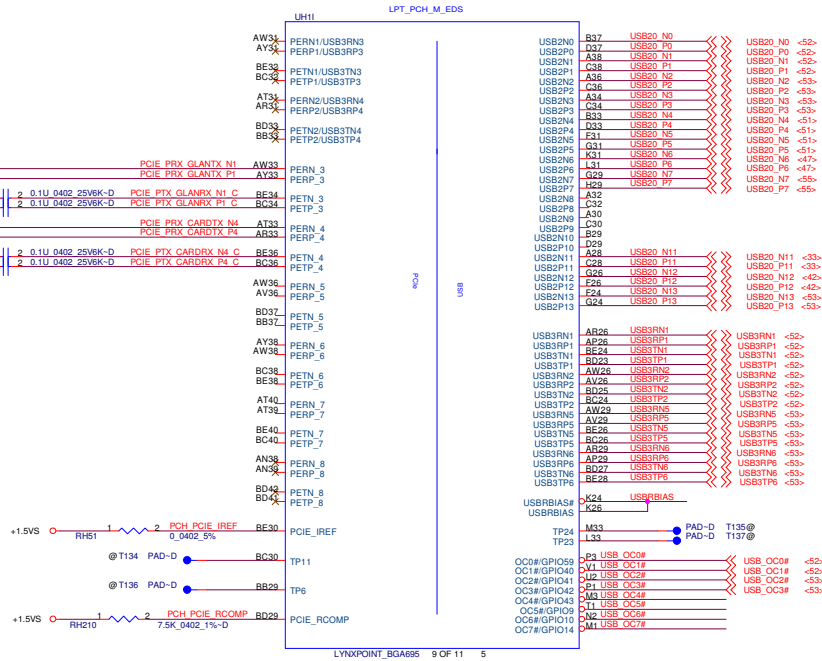




Security Classification	Compal Secret Data			Title PCH (4/9) SPI, SMBUS, LPC
Issued Date	2012/06/22	Deciphered Date	2013/06/21	
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10/100/1G LAN

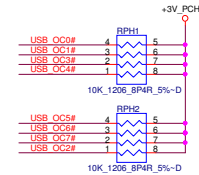
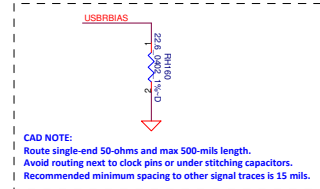
CARD READER



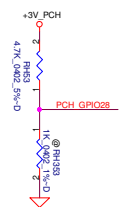
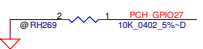
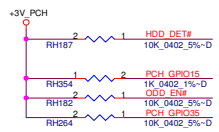
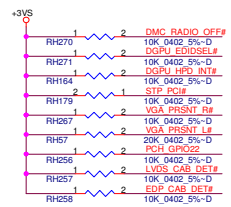
- JUSB1
- JUSB2
- JUSB3
- JUSB4
- Mini Card(WLAN)
- Mini Card(DMC)
- ELC LED
- IR sensor

- eDP Camera
- LVDS Camera
- VPK K/B

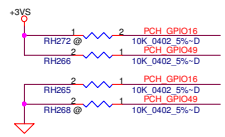
- P1: JUSB1
- P2: JUSB2
- P5: JUSB3
- P6: JUSB4



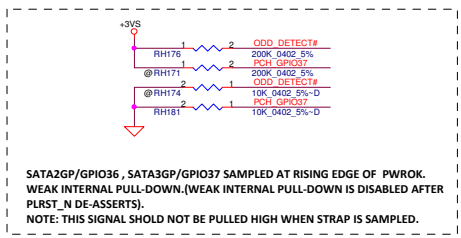
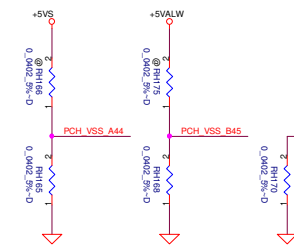
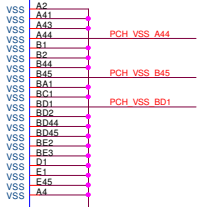
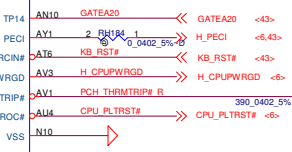
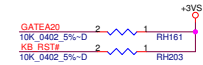
Security Classification	Compal Secret Data		Title PCH (5/9) PCIE,USB
Issued Date	2012/06/22	Deciphered Date	
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			Sheet 21 of 61 Rev 0.1



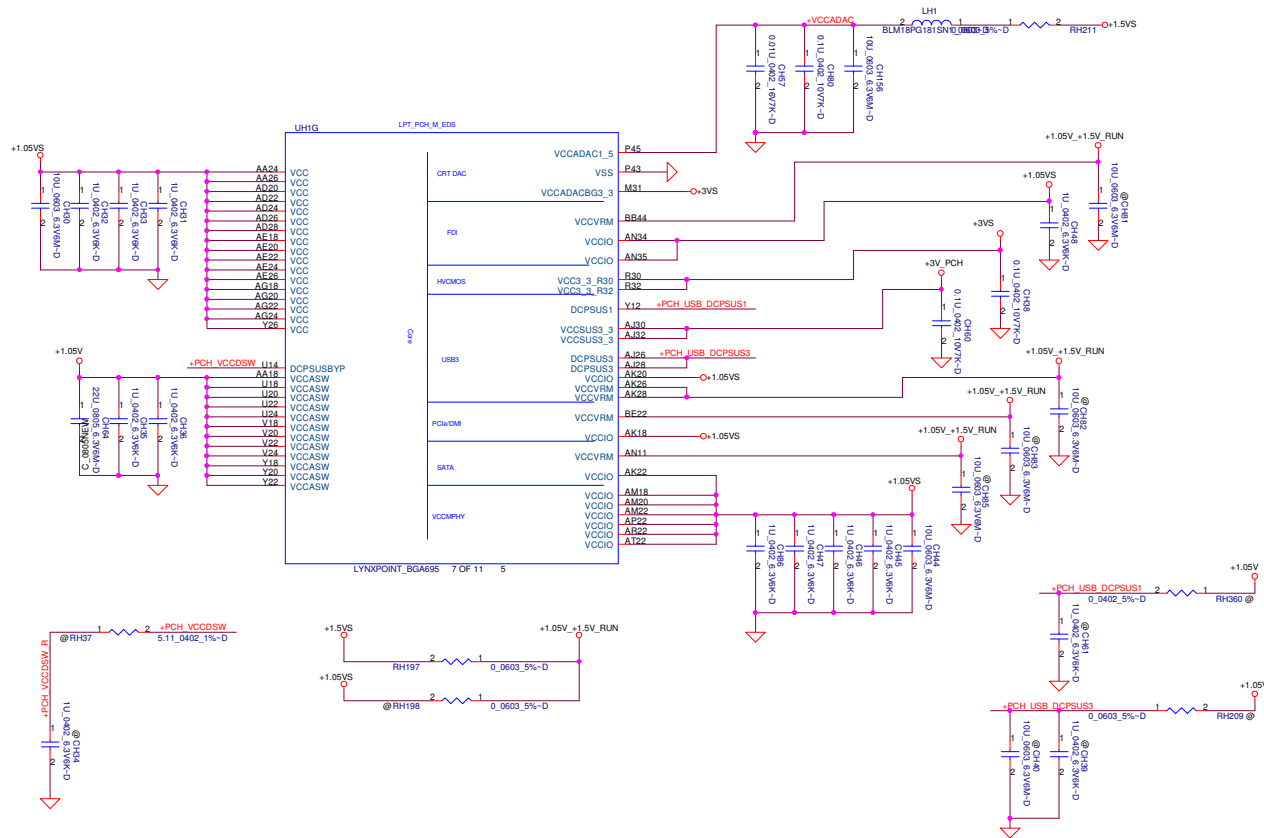
PLL ON DIE VR ENABLE
 ENABLED - HIGH(DEFAULT)
 DISABLED - LOW



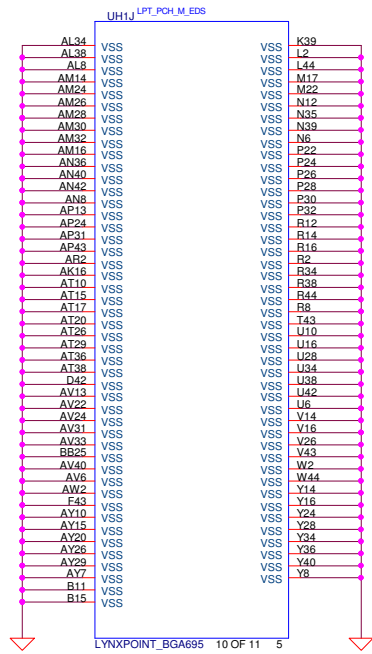
Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
* USB X6,PCIEX8,SATAX4	01



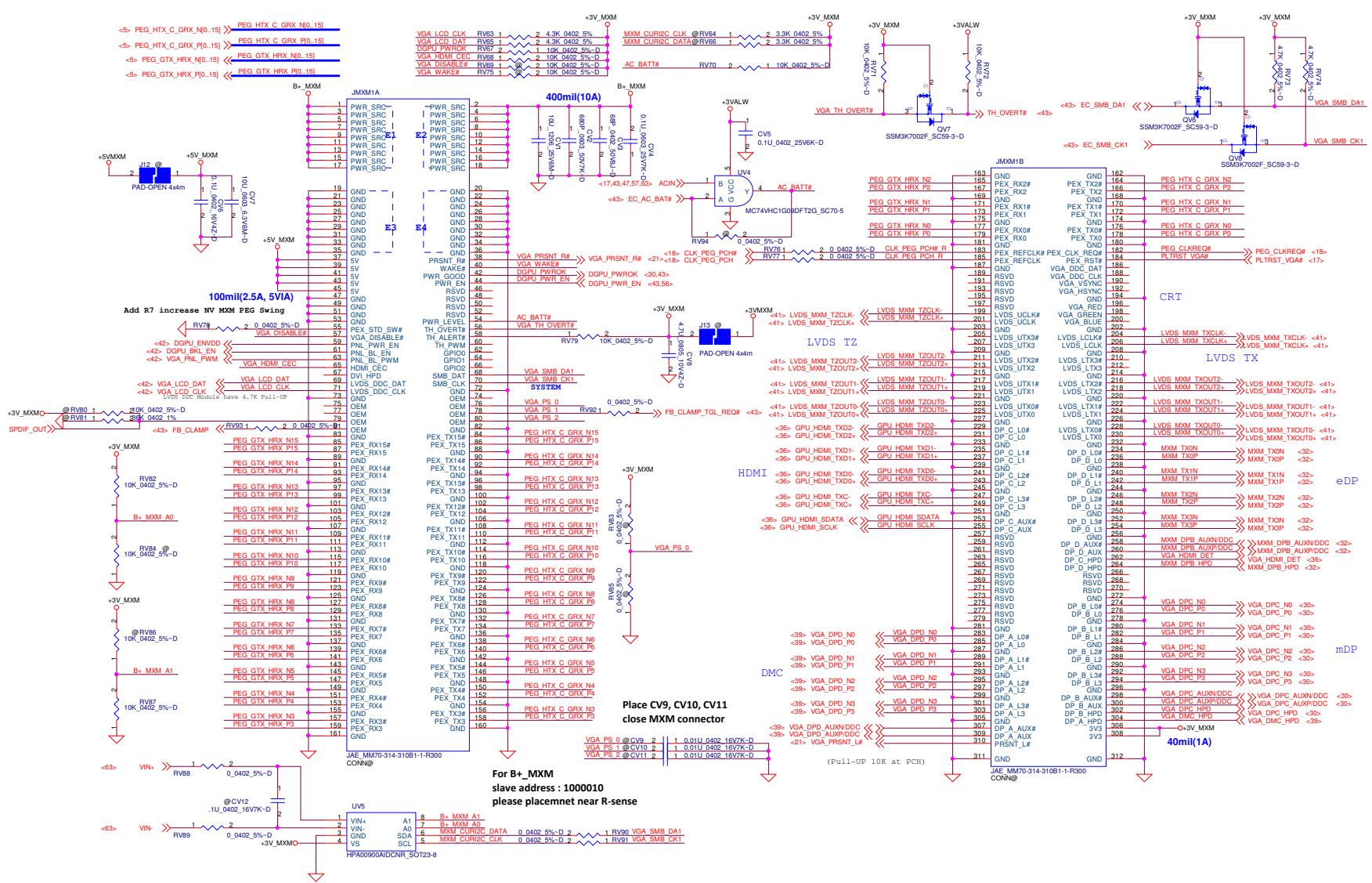
Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals				
USB3_1	USB3_2	USB3_5	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3			
				(00)	(00)							(10)	(10)							
				USB3_3	USB3_4							PCIE_1	PCIE_2							
				(01)	(01)							(01)	(01)							



PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



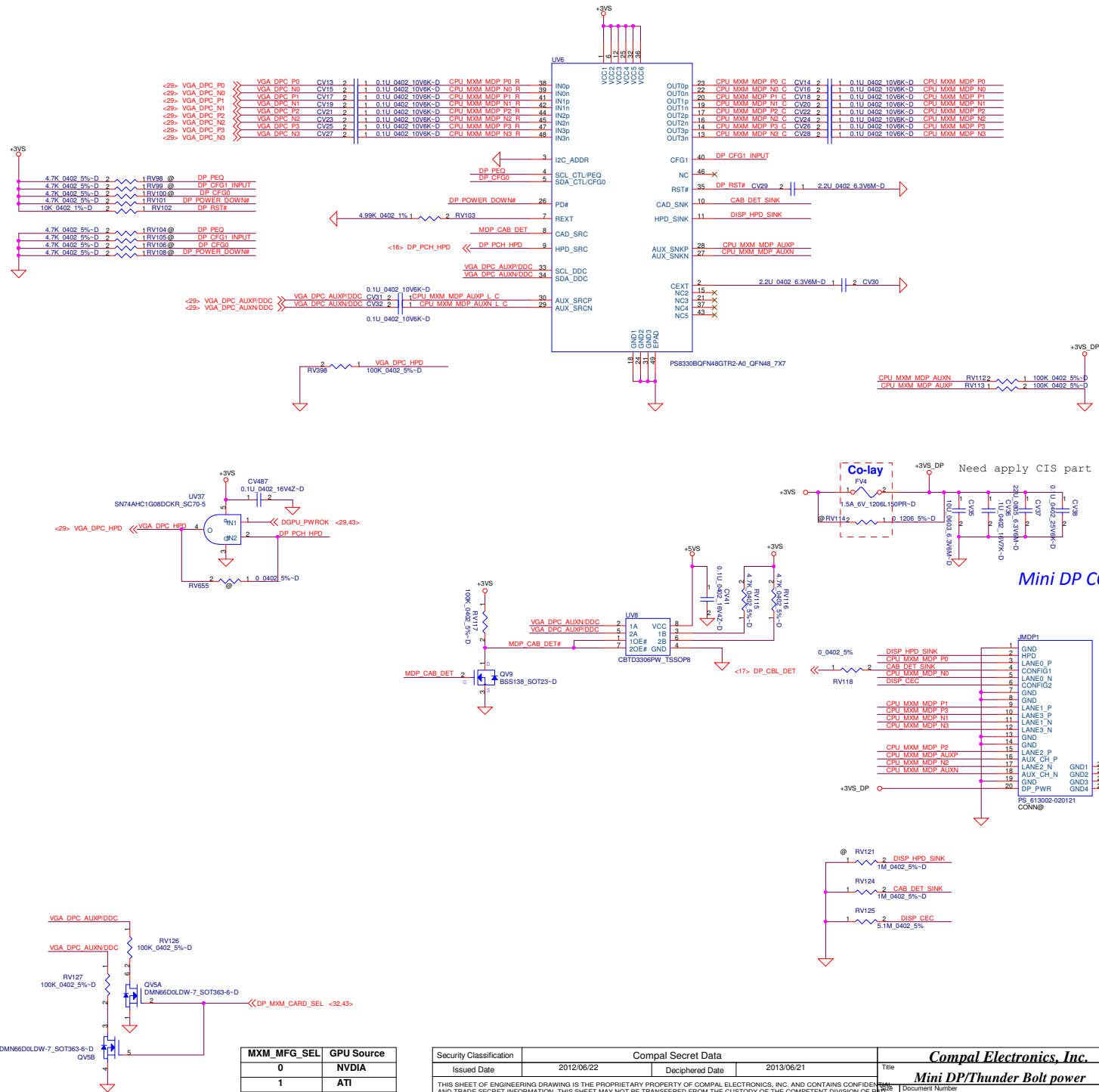
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title	PCH (9/9) Power
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				LA-9331P	0.1
				Date: Friday, June 22, 2012	Sheet 25 of 61



Security Classification	Compal Secret Data		Title
Issued Date	2012/06/22	Deciphered Date	2013/06/21
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Compal Electronics, Inc.	
MXMIII Connector	
Rev	0.1

DP Redriver



MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI

Security Classification	Compal Secret Data
Issued Date	2012/06/22
Deciphered Date	2013/06/21

Compal Electronics, Inc.	
Title: Mini DP/Thunder Bolt power	
Document Number:	LA-931P
Date:	Friday, June 22, 2012
Sheet:	27 of 61

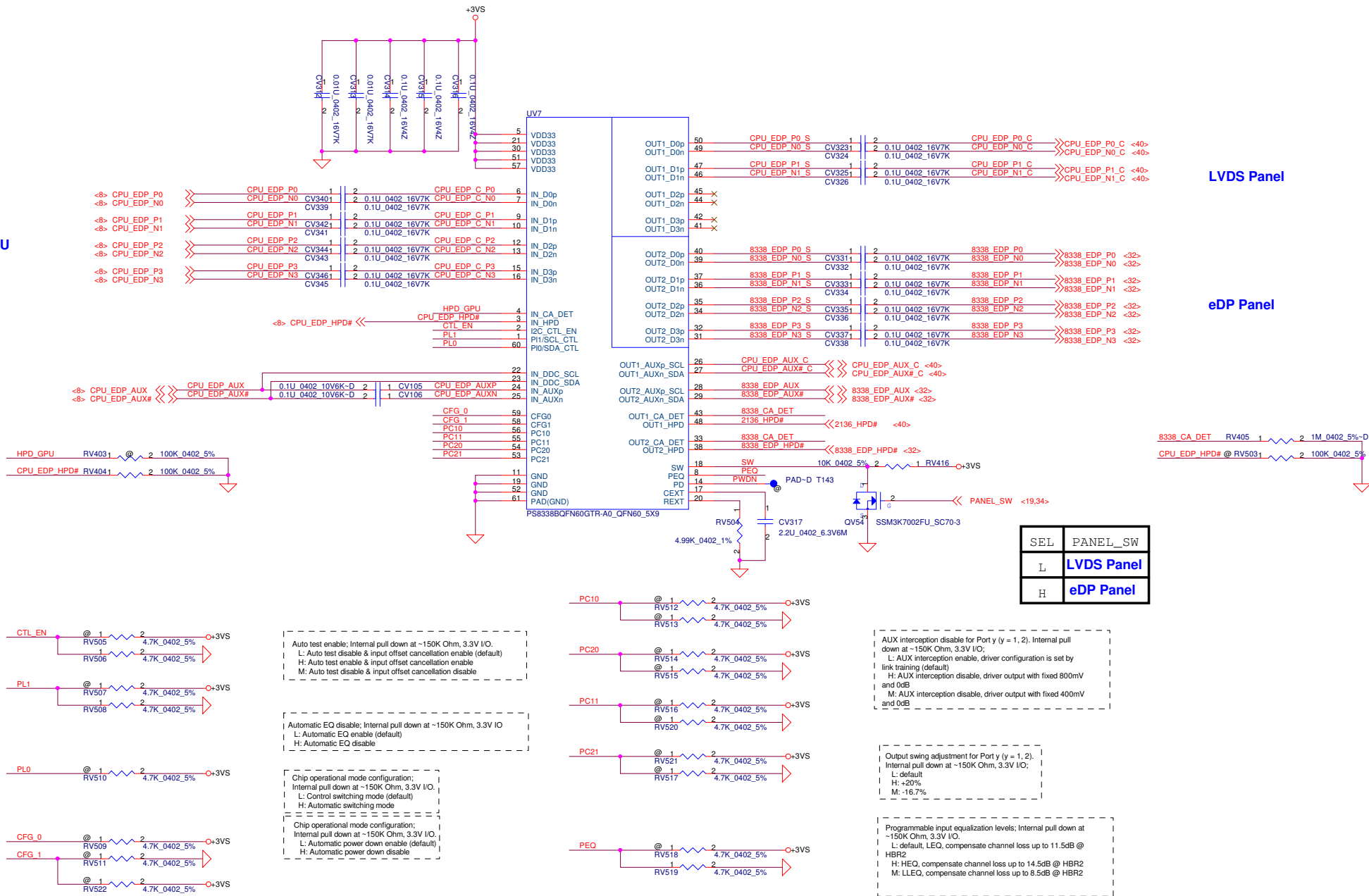
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CPU to EDP & LVDS MUX

CPU

LVDS Panel

eDP Panel



Auto test enable; Internal pull down at ~150K Ohm, 3.3V I/O.
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

Automatic EQ disable; Internal pull down at ~150K Ohm, 3.3V I/O
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

Chip operational mode configuration;
 Internal pull down at ~150K Ohm, 3.3V I/O.
 L: Control switching mode (default)
 H: Automatic switching mode

Chip operational mode configuration;
 Internal pull down at ~150K Ohm, 3.3V I/O.
 L: Automatic power down enable (default)
 H: Automatic power down disable

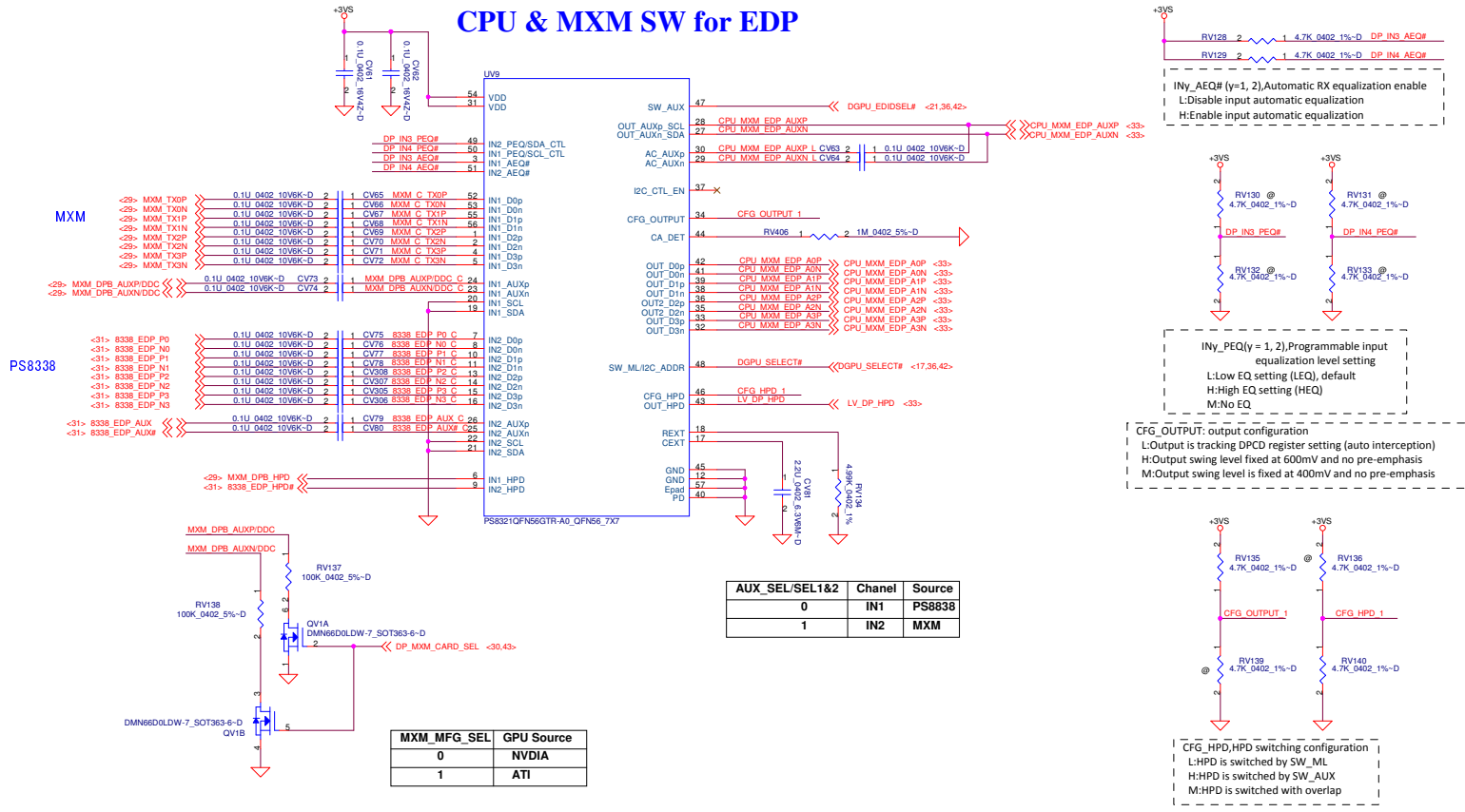
AUX interception disable for Port y (y = 1, 2). Internal pull down at ~150K Ohm, 3.3V I/O;
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

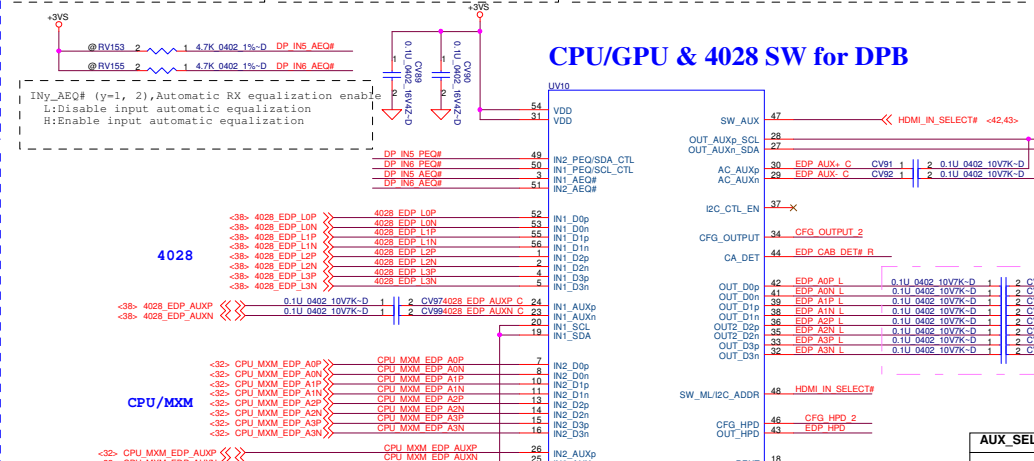
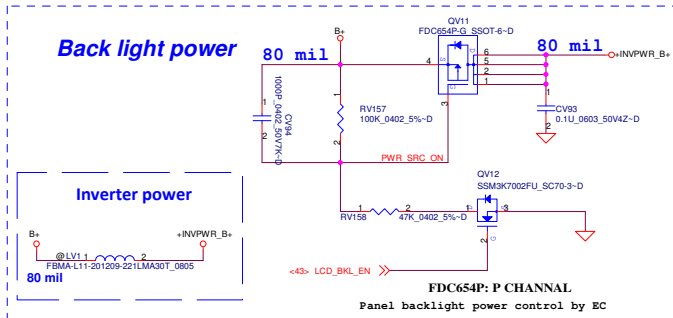
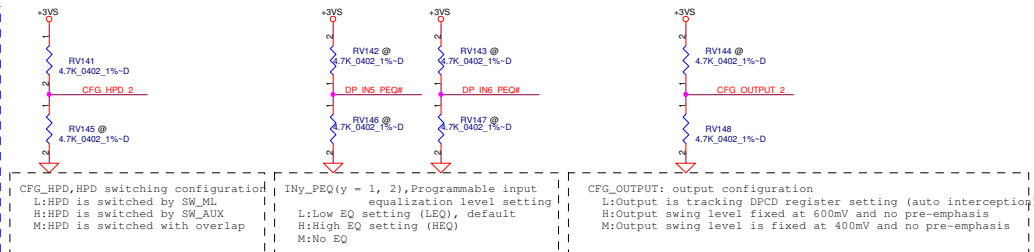
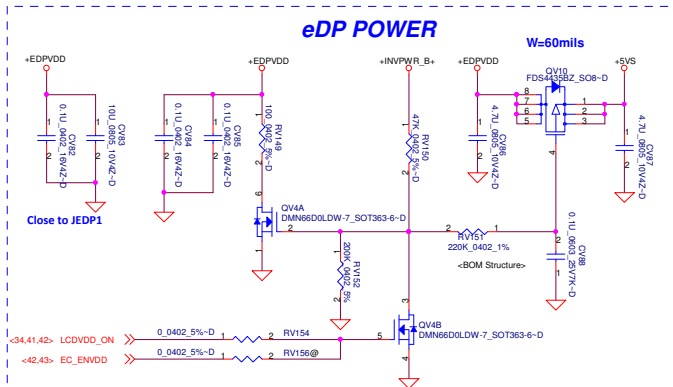
Output swing adjustment for Port y (y = 1, 2).
 Internal pull down at ~150K Ohm, 3.3V I/O;
 L: default
 H: +20%
 M: -16.7%

Programmable input equalization levels; Internal pull down at ~150K Ohm, 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

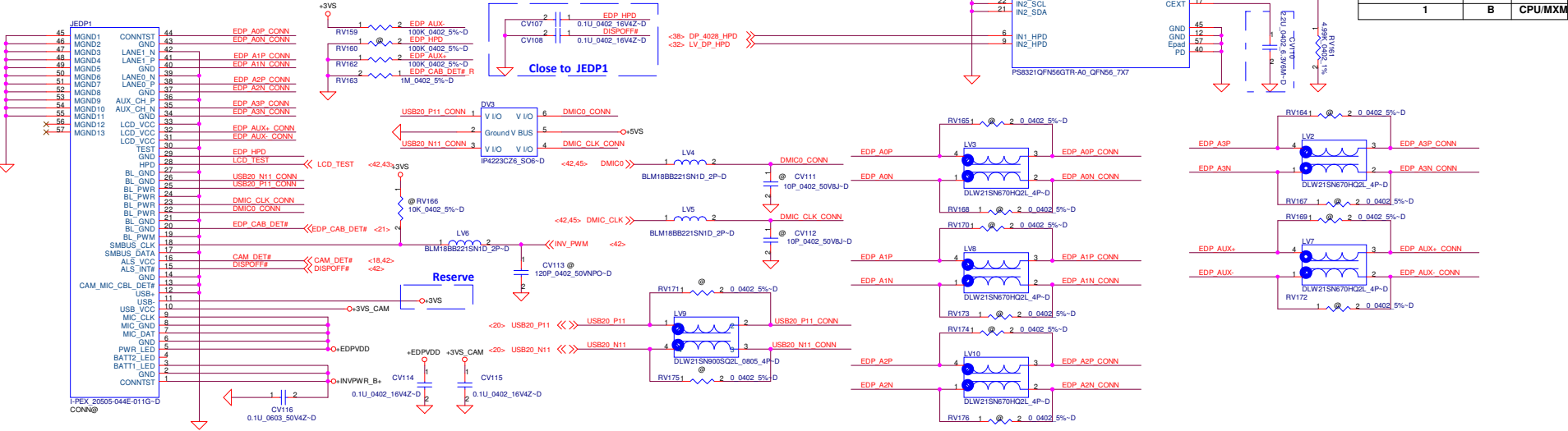
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Issued Date	2012/06/22	Deciphered Date	2013/06/21
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			Rev 0.1
			Sheet 28 of 61

CPU & MXM SW for EDP

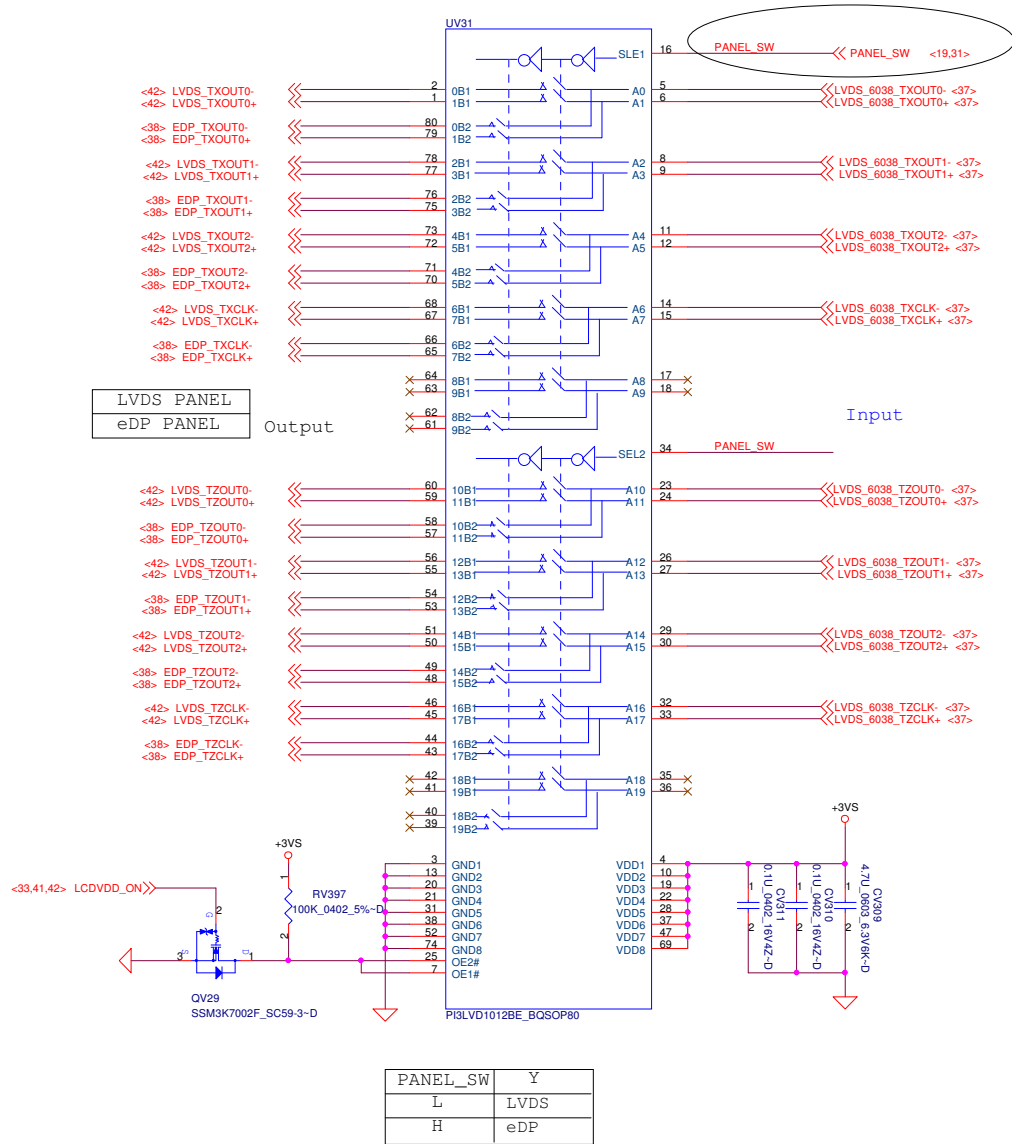




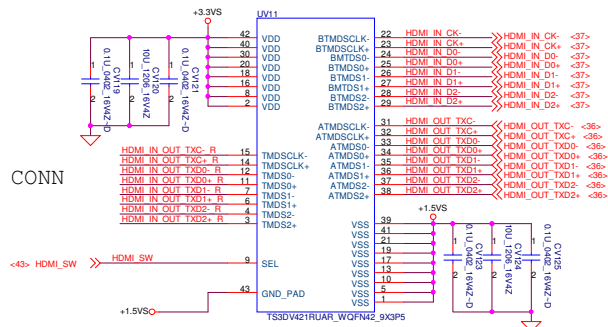
AUX_SEL/SEL1&2	Chanel	Source
0	A	4028
1	B	CPU/MXM



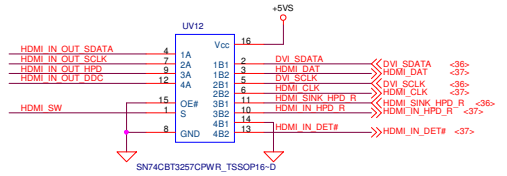
STDP6038 to EDP & LVDS MUX



HDMI CONN



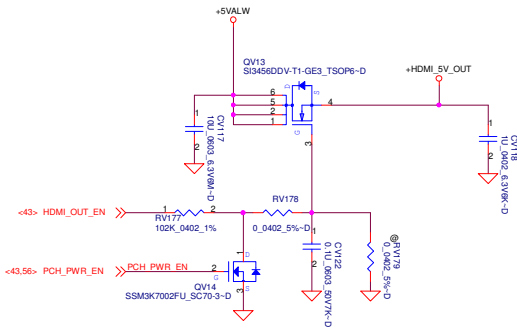
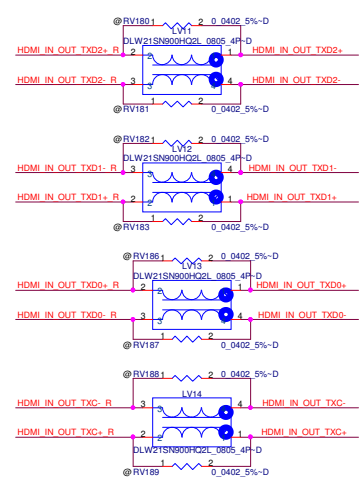
SEL	OUTPUT
L	A
H	B



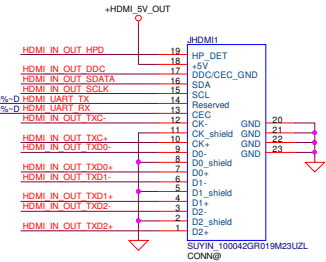
SEL	OUTPUT
L	B1
H	B2

STDP6038

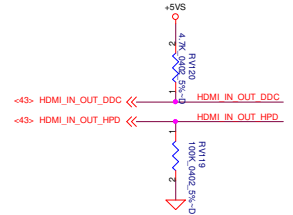
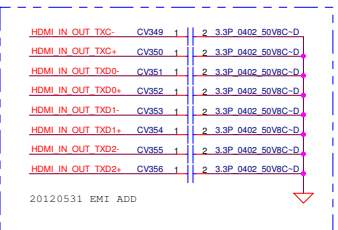
CPU/MXM

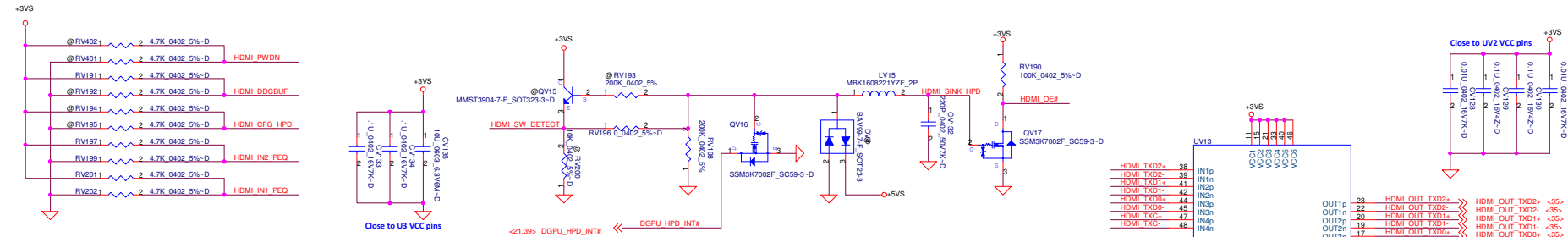


HDMI Input/Output Connector



Part Number	Description
800000028R	HDMI W/Logo:800000028R





PS8271
PEQ=L, Middle level receiving equalization selection
PEQ=H, High level receiving equalization selection
PEQ=M, Low level receiving equalization selection

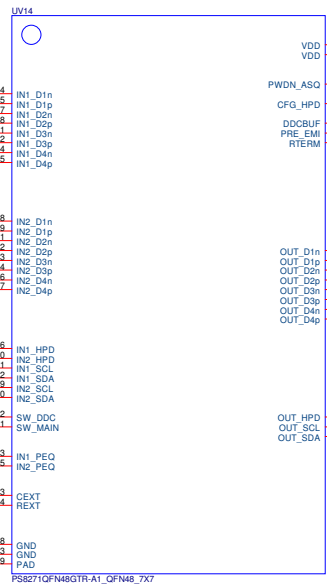
PS121
When DDCBUF_EN# is HIGH, the DDC channel is disabled,
SCL/SDA and SCLZ/SDAZ are disconnected

MXM

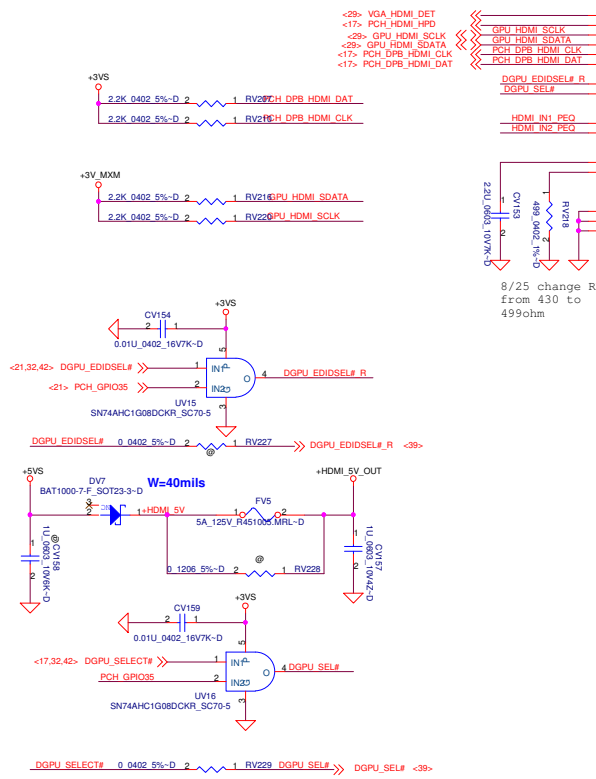
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<29> GPU_HDMI_TXD2+>	>>> GPU_HDMI_TXD2+>	CV1372	1	1U_0402_16V7K-D	GPU_HDMI_TXD2+>	C	45	IN1_D1p
<29> GPU_HDMI_TXD1<	>>> GPU_HDMI_TXD1<	CV1382	1	1U_0402_16V7K-D	GPU_HDMI_TXD1<	C	47	IN1_D2n
<29> GPU_HDMI_TXD1+>	>>> GPU_HDMI_TXD1+>	CV1382	1	1U_0402_16V7K-D	GPU_HDMI_TXD1+>	C	48	IN1_D2p
<29> GPU_HDMI_TXD0<	>>> GPU_HDMI_TXD0<	CV1465	1	1U_0402_16V7K-D	GPU_HDMI_TXD0<	C	2	IN1_D3n
<29> GPU_HDMI_TXD0+>	>>> GPU_HDMI_TXD0+>	CV1412	1	1U_0402_16V7K-D	GPU_HDMI_TXD0+>	C	2	IN1_D3p
<29> GPU_HDMI_TXC<	>>> GPU_HDMI_TXC<	CV1422	1	1U_0402_16V7K-D	GPU_HDMI_TXC<	C	4	IN1_D4n
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CPU

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<8> CPU_HDMI_N1<	>>> CPU_HDMI_N1<	CV147	1	2	1U_0402_16V7K-D	CPU_HDMI_N1<	C	11	IN2_D2n
<8> CPU_HDMI_P1<	>>> CPU_HDMI_P1<	CV148	1	2	1U_0402_16V7K-D	CPU_HDMI_P1<	C	12	IN2_D2p
<8> CPU_HDMI_N0<	>>> CPU_HDMI_N0<	CV149	1	2	1U_0402_16V7K-D	CPU_HDMI_N0<	C	13	IN2_D3n
<8> CPU_HDMI_P0<	>>> CPU_HDMI_P0<	CV150	1	2	1U_0402_16V7K-D	CPU_HDMI_P0<	C	14	IN2_D3p
<8> CPU_HDMI_N3<	>>> CPU_HDMI_N3<	CV151	1	2	1U_0402_16V7K-D	CPU_HDMI_N3<	C	16	IN2_D4n
<8> CPU_HDMI_P3<	>>> CPU_HDMI_P3<	CV152	1	2	1U_0402_16V7K-D	CPU_HDMI_P3<	C	17	IN2_D4p

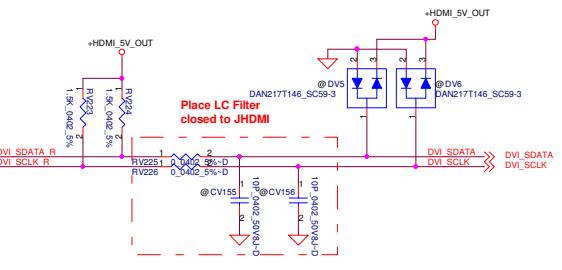
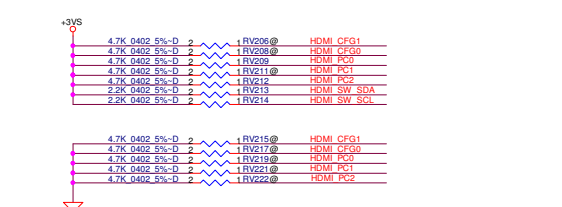


HDMI_SW_DET	0	1
Y	IN1	IN2
	MXM	PCH



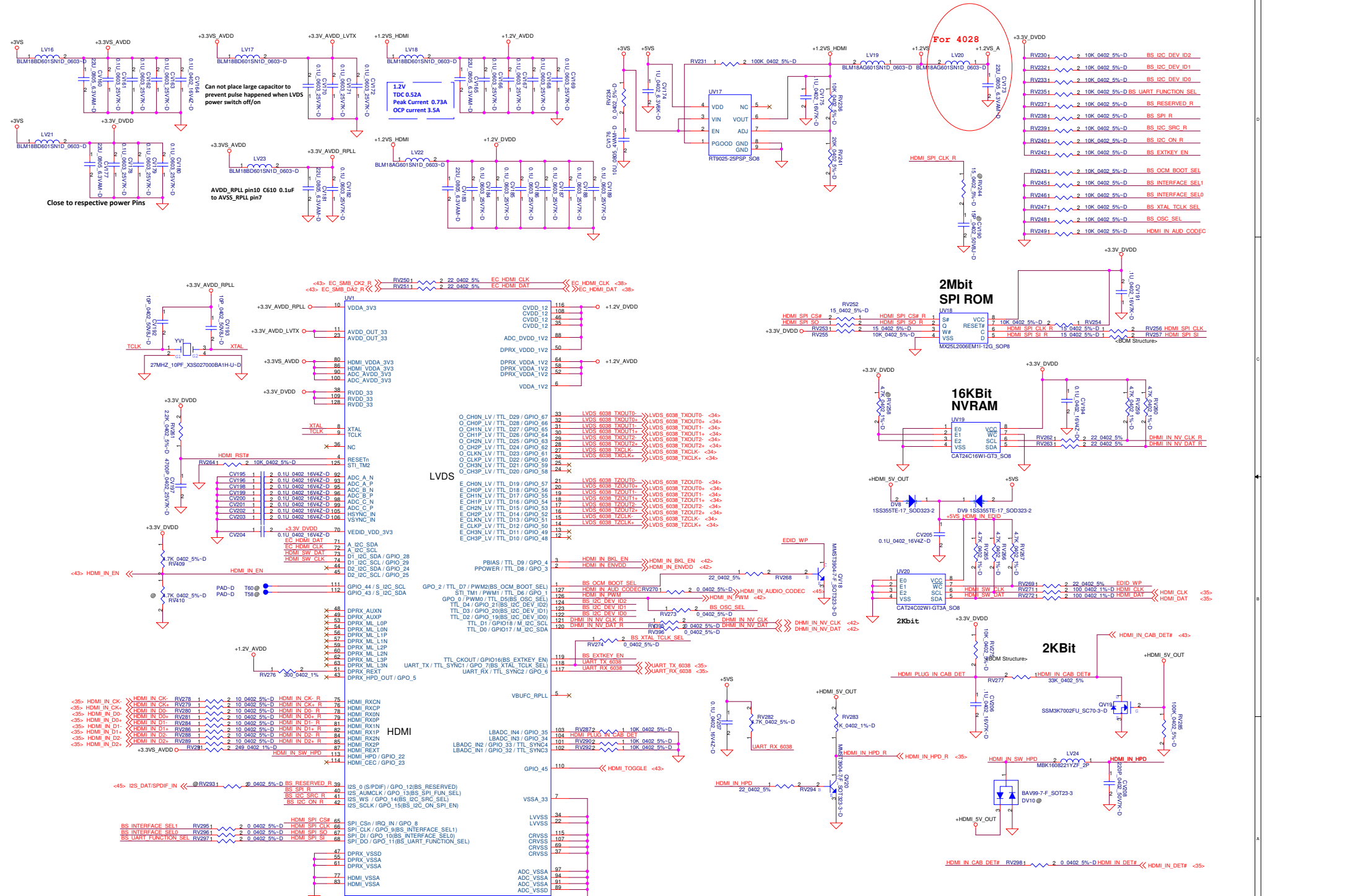
DGPU_SELECT#	0	1
Y	IN1	IN2
	MXM	PCH

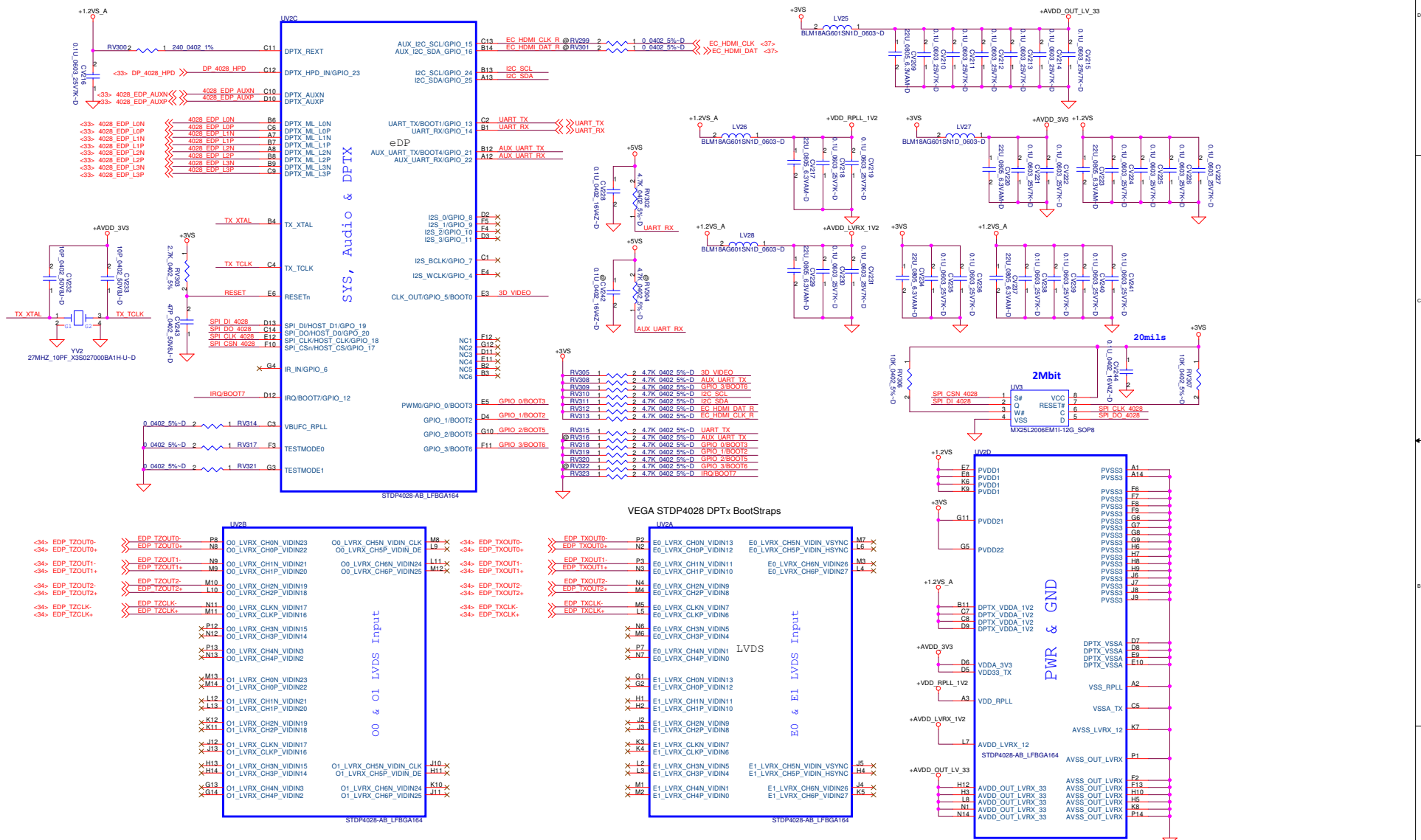
PS121 CFG0/CFG1
SCLZ/SDAZ output voltage select;
CFG1:0=00 LOW-level input voltage: <0.40V LOW-level output voltage: 0.60V
PS121 PC0/PC1/PC2
Inputs equalization control, default inputs equalization setting at 12 dB
000: 12 dB, 001: 16 dB, 010: 10 dB, 011: 7 dB
100: 1.5 dB, 101: 4 dB, 110: 9 dB, 111: 7 dB

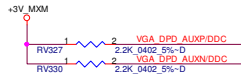


DVI_SELECT#	0	1
Y	IN1	IN2
	MXM	PCH

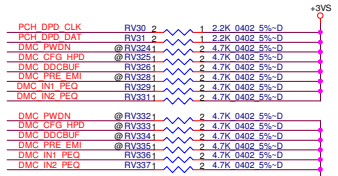
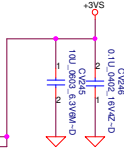
CONN





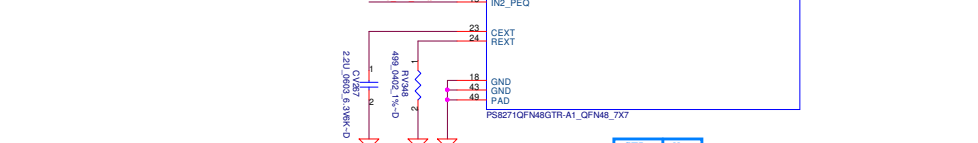
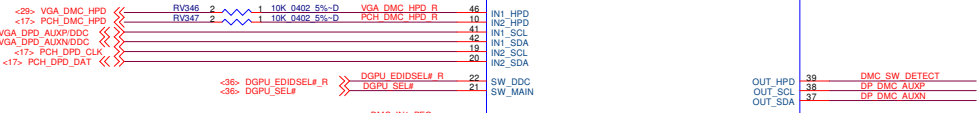
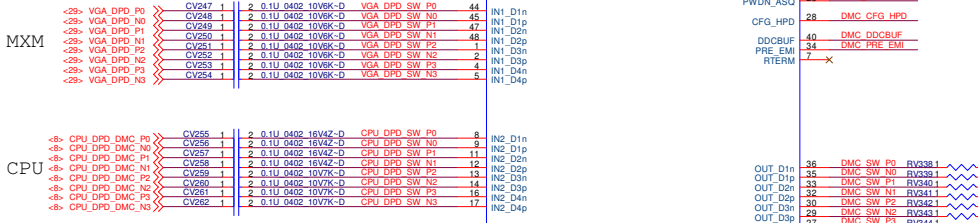


PCH/GPU AUX&LANE SW for DPB

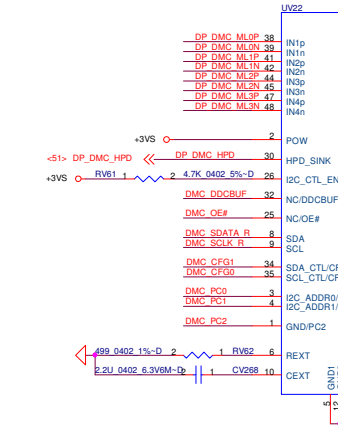
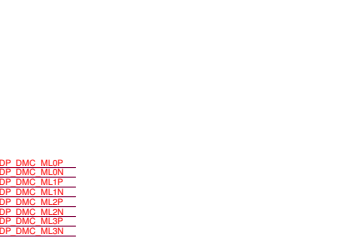
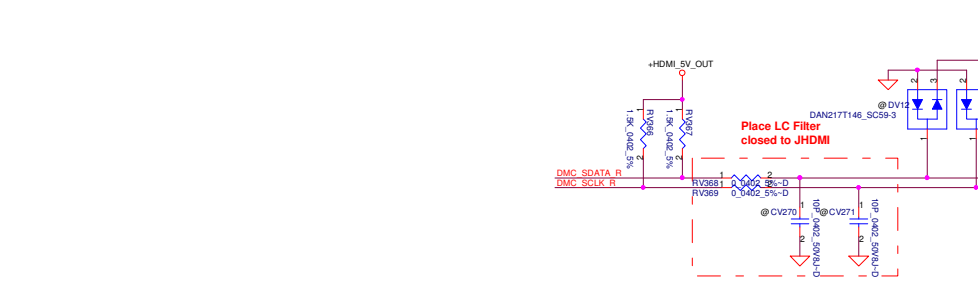
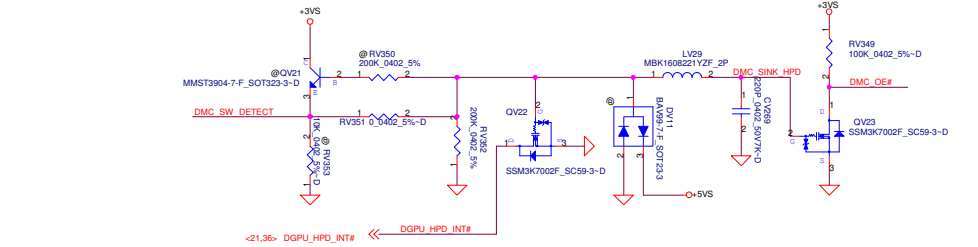


MXM

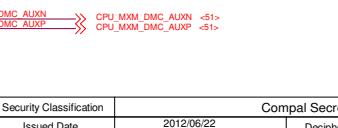
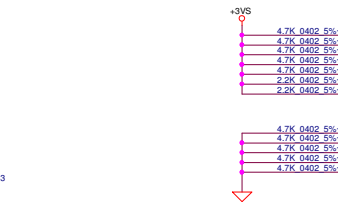
CPU



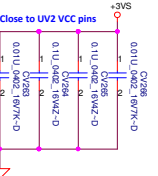
SEL	Y
0	IN1
1	IN2



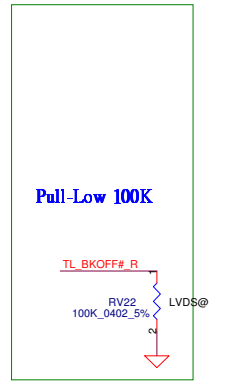
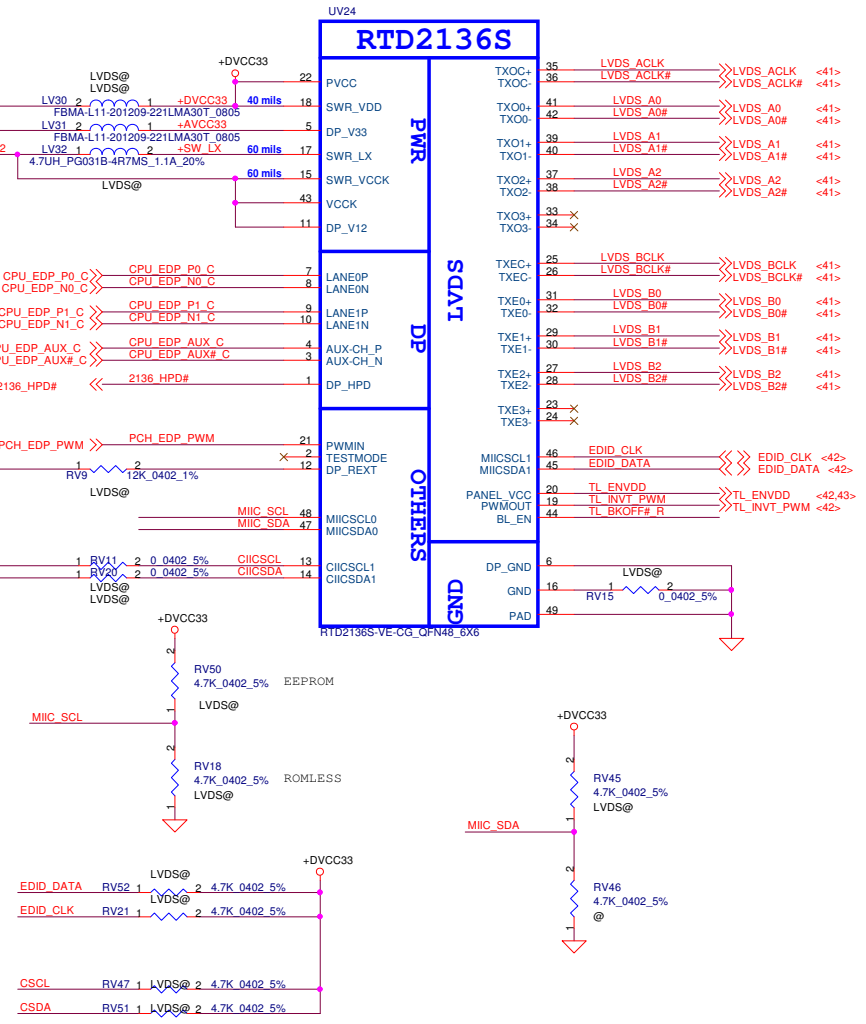
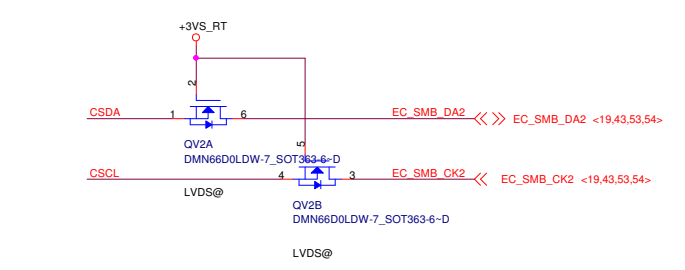
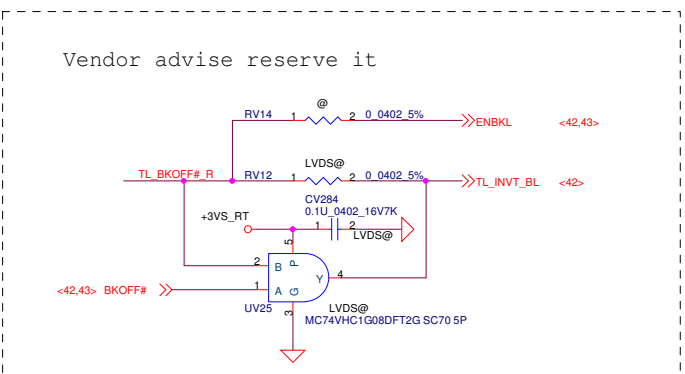
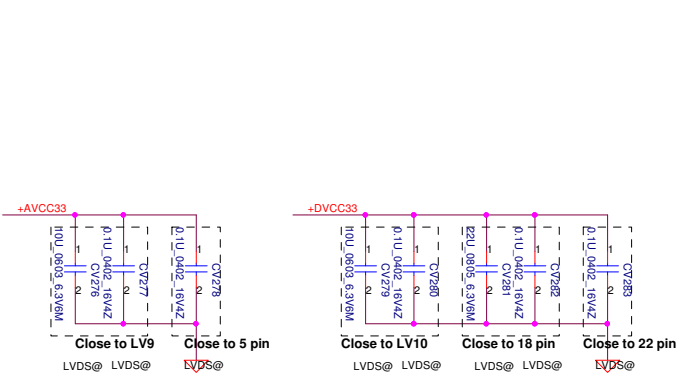
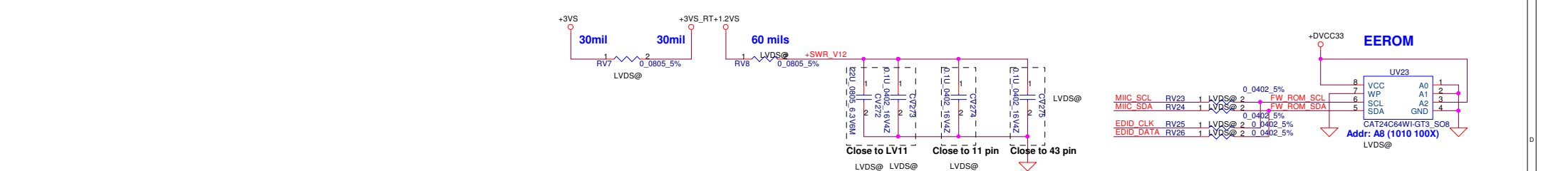
PS121 CFG0/CFG1
SCLZ/SDAZ output voltage select;
CFG1:0=00 LOW-level input voltage: <0.40V LOW-level output voltage: 0.60V
PS121 PC0/PC1/PC2
Inputs equalization control, default inputs equalization setting at 12 dB
000: 12 dB, 001: 16 dB, 010: 10 dB, 011: 7 dB
100: 1.5 dB, 101: 4 dB, 110: 9 dB, 111: 7 dB



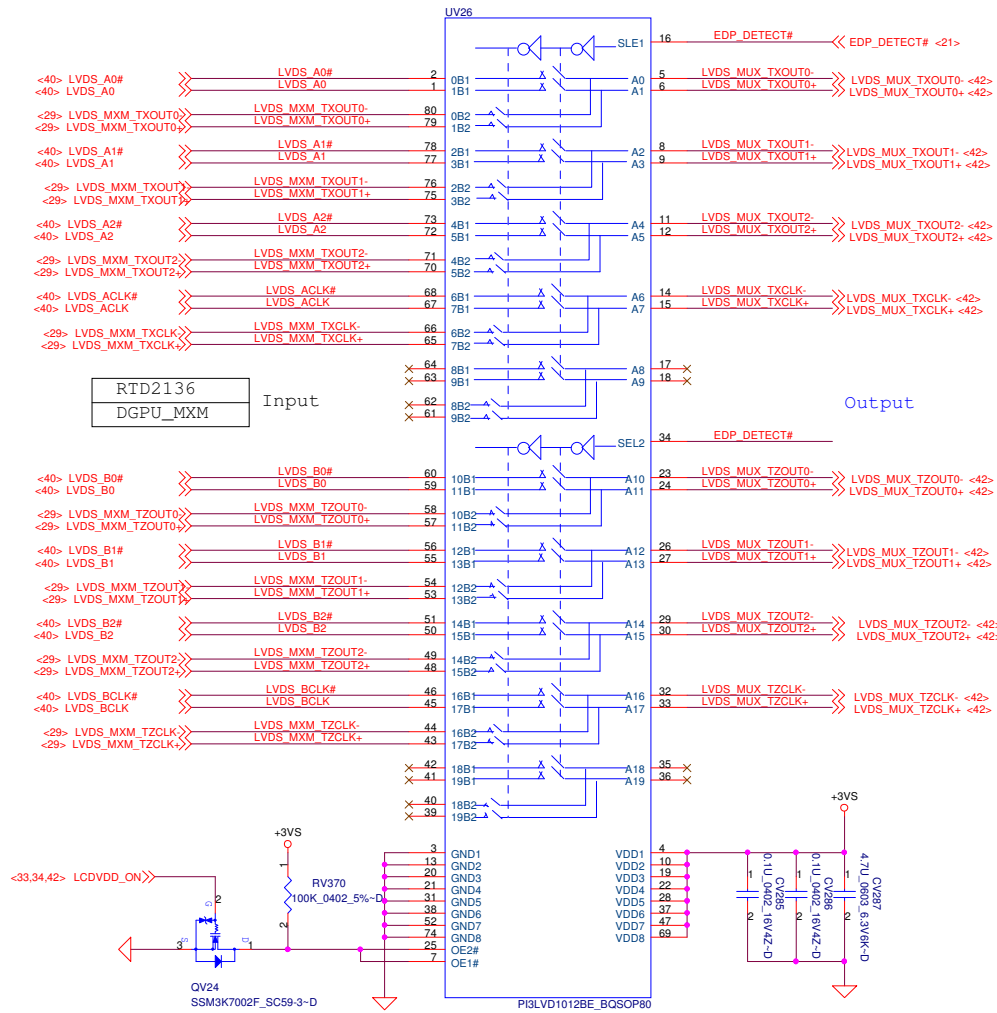
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STDP6038 SW STDP4028 PCH/GPU AUX for LVDS



RTD2136
DGPU_MXM

Input

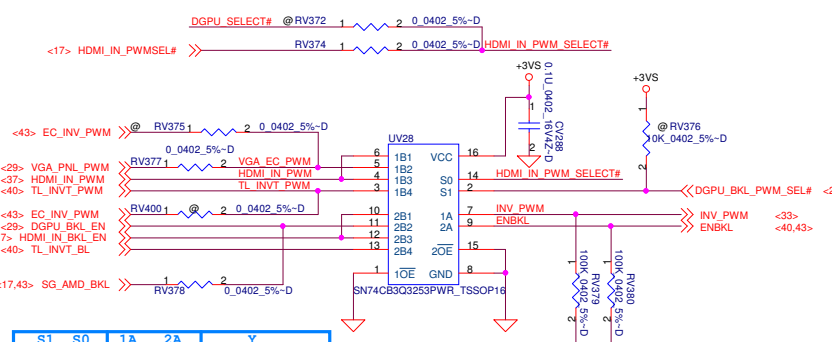
Output

SEL	Y
L	RTD2136
H	DGPU_MXM

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Issued Date	2012/06/22	Deciphered Date
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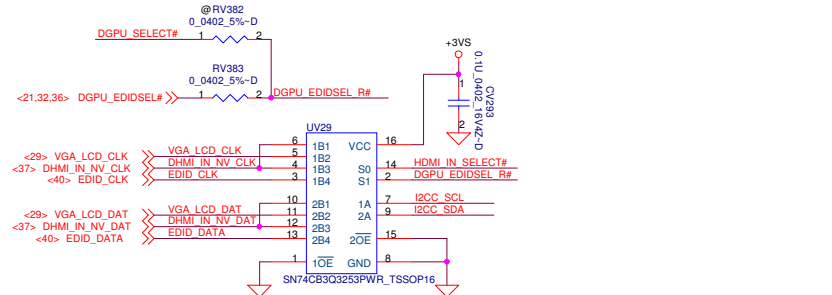
Compal Electronics, Inc.	
LVDS SW- 1 to 2 & GPU/PCH	
Document Number	Rev
LA-9331P	0.1
Date: Friday, June 22, 2012	Sheet 38 of 61

LCD Backlight Selector



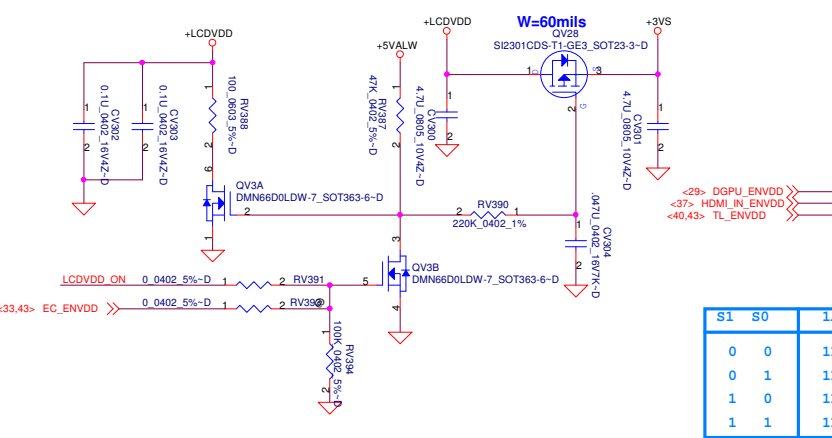
S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN (D)
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN (I)
1	1	1B4	2B4	UMA

LCD DDC Selector



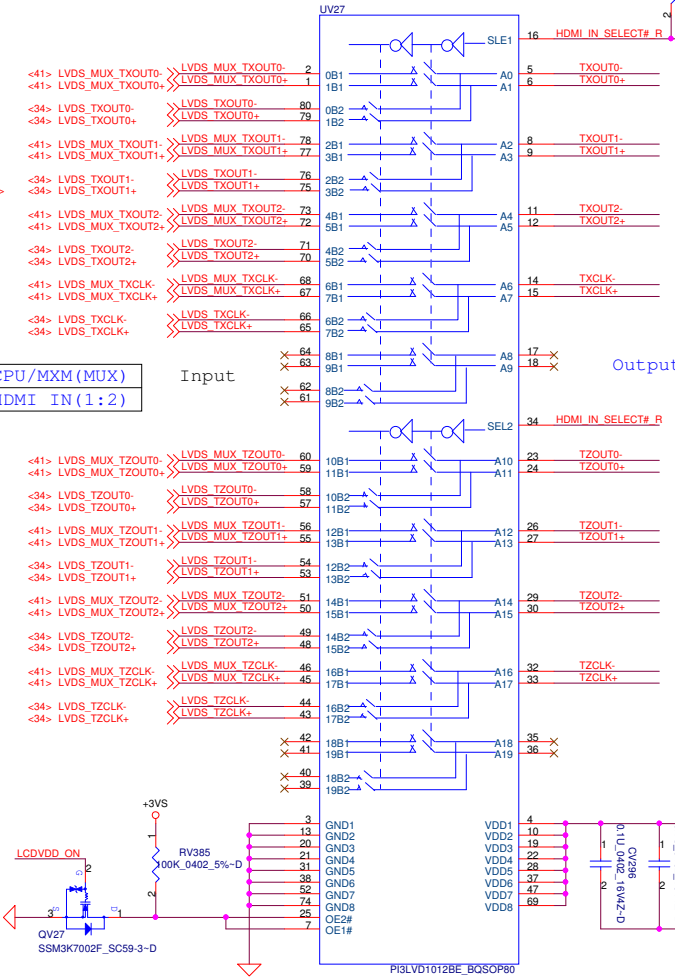
S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN (D)
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN (I)
1	1	1B4	2B4	UMA

LCD POWER



S1	S0	1A	2A	Y
0	0	1B1	2B1	HDMI IN
0	1	1B2	2B2	DSC
1	0	1B3	2B3	HDMI IN
1	1	1B4	2B4	UMA

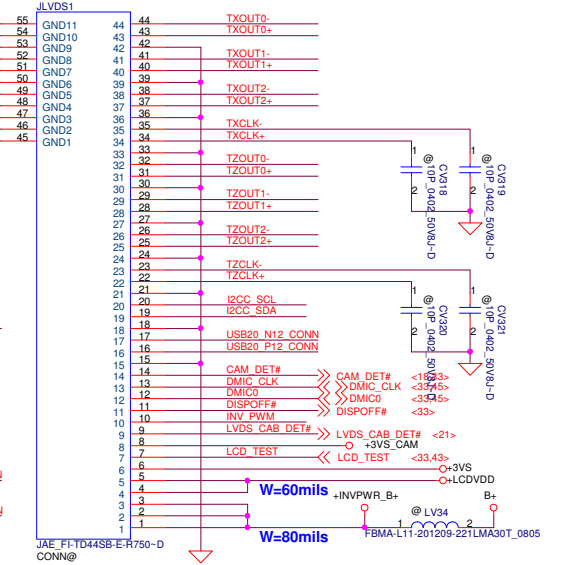
PCH/GPU MUX & 6038 MUX SW for LVDS



Input	Output
CPU/MXM (MUX)	HDMI IN (1:2)

SEL	Y
L	B1
H	B2

LVDS Conn.



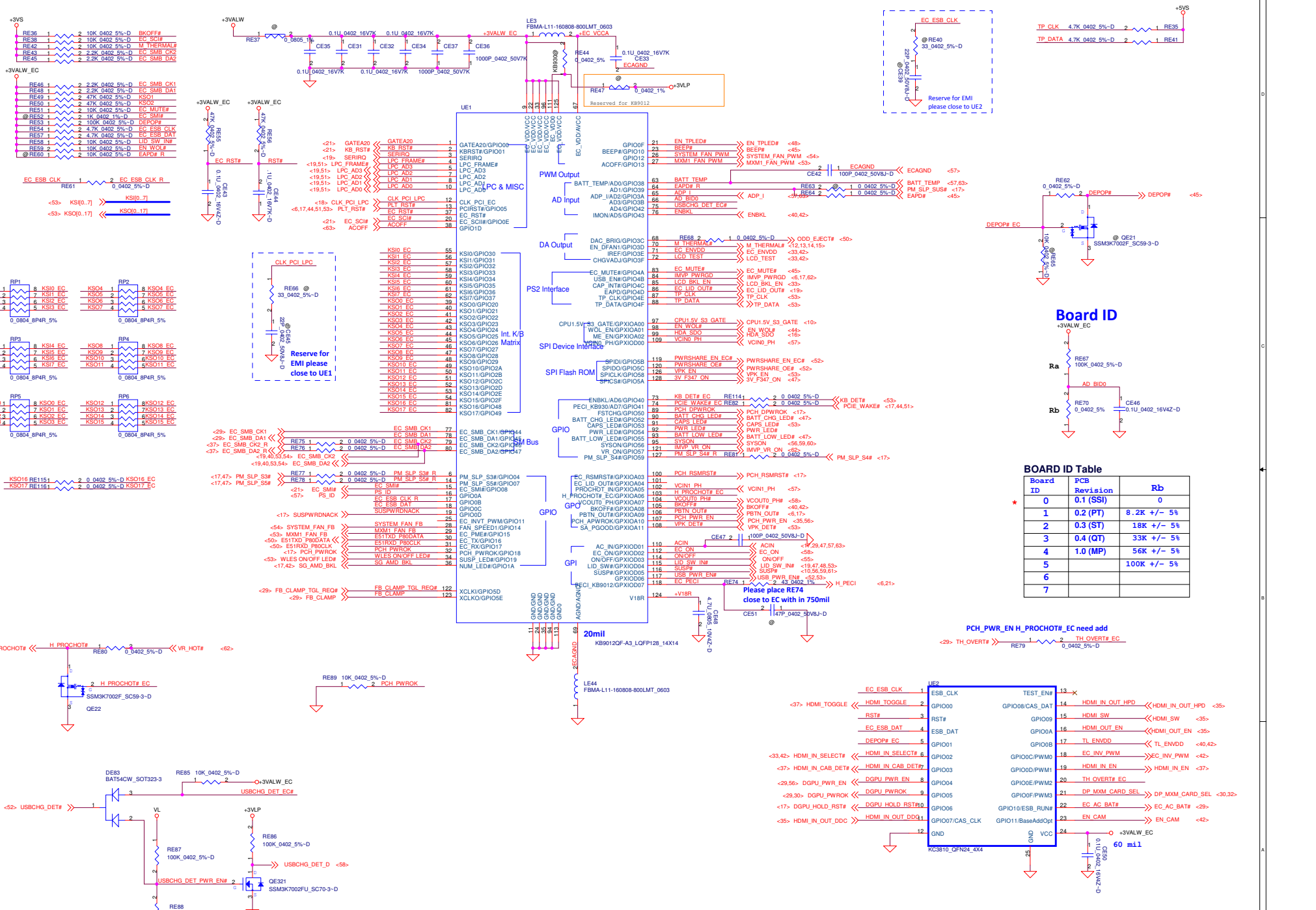
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

LVDS SW- 6038/SYSTEM & CONN

LA-9331P

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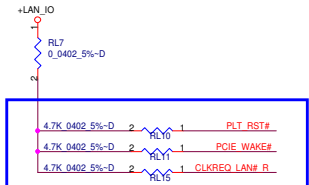


BOARD ID Table

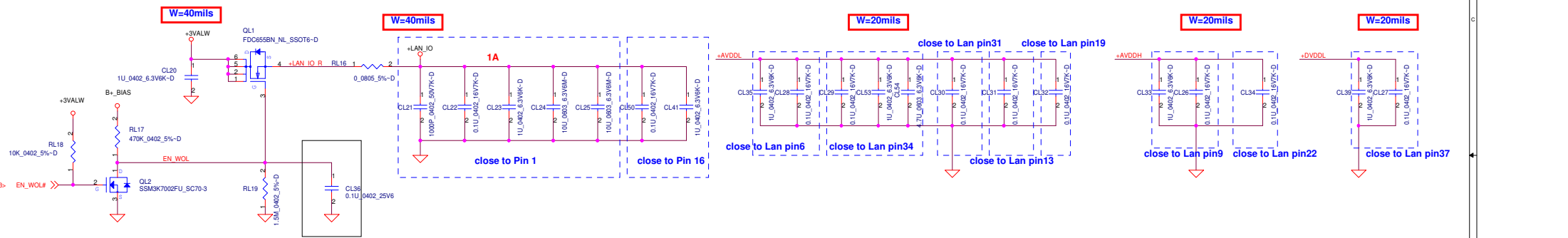
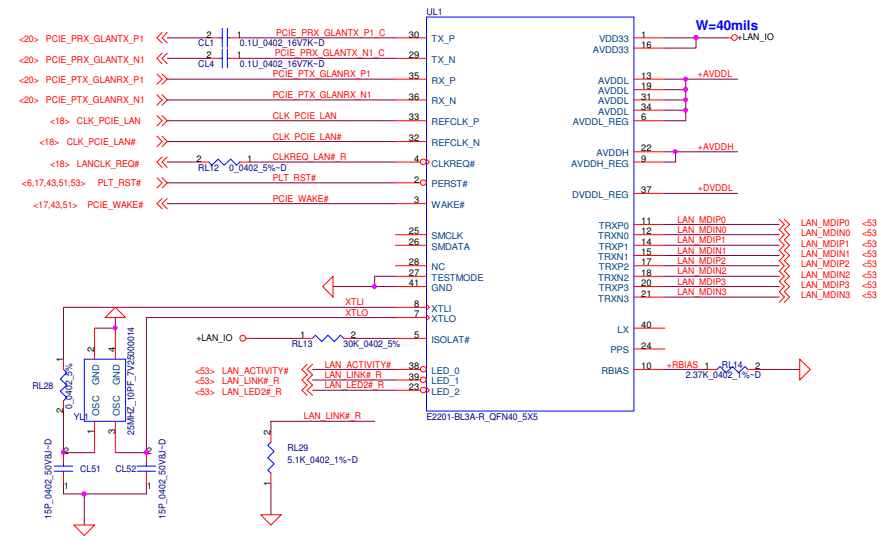
Board ID	PCB Revision	Rb
0	0.1 (SSI)	0
1	0.2 (PT)	8.2K +/- 5%
2	0.3 (ST)	18K +/- 5%
3	0.4 (QT)	33K +/- 5%
4	1.0 (MP)	56K +/- 5%
5		100K +/- 5%
6		
7		

PCB_PWR_EN_H_PROCHOT#_EC need add

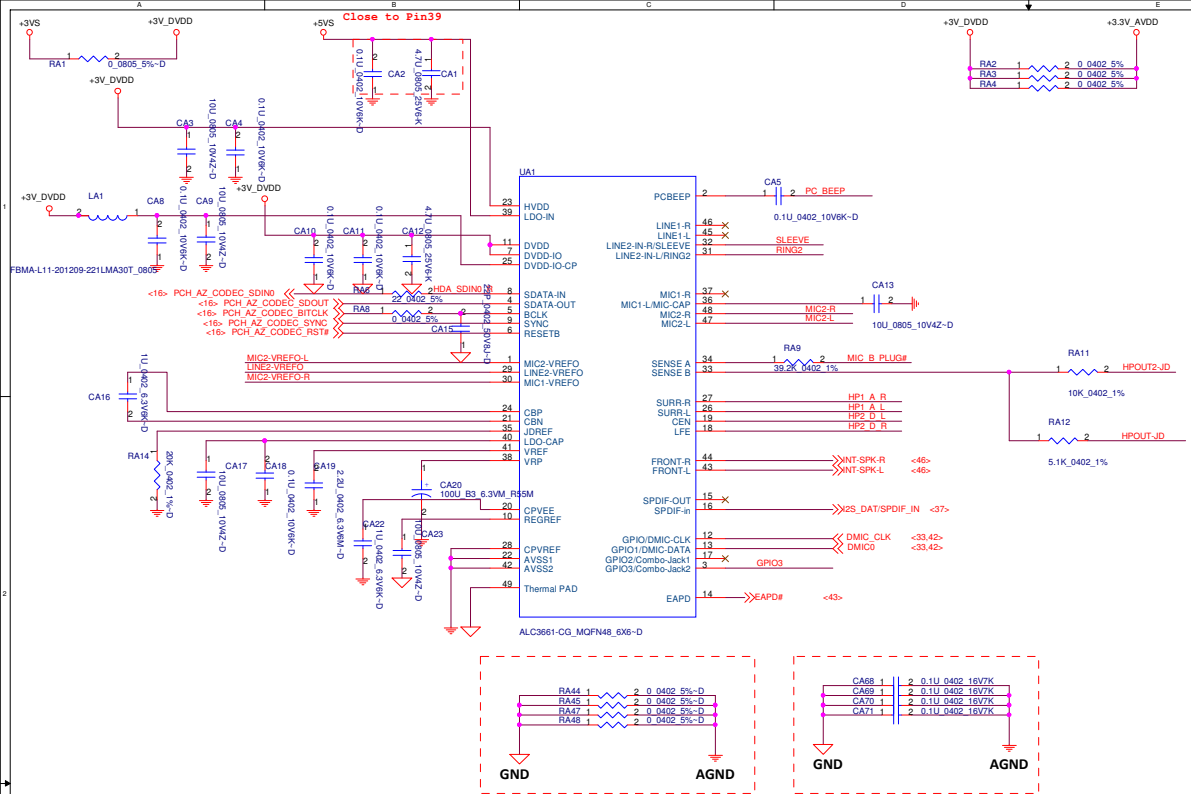
<29> TH_OVERT# EC RE79 1 2 TH_OVERT# EC 0.0402_5%-D



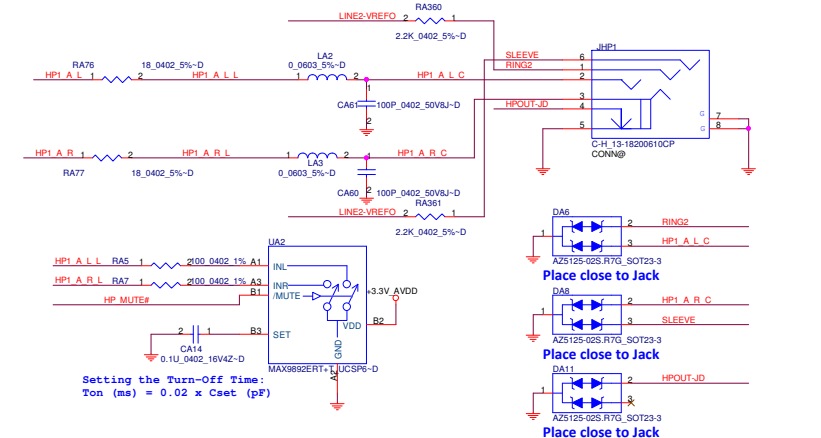
The pull-up resistors might not be necessary due to existence on PCH side.



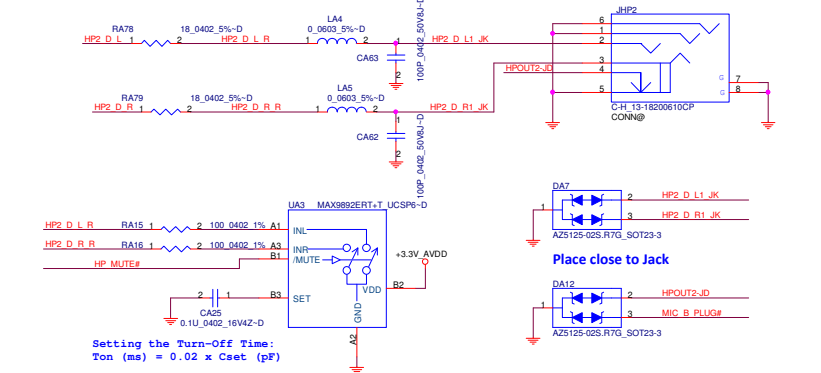
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title
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Size				Document Number
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Date: Friday, June 22, 2012				0.1
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			61	



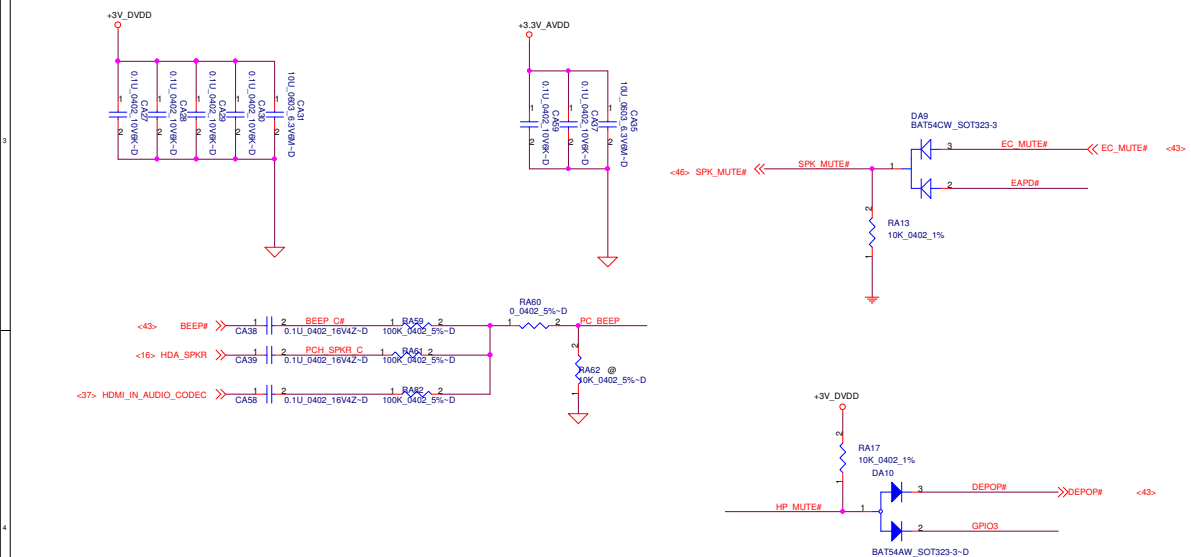
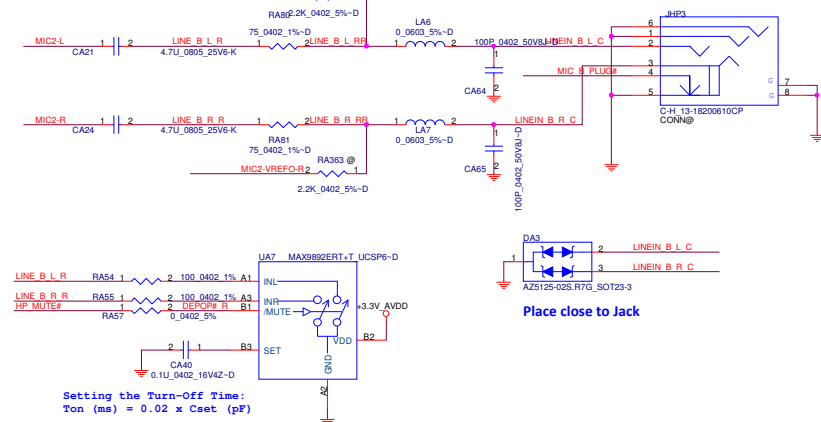
S1 (Out + In) : Front L/R + HP1 + MIC (auto-sense)



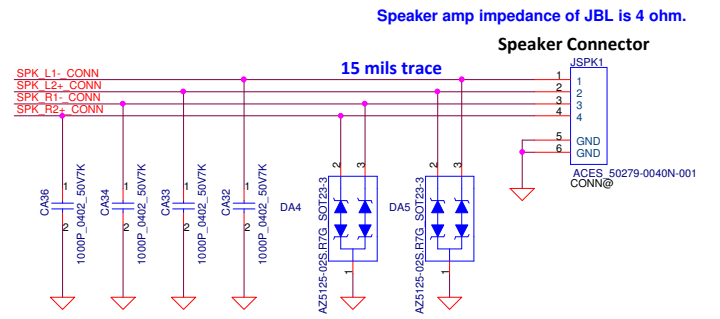
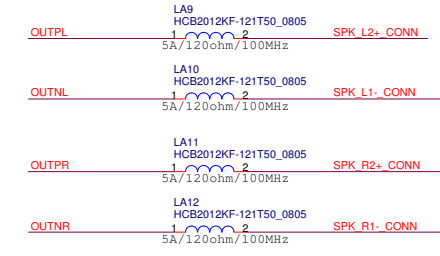
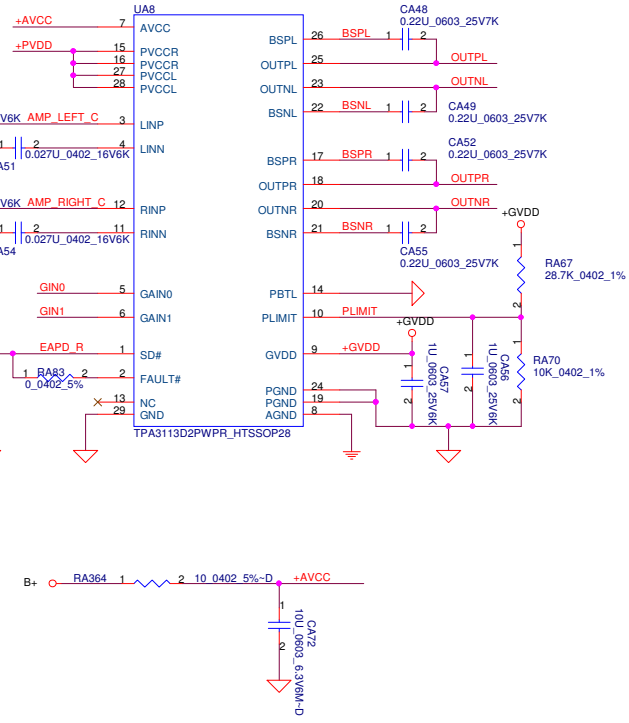
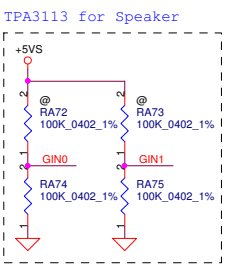
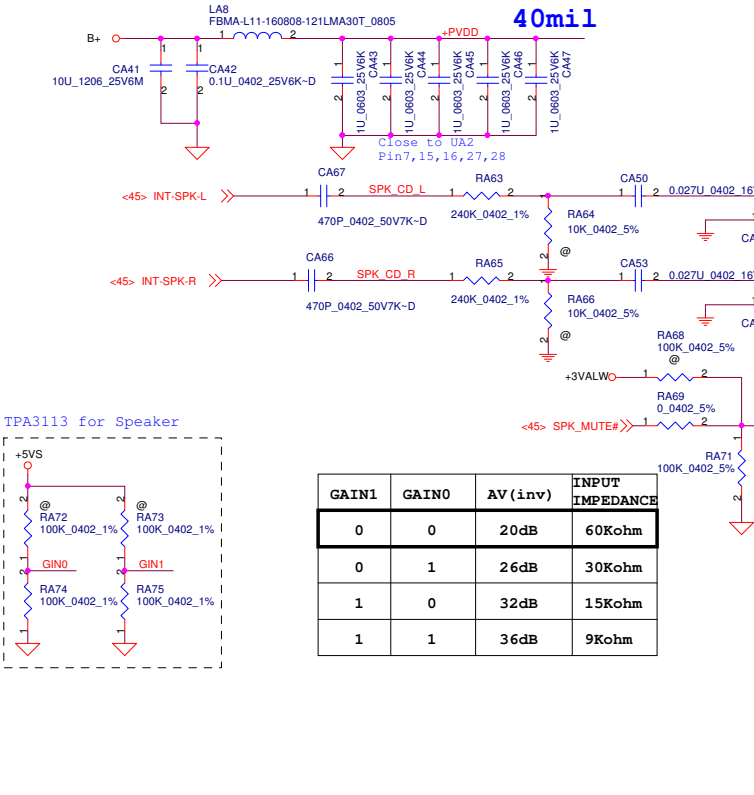
S2 (Out) : Center + HP2



S3 (Out) : Rear L/R



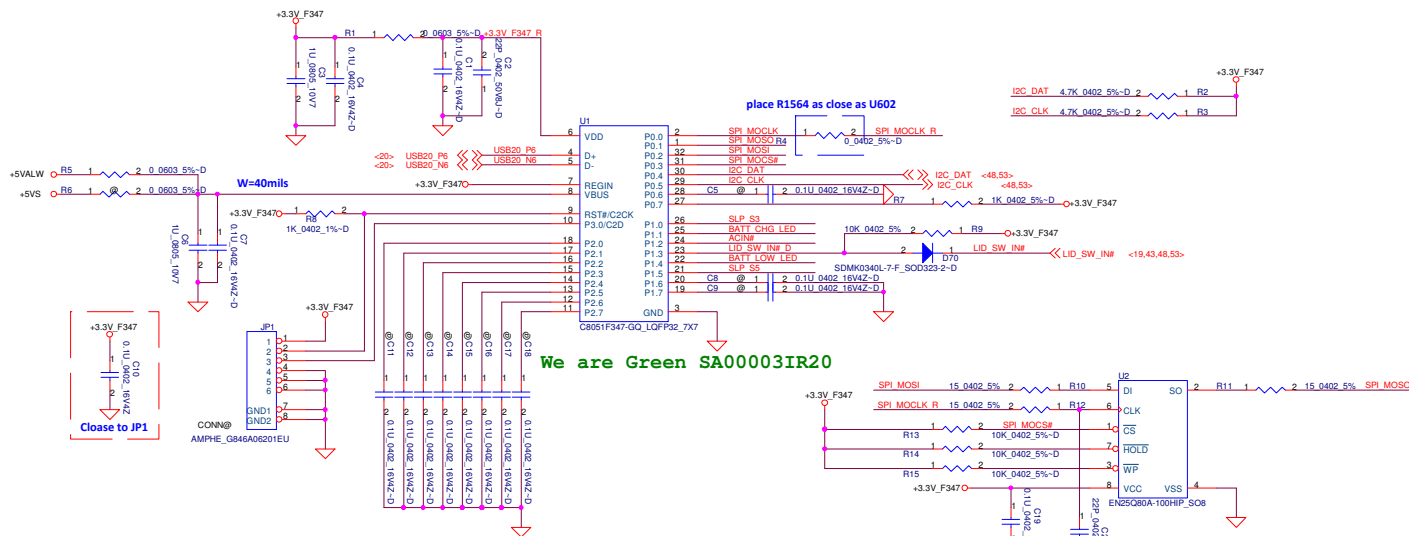
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Issued Date	2012/06/22	Deciphered Date	2013/06/21	HD Audio ALC3661	
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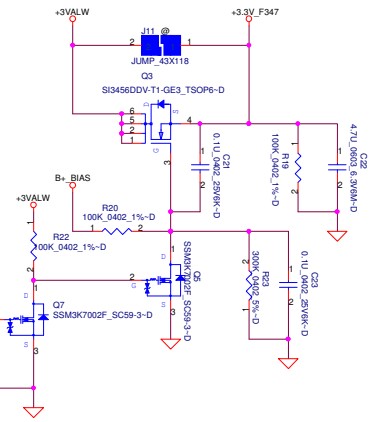
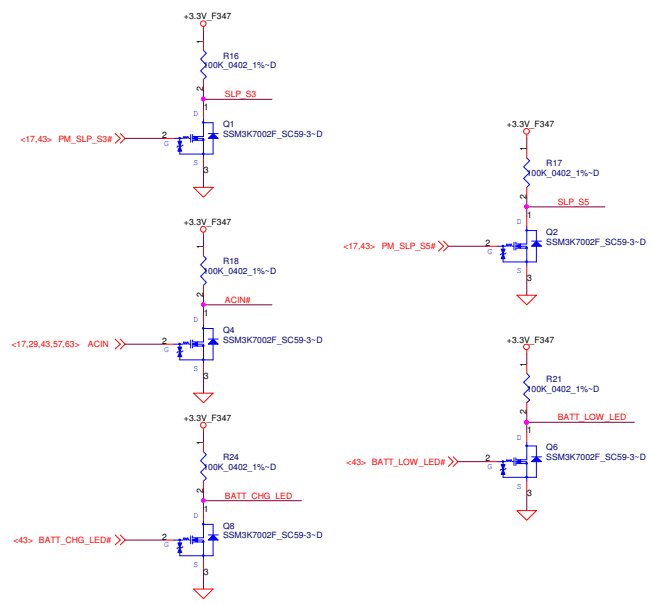
Speaker amp impedance of JBL is 4 ohm.

Speaker Connector

15 mils trace



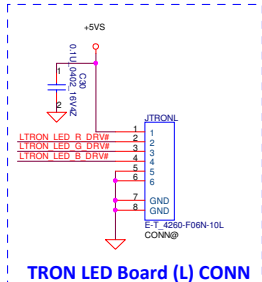
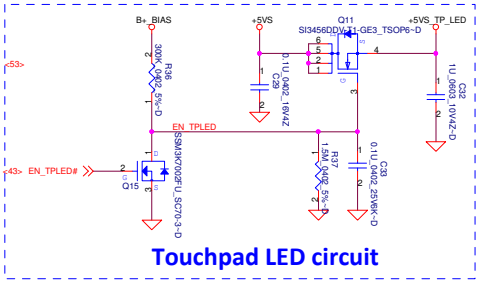
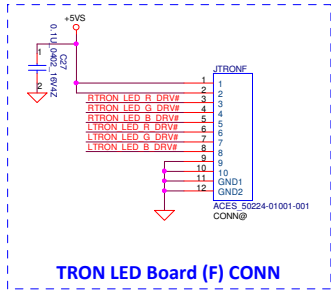
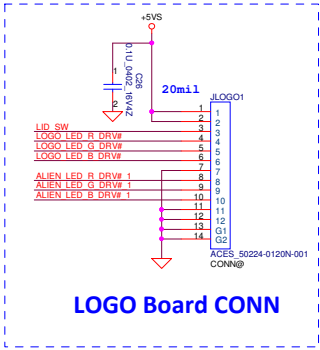
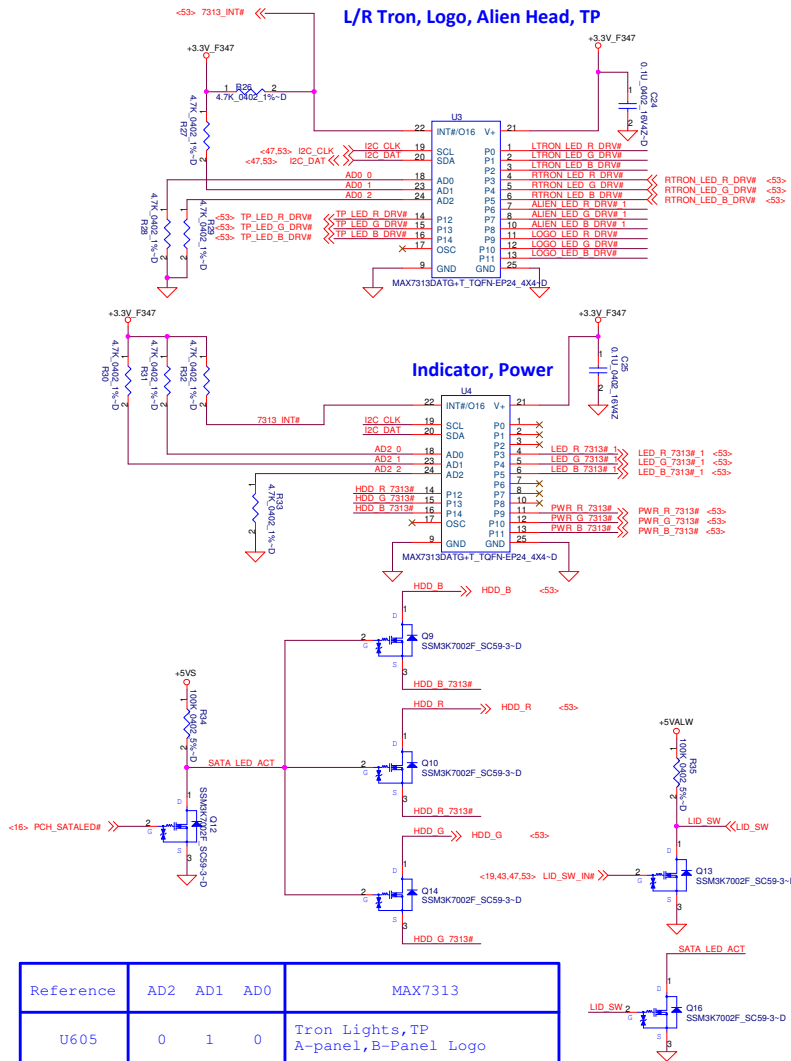
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b



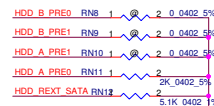
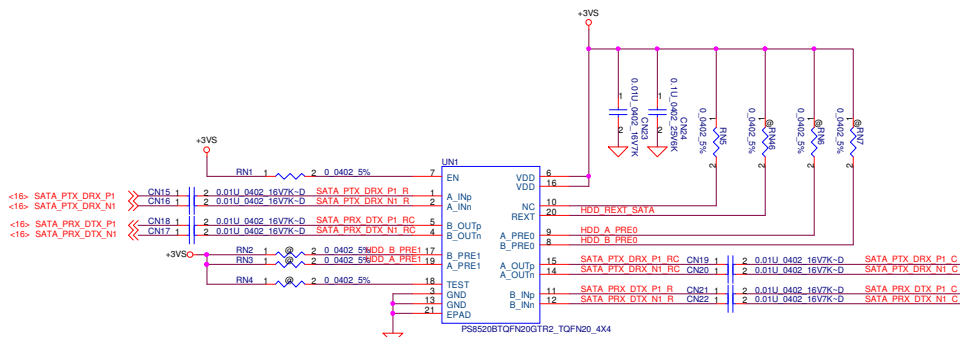
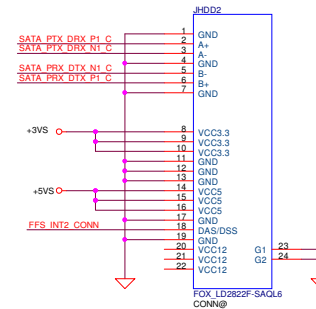
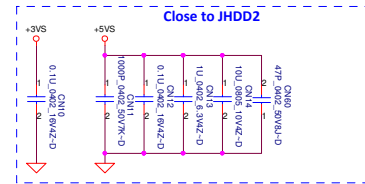
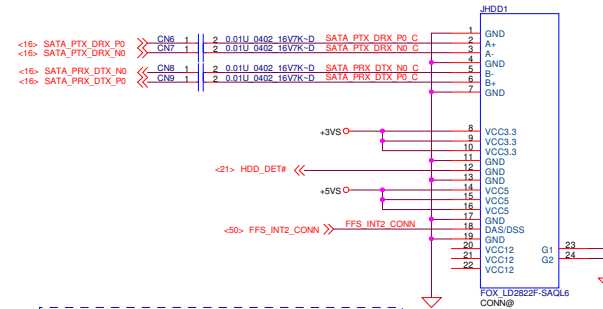
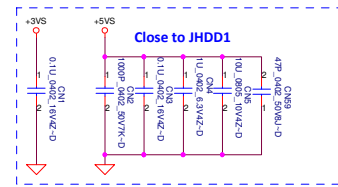
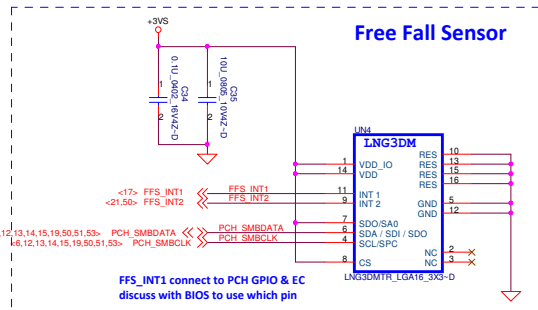
+3.3V F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5 turn off ELC controller



Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights, TP A-panel, B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness



Pin 20:
PARADE PS8250B:
Reserve RN46, Mount RN12

PERICOM P13EQX6741ST:
Mount RN46, Reserve RN12

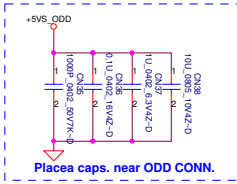
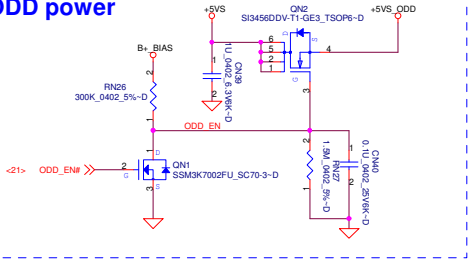
ASMEDIA ASM1466:
Mount RN46, Reserve RN12

Pin 9:
PARADE PS8250B:
Reserve RN11.

PERICOM P13EQX6741ST:
Reserve RN11

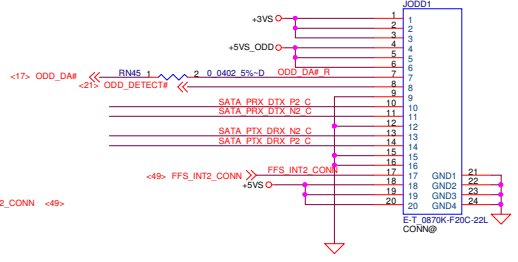
ASMEDIA ASM1466:
Mount RN11 to pull down

ODD power

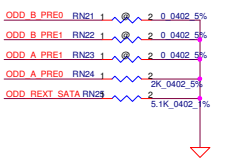
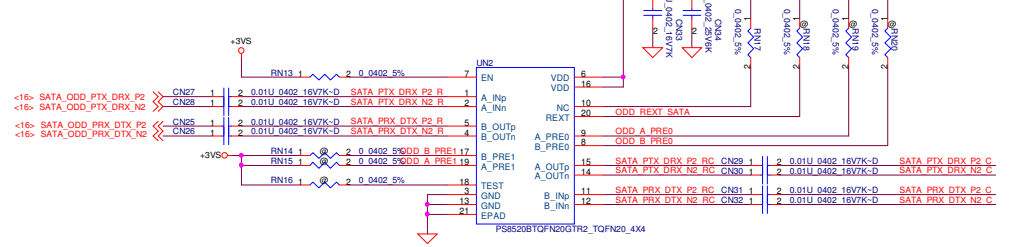


1. Host generate Low pulse 40ms to eject ODD
2. After this pulse, signal remain high and no pulse is allowed within 7s

SATA ODD Conn.

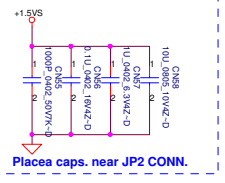
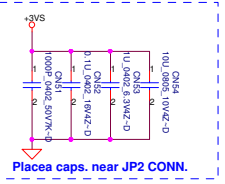
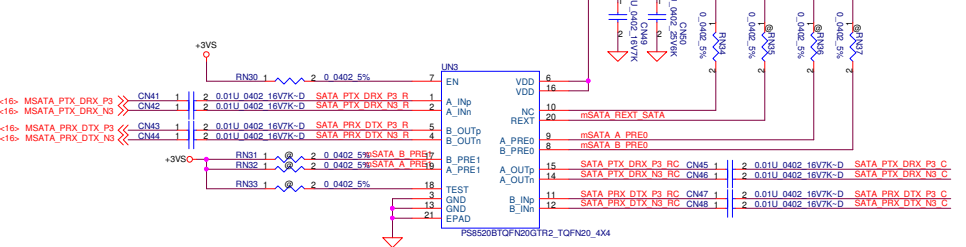


ODD Redriver

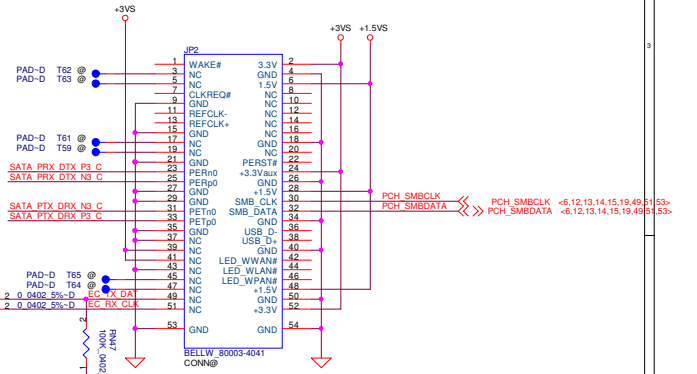


- Pin 20: PARADE PS8250B: Reserve RN18, Mount RN25
- Pin 9: PARADE PS8250B: Reserve RN24
- PERICOM P13EQX6741ST: Mount RN18, Reserve RN25
- PERICOM P13EQX6741ST: Reserve RN24
- ASMEIDIA ASM1466: Mount RN18, Reserve RN25
- ASMEIDIA ASM1466: Mount RN24 to pull down

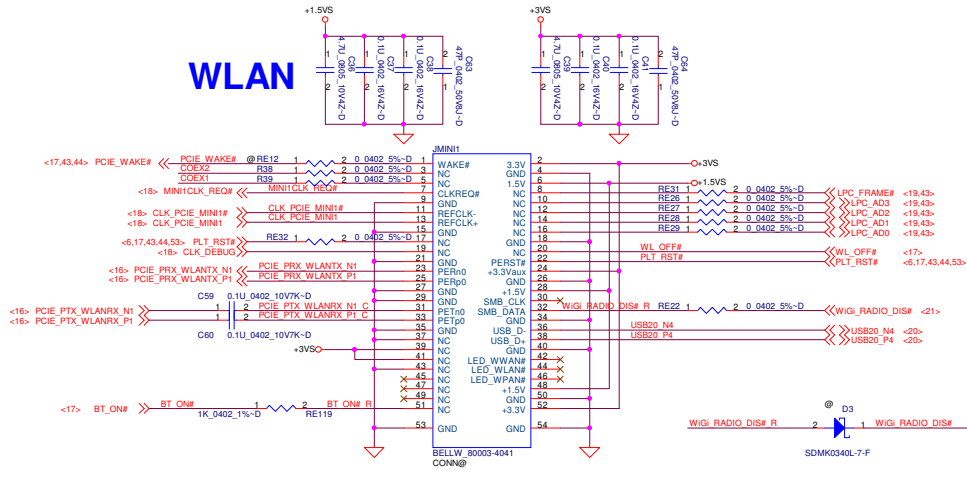
m-SATA Re-Driver



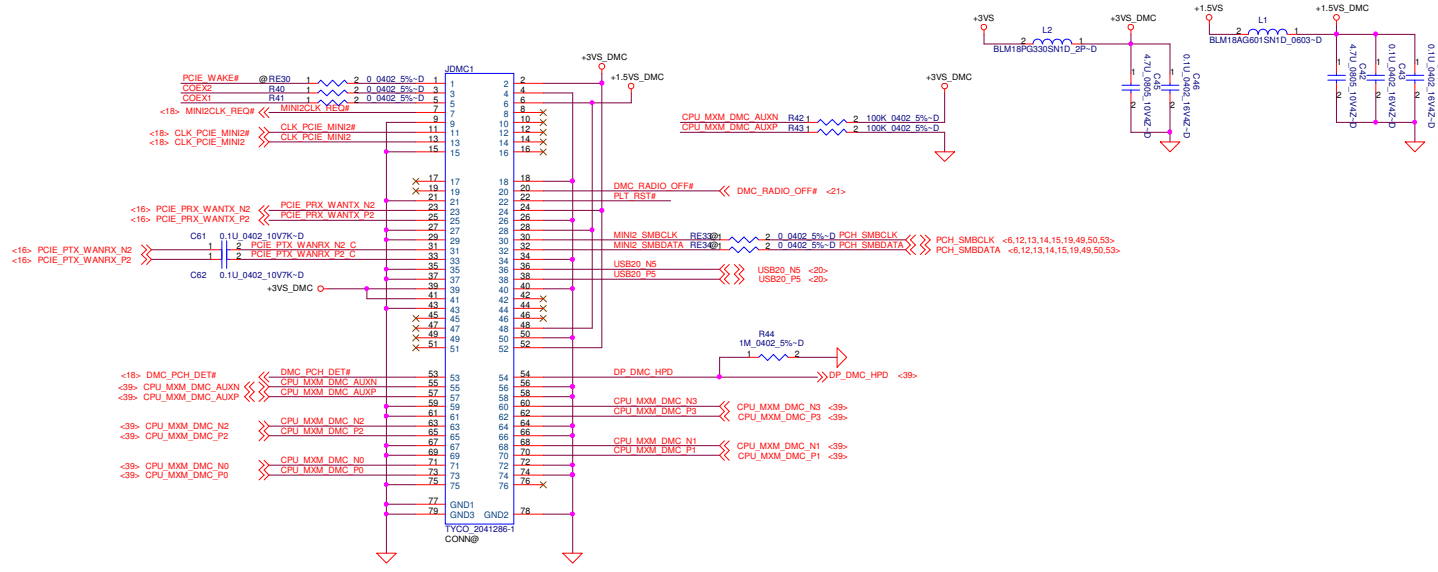
- Pin 20: PARADE PS8250B: Reserve RN35, Mount RN42
- Pin 9: PARADE PS8250B: Reserve RN41
- PERICOM P13EQX6741ST: Mount RN35, Reserve RN42
- PERICOM P13EQX6741ST: Reserve RN41
- ASMEIDIA ASM1466: Mount RN35, Reserve RN42
- ASMEIDIA ASM1466: Mount RN41 to pull down



WLAN

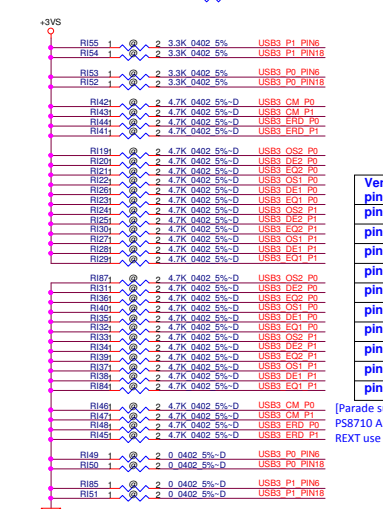
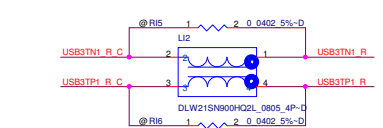
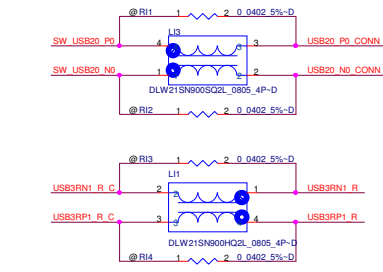


Display Mini Card (DMC)



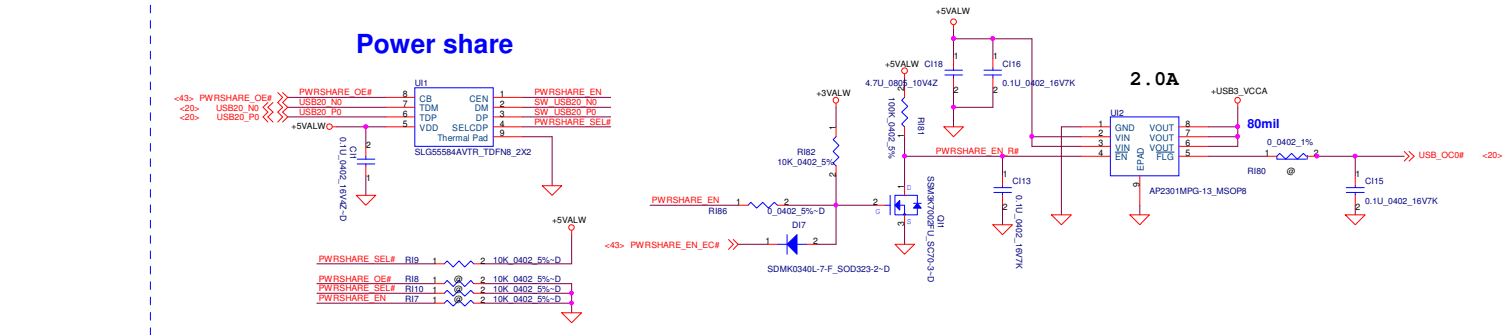
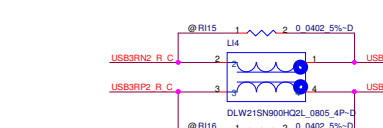
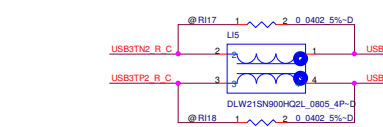
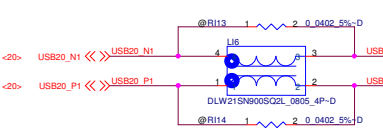
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Issued Date	2012/06/22	Deciphered Date	2013/06/21	Mini Card -WLAN/DMC/BT
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Power share

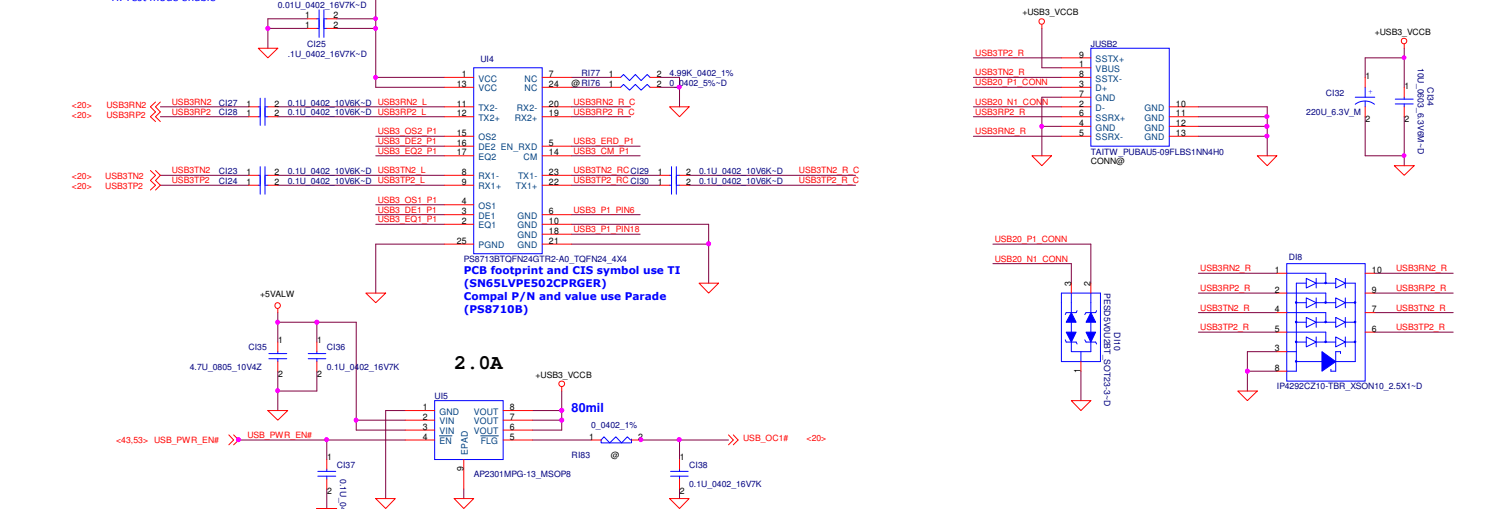
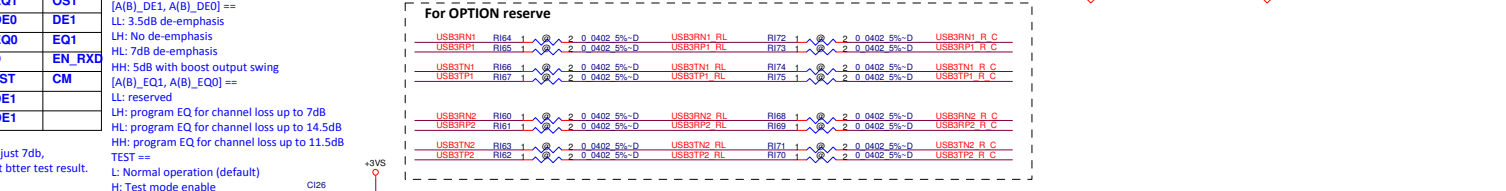
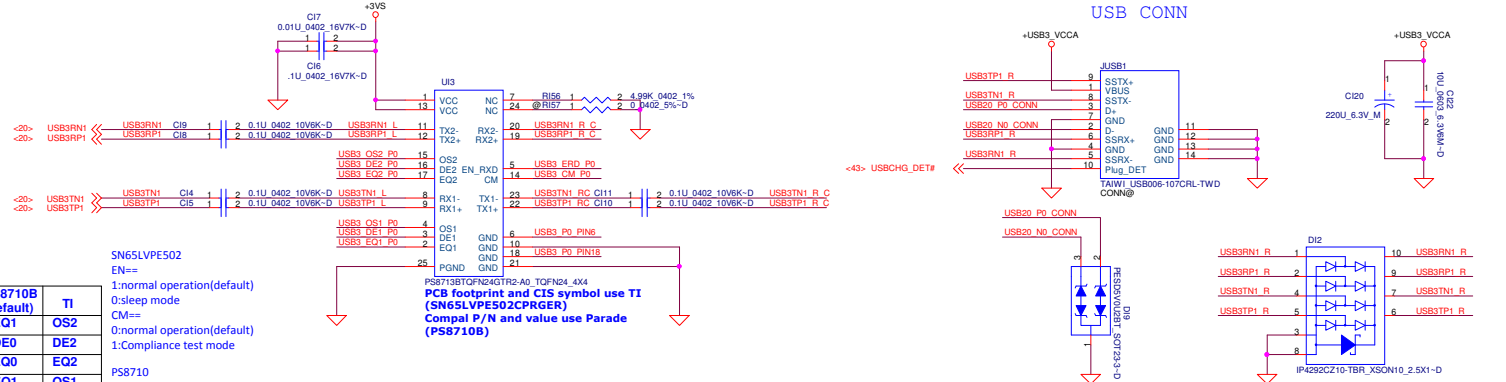


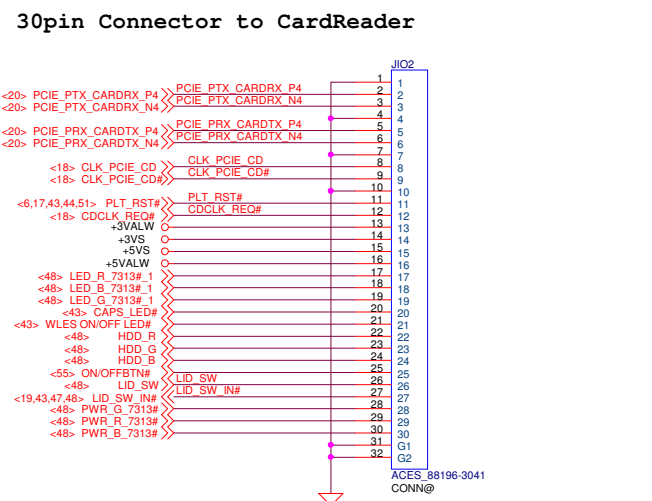
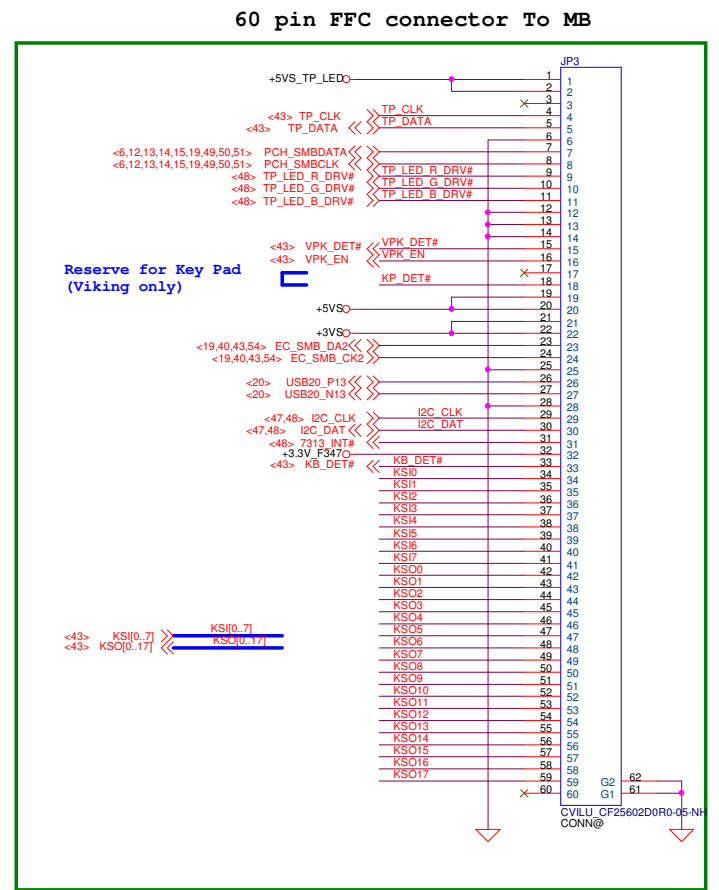
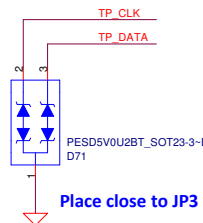
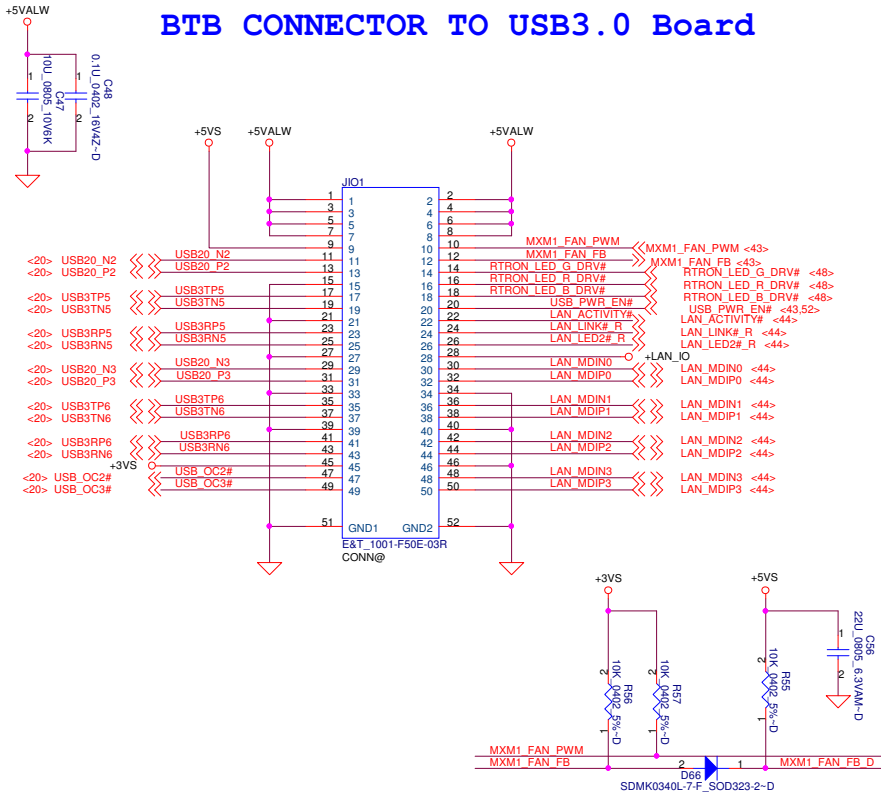
Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

[Parade suggest]
PS8710 AEQ0,BEQ0 adjust 7db,
REXT use 3.3 K well get btter test result.



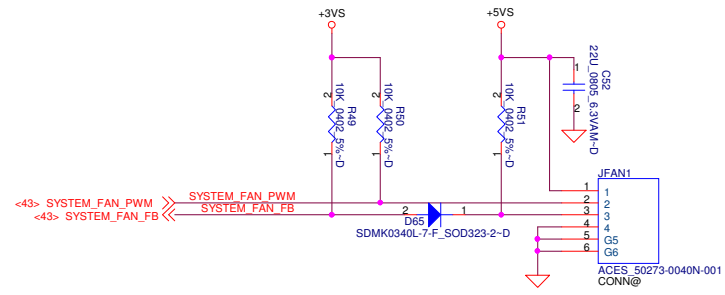
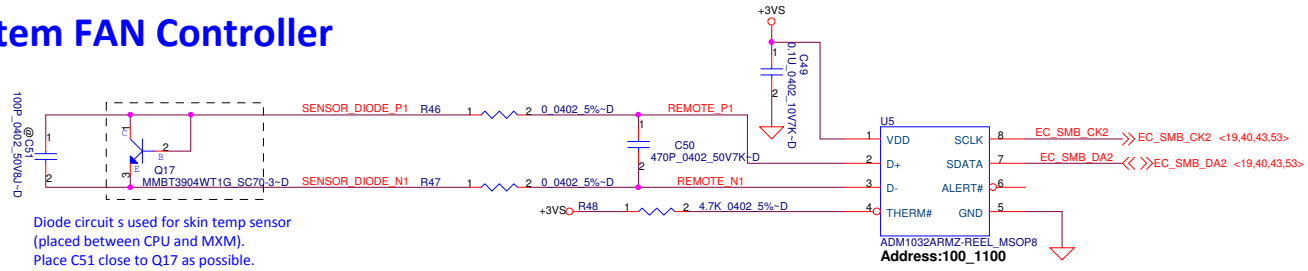
USB CONN



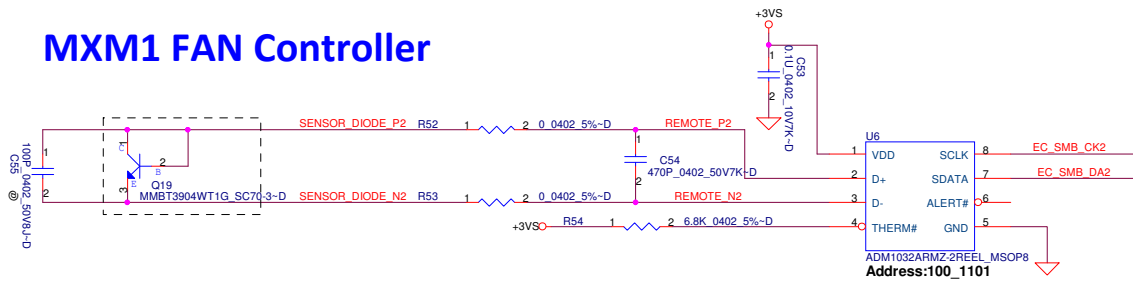


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System FAN Controller

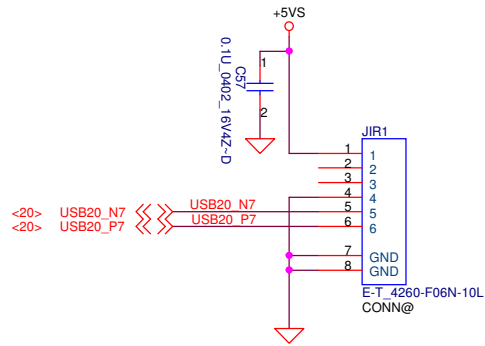


MXM1 FAN Controller

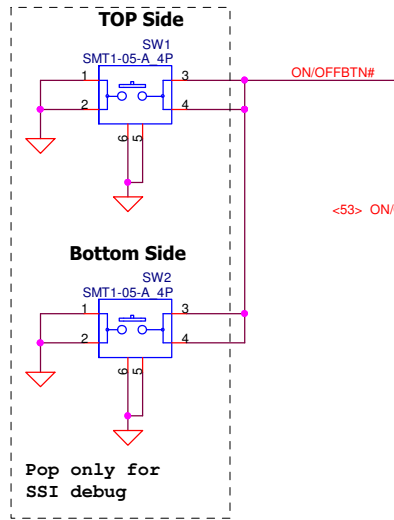


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Issued Date	2012/06/22	Deciphered Date	2013/06/21	Compal Electronics, Inc.	
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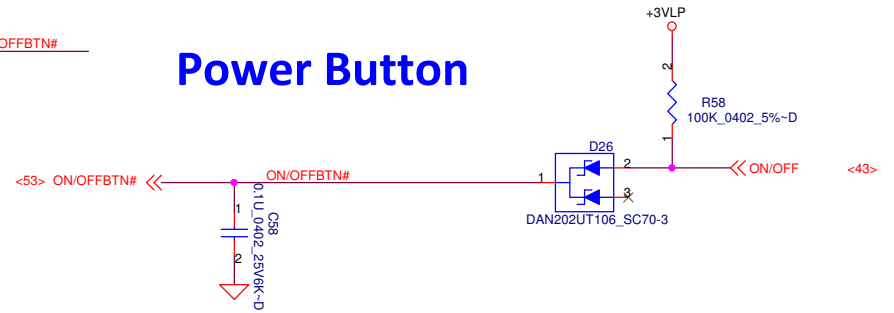
IR SENSOR connector



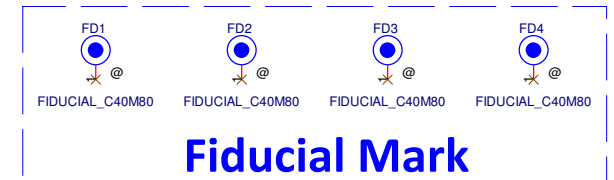
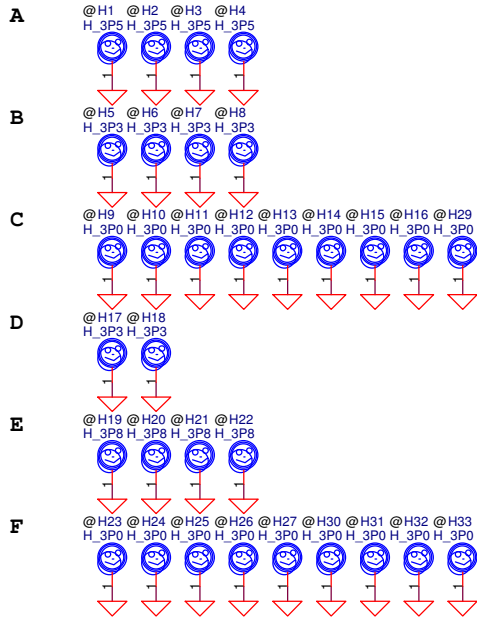
ON/OFF switch



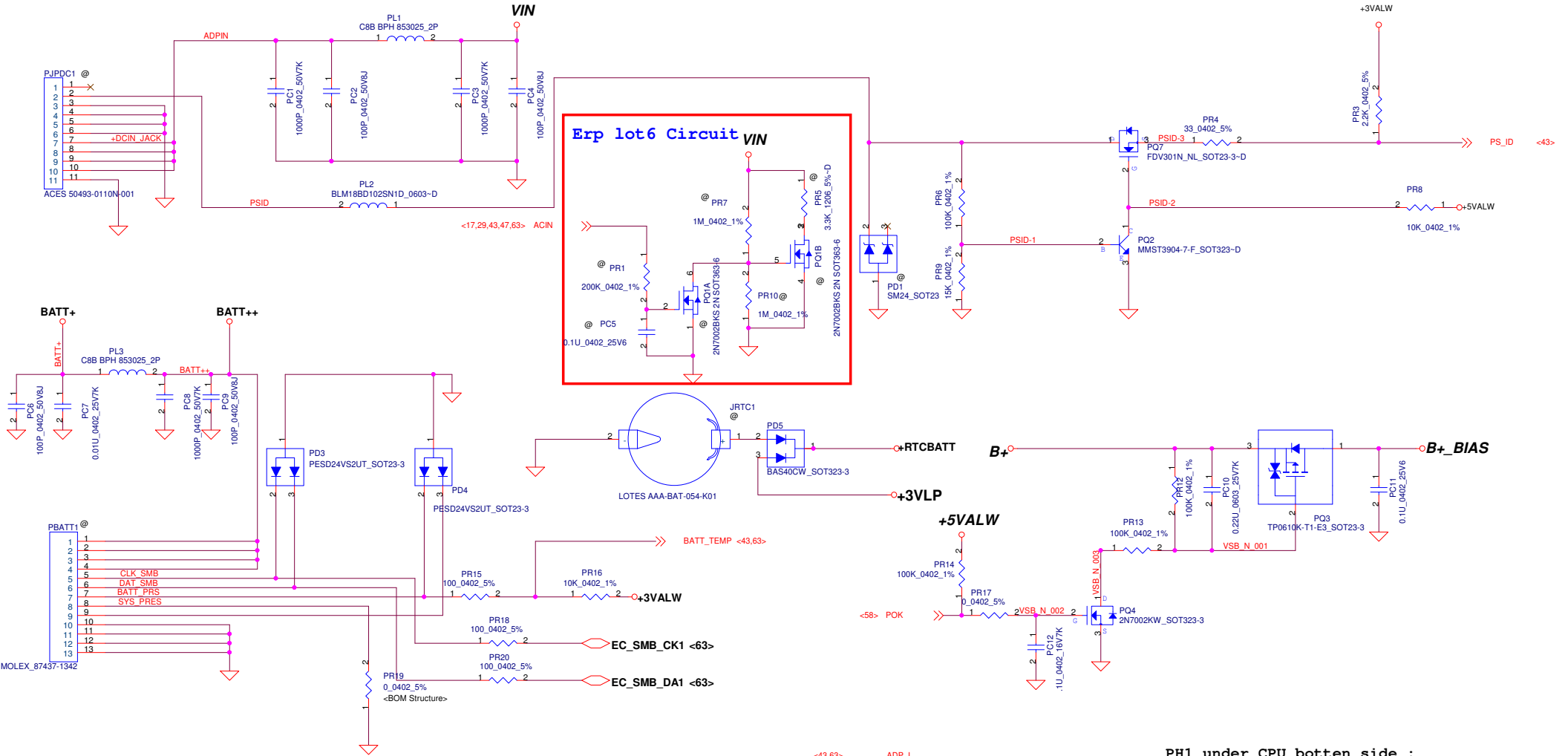
Power Button



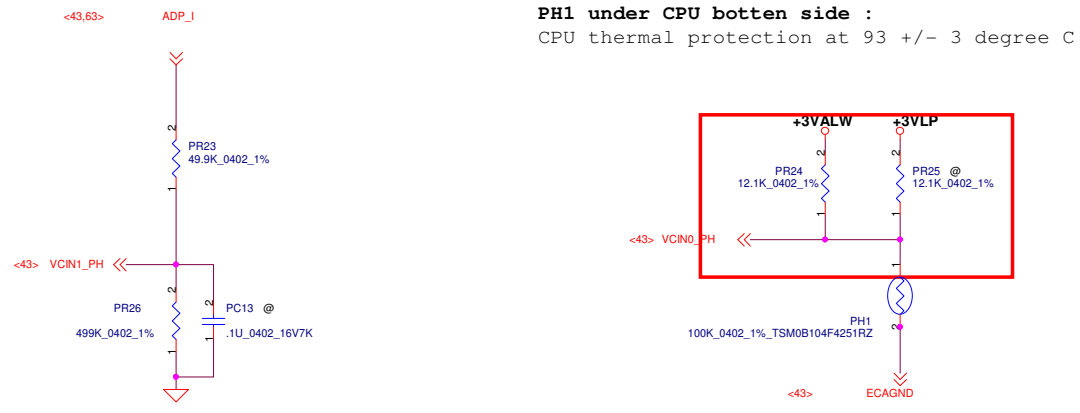
Pop only for SSI debug



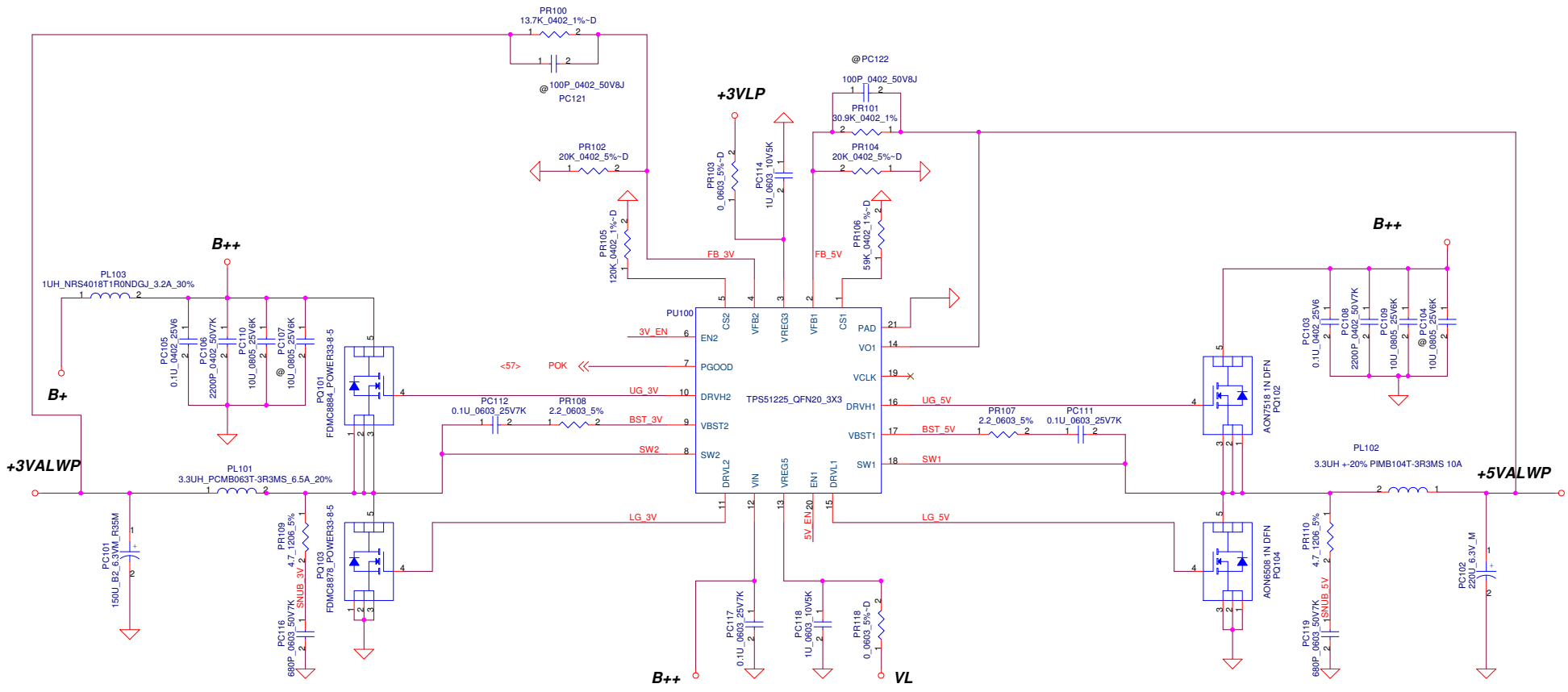
Security Classification	Compal Secret Data			Title	KB & Power Button & IR	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Size	Document Number	Rev
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PH1 under CPU bottom side :
 CPU thermal protection at 93 +/- 3 degree C

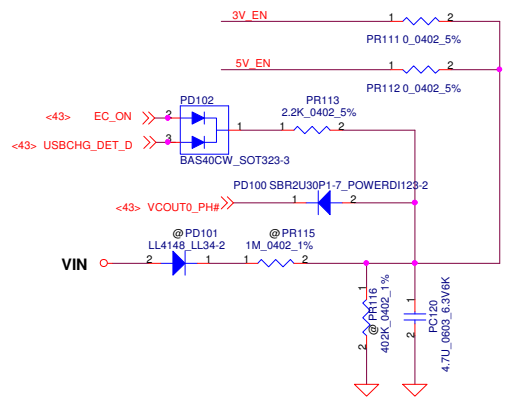


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3VALWP
 TDC 6.08A
 Peak Current 8.11A
 OCP current 9.73A

	TYP	MAX
H/S Rds (on)	:22mohm	30mohm
L/S Rds (on)	:12.1mohm	17mohm



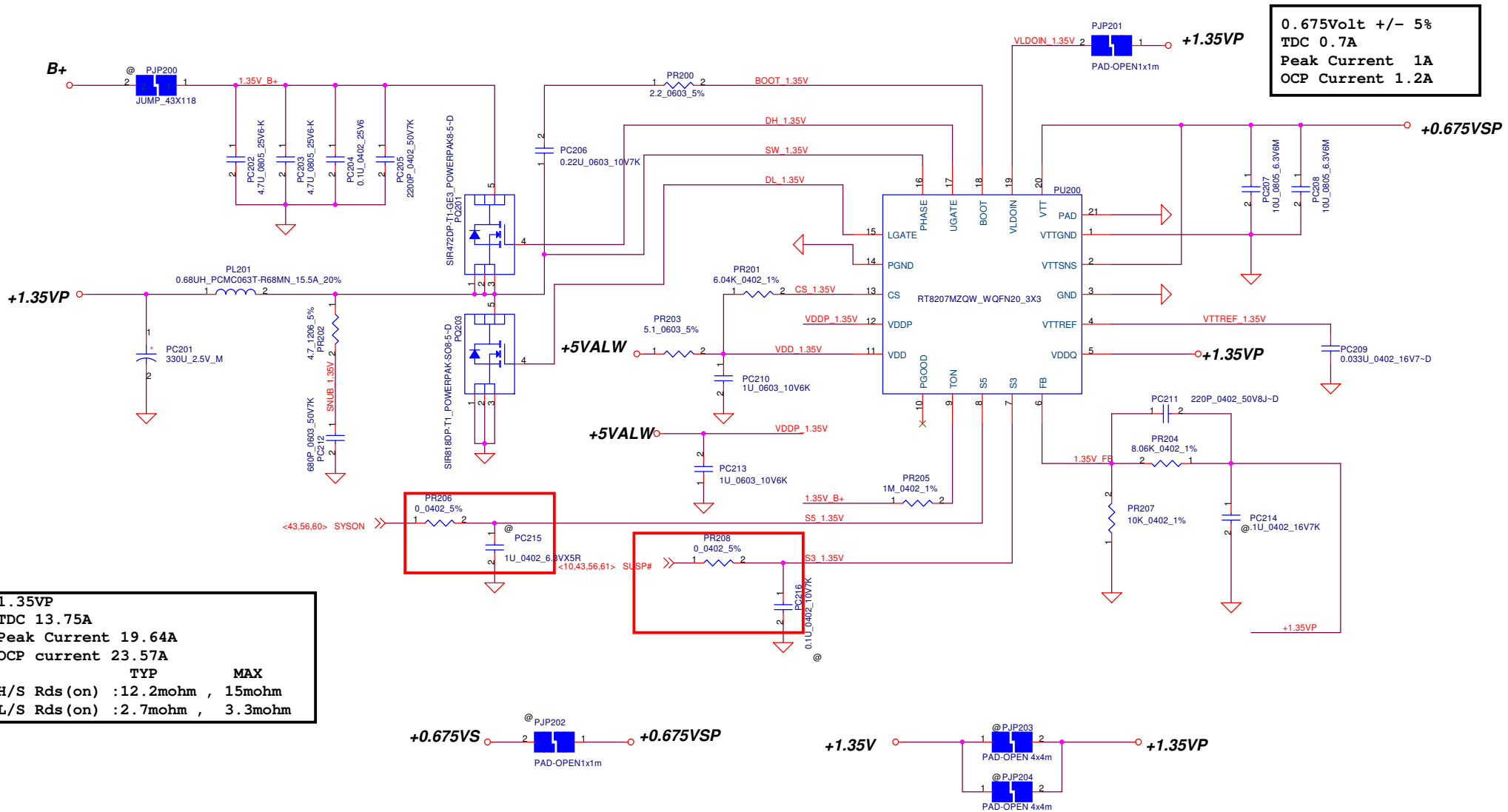
5VALWP
 TDC 10.64A
 Peak Current 14.19A
 OCP current 17.03A

	TYP	MAX
H/S Rds (on)	11.2mohm	14mohm
L/S Rds (on)	:3.7mohm	5mohm

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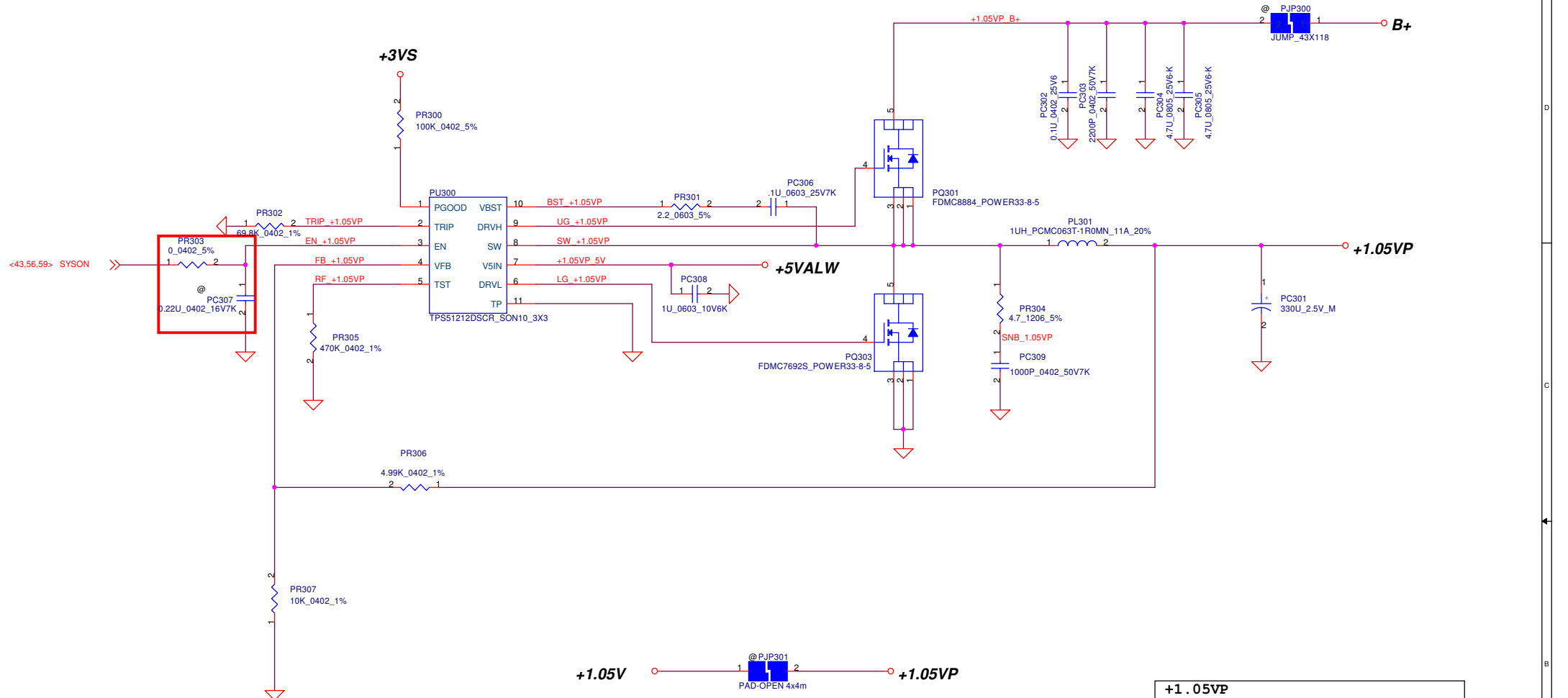
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Title	PWR-3VALWP/SVALWP
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0.675V_{olt} +/- 5%
 TDC 0.7A
 Peak Current 1A
 OCP Current 1.2A

1.35VP
 TDC 13.75A
 Peak Current 19.64A
 OCP current 23.57A
 TYP MAX
 H/S Rds (on) : 12.2mohm , 15mohm
 L/S Rds (on) : 2.7mohm , 3.3mohm

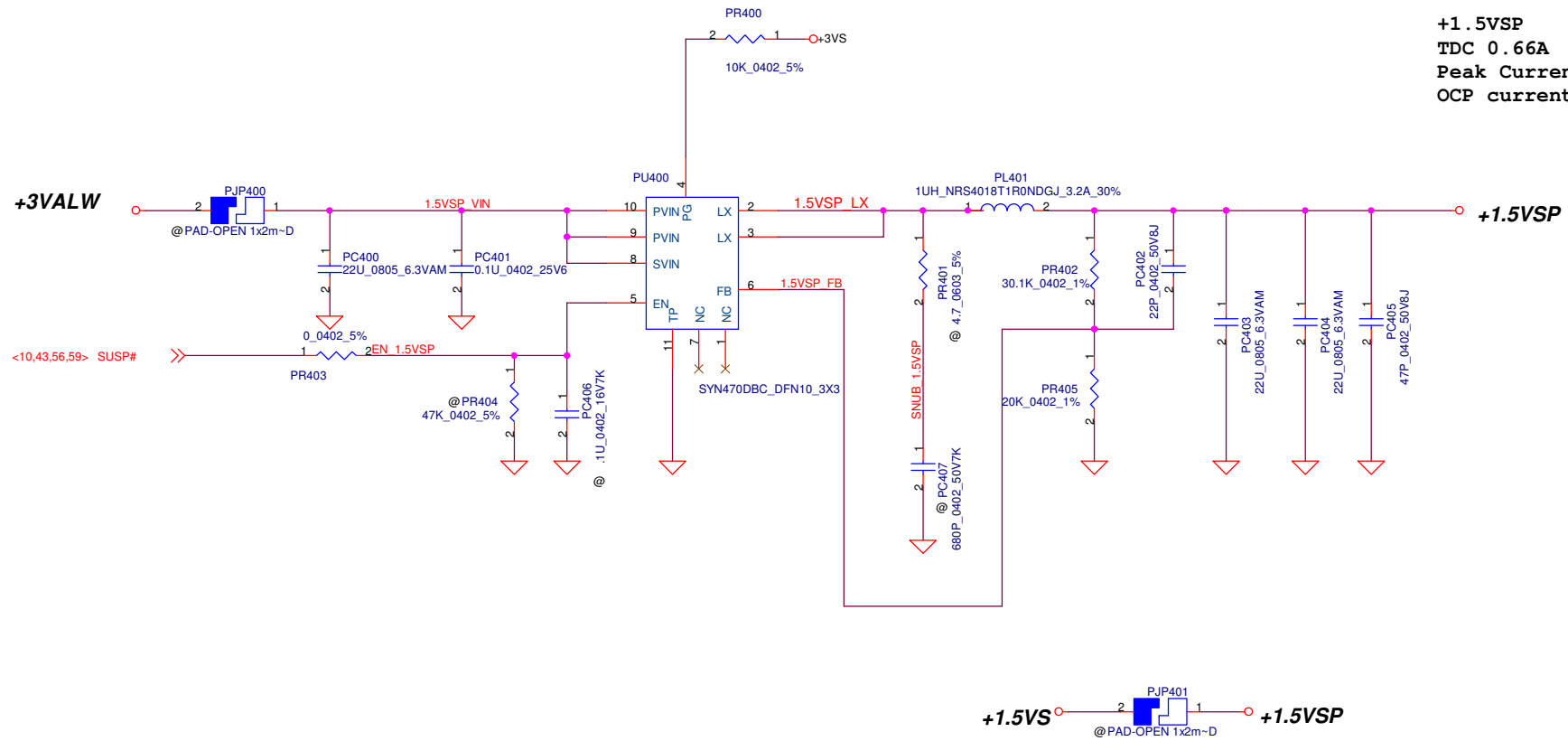
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+1.05VP	
TDC 4.56A	
Peak Current 6.51A	
OCP current 7.81A	
	TYP MAX
H/S Rds (on)	: 22mohm , 30mohm
L/S Rds (on)	: 10.8mohm , 13.6mohm

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PWR+1.05VP
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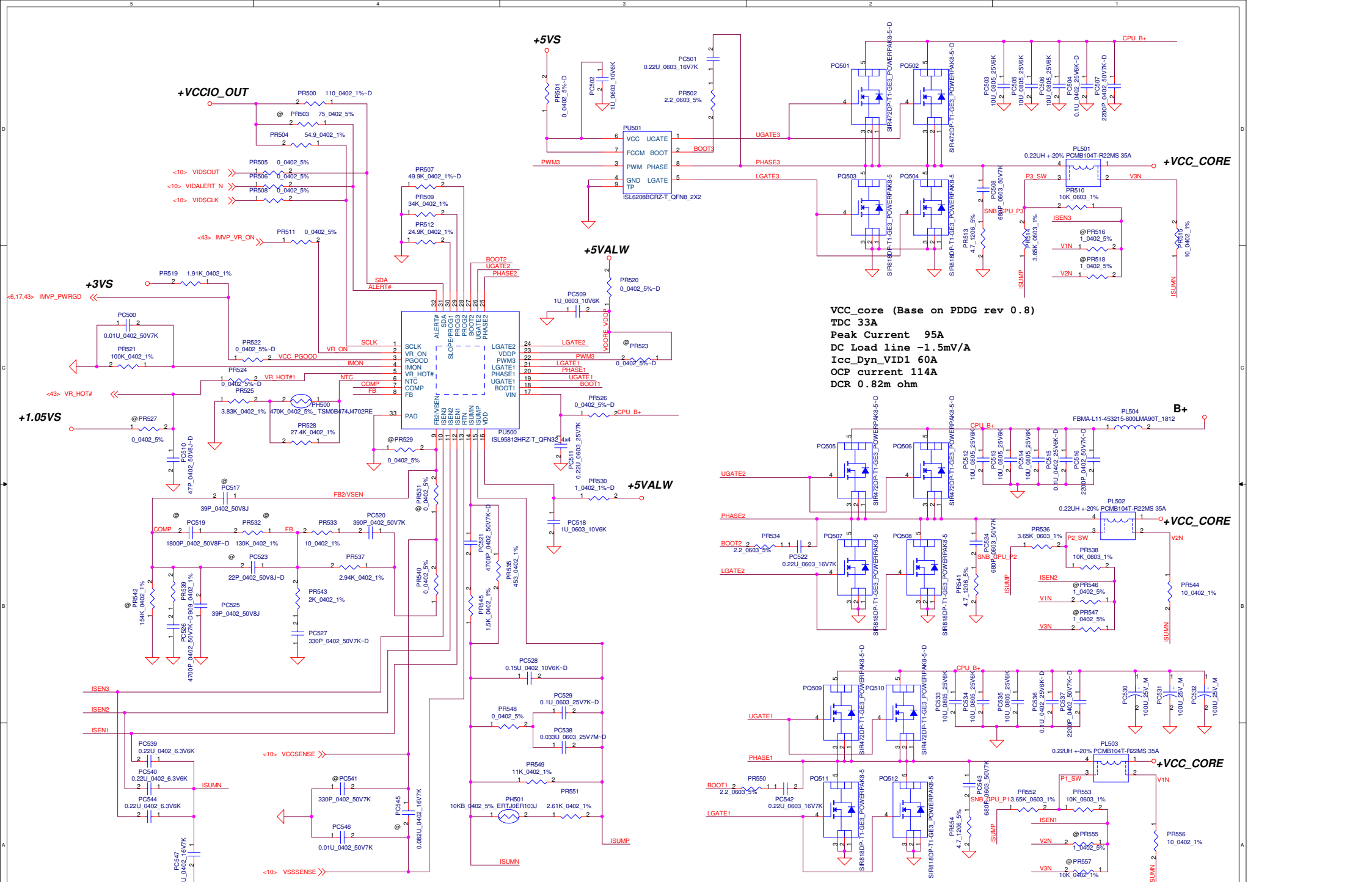


+1.5VSP
TDC 0.66A
Peak Current 0.88A
OCp current 1.06A

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VCC_core (Base on PDDG rev 0.8)
TDC 33A
Peak Current 95A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCp current 114A
DCR 0.82m ohm

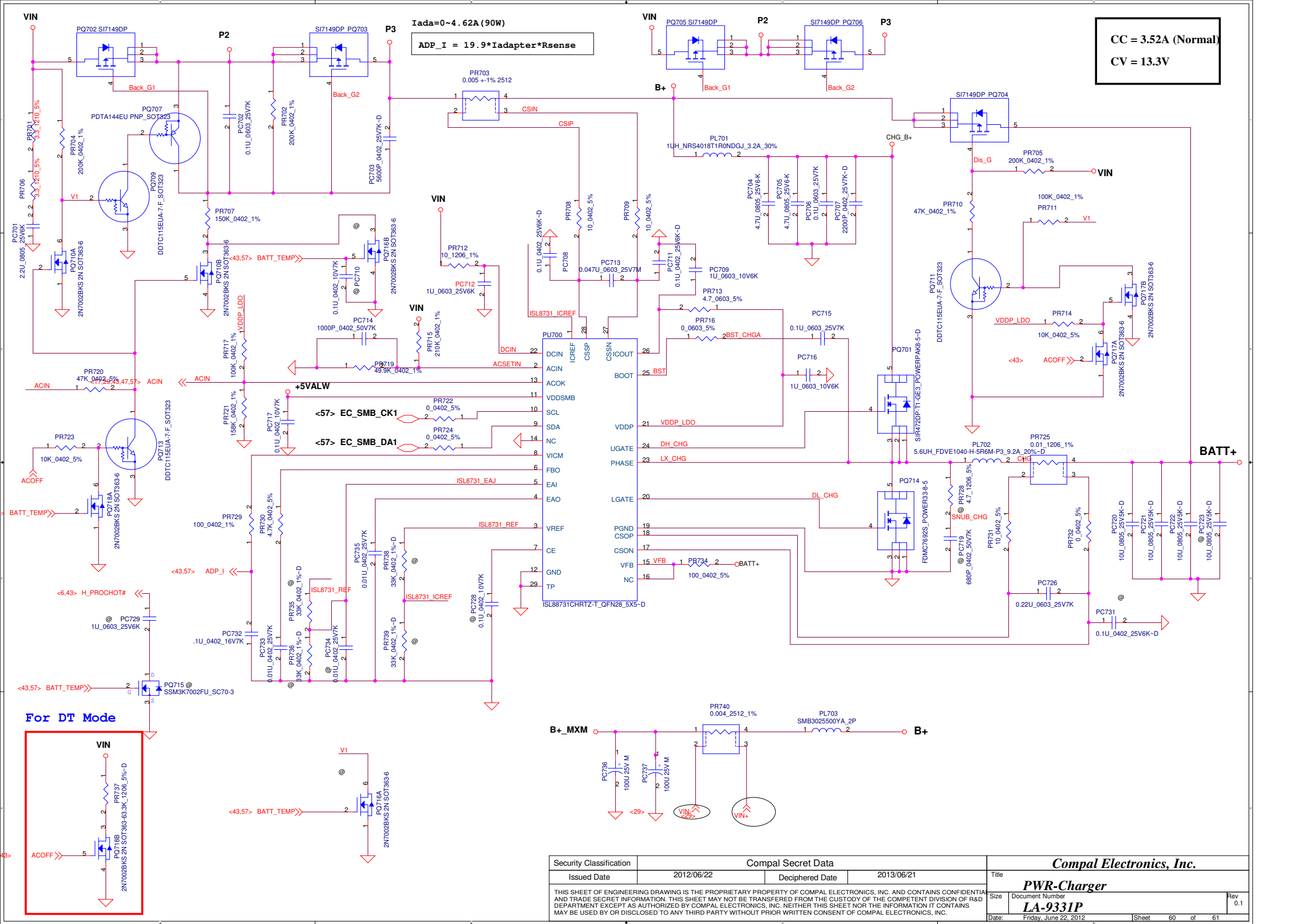
Local sense put on HW site

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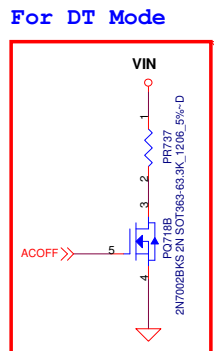
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File		+VCC_CORE	
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Tada=0~4.62A (90W)
 $ADP_I = 19.9 * I_{adapter} * R_{sense}$

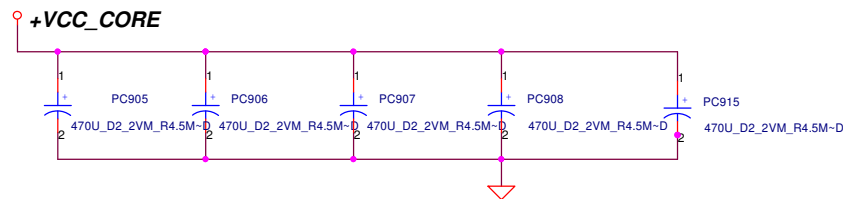
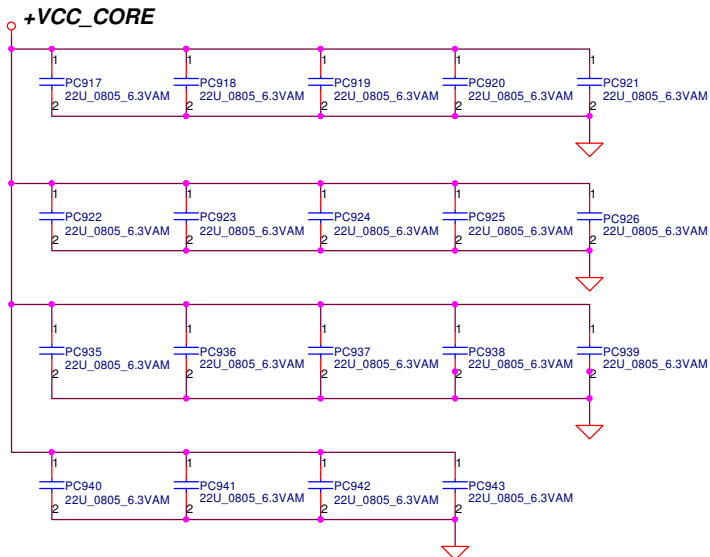
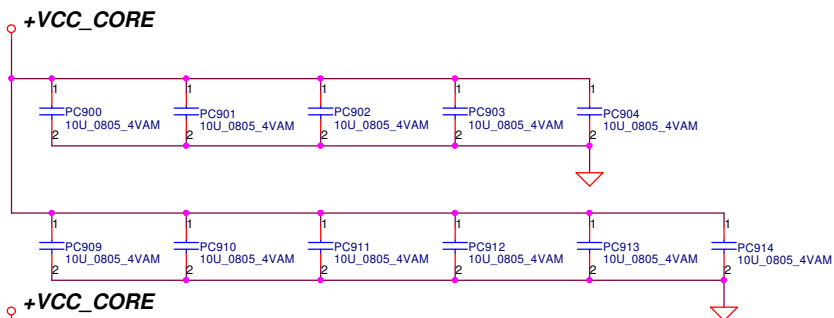
CC = 3.52A (Normal)
 CV = 13.3V



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Based on PDDG rev 0.8 Table 5-1.



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