

Compal Confidential

Model Name : VIUS1
File Name : LA-9611P
BOM P/N:

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M/B Schematics Document
Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU AMD

2012-02-18
REV:0.4

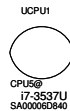
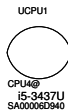
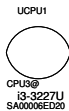
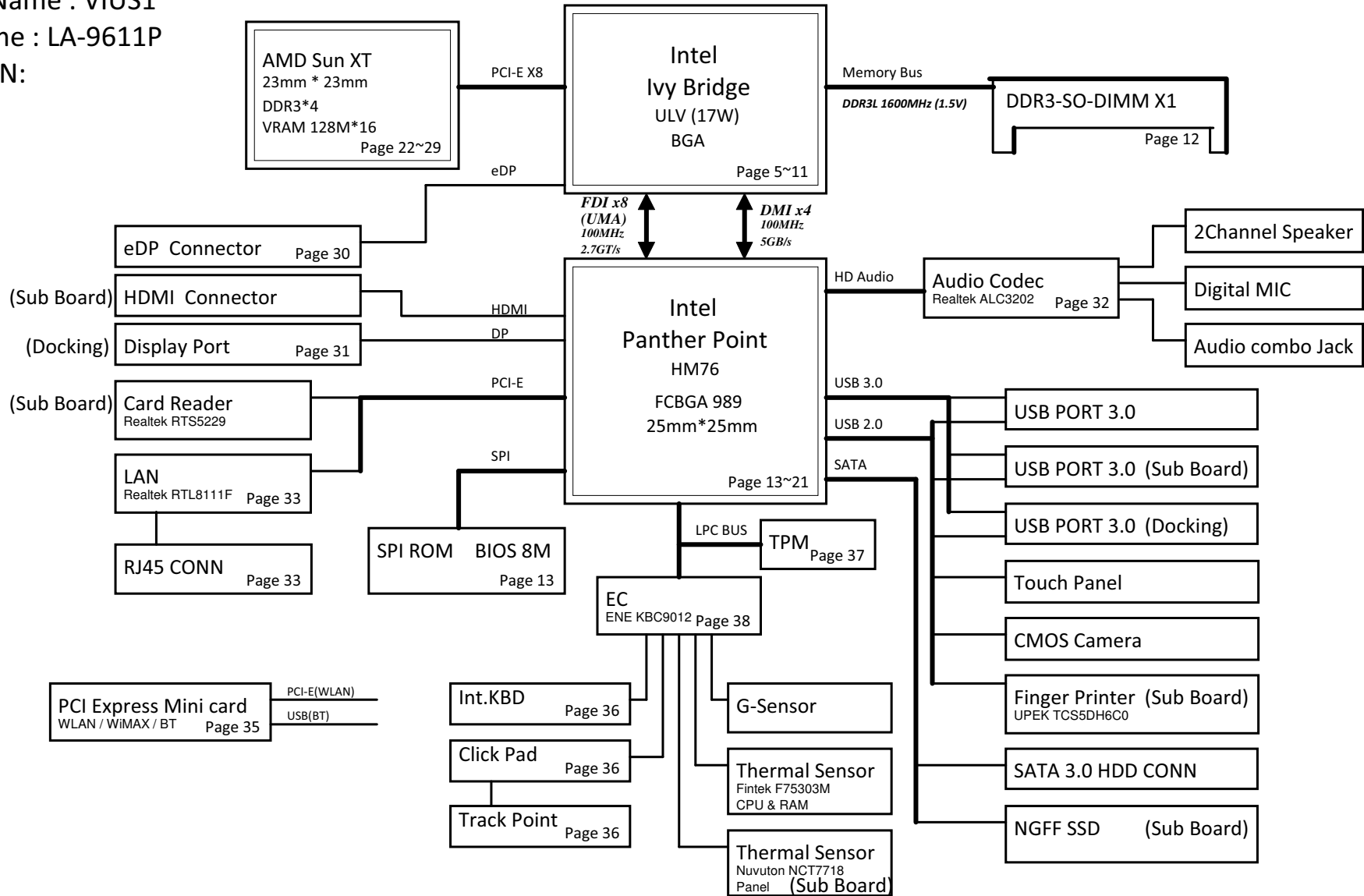
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	Cover Sheet
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power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM- (SBA Only)
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

BOARD ID Table

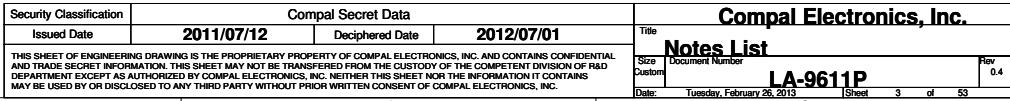
USB Port Table

BOM Structure Table

[illegible]**EC SM Bus2 address**

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SMLOCLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X



MB Bottom view

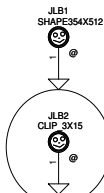
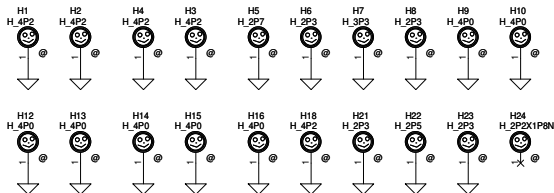


PCH

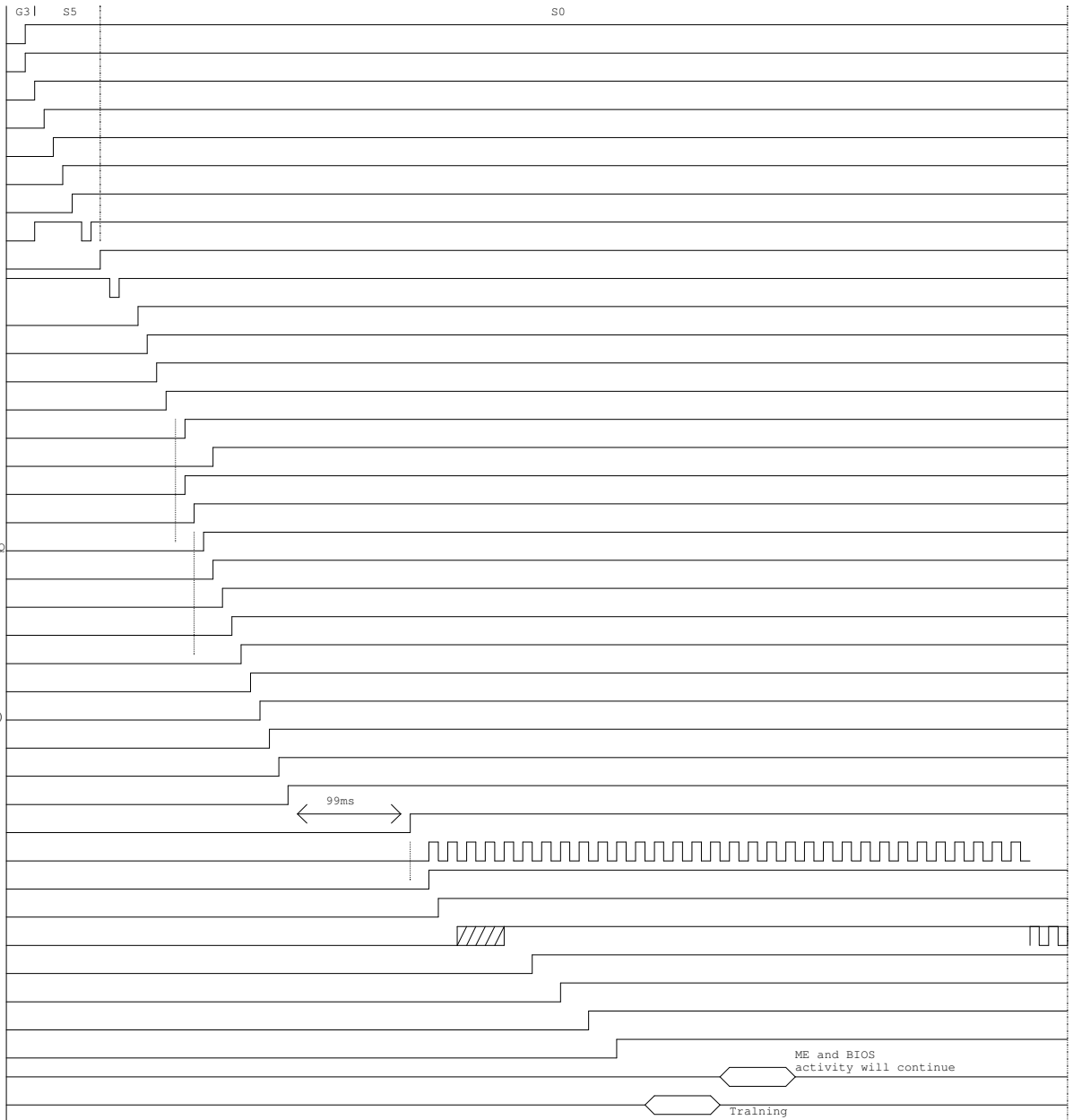
GPU

RAM

CPU



RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
M_PWR_ON
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CUPFWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI

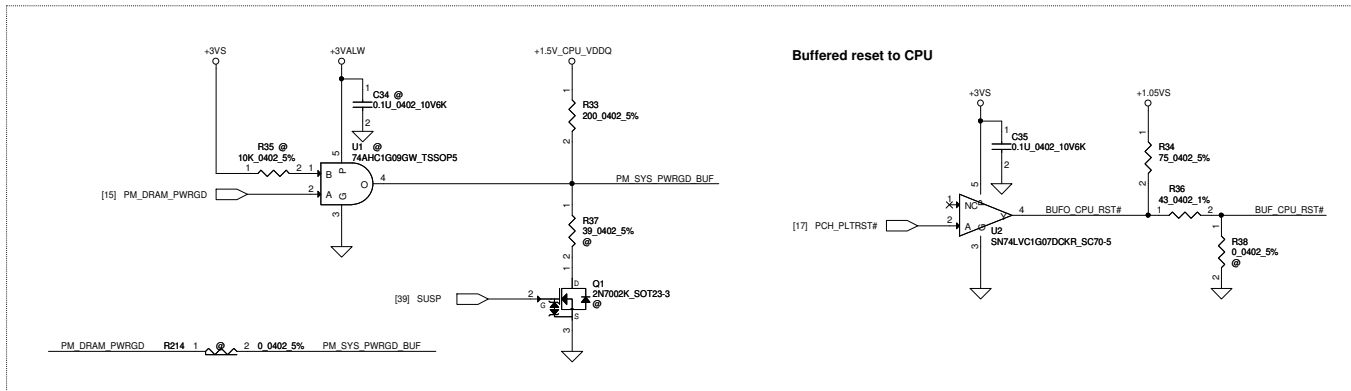
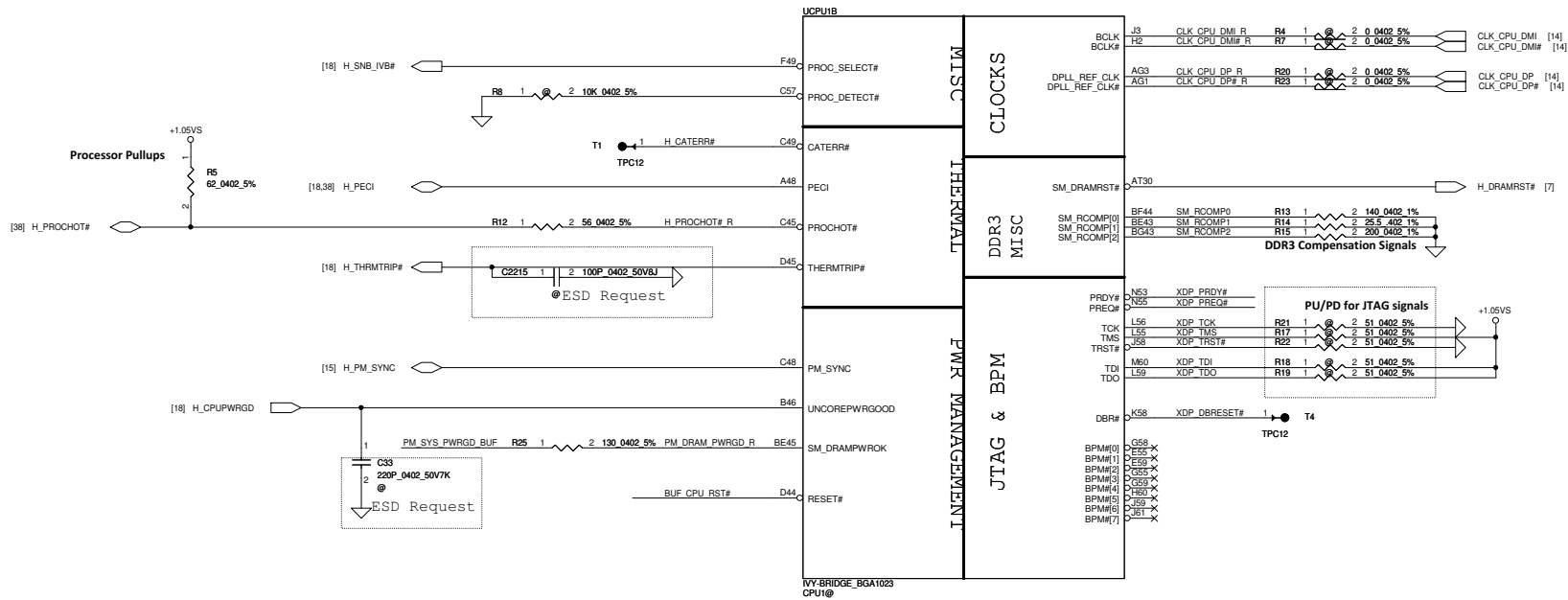


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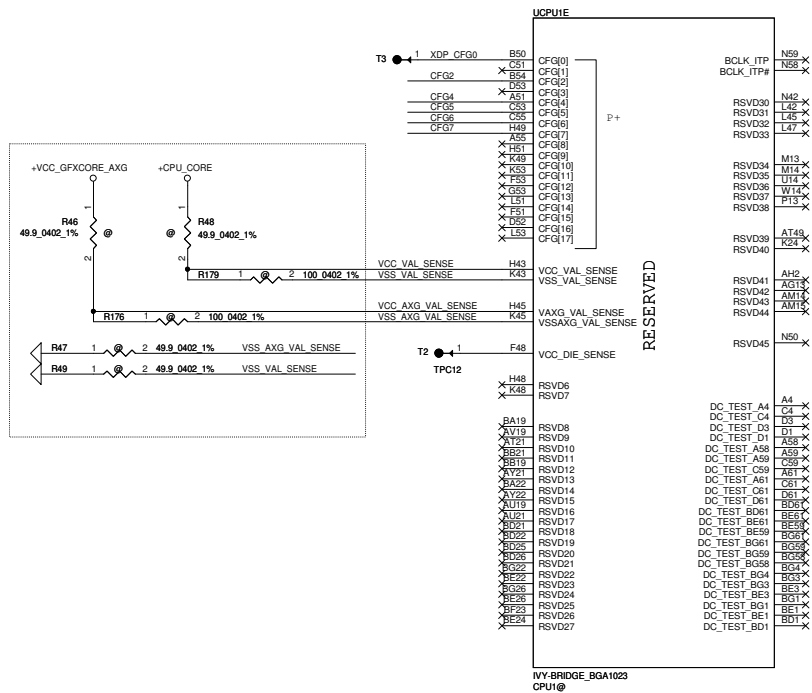
Compal Electronics, Inc.

Screw Hole

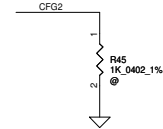
Rev 0.4



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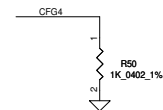


CFG Straps for Processor



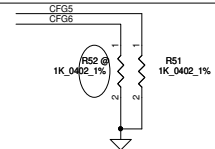
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	---



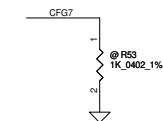
Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	---



PCIe Port Bifurcation Straps

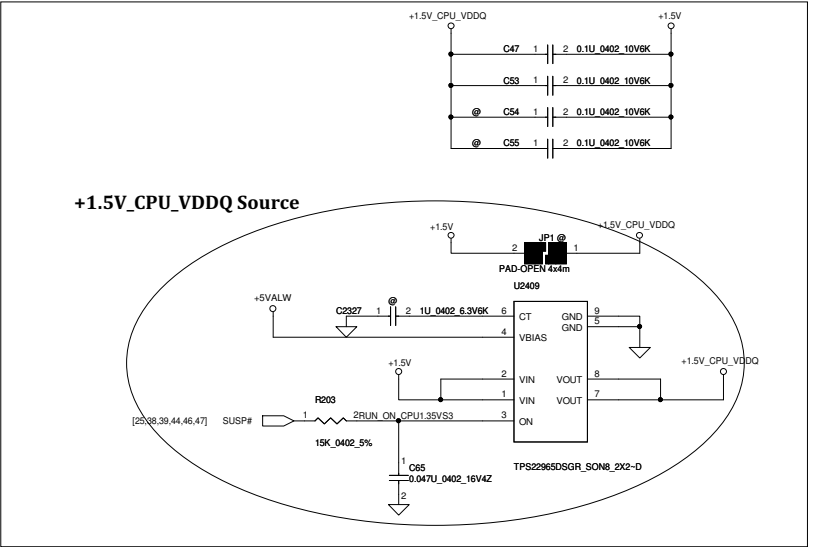
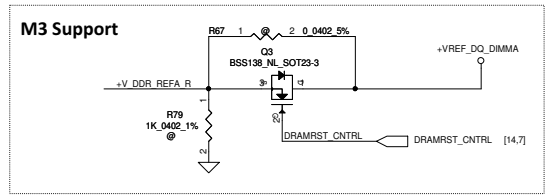
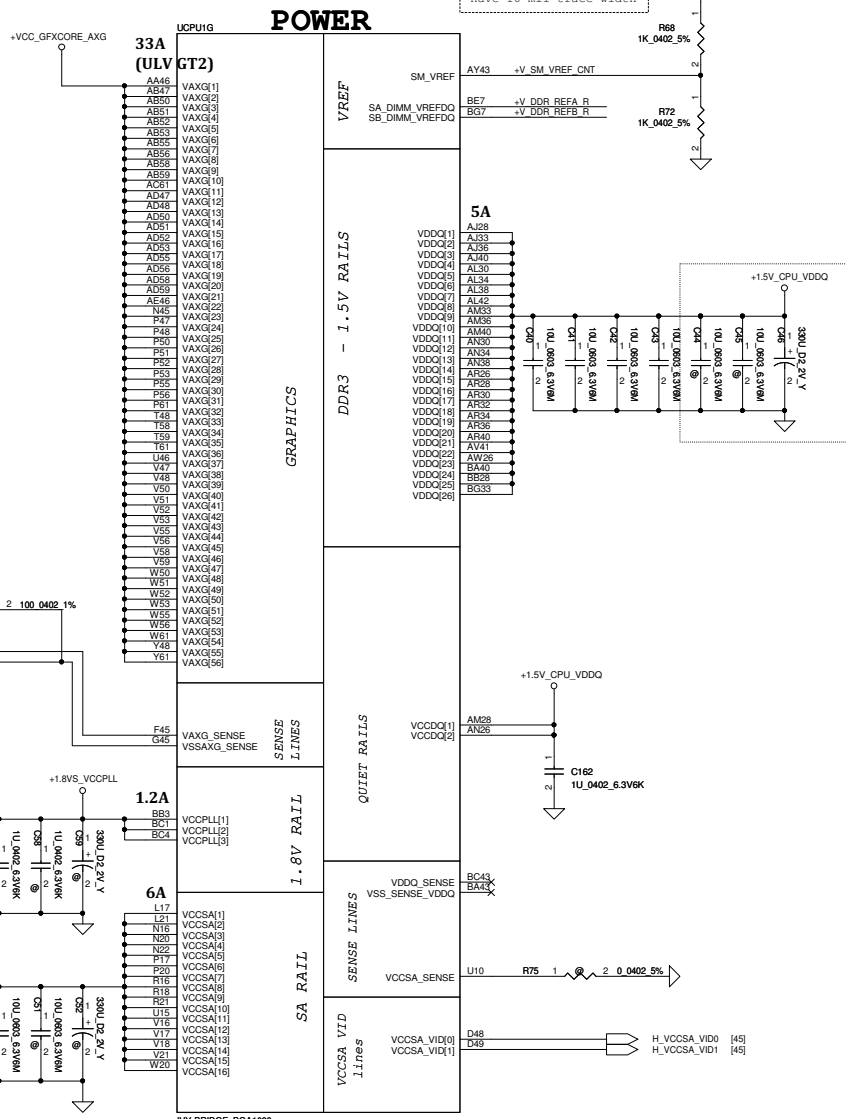
CFG[6:5]	— 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved ★ — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express*
----------	---



PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	--

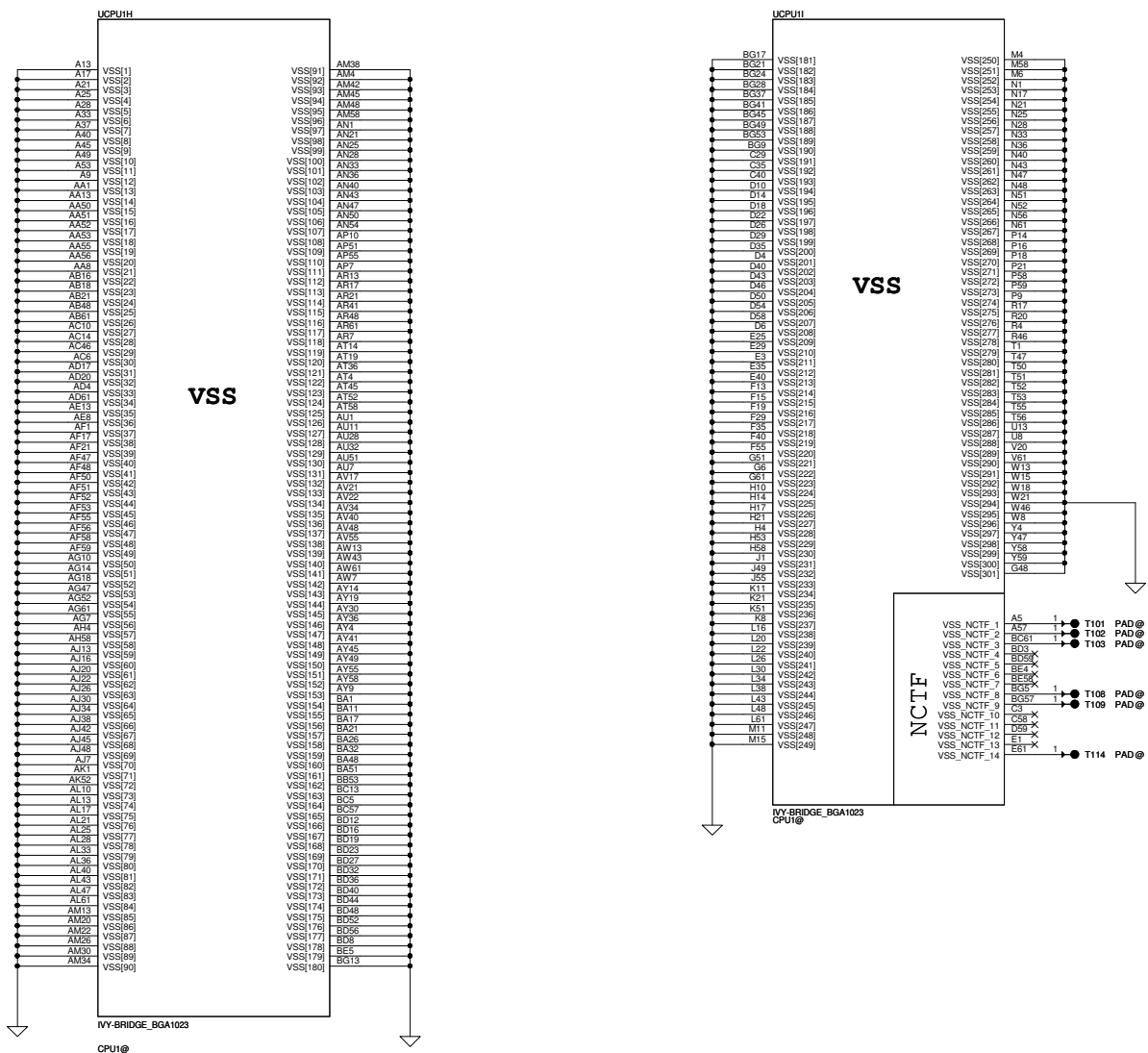
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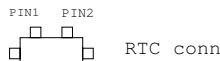
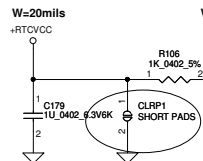
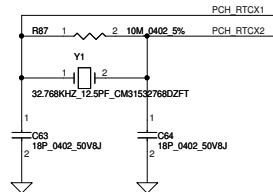


Vaxg

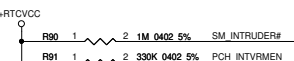
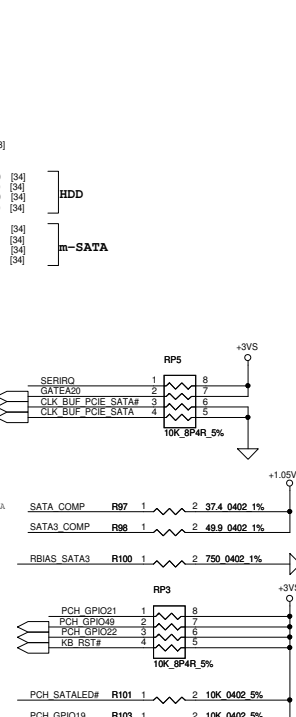
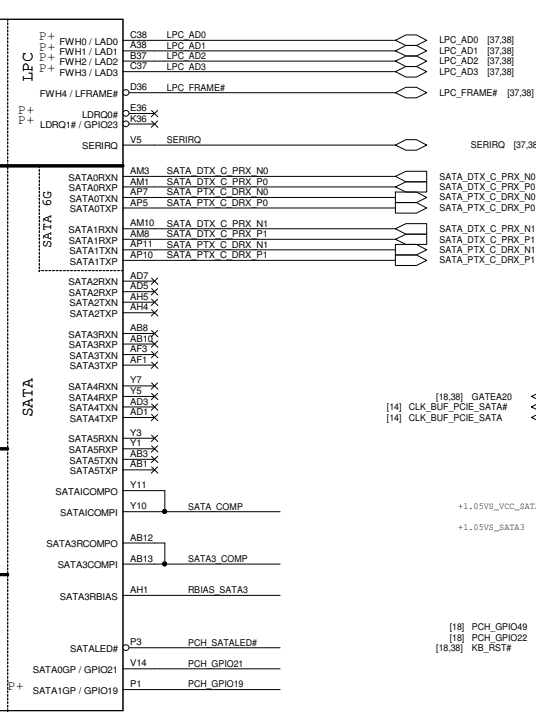
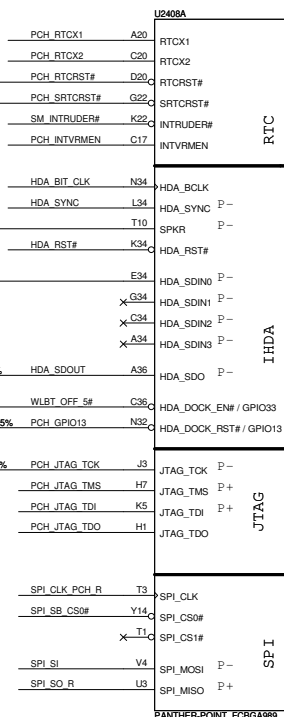
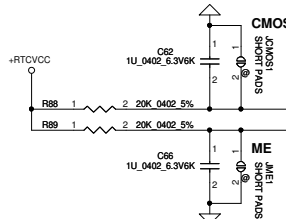
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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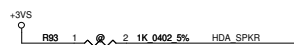




CLR1P1, JCMOS1, JME1 place near the door



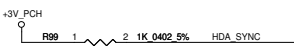
INTVRMEN
 ★ H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



HIGH= Enable (No Reboot)
 ★ **LOW= Disable (Default)**



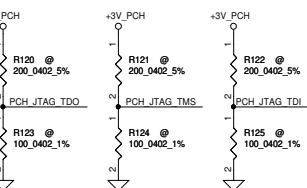
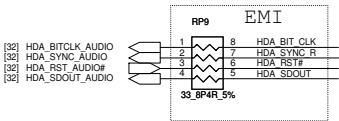
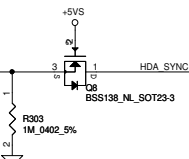
HDA_SDO
 ME debug mode this signal has a weak internal PD
 Low = Disabled (Default)
 High = Enabled [Flash Descriptor Security Override]



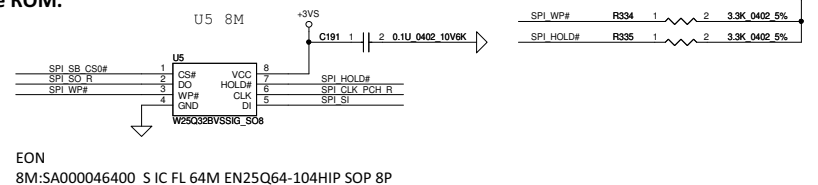
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
 ★ 1.5V when sampled high
 Needs to be pulled High for Huron River platform

Prevent back drive issue.



**8MB SPI ROM FOR 1.5M ME
 & Non-share ROM.**



EON
 8M:SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P

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Card Reader

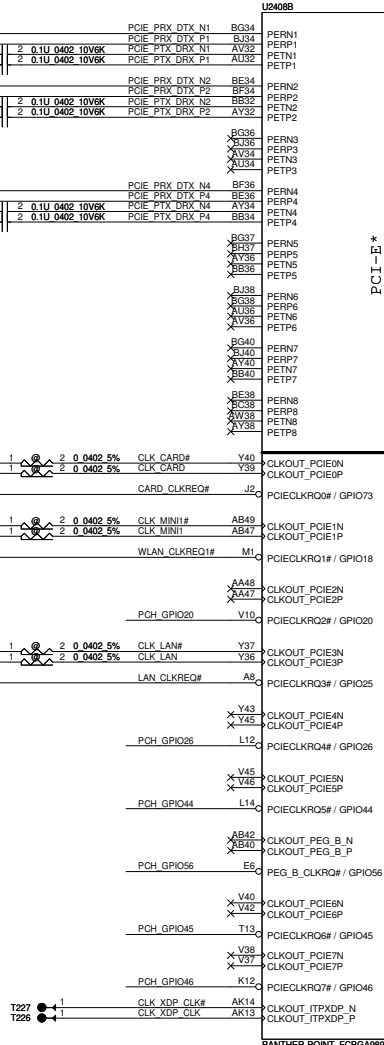
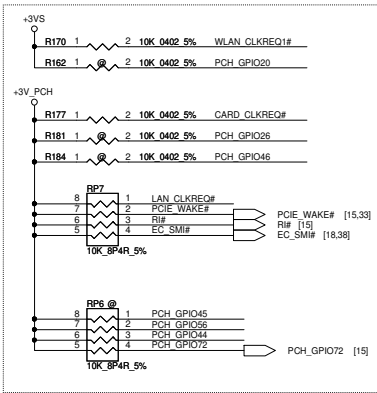
Wireless LAN

PCIE LAN

Card Reader

Wireless LAN

PCIE LAN



PCI-E *

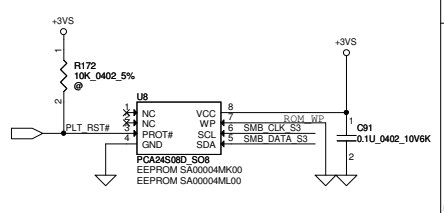
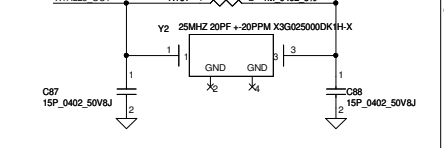
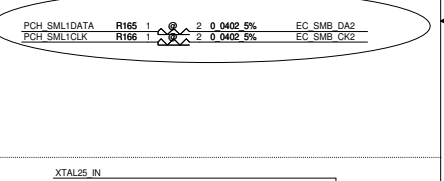
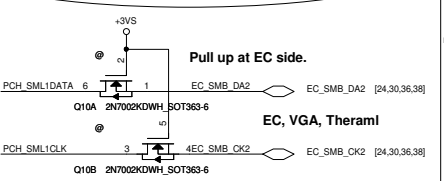
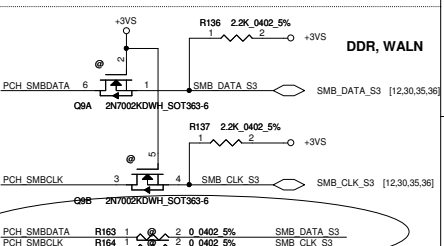
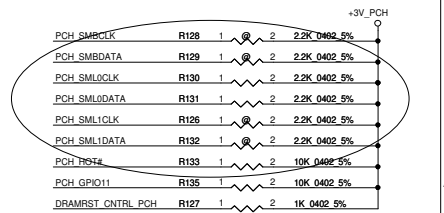
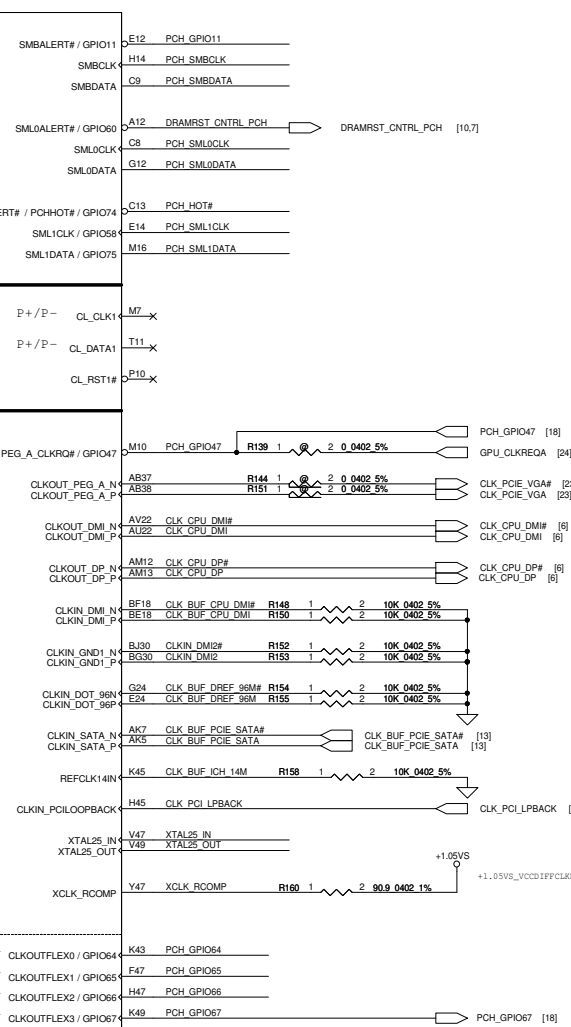
CLOCKS

PLT_FLEX

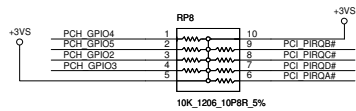
Controller Link

CLOCKS

PLT_FLEX



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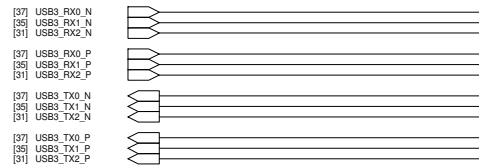
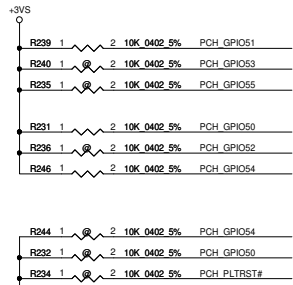


GNT0#, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55
PCI Grants: The PCH supports up to 4 masters on the PCI bus.

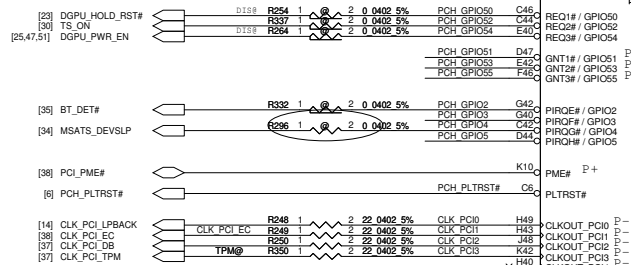
GNT[3:1]# pins can instead be used as GPIO.
Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.

NOTES:

1. GNT[3:1]#/GPIO[55,53,51] are sampled as a functional strap. See Section 2.27 for details.

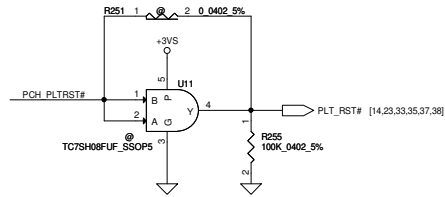


GPIO50 /52 /54 default = Native



Boot BIOS Strap bit1 BBS1		
GPIO51 GPIO19	Boot BIOS	Destination
Bit11 Bit10		
0 1		Reserved
1 0		PCI
1 1	*	SPI (Default)
0 0		LPC

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

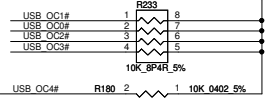


USB 3.0 (I/O Board)
USB 3.0 (MB)
USB 3.0 (Docking)
CMOS Camera (LVDS)

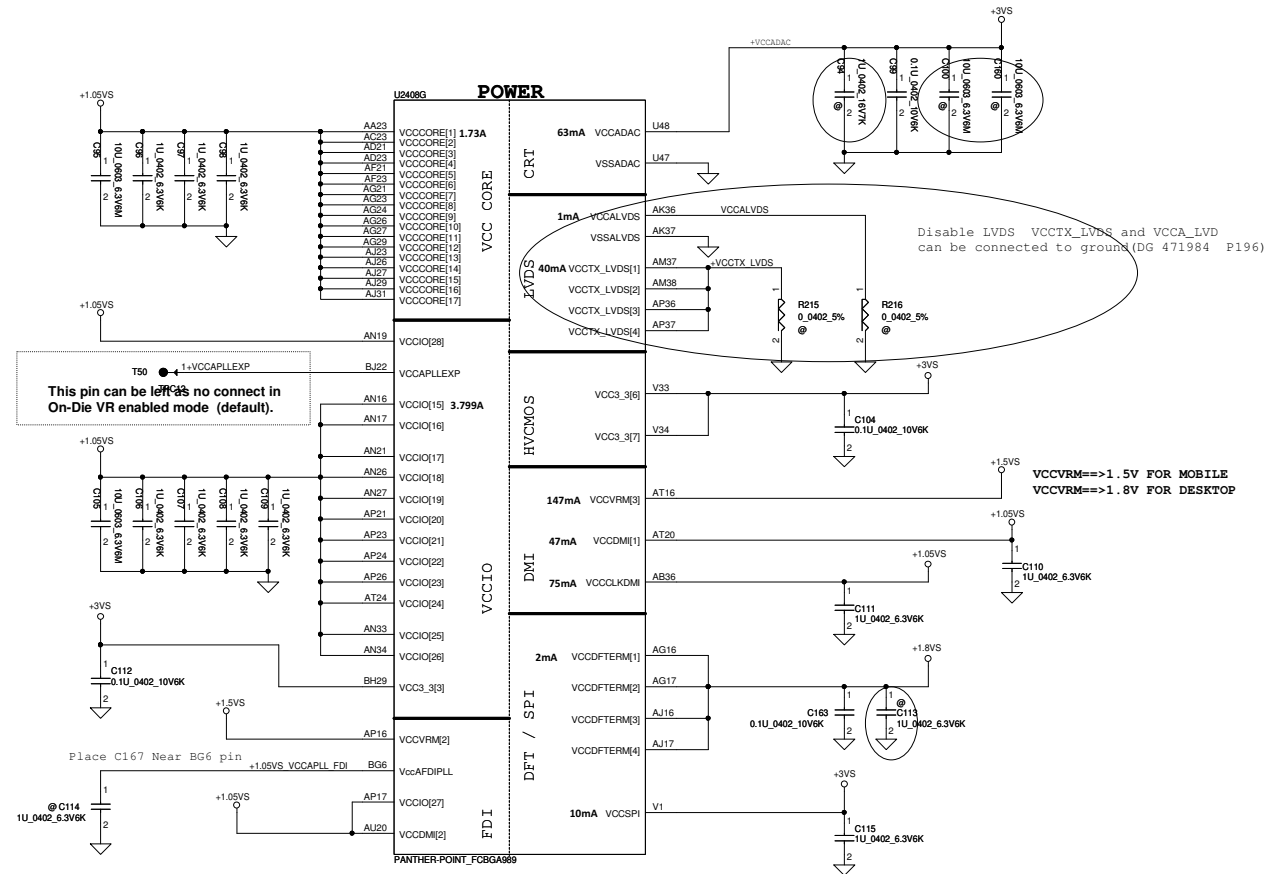
Touch panel
(Test Point for BIOS Debug)
Mini Card(WLAN/BT)
FingerPrint

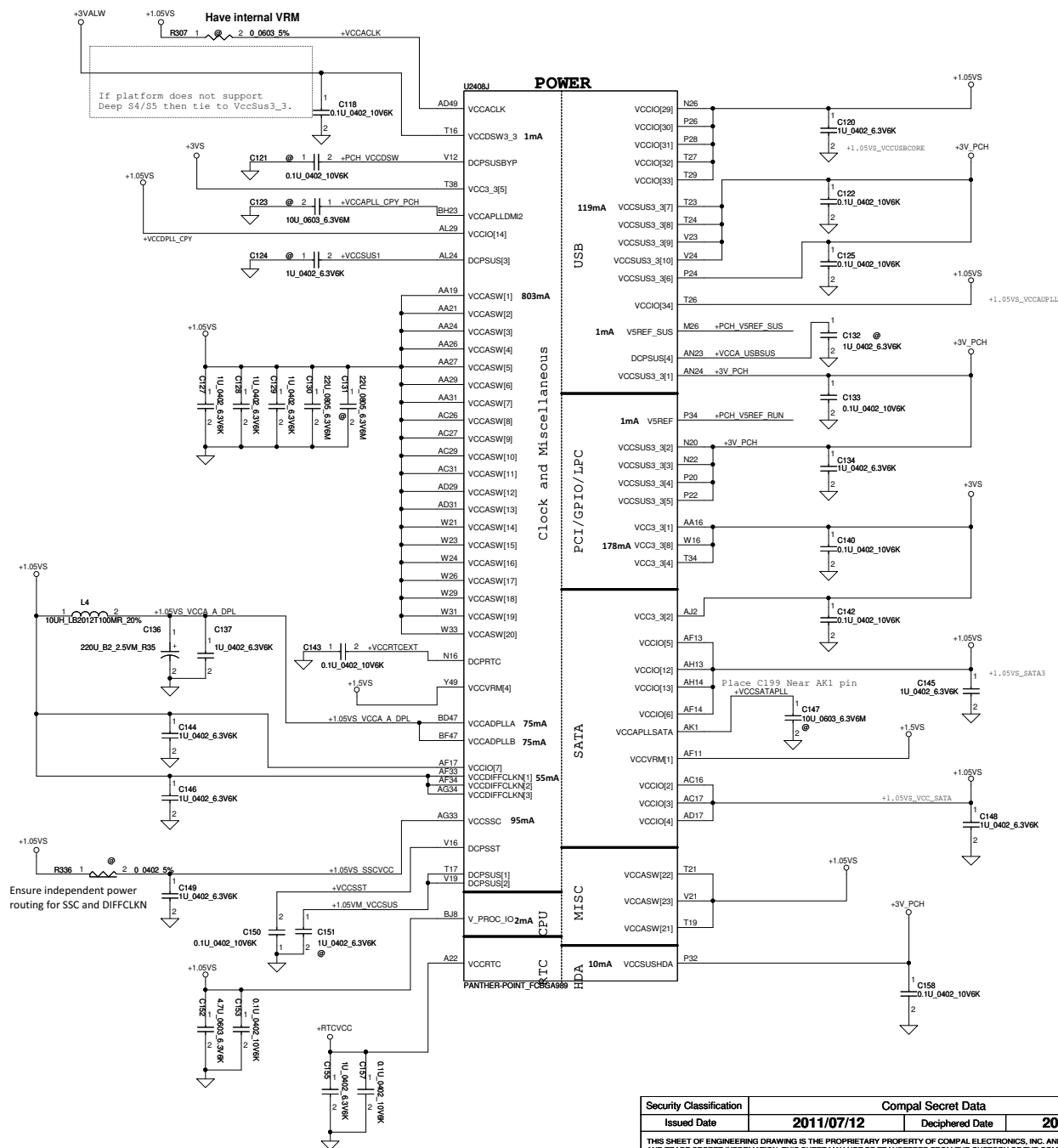
Within 500 mils
OC0# USB 3.0 (I/O Board) (MB)

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

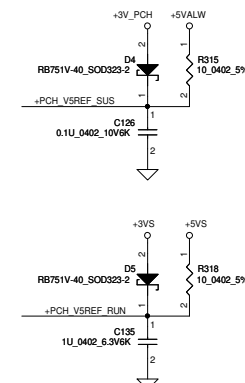


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				LA-9611P	
				Date: Wednesday, February 27, 2013	Sheet 17 of 53

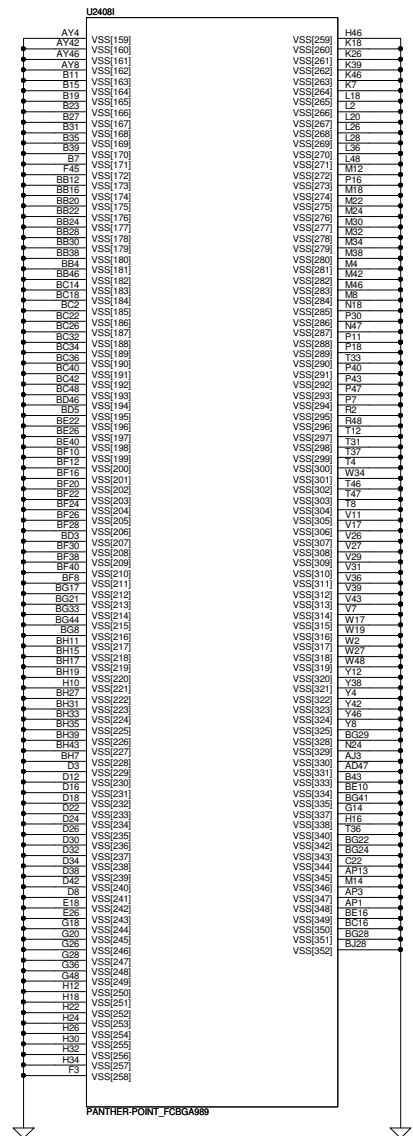
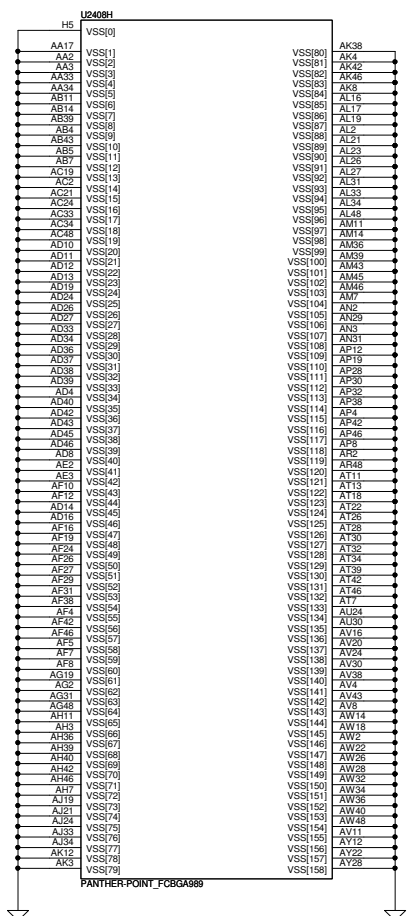




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VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec
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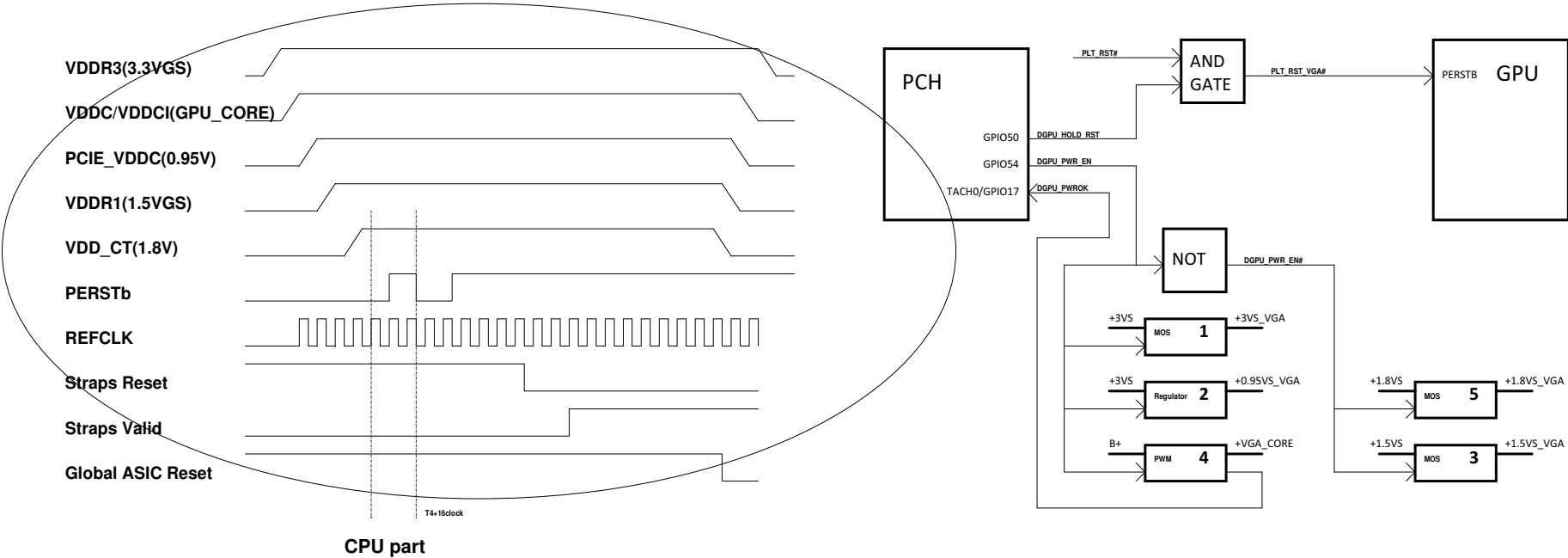


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						Size	Document Number		Rev
						Custom	LA-9611P		0.
						Date:	Tuesday, February 26, 2013	Sheet	20 of 53



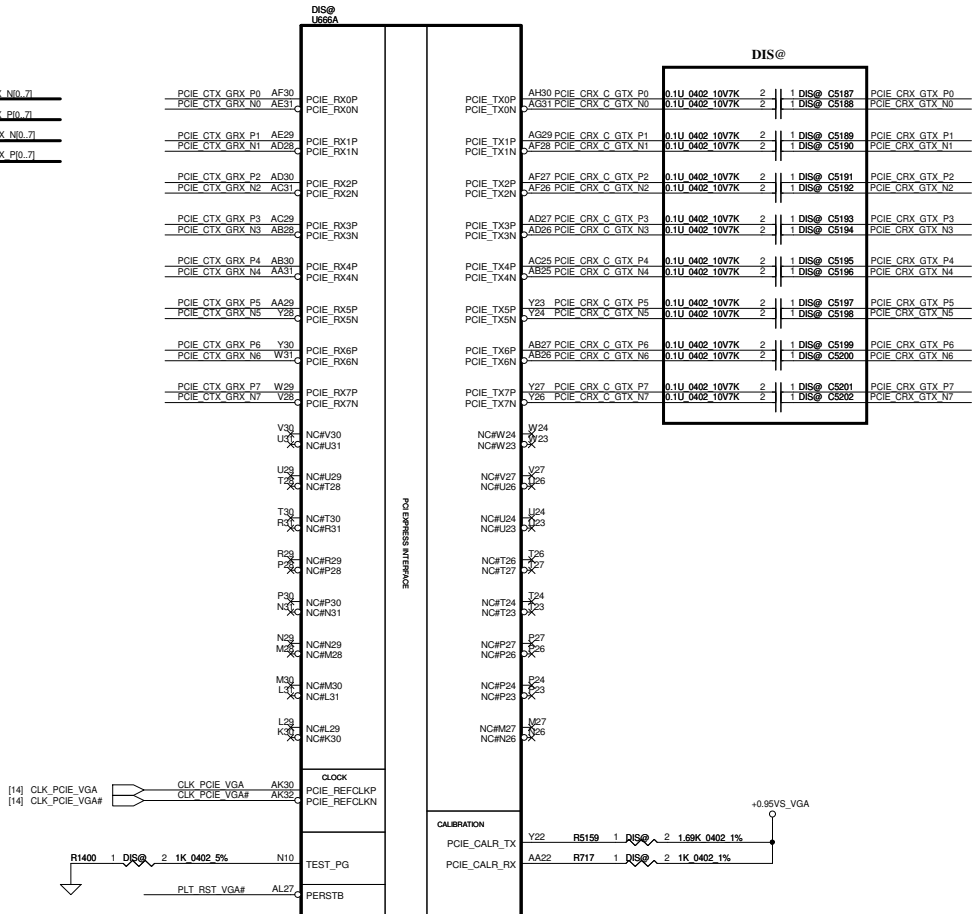
Power-Up/Down Sequence

- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- 2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- 3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- 4. For power down, reversing the ramp-up sequence is recommended.

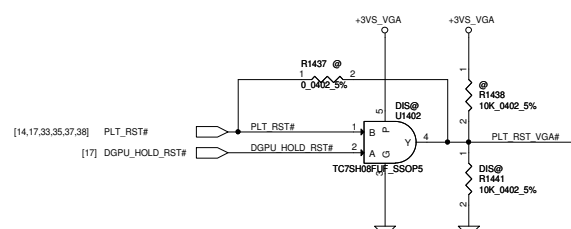
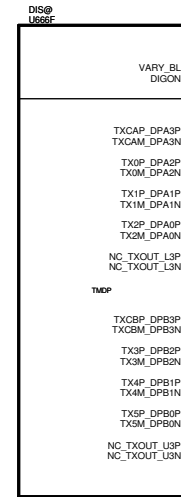


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				Date:	Tuesday, February 26, 2013
				Sheet	22 of 53
				Rev	0.4

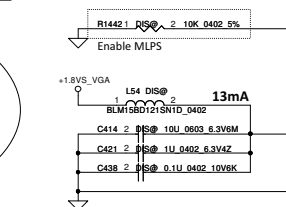
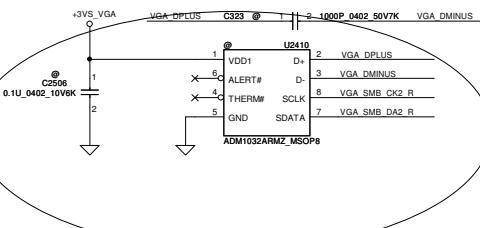
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[5] PCIE_CTX_GRX_P0..7) PCIE_CTX_GRX_P0..7)
[5] PCIE_CRX_GTX_N0..7) PCIE_CRX_GTX_N0..7)
[5] PCIE_CRX_GTX_P0..7) PCIE_CRX_GTX_P0..7)



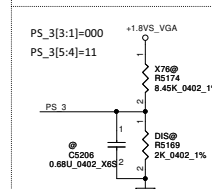
No Use GPU Display Port output



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				Rev	0.4
				Date	Tuesday, February 26, 2013
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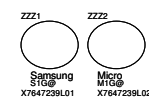


Cap (nF) CS206	Bitd [5:4]	Compal PN
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN
NC	11	



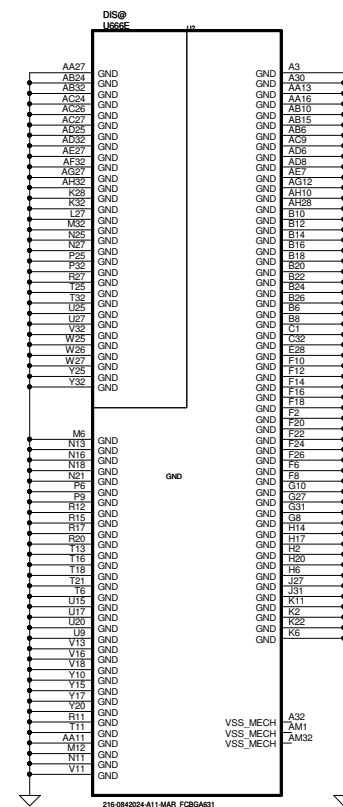
Memory ID	Memory Type	Configuration	Size
1	gDDR3-2133	Samsung K4W2G1646E-BC1A	2Gb X4 (256GBX4)
	SA000068U00 - 5 IC D3 128MX16 K4W2G1646E-BC1A FBGA 96P		
2	gDDR3-2000	Micro MT41J128M16JT-093G	2Gb X4 (256GBX4)
	SA000067500 - 5 IC D3 128M16 MT41J128M16JT-093G;K FBGA		

```
EX:
PS_3=11001 (PU=NC, PD=4.75K, C=NC) for Samsung 1GB
PS_3=11010 (PU=8.45K ,PD=2K, C=NC) for Micro 1GB
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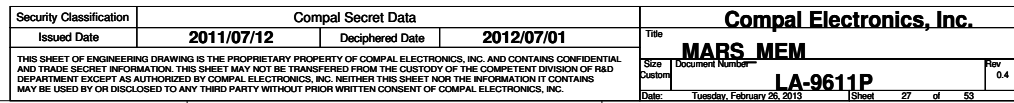


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Figure 1: Schematic diagram of the power supply circuit. The circuit shows a 10K 0.402 5% resistor (R1477) in series with a 0.1uF 100K capacitor (C159) connected to the SUSP# pin. A 10K 0.402 5% resistor (R1478) is connected to the DGPU_PWR_EN pin. A 10K 0.402 5% resistor (R1480) is connected to the 2N7002K_SOT23-3 MOSFET gate. A 10K 0.402 5% resistor (R1479) is connected to the DGPU_PWR_EN pin. The MOSFET is driven by a 2N7002K_SOT23-3 MOSFET. The output is connected to a 10K 0.402 5% resistor (R1479) and a 0.1uF 100K capacitor (C159).

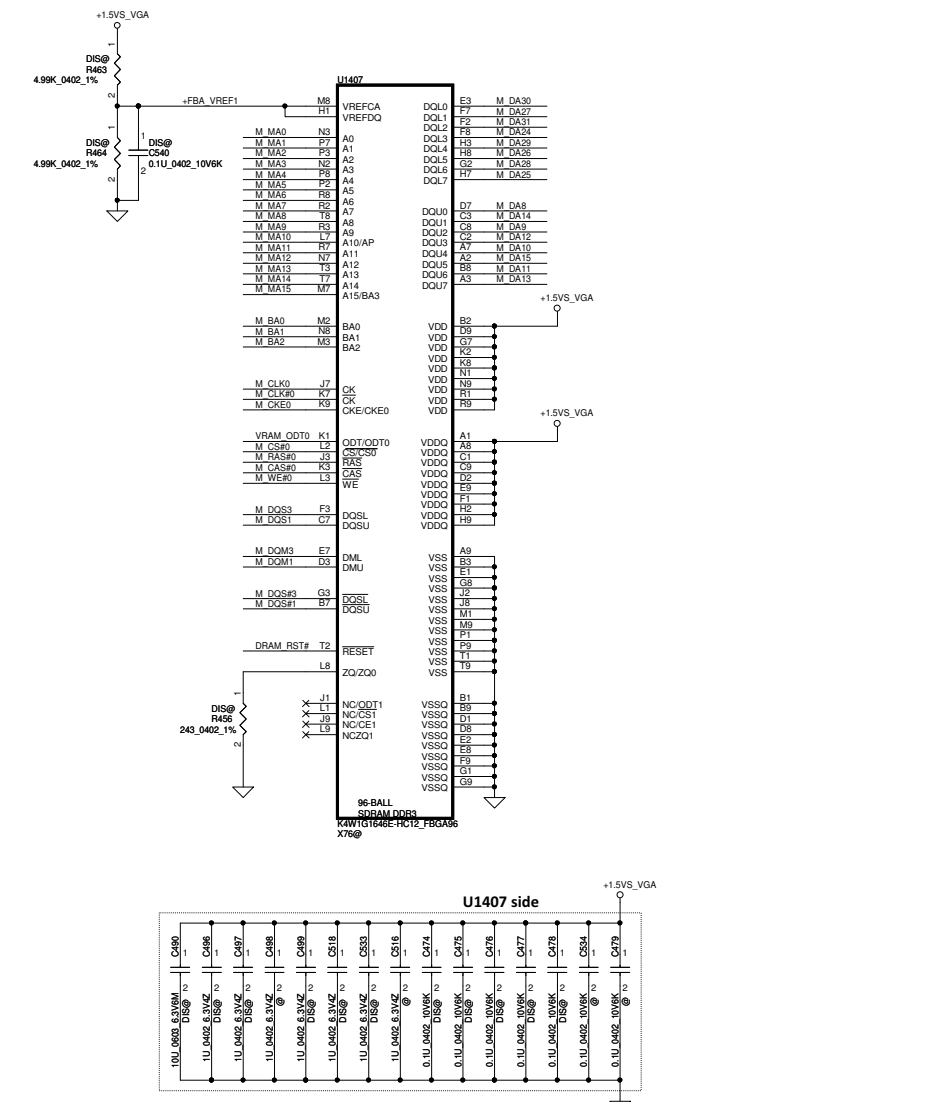
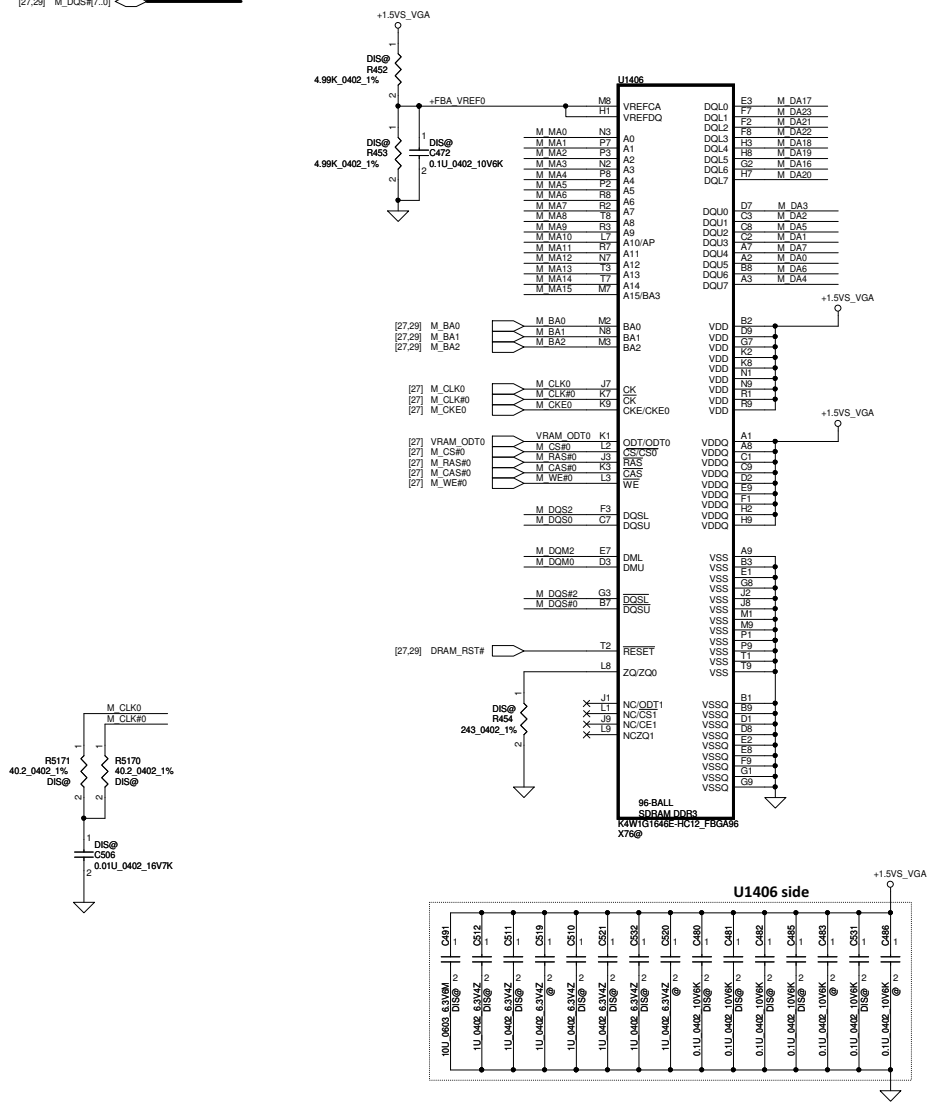


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				Drawn Checked Date: Tuesday, February 26, 2013	
				Document Number LA-9611P	Rev 04
				Sheet 25	of 53

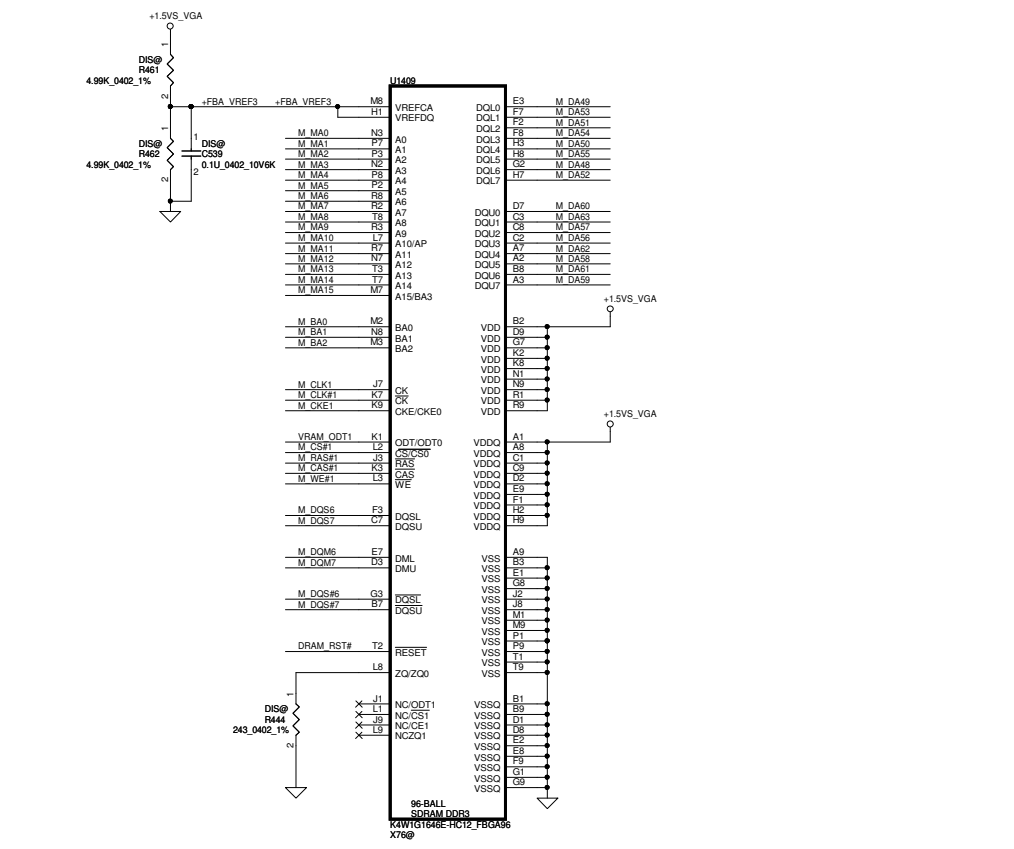
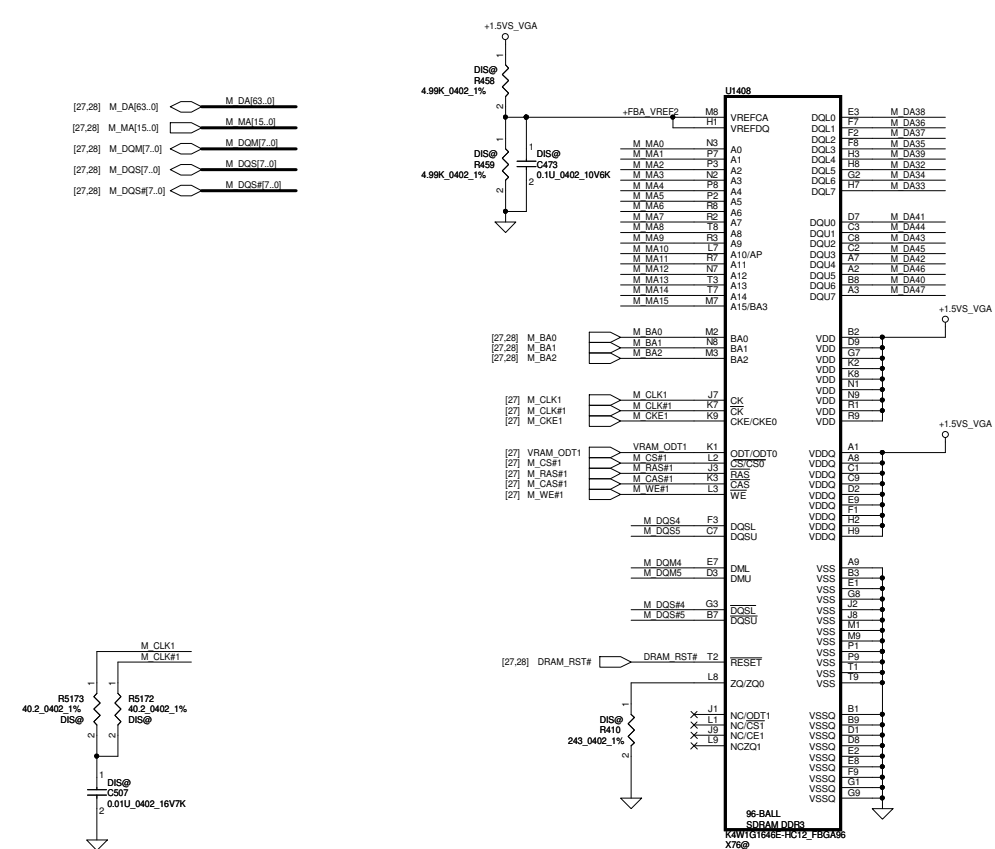


Memory Partition A - Lower 32 bits

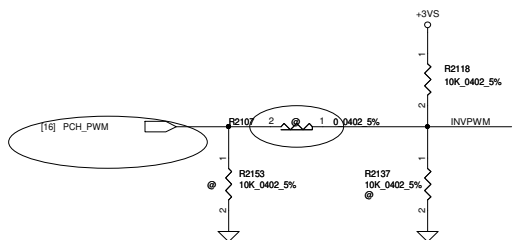
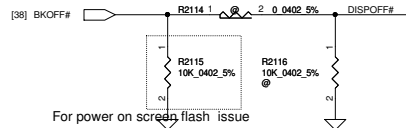
- [27.29] M_DA[63..0] M_DA[63..0]
- [27.29] M_MA[15..0] M_MA[15..0]
- [27.29] M_DQM[7..0] M_DQM[7..0]
- [27.29] M_DQS[7..0] M_DQS[7..0]
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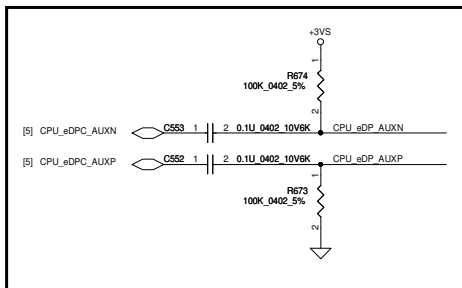
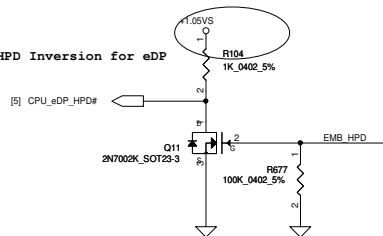
Memory Partition A - Upper 32 bits



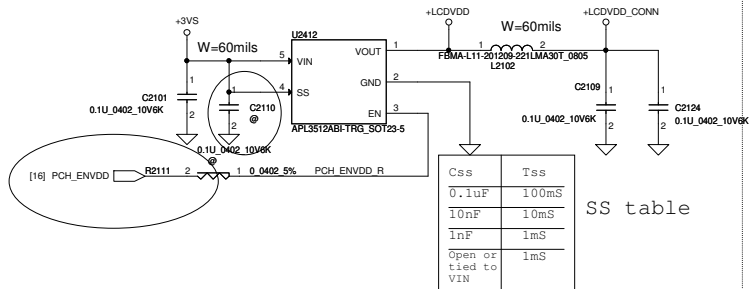
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				LA-9611P	
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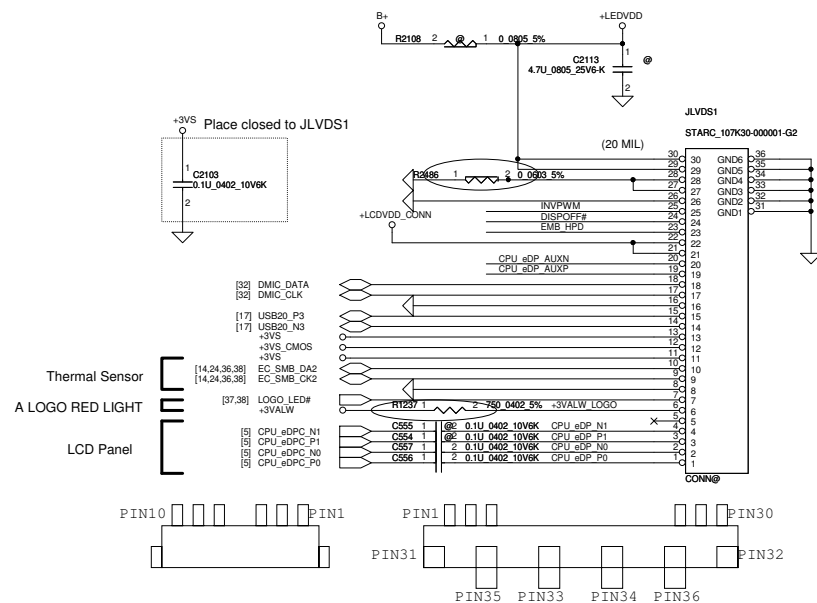
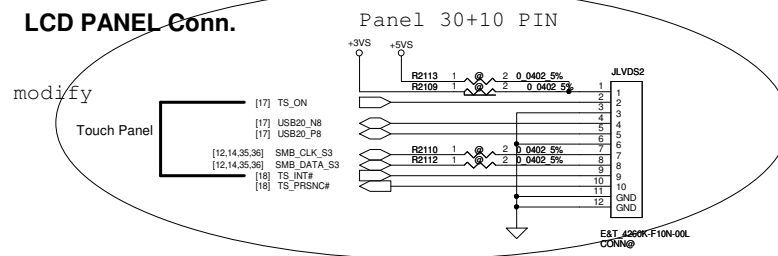
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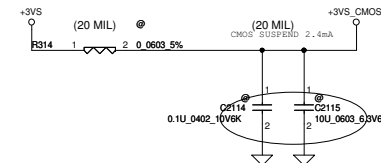
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LCD PANEL Conn.

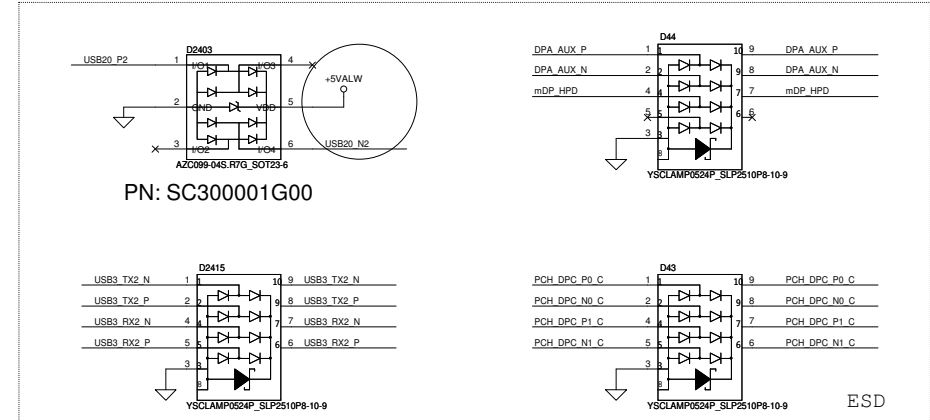


CMOS Camera Conn

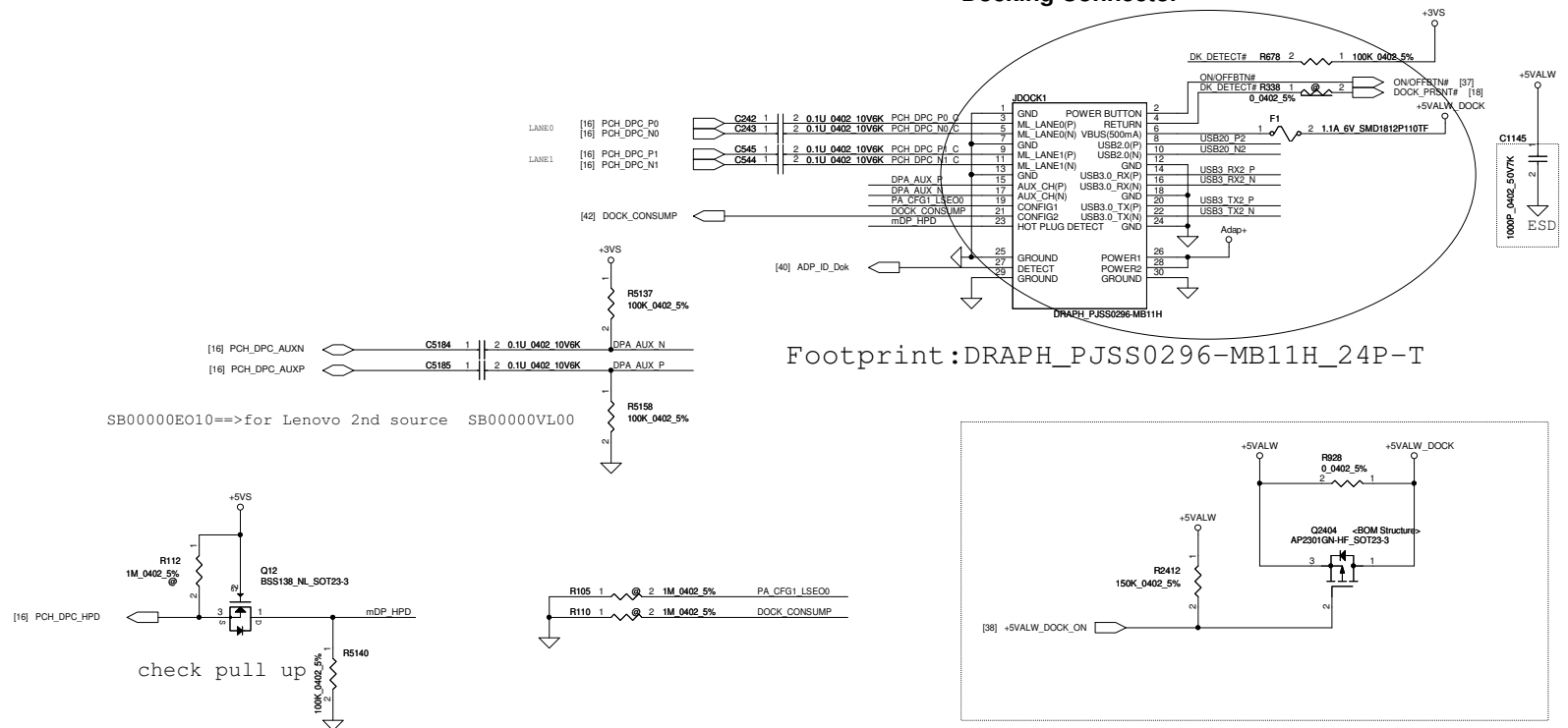


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		1						LA-9611P		Rev	
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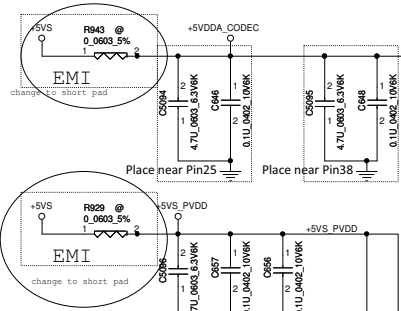
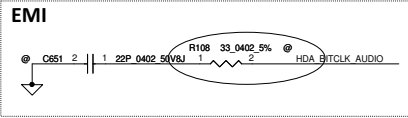
Docking (USB3.0)



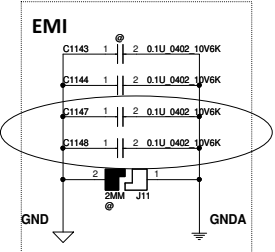
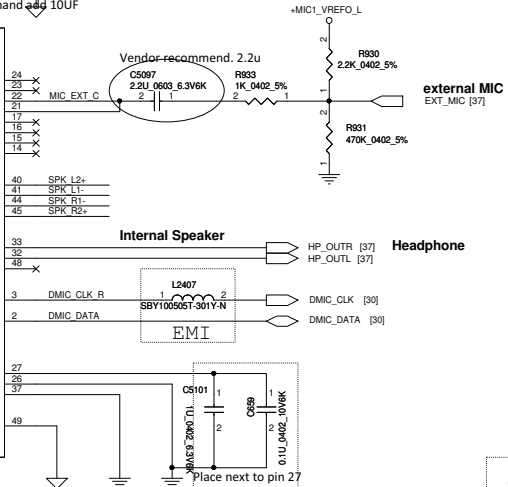
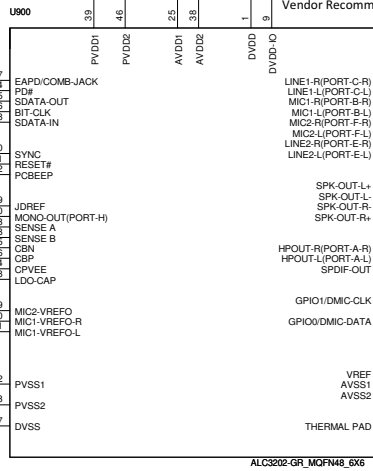
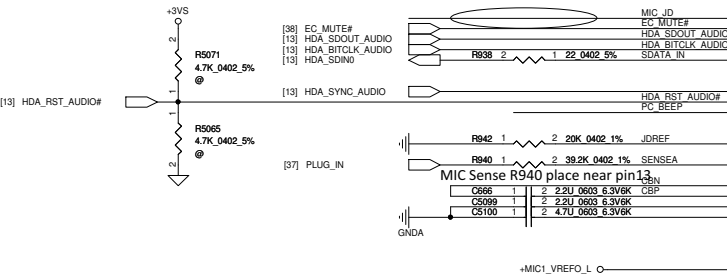
Docking (Display Port)



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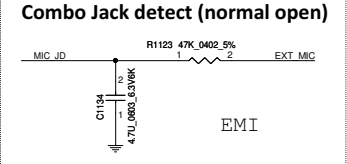


Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

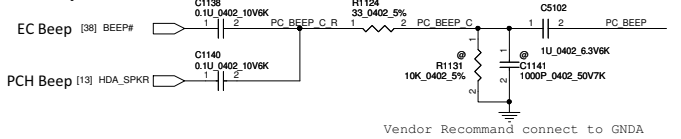


ALC3202 VC3
SA000058310

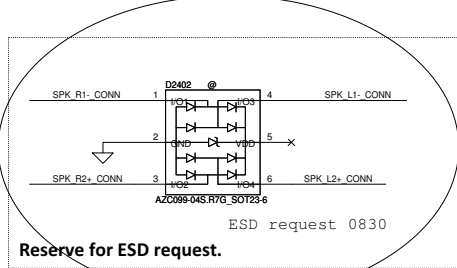
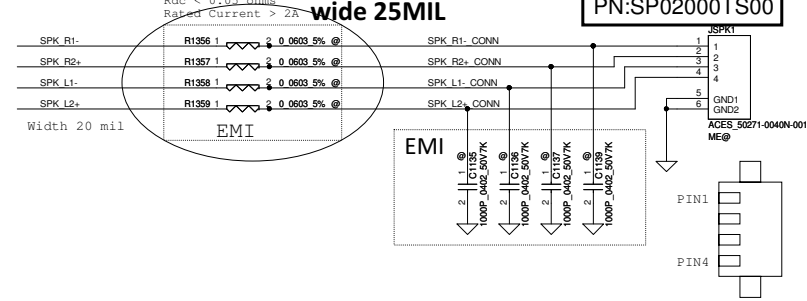
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in



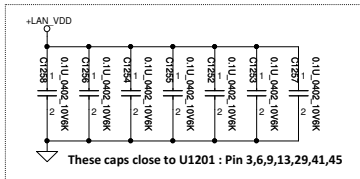
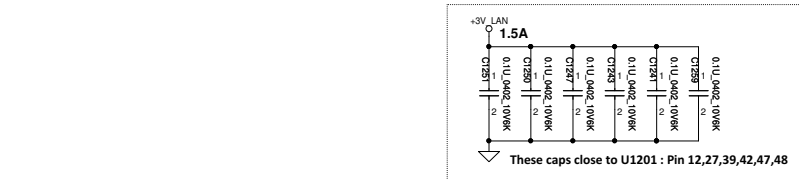
PC BEEP



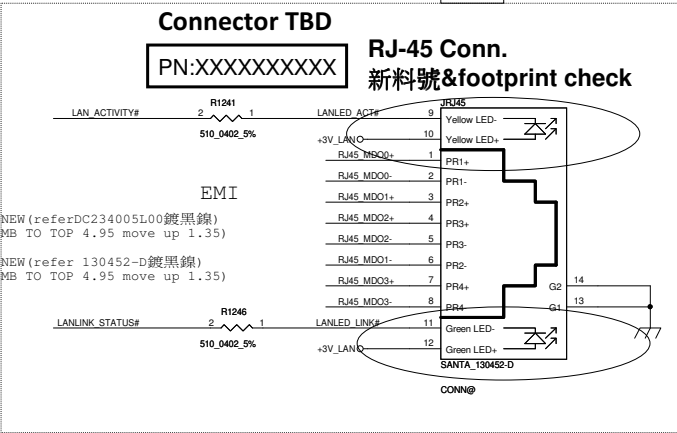
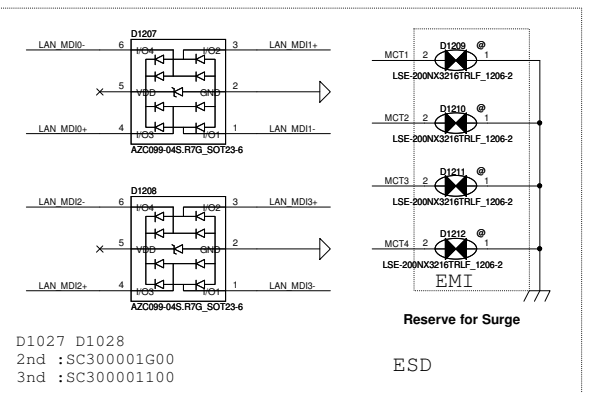
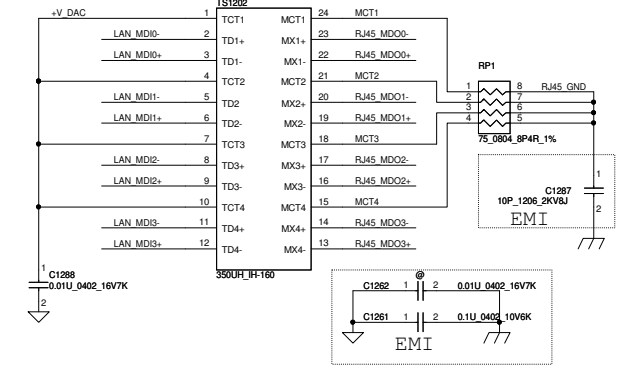
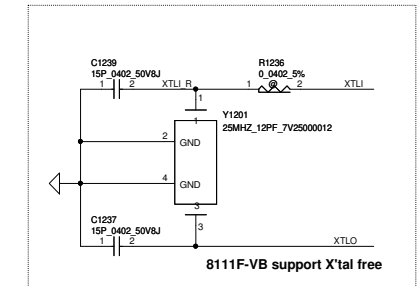
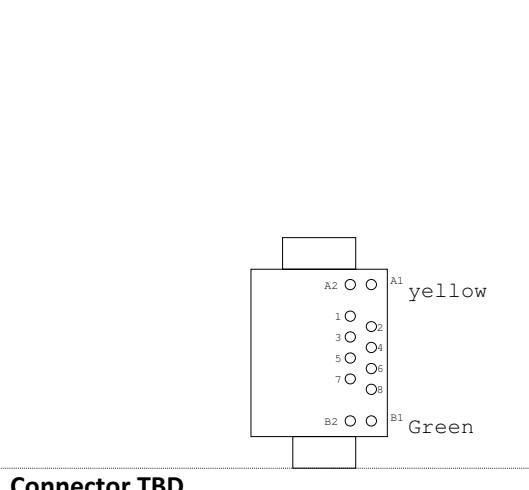
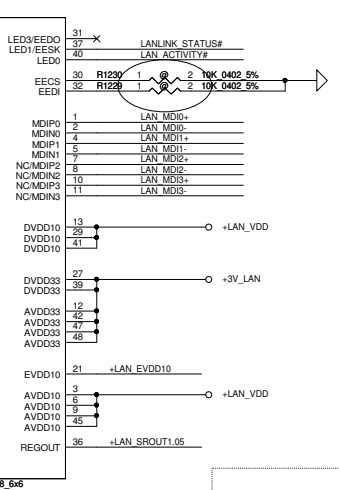
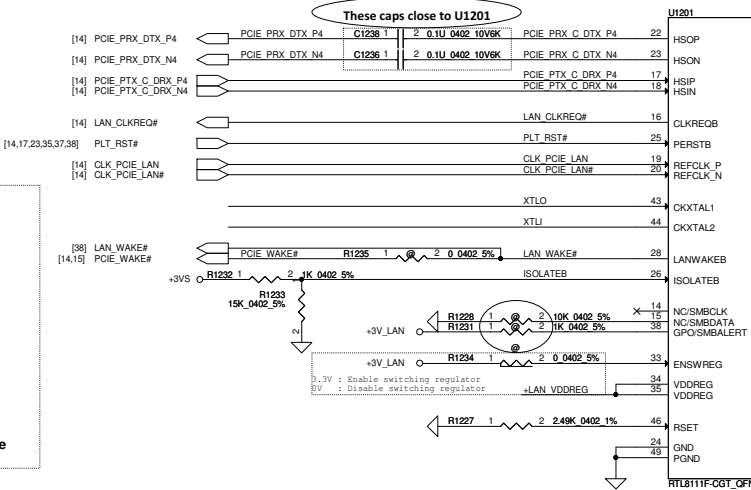
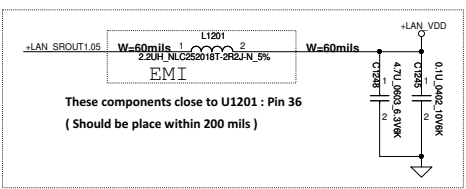
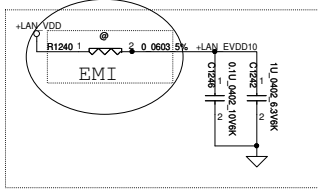
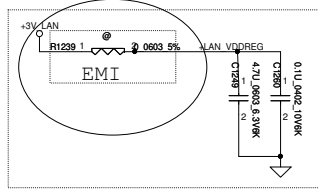
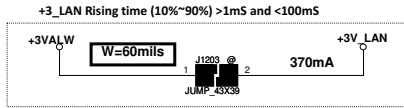
Internal Speaker



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Deciphered Date	2012/07/01	2012/07/01
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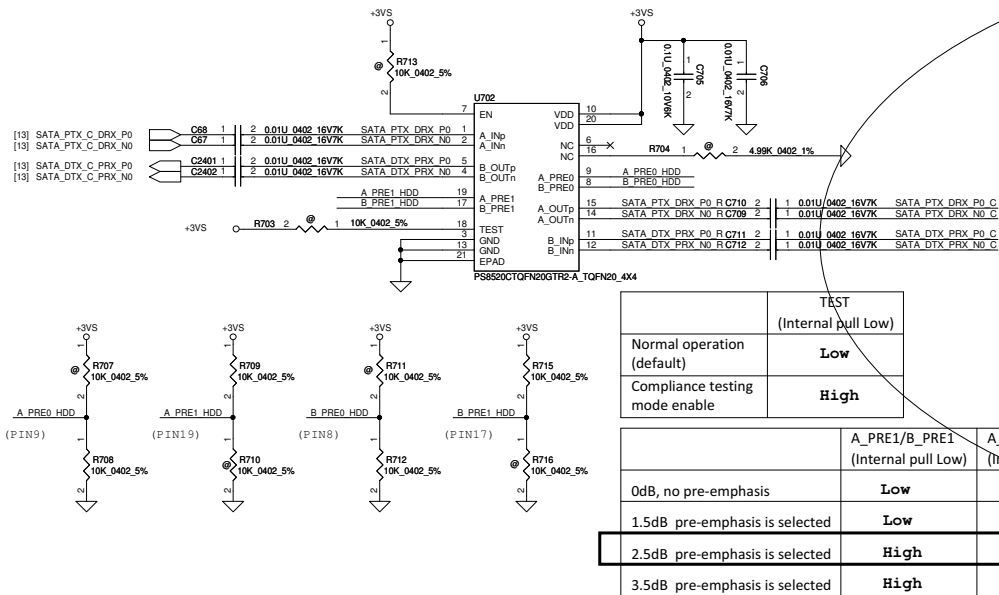


The BRD need check +3V_LAN, +LAN_VDD Capacitor placement

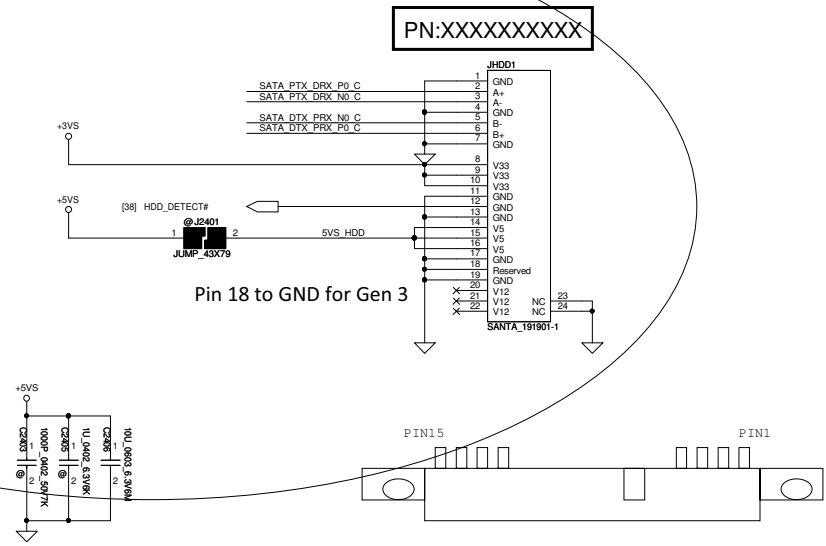


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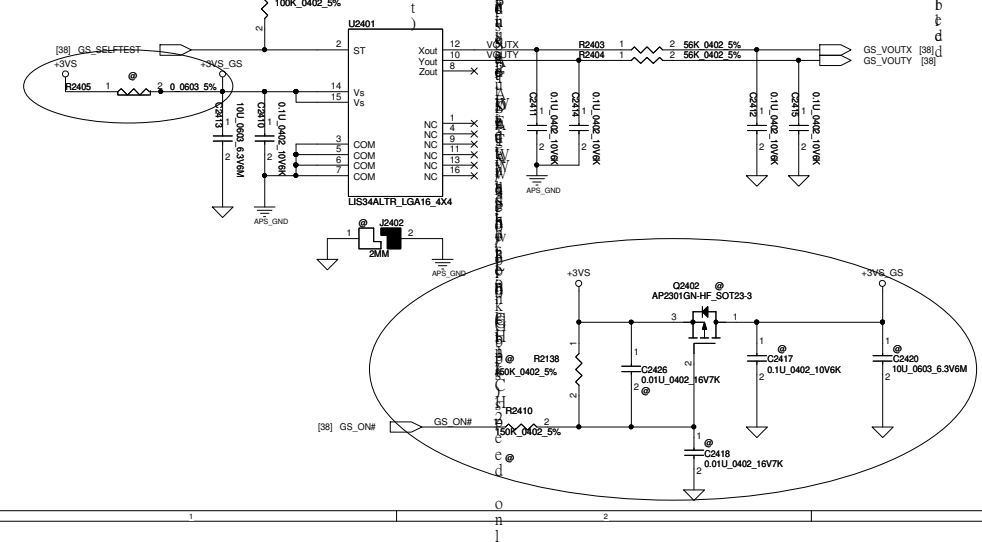
SATA HDD BTB CONN.



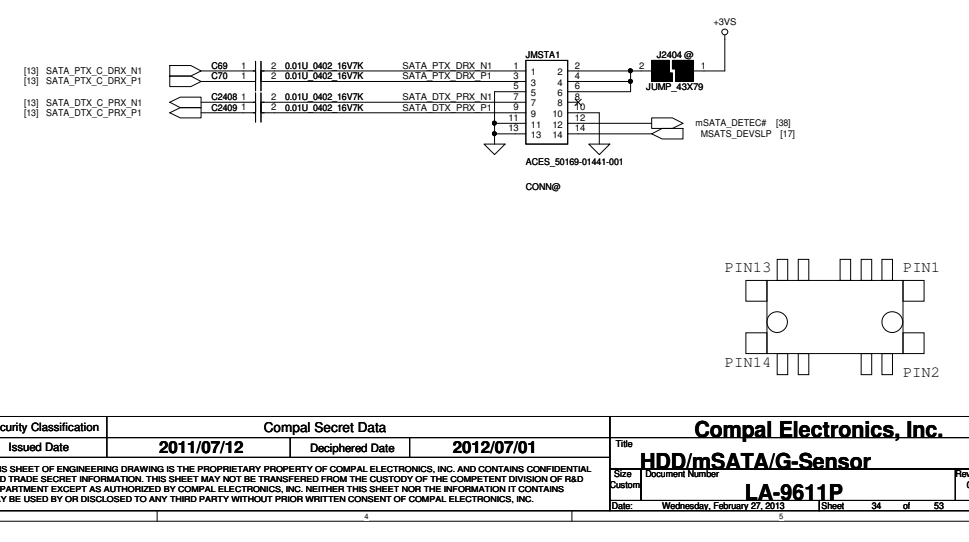
SATA HDD CONN.



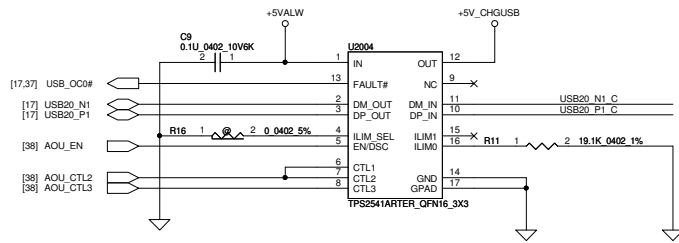
APS G-Sensor



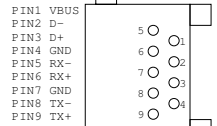
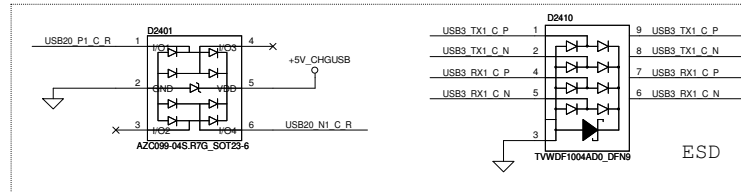
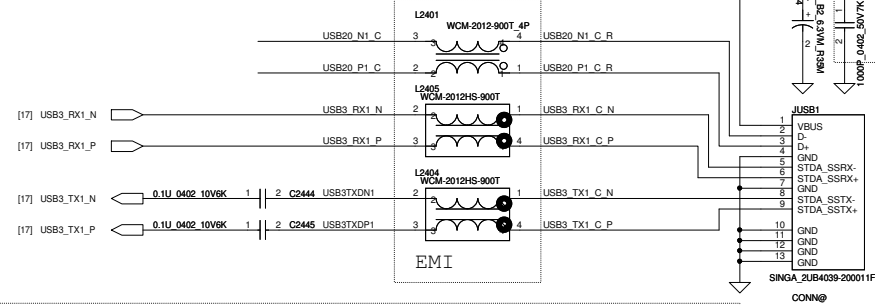
mSATA CONN.



USB 3.0 Charger & Conn.

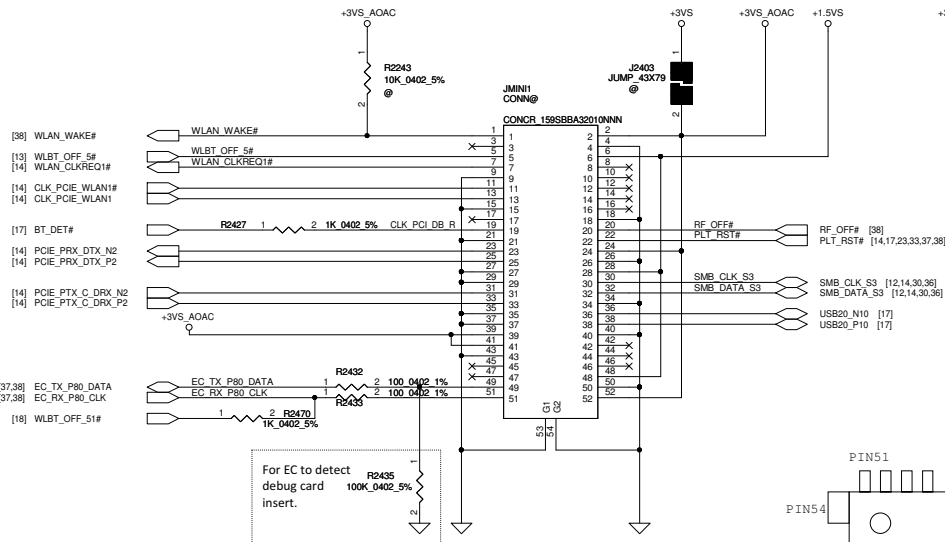


Superworld's common mode choke(SM070001V00) has quality issue for USB 3.0



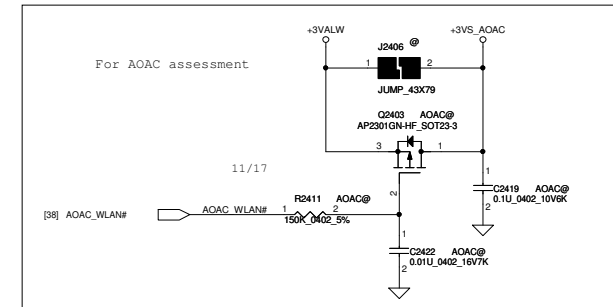
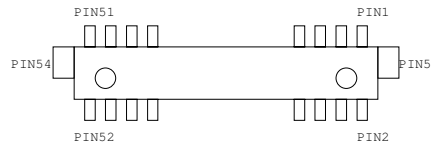
Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



For EC to detect debug card insert.

NEW(apply compal PN)
159SBA32010NNN

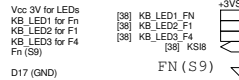


Need check WLAN/BT module OFF pin

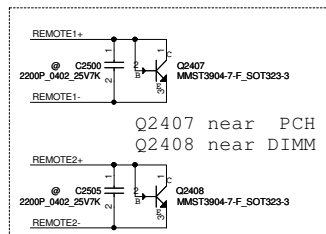
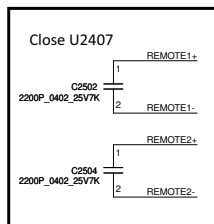
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Date: Tuesday, February 26, 2013				Sheet	35 of 53

KSII[0..7] KSII[0..7] [38]

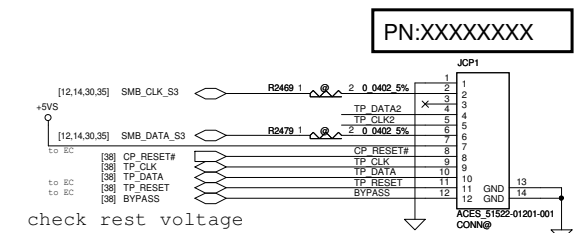
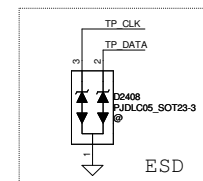
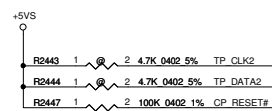
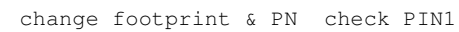
KSO[0..17] KSO[0..17] [38]



2nd source
SA000029210-->EMC1403-2-AIZL-TR

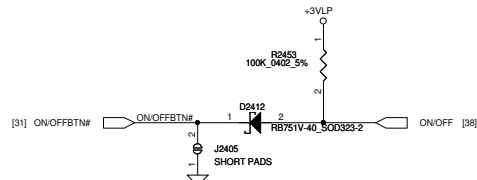


Track point

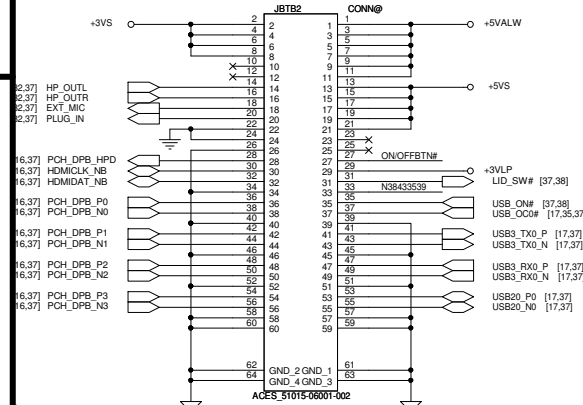


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Power Button



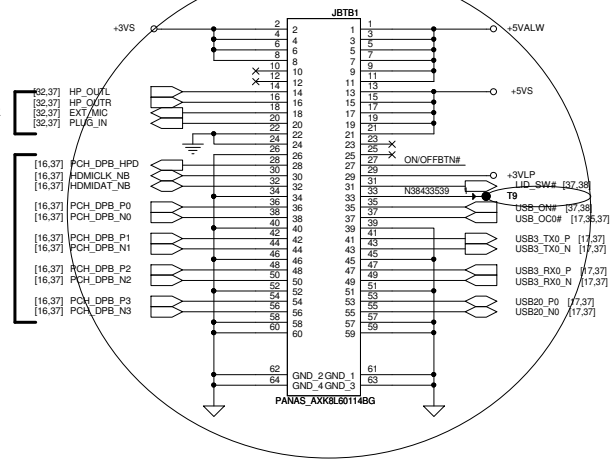
I/O Board CONN.



Audio combo Jack

HDMI

Connector: 0.3A / pin



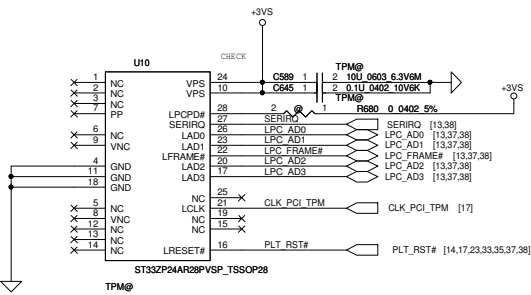
Power Button
Lid Switch & LED

to EC

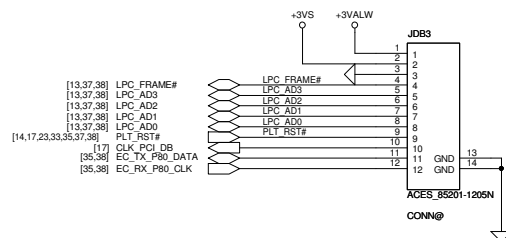
USB3.0

ESD request 0827

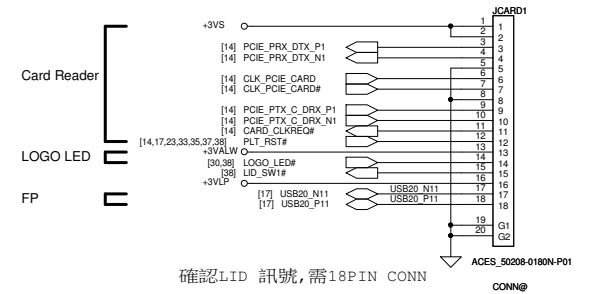
TPM



Debug Conn.



Card Reader CONN.



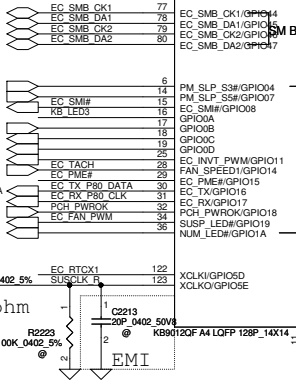
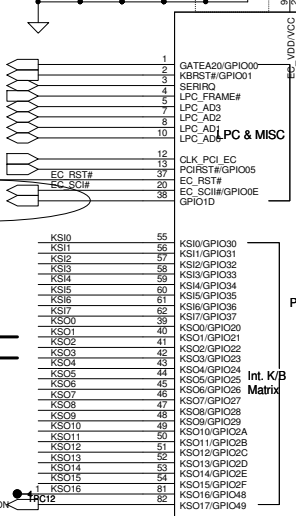
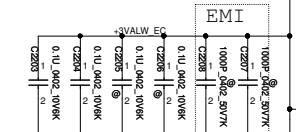
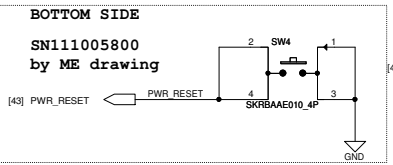
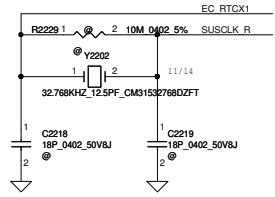
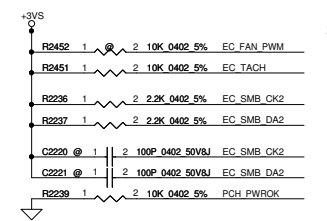
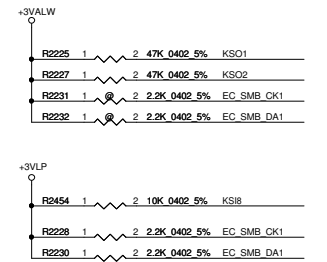
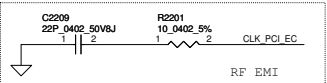
確認LID 訊號, 需18PIN CONN

ACES_50208-0180N-P01

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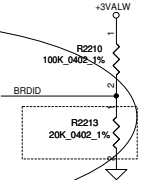
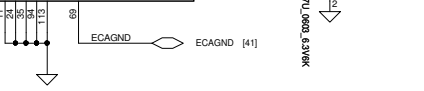
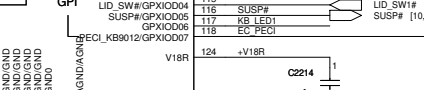
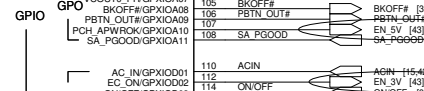
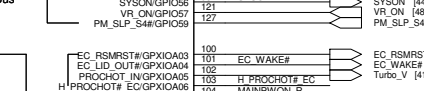
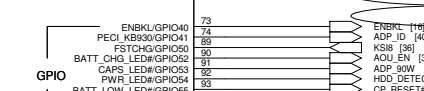
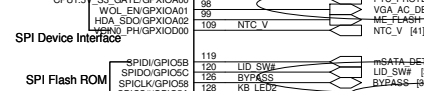
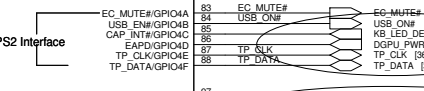
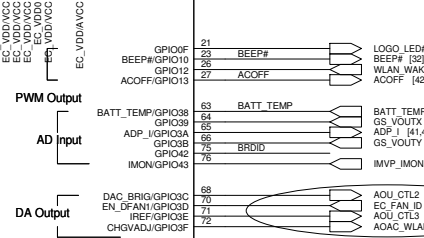
Can't internal pull up

GPIO44
GPIO45
GPIO46
GPIO47
GPIO4A
GPIO4B
GPIO4E
GPIO4F
GPIO50
GPIO5B

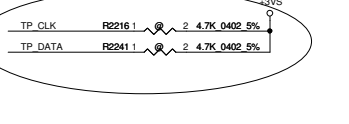
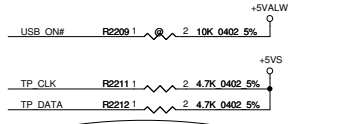
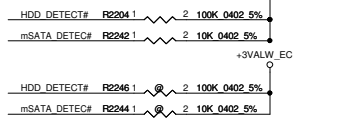
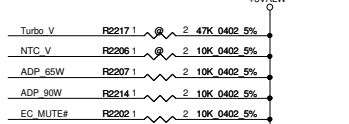
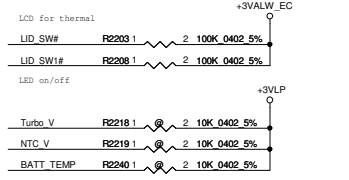


SD034120280 S RES 1/16W 12K +-1% 0402
SD034150280 S RES 1/16W 15K +-1% 0402
SD034200280 S RES 1/16W 20K +-1% 0402
SD034270280 S RES 1/16W 27K +-1% 0402
SD034330280 S RES 1/16W 33K +-1% 0402

EC 要求須改為1%



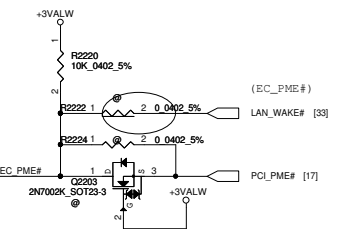
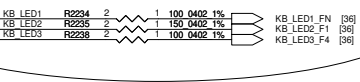
Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	12K +/- 5%	0.347 V	0.354 V	0.360 V	FVT
2	15K +/- 5%	0.423 V	0.430 V	0.438 V	SIT
3	20K +/- 5%	0.541 V	0.550 V	0.559 V	SVT
4	27K +/- 5%	0.691 V	0.702 V	0.713 V	
5	33K +/- 5%	0.807 V	0.819 V	0.831 V	



for 5 button

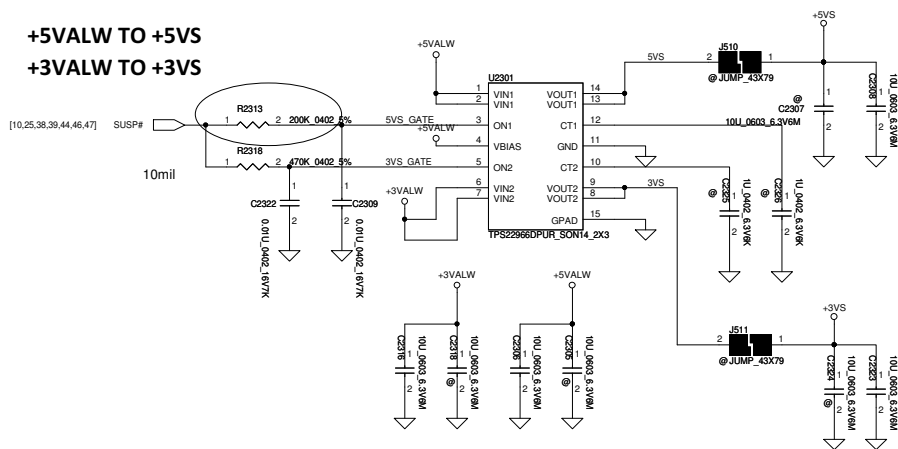
LCD on/off

add resistor

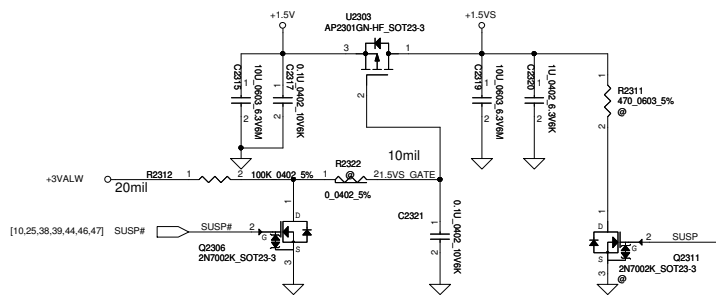


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+5VALW TO +5VS +3VALW TO +3VS

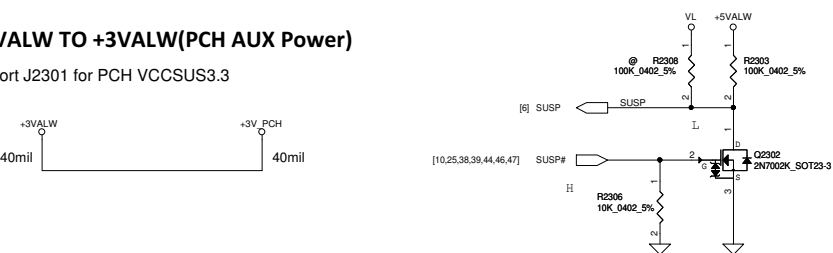


+1.5V to +1.5VS

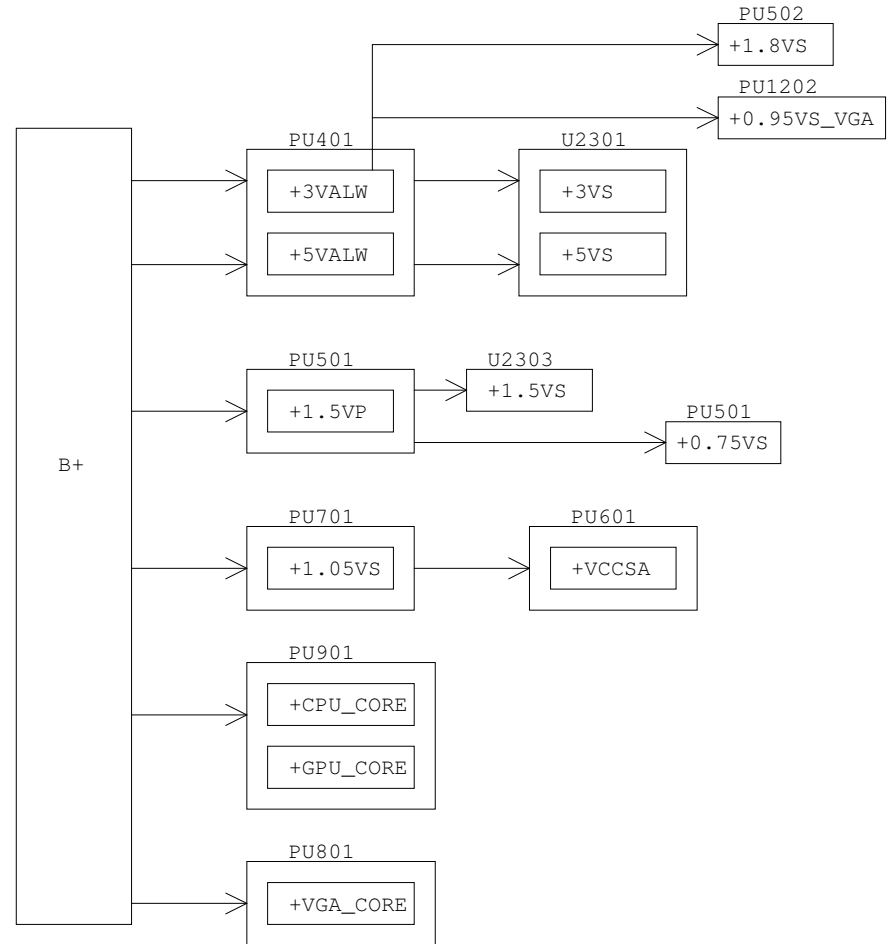
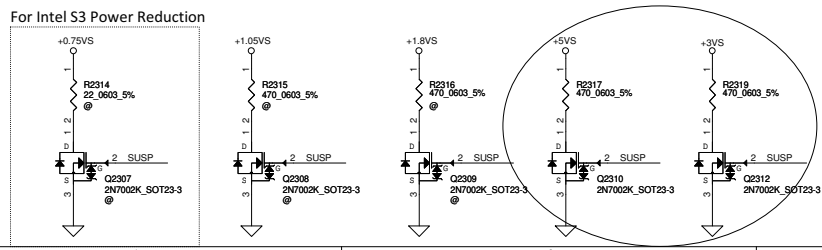


+3VALW TO +3VALW(PCH AUX Power)

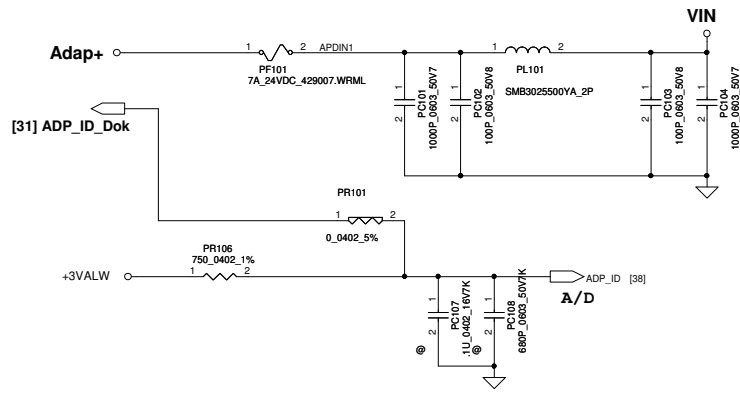
Short J2301 for PCH VCCSUS3.3



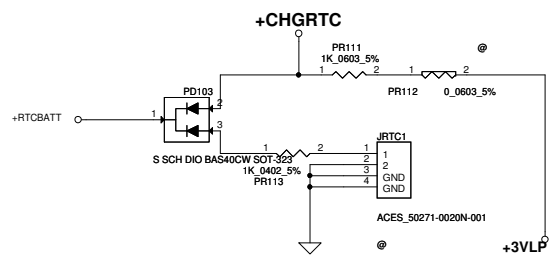
For Intel S3 Power Reduction

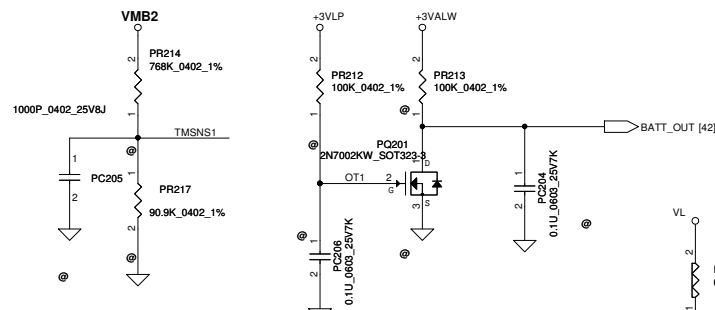
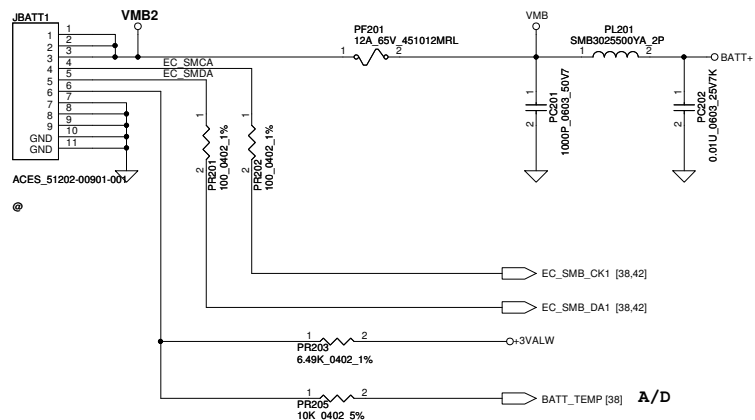


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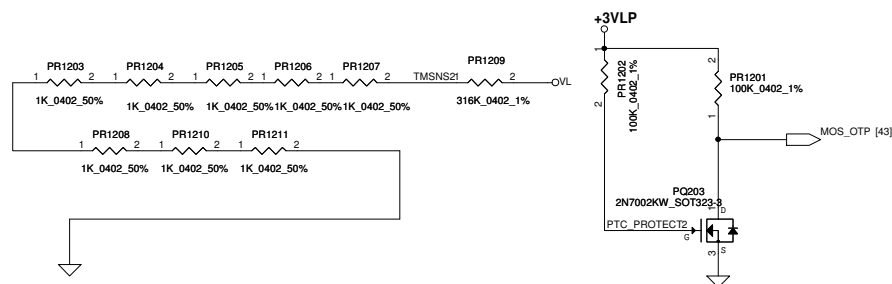


ADP_ID				
AC Adapter	45W	65W	90W	135W
R(ohm)	118	287	549	1000
ADP_ID(V)	0.449	0.913	1.395	1.886
Detection	<=0.663,			
-Voltage(V)	>0.234			





Posestor



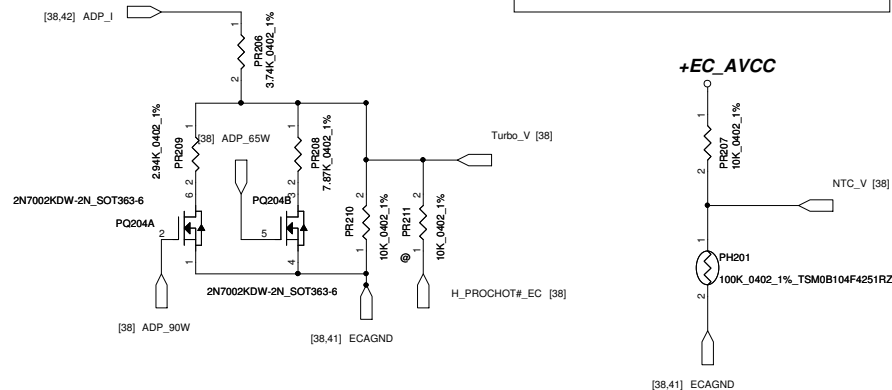
Resistance between Turbo_V and ECAGND:

45 W: 10K (Default)
 65 W: 4.4K (ADP_65W to High, ADP_90W to Low)
 90 W: 2.27K (ADP_90W to High, ADP_65W to Low)

Trigger Power:

45 W → 55 W → ADP_I:1.65
 65 W → 74 W → ADP_I:2.22
 90 W → 106 W → ADP_I:3.18

PH201 under CPU bottom side :
 CPU thermal protection at 100 degree C



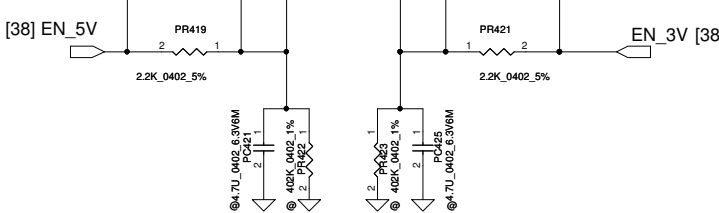
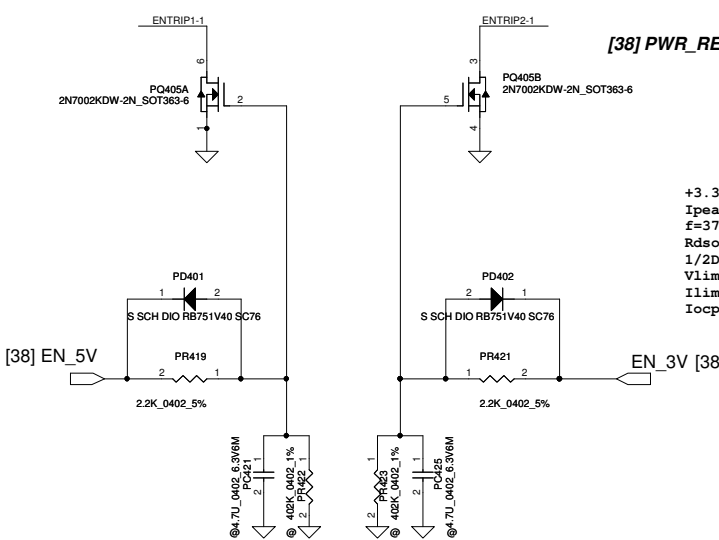
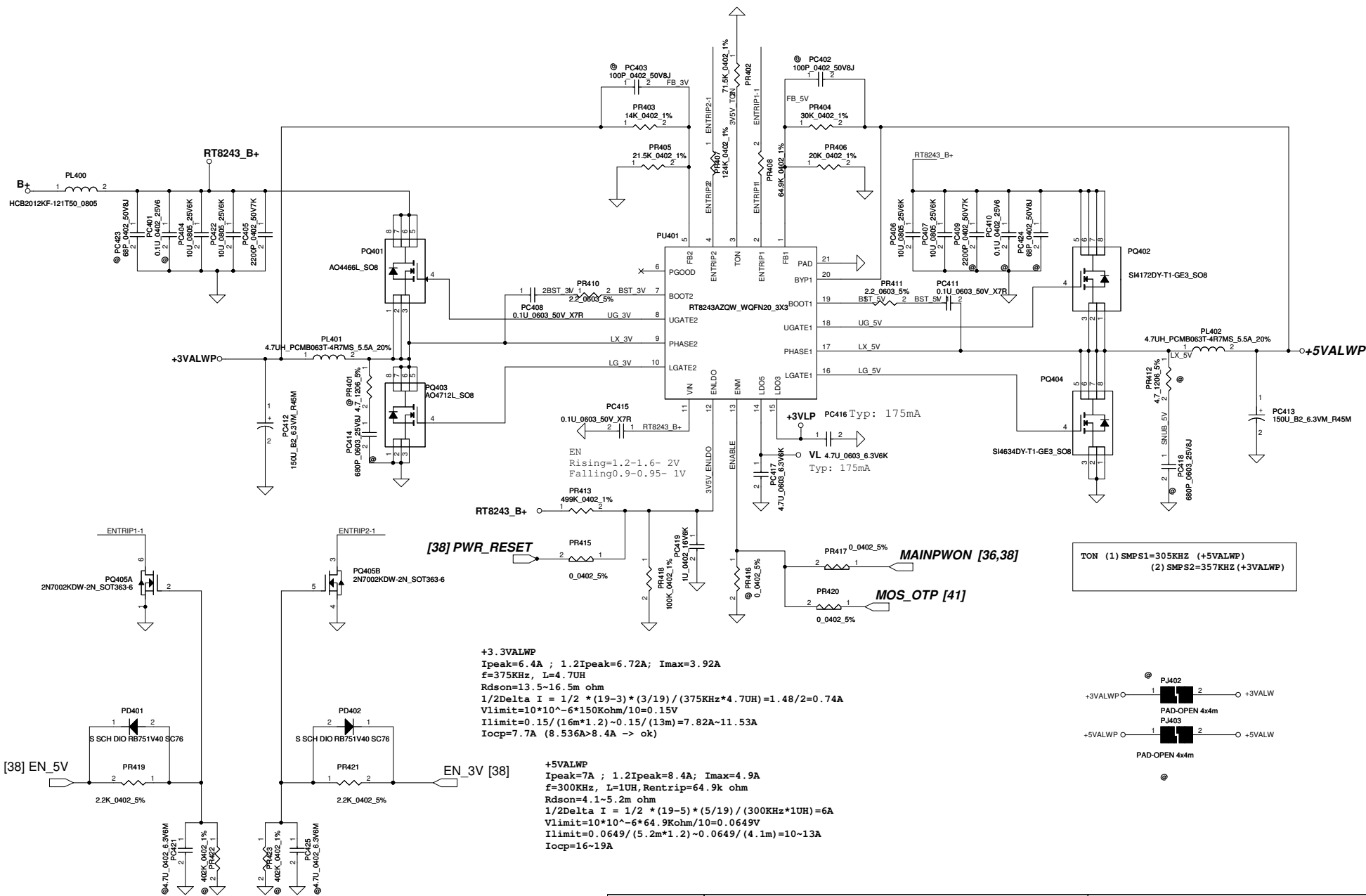
PH201:

Temp.	Rman.	Rnor.	Rmin. (Kohm)
93	7.3419	7.0792	6.8253

MOS_OTP:
 Default:High
 Active :Low

PTC_PROTECT:
 Default:Low
 Active :High

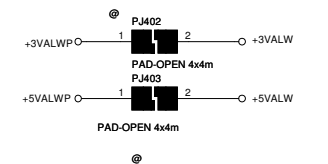
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2012/10/19
check the EN circuit

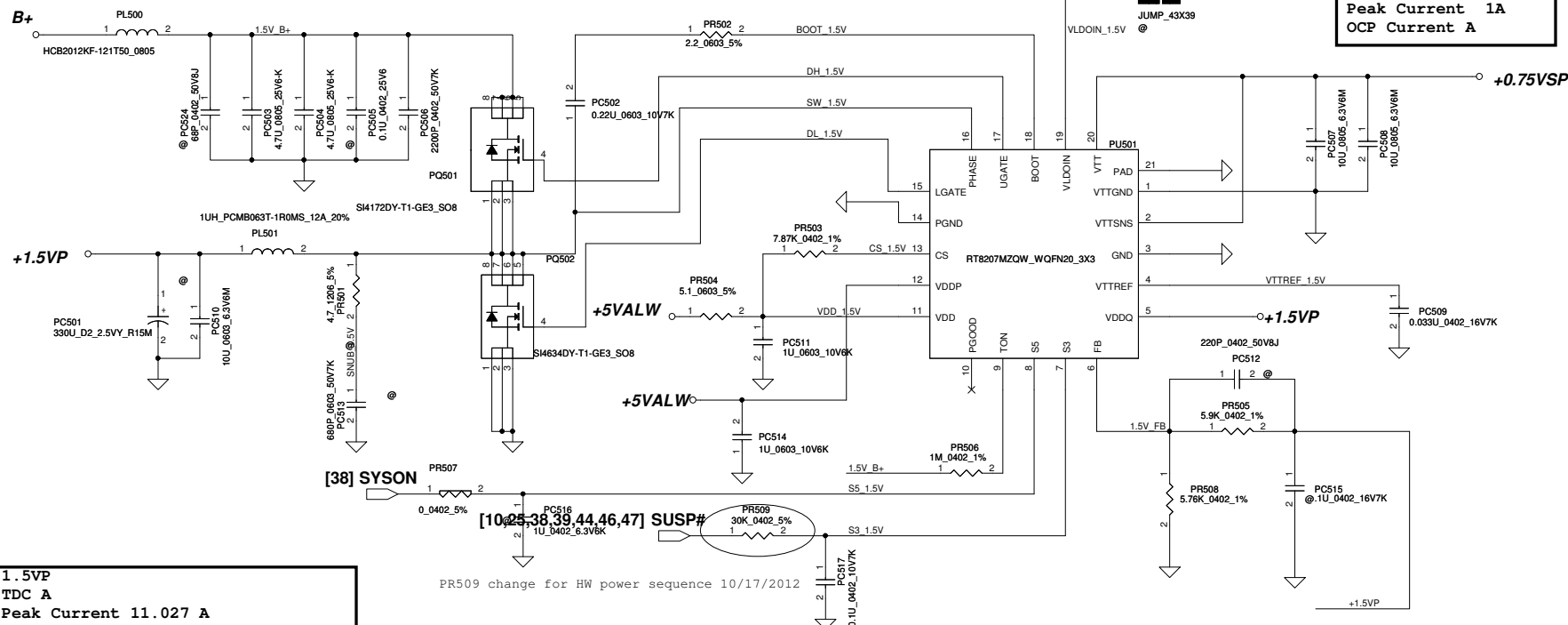
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TON (1) SMP=S1=305KHZ (+5VALWP)
(2) SMP=S2=357KHZ (+3VALWP)



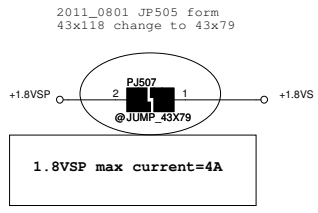
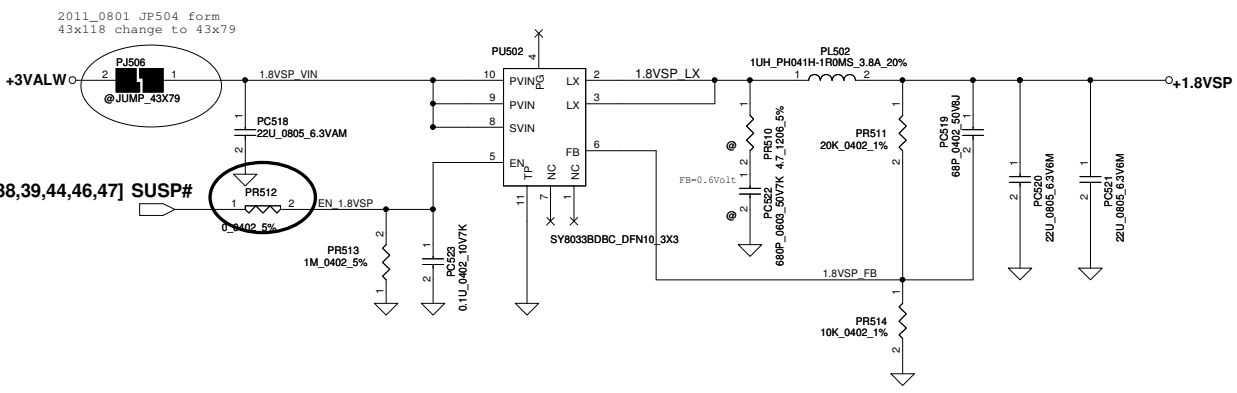
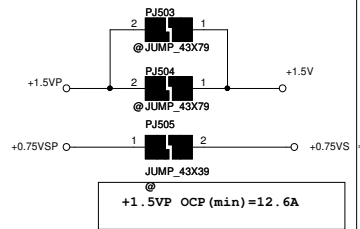
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0.75Volt +/- 5%
TDC A
Peak Current 1A
OCP Current A



1.5VP
TDC A
Peak Current 11.027 A
OCP current 13.36~18.27 A
TYP MAX
H/S Rds(on) :11.7mohm , 14.5mohm
L/S Rds(on) :2.6mohm , 3.2mohm

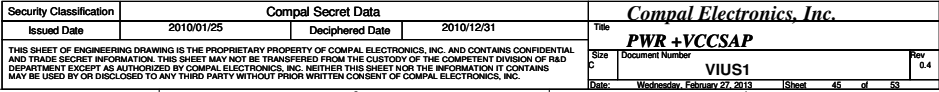
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
(Discharge) (Discharge) (Discharge)					



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output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

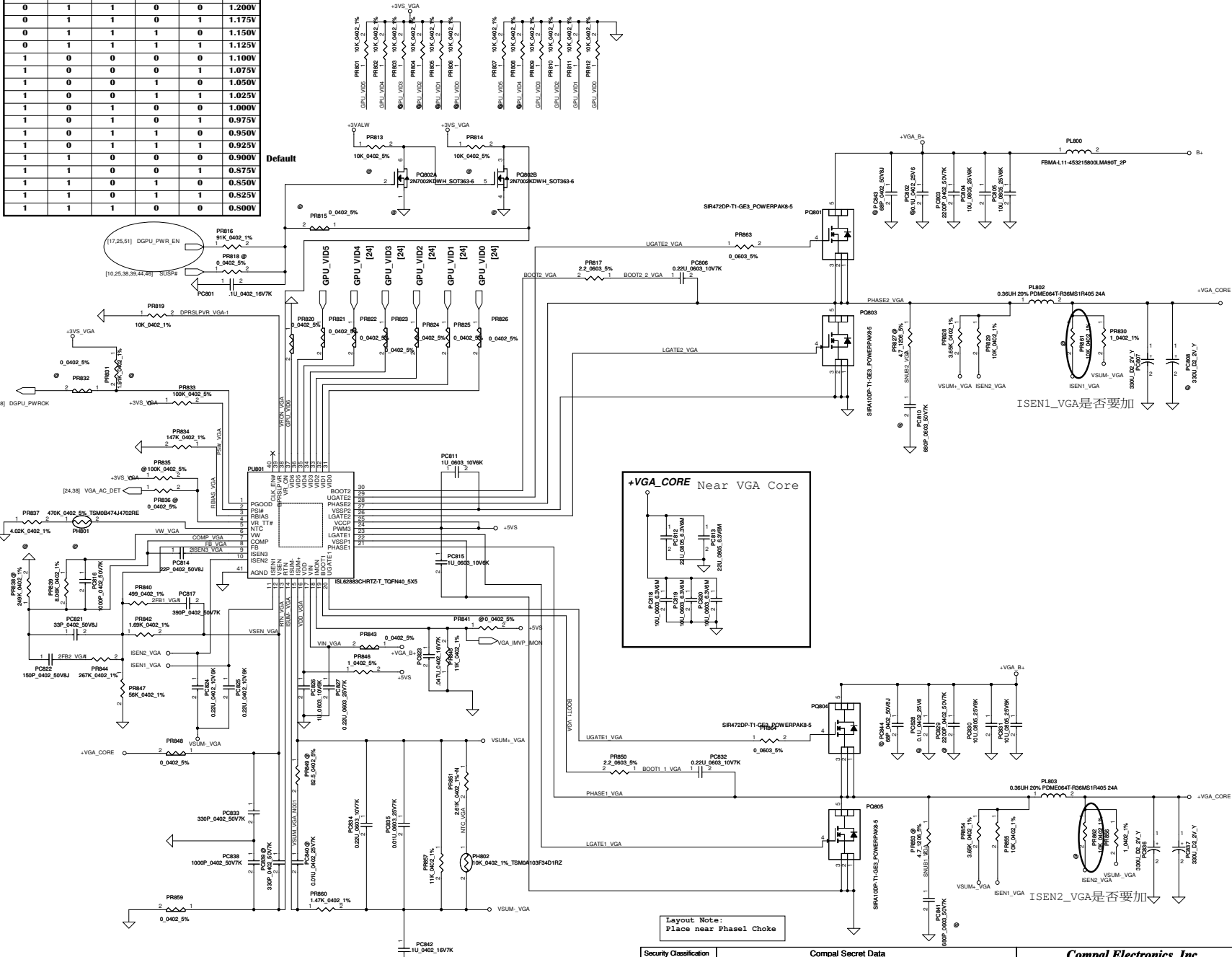




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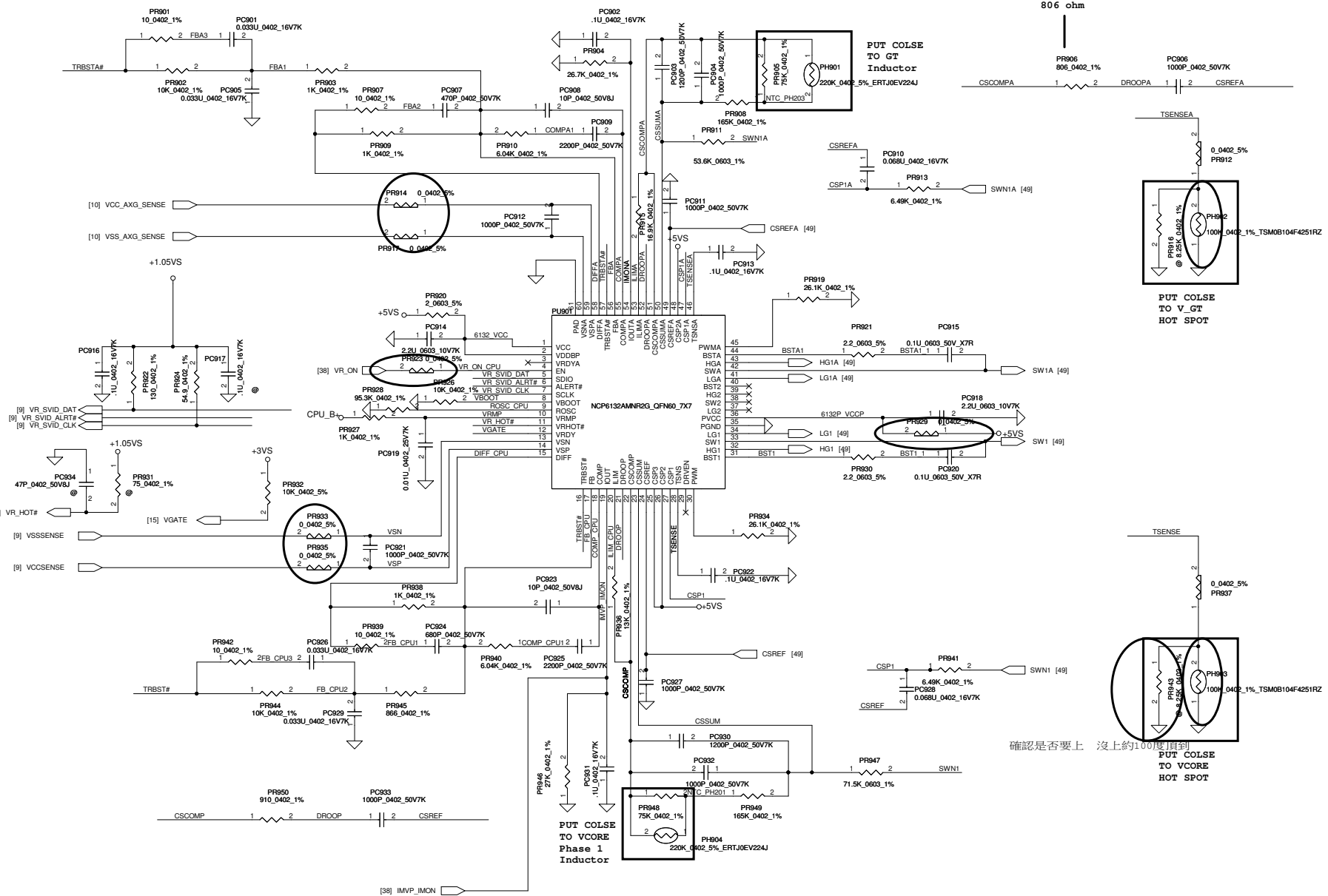
GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	0	0	1.200V
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default

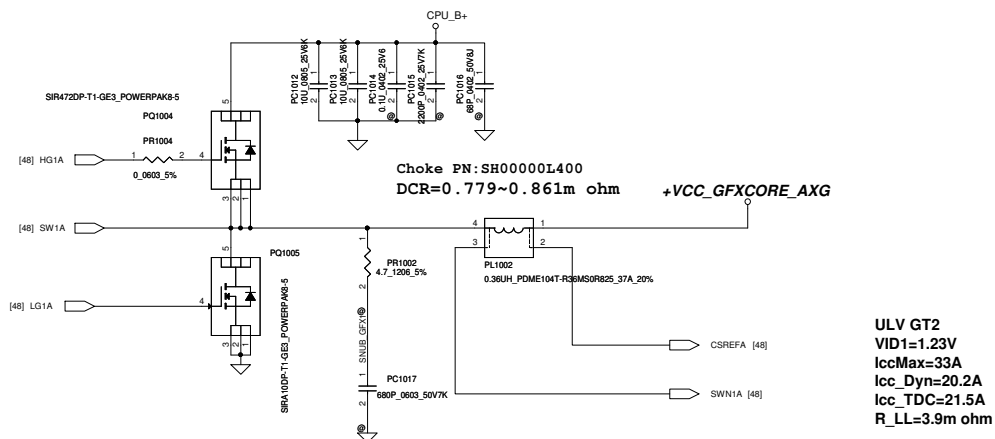
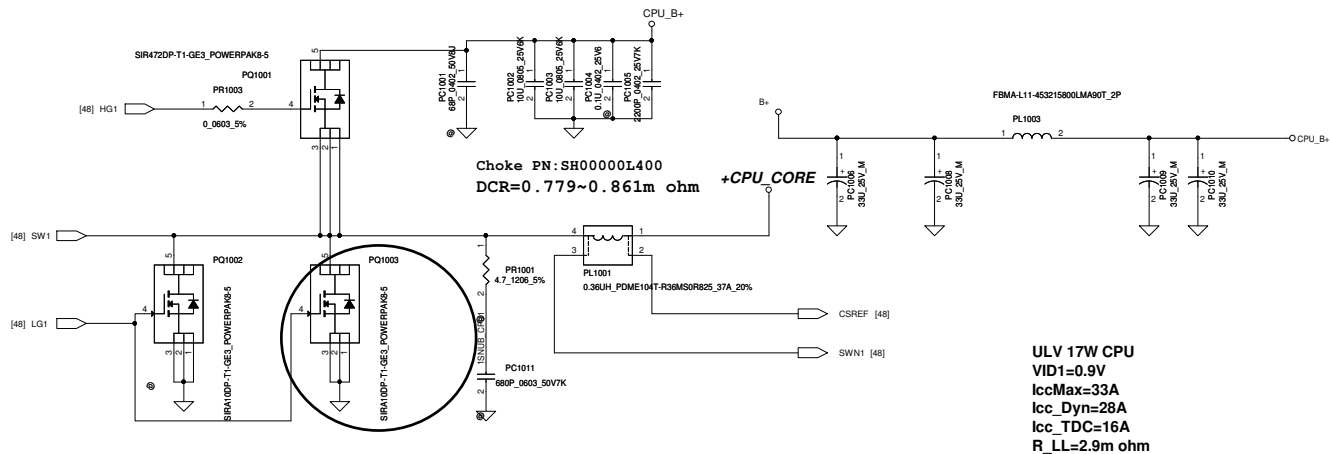


Layout Note:
Place near Phasel Choke

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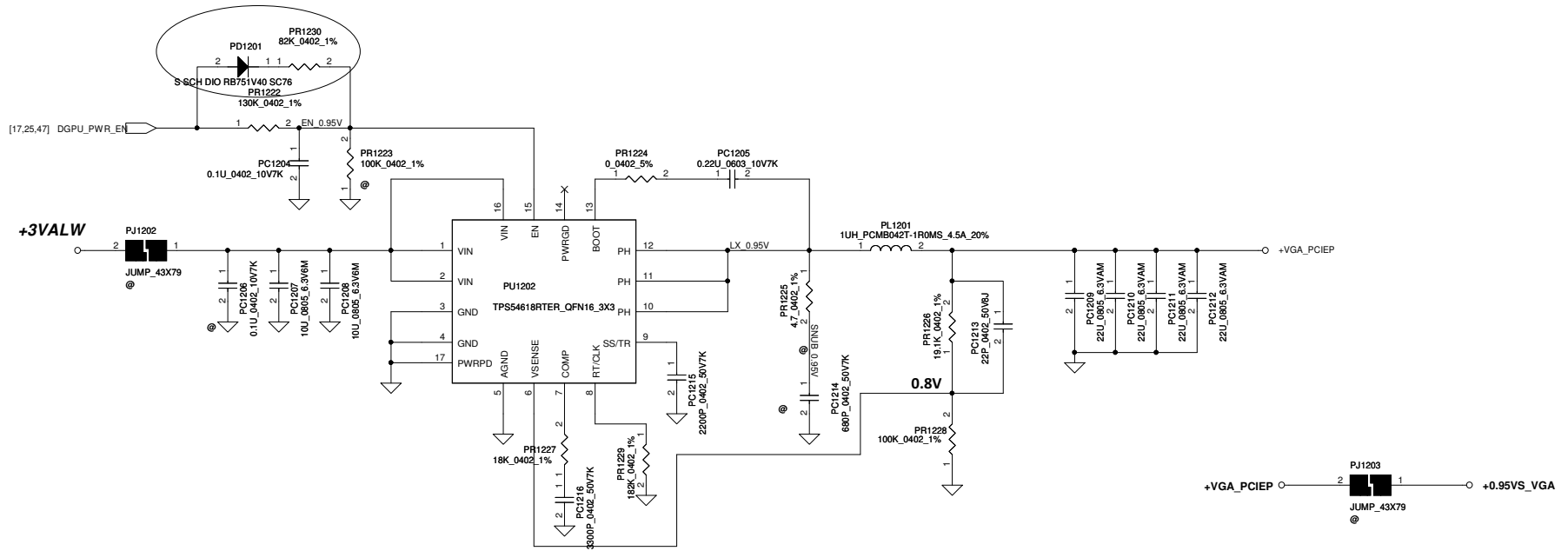


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PR1230,PD1201 add for HW power sequence required 10/31/2012



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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	P6#	Modify List	Date	Phase
1				2012/06/05	
2				2012/06/08	
3				2012/06/08	
4				2012/06/08	
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power

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