

VFKTA

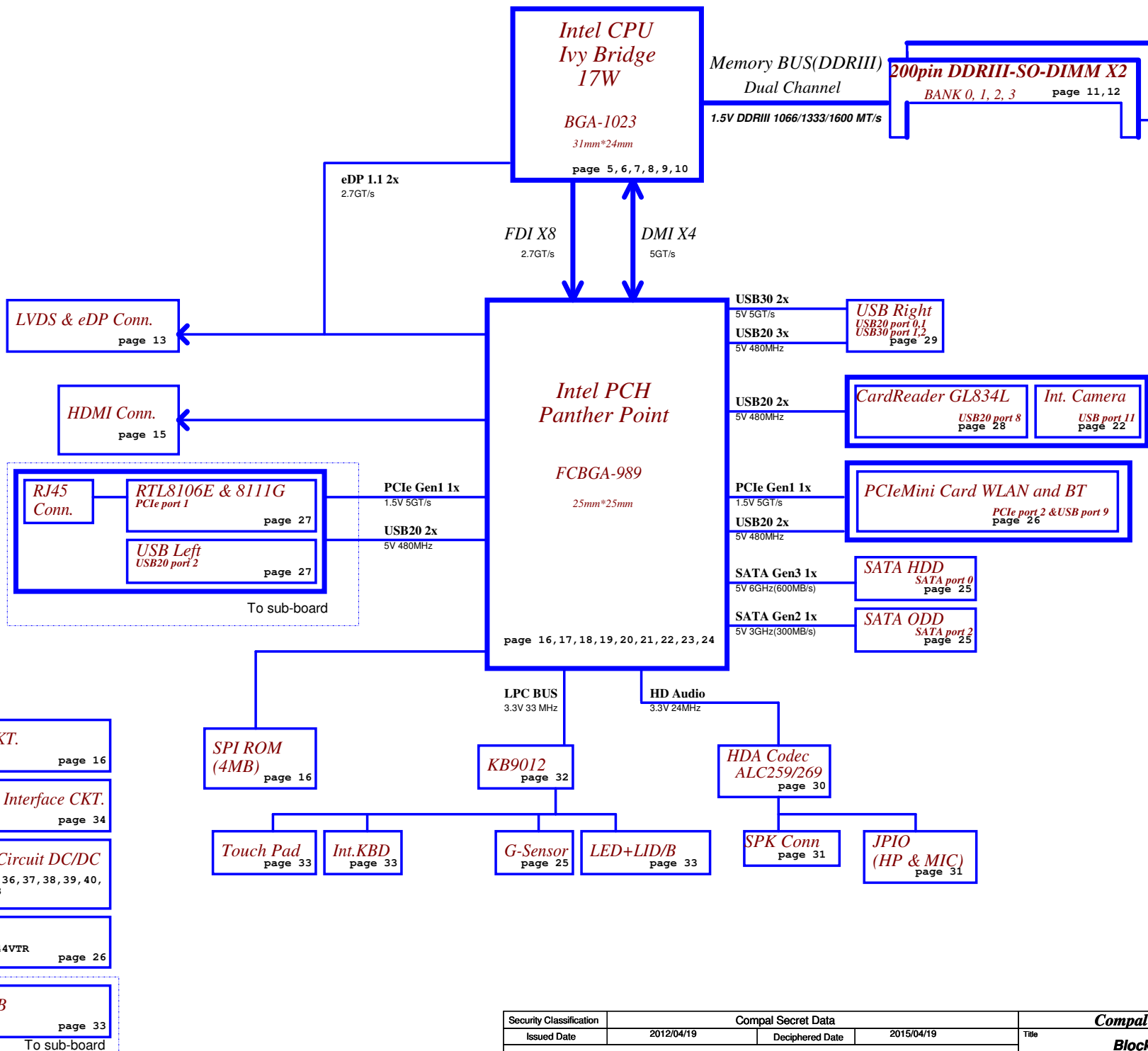
Rosetta 10FT/10FTG

LA-9862P REV 1.0 Schematic

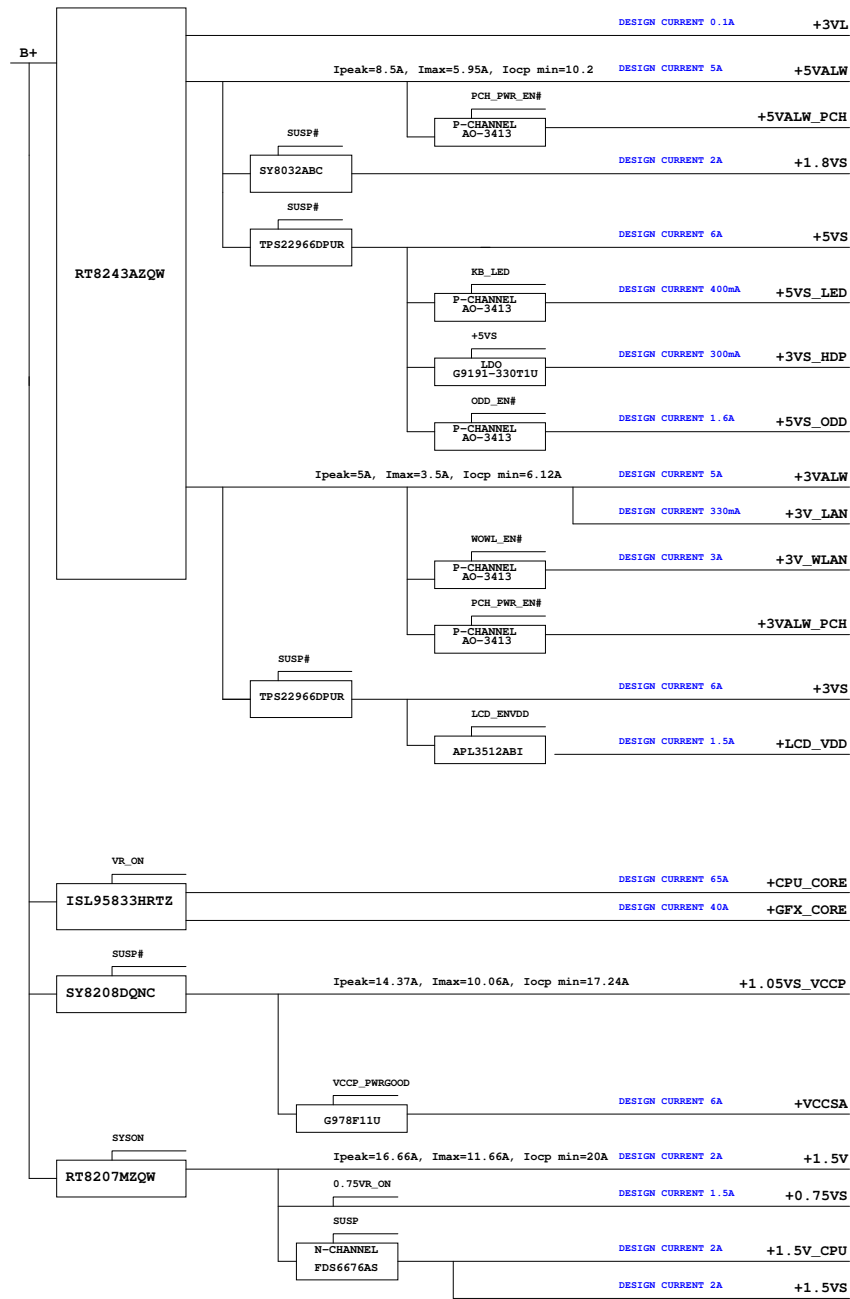
Intel Processor (Ivy Bridge/Sandy Bridge)+
PCH(Panther Point)

2013-02-06 Rev 1.0

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page		
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Voltage Rails

(O MEANS ON X MEANS OFF)

BTO Option Table

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.5V_CPU +0.75VS +CPU_CORE +GFX_CORE +VCCSA +1.05VS_VCCP +3V_WLAN +3V_LAN +LCD_VDD
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Function	CPU					PCH	
description	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847	Panther Point	
explain	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847	HM76	HM70
BTO	CPUI53337UR1@	CPUI33227UR1@	CPUI32375MR1@	CPUP2117UR1@	CPUC847R1@	HM76R1@	HM70R1@
	CPUI53337UR3@	CPUI33227UR3@	CPUI32375MR3@	CPUP2117UR3@	CPUC847R3@	HM76R3@	HM70R3@

Function	LVDS-eDP	Camera & Mic	USB S&C	CRT	EC
description	LVDS-eDP	Camera & Mic	14640 14641	CRT	EC
explain	LVDS eDP	Camera & Mic	14640 14641	w/ CRT w/o CRT	KB9012 NPCE885N
BTO	LVDS@ IEDP@	CAM_EMI@	14640@ 14641@	CRT@ CRT_EMI@ NOCRT@	9012@ 885@

Function	WOWL	G-SENSOR	ZPODD	GCLK	Touch Screen
description	WOWL	G-SENSOR	ZPODD	GCLK non-GCLK	Touch Screen
explain	w/ w/o	G-SENSOR	w/ w/o	GCLK non-GCLK	Touch Screen
BTO	WOWL@ NOWOWL@	GSENSOR@	ZPODD@ NONZP@	GCLK@ NOGCLK@	TOUCH_EMI@

Function	Sleep & Music	KB Light	EMI/ESD/RF part	ISPD
description	Sleep & Music	KB Light	EMI/ESD/RF part	HDMI Logo
explain	w/ S&M w/o S&M	KB Light	EMI/ESD/RF part	HDMI Logo
BTO	269@ 259@	KBL@	EMI@ @EMI@ ESD@ @ESD@ @RF@	HDMI45@

Red Word: always un-mount

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Touch Pad	2C H	0010 1100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b
+3VL	USB S&C 14640	35 H	0011 0101 b

EC SM Bus2 Address

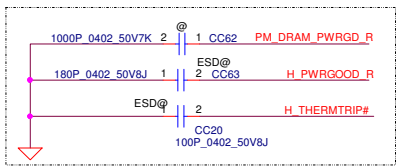
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	G-Sensor	40 H	0100 0000 b

07/22/13 Add G-sensor reference hexman

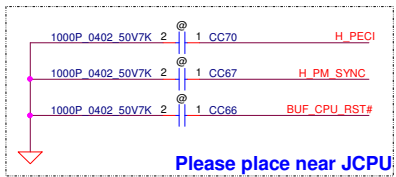
07/22/13 Add Smart Charger SMbus address: 0x12 hexman we Add already

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

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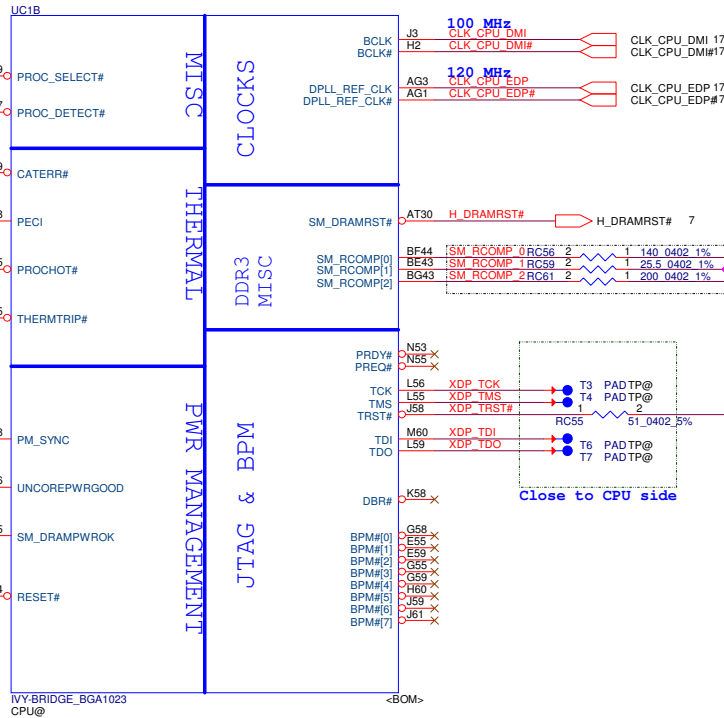
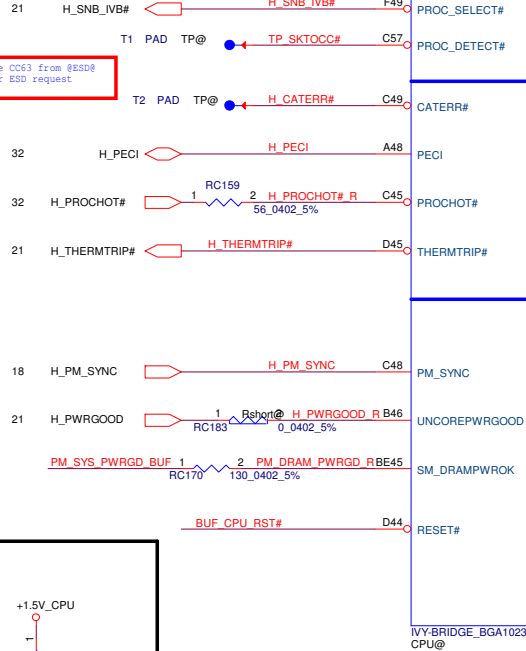


by ESD request and place near CPU

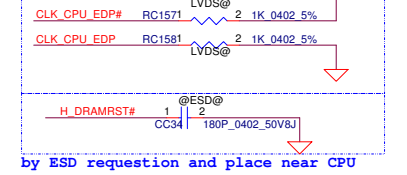


Please place near JCPU

11/30 Change CC63 from @ESD@ to ESD@ for ESD request



Stuff RC158&RC157 if do not support eDP

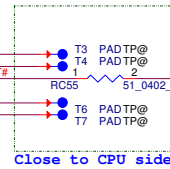


by ESD request and place near CPU

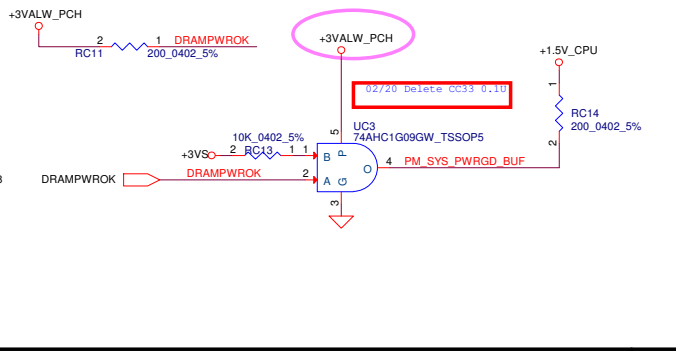
DDR3 Compensation Signals
Layout Note: Place these resistors near Processor



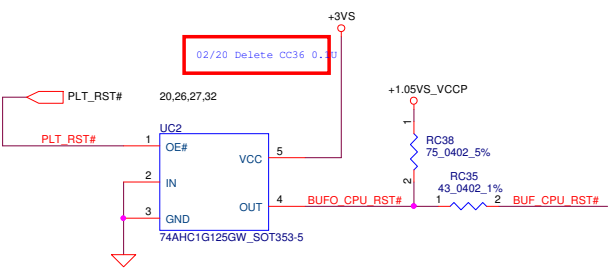
Routed as a single daisy chain



Close to CPU side

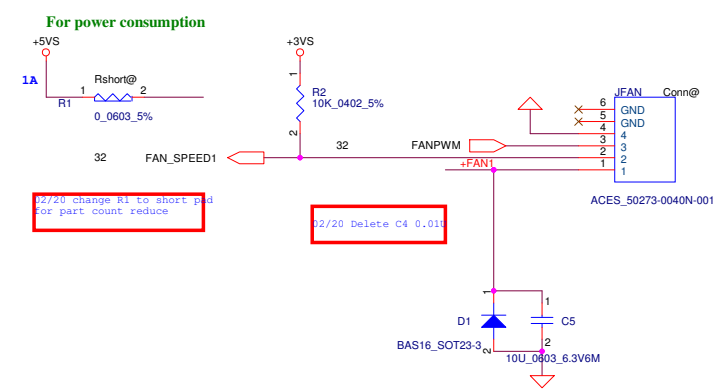


Buffered Rest to CPU

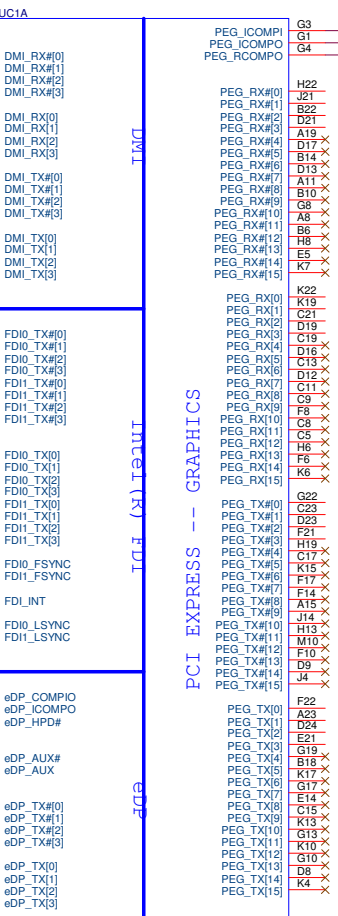
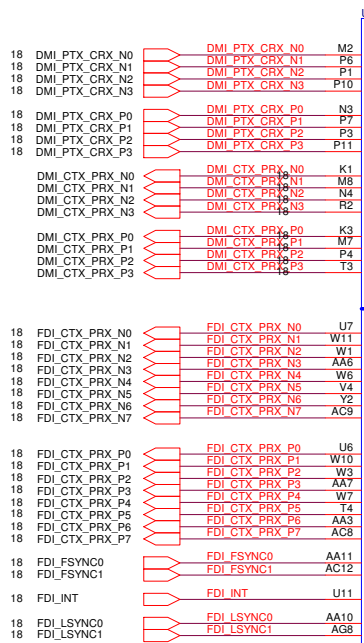


XDP Connector

FAN Control Circuit



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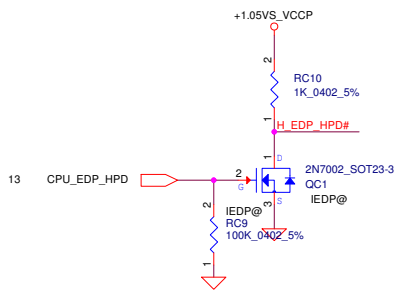


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

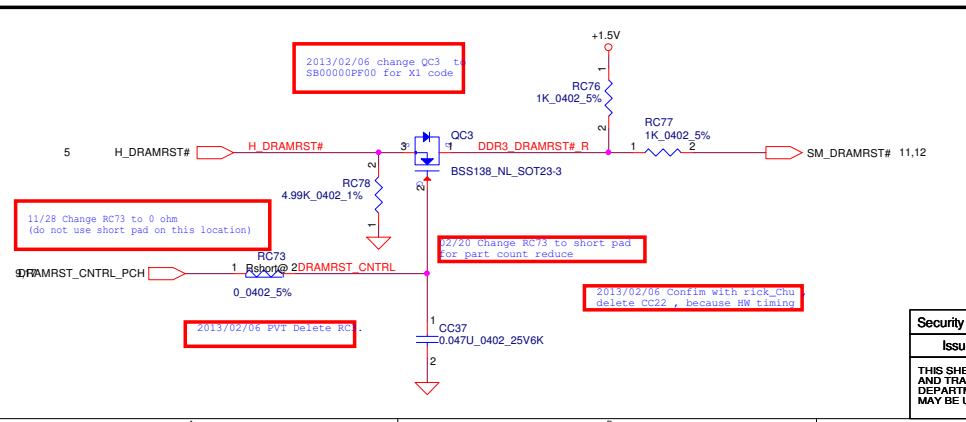
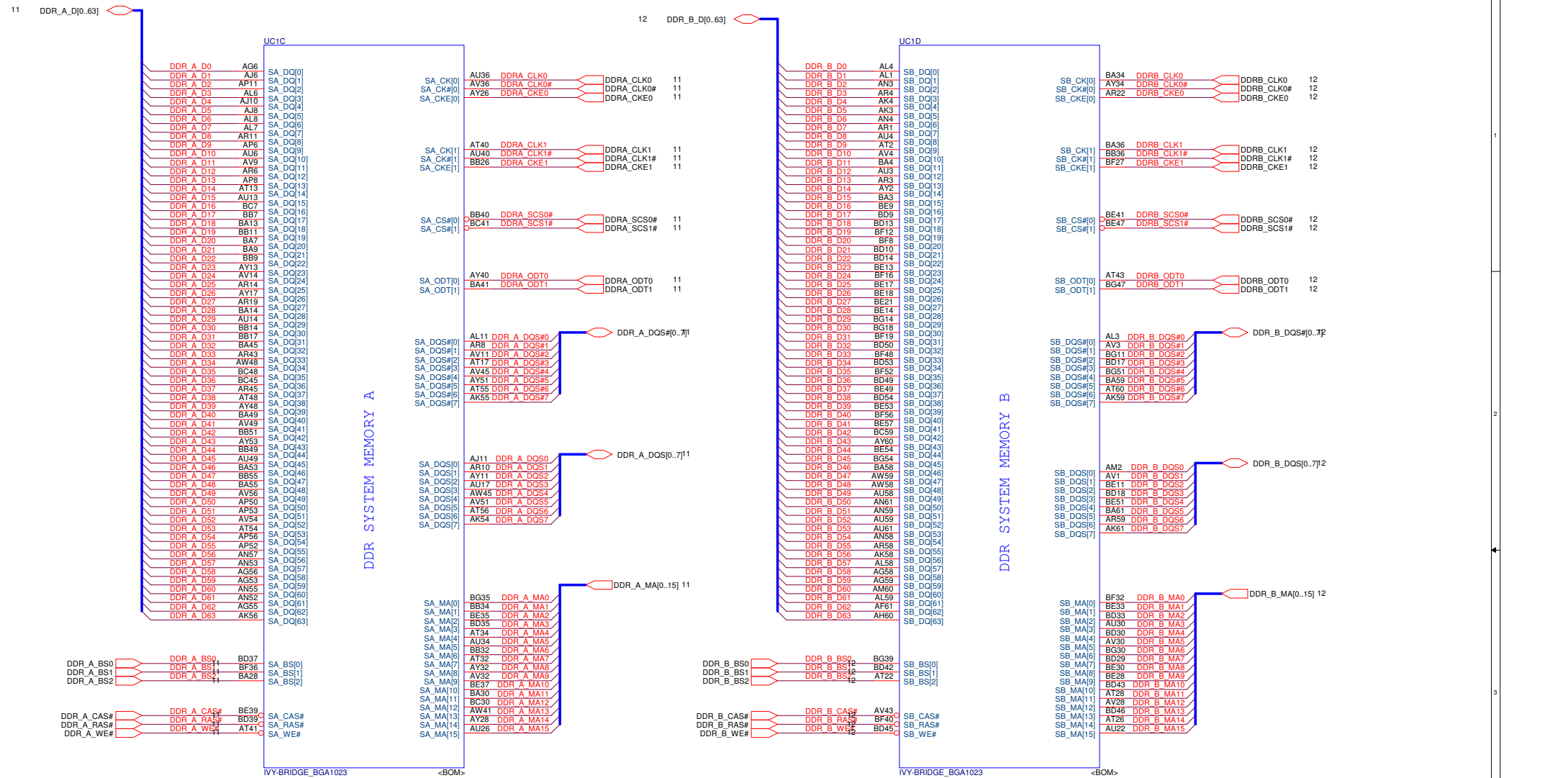
eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

10/24 SWAP pin H_EDP_AUXN/P

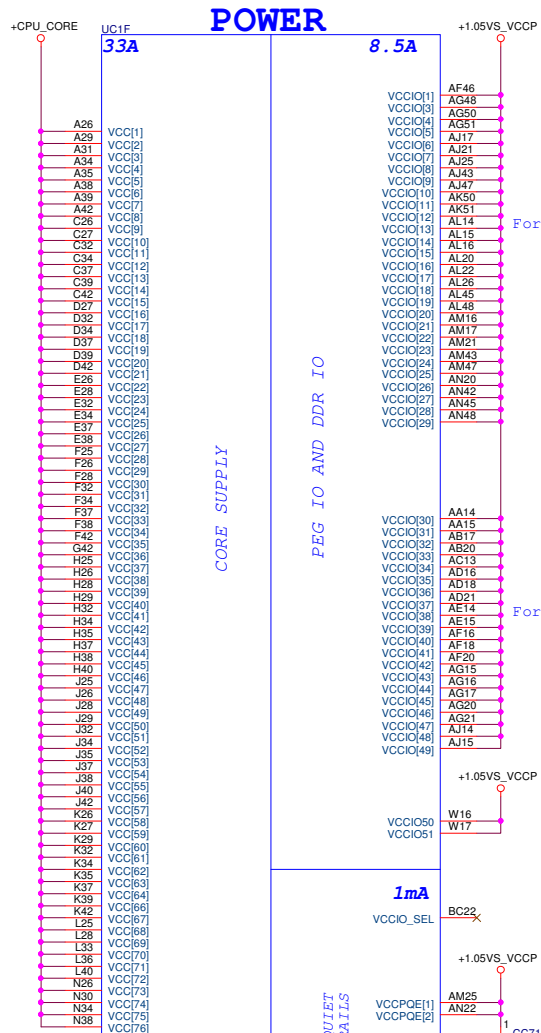
02/20 Swap H_EDP_TXN[0\1] to H_EDP_TXP[0\1]



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POWER

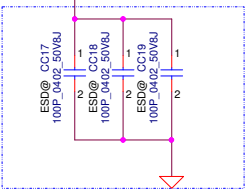
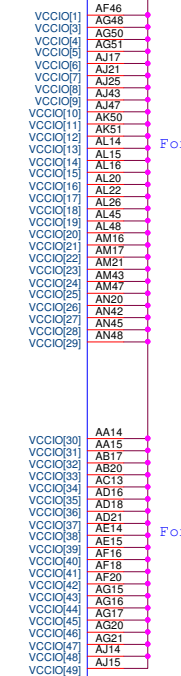
CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

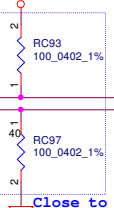
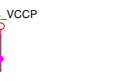
SVID

SENSE LINES



by ESD request and place near CPU

11/30 install 3 CAP(100pF)CC17,CC18,CC19 on +1.05Vs_Vccp and must close to CPU



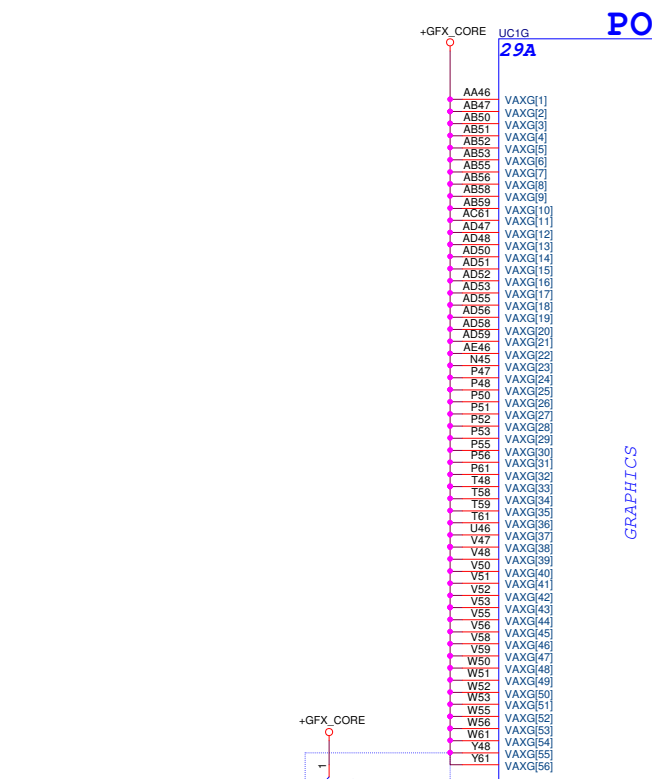
Pull high resistor on VR side

Close to CPU

Ivy BRIDGE_BGA1023 CPU@

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Title		
Ivy Bridge_POWER-1		
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POWER

GRAPHICS

DDR3 - 1.5V RAILS

QUIET RAILS

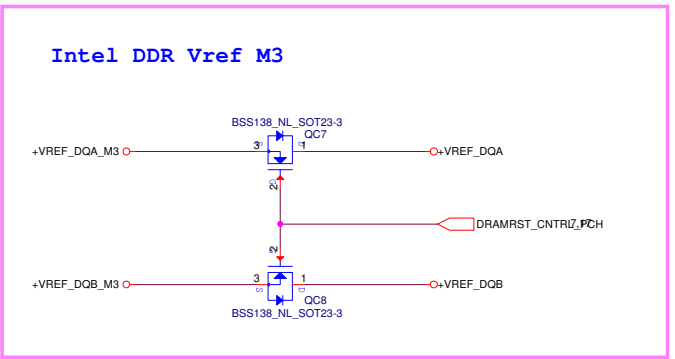
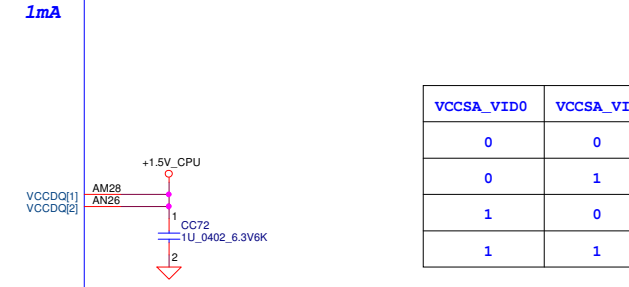
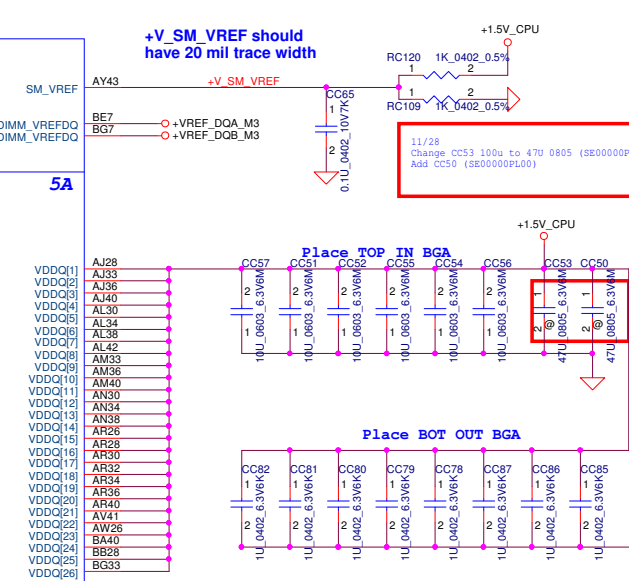
1.8V RAIL

1.8V RAIL

SENSE LINES

SENSE LINES

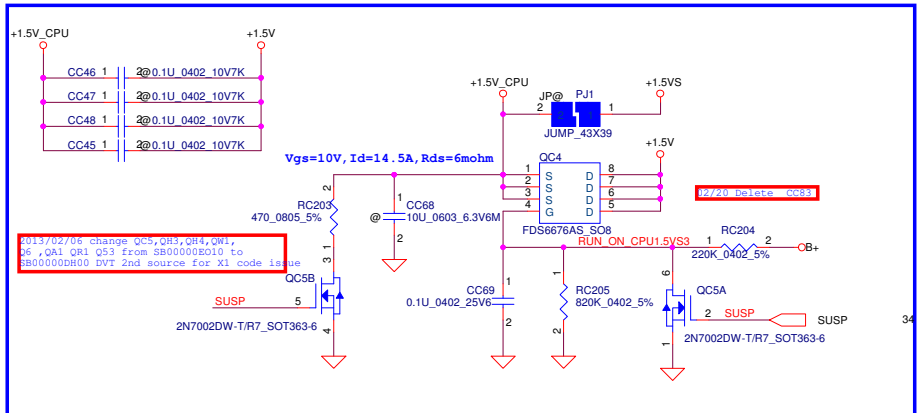
SENSE LINES



+1.5V_CPU Decoupling:
2X 47U (MLCC), 6X 10U, 8X 1U

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge



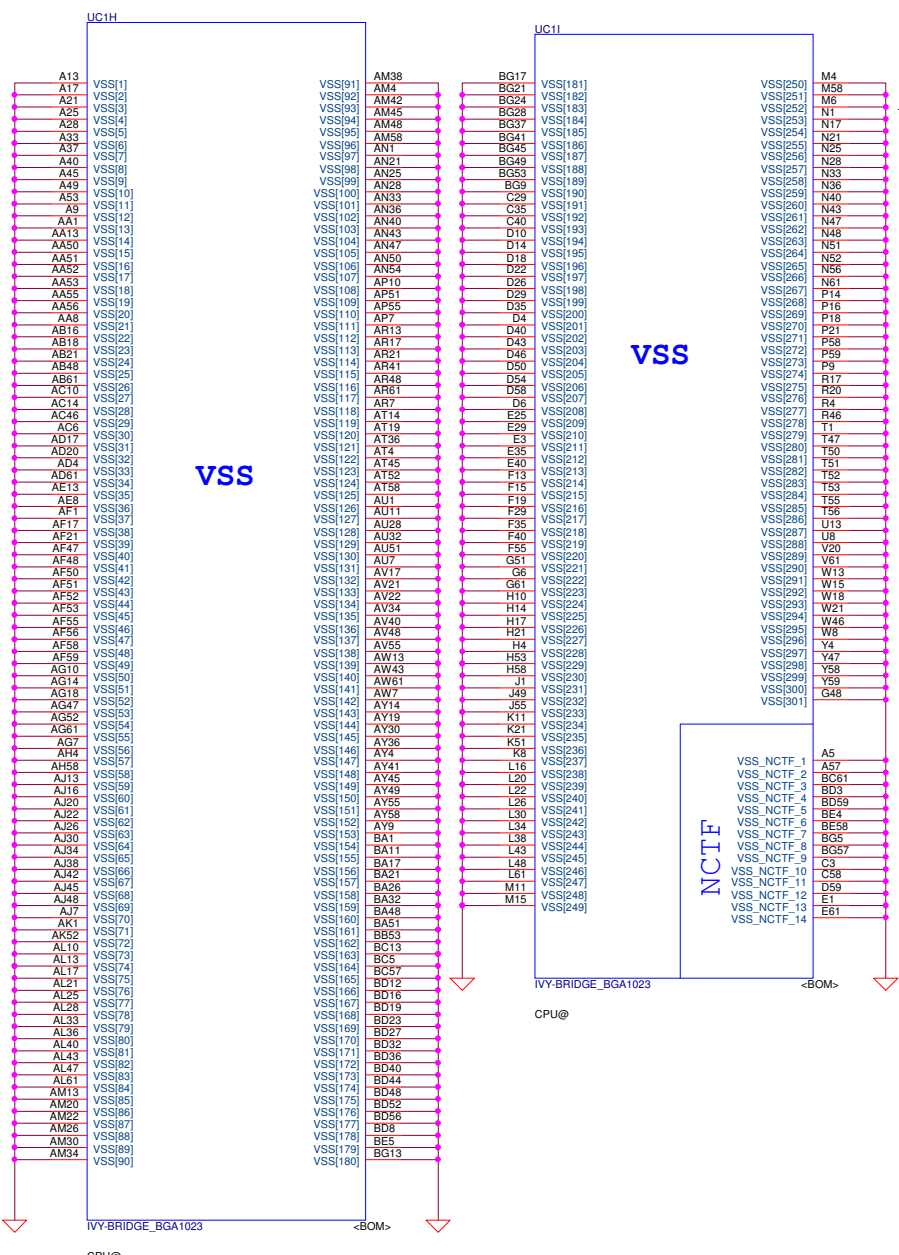
VCCPLL Decoupling:
1x 330U (6m ohm), 1x 10U, 2x1U

Reserve for power consumption
Remove on PVT phase

+VCCSA Decoupling:
2X 47U (MLCC), 3X 10U, 5X 1U

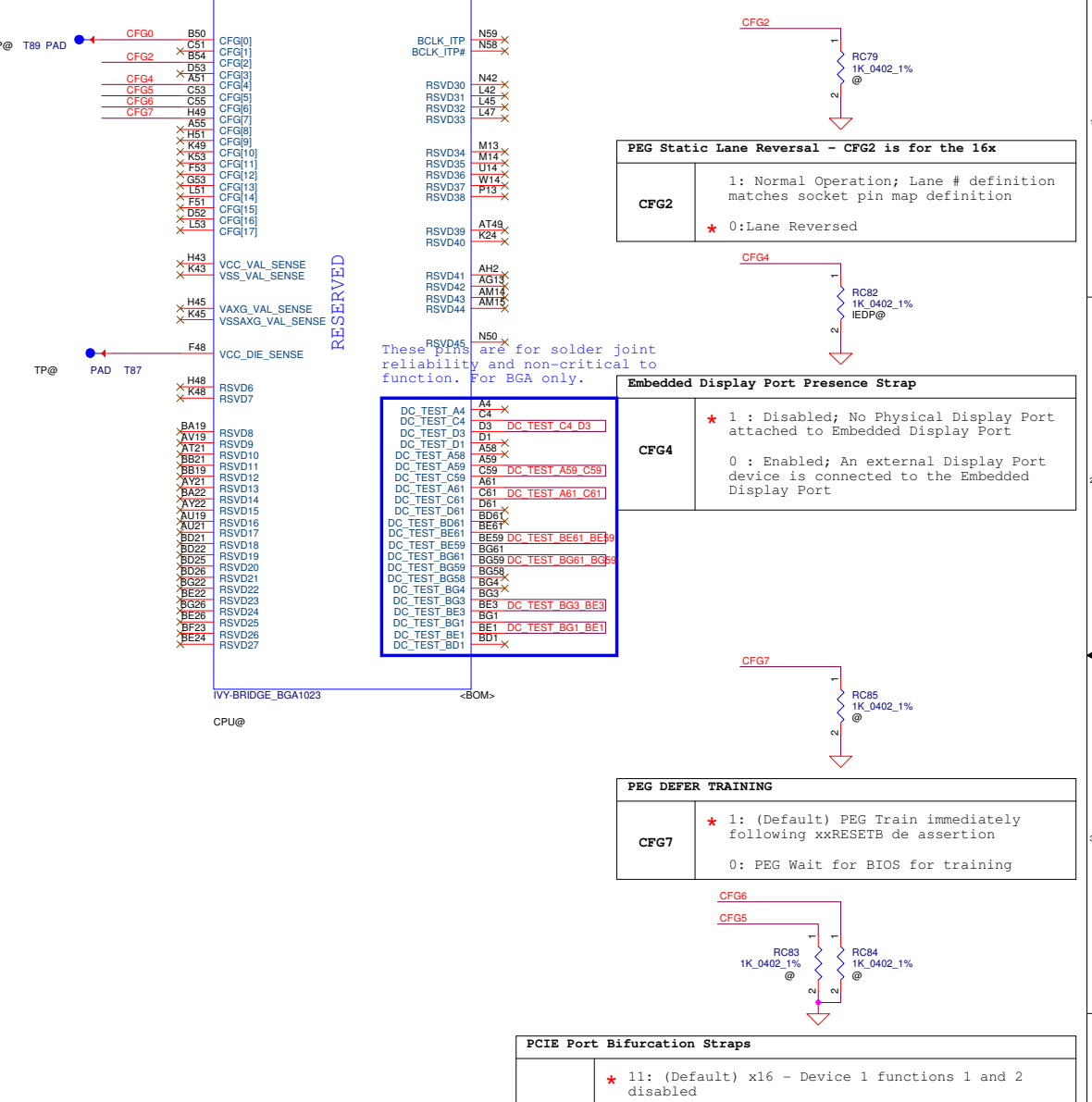
11/28 change CC44 100u to 0805 size (SB00000PL00), Add CC40 (SB00000PL00)

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CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2

1: Normal Operation; Lane # definition matches socket pin map definition

* 0: Lane Reversed

Embedded Display Port Presence Strap

CFG4

* 1 : Disabled; No Physical Display Port attached to Embedded Display Port

0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING

CFG7

* 1: (Default) PEG Train immediately following xxRESETB deassertion

0: PEG Wait for BIOS for training

PCIe Port Bifurcation Straps

CFG [6 : 5]

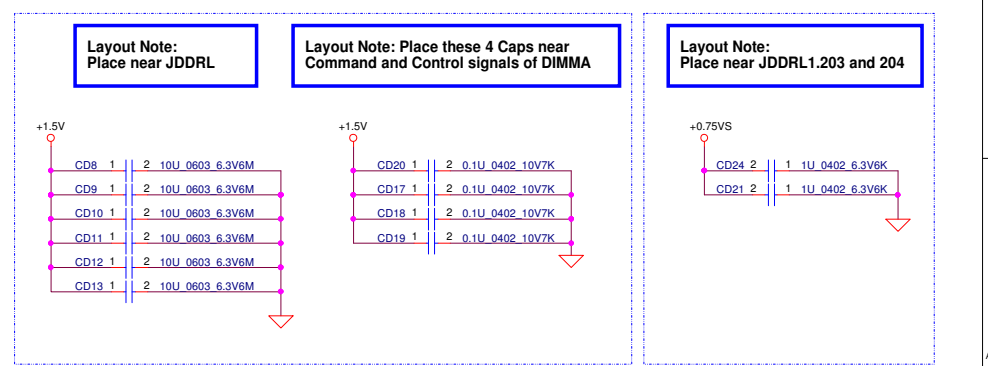
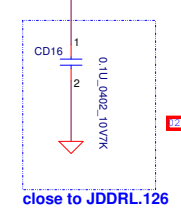
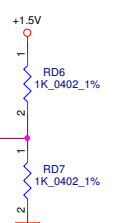
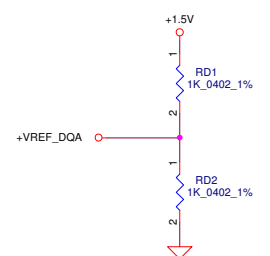
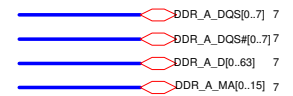
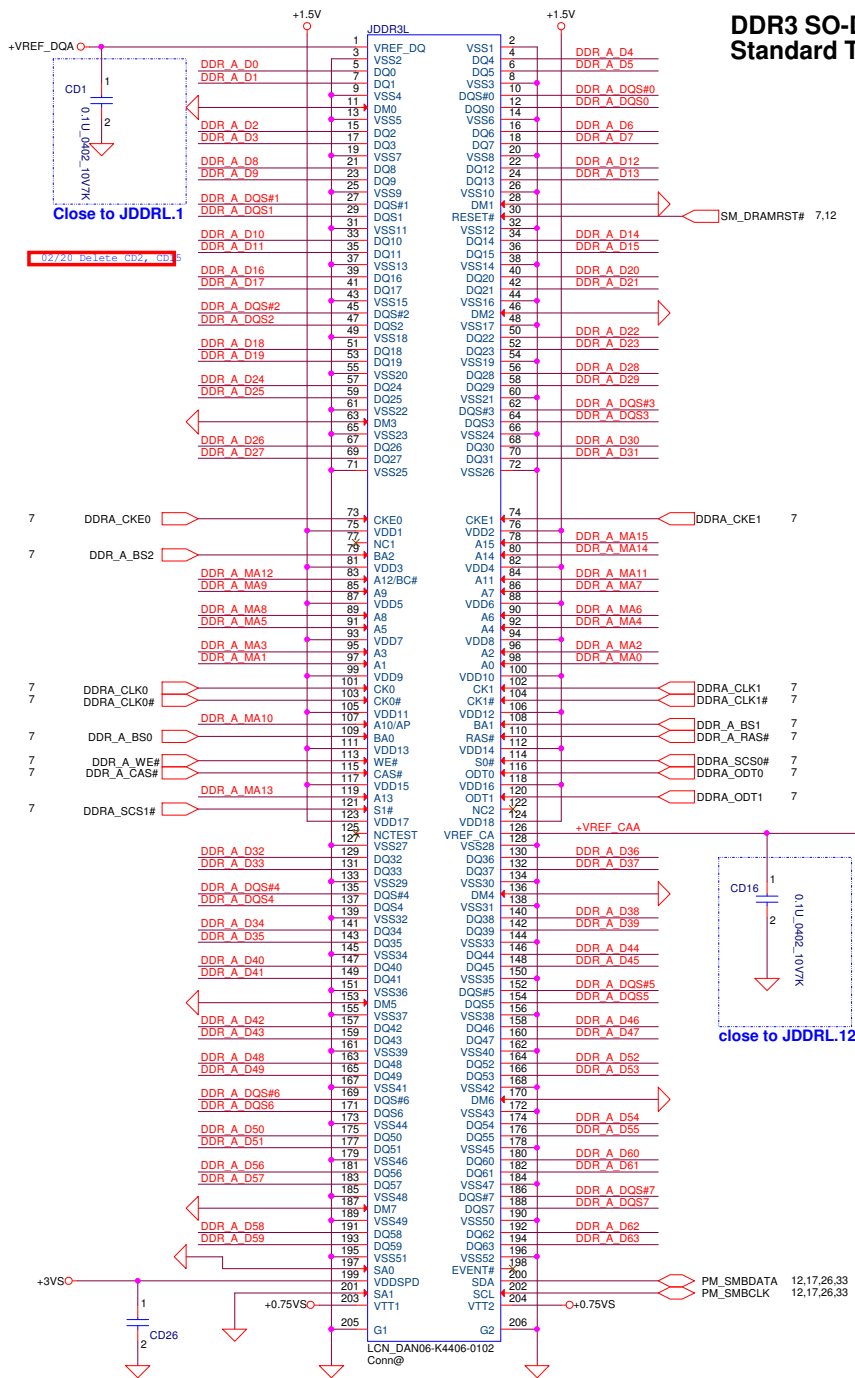
* 11: (Default) x16 - Device 1 functions 1 and 2 disabled

10: x8, x8 - Device 1 function 1 enabled; function 2 disabled

01: Reserved - (Device 1 function 1 disabled; function 2 enabled)

00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

DDR3 SO-DIMM A Standard Type



SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

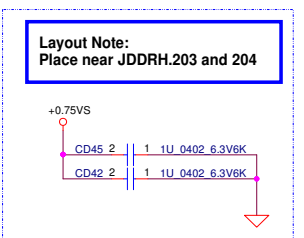
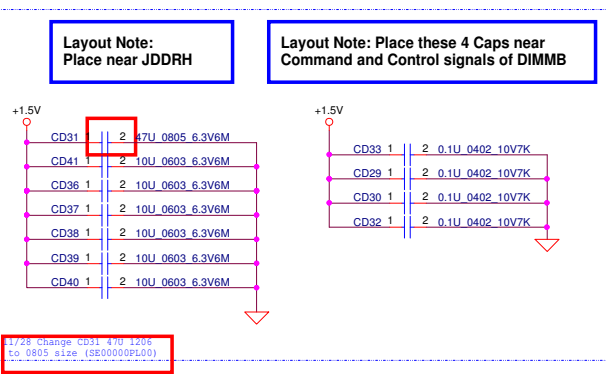
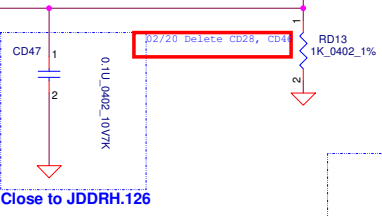
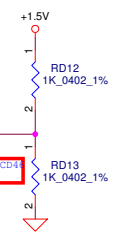
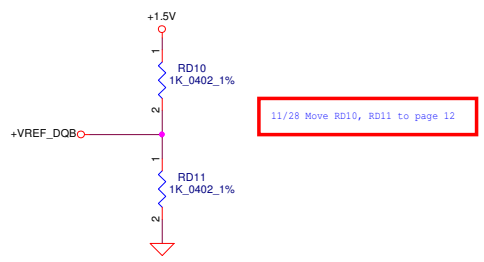
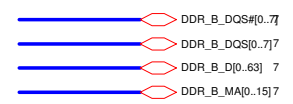
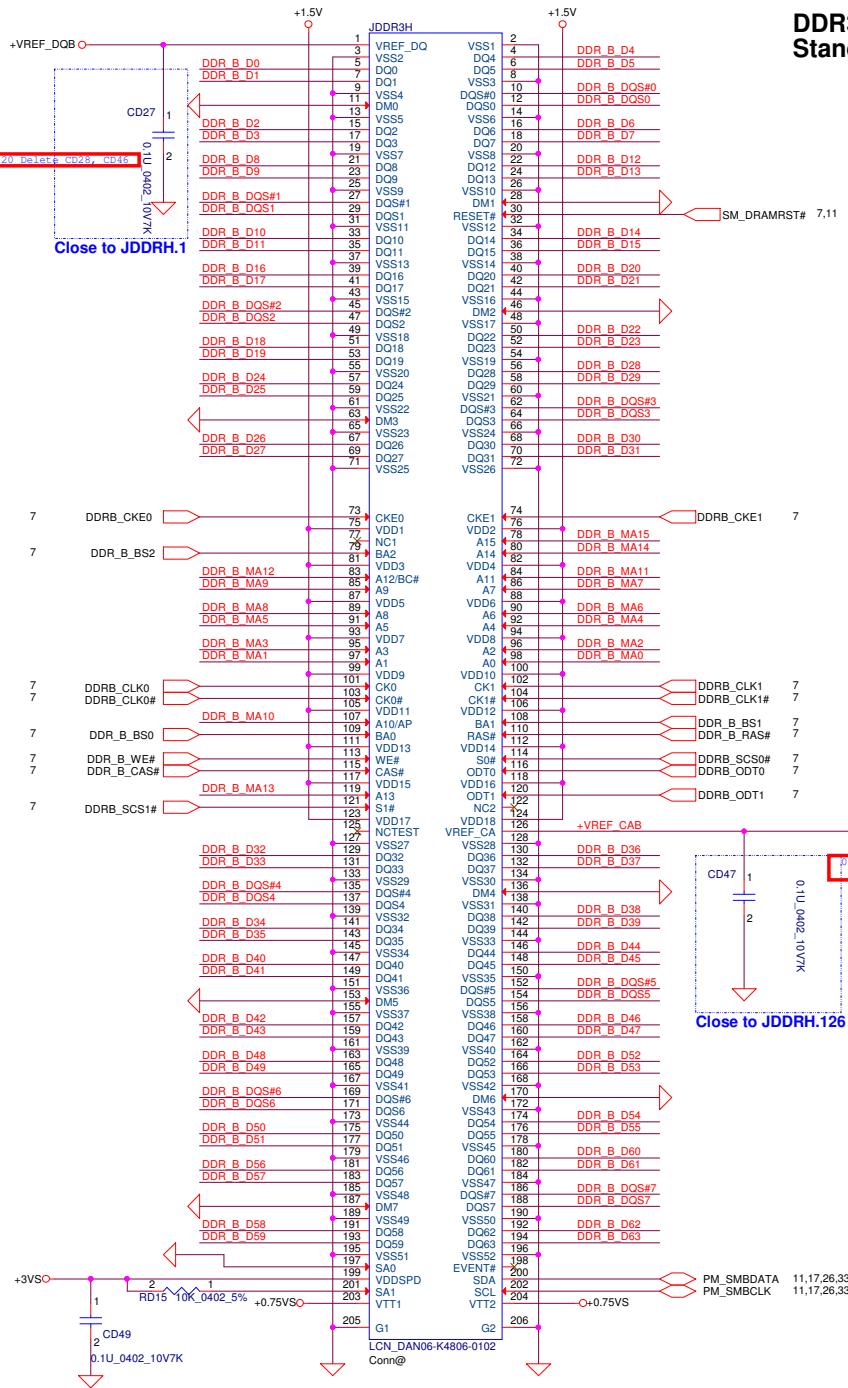
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DDR3II-SODIMMO

VFKTA

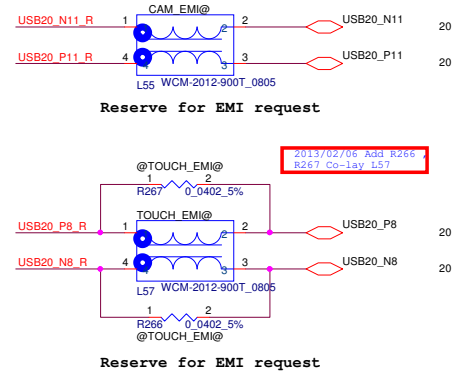
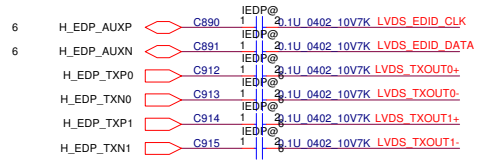
DDR3 SO-DIMM B Standard Type



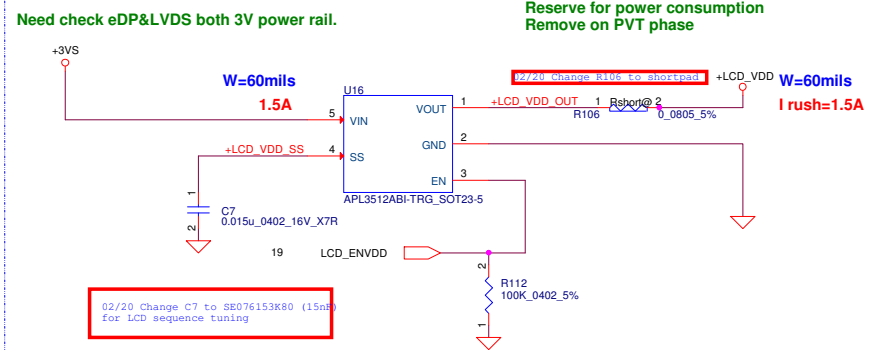
SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

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				Date: Monday, March 11, 2013	Sheet 12 of 46

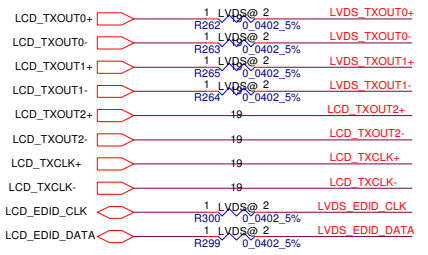
For eDP Panel



LCD POWER CIRCUIT



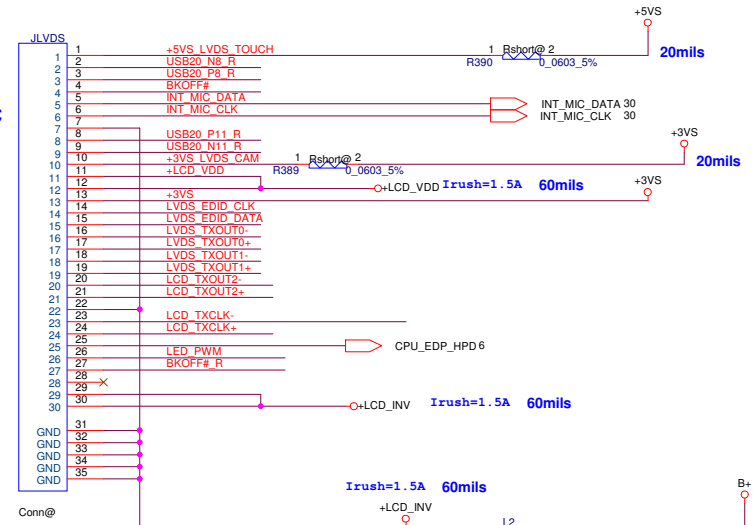
For LVDS 1ch Panel



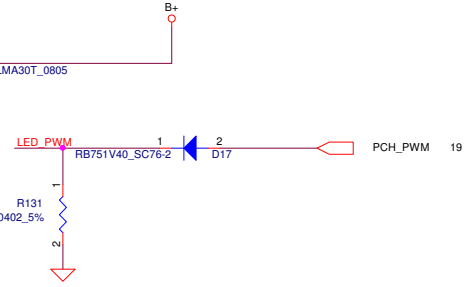
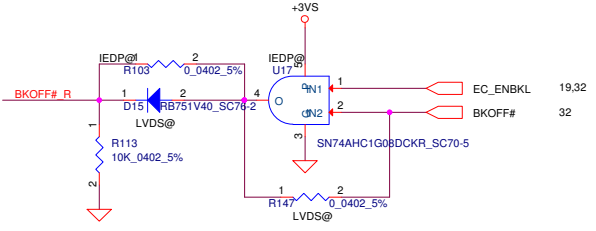
LVDS colay eDP cable

Pin define will be change after ME ready

- pin1-4 Touch function for panel
- pin5-10 For Webcam with single or dual MIC
- pin11-30 For LVDS or eDP panel

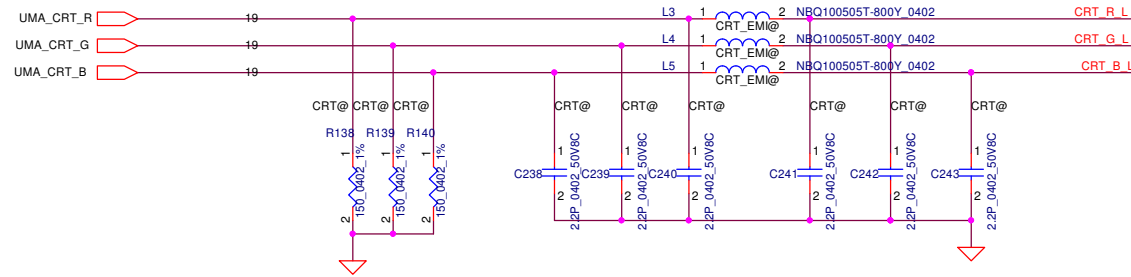


Reserve for eDP panel potential issue



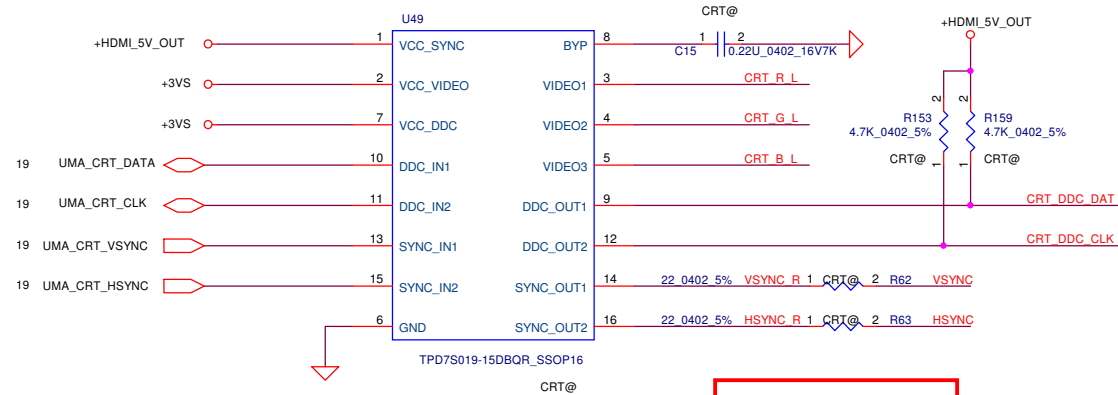
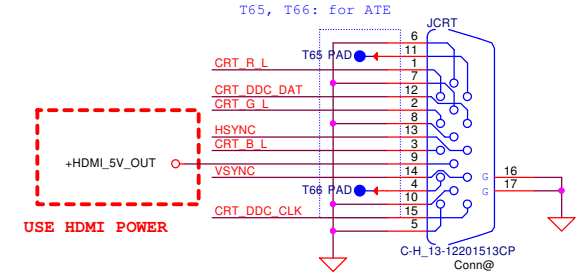
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CRT CONNECTOR



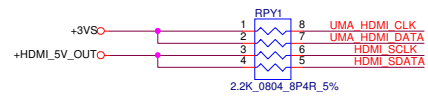
11/28
change BOM structure C238 C239 C240
C241 C242 C243 to CRT@EMI@

02/20 Delete C250 0.1uF

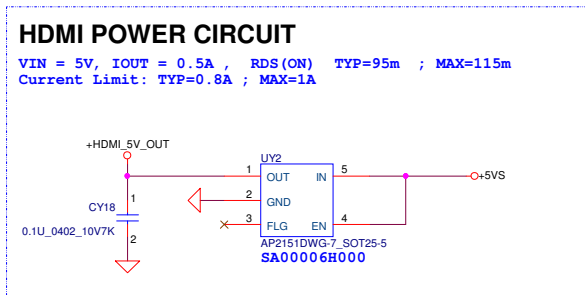


11/29 add 22-ohm (FN: SD028220A80)
on CRT HSYNC/VSYNC trace.

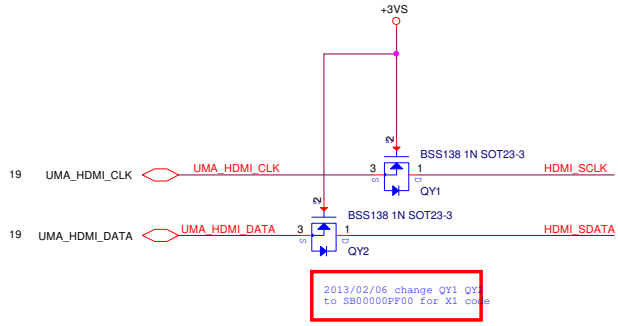
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	
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Size	Document Number			Rev	1.0
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		VFKTA			



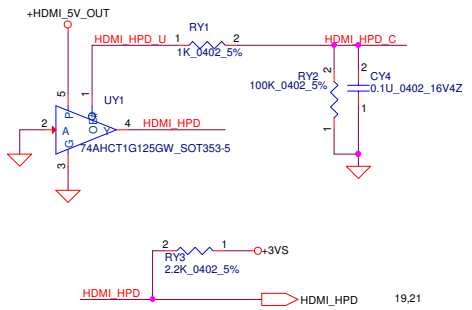
OE#	A	Y
L	L	L
L	H	H
H	X	Z



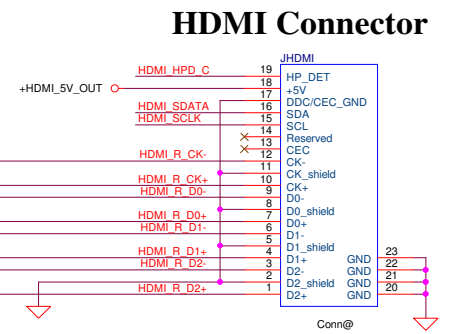
11/28 Update HDMI current limited IC from AP230W-7 to AP2151DDWG-7.



2013/02/06 change QY1 QY2 to SB00000PF00 for xl code



12/04 SWAP RPY4 netname



11/28 Add @ to JHDMI

HDMI Royalty

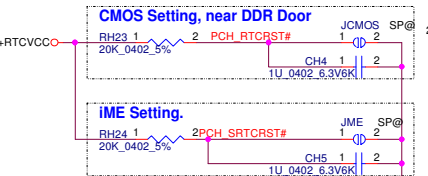
 RO000003HM
 HDMI W/Logo + HDCP

10/18 Modify the BOM structure @ to HDMI45@, change Location HDMI to ZZ.

HDMI W/O Logo: RO000001HM
 HDMI W/Logo: RO000002HM
 HDMI W/Logo + HDCP: RO000003HM

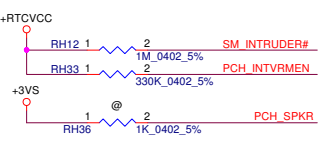
please manually load this virtual material to 45@ BOM

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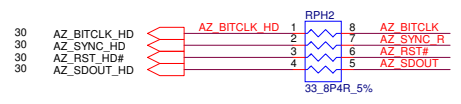
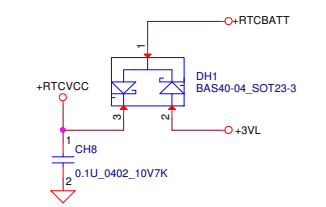


Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

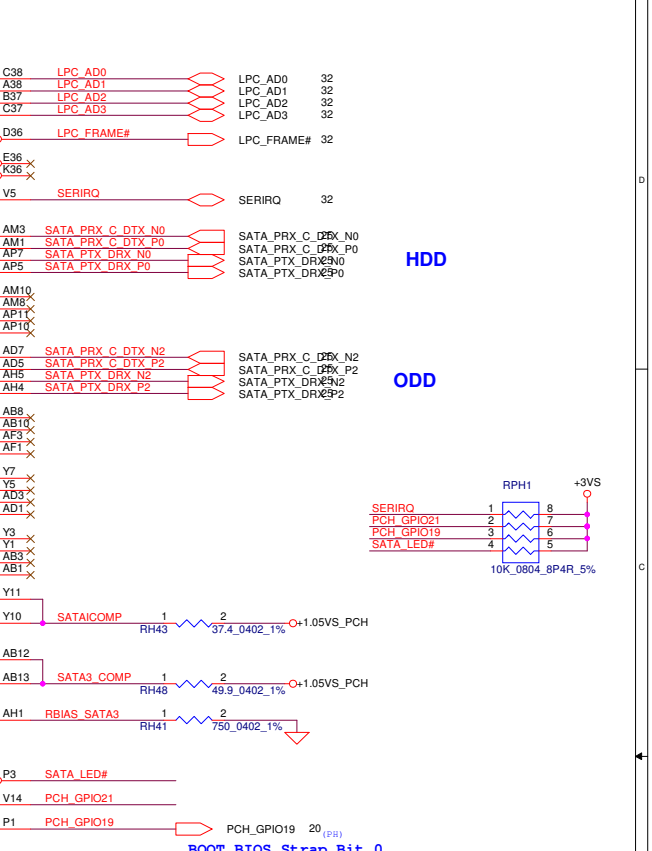
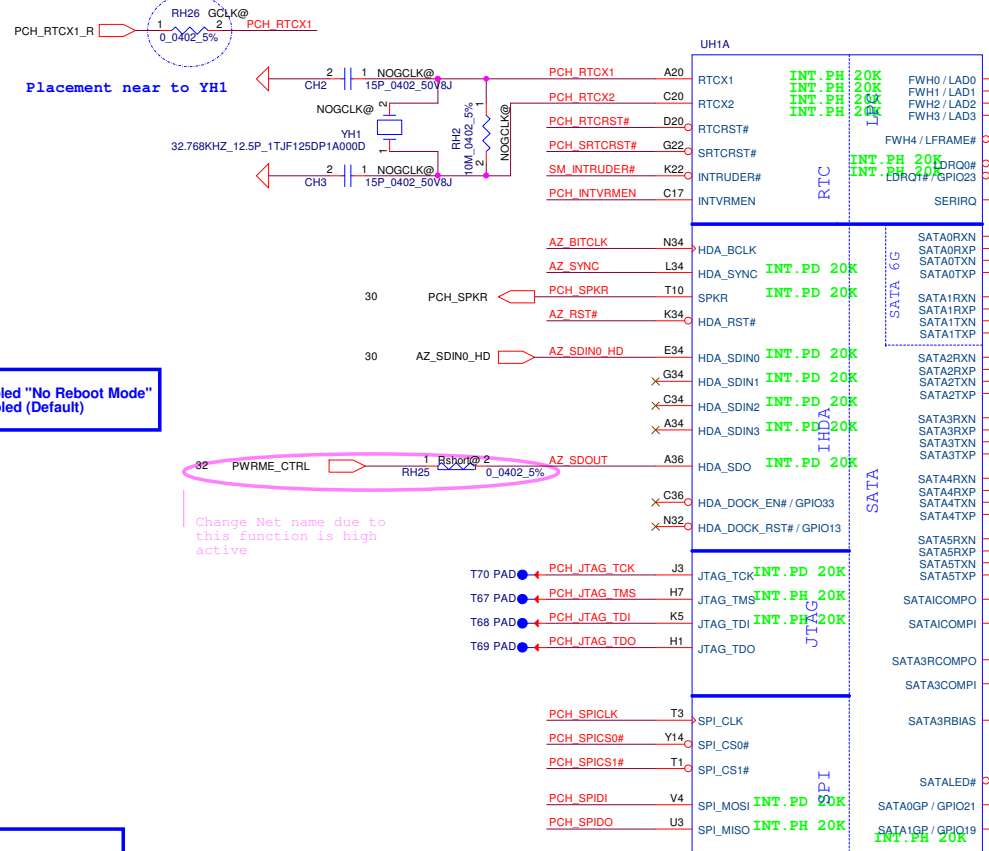
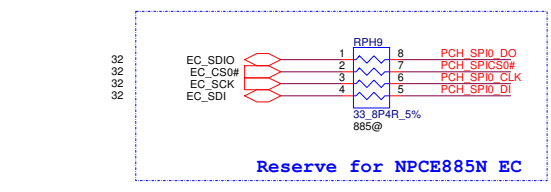
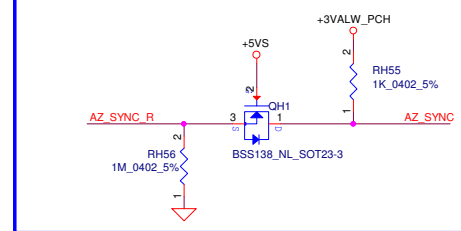


PCH_SPKR
High = Enabled "No Reboot Mode"
Low = Disabled (Default)



HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security override)

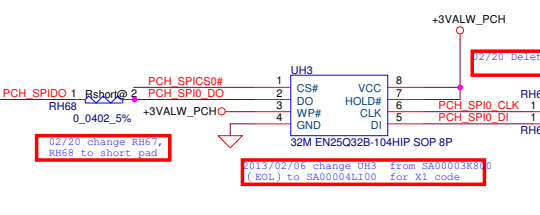
HDA_SYNC
*This signal has a weak internal pull down
H->On Die PLL is supplied by 1.5V
L->On Die PLL is supplied by 1.8V
Need to pull high for Chief River Mobile platform



11/28 Change UH3 from socket to IC, modify the footprint

10/19A Change RH66 to short pad

SPI ROM for BIOS & ME (4MByte)

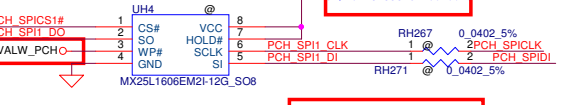


4MB ROM P/N:
SA00003K800
SA00004L100

Socket: SP07000F500/SP07000H900
Please place UH3 & UH4 close to UH1 PCH,
please place RH66, RH67, RH68 near UH3
Please place RH267 near RH66, Please place RH271 near RH67,
Please place RH269 near RH68.

11/29 change UH4 2M ROM circuit to *@*

SPI ROM for Win8 (2MByte)



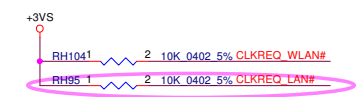
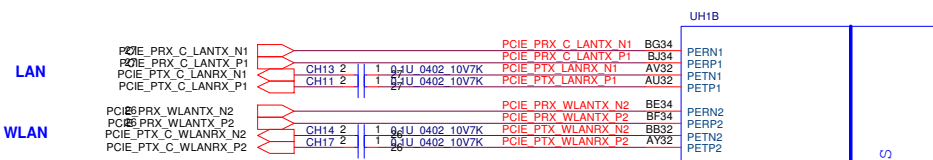
2MB ROM P/N:
SA000041N00
SA00003FO10

10/19A Change RH267 to short pad

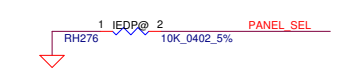
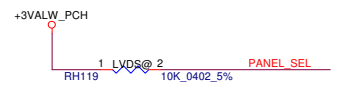
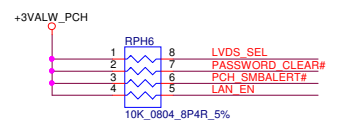
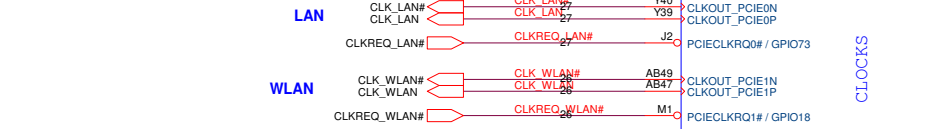
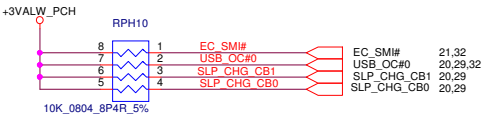
10/19A Remove RH65, CB7

10/19A Remove RH69, CH21

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Document Number	Custom	Customer	VFKTA	Rev	1.0
Date	Monday, March 11, 2013	Sheet	16	of	46



Intel Spec: PCIECLK# RQ0# is suspend well, but we pull high to +3VS for LAN enable/disable function



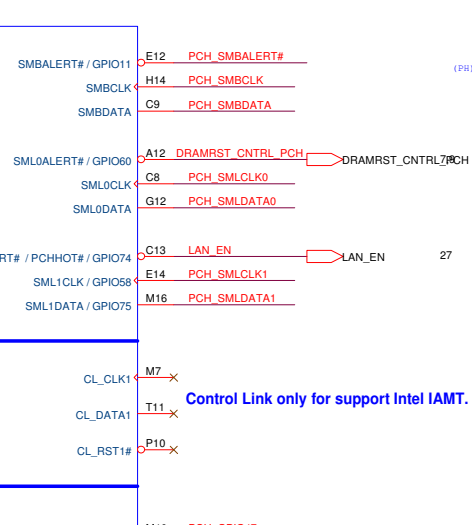
Note: place in DDR area



LVDS_SEL		
LVDS_SEL	H	L
Channel	Single (Default)	Dual

PANEL_SEL		
PANEL_SEL	H	L
Channel	LVDS	EDP

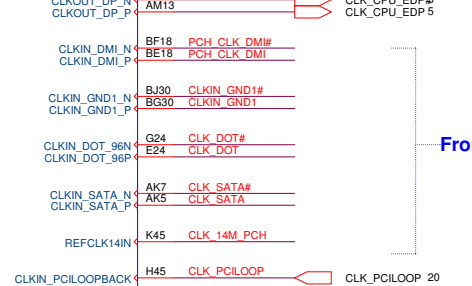
PCH_GPIO67		
PCH_GPIO67	H	L
M/B SKU	UMA	DIS/OPT



Control Link only for support Intel IAMT.

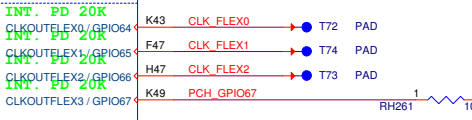


9/28 Delete CLK_VGA, change CLK_REQ_VGA# to PCH_GPIO47

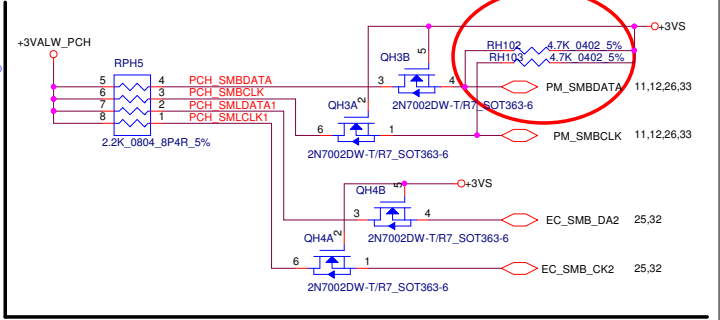


120 Mhz for eDP

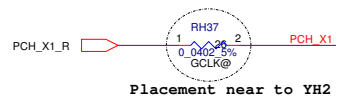
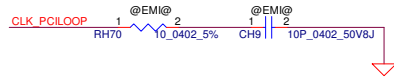
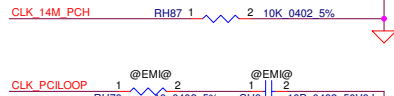
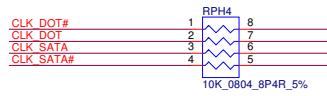
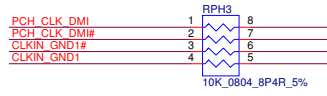
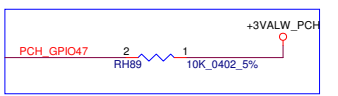
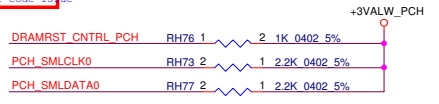
From Clock Gen.



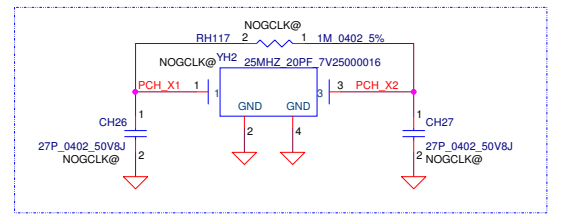
9/28 Change DGPU_PRESENT# to PCH_GPIO67, then pull high to +3VS



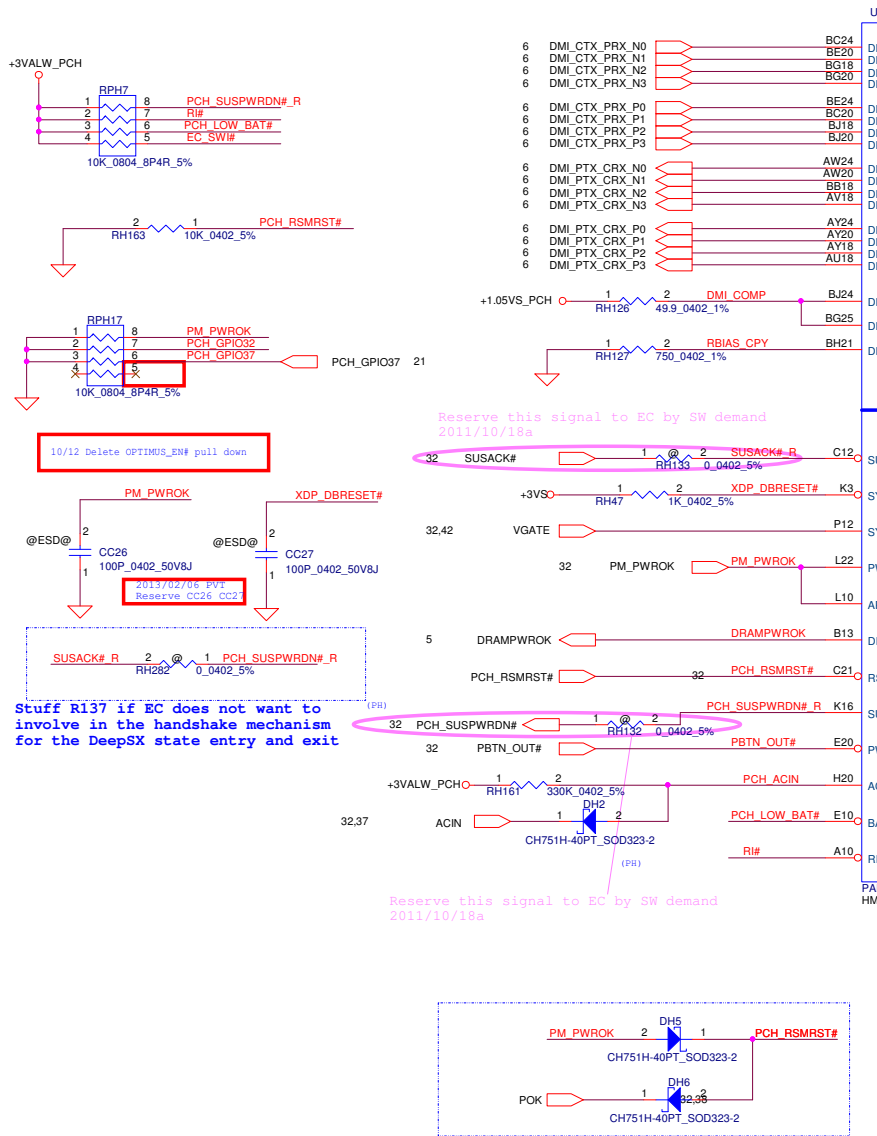
013/02/06 change Qc5,Qb3,Qh4,Qw1, Qc6, Qa1 Qr1 Qs3 from SB00000E010 to SB00000B010 DVT 2nd source for X1 code is 1



Placement near to YH2



Compal common design SW request to add DGPU_Present on this GPIO67



Reserve this signal to EC by SW demand
2011/10/18a

Reserve this signal to EC by SW demand
2011/10/18a

10/12 Delete OPTIMUS_EN# pull down

Stuff R137 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

2013/02/06 EMI Reserve CC26, CC27

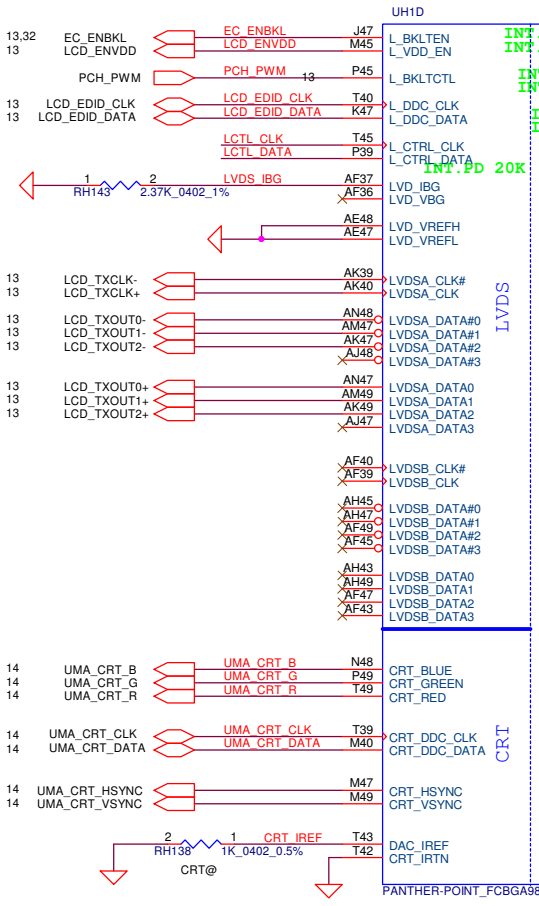
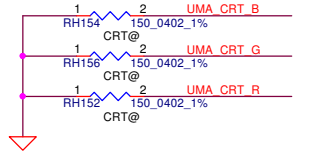
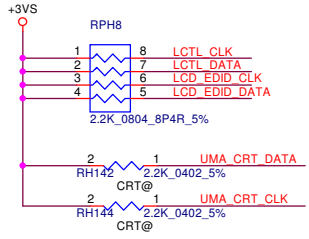
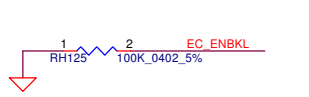
UH1C		DMI		FDI	
6	DMI_CTX_PRX_N0	BC24	DMIORXN	BJ14	FDI_RXN0
6	DMI_CTX_PRX_N1	BE20	DMIHRXN	AY14	FDI_RXN1
6	DMI_CTX_PRX_N2	BG18	DMI2RXN	BE14	FDI_RXN2
6	DMI_CTX_PRX_N3	BG20	DMI3RXN	BH13	FDI_RXN3
6	DMI_CTX_PRX_P0	BE24	DMIORXP	BC12	FDI_RXN4
6	DMI_CTX_PRX_P1	BC20	DMIHRXP	BJ12	FDI_RXN5
6	DMI_CTX_PRX_P2	BJ18	DMI2RXP	BG10	FDI_RXN6
6	DMI_CTX_PRX_P3	BJ20	DMI3RXP	BG9	FDI_RXN7
6	DMI_PTX_CRX_N0	AW24	DMIOTXN	BG14	FDI_RXP0
6	DMI_PTX_CRX_N1	AW20	DMIHTXN	BB14	FDI_RXP1
6	DMI_PTX_CRX_N2	BB18	DMI2TXN	BF14	FDI_RXP2
6	DMI_PTX_CRX_N3	AY18	DMI3TXN	BG13	FDI_RXP3
6	DMI_PTX_CRX_P0	AY24	DMIOTXP	BE12	FDI_RXP4
6	DMI_PTX_CRX_P1	AY20	DMIHTXP	BG12	FDI_RXP5
6	DMI_PTX_CRX_P2	AY18	DMI2TXP	BJ10	FDI_RXP6
6	DMI_PTX_CRX_P3	AU18	DMI3TXP	BH9	FDI_RXP7
		BJ24	DMI_ZCOMP	AW16	FDI_INT
		BG25	DMI_IRCOMP	AV12	FDI_FSYNC0
		BH21	DMI2RBIAS	BC10	FDI_FSYNC1
				AV14	FDI_LSYNC0
				BB10	FDI_LSYNC1
				A18	DSWVREMEN
				E22	DPWRCK
				B9	WAKE#
				N3	CLKRUN# / GPIO32
				G8	SUS_STAT# / GPIO61
				N14	SUSCLK / GPIO62
				D10	SLP_S5# / GPIO63
				H4	SLP_S4#
				F4	SLP_S3#
				G10	SLP_A#
				G16	SLP_SUS#
				AP14	PMSYNCH
				K14	SLP_LAN# / GPIO29

System Power Management

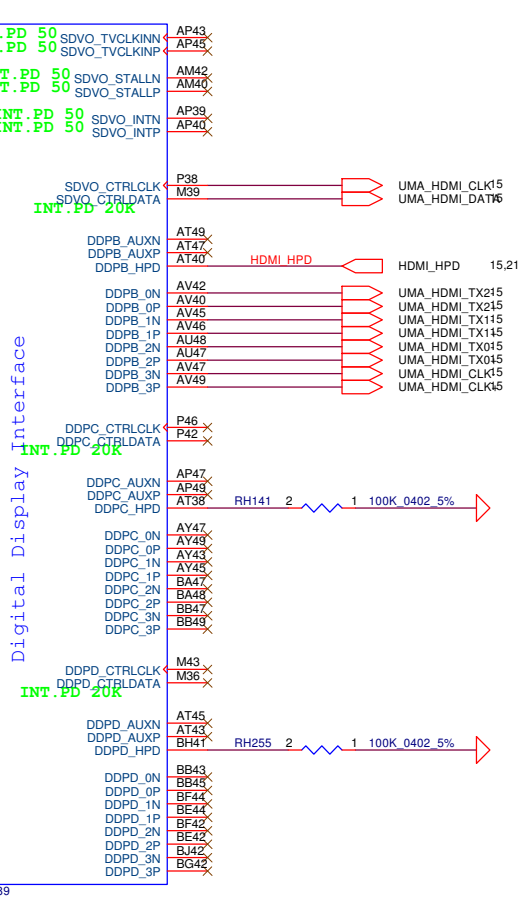
PCH_DPWRCK RH128 0.0402_5% PCH_RSMRST#
Do not support DeepSX state

DSWVREMEN RH150 2 330K 0.402 5% +RTCVCC
DSWVREMEN must be always pulled high to +RTCVCC
DSWVREMEN - Internal Deep Sleep 1.05V regulator
* H : Enable
L : Disable

Follow EC check list demand, but don't implement CLKRUN# this function



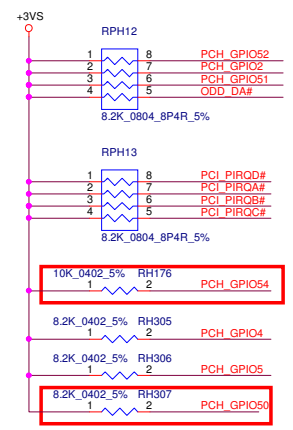
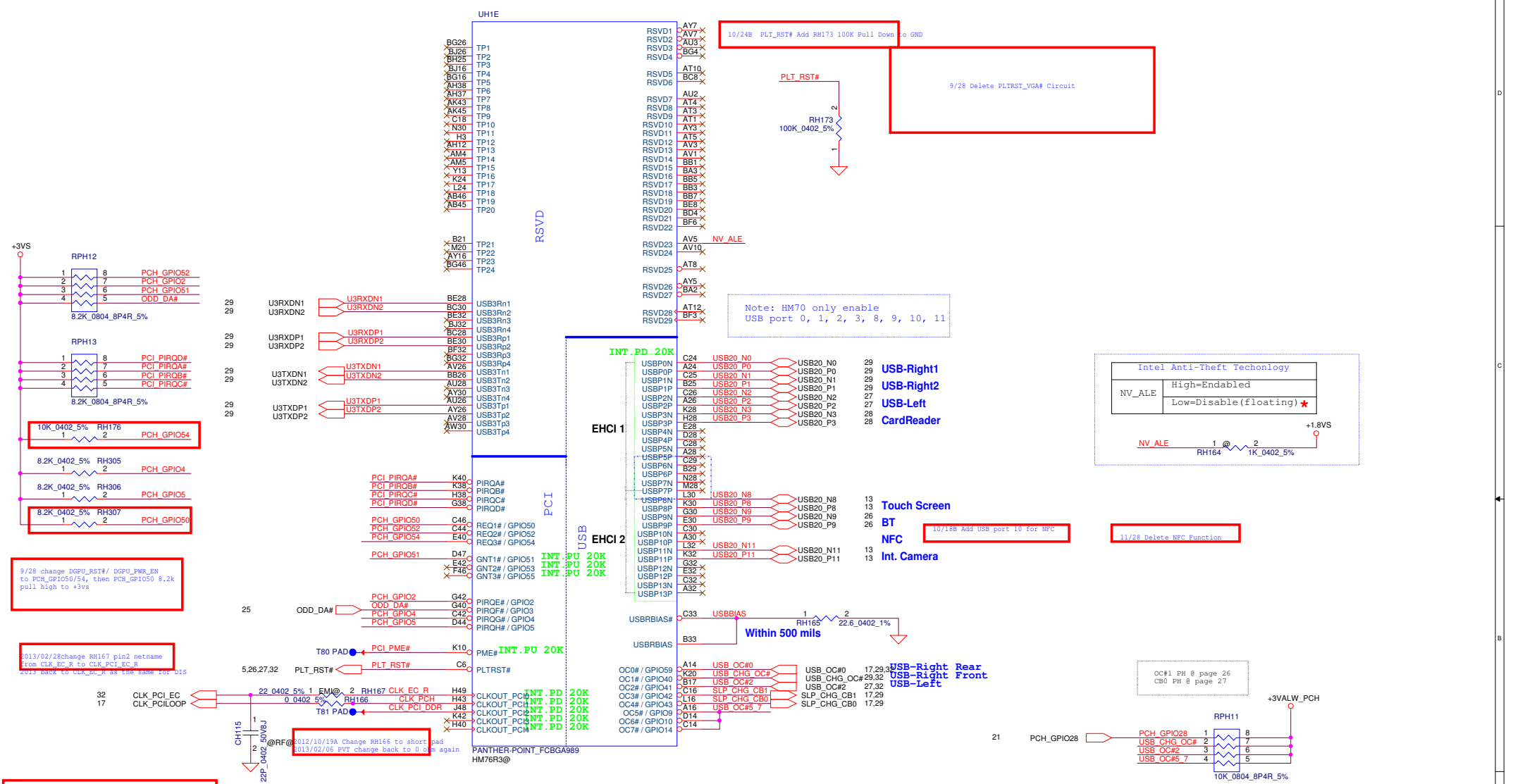
RH138
1K_0402_5%
NOCRT@



02/20 Delete RH254 100K

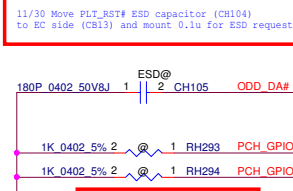
HDMI

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Size	Document Number	Rev		1.0	
Custom	VFKTA	Date:		Monday, March 11, 2013	
				Sheet	19 of 46



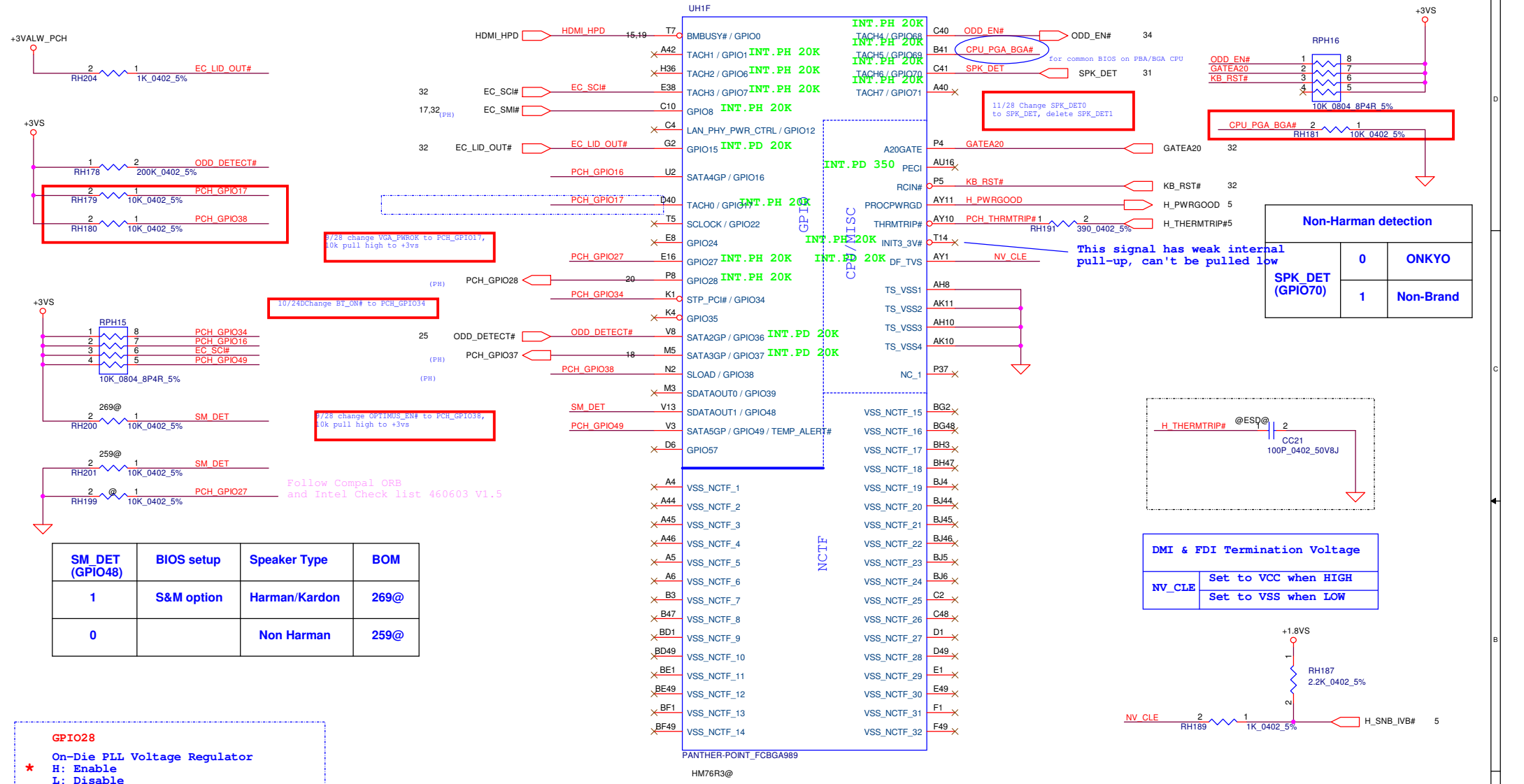
9/28 change DGPU_RST# / DGPU_PWR_EN to PCH_GPIO50/54, then PCH_GPIO50 8.2k pull high to +3vs

013/02/28change RH167 pin2 netname from CLK_EC_R to CLK_PCI_EC_R
2013 back to CLK_EC_R as the same for D15



Boot BIOS Strap		
PCH_GPIO51	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
*	Low= A16 swap override Enable High= A16 swap override Disable



7/28 change VGA_PWROK to PCH_GPIO17, 10k pull high to +3vs

10/24/0 Change BT_ON# to PCH_GPIO34

7/28 change OPTIMUS_EN# to PCH_GPIO38, 10k pull high to +3vs

Follow Compal ORB and Intel Check list 460603 V1.5

11/28 Change SPK_DET0 to SPK_DET, delete SPK_DET1

SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

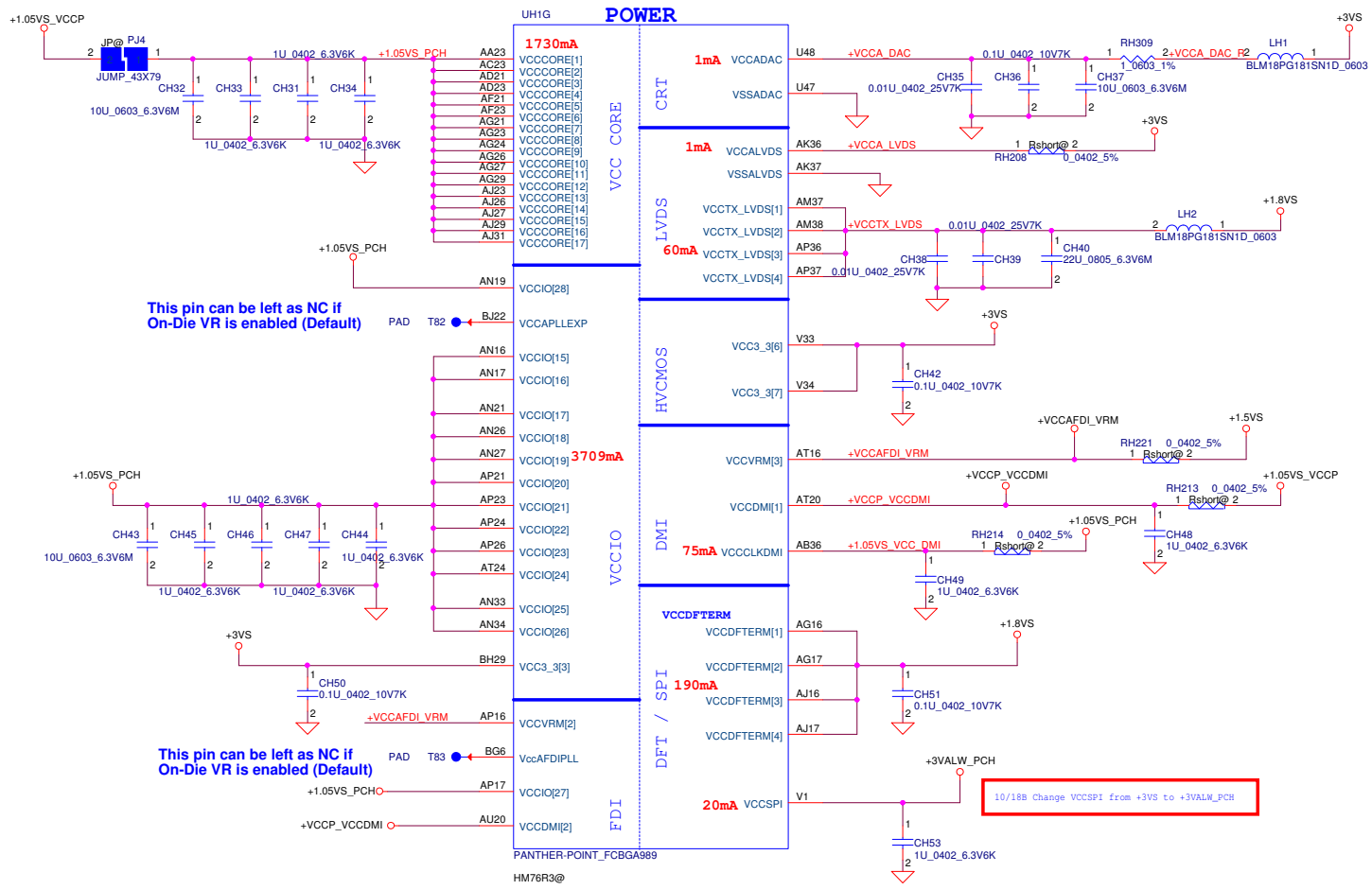
Non-Harman detection	
SPK_DET (GPIO70)	0 ONKYO
	1 Non-Brand

DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

GPIO28
 * On-Die PLL Voltage Regulator
 H: Enable
 L: Disable

GPIO8
 Integrated Clock Chip Enable (Removed)
 H: Disable
 * L: Enable

OPTIMUS_EN#		
OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

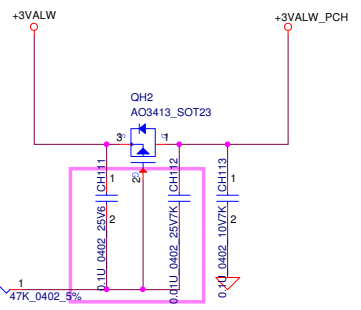


This pin can be left as NC if On-Die VR is enabled (Default)

This pin can be left as NC if On-Die VR is enabled (Default)

10/188 Change VCCSPI from +3VS to +3VALW_PCH

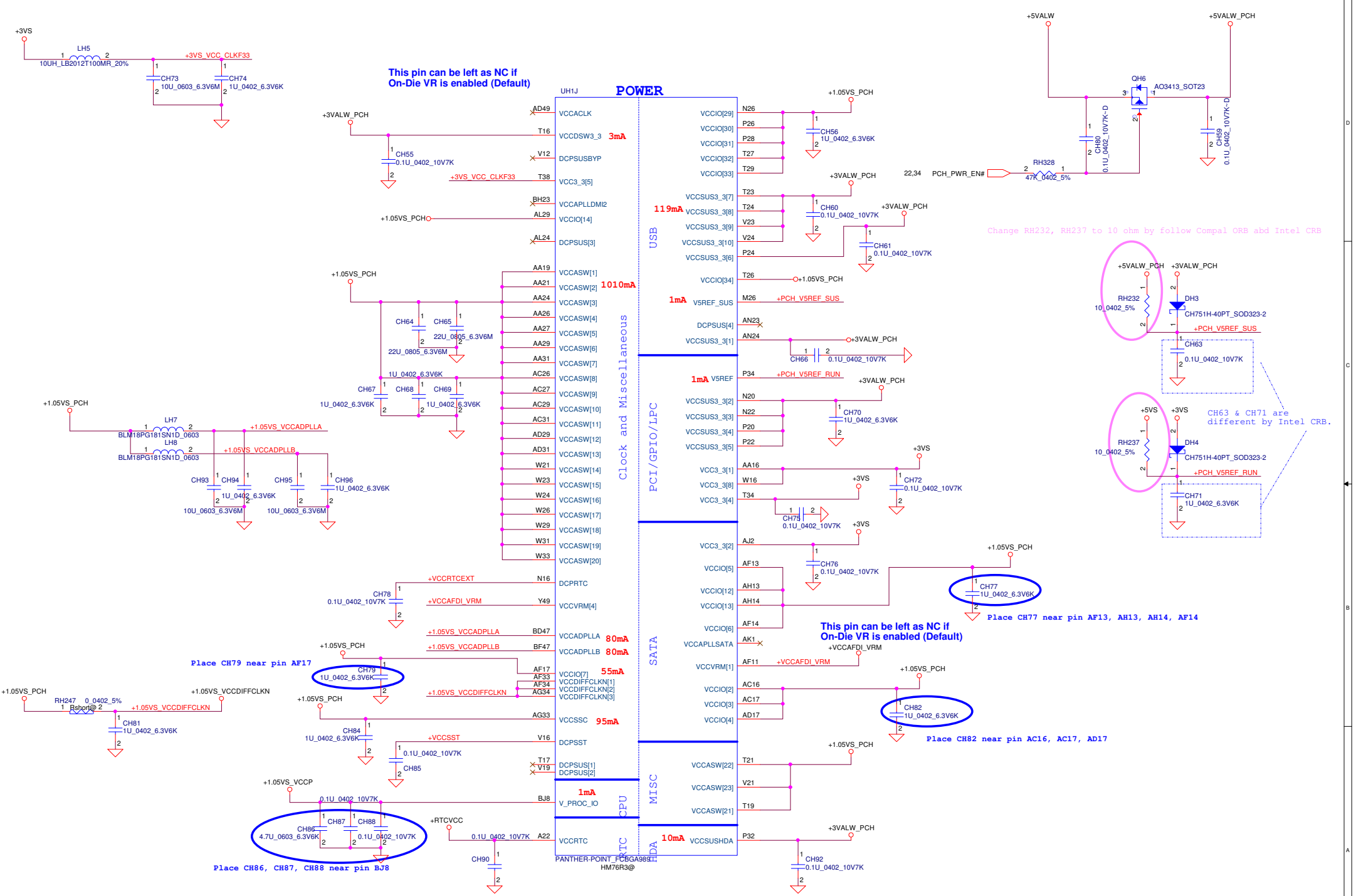
+3VALW to +3VALW_PCH



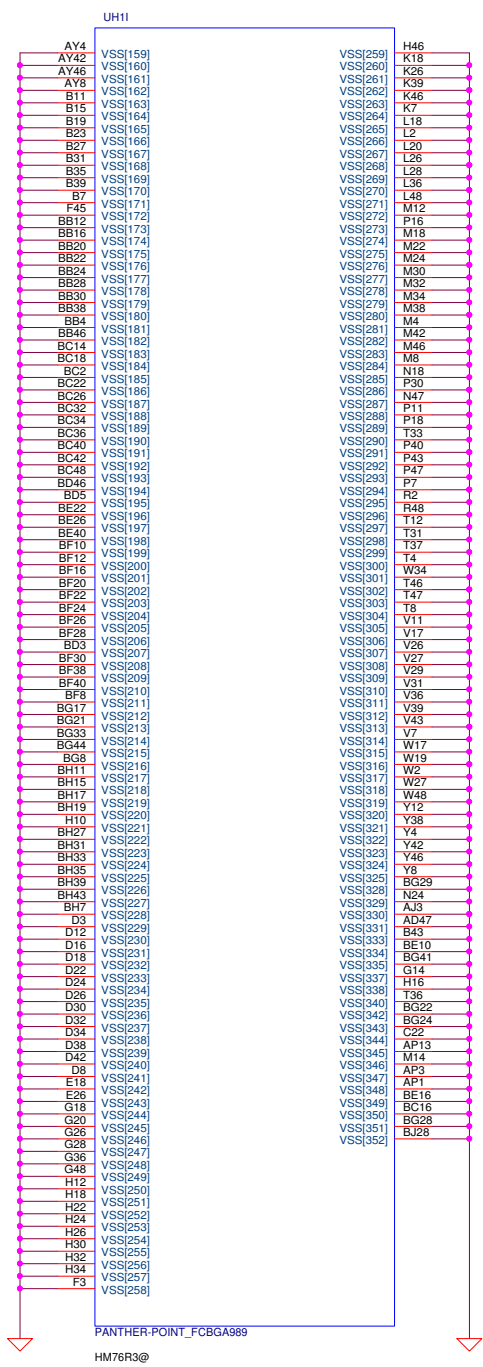
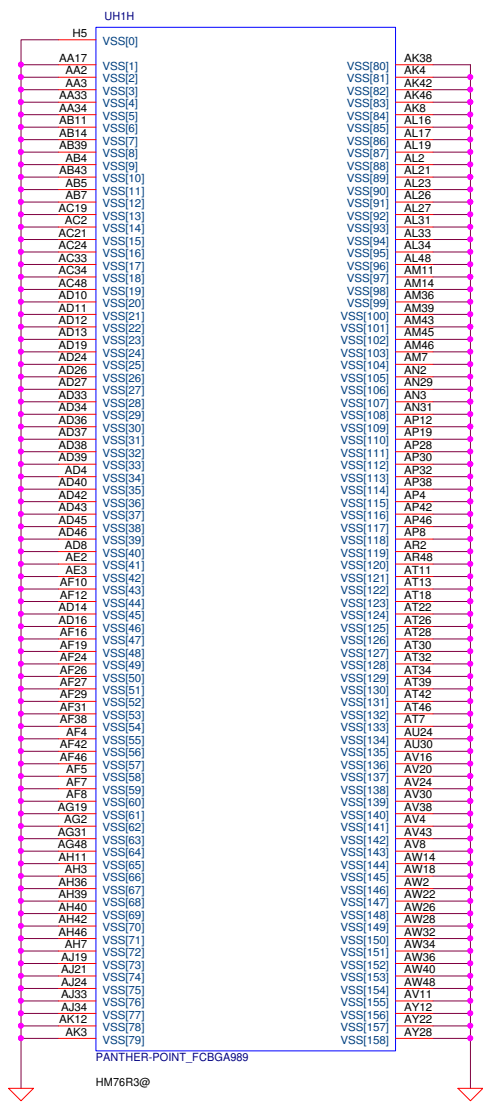
PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

23.34 PCH_PWR_EN# PCH_PWR_EN#

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				Sheet 22 of 46 Rev 1.0

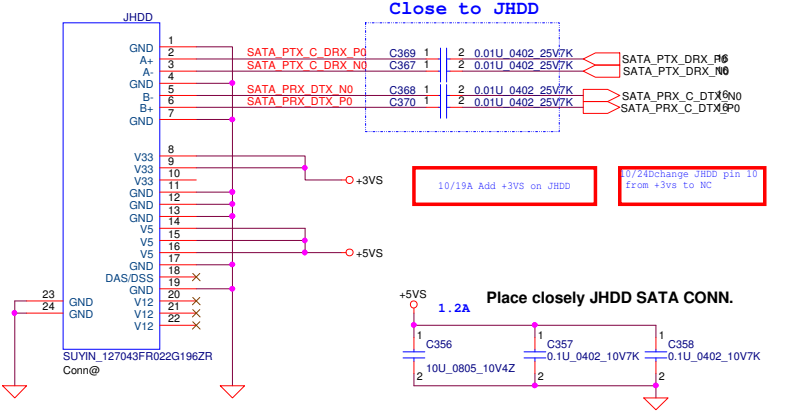


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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				PCH_POWER-2
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			Document Number VFKTA	Sheet 23 of 46
				Date: Monday, March 11, 2013

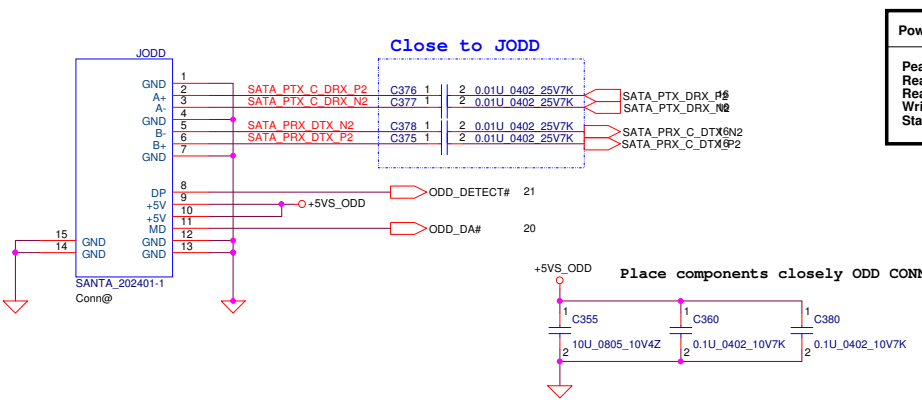


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Date:	Monday, March 11, 2013	Sheet	24	of 46

SATA HDD Conn.

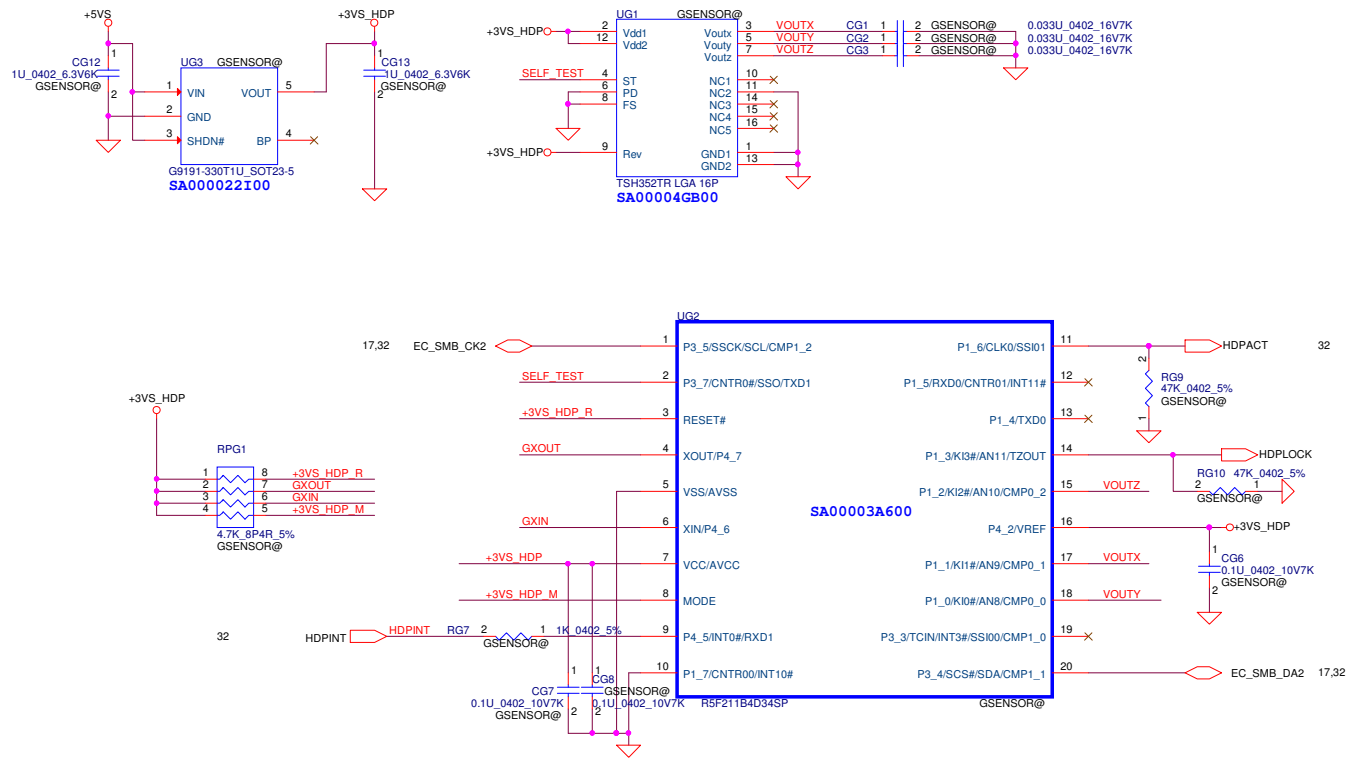


SATA ODD Conn

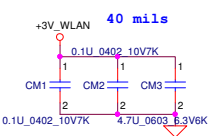


Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

G-Sensor



Slot 1 Half PCIe Mini Card-WLAN



Reserve +1.5 power rail & cap. to support unknown keypart.

10/24 Remove +1.5V on WLAN pin6/28/48, delete CM7, CM8 Delete RM22 (EC will programming H/L)

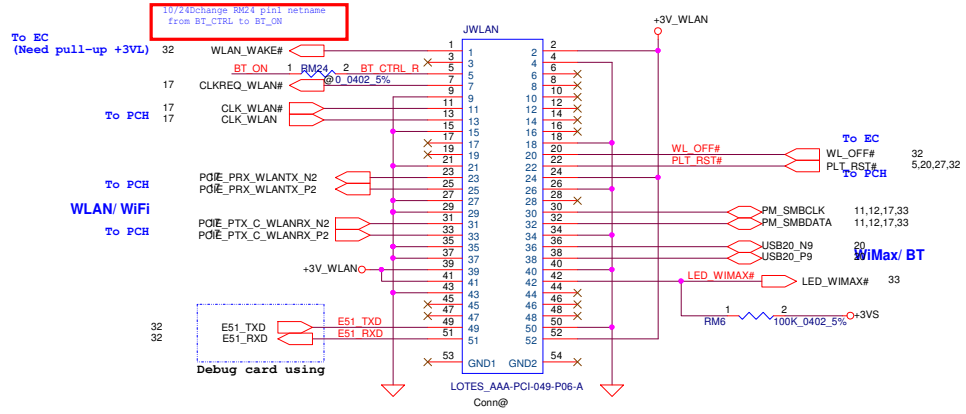
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

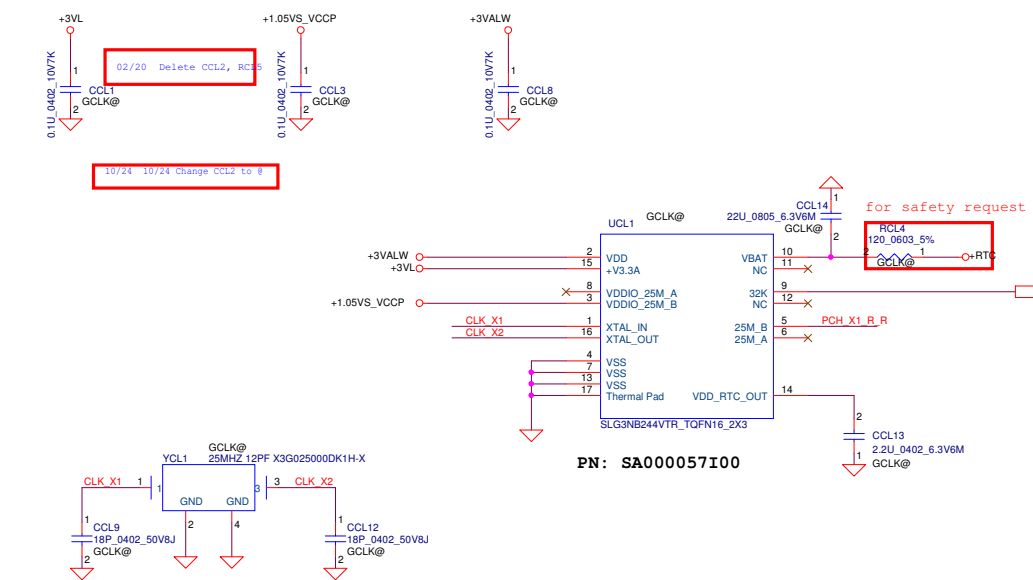
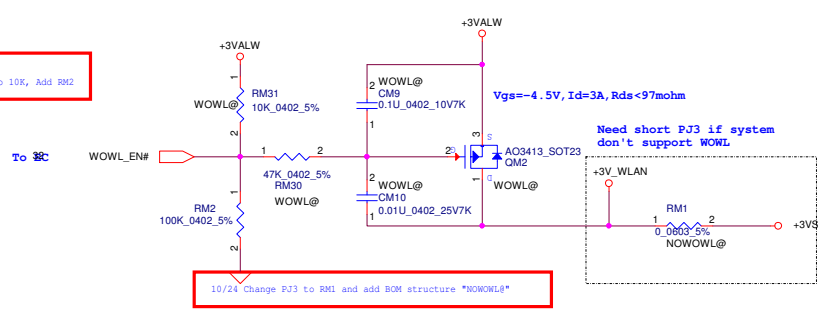
10/24: Delete CM1, change BT_ON design

From 32: BT_ON → BT_ON → 1 RM27 2 E51 RXD → 1K_0402_5%

For isolate BT_ON and Compal Debug Card.



+3VALW TO +3V_WLAN for WOWL

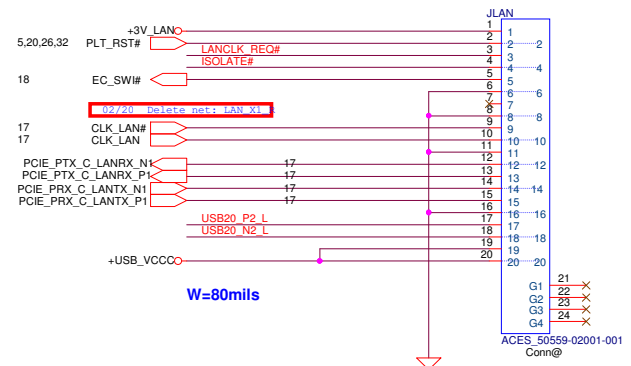
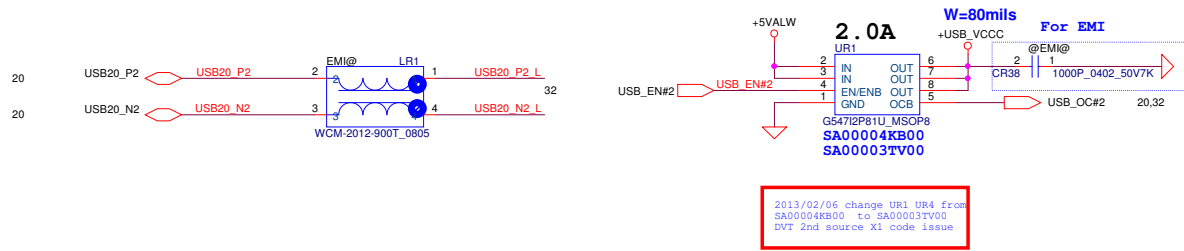


10/24 Change CCL2 to 8

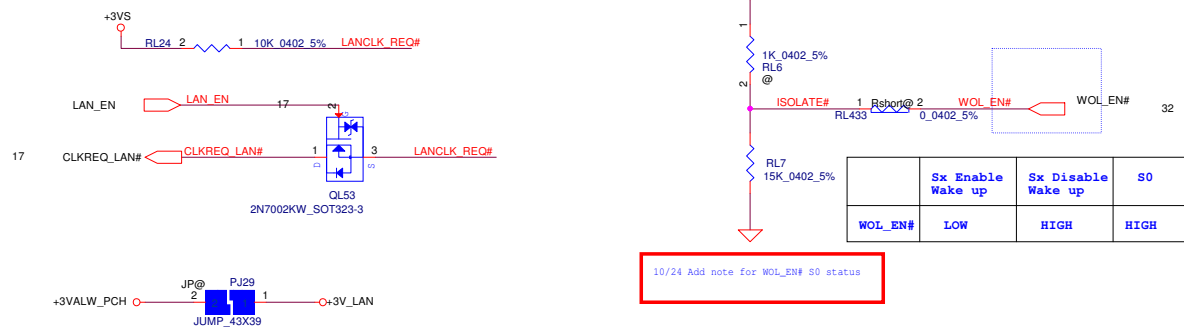
10/19A Change Rcl2 to short pad

02/20 Delete RCL2 LAN_X1_R_B, LAN_X1_R

Left USB 2.0 x 1



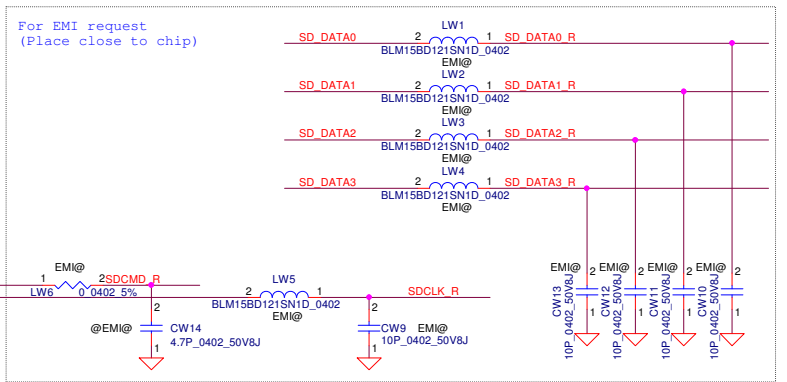
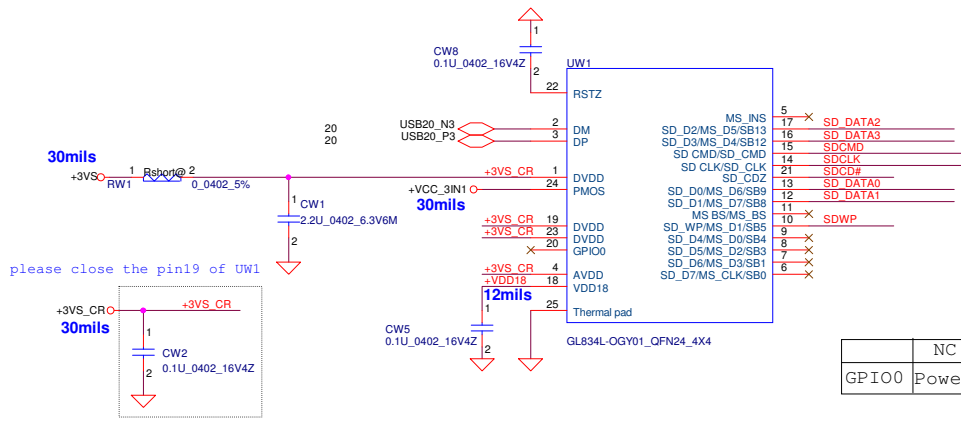
For LAN function



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

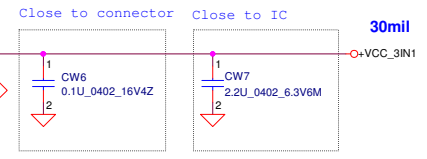
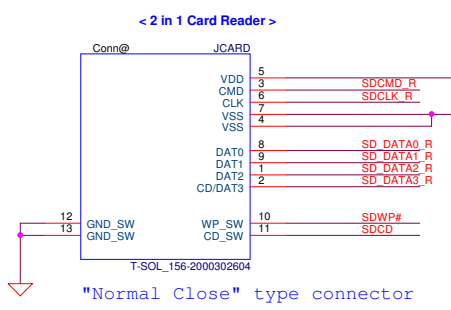
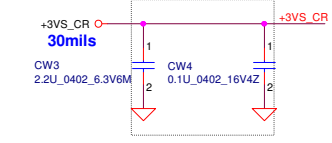
LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

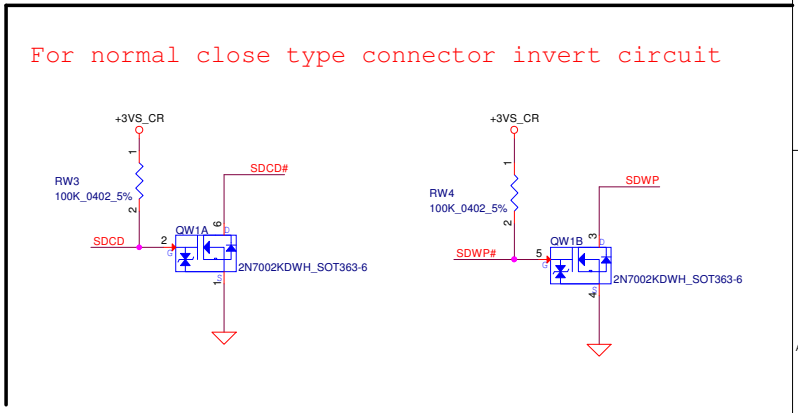


GPIO0	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

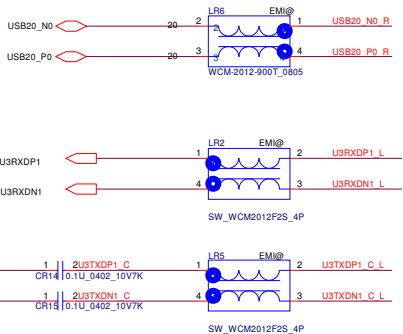


USB Sleep & Charge

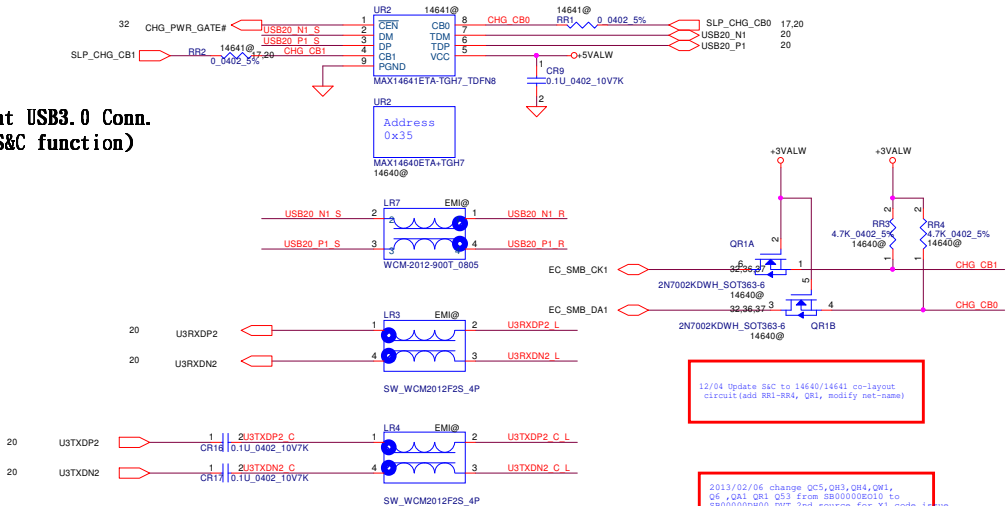
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode. DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

12/05 SAC TC Pin1 was connected to the KC(IP1049) Pin82.

Right rear USB3.0 Conn.



Right front USB3.0 Conn. (Support S&C function)



2013/02/06 change LR2, LR3, LR4, LR5 from SMD70001000 to SMD70001800 DVT 2nd source for XI code issue

02/22 S&C Check pin1 USTXDN2 to CR17 pin1 U3TXDP2

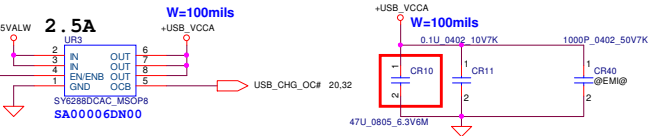
11/28 change CR10, CR12 from 47u 1206 to 0805 size (SB00000PFL00)

12/04 Update SAC to 14640/14641 co-layout circuit (add RRI-RR4, QR1, modify net-name)

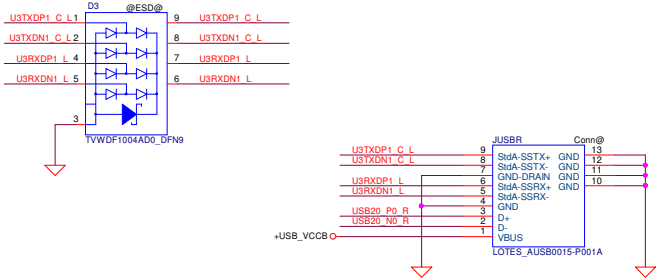
2013/02/06 change QC5, QR1, QR4, QR1, QR6, QR1, QR1 Q53 from SB00000E0D10 to SB00000D000 DVT 2nd source for XI code issue

2013/02/06 change UR1, UR4 to SA00004KB00 to SA00003TY00 DVT 2nd source XI code issue

02/20 Delete CR7, CR8

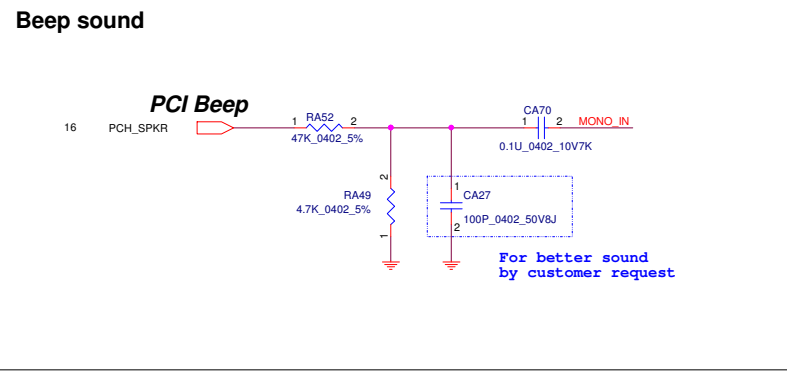
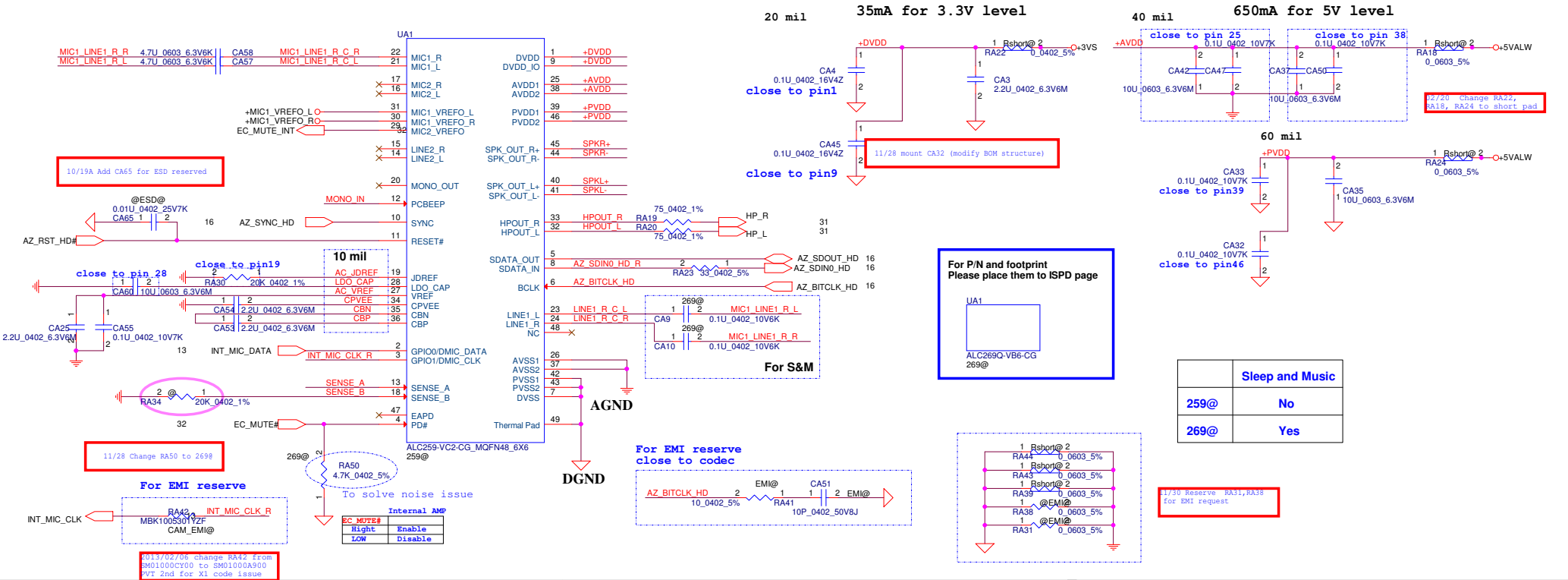


10/22A ESD request Delete DR1, DR2

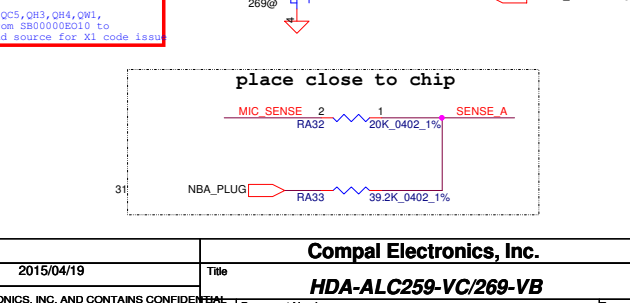
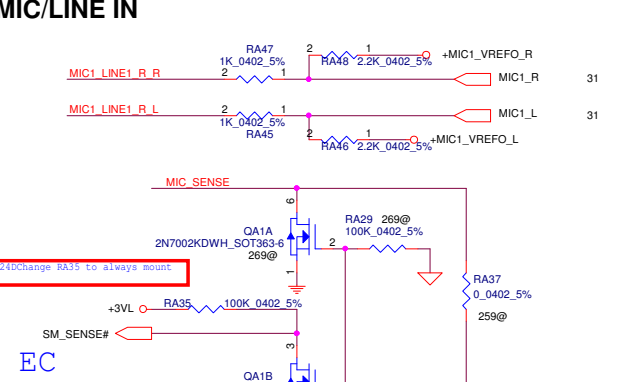
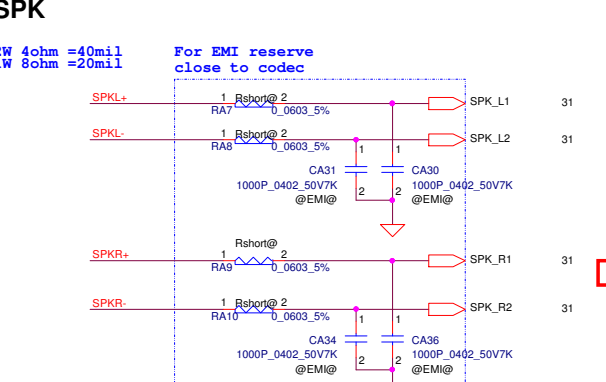


10/22A ESD request Delete DR1, DR2

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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



SPK Conn.

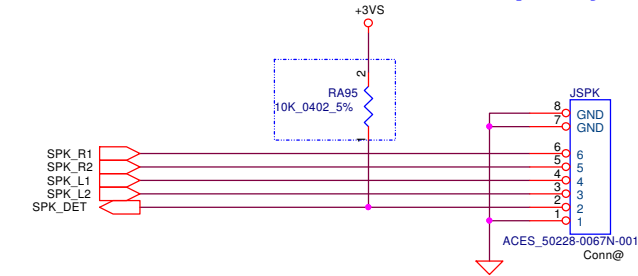
For common design, pull-high resistor should be placed at connector side.

10/19A Follow the latest connector list to change SPK footprint, The ME drawing with new JSPK will be updated 10/20

SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

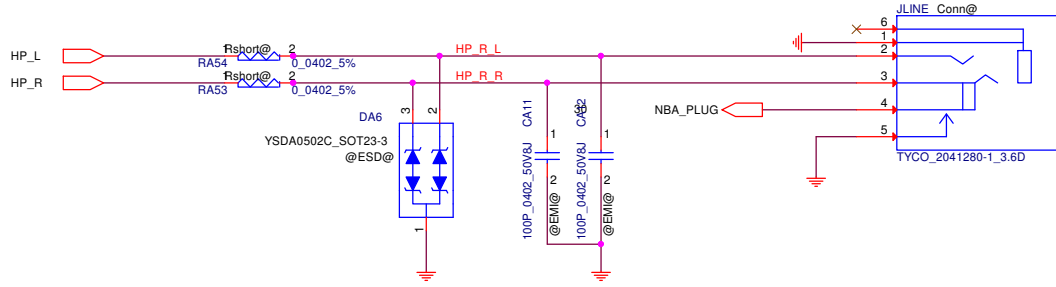
Non-Harman detection		
SPK_DET (GPIO70)	0	ONKYO
	1	Non-Brand

11/28 Change SPK connector to 6 pin, change SPK_DET0 to SPK_DET, delete SPK_DET1 and RA96



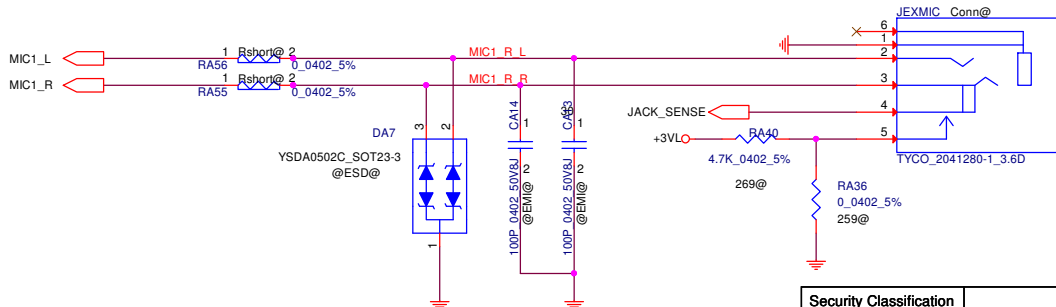
10/22A ESD request Delete DA5, DA8 covered by ME design

HeadPhone/LINE Out JACK

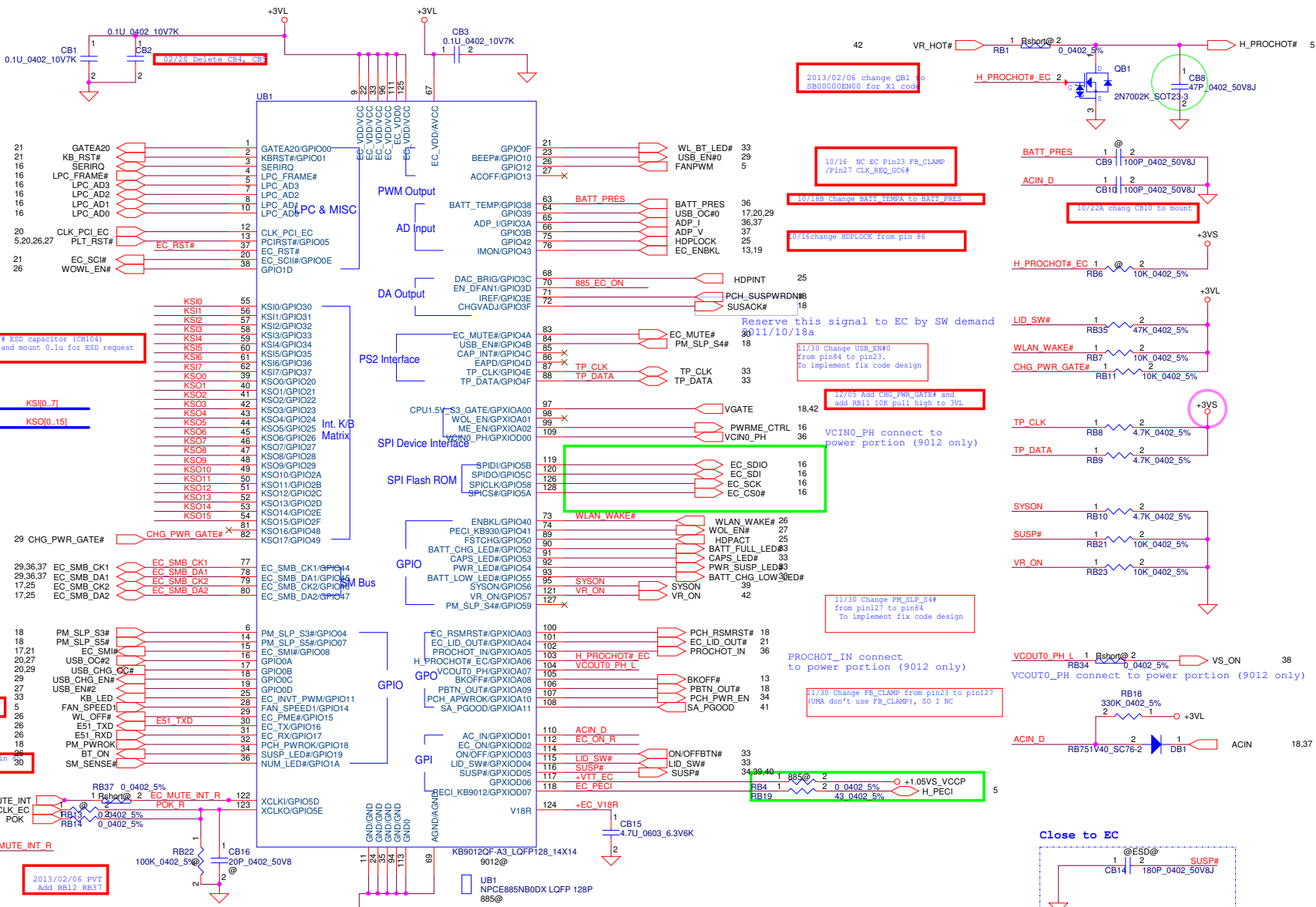
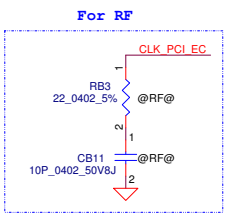


10/24 Change RA53-56 to short pad.....again.....-

MIC/LINE IN JACK



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11/30 Move PLT_RST# ESD capacitor (CB104) to EC side (CB13) and mount 0.1u for ESD request

2013/02/06 change CB1 to 47P for X1 code

10/16 NC EC Pin23 FB_CLAMP /Pin27 CLK_RST_GCS#

10/18 change BATT_TEMP to BATT_PRES

10/16 change HDLOCK from pin 86

12/05 Add CHG_PWR_GATE# and add RB11 10K pull high to +3VL

11/30 Change PM_SLP_S4# from pin127 to pin54 To implement fix code design

PROCHOT_IN connect to power portion (9012 only)

11/30 Change FB_CLAMP from pin23 to pin121 (UMA don't use FB_CLAMP), so I NC

11/28 Change RB36 from 2.2k to 0 ohm and CB50 to 0

Close to EC

2013/02/06 PVT Reserve CC21 CC23 CC24 CC25 CC26 CC27, ABD CC35 CC20 main source SCV00001R00, 2nd source SCV21005 10

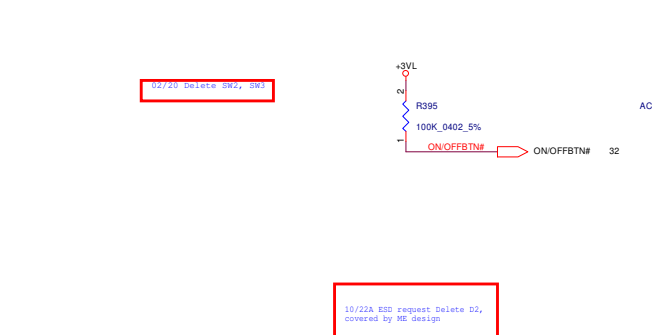
Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109	>1.2V	<1.2V
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)

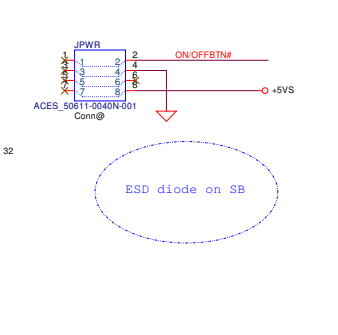
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	1.0
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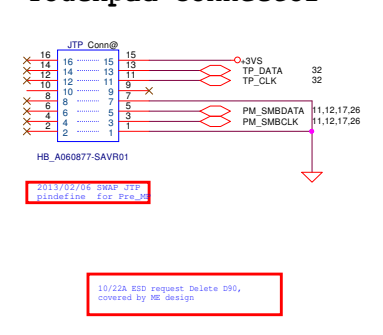
Power Button



Conn.



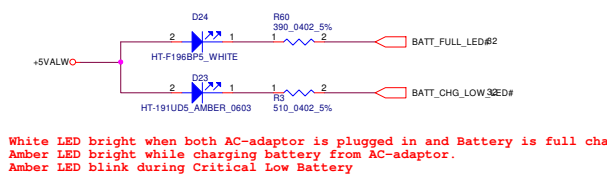
Touchpad Connector



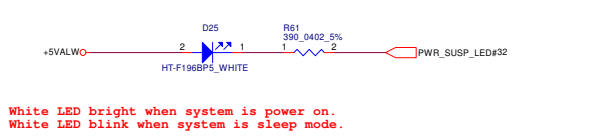
NFC



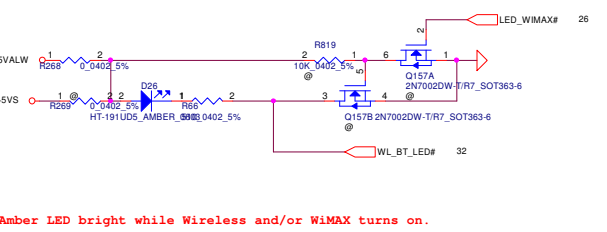
BATT CHARGE /FULL LED



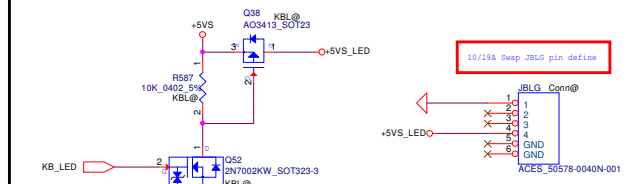
POWER LED



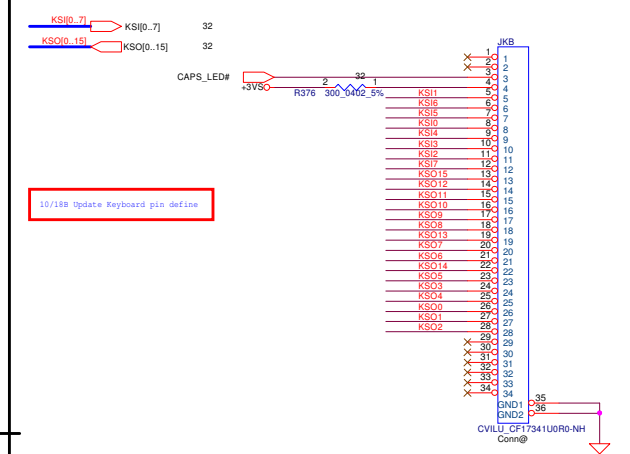
WLAN/WiMAX LED



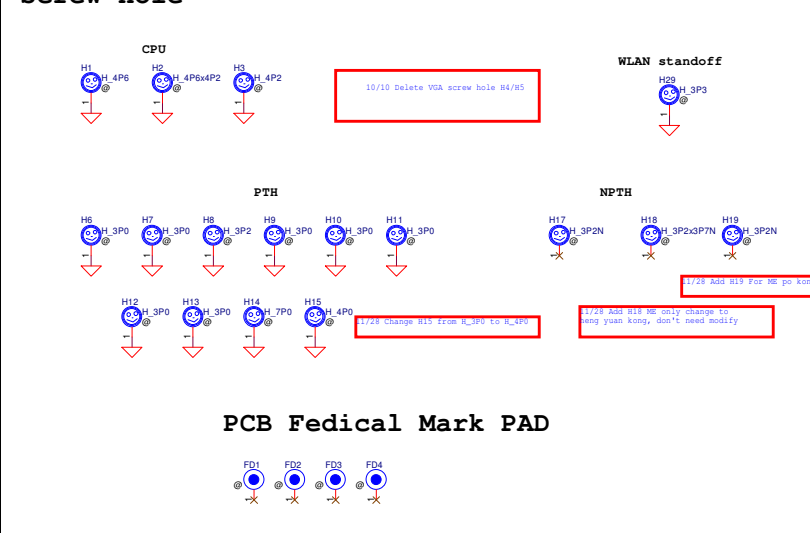
Keyboard LED



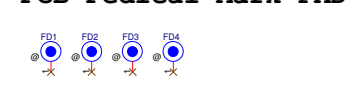
KEYBOARD CONN.



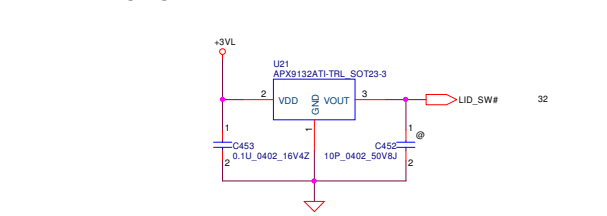
Screw Hole



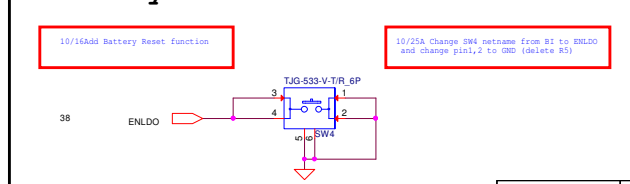
PCB Federal Mark PAD



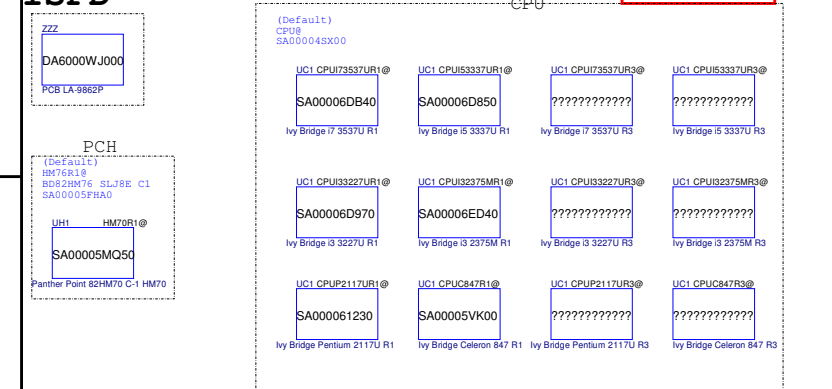
Lid SW



Battery Reset

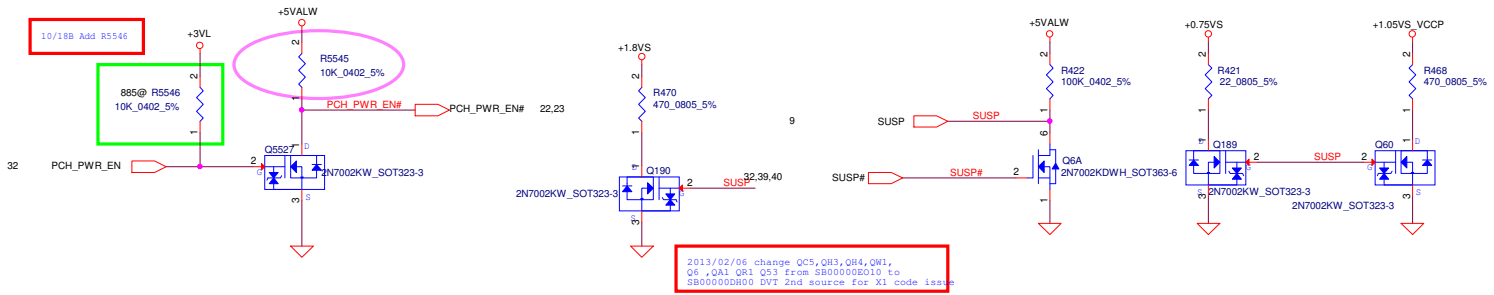
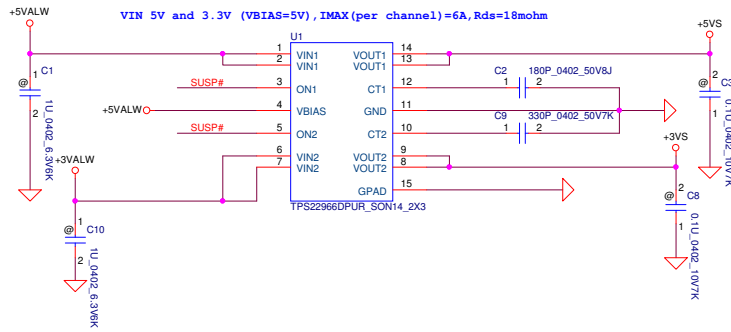


ISP

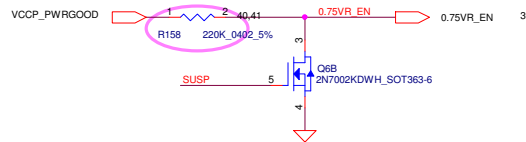


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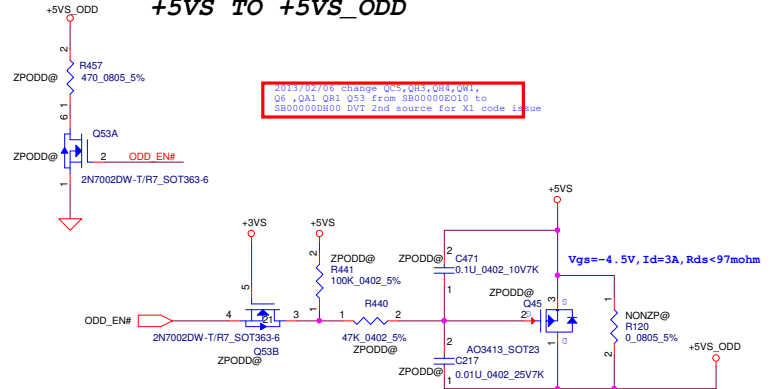
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



For S3 CPU Power Saving

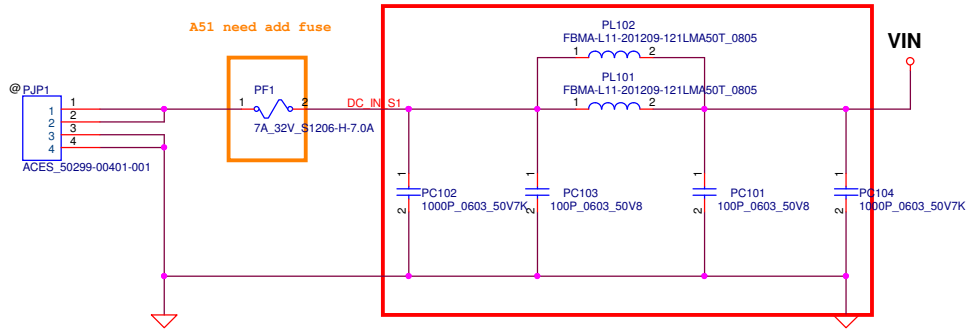


+5VS TO +5VS_ODD



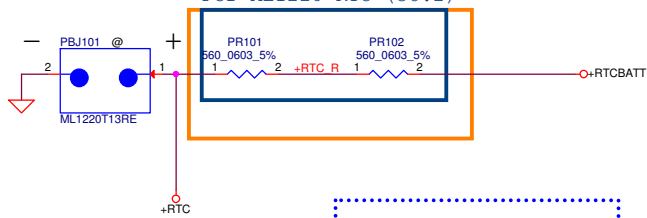
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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title
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EMI Part (47.1)



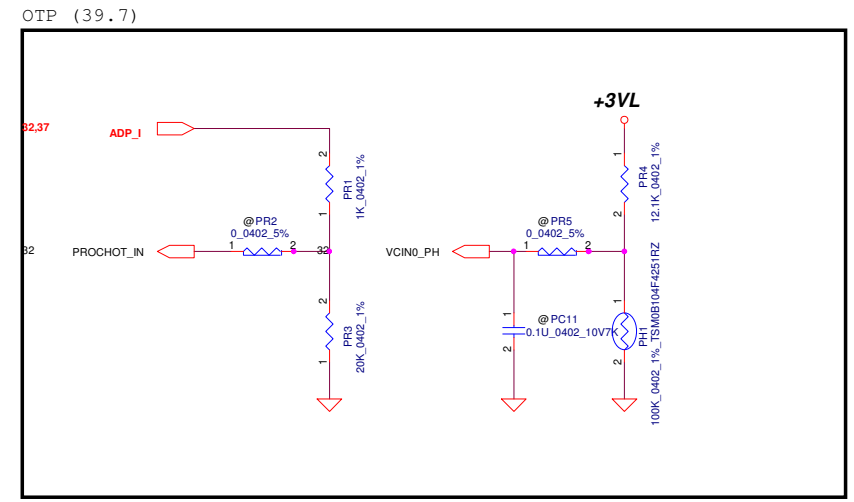
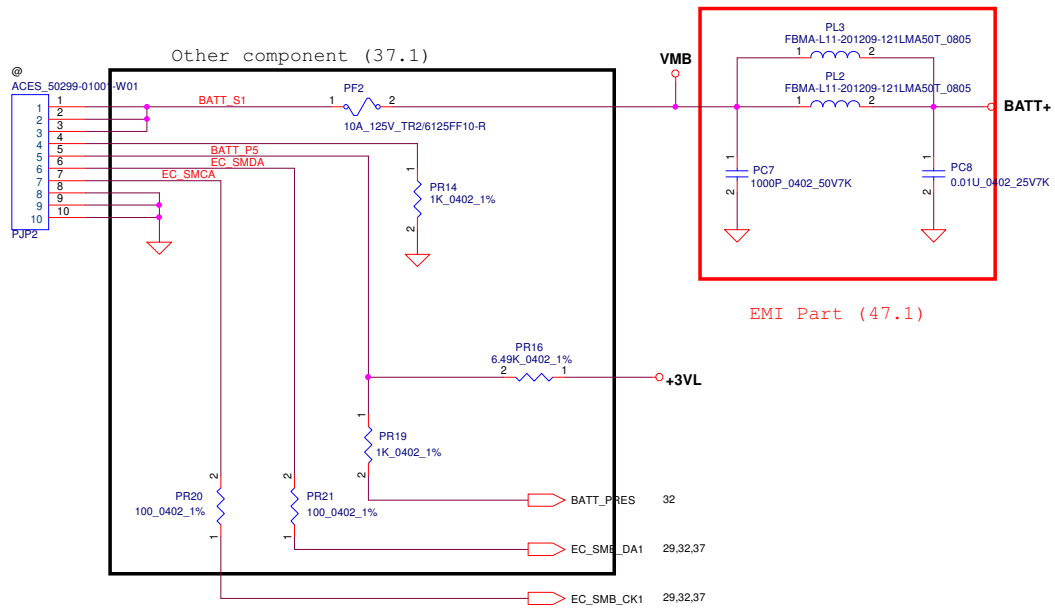
A51 need add fuse

For ML1220 RTC (38.2)



01/17: Change PBJ101 footprint to BJ_ML1220T10_2P

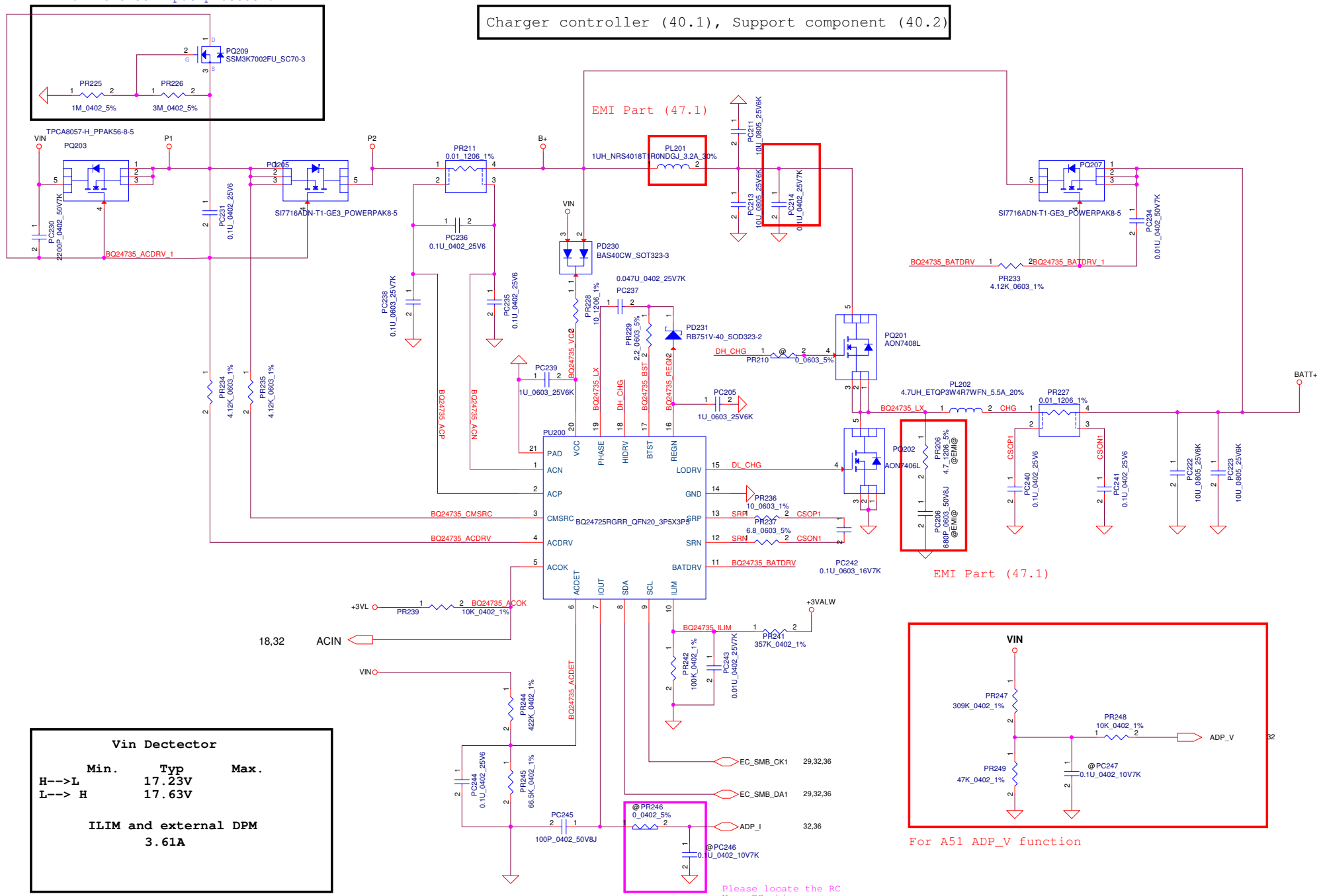
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	DCIN/PRECHARGE	
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for reverse input protection

Charger controller (40.1), Support component (40.2)

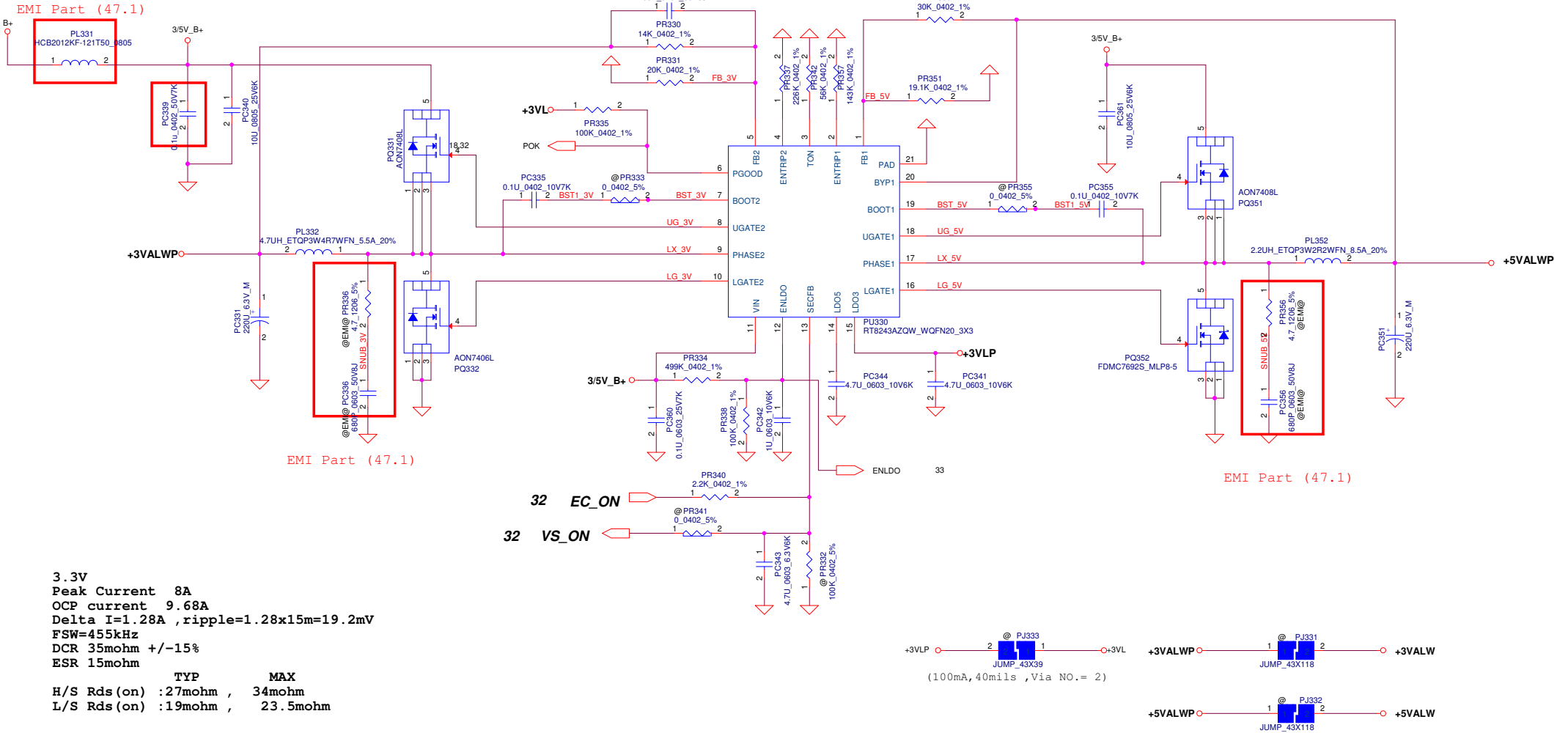


Vin Dectector			
	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	
ILIM and external DPM			
3.61A			

Please locate the RC Near EC chip 2011-02-22

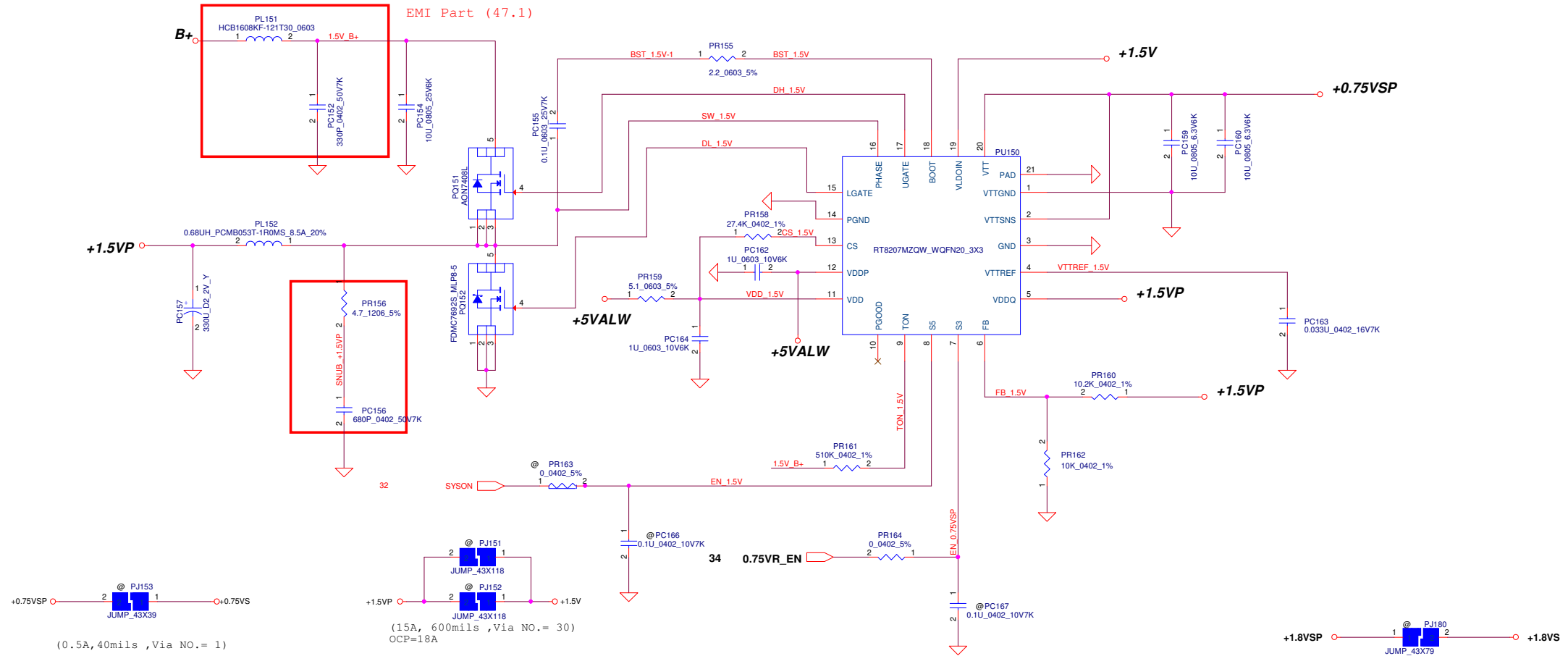
Security Classification		Compal Secret Data		Title	
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5V
 Peak Current 10A
 OCP current 12.03A
 FSW=390kHz
 Delta I=4.29A, ripple=4.29*17m=72.93mV
 DCR 15.5mohm+/-15%
 ESR 17mohm
 TYP MAX
 H/S Rds (on) :27mohm , 34mohm
 L/S Rds (on) :10.8mohm , 13.6mohm



3.3V
 Peak Current 8A
 OCP current 9.68A
 Delta I=1.28A , ripple=1.28x15m=19.2mV
 FSW=455kHz
 DCR 35mohm +/-15%
 ESR 15mohm
 TYP MAX
 H/S Rds (on) :27mohm , 34mohm
 L/S Rds (on) :19mohm , 23.5mohm

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Date:	Sheet	38	of	46



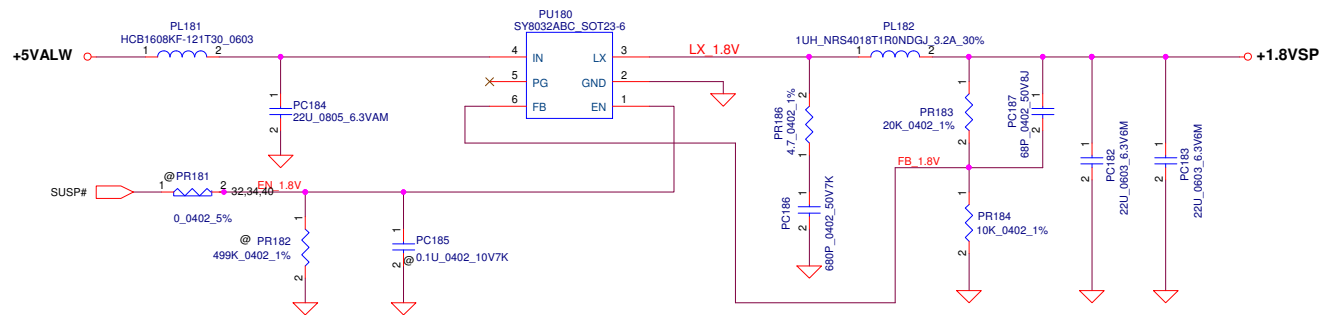
1.5V
Peak Current 16.8A
OCP current 20 A
FSW=495kHz
DCR 13mohm
ESR 9mohm

	TYP	MAX
H/S Rds (on)	:27mohm	34mohm
L/S Rds (on)	:10.8mohm	13.6mohm

STATE	S3	S5	1.5VP	VIT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

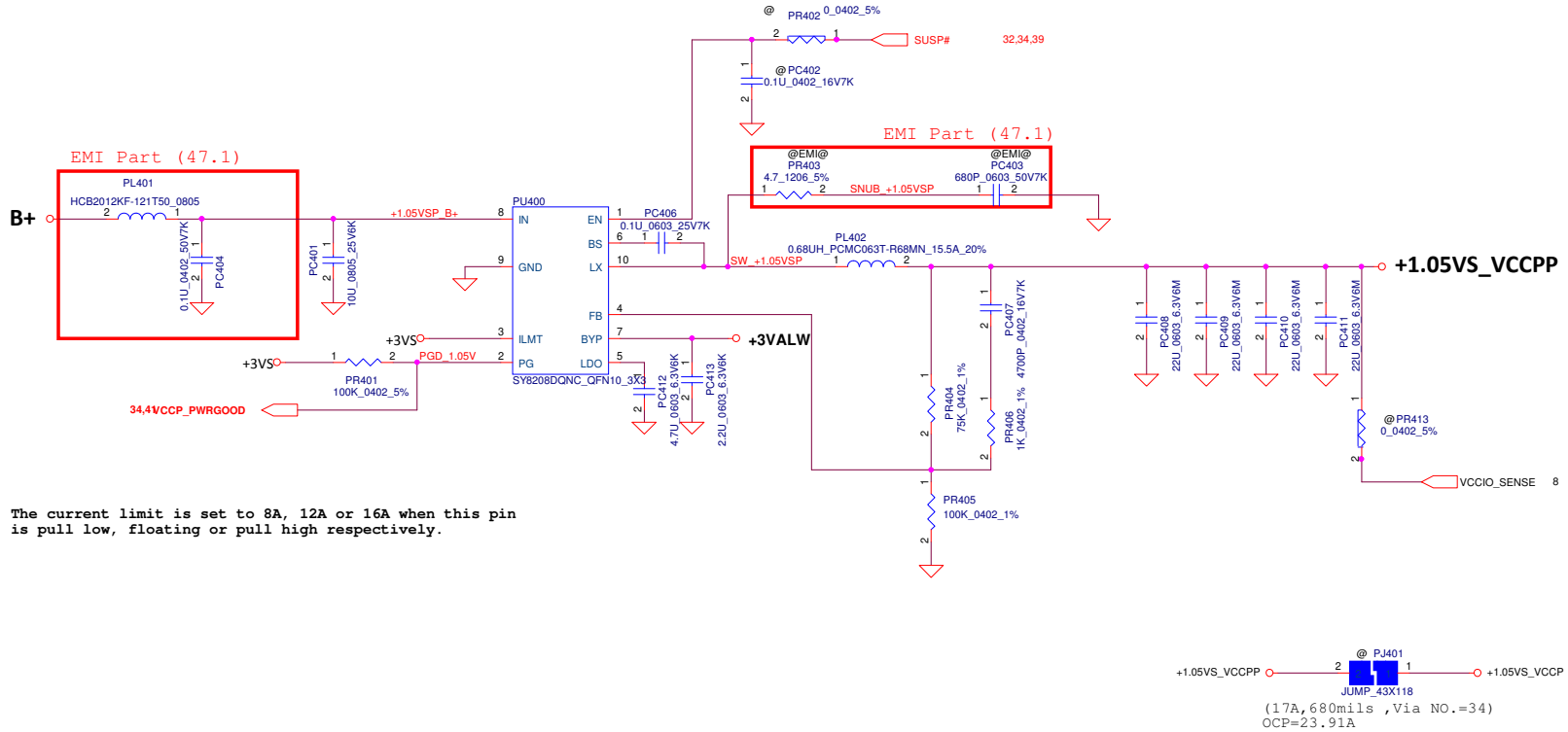
1.8VS controller (35.15), Support component (35.16)



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1.5VP/0.75VSP/1.8VSP

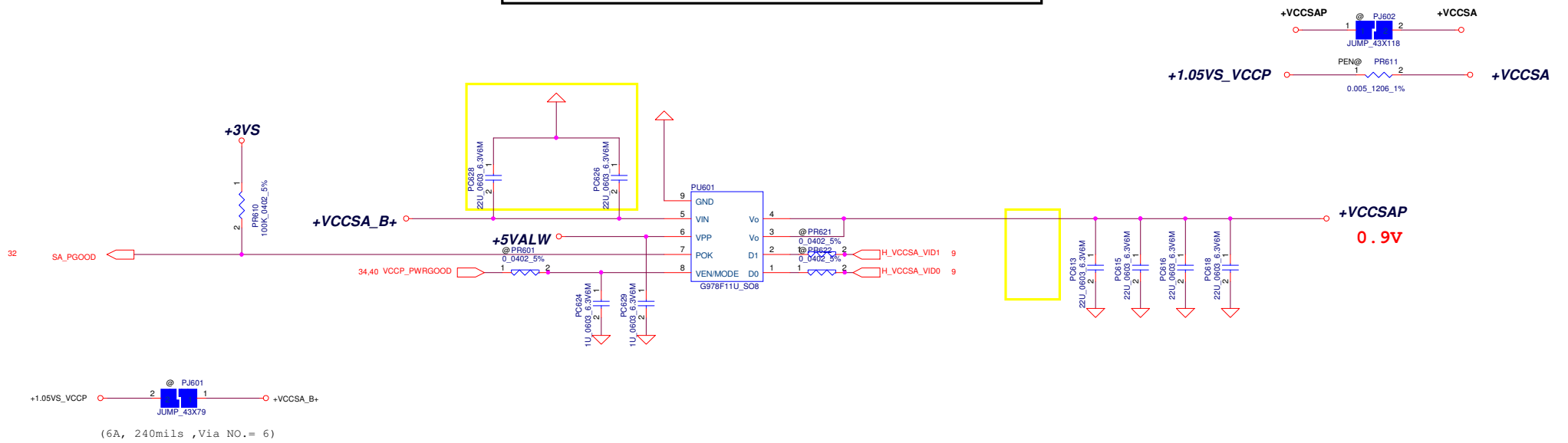
1.05VCCP controller (35.5), Support component (35.6)



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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	+1.05VS_VCCP
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VID [0]	VID [1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

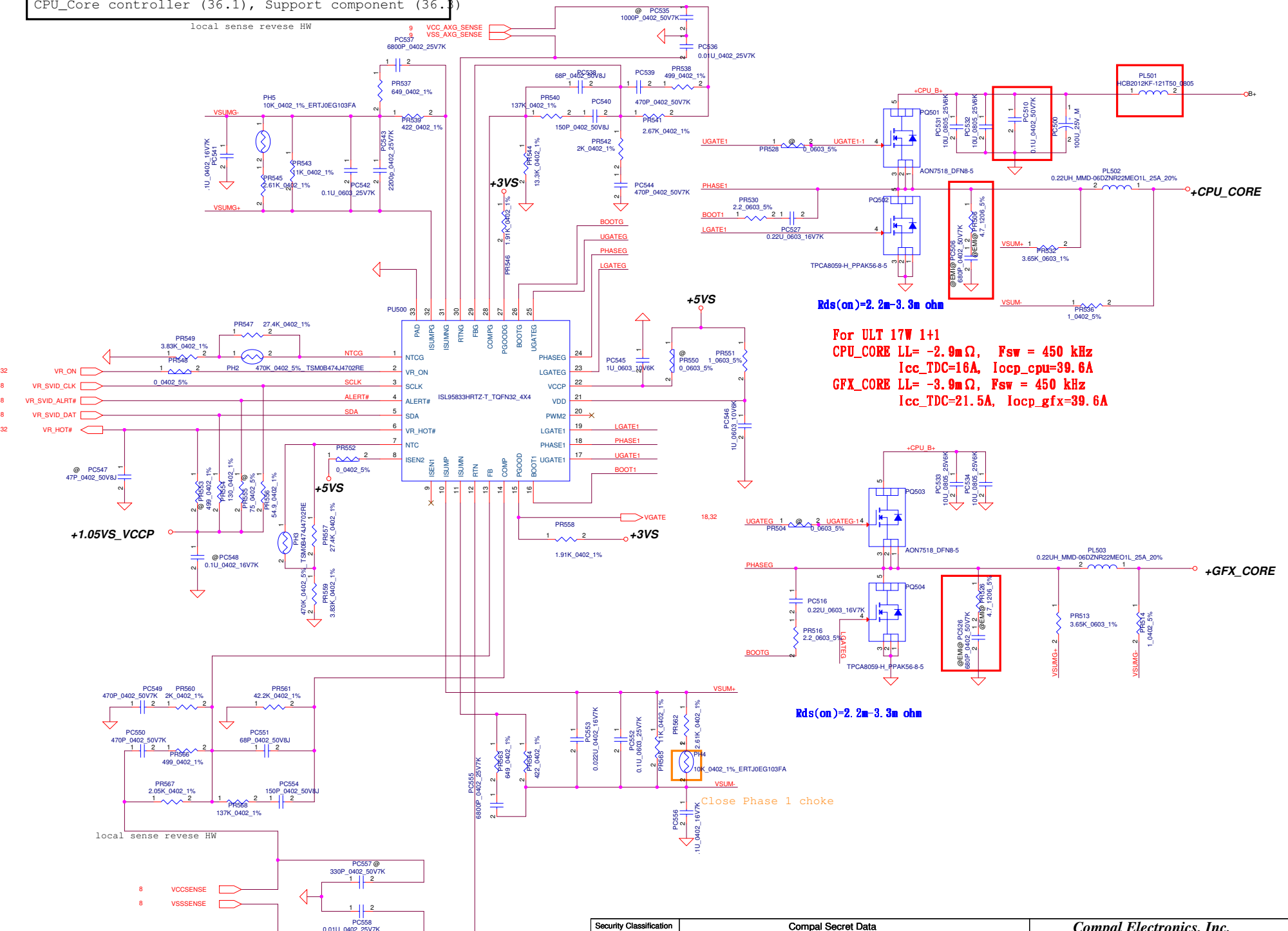
VCCSA controller (35.17), Support component (35.18)



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CPU_Core controller (36.1), Support component (36.3)

local sense reverse HW



For ULT 17W 1+1
CPU_CORE LL= -2.9mΩ, Fsw = 450 kHz
Icc_TDC=18A, Iocp_cpu=39.6A
GFX_CORE LL= -3.9mΩ, Fsw = 450 kHz
Icc_TDC=21.5A, Iocp_gfx=39.6A

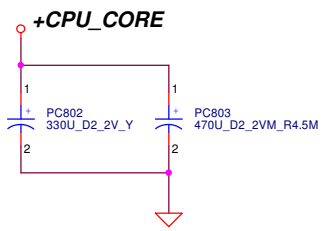
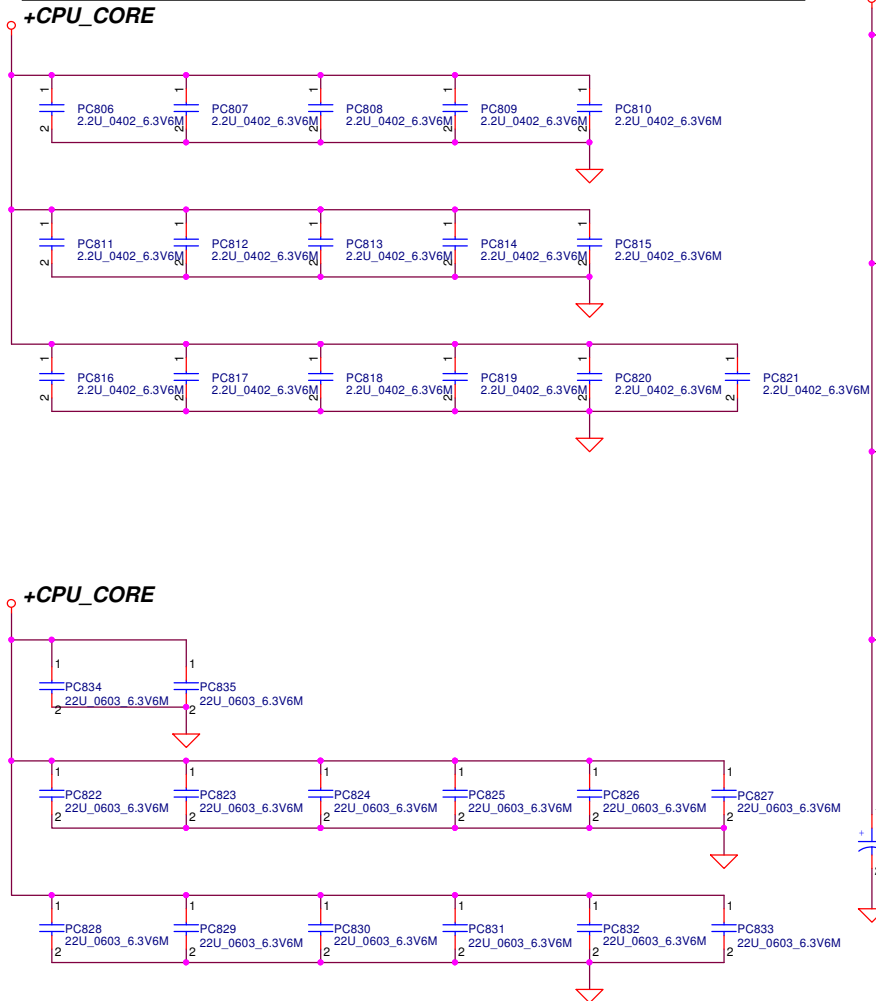
Rds(on)=2.2m-3.3m ohm

Rds(on)=2.2m-3.3m ohm

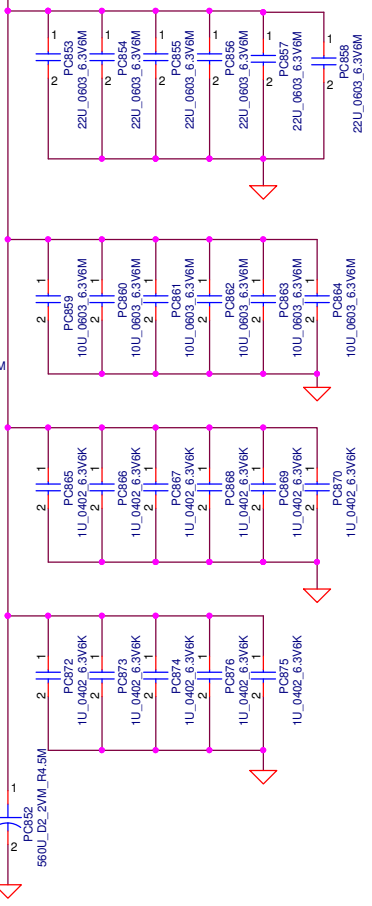
Close Phase 1 choke

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				CPU CORE
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CPU_Core output CAP (Including MLCC) 36.4

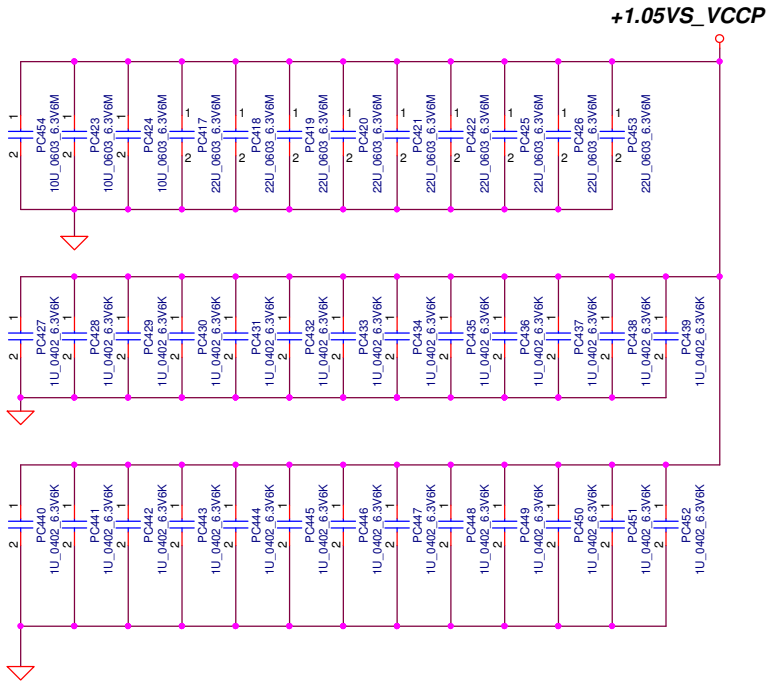


+GFX_CORE



GFX output CAP (Including MLCC) 36.5

VCCP output Cap (Including MLCC) 36.6



	Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF	470uF	560uF
CPU	2	14			16			
GFX_CORE			6	6		11	1	
1.05V_VCCP				10		26		1

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				Size	Document Number
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Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)
1	EVT--2012/10/24	P36-PWR-BATTERY CONN / OTP	@PD5 / Remove ESD diode	company	For part count reduction
2	EVT--2012/10/24	P36-PWR-BATTERY CONN / OTP	@PD6 / Remove ESD diode	company	For part count reduction
3	EVT--2012/10/24	P37-PWR-CHARGER	@PC221 /Remove 10uF capacitor	company	For part count reduction
4	EVT--2012/10/24	P38-PWR-3VALW/5VALW	PC331 /Reserve	PWR	ME limitation
5	EVT--2012/10/24	P38-PWR-3VALW/5VALW	@PC354/mount	PWR	ME limitation
6	EVT--2012/10/24	P38-PWR-3VALW/5VALW	PR337/235K change to 137K	PWR	for RT8243 3V OCP setting
7	EVT--2012/10/24	P38-PWR-3VALW/5VALW	PR357/156K change to 143K	PWR	for RT8243 5V OCP setting
8	EVT--2012/10/24	P39-1.5VP/0.75VSP/1.8VSP	PR158/16.2K change to 27.4K	PWR	for RT8207 OCP setting
9	EVT--2012/10/24	P43-PWR +CPU_CORE DECOUPLING	PC416/ change 560uF	PWR	Based on height and space limitation
10	EVT--2012/10/24	P43-PWR +CPU_CORE DECOUPLING	PC415/ Remove	PWR	Based on height and space limitation
11	EVT--2012/10/25	P37-PWR-CHARGER	PQ203/change to TPCA8507	PWR	for design change
12	DVT--2012/12/06	P37-PWR-CHARGER	PU200/change to BQ24725RGR	PWR	for design change
13	DVT--2012/12/06	P37-PWR-CHARGER	PQ203/ change to TPCA8507	PWR	AON6504 has burnt out issue
14	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC534,PC351/Delete	PWR	Based on height and space limitation
15	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PR335/add 100K ohm	PWR	Pull high +3VL
16	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC344/add 4.7U	PWR	for design request
17	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC341/change to 4.7U	PWR	for design request
18	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC352,PC353/add 150U_D2	PWR	Based on height and space limitation
19	DVT--2012/12/06	P39-1.5VP/0.75VSP/1.8VSP	PL152/change to 0.68UH	PWR	for design change
20	DVT--2012/12/06	P40-PWR-1.05VS_VCCP	PL401/change PN	PWR	to integrate PN
21	DVT--2012/12/06	P40-PWR-1.05VS_VCCP	PR403 PC403/Reserve	EMI	EMI Command
22	DVT--2012/12/06	P42-CPU_CORE	CPU_CORE(PR5XX,PC5XX)/change solution	PWR	change solution
23	DVT--2012/12/06	P43-PWR +CPU_CORE DECOUPLING	PC802 PC803/change to 470U	PWR	change solution
24	DVT--2012/12/06	P36-PWR-BATTERY CONN / OTP	PF2/change PN	company	For cost down
25	PVT--2013/01/18	P39-1.5VP/0.75VSP/1.8VSP	PC157/change 390U	PWR	for design change
26	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC414 / change 0ohm	PWR	change solution
27	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC417,PC418,PC419,PC420,PC421,PC422,PC425/change to 22U	PWR	for 1.05VCCP test
28	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC426,PC453/add 22U	PWR	for 1.05VCCP test
29	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC407/change 4700P	PWR	for design change
30	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC416/Delete	PWR	for 1.05VCCP test
31	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PL402/change to 0.68U	PWR	for 1.05VCCP test
32	PVT--2013/01/18	P42-CPU_CORE	PQ501,PQ503 /change AON7518	PWR	AON7514 EOL
33	PVT--2013/01/18	P42-CPU_CORE	PR553/Reserve	PWR	change solution
34	PVT--2013/01/18	P42-CPU_CORE	PR541/change to 2.67K	PWR	for CPU setting
35	PVT--2013/01/18	P42-CPU_CORE	PC543/change to 2.2nF	PWR	for CPU setting
36	PVT--2013/01/18	P42-CPU_CORE	PC553/change to 8.2nF	PWR	for CPU setting
37	PVT--2013/01/18	P42-CPU_CORE	PR567/change to 2.05K	PWR	for CPU setting
38	PVT--2013/01/21	P43-PWR +CPU_CORE DECOUPLING	PC802,PC852/change to 560U	PWR	for CPU,GFX Transient
39	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PC152/add 2200p	PWR	EMI Command
40	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PR156/add 4.7ohm	PWR	EMI Command
41	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PC156/add 680p	PWR	EMI Command
42	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PR155/add 2.2ohm	PWR	EMI Command
43	PVT--2013/01/21	P42-CPU_CORE	PQ502,PQ504 /change TPCA8059	PWR	for design change
44	Pre-MP--2013/03/05	P37-PWR-CHARGER	PC214/add 0.1u	PWR	EMI Command
45	Pre-MP--2013/03/05	P38-PWR-3VALW/5VALW	PC339/add 0.1u	PWR	EMI Command
46	Pre-MP--2013/03/05	P39-1.5VP/0.75VSP/1.8VSP	PC157 /change to 330u	PWR	ME limitation
47	Pre-MP--2013/03/05	P39-1.5VP/0.75VSP/1.8VSP	PC152 /change to 330p	PWR	EMI Command
48	Pre-MP--2013/03/05	P40-PWR-1.05VS_VCCP	PR406/add 1 K ohm	PWR	for 1.05 VCCP test(change to location sense)
49	Pre-MP--2013/03/05	P40-PWR-1.05VS_VCCP	PC404/add 0.1u	PWR	EMI Command
50	Pre-MP--2013/03/05	P42-CPU_CORE	PC510/add 0.1u	PWR	EMI Command
51	Pre-MP--2013/03/05	P42-CPU_CORE	PC553/change to 22nF	PWR	for CPUtransient
52	Pre-MP--2013/03/05	P43-PWR +CPU_CORE DECOUPLING	PC802/change to 330U	PWR	for CPUtransient

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HW PIR (Product Improve Record)

VFKTA LA-9862P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/28	(P.30)	Mount CA32 (SE102104K00)	BOM structure change
2.	11/28	(P.32)	Change RB36 from 2.2k to 0 ohm and CB50 to @	Design change
3.	11/28	(P.24)	Add @ to JHDMI	BOM structure change
4.	11/28	(P.11)	Move RD10, RD11 to page 12.	
5.	11/28	(P.33)	Delete NFC Function	Design change
6.	11/28	(P.28)	Change JCARD.10 to SDWP# and JCARD.11 to SDCD. (P.28) Add QW1, RW3, RW4 for normal close type connector	Design change
7.	11/28	(P.13)	Add D92 for LID_SW#_D to isolate the +3VL power rail from LID_SW#	Design change
8.	11/28	(P.15)	Update HDMI power circuit	Design change
9.	11/28	(P.20)	Change USB port 10 to NC.	Design change
10.	11/28	(P.16)	Change UH3 from socket to IC	Design change
11.	11/28	(P.09)	Change CC44 to 0805 size (SE00000PL00), Add CC40 (P.09) Change CC53 to 47U 0805 (SE00000PL00), Add CC50 (SE00000PL00) (P.12) Change CD31 to 0805 size (SE00000PL00) (P.29) Change CR10, CR12 to 0805 size (SE00000PL00)	For 1206 MLCC Crack issue
12.	11/28	(P.14)	change BOM structure C238, C239, C240, C241, C242, C243 to CRT@EMI@	EMI request
13.	11/28	(P.16)	Change UH3 from socket to IC	Design change
14.	11/28	(P.07)	Change RC73 to 0 ohm (do not use short pad on this location)	For debug
15.	11/28	(P.30)	Change RA50 to 269@	Design change
16.	11/28	(P.31)	Change SPK connector to 6 pin, change SPK_DET0 to SPK_DET, delete SPK_DET1 and RA96	Design change
17.	11/28	(P.21)	Change SPK_DET0 to SPK_DET, delete SPK_DET1	Design change
18.	11/28	(P.13)	Delete D92 and change the netname to BKOFF# for touch Screen	Avoid LCD_INV leak to Touch/B
19.	11/28	(P.13)	SWAP R92, R100 L60 config, SWAP R93, R101, L59 config	BOM structure change
20.	11/28	(P.13)	Reverse LVDS connector pin definition	Design change
21.	11/28	(P.33)	Change H15 from H_3P0 to H_4P0, Add h19 H_3P2N ME follow ME change	ME request
22.	11/29	(P.28)	Modify Jcard @ to update Netlist	BOM structure change
23.	11/29	(P.13)	Delete R87, R88, R89, R90, R92, R93, R100, R101, L59, L60, JCAM, JEDP (P.13) Change L56 to L55, L58 to L57, JLVDS type and modify net name for LVDS	Design change
24.	11/29	(P.14)	add R62, R63, 22-ohm (PN: SD028220A80) on CRT HSYNC/VSYNC trace.	For CRT undershoot issue
25.	11/29	(P.16)	Change UH4, RH269, RH271 to @, change RH267 from shortpad to 0-ohm	Design change
26.	11/30	(P.8)	Add CC17~CC19 for ESD request	ESD request
27.	11/30	(P.20)	Move PLT_RST# ESD capacitor (CH104) to EC side (CB13) and mount 0.1uF	ESD request
28.	11/30	(P.5)	Change CC63 from @ESD@ to ESD@ for ESD request	ESD request
29.	11/30	(P.30)	Reserve RA31, RA38 for EMI request	EMI request
30.	11/30	(P.32)	Change PM_SLP_S4# from pin127 to pin84. (P.32) Change USB_EN#0 from pin84 to pin23.	
31.	11/31	(P.33)	Update CPU config&PN	
32.	12/04	(P.29)	Update S&C to 14640/14641 co-layout circuit , add RR1~RR4, QR1, modify net-name	Design change

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	01/18	(P.28)	Delete QW2	Design Change
2.	01/18	(P.20)	Change RH166 from ShortPad to 0 ohm resistor.	For ESD Request
3.	01/18	(P.07)	Delete RC3.	Design Change
4.	01/18	(P.32)	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	For boot bobo issue
5.	01/18	(P.05)	Add CC35, CC20	For ESD Request
6.	01/18	(P.21)	reserve CC21	For ESD Request
7.	01/18	(P.32)	reserve CC23, CC24, CC25	For ESD Request
8.	01/18	(P.18)	reserve CC26, CC27	For ESD Request
9.	01/18	(P.32)	Change CB13 to 100P P/NSE071101J80	Design Change
10.	01/18	(P.28)	Add RW2 CW9	For EMI Request

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HW PIR (Product Improve Record)

HW PIR (Product Improve Record)

VFKTA LA-9862P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	01/28	(P.33)	Modify JTP pin with the same as VFKTA DIS	Design Change
2.	01/28	(P.13)	Reserve R267&R266 0 ohm	For EMI cost down
3.	01/28	(P.32)	Change QB1 to SB00000EN00	For X1 code issue
4.	01/28	(P.07)	Change QC3 to SB00000PF00	For X1 code issue
5.	01/28	(P.15)	Change QY1 QY2 to SB00000PF00	For X1 code issue
6.	01/28	(P.16)	Change UH3 from SA00003K800 to SA00004LI00	For X1 code issue
7.	01/28	(P.27/29)	Change UR1 UR4 from SA00004KB00 to SA00003TV00	For X1 code issue
8.	01/28	(P.13)	Change L2 SM01000CD00E to SM01000JB00	For EOL issue
9.	01/28	(P.9/17/28/34/30/29)	Change QC5,QH3,QH4,QW1,Q6 ,QA1, QR1, Q53 from SB00000EO10 to SB00000DH00	For X1 code issue
10.	01/28	(P.30)	Change RA42 from SM01000CY00 to SM01000A900	For X1 code issue
11.	01/28	(P.29)	Change LR2,LR3,LR4,LR5 from SM070001U00 to SM070001R00	For X1 code issue
12.	02/18	(P.06)	Swap H_EDP_TXN[0\1] to H_EDP_TXP[0\1]	Design mistake
13.	02/18	(P.13)	Change C7 to SE076153K80 (15nF)	for LCD sequence tuning
14.	02/19	(P.05)	Delete CC33, CC36, C4; change R1 to short pad	for part count reduce
15.	02/19	(P.07)	Change RC73 to short pad	for part count reduce
16.	02/19	(P.09)	Delete CC61, CC83; change RC119 to short pad	for part count reduce
17.	02/19	(P.11)	Delete CD2, CD15	for part count reduce
18.	02/19	(P.12)	Delete CD28, CD46	for part count reduce
19.	02/19	(P.13)	Change R106 to shortpad	for part count reduce
20.	02/19	(P.14)	Delete C250	for part count reduce
21.	02/19	(P.16)	Delete CH6, CH100; change RH67, RH68 to short pad	for part count reduce
22.	02/19	(P.19)	Delete RH254	for part count reduce
23.	02/19	(P.26)	Delete CCL2, RCL5, RCL2, net: LAN_X1_R_R, LAN_X1_R	for part count reduce
24.	02/19	(P.27)	Delete net: LAN_X1_R	for part count reduce
25.	02/19	(P.28)	Change RW1 to shortpad	for part count reduce
26.	02/19	(P.29)	Delete CR7, CR8	for part count reduce
27.	02/19	(P.30)	Change RA22, RA18, RA24 to short pad	for part count reduce
28.	02/19	(P.41)	Delete CB4, CB5, CB50	for part count reduce
29.	02/19	(P.42)	Delete SW2, SW3	for part count reduce
30.	02/28	(P.32)	Connect RB14 form CLK_EC_R to POK and reserve RB13,RB22,CB16	for abnormal shut down power request
31.	02/28	(P.20)	change RH167 pin2 netname from CLK_EC_R to CLK_PCI_EC_R	
32.	03/04	(P.20)	change RH167 pin2 netname from CLK_PCI_EC_R to CLK_EC_R	For keep the same as DIS
33.	03/04	(P.32)	Connect RB14 from POK_R to POK and reserve RB13,RB22,CB16	for abnormal shut down power request
34.	03/04	(P.28)	Add RW5~RW8 for EMI request and change netname SD_DATA[0...3] to SD_DATA[0...3]_R on connector side	for EMI request
35.	03/06	(P.28)	Add 10pF CV10~CV13 on SD_DATA[0:3]	for EMI request.

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