Compal Confidential

VSKAA Schematics Document

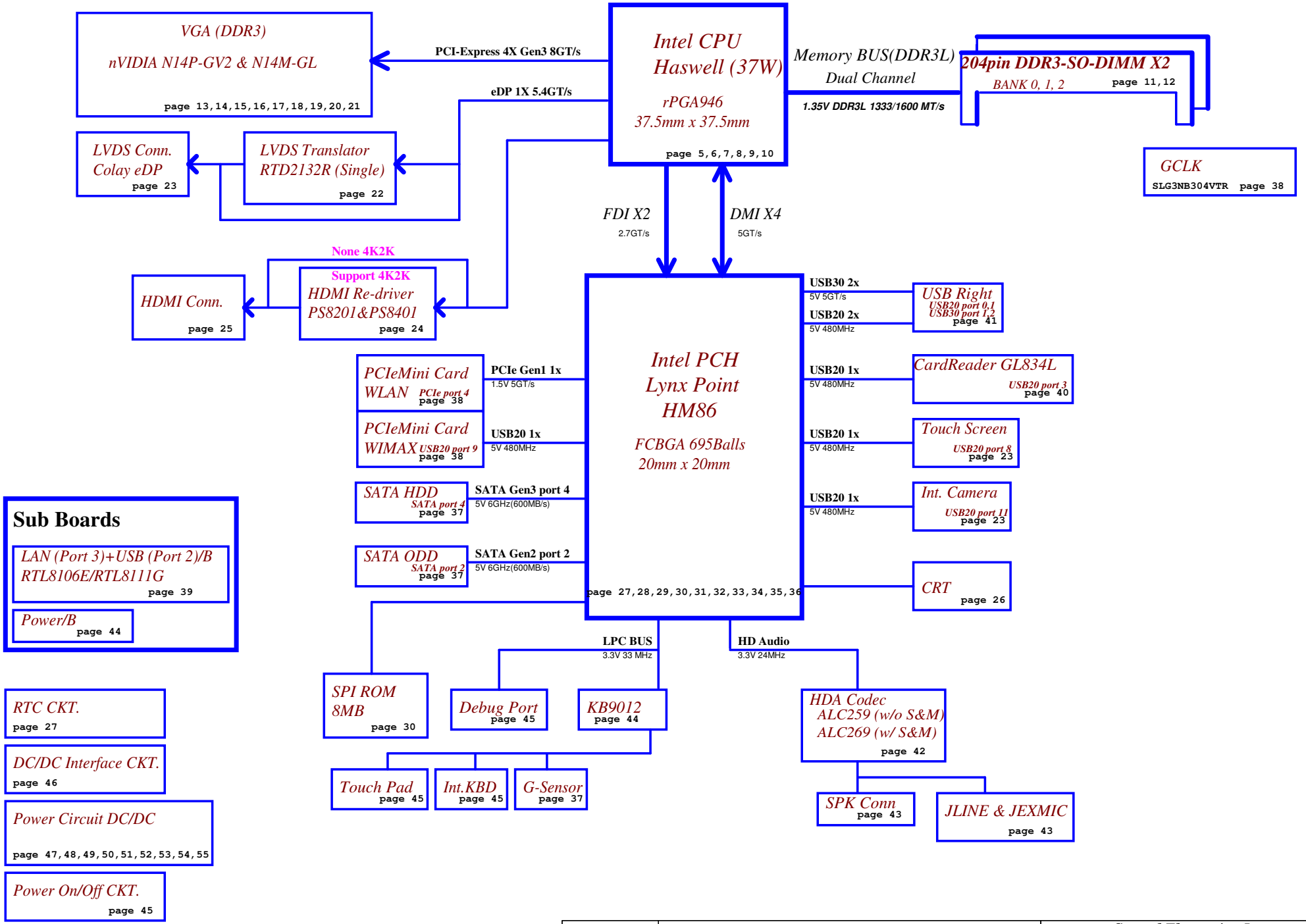
Haswell with DDR3L + Lynx Point PCH

nVIDIA N14P-GV2 (Dual Rank)
nVIDIA N14M-GL

LA-9866P REV 1.0 Schematic

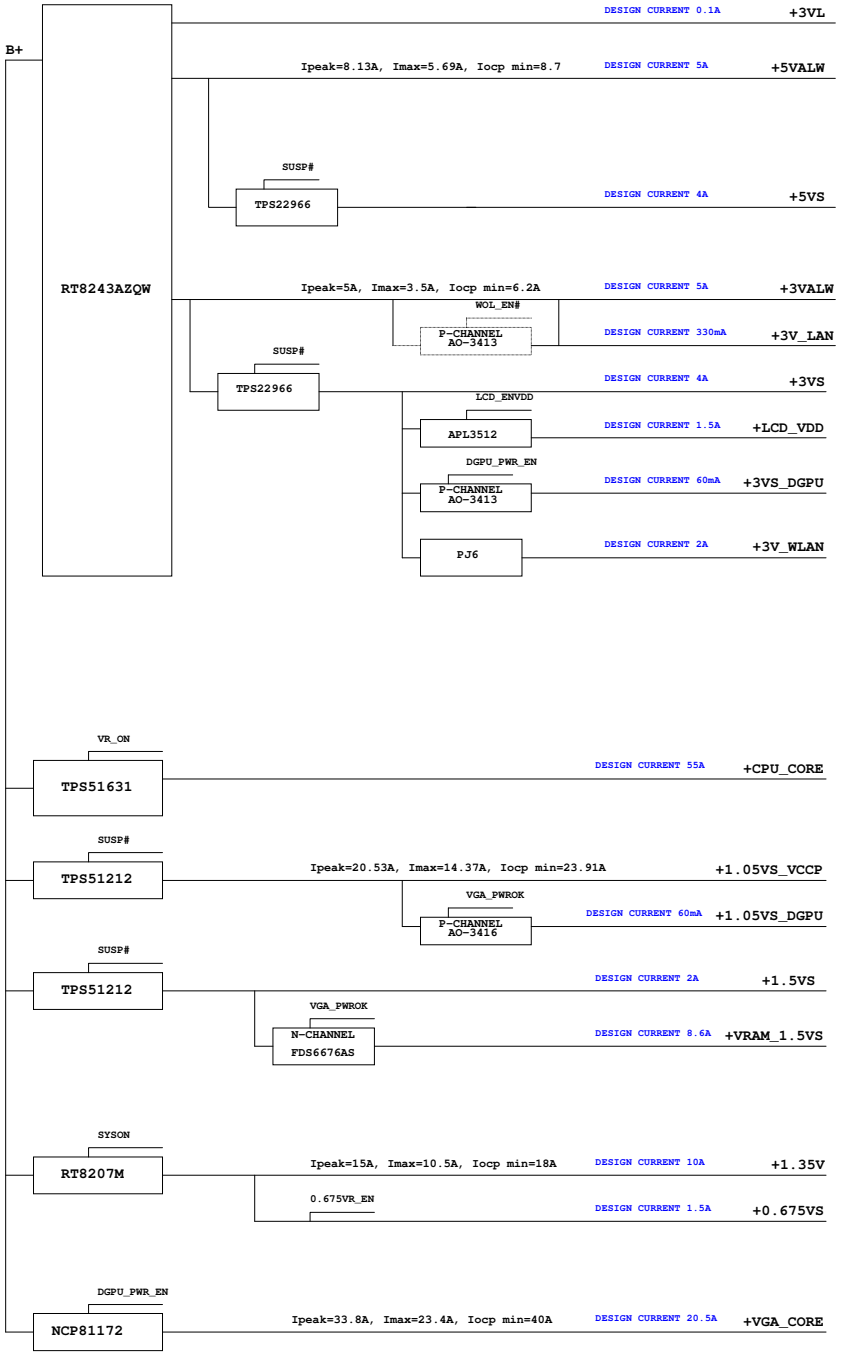
Intel Processor (Haswell) / PCH(Lynx Point)
2013-04-28 Rev 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title: Cover Page	
Size: Custom	Document Number: VSKAA				Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 1 of 57				



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: Block Diagram			
Size: B	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 2 of 57		



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: Power Tree			
Size	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 3 of 57		

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.35V	+5VS +3VS +1.8VS +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

Platform	SKU	CPU	PCH	VGA
Chief River		Ivy Bridge i3 (CPUI3@) Ivy Bridge i5 (CPUI5@)	HM77C1(HM77@) HM77C1_R1(HM77R1@) HM77C1_R3(HM77R3@)	nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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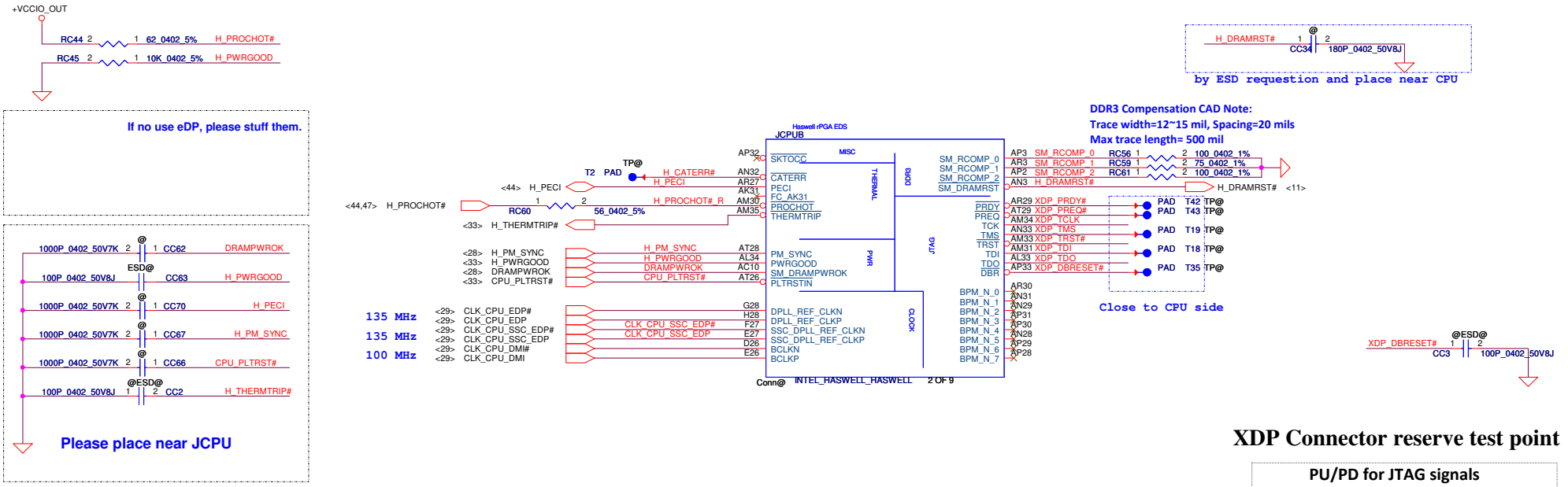
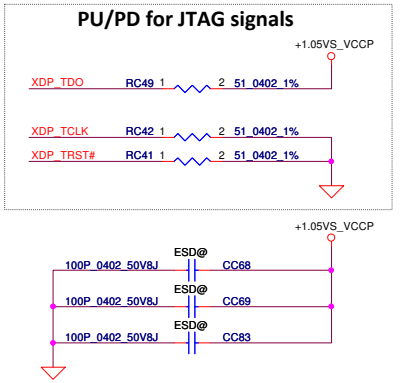
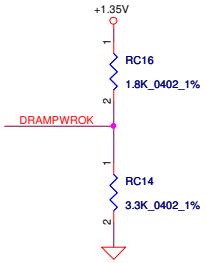
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: Notes List
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 4 of 57		



XDP Connector reserve test point

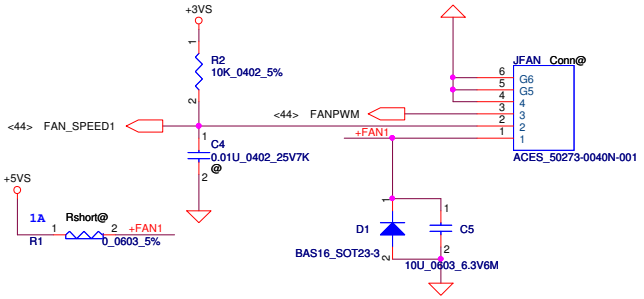


SM_DRAMPWROK for nonsupport Deep S3



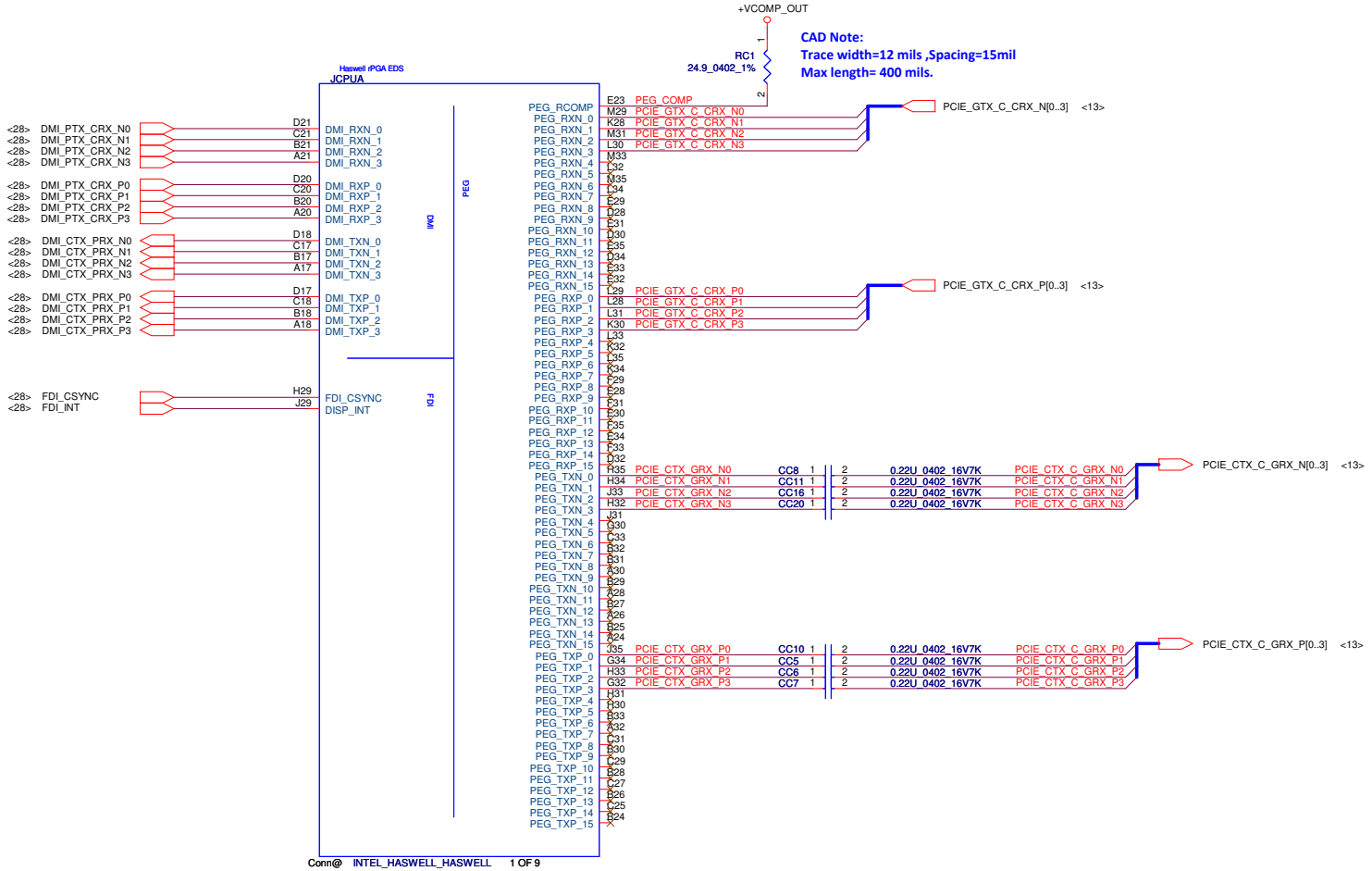
Buffered Rest to CPU

FAN Control Circuit



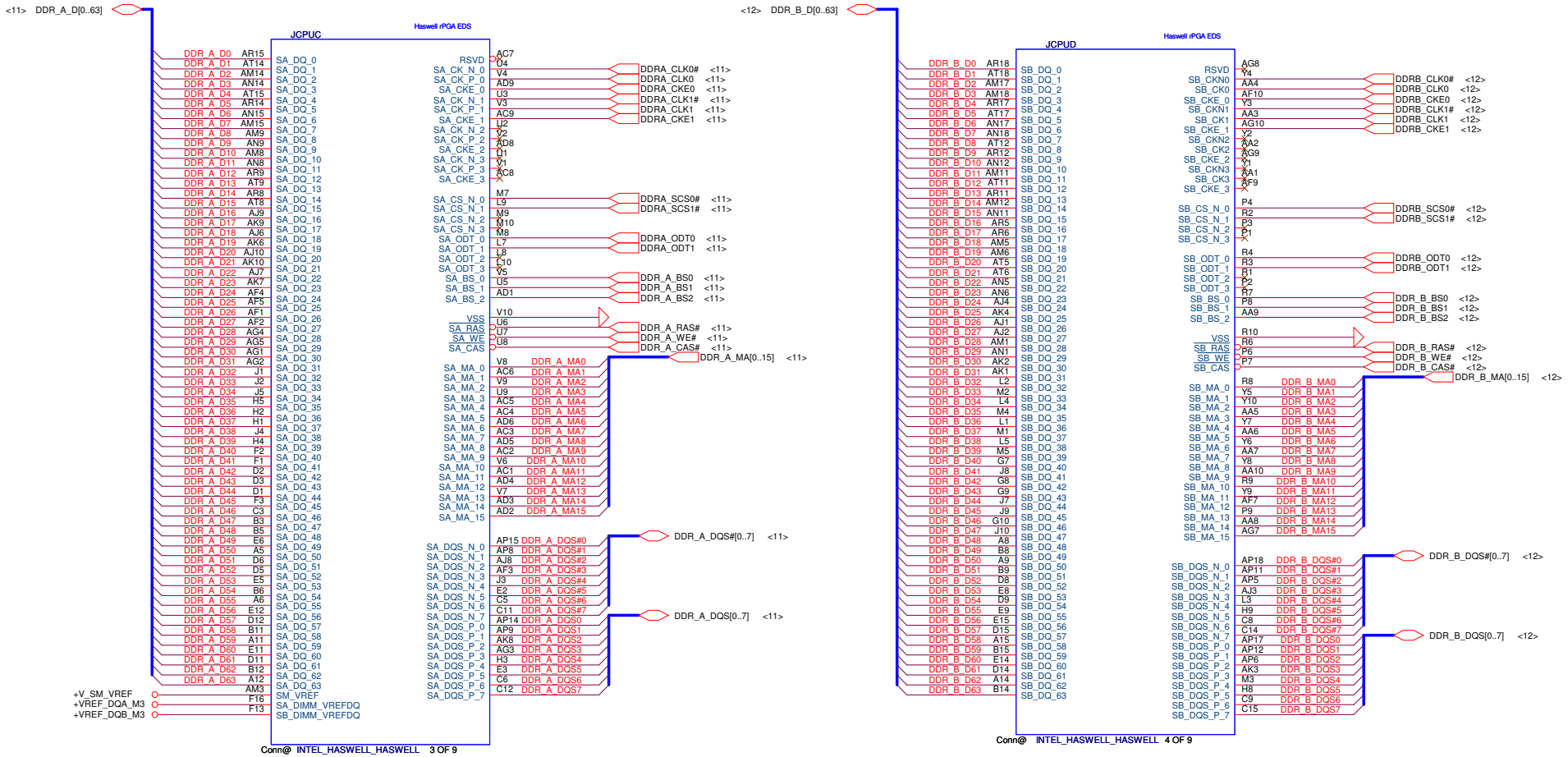
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	Haswell_JTAG/XDP/FAN		
Size Custom	Document Number VSKAA		Rev 1.0
Date: Thursday, May 09, 2013	Sheet 5 of 57		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: Haswell_DMI/PEG/FDI

Size: B2S Custom	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 6 of 57		

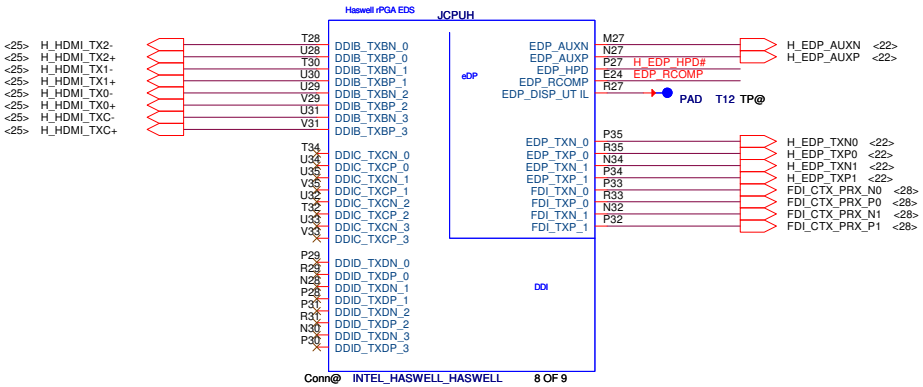


Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

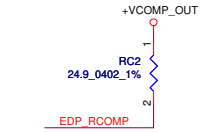
Compal Electronics, Inc.

Title: ***Haswell_DDR3***

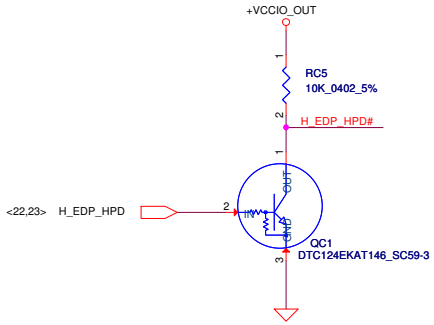
Size: Custom	Document Number: VSKAA	Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 7 of 57	



COMPENSATION PU FOR eDP



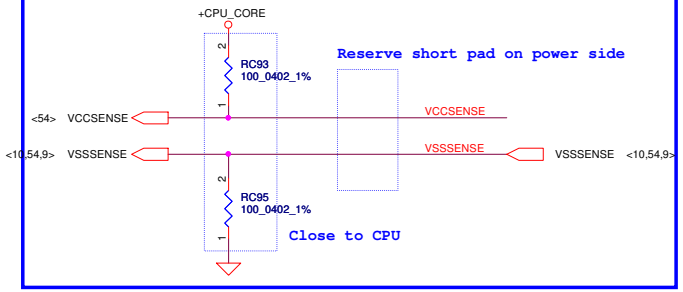
CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.



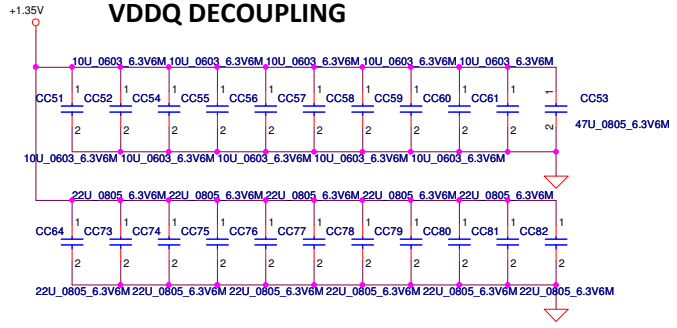
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: Haswell_DDI/eDP

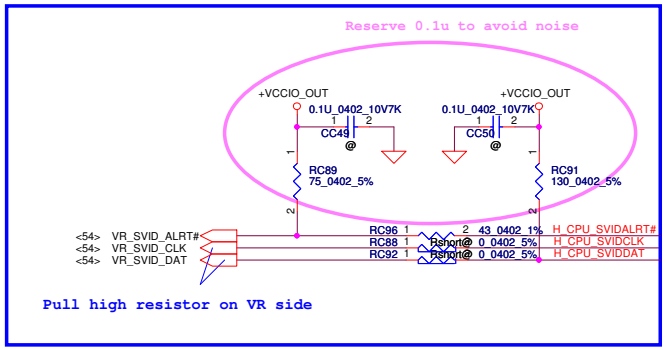
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 8 of 57		

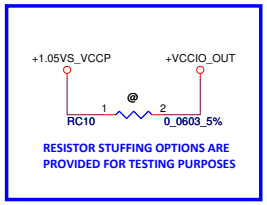
VCC_SENSE

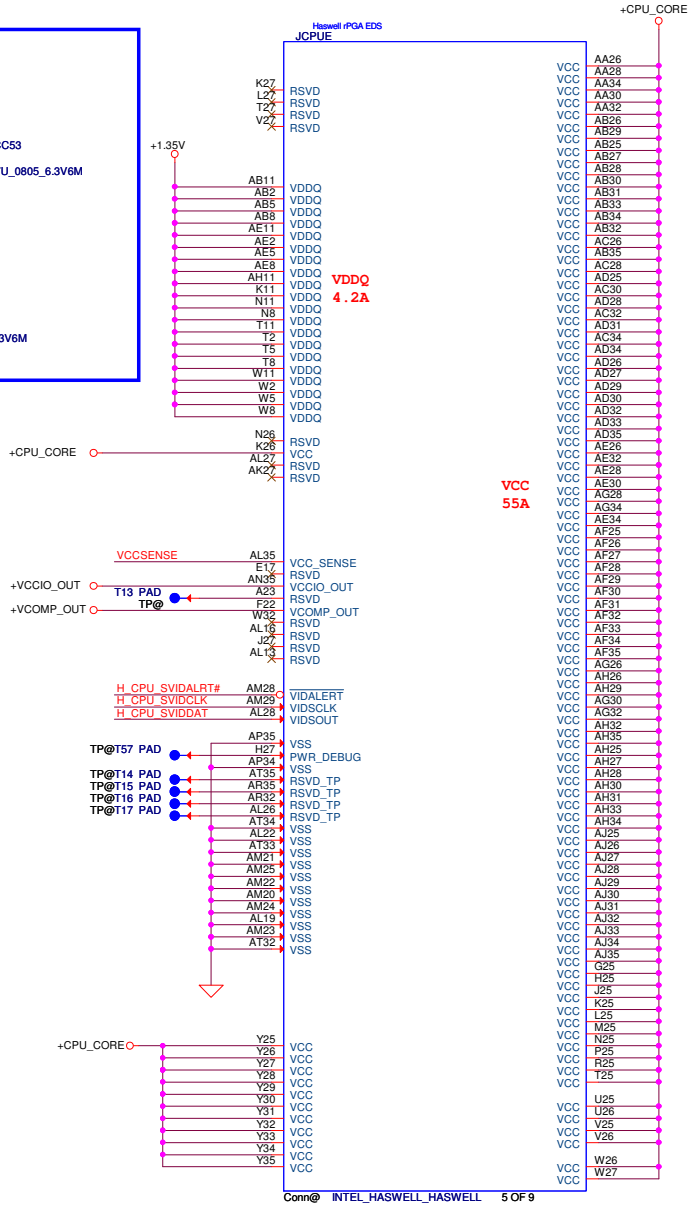


VDDQ DECOUPLING









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Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

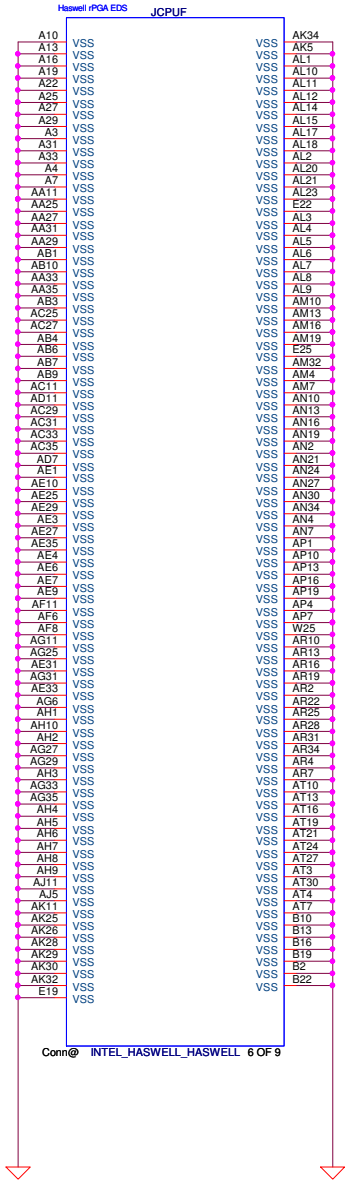
Title: ***Haswell_POWER***

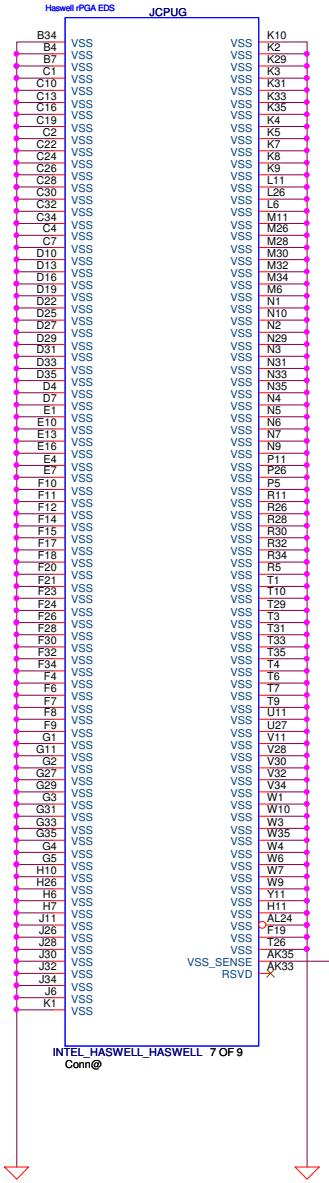
Size: Custom | Document Number: **VSKAA** | Rev: 1.0

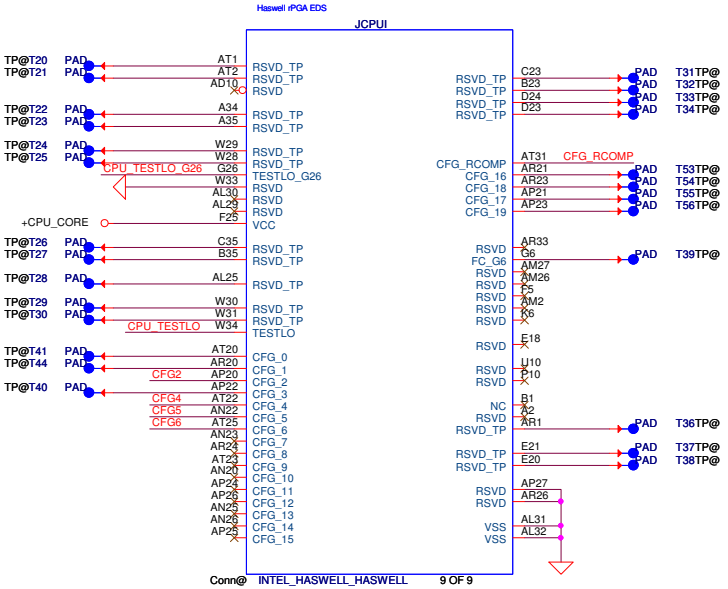
Date: Thursday, May 09, 2013 | Sheet 9 of 57

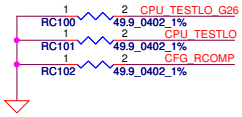
CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)

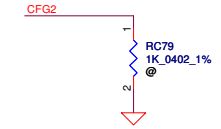




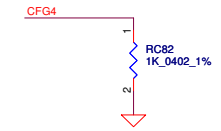




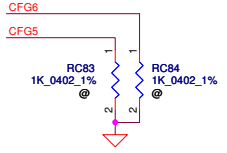
VSSSENSE <54,9>



PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled; function 2 disabled 01: Reserved – (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

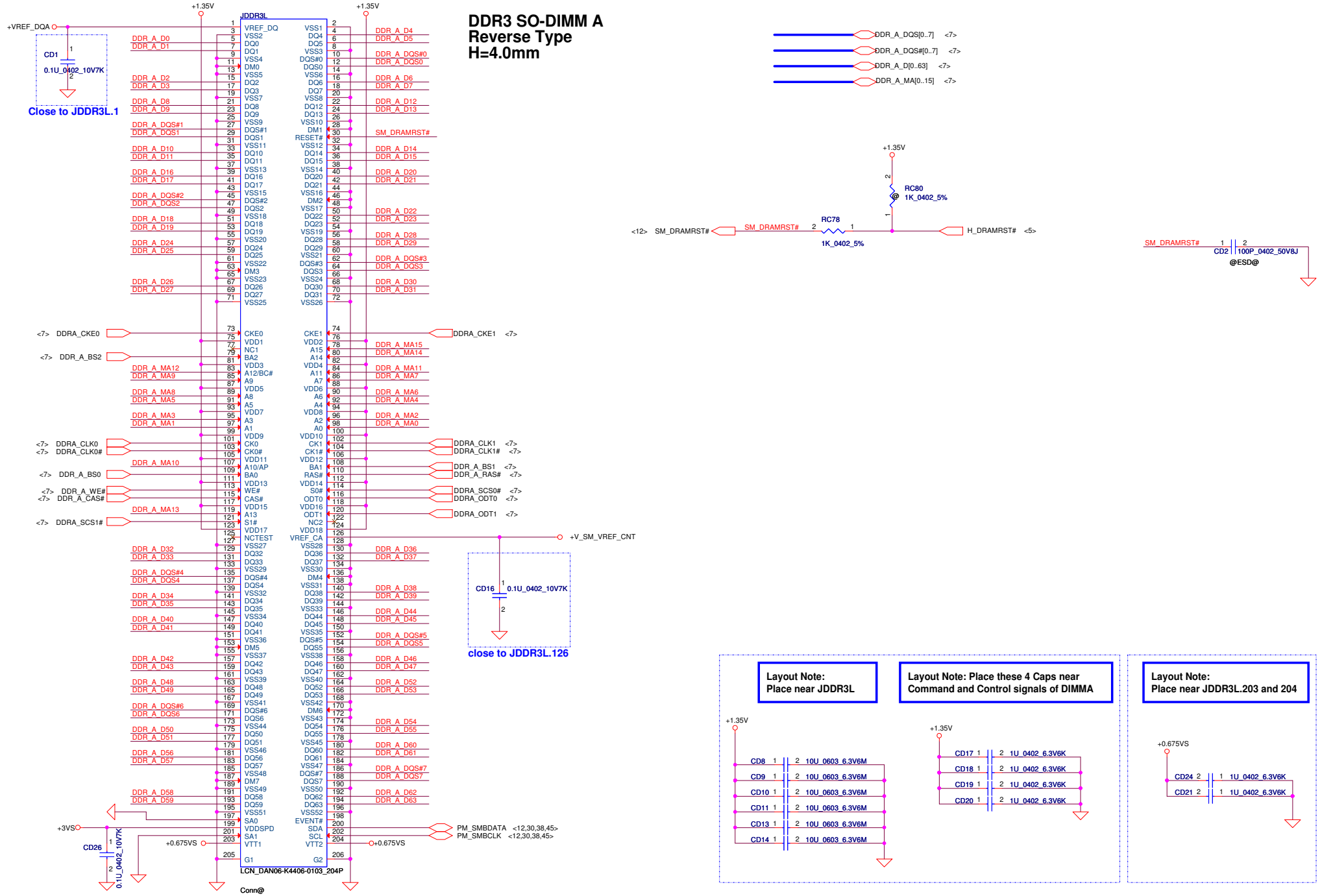
Compal Electronics, Inc.

Title: *Haswell_GND/RSVD/CFG*

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 10 of 57

DDR3 SO-DIMM A
Reverse Type
H=4.0mm



SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

DDR_A_DQS[0..7] <7>
DDR_A_DQS#[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_MA[0..15] <7>

Layout Note:
Place near JDDR3L

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

Layout Note:
Place near JDDR3L.203 and 204

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM0***

Size: Custom	Document Number: VSKAA	Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 11 of 57	

DDR3 SO-DIMM B
Reverse Type
H=9.0mm

JDDR3H

+1.35V

+VREF_DQB

CD27 1 — 0.1U_0402_10V7K — 2

Close to JDDR3H.1

1	VREF_DQ	VSS1	2		
3	VSS2	DQ4	4	DDR_B_D4	DDR_B_D0
5	DQ0	DQ5	6	DDR_B_D5	DDR_B_D1
7	DQ1	VSS3	8		
9	VSS4	DQS#0	10	DDR_B_DQS#0	
11	DM0	DQS0	12	DDR_B_DQS0	
13	VSS5	VSS6	14		
15	DQ2	DQ6	16	DDR_B_D6	DDR_B_D2
17	DQ3	DQ7	18	DDR_B_D7	DDR_B_D3
19	VSS7	VSS8	20		
21	DQ8	DQ12	22	DDR_B_D12	DDR_B_D8
23	DQ9	DQ13	24	DDR_B_D13	DDR_B_D9
25	VSS9	VSS10	26		
27	DQS#1	DM1	28		
29	DQS1	RESET#	30	SM_DRAMRST# <11>	
31	VSS11	VSS12	32		
33	DQ10	DQ14	34	DDR_B_D14	DDR_B_D10
35	DQ11	DQ15	36	DDR_B_D15	DDR_B_D11
37	VSS13	VSS14	38		
39	DQ16	DQ20	40	DDR_B_D20	DDR_B_D16
41	DQ17	DQ21	42	DDR_B_D21	DDR_B_D17
43	VSS15	VSS16	44		
45	DQS#2	DM2	46		
47	DQS2	VSS17	48		
49	VSS18	DQ22	50	DDR_B_D22	DDR_B_D18
51	DQ18	DQ23	52	DDR_B_D23	DDR_B_D19
53	DQ19	VSS19	54		
55	VSS20	DQ28	56	DDR_B_D28	DDR_B_D24
57	DQ24	DQ29	58	DDR_B_D29	DDR_B_D25
59	DQ25	VSS21	60		
61	VSS22	DQS#3	62	DDR_B_DQS#3	DDR_B_DQS#2
63	DM3	DQS3	64	DDR_B_DQS3	
65	VSS23	VSS24	66		
67	DQ26	DQ30	68	DDR_B_D30	DDR_B_D26
69	DQ27	DQ31	70	DDR_B_D31	DDR_B_D27
71	VSS25	VSS26	72		
73	CKE0	CKE1	74	DDRB_CKE1 <7>	<7> DDRB_CKE0
75	VDD1	VDD2	76	DDR_B_MA15	
77	NC1	A15	78	DDR_B_MA14	<7> DDR_B_BS2
79	BA2	A14	80		
81	VDD3	VDD4	82		
83	A12/BC#	A11	84	DDR_B_MA11	DDR_B_MA12
85	A9	A7	86	DDR_B_MA7	DDR_B_MA9
87	VDD5	VDD6	88		
89	A8	A6	90	DDR_B_MA6	DDR_B_MA8
91	A5	A4	92	DDR_B_MA4	DDR_B_MA5
93	VDD7	VDD8	94		
95	A3	A2	96	DDR_B_MA2	DDR_B_MA3
97	A1	A0	98	DDR_B_MA0	DDR_B_MA1
99	VDD9	VDD10	100		
101	CK0	CK1	102	DDRB_CLK1 <7>	<7> DDRB_CLK0
103	CK0#	CK1#	104	DDRB_CLK1# <7>	<7> DDRB_CLK0#
105	VDD11	VDD12	106		
107	A10/AP	BA1	108	DDR_B_BS1 <7>	DDR_B_MA10
109	BA0	RAS#	110	DDR_B_RAS# <7>	<7> DDR_B_BS0
111	VDD13	VDD14	112		
113	WE#	S0#	114	DDRB_SCS0# <7>	<7> DDR_B_WE#
115	CAS#	ODT0	116	DDRB_ODT0 <7>	<7> DDR_B_CAS#
117	VDD15	VDD16	118		
119	A13	ODT1	120	DDRB_ODT1 <7>	DDR_B_MA13
121	S1#	NC2	122		<7> DDRB_SCS1#
123	VDD17	VDD18	124		
125	NCTEST	VREF_CA	126	+V_SM_VREF_CNT	
127	VSS27	VSS28	128		
129	DQ32	DQ36	130	DDR_B_D36	DDR_B_D32
131	DQ33	DQ37	132	DDR_B_D37	DDR_B_D33
133	VSS29	VSS30	134		
135	DQS#4	DM4	136		
137	DQS4	VSS31	138		
139	VSS32	DQ38	140	DDR_B_D38	DDR_B_D34
141	DQ34	DQ39	142	DDR_B_D39	DDR_B_D35
143	DQ35	VSS33	144		
145	VSS34	DQ44	146	DDR_B_D44	DDR_B_D40
147	DQ40	DQ45	148	DDR_B_D45	DDR_B_D41
149	DQ41	VSS35	150		
151	VSS36	DQS#5	152	DDR_B_DQS#5	DDR_B_DQS#4
153	DM5	DQS5	154	DDR_B_DQS5	DDR_B_DQS4
155	VSS37	VSS38	156		
157	DQ42	DQ46	158	DDR_B_D46	DDR_B_D42
159	DQ43	DQ47	160	DDR_B_D47	DDR_B_D43
161	VSS39	VSS40	162		
163	DQ48	DQ52	164	DDR_B_D52	DDR_B_D48
165	DQ49	DQ53	166	DDR_B_D53	DDR_B_D49
167	VSS41	VSS42	168		
169	DQS#6	DM6	170		
171	DQS6	VSS43	172		
173	VSS44	DQ54	174	DDR_B_D54	DDR_B_D50
175	DQ50	DQ55	176	DDR_B_D55	DDR_B_D51
177	DQ51	VSS45	178		
179	VSS46	DQ60	180	DDR_B_D60	DDR_B_D56
181	DQ56	DQ61	182	DDR_B_D61	DDR_B_D57
183	DQ57	VSS47	184		
185	VSS48	DQS#7	186	DDR_B_DQS#7	
187	DM7	DQS7	188	DDR_B_DQS7	
189	VSS49	VSS50	190		
191	DQ58	DQ62	192	DDR_B_D62	DDR_B_D58
193	DQ59	DQ63	194	DDR_B_D63	DDR_B_D59
195	VSS51	VSS52	196		
197	SA0	EVENT#	198		
199	VDDSPD	SDA	200	PM_SMBDATA <11,30,38,45>	
201	SA1	SCL	202	PM_SMBCLK <11,30,38,45>	
203	VTT1	VTT2	204	+0.675VS	+3VS
205	G1	G2	206		

+3VS — RD15 1 — 10K_0402_5% — 2 — +0.675VS

CD49 1 — 0.1U_0402_10V7K — 2

LCN_DAN06-K4806-0103_204P
Conn@

CD47 1 — 0.1U_0402_10V7K — 2

Close to JDDR3H.126

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

DDR_B_DQS#[0..7] <7>
DDR_B_DQS[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>

All VREF traces should have 20 mil trace width

+1.35V — RC121 1K_0402_1% — +VREF_DQA
+VREF_DQA_M3 — RC187 2_0402_1% — CC71 0.022U_0402_25V7K — RC110 1K_0402_1%
RC8 24.9_0402_1%

+1.35V — RC122 1K_0402_1% — +VREF_DQB
+VREF_DQB_M3 — RC188 2_0402_1% — CC72 0.022U_0402_25V7K — RC111 1K_0402_1%
RC9 24.9_0402_1%

+1.35V — RC120 1K_0402_1% — +V_SM_VREF_CNT
+V_SM_VREF — RC189 2_0402_1% — CC65 0.022U_0402_25V7K — RC109 1K_0402_1%
RC3 24.9_0402_1%

Layout Note:
Place near JDDR3H

+1.35V
CD31 1 — 47U_0805_6.3V6M — 2
SE00000PL00
CD41 1 — 10U_0603_6.3V6M — 2
CD36 1 — 10U_0603_6.3V6M — 2
CD37 1 — 10U_0603_6.3V6M — 2
CD39 1 — 10U_0603_6.3V6M — 2
CD40 1 — 10U_0603_6.3V6M — 2
CD58 1 — 10U_0603_6.3V6M — 2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

+1.35V
CD29 2 — 1U_0402_6.3V6K — 1
CD30 2 — 1U_0402_6.3V6K — 1
CD32 2 — 1U_0402_6.3V6K — 1
CD33 2 — 1U_0402_6.3V6K — 1

Layout Note:
Place near JDDR3H.203 and 204

+0.675VS
CD45 2 — 1U_0402_6.3V6K — 1
CD42 2 — 1U_0402_6.3V6K — 1

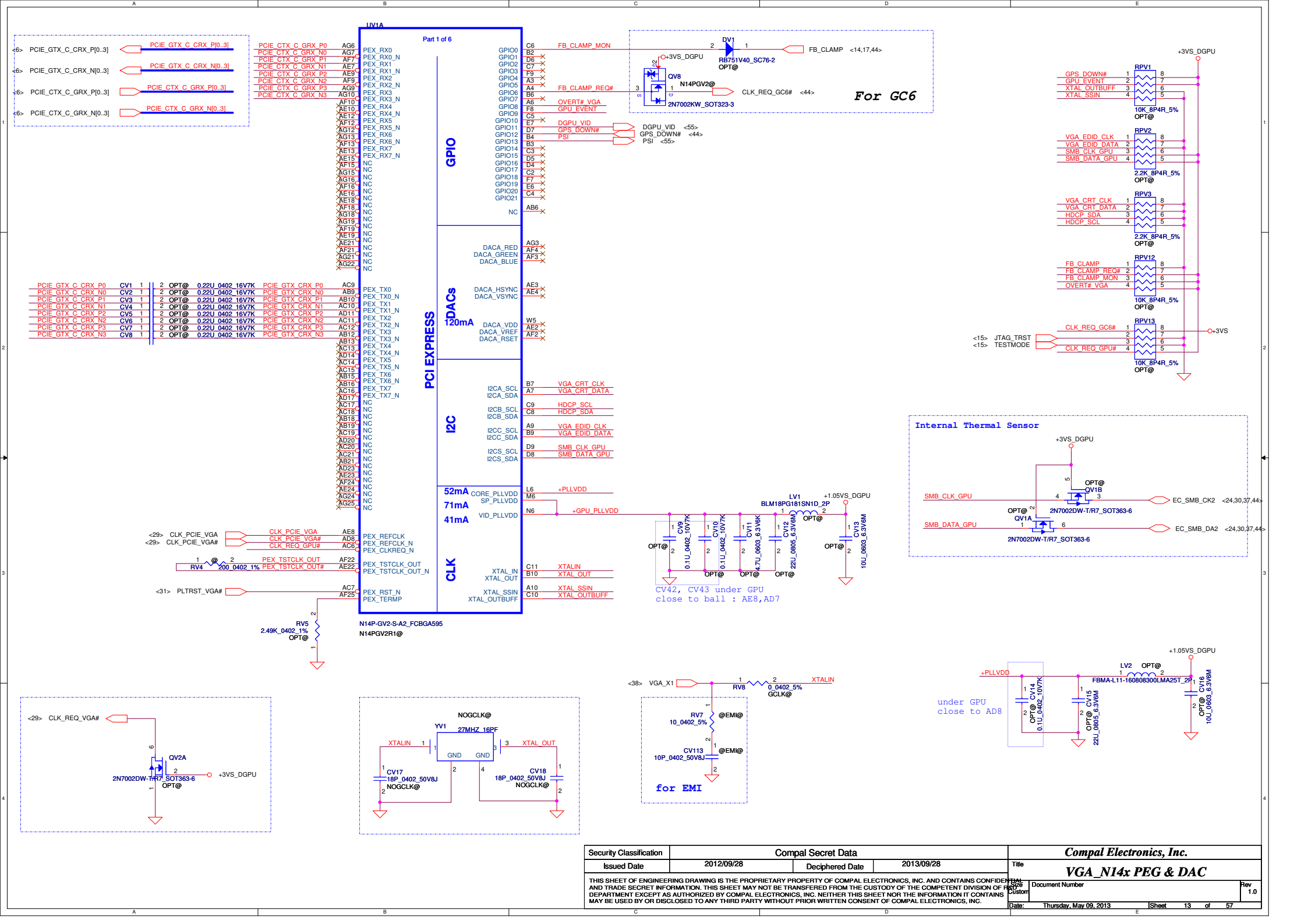
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

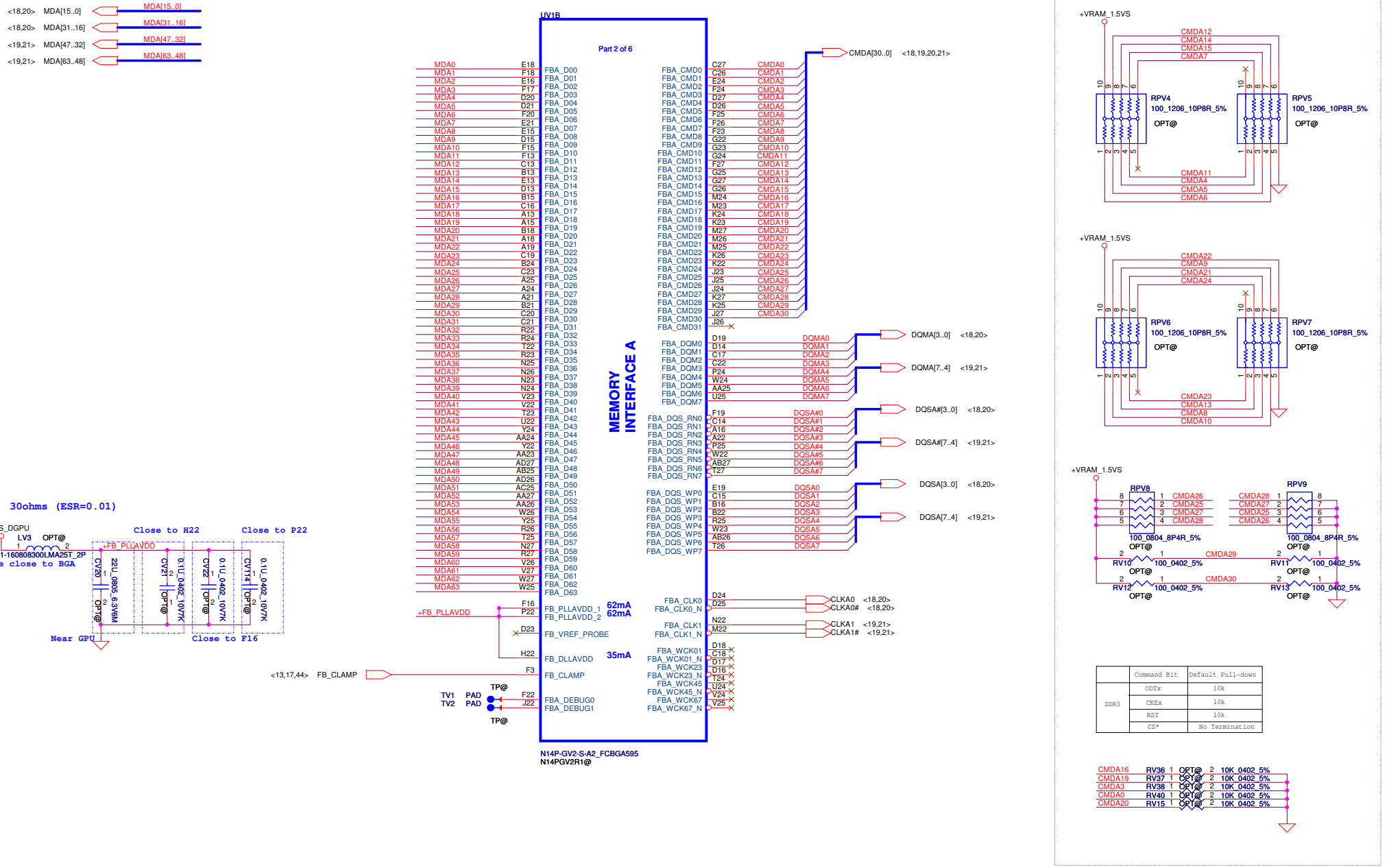
Title: ***DDRIII-SODIMM1***

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 12 of 57

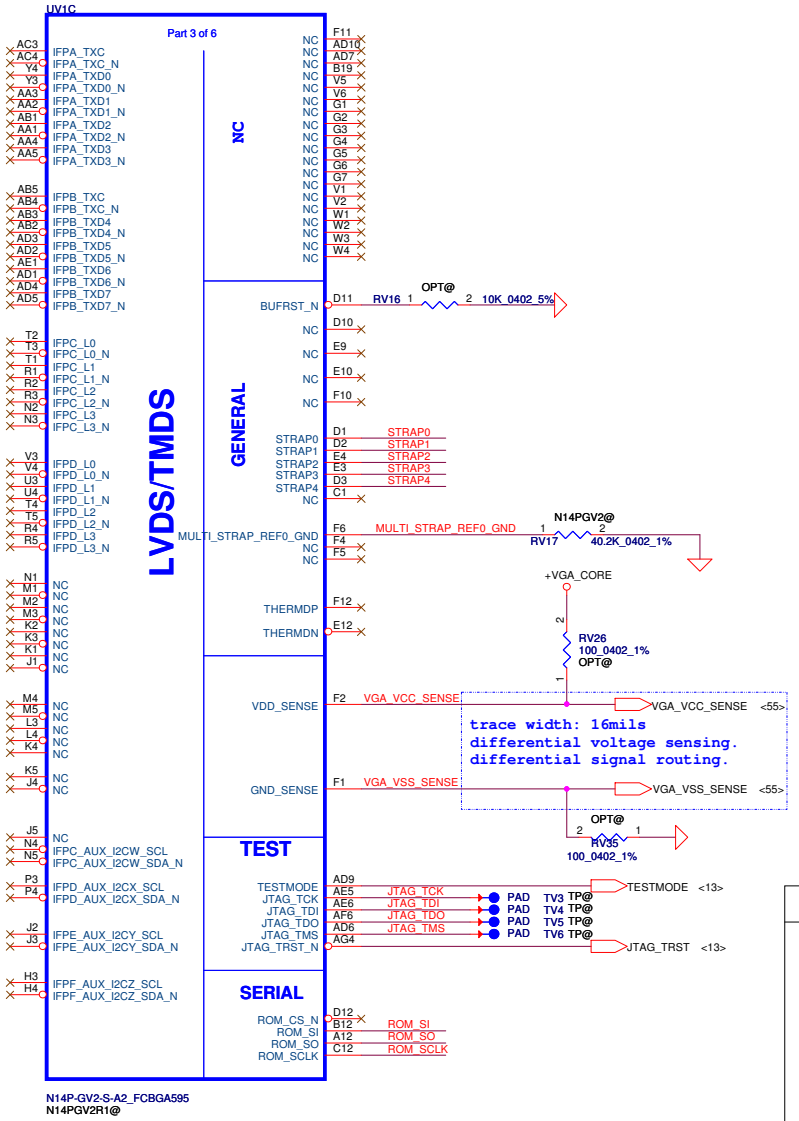

UV1A
Part 1 of 6
PCI EXPRESS
GPIO
DACs
120mA
I2C
CLK
52mA
71mA
41mA
N14P-GV2-S-A2_FCBGA595
N14PGV2R1@
For GC6
Internal Thermal Sensor
CV42, CV43 under GPU close to ball : AE8,AD7
under GPU close to AD8
for EMI
NOGCLK@
YV1
27MHZ_16PF
Compal Secret Data
Compal Electronics, Inc.
VGA_N14x PEG & DAC
Issued Date 2012/09/28
Deciphered Date 2013/09/28
Thursday, May 09, 2013
Sheet 13 of 57

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.			
Title: N14x VRAM Interface			
Size: Custom	Document Number		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 14 of 57		

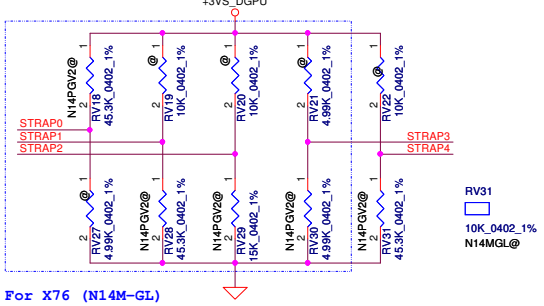


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

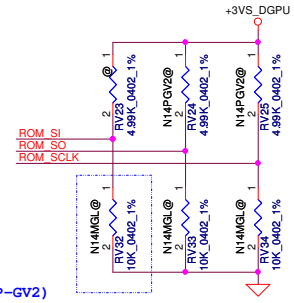
SKU	Device ID	biit5 to bit0
N14P-GV2	0x1292	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS



For X76 (N14M-GL)



For X76 (N14P-GV2)

GPU		FB Memory gDDR3			ROM_SI
N14P-GV2	128Mx16	Samsung	900MHz	K4W2G1646E-BC11	PD 45.3K
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	PD 34.8K
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	PD 30K
	256Mx16	Samsung	900MHz	K4W4G1646B-HC11	PD 20K
		Micron	900MHz	MT41K256M16HA-107G	PD 10K

GPU		FB Memory gDDR3			STRAP[3:0]
N14M-GL	128Mx16	Samsung	900MHz	K4W2G1646E-BC11	0101
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	0110
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	0001
	256Mx16	Samsung	900MHz	K4W4G1646B-HC11	1011
		Hynix	900MHz	H5TC4G63AFR-11C	0100
		Micron	900MHz	MT41K256M16HA-107G	1101

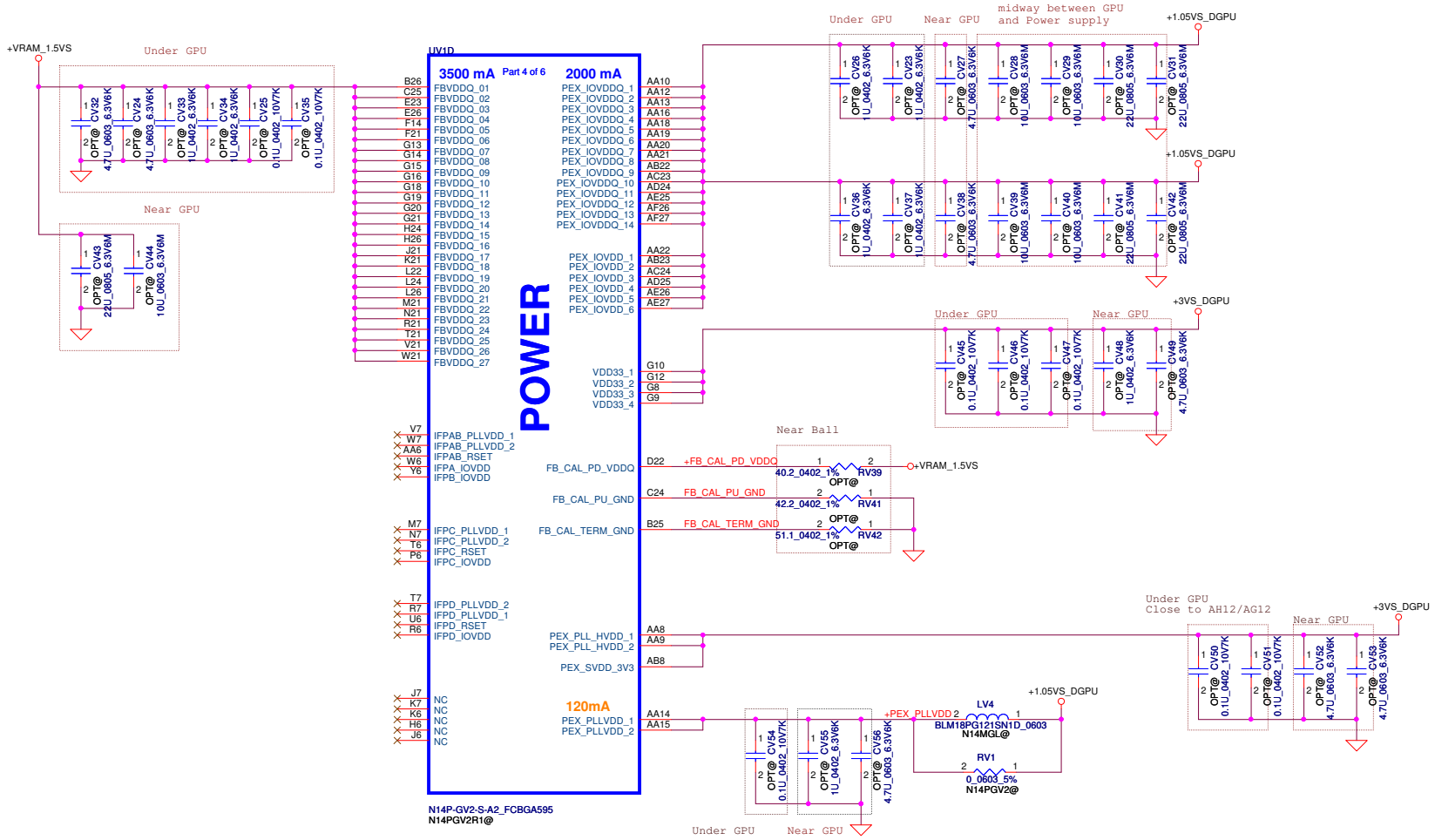
Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N14x LVDS&TMDS

Size: Custom | Document Number | Rev 1.0

Date: Thursday, May 09, 2013 | Sheet 15 of 57



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/28	Deciphered Date 2013/09/28	Title: VGA_N14x POWER
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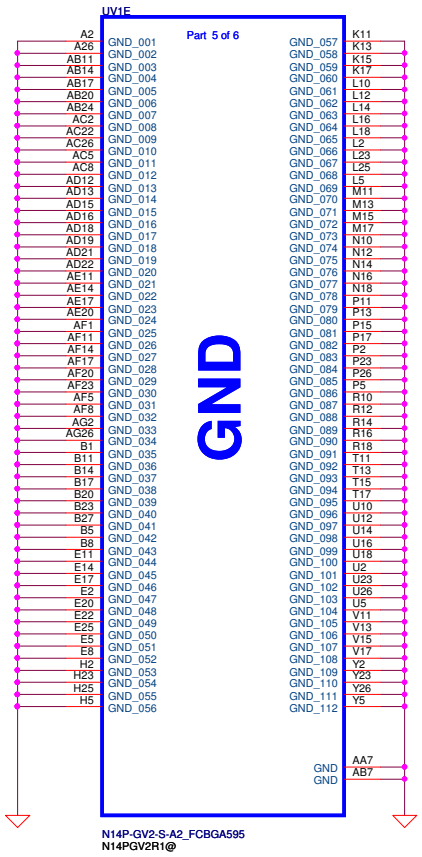
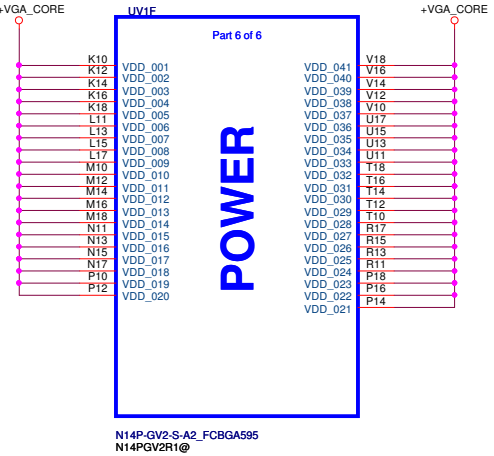
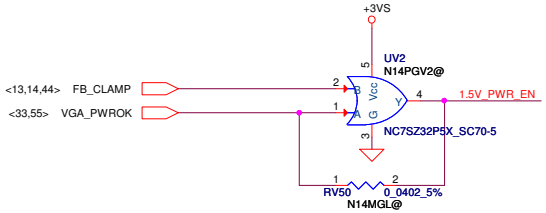
			Date: Thursday, May 09, 2013; Sheet 16 of 57

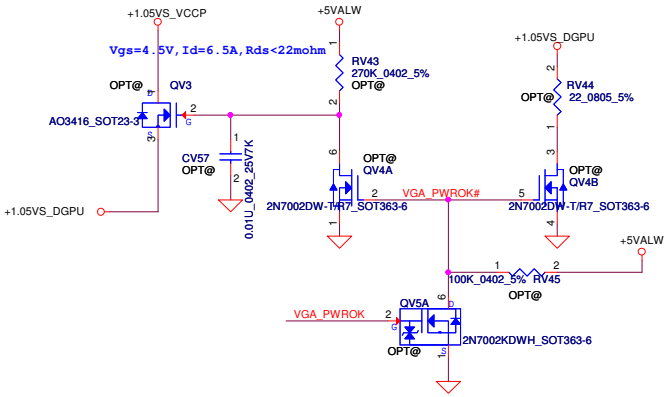




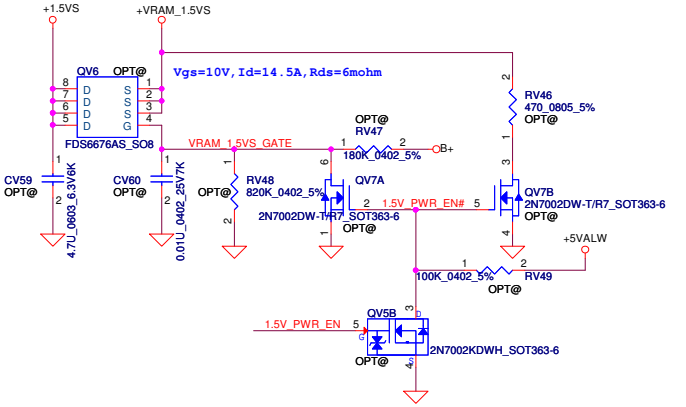
For GC6



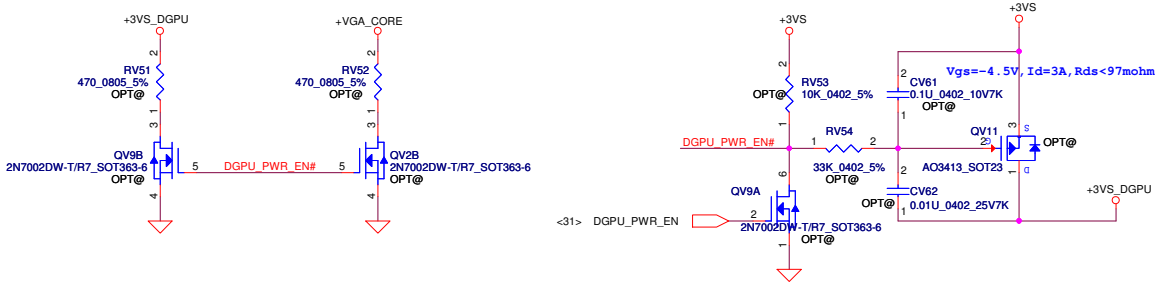
+1.05VS_VCCP to +1.05VS_DGPU



+1.5V to +VRAM_1.5VS



+3VS to +3VS_DGPU



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

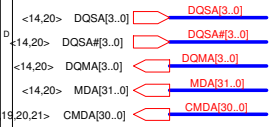
Title: **VGA_N14x POWER & GND**

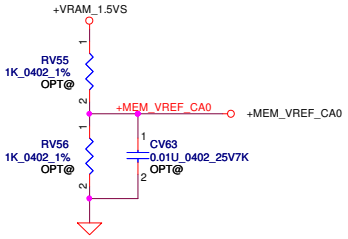
Size	Document Number	Rev
Custom		1.0

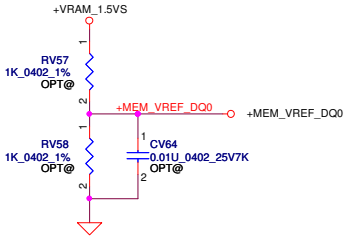
Date: Thursday, May 09, 2013 Sheet 17 of 57

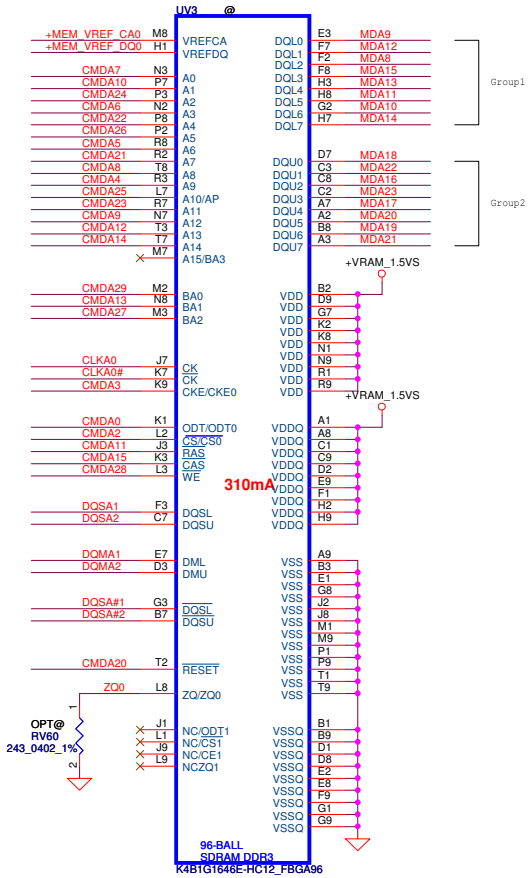
RANK 0 [31...0]

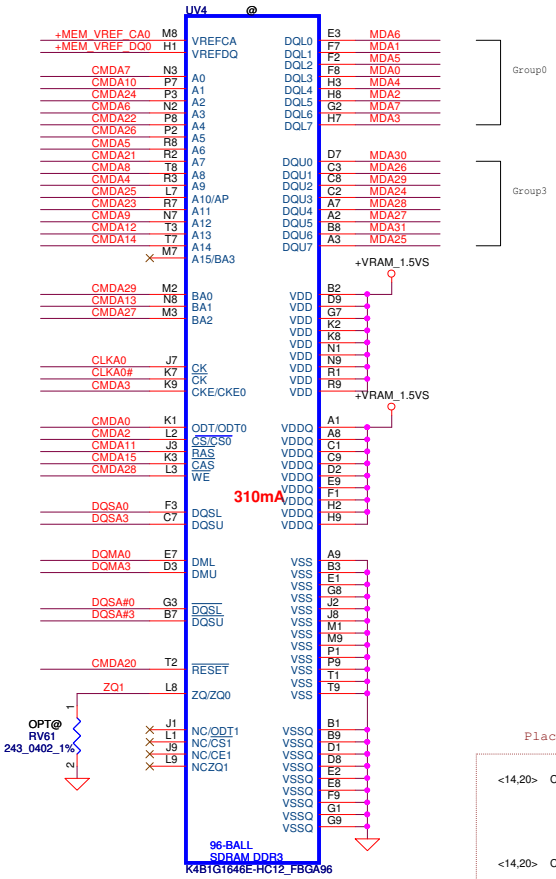
VRAM DDR3 Chips





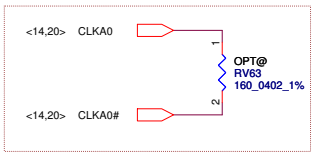


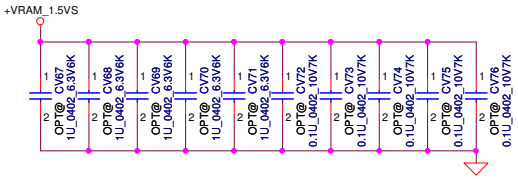


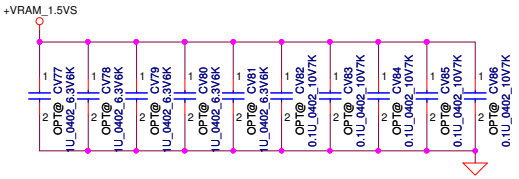


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

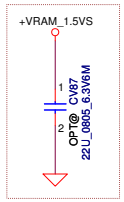
Place close to the first T point







Place close to RANK0 VRAM



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

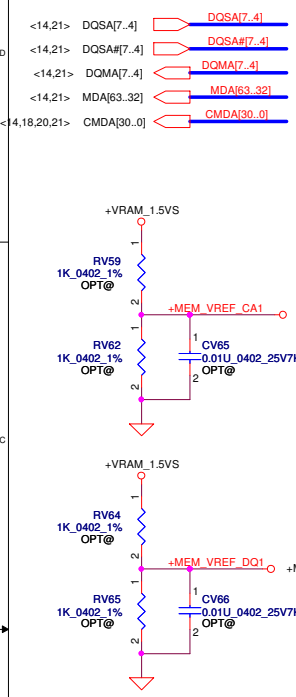
Title: **VGA_N14x VRAM RANK 0L**

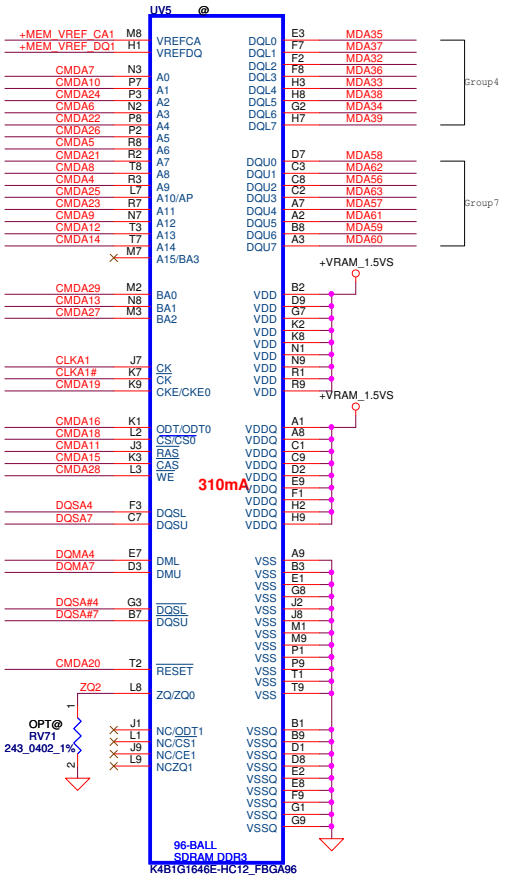
Size: Custom | Document Number | Rev: 1.0

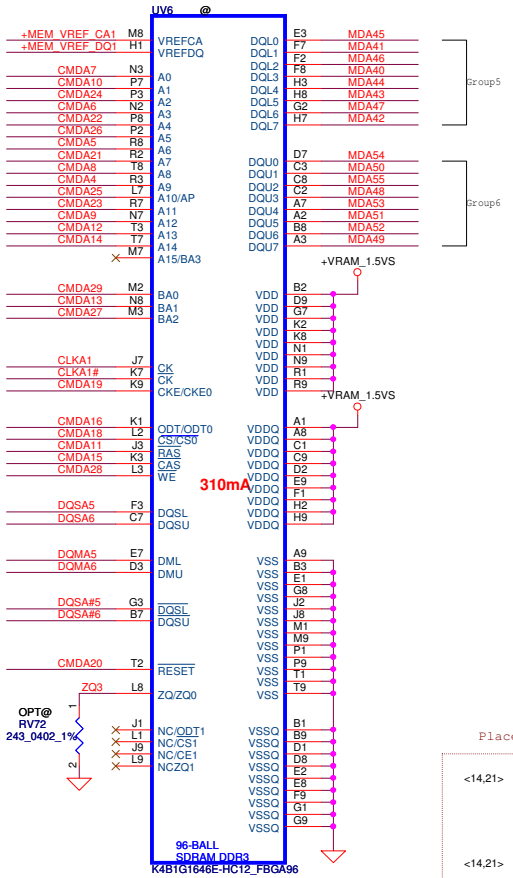
Date: Thursday, May 09, 2013 | Sheet 18 of 57

RANK 0 [63...32]

VRAM DDR3 Chips

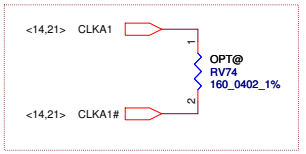


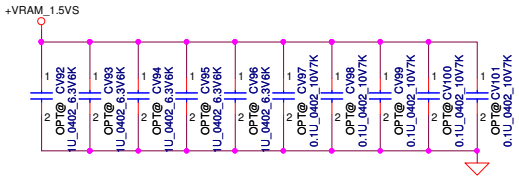


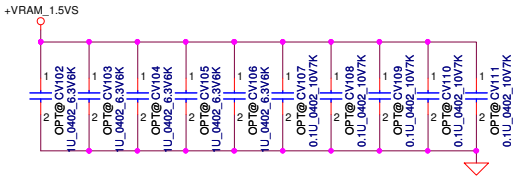


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

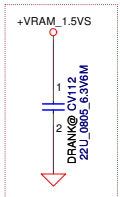
Place close to the first T point







Place close to RANK1 VRAM



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 0H

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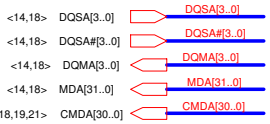
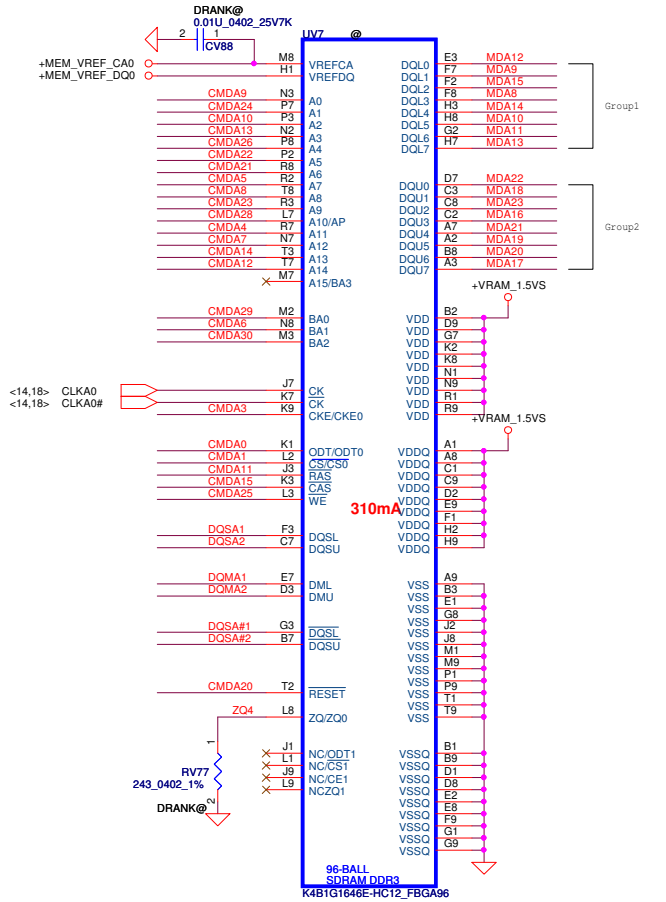
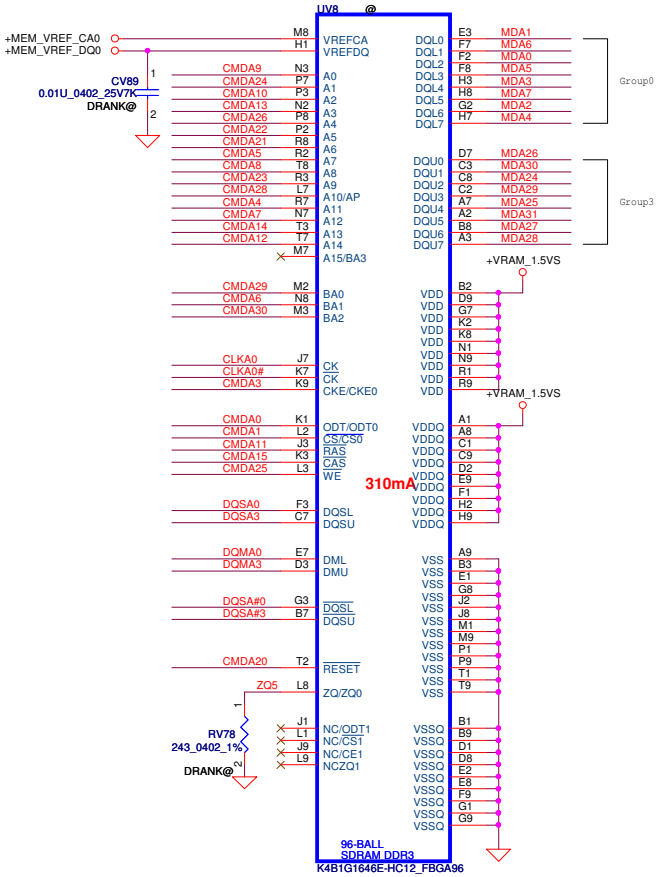
Date: Thursday, May 09, 2013 | Sheet 19 of 57

RANK 1 [31...0]

VRAM DDR3 Chips







Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

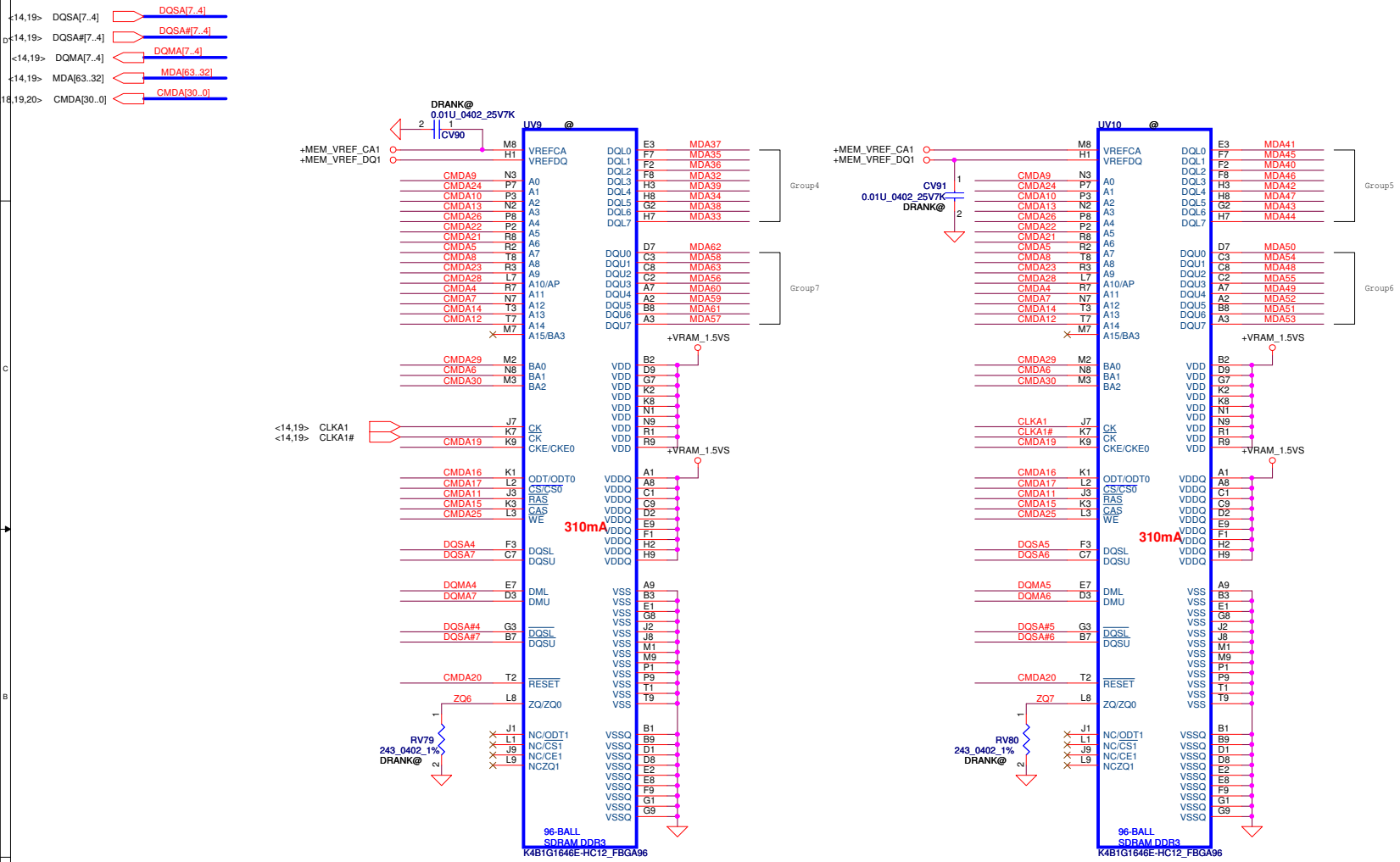
Title: VGA_N14x VRAM RANK 1L

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 20 of 57

RANK 1 [63...32]

VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 1H

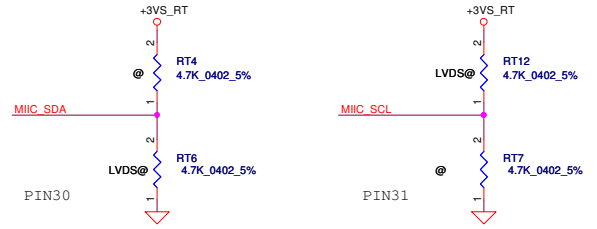
Size: Custom | Document Number | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 21 of 57

Mode Configure

ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
※EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

〈 ※Default mode 〉



SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT3
2132R	Use 0 ohm	mount LT3

※ If use 2132R, please select LDO mode as default.

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

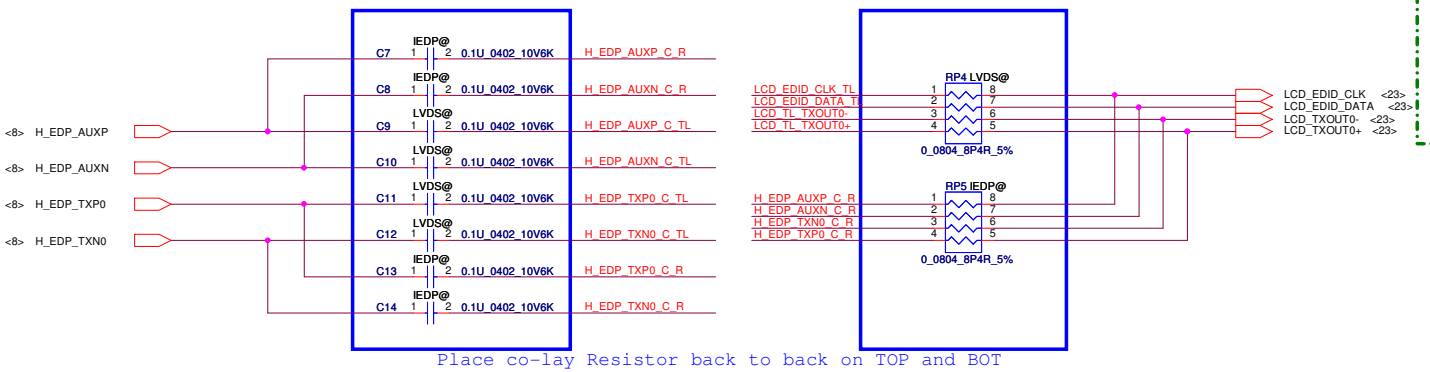
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

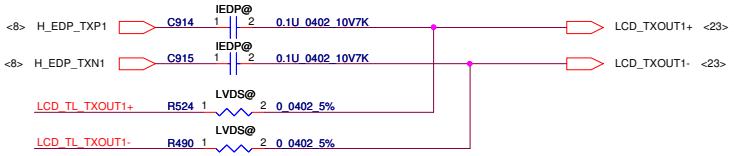
PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

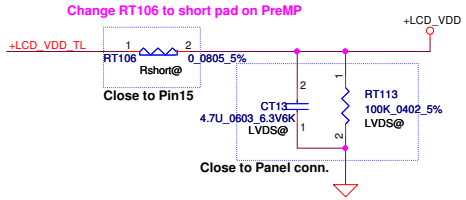
* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R

2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter







Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: LVDS Translator - RTD2132S

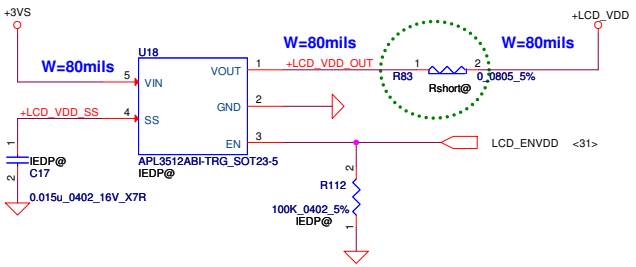
Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 22 of 57

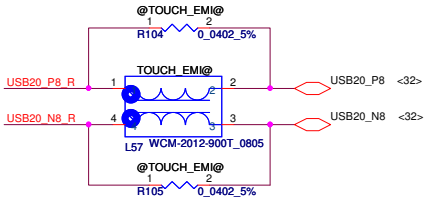
LCD POWER CIRCUIT (For EDP panel only)

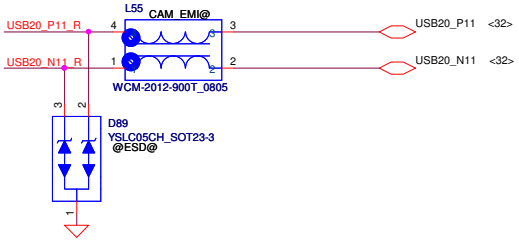
When you use 2132R series type of LVDS translator,
You can delete this portion. If you use 2132S, please don't.

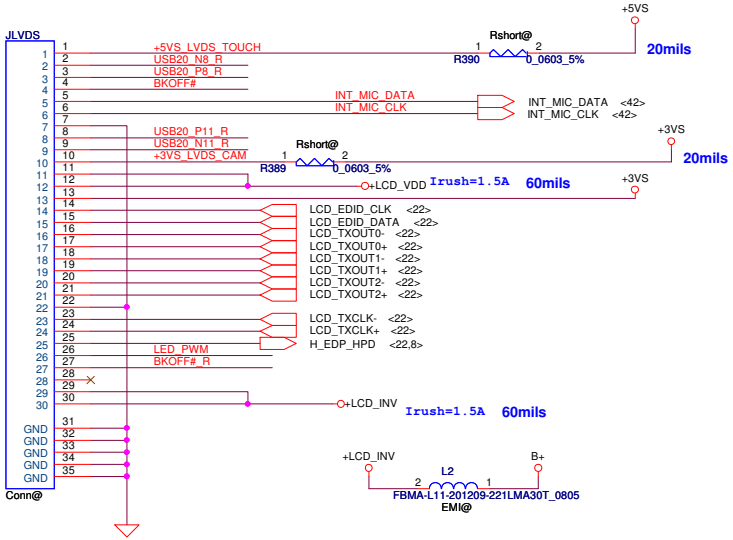
Change R83 to short pad on PreMP

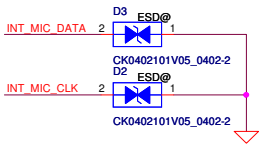


BTO : TOUCH@EMI@

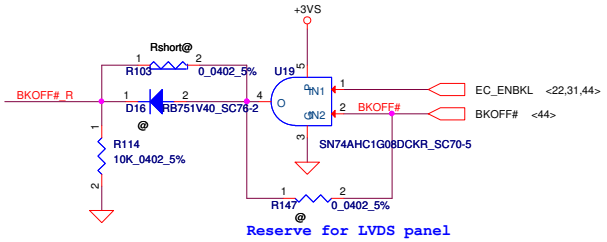




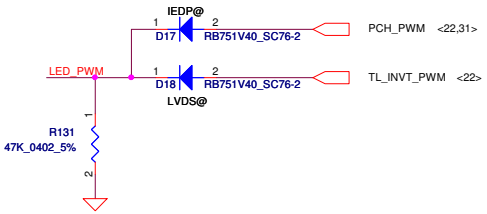




Mount U19 for flash line issue on LVDS panel and change R103 to short pad for PreMP



Reserve for LVDS panel



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: *LVDS*

Size: Custom	Document Number: VSKAA	Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 23 of 57	

Default to PS8401 & PS8201 I2C Control Mode

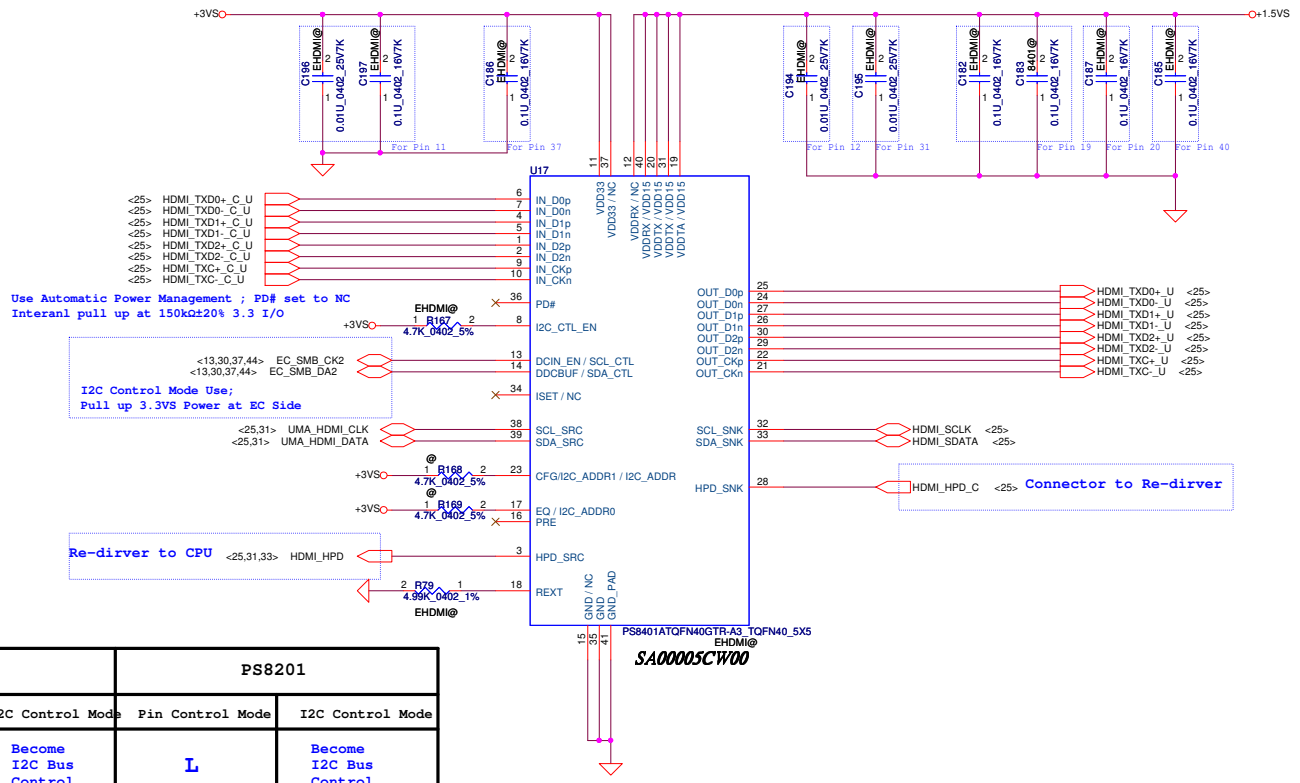
I2C Mode HDMI ID Setting

If PS8401 use I2C Mode , EQ=I2C_ADDR0 , CFG = I2C_ADDR1

For PS8401
I2C control bus address LSB; Internal pull down at 150kohz±20%, 3.3V I/O.
[I2C_ADDR1, I2C_ADDR0] ; I2C Address (W/R)=
LL: 0x4C/4D (default)
LH: 0x5C/5D
HL: 0xCC/CD
HH: 0xEC/ED

If PS8401 use I2C Mode , EQ=I2C_ADDR

For PS8201
I2C control bus address LSB; Internal pull down at ~150k ohz, 3.3V I/O.
[I2C_ADDR] ; I2C Address (W/R)=
L: 0x64/65 (default)
H: 0xE4/E5

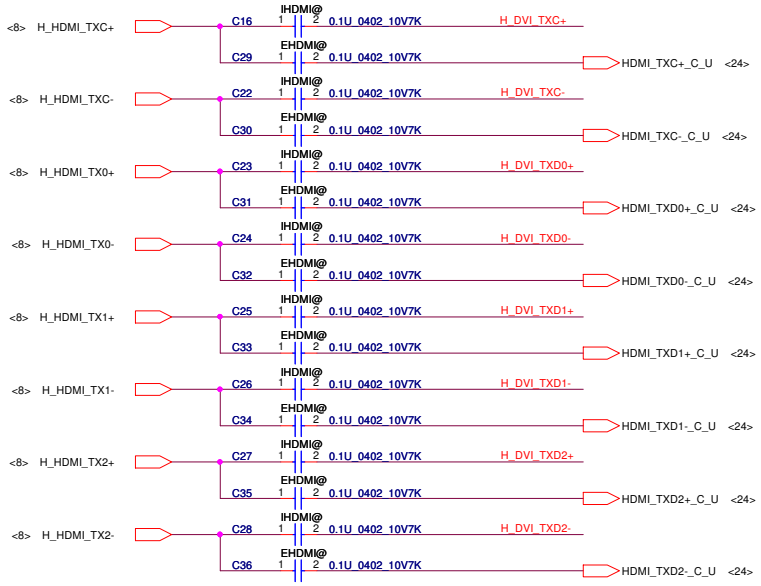


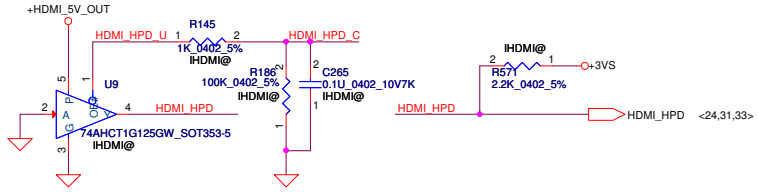
Strap H:3.3V M:1.65V L:0V

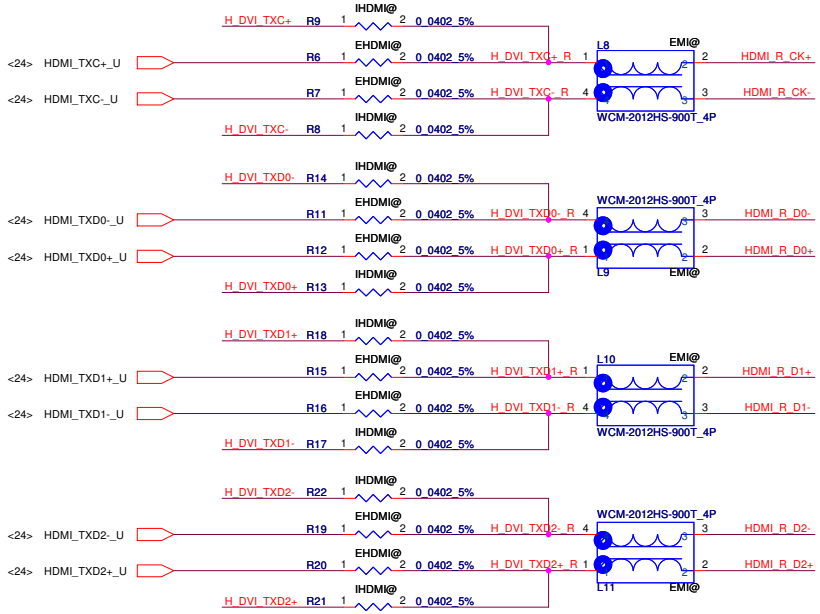
Net name	Description	PS8401		PS8201	
		Pin Control Mode	I2C Control Mode	Pin Control Mode	I2C Control Mode
DCIN_EN	DC cou;ing enable; Internal pull down at 150k ohz ±20%, 3.3V I/O. L: default, AC coupling input H: DC coupling input	L	Become I2C Bus Control	L	Become I2C Bus Control
DDCBUF	Enable active DDC buffer; Internal pull down at 150k?±20%, 3.3V I/O. L: default, passive DDC pass-through H: active DDC buffer with default threshold M: active DDC buffer without internal pull up resistor	M	Become I2C Bus Control	M	Become I2C Bus Control
ISET	TMDS output swing adjustment; Internal pull down at 150kΩ±20%, 3.3V I/O. For PS8401 Only ISET = L: Default H: Increase +13% M: Reduce -13%	L	NC	NC	NC
CFG	CFG: Configuration pin, 3.3V IO, internal pull down at 150kΩ±20%. 3.3V I/O CFG = L: HDMI ID disable H: HDMI ID enable	H	NC	H	NC
EQ	EQ:Receiver equalization setting;; Internal pull down at ~150k?, 3.3V I/O For PS801 EQ = L:programmable EQ for channel loss up to 6.5dB @ 3.0Gbps H:programmable EQ for channel loss up to 9.5dB @ 3.0Gbps M:programmable EQ for channel loss up to 3dB @ 3.0Gbps For PS8401 EQ = L:programmable EQ for channel loss up to 12.4dB H:programmable EQ for channel loss up to 4.3dB M:programmable EQ for channel loss up to 8.6dB	M	NC	M	NC
PRE	Output pre-emphasis setting; Internal pull down at 150kΩ±20%, 3.3V I/O. PRE = L: No pre-emphasis H: 1.6dB pre-emphasis M: 2.5dB pre-emphasis	L	NC	L	NC
I2C_CTL_EN	I2C Control enable. Internal pull down at 150kΩ±20%. 3.3V I/O I2C_CTL_EN = LOW (L): Pin Control is selected. HIGH (H): I2C Control is selected.	L	H	L	H

Note: PS8401 have Jitter cleaning function and can control TMDS output swing , PS8201 don't have.

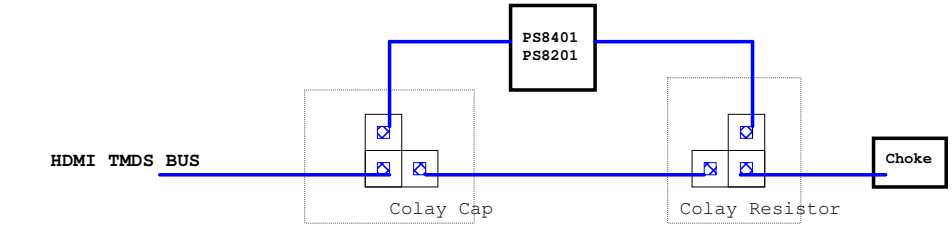
Compal Electronics, Inc.
Title: HDMI Re-driver
Size: Document Number: PS8201A & PS8401A Rev: 1.0
Date: Thursday, May 09, 2013 Sheet 24 of 57



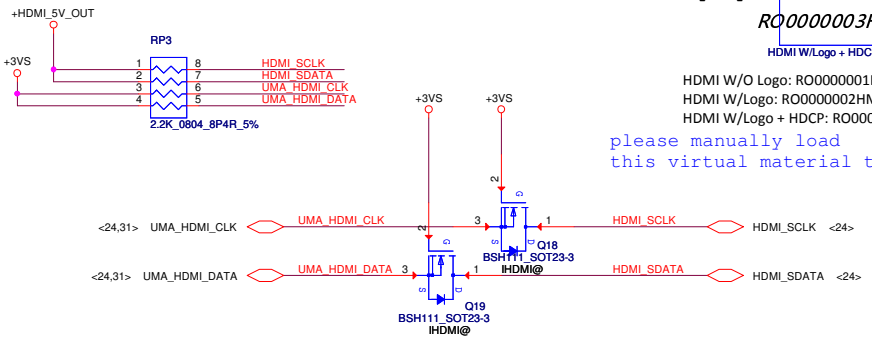




Common CHOKE use 90ohm



Componet close to Conn.
Impedance depend on platform design guide



HDMI Royalty

ZZZ HDMI45@

RO0000003HM

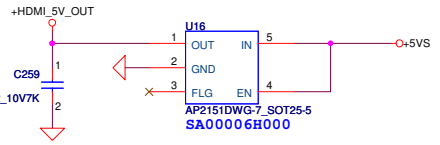
HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

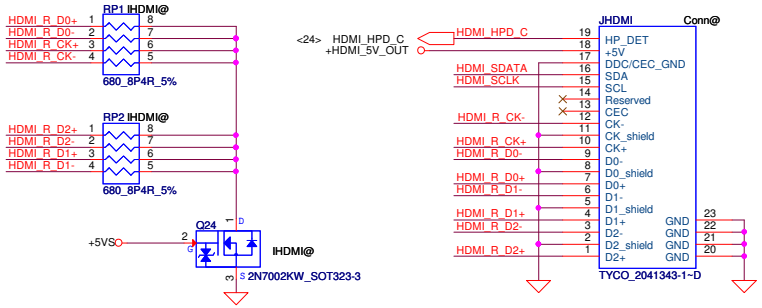
please manually load
this virtual material to 45@ BOM

HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

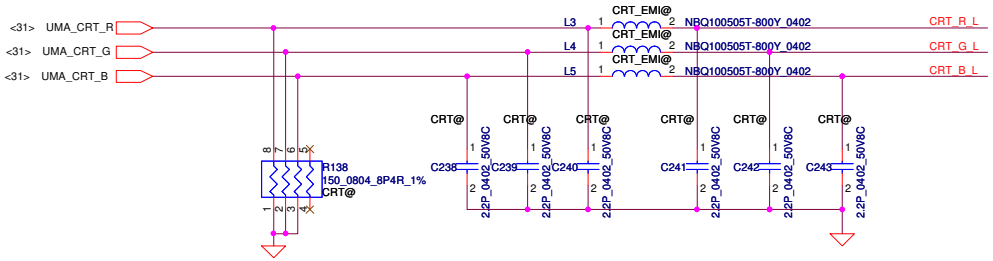
Title: ***HDMI Conn.***

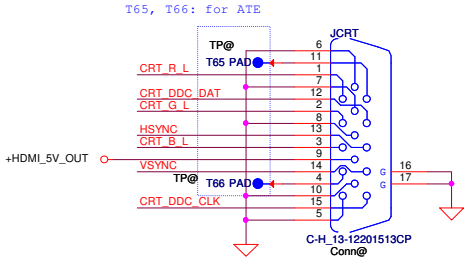
Size: B | Document Number: **VSKAA** | Rev: 1.0

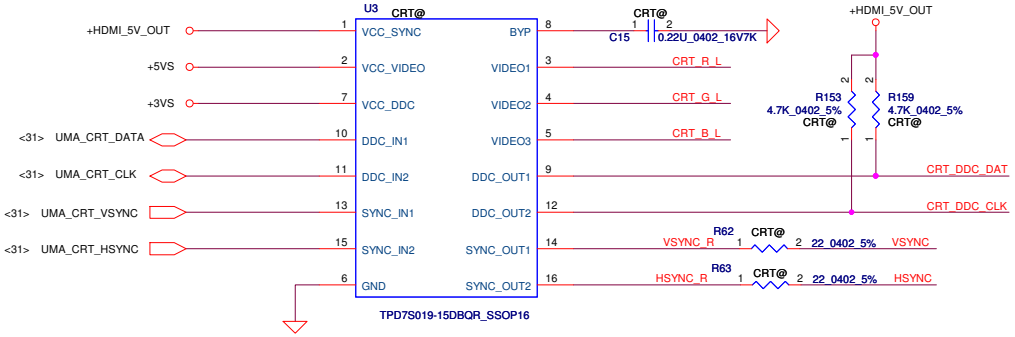
Date: Thursday, May 09, 2013 | Sheet 25 of 57

CRT CONNECTOR

BTO : CRT_EMI@

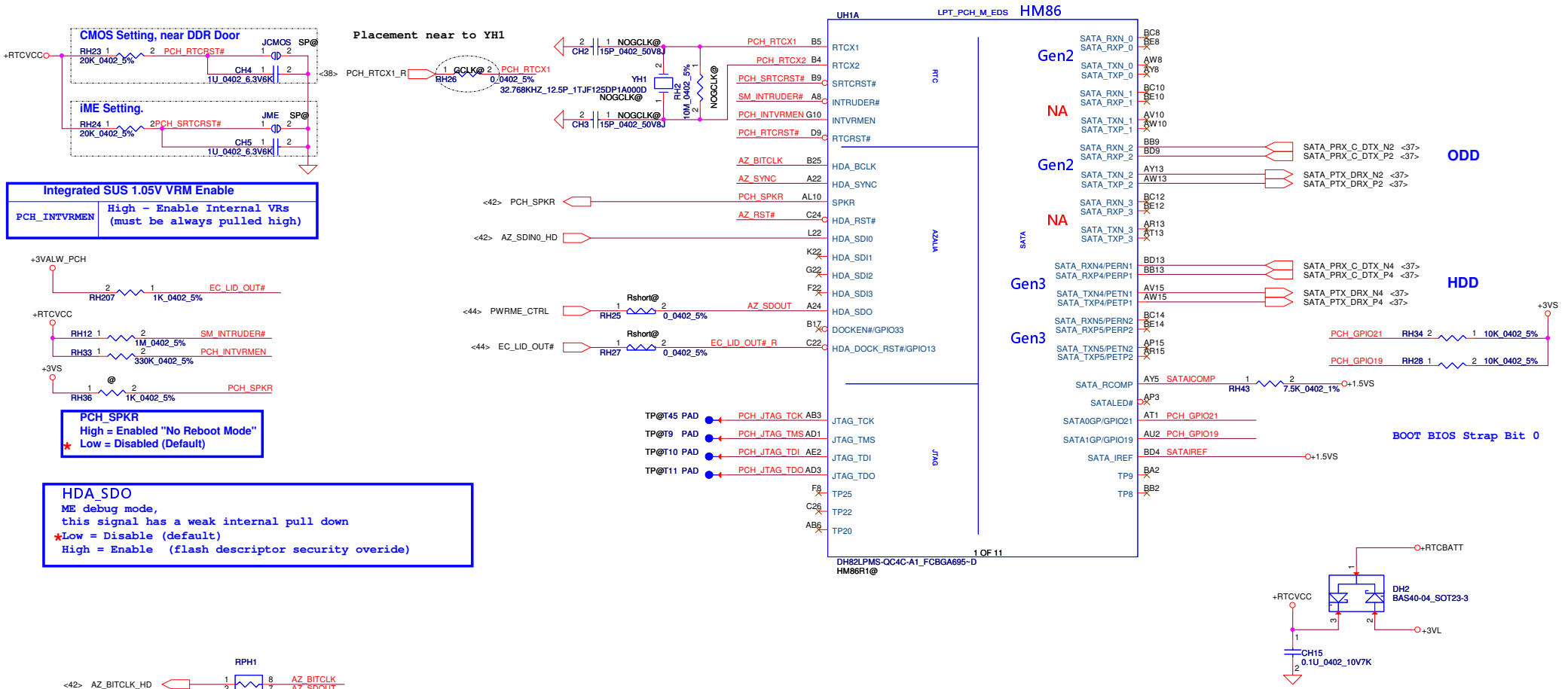






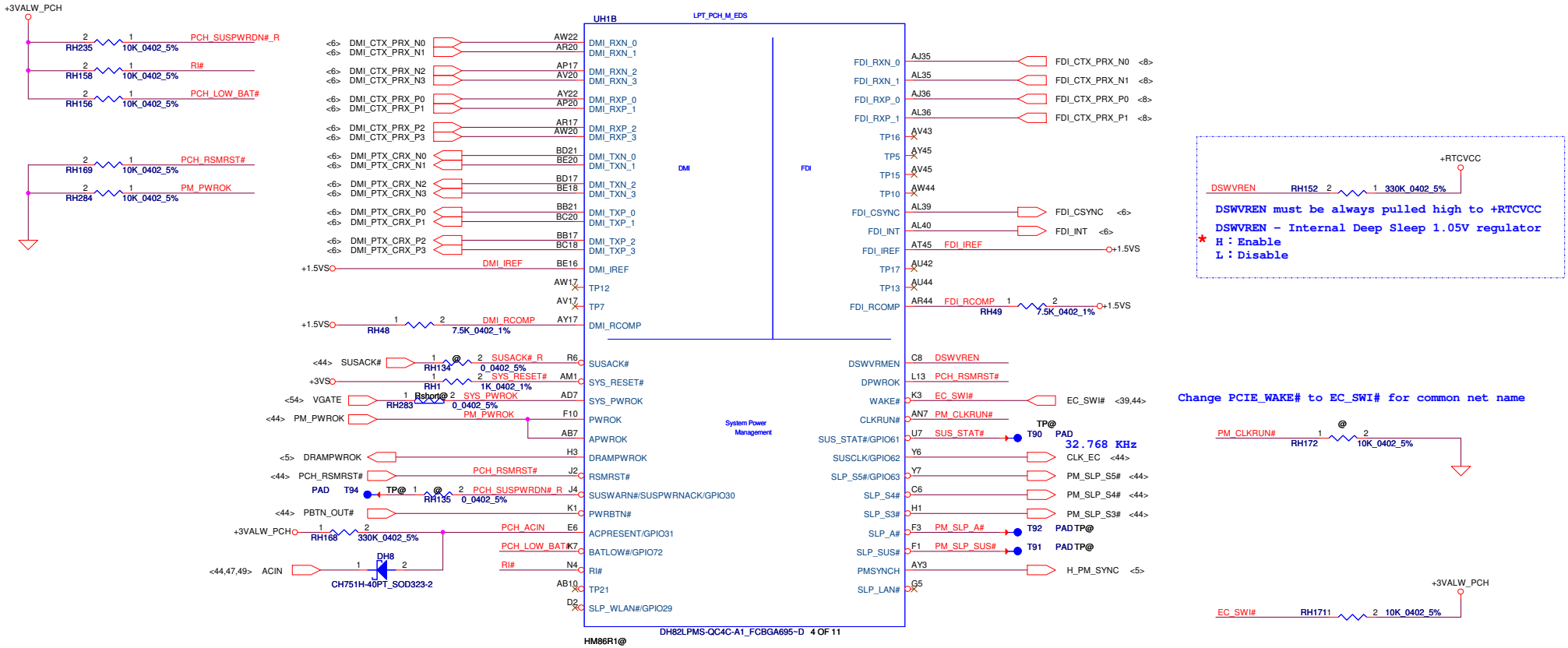
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/11/11	Deciphered Date	2012/12/31	Title: CRT

File: 5525	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 26 of 57		



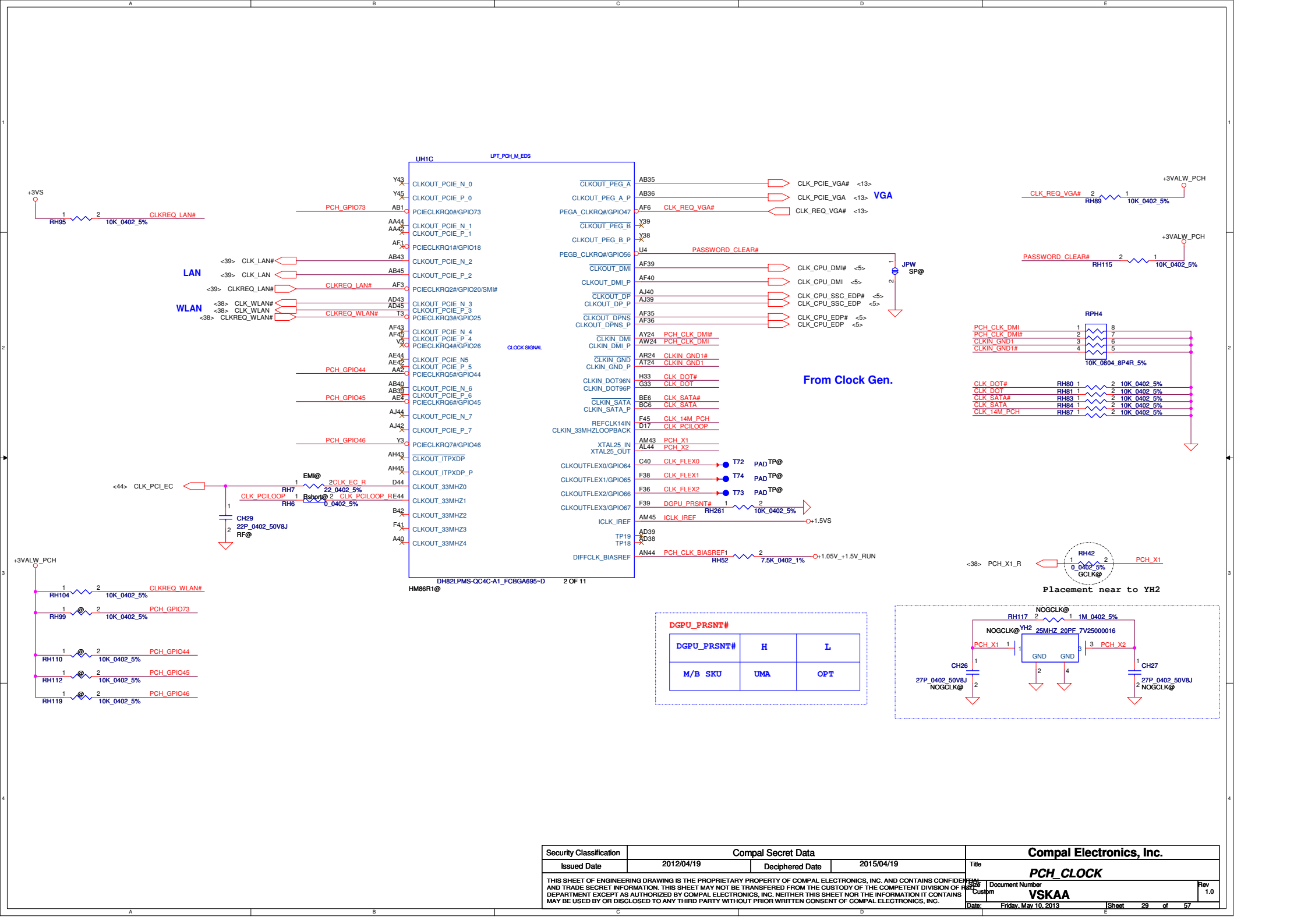
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

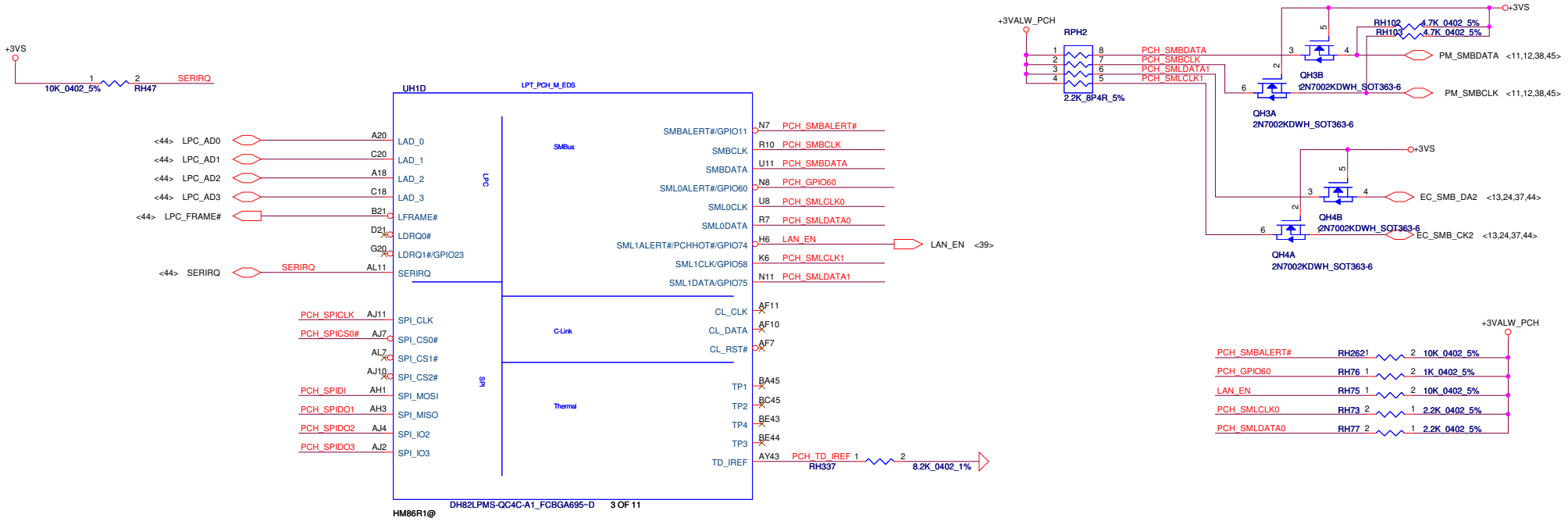
Compal Electronics, Inc.			
Title	PCH_HDA/JTAG/SATA		
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Friday, May 10, 2013	Sheet 27 of 57		



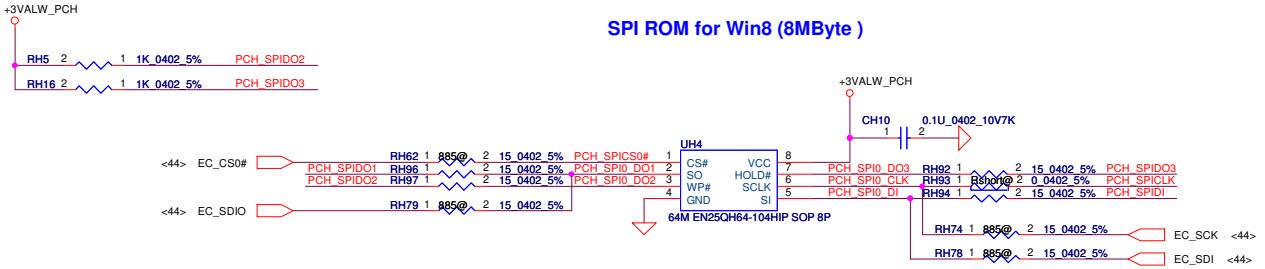
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_DMI/FDI/PM

Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Friday, May 10, 2013	Sheet 28 of 57		


UH1C
LPT_PCH_M_EDS
CLOCK SIGNAL
DH82LPMS-QC4C-A1_FCBGA695-D
2 OF 11
HM86R1@
From Clock Gen.
VGA
LAN
WLAN
JPW
SP@
RPH4
10K_0804_8P4R_5%
Placement near to YH2
DGPU_PRSNT#
DGPU_PRSNT# | H | L
M/B SKU | UMA | OPT
25MHZ_20PF_7V25000016
Security Classification
Compal Secret Data
Issued Date
2012/04/19
Deciphered Date
2015/04/19
Compal Electronics, Inc.
PCH_CLOCK
Document Number
VSKAA
Rev
1.0
Friday, May 10, 2013
Sheet 29 of 57



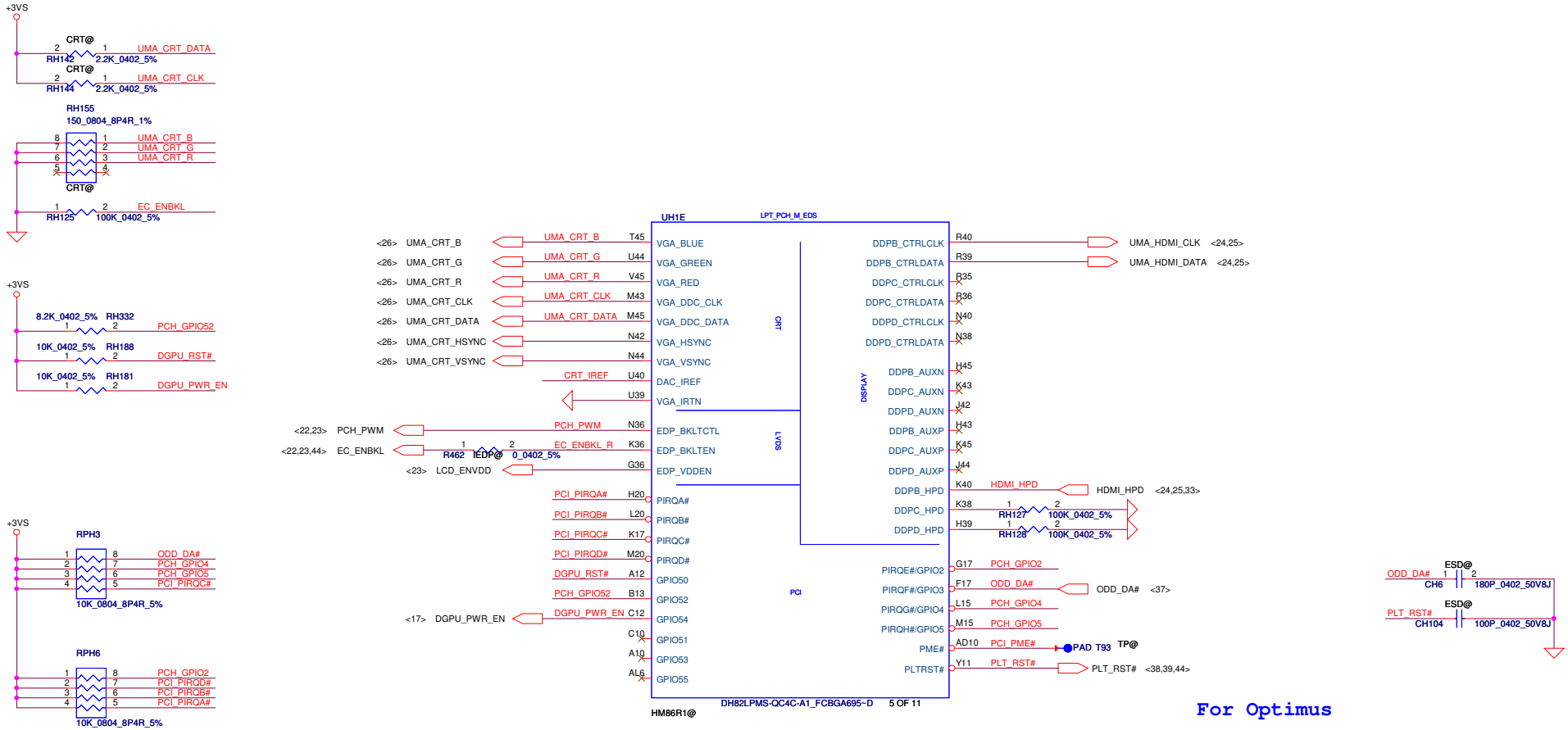
SPI ROM for Win8 (8MByte)



Socket: SP07000F500/SP07000H900

Please place UH4 close to UH1 PCH

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_LPC/SPI/SMBUS
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Friday, May 10, 2013	Sheet 30 of 57		



Boot BIOS Strap		
RF_OFF# PCH_GPIO51	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	* Low= A16 swap override Enable High= A16 swap override Disable

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_CRT/LVDS/HDMI/PCI
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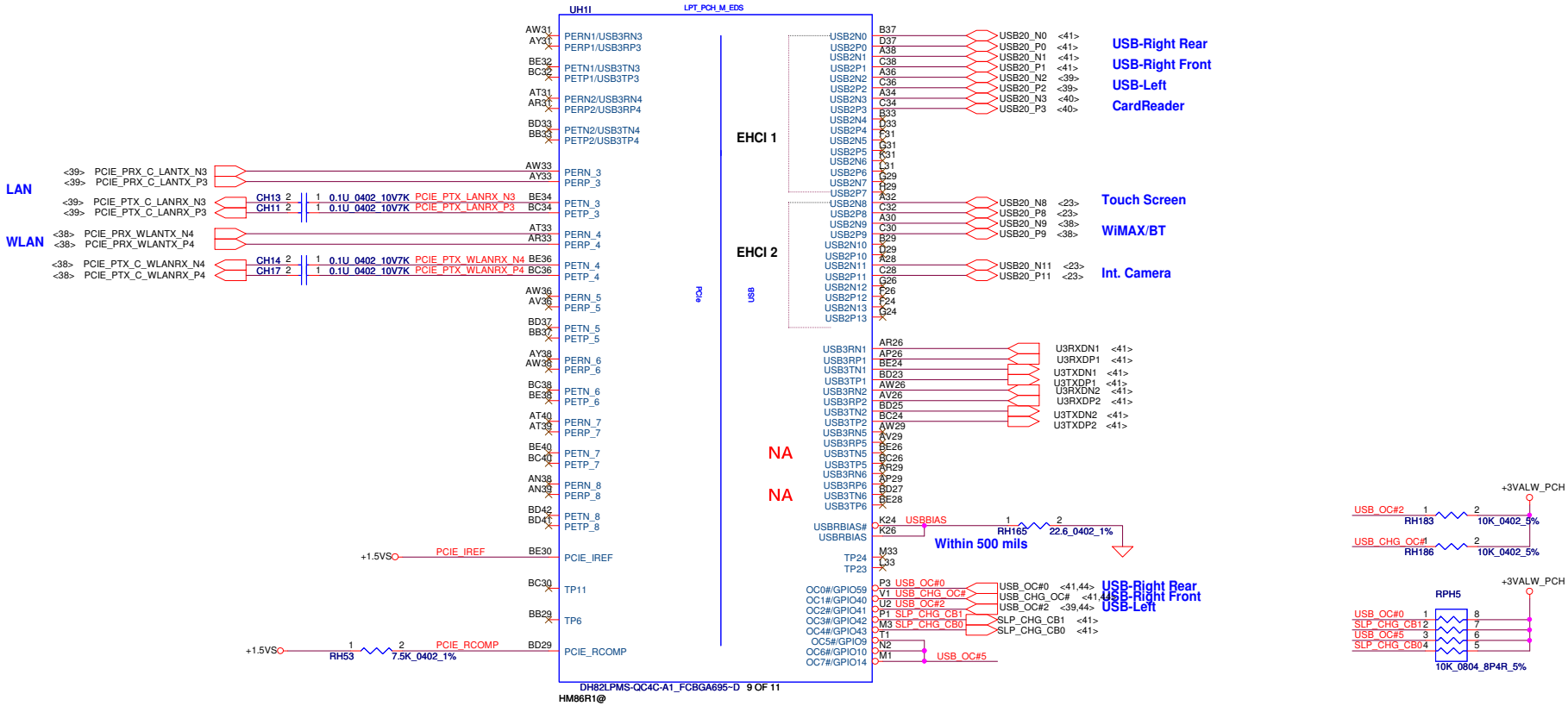
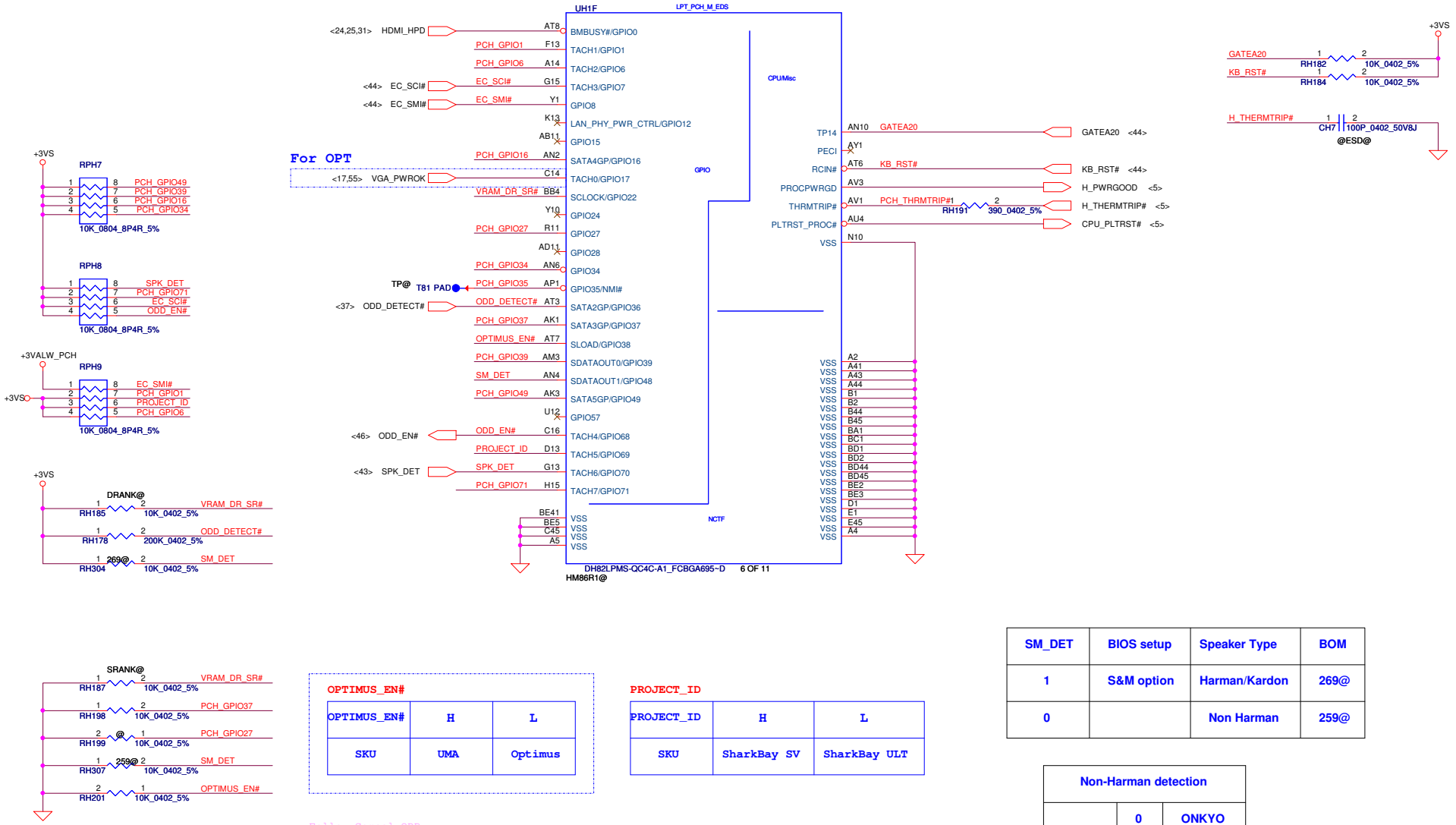
			Date: Friday, May 10, 2013; Sheet 31 of 57



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_PCIE/USB

Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Friday, May 10, 2013	Sheet 32 of 57		



OPTIMUS_EN#

OPTIMUS_EN#	H	L
SKU	UMA	Optimus

PROJECT_ID

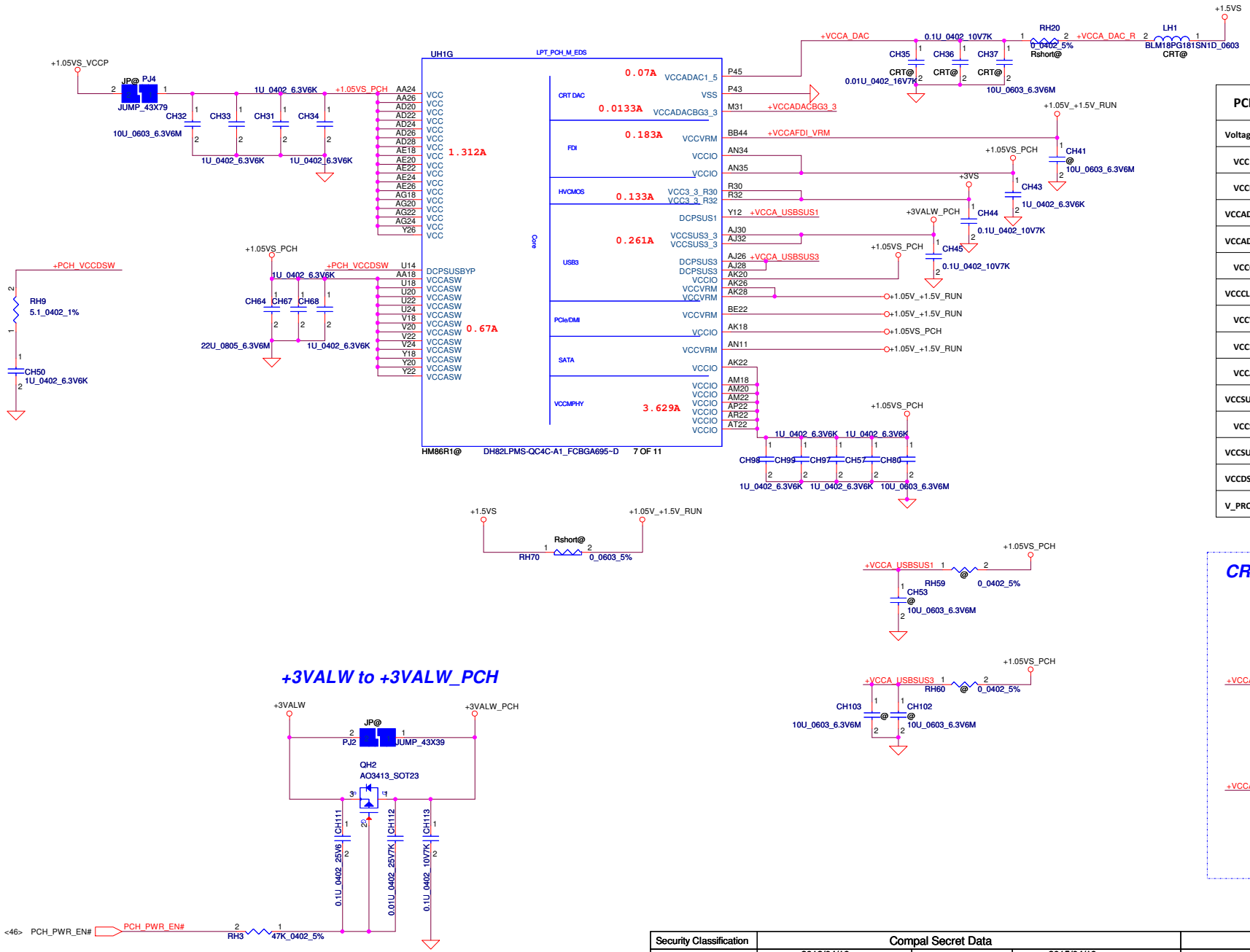
PROJECT_ID	H	L
SKU	SharkBay SV	SharkBay ULT

SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

Follow Compal ORB
and Intel Check list 460603 V1.5

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_CPU/GPIO
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Friday, May 10, 2013	Sheet 33 of 57		



PCH Power Rail Table (EDS Rev1.0)

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

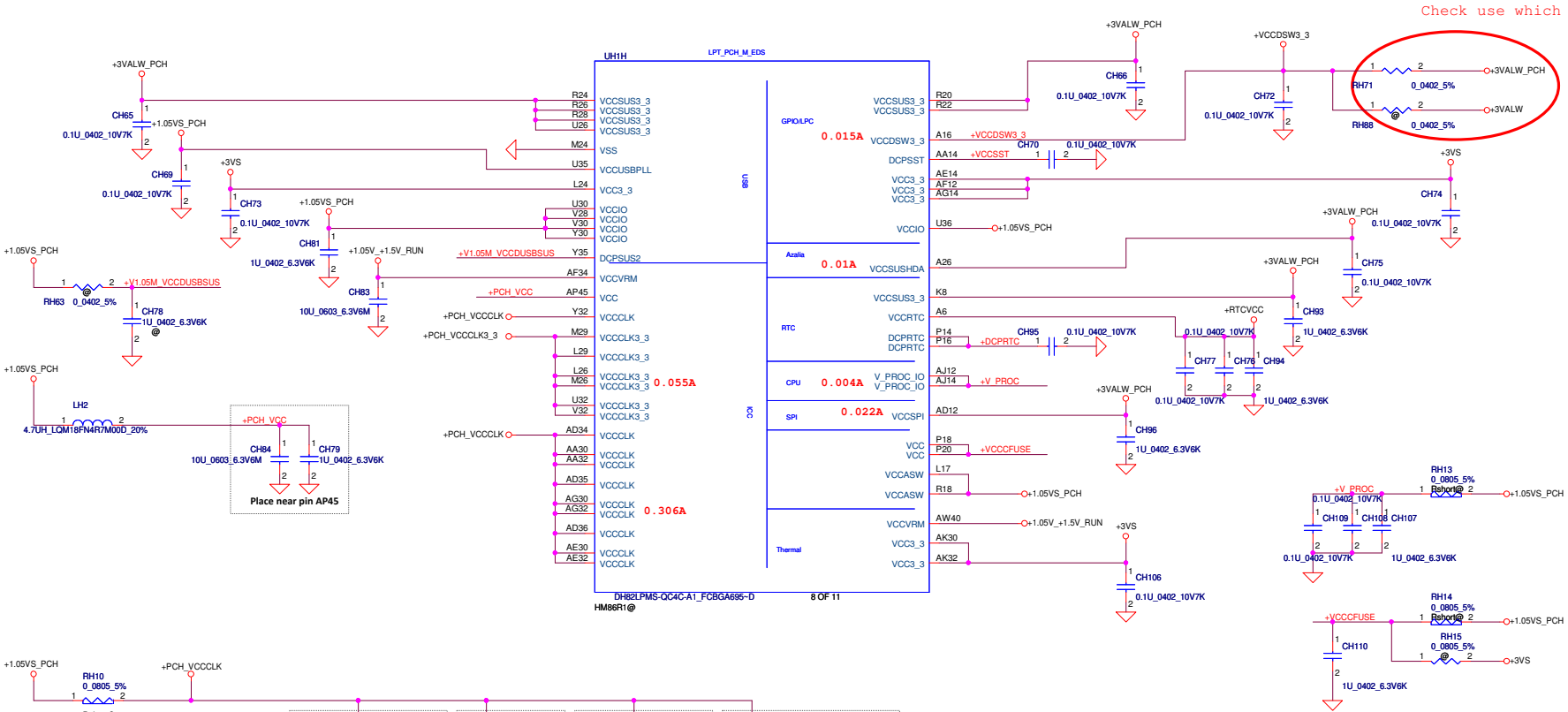
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: PCH_POWER-1

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Friday, May 10, 2013 | Sheet 34 of 57



PCH Power Rail Table (EDS Rev1.0)

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

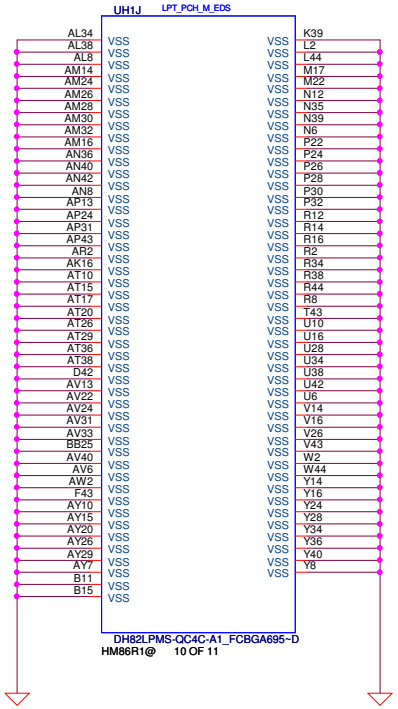
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

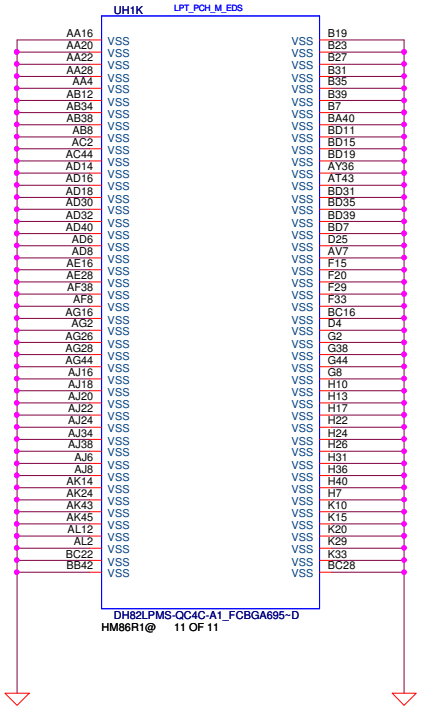
Compal Electronics, Inc.

Title: *PCH_POWER-2*

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Friday, May 10, 2013 | Sheet 35 of 57

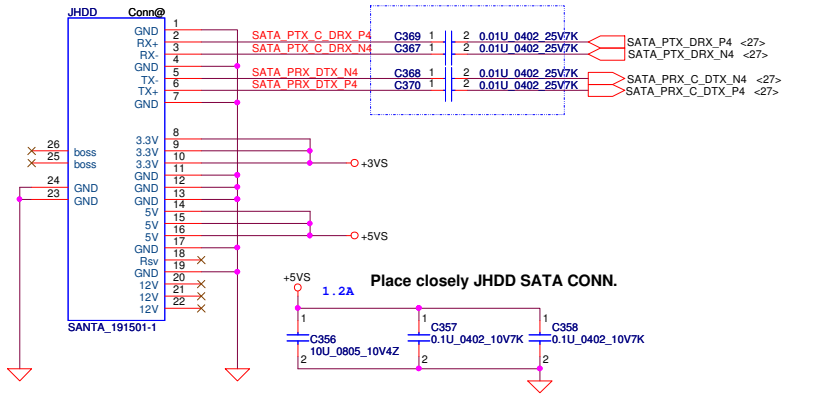




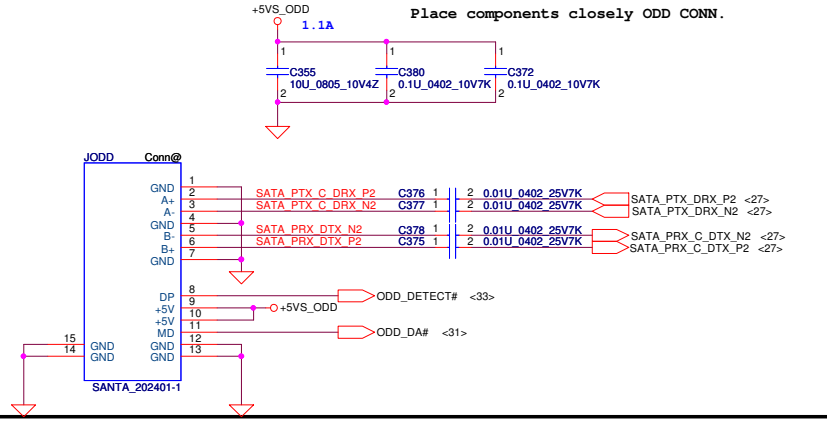
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Title	PCH_GND		
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date: Friday, May 10, 2013	Sheet 36 of 57		

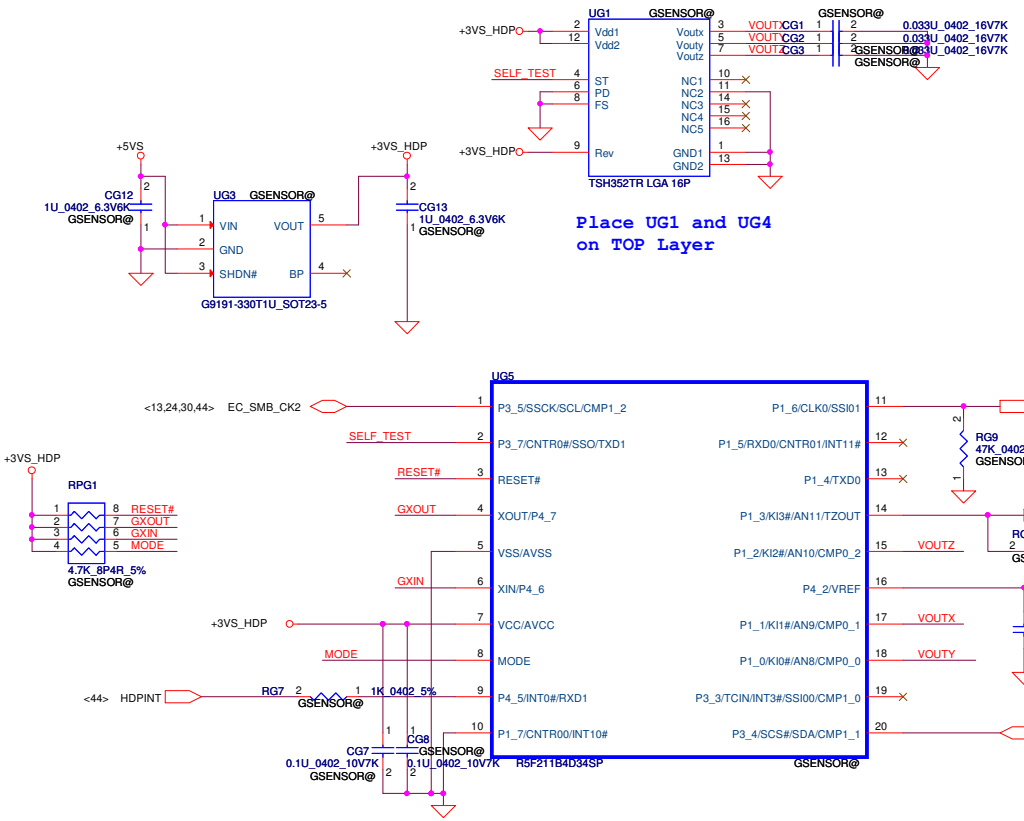
SATA HDD Conn.



SATA ODD Conn



G-Sensor



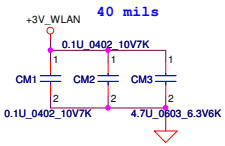
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

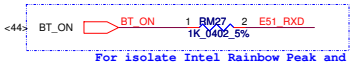
Compal Electronics, Inc.			
Title: HDD/Gsensor			
Size:	Document Number: VSKAA		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 37 of 57		

Slot 1 Half PCIe Mini Card-WLAN

WLAN&BT Combo module circuits

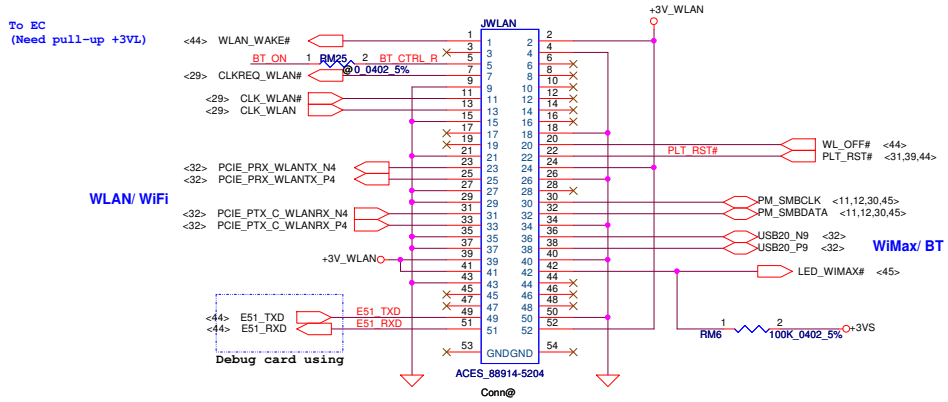
	BT on module Enable	BT on module Disable
BT_ON	H	L

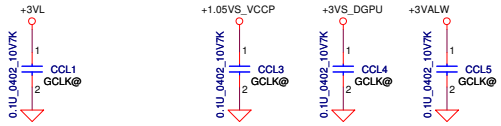


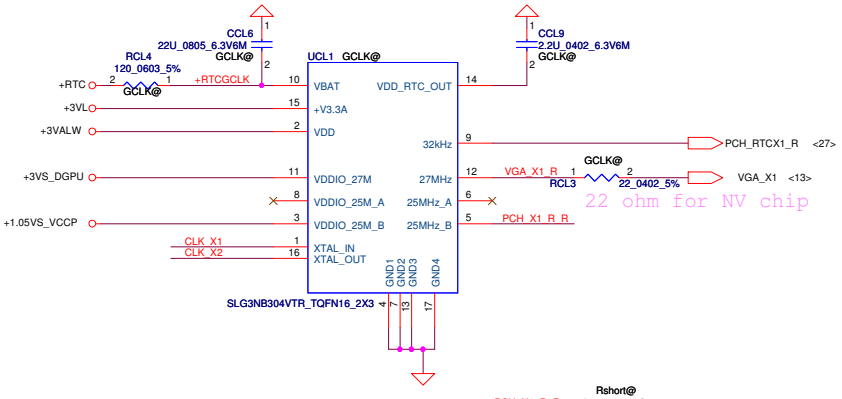


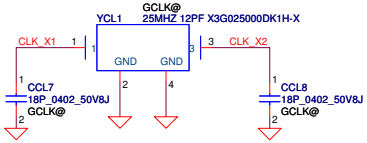
For isolate Intel Rainbow Peak and Compal Debug Card.

Slot 2 Full PCIe Mini Card- mSATA 14" no support









Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

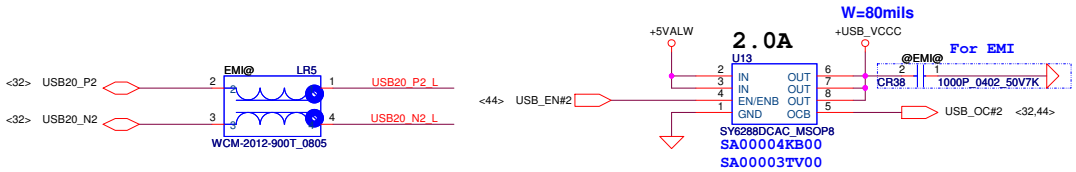
Compal Electronics, Inc.

Title: PCIe-WLAN/mSATA/GCLK

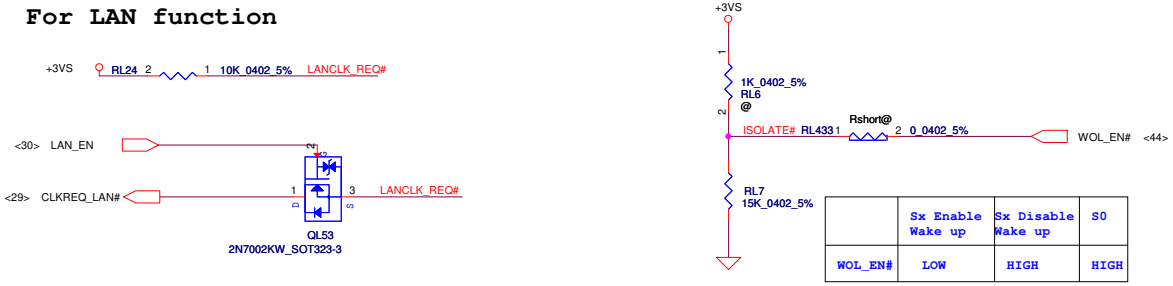
Size | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 38 of 57

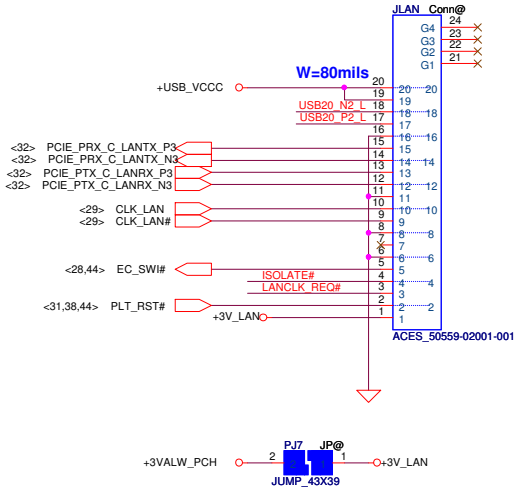
Left USB 2.0 x 1



For LAN function



	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

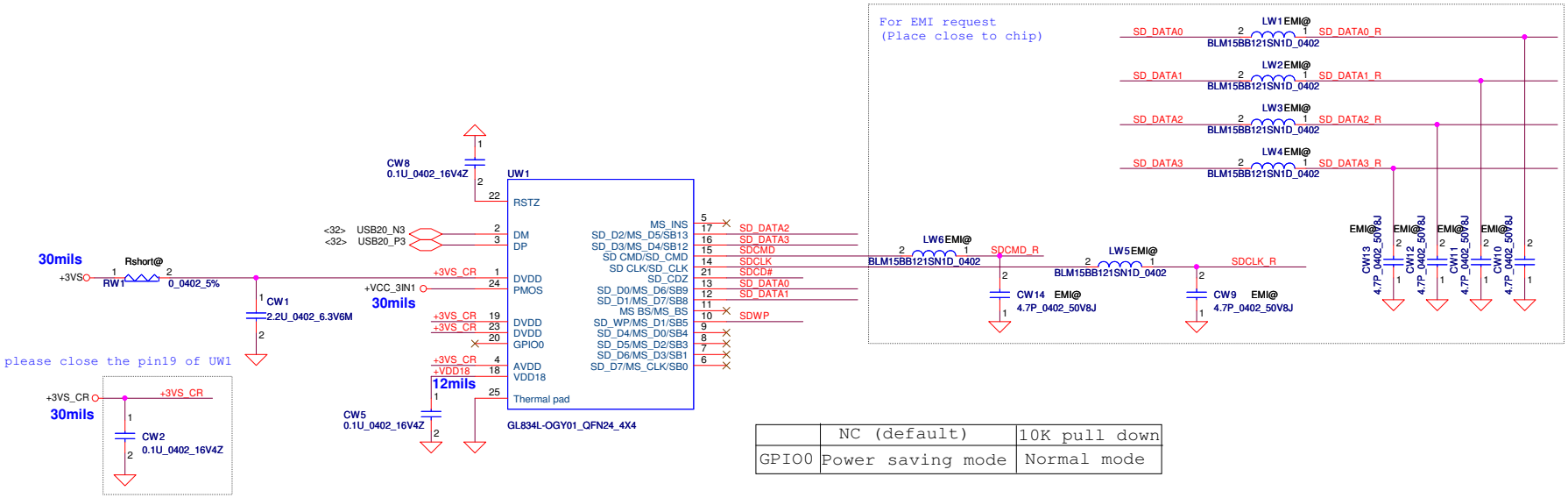
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E

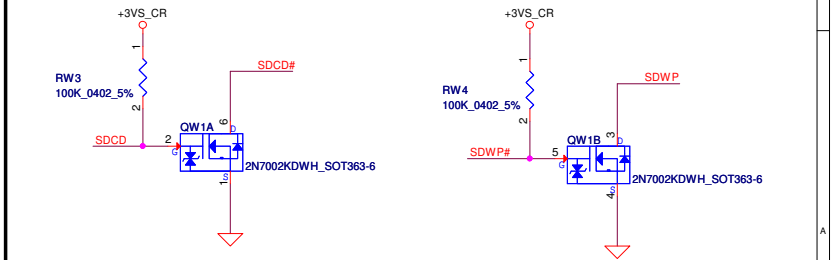
Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 39 of 57



	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

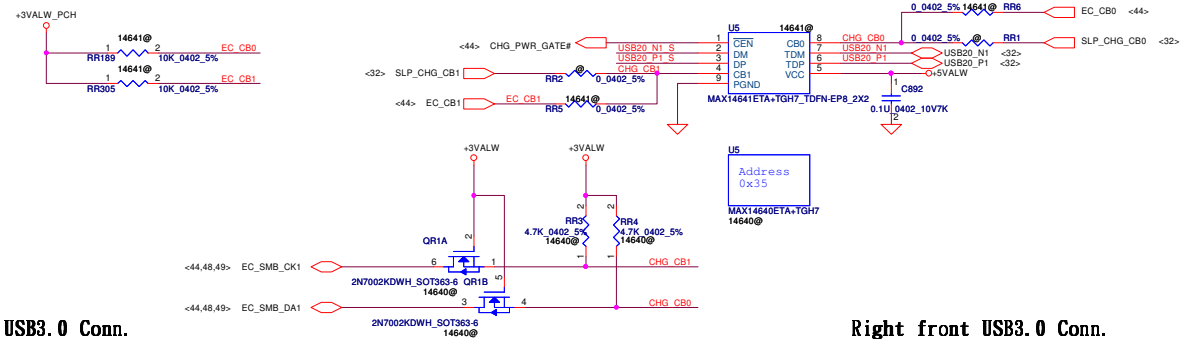
Title: USB-CardReader Genesys GL834L

Size	Document Number	Rev
Custom	VSKAA	1.0

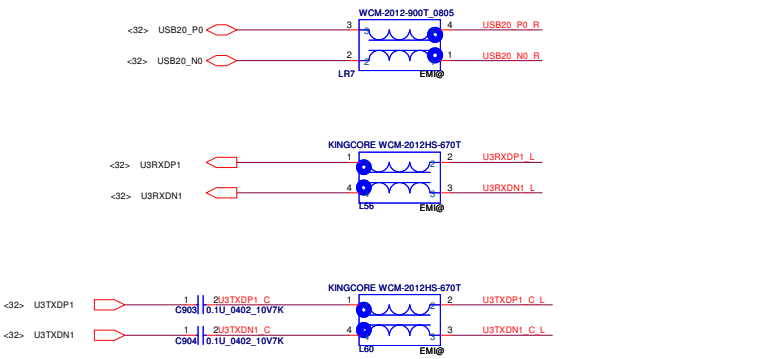
Date: Thursday, May 09, 2013 Sheet 40 of 57

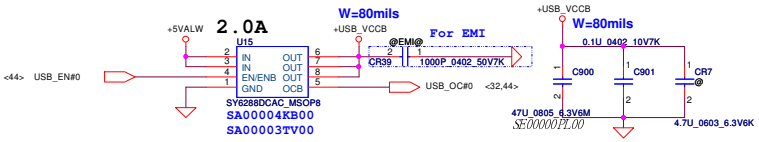
Right side USB 3.0 x 2/ Sleep&Charge

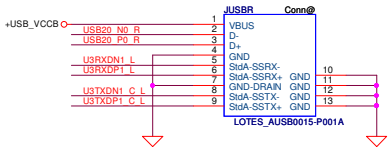
State table for MAX14641			
CB0	**CB1**	**Mode**	**STATUS**
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

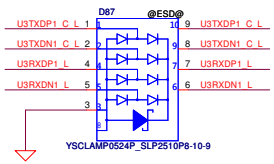


Right rear USB3.0 Conn.

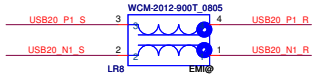


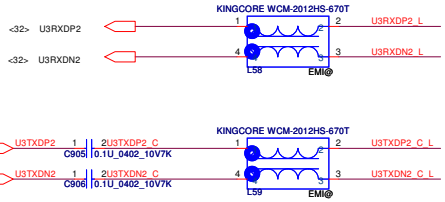


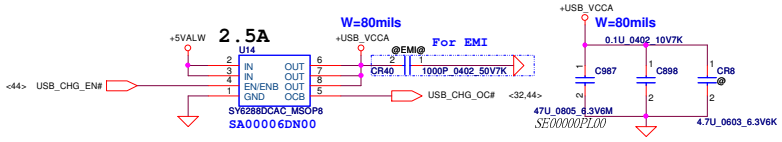


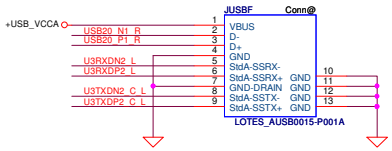


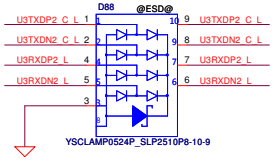
Right front USB3.0 Conn. (Support S&C function)











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Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title RUSB/S&C
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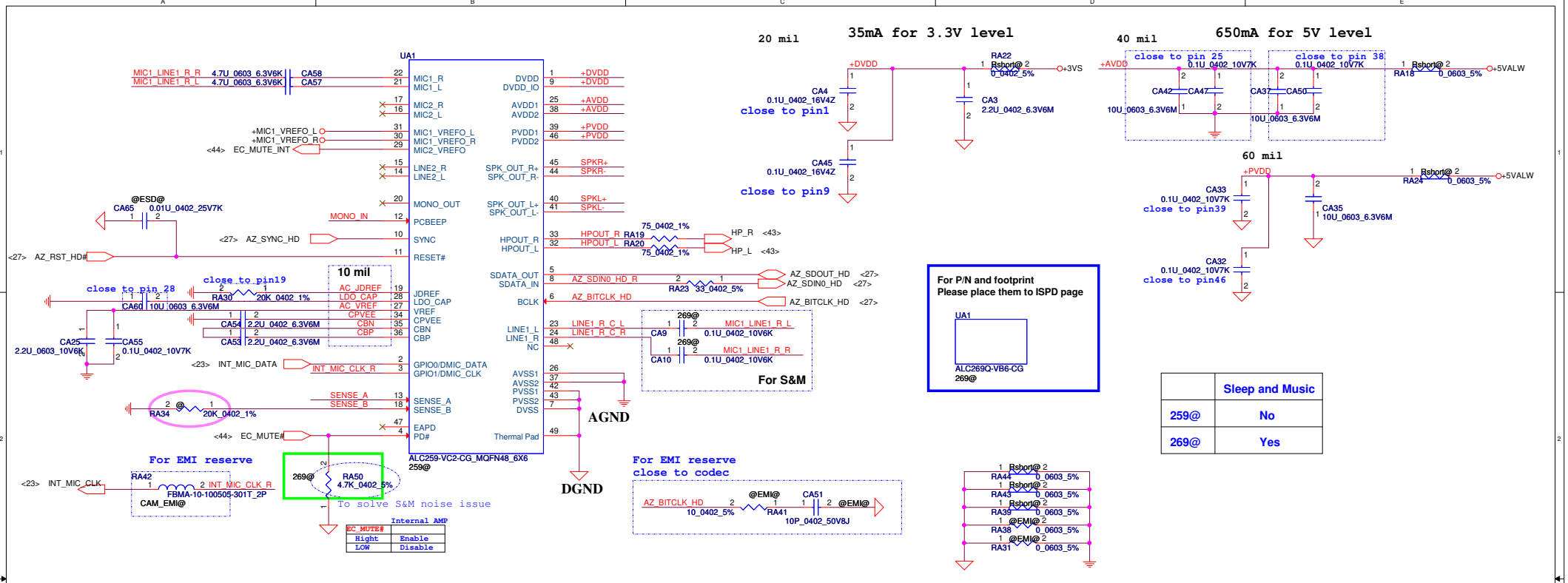
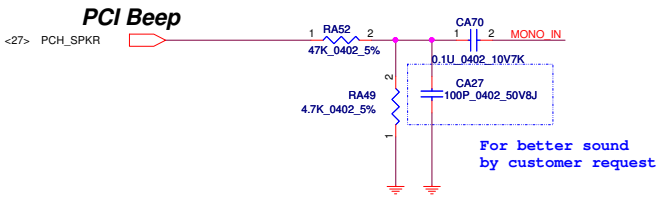
			Date: Thursday, May 09, 2013 / Sheet 41 of 57



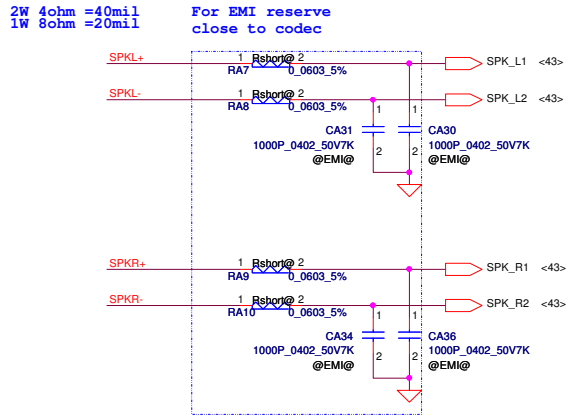
	Sleep and Music
259@	No
269@	Yes

Beep sound

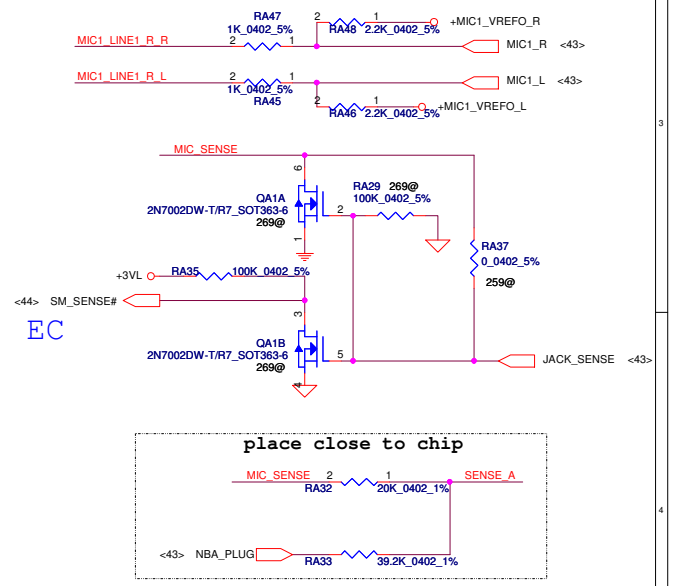


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

SPK



MIC/LINE IN



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Issued Date	2012/04/19	Deciphered Date	2015/04/19

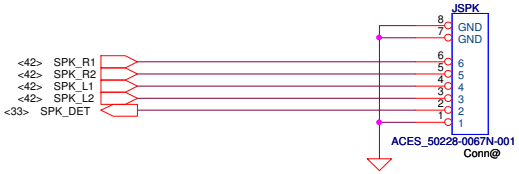
Compal Electronics, Inc.

Title: ***HDA-ALC259-VC***

Size	Document Number	Rev
Custom		

Date: Thursday, May 09, 2013 | Sheet 42 of 57

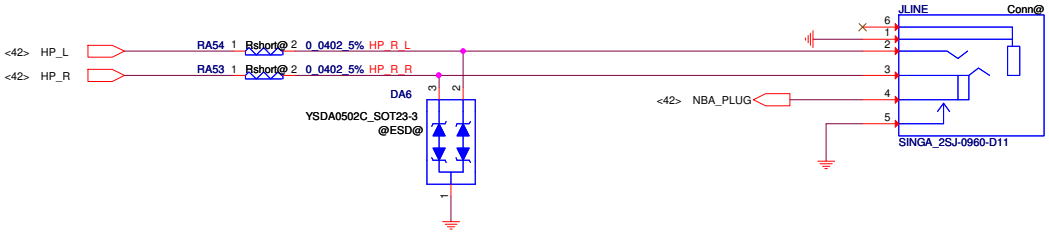
SPK Conn.



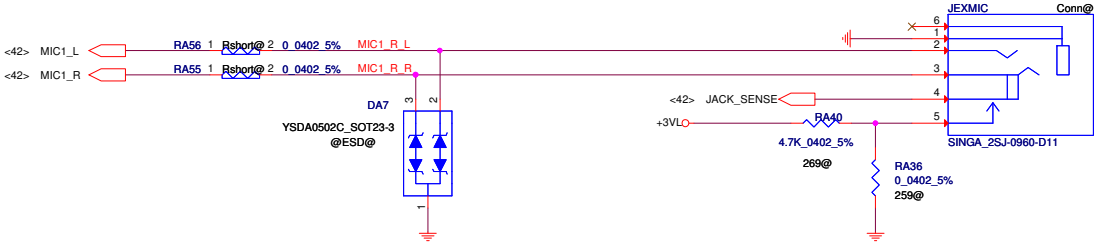
SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

HeadPhone/LINE Out JACK



MIC/LINE IN JACK



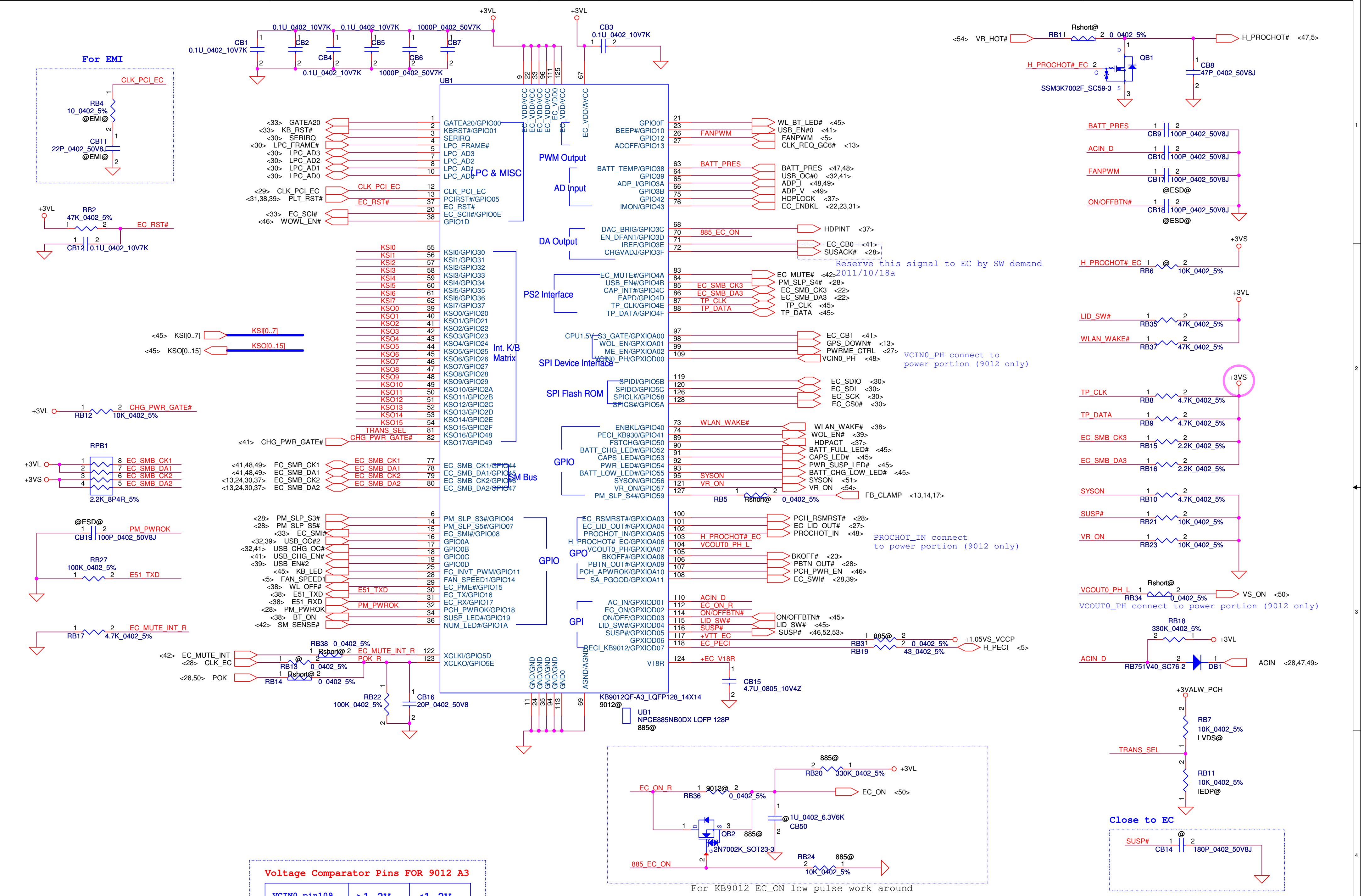
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: AUDIO CONN

Size: B | Document Number | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 43 of 57



Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109 VCIN1 pin102	>1.2V	<1.2V
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: LPC-EC-KB9012&930

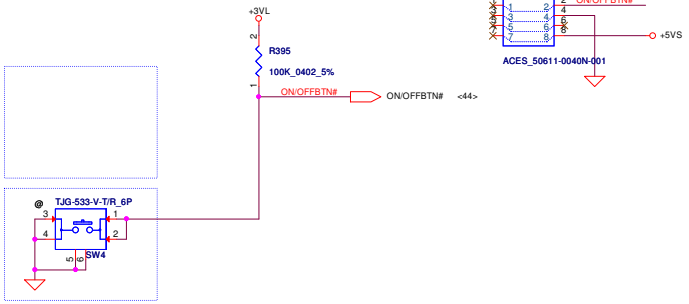
Size | Document Number | Rev 1.0

Date: Thursday, May 09, 2013 | Sheet 44 of 57

Power Button

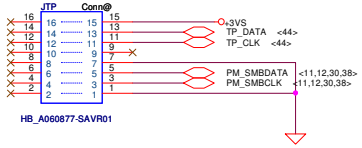
Place on TOP

Place on BOT

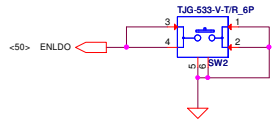


Conn.

Touchpad Connector

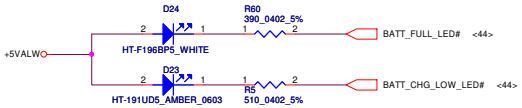


Battery Reset



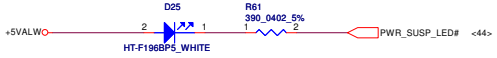
LED/LID

BATT CHARGE /FULL LED



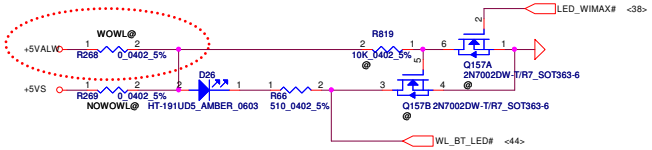
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED

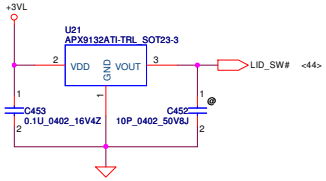


White LED bright when system is power on.
White LED blink when system is sleep mode.

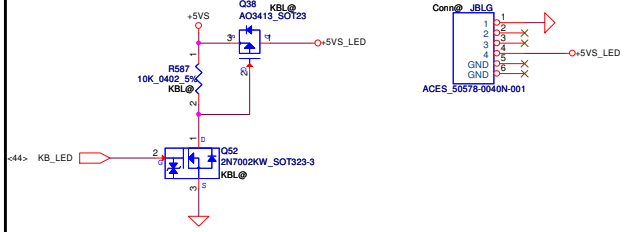
WLAN/WiMAX LED



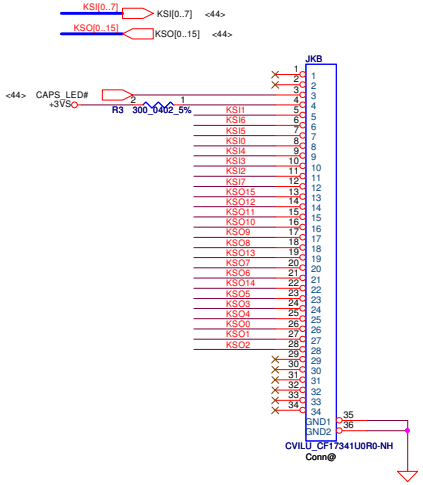
Amber LED bright while Wireless and/or WiMAX turns on.



Keyboard LED

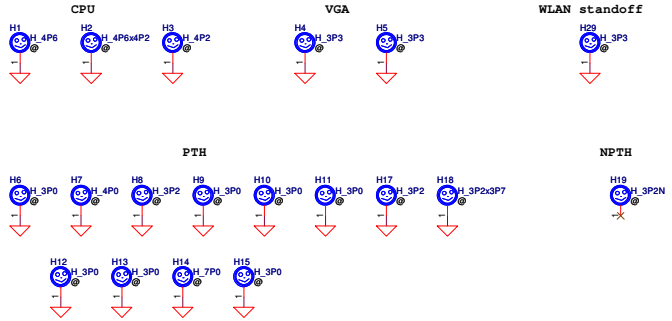


NEW KEYBOARD CONN.

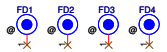


NFC

Screw Hole

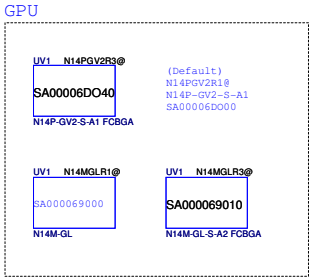


PCB Fedical Mark PAD



ISPD

GPU



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

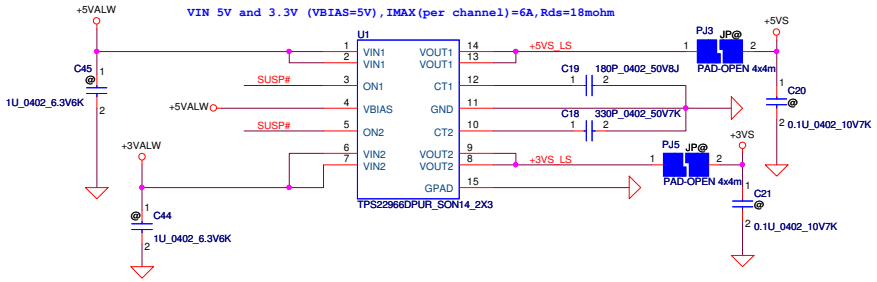
Compal Electronics, Inc.

Title: TP/ISPD/KB/Screw

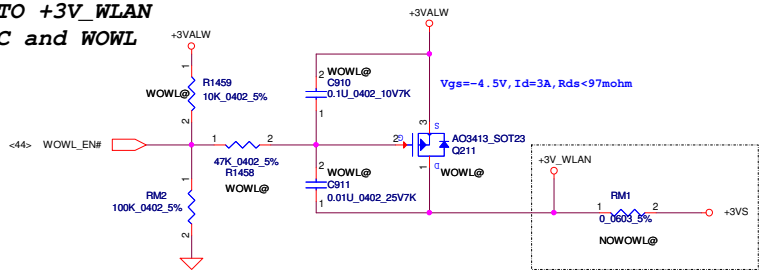
Size: | Document Number: VSKAA | Rev: 1.0

Date: Friday, May 10, 2013 | Sheet 45 of 57

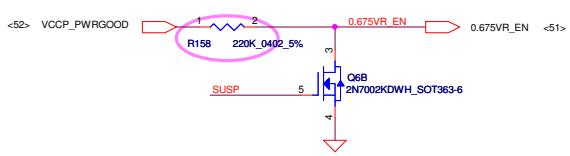
+3VALW TO +3VS
+5VALW TO +5VS
Load Switch

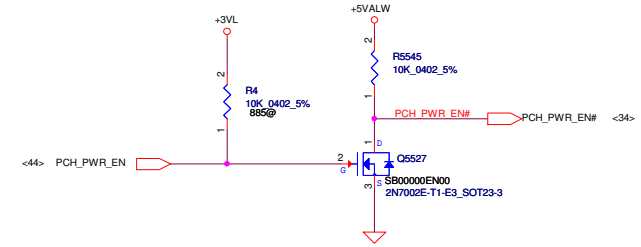


+3VALW TO +3V_WLAN
for AOAC and WOWL

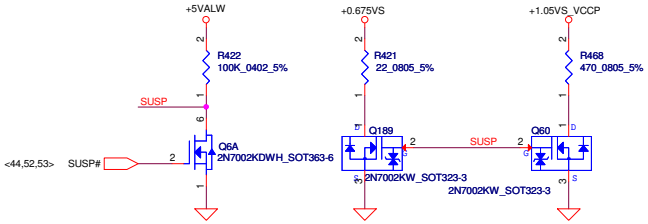


For S3 CPU Power Saving

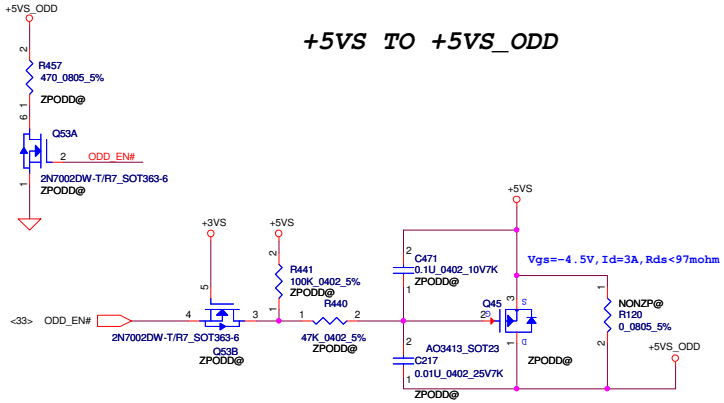




Reserve CAP to avoid Power Noise



+5VS TO +5VS_ODD



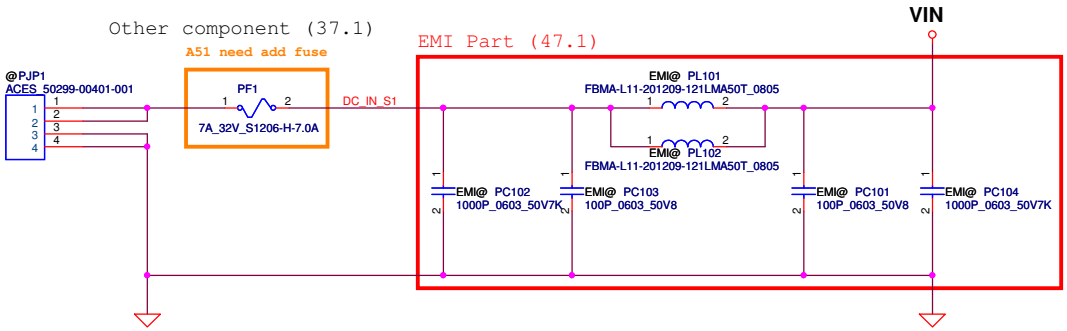
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

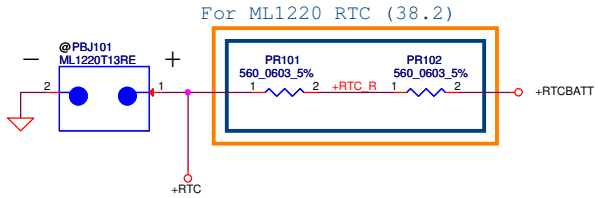
Compal Electronics, Inc.

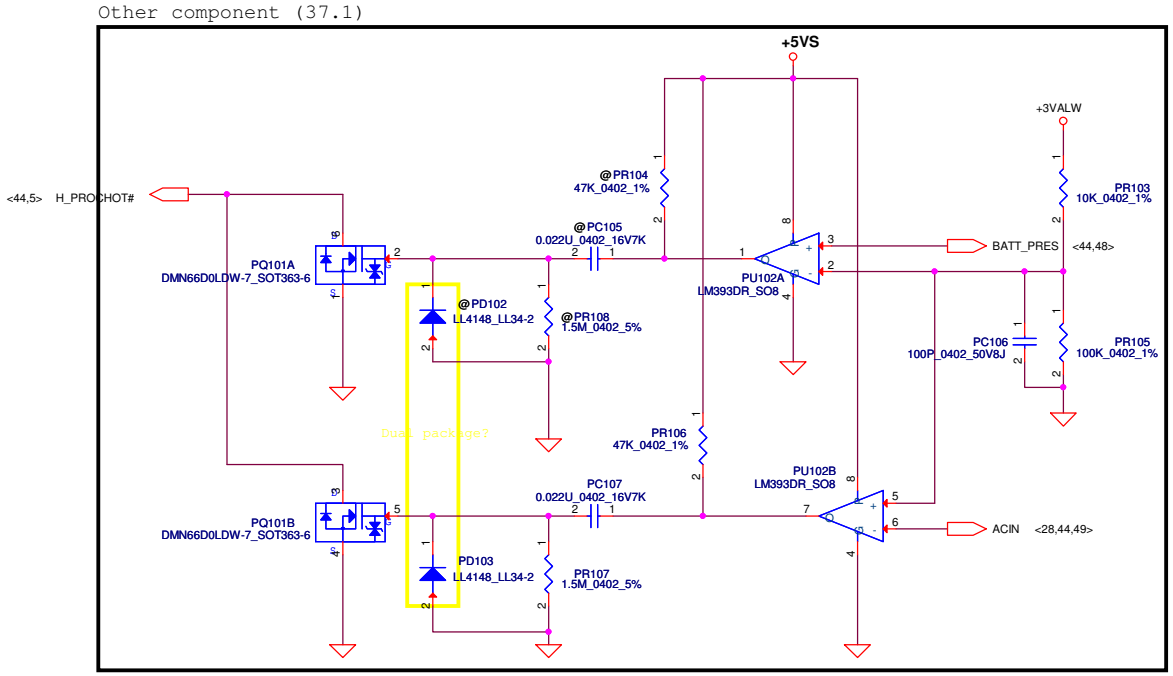
Title: DC-DC INTERFACE

Size | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 46 of 57







Remark :
Check Adapter/Battery surge load when Iccmax.

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

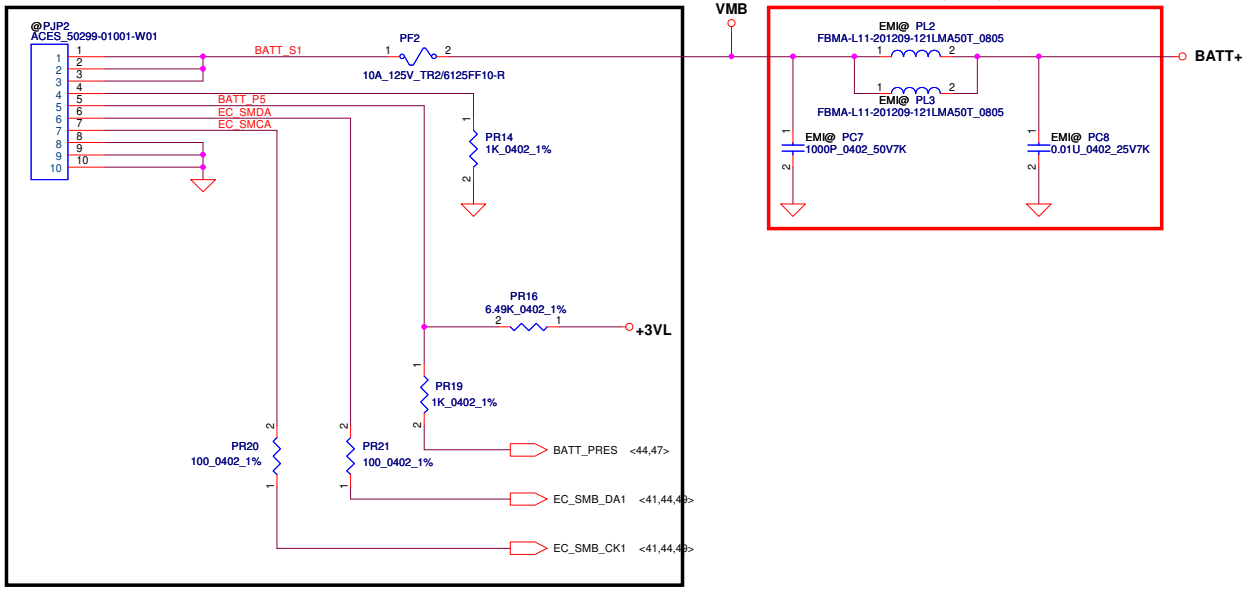
Compal Electronics, Inc.

Title: *DCIN/Surge load protect*

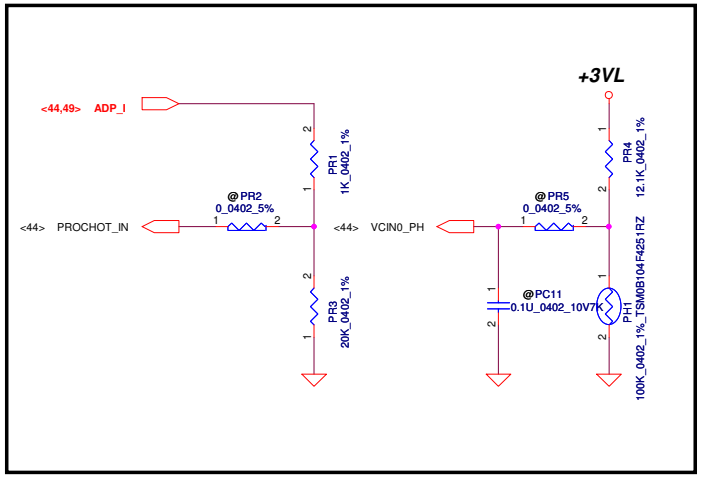
Size: Custom | Document Number: *VSKAA* | Rev: 1.0

Date: | Sheet 47 of 57

Other component (37.1)



OTP (39.7)



	Initial	Recovery
75W N14M-GL	0.90V	0.72V
90W N14P-GV2	1.05V	0.90V

	Initial	Recovery
CPU OTP	90 C	70 C

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

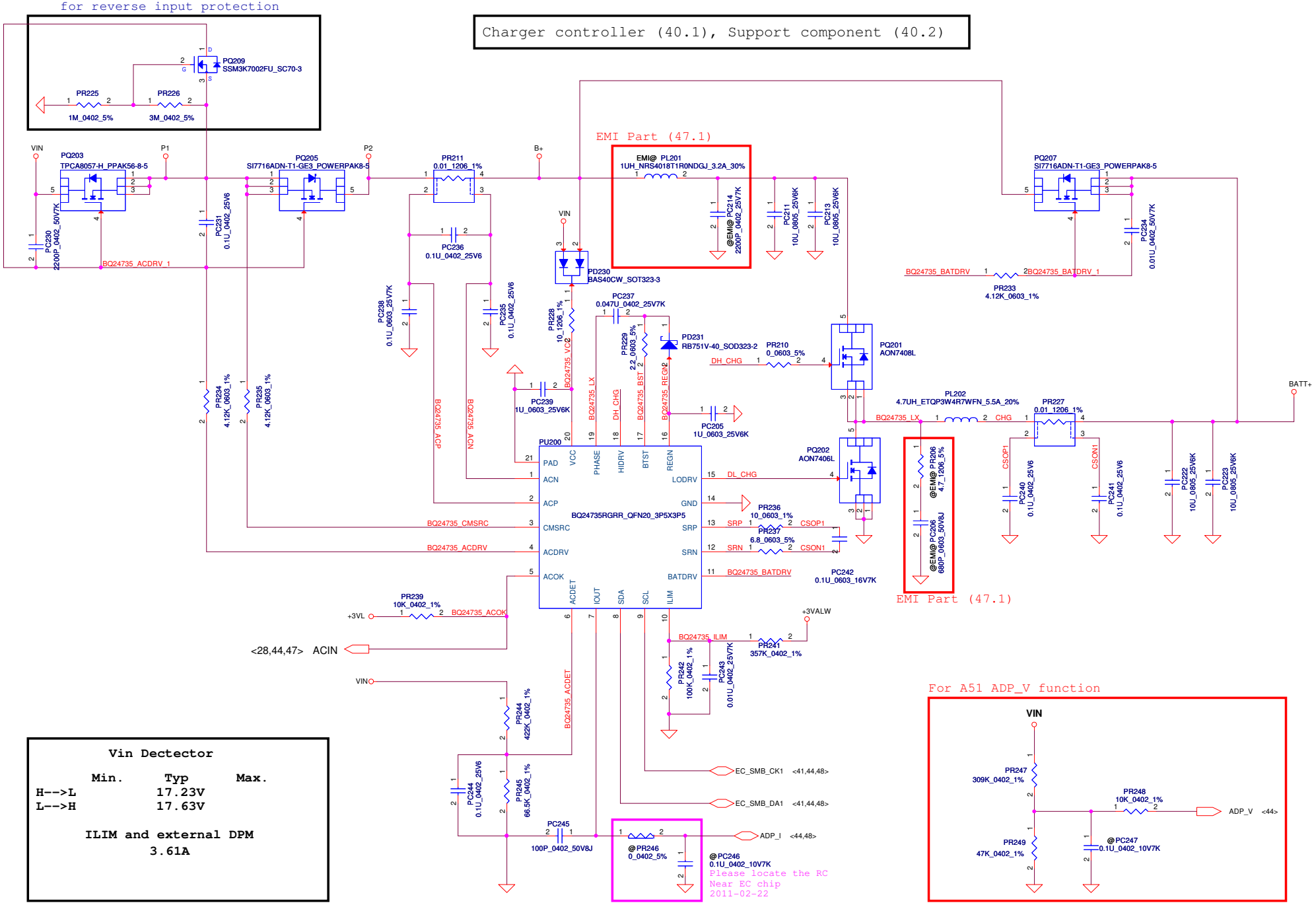
Title: BATTERY CONN / OTP

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: | Sheet 48 of 57

for reverse input protection

Charger controller (40.1), Support component (40.2)



For A51 ADP_V function

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.61A

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: VSKAA | Rev: 1.0

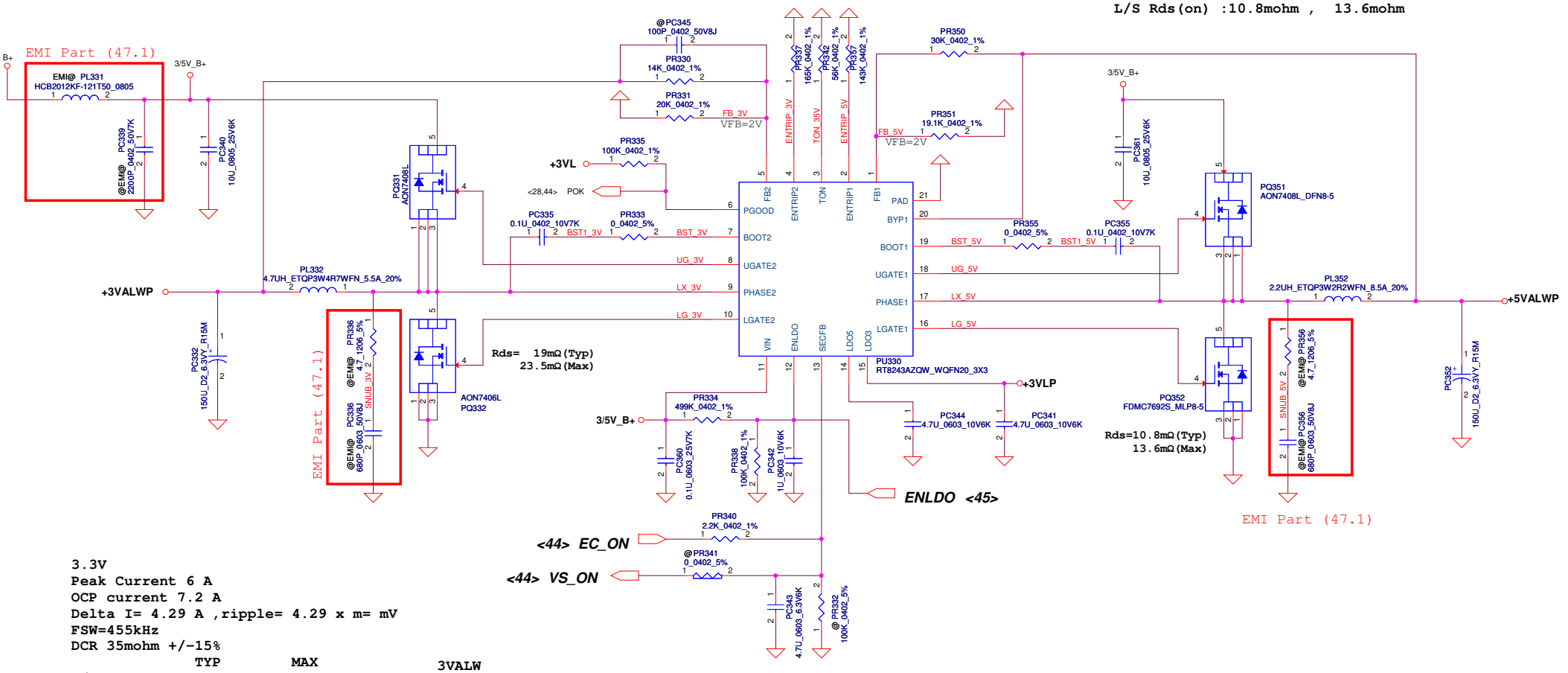
Date: | Sheet 49 of 57

3/5VALW controller (35.1), Support component (35.2)

5VALW
Ipeak : 12.5 A
Imax : 8.75 A
Iocp : 15 A
FSW : 390 kHz

5V
Peak Current 10 A
OCP current 12 A
FSW=390kHz
Delta I= 1.28 A,ripple V = 1.28 * 25 m= 32 mV
DCR 13.2mohm +/-5%

	TYP	MAX
H/S Rds(on)	27mohm	34mohm
L/S Rds(on)	10.8mohm	13.6mohm



3.3V
Peak Current 6 A
OCP current 7.2 A
Delta I= 4.29 A ,ripple= 4.29 x m= mV
FSW=455kHz
DCR 35mohm +/-15%

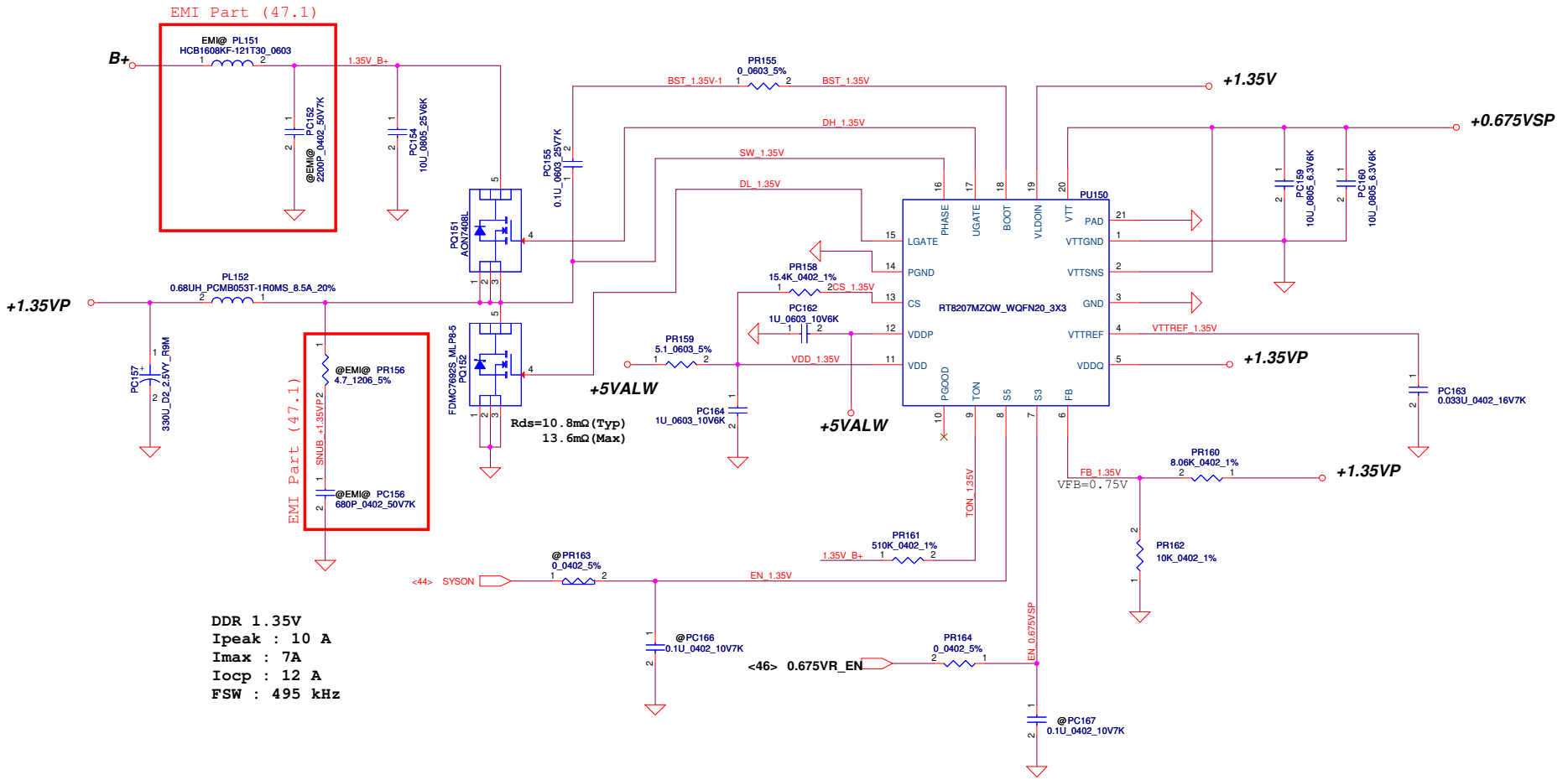
	TYP	MAX
H/S Rds(on)	27mohm	34mohm
L/S Rds(on)	19mohm	23.5mohm

3VALW
Ipeak : 8 A
Imax : 5.6 A
Iocp : 9.6 A
FSW : 455 kHz

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

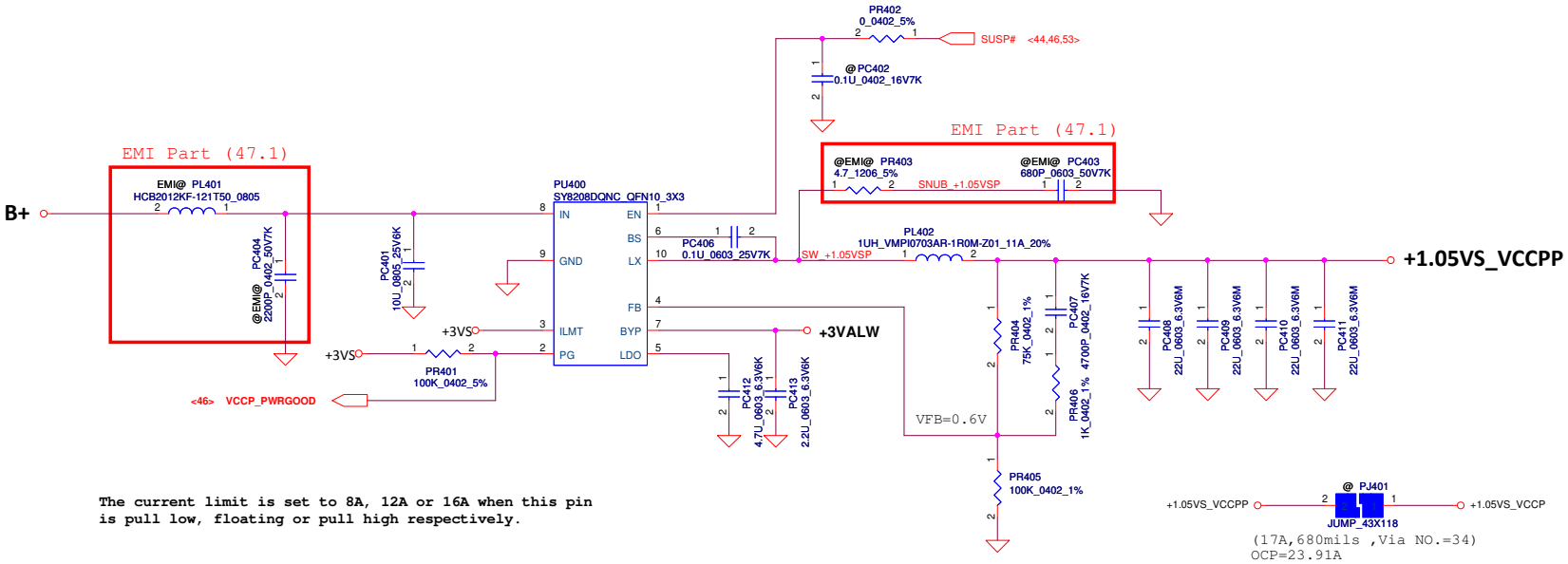
Compal Electronics, Inc.	
Title	3VALW/5VALW
Size: Custom	Document Number: VSKAA
Rev	1.0
Date:	Sheet 50 of 57

DDR controller (35.3), Support component (35.4)



Compal Electronics, Inc.	
Title	1.35VP/0.675VSP
Size: Custom	Document Number: VSKAA
Rev: 1.0	
Date:	Sheet 51 of 57

1.05VCCP controller (35.5), Support component (35.6)



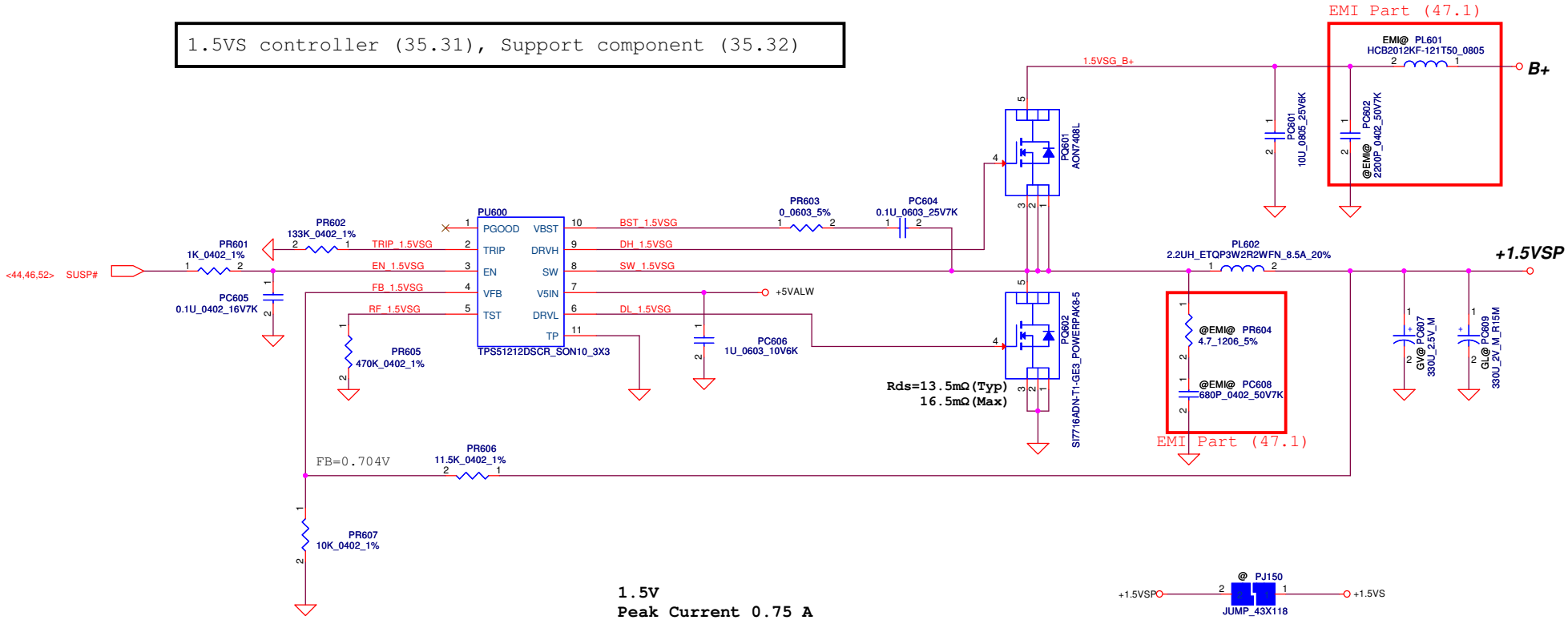
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

1.05V
Peak Current 11.35 A
OCP current 16 A
FSW=800kHz
Delta I= 1.24 A,Rippe= x m= mV
DCR 8.3~10 mohm

	TYP	MAX
H/S Rds(on)	:22 mohm ,	mohm
L/S Rds(on)	:11 mohm ,	mohm

Compal Electronics, Inc.			
Title	+1.05VS_VCCP		
Size: Custom	Document Number: VSKAA		Rev: 1.0
Date:	Sheet 52 of 57		

1.5VS controller (35.31), Support component (35.32)



1.5V
Peak Current 0.75 A
OCP current 0.95 A
FSW= 290 kHz
Delta I= A,Rippe= x m= mV
DCR 8.3~10 mohm

	TYP	MAX
H/S Rds(on) :	27 mohm ,	34 mohm
L/S Rds(on) :	13.5 mohm ,	16.5 mohm

(15A, 600mils ,Via NO.= 30)
OCP=18A

TPS51212 for DIS SKU
APL5930 for UMA SKU
Confirm with HW for sequence control

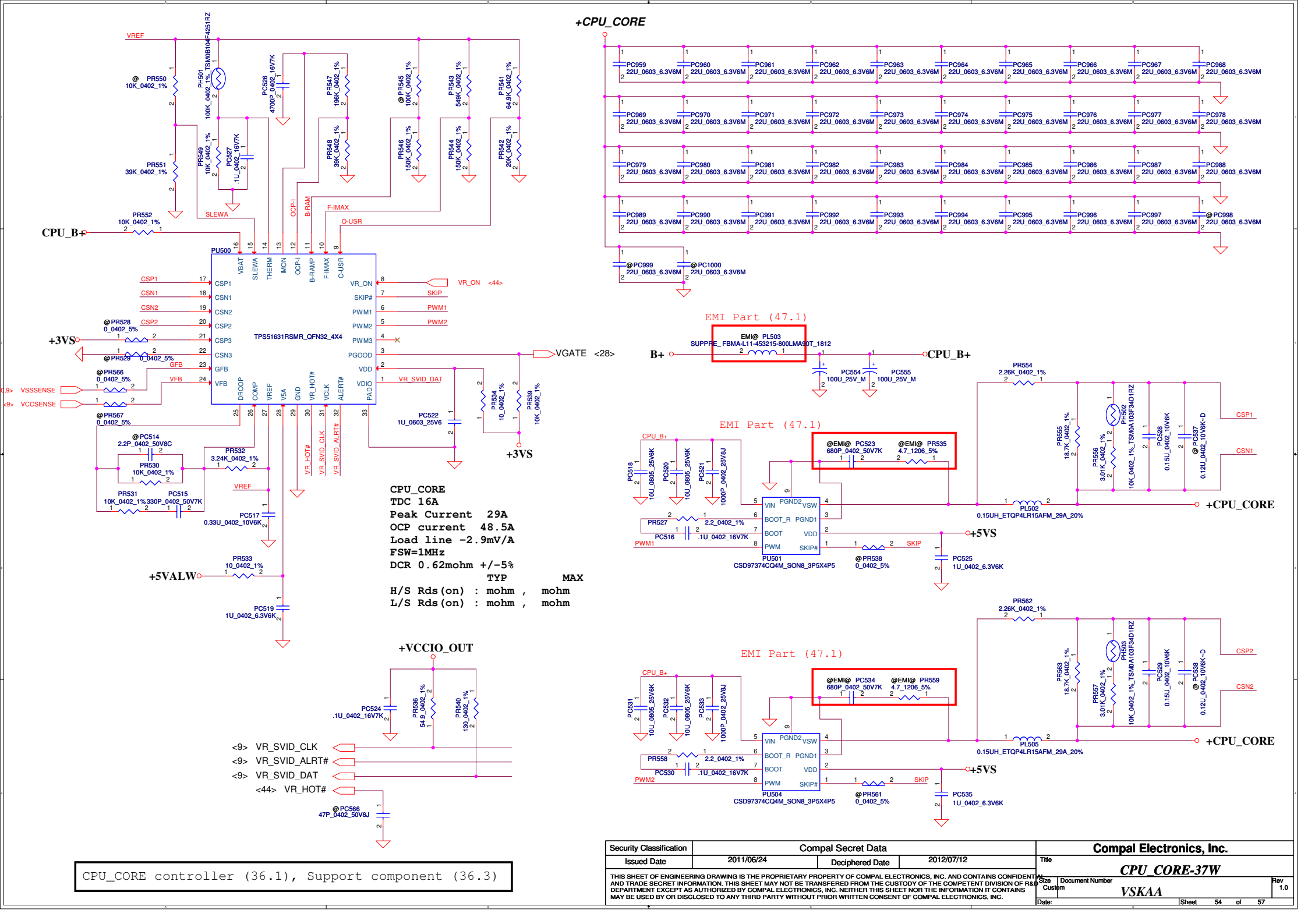
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: +1.5VS

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: Thursday, May 09, 2013 | Sheet 53 of 57



CPU_CORE controller (36.1), Support component (36.3)

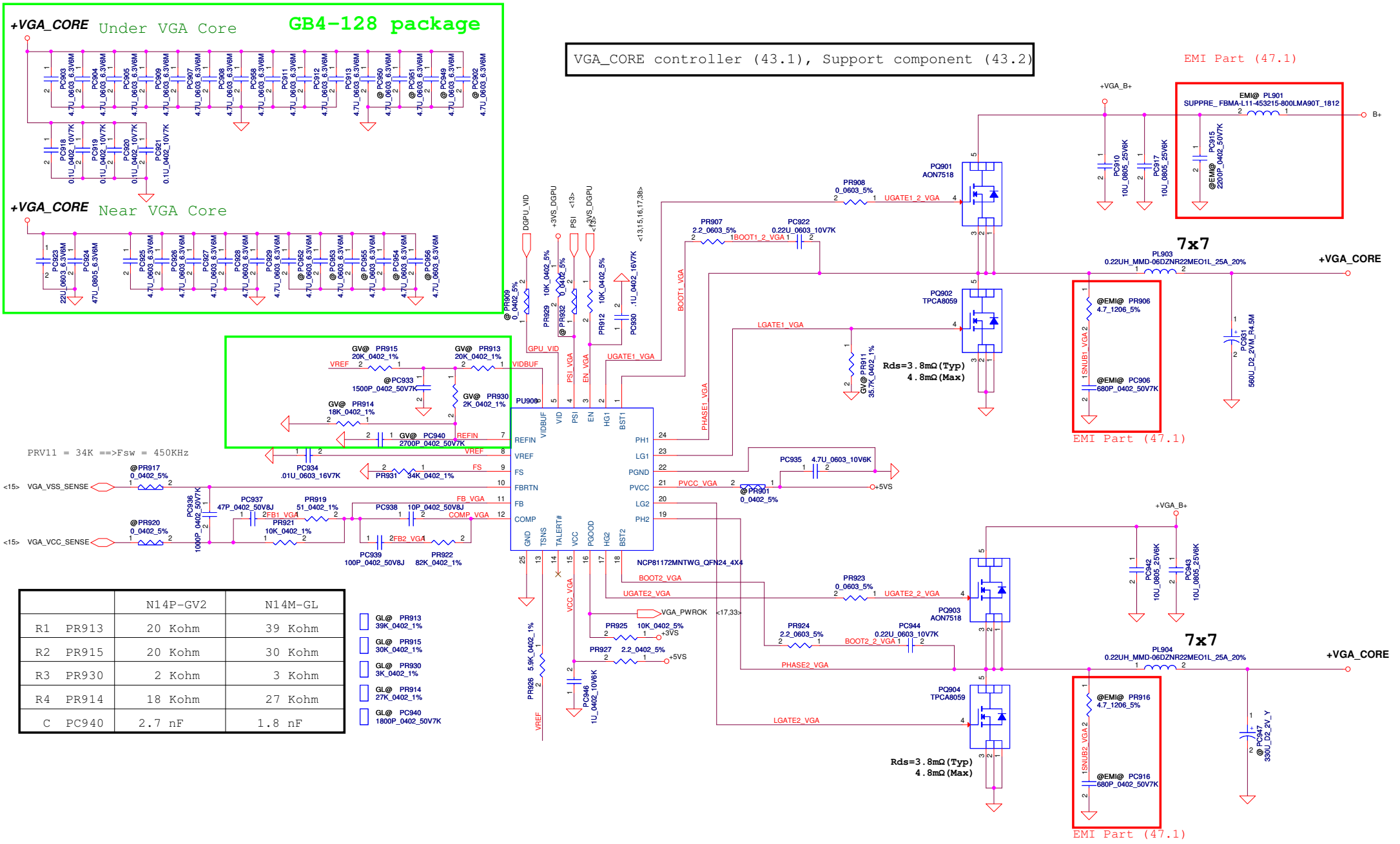
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: *CPU_CORE-37W*

Size: Custom | Document Number: *VSKAA* | Rev: 1.0

Date: | Sheet 54 of 57



	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

GL@ PR913 39K_0402_1%
GL@ PR915 30K_0402_1%
GL@ PR930 3K_0402_1%
GL@ PR914 27K_0402_1%
GL@ PC940 1800P_0402_50V7K

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom | Document Number: VSKAA | Rev: 1.0

Date: | Sheet 55 of 57

PWR PIR (Product Improve Record)

VSKAA LA-9866P Schematic Change List

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)
1	EVT--2012/10/24	P48-PWR-BATTERY CONN/OTP	@PD5 / Remove ESD diode	COMPANY	For part count reducation
2	EVT--2012/10/24	P48-PWR-BATTERY CONN/OTP	@PD6 / Remove ESD diode	COMPANY	For part count reducation
3	EVT--2012/10/24	P49-PWR-CHARGER	@PC221 / Remove 10uF capacitor	COMPANY	For part count reducation
4	EVT--2012/10/24	P50-PWR-3VALW/5VALW	PC331,@PC332 / PC331 Reserve & PC332 Mount	ME	ME limitation
5	EVT--2012/10/24	P51-PWR-1.35VP/0.675VSP	@PJ675 / JUMP_43x79 change to JUMP_43x39	PWR	For design change
6	EVT--2012/10/24	P51-PWR-1.35VP/0.675VSP	@PJ1352 / Remove	PWR	For design change
7	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	PR541 / 475K change to 169K	PWR	For TPS51631 under-shoot setting
8	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	@PR553 / Remove (PWM3 floating)	COMPANY	For part count reducation
9	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	@PC537 / Add 0402 Cap footprint	PWR	For TPS51631 thermal setting
10	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	@PC538 / Add 0402 Cap footprint	PWR	For TPS51631 thermal setting
11	EVT--2012/10/24	P55-PWR-GPU_CORE	PR929 / Add 10K resistor	HW	Pull high PSI port
12	EVT--2012/10/24	P55-PWR-GPU_CORE	PR913 / 39K change to 20K(GV@)	PWR	For N14 PWM VID setting
13	EVT--2012/10/24	P55-PWR-GPU_CORE	PR915 / 39K change to 20K(GV@), 30K(GL@)	PWR	For N14 PWM VID setting
14	EVT--2012/10/24	P55-PWR-GPU_CORE	PR930 / 1.5K change to 2K(GV@), 3K(GL@)	PWR	For N14 PWM VID setting
15	EVT--2012/10/24	P55-PWR-GPU_CORE	PR914 / 30K change to 18K(GV@), 24K(GL@)	PWR	For N14 PWM VID setting
16	EVT--2012/10/24	P55-PWR-GPU_CORE	PR904 / 1.5K change to 0(GV@), 3K(GL@)	PWR	For N14 PWM VID setting
17	EVT--2012/10/24	P55-PWR-GPU_CORE	PC940 / Add 2.7nF(GV@), 1.8nF(GL@)	PWR	For N14 PWM VID setting
18	EVT--2012/10/24	P55-PWR-GPU_CORE	PC933 / Reserve	PWR	For N14 PWM VID setting
19	EVT--2012/10/24	P50-PWR-3VALW/5VALW	PR337 / 235K change to 165K	PWR	For RT8243 3V OCP setting
20	EVT--2012/10/24	P50-PWR-3VALW/5VALW	PR357 / 156K change to 143K	PWR	For RT8243 5V OCP setting
21	EVT--2012/10/24	P51-PWR-1.35VP/0.675VSP	PR158 / 16.2K change to 15.4K	PWR	For RT8208 1.35V OCP setting
22	EVT--2012/10/24	P55-PWR-GPU_CORE	PR931 / 71.5K change to 34K	PWR	For NCP81172 Fsw setting
23	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	PC521 / Add 1000P_0402 Capacitor	PWR	For design change
24	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	PC533 / Add 1000P_0402 Capacitor	PWR	For design change
25	EVT--2012/10/24	P55-PWR-GPU_CORE	PR927 / change resistor PN	PWR	For PN setting error
26	DVT--2012/12/07	P48-PWR-BATTERY CONN/OTP	PF2 / change component for cost down	COMPANY	For cost down
27	DVT--2012/12/07	P49-PWR-CHARGER	PQ203 / AON6504 Change to TPCA8057	PWR	For design issue
28	DVT--2012/12/07	P50-PWR-3VALW/5VALW	PC351, PC352 / Remove OSCON mount polymer CAP	ME	ME limitation
29	DVT--2012/12/07	P50-PWR-3VALW/5VALW	PR409 / Add 100K	PWR	Pull high for PGOOD port
30	DVT--2012/12/07	P50-PWR-3VALW/5VALW	PC341, PC344 / Add 4.7U for LDO5 & Change PC341 size to 0603	PWR	for IC default setting
31	DVT--2012/12/07	P51-PWR-1.35VP/0.675VSP	PL152 / Change choke value	PWR	Common design change
32	DVT--2012/12/07	P52-1.05VS_VCCP	PL401 / Change bead	PWR	Common design change
33	DVT--2012/12/07	P52-1.05VS_VCCP	PR403, PC403 / Reserve PR403 & PC403		
34	DVT--2012/12/07	P54-PWR-CPU_CORE-37W	PL502, PL505 / Change choke value	PWR	Common design change
35	DVT--2012/12/07	P54-PWR-CPU_CORE-37W	PC528, PC529, PC537, PC538 / Add 0402 Cap footprint	PWR	Common design change
36	DVT--2012/12/07	P55-PWR-GPU_CORE	PC993, PC994, PC995, PC996, PC997, PC1101, PC1103 / Add MLCC PC993~PC997, remove polymer PC1101, PC1103	PWR	For HF design
37	DVT--2012/12/07	P55-PWR-GPU_CORE	PC934 /	PWR	Common design change
38	DVT--2012/12/07	P55-PWR-GPU_CORE	PL903, PL904 / Change vendor	PWR	Change for losing
39	DVT--2012/12/07	P55-PWR-GPU_CORE	PR912 / Change short pad to 10K	PWR	Pull high for EN port
40	DVT--2012/12/07	P52-1.05VS_VCCP	PC407 /	PWR	Common design change
41	PVT--2013/02/25	P54-PWR-CPU_CORE-37W	PR541 change from 169K to 64.9K PR542 change from 150K to 20K PR547 change from 174K to 196K PC514 reserve PR532 change from 3.16K to 3.24K PR554,PR562 change from 2.37K to 2.26K PR555,PR563 change from 17.8K to 18.7K	PWR	for IC TPS51631 edition change from ES1.1 to ES2.1 fine tune
42	PVT--2013/03/04	P55-PWR-VGA_CORE	PR904,PR918,PR928,PC945 remove PR914 change from 24K to 27K	PWR	Remove and change for Richtek solution setting
43	PVT--2013/03/04	P52-1.05VS_VCCP	PR406 add 1K PC407 change from 330p to 4700p	PWR	Common design change
44	PVT-2013/03/21	P55-PWR-VGA_CORE	PR911 mount	PWR	Mount for GV2 setting
45	PVT-2013/03/21	P55-PWR-VGA_CORE	PC947 reserve	PWR	For part count reducation
46	PVT-2013/03/21	P53-PWR-1.5VS	PR602 change to 133K	PWR	adjust current limit value
47	PVT-2013/03/21	P52-PWR-1.05VS_VCCP	add PR406	PWR	circuit protection function
48	PVT-2013/03/21	P51-PWR-1.35VP/0.675VSP	change PL152 part number	PWR	for design change

Compal Electronics, Inc.			
Title: DC-DC INTERFACE			
Size: Custom	Document Number		Rev: 1.0
Date: Thursday, May 09, 2013	Sheet 56 of 57		

HW PIR (Product Improve Record)

VSKAA LA-9866P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/12/05

NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
Item	Date	Page	Action	Component	Request
1)	11/19	24	Delete	R23,R24,R25,R26	HDMI Redriver SMBus connect to EC directly
2)	11/19	31	Change Config	RH17 to LVDS@	
3)	11/19	31	Change Config	RH18 to IEDP@	
4)	11/19	44	Change	RB36 from 2.2K to 0 ohm	Change EC_ON workround to power side
5)	11/19	44	Change Config	CB50 to @	
6)	11/19	42	Change Config	CA32 to always mount	
7)	11/19	30	Change	PCH_SPICS1# to UH3, PCH_SPICS0# to UH4	For Shark Bay ME code location
8)	11/19	44	Change	EC pin128 from EC_CS0# to EC_CS1#	For SW request
9)	11/22	33	Change	PCH_GPIO69 to PROJECT_ID	For SW request
10)	11/22	33	Change	PCH_GPIO22 to VRAM_DR_SR#	For VBIOS setting of DRANK or SRANK
11)	11/23	26	Change Config	C238~C243 to CRT@EMI@	
12)	11/23	23	Add	D92	For isolate the +3VL power rail form LID_SW#
13)	11/28	41	Change	Change C987,C900 from 1206 to 0805	To avoid MLCC from cracking
14)	11/29	23	Change	Change JLVDS.4 from LID_SW# to BK_OFF#	Common design change
15)	11/29	43	Change	Change JSPK from 8 pins to 6 pins	Common design change
16)	11/29	33	Change	Delete SPK_DET1 and change SPK_DET0 netname to SPK_DET	SPK detection method was changed
17)	11/29	42	Change	Change RA50 to 269@	Used for avoiding from S&M noise issue
18)	11/29	12	Change	Change CD31 from 1206 to 0805	To avoid MLCC from cracking
19)	11/29	24	Change	Stuff 8401@ as default add reserve R168,R169	For the purpose of HDMI 4K2K jetter cleaner
20)	11/29	40	Add	Add QW1,RW3,RW4 to have inversion circuit	For normal close connector type
21)	11/29	45	Add	Add H19, change H7 to H_4P0,change H4,H5 to H_3P3	ME's requirement
22)	12/02	26	Add	Add R62 R63 22ohm	For CRT undershoot issue
23)	12/02	44	Change	Change PM_SLP_S4# from pin127 to pin84	For EC fix code design
24)	12/02	44	Change	Change USB_EN#0 from pin84 to pin23	For EC fix code design
25)	12/02	44	Change	Change FB_CLAMP from pin23 to pin127	For EC fix code design
26)	12/03	05	Add	Add CC63,CC68,CC69,CC83 100P	For ESD
27)	12/03	31	Change	Change CH104 to 0.1U	For ESD
28)	12/03	10	Change	Change CC53 to 47U	For cost down
29)	12/03	41	Add	Add QR1,RR1,RR2,RR3,RR4	For colay 14640 Charge IC
========== PVT Modify Items ==========					
1)	02/03	05	Del	Del C6 (1000P on +FAN1)	
2)	02/03	11	Change	Change RC78 to 1K	For SM_DRAMRST# rising smoothly
3)	02/03	11	Del	Del CD15,CD2,CD22,CD23,CD12	For cost down
4)	02/03	12	Del	Del CD28,CD46,CD43,CD44,CD38	For cost down
5)	02/03	12	Change	RC109,RC110,RC111,RC120,RC121,RC122 from 0.5% to 1%	For cost down
6)	02/03	12	Reserve	CC65,CC71,CC72,RC3,RC8,RC9	For common design
7)	02/03	17	Del	CV58	For part coumt
8)	02/03	25	Del	C264	For part coumt
9)	02/03	25	Change	U16 to SA00006H000	For common design
10)	03/08	23	Reserve	D89	For ESD request
11)	03/15	44	Reserve	CB17, CB18, CB19	For ESD request
12)	03/15	05	Reserve	CC2,CC3	For ESD request
13)	03/15	33	Reserve	CH7	For ESD request
14)	03/15	23	Add	D2, D3 on INT_MIC_DATA & INT_MIC_CLK	For ESD request
15)	03/15	40	Add	CW10~CW14, LW1~LW6	For solving EMI test fail
16)	03/15	23	Reserve	R104, R105	For colay EMI common mode choke
17)	03/15	26	Change	R138 to 150ohm array chip resistor	For part count reduce
18)	03/15	45	Add	R268,R269	For WOWL LED behavior requested by customer
19)	03/15	42	Change	RA42 from 0 ohm to bead	For EMI request
20)	03/15	44	Add	RB17, RB38	For solving bobo noise
21)	03/15	44	Add	RB14 & link EC pin 123 to POK	For power request
22)	03/15	11	Change	RC78 from o ohm to 1K	For making SM_DRAMRST# rising more better
23)	03/15	31	Add	RH127, RH128	For HDMI_HPD no use port to default pull down
24)	03/15	35	Change	RH14 to short pad & reserve RH15 to ohm	For change +VCCCFUSE to +1.05VS_PCH
25)	03/15	31	Change	RH155 to 150ohm array chip resistor	For part count reduce
26)	03/15	25	Change	U16 from AP2330 to AP2151	For common design
27)	03/15	30	Change	4M+2M solution to 8M only solution	For common design
28)	03/15	25	Del	C264	For part count reduce
29)	03/15	17	Del	CV58	For part count reduce
30)	03/15	22	Del	LT3	For no colay RTD2132S
31)	03/15	23	Del	R81, R82	For no colay RTD2132S
32)	03/15	40	Change	CW9 from 10P to 4.7P	For vendor recommendation
33)	03/15	45	Del	SW3	For ME limitation