

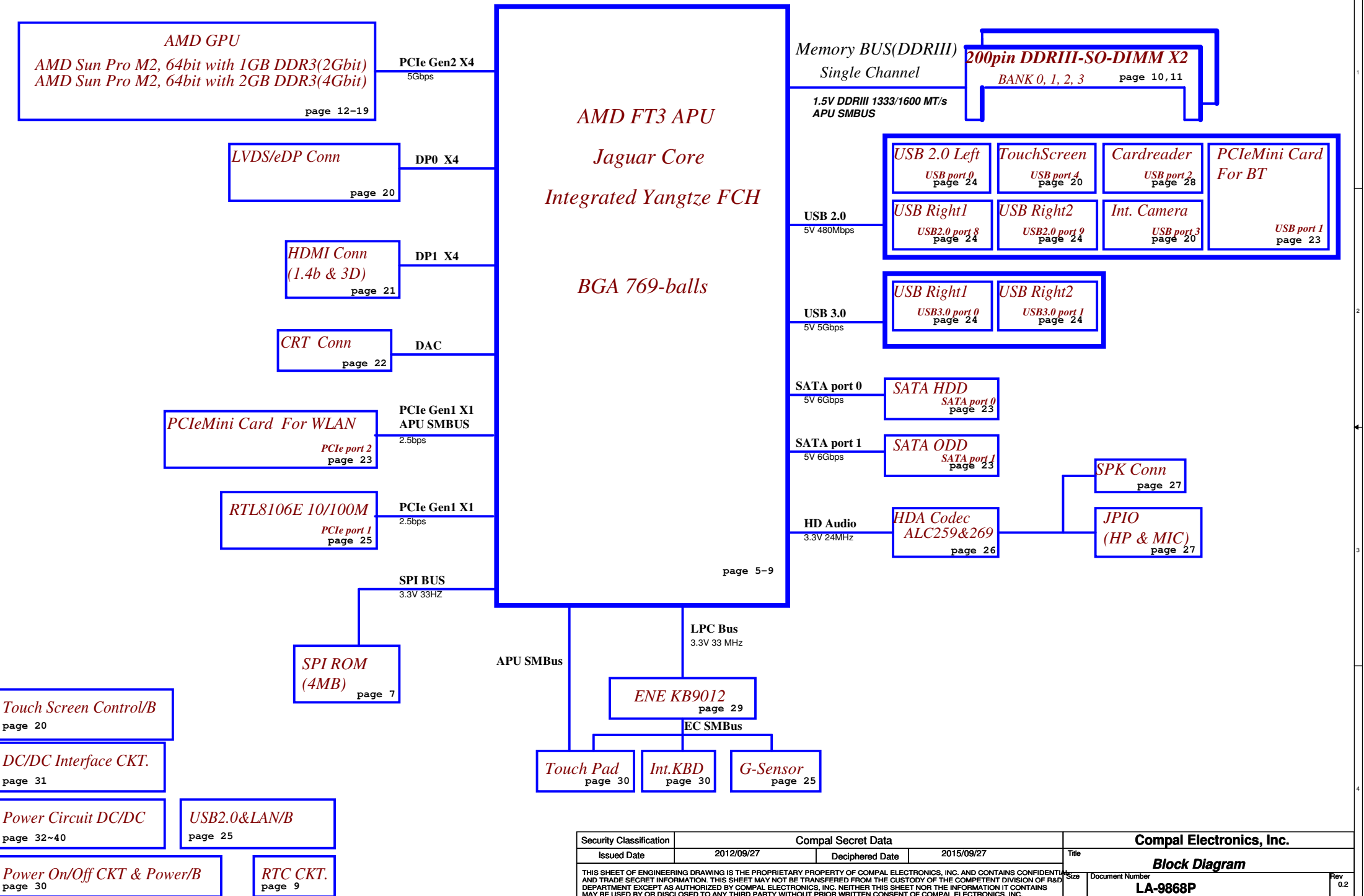
VNKAE

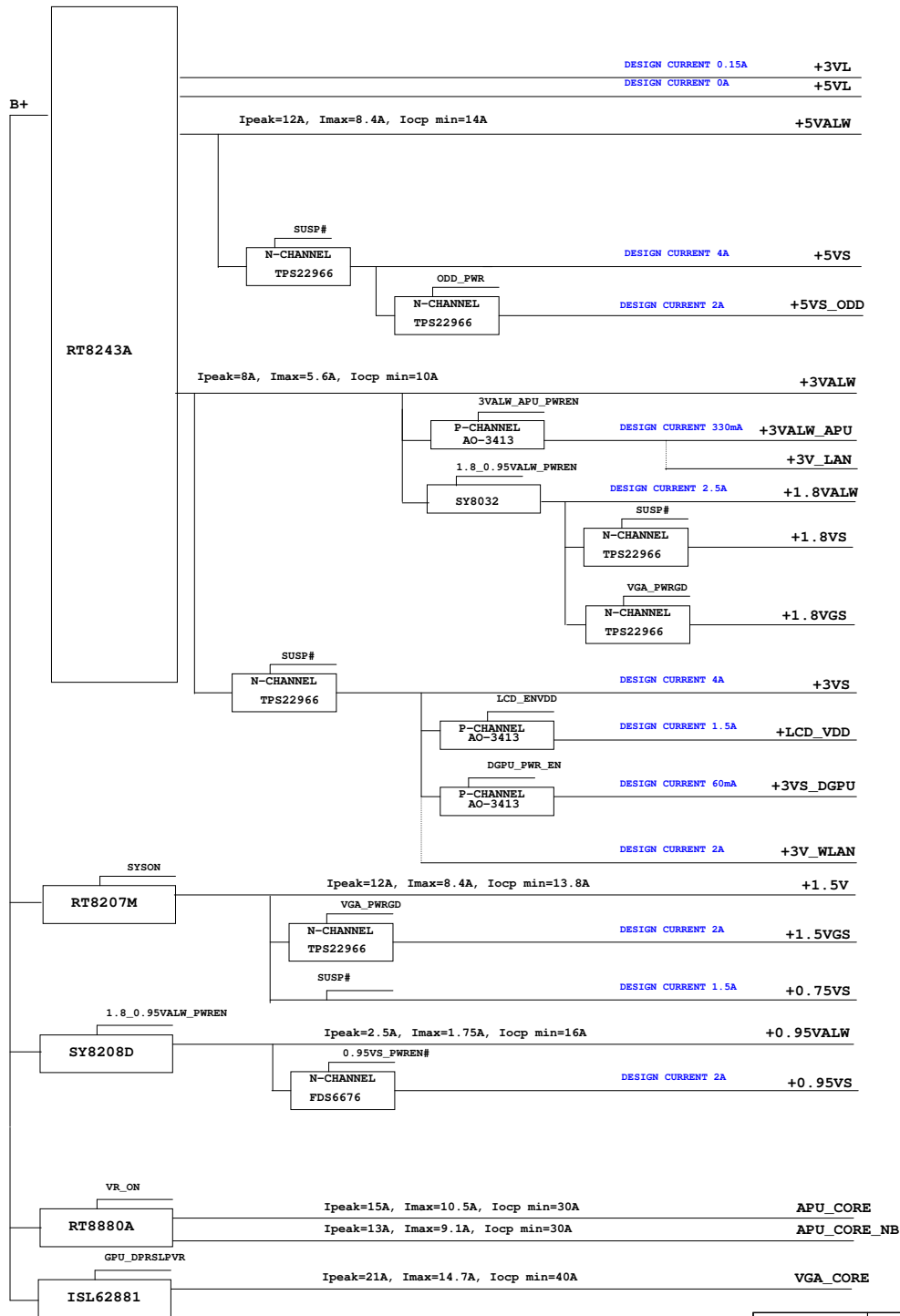
Rosetta 10AN/10ANG

LA-9868P REV 0.2 Schematic

AMD KABINI Quad Core 25W only for UMA
AMD KABINI Quad Core 15W for DIS&UMA
2012-12-20 Rev 0.2

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Voltage Rails

(O MEANS ON X MEANS OFF)

UMA

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

APU SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM A	A0H	1010 0000 b
+3VS	DDR SO-DIMM B	A2H	1010 0010 b
+3VS	WLAN		

EC SM Bus1 Address

EC SM Bus2 Address

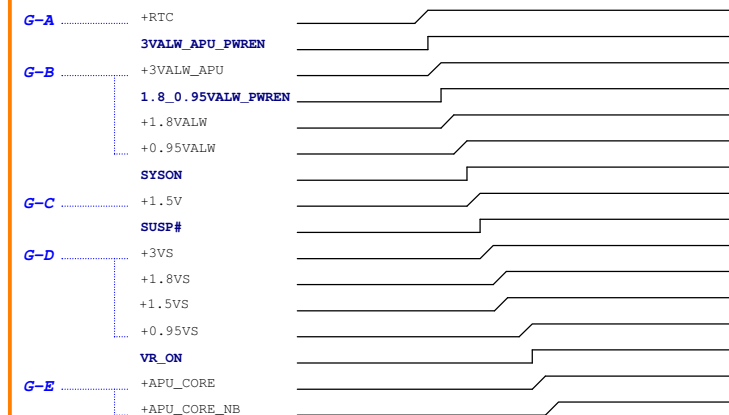
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b	+3VS	G-Sensor	40H	0100 0000 b
+3VL	Charger	12H	0001 0010 b	+3VS	VGA thermal	82H	1000 0010 b
				+3VS	APU thermal	98H	1001 1000 b

BTO Option Table

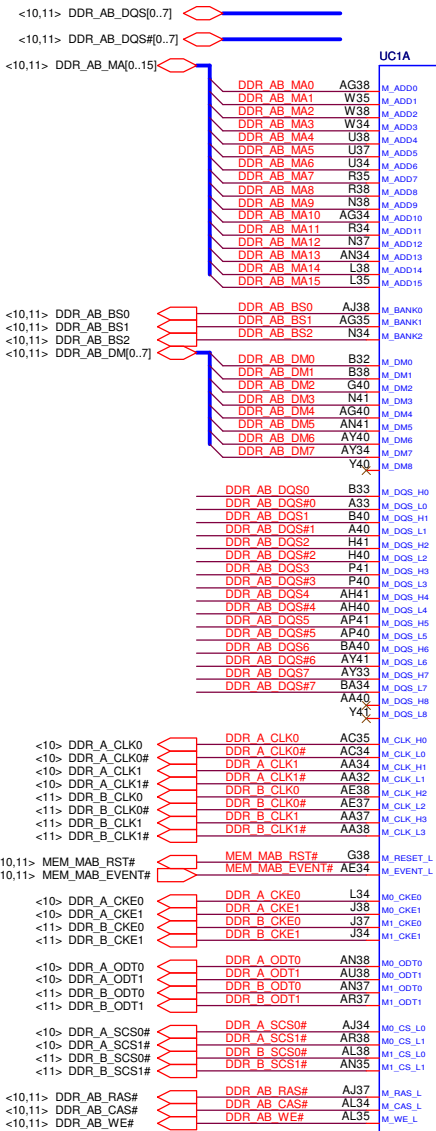
Function								
description								
explain								
BTO								

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

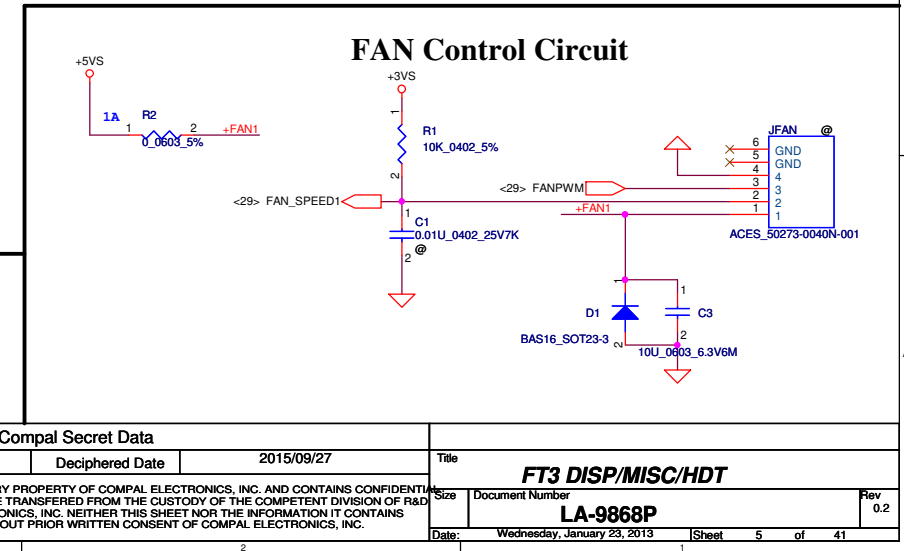
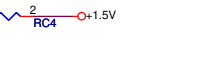
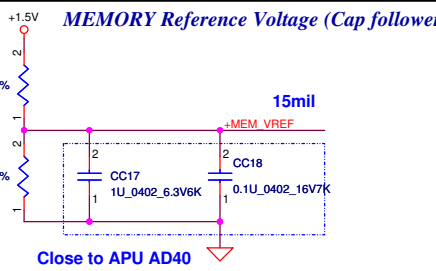
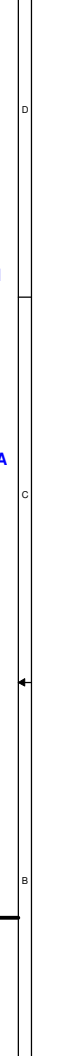
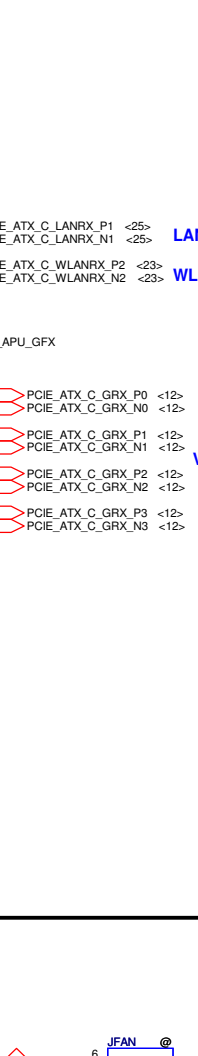
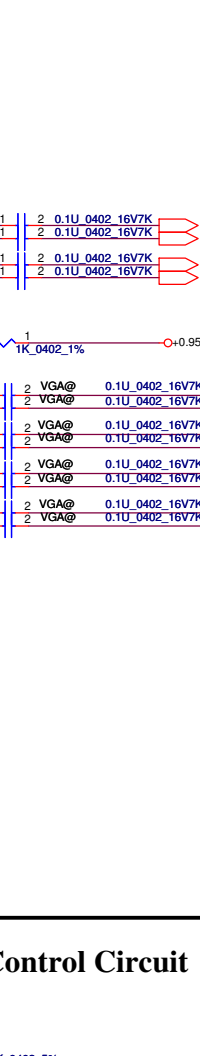
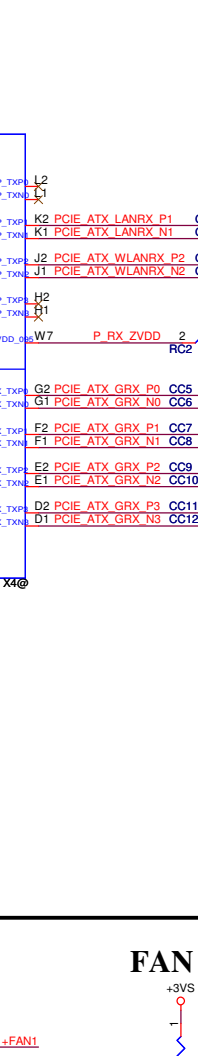
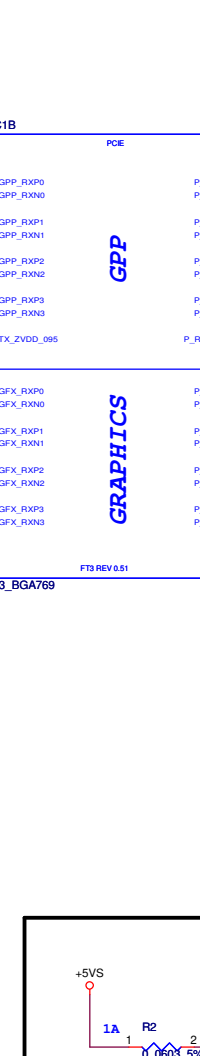
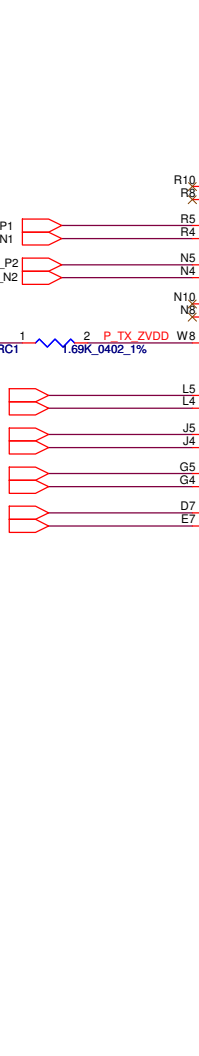
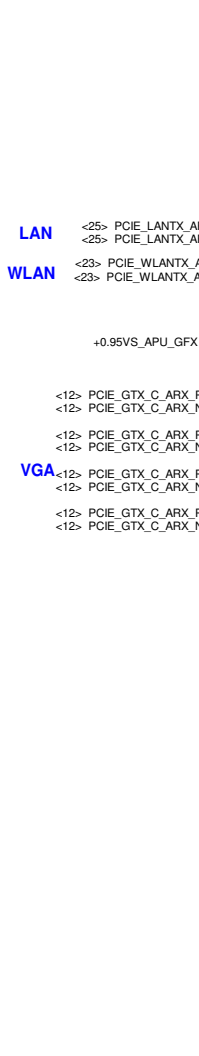
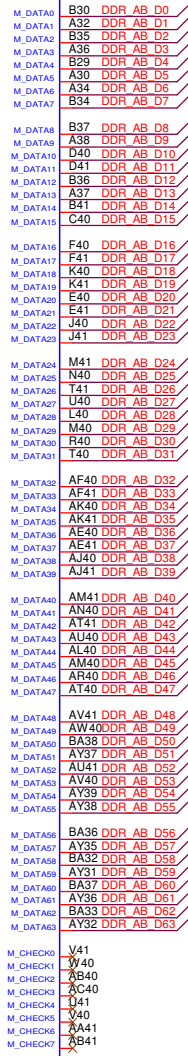
APU POWER SEQUENCE



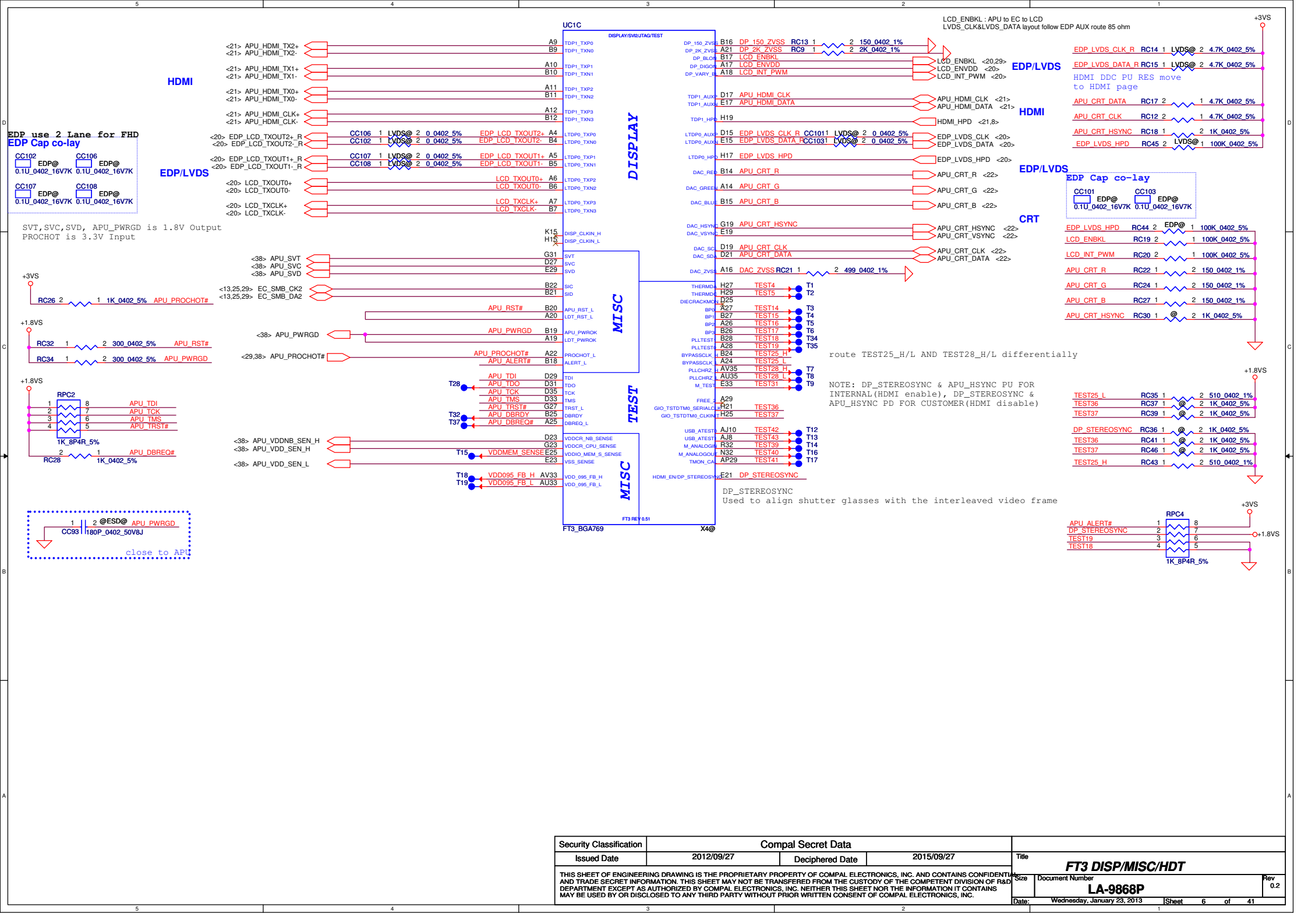
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MEMORY



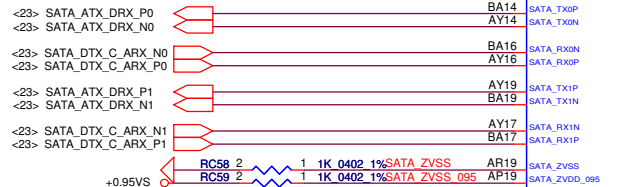
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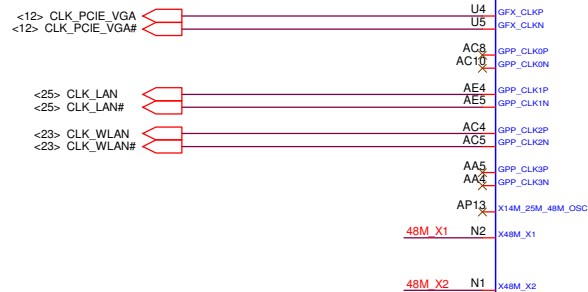
SATA HDD

SATA ODD

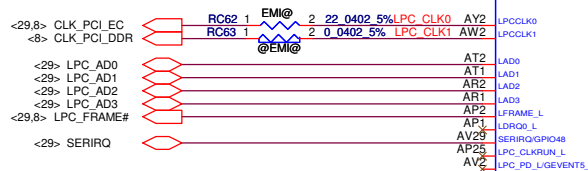


VGA

LAN
WLAN



EC



UC1E

SATA

USB

CLK

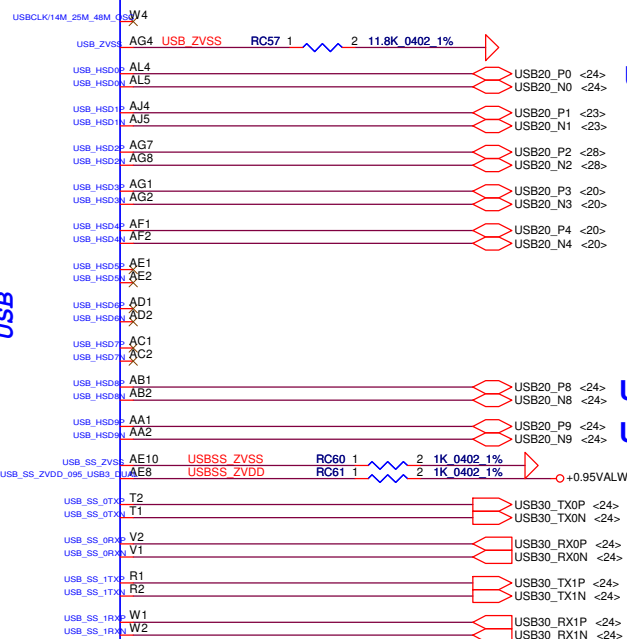
LPC

SPI

FT3_BGA769

X4@

FT3 REV 0.51

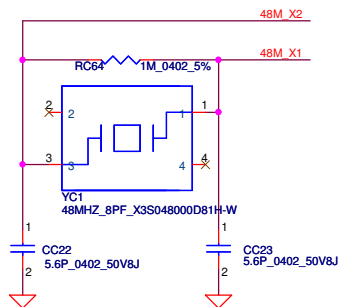


USB2.0-Left1 (Debug Port)
WLAN (BT)
Cardreader
Int. Camera
Touch Screen

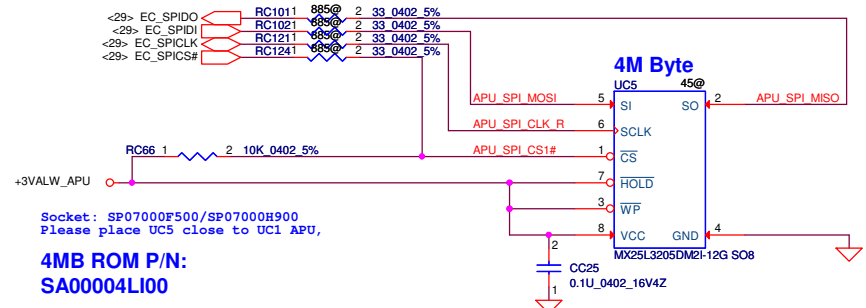
USB2.0-Right1
USB2.0-Right2

USB3.0-Right1
USB3.0-Right2

48KMHZ CRYSTAL



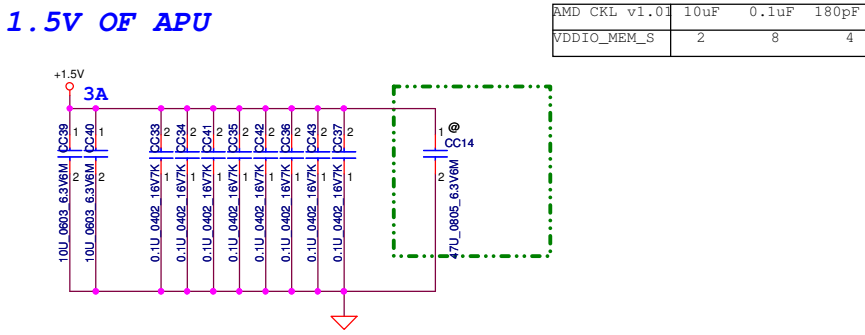
SPI ROM



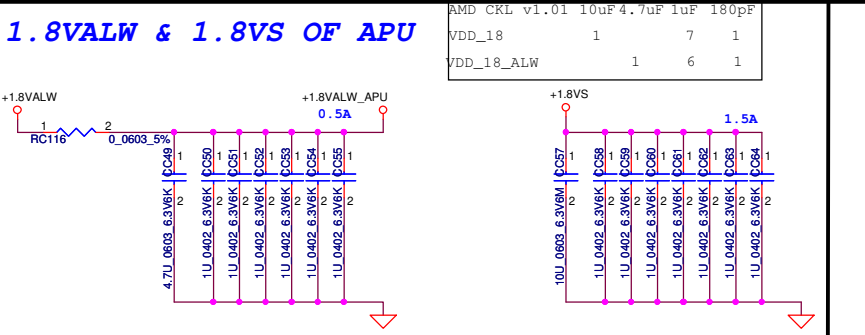
SW said ROM can change to 4MB

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				FT3-SATA/CLK/USB/SPI/LPC		
				Size	Document Number	Rev
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				Date:	Wednesday, January 23, 2013	
3		2		1		

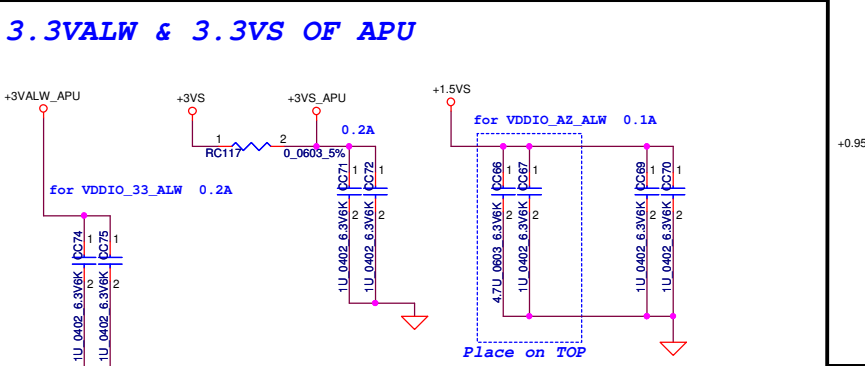
1.5V OF APU



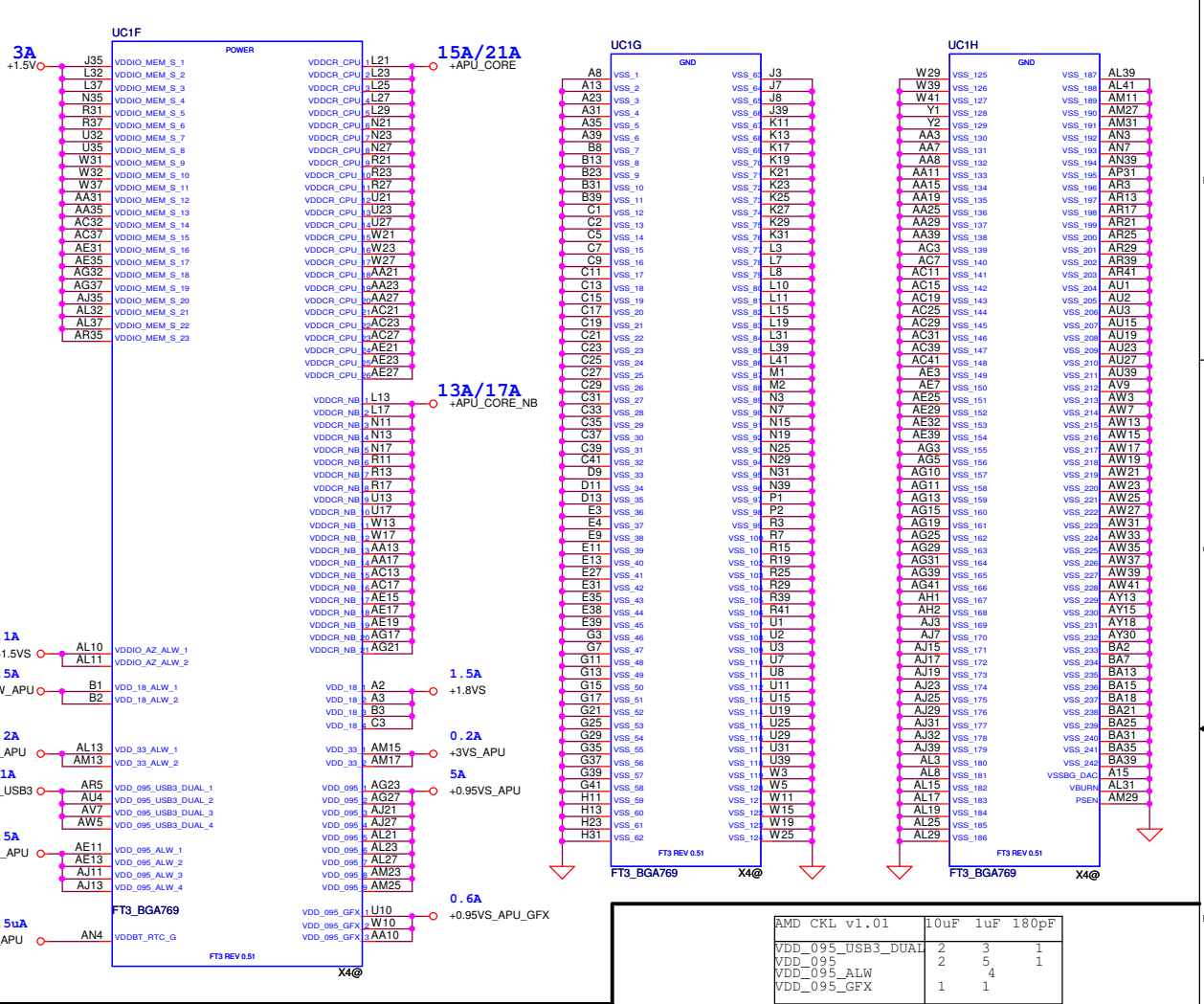
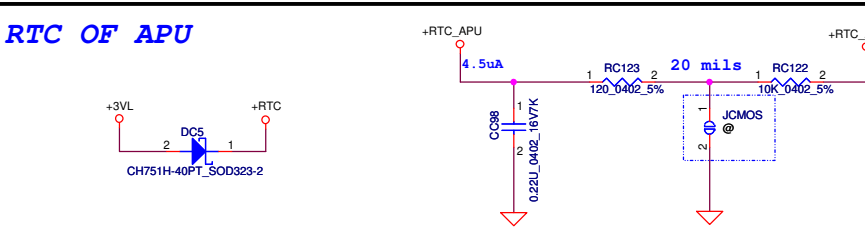
1.8VALW & 1.8VS OF APU



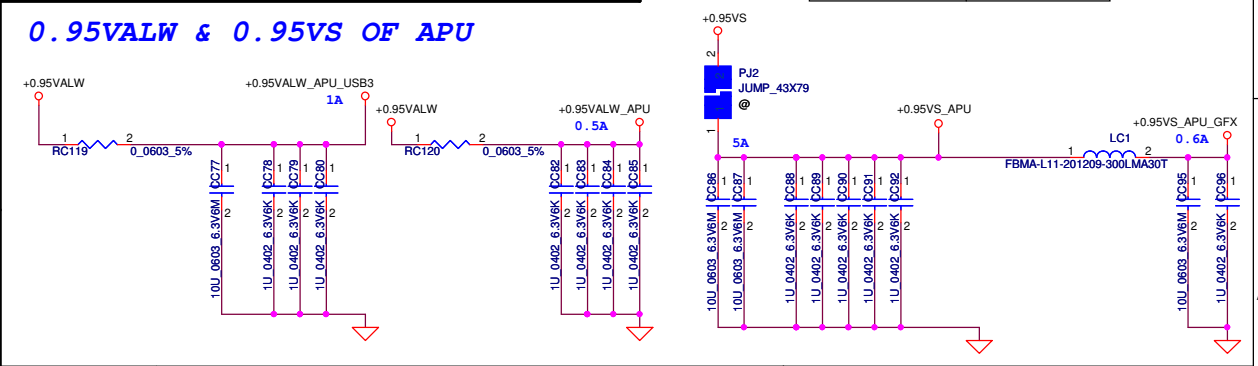
3.3VALW & 3.3VS OF APU



RTC OF APU



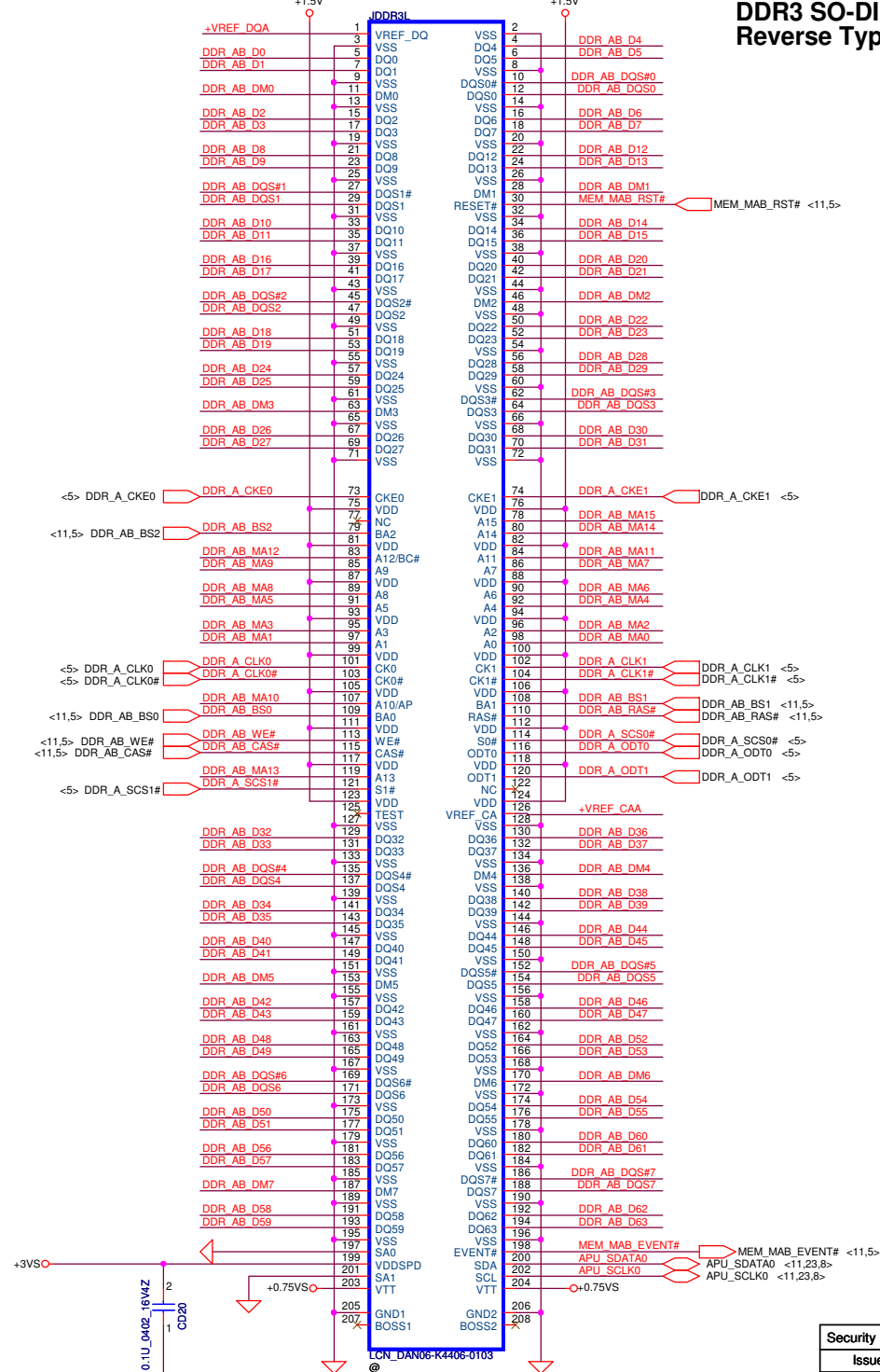
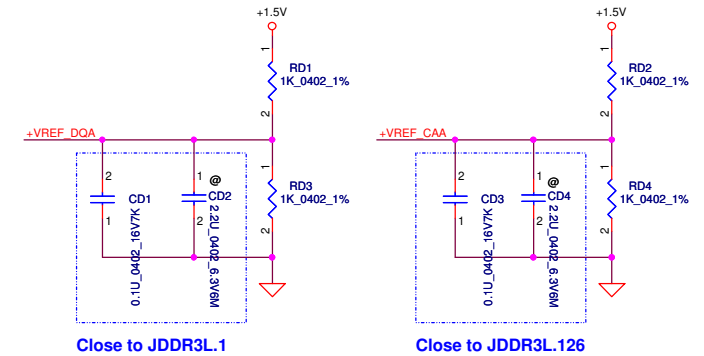
0.95VALW & 0.95VS OF APU



DDR3 SO-DIMM A Reverse Type

DDR_AB_DQS[0..7] <11,5>
DDR_AB_DQS[0..7] <11,5>
DDR_AB_DM[0..7] <11,5>
DDR_AB_MA[0..15] <11,5>

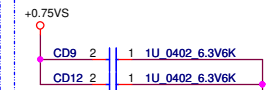
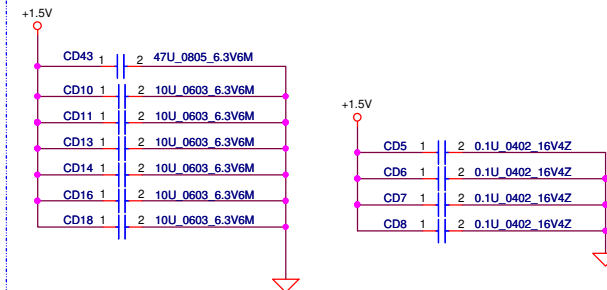
SO-DIMM VREF



Layout Note:
Place near JDDR3L

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMA

Layout Note:
Place near JDDR3L.203 and 204

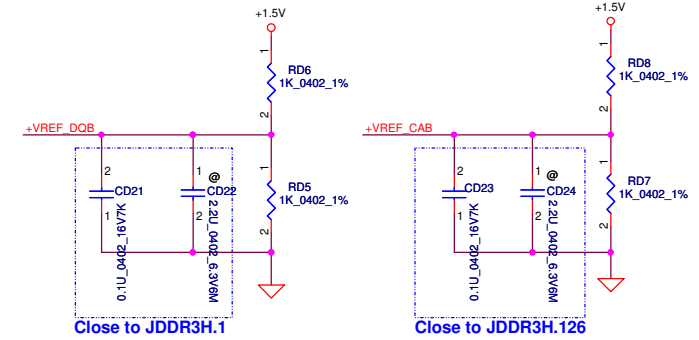


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DDR3 SO-DIMM B Reverse Type

DDR_AB_DQS[0..7] <10,5>
DDR_AB_DQS#0..7 <10,5>
DDR_AB_D[0..63] <10,5>
DDR_AB_DM[0..7] <10,5>
DDR_AB_MA[0..15] <10,5>

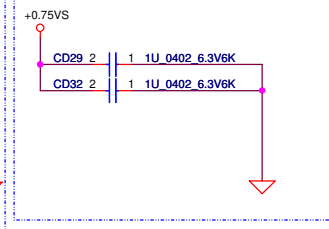
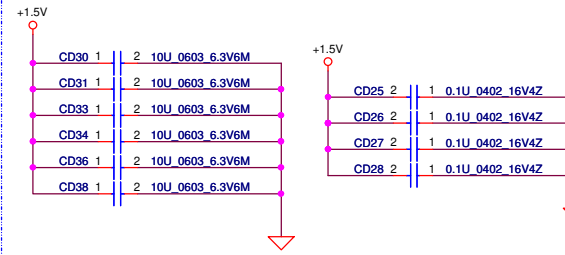
SO-DIMM VREF



Layout Note:
Place near JDDR3H

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

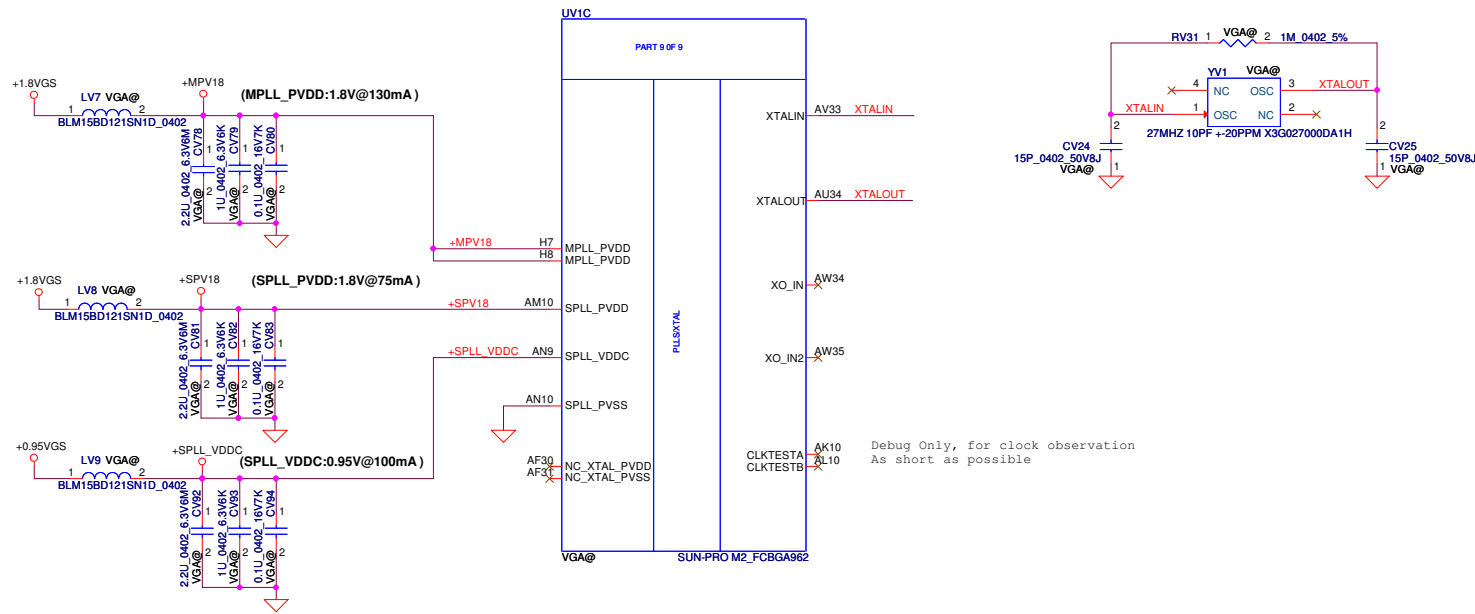


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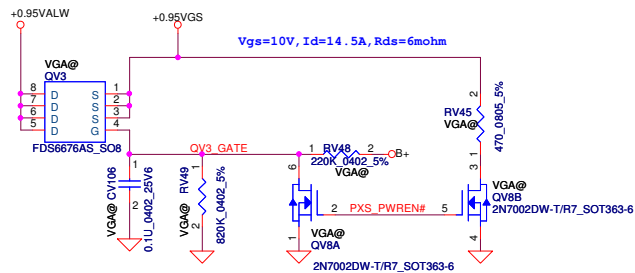
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

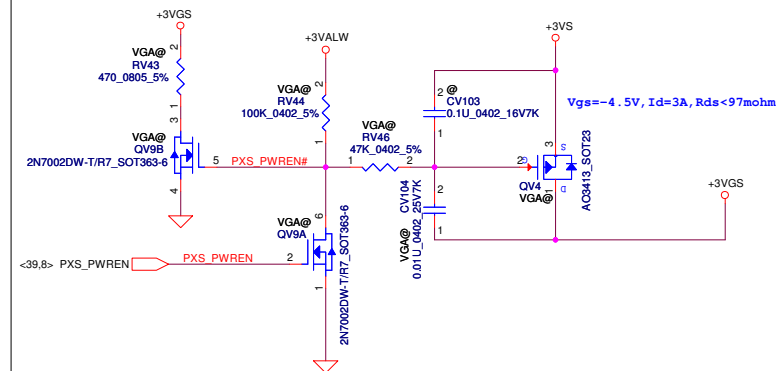
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+0.95VS to +0.95VGS



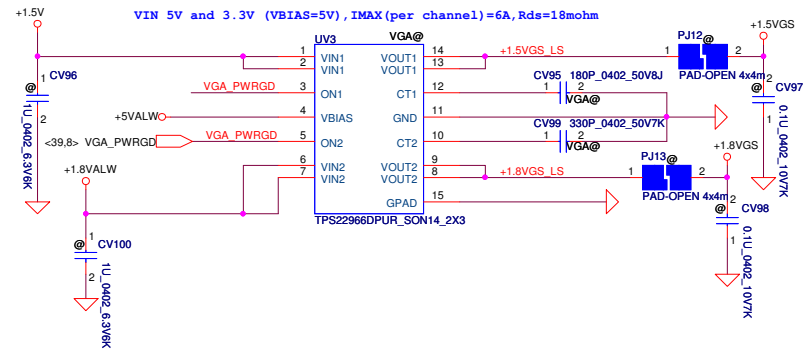
+3VS to +3VGS



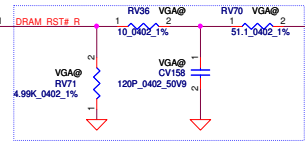
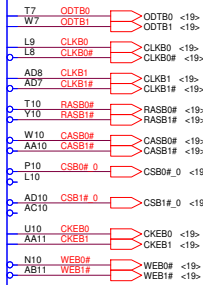
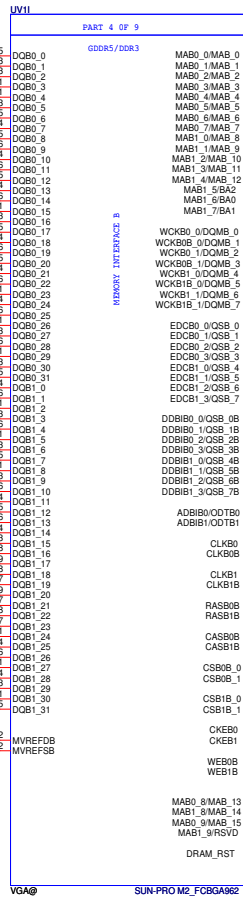
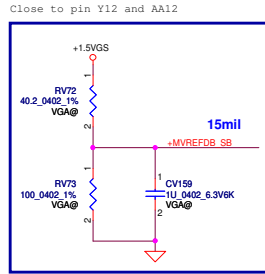
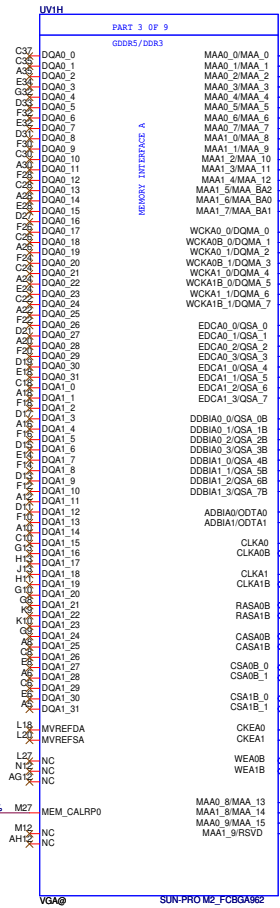
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Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS



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Place all these components close to GPU (Within 25mm) and keep all component close to each other

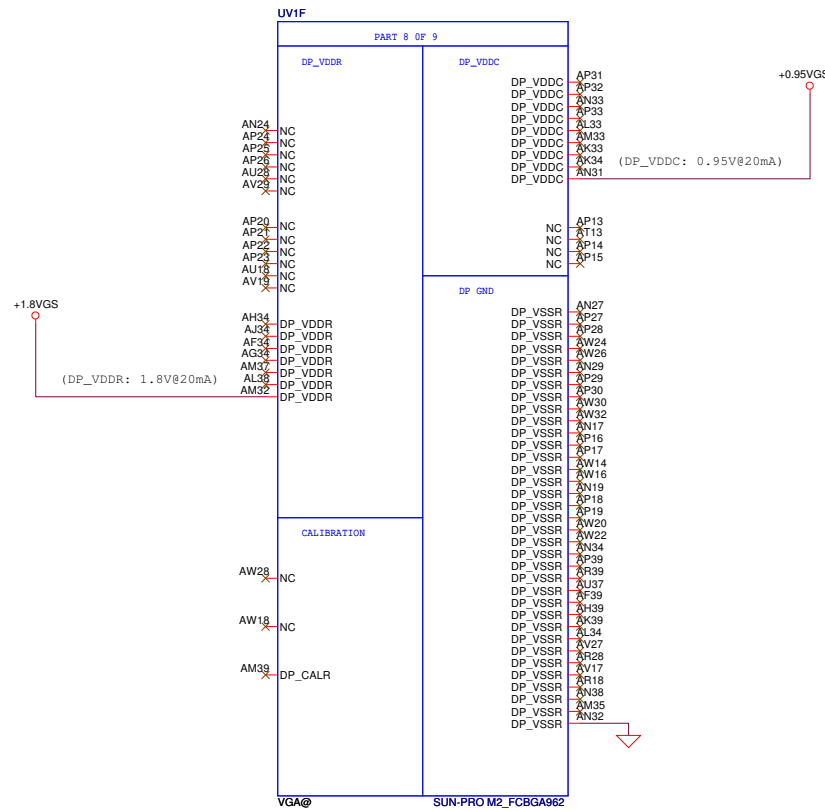
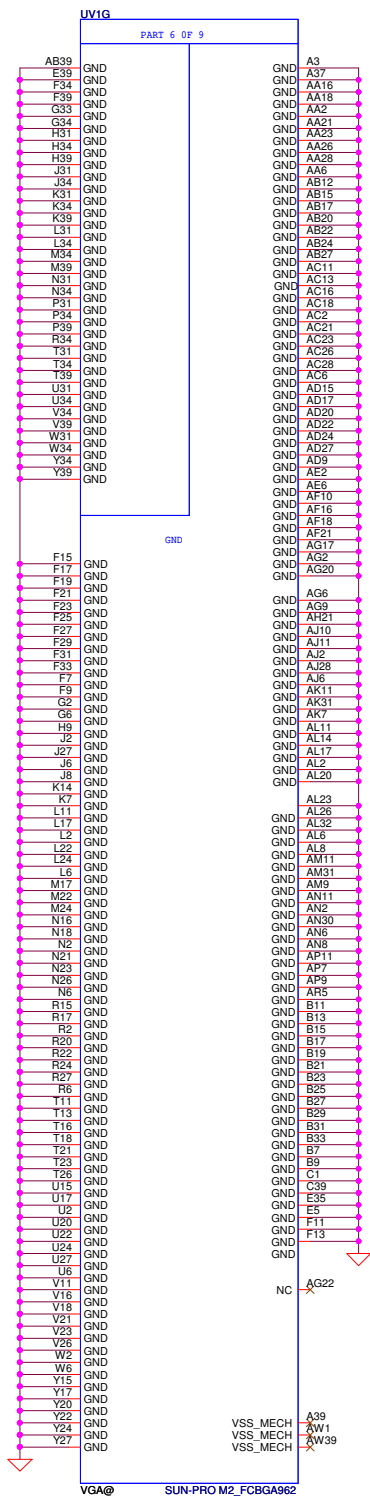
Memory clock 900MHz RC99 10K pull down

R_pu & R_pd resistor:
0402 1% resistors are required.

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA00003YO70	H5TQ2G63DFR-11C	X7648051L01	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Micron	SA00005XB00	MT41K128M16JT-107G.K	X7648051L03	2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH00	K4W2G1646E-BC11	X7648051L04	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC

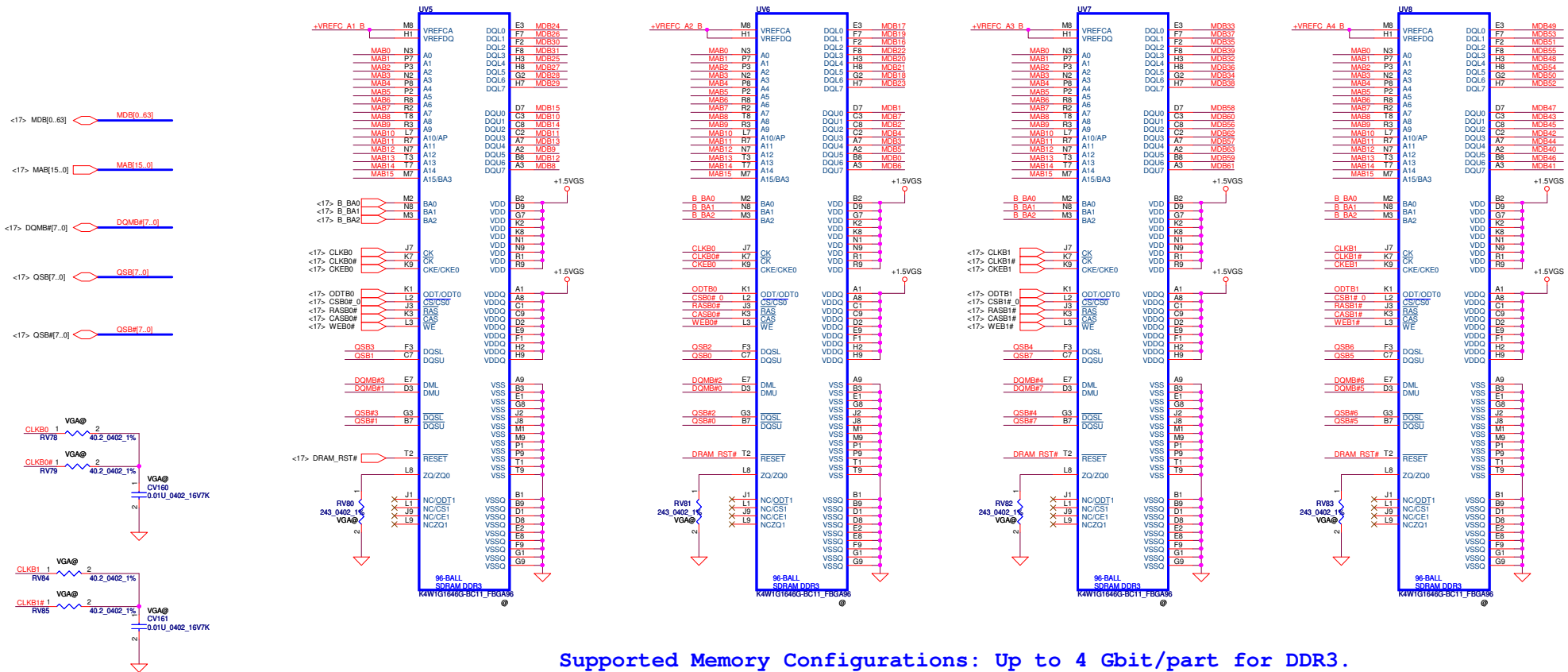
Memory clock 1GHz RC95 10K pull high

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA000065300	H5TQ2G63DFR-N0C	X7648051L02	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Samsung	SA000068U00	K4W2G1646E-BC1A	X7648051L05	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC

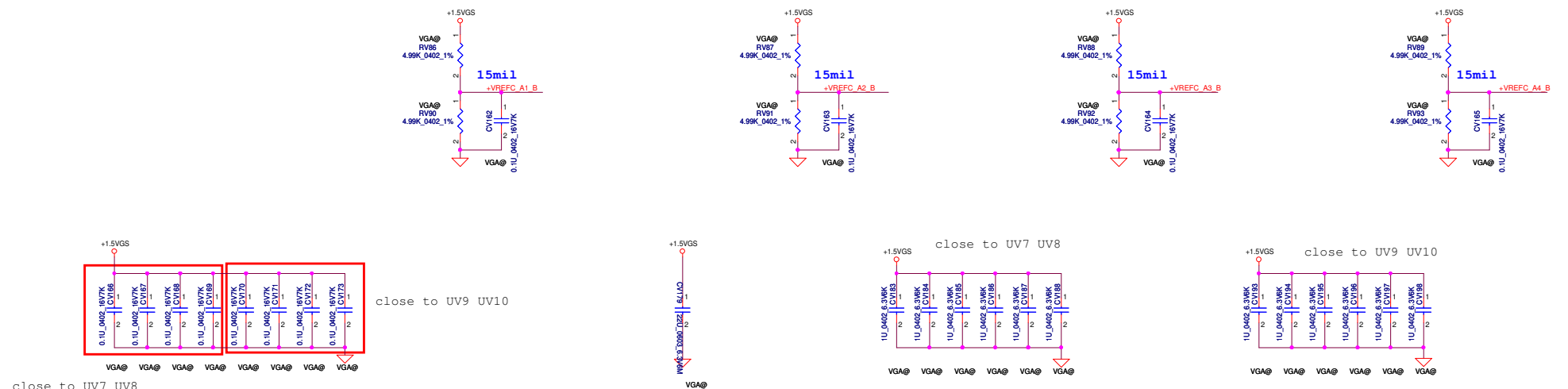


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				Rev	0.2	
Date: Wednesday, January 23, 2013				Sheet	18	of 41

CHANNEL B: 512MB/1024MB DDR3



Supported Memory Configurations: Up to 4 Gbit/part for DDR3.

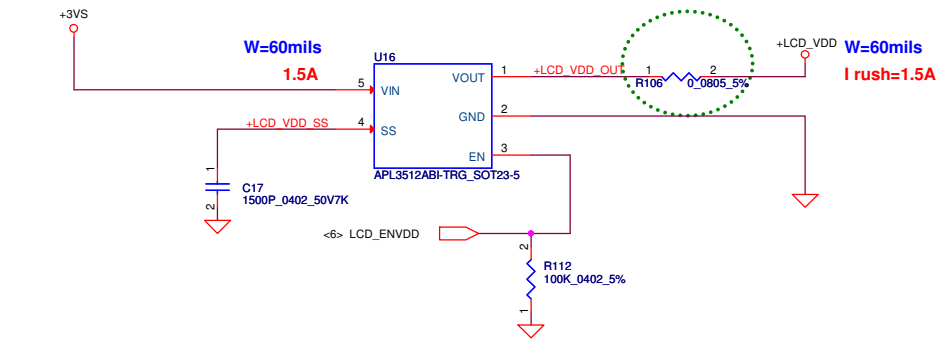


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Issued Date	2012/09/27	Deciphered Date	2015/09/27	Size		VRAM Channel B	
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				Date:	Wednesday, January 23, 2013	Sheet	19 of 41

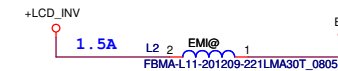
LCD_VDD

Need check eDP&LVDS both 3V power rail.

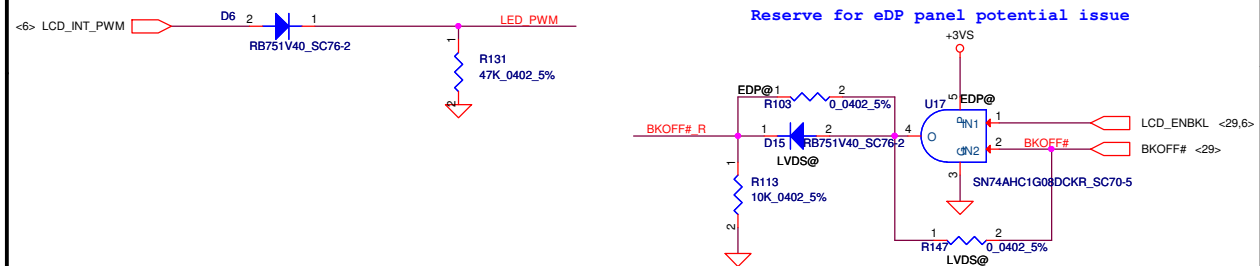
Reserve for power consumption
Remove on PVT phase



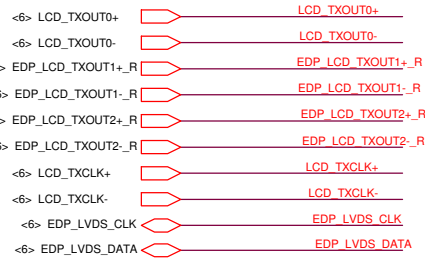
LCD_INV



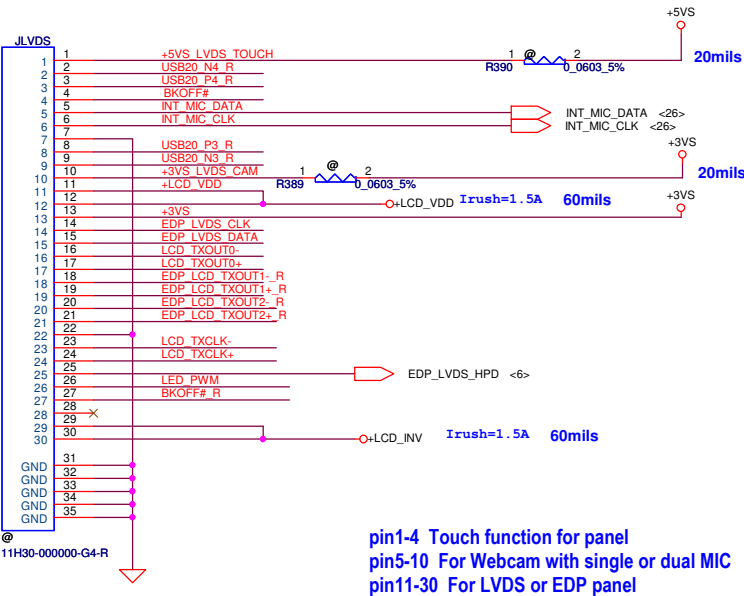
LCD Control



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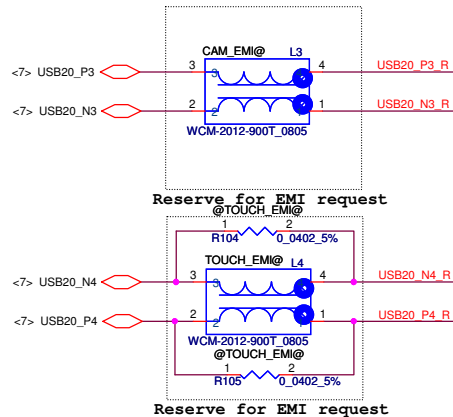


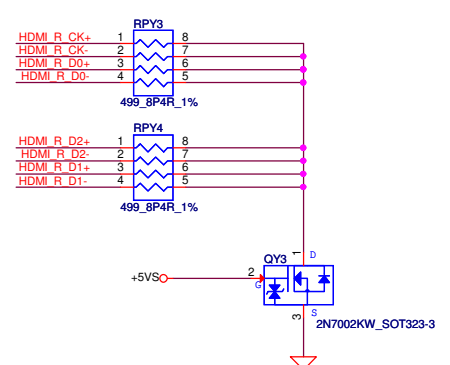
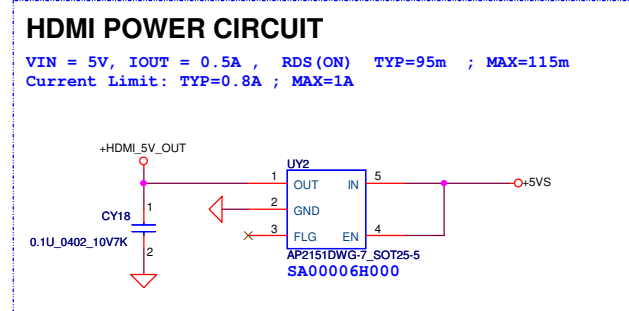
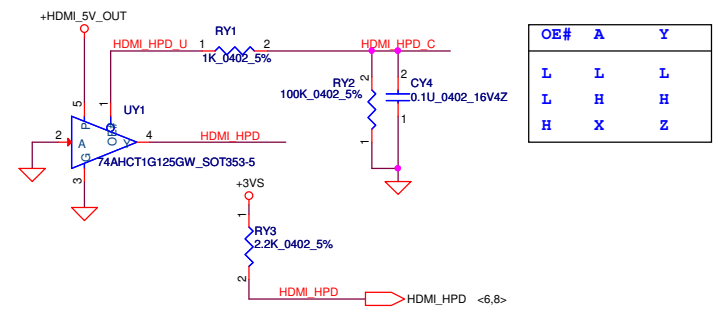
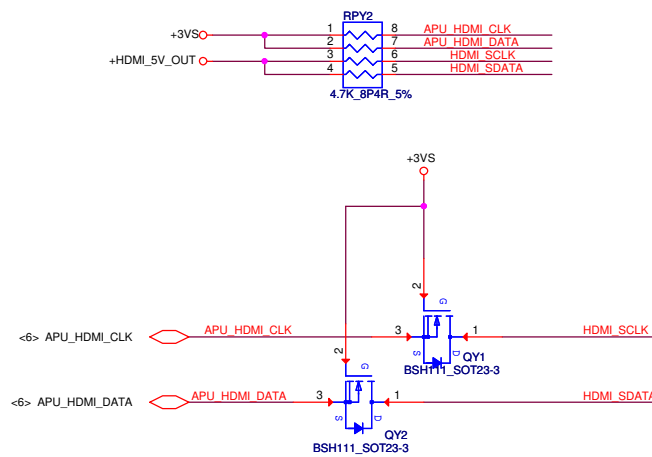
If it's EPD, they're become
LCD_TXOUT2+_R = EDP_TX0+
LCD_TXOUT2-_R = EDP_TX0-
LCD_TXOUT1+_R = EDP_TX1+
LCD_TXOUT1-_R = EDP_TX1-
LVDS_CLK = EDP_AUXP
LVDS_DATA = EDP_AUXN



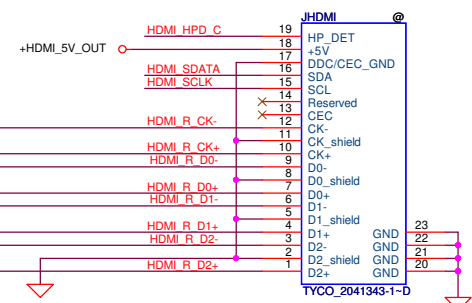
pin1-4 Touch function for panel
pin5-10 For Webcam with single or dual MIC
pin11-30 For LVDS or EDP panel

Camera & Touch Screen





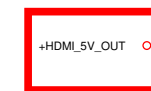
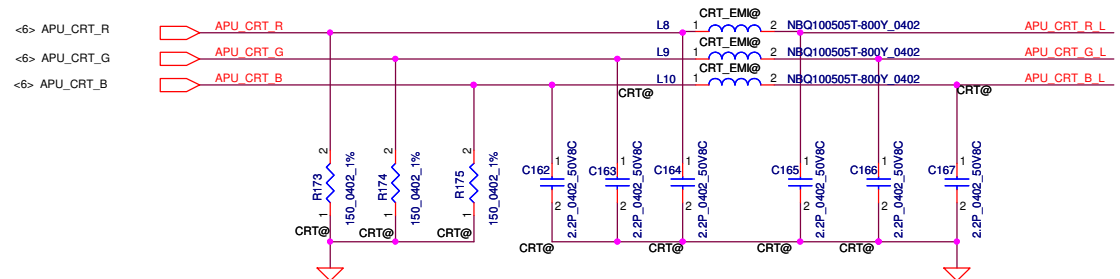
HDMI Connector



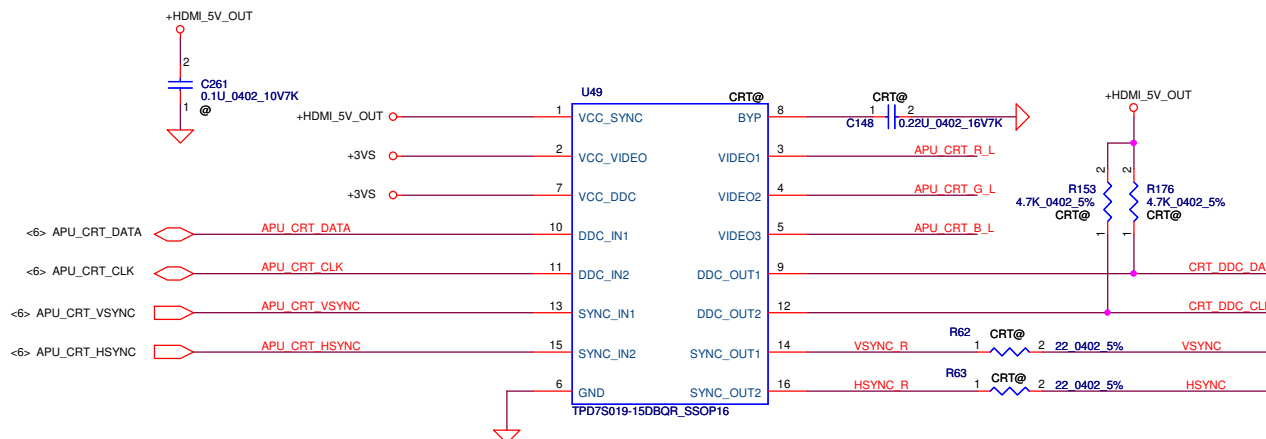
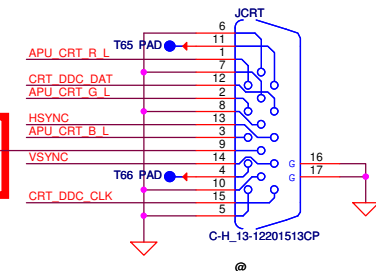
HDMI Royalty
RO0000003HM
HDMI W/Logo + HDCP
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

please manually load
this virtual material to 45@ BOM

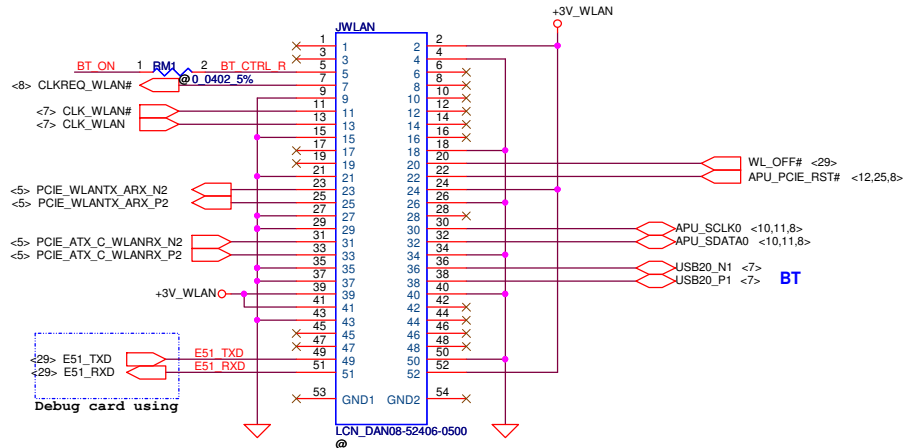
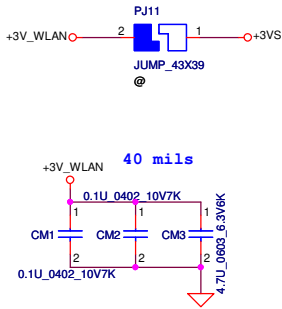
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						Size	Document Number		Rev				
							LA-9868P		0.2				
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USE HDMI POWER



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Size		Document Number			Rev
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Slot 1 Half PCIe Mini Card-WLAN

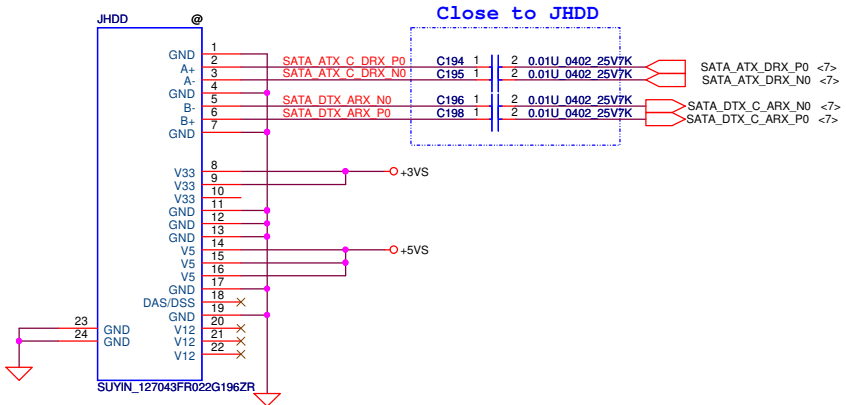
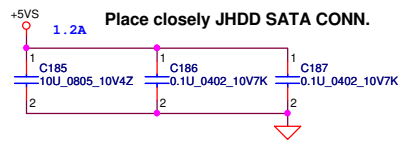
WLAN&BT Combo module circuits		
	BT on module Enable	BT on module Disable
BT_ON	H	L

From EC

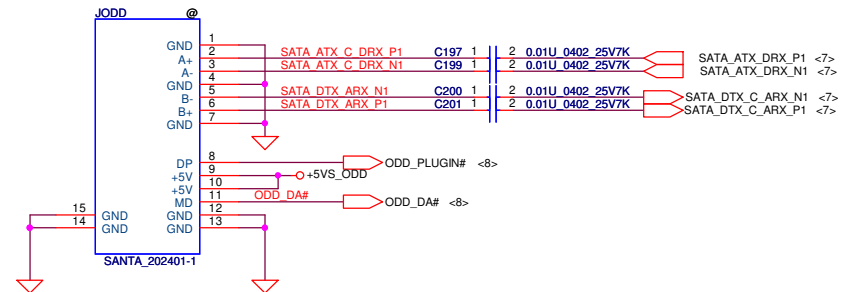
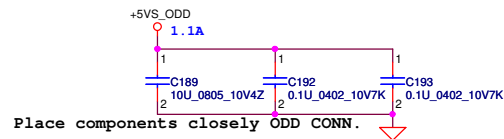
<29> BT_ON  BT ON 1 RM2 2 E51 RXD
1K_0402_5%

For isolate BT_CTRL and
Compal Debug Card.

SATA HDD Conn.



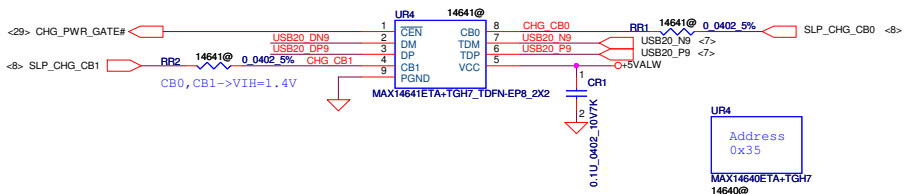
SATA ODD Conn



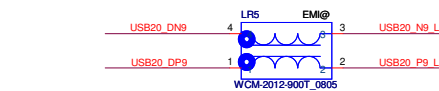
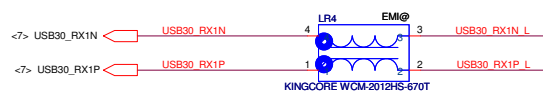
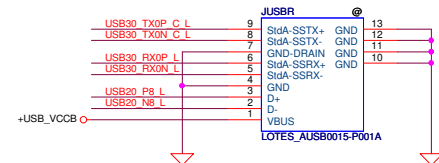
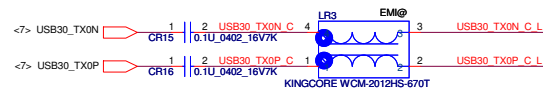
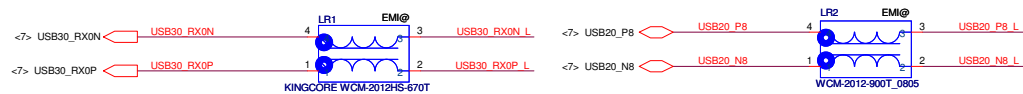
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Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	WLAN/SATA HDD&ODD	
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USB Sleep & Charge

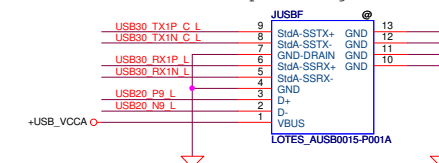
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.



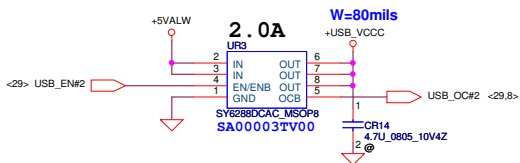
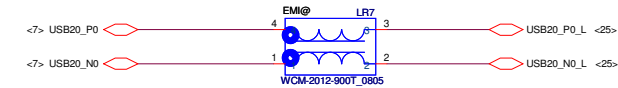
Right side USB 3.0 x 2/ Sleep&Charge



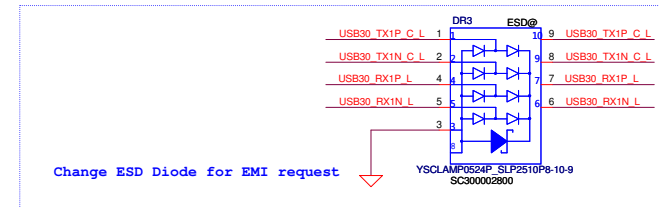
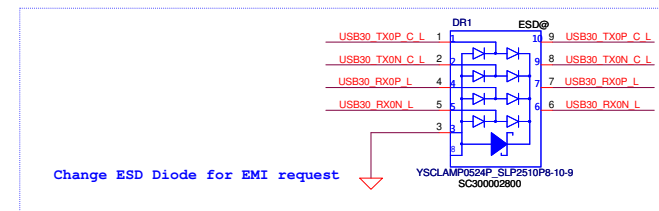
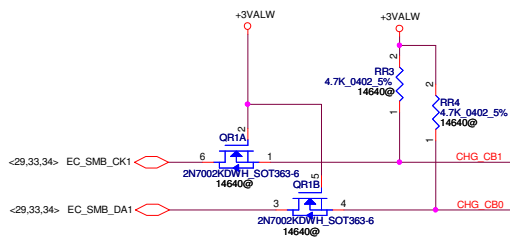
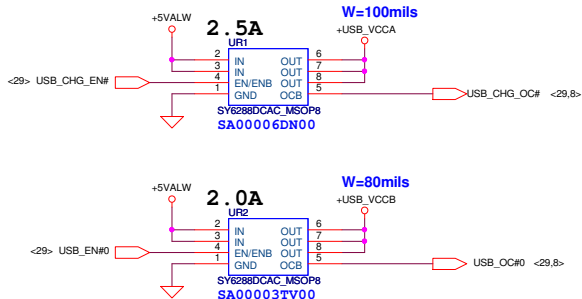
Sleep & Charge Port



Left Side USB Port



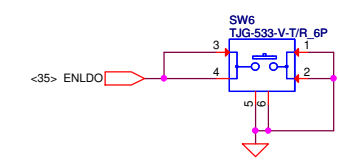
USB POWER SWITCH



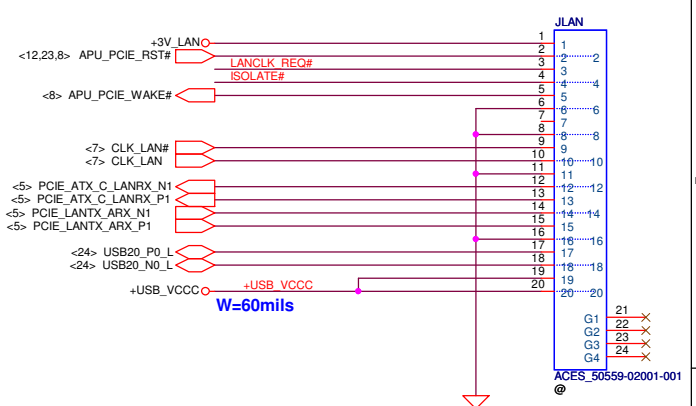
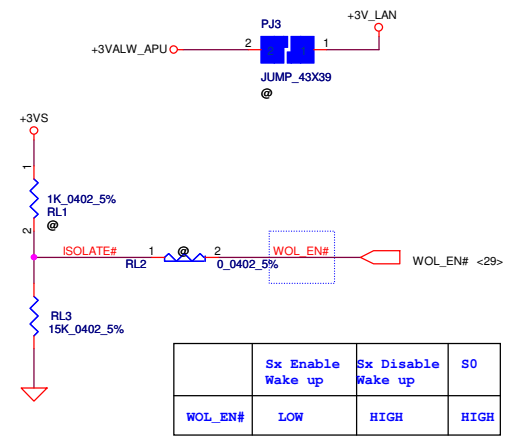
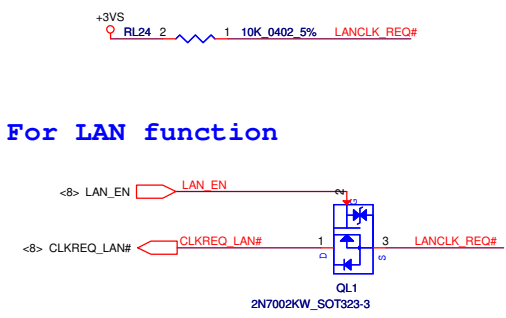
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Battery Reset

LAN Conn

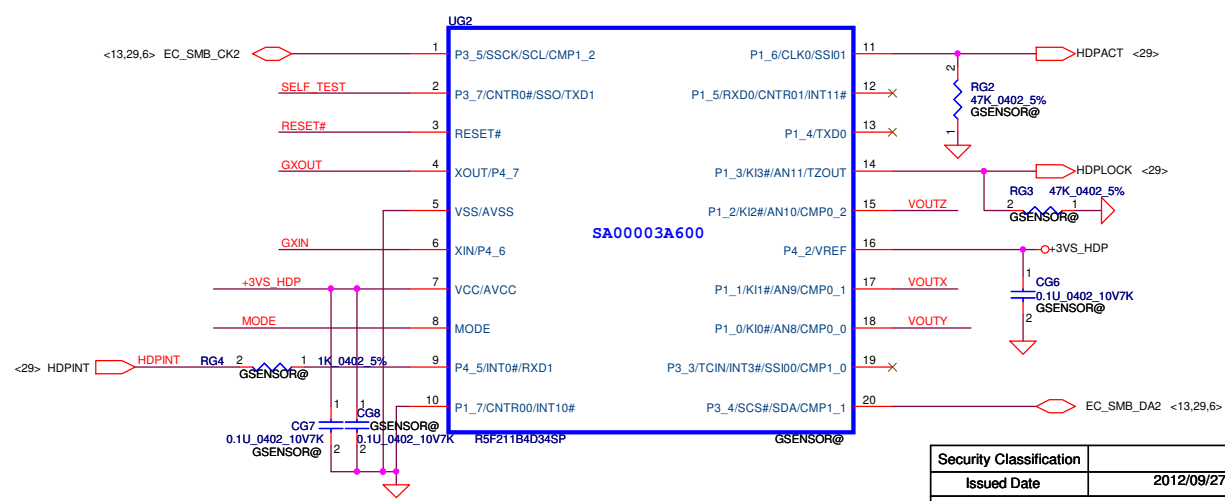
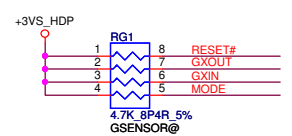
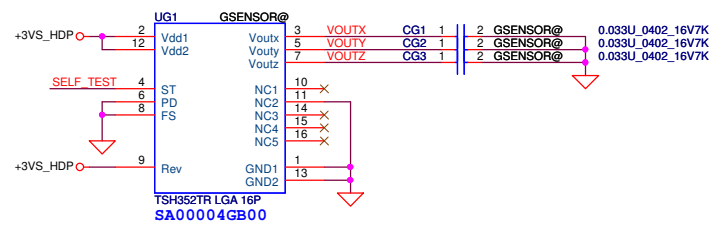
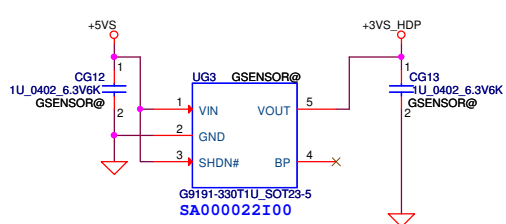


For LAN function



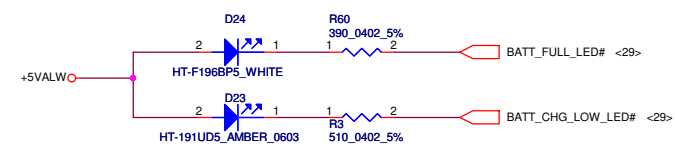
	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

G-SENSOR



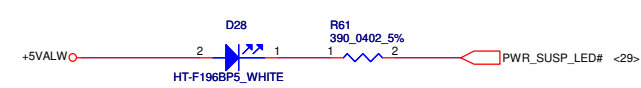
LED

BATT CHARGE /FULL LED



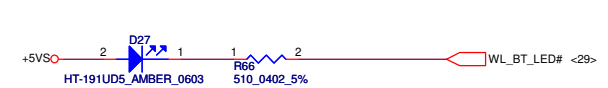
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED



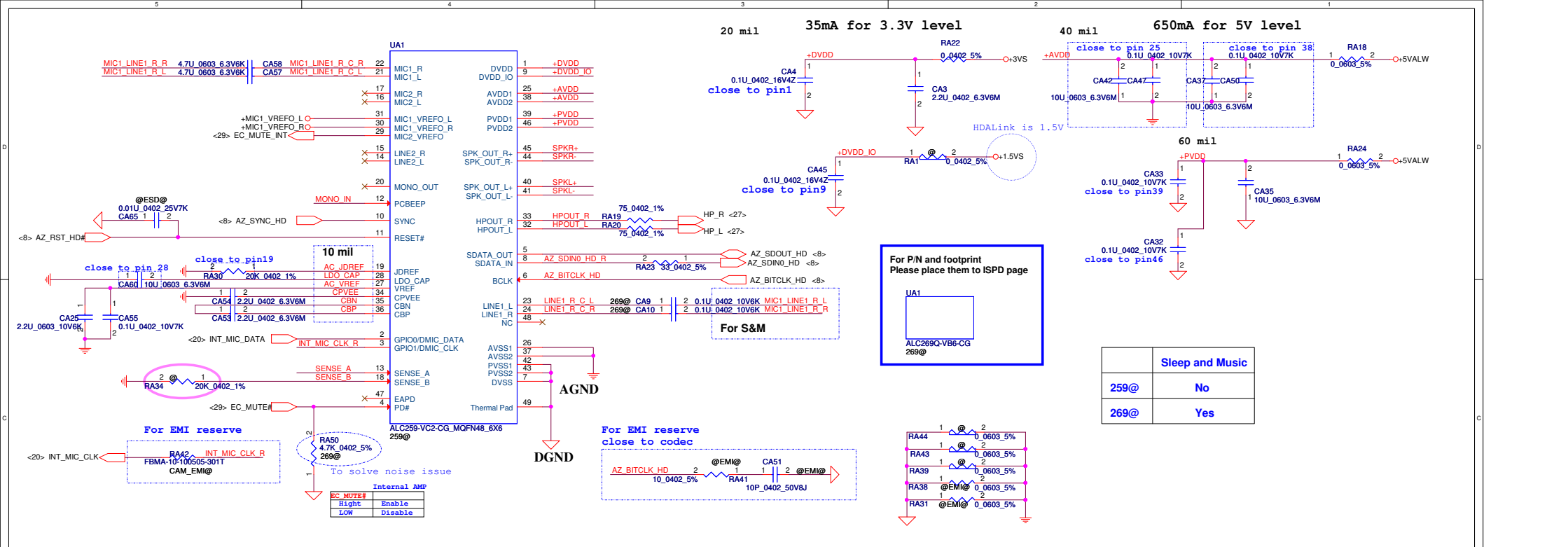
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED (AMD NO WiMAX)

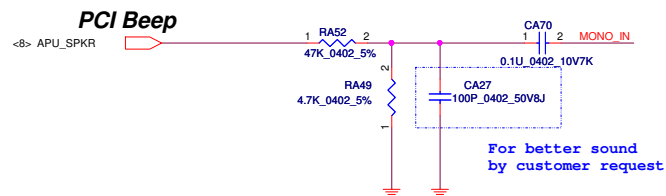


Amber LED bright while Wireless and/or WiMAX turns on.

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		LAN/G-SENSOR/LED/B_RES
Size	Document Number	Rev
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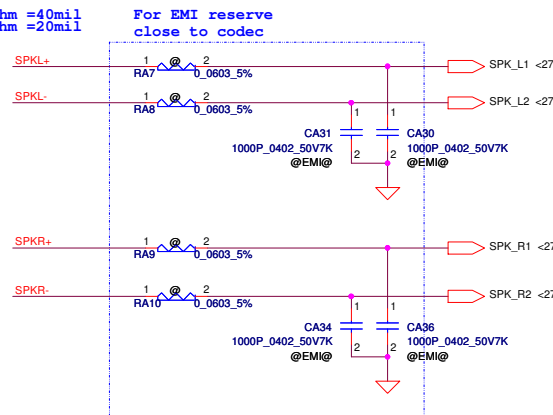


Beep sound

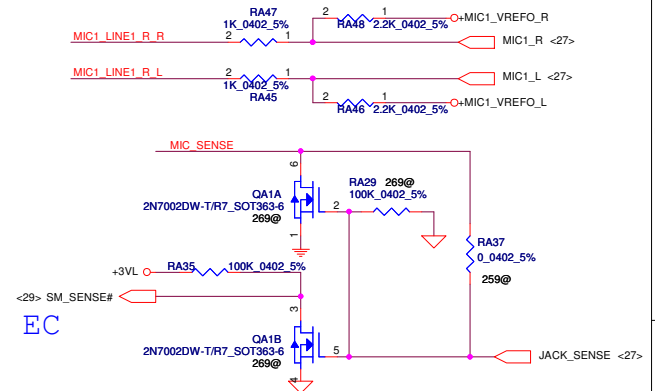


SPK

2W 4ohm =40mil
1W 8ohm =20mil

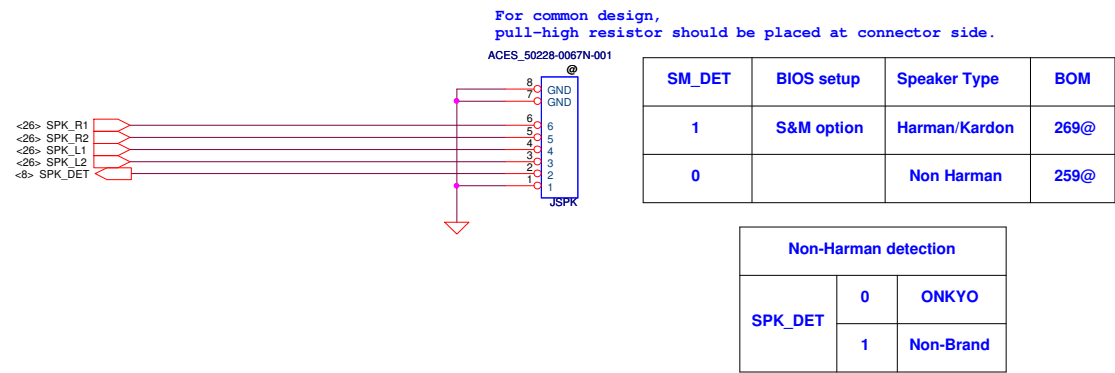


MIC/LINE IN

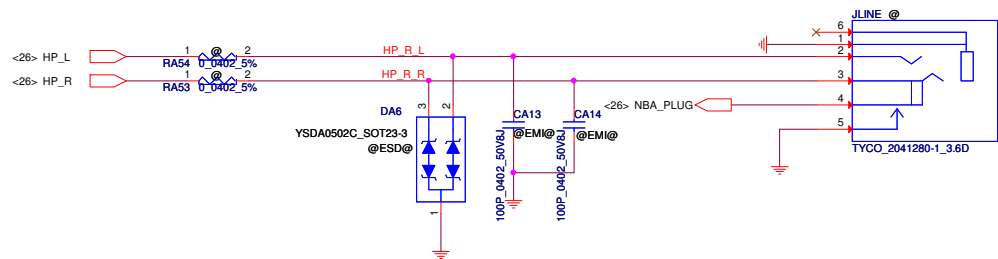


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

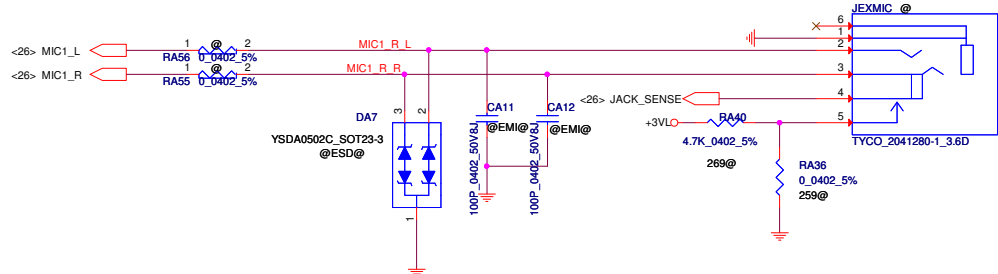
SPK Conn.

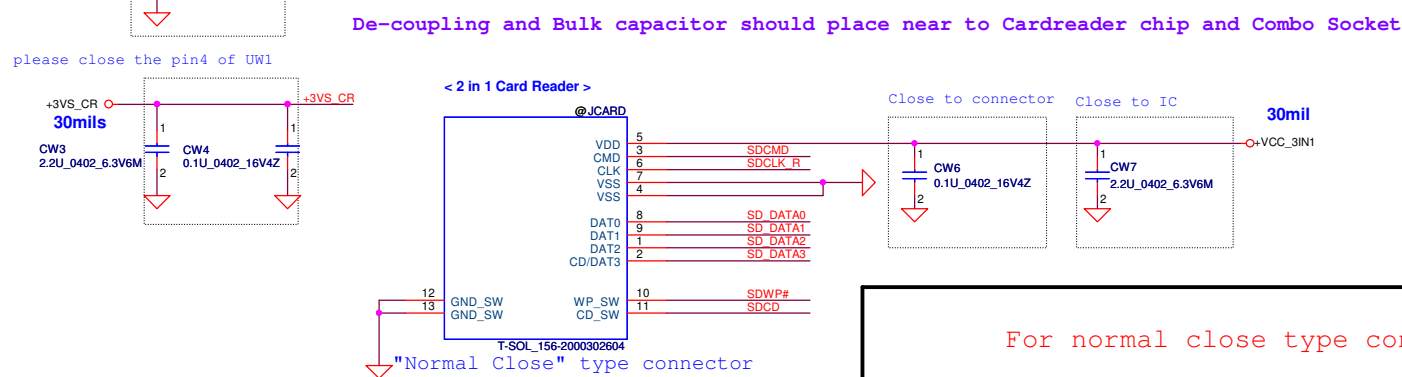
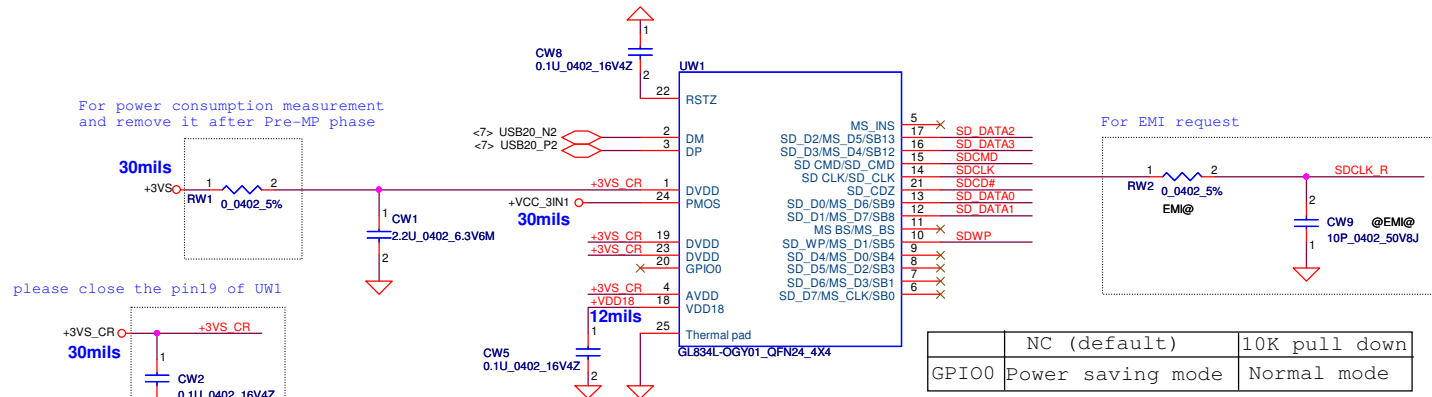


HeadPhone/LINE Out JACK



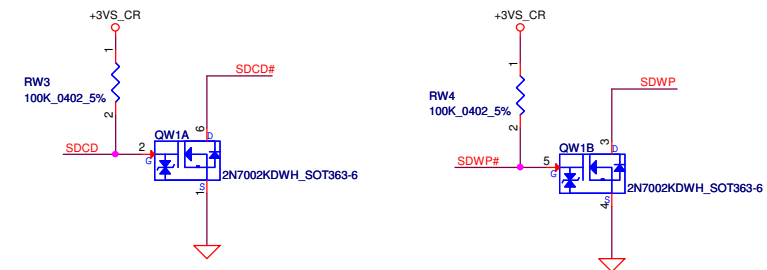
MIC/LINE IN JACK

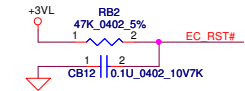
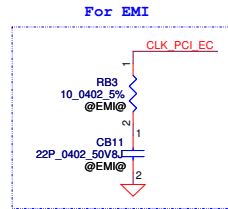




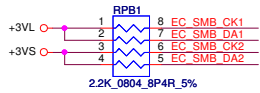
	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit

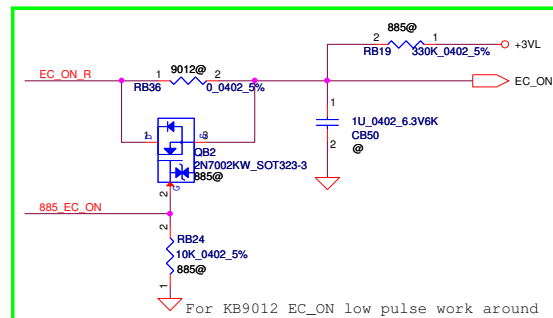
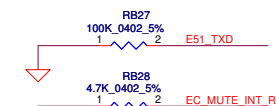
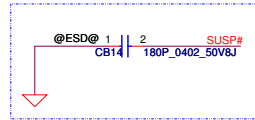




SMBUS1->BATT, Smart Charger
SMBUS2->G-Sensor, GPU Thermal Sensor,
APU Thermal Sensor
EC SMBus2 for S0, SMBus1 for S5

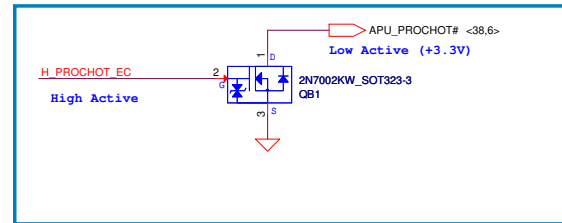


P.32_SYS_PWRGD OD/L
for 1.8V PU APU

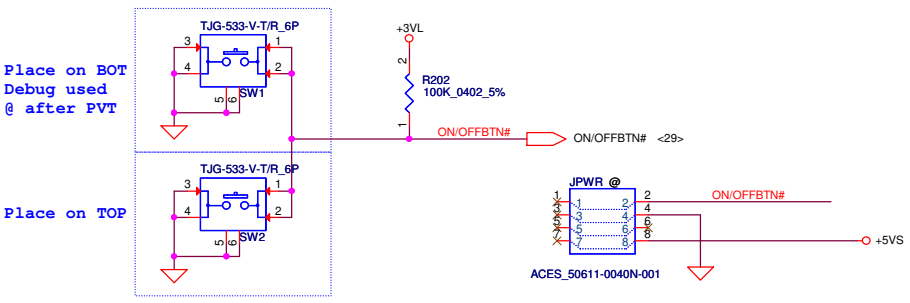


Voltage Comparator Pins FOR 9012 A3

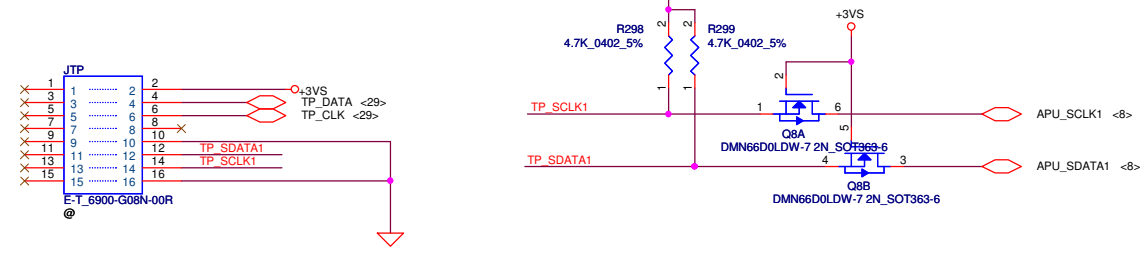
VCIN0 pin109	>1.2V	<1.2V
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



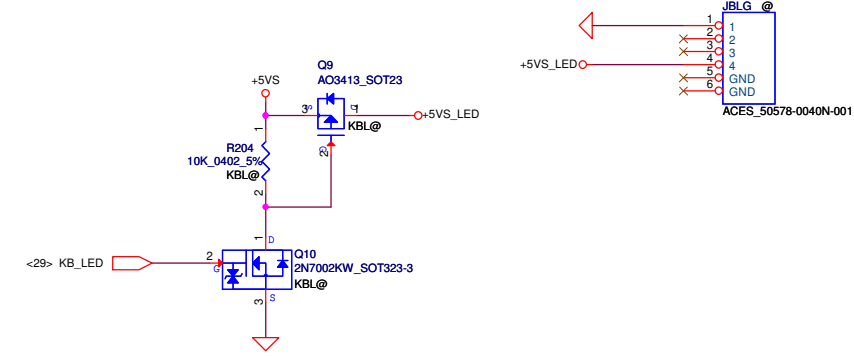
Power Button



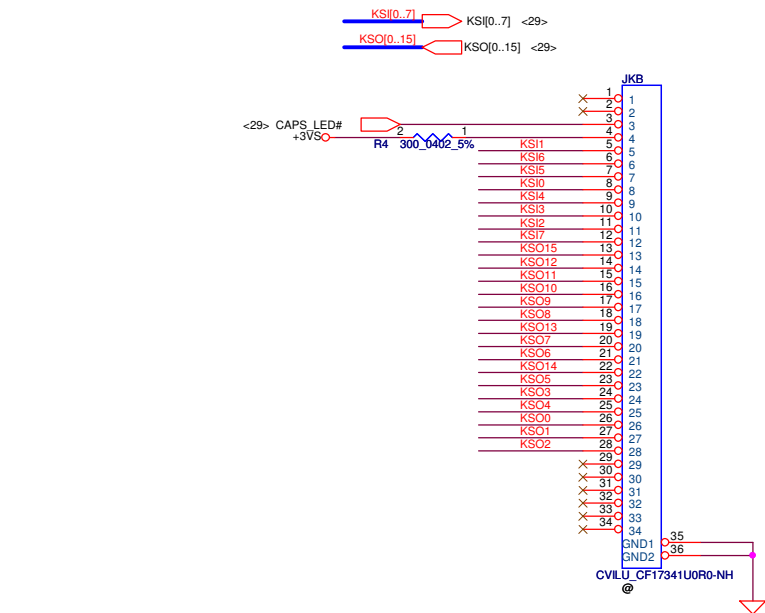
Touchpad Connector



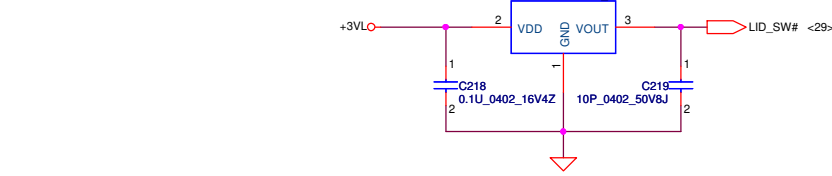
Keyboard LED



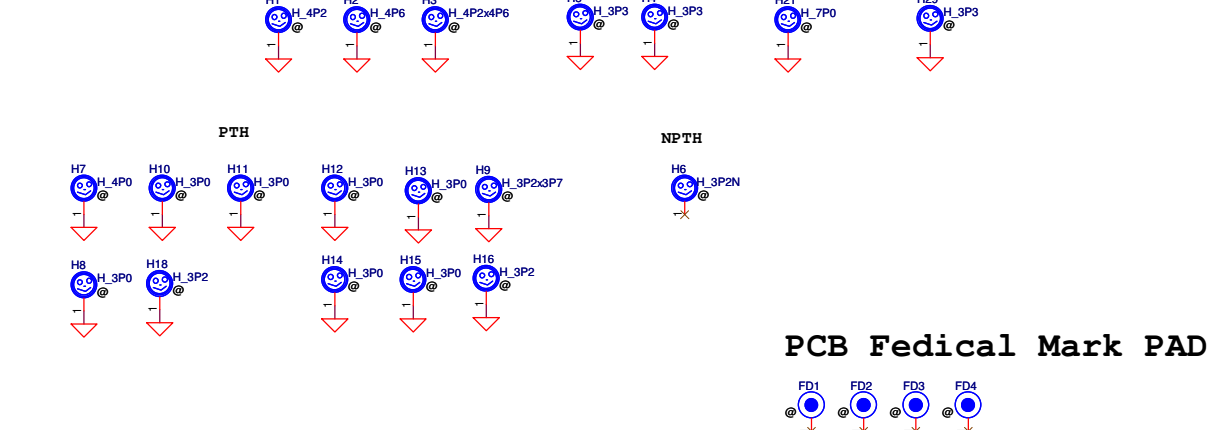
NEW KEYBOARD CONN.



Lid SW



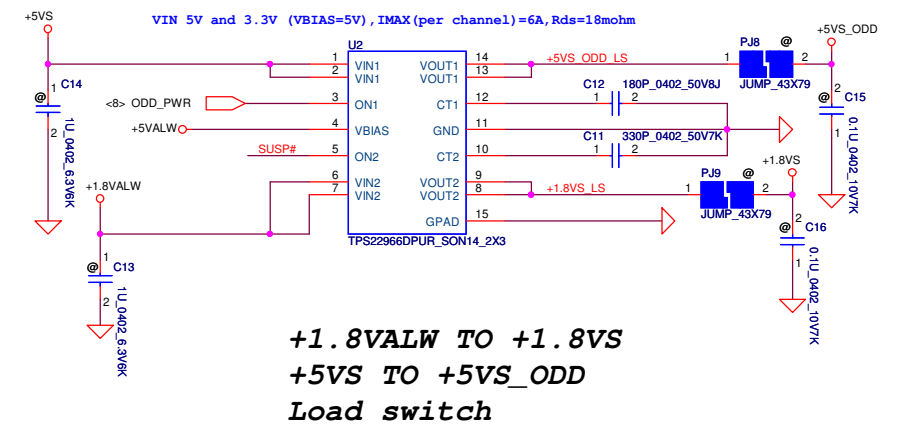
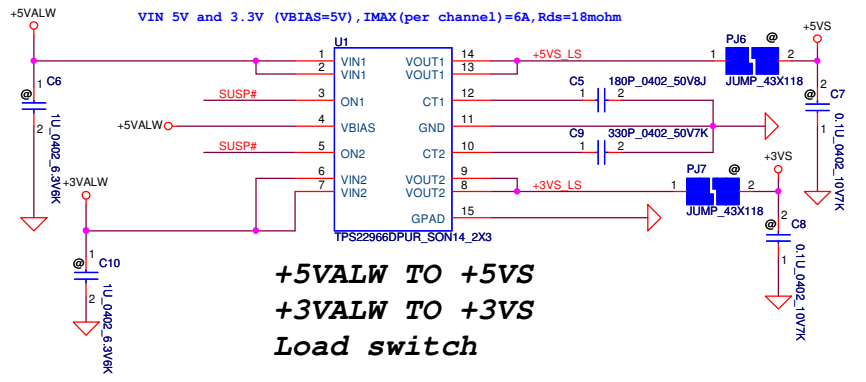
Screw Hole



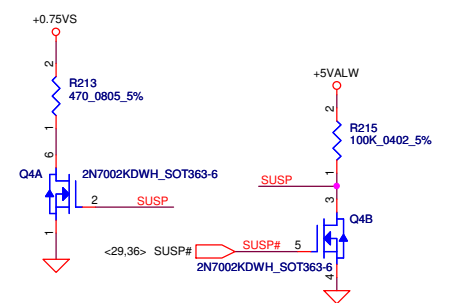
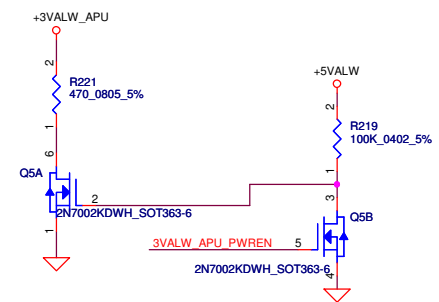
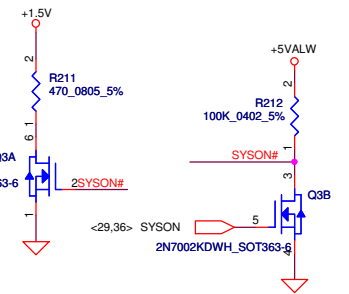
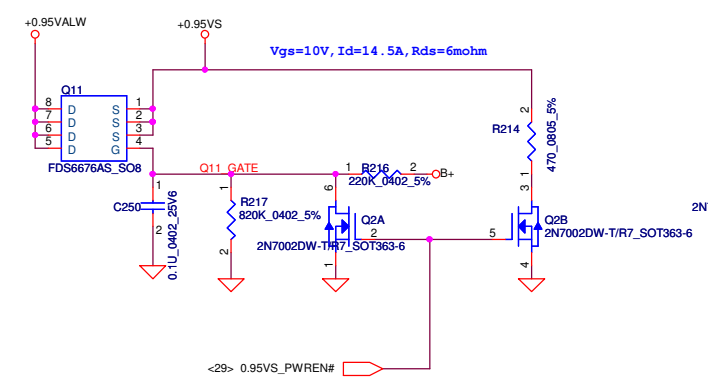
ISPD



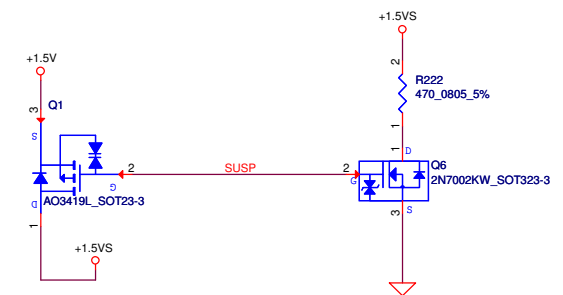
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Issued Date		2012/09/27		Deciphered Date		2015/09/27		Title			
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						Size		Document Number		Rev	
						LA-9868P		0.2			
						Date:		Wednesday, January 23, 2013			
						Sheet		30 of 41			



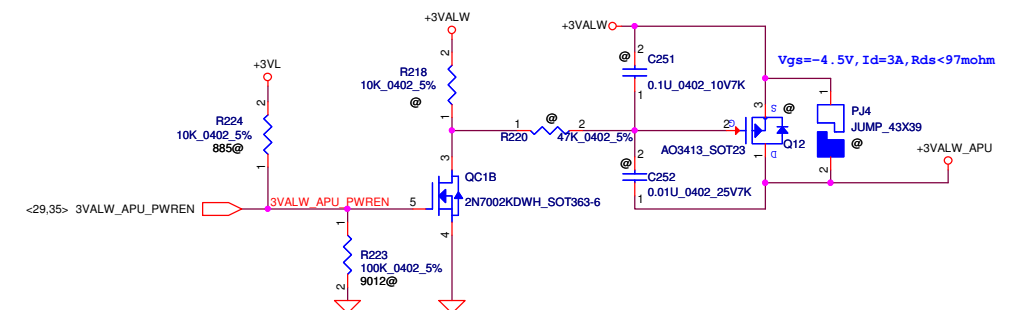
+0.95VALW to +0.95VS



+1.5V to +1.5VS



+3VALW to +3VALW_FCH

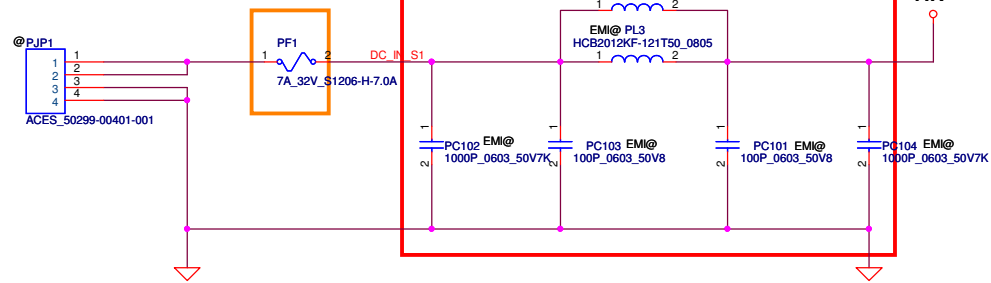


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					LA-9868P	0.2
				Date	Wednesday, January 23, 2013	Sheet 31 of 41

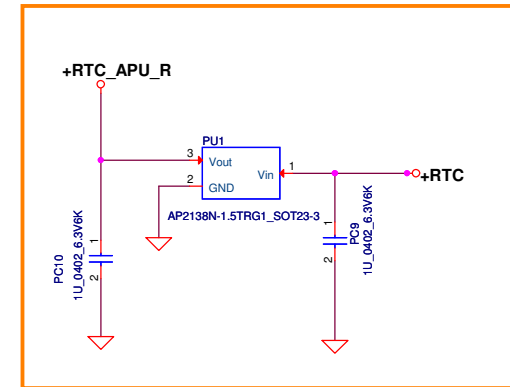
EMI Part (47.1)

Other component (37.1)

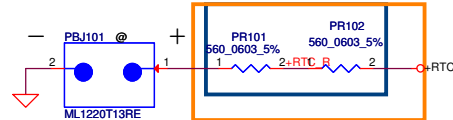
A51 need add fuse



For RTC (38.2)

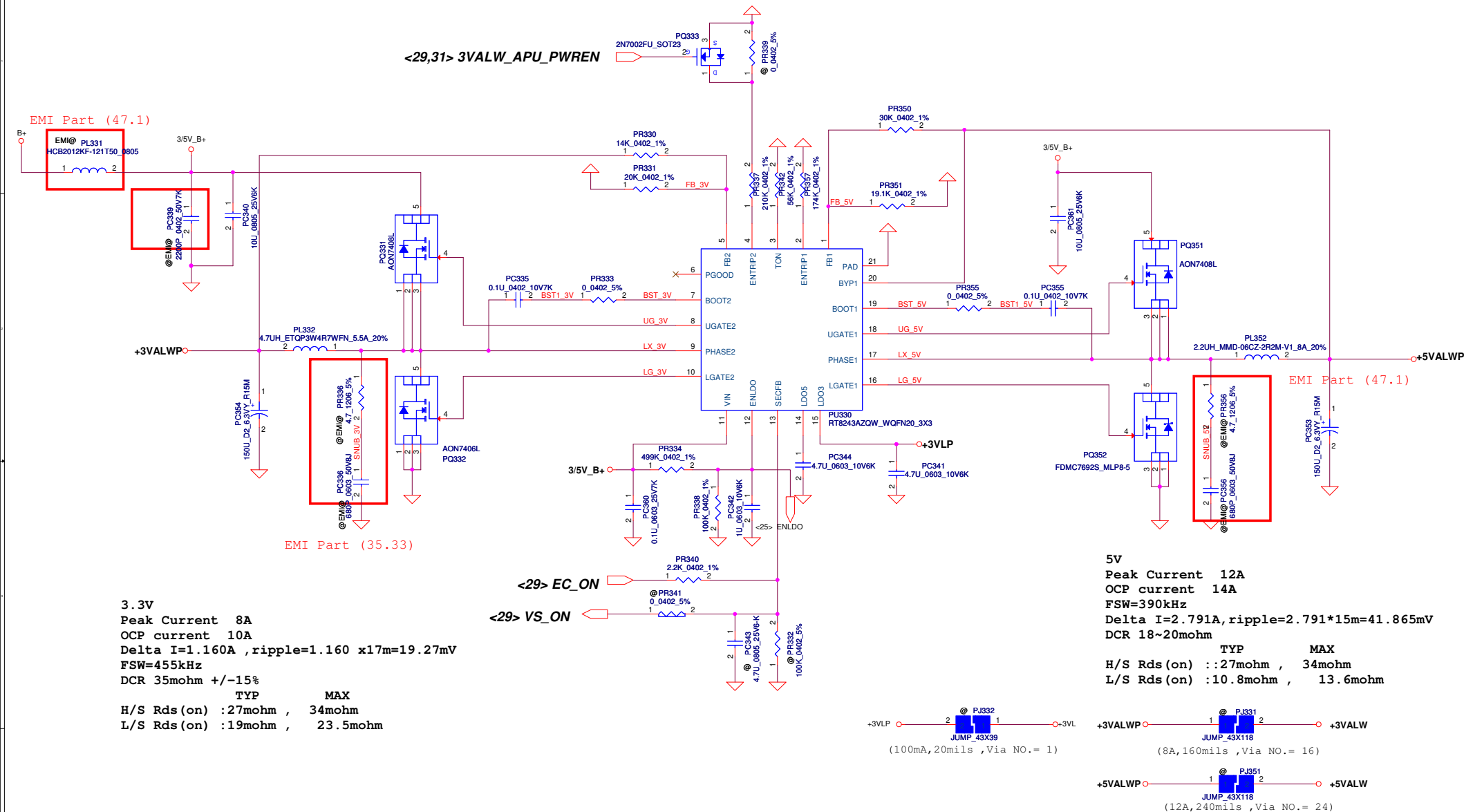


For ML1220 RTC (38.2)

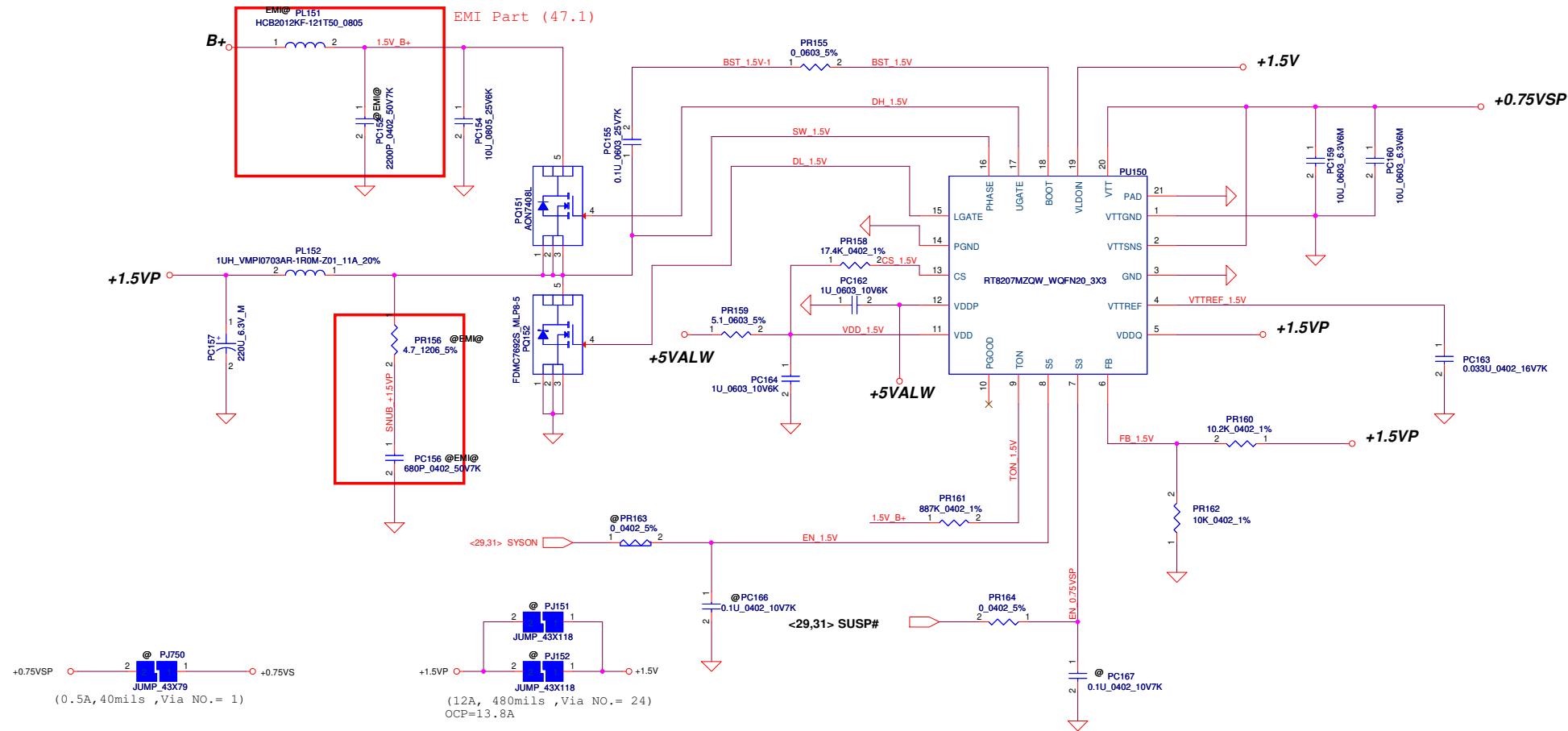


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title
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Date:				Rev 0.2
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<29,31> 3VALW_APU_PWREN



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Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	
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				Sheet 35 of 41	



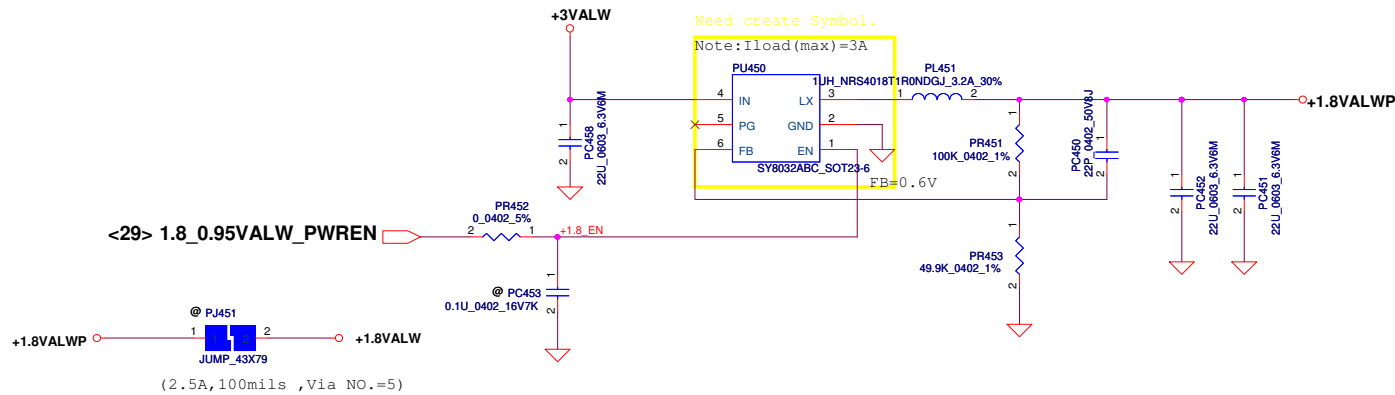
1.5V
Peak Current 12A
OCP current 13.38A
FSW=500kHz
DCR 8.3 ~ 10mohm
TYP MAX
H/S Rds (on) :27mohm , 34mohm
L/S Rds (on) :10.8mohm , 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title	1.5VP/0.75VSP/1.8VSP
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				Date:	Rev 0.2
				Sheet 36 of 41	

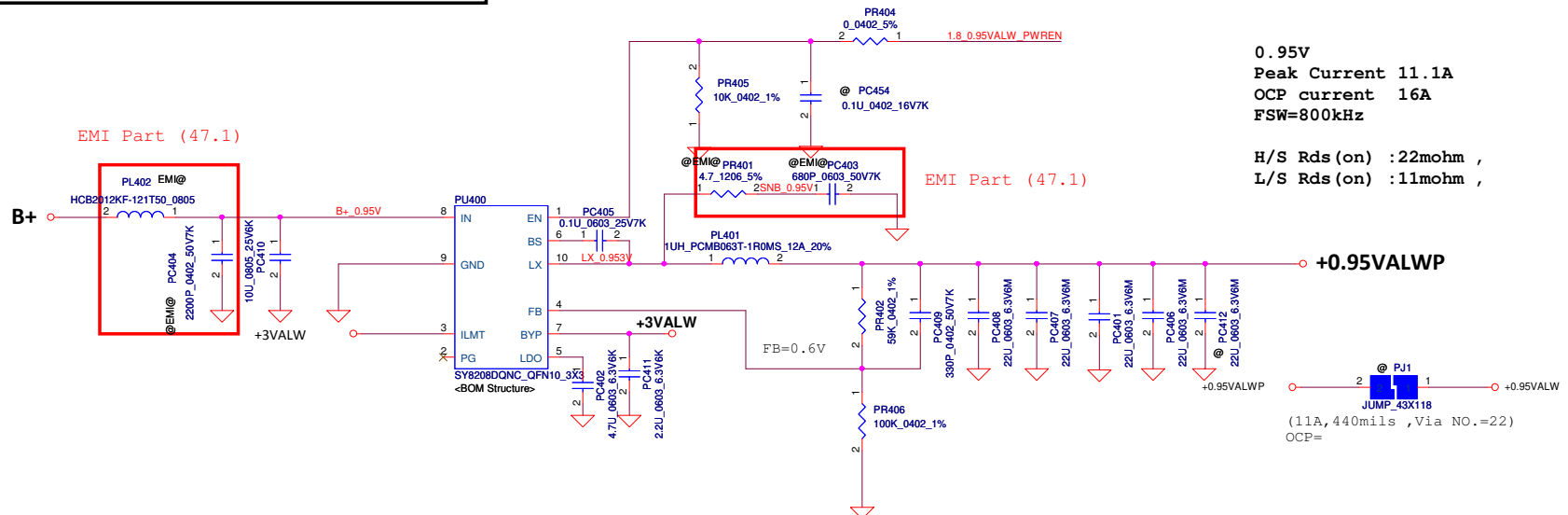
```
1.8V controller (35.15), Support component (35.16)
```



1.8V
Peak Current 2.5A
OCP current 3.5A
FSW=800kHz

H/S Rds (on) : 100mohm ,
L/S Rds (on) : 80mohm ,

0.95V controller (35.5), Support component (35.6)

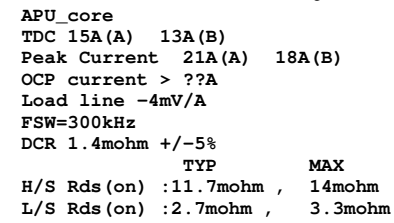


0.95V
Peak Current 11.1A
OCP current 16A
FSW=800kHz

H/S Rds (on) : 22mohm ,
L/S Rds (on) : 11mohm ,

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Title +1.8VALWP/+0.95VALWP		
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				Custom	LA-9868P	0.2
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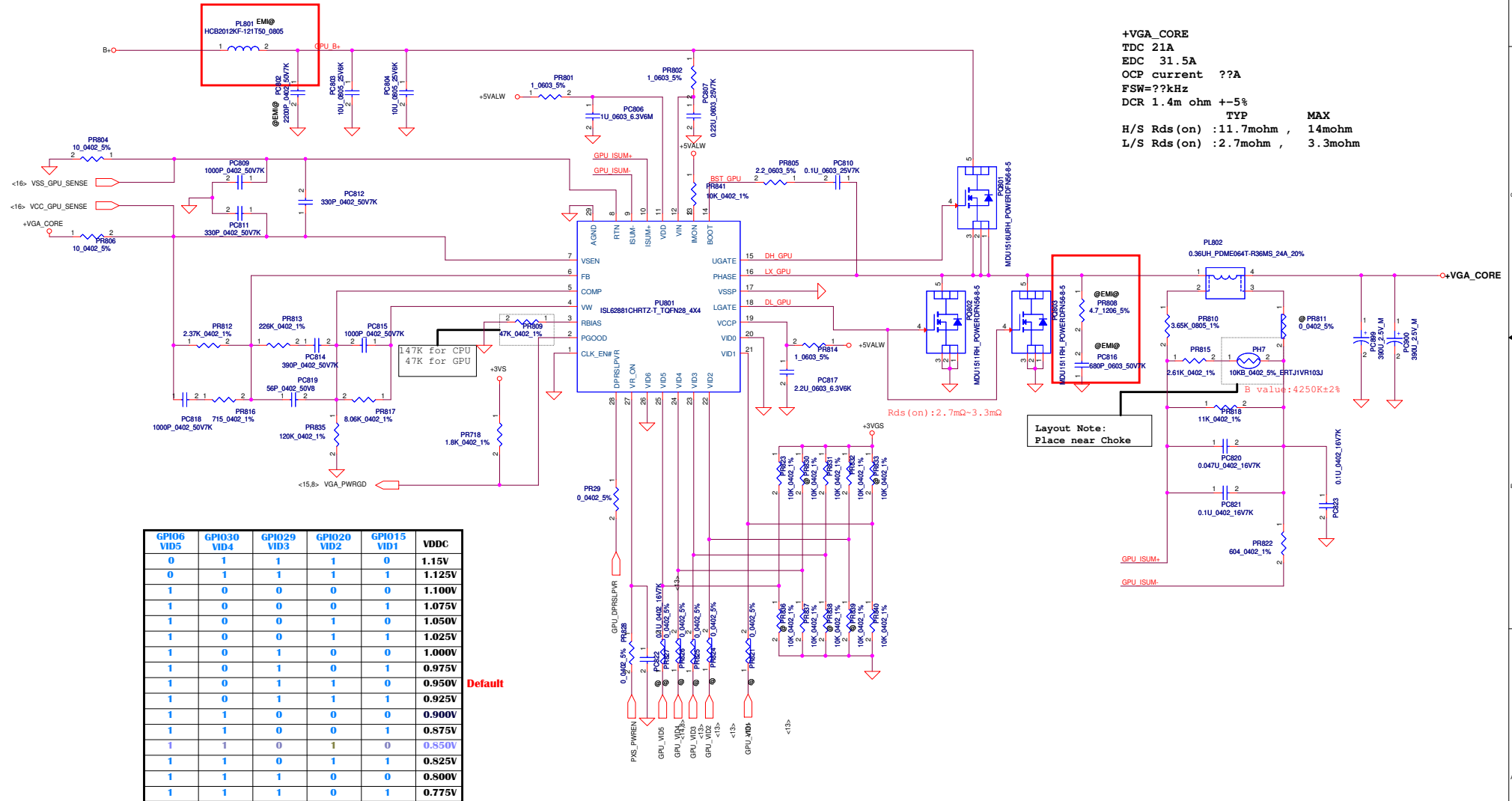
EMI Part (47.1)



Security Classification		Compal Secret Data		Compal Electronics, Inc. +CPU CORE/VDDNBP	
Issued Date	2012/09/27	Deciphered Date		Title	
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				Date: Wednesday, January 23, 2013	Sheet 38 of 41

VGA controller (43.1),Driver (43.2) Support component (43.3)

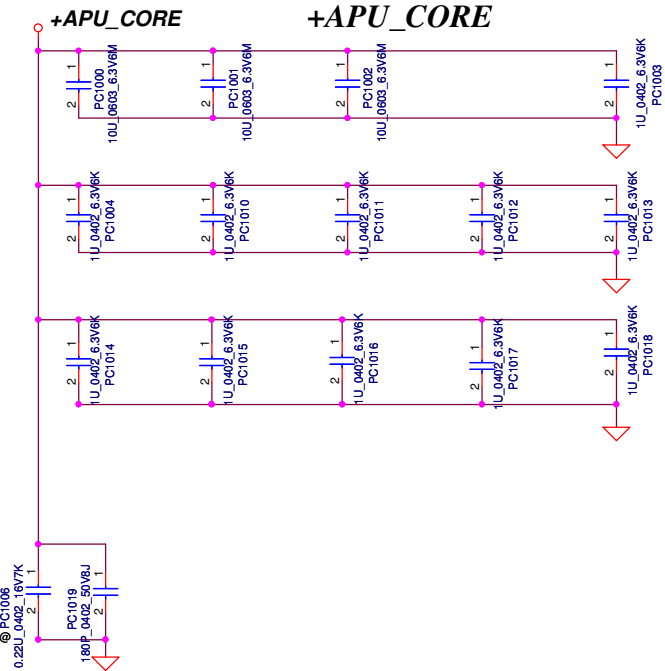
EMI Part (47.1)



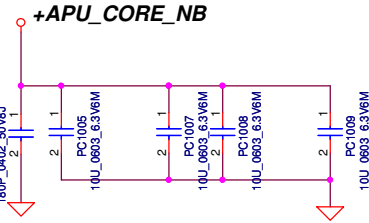
+VGA_CORE
TDC 21A
EDC 31.5A
OCP current ??A
FSW=??kHz
DCR 1.4m ohm +-5%
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

Layout Note:
Place near Choke

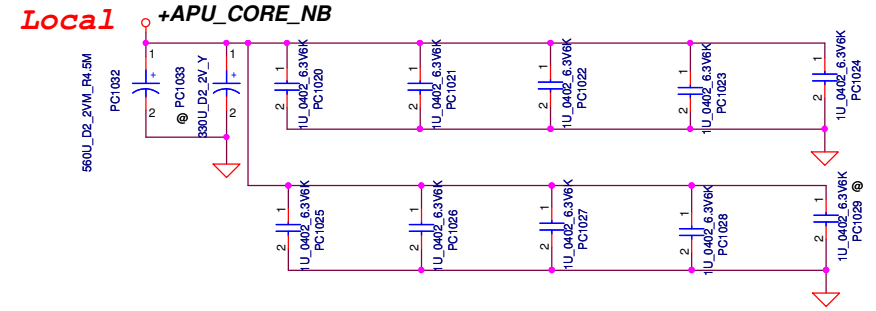
CPU_Core output CAP (Including MLCC) 36.4



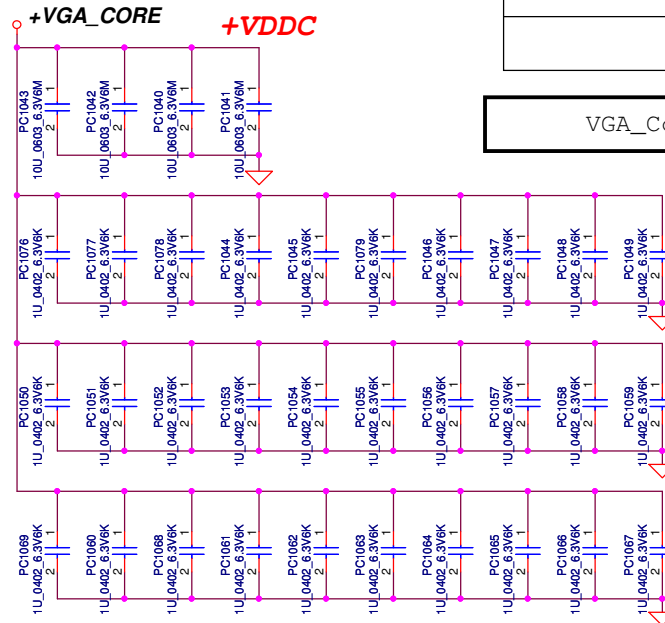
+APU_CORE_NB



GFX output CAP (Including MLCC) 36.5



+VGA_CORE



VGA_Core output CAP (Including MLCC) 43.9

kabini	560uF*4.5m	10uF (0603)	1u (0402)	0.22uF	180P (0402)
VDD	2	3	11		1
VDD_NB	1	4	9		1

HW PIR (Product Improve Record)

VNKAE LA-9868P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

Item	Page	Date	Request	Solution
1	P24	2012/12/5a	Co-lay 14640 S&C IC	Add CHG_PWR_GATE# to pin1 of UR4 and connect to pin82 of UB1
2	P29	2012/12/5a	Co-lay 885 EC and change common pin	Change 1.8_0.95VALW_PWREN form pin71 to pin127.
3	P29	2012/12/5a	Co-lay 885 EC and change common pin	Change USB_EN#0 from pin84 to pin23.
4	P17	2012/12/5a	update X76 setting table	
5	P24	2012/12/5a	Co-lay 14640 S&C IC	Change power rail of QR1 to +3VALW
6	P08	2012/12/5a	Co-lay 14640 S&C IC	SLP_CHG_CB0, SLP_CHG_CB1 PU to +1.5V(MAXIM IC VIH=1.4V)
7	P13	2012/12/5a	PN error	Change PN of CV21 to SE00000V280
8	P31	2012/12/12a	For +1.5VS power rail	Add Q1(SB00000VG00) for switch +1.5VS powe rail to HDA link used
9	P09	2012/12/12a	For +1.5VS power rail	Change pin.AL10,AL11 from +3VS_APU to +1.5VS
10	P26	2012/12/12a	For +1.5VS power rail	Change pin.9 from +3VS to +1.5VS to HDA link used
11		2012/12/12a	update power circuit	
12	P24	2012/12/12b	Remove +3VALW_APU circuit	Change QR1 to +3VALW_APU
13	P14	2012/12/12b	Remove +3VALW_APU circuit	Change RV44 to +3VALW_APU
14	P31	2012/12/12b	Remove +3VALW_APU circuit	Change pin6,7 of U1 to +3VALW_APU; remove +3VALW_APU switch circuit
15	P31	2012/12/12b	Remove +3VALW_APU circuit	Move R224, R223 to P.29 LPC-EC-KB9012
16	P10	2012/12/13a	For common design	Change CD2, CD4 to @; remove CD19,CD17,CD15
17	P11	2012/12/13a	For common design	Change CD22,CD24 to @; remove CD35,CD37,CD42; change CD25,CD26,CD27,CD28 to 0.1uF
18	P31	2012/12/13a	+3VALW_APU switch circuit to BTO	Change R218,R220,C251,C252,Q12 to @
19	P24	2012/12/17a	Remove +3VALW_APU circuit	Change QR1 to +3VALW and reverse D and S termination
20	P14	2012/12/17a	Remove +3VALW_APU circuit	Change RV44 to +3VALW
21		2012/12/17a	update power circuit	
22		2012/12/18a	update power circuit	
23	P11	2012/12/18b	For common design	Add RD5,RD6,RD7,RD8, RD9 to follow DDR schematic common design
24	P31	2012/12/18b	For +1.5VS power rail	Change gate of P-MOSFET from +3VS to SUSP
25	P27	2012/12/18b	For PRD request	Add RA2,RA3 to PU SPK_DET0, SPK_DET1 which connect to GPIO61, GPIO62 of APU
26	P30	2012/12/20a	For ME request	Change H9,H16 from NPTH to PTH
27	P31	2012/12/20a	For power discharge circuit	Add R221, R219, Q5 to +3VALW_APU discharge circuit
28	P07	2012/12/20a	Vendor recommand	Change C22,C23 from 15pF(SE071150J80) to 5.6pF(SE07156AD00)
29		2012/12/20b	update power circuit	
30	P29	2012/12/20c	For 885 common	Exchange pin.107 and pin.127
31	P31	2012/12/22a	For power discharge circuit	Add Q6 and R222 to discharge +1.5VS
32	P08	2012/12/22a	For common design	Change PW_CLEAR# from GPIO49 to GPIO50 and enable internal PU
33	P06	2012/12/22a	For +HDMI_5V_OUT leakage	Remove DC4 and change netname from HDMI_HPD_D to HDMI_HPD
34	P08	2012/12/22a	For +HDMI_5V_OUT leakage	Add QC2 and reserve RC132 to Level Shift GEVENT10
35	P08	2012/12/22a	Change part name	Change QC5530 to QC3
36	P30	2012/12/22a	Change part name	Change QC5531 to Q8
37	P21	2012/12/22a	For +HDMI_5V_OUT leakage	Add RY3 to PU HDMI_HPD to +3VS
38	P12	2012/12/22a	For common design	Change UV13 from +3VGS to +3VS

Title			HW PIR
Size	Document Number	Rev	
B	LA-9868P	0.2	
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