

Compal Confidential

G400S/G500S UMA M/B Schematics Document Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

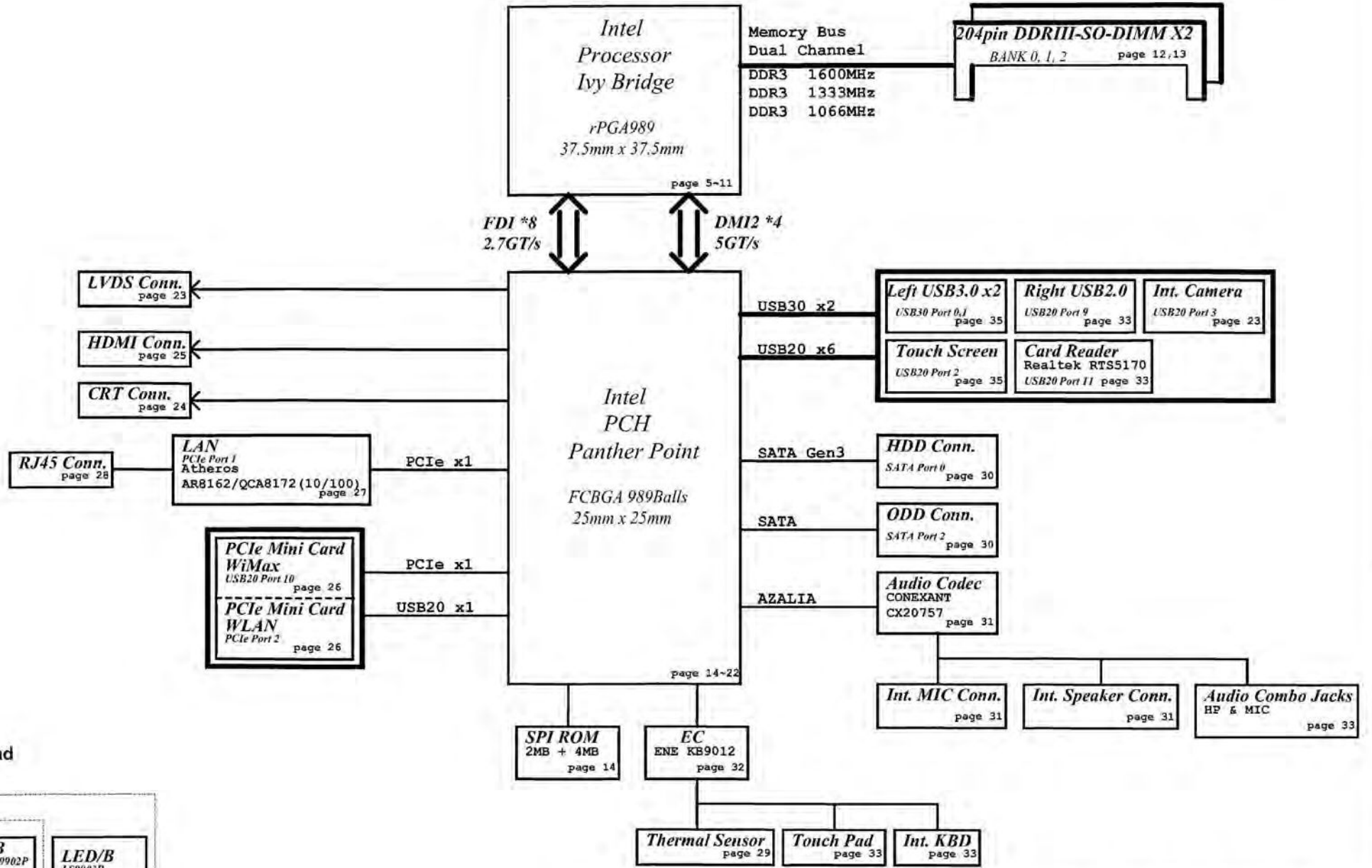
LA-9902P

2013-05-06

REV: 1.0

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Chief River



Sub-board

15"

14"

Power/B LS9902P page 33	LED/B LS9903P page 33
IO/B LS9901P page 33	ODD/B LS9904P page 30

Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+V1.05S_VCCP
				+VCC_CORE
				+VGA_CORE
				+VCC_GFXCORE_AXG
				+1.8VS
				+0.75VS
				+1.05VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor	1001 100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	V	X	X	X	X	X	V
SMB_EC_DA2	+3VALW	+3VS_VGA						+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS_VGA		+3VS			+3VS	

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID table for AD channel

Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD
0	0	0 V	0 V	0.300 V	0x00 - 0x0B MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26 DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30 EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) ^{USB3.0}
		1	USB Port (Left Side) ^{USB3.0}
	UHCI1	2	Touch Screen
		3	USB Camera
	UHCI2	4	
		5	
	UHCI3	6	
EHCI2		7	
		8	
	UHCI4	9	USB/B (Right Side USB2.0)
		10	Mini Card(WLAN)
	UHCI5	11	Card Reader
		12	
		13	

BOM Structure Table

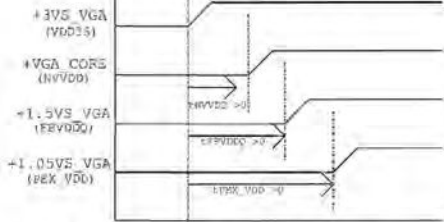
BTO Item	BOM Structure
45 LEVEL	45@
Connector	ME@
For VILG2 (14")	14@
For VILG1 (15")	15@
HDMI	HDMI@
Camera	CMOS@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
10/100 LAN (AR8162L)	8162@
10/100 LAN (QC8172)	8172@
Green clock (DIS sku)	GCLK304@
Green clock (UMA sku)	GCLK244@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Touch Screen SKU	TS@
Optimus SKU	OPT@
UMA SKU	UMA@
PCH (NM70 sku)	NM70@
PCH (HM70 sku)	HM70@
PCH (HM76 sku)	HM76@
VRAM (1000MHz)	1000M@
VRAM (900MHz)	900M@
Unpop	@

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N14x GPIO Pin Definition Table

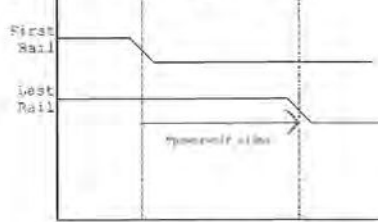
Pin Name	Normal Function	I/O	Functional Description	Default PU/PD
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM_VDD Strap to boot FBVDDIQ
GPIO2-4	Non-support for LCD	O	Panel	100k PD
GPIO5	Reserve			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3D Vision	O	3D Vision L/R signal	100k PD
GPIO8	OVERT	IO	Active Low Thermal Catastrophic Over Temperature	100k PU
GPIO9	ALERT	IO	Active Low Thermal Alert	100k PU
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100k PD
GPIO11	PWM_VID	O	GPU Core VDD PWM control supply overdraw input	
GPIO12	PWR_LEVEL	I	AC power detect or control signal	100k PU
GPIO13	PSI	O	Phase Shedding	PSI 100k PU to enable two phase
GPIO14-19	Non-support for HDA	I	Hot Plug	
GPIO20-21	Reserve			

GPU Power On



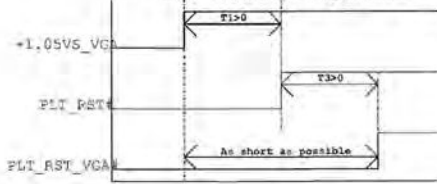
- All power rail ramp up time should be longer than 400ns
- The total time for all rails to rise should be within 500ns
- A power rail may ramp up 30% before the next power rail is sequenced up
- No signal should be applied to the GPU before the power rail is fully ramped.

GPU Power Down

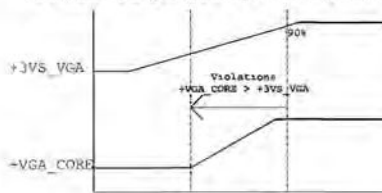


1. All GPU power rails should be turned off within 100ns

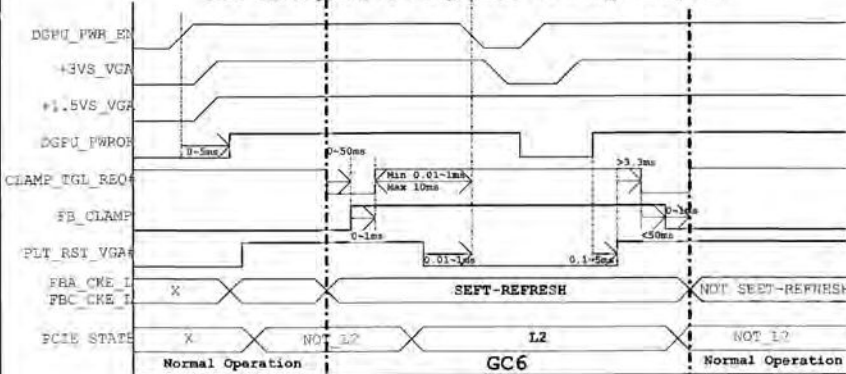
GPU Reset Sequence



Power sequencing violations



GC6 Entry/Exit Sequence Timing Diagram



For N14P-GV2 strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M*16*4 1GB	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14P-GV3	1 GHz	128M*16*4 1GB	MT41J28M16JT-093G-K	R	R	R	R	R	R	R	R
N14P-GV4	1 GHz	128M*16*4 1GB	Hylix H5TQ2G63DFR-NOC	R	R	R	R	R	R	R	R
N14P-GV5	900 MHz	256M*16*4 2GB	Samsung K4W4G1646B-HC11	R	R	R	R	R	R	R	R
N14P-GV7	900 MHz	256M*16*4 2GB	MT41K256M16HA-107G-E	R	R	R	R	R	R	R	R

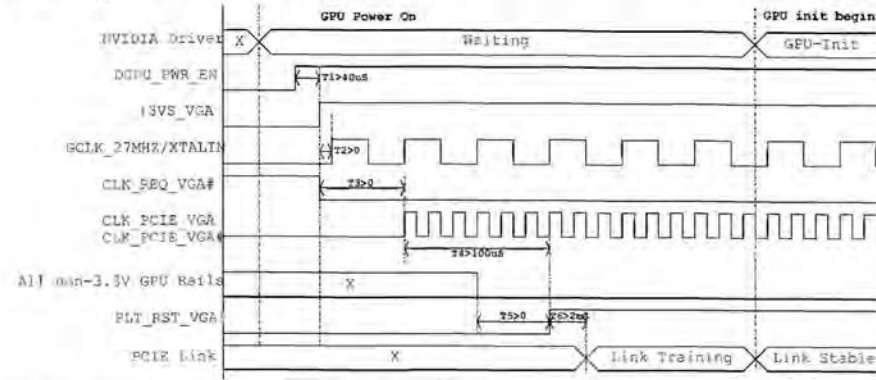
For N14P-GS strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M*16*4 2GB	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14P-GS1	1 GHz	128M*16*4 2GB	MT41J28M16JT-093G-K	R	R	R	R	R	R	R	R
N14P-GS2	1 GHz	128M*16*4 2GB	Hylix H5TQ2G63DFR-NOC	R	R	R	R	R	R	R	R
N14P-GS3	900 MHz	256M*16*4 4GB	Samsung K4W4G1646B-HC11	R	R	R	R	R	R	R	R
N14P-GS4	900 MHz	256M*16*4 4GB	MT41K256M16HA-107G-E	R	R	R	R	R	R	R	R

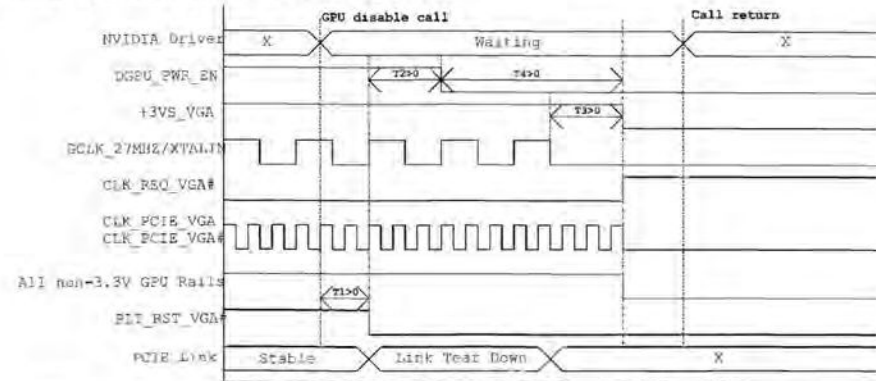
For N14M-GE strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M*16*4 1GB	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14M-GE1	1 GHz	128M*16*4 1GB	MT41J28M16JT-093G-K	R	R	R	R	R	R	R	R
N14M-GE2	1 GHz	128M*16*4 1GB	Hylix H5TQ2G63DFR-NOC	R	R	R	R	R	R	R	R
N14M-GE3	900 MHz	256M*16*4 2GB	Samsung K4W4G1646B-HC11	R	R	R	R	R	R	R	R
N14M-GE4	900 MHz	256M*16*4 2GB	MT41K256M16HA-107G-E	R	R	R	R	R	R	R	R

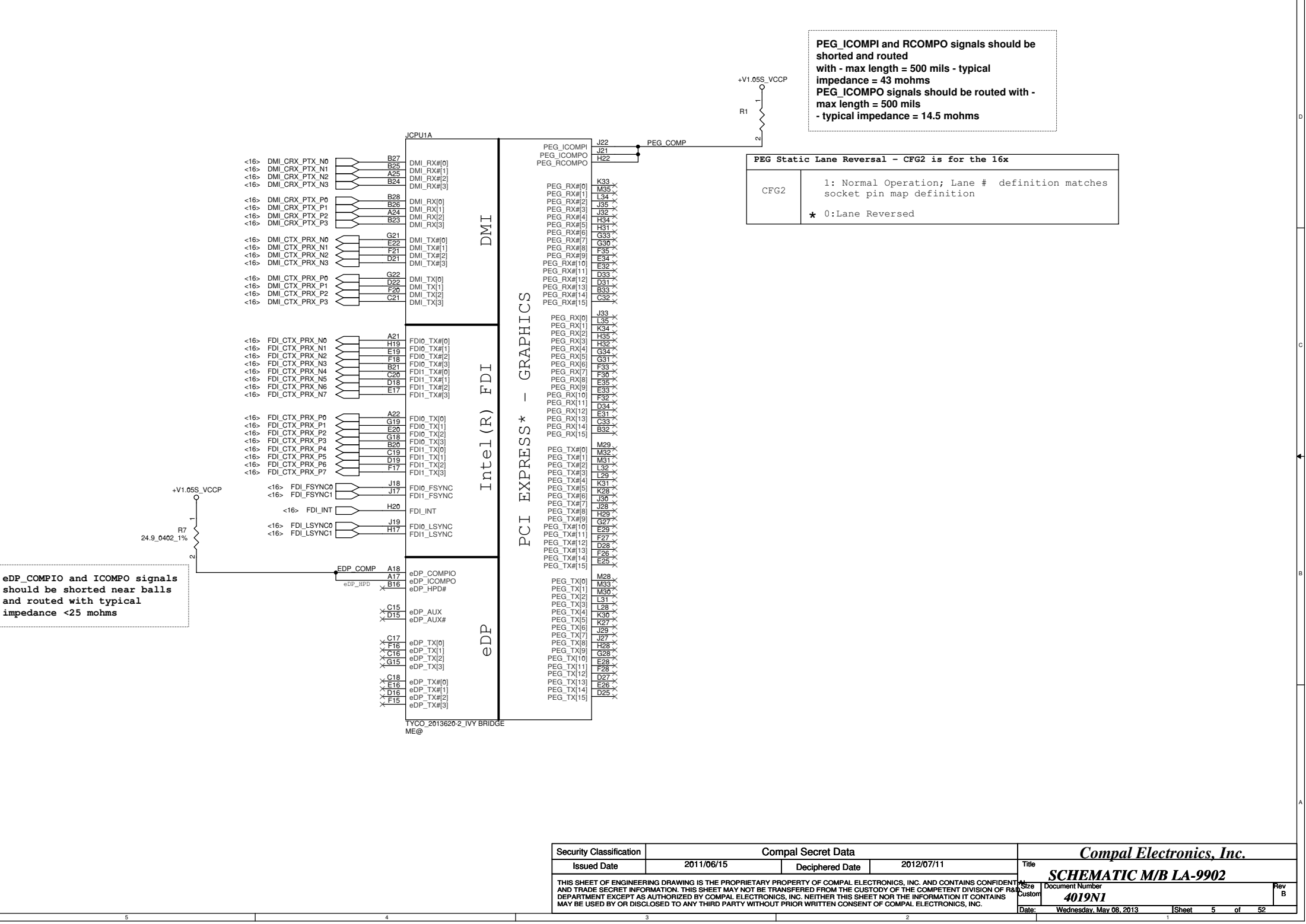
Optimus Typical Power-Up Sequence



Optimus Typical Power-Down Sequence



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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

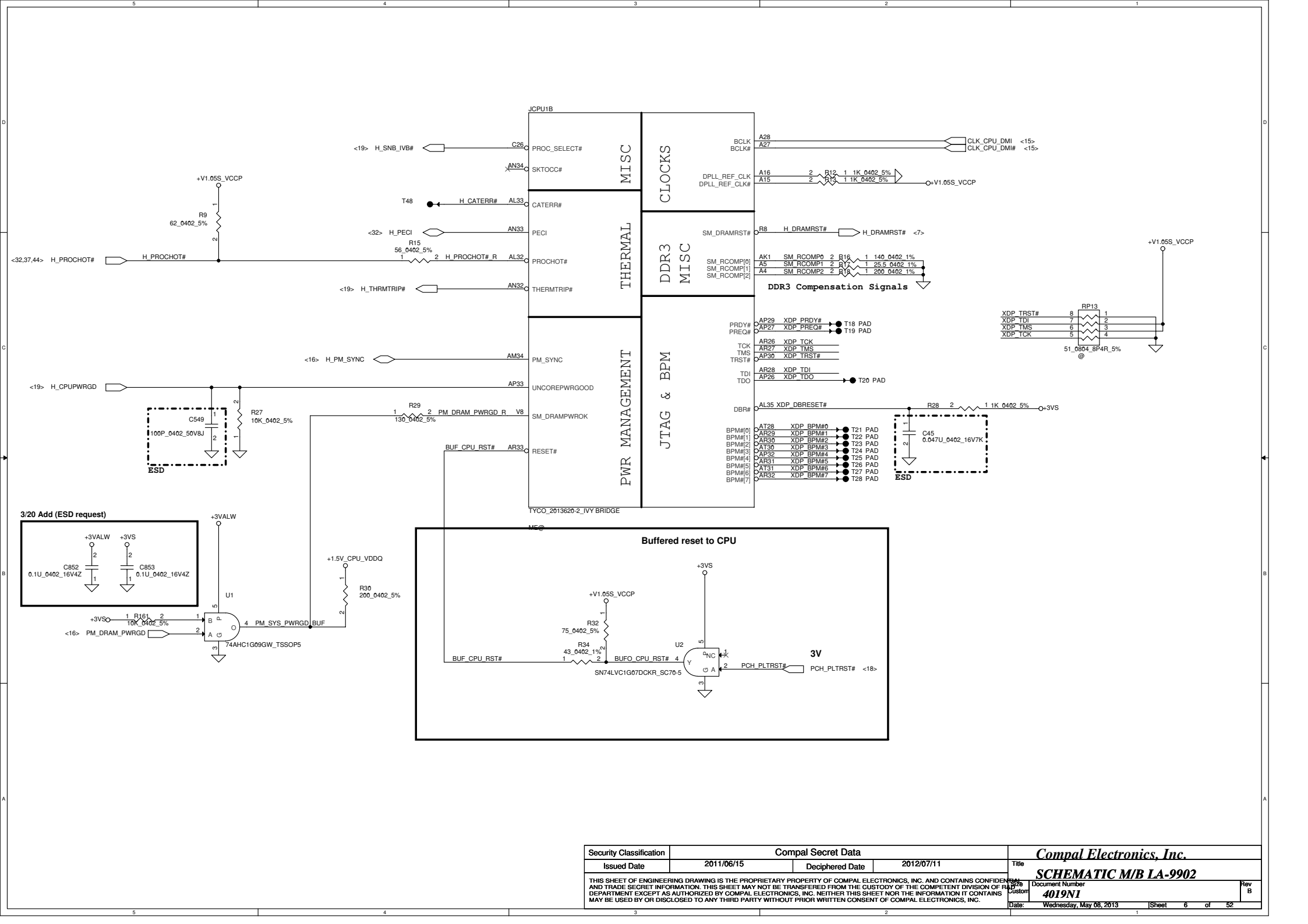
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
*	0: Lane Reversed

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

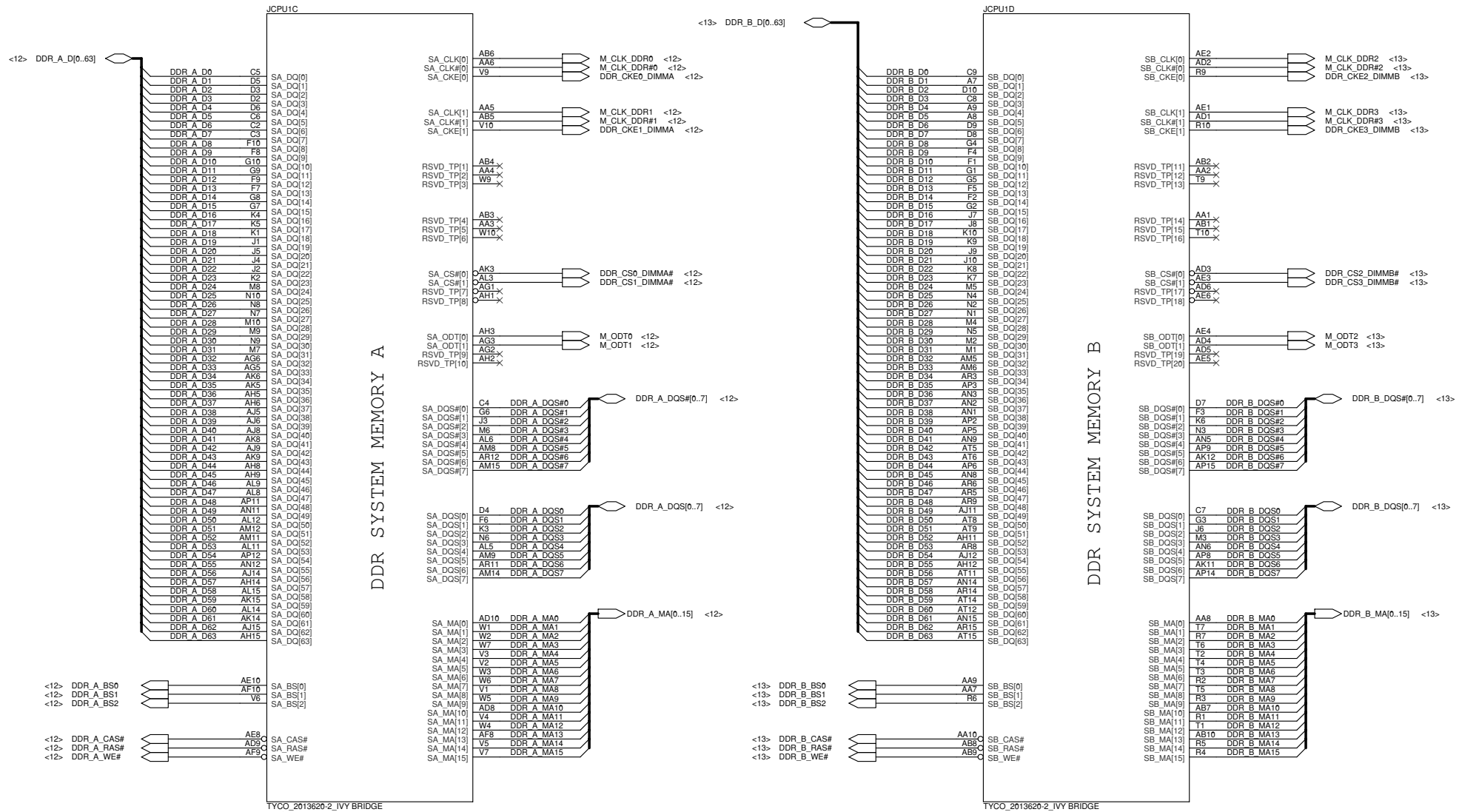
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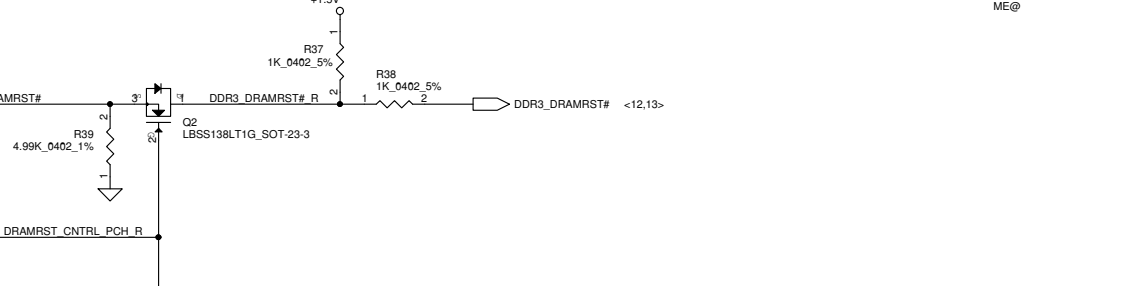


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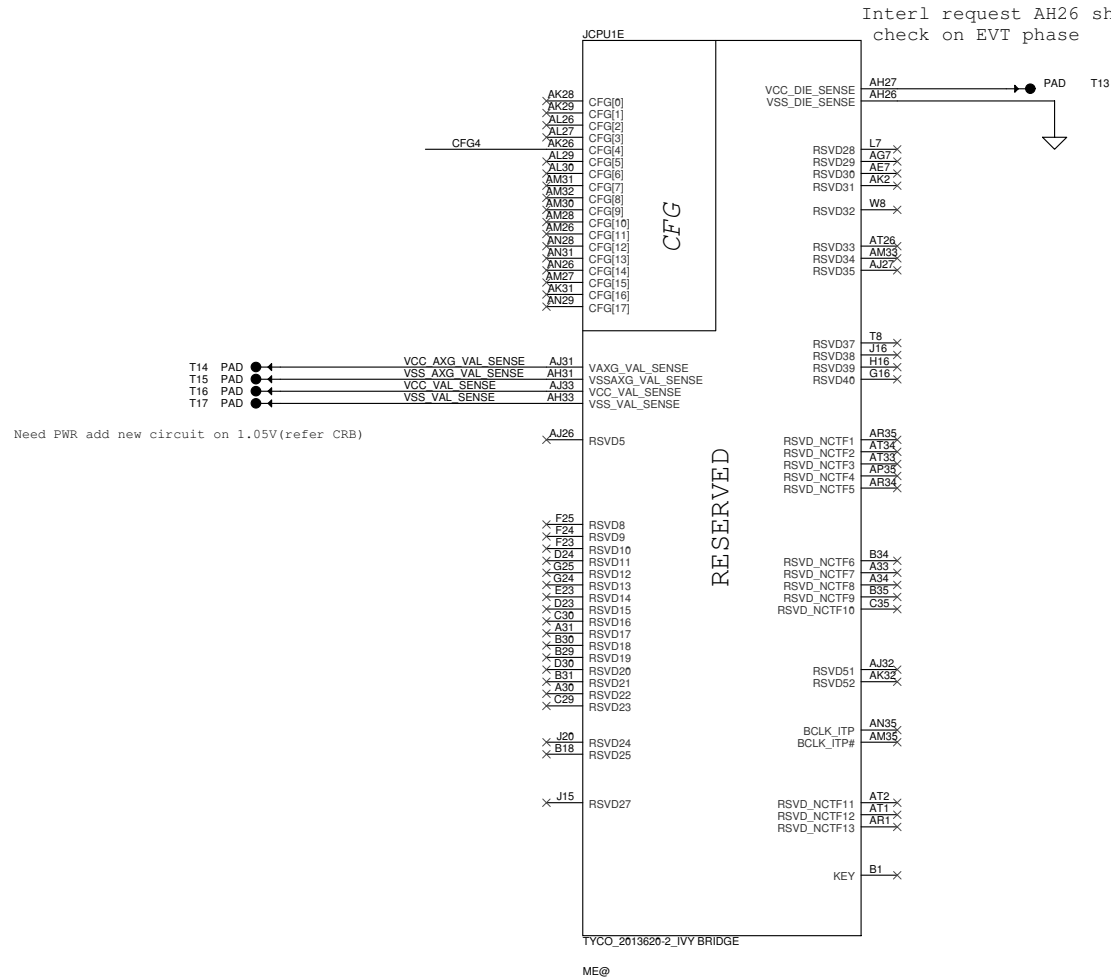
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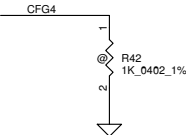
Eiffel used 0.01u
Module design used 0.047u

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CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

POWER

QC=94A
DC=53A

JCPU1F

+V1.05S_VCCP
8.5A

CORE SUPPLY

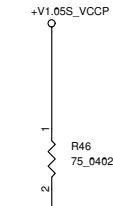
PEG AND DDR

SVID

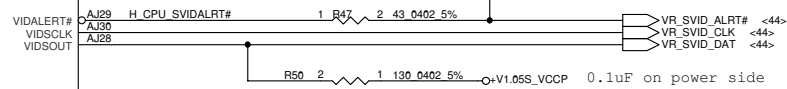
SENSE LINES

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

- AH13 VCCIO1
- AH10 VCCIO2
- AG10 VCCIO3
- AC10 VCCIO4
- Y10 VCCIO5
- U10 VCCIO6
- P10 VCCIO7
- L10 VCCIO8
- J13 VCCIO9
- J12 VCCIO10
- J11 VCCIO11
- H12 VCCIO12
- H14 VCCIO13
- H12 VCCIO14
- H11 VCCIO15
- G14 VCCIO16
- G13 VCCIO17
- G12 VCCIO18
- F14 VCCIO19
- F13 VCCIO20
- F12 VCCIO21
- F11 VCCIO22
- E14 VCCIO23
- E12 VCCIO24
- E11 VCCIO25
- D14 VCCIO26
- D13 VCCIO27
- D12 VCCIO28
- D11 VCCIO29
- G14 VCCIO30
- C13 VCCIO31
- C12 VCCIO32
- C11 VCCIO33
- B14 VCCIO34
- B12 VCCIO35
- A14 VCCIO36
- A13 VCCIO37
- A12 VCCIO38
- A11 VCCIO39
- J23 VCCIO40

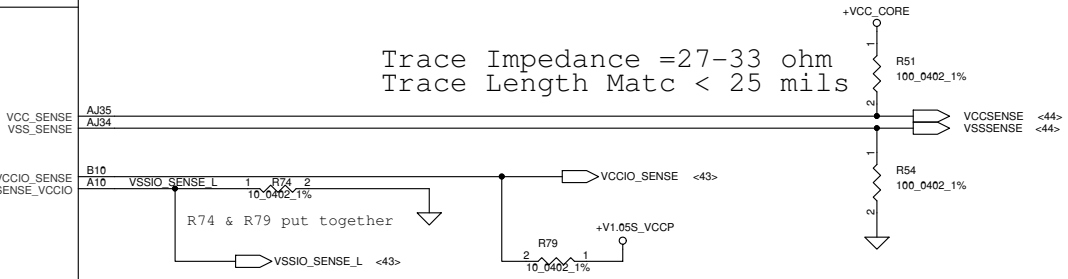


VR_SVID_CLK series-resistors close to VR



VCC_SENCE 100ohm +-1% pull-up to VCC near processor

Trace Impedance = 27-33 ohm
Trace Length Matc < 25 mils

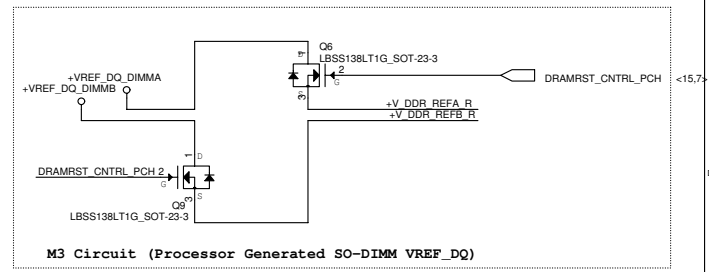
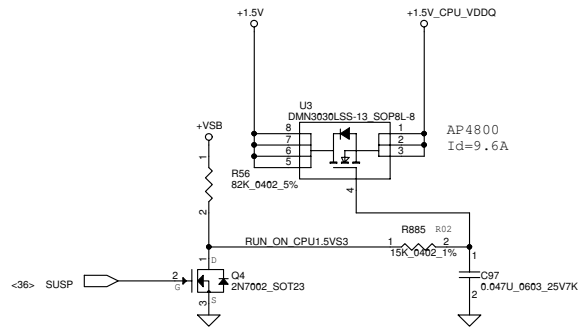


VSS_SENCE 100ohm +-1% pull-down to GND near processor

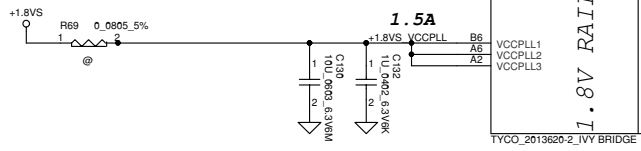
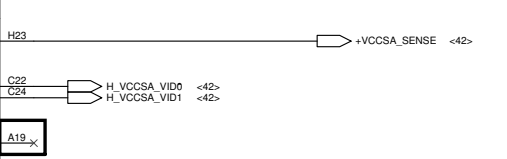
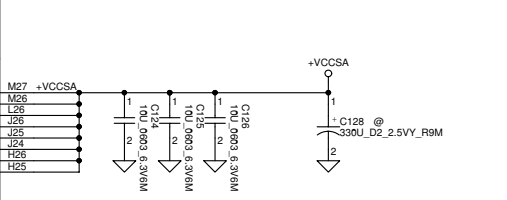
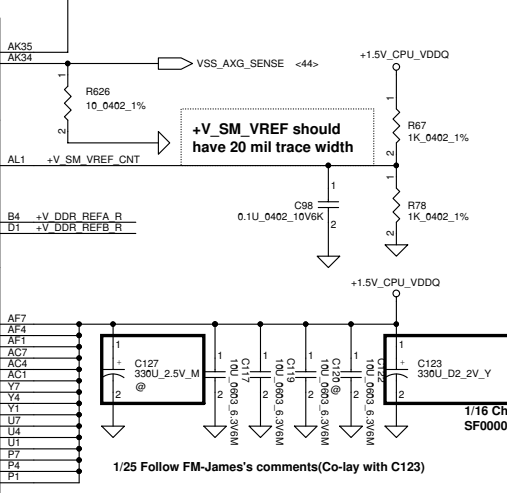
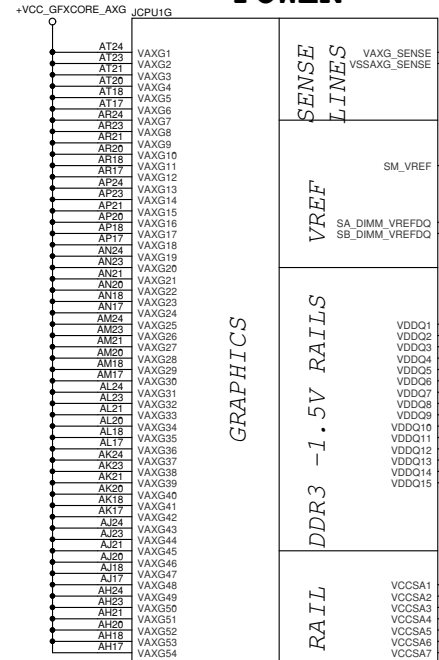
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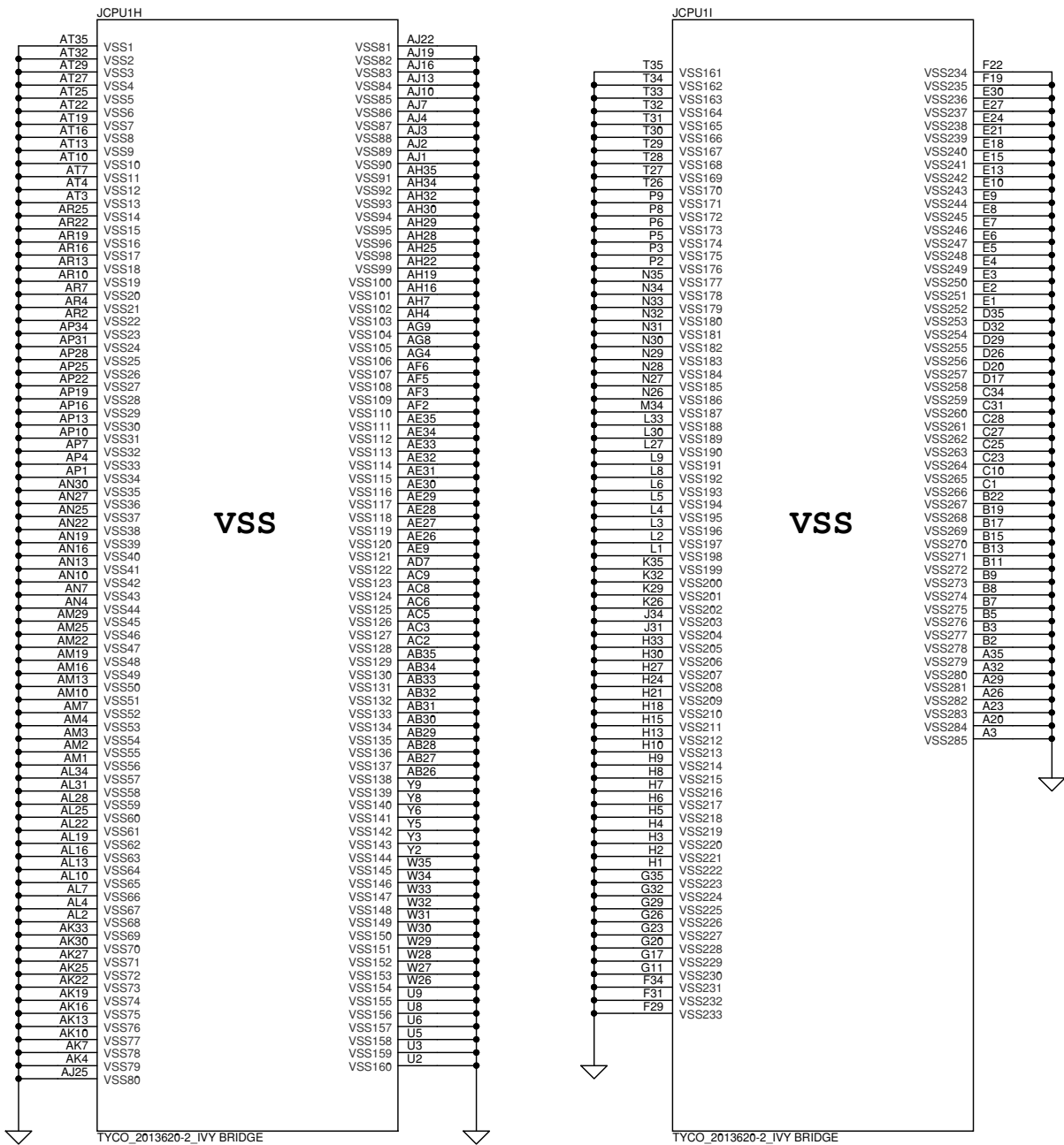


POWER



IVY Bridge drives VCCIO_SEL low
 VCCP_PWRCTRL:0
 Sandy Bridge is NC for A19
 VCCP_PWRCTRL:1

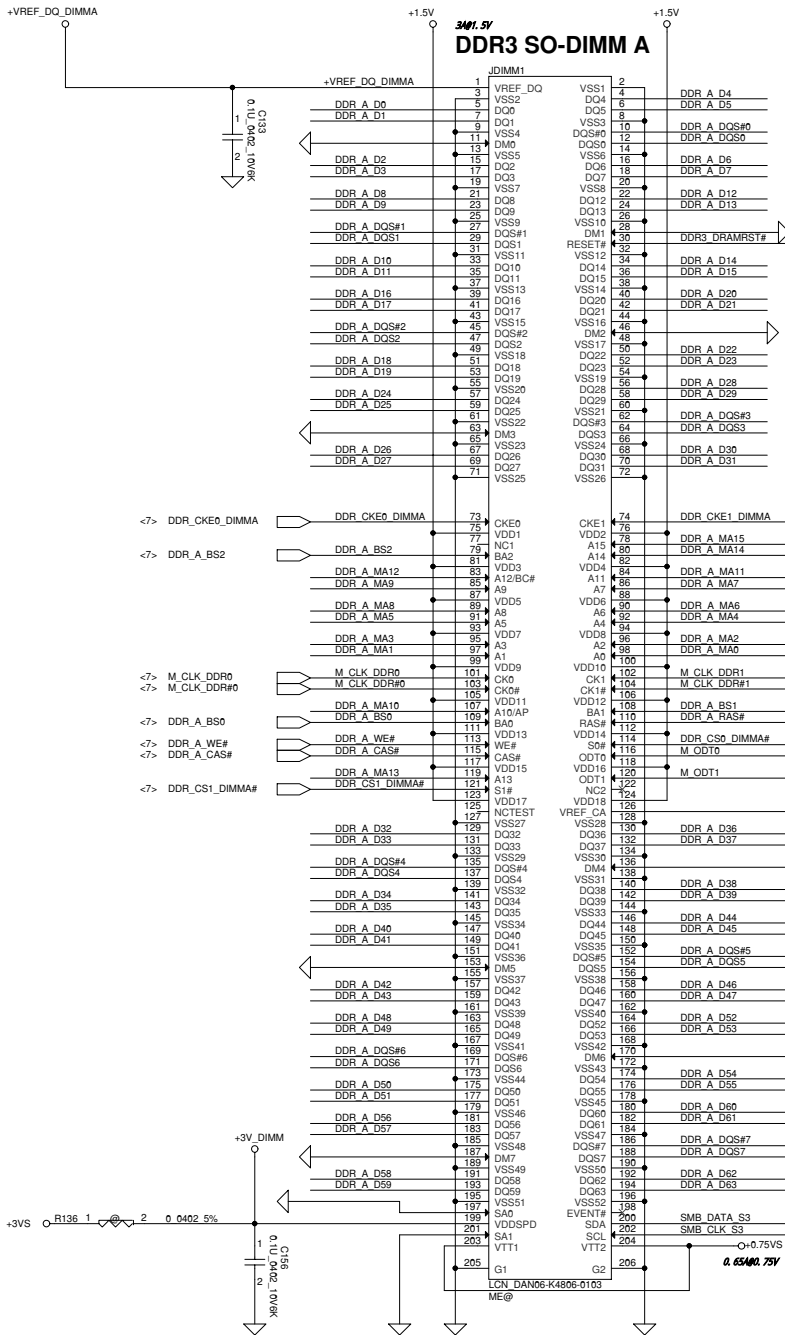
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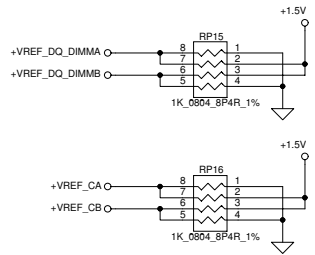
TYCO_2013620-2_IVY BRIDGE
ME@

TYCO_2013620-2_IVY BRIDGE
ME@

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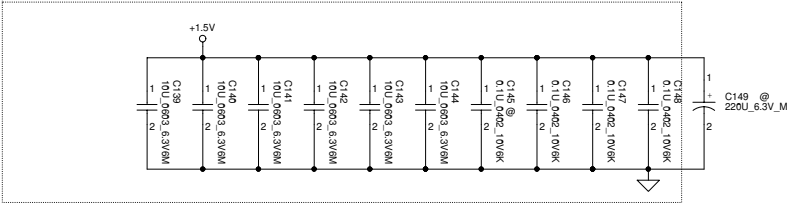


- <7> DDR_A_D[0..63]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_DQS#[0..7]
- <7> DDR_A_MA[0..15]

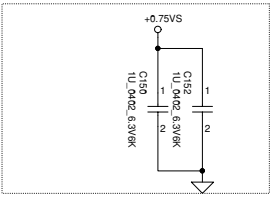


OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



VDDQ (1.5V) =
3*330uF / 12m ohm (TOTAL FOR 2 SO-DIMM#)
6*0603 10uF (PER CONNECTOR)

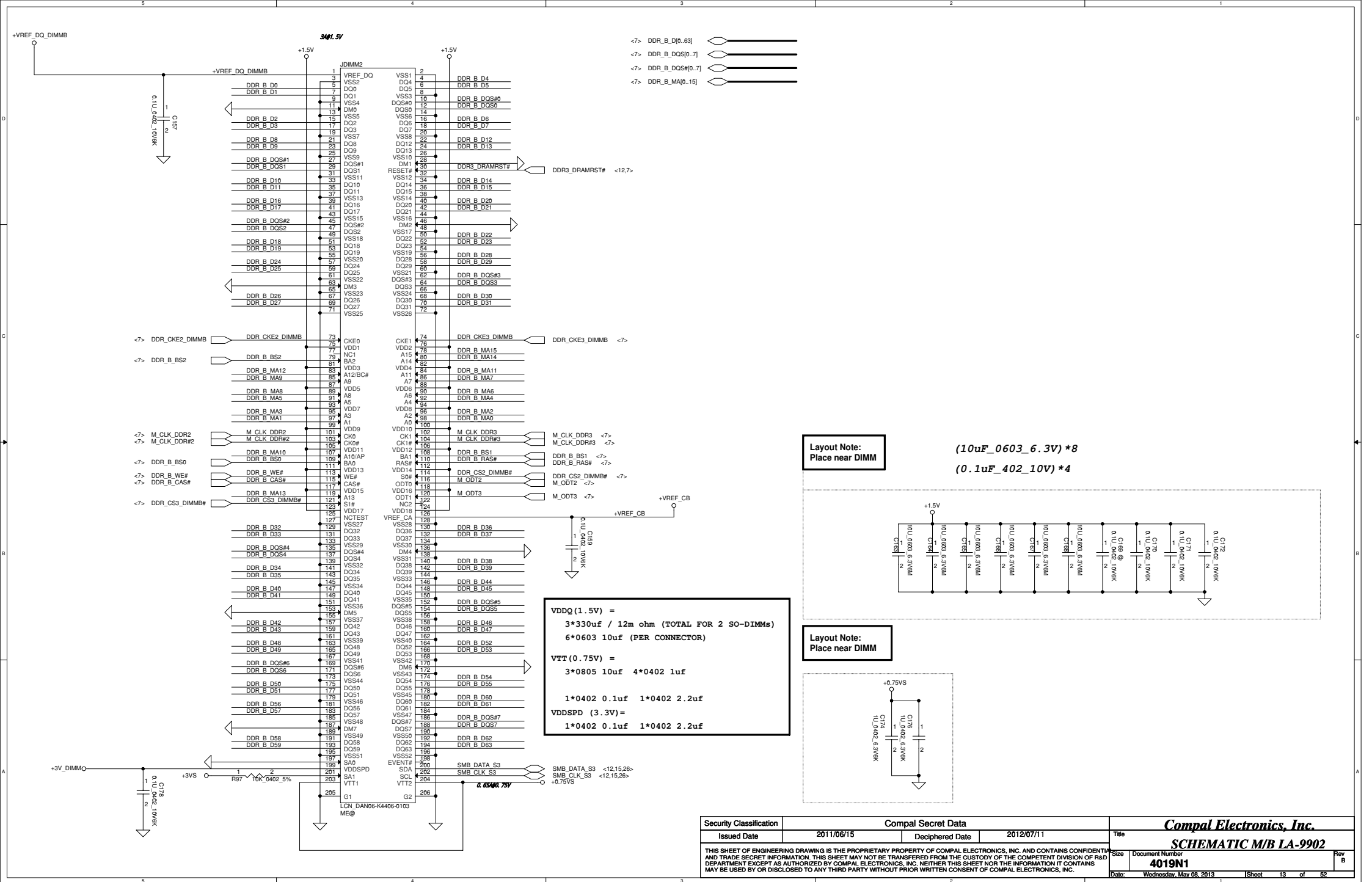
VTT (0.75V) =
3*0805 10uF 4*0402 1uF

VREF =
1*0402 0.1uF 1*0402 2.2uF

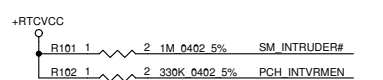
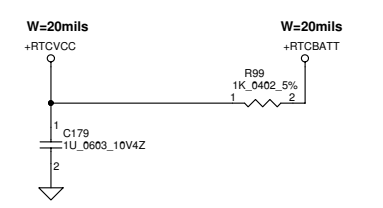
VDDSPD (3.3V) =
1*0402 0.1uF 1*0402 2.2uF

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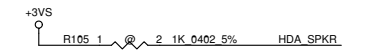
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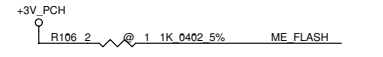
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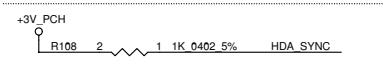
INTVRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



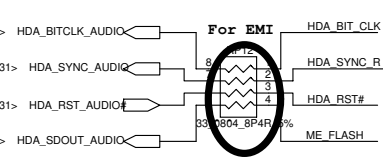
HIGH= Enable (No Reboot)
 * **LOW= Disable (Default)**



* **Low = Disabled (Default)**
High = Enabled (Flash Descriptor Security Override)



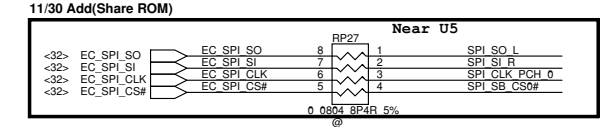
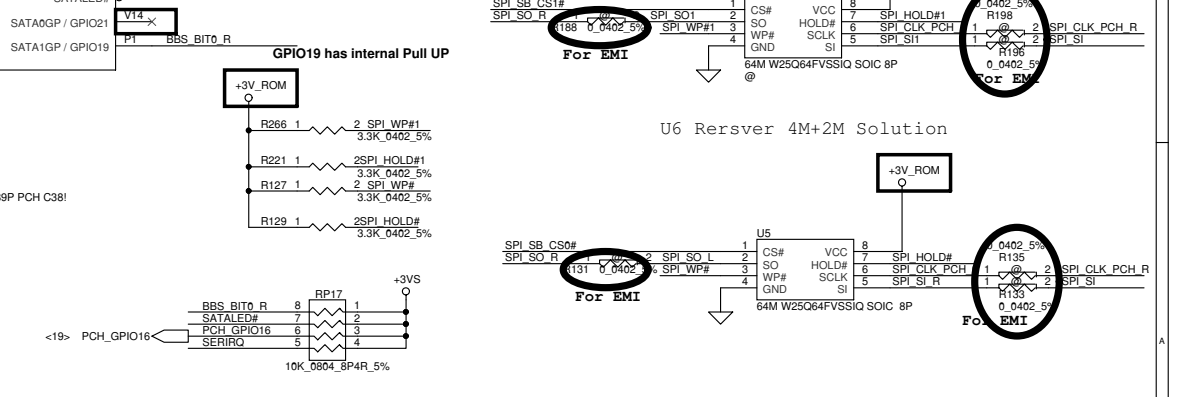
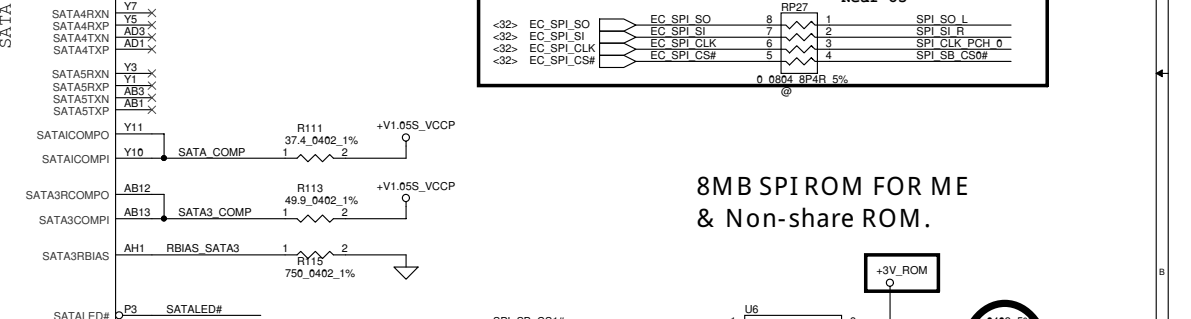
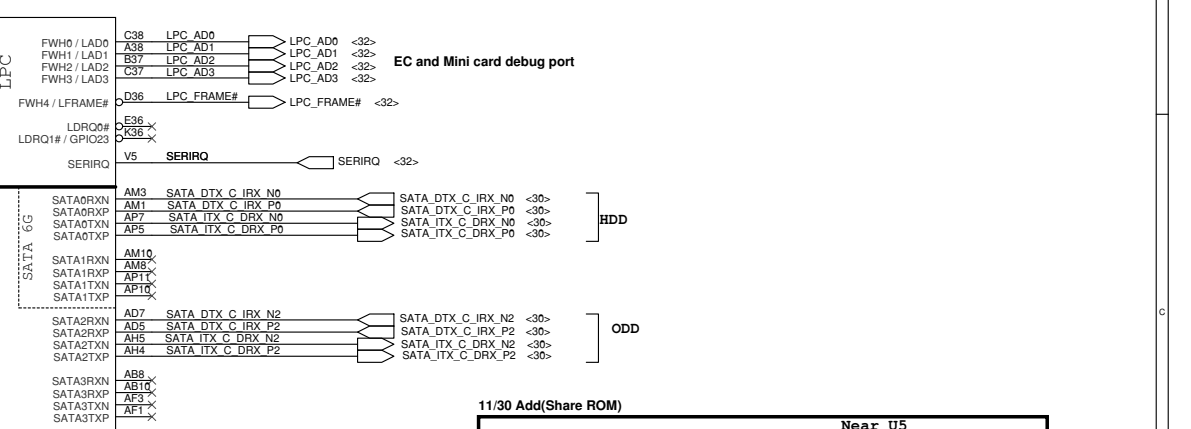
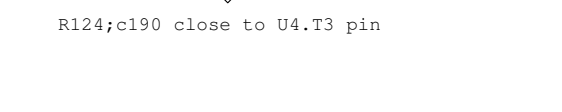
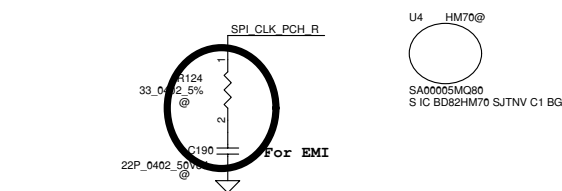
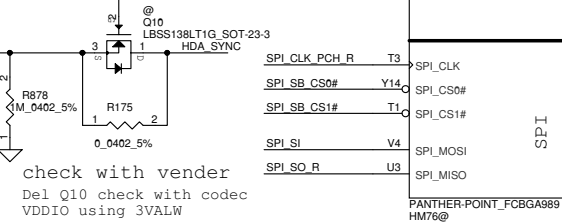
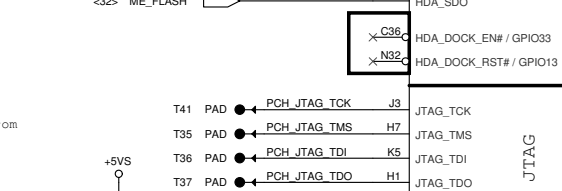
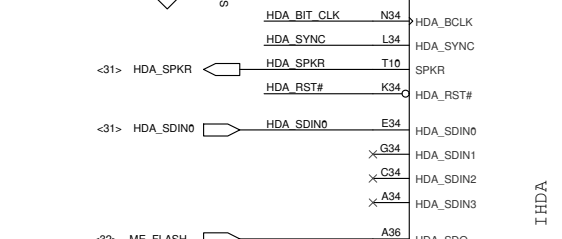
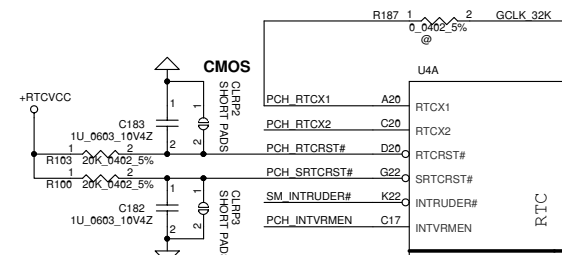
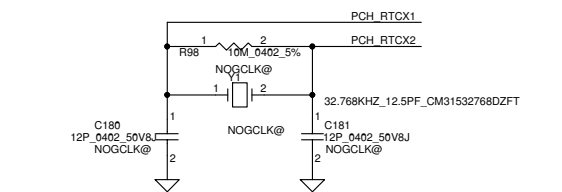
This signal has a weak internal pull-down
 On Die PLL VR is supplied by
 1.5V when sampled high (For mobile only)
 1.8V when sampled low (For Desktop only)
 Needs to be pulled High for Chief River platform



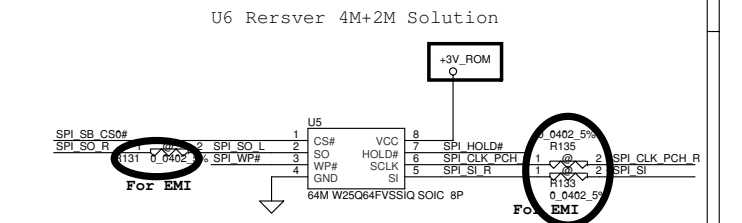
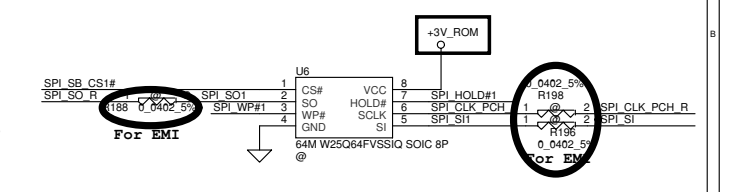
check with vender
 Del Q10 check with codec
 VDDIO using 3VALW



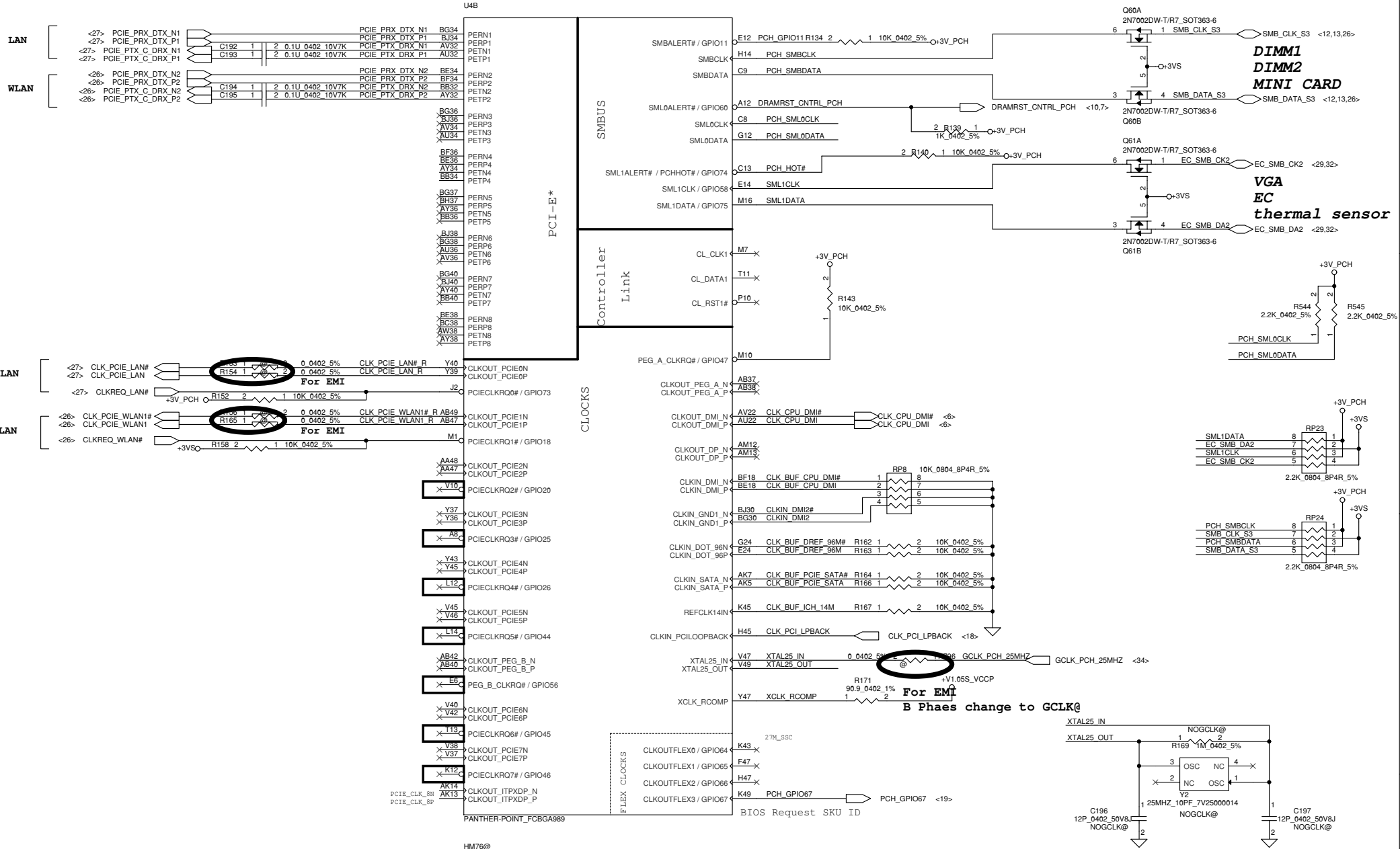
R124;c190 close to U4.T3 pin



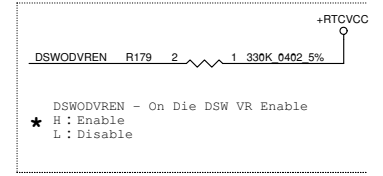
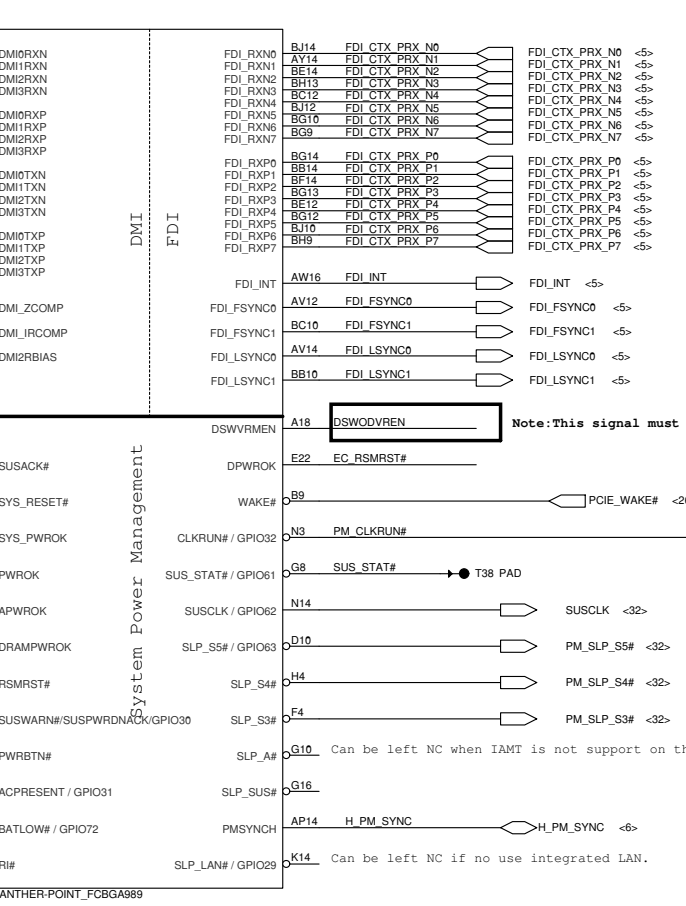
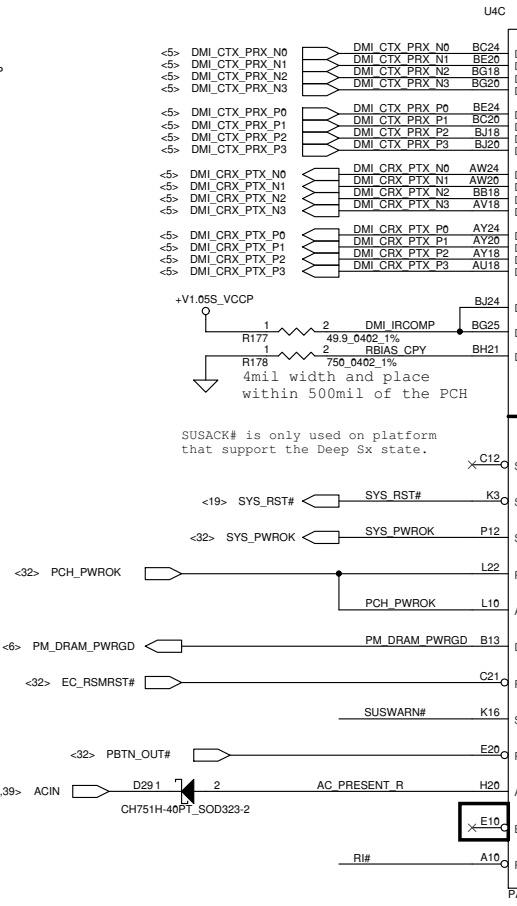
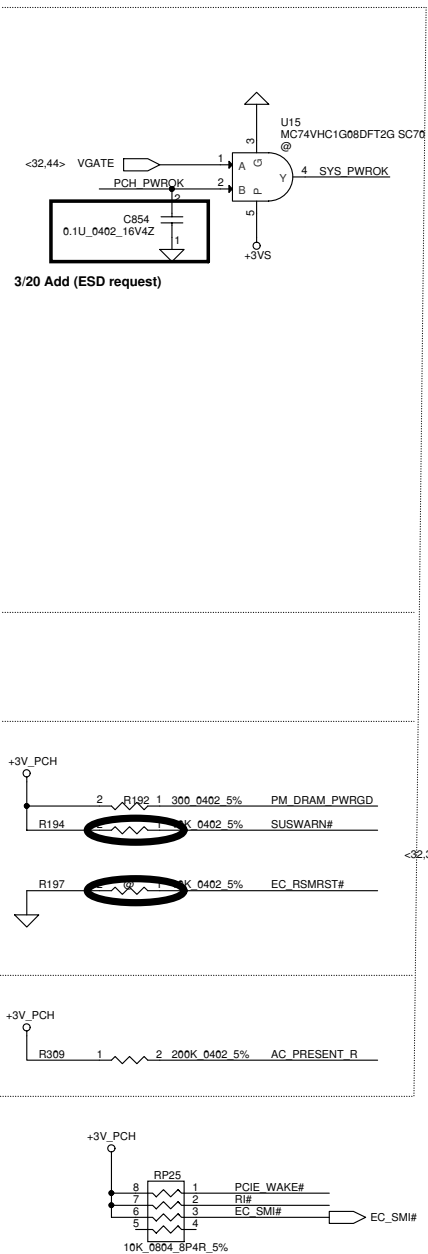
8MB SPIROM FOR ME & Non-share ROM.



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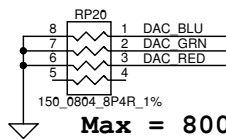
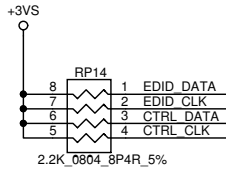
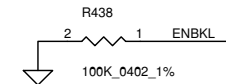


System Power Management

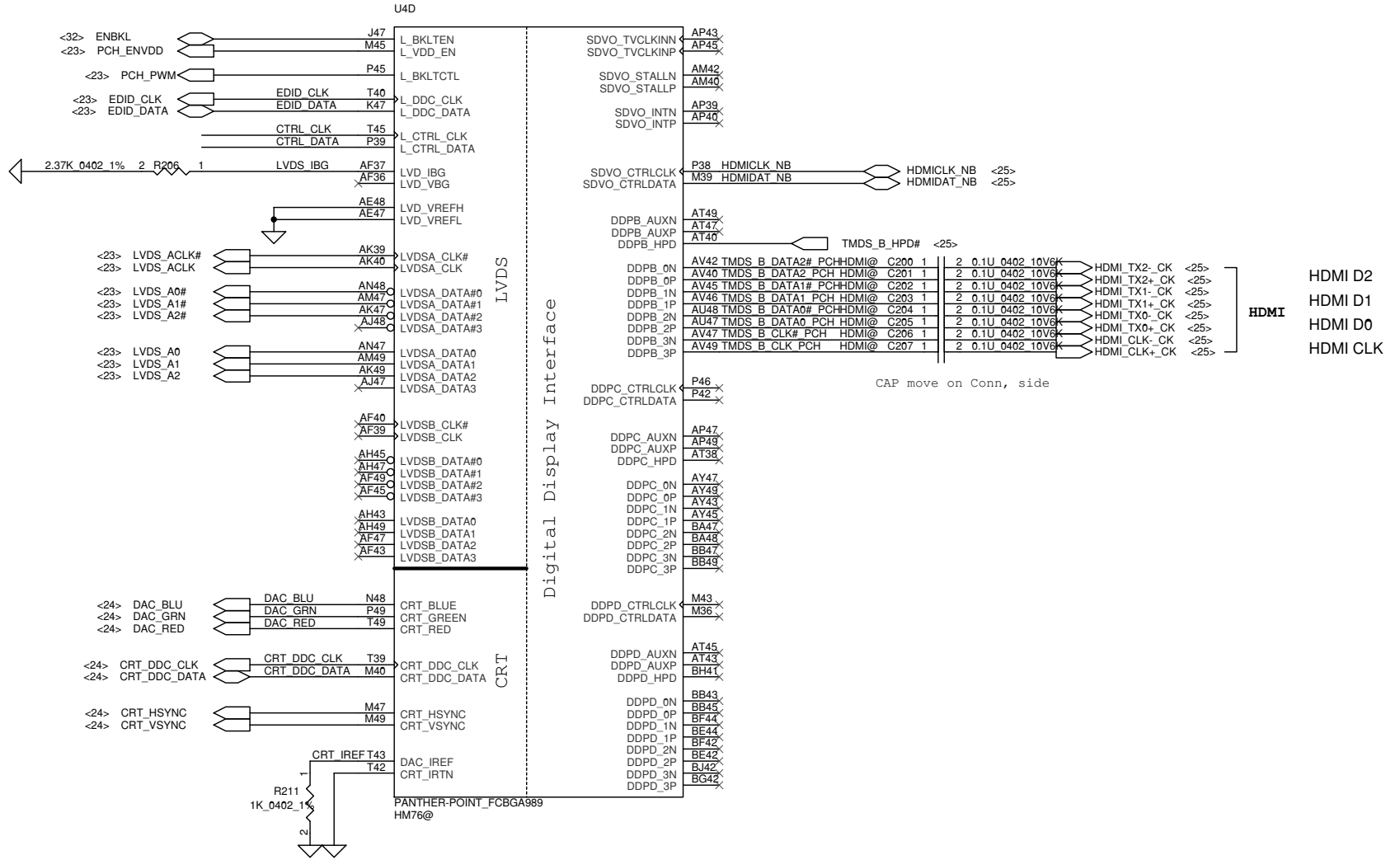
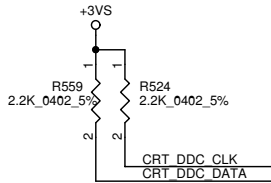
Note: This signal must be always pulled-up to VccRTC.

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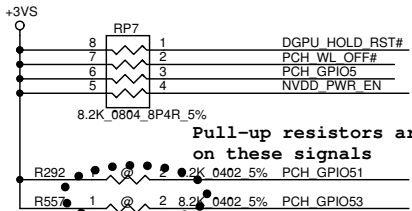
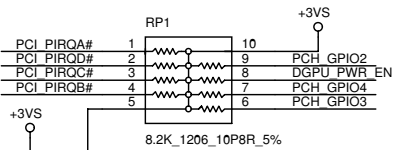
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Max = 800 mils

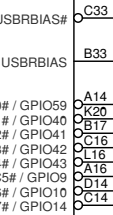
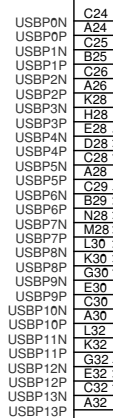
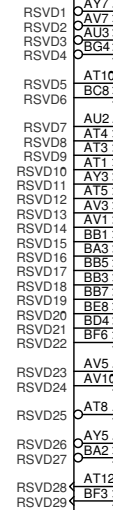
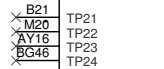
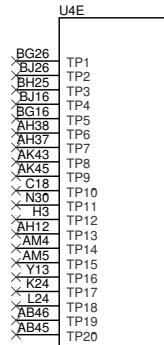
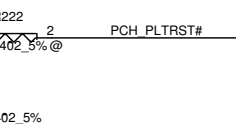
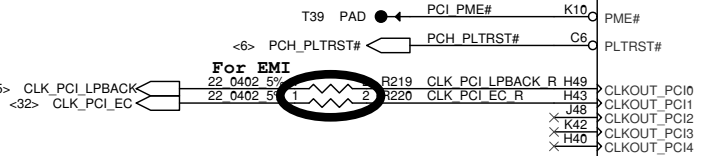
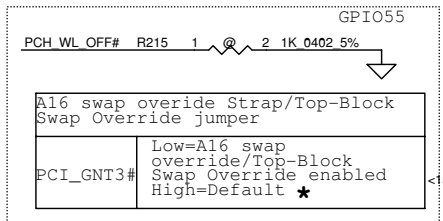
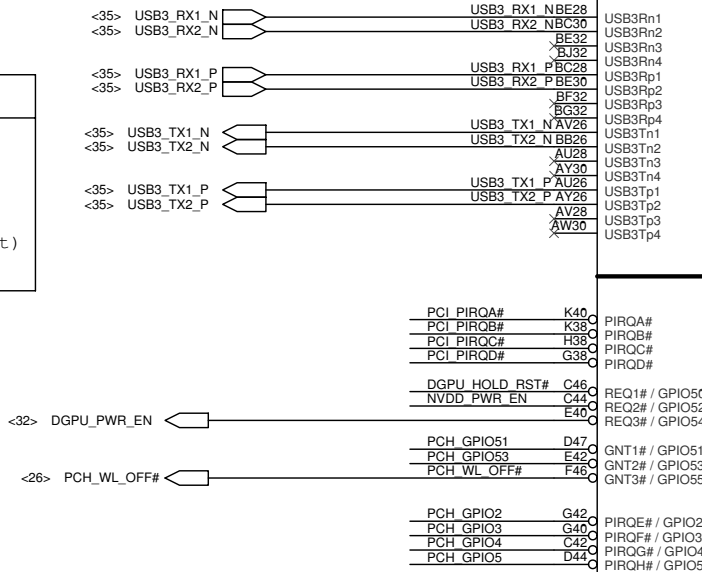


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Pull-up resistors are not required on these signals

Boot BIOS Strap			
GNT1# / GPIO51	GPIO51 Bit11	GPIO19 Bit10	Boot BIOS Destination
SATA1GP / GPIO19	0	1	Reserved
Internal PH	1	0	PCI
	1	1	★ SPI (Default)
	0	0	LPC



USB DEBUG=PORT1 AND PORT9

- LEFT USB (USB 3.0)
- LEFT USB
- Touch Screen
- USB Camera

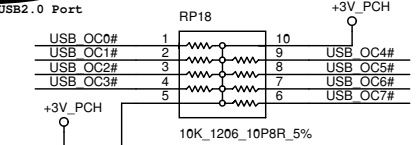
HM76 not support USB2.0 for port 6-7
 HM70 not support USB2.0 for port 4-7 & 12 & 13
 NM70 not support USB2.0 for port 4-7 & 12 & 13

- USB2.0
- WLAN
- CARD READER

Within 500 mils

For LEFT USB3.0 Port

For RIGHT USB2.0 Port



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PCH_GPIO69	PCH_GPIO70	Function
-	-	NM70
-	-	Reserved
-	1	HM70
-	0	HM76

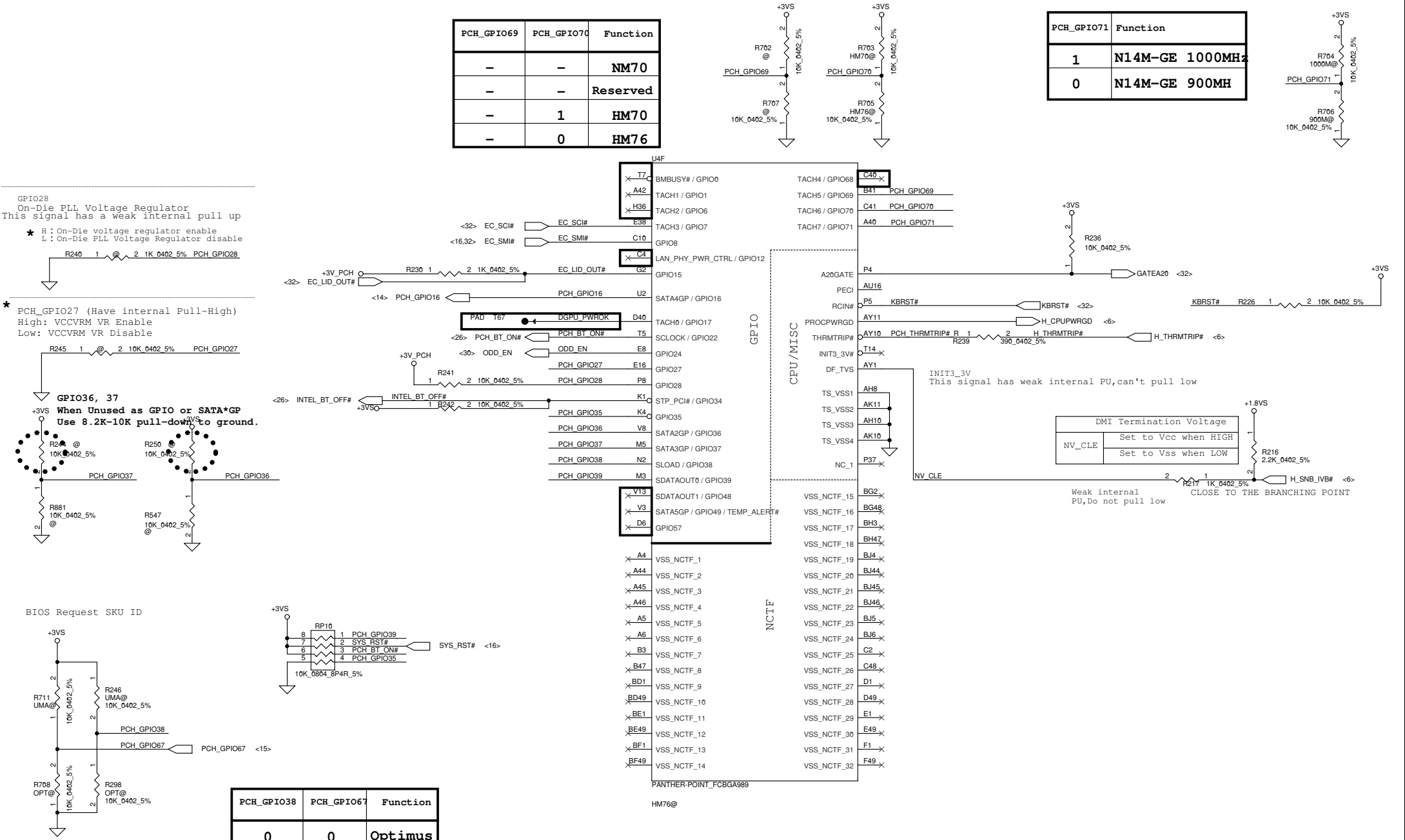
PCH_GPIO71	Function
1	N14M-GE 1000MHz
0	N14M-GE 900MH

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.

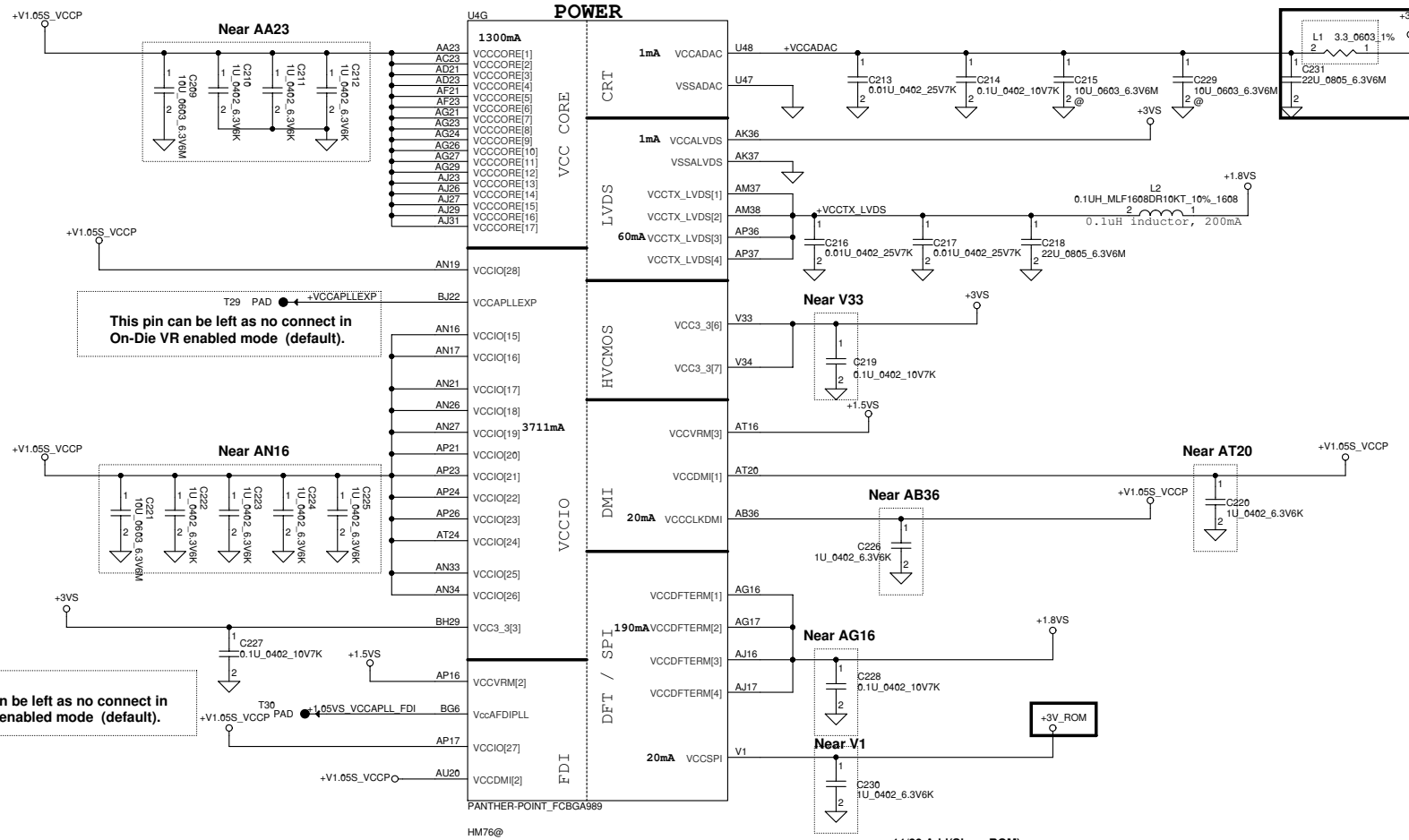
BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

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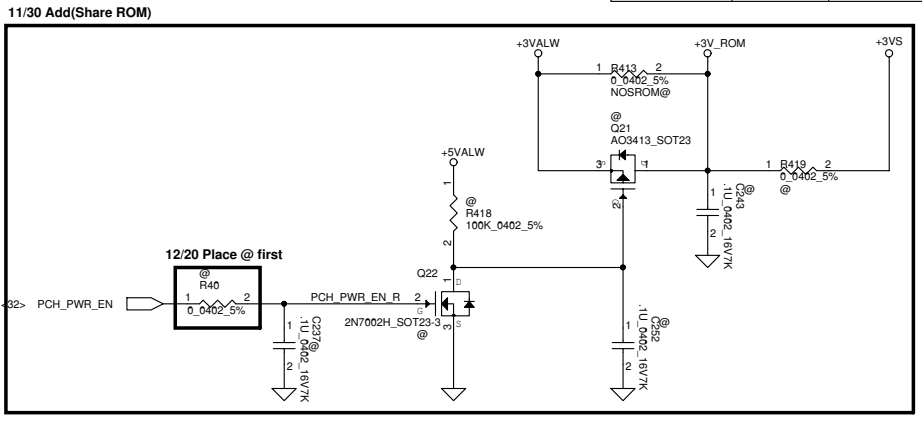


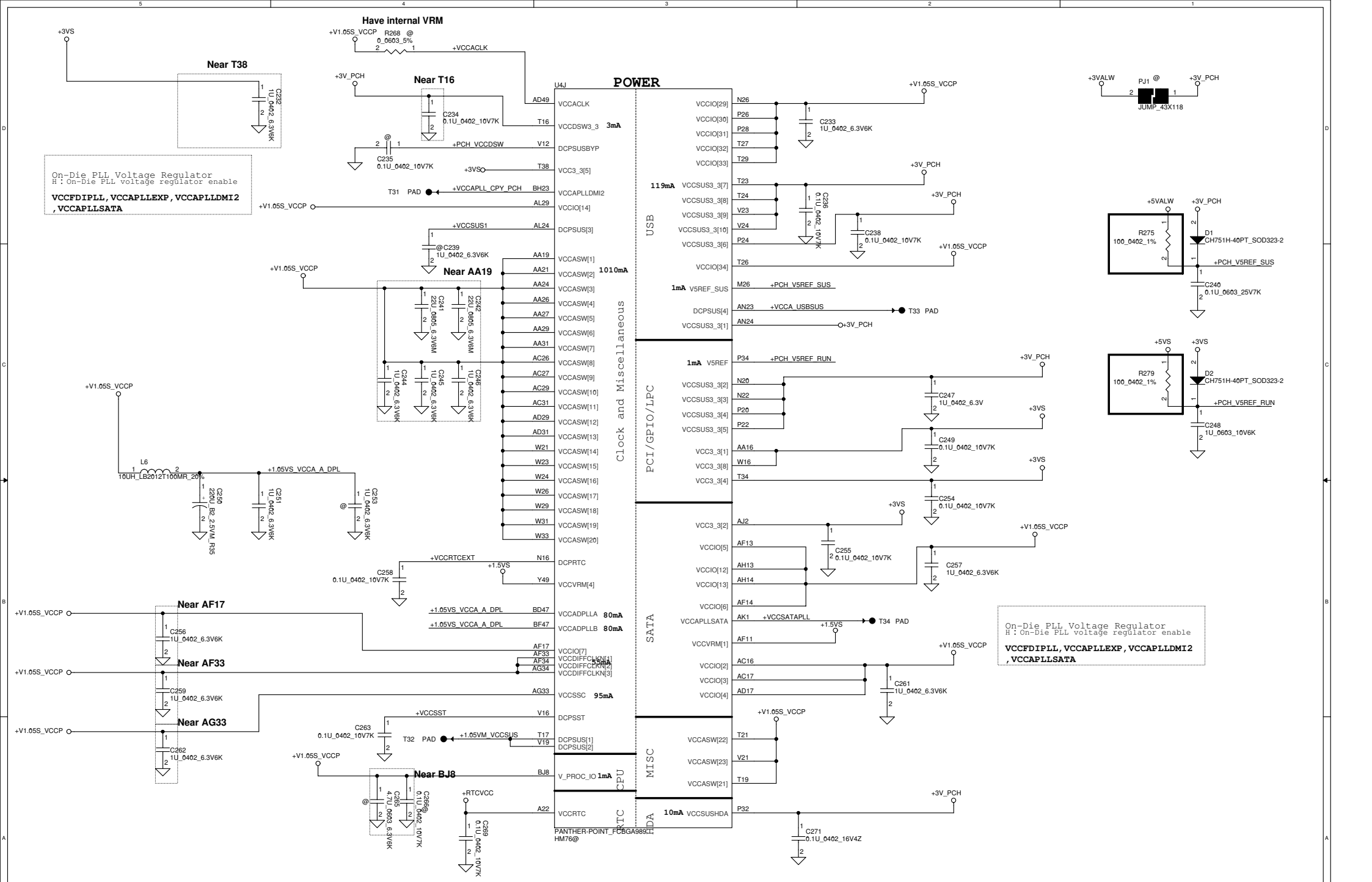
PCH Power Rail Table		
Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

T29 PAD ● +VCCAPLLEXP
 This pin can be left as no connect in On-Die VR enabled mode (default).

T30 PAD ● +V1.05S_VCCAPLL_FDI
 This pin can be left as no connect in On-Die VR enabled mode (default).

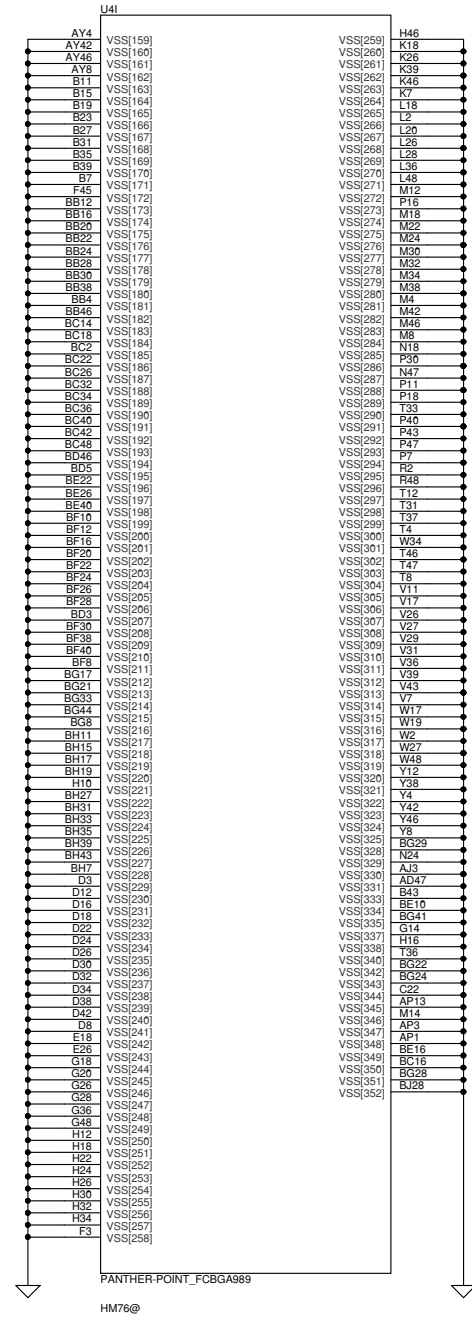
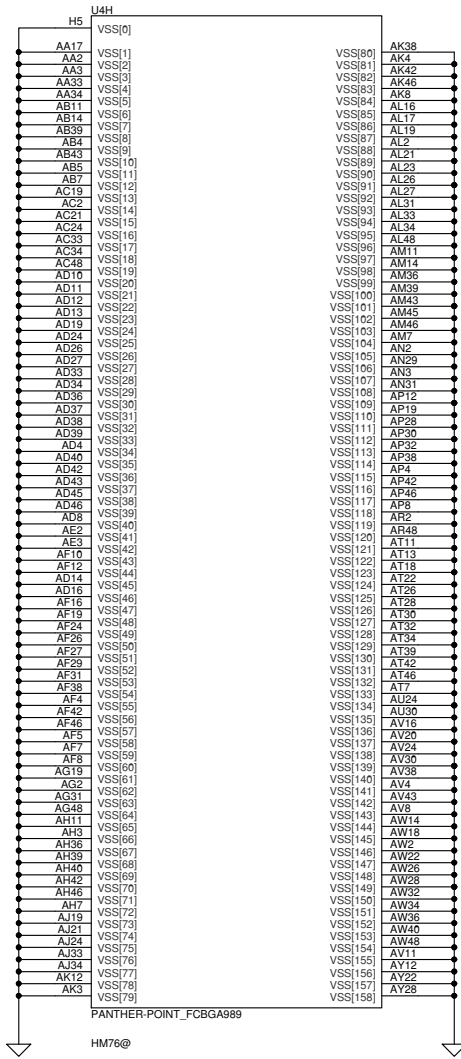
Intel recommend VCCVRM=>1.5V FOR MOBILE
 stuff R265 and unstuff R266 VCCVRM=>1.8V FOR DESKTOP
 VCCVRM = 160mA detal waiting for newest spec





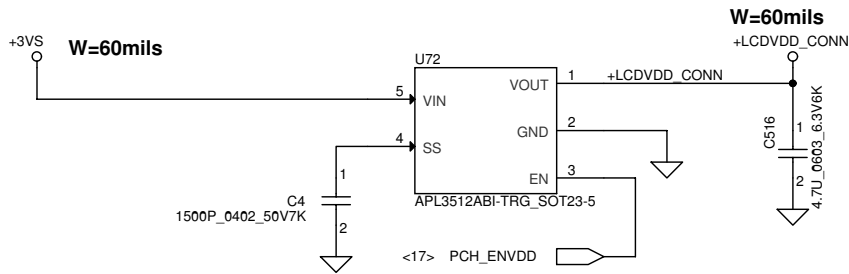
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Compal Electronics, Inc.	
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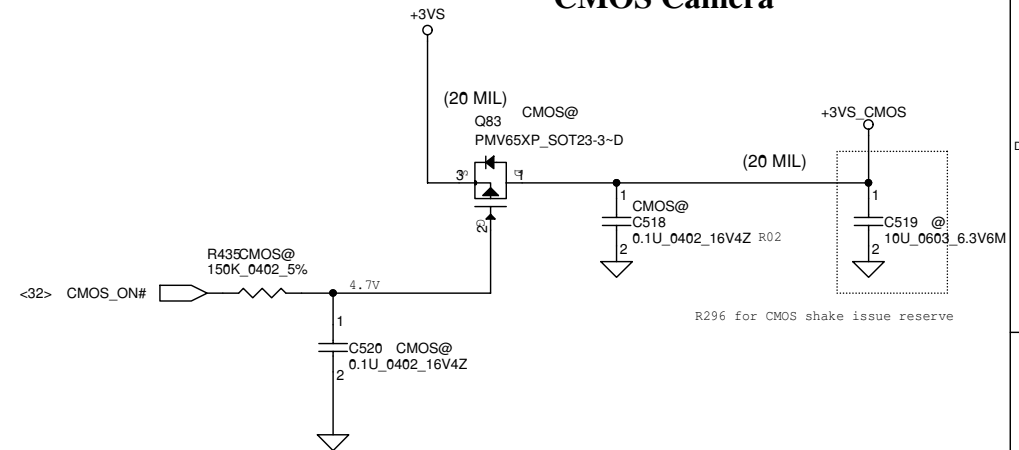


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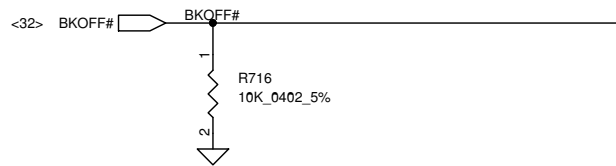
LCD POWER CIRCUIT



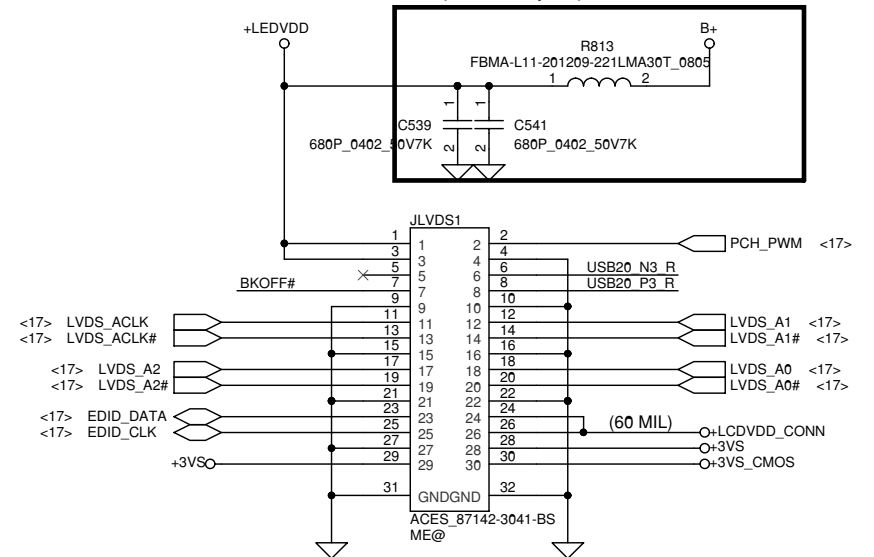
CMOS Camera



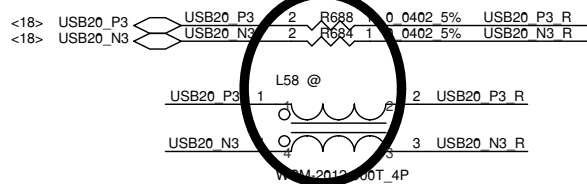
VGA LCD/PANEL BD. Conn.



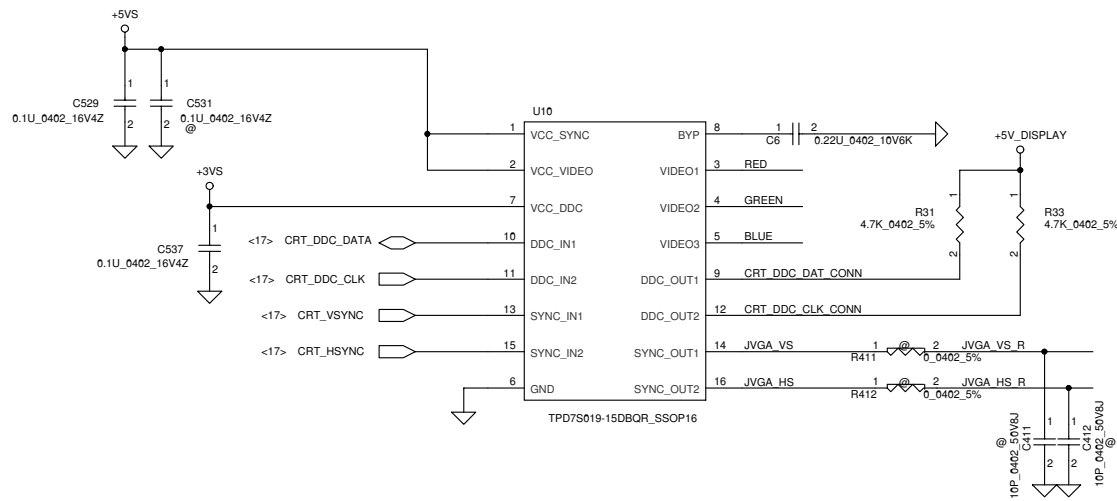
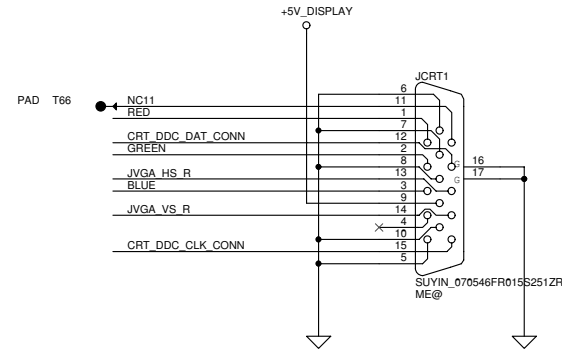
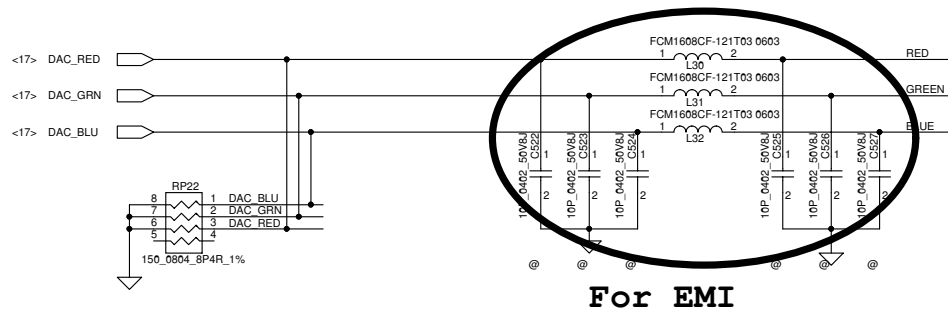
12/12 Mount C539/C541 of 680pF, Change R813 to 220 ohm bead. (For EMI request)



For EMI

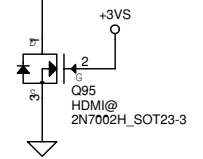
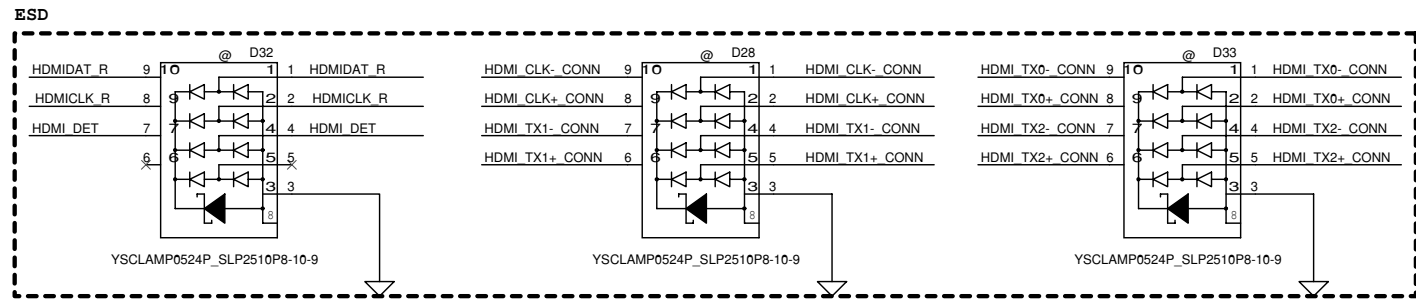
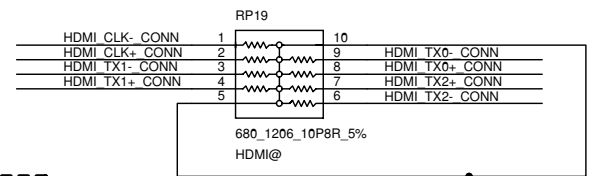
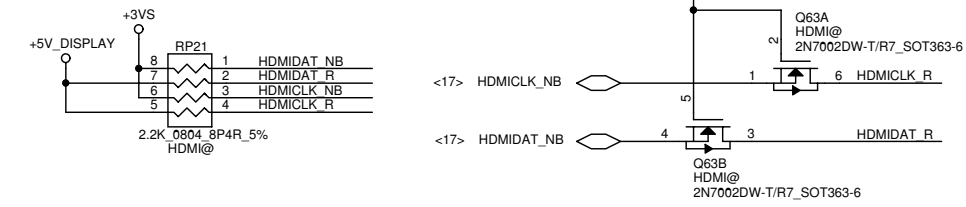
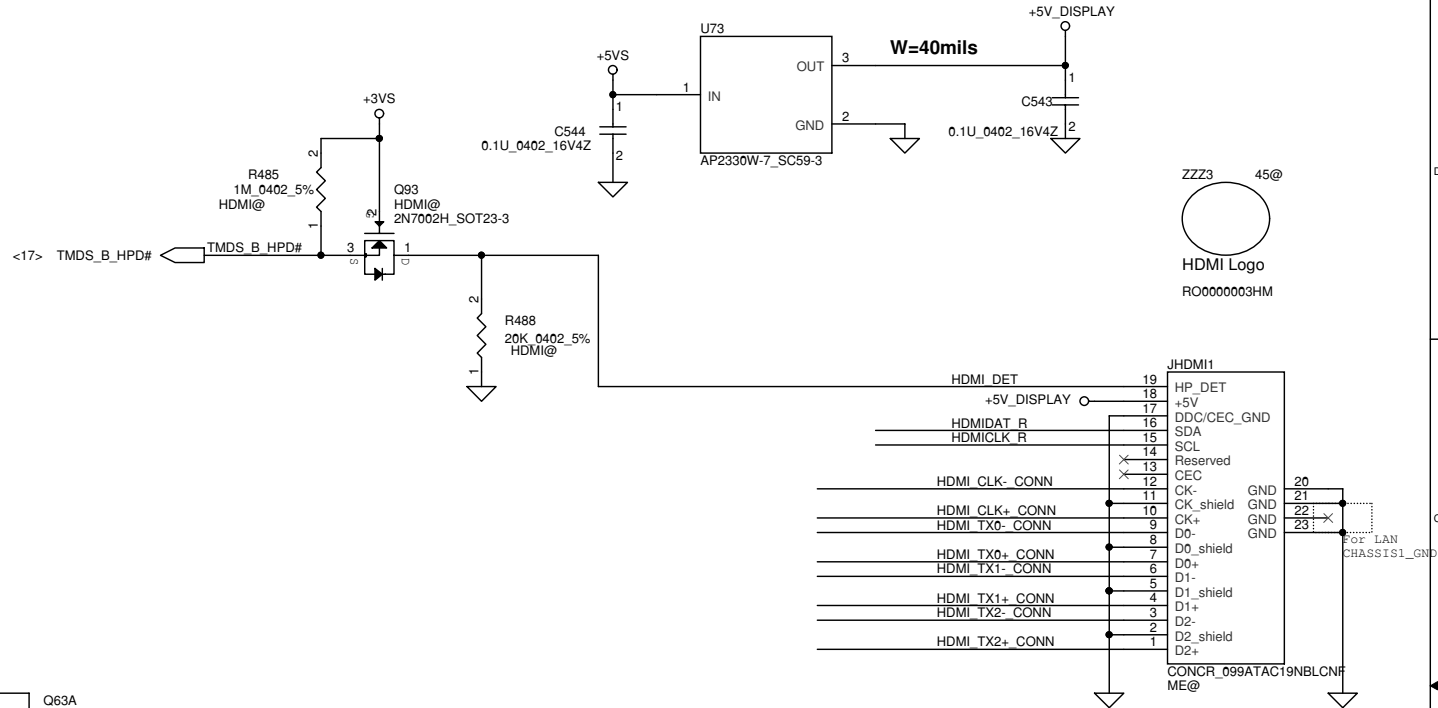
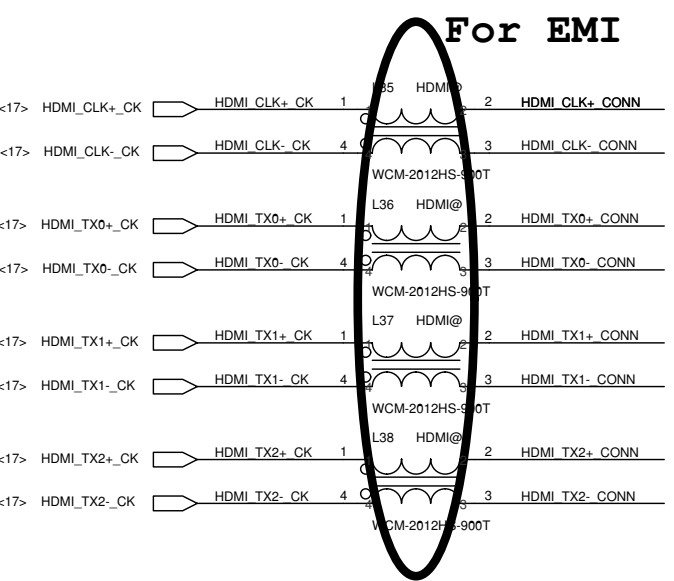


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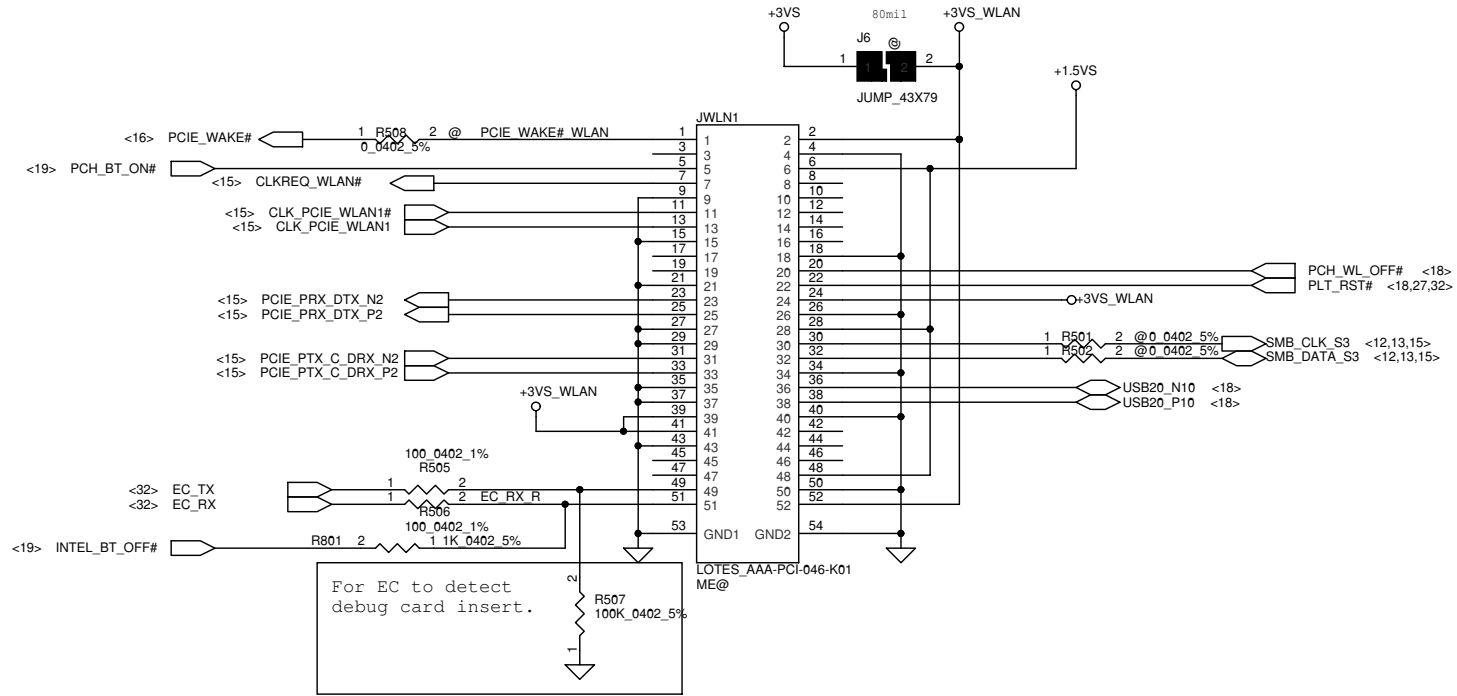
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For EMI



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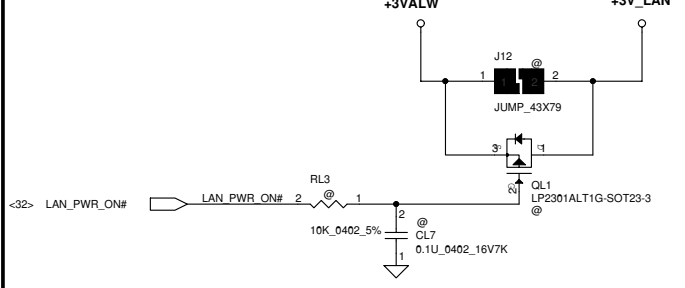
Mini-Express Card for WLAN/WiMAX(Half)



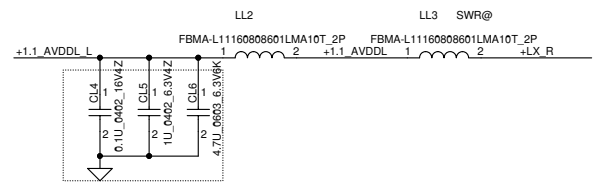
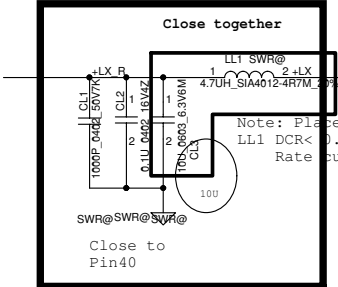
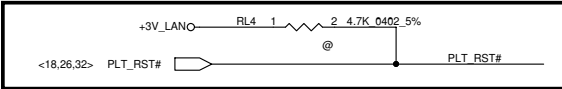
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

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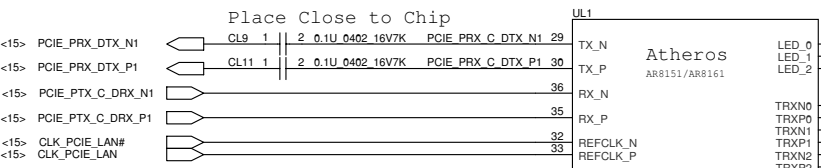
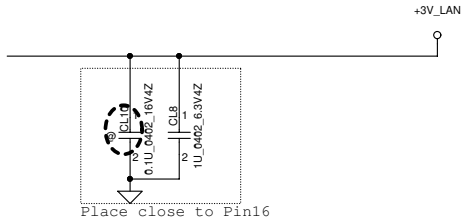
For LAN & Green CLK



Vendor recommend reseve the PU resistor close LAN chip

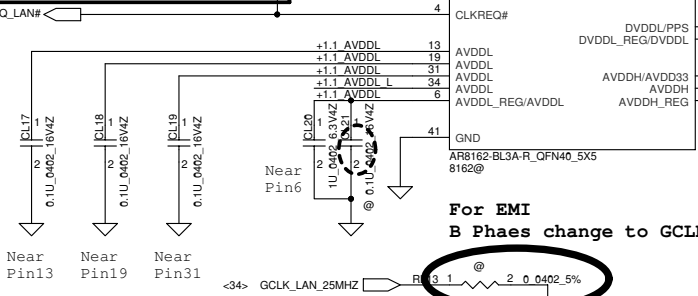


Pin	Configure signal	Description
LED[1]	Regulator select	1 Switch mode regulator(SWR) mode 0 Linear regulator (LDO) mode *

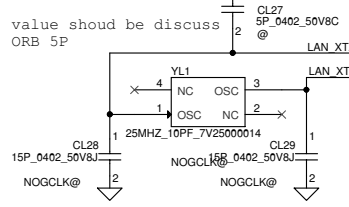


Vendor recommend reseve the PU resistor close LAN chip

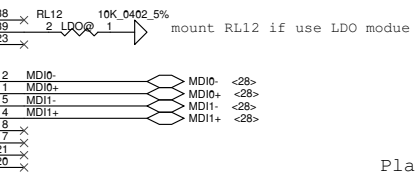
Vendor recommend reseve the PU resistor close LAN chip



For EMI B Phaes change to GCLK@



value should be discuss ORB 5P



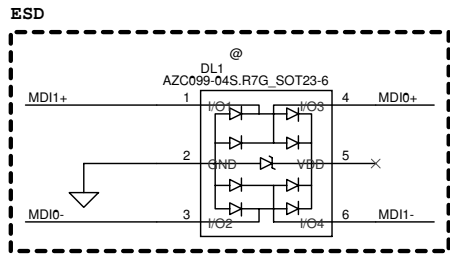
Place Close to PIN1

don't @ (could be B C cost done)

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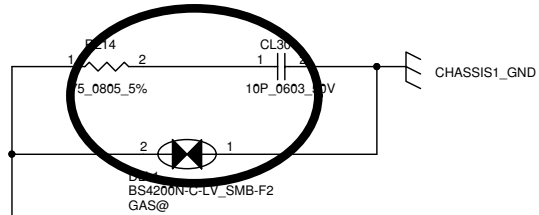
DL1
 1'S PN:SC300001G00
 2'S PN:SC300002E00

Place Close to TL1



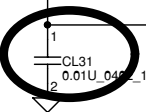
Reserve gas tube for EMI go rural solution

For EMI

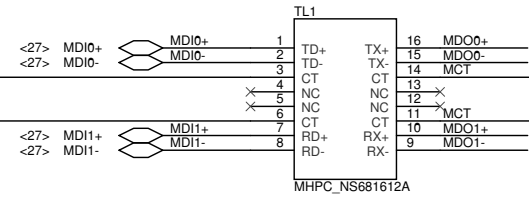


Place Close to TL1

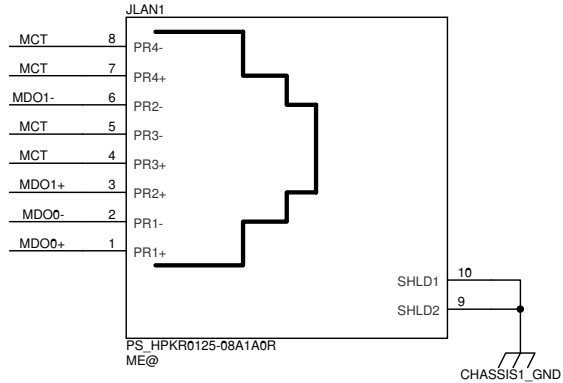
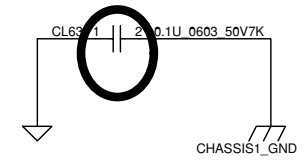
For EMI



12/12 Change BOM Structure of CL31 from @ to mount(EMI request)

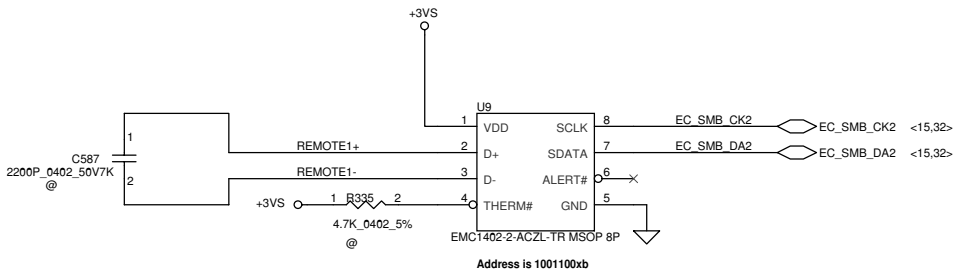


For EMI



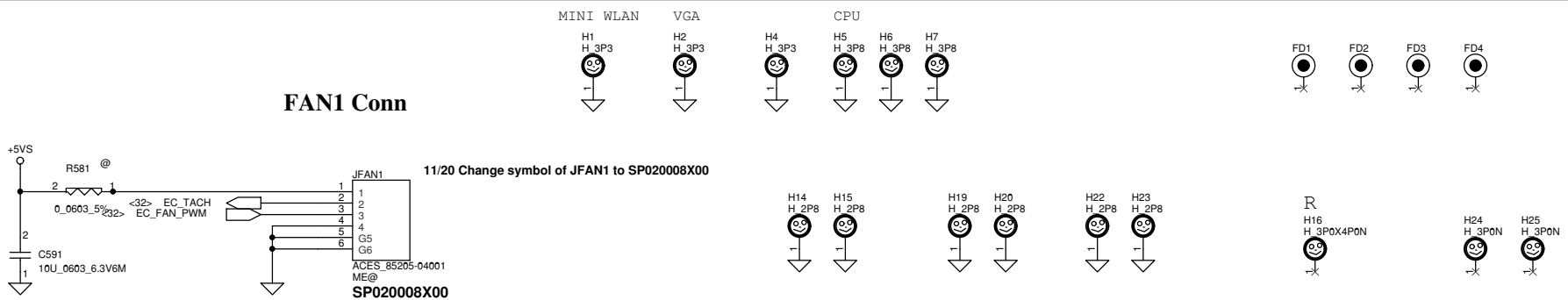
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**SMSC thermal sensor
placed near VRAM**



REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

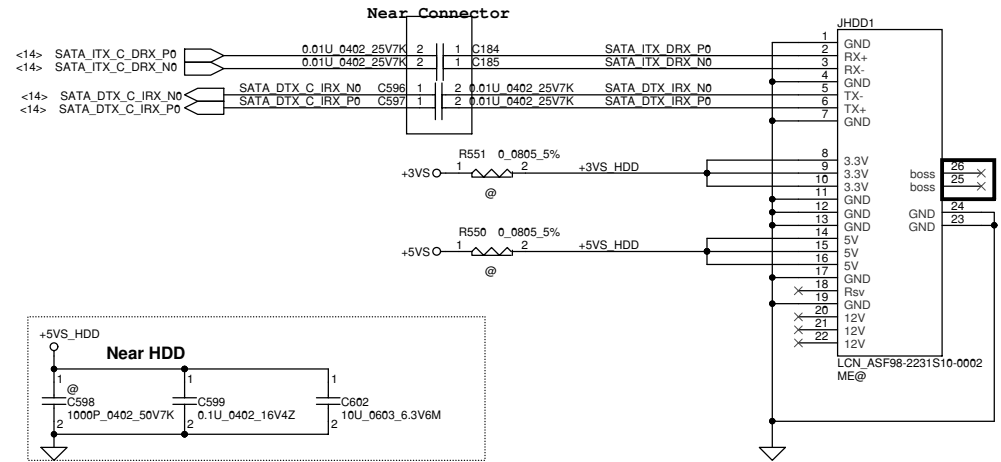
FAN1 Conn



E
M/B 橢圓孔 M/B 圓孔

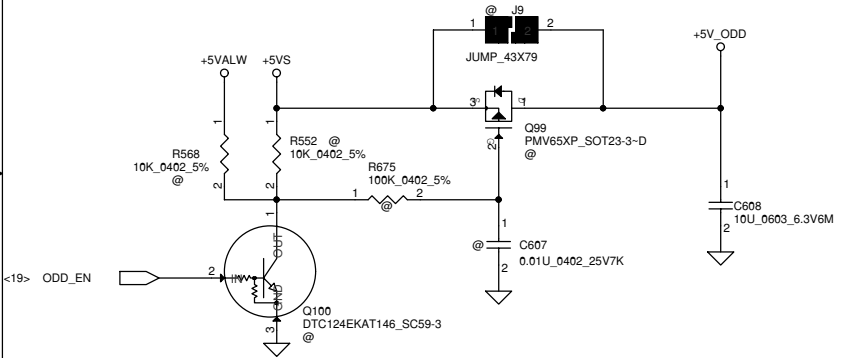
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SATA HDD Conn.

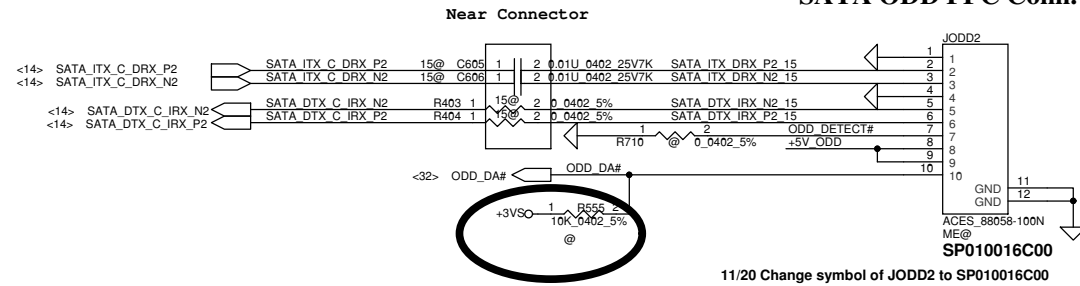


1/16 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 to DC010009C00)

ODD Power Control



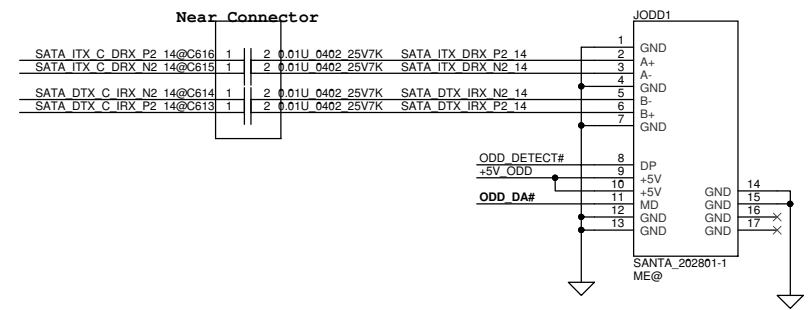
FOR 15" SATA ODD FFC Conn.



11/20 Change symbol of JODD2 to SP010016C00

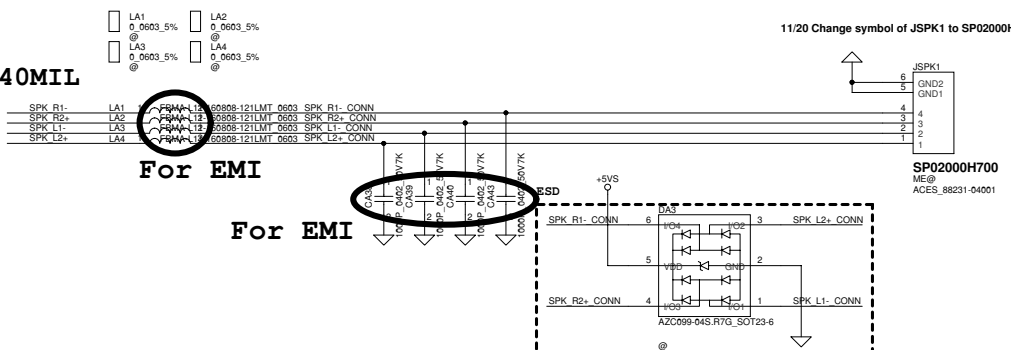
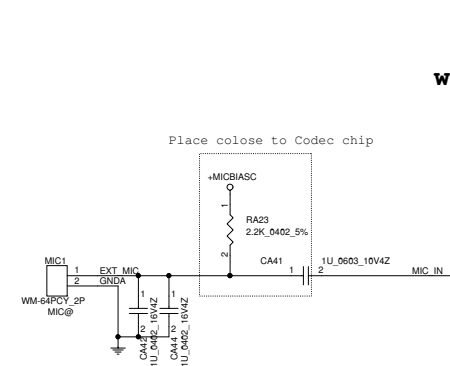
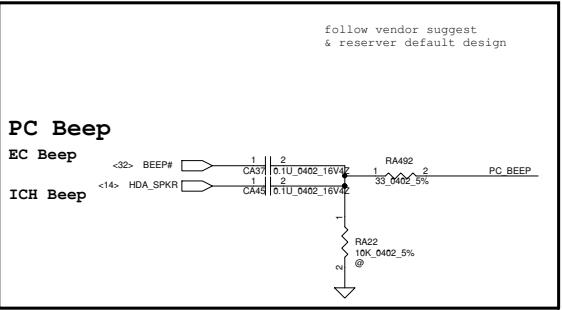
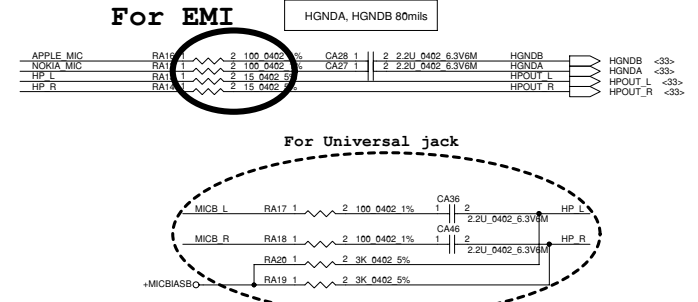
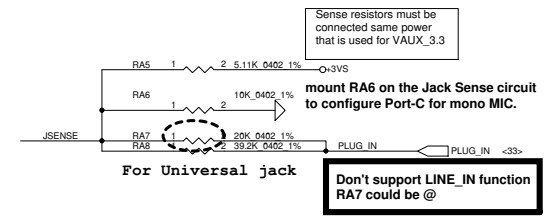
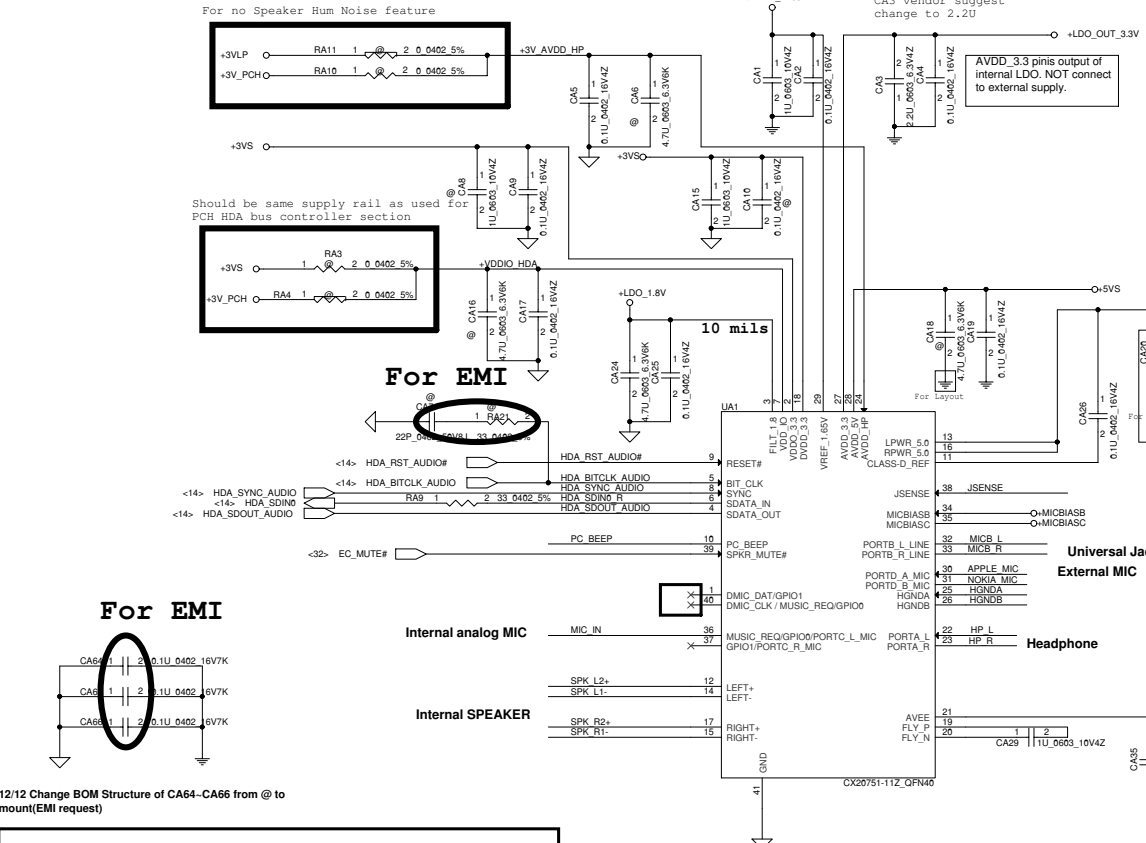
Co-lay

FOR 14" SATA ODD Conn.

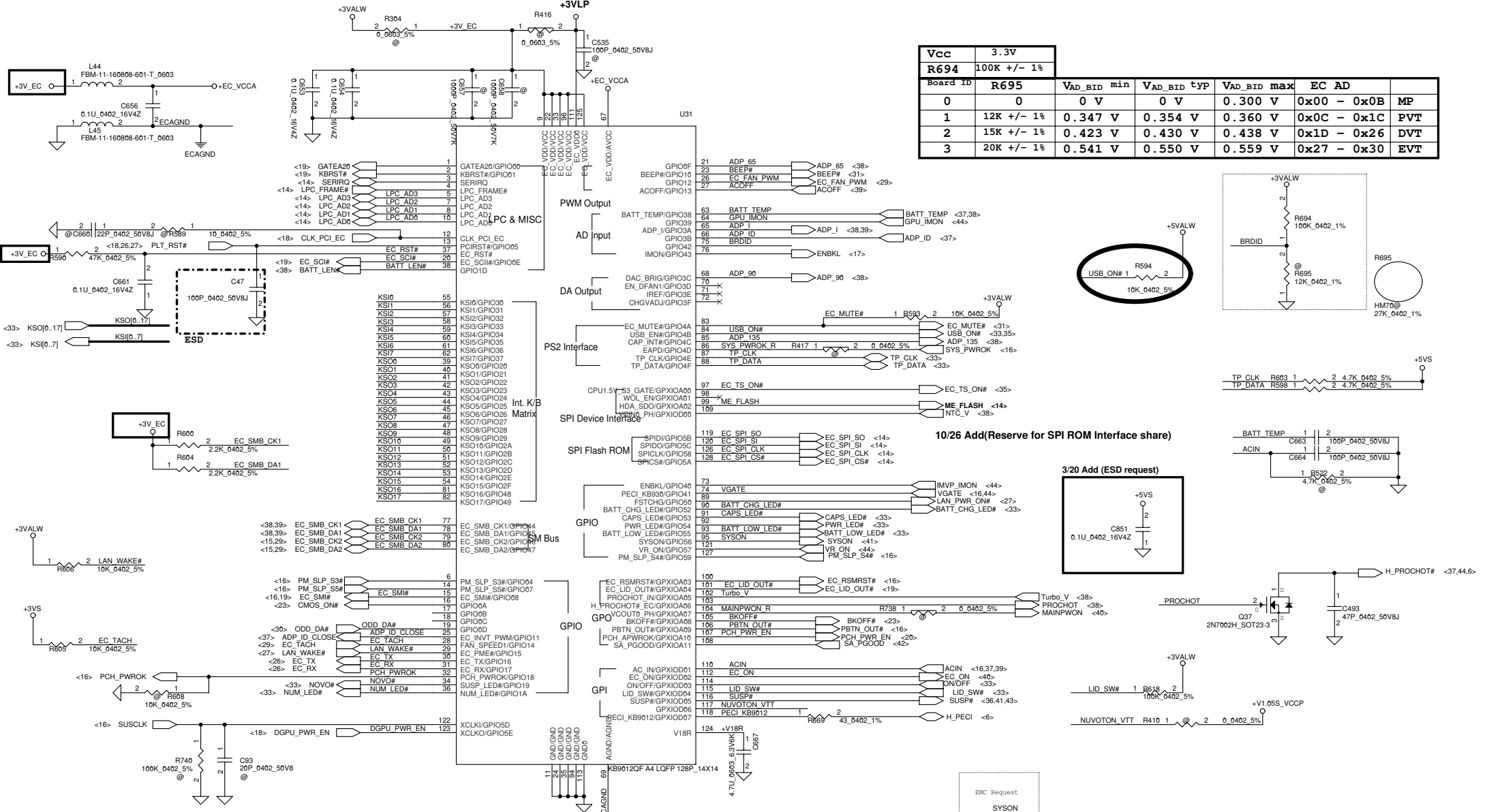


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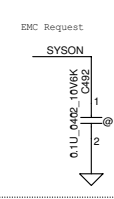
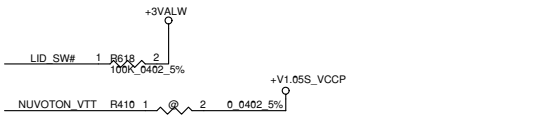
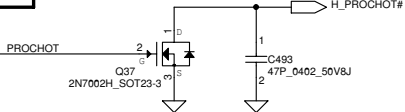
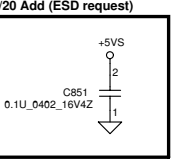
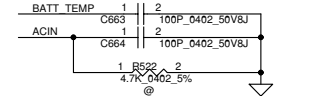
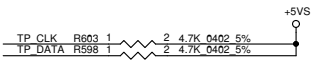
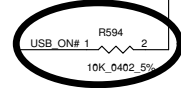
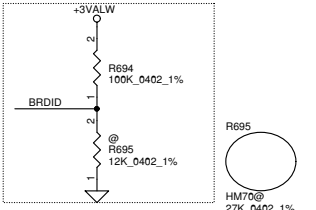
CX20757
 High Definition Audio Codec SoC
 With Integrated Class-D Stereo
 Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).



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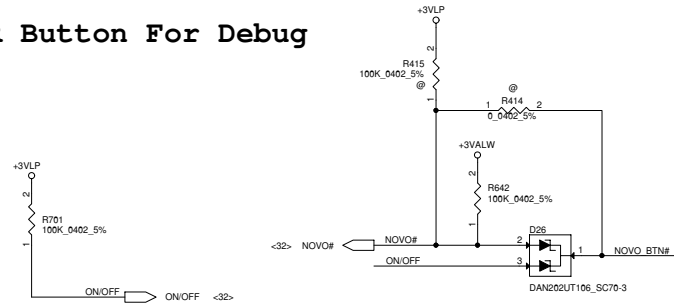
Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT



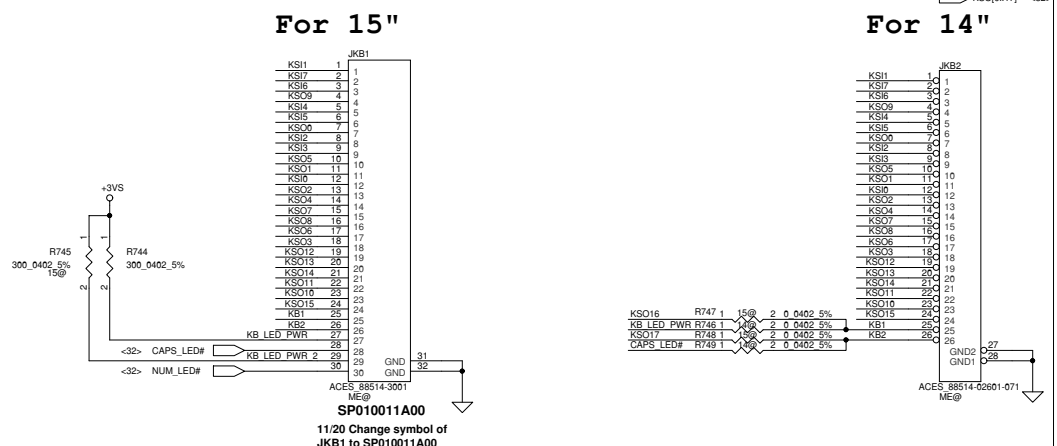
PN : SA000040B20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

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PWR Button For Debug

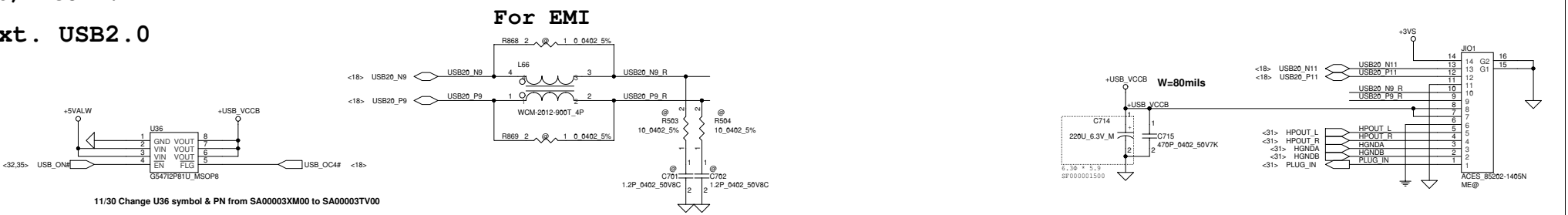


Key Board Conn.

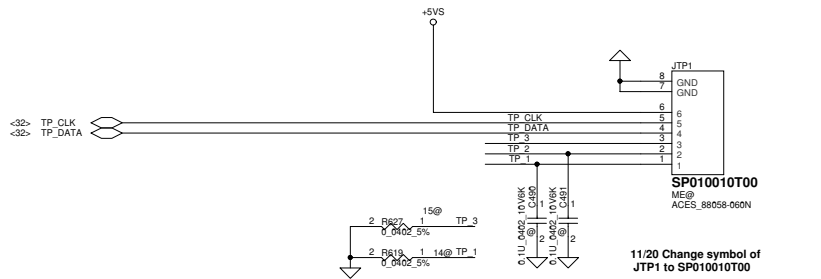


IO/B Conn.

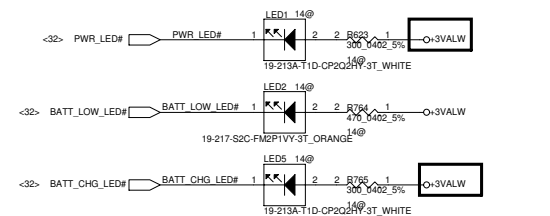
Ext. USB2.0



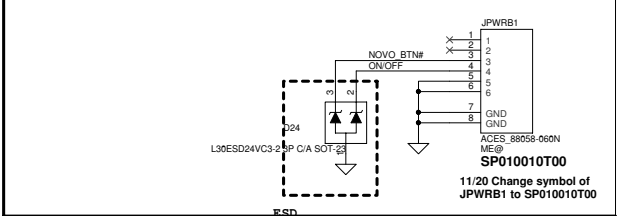
TP Switch & TP Conn.



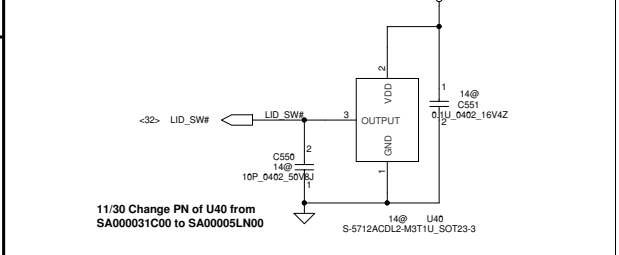
LED



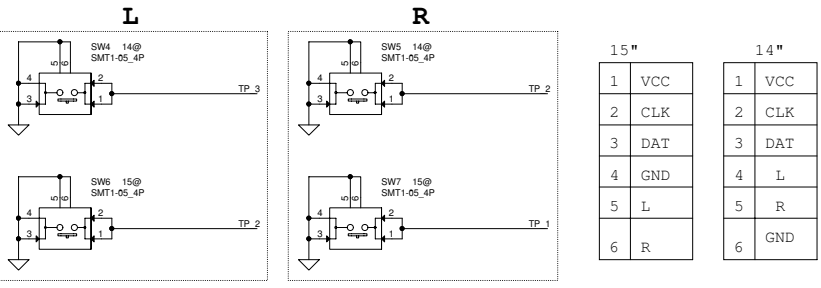
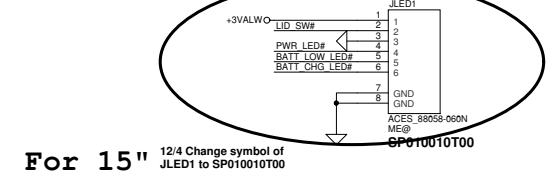
PWR/B Conn.



Lid SW (For 14")

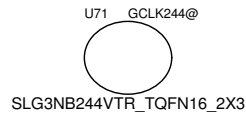


LED/B Conn.



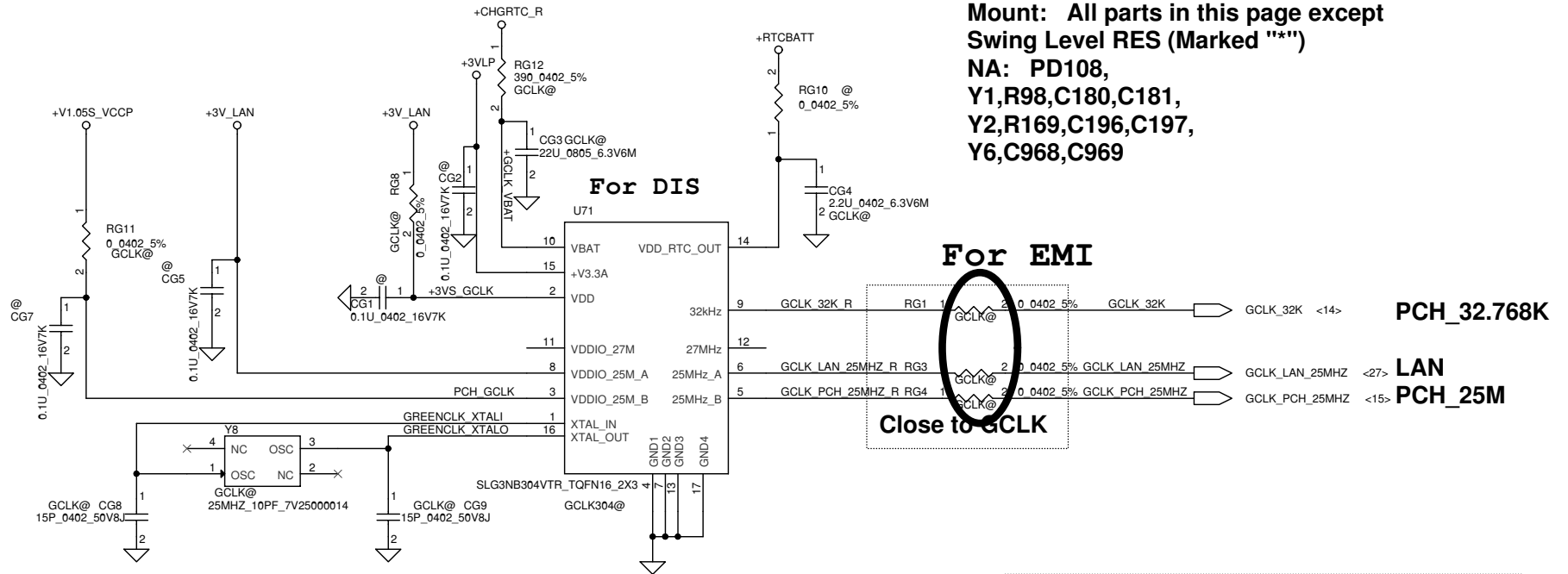
For 15" 12/4 Change symbol of JLED1 to SP010010T00

For UMA

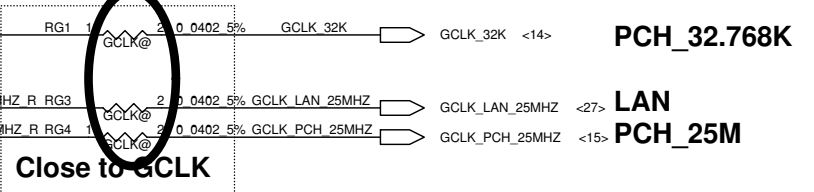


Every power trace need:
W=20mils

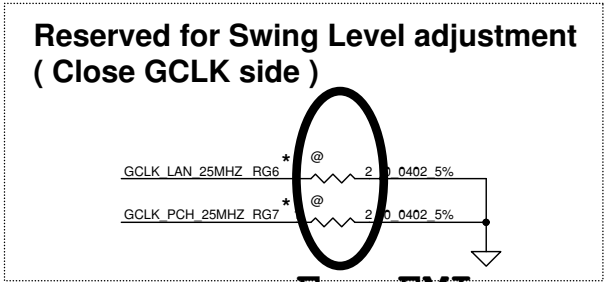
For GreenCLK generate CLK:
Mount: All parts in this page except
Swing Level RES (Marked "**")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969



For EMI



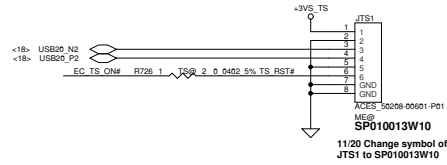
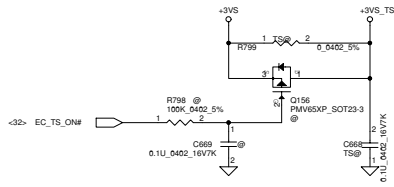
Close to GCLK



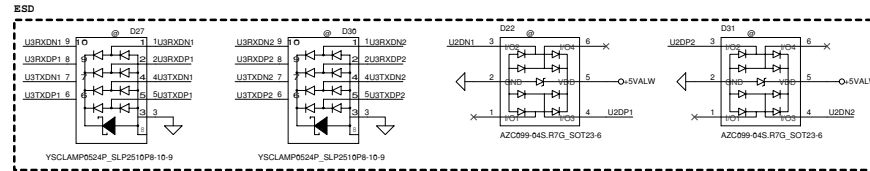
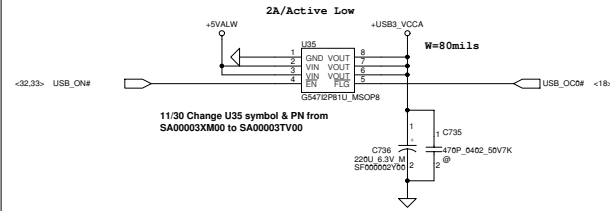
For EMI

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				B	4019N1	B
				Date:	Wednesday, May 08, 2013	Sheet 34 of 52

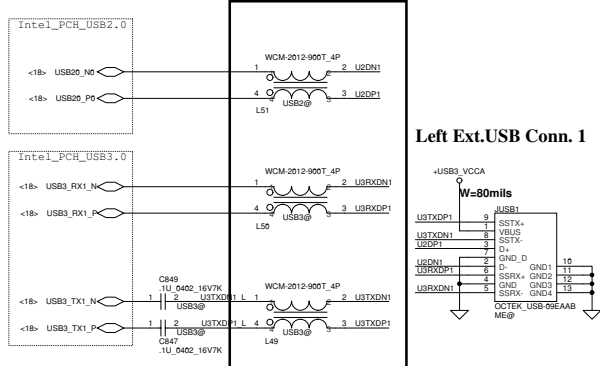
Touch Screen



USB3.0



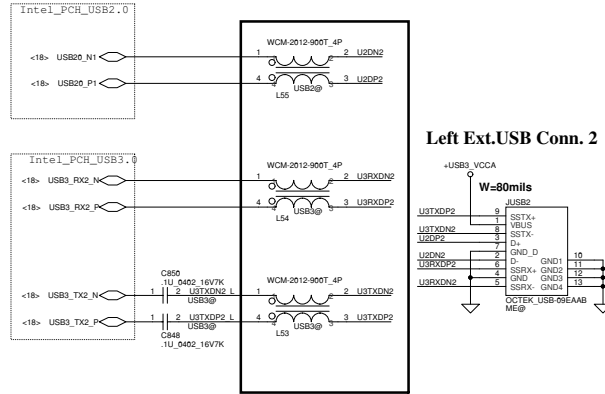
For EMI



Place TX AC coupling Cap (C843-C850). Close to connector

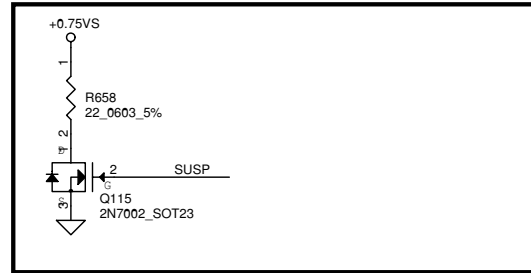
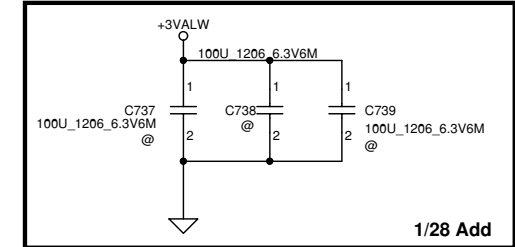
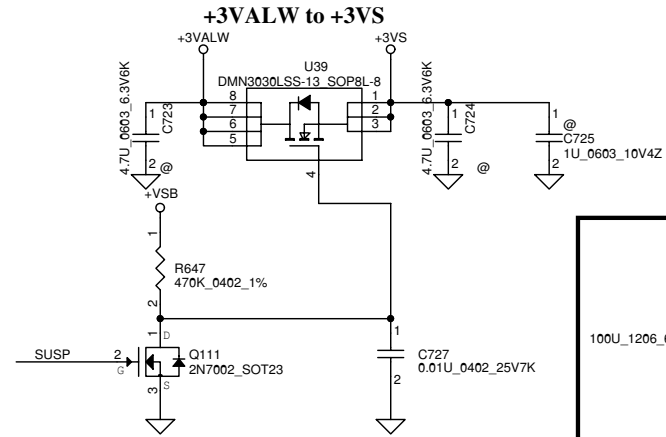
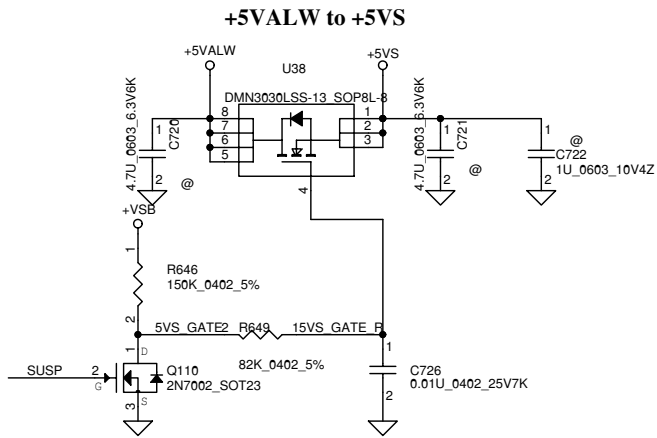
Left Ext.USB Conn. 1

For EMI

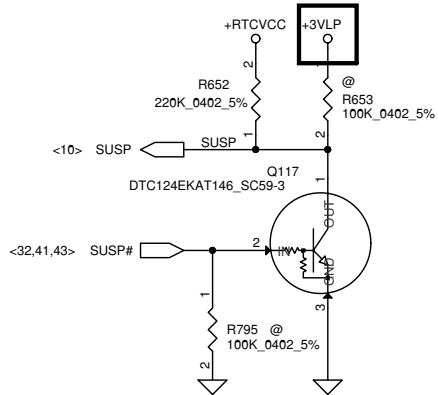
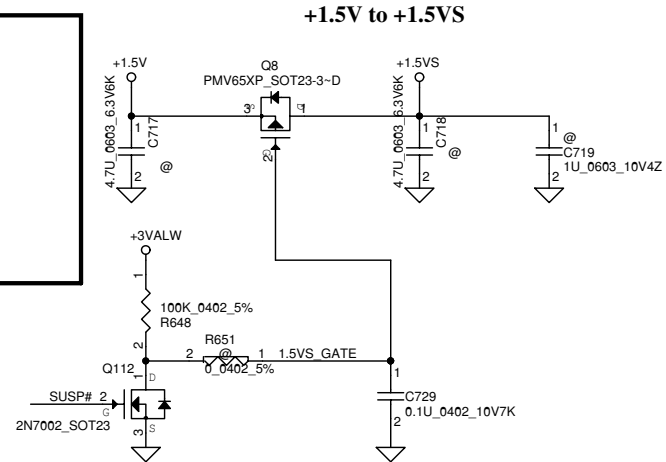


Left Ext.USB Conn. 2

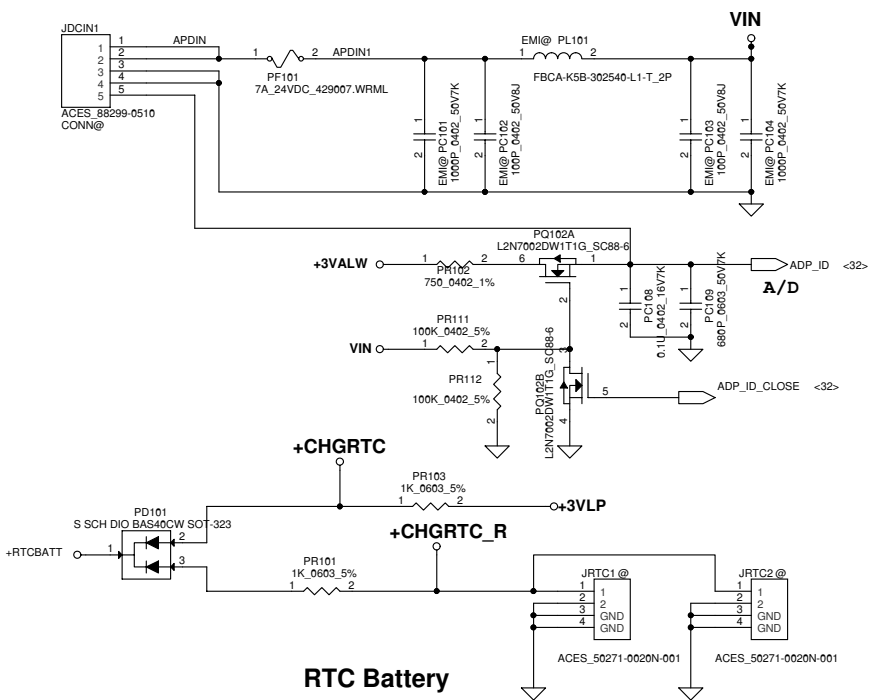
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For Intel S3 Power Reduction.

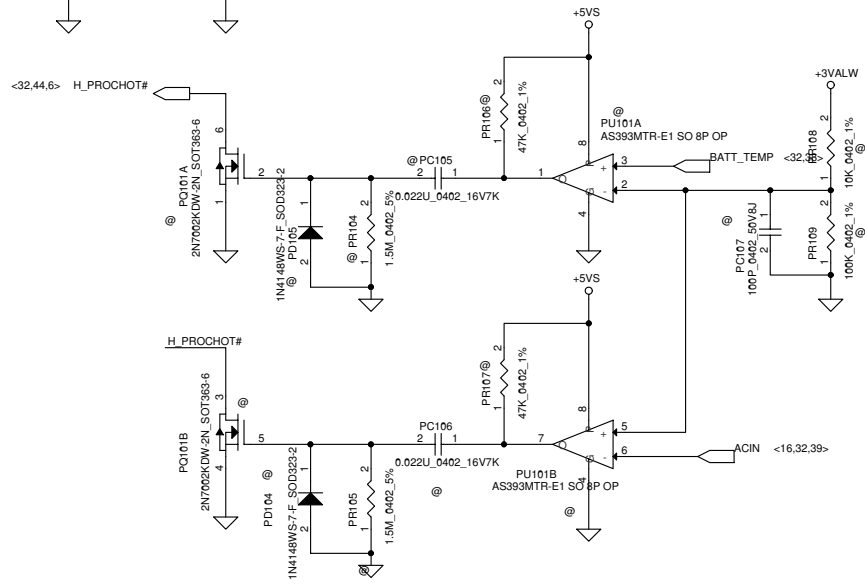


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				4019N1	
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ADP_ID	AC Adapter	90W	65W
R(K ohm)	open	10	
ADP_ID(V)	3.3	1.65	
Detection voltage	>2.64	1.32~1.98	

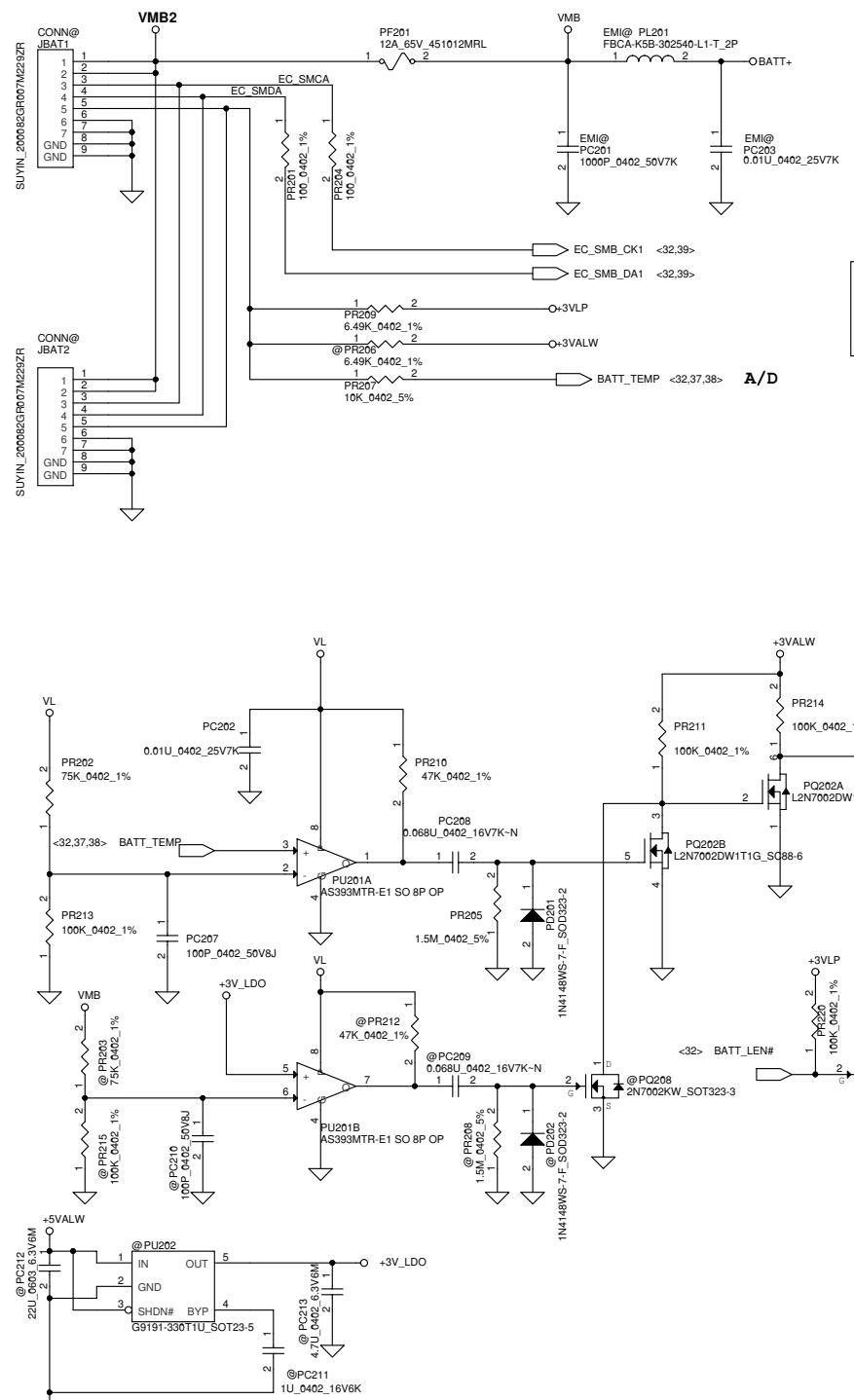
RTC Battery



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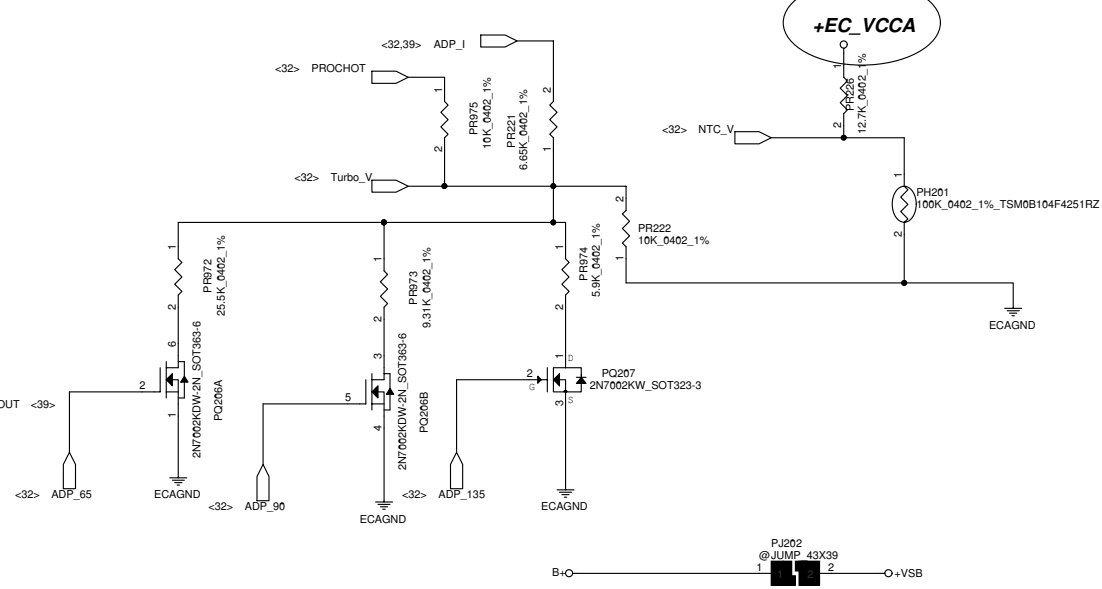
Compal Electronics, Inc.			
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PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA) : 1.65K 70W active 65W recovery

20120314
 Change to +EC_VCCA from +3VLP

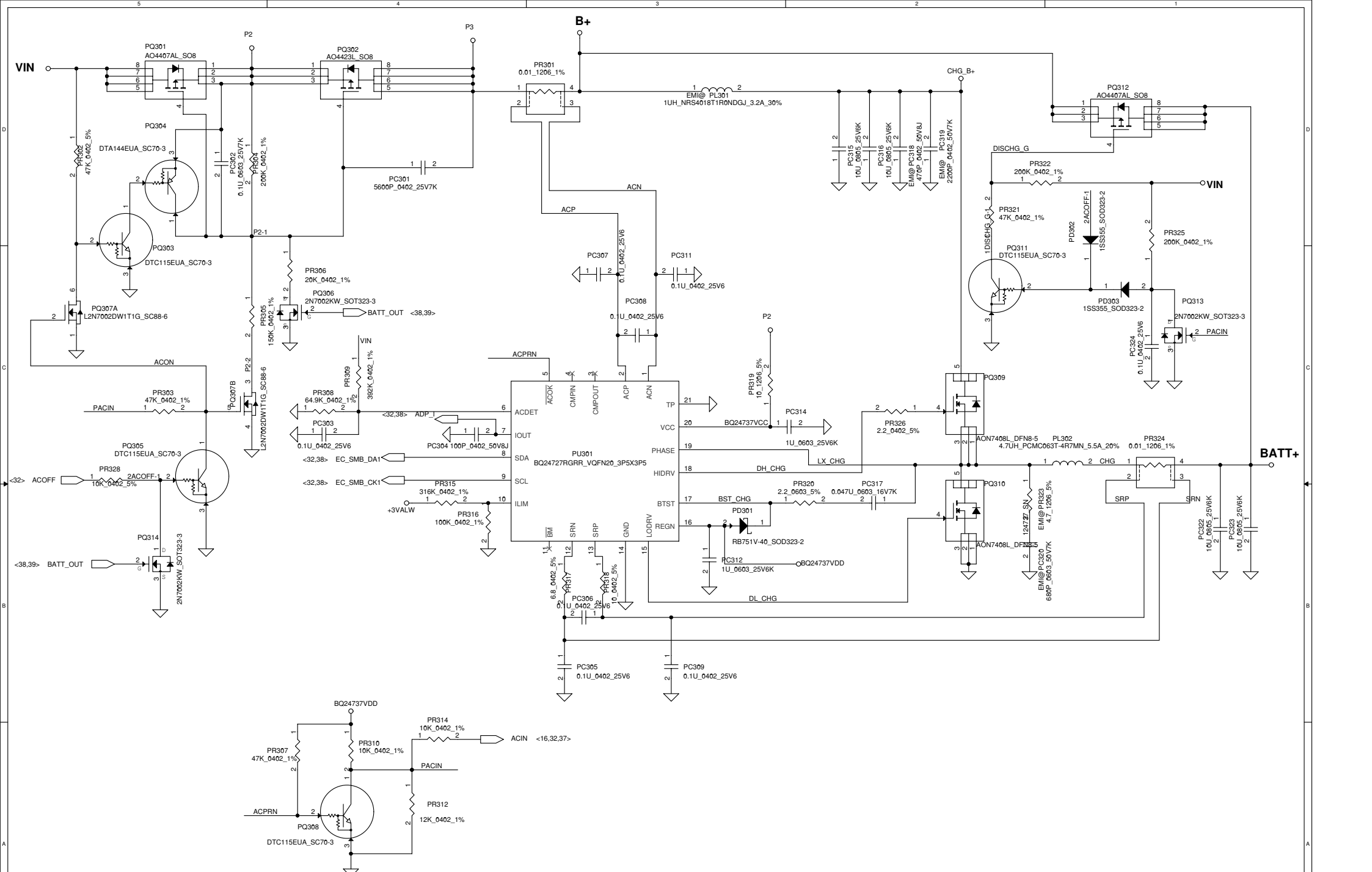


Security Classification	Compal Secret Data	
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		2012/07/11

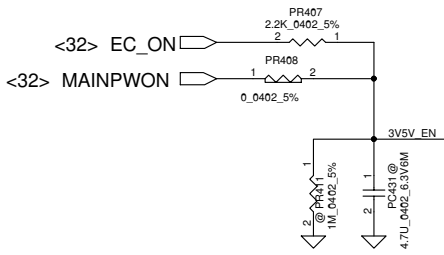
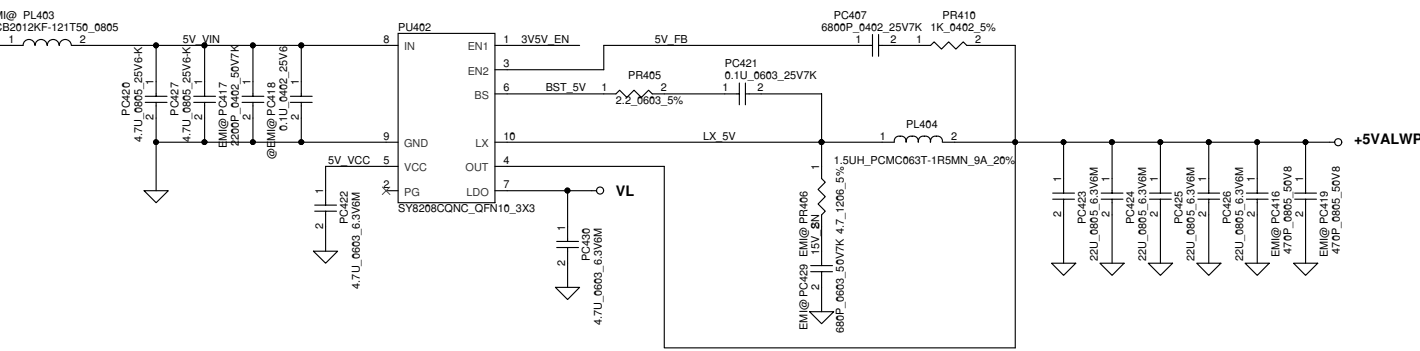
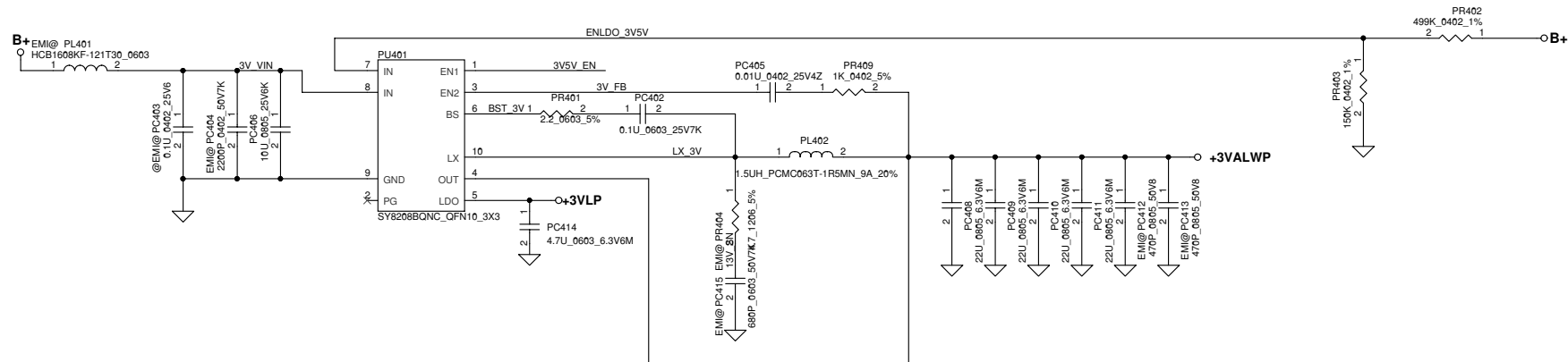
Compal Electronics, Inc.
SCHEMATIC M/B LA-9902

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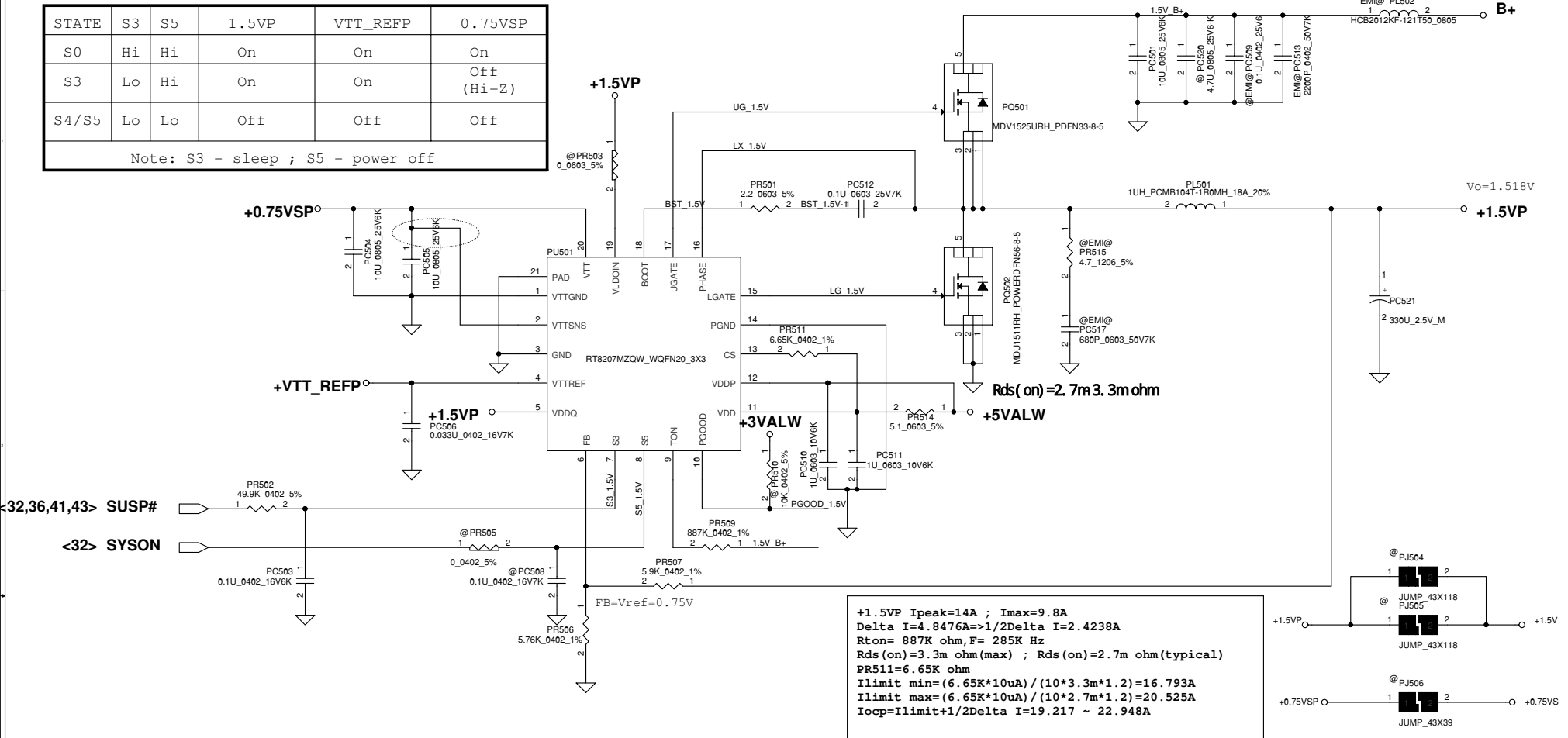
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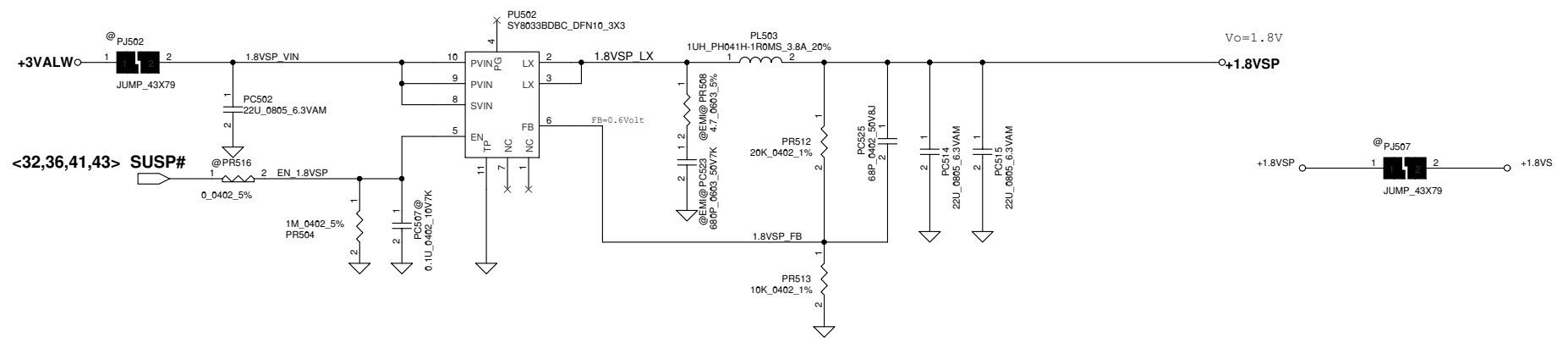
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

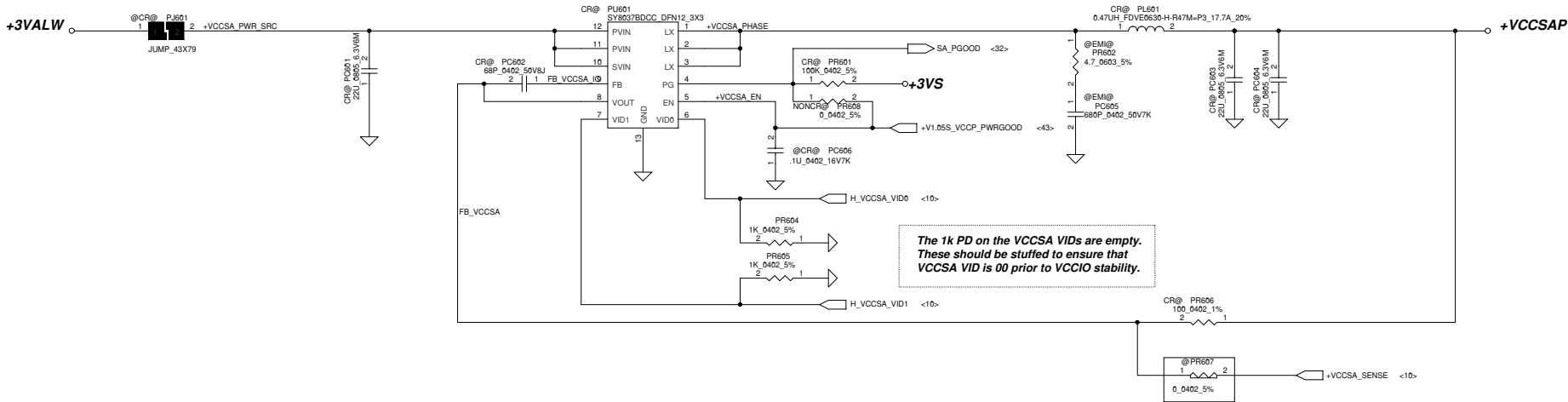
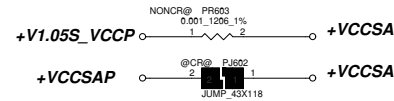


+1.5VP Ipeak=14A ; Imax=9.8A
 $\Delta I = 4.8476A \Rightarrow 1/2\Delta I = 2.4238A$
 $R_{ton} = 887K \text{ ohm}, F = 285K \text{ Hz}$
 $R_{ds(on)} = 3.3K \text{ ohm (max)} ; R_{ds(on)} = 2.7m \text{ ohm (typical)}$
 $PR511 = 6.65K \text{ ohm}$
 $I_{limit_min} = (6.65K * 10\mu A) / (10 * 3.3m * 1.2) = 16.793A$
 $I_{limit_max} = (6.65K * 10\mu A) / (10 * 2.7m * 1.2) = 20.525A$
 $I_{ocp} = I_{limit} + 1/2\Delta I = 19.217 \sim 22.948A$



VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

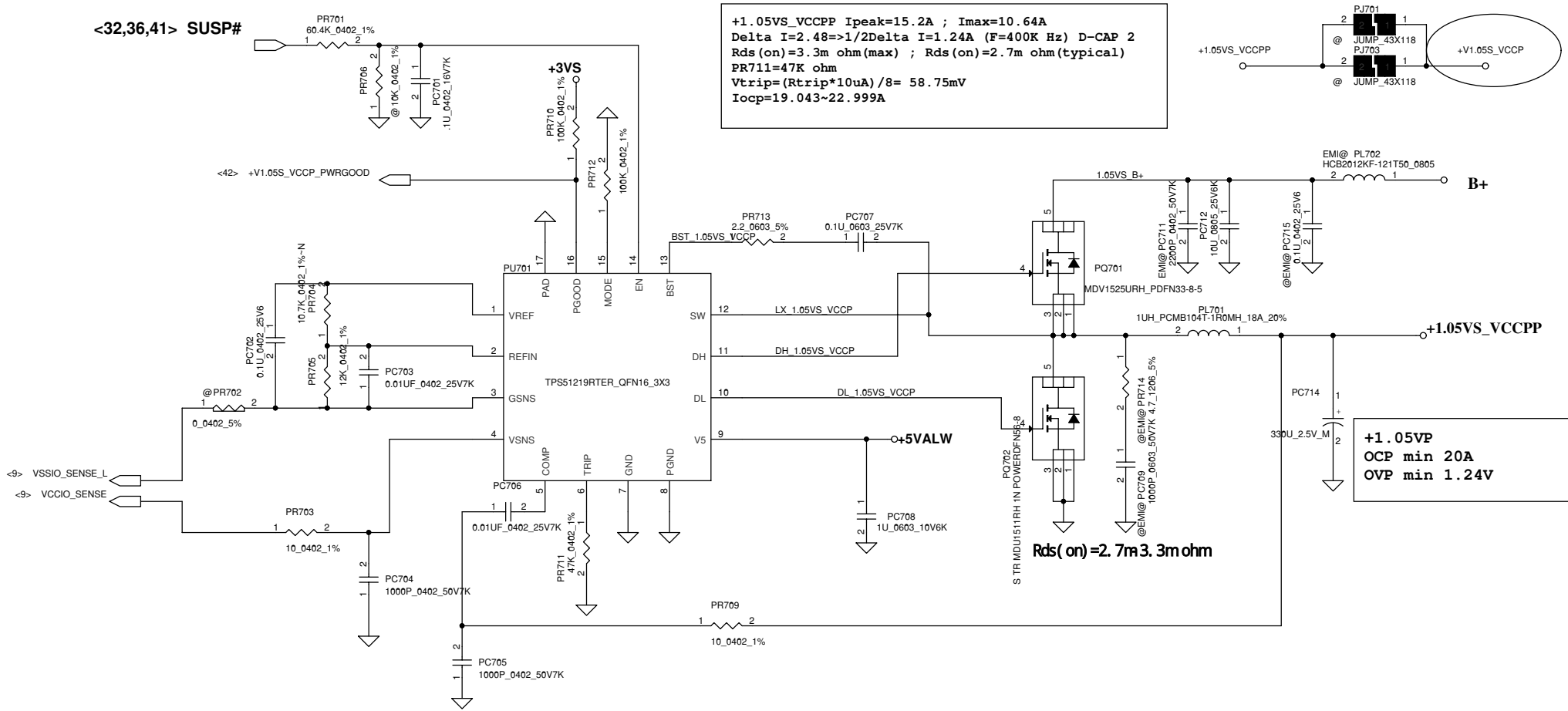
output voltage adjustable network



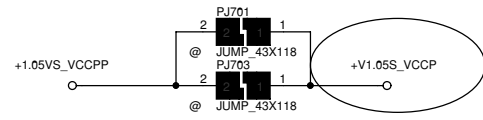
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

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<32,36,41> SUSP#



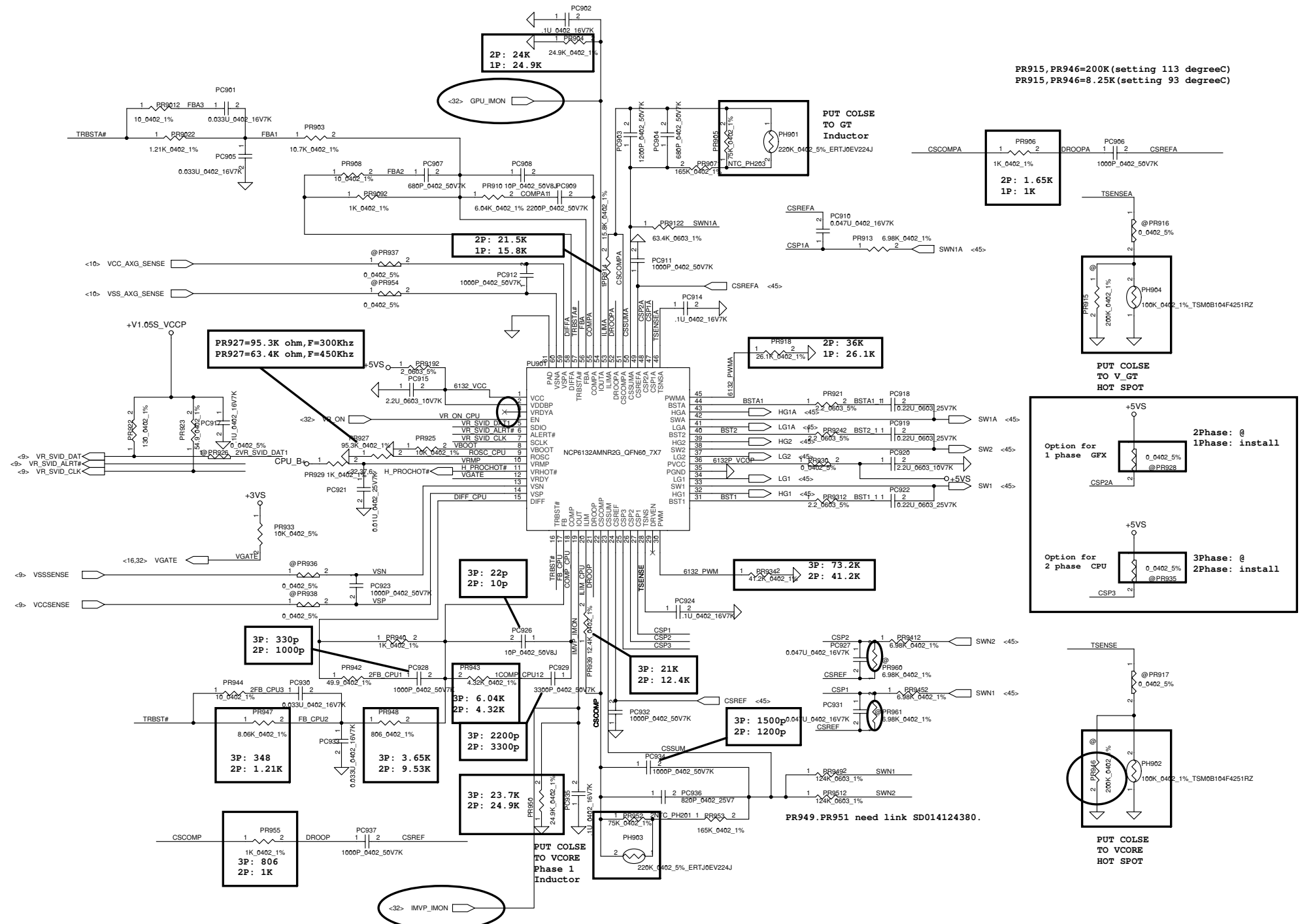
+1.05VS_VCCPP Ipeak=15.2A ; Imax=10.64A
 Delta I=2.48=>1/2Delta I=1.24A (F=400K Hz) D-CAP 2
 Rds (on)=3.3m ohm(max) ; Rds (on)=2.7m ohm(typical)
 PR711=47K ohm
 $V_{trip}=(R_{trip} \cdot 10\mu A) / 8 = 58.75mV$
 Iocp=19.043-22.999A



+1.05VP
 OCP min 20A
 OVP min 1.24V

Rds (on)=2.7m 3.3m ohm

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PR915, PR946=200K(setting 113 degreeC)
 PR915, PR946=8.25K(setting 93 degreeC)

PUT COLSE
 TO GT
 Inductor

2P: 1.65K
 1P: 1K

2P: 21.5K
 1P: 15.8K

PR927=95.3K ohm, F=300Khz
 PR927=63.4K ohm, F=450Khz

2P: 36K
 1P: 26.1K

PUT COLSE
 TO V_GT
 HOT SPOT

Option for
 1 phase GFX
 2Phase: @
 1Phase: install

Option for
 2 phase CPU
 3Phase: @
 2Phase: install

3P: 22p
 2P: 10p

3P: 73.2K
 2P: 41.2K

3P: 330p
 2P: 1000p

3P: 21K
 2P: 12.4K

3P: 348
 2P: 1.21K

3P: 3.65K
 2P: 9.53K

3P: 6.04K
 2P: 4.32K

3P: 2200p
 2P: 3300p

3P: 1500p
 2P: 1200p

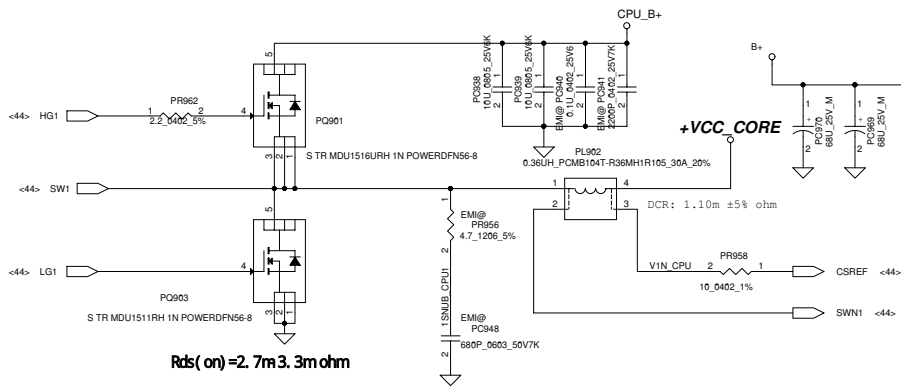
3P: 806
 2P: 1K

PUT COLSE
 TO VCORE
 Phase 1
 Inductor

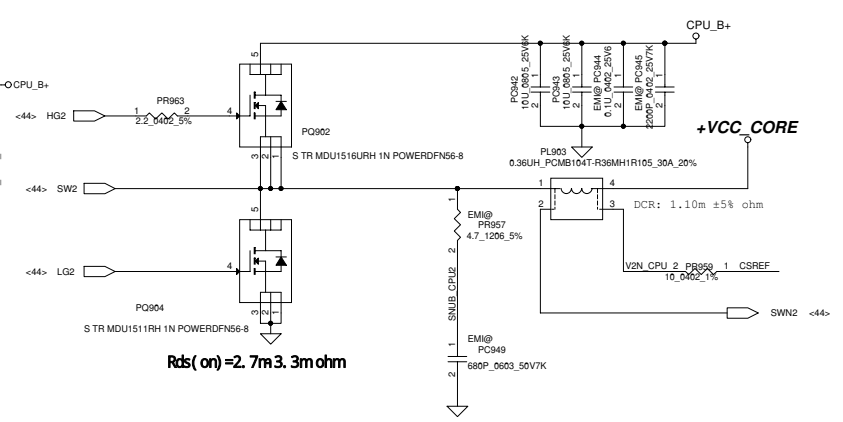
PUT COLSE
 TO VCORE
 HOT SPOT

PR949, PR951 need link SD014124380.

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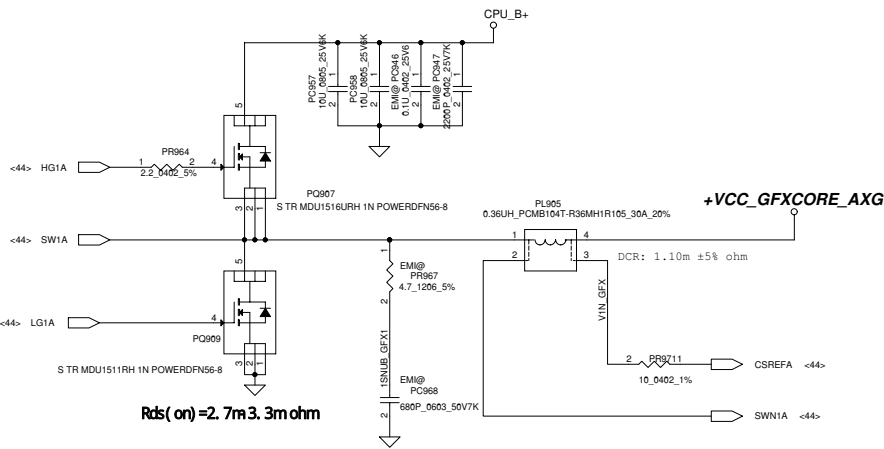
Rds(on) = 2.7m 3.3m ohm



Rds(on) = 2.7m 3.3m ohm

QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A

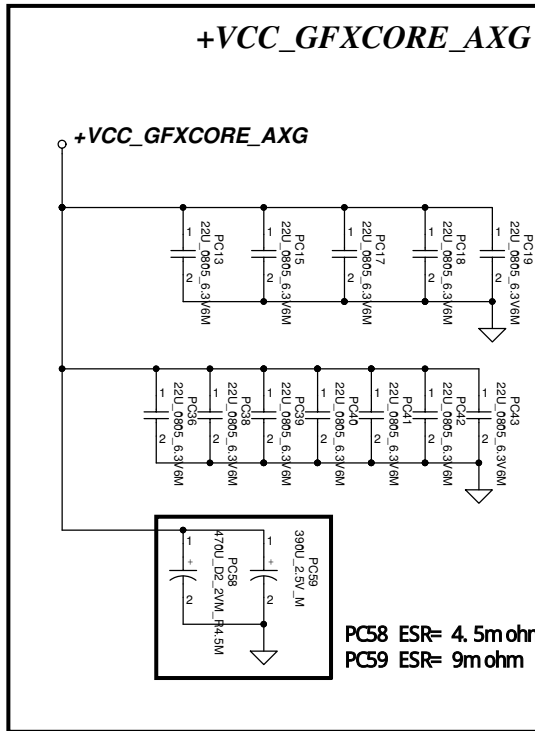
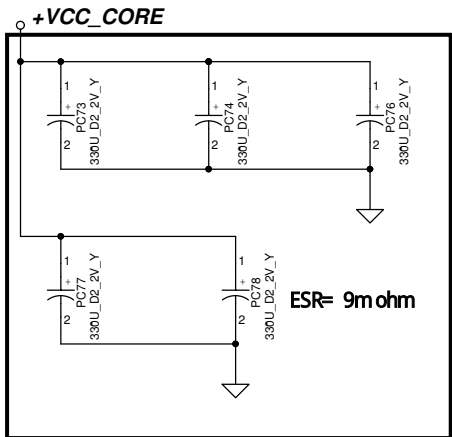
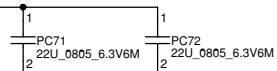
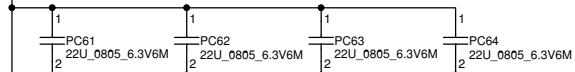
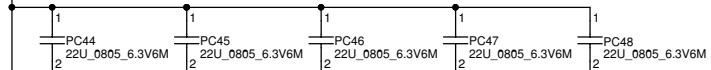
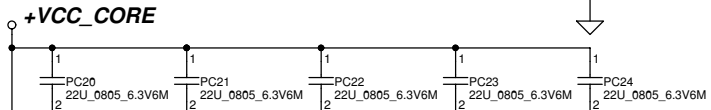
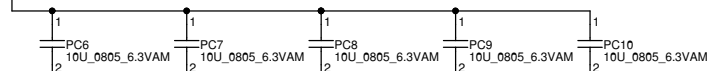
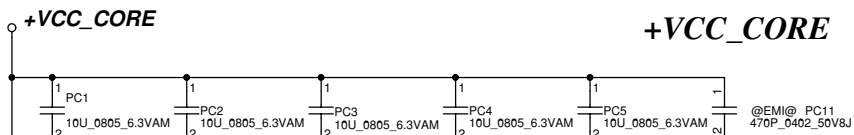


Rds(on) = 2.7m 3.3m ohm

QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

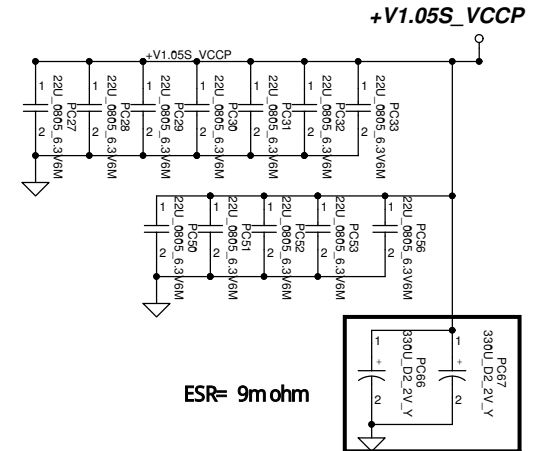
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

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Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Design Change of IC Package.	40	Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM)	2012/11/22	DVT
2	Design Change of IC Package.	40	Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM)	2012/11/22	DVT
3	Add ADP_ID Circuit.	37	Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402)	2012/12/03	DVT
4	Factory lack of material.	41	Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL)	2012/12/06	DVT
5	Factory lack of material.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2012/12/06	DVT
6	EMI request adjust +3VALWP/+5VALWP snubber function.	40	Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429.	2012/12/06	DVT
7	EMI request adjust +3VALWP/+5VALWP boost resistor.	40	Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603).	2012/12/06	DVT
8	EMI request add bypass capacitor.	40	Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6)	2012/12/06	DVT
9	EMI request adjust CPU/GFX CORE snubber function.	45	Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968.	2012/12/06	DVT
10	EMI request adjust bypass capacitor.	45	Change @PC940 to PC940.	2012/12/06	DVT
11	EMI request add bypass capacitor.	45	Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402)	2012/12/06	DVT
12	Design Change of input capacitor.	40	Change PC420 to SE000000F80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Add PC427 to SE000000F80(S CER CAP 4.7U 25V K X6S 0805 H1.25)	2012/12/07	DVT
13	Design Change of IC Application.	40	Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/10	DVT
14	Design Change of IC Application.	44	Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402) Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402) Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402) Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR943 to SD00000J280(S RES 1/16W 4.32K +-1% 0402) Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO)	2012/12/17	DVT
15	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A)	2012/12/21	DVT
16	Design Change of VCCSA(LDO).	42	Delete PC607.PC608.PC609.PC610.PC611.PC612.PC613.PC614.PJ603.PJ604.PR608.PR609.PR610.PR611.PU602	2012/12/21	DVT
17	Reduction Part Count.	37	Delete PR110.	2013/01/18	PVT
18	Reduction Part Count.	42	Delete PR603.	2013/01/18	PVT
19	Reduction Part Count.	44	Delete PC916.	2013/01/18	PVT
20	Design Change of IC Application.	40	Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410. Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT

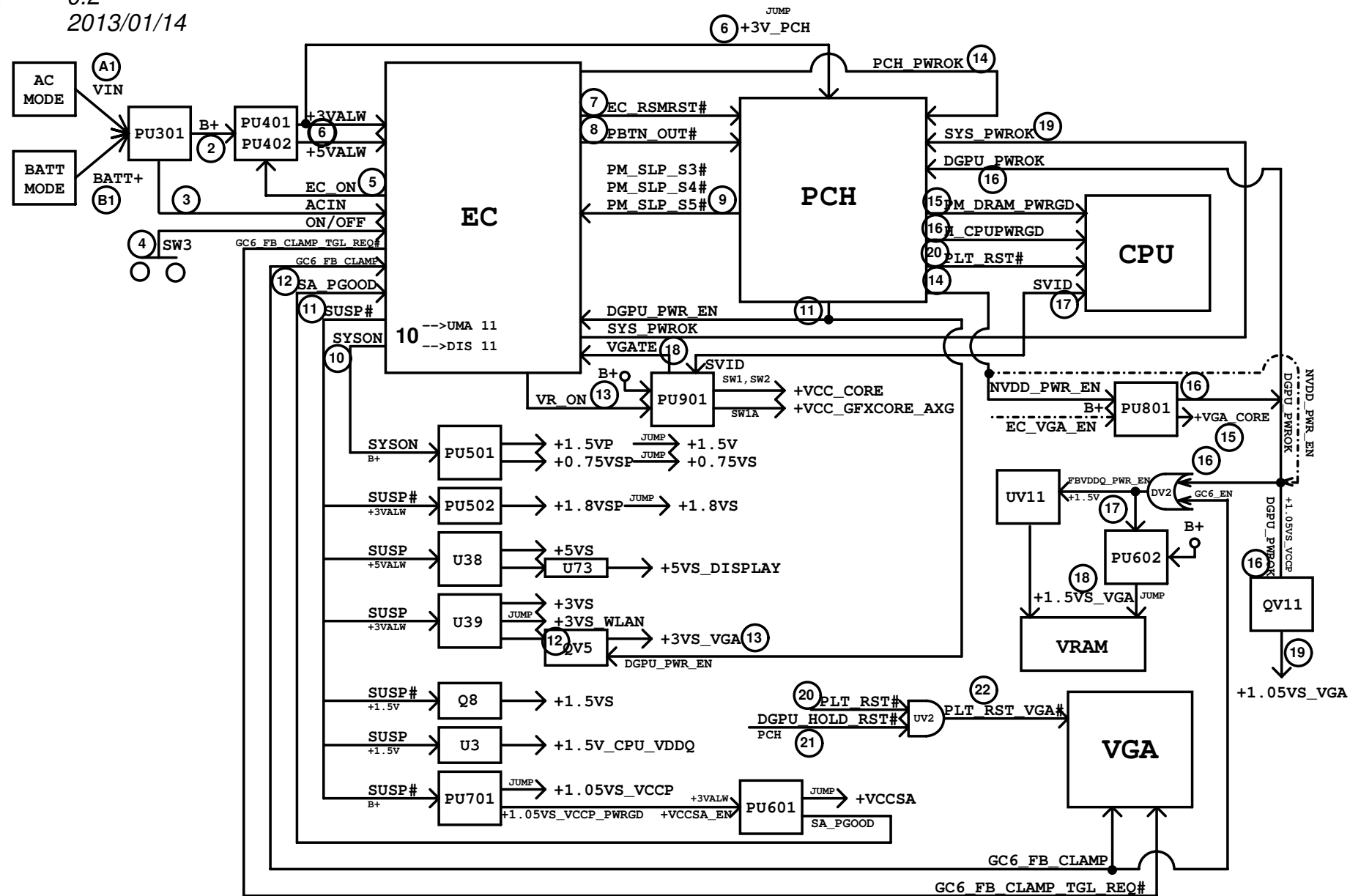
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Item	Reason for change	PG#	Modify List	Date	Phase
21	Reduction Part Count.	41	Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603)	2013/01/18	PVT
22	Design Change of Thermal Application.	41	Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2013/01/18	PVT
23	Reduction Part Count.	43	Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
24	Reduction Part Count.	44	Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
25	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2013/01/18	PVT
26	Design Change of CPU/GFX CORE Frequence.	44	Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402)	2013/01/18	PVT
27	Factory lack of material.	40	Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	2013/01/18	PVT
28	Reduction Part Count.	40	Delete PR411.	2013/01/21	PVT
29	Design Change of Power Circuit Application.	38	Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402)	2013/01/23	PVT
30	Design Change of Power Circuit Application.	39	Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402) Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3)	2013/01/23	PVT
31	Design Change of Power Circuit Application.	40	Change PC405 to SE072103280(S CER CAP .01U 25V Z Y5V 0402) Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402)	2013/03/04	PVT
32	Design Change of Power Circuit Application.	42	Add PR608 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/03/14	Pre-MP

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MODEL NAME: Power Sequence Block Diagram
 PCB NAME: LA-9901P
 REVISION: 0.2
 DATE: 2013/01/14



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VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 5~11	Change footprint of JCPU1	For Lenovo rule
2	P. 14	Add R406, R407, R408, R409	Reserve for improvement factory processes
3	P. 42	Add EC_SPI_SQ, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
4	P. 42	Add PCH_PWR_EN to EC Pin. 107	Reserve for improvement factory processes
5	P. 42	Reserve R410	Reserve Pull-high for GPIO use
6	P. 42	Change EC_FAN_PWM from EC Pin. 34 to EC Pin. 26	For common design
7	P. 42	Change NVO# from EC Pin. 26 to EC Pin. 34	For common design
8	P. 42	Change ENBKL from EC Pin. 73 to EC Pin. 76	For common design
9	P. 42	Change IMWP_IMDN from EC Pin. 76 to EC Pin. 73	For common design
10	P. 42	Change DGPU_PWR_EN from EC Pin. 107 to EC Pin. 123	For common design
11	P. 34	Add R411, R412, C411, C412	Reserve for EM
12	P. 20	Add Q21, R40, C237, Q22, R418, C243, C252, R413	Reserve for power consumption
13	P. 25	Del Q12/R806	For Change Audio Jack type from Nbrnal close to Nbrnal open

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VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	
1	P. 26	Reserve R508	For leakage current issue of Atheros WLAN	DVT TO PVT
2	P. 31	Change RA22 to reserve	For PC Beep issue(can't heard sound of "di" on BIOS setup menu)	
3	P. 31	Reserve RA10/RA11	For solve Codec speaker Humnoise issue(Zi zi)	
4	P. 32	Reserve R416	Reserve +3VLP power rail to EC	
5	P. 32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC	
6	P. 32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC	
7	P. 14	Change U5 from 4MB to 8MB ROM	Follow common design	
1	P. 32	Change R416 to shortpad		PVT TO Pre-MP
2	P. 42	Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PG00D	For Celeron/Pentium CPU	

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