Compal Confidential

C560 LA-A061P Schematics Document

INTEL Haswell CPU with DDRIII + PCH Lynx-Point

AIO M/B

September 24, 2013

REV:1.0

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Title: *Cover Page*			
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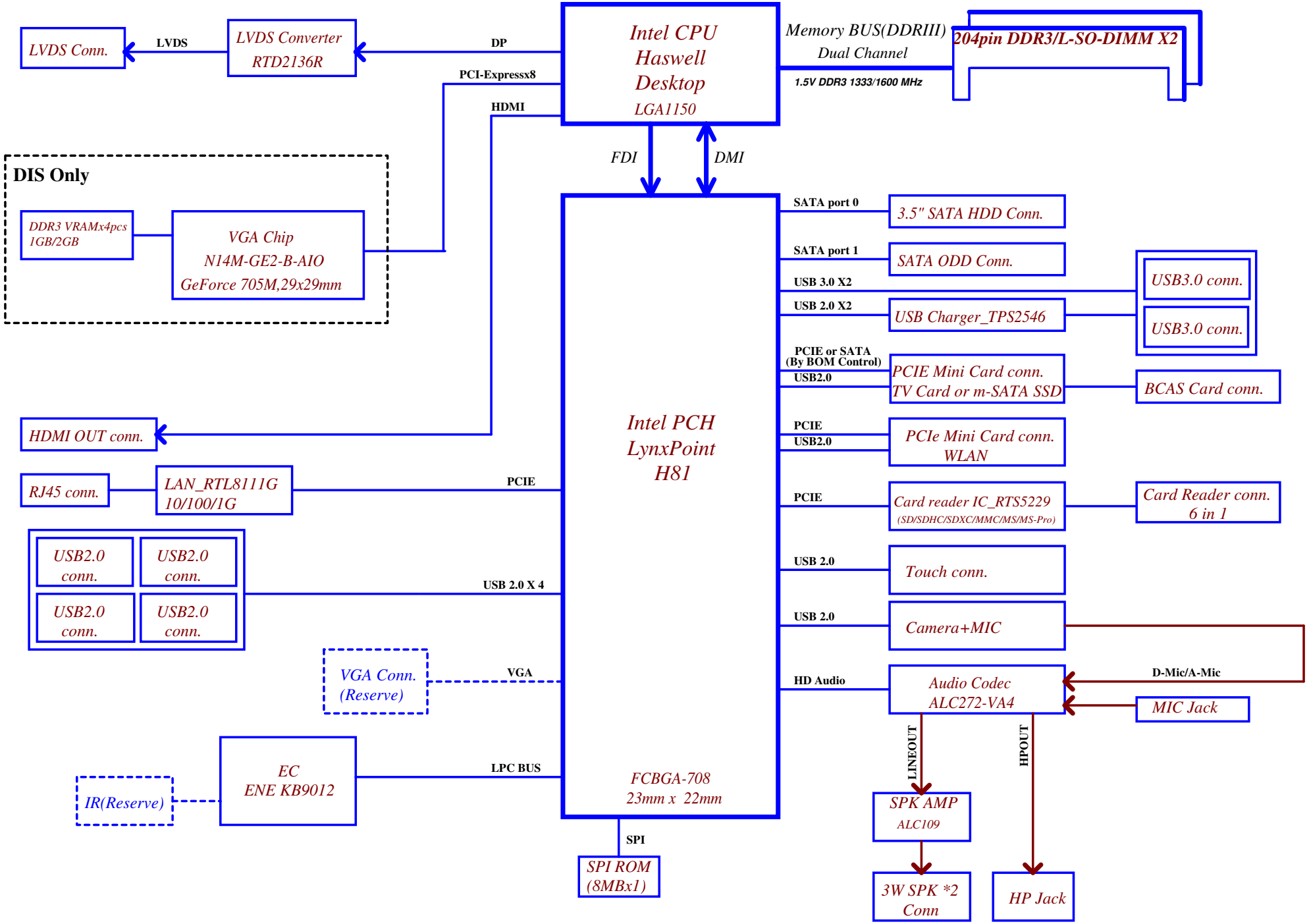

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Title: **Block Diagram**

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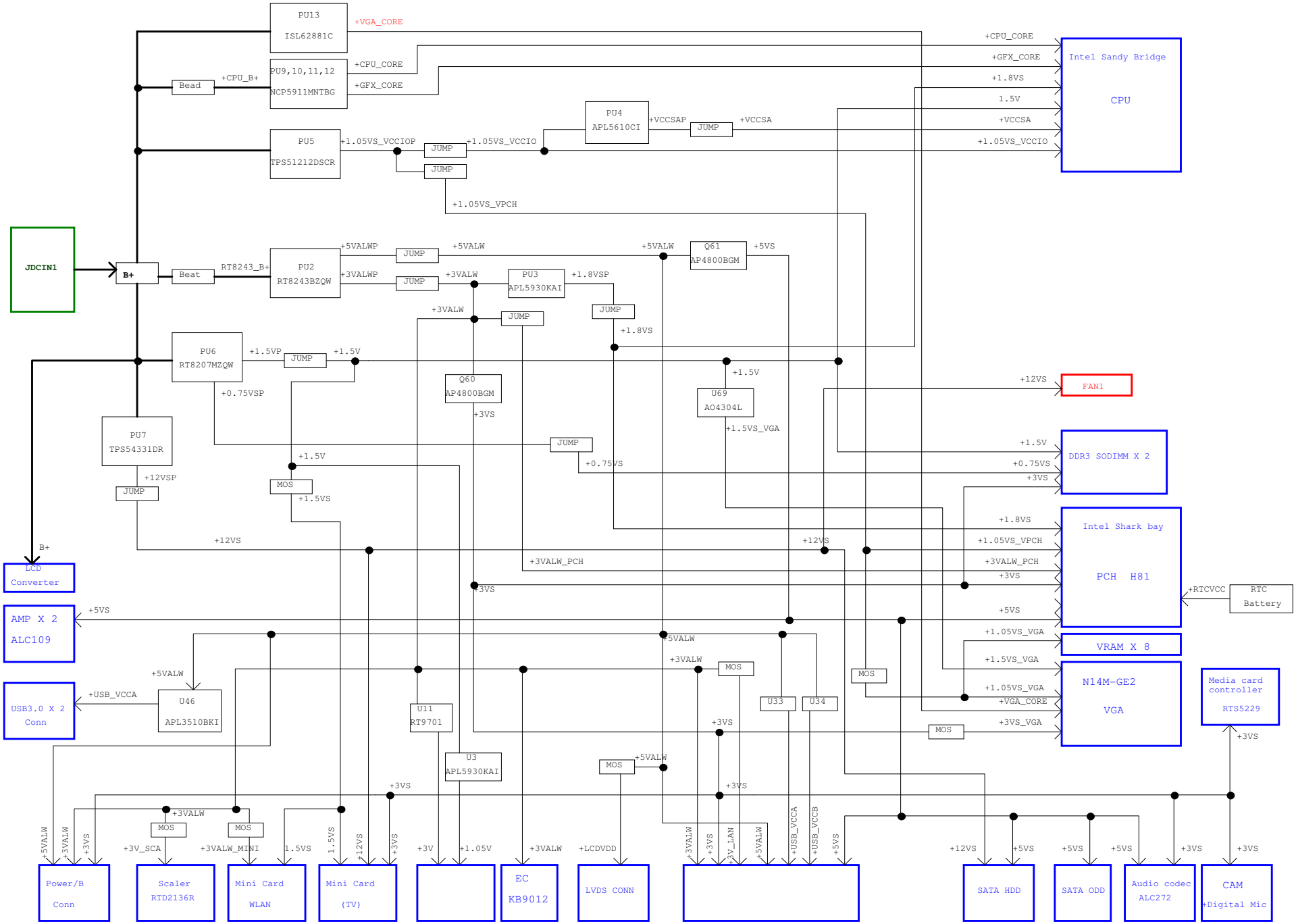

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Title: **Power Tree**

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STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW *1	+VS *2	+1.5V	+0.75VS	+RTCVCC
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	OFF	ON	OFF	ON
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF	ON
S5(Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF	ON

Note:

*1:+VALW power reail include +3VALW,+5VALW,B+,+VSB,+3VALW_PCH

*2:+VS power reail include +3VS,+5VS,+12VS,+1.05VS_VPCH,+1.5VS_VGA,+VGA_CORE,+CPU_CORE

USB Port Table

USB 2.0	USB 1.1	Port	Device
RMH1	UHCI0	0	Co-lay w/USB30 PORT0
		1	Co-lay w/USB30 PORT1(Debug)
	EHCI1	2	Rear IO USB20 Conn
		3	Rear IO USB20 Conn
	UHCI2	4	WLAN
		5	Touch
	UHCI3	6	Disabled on H81
		7	Disabled on H81
RMH2	UHCI4	8	Rear IO USB20 Conn
		9	Rear IO USB20 Conn(Debug)
	UHCI5	10	TV
		11	Camera
	UHCI6	12	Disabled on H81
		13	Disabled on H81

BOM Structure Table

BTO Item	BOM Structure
ME components	CONN@
UMA Only	UMA@
DISCRETE Only	DIS@
EMI Pop components	EMI@
ESD Pop components	ESD@
EMI Unpop components	@EMI@
ESD Unpop components	@ESD@
HDMI OUT	HDMIO@
TV	TV@
SSD	SSD@
CRT	CRT@ (EVTonly)
Unpop	@
VRAM select	X76@
EVT for Reserve components	EVT@
PCB	PCB@
SKU IO Select	GPIO68_H@
	GPIO68_L@
	GPIO69_H@
	GPIO69_L@
	GPIO70_H@
	GPIO70_L@
Touch	TOUCH@
Non Charger	NCHG@
Charger	CHG@

SATA Port Table

Port		Device
6G	0	HDD
	1	m-SATA
3G	2	Disabled on H81
	3	Disabled on H81
	4	ODD
	5	NC

PCIE Port Table

Port	Device
1	LAN
2	Card Reader
3	WLAN
4	TV
5	NC
6	NC
7	Disabled on H81
8	Disabled on H81

BOARD ID Table

Board ID	PCB Revision
0	0.1
3	0.2
4	0.3
5	

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR(JDDRL2)		1010 000X b
+3VS	DDR(JDDRH1)		1010 010X b

EC SM Bus1 Address

Power	Device	HEX	Address
	ALC106	48H	0100_100xb

PCH SML1 Bus Address

Power	Device	HEX	Address
	VGA Ext. thermal sensor		
	VGA Int. thermal sensor (default)		0x9b

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00 - 0xDC
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31 - 0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A - 0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A - 0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F - 0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC - 0xFF

SKU ID(Project) Table

Project_ID2 (GPIO68)	Project_ID1 (GPIO69)	Project_ID0 (GPIO70)	SKU	
0	0	0	UMA 4519QH38L04	TV@ NLDO@ EMI@ 8111G@ ESD@ CHG@ GPIO68_L@ GPIO69_L@ GPIO70_L@ PCB@
0	0	1	UMA_W/HDMI 4519QH38L05	HDMIO@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_L@ GPIO69_L@ TOUCH@ GPIO70_H@ PCB@
0	1	0	DIS-MIC1G 4519QH38L06	DIS@ NLDO@ EMI@ 8111G@ ESD@ TOUCH@ GPIO68_L@ GPIO69_H@ GPIO70_L@ PCB@
0	1	1	DIS-SAM1G_W/HDMI 4519QH38L07	DIS@ HDMIO@ TV@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_L@ GPIO69_H@ GPIO70_H@ PCB@
1	0	0	DIS-MIC2G_W/HDMI 4519QH38L08	DIS@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_H@ GPIO69_L@ TOUCH@ GPIO70_L@ PCB@
1	0	1	DIS-MIC2G_W/HDMI 4519QH38L09	DIS@ HDMIO@ TV@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_H@ GPIO69_L@ TOUCH@ GPIO70_L@ PCB@
1	1	0		
1	1	1		

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Title: Notes List

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Trace width=12mil, spacing 20mil, max L=500mil

PECI 10mil spacing and Max Length < 15"

R11 follow CDB R42PR add 0ohm serial resistor

R12 follow CDB R34PR add 0ohm serial resistor

ESD request Close to CPU as possible

Place C6 close to CPU pin J40 as close as possible. No stub

100 MHz

For BDW new CPU

v0.2 update

HDMI OUT (To Conn.)

FDI For VGA

eDP brightness

eDP (To LVDS Converter)

DP_RCOMP trace width=20mil spacing 25mil length<200mil

ESD request Close to JCPU1 G40

v1.0 update

v0.2 update

PU/PD for JTAG signals

v0.2 update
ESD request Close to JCPU1

Table 8-1. Configuration-wise Mapping of HDMI signals for Processor on DDI ports

Port	Digital Display Interface Differential Pairs	HDMI Signals	Processor Digital Display Interface Pins
Port B	DDIB_TXBP0	HDMIB_TX2_DP	DDIB_TXB[0]
	DDIB_TXBN0	HDMIB_TX2_DN	DDIB_TXB#[0]
	DDIB_TXBP1	HDMIB_TX1_DP	DDIB_TXB[1]
	DDIB_TXBN1	HDMIB_TX1_DN	DDIB_TXB#[1]
	DDIB_TXBP2	HDMIB_TX0_DP	DDIB_TXB[2]
	DDIB_TXBN2	HDMIB_TX0_DN	DDIB_TXB#[2]
	DDIB_TXBP3	HDMIB_CLK_DP	DDIB_TXB[3]
	DDIB_TXBN3	HDMIB_CLK_DN	DDIB_TXB#[3]
	DDPB_HPD	DDSP_1_HPD0	Hot plug detect used by HDMI Port B
	DDPB_CTRLCLK	DDPB_CTRL_CLK	HDMI DDC lines for Port B
	DDPB_CTRLDATA	DDPB_CTRL_CLK	
Port C	DDIC_TXBP0	HDMIC_TX2_DP	DDIC_TXB[0]
	DDIC_TXBN0	HDMIC_TX2_DN	DDIC_TXB#[0]
	DDIC_TXBP1	HDMIC_TX1_DP	DDIC_TXB[1]
	DDIC_TXBN1	HDMIC_TX1_DN	DDIC_TXB#[1]
	DDIC_TXBP2	HDMIC_TX0_DP	DDIC_TXB[2]
	DDIC_TXBN2	HDMIC_TX0_DN	DDIC_TXB#[2]
	DDIC_TXBP3	HDMIC_CLK_DP	DDIC_TXB[3]
	DDIC_TXBN3	HDMIC_CLK_DN	DDIC_TXB#[3]
	DDPC_HPD	DDSP_2_HPD1	Hot plug detect used by HDMI Port C
	DDPC_CTRLCLK	DDPC_CTRL_CLK	HDMI DDC lines for Port C
	DDPC_CTRLDATA	DDPC_CTRL_CLK	
Port D	DDID_TXBP0	HDMID_TX2_DP	DDID_TXB[0]
	DDID_TXBN0	HDMID_TX2_DN	DDID_TXB#[0]
	DDID_TXBP1	HDMID_TX1_DP	DDID_TXB[1]
	DDID_TXBN1	HDMID_TX1_DN	DDID_TXB#[1]
	DDID_TXBP2	HDMID_TX0_DP	DDID_TXB[2]
	DDID_TXBN2	HDMID_TX0_DN	DDID_TXB#[2]
	DDID_TXBP3	HDMID_CLK_DP	DDID_TXB[3]
	DDID_TXBN3	HDMID_CLK_DN	DDID_TXB#[3]
	DDPD_HPD	DDSP_3_HPD2	Hot plug detect used by HDMI Port D
	DDPD_CTRLCLK	DDPD_CTRL_CLK	HDMI DDC lines for Port D
	DDPD_CTRLDATA	DDPD_CTRL_CLK	

PDG P132

HSW A0+LPT A0 change R21 to 4.7K, R19 to 3.3K

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Title: Haswell_JTAG/XDP/DDI

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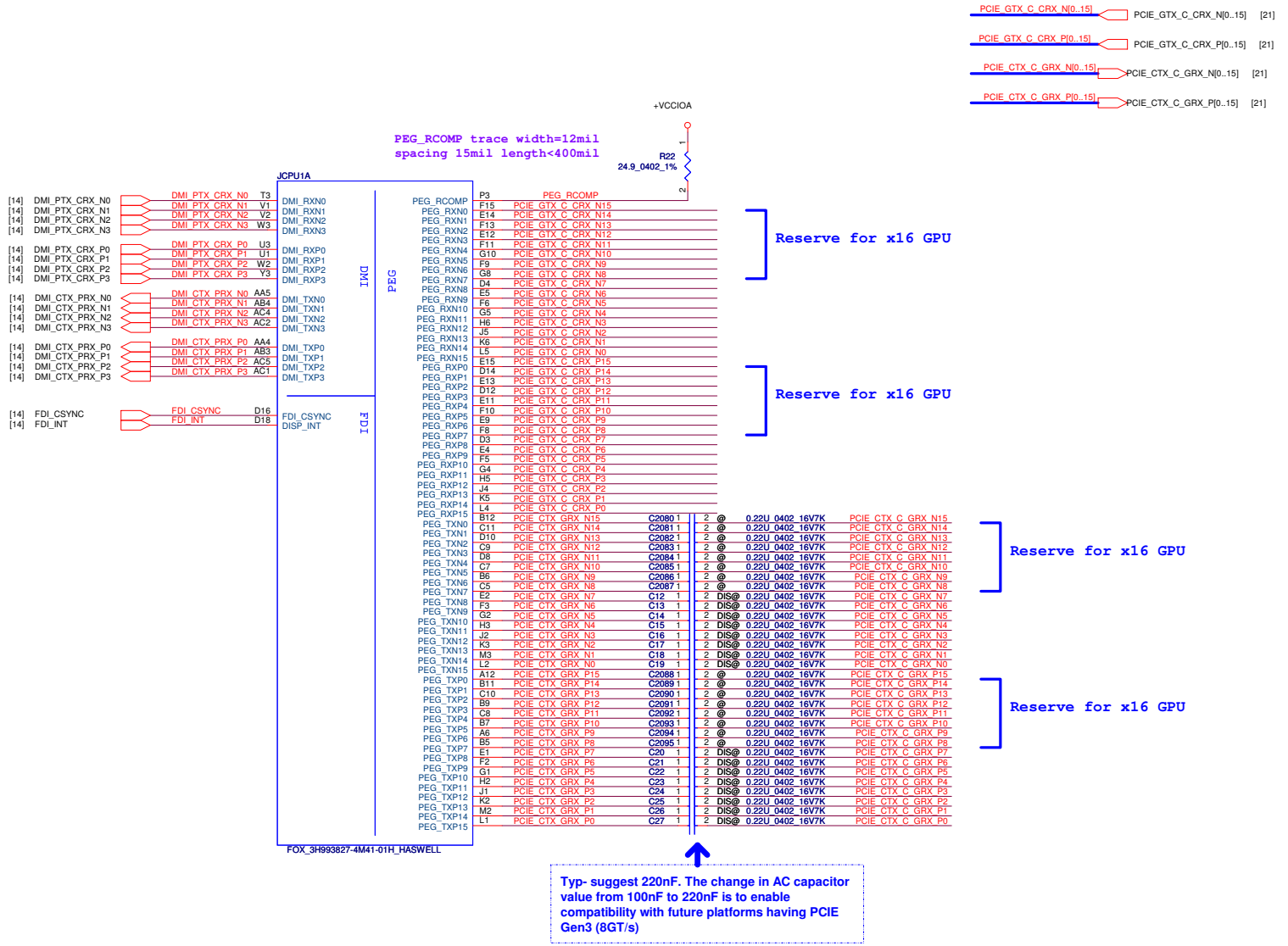

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Title: *Haswell_DMI/PEG/FDI*

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[10] DDR_A_D[0..63]

[11] DDR_B_D[0..63]

JCPU1C

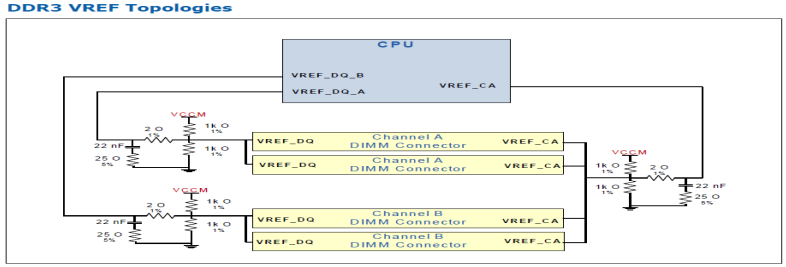
JCPU1D

+V_SM_VREF should have 20 mil trace width

FOX_3H993827-4M41-01H_HASWELL

FOX_3H993827-4M41-01H_HASWELL

DDR3 VREF Topologies



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Title: *Haswell_DDR3*

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

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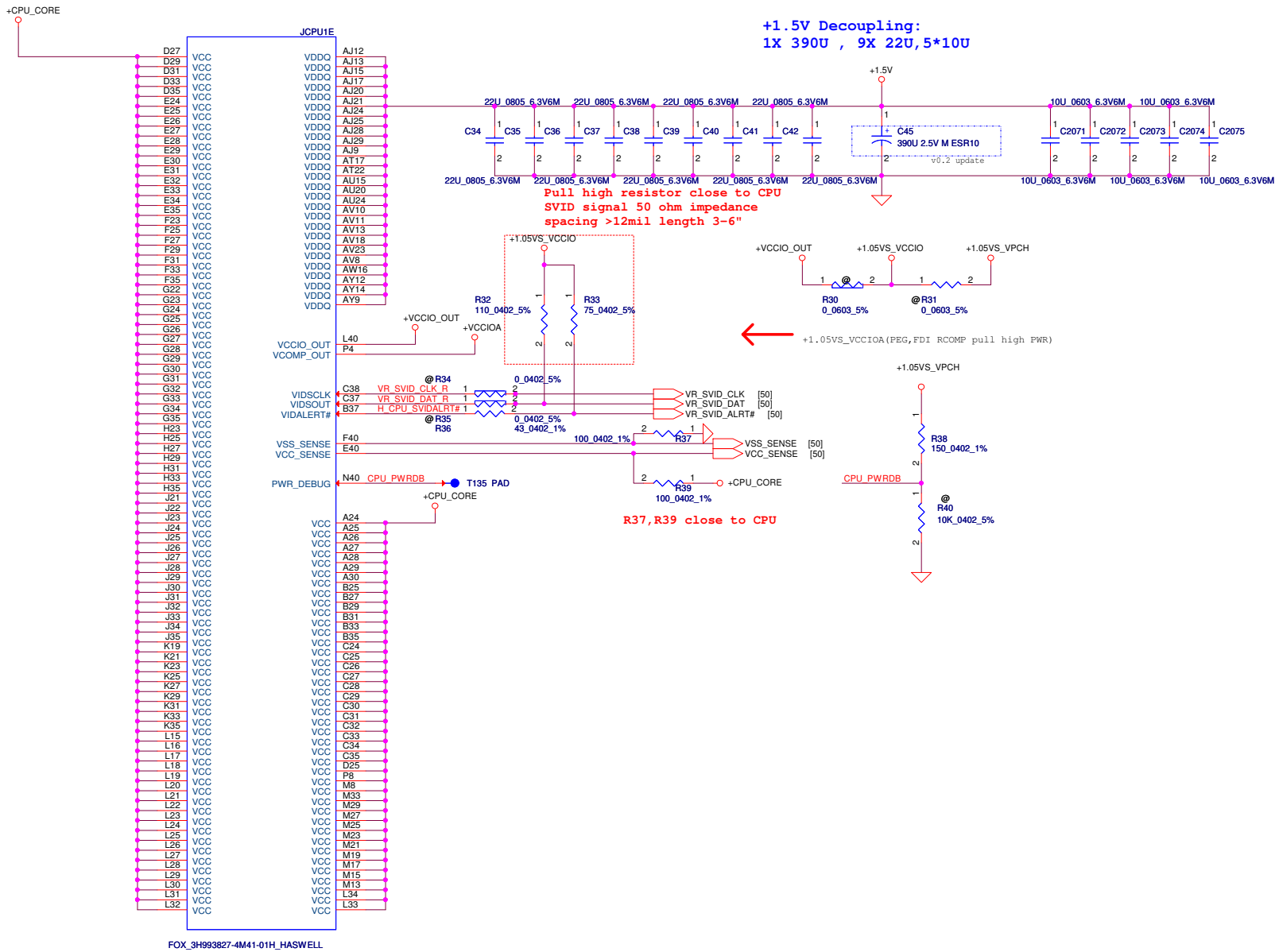

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Title	Haswell_POWER		
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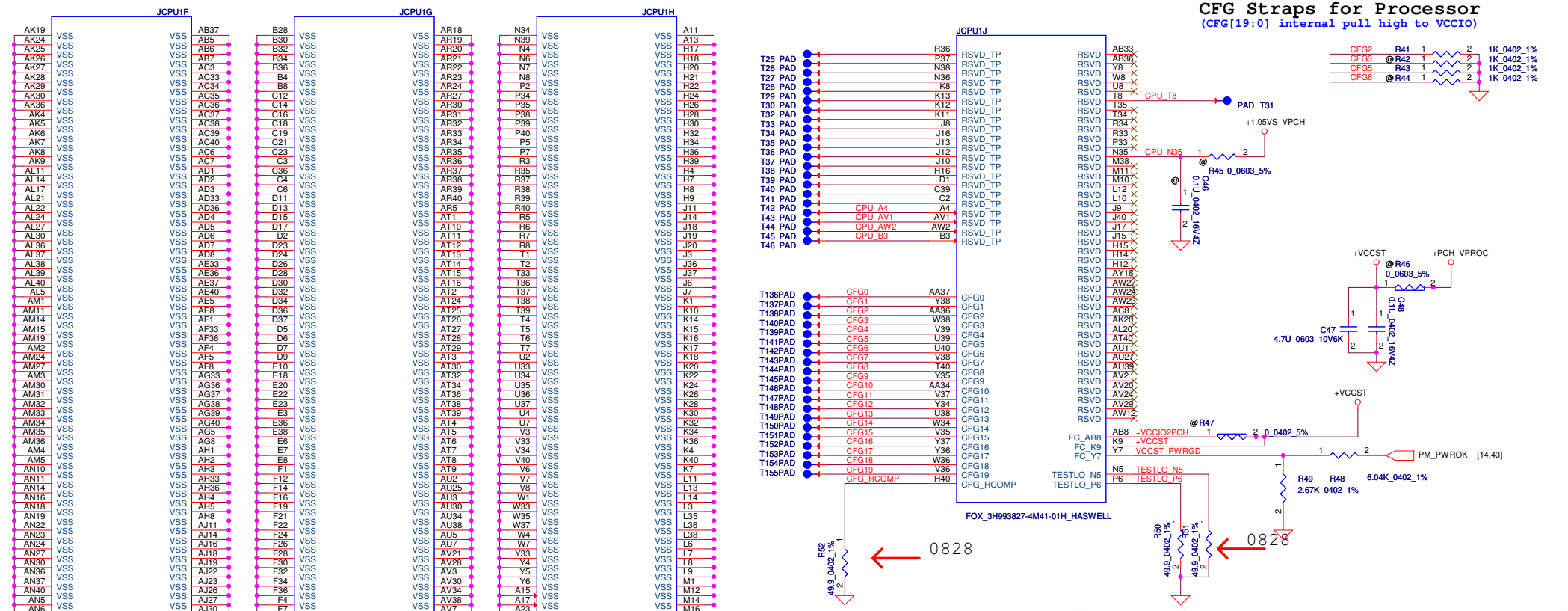

Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]: MSR Privacy Bit Feature** – 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting – 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** [1] – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.

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Title	Haswell_GND/CFG
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[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_D[0..63]
[7] DDR_A_MA[0..15]

CHA SO-DIMM 0(A0)

JDIMM1

R626 1K_0402_1% — +1.5V — +VREF_DQA
R627 1K_0402_1% — +VREF_DQA
C2030 0.1U_0402_16V4Z
C2031 2.2U_0603_6.3V6K
Close to JDIMM1

	VREF_DQ	1	2	VSS1		DDR_A_D4
DDR_A_D0	VSS2	3	4	DQ4		DDR_A_D5
DDR_A_D1	DQ0	5	6	DQ5		
	DQ1	7	8	VSS3		DDR_A_DQS#0
	VSS4	9	10	DQS#0		DDR_A_DQS0
DDR_A_D2	DM0	11	12	DQS0		
DDR_A_D3	VSS5	13	14	VSS6		DDR_A_D6
	DQ2	15	16	DQ6		DDR_A_D7
DDR_A_D8	DQ3	17	18	DQ7		
DDR_A_D9	VSS7	19	20	VSS8		DDR_A_D12
	DQ8	21	22	DQ12		DDR_A_D13
DDR_A_DQS#1	DQ9	23	24	DQ13		
DDR_A_DQS1	VSS9	25	26	VSS10		
	DQS#1	27	28	DM1		
DDR_A_D10	DQS1	29	30	RESET#		SM_DRAMRST# [11,5]
DDR_A_D11	VSS11	31	32	VSS12		DDR_A_D14
	DQ10	33	34	DQ14		DDR_A_D15
DDR_A_D16	DQ11	35	36	DQ15		
DDR_A_D17	VSS13	37	38	VSS14		DDR_A_D20
	DQ16	39	40	DQ20		DDR_A_D21
DDR_A_DQS#2	DQ17	41	42	DQ21		
DDR_A_DQS2	VSS15	43	44	VSS16		
	DQS#2	45	46	DM2		
DDR_A_D18	DQS2	47	48	VSS17		
DDR_A_D19	VSS18	49	50	DQ22		DDR_A_D22
	DQ18	51	52	DQ23		DDR_A_D23
DDR_A_D24	DQ19	53	54	VSS19		
DDR_A_D25	VSS20	55	56	DQ28		DDR_A_D28
	DQ24	57	58	DQ29		DDR_A_D29
DDR_A_D26	DQ25	59	60	VSS21		
DDR_A_D27	VSS22	61	62	DQS#3		DDR_A_DQS#3
	DM3	63	64	DQS3		DDR_A_DQS3
	VSS23	65	66	VSS24		
	DQ26	67	68	DQ30		DDR_A_D30
	DQ27	69	70	DQ31		DDR_A_D31
	VSS25	71	72	VSS26		
[7] DDRA_CKE0	CKE0	73	74	CKE1		DDRA_CKE1 [7]
	VDD1	75	76	VDD2		
	NC1	77	78	A15		DDR_A_MA15
[7] DDR_A_BS2	BA2	79	80	A14		DDR_A_MA14
	VDD3	81	82	VDD4		
DDR_A_MA12	A12/BC#	83	84	A11		DDR_A_MA11
DDR_A_MA9	A9	85	86	A7		DDR_A_MA7
	VDD5	87	88	VDD6		
DDR_A_MA8	A8	89	90	A6		DDR_A_MA6
DDR_A_MA5	A5	91	92	A4		DDR_A_MA4
	VDD7	93	94	VDD8		
DDR_A_MA3	A3	95	96	A2		DDR_A_MA2
DDR_A_MA1	A1	97	98	A0		DDR_A_MA0
	VDD9	99	100	VDD10		
DDRA_CLK0	CK0	101	102	CK1		DDRA_CLK1
[7] DDRA_CLK0 / DDRA_CLK0#	CK0#	103	104	CK1#		DDRA_CLK1# [7] / DDRA_CLK1 [7]
	VDD11	105	106	VDD12		
DDR_A_MA10	A10/AP	107	108	BA1		DDR_A_BS1
DDR_A_BS0	BA0	109	110	RAS#		DDR_A_RAS# [7] / DDR_A_BS1 [7]
	VDD13	111	112	VDD14		
DDR_A_WE#	WE#	113	114	S0#		DDRA_SCS0#
DDR_A_CAS#	CAS#	115	116	ODT0		DDRA_ODT0 [7] / DDRA_SCS0# [7]
	VDD15	117	118	VDD16		
DDR_A_MA13	A13	119	120	ODT1		DDRA_ODT1
DDRA_SCS1#	S1#	121	122	NC2		DDRA_ODT1 [7]
	VDD17	123	124	VDD18		
	NCTEST	125	126	VREF_CA		+VREF_CAA
DDR_A_D32	VSS27	127	128	VSS28		
DDR_A_D33	DQ32	129	130	DQ36		DDR_A_D36
	DQ33	131	132	DQ37		DDR_A_D37
DDR_A_DQS#4	VSS29	133	134	VSS30		
DDR_A_DQS4	DQS#4	135	136	DM4		
	VSS32	137	138	VSS31		
DDR_A_D34	DQ34	139	140	DQ38		DDR_A_D38
DDR_A_D35	DQ35	141	142	DQ39		DDR_A_D39
	VSS34	143	144	VSS33		
DDR_A_D40	DQ40	145	146	DQ44		DDR_A_D44
DDR_A_D41	DQ41	147	148	DQ45		DDR_A_D45
	VSS36	149	150	VSS35		
	DM5	151	152	DQS5		DDR_A_DQS#5
	VSS37	153	154	DQS#5		DDR_A_DQS5
DDR_A_D42	DQ42	155	156	VSS38		
DDR_A_D43	DQ43	157	158	DQ46		DDR_A_D46
	VSS39	159	160	DQ47		DDR_A_D47
DDR_A_D48	DQ48	161	162	VSS40		
DDR_A_D49	DQ49	163	164	DQ52		DDR_A_D52
	VSS41	165	166	DQ53		DDR_A_D53
DDR_A_DQS#6	DQS#6	167	168	VSS42		
DDR_A_DQS6	DQS6	169	170	DM6		
	VSS44	171	172	VSS43		
DDR_A_D50	DQ50	173	174	DQ54		DDR_A_D54
DDR_A_D51	DQ51	175	176	DQ55		DDR_A_D55
	VSS46	177	178	VSS45		
DDR_A_D56	DQ56	179	180	DQ60		DDR_A_D60
DDR_A_D57	DQ57	181	182	DQ61		DDR_A_D61
	VSS48	183	184	VSS47		
	DM7	185	186	DQS7		DDR_A_DQS#7
	VSS49	187	188	DQS#7		DDR_A_DQS7
DDR_A_D58	DQ58	189	190	VSS50		
DDR_A_D59	DQ59	191	192	DQ62		DDR_A_D62
	VSS51	193	194	DQ63		DDR_A_D63
	SA0	195	196	VSS52		
	VDDSPD	197	198	EVENT#		
	SA1	199	200	SDA		PM_SMBDATA [11,13,40,5]
	VTT1	201	202	SCL		PM_SMBCLK [11,13,40,5]
	G1	203	204	VTT2		+0.75VS
		205	206	G2		

FOX_AS0A626-U2SN-7F
CONN@

+3VS — C2048 2.2U_0603_6.3V6K — C2049 0.1U_0402_16V4Z — R630 @ 0_0402_5% — +0.75VS

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

Standard H:5.2mm

Layout Note: Place near JDIMM1

+1.5V
C2032 390U 2.5V M ESR10
C2033 10U_0805_6.3V6M
C2034 10U_0805_6.3V6M
C2035 10U_0805_6.3V6M
+1.5V
C2036 0.1U_0402_16V4Z
C2037 0.1U_0402_16V4Z
C2038 0.1U_0402_16V4Z
C2039 0.1U_0402_16V4Z
C2040 0.1U_0402_16V4Z
C2041 0.1U_0402_16V4Z
C2042 0.1U_0402_16V4Z
C2043 0.1U_0402_16V4Z

Layout Note: Place these Caps near +1.5V of JDIMM1

+1.5V — R628 1K_0402_1% — +VREF_CAA — R629 1K_0402_1%
C2044 2.2U_0603_6.3V6K — C2045 0.1U_0402_16V4Z
close to JDIMM1.126

Layout Note: Place near JDIMM1 Pin203 and 204

+0.75VS — C2046 4.7U_0603_6.3V6K — C2047 0.1U_0402_16V4Z

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Title: ***DDRIII-SODIMMA***

Size	Document Number	Rev
C	ZEA00 LA-A061P M/B	0.3

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[7] DDR_B_DQS#[0..7]
[7] DDR_B_DQS[0..7]
[7] DDR_B_D[0..63]
[7] DDR_B_MA[0..15]

CHB SO-DIMM

JDIMM2

1	VREF_DQ	VSS1	2		3	VSS2	DQ4	4	DDR_B_D4
5	DDR_B_D0	DQ0	DQ5	6	DDR_B_D5				
7	DDR_B_D1	DQ1	VSS3	8		9	VSS4	DQS#0	10	DDR_B_DQS#0
11	DDR_B_DQS0	DM0	DQS0	12		13	VSS5	DQ2	14	
15	DDR_B_D2	DQ3	VSS6	16	DDR_B_D6					
17	DDR_B_D3	DQ7	DQ6	18	DDR_B_D7					
19	DQ3	VSS7	20		21	DDR_B_D8	DQ8	VSS8	22	DDR_B_D12
23	DDR_B_D9	DQ9	DQ13	24	DDR_B_D13					
25	VSS9	VSS10	26		27	DDR_B_DQS#1	DQS#1	DM1	28	
29	DDR_B_DQS1	DQS1	RESET#	30	SM_DRAMRST#					
31	VSS11	VSS12	32		33	DDR_B_D10	DQ10	VSS12	34	DDR_B_D14
35	DDR_B_D11	DQ11	DQ14	36	DDR_B_D15					
37	VSS13	VSS14	38		39	DDR_B_D16	DQ16	DQ20	40	DDR_B_D20
41	DDR_B_D17	DQ17	DQ21	42	DDR_B_D21					
43	VSS15	VSS16	44		45	DDR_B_DQS#2	DQS#2	DM2	46	
47	DDR_B_DQS2	DQS2	VSS17	48		49	VSS18	DQ22	50	DDR_B_D22
51	DDR_B_D18	DQ18	DQ23	52	DDR_B_D23					
53	DDR_B_D19	DQ19	VSS19	54		55	VSS20	DQ28	56	DDR_B_D28
57	DDR_B_D24	DQ24	DQ29	58	DDR_B_D29					
59	DDR_B_D25	DQ25	VSS21	60		61	VSS22	DQS#3	62	DDR_B_DQS#3
63	DDR_B_DQS3	DM3	DQS3	64		65	VSS23	DQ26	66	DDR_B_D30
67	DDR_B_D26	DQ27	DQ30	68	DDR_B_D31					
69	DDR_B_D27	DQ31	VSS24	70		71	VSS25	VSS26	72	
[7] DDRB_CKE0	DDRB_CKE0	73	CKE0	CKE1	74	DDRB_CKE1	DDRB_CKE1 [7]			
75	VDD1	VDD2	76		77	NC1	A15	78	DDR_B_MA15	
[7] DDR_B_BS2	DDR_B_BS2	79	BA2	A14	80	DDR_B_MA14				
81	VDD3	VDD4	82		83	DDR_B_MA12	A12/BC#	A11	84	DDR_B_MA11
85	DDR_B_MA9	A9	A7	86	DDR_B_MA7					
87	VDD5	VDD6	88		89	DDR_B_MA8	A8	A6	90	DDR_B_MA6
91	DDR_B_MA5	A5	A4	92	DDR_B_MA4					
93	VDD7	VDD8	94		95	DDR_B_MA3	A3	A2	96	DDR_B_MA2
97	DDR_B_MA1	A1	A0	98	DDR_B_MA0					
99	VDD9	VDD10	100		101	DDRB_CLK0	CK0	CK1	102	DDRB_CLK1
[7] DDRB_CLK0	DDRB_CLK0#	103	CK0#	CK1#	104	DDRB_CLK1#	DDRB_CLK1 [7]			
[7] DDRB_CLK0#	DDRB_CLK1# [7]	105	VDD11	VDD12	106		107	DDR_B_MA10	A10/AP	BA1
108	DDR_B_BS1	DDR_B_BS1 [7]								
[7] DDR_B_BS0	DDR_B_BS0	109	BA0	RAS#	110	DDR_B_RAS#	DDR_B_RAS# [7]			
111	VDD13	VDD14	112		113	DDR_B_WE#	WE#	S0#	114	DDRB_SCS0#
[7] DDR_B_WE#	DDR_B_CAS#	115	CAS#	ODT0	116	DDRB_ODT0	DDRB_SCS0# [7]			
[7] DDR_B_CAS#	DDRB_ODT0 [7]	117	VDD15	VDD16	118		119	DDR_B_MA13	A13	ODT1
120	DDRB_ODT1	DDRB_ODT1 [7]								
[7] DDRB_SCS1#	DDRB_SCS1#	121	S1#	NC2	122		123	VDD17	VDD18	124
125	NCTEST	VREF_CA	126	+VREF_CAB	127	VSS27	VSS28	128		129
DDR_B_D32	130	DDR_B_D36	131	DDR_B_D33	DQ32	DQ36	132	DDR_B_D37		
133	VSS29	VSS30	134		135	DDR_B_DQS#4	DQS#4	DM4	136	
137	DDR_B_DQS4	DQS4	VSS31	138		139	VSS32	DQ38	140	DDR_B_D38
141	DDR_B_D34	DQ34	DQ39	142	DDR_B_D39					
143	DDR_B_D35	DQ35	VSS33	144		145	VSS34	DQ44	146	DDR_B_D44
147	DDR_B_D40	DQ40	DQ45	148	DDR_B_D45					
149	DDR_B_D41	DQ41	VSS35	150		151	VSS36	DQS#5	152	DDR_B_DQS#5
153	DDR_B_DQS5	DM5	DQS5	154		155	VSS37	VSS38	156	
157	DDR_B_D42	DQ42	DQ46	158	DDR_B_D46					
159	DDR_B_D43	DQ43	DQ47	160	DDR_B_D47					
161	VSS39	VSS40	162		163	DDR_B_D48	DQ48	DQ52	164	DDR_B_D52
165	DDR_B_D49	DQ49	DQ53	166	DDR_B_D53					
167	VSS41	VSS42	168		169	DDR_B_DQS#6	DQS#6	DM6	170	
171	DDR_B_DQS6	DQS6	VSS43	172		173	VSS44	DQ54	174	DDR_B_D54
175	DDR_B_D50	DQ50	DQ55	176	DDR_B_D55					
177	DDR_B_D51	DQ51	VSS45	178		179	VSS46	DQ60	180	DDR_B_D60
181	DDR_B_D56	DQ56	DQ61	182	DDR_B_D61					
183	DDR_B_D57	DQ57	VSS47	184		185	VSS48	DQS#7	186	DDR_B_DQS#7
187	DDR_B_DQS7	DM7	DQS7	188		189	VSS49	VSS50	190	
191	DDR_B_D58	DQ58	DQ62	192	DDR_B_D62					
193	DDR_B_D59	DQ59	DQ63	194	DDR_B_D63					
195	VSS51	VSS52	196		197	SA0	EVENT#	198		199
VDDSPD	PM_SMBDATA	200	SDA	PM_SMBDATA [10,13,40,5]						
201	SA1	SCL	202	PM_SMBCLK	PM_SMBCLK [10,13,40,5]					
203	VTT1	VTT2	204	+0.75VS	205	G1	G2	206		

SUYIN_600023HB204G208ZL
CONN@

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

R631 1K_0402_1% +1.5V +VREF_DQB
R632 1K_0402_1%
C2050 2.2U_0603_6.3V6K
C2051 0.1U_0402_16V4Z
Close to JDIMM2

+3VS R635 10K_0402_5% +0.75VS
@C2068 2.2U_0603_6.3V6K
C2069 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2

+1.5V
C2052 @ 390U 2.5V M ESR10
C2053 10U_0805_6.3V6M
C2054 10U_0805_6.3V6M
C2055 10U_0805_6.3V6M

+1.5V
C2056 0.1U_0402_16V4Z
C2057 0.1U_0402_16V4Z
C2058 0.1U_0402_16V4Z
C2059 0.1U_0402_16V4Z
C2060 0.1U_0402_16V4Z
C2061 0.1U_0402_16V4Z
C2062 0.1U_0402_16V4Z
C2063 0.1U_0402_16V4Z

Layout Note: Place these Caps near
+1.5V of JDIMM2

+1.5V R633 1K_0402_1% +VREF_CAB
R634 1K_0402_1%
C2064 2.2U_0603_6.3V6K
C2065 0.1U_0402_16V4Z
Close to JDIMM2

+0.75VS
C2066 4.7U_0603_6.3V6K
C2067 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2 Pin203 and 204

Standard H:9.2mm

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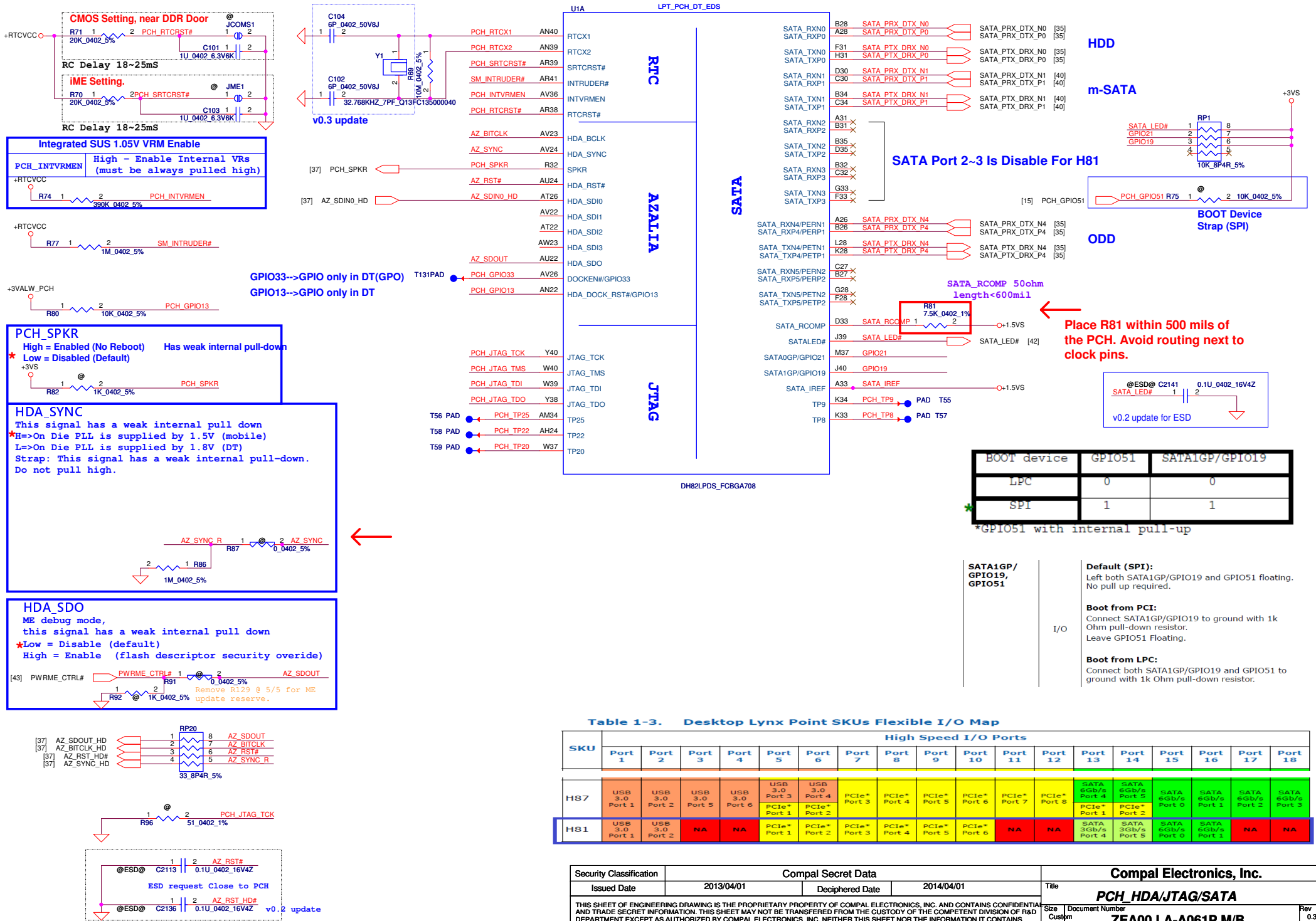

BOOT device	GPIO51	SATA1GP/GPIO19
LPC	0	0
SPI	1	1

*GPIO51 with internal pull-up

SATA1GP/ GPIO19, GPIO51	I/O	**Default (SPI):** Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required. **Boot from PCI:** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating. **Boot from LPC:** Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

Table 1-3. Desktop Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	NA	NA	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	NA	NA

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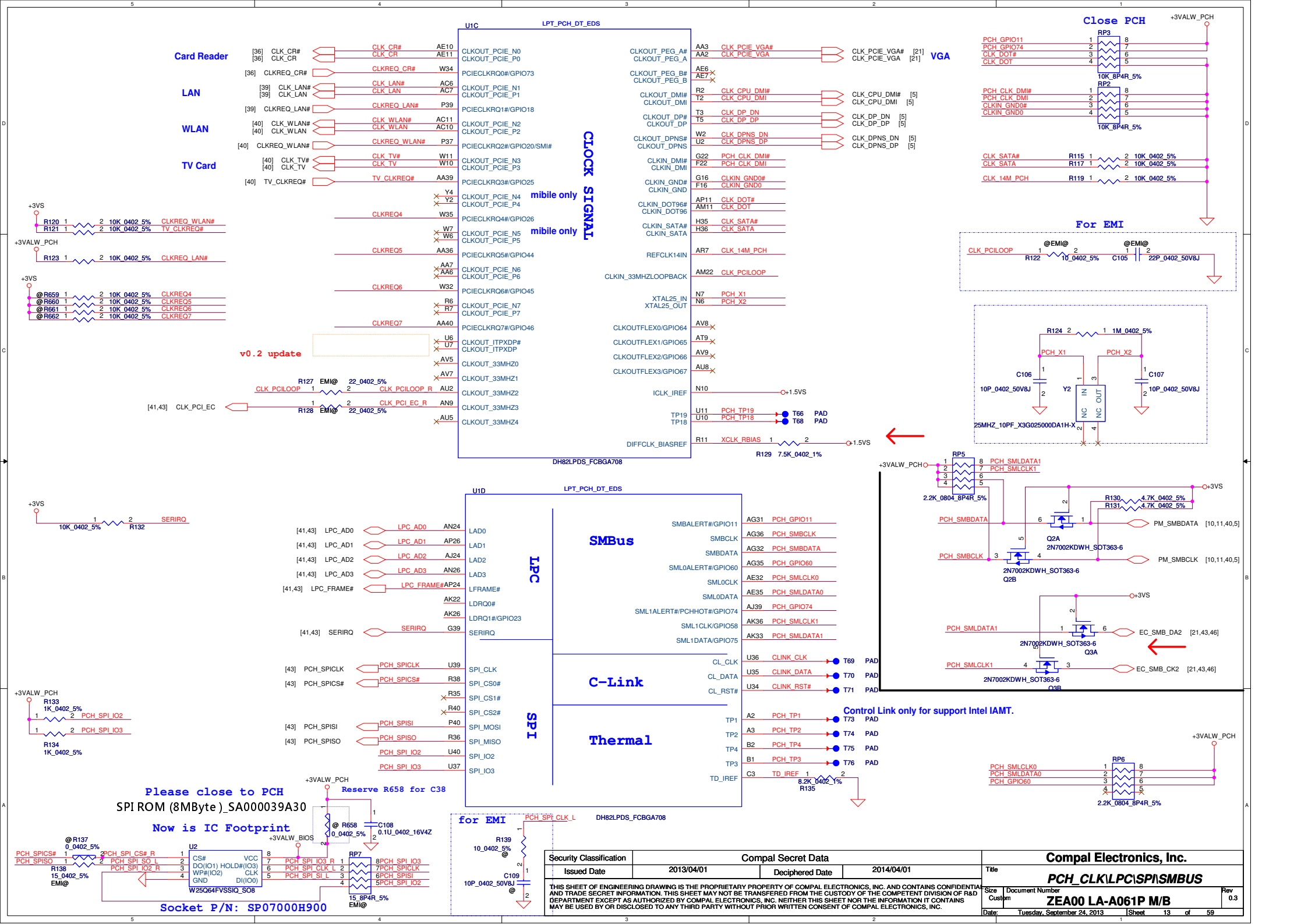
Close PCH
For EMI
Card Reader
LAN
WLAN
TV Card
VGA
CLOCK SIGNAL
mibile only
v0.2 update
U1C
LPT_PCH_DT_EDS
DH82LPDS_FCBGA708
U1D
LPC
SPI
SMBus
C-Link
Thermal
Control Link only for support Intel IAMT.
Please close to PCH
SPI ROM (8MByte)_SA000039A30
Now is IC Footprint
Reserve R658 for C38
Socket P/N: SP07000H900
for EMI
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PCH_CLK\LPC\SPI\SMBUS
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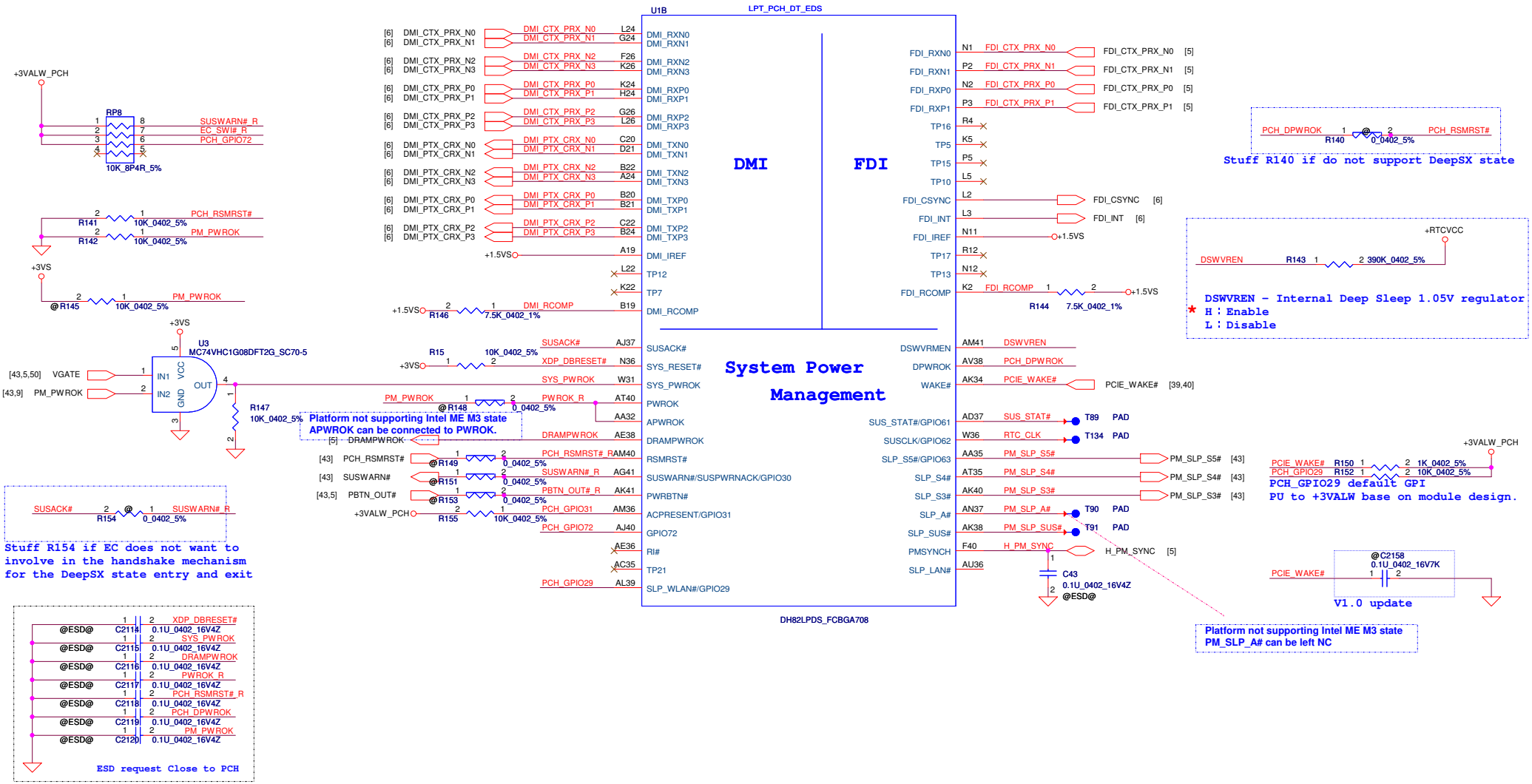

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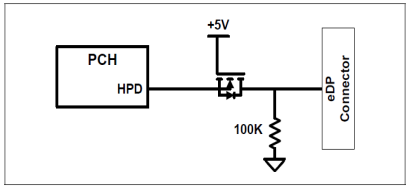
Figure 9-3. Processor Graphics eDP* HPD Signal off of Digital Port D



PCI PU resistor

RP9
PCI_PIRQD#
PCI_PIRQB#
PCH_GPIO5
PCI_PIRQC#
8.2K_8P4R_5%

R159 8.2K_0402_5% PCH_GPIO50
R160 8.2K_0402_5% PCH_GPIO52
R161 8.2K_0402_5% PCH_GPIO54

RP10
PCH_GPIO4
PCI_PIRQA#
PCH_GPIO3
PCH_GPIO2
8.2K_8P4R_5%

R162 CRT@ 2.2K_0402_5% PCH_CRT_CLK
R163 CRT@ 2.2K_0402_5% PCH_CRT_DATA

RP11
PCH_CRT_B
PCH_CRT_G
PCH_CRT_R
150_0804_8P4R_1% CRT@

Close to PCH <250mils

@R157 10K_0402_5% PCH_GPIO53
@R158 10K_0402_5% PCH_GPIO55

Internal pull high
Strap defalut high
GPIO53 DMI AC mode if Low
GPIO55 A16 SWAP OVERRIDE if Low

NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

RP17
PCH_DPD_CLK
PCH_DPD_DAT
PCH_HDMIOUT_CLK
PCH_HDMIOUT_DATA
2.2K_0804_8P4R_5%
+3VS

+5VS
Q57 BSS138LT1G_SOT23-3
DDPD_HPD
PCH_DDPD_HPD [29]
R605 @ 0_0402_5%
R606 100K_0402_5%

U1E LPT_PCH_DT_EDS

Data Need longer than CLK 1 inch

HDMI OUT (To Conn.)

eDP (LVDS Converter)

Seperate U10, U57 location

CRT
[41] PCH_CRT_B AC3 VGA_BLUE
[41] PCH_CRT_G AE2 VGA_GREEN
[41] PCH_CRT_R AC2 VGA_RED
[41] PCH_CRT_CLK AL2 VGA_DDC_CLK
[41] PCH_CRT_DATA AL3 VGA_DDC_DATA
[41] PCH_CRT_HSYNC AH3 VGA_HSYNC
[41] PCH_CRT_VSYNC AH2 VGA_VSYNC
CRT_IREF AF5 DAC_IREF
R165 649_0402_1% AG4 VGA_IRTN

Disable use 1K on mobile
CRT_IREF Close to PCH <500mils

LVDS
To Converter [29] PCH_EDP_PWM AP2 EDP_BKLTCTL
[29] PCH_EDP_BLEN AT2 EDP_BKLTEN
v0.2 update T133 PAD PCH_EDP_VDDEN AP1 EDP_VDDEN

DISPLAY

PCI
PCI_PIRQA# AU29 PIRQA#
PCI_PIRQB# AU27 PIRQB#
PCI_PIRQC# AW28 PIRQC#
PCI_PIRQD# AV27 PIRQD#
[21,43] DGPU_HOLD_RST# @R167 0_0402_5% PCH_GPIO50 AH26 GPIO50
PCH_GPIO52 AJ26 GPIO52
[23,43] DGPU_PWR_EN @R170 0_0402_5% PCH_GPIO54 AW33 GPIO54
[12] PCH_GPIO51 PCH_GPIO51 AU31 GPIO51
PCH_GPIO53 AV31 GPIO53
PCH_GPIO55 R30 GPIO55

DDPB_CTRLCLK AM1 PCH_HDMIOUT_CLK → PCH_HDMIOUT_CLK [30]
DDPB_CTRLDATA AJ5 PCH_HDMIOUT_DATA → PCH_HDMIOUT_DATA [30]
DDPC_CTRLCLK AN3 PCH_HDMI_CLK → PAD T92
DDPC_CTRLDATA AM2 PCH_HDMI_DATA → PAD T93
DDPD_CTRLCLK AN4 PCH_DPD_CLK
DDPD_CTRLDATA AN2 PCH_DPD_DAT

DDPB_AUXN AK6 DDPB_AUXN → PAD T96
DDPC_AUXN AG7 DDPC_AUXN → PAD T97
DDPD_AUXN AG11 PCH_DDPD_AUXN C112 0.1U_0402_16V4Z → PCH_DDPD_AUXN_C [29] LVDS Converter
DDPB_AUXP AK8 DDPB_AUXP → PAD T98
DDPC_AUXP AG6 DDPC_AUXP → PAD T99
DDPD_AUXP AG10 PCH_DDPD_AUXP C113 0.1U_0402_16V4Z → PCH_DDPD_AUXP_C [29] LVDS Converter
DDPB_HPD AJ2 PCH_HDMIOUT_HPD → PCH_HDMIOUT_HPD [30] HDMI OUT
DDPC_HPD AH5 DPD_HPD → PAD T100
DDPD_HPD AJ4 DDPD_HPD LVDS Converter

PIRQE#/GPIO2 AR30 PCH_GPIO2
PIRQF#/GPIO3 AV29 PCH_GPIO3
PIRQG#/GPIO4 AV28 PCH_GPIO4
PIRQH#/GPIO5 AT27 PCH_GPIO5
PME# AA31 PCI_PME# → PADT101
PLTRST# AA37 PCH_PLT_RST#
C2121 0.1U_0402_16V4Z @ESD@

DH82LPDS_FCBGA708

PCH_DDPD_AUXN_C R172 @ 100K_0402_5% +3VS
PCH_DDPD_AUXP_C R173 @ 100K_0402_5%
CRB Reserve PU/PL

@R164 0_0402_5% +3VS
C111 0.1U_0402_16V4Z
U4 MC74VHC1G08DFT2G_SC70-5
PCH_PLT_RST# → IN1, IN2 → OUT PLT_RST# [21,41,43]
For GPU/TPM/EC
R166 100K_0402_5%

R677 0_0402_5% +3VALW_PCH
@R678 0_0402_5% +3VS
v0.3 update for wake from WLAN(BCM43142)
@ C2029 0.1U_0402_16V4Z
For Card reader/ LAN/WLAN/TV
U5 MC74VHC1G08DFT2G_SC70-5
OUT PLT_A_RST# [36,39,40]
R171 100K_0402_5%
C2135 ESD@ 0.1U_0402_16V4Z
v0.2 update

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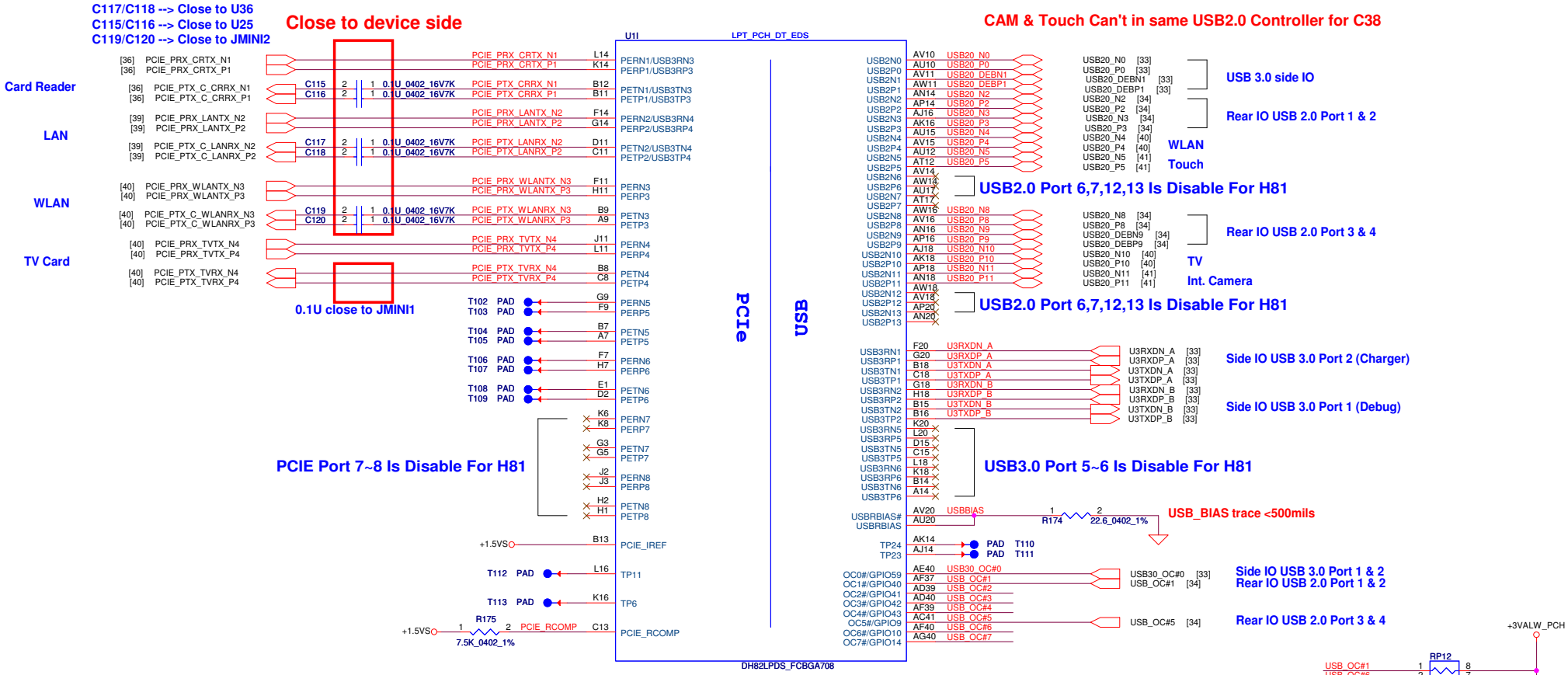

- Port mapping restrictions removed
  - USB 3.0 signals can now be paired with any of USB2.0 signal 0-13
  - Custom mapping through ACPI table/BIOS
  - Default mapping USB 3.0 1-6 to USB 2.0 0-5 ports

Example Only

USB 2.0 Signal	USB 3.0 Signal
0	1
1	2
2	3
3	4
4	5
5	6

- Better USB 2.0 performance than EHCI
- Windows* 8 is expected to include a native inbox xHCI driver

Table 14-4. Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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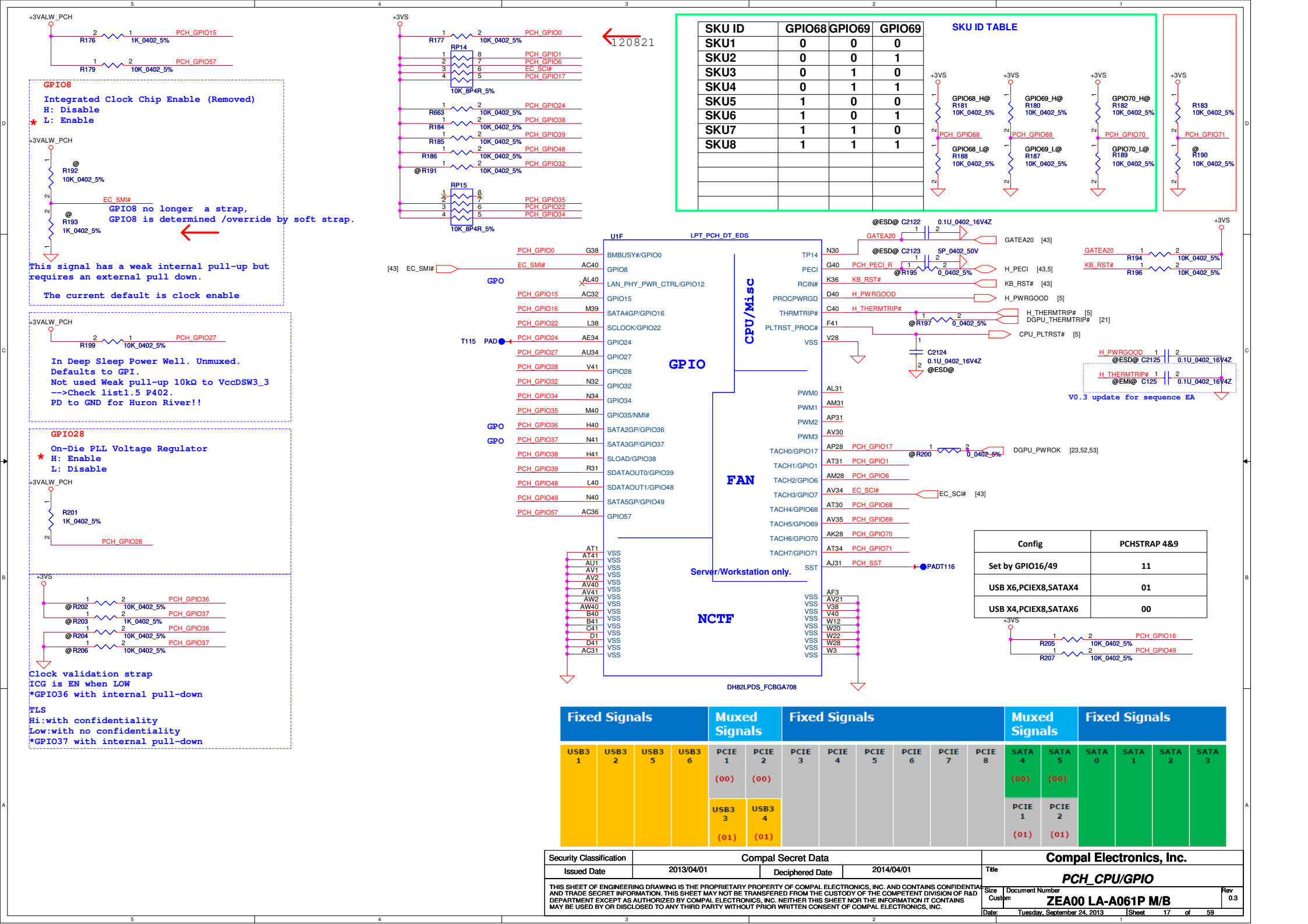
GPIO8
Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable
GPIO8 no longer a strap,
GPIO8 is determined /override by soft strap.
This signal has a weak internal pull-up but requires an external pull down.
The current default is clock enable
In Deep Sleep Power Well. Unmuxed.
Defaults to GPI.
Not used Weak pull-up 10kΩ to VccDSW3_3
-->Check list1.5 P402.
PD to GND for Huron River!!
GPIO28
On-Die PLL Voltage Regulator
* H: Enable
L: Disable
Clock validation strap
ICG is EN when LOW
*GPIO36 with internal pull-down
TLS
Hi:with confidentiality
Low:with no confidentiality
*GPIO37 with internal pull-down
120821
SKU ID TABLE
SKU ID | GPIO68 | GPIO69 | GPIO69
SKU1 | 0 | 0 | 0
SKU2 | 0 | 0 | 1
SKU3 | 0 | 1 | 0
SKU4 | 0 | 1 | 1
SKU5 | 1 | 0 | 0
SKU6 | 1 | 0 | 1
SKU7 | 1 | 1 | 0
SKU8 | 1 | 1 | 1
U1F
LPT_PCH_DT_EDS
GPIO
CPU/Misc
FAN
NCTF
Server/Workstation only.
DH82LPDS_FCBGA708
Config | PCHSTRAP 4&9
Set by GPIO16/49 | 11
USB X6,PCIEX8,SATAX4 | 01
USB X4,PCIEX8,SATAX6 | 00
V0.3 update for sequence EA
Fixed Signals
Muxed Signals
Fixed Signals
Muxed Signals
Fixed Signals
USB3 1
USB3 2
USB3 5
USB3 6
PCIE 1 (00)
PCIE 2 (00)
USB3 3 (01)
USB3 4 (01)
PCIE 3
PCIE 4
PCIE 5
PCIE 6
PCIE 7
PCIE 8
SATA 4 (00)
SATA 5 (00)
PCIE 1 (01)
PCIE 2 (01)
SATA 0
SATA 1
SATA 2
SATA 3
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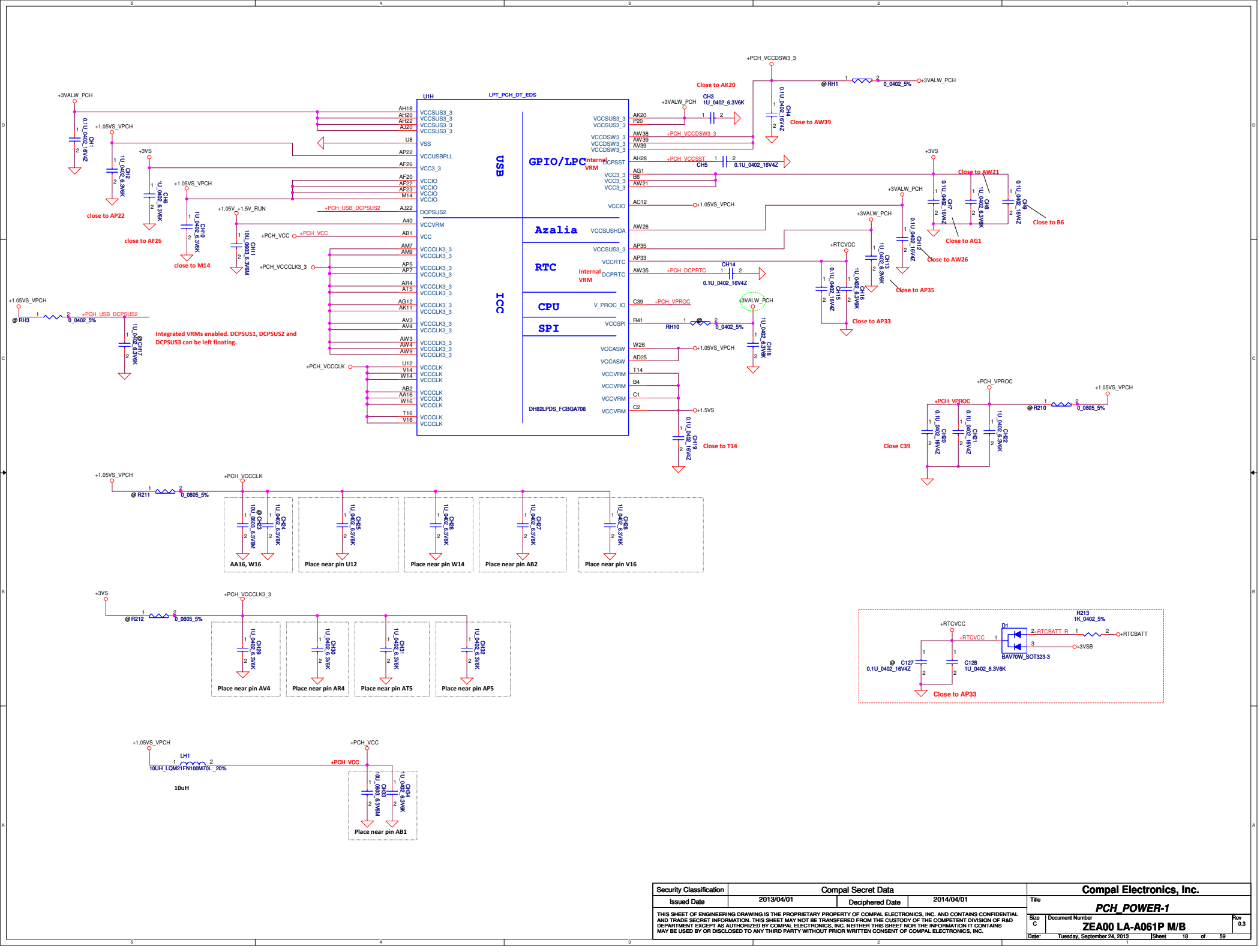
Title
PCH_CPU/GPIO
Size Custom
Document Number
ZEA00 LA-A061P M/B
Rev 0.3
Date: Tuesday, September 24, 2013
Sheet 17 of 59



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Compal Electronics, Inc.

Title: *PCH_POWER-1*

Size	Document Number	Rev
C	ZEA00 LA-A061P M/B	0.3

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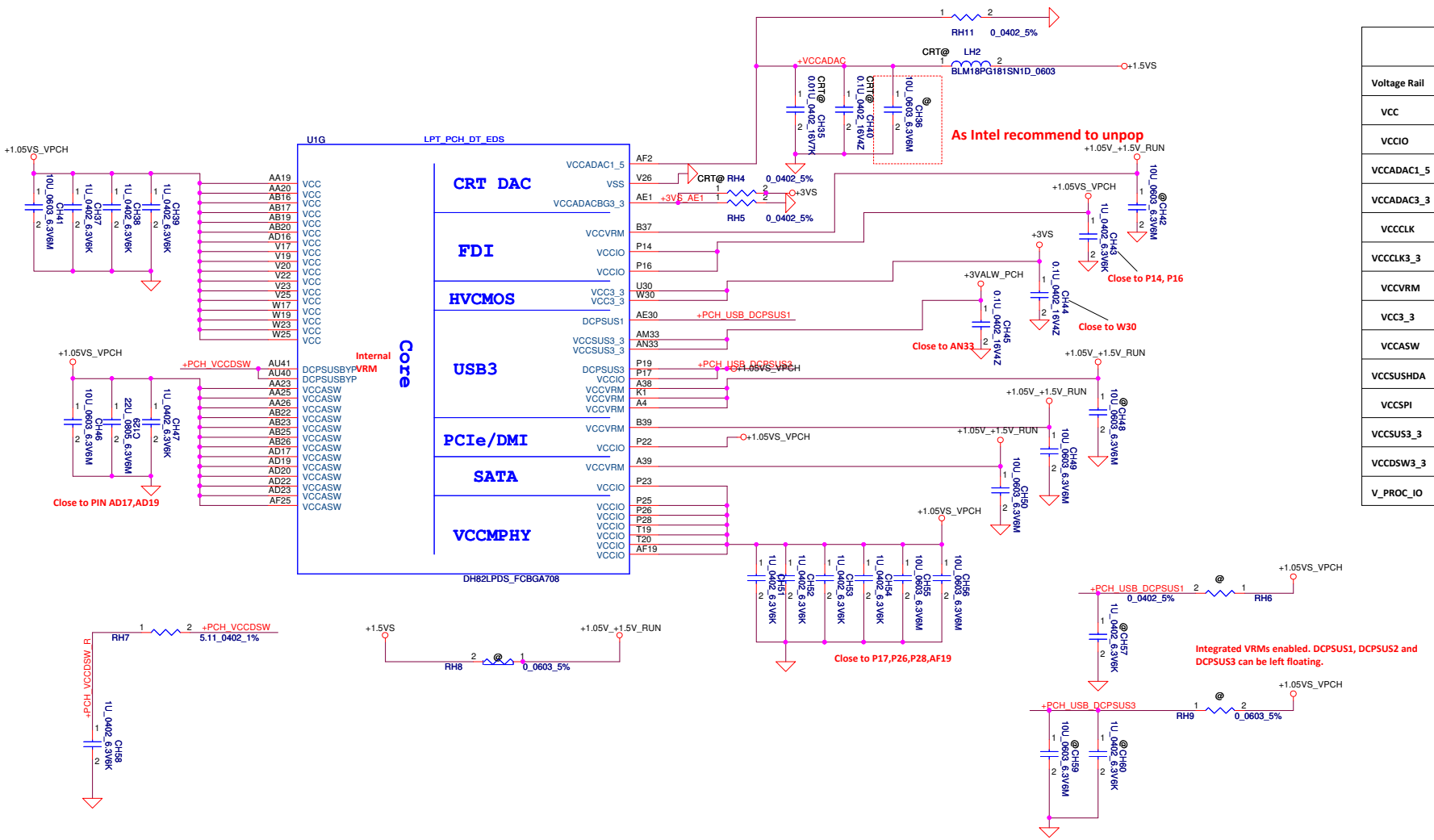
If CRT disable Pin AF2 & Pin AE1 can connect to GND



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Title: *PCH_POWER-2*

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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Compal Electronics, Inc.

Title: ***PCH_GND***

Size	Document Number	Rev
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[6] PCIE_CTX_C_GRX_P[0..15] PCIE_CTX_C_GRX_P[0..15]
[6] PCIE_CTX_C_GRX_N[0..15] PCIE_CTX_C_GRX_N[0..15]
[6] PCIE_GTX_C_CRX_P[0..15] PCIE_GTX_C_CRX_P[0..15]
[6] PCIE_GTX_C_CRX_N[0..15] PCIE_GTX_C_CRX_N[0..15]

U6A DIS@ — Part 1 of 7 — N14M-GE2-B-AIO-A2

PCI EXPRESS: GPIO, DACs, I2C, CLK

Reserve for x16 GPU

Reserve for x16 GPU

Differential signal

GPIO0 P6 GPU_VID4 — T117
GPIO1 M3 GPU_VID3 — T118
0327 Update
GPIO2 L6
GPIO3 P5 VGA_GPIO3 — T129
GPIO4 P7
GPIO5 L7 GPU_VID1 — T119
GPIO6 M7 GPU_VID2 — T120
0327 Update
GPIO7 N8
GPIO8 M1 OVERT#
GPIO9 M2 EVENT# R
GPIO10 L1
GPIO11 M5 GPU_PWM_VID — GPU_PWM_VID [52]
GPIO12 N3 VGA_GPIO12 — NVVDD_PSI [52]
GPIO13 M4 NVVDD_PSI
GPIO14 N4
GPIO15 P2
GPIO16 R8 VGA_GPIO16 — T130
0327 Update
GPIO17 M6
GPIO18 R1
GPIO19 N3
GPIO20 P4
GPIO21 P1
0327 Update

DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
DACA_VDD AG10 +DACA_VDD — R224 10K_0402_5%
DACA_VREF AP9
DACA_RSET AP8

I2CA_SCL R4 VGA_CRT_CLK
I2CA_SDA R5 VGA_CRT_DATA
I2CB_SCL R7 I2CB_SCL
I2CB_SDA R6 I2CB_SDA
I2CC_SCL R2 VGA_EDID_CLK
I2CC_SDA R3 VGA_EDID_DATA
I2CS_SCL T4 VGA_SMB_CK2
I2CS_SDA T3 VGA_SMB_DA2

PLLVDD AD8 — 60mA +PLLVDD — R227 0_0402_5% — 30 ohms @100MHz (ESR=0.05) — L1 SBY100505T-300Y-N_0402 — +1.05VS_VGA
SP_PLLVDD AE8 — 45mA
VID_PLLVDD AD7 — 45mA — +SP_PLLVDD
XTAL_IN H3 XTALIN
XTAL_OUT H2 XTAL_OUT
XTAL_OUTBUFF J4 XTALOUT
XTAL_SSIN H1 XTALSSIN

PEX_WAKE_N AJ11
PEX_REFCLK AL13 — [13] CLK_PCIE_VGA
PEX_REFCLK_N AK13 — [13] CLK_PCIE_VGA#
PEX_CLKREQ_N AK12 — CLK_REQ_GPU#
PEX_TSTCLK_OUT AJ26 — PEX_TSTCLK_OUT — R230 200_0402_1%
PEX_TSTCLK_OUT_N AK26 — PEX_TSTCLK_OUT#
PEX_RST_N AJ12 — PLT_RST_VGA#
PEX_TERMP AP29 — R234 2.49K_0402_1% DIS@

R232 10K_0402_5% DIS@
R233 10K_0402_5% DIS@

Near GPU
Under GPU

+3VS_VGA R214 10K_0402_5% — C130 0.1U_0402_10V6K — Q4B DMN66D0LDW-7 2N_SOT363-6 DIS@ — DGPU_THERMTRIP# [17]
Q4A DMN66D0LDW-7 2N_SOT363-6 DIS@

EVENT# R R217 10K_0402_5%
VGA_EDID_CLK R218 2.2K_0402_5%
VGA_EDID_DATA R219 2.2K_0402_5%
VGA_CRT_DATA R220 2.2K_0402_5%
VGA_CRT_CLK R221 2.2K_0402_5%
I2CB_SCL R222 2.2K_0402_5%
I2CB_SDA R223 2.2K_0402_5%
OVERT# R225 10K_0402_5%
VGA_GPIO12 R226 10K_0402_5%
0327 Update

Table 102. GB2-64 and GB4-128 GPIO Description

GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100k pull-down PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVVDD
GPIO7	3DVision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

PCIE_GTX_C_CRX_P0 DIS@ C131 — PCIE_GTX_C_CRX_P0 AK14
PCIE_GTX_C_CRX_N0 DIS@ C132 — PCIE_GTX_C_CRX_N0 AJ14
PCIE_GTX_C_CRX_P1 DIS@ C133 — PCIE_GTX_C_CRX_P1 AH14
PCIE_GTX_C_CRX_N1 DIS@ C134 — PCIE_GTX_C_CRX_N1 AG14
PCIE_GTX_C_CRX_P2 DIS@ C135 — PCIE_GTX_C_CRX_P2 AK15
PCIE_GTX_C_CRX_N2 DIS@ C136 — PCIE_GTX_C_CRX_N2 AJ15
PCIE_GTX_C_CRX_P3 DIS@ C137 — PCIE_GTX_C_CRX_P3 AL16
PCIE_GTX_C_CRX_N3 DIS@ C138 — PCIE_GTX_C_CRX_N3 AK16
PCIE_GTX_C_CRX_P4 DIS@ C139 — PCIE_GTX_C_CRX_P4 AK17
PCIE_GTX_C_CRX_N4 DIS@ C140 — PCIE_GTX_C_CRX_N4 AJ17
PCIE_GTX_C_CRX_P5 DIS@ C141 — PCIE_GTX_C_CRX_P5 AH17
PCIE_GTX_C_CRX_N5 DIS@ C142 — PCIE_GTX_C_CRX_N5 AG17
PCIE_GTX_C_CRX_P6 DIS@ C143 — PCIE_GTX_C_CRX_P6 AK18
PCIE_GTX_C_CRX_N6 DIS@ C144 — PCIE_GTX_C_CRX_N6 AJ18
PCIE_GTX_C_CRX_P7 DIS@ C145 — PCIE_GTX_C_CRX_P7 AL19
PCIE_GTX_C_CRX_N7 DIS@ C146 — PCIE_GTX_C_CRX_N7 AK19
PCIE_GTX_C_CRX_P8 @ C2096 — PCIE_GTX_C_CRX_P8 AK20
PCIE_GTX_C_CRX_N8 @ C2097 — PCIE_GTX_C_CRX_N8 AJ20
PCIE_GTX_C_CRX_P9 @ C2098 — PCIE_GTX_C_CRX_P9 AH20
PCIE_GTX_C_CRX_N9 @ C2099 — PCIE_GTX_C_CRX_N9 AG20
PCIE_GTX_C_CRX_P10 @ C2100 — PCIE_GTX_C_CRX_P10 AK21
PCIE_GTX_C_CRX_N10 @ C2101 — PCIE_GTX_C_CRX_N10 AJ21
PCIE_GTX_C_CRX_P11 @ C2102 — PCIE_GTX_C_CRX_P11 AL22
PCIE_GTX_C_CRX_N11 @ C2103 — PCIE_GTX_C_CRX_N11 AK22
PCIE_GTX_C_CRX_P12 @ C2104 — PCIE_GTX_C_CRX_P12 AK23
PCIE_GTX_C_CRX_N12 @ C2105 — PCIE_GTX_C_CRX_N12 AJ23
PCIE_GTX_C_CRX_P13 @ C2106 — PCIE_GTX_C_CRX_P13 AH23
PCIE_GTX_C_CRX_N13 @ C2107 — PCIE_GTX_C_CRX_N13 AG23
PCIE_GTX_C_CRX_P14 @ C2108 — PCIE_GTX_C_CRX_P14 AK24
PCIE_GTX_C_CRX_N14 @ C2109 — PCIE_GTX_C_CRX_N14 AJ24
PCIE_GTX_C_CRX_P15 @ C2110 — PCIE_GTX_C_CRX_P15 AL25
PCIE_GTX_C_CRX_N15 @ C2111 — PCIE_GTX_C_CRX_N15 AK25
All: 0.22U_0402_16V7K

PEX_TX0 PEX_TX0_N PEX_TX1 PEX_TX1_N PEX_TX2 PEX_TX2_N PEX_TX3 PEX_TX3_N PEX_TX4 PEX_TX4_N PEX_TX5 PEX_TX5_N PEX_TX6 PEX_TX6_N PEX_TX7 PEX_TX7_N PEX_TX8 PEX_TX8_N PEX_TX9 PEX_TX9_N PEX_TX10 PEX_TX10_N PEX_TX11 PEX_TX11_N PEX_TX12 PEX_TX12_N PEX_TX13 PEX_TX13_N PEX_TX14 PEX_TX14_N PEX_TX15 PEX_TX15_N

PEX_RX0 PEX_RX0_N PEX_RX1 PEX_RX1_N PEX_RX2 PEX_RX2_N PEX_RX3 PEX_RX3_N PEX_RX4 PEX_RX4_N PEX_RX5 PEX_RX5_N PEX_RX6 PEX_RX6_N PEX_RX7 PEX_RX7_N PEX_RX8 PEX_RX8_N PEX_RX9 PEX_RX9_N PEX_RX10 PEX_RX10_N PEX_RX11 PEX_RX11_N PEX_RX12 PEX_RX12_N PEX_RX13 PEX_RX13_N PEX_RX14 PEX_RX14_N PEX_RX15 PEX_RX15_N

PLT_RST# — R228 0_0402_5% — +3VS_VGA — R229 10K_0402_5%
[15,41,43] PLT_RST#
[15,43] DGPU_HOLD_RST#
U7 MC74VHC1G08DFT2G SC70 5P
R231 100K_0402_5%
v0.2 update
v0.2 update

Under GPU(below 150mils)
Put C169 close to U65.AE8

+1.05VS_VGA — L2 BLM18PG330SN1D_0603 DIS@ — 180ohms (ESR=0.2) Bead — 150mA — +SP_PLLVDD
C165 22U_0805_6.3V6M DIS@
C166 4.7U_0402_6.3V6M DIS@
C167 0.1U_0402_10V6K DIS@
C168 0.1U_0402_10V6K DIS@
C169 0.1U_0402_10V6K DIS@

+3VS_VGA — R236 2.2K_0402_5% DIS@ — R237 2.2K_0402_5% DIS@ — Q5B 2N7002DW-T/R7_SOT363-6 DIS@ — VGA_SMB_CK2 — EC_SMB_CK2 [13,43,46]
Q5A 2N7002DW-T/R7_SOT363-6 DIS@ — VGA_SMB_DA2 — EC_SMB_DA2 [13,43,46]

+3VS_VGA — R238 10K_0402_5% — CLK_REQ_GPU# — R239 10K_0402_5%
Reserve pull-up and down. Don't have to install component for default, NV reply on 5/4. when system no support CLKREQ

R235 10M_0402_5% DIS@
Y3 27MHZ 10PF +-20PPM X3G027000DA1H DIS@ — XTALIN — XTAL_OUT
C170 10P_0402_50V8J DIS@
C171 10P_0402_50V8J DIS@
v0.3 update

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Title: N14M-GE2-PCIE/DAC/GPIO
Size: Document Number: ZEA00 LA-A061P M/B Rev: 0.3
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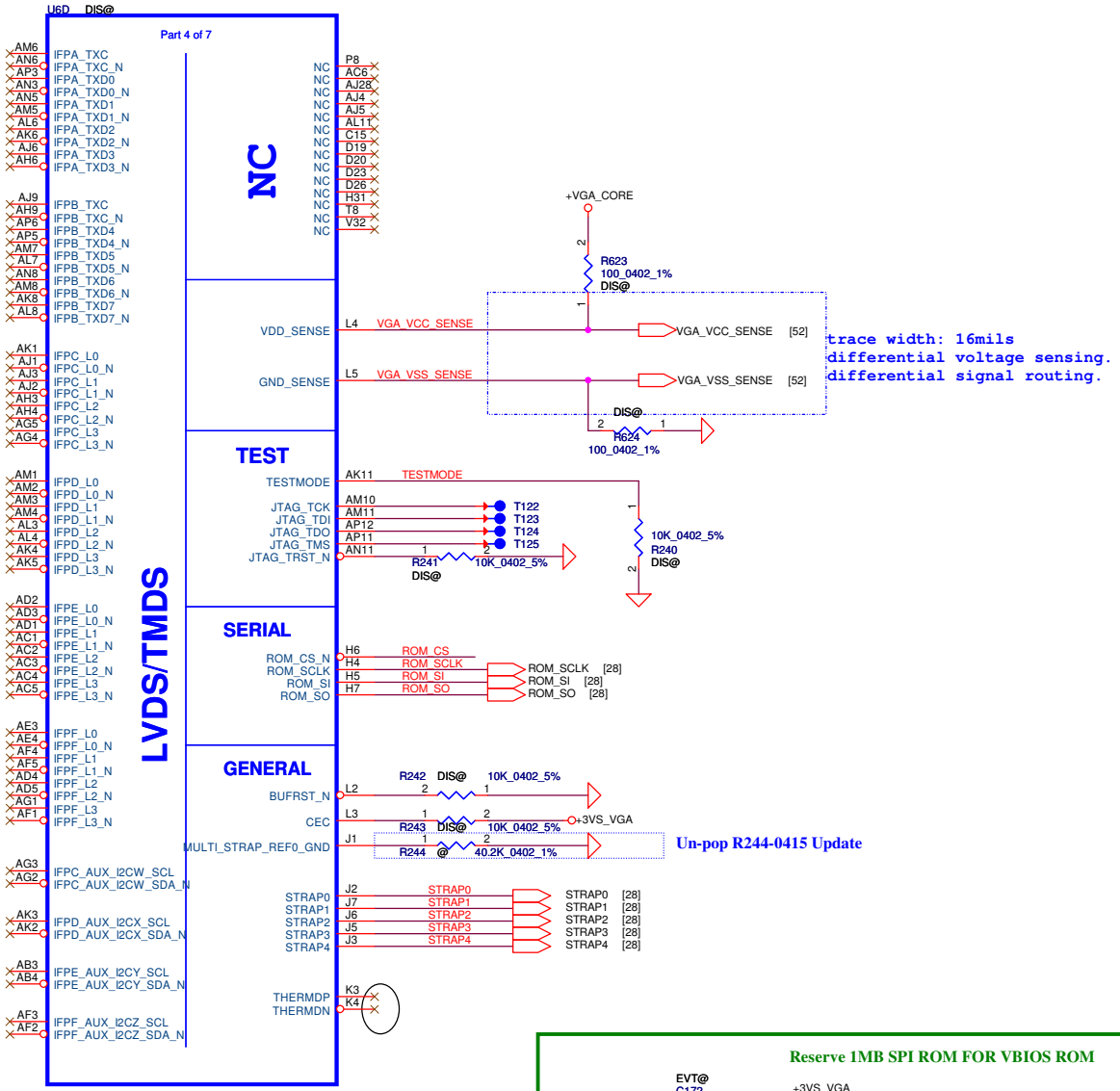
Table 66. N13x Family Display Link Summary

Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI



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Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-LVDS/HDMI/DP/THM

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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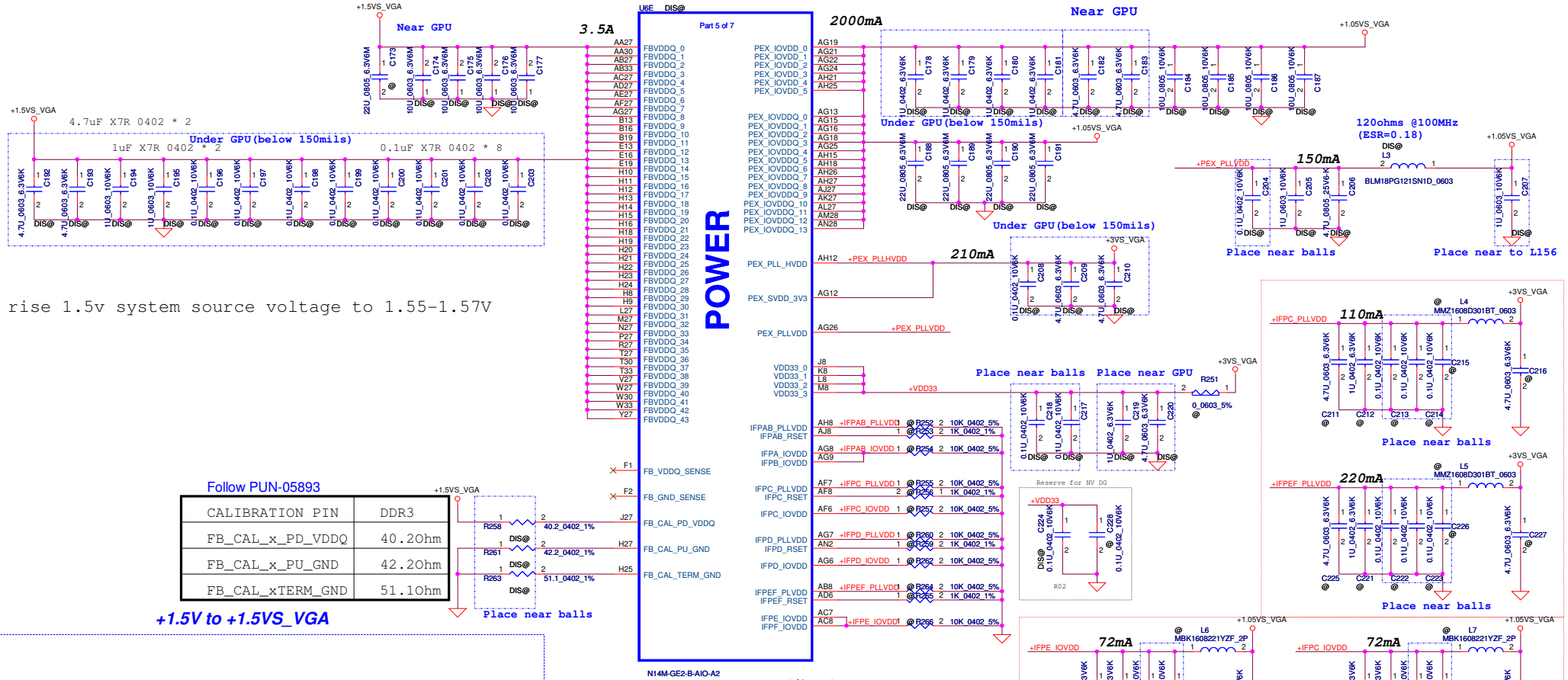

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Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-POWER

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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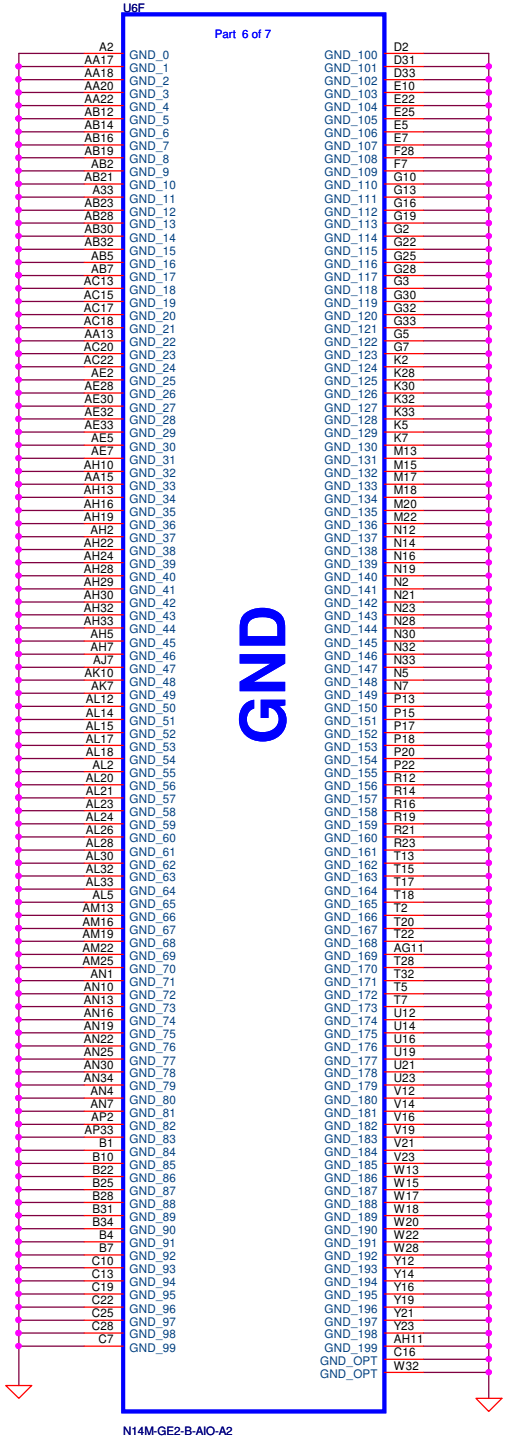

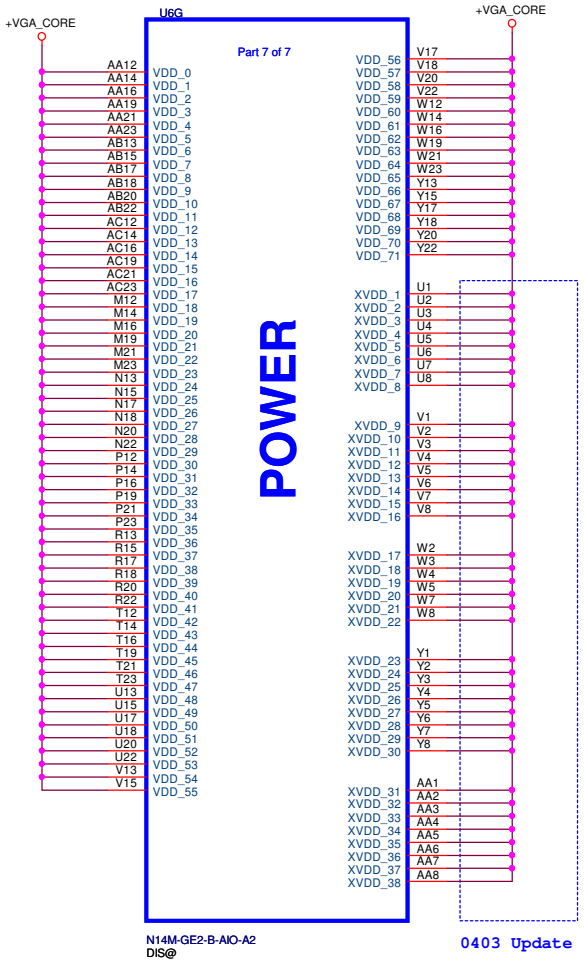

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Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-VGA CORE, GND

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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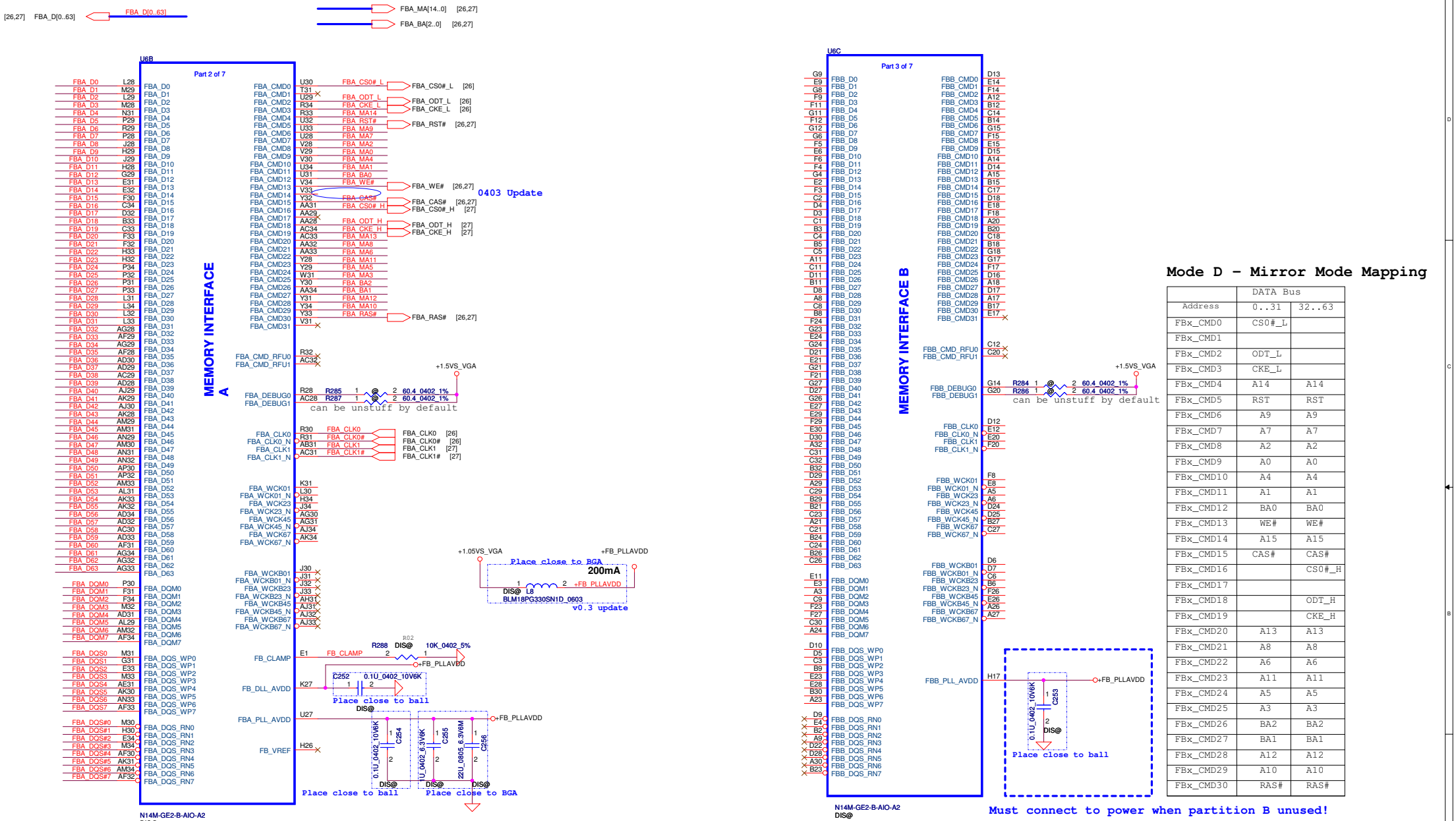

Mode D – Mirror Mode Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **N14M-GE2-MEM Interface**

Size	Document Number	Rev
	ZEA00 LA-A061P M/B	0.3

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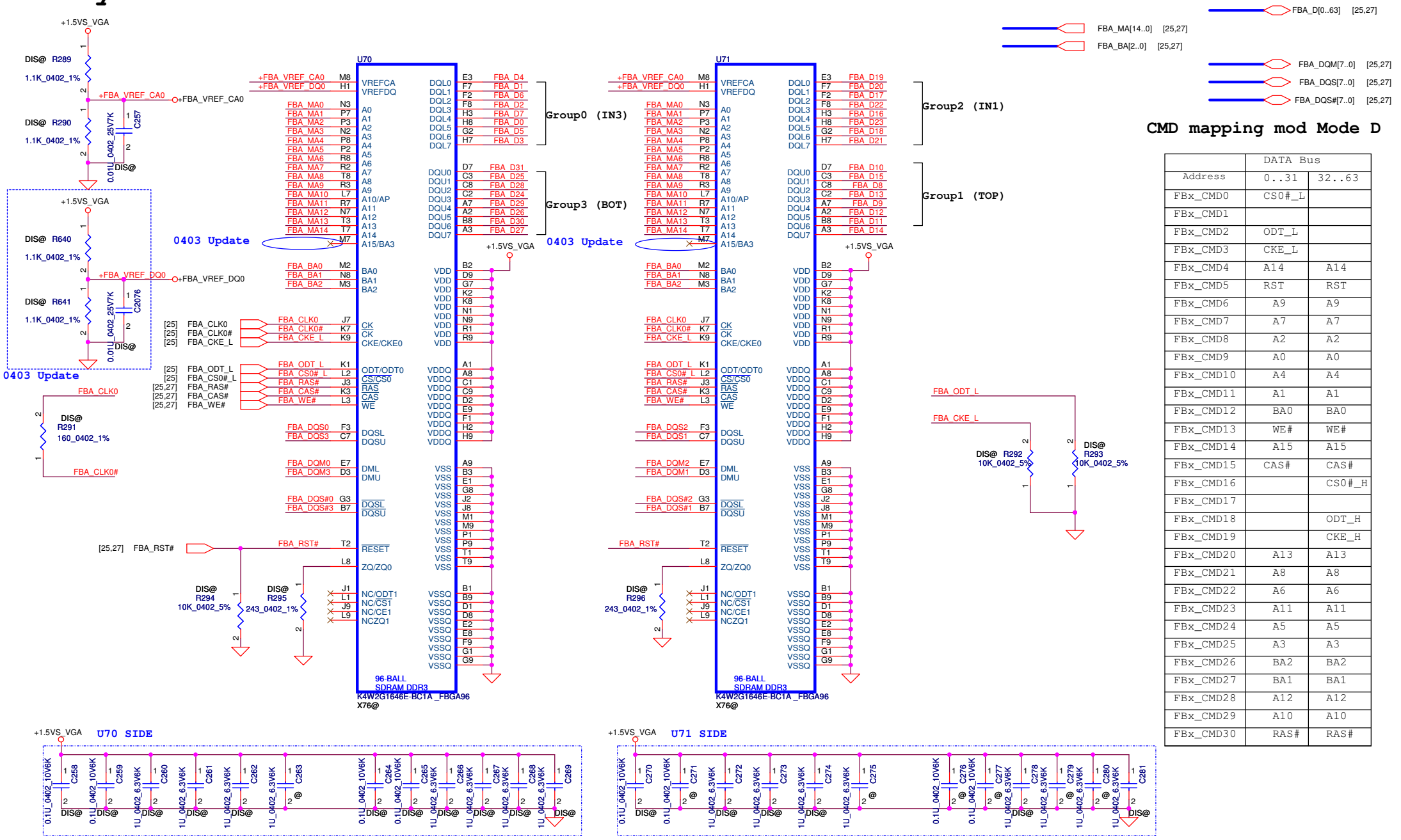
Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-VRAM A Lower

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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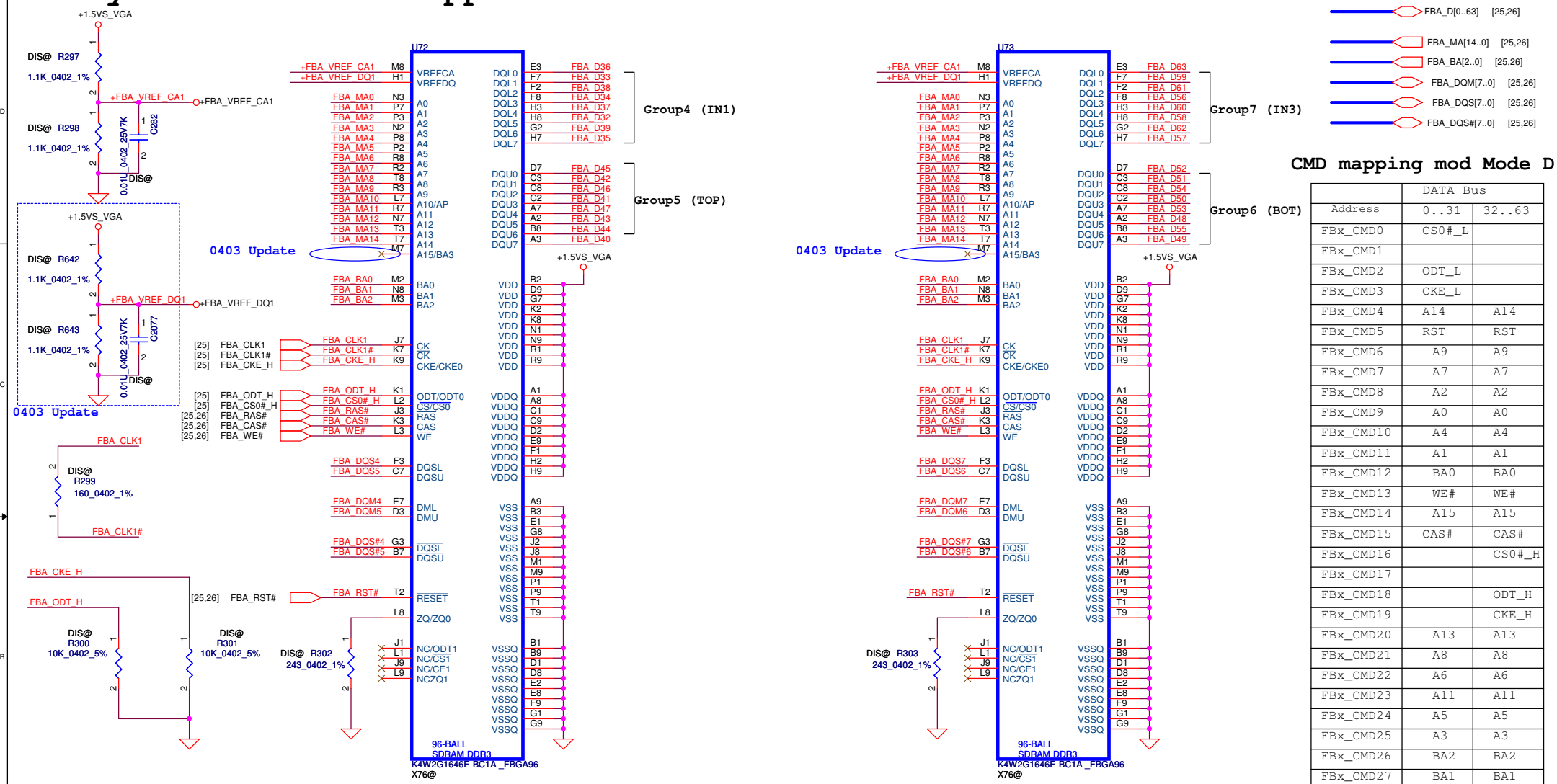
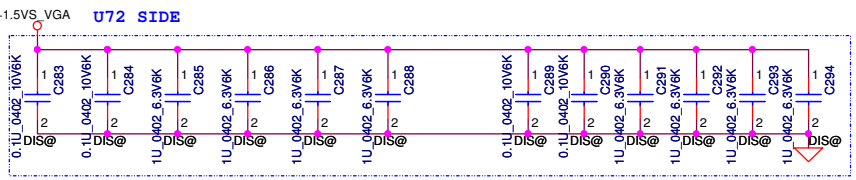
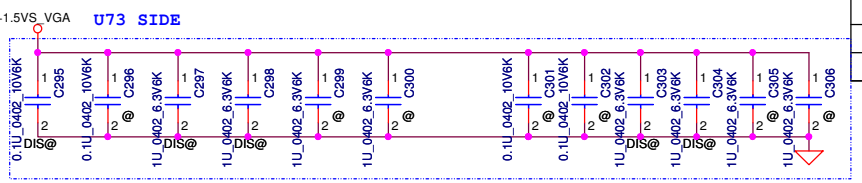
Memory Partition A – Upper 32 bits







FBA_D[0..63] [25,26]
FBA_MA[14..0] [25,26]
FBA_BA[2..0] [25,26]
FBA_DQM[7..0] [25,26]
FBA_DQS[7..0] [25,26]
FBA_DQS#[7..0] [25,26]

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Title	N14M-GE2-VRAM A Upper
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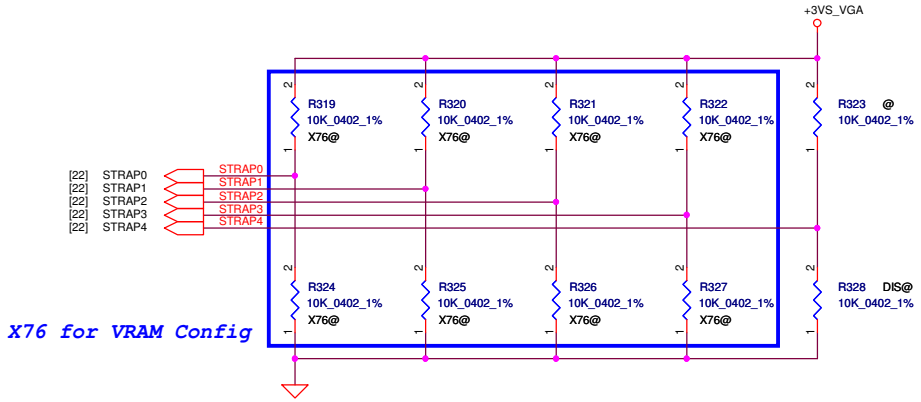
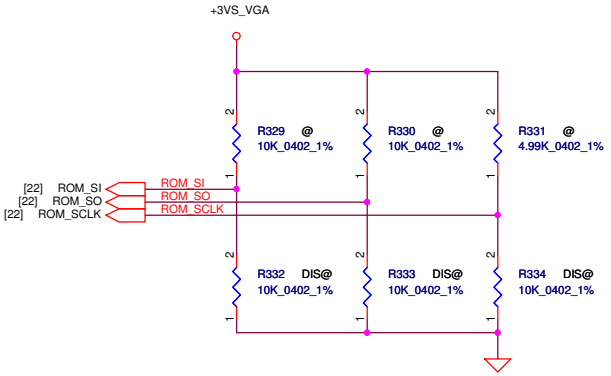


X76 for VRAM Config



[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

[VRAM Config-RVL-06366-001]

GPU	Frenq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0
N14M-GE2	900 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BFR-11C SA00003YO10	0 R327 PD 10K	1 R321 PU 10K	1 R320 PU 10K	0 R324 PD 10K
			Samsung (0x5) K4W2G1646E-BC11 SA00005SH00	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Micron (0x1) MT41J128M16JT-107G:K SA00005SM30	0 R327 PD 10K	0 R326 PD 10K	0 R325 PD 10K	1 R319 PU 10K
N14M-GE2	900 MHz	256M* 16* 4 2GB	Micron (0xD) MT41K256M16HA-107G:E SA000065D20	1 R322 PU 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Samsung (0xB) K4W4G1646B-HC11 SA000068R10	1 R322 PU 10K	0 R326 PD 10K	1 R320 PU 10K	1 R319 PU 10K
			Hynix (0x4) H5TC4G63AFR-11C SA00006E800	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	0 R324 PD 10K

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Power Consumption:

Pin 22 (PVCC) < 50 mA
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)

Pin5 (DPV33) < 20mA

Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)

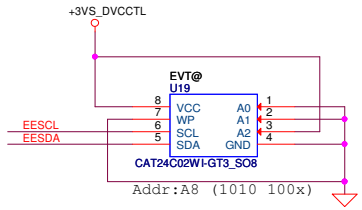
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 43 (VCCK) < 50mA
Pin 11 (DPV12) < 100mA

v0.2 update

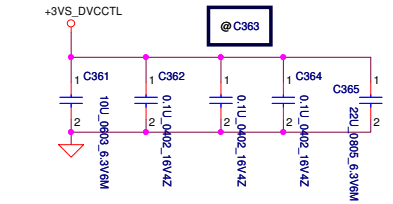
SE070104Z80
S CER CAP .1U 16V Z Y5V 0402
S CER CAP .1U 16V Z Y5V 0402

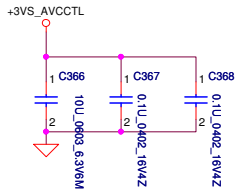
v0.2 update

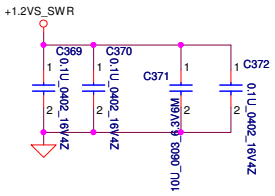
Vendor suggest to reserve for FW/EDID debug

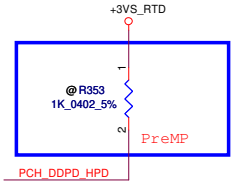


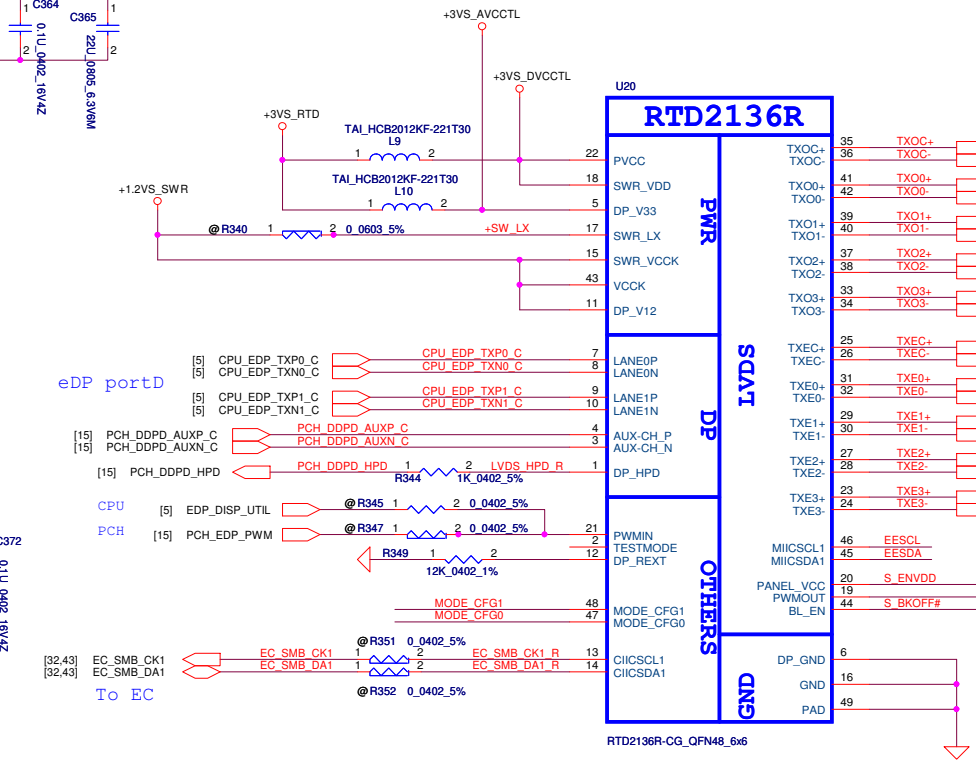
EVT Debug Only, un-pop for DVT

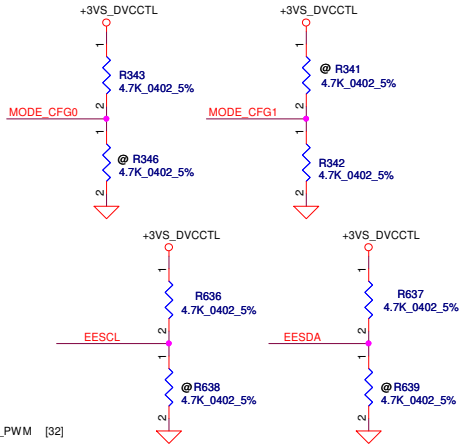












	Pin 47	
	0	1
Pin 48 0	X	EP Mode
Pin 48 1	ROM	EEPROM

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Title	LVDS Converter RTD2136S		
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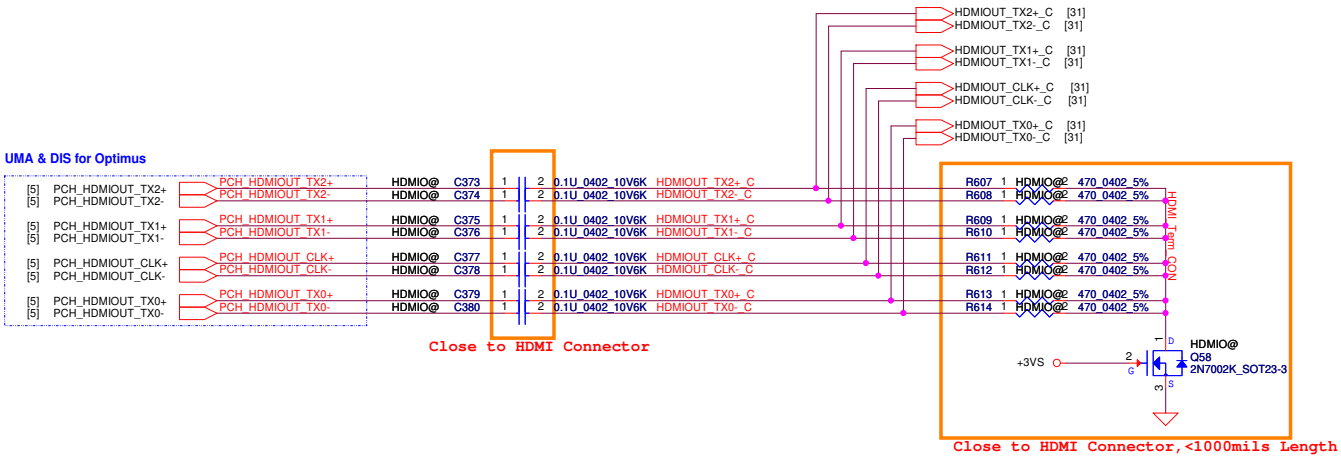

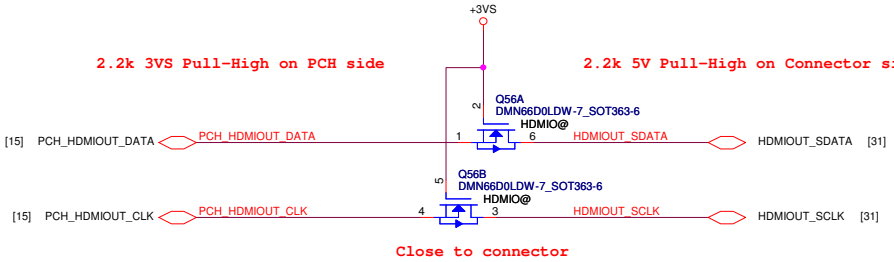

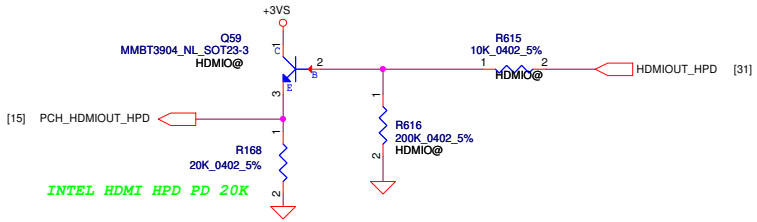

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Compal Electronics, Inc.

Title: ***HDMI-OUT Level Shift***

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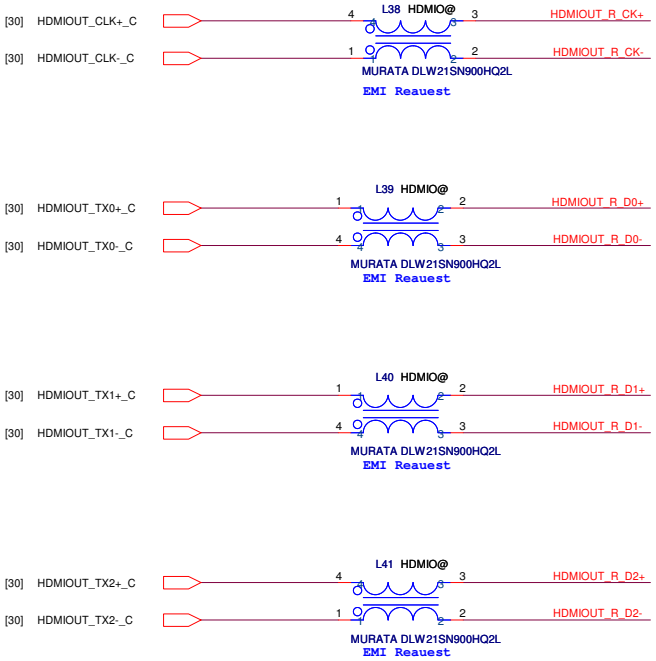
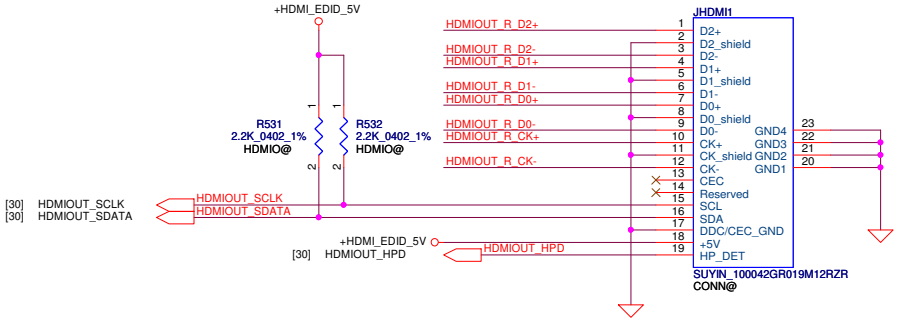
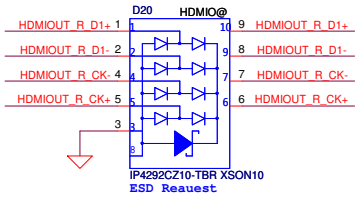
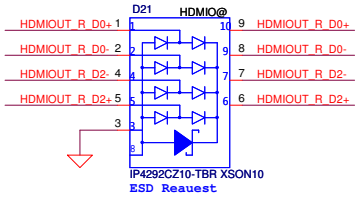
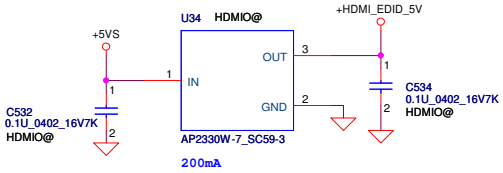
HDMI-OUT Connector

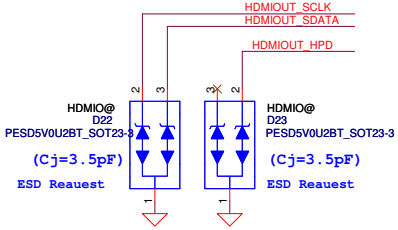












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Compal Electronics, Inc.

Title: HDMI-OUT

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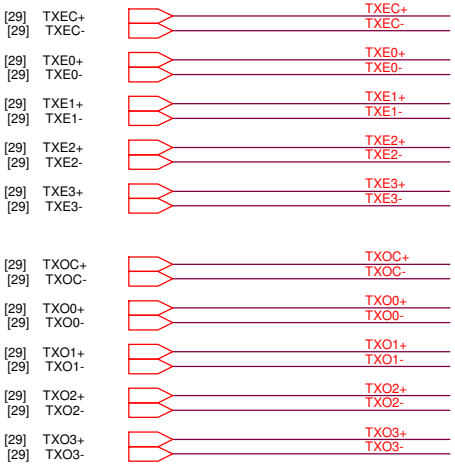
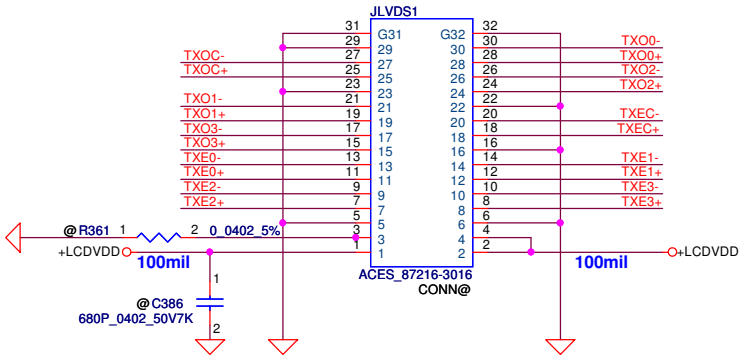
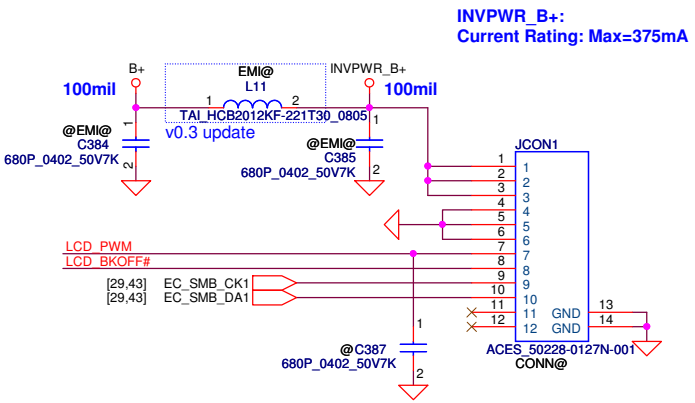
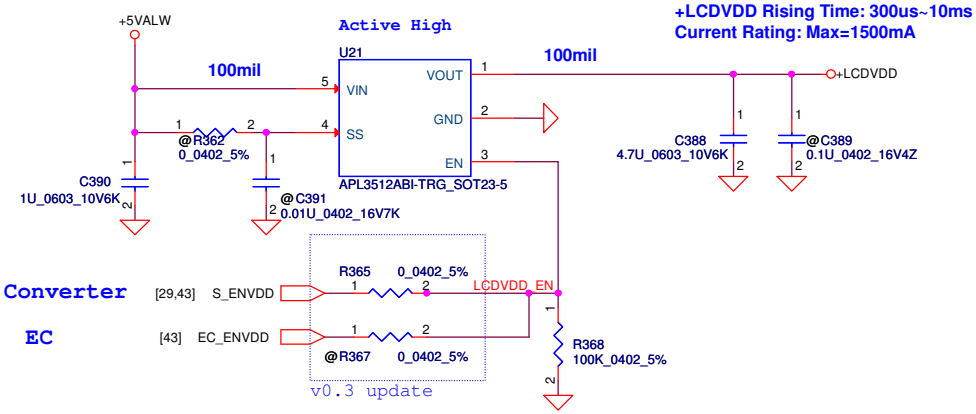
LVDS Conn.

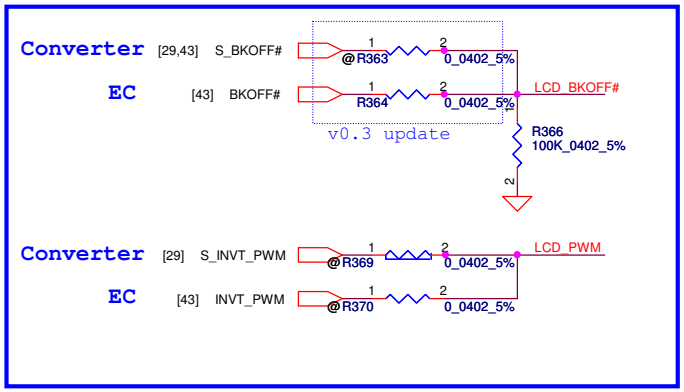




Converter







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Title: **LVDS**

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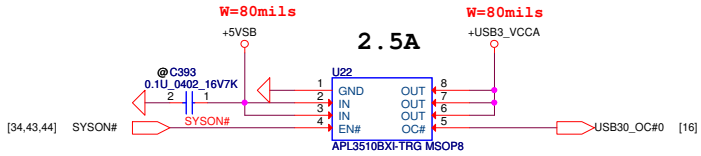
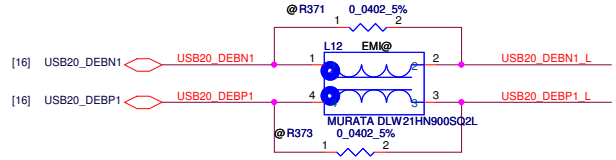
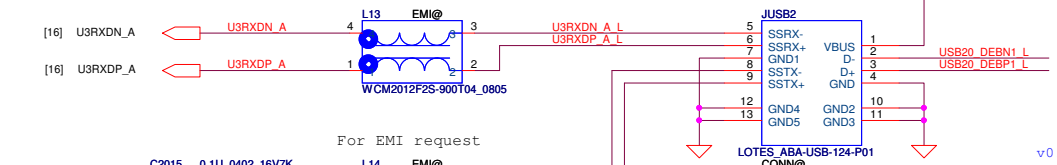
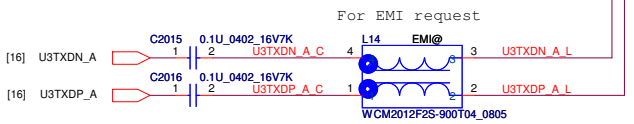
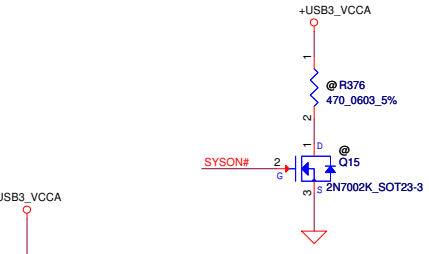
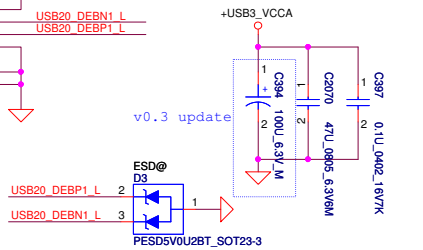


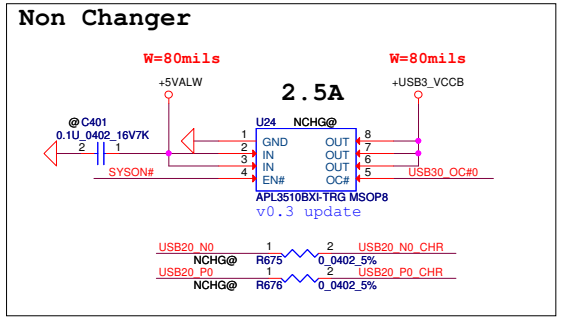


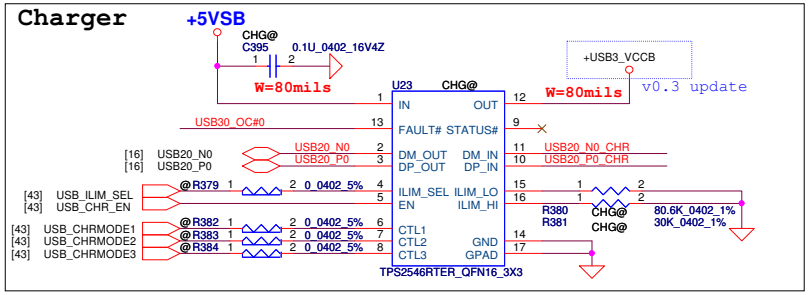






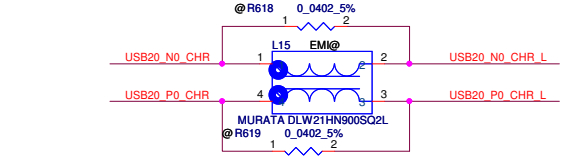


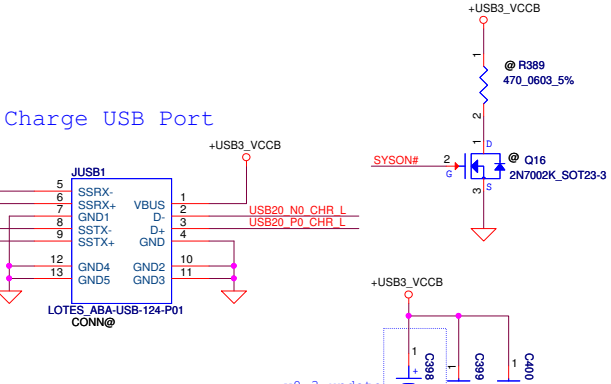


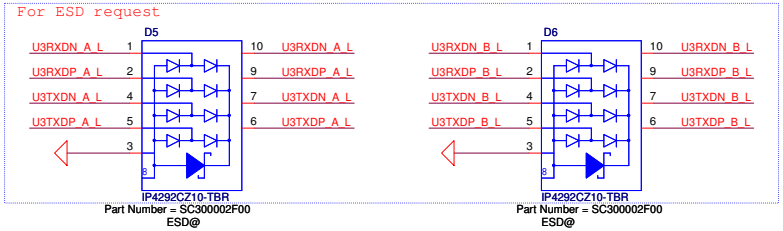


Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPXIOA07(pin104)	GPIO22(pin41)	GPXIOA11(pin108)	GPIO21(pin40)
S0(CDP)	1	1	1	1
S3(SDP)	1	1	1	0
S4/S5(DCP)	0	0	1	1

System Global Power State	TPS2546/TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake	0	0	1	1	ILIM_HI







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Issued Date		Deciphered Date	Title: USB 3.0 CONN
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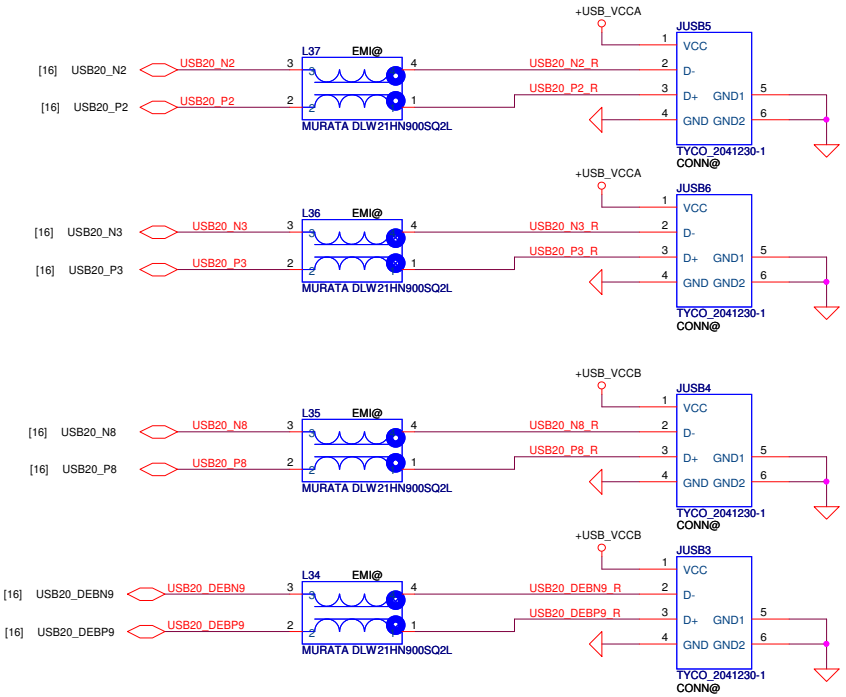
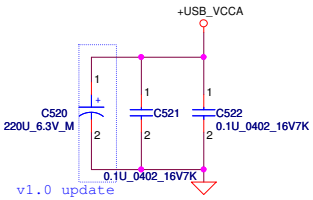
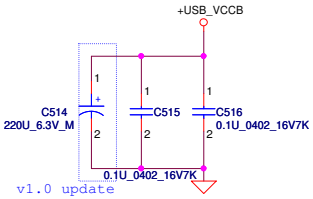
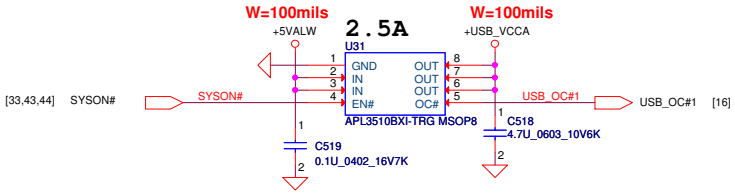
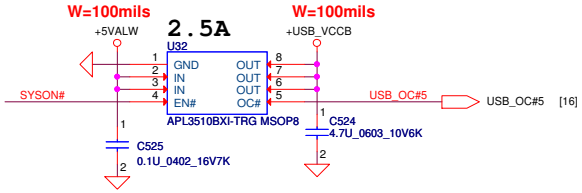
USB20



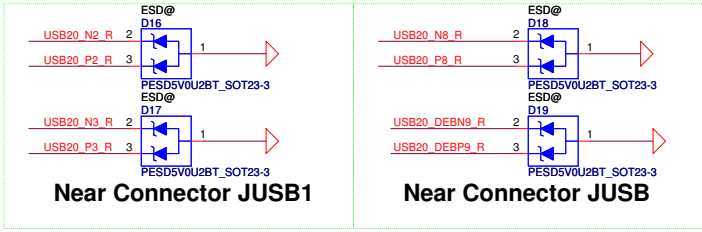


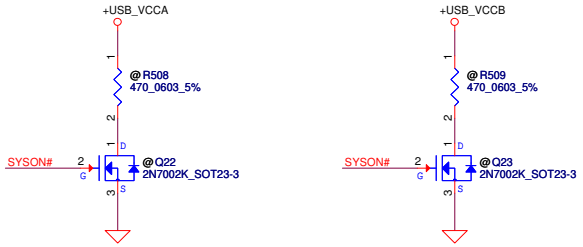






For USB2.0 ESD diode





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Title: USB20			
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
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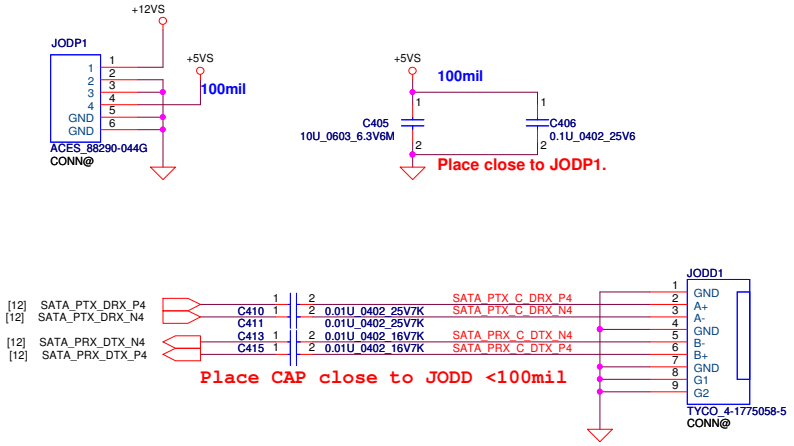
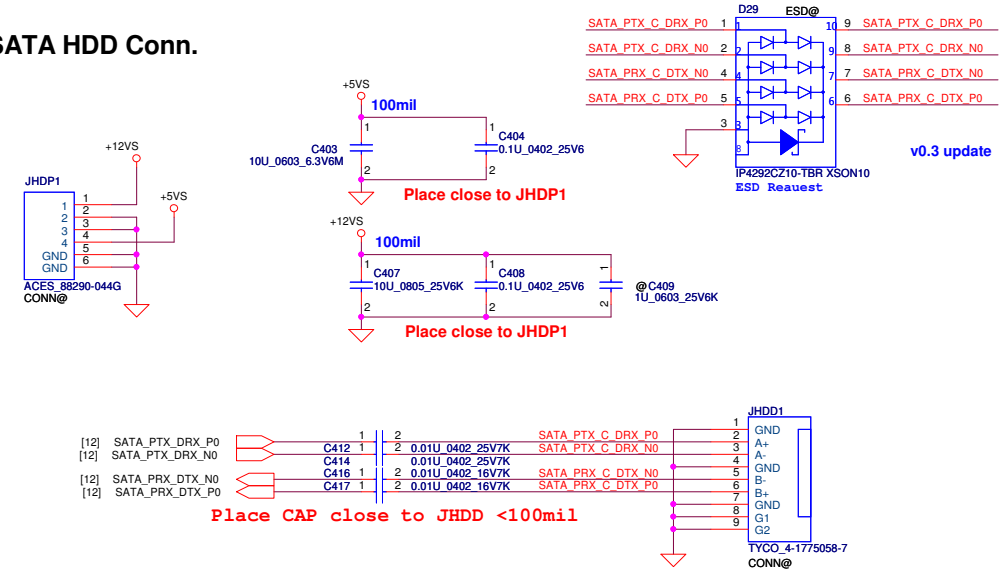
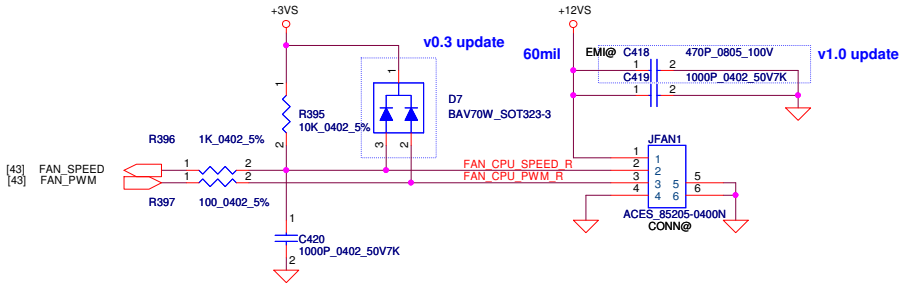
SATA ODD Conn



SATA HDD Conn.



FAN Control Circuit



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Compal Electronics, Inc.			
Title	SATA-HDD/ODD/USB		
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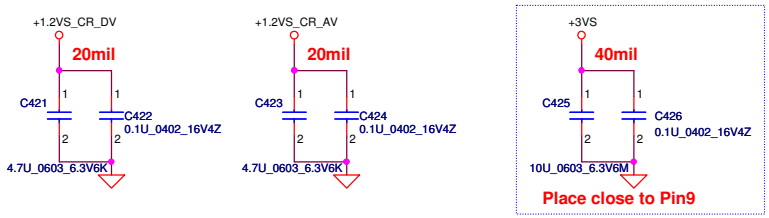
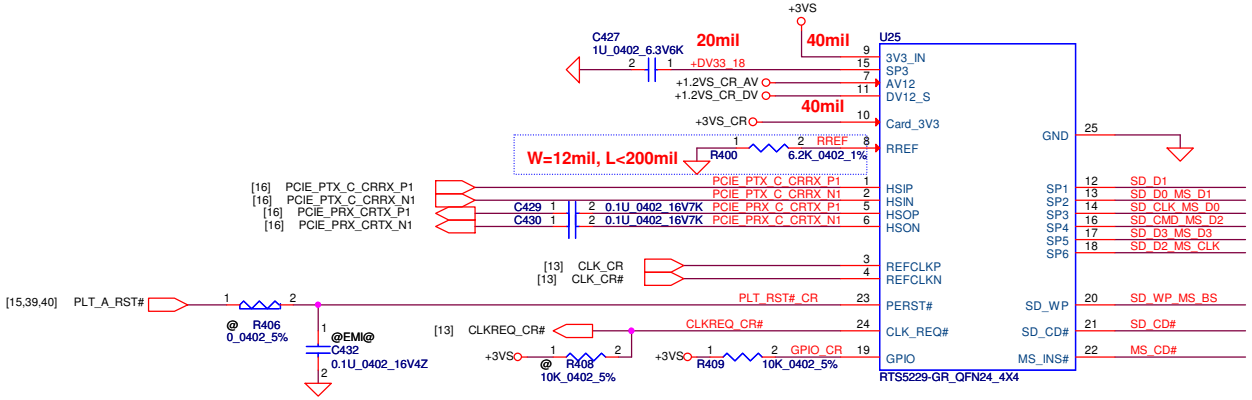
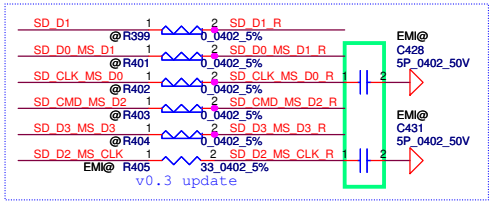
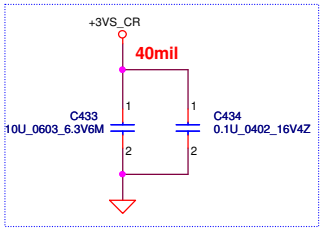


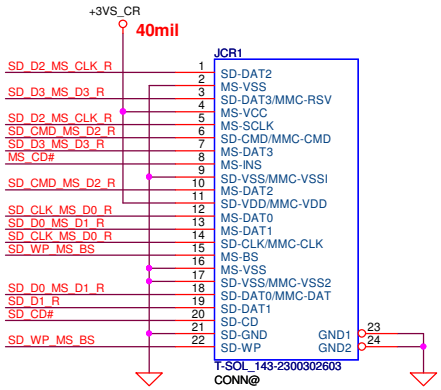


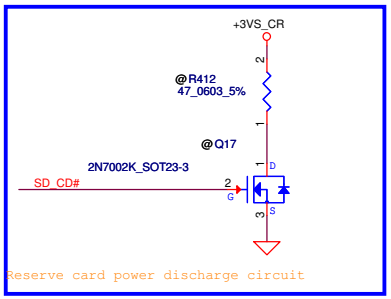
Length of per trace 2inch no more 2 via
mismatch trace length <100mil
50ohm +-15% impedance.



Place close to JCR1 pin 12,21







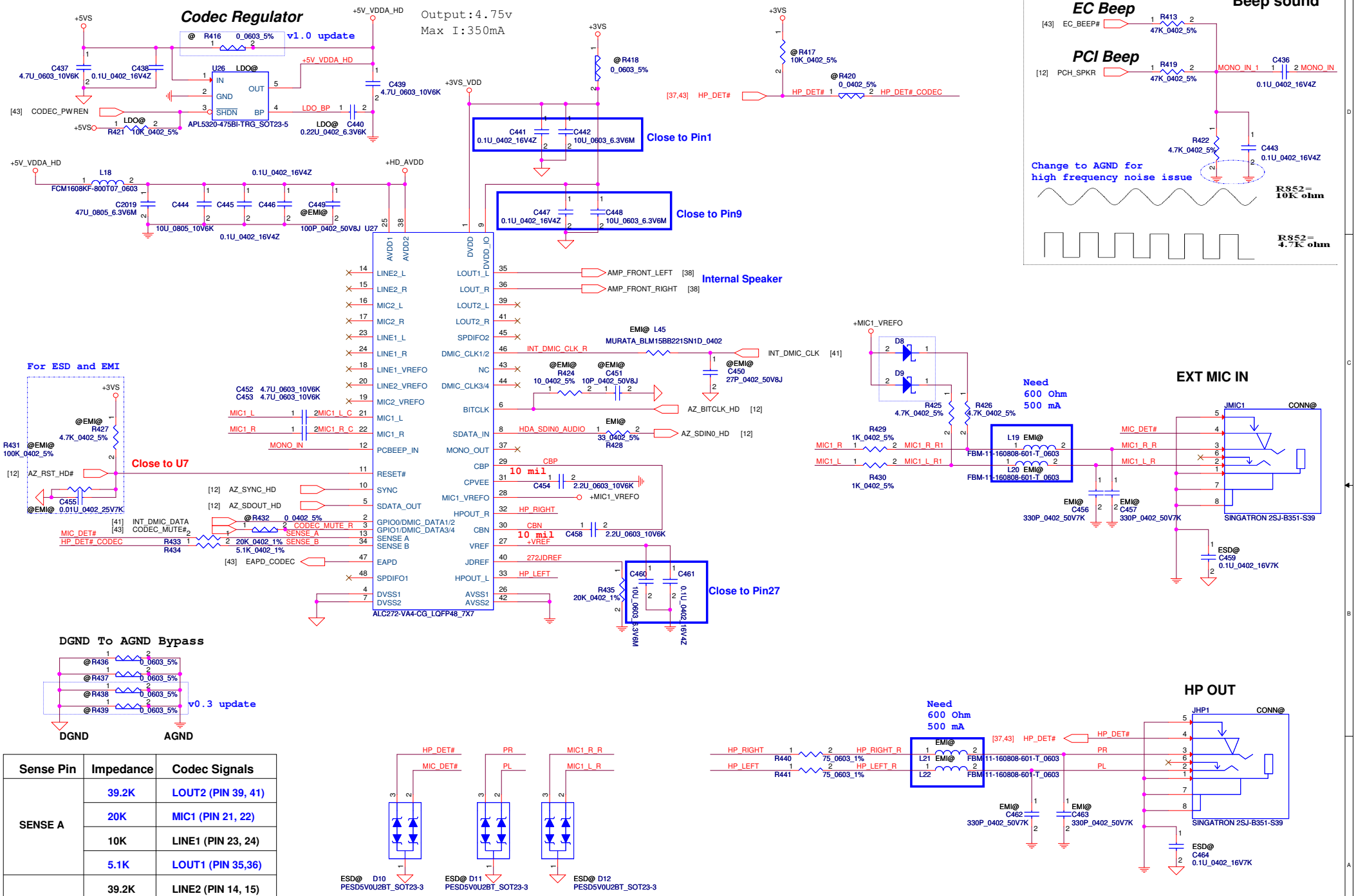
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: RTS5229 Media Card Controller

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

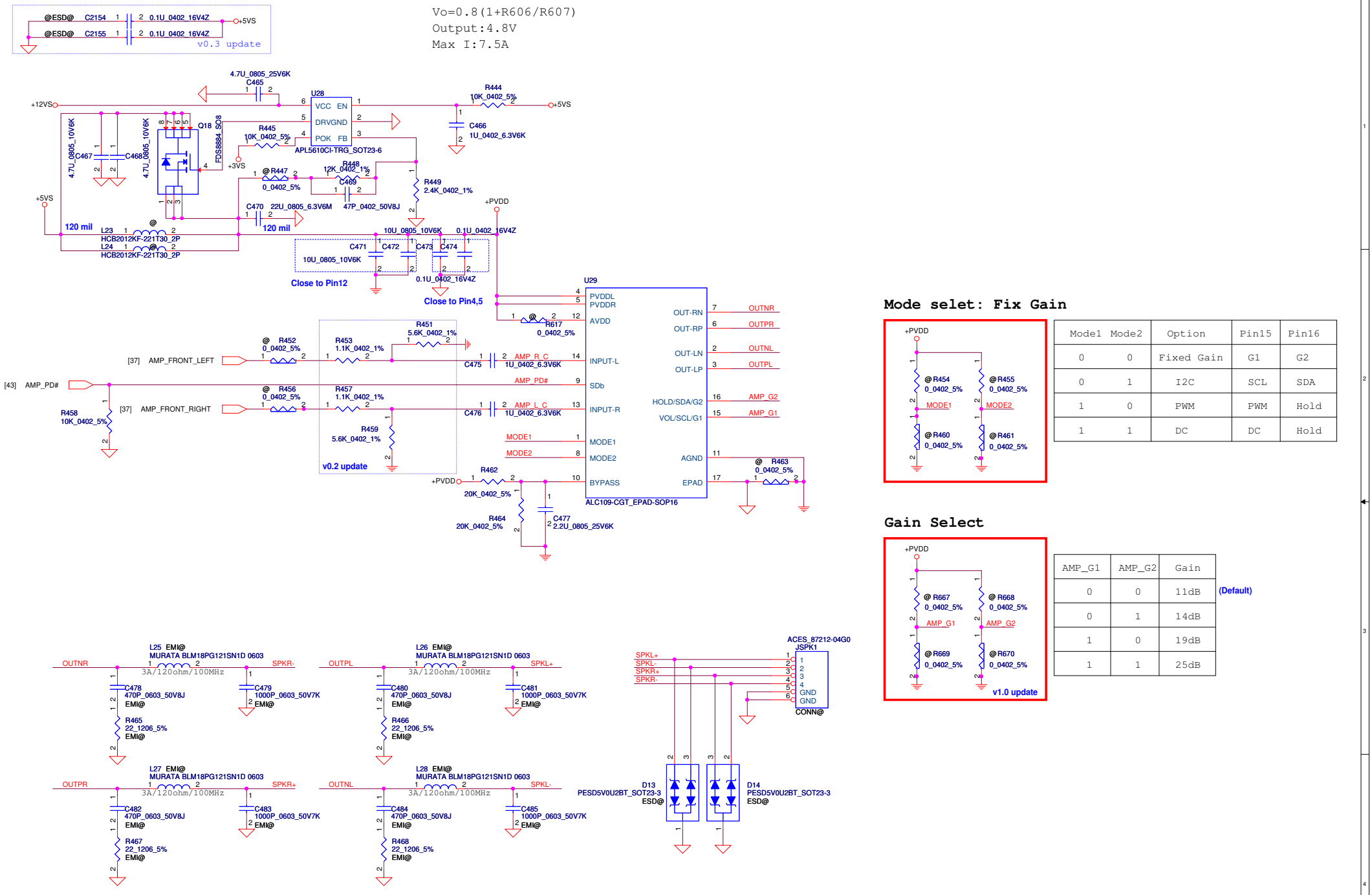
Date: Tuesday, September 24, 2013 | Sheet 36 of 59



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	LOUT2 (PIN 39, 41)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	10K	
	5.1K	HP-OUT (PIN 32,33)

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Title	HDA-ALC272/HP/MIC		
Size	Document Number		Rev
	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	37 of 59



Mode selet: Fix Gain

Mode1	Mode2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold

Gain Select

AMP_G1	AMP_G2	Gain	
0	0	11dB	(Default)
0	1	14dB	
1	0	19dB	
1	1	25dB	

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: AMP

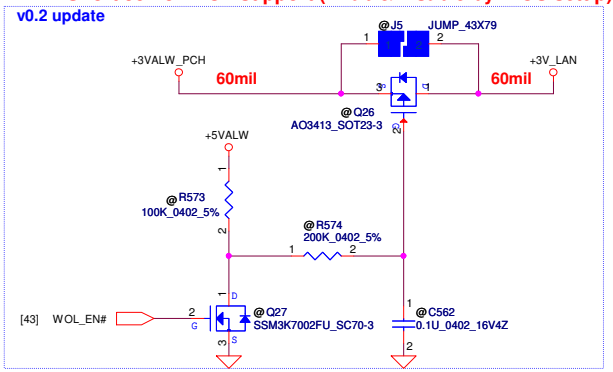
Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 38 of 59

WOL circuit

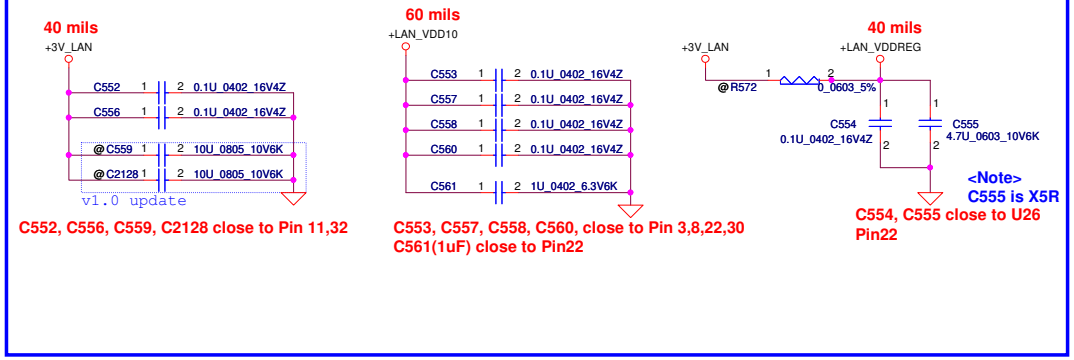
Short J5 for WOL support (Enable/Disable by BIOS setup)

v0.2 update

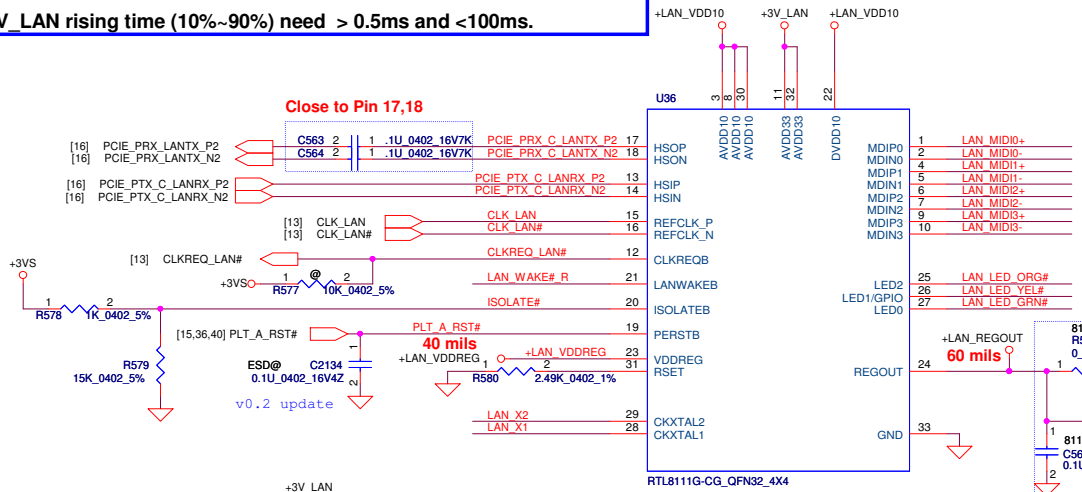


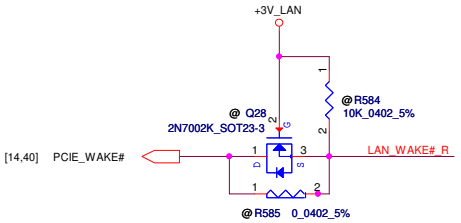
+3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

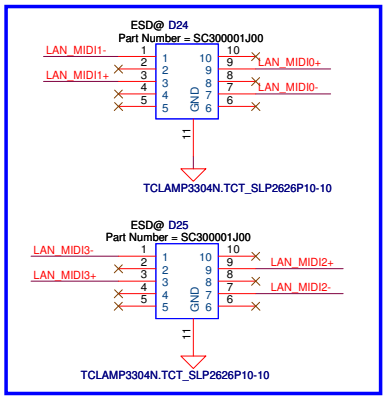
Power (Decoupling Cap.)



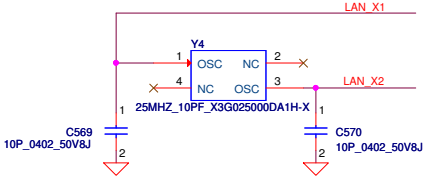
Close to Pin 17,18







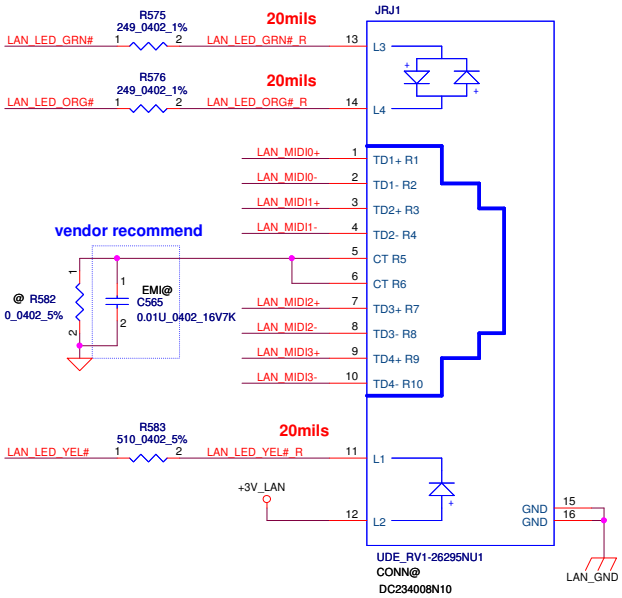
Crystal

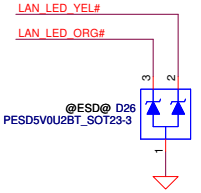


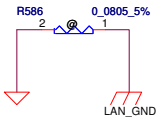
Green / Orage

Yellow

vendor recommend







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: LAN RTL8111G

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

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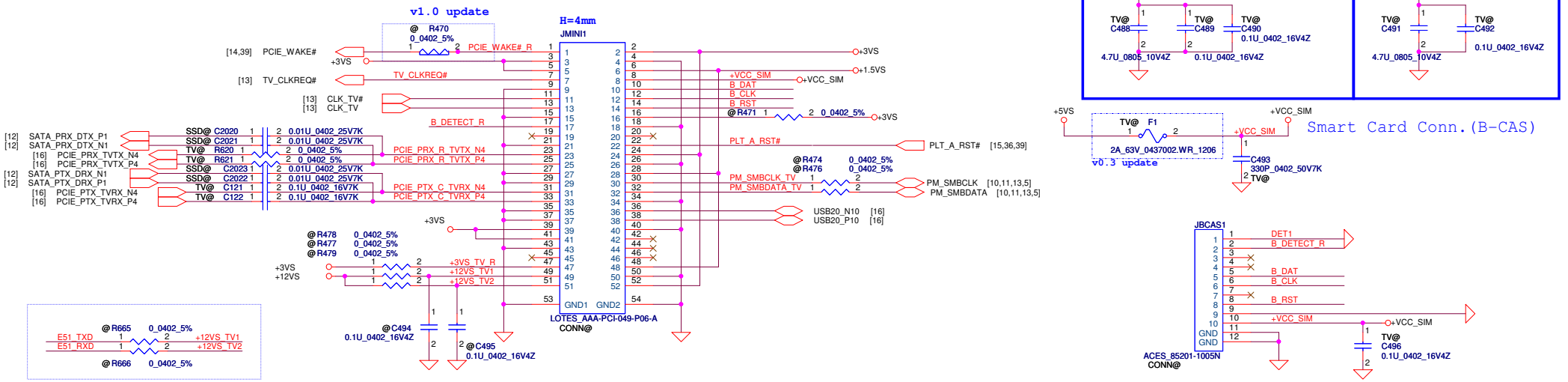
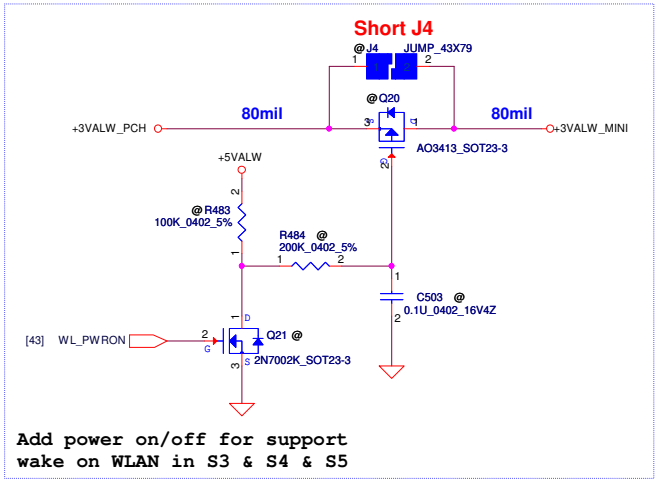
MINI (TV) /m-SATA SSD

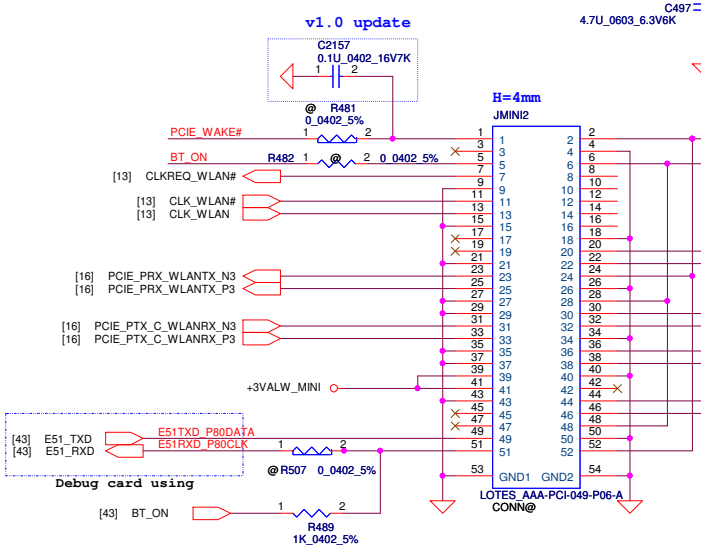
Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA

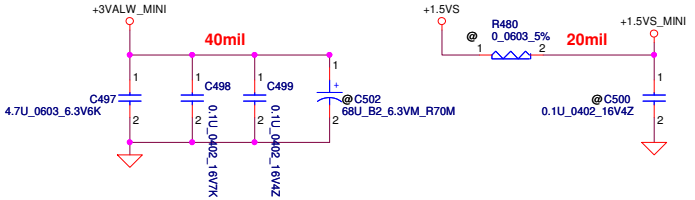


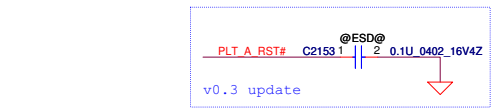
WLAN & Bluetooth Combo Card

Mini Card Slot 2--- WLAN Current: 3.3 : 750mA,









Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Title	PCIe-WLAN/TV_B-CAS		
Size	Document Number		Rev
	ZEA00 LA-A061P M/B		0.3
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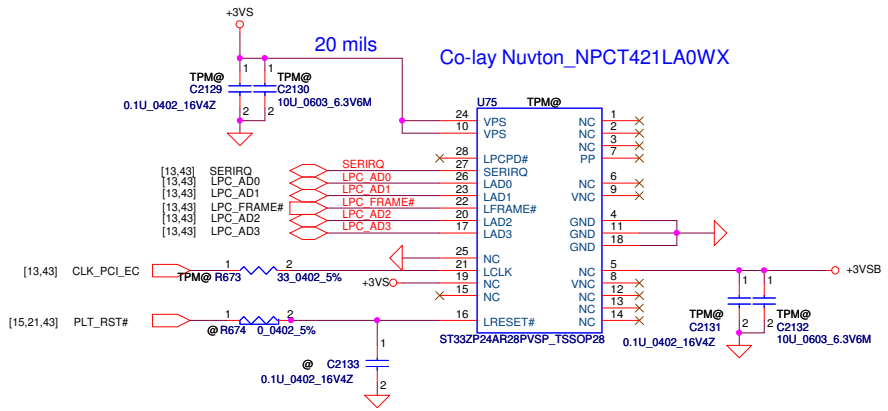
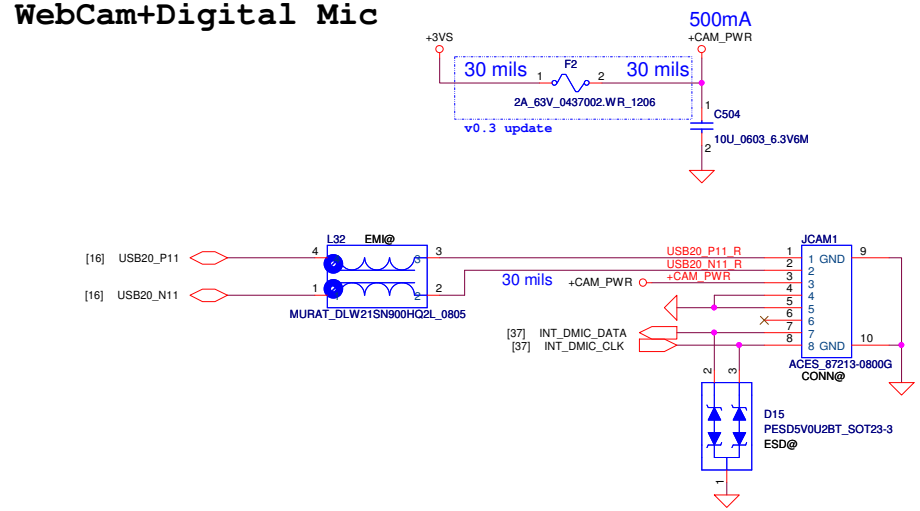
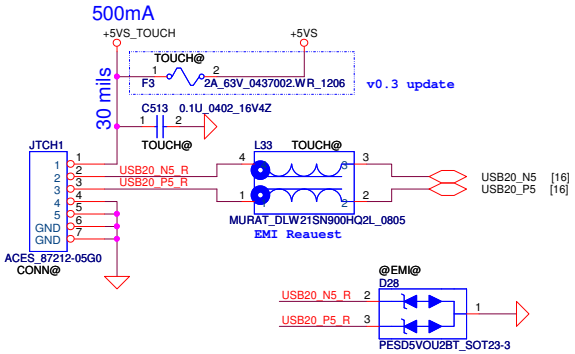
TPM(Reserve)



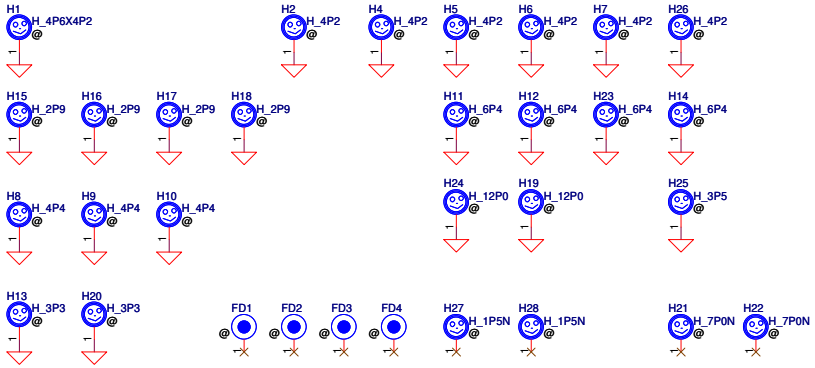
WebCam+Digital Mic



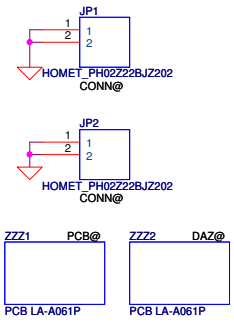
Touch



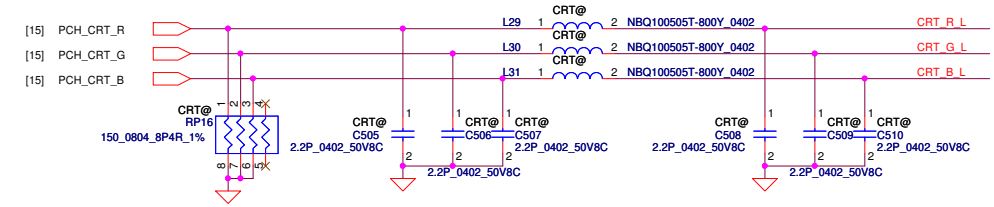
Screw Hole



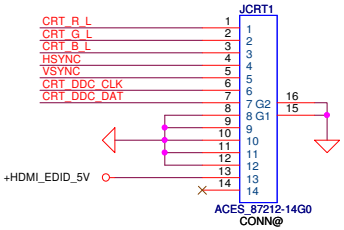
PCH heat sink

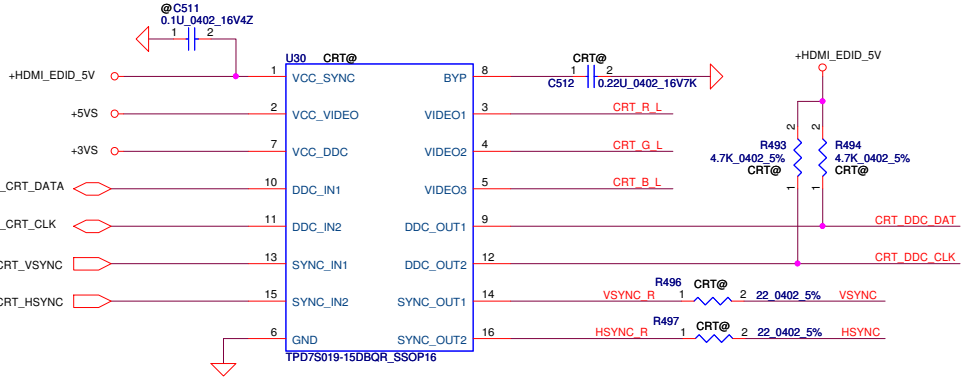


CRT Conn(Reserve 15pin)



Need PU/PL on PCH/FCH side
(2.2K*2pcs for DDC & 150_8P4R*1pcs for RGB)



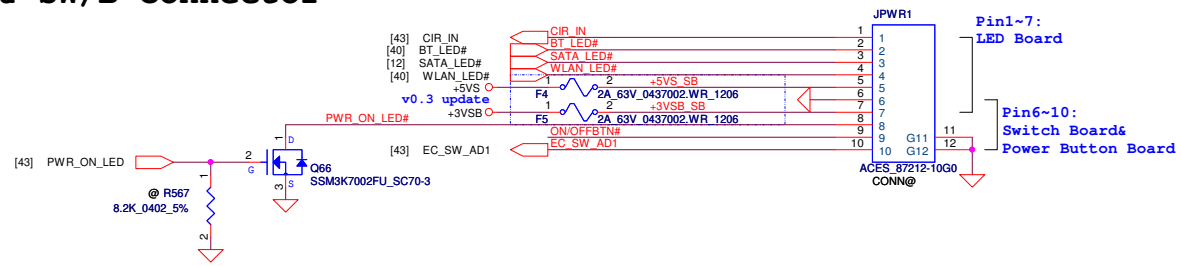


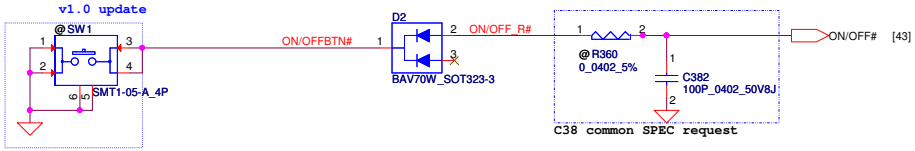
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

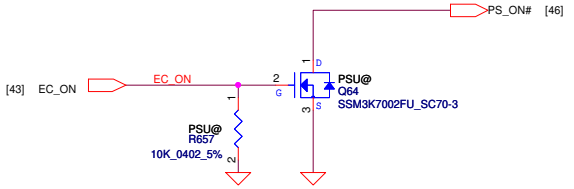
Title	PWR/Cap./TP/LED/LP/LS/Screw		
Size	Document Number	ZEA00 LA-A061P M/B	Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 41 of 59		

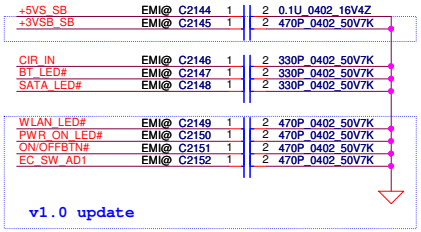
Power/B & SW/B Connector

8Pin sub-board Conncetor

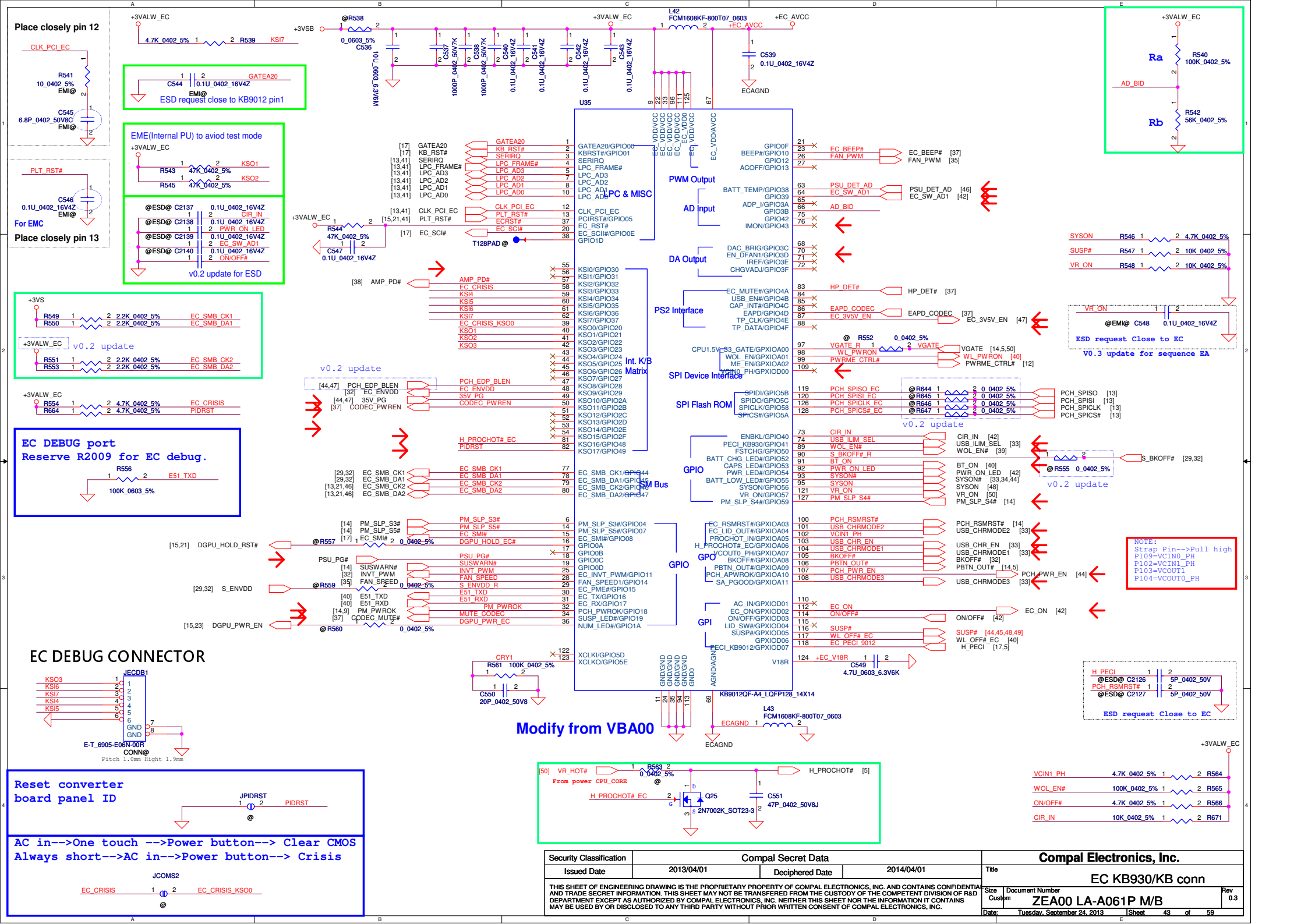








Compal Electronics, Inc.			
Title	Sub-board Connector		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 42 of 59		

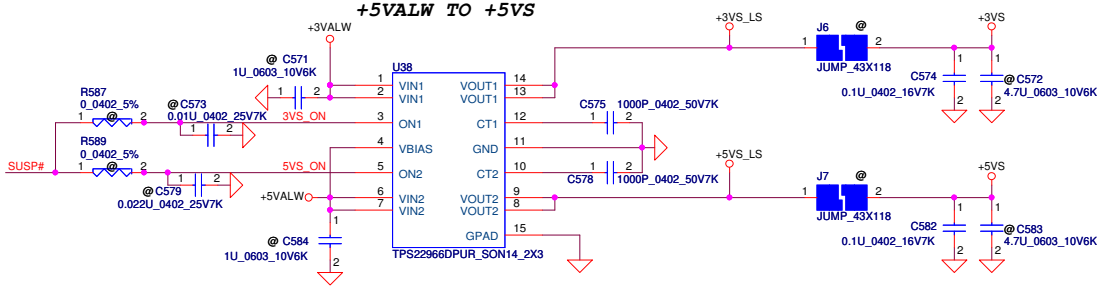


Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

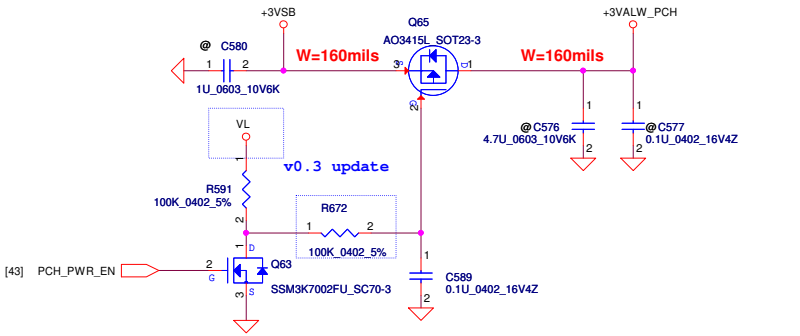
Compal Electronics, Inc.			
Title	EC KB930/KB conn		
Size	Document Number		Rev
Custom	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	43 of 59

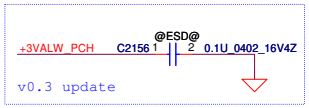
+3VALW TO +3VS
+5VALW TO +5VS

Vgs=10V, Id=9A, Rds=18.5mohm



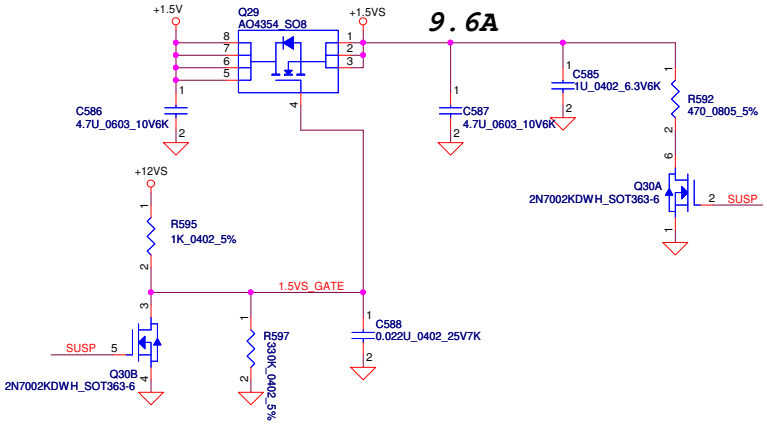
+3VALW TO +3VALW_PCH

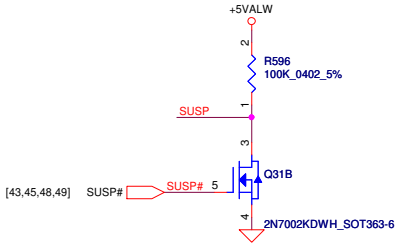




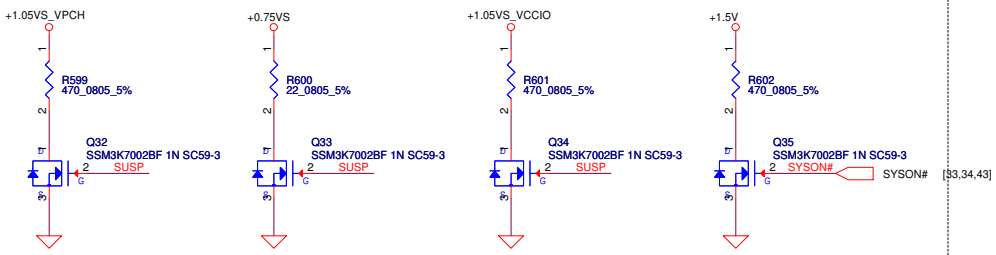
+1.5V to +1.5VS

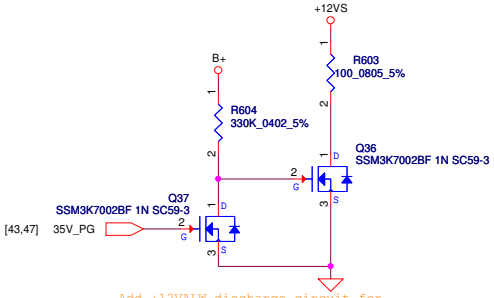
9.6A





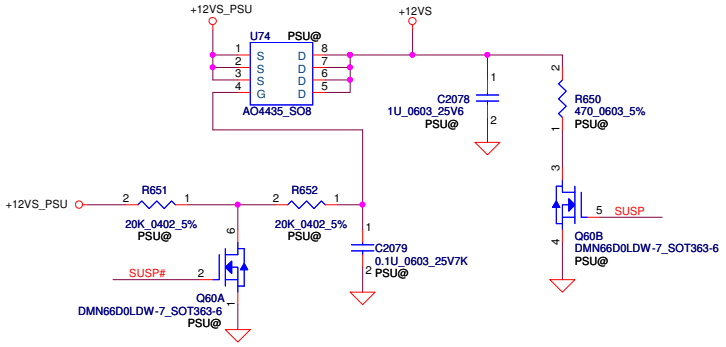
Discharge circuit





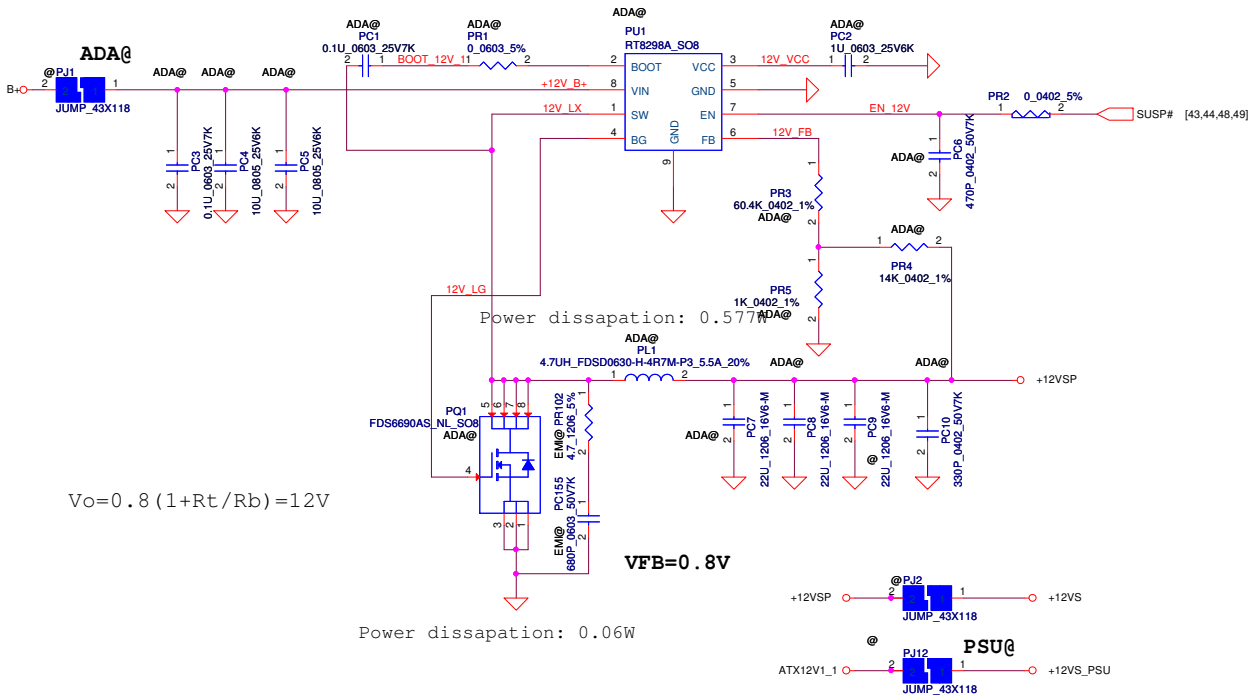
Add +12VALW discharge circuit for prevent DC plug in leakage 5/5.

+12V1 TO +12VS (Reserve for PSU)



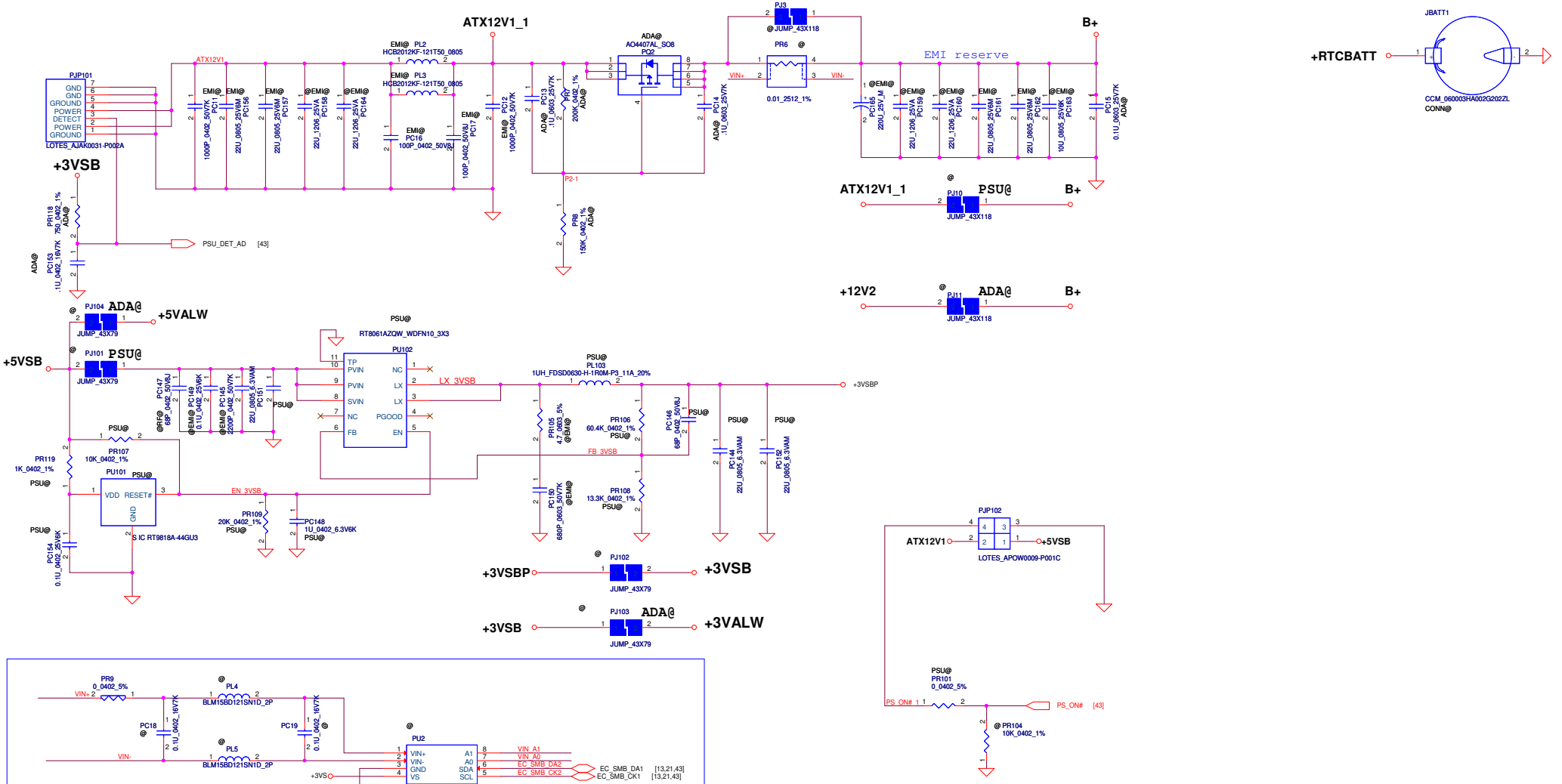
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

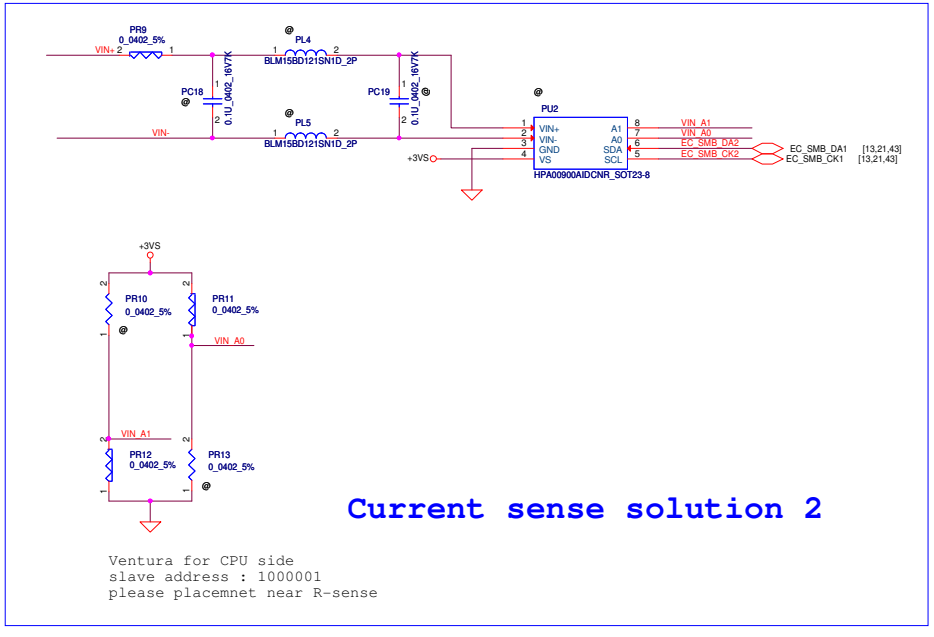
Compal Electronics, Inc.			
Title	DC-DC INTERFACE		
Size	Document Number ZEA00 LA-A061P M/B		Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 44 of 59		



Security Classification	Compal Secret Data		
Issued Date	2012/04/27	Deciphered Date	2013/04/27

Compal Electronics, Inc.			
Title: PWR- 12VSP			
Size: Custom	Document Number: VBA11 LA-A111 M/B		Rev: 0.1
Date: Tuesday, September 24, 2013	Sheet 45 of 56		





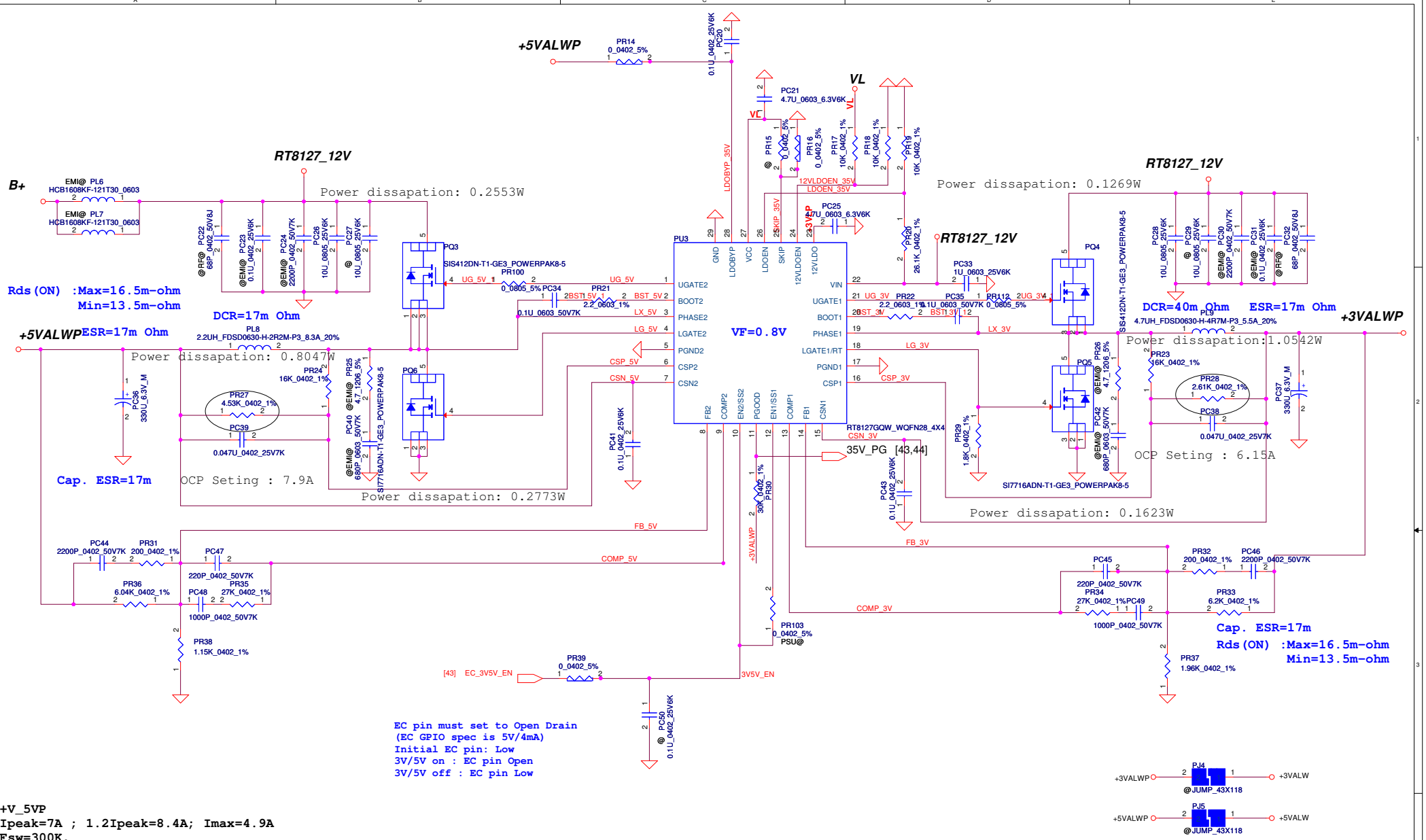
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2012/11/12

Compal Electronics, Inc.

Title: PSU IN

Size	Document Number	Rev
C		0.1

Date: Tuesday, September 24, 2013 | Sheet 46 of 56



+V_5VP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
Fsw=300K,
Iocp>=8.66A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

+V_3.3VP
Ipeak=4.437A ; 1.2Ipeak=5.325A; Imax=3.106A
Fsw=300K
Iocp>=5.33A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

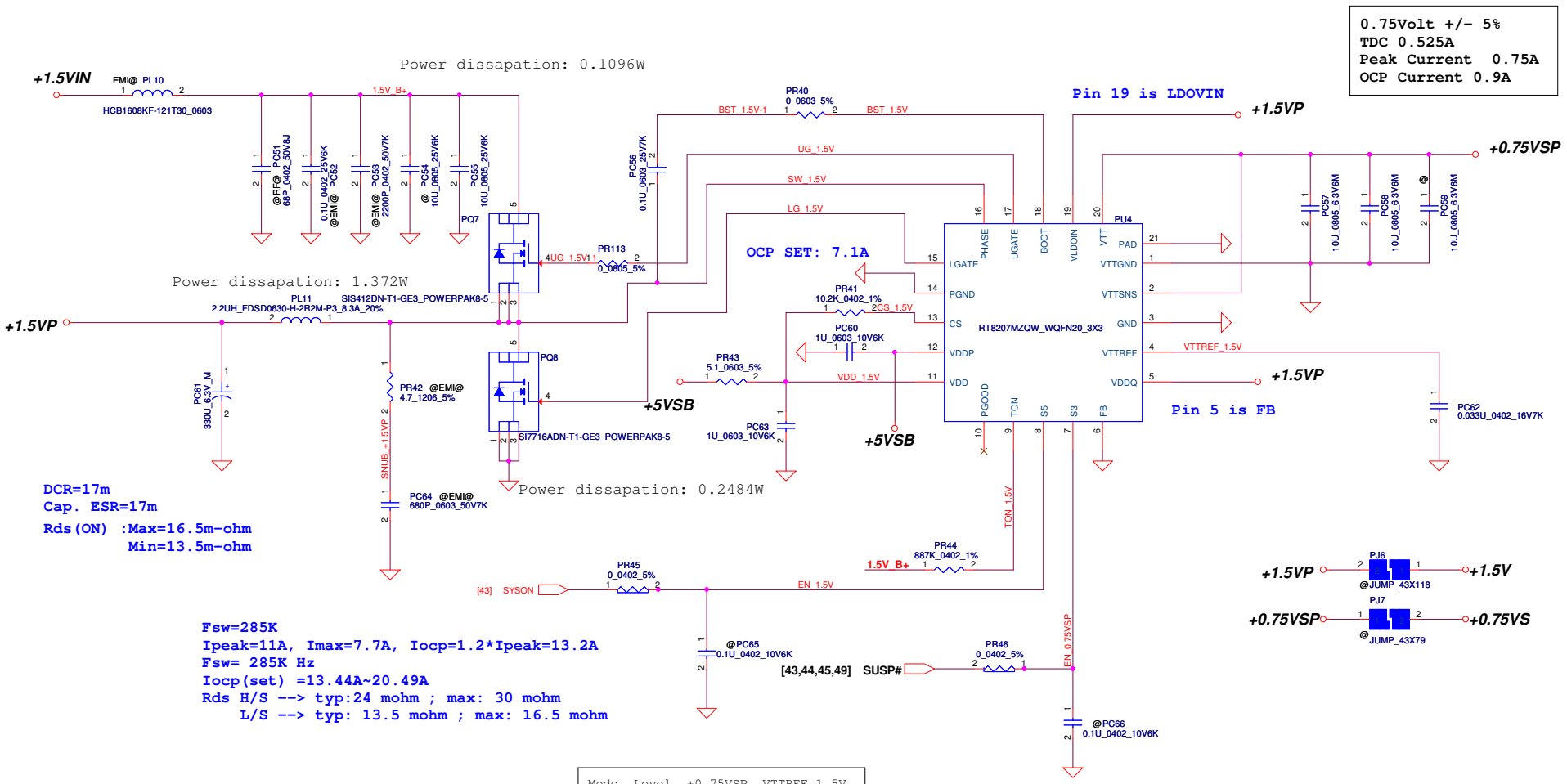
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR- 3VALWP/5VALWP

Size: Custom | Document Number: VCA00 LA-9792P M/B | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 47 of 56

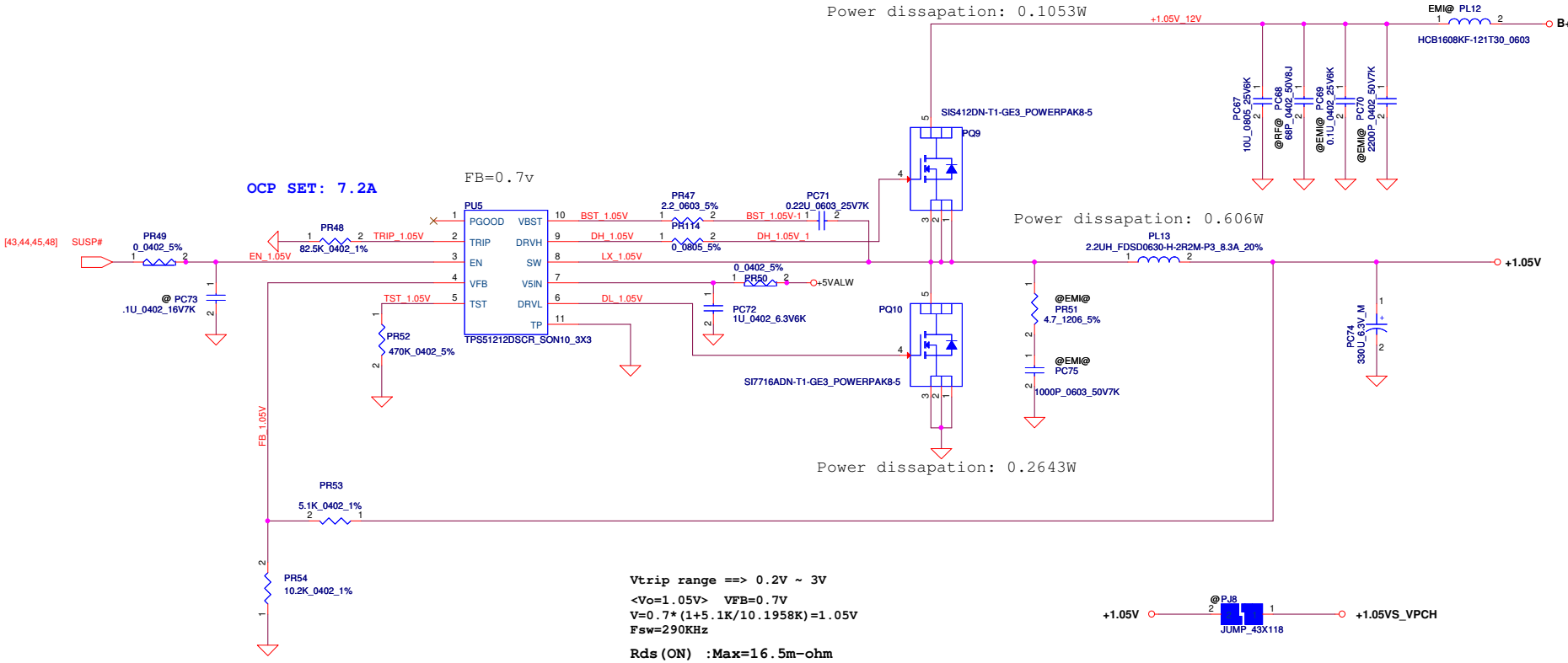


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.			
Title: 1.5VP			
Size: B	Document Number		Rev: 0.1
Date: Tuesday, September 24, 2013	Sheet 48 of 56		



Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: +1.05VSP

Size: Custom | Document Number | Rev: 0.1

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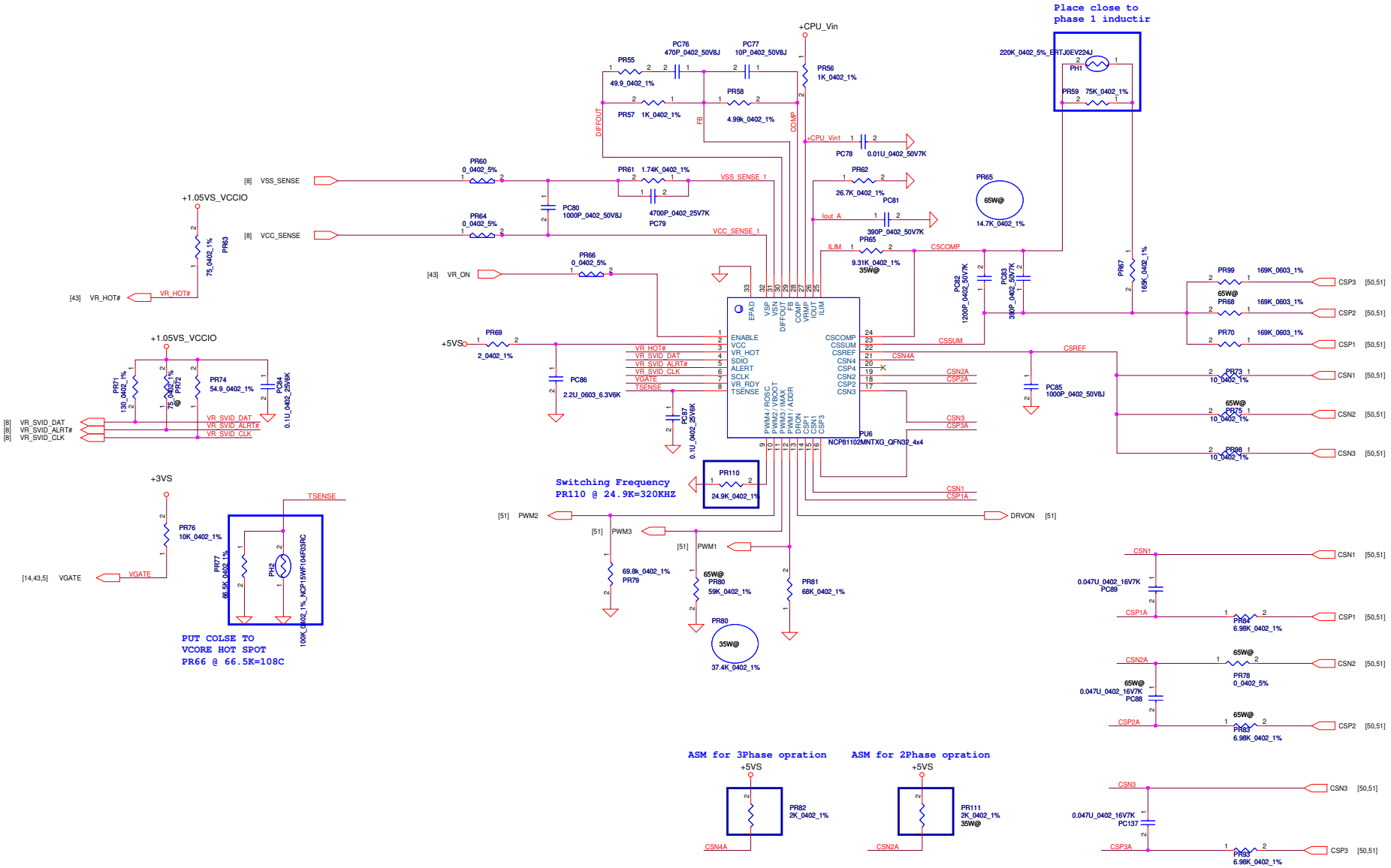
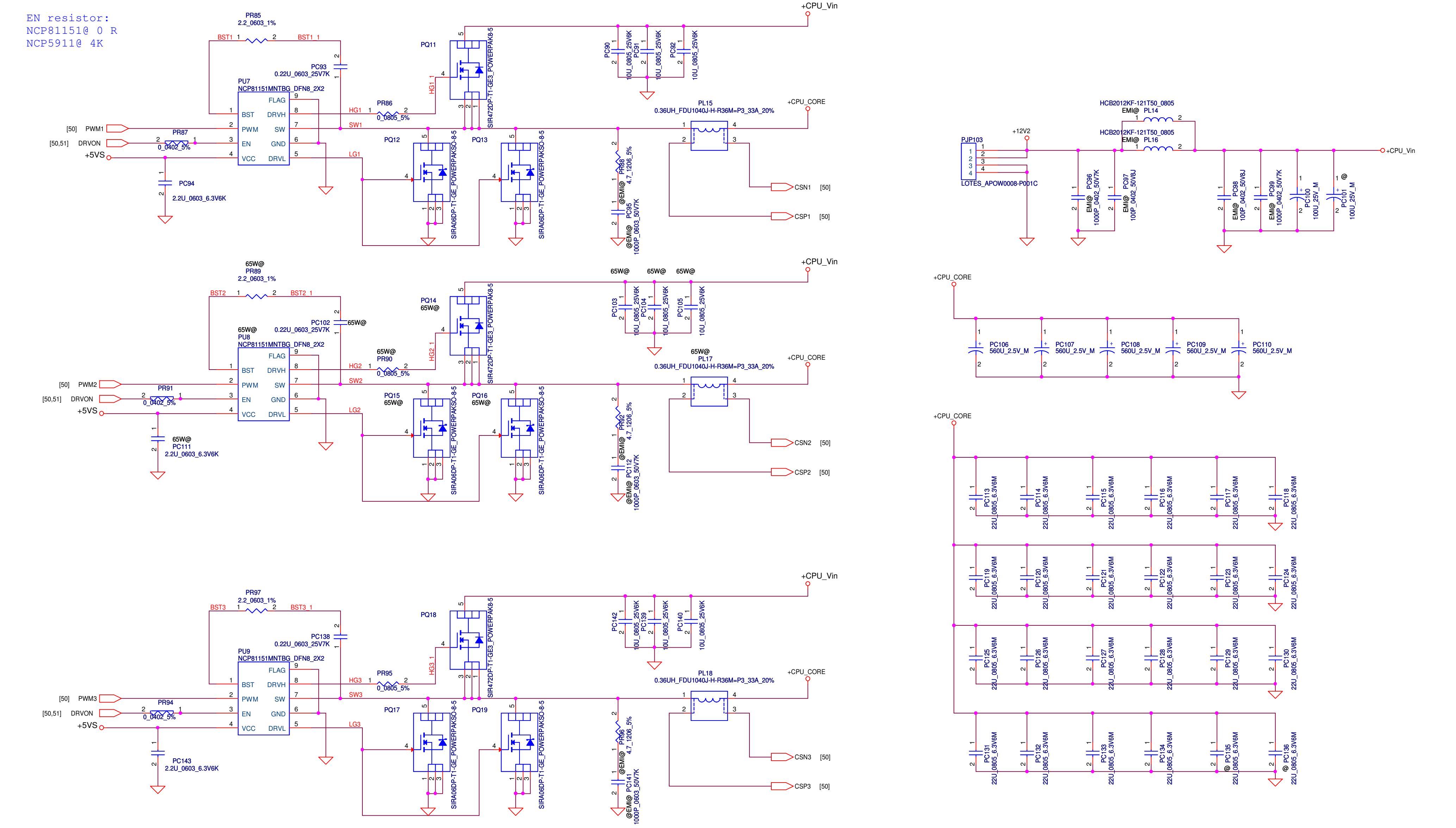


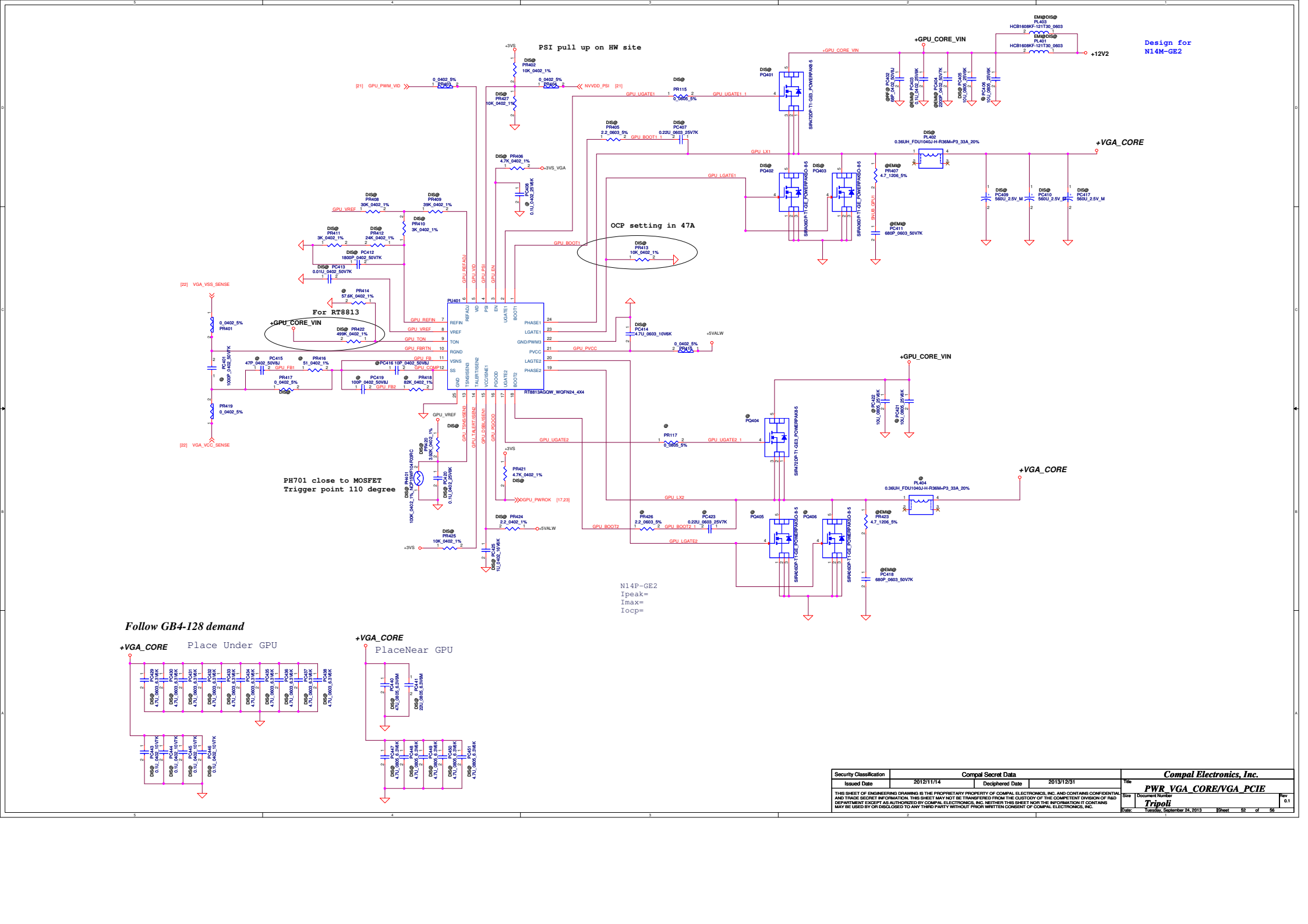
Title	NCP81102	
Size	Document Number VCA00 LA-9792P M/B	Rev 0.1
Date: Tuesday, September 24, 2013	Sheet 50 of 56	



Title
Power Stage

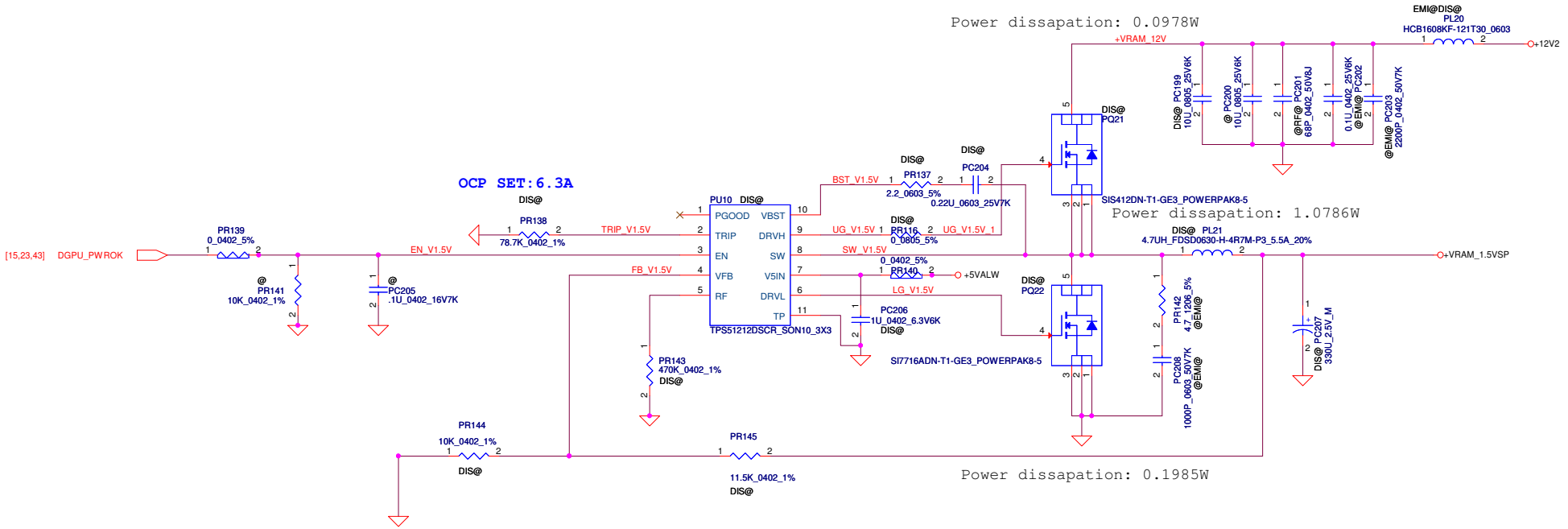
Size | Document Number | Rev
VCA00 LA-9792P M/B | 0.1

Date: Tuesday, September 24, 2013 | Sheet 51 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/11/14	Deciphered Date	2013/12/31

Compal Electronics, Inc.	
Title	PWR_VGA_CORE/VGA_PCIE
Size	Document Number: Tripoli
Rev	0.1
Date: Tuesday, September 24, 2013	Sheet 52 of 56



Cap. ESR=17m
Rds(ON) :Max=15m-ohm
Typ=12m-ohm
Vtrip range ==> 0.2V ~ 3V
<Vo=1.5V> VFB=0.7V
V=0.7*(1+11.5K/10K)=1.505V
Fsw=290KHz

Ipeak=4.7A, Imax=3.29A, Iocp=1.2*Ipeak=5.64A

Iocp(set)=5.718A~8.304A

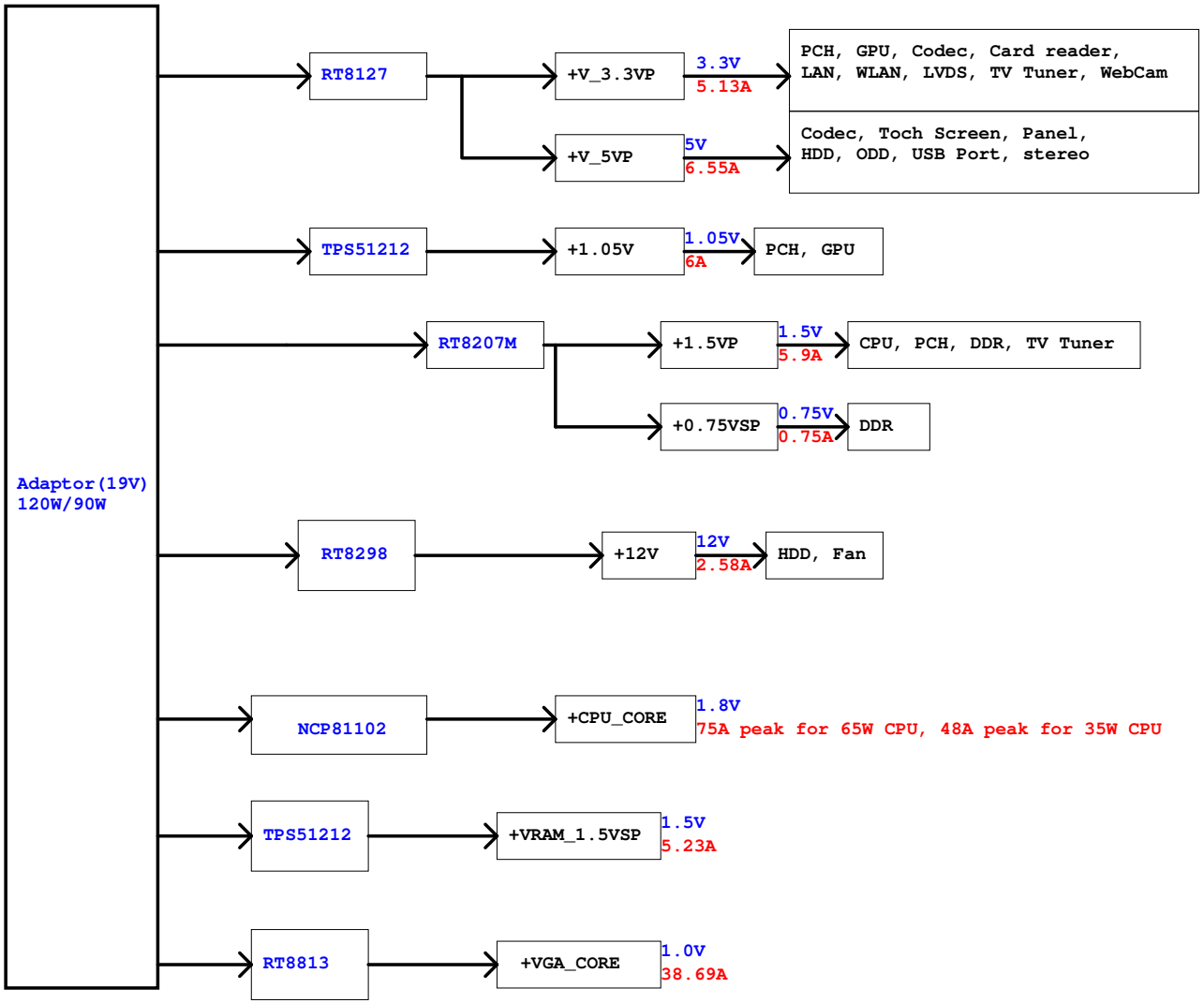
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR-VRAM_1.5VSP

Size: Custom | Document Number: VCA00 LA-9792P M/B | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/09/12	Deciphered Date	2012/09/12

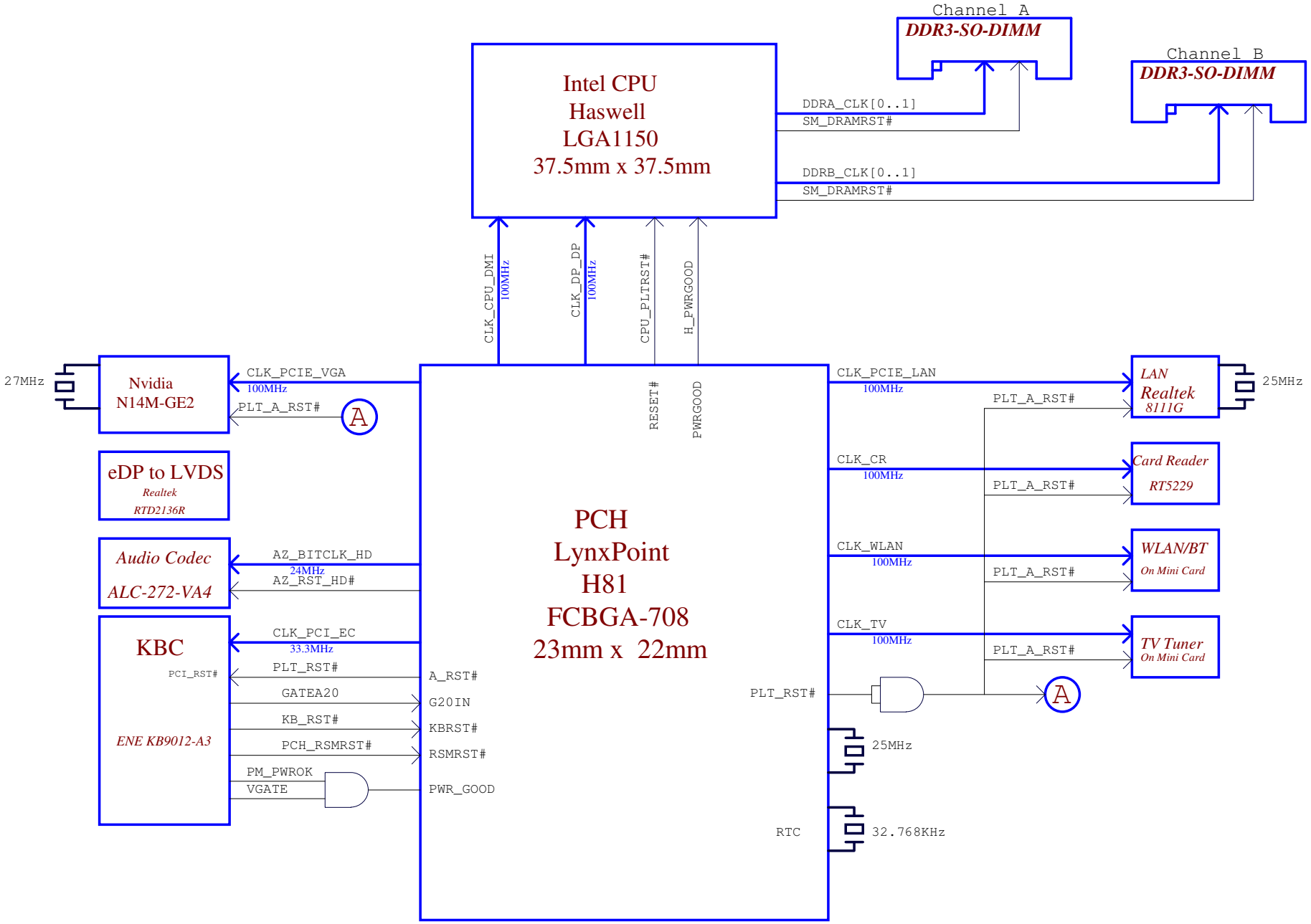
Compal Electronics, Inc.

Title: Power Rail

Size	Document Number	Rev
Custom	QLA13/15 LA-8501P M/B	0.4

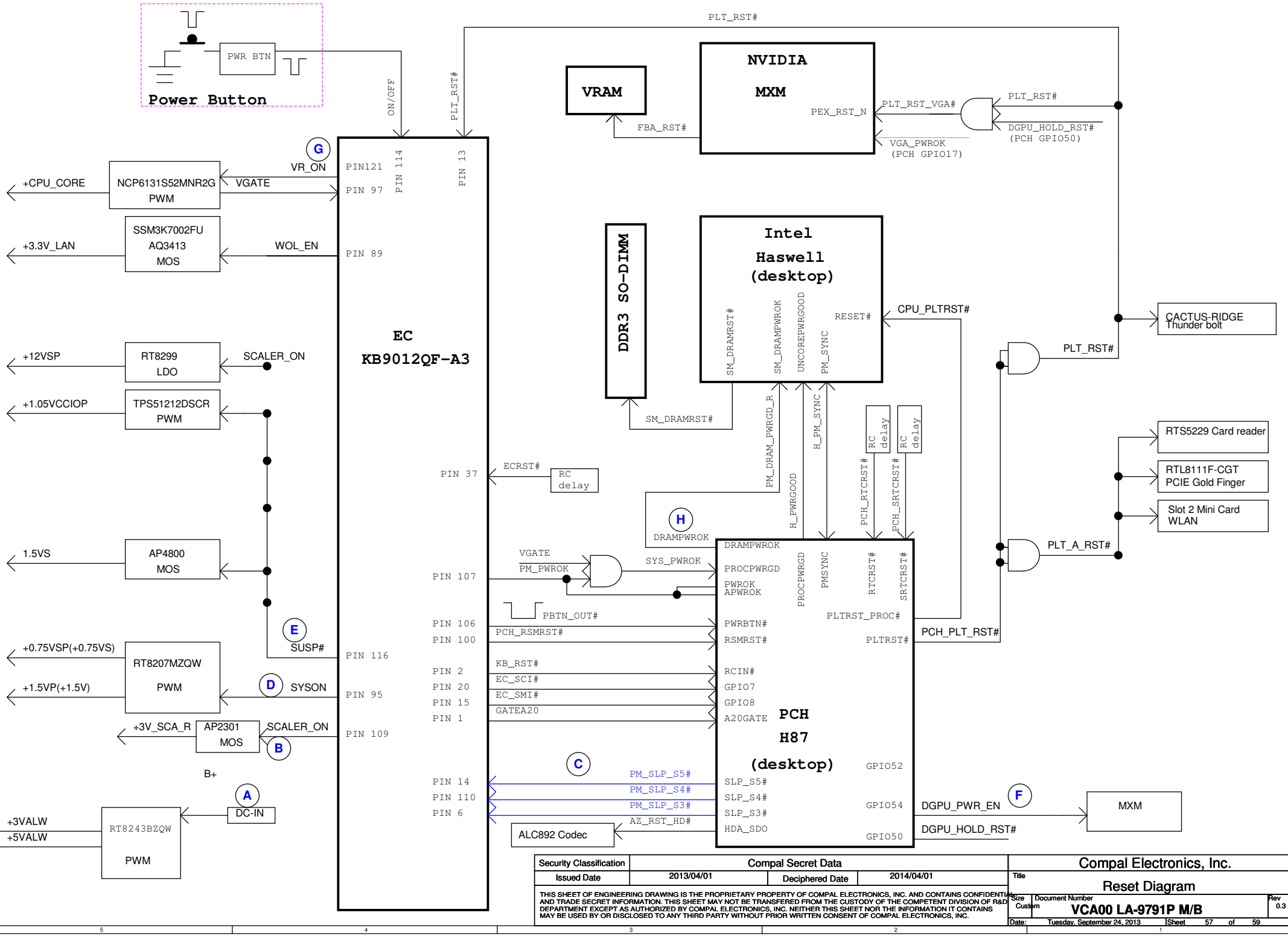
Date: Tuesday, September 24, 2013 | Sheet 55 of 59

Clock and Reset Diagram



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title: Clock/Reset Diagram			
Size: Custom	Document Number: VIA15 LA-A071P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 56 of 59		



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Reset Diagram

Size	Document Number	Rev
Custom	VCA00 LA-9791P M/B	0.3

Date: Tuesday, September 24, 2013 Sheet 57 of 59

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	20130604	P47	Add PC154 and Change the pu101 to SA00005A600	For Pericom issue
2.	20130729	P45	Add PR105 ,PC155 Snaber	For EMI Request
3.	20130729	P45	Add PR1	For EMI Request
3.	20130729	P45	Add PR39	For S5 power loss issue

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/09/12	Deciphered Date	2012/09/12

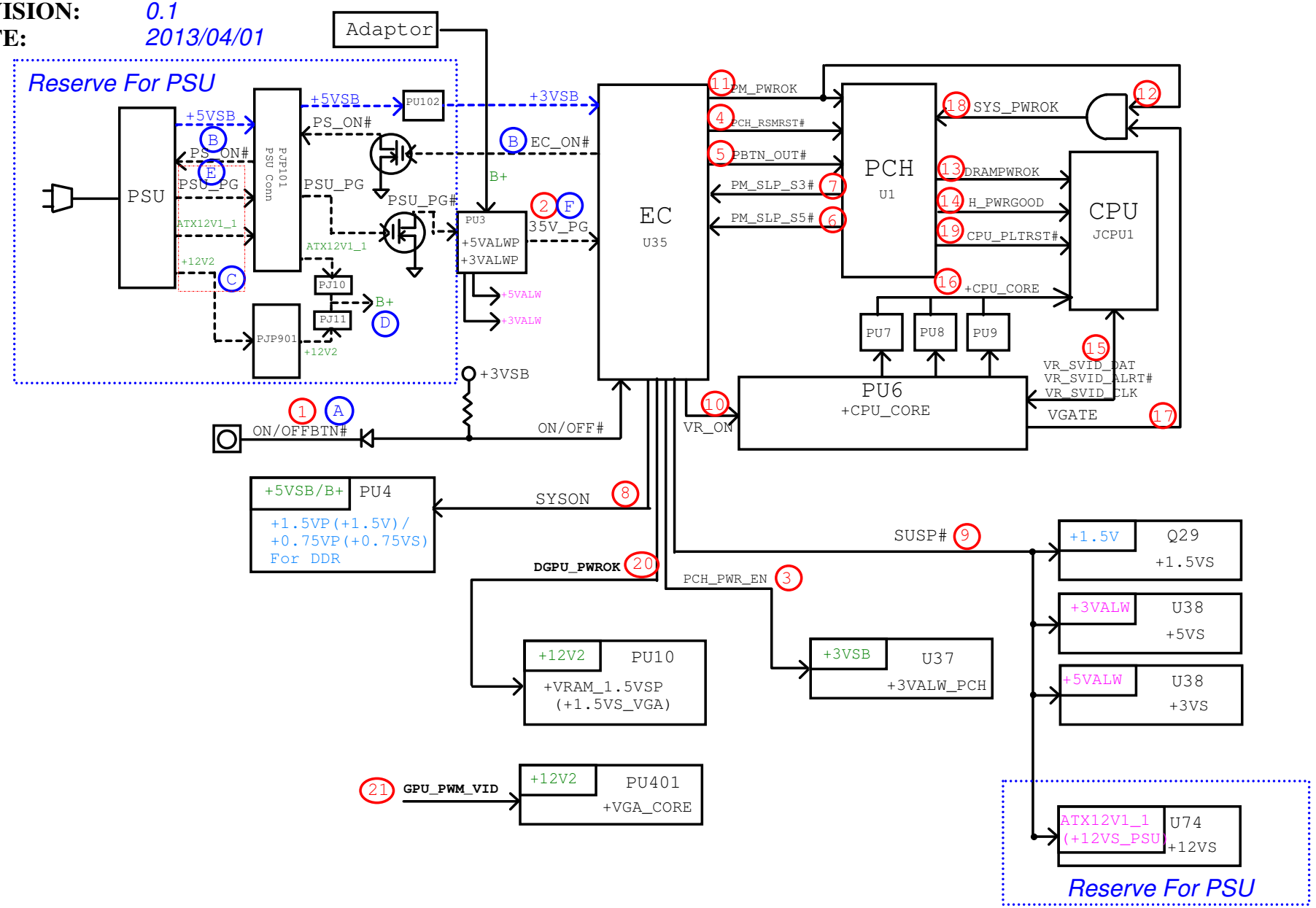
Title: PWR_PIR

Size: Custom | Document Number: B555 VAA15 LA-A072P MB | Rev: 0.5

Date: Tuesday, September 24, 2013 | Sheet 57 of 60

COMPAL CONFIDENTIAL

MODEL NAME: *ZEA00 Power Sequence Block Diagram (Discrete)*
PCB NAME: *LA-A061P*
REVISION: *0.1*
DATE: *2013/04/01*



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/01	Deciphered Date	2014/04/01
Title	Power Sequence Diagram		
Size Custom	Document Number ZEA00 LA-A061P M/B		Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 58 of 59		

HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 --> 0.2
GERBER-OUT DATE: 2013/06/20

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1. Change C45 from SF000002V00 to SF000003X00
2. Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.
3. ~~Change LCD_BKOFF# control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.~~
4. Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.
5. Pop R428 for AZ_SDIN0_HD.
6. U2 footprint change from socket to IC.
7. Add RH11
8. Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF
9. Change R423 location to L45
10. Change D7 from SC2N202U010 to SC600000B00 for 替代料
11. Change Q29 from SB548000210 to SB00000ZN00.
12. Change D8&D9 from SCS00002G00 to SCS00000Z00
13. X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB00000EO00. 2.Change Q9 from SB934130020 to SB934130000.
    3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00.
14. Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.
15. Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).
16. Change Q10 from SB00000FC00 to SB00000L800 for 替代料
17. Remove R469 0ohm for TV.
18. Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.
19. Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.
20. Pop U7&R231, un-pop R228 for PLT_RST_VGA#.
21. Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.
22. Un-pop LAN power components Q26,Q27,R573,R574,C562.
23.0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647
24.Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.
25.Pop R438,R439 for ESD request.

PVT change list:
1. Change Q10 from SB00000FC00(EOL soon) to SB00000ZN00(同Q29),SB00000FC00 as 2nd source.Schematic,需驗證
2. Change U23 pin12_+USB3_VCCA to +USB3_VCCB, pop U22, un-pop U24 for USB charger
3. R365 change from short pad to 0ohm.
4. U5 pin5 change from +3VSto +3VALW_PCH for BCM43142 wake from WLAN issue.
5. Change R473,R490,R677,R678,R679 from SP040005X00_0603 size to F1,F2,F4,F5,F3 SP040003S00_1206 size.
6. Change L11 from SM010014520 to SM01000EJ00 for ACL request
7. Change L8 from SM010007W00 to SM010019400 for ACL request
8. Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..
9. Change RP19 from SD309510A80(T88 P/N) to SD309510A10.
11. Change R276 from 10k to 100k for +3VS_VGA rise time.
12. Change R672 from 10k to 100k for +3VALW_PCH rise time.
14. Change R438 & R439 from 0_0603 to short pad.
15. Un-pop C125 & C548 for sequence EA.
16. Change C394, C398,C520 & C514 from 220uF(LELON_SF000001F00) to 100uF (Panasonic_SF000005100) to meet Inrush EA & ACL request.
17. Change C170 & C171 from 12pF to 10pF for EA.
20. Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.
21. Add R677 & reserve R678 on U5 AND gate for PLT_A_RST#
13. Change JUSB1 & JUSB2 from DC23300AE00 to DC233008R00(VBA11)
24. Change R591 pull-high from +5VSB to VL for power S5 Erp request.
22. Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request
23. Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request
10. Add C2144~C2152 for EMI request.
18. Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.
19. Reserve C2153,C2154,C2155,C2156, add D29 for ESD.
20. Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.
21. Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

pre-MP change list:
1. Change R399,R401,R402,R403,R404 from 0ohm to short pad.
2. Add C2157 and reserve C2158.
3. Change R8,R470,R669,R670,R416 from 0ohm to short pad.
4. Un-pop JECDB1 & SW1.
5. For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.
6. Change C520 & C514 from 100uF to 220uF.
7. Pop C2149~C2152 for ESD request.
8. Change C559 & C2128 from 0603 to 0805.
9. Change C2145 from 0.1uF to 470pF, change C2149~C2152 from 330pF to 470pF for EMI.
10. Add C418 for EMI.

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: *HW-PIR*

Size | Document Number: VCA00 LA-9791P M/B | Rev: 0.3

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