

Model Name : Z5WE3/Z5WT3

File Name : LA-A621P

Compal Confidential

EA50_BM UMA M/B Schematics Document

Intel Bay Trail M

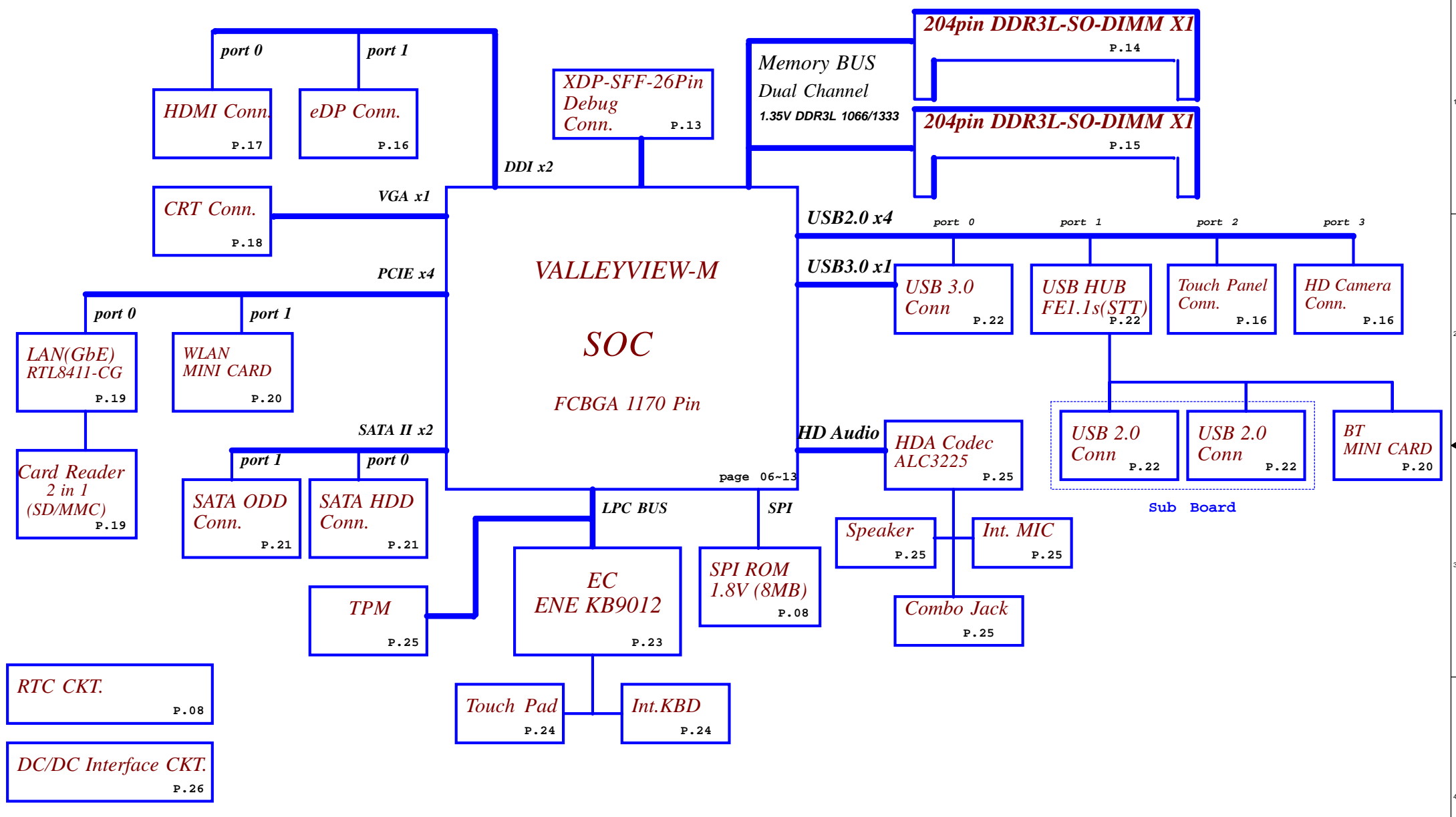
2013-09-03

REV:0.3

PCB@
ZZZ PCB 12R LA-A621P REV0 M/B

Part Number	Description
DA60012W000	PCB 12R LA-A621P REV0 M/B

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				Block Diagrams	
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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

43 level BOM table

43 Level	Description	BOM Structure
4319QPBOL01	SMT MB AA621 Z5WE3 BTM 1.67G HDMI	DBG@/EMC@/TS@/XDP@/B0@
4319QPBOL02	SMT MB AA621 Z5WE3 N2910 1.67G HDMI	DBG@/EMC@/TS@/XDP@/N2910@
4319QPBOL03	SMT MB AA621 Z5WE3 N3510 2.16G HDMI	DBG@/EMC@/TS@/XDP@/N3510@
4319QPBOL04	SMT MB AA621 Z5WE3 N2910 B2 1.67G HDMI	DBG@/EMC@/TS@/XDP@/N2910B2@



S IC FH8065301546401 QF9D B1 1.67G ABO!
Part Number = SA000072B20



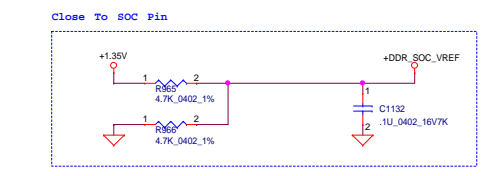
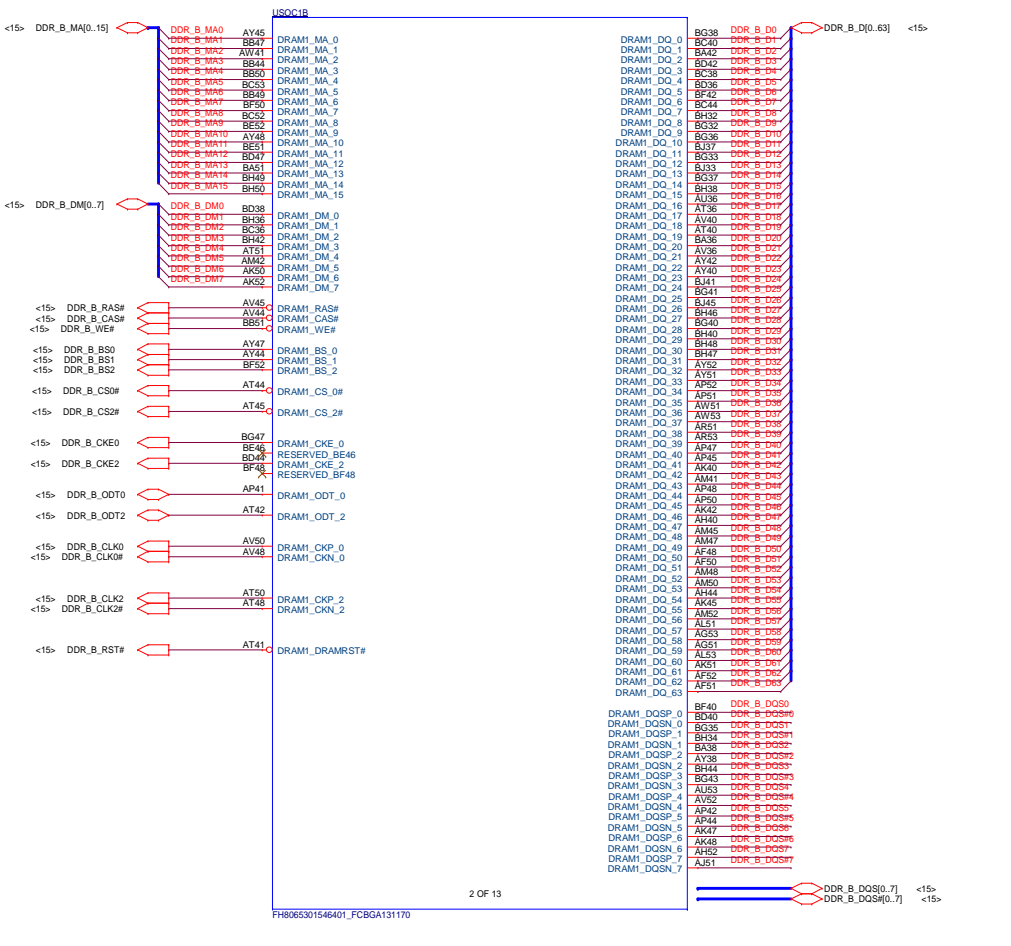
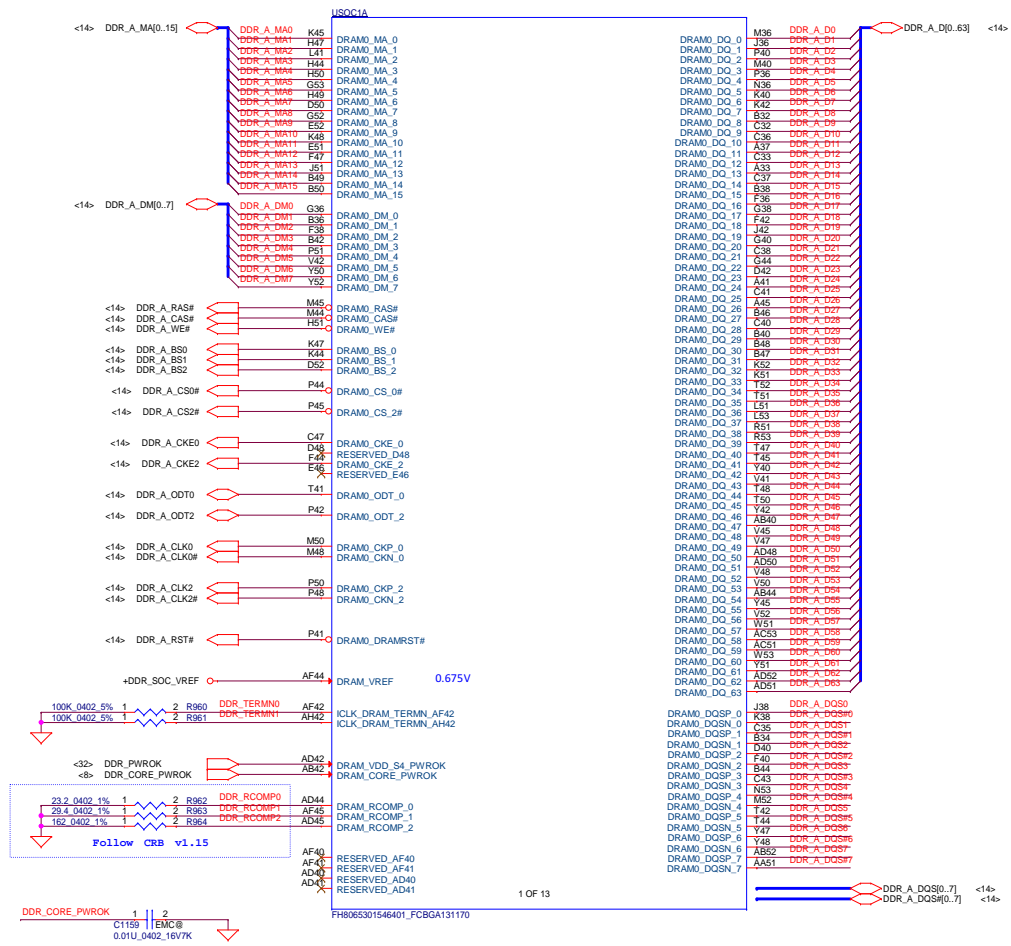
S IC FH8065301546300 QF9E B1 2.16G ABO!
Part Number = SA000075010



S IC FH8065301546402 QFH0 B2 1.6G ABO!
Part Number = SA000072B60

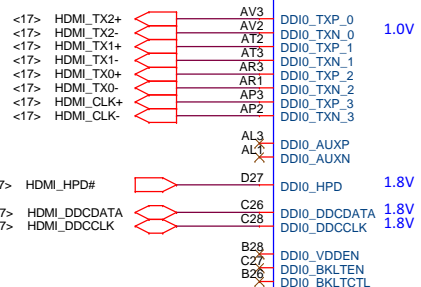
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Intel BayTrail-M Platform

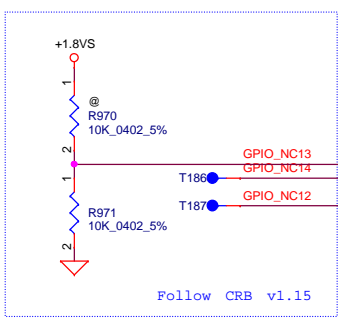


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								5	Intel BayTrail-M Platform	0.3	
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HDMI



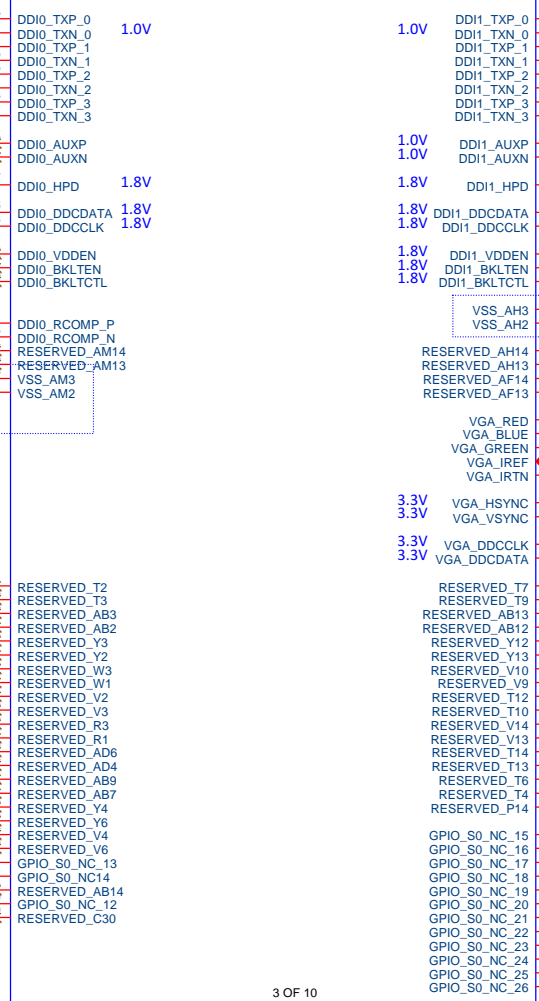
Follow CRB v1.15 0ohm till to GND



Follow CRB v1.15

GPIO_S0_NC[13]:
Multiplexed with Hardware Straps Pin:MDSI_DDCDATA

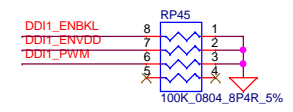
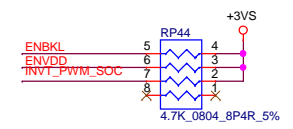
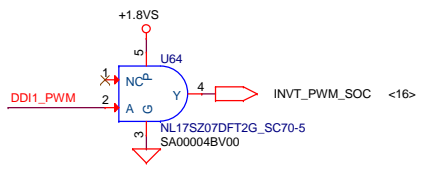
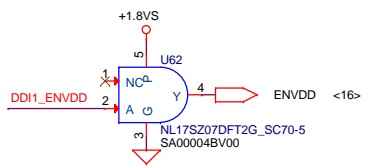
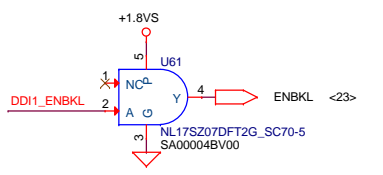
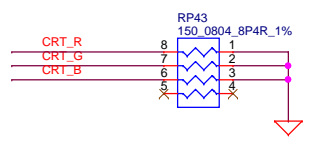
USOC1C



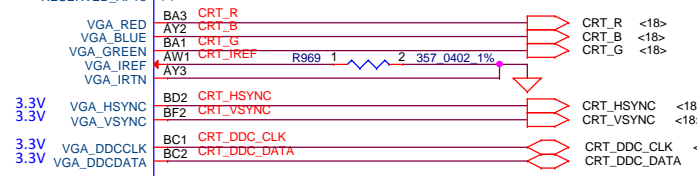
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FH8065301546401_FCBGA131170

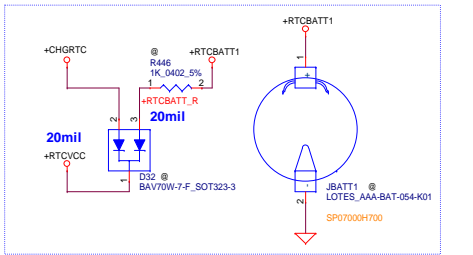
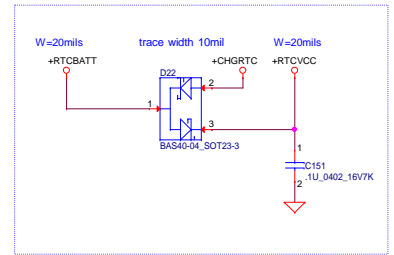
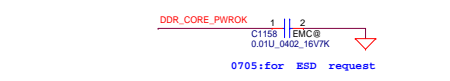
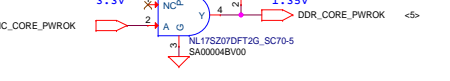
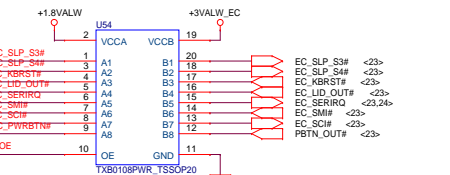
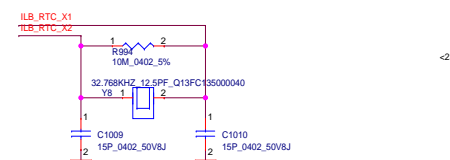
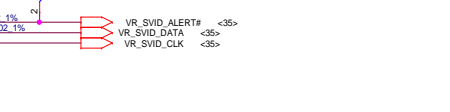
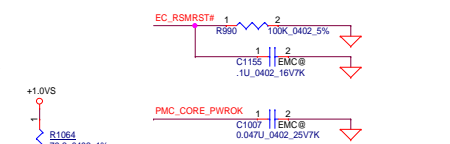
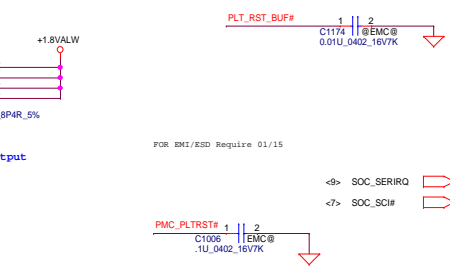
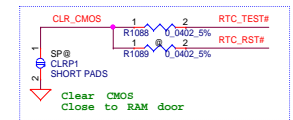
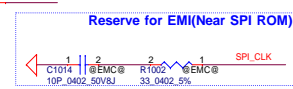
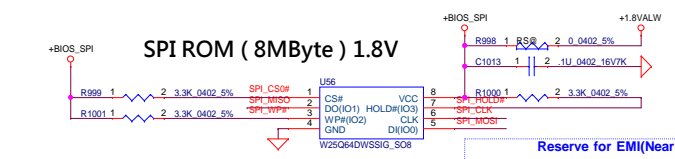
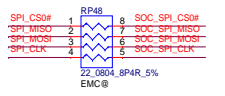
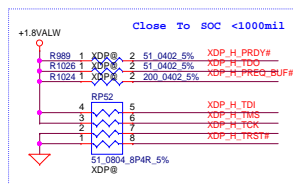
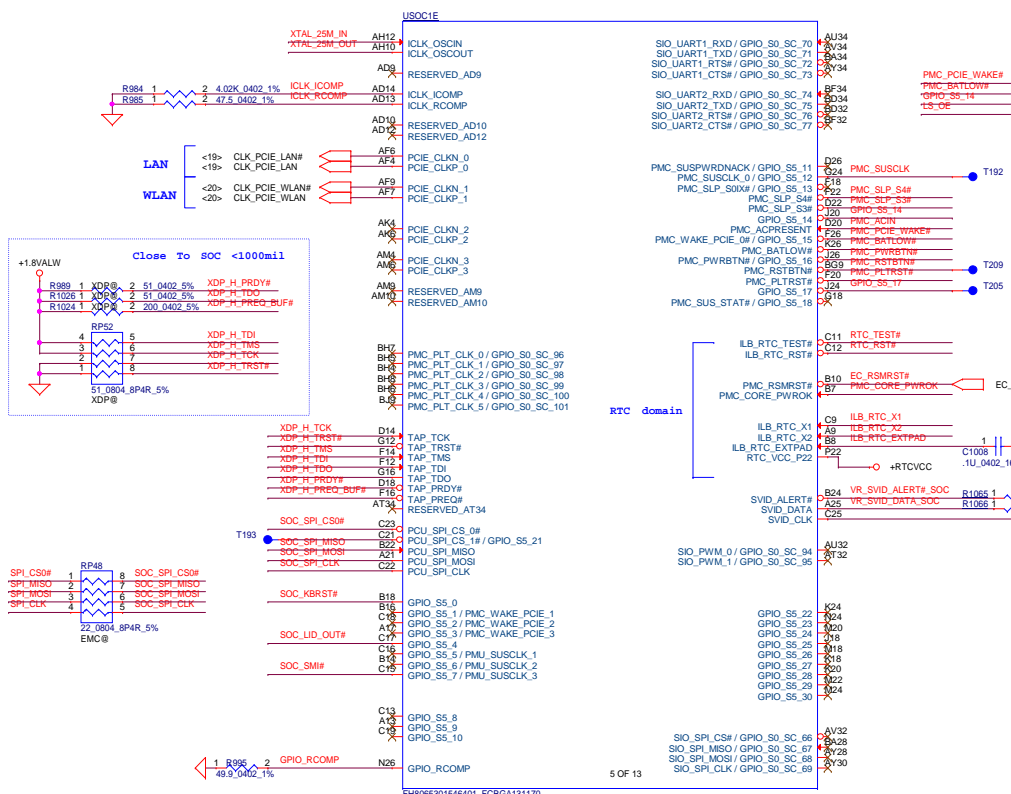
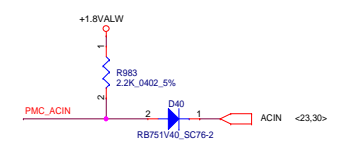
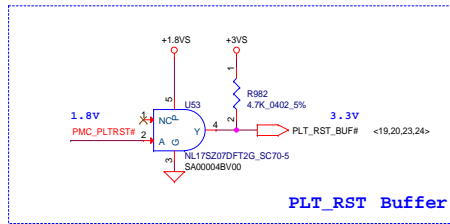
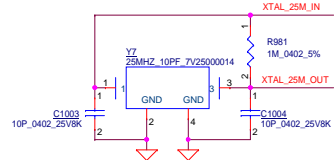
eDP Panel



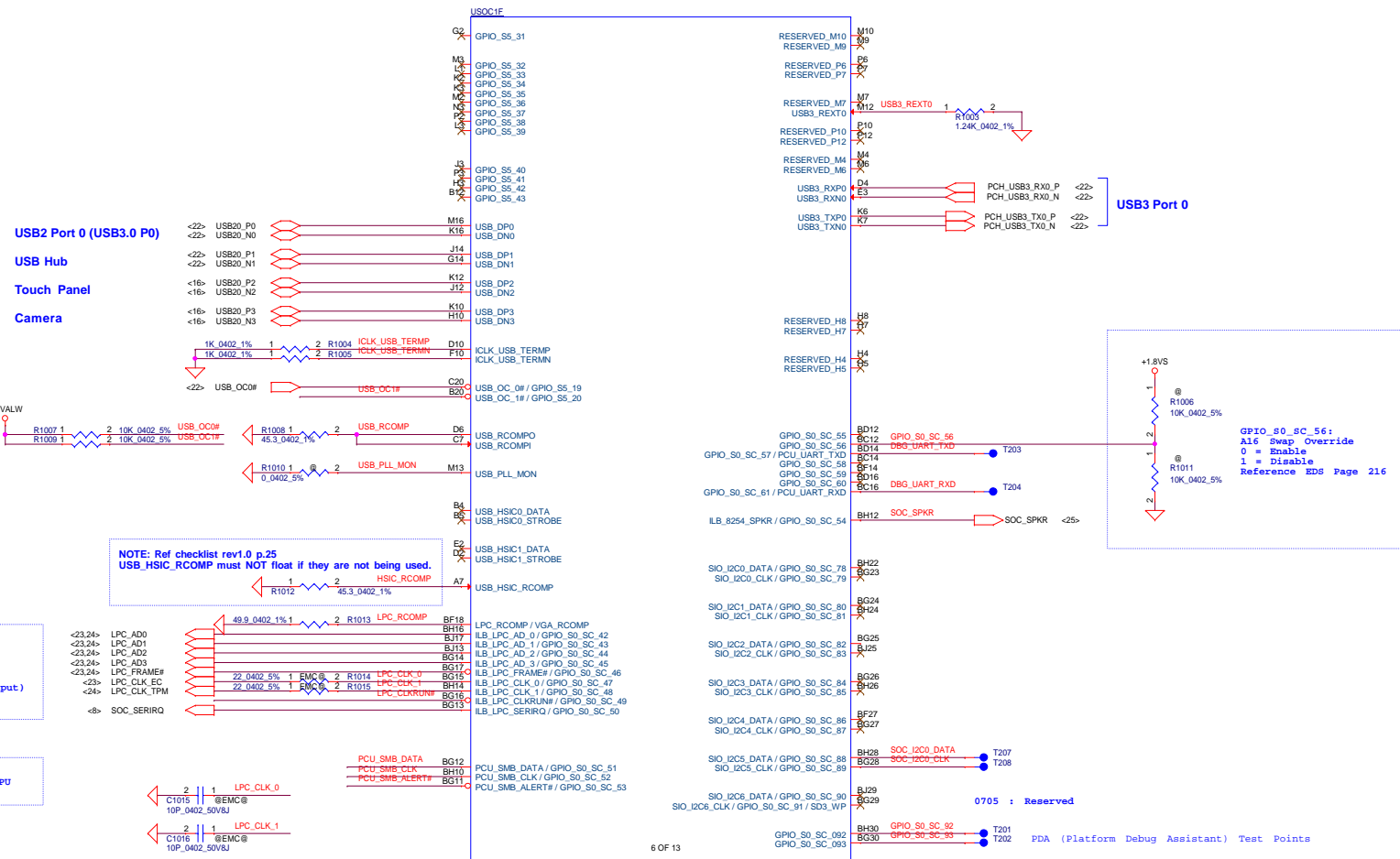
CRT



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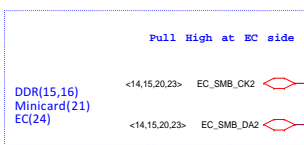
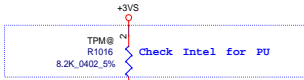


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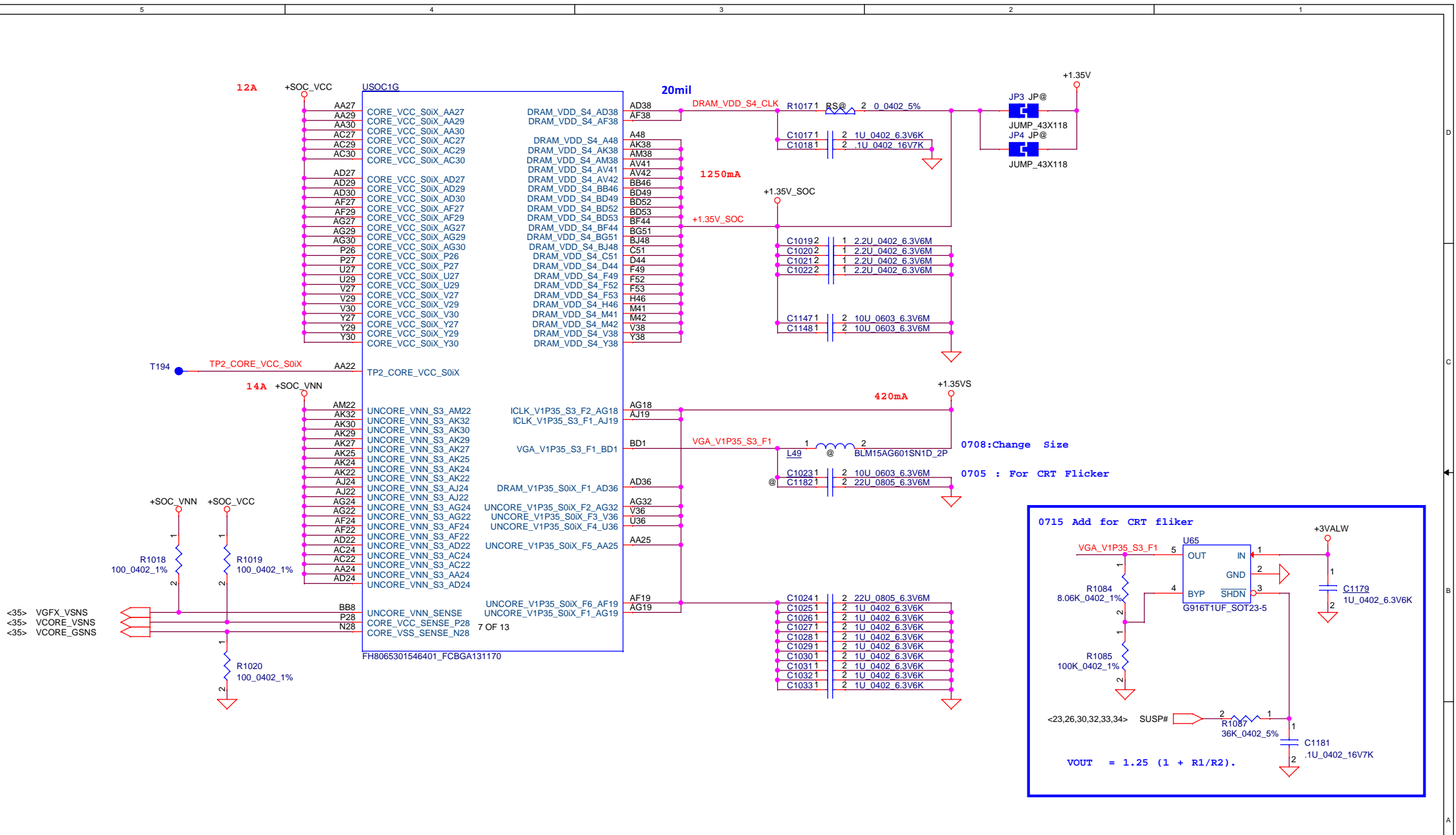


ILB_LPC_CLK_0 : Output of 25MHz,
Need Check with EC

ILB_LPC_CLK_1 is for CLK_0 feedback.(Input)
Set to Output for Normal Usage

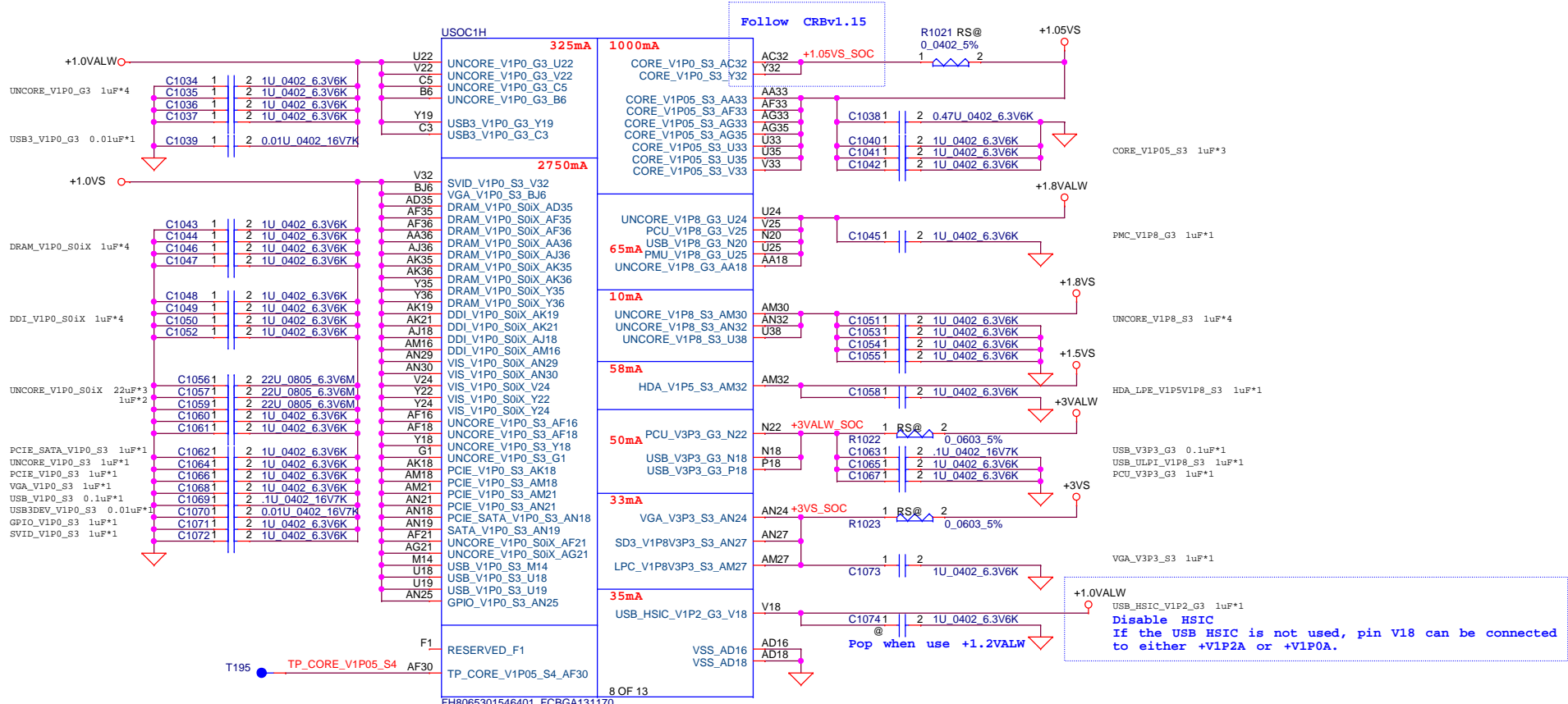


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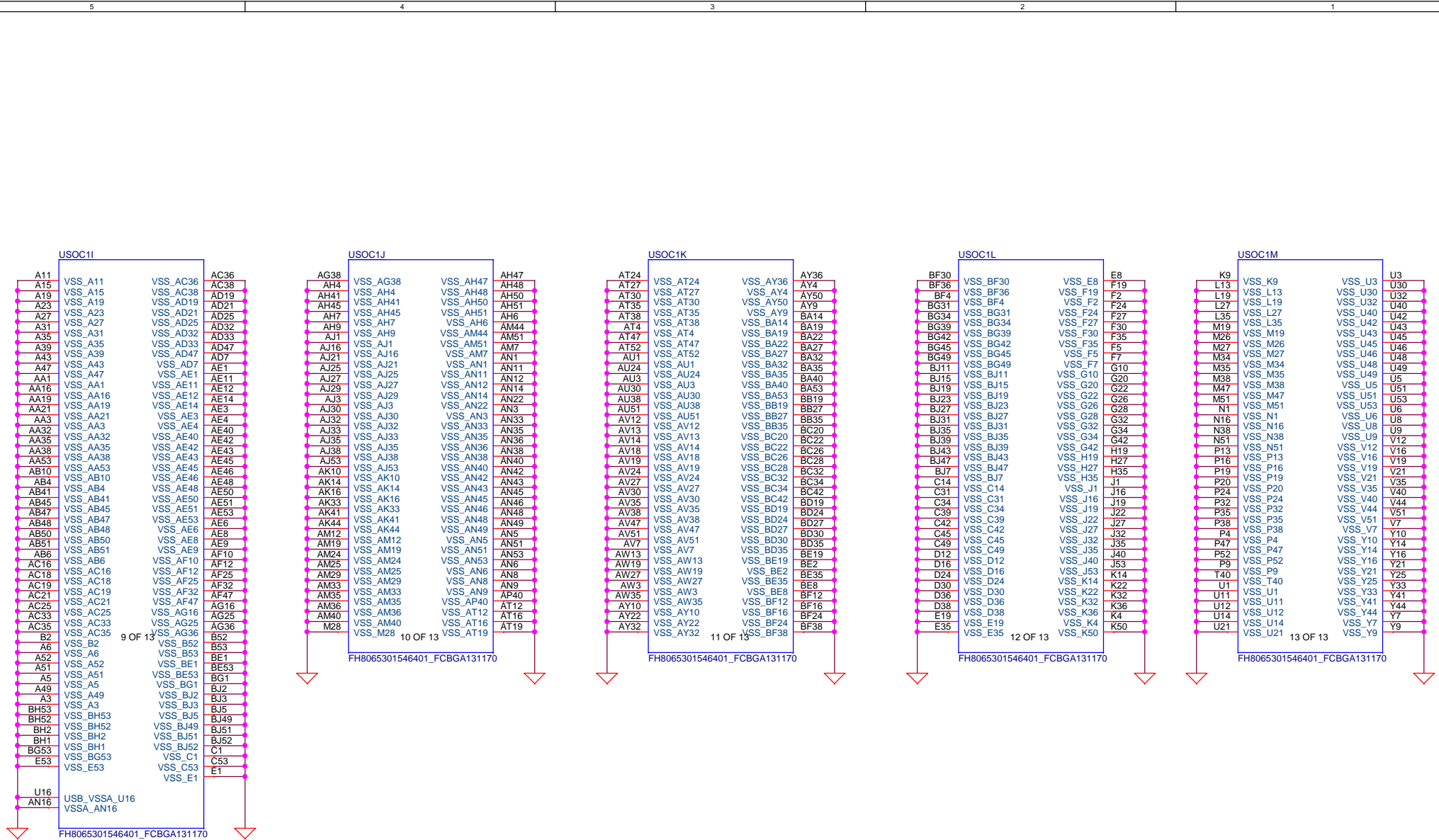


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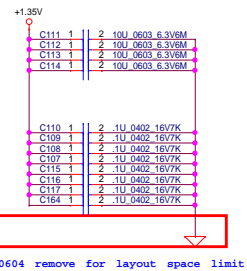


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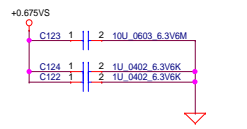
PVT 0827: Remove Debug Connector for ESD request.

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Layout Note:
Place near jDIMM1

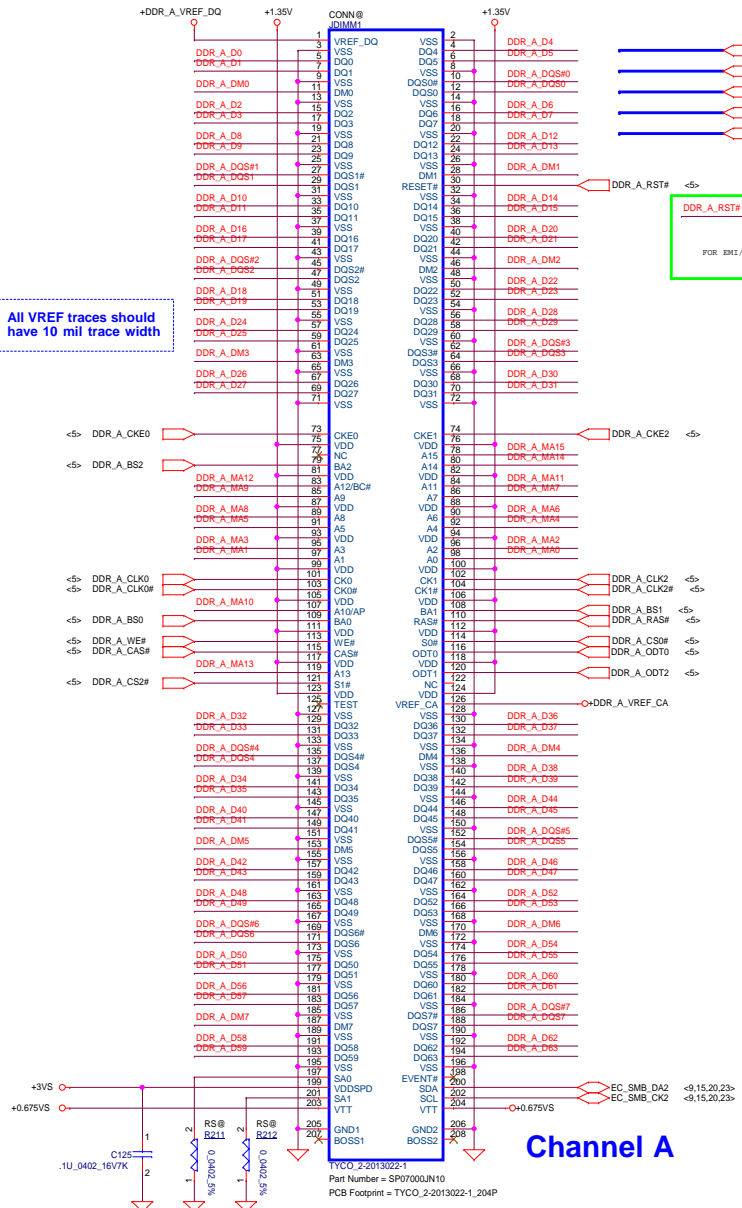


0604 remove for layout space limit



Layout Note:
Place near jDIMM1.203,204

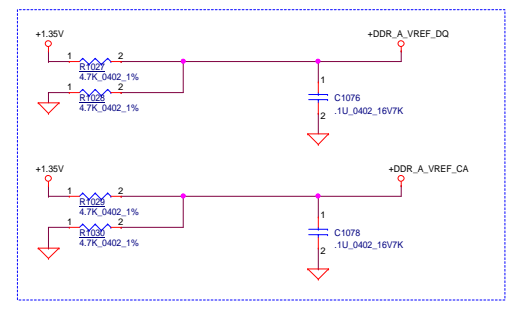
All VREF traces should have 10 mil trace width



Channel A

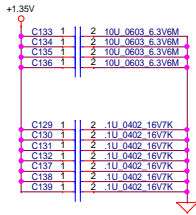
<Address: SA1:SA0=00 (A0H)>
DIMM_1 STD H:4mm

Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO DIMMS ON DIMM_VREF_CA // DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.



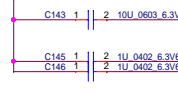
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Layout Note:
Place near JDIMM2

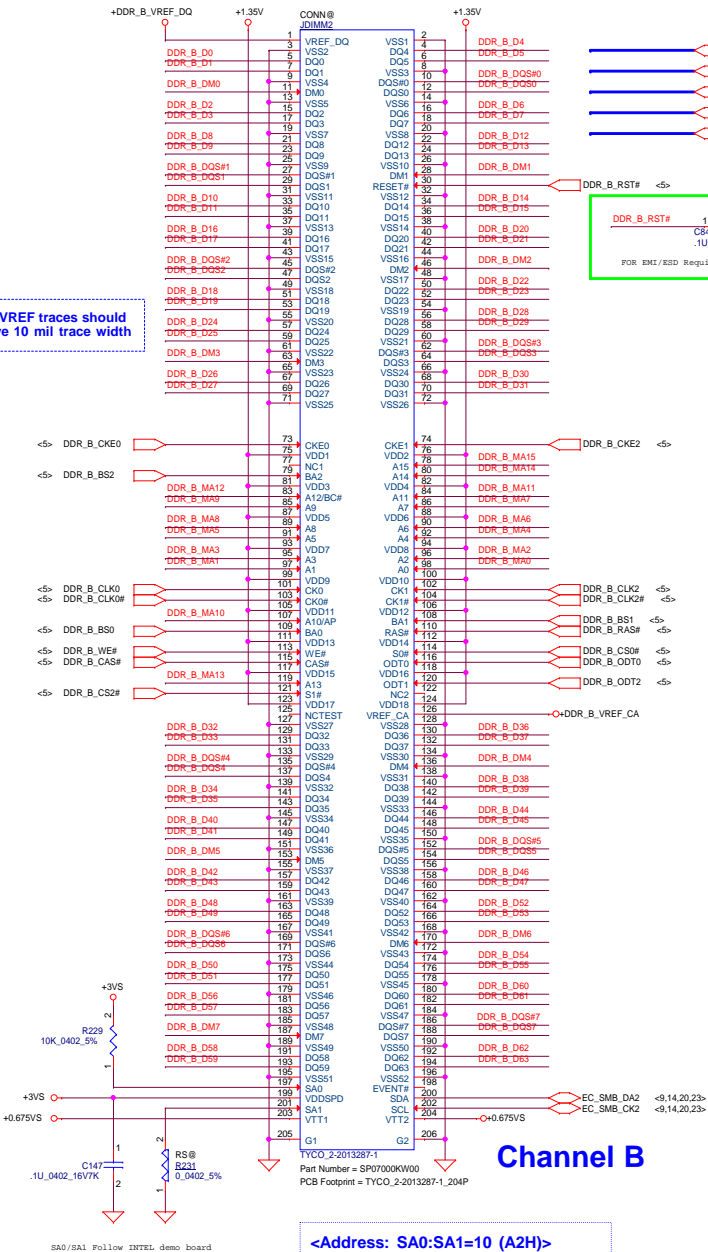


All VREF traces should have 10 mil trace width

+0.675VS

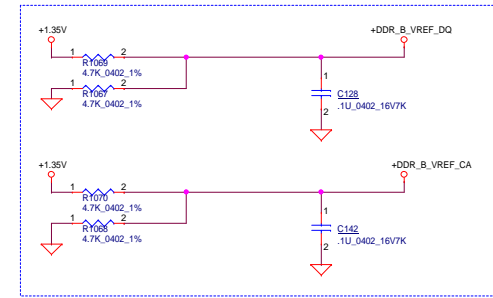


Layout Note:
Place near JDIMM2.203,204

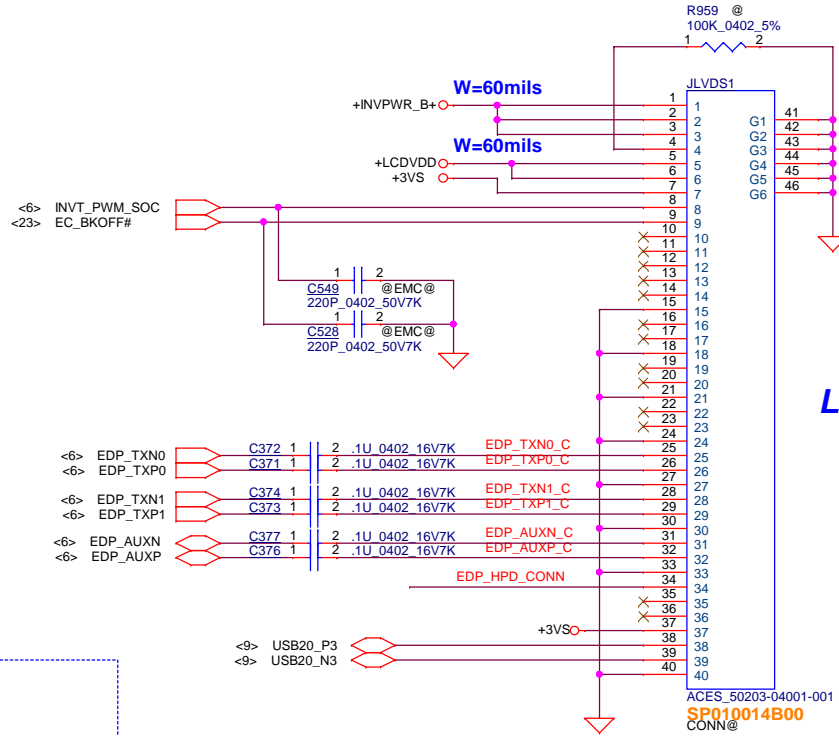
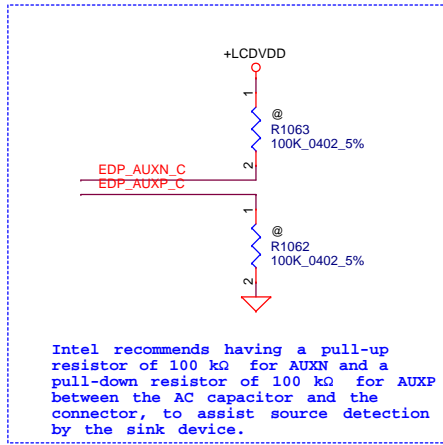
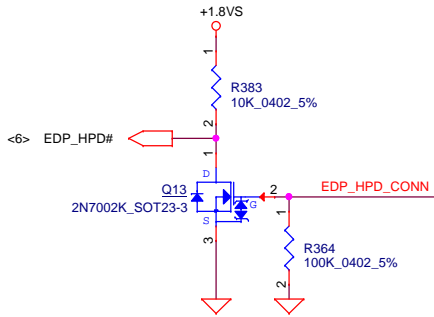
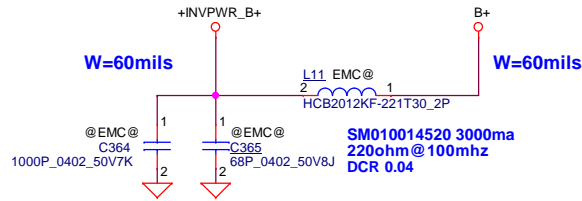
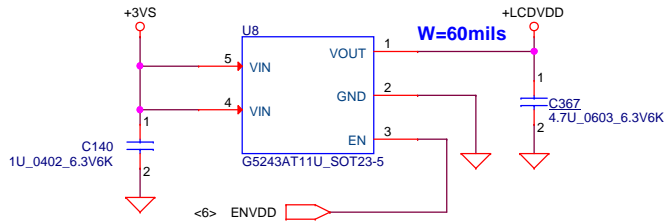


Channel B

<Address: SA0:SA1=10 (A2H)>
DIMM_2 REV H:4mm



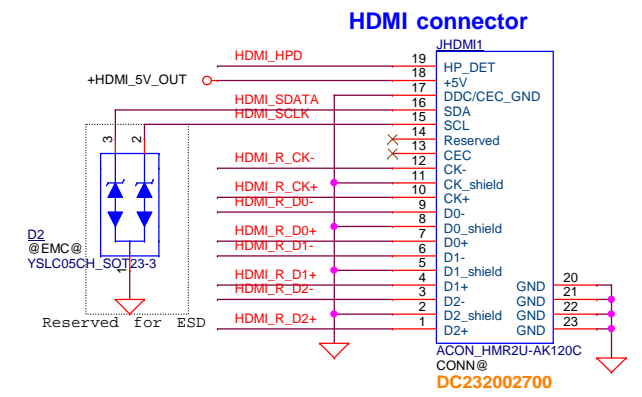
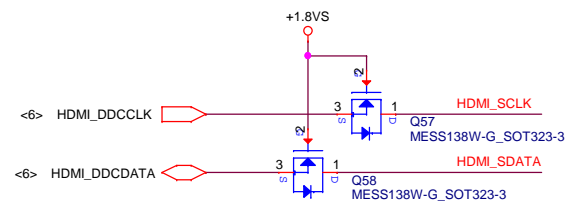
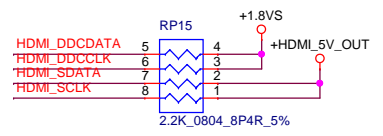
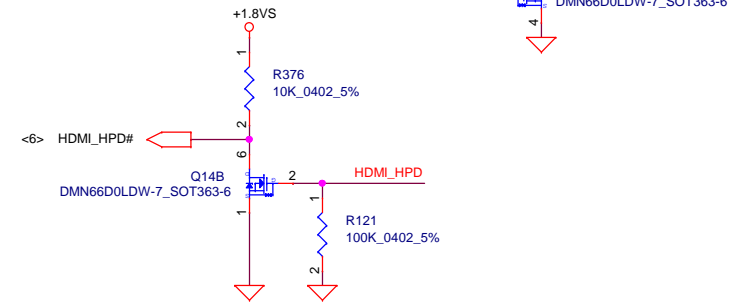
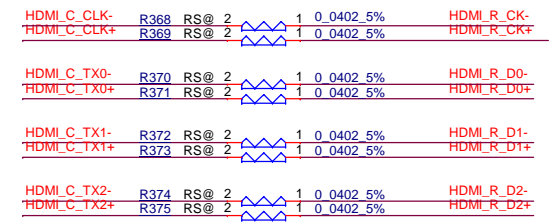
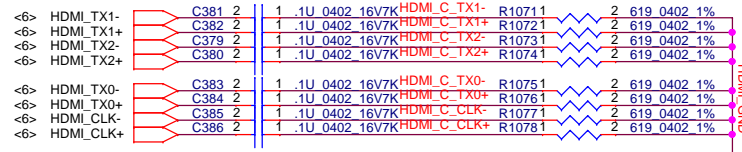
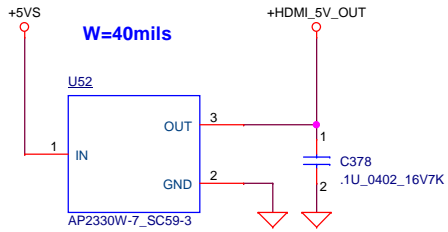
LCD POWER CIRCUIT



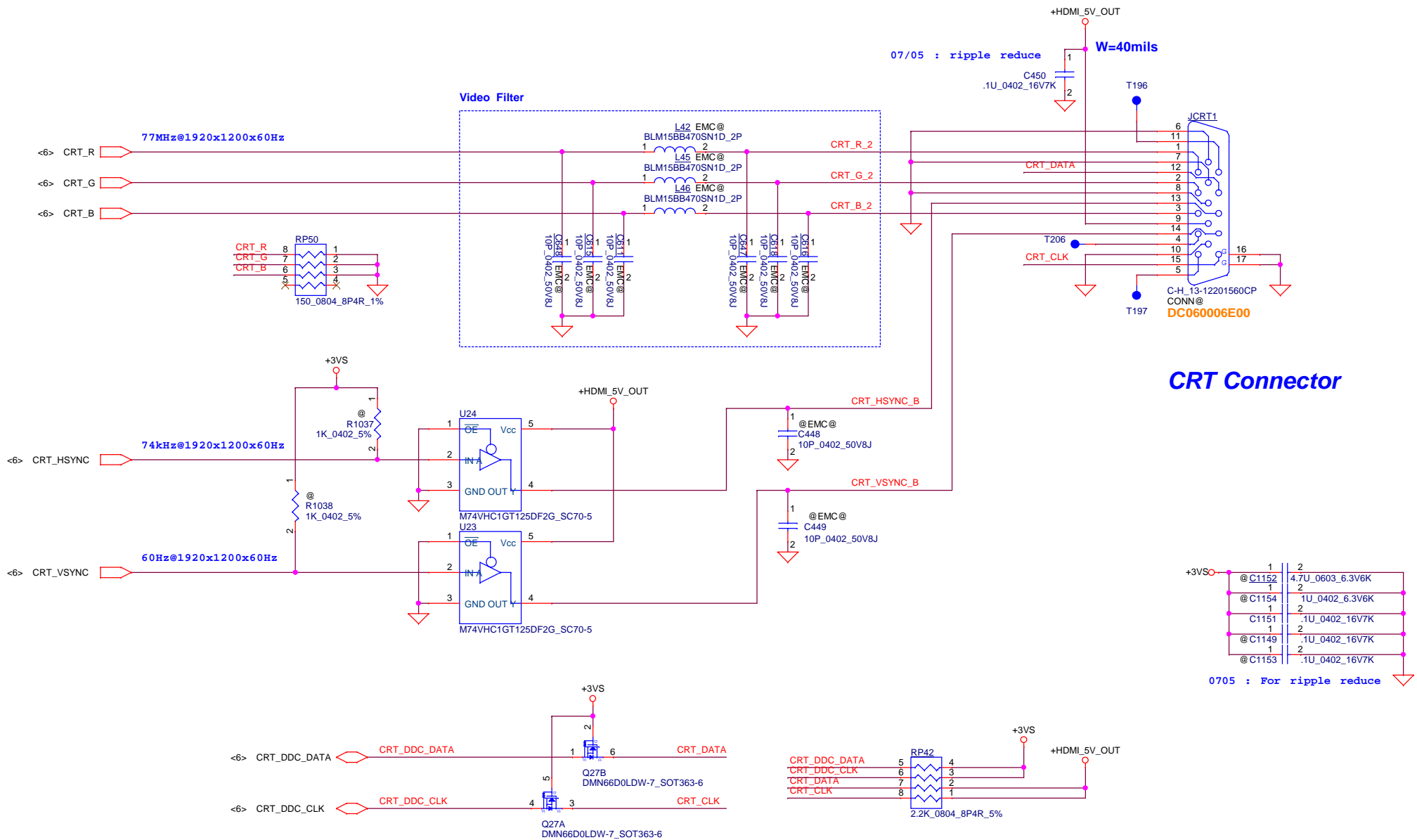
LCD/ LED PANEL Conn.

Touch Module

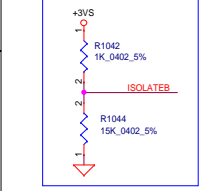
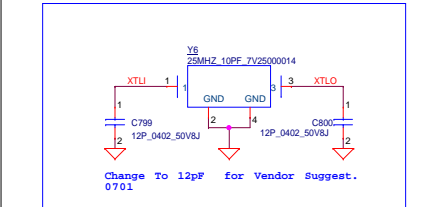
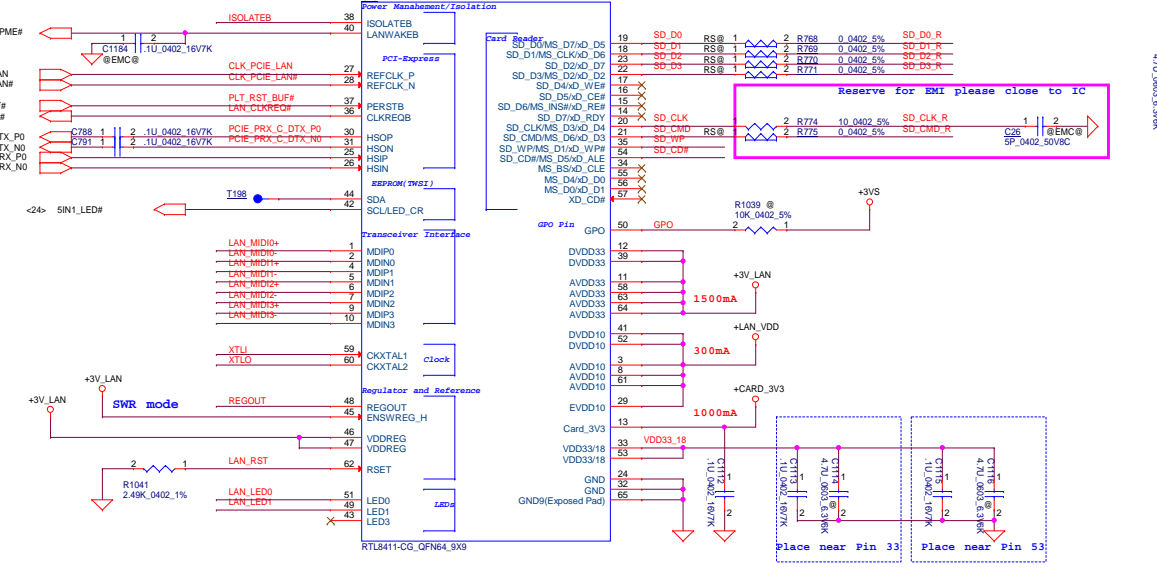
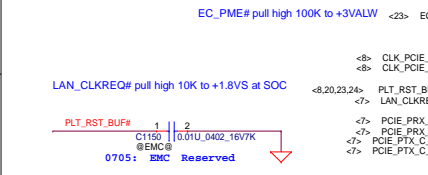
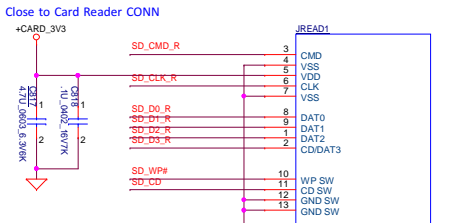
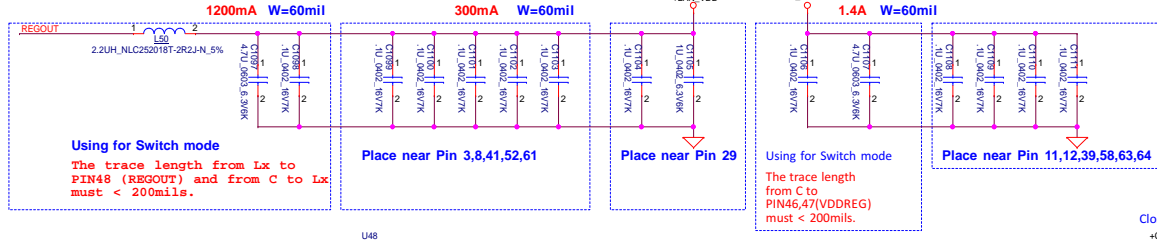
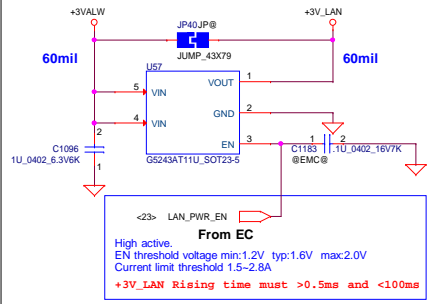
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	
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Size	Document Number	Intel BayTrail-M Platform		Rev	0.3
Date: Tuesday, September 03, 2013		Sheet 16 of 37			



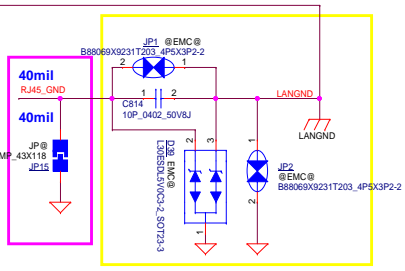
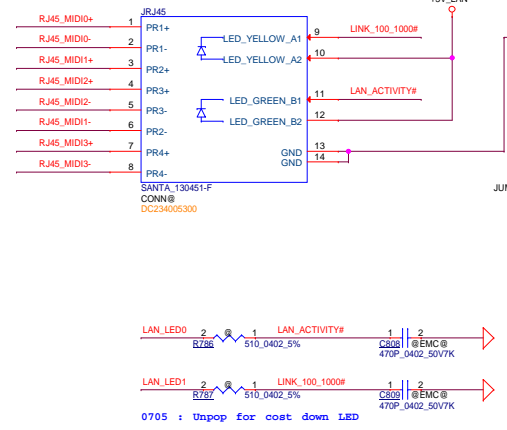
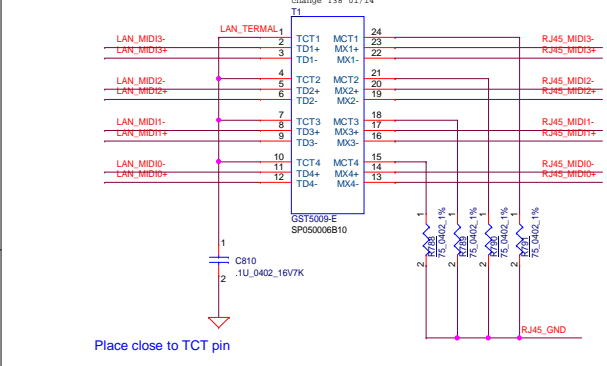
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	
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Size	Document Number			Rev	
B	Intel BayTrail-M Platform			0.3	
Date:	Tuesday, September 03, 2013	Sheet	17	of 37	



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Size	Document Number			Rev	
B	Intel BayTrail-M Platform			0.3	
Date:	Tuesday, September 03, 2013	Sheet	18	of 37	

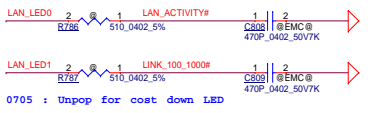


LAN Connector

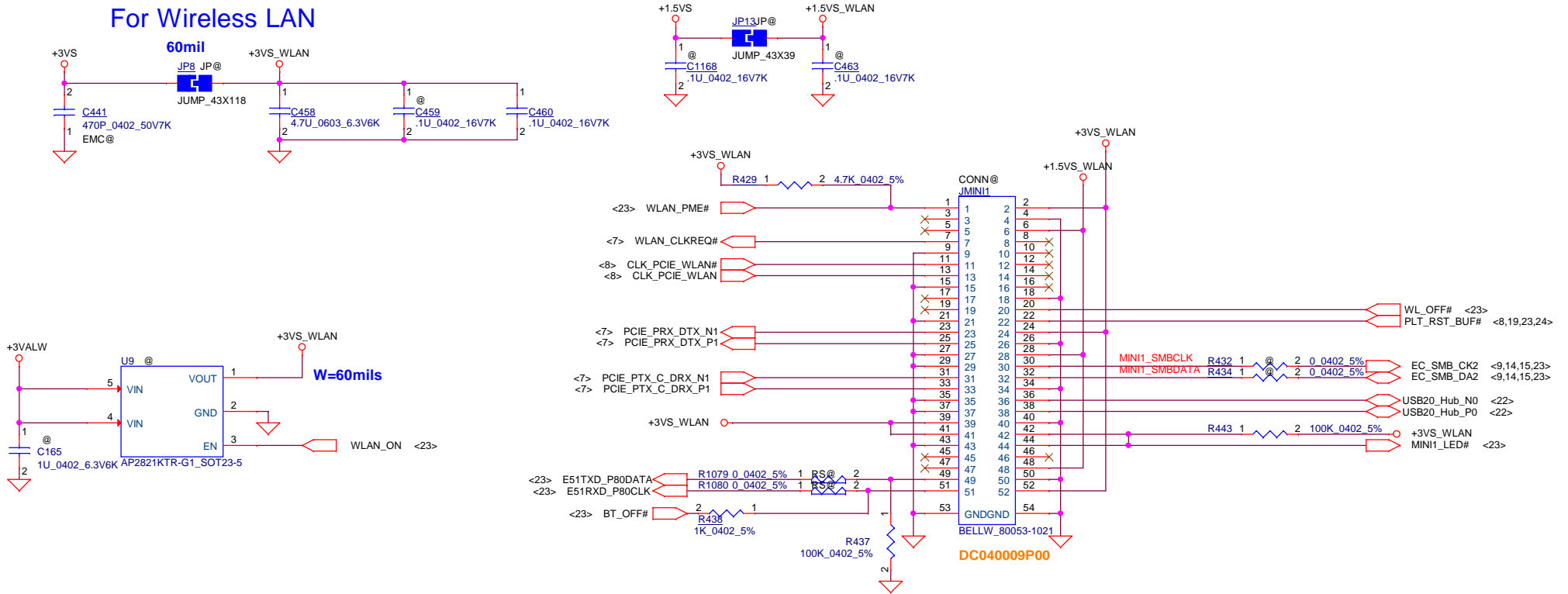


	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN

Place close to TCT pin

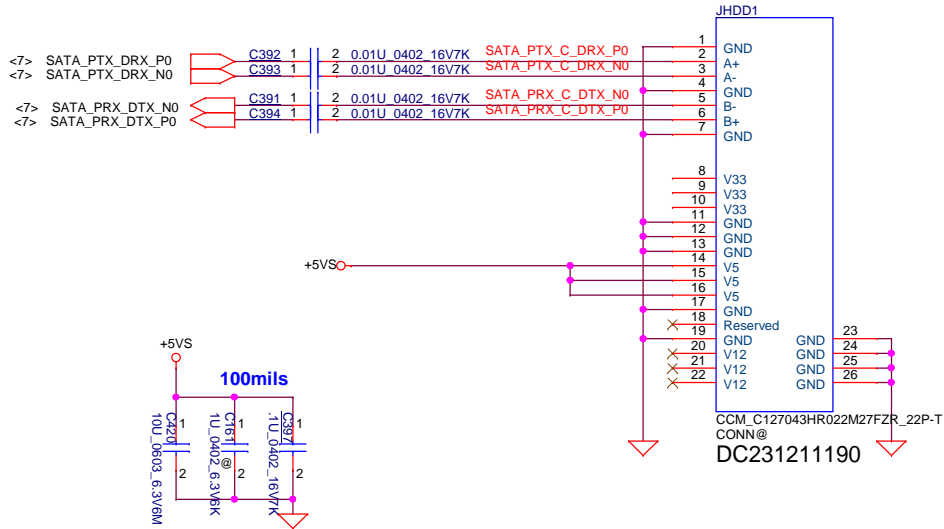


For Wireless LAN

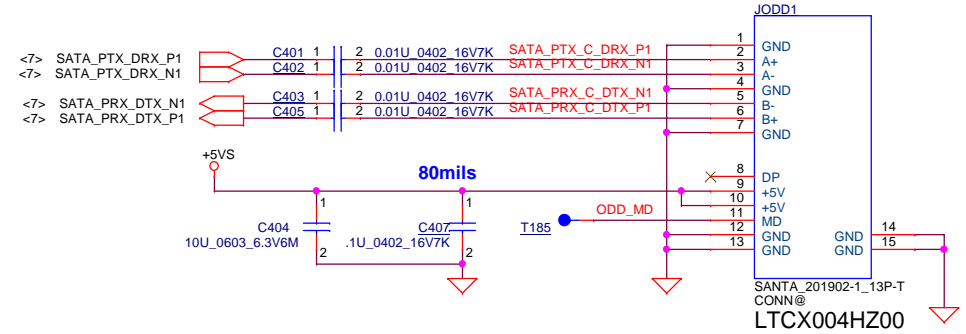


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				Size B	Document Number
Date:	Tuesday, September 03, 2013	Sheet	20	of	37

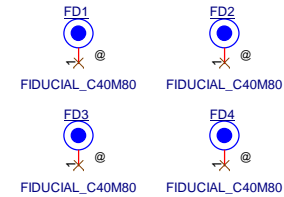
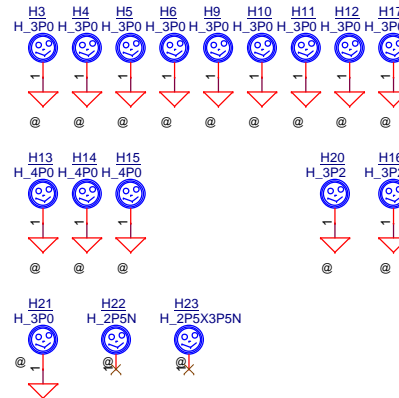
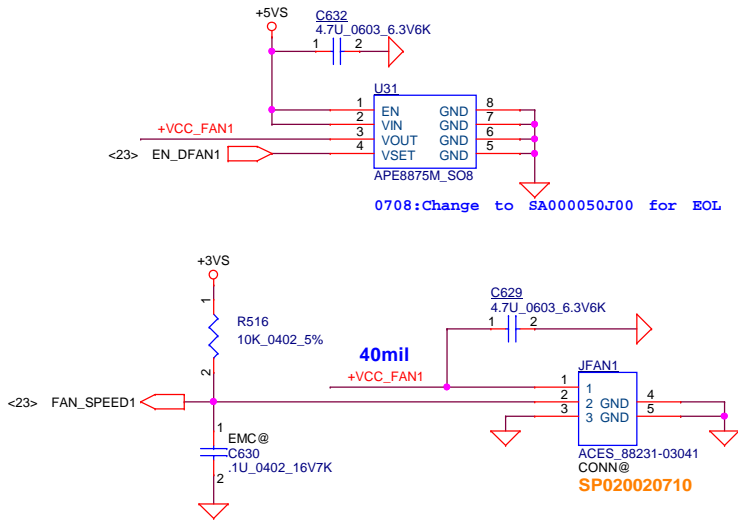
SATA HDD1 Conn.



SATA ODD Conn.

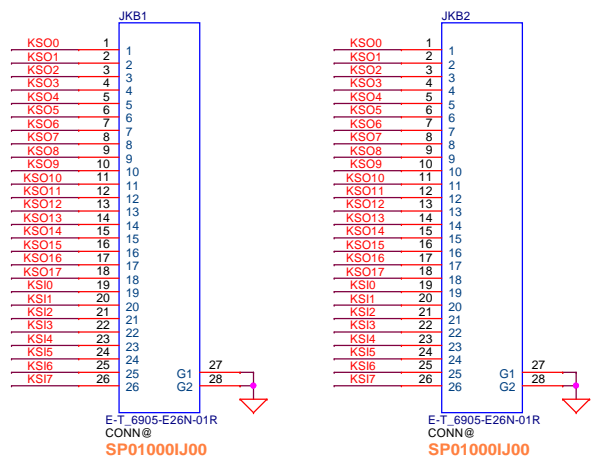


FAN1 Conn.



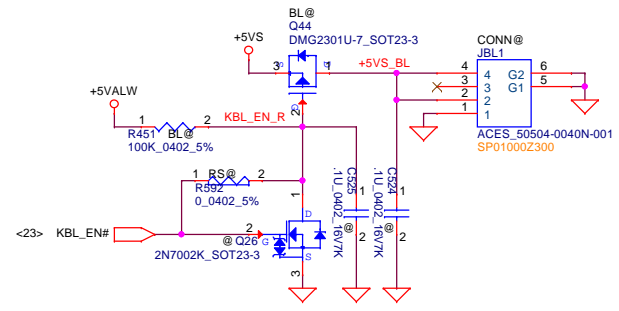
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	
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Size	Document Number	Rev		0.3	
Date: Tuesday, September 03, 2013		Sheet		21 of 37	
Intel BayTrail-M Platform					

KB Conn.

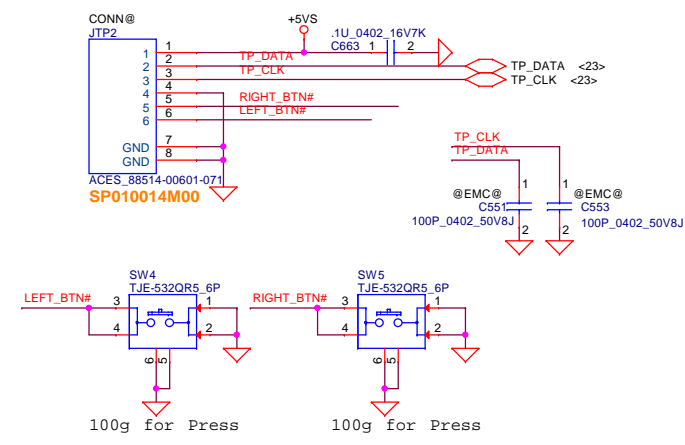


KSJ[0..7] <23>
KSOI[0..17] <23>

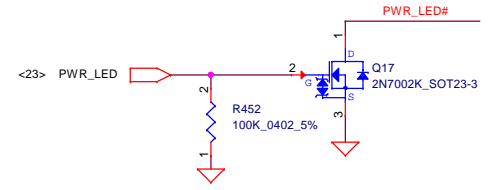
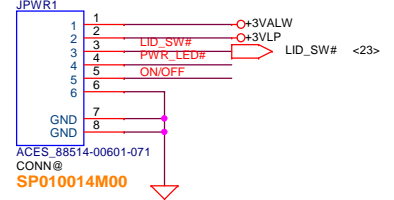
KB BackLight Conn.



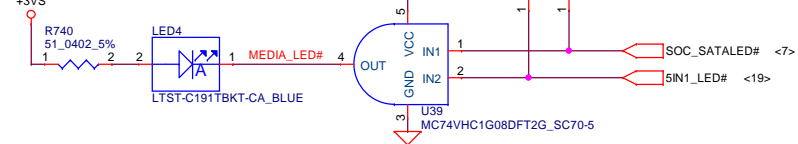
To TP/B Conn.



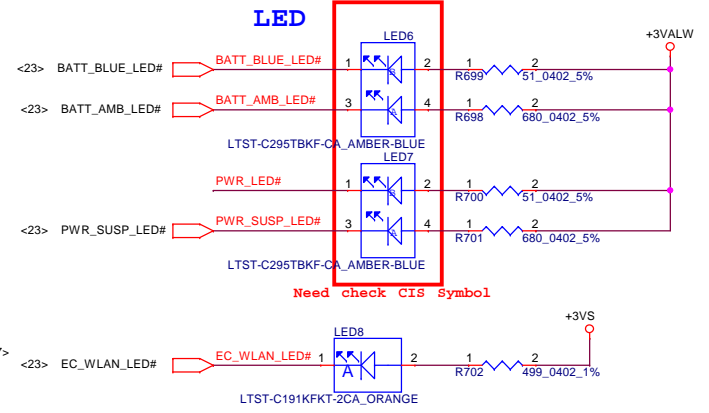
PWR/B



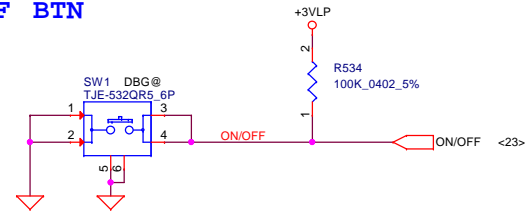
MEDIA LED



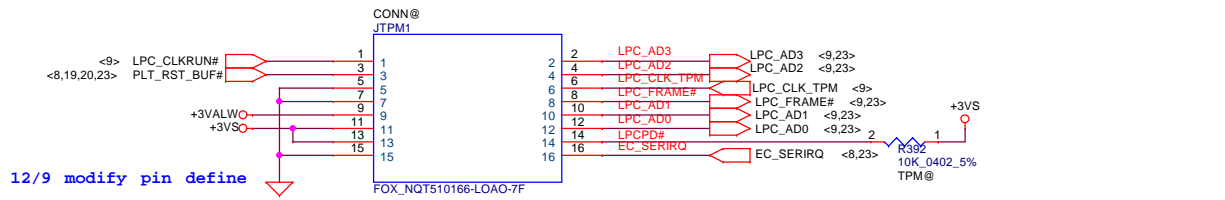
LED



ON/OFF BTN



TPM Board



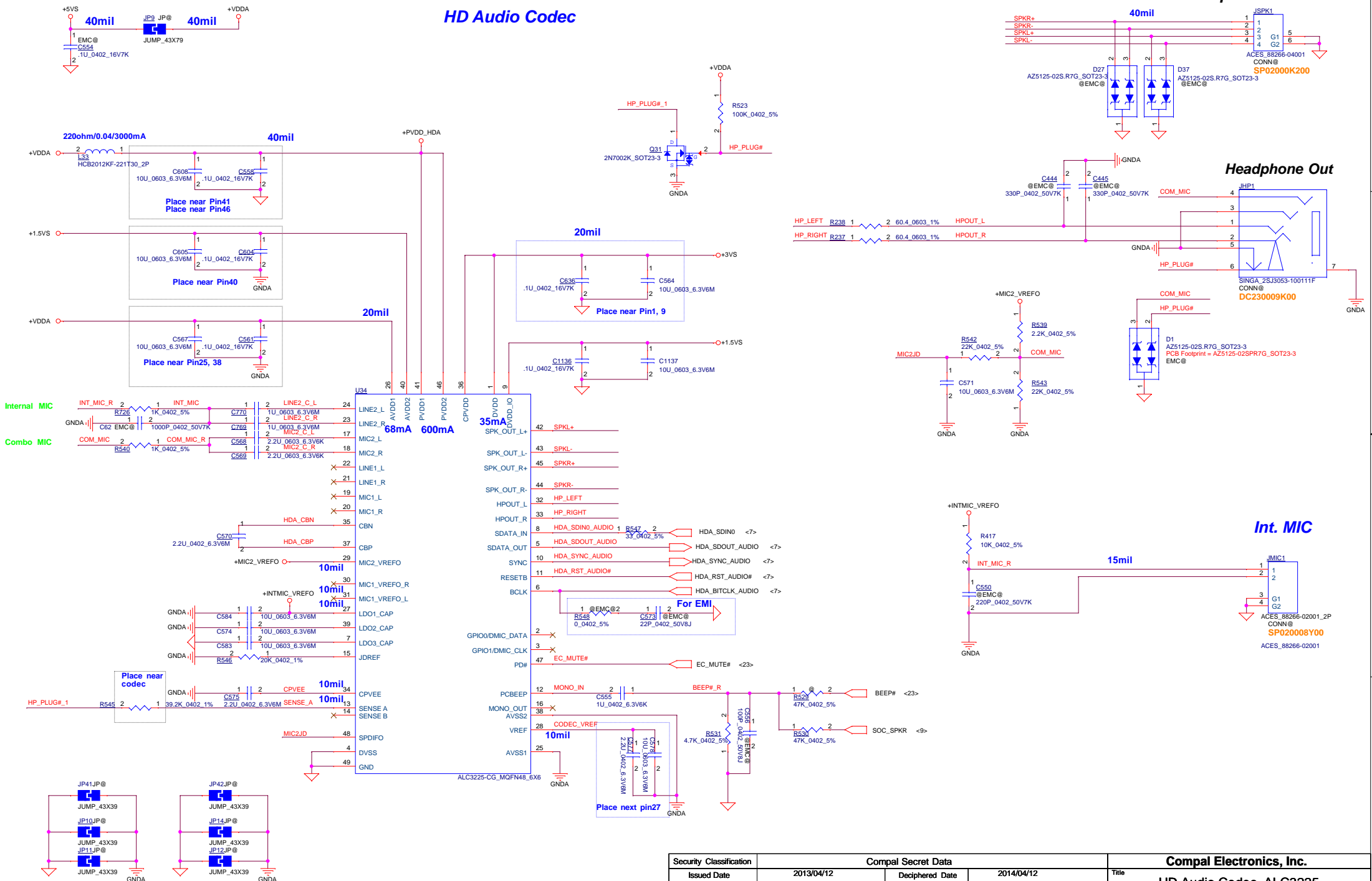
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	KB/TP/LED/TPM
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				Intel BayTrail-M Platform	
				Date:	Tuesday, September 03, 2013
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HD Audio Codec

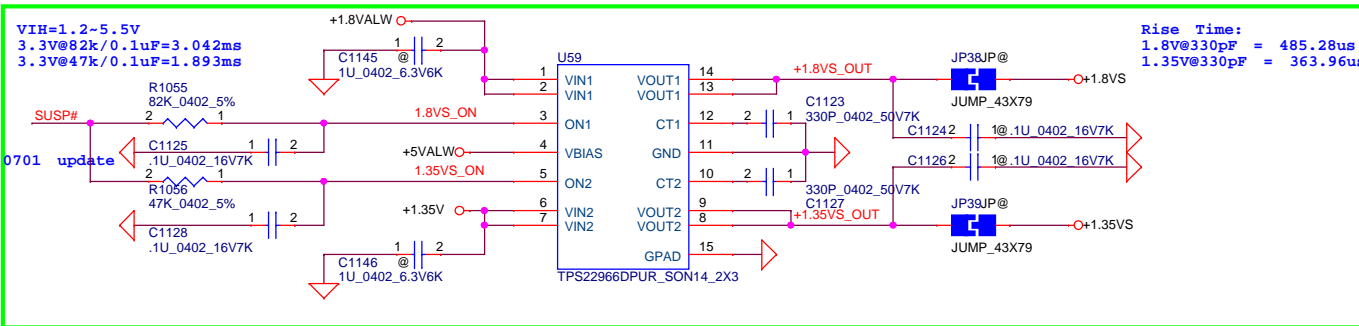
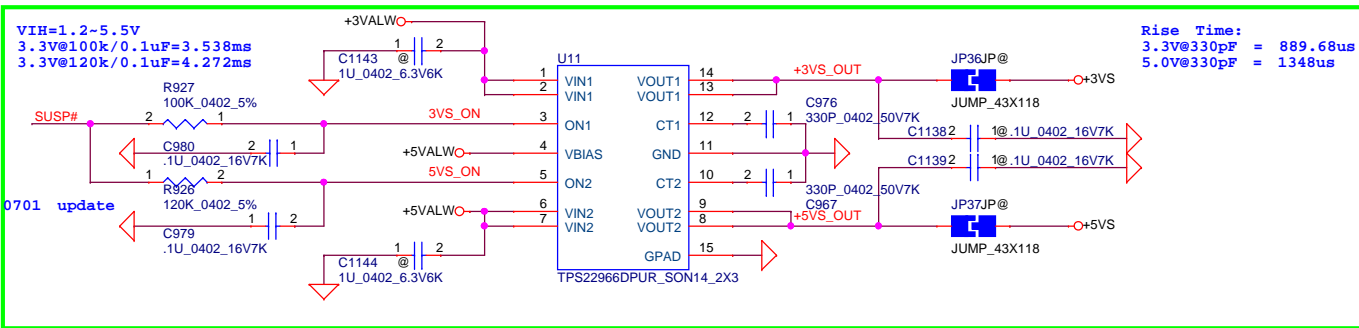
Int. Speaker Conn.

Headphone Out

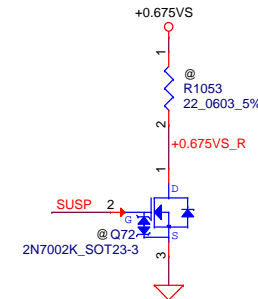
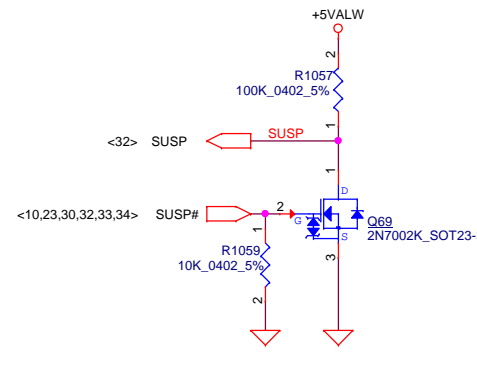
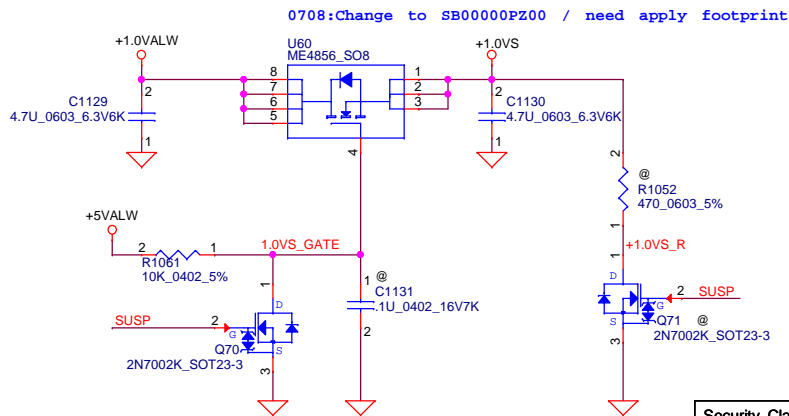
Int. MIC



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2013/04/12		2014/04/12		HD Audio Codec_ALC3225	
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				Customer Intel BayTrail-M Platform	
				Rev 0.3	
				Date: Tuesday, September 03, 2013	
				Sheet 25 of 37	



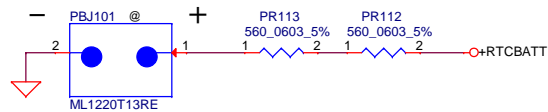
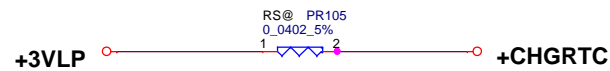
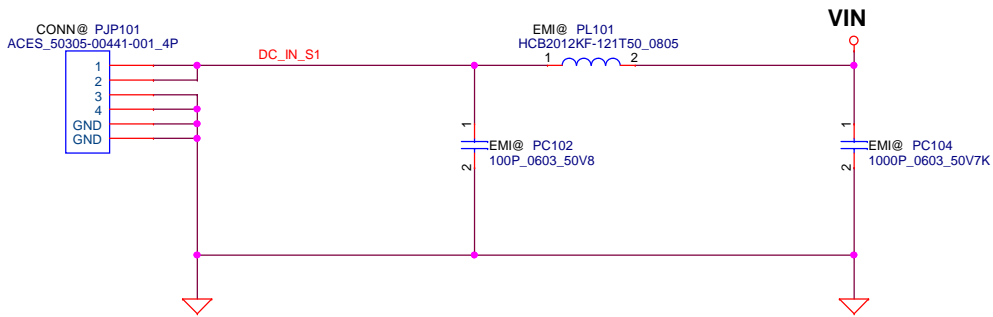
+1.0VALW TO +1.0VS



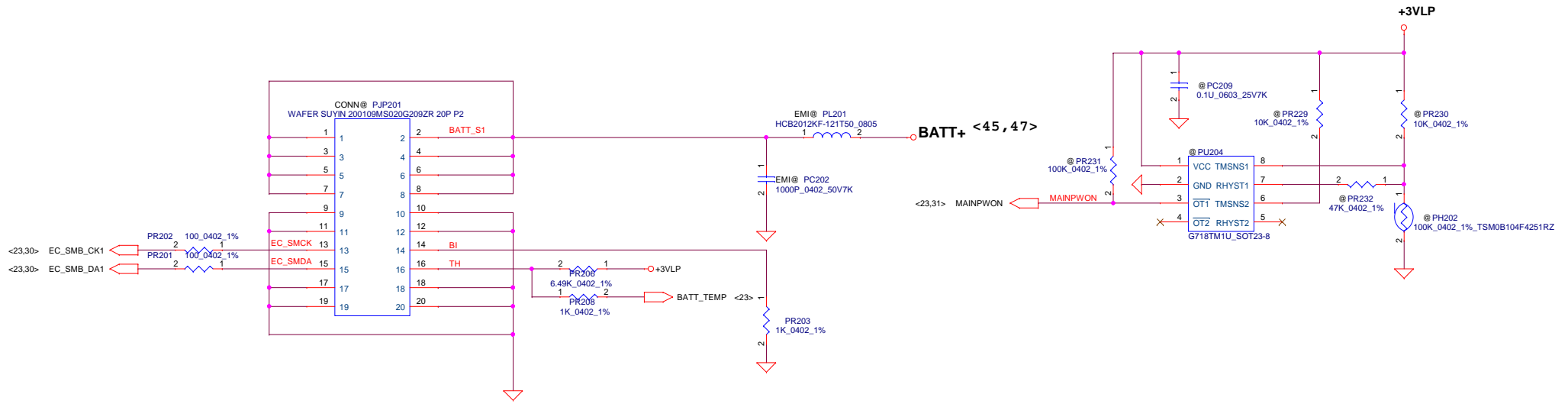
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Size	Document Number			Rev	
B	Intel BayTrail-M Platform			0.3	
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1. Change U8,U57 (SA000028Y10) to SA00006EE00 (S IC AP2821KTR-G1 SOT-23 5P PWR SW)
2. Change U28 to SA00004OB30(S IC KB9012QF A4 LQFP 128P KB CONTROLLER)
3. Change U31 to SA000050J00 (S IC APE8875M SO 8P FAN CONTROL)
4. Change Q57,Q58,Q62,Q63,Q64,Q65 to SB00000S700(S TR MESS138W-G 1N SOT323-3)
5. Change D40 to SCS00003500 (S SCH DIO RB751V-40 SOD-323 YEASHIN)
6. Unpop R1025 for +1.8VS leakage
7. Pop R1061 for +1.0VS leakage
8. Change RP53 to R1081,R1082 and change SD_CD PU to +3VS for Card Reader un-plug issue
9. Change R927 to 100k for +3VS power sequence
10. Change R926 to 120k for +5VS power sequence
11. Change R1055 to 82k for +1.8VS power sequence
12. Change R1056 to 47k for +1.35VS power sequence
13. Unpop R786,R787 for cost down RJ45 Conn.
14. Pop C449,C450 for CRT_VSYNC_B reduce noise
15. Change C1003,C1004 to 10P for System 25MHz Crystal fine tune
16. Change C799,C800 to 12P for LAN 25MHz Crystal fine tune
17. Change C1009,C1010 to 15P for System 32.768kHz Crystal fine tune
18. Change C1006 from 0.01U to 0.1U for ESD request
19. ADD C1151,C1152 for CRT flicker
20. Change L31,L32,L49 to 0402 Size
21. Add C1169 0.1uF for ESD request
22. Pop C1007 0.047uF for ESD request
23. 0708:Changg U60 to ME4856_SO8(SB00000PZ00)
24. Unpop L49 and Add U65,R1084,R1085,R1087,C1179,C1181 for +1.35VS LDO for CRT
25. Unpop Q71,Q72,R1052,R1053 for power discharge
26. Add C1155,C1156,C1157,C1158,C1159 for ESD request
26. Add C1160~C1167,C1167~C1173 for Debug Port for ESD

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				Size B	Document Number
Date:	Tuesday, September 03, 2013	Sheet	27 of 37		



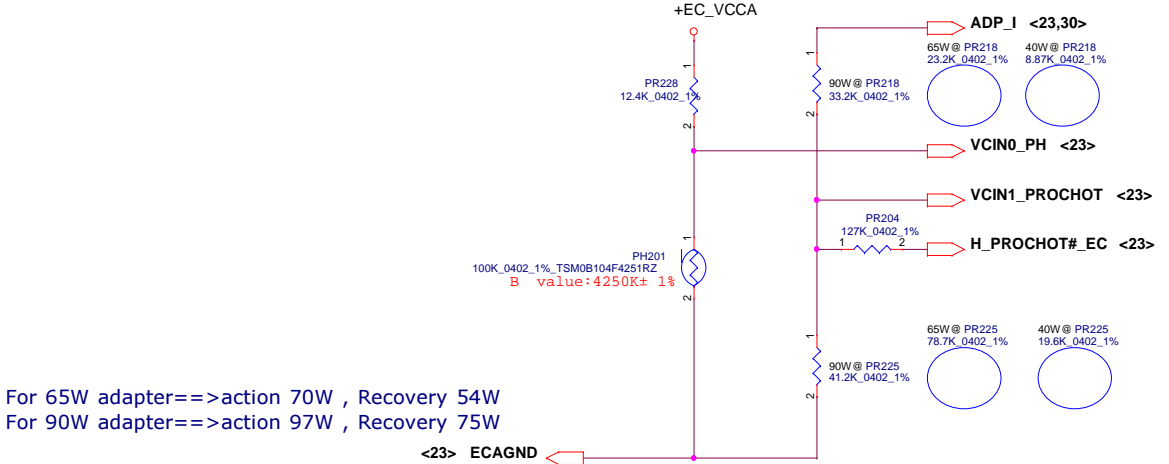
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	
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Size	Document Number			Rev
B	Bay Trail M LA-A621P			0.3
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For KB9012 OTP	
92 °C	1.2V, Active
56 °C	2.255V, Recovery

For KB9012 sense 20mΩ	Active	Recovery
40W	50W, 0.7V	40W, 0.7V
65W	84W, 1.2V	56W, 1.2V
90W	117W, 1.2V	77W, 1.2V

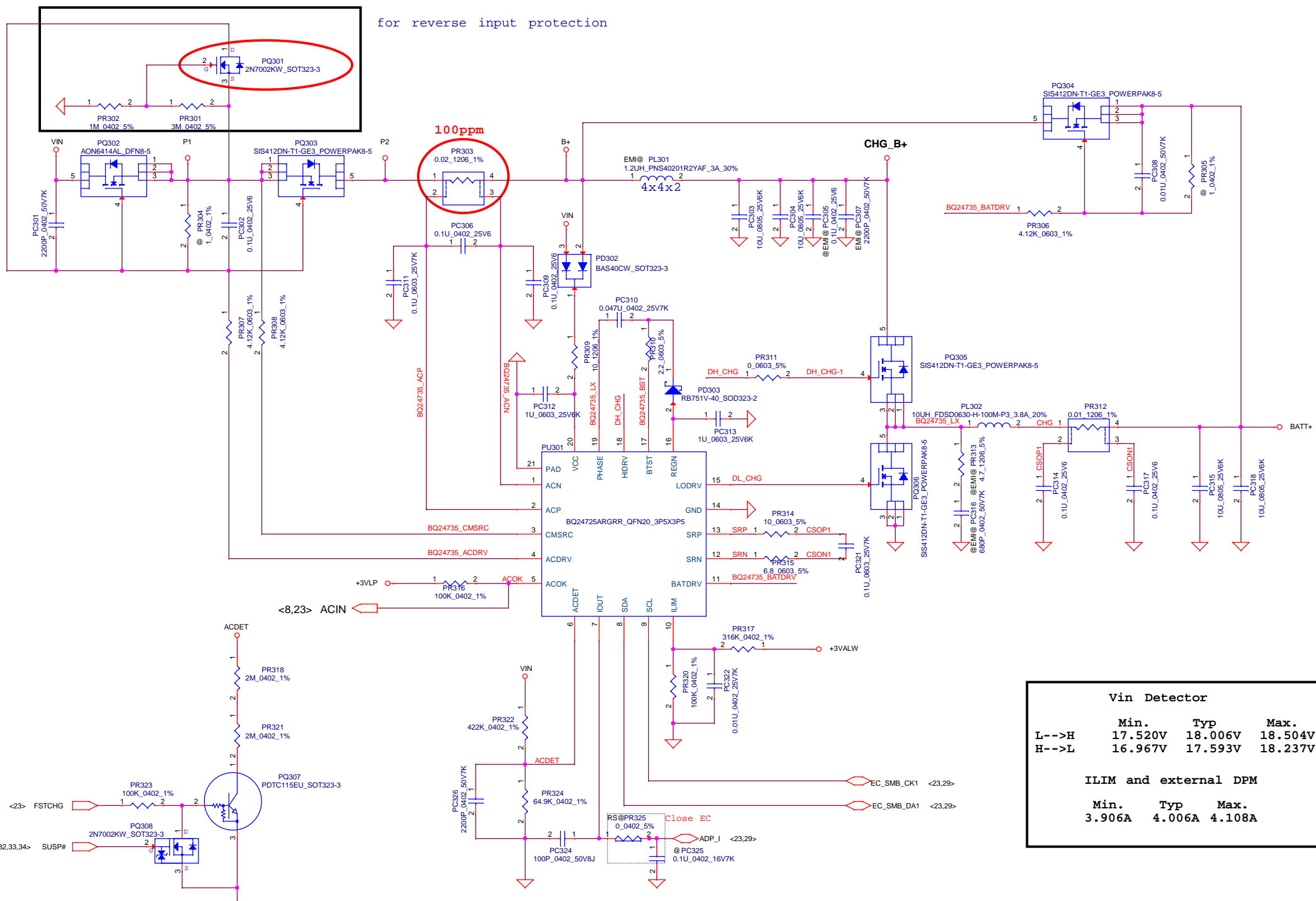
PH201 under CPU bottom side :
 CPU thermal protection at 92 degree C (shutdown)
 Recovery at 56 degree C



For 65W adapter==>action 70W , Recovery 54W
 For 90W adapter==>action 97W , Recovery 75W

Security Classification			Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title				
				BATTERY CONN / OTP				
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				Custom	Bay Trail M LA-A621P	0.3		
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for reverse input protection



Vin Detector			
	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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				CHARGER	
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```

+1.35VP
Ipeak = max{ 0.7*Ibudget, 1st +2nd max loading}
Ipeak = max{ 12.34*0.7 , 4.2+8.14 }
Ipeak=12.34A ; 1.2Ipeak=14.808A ;Imax=8.638A
1/2Delta I=0.7353A (F=300K Hz)
PR504=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2/9uA=8.45Kohm
choose PR504=8.45Kohm (for safety >1.2Ipeak)
Rds(on)=5.0m ohm(max) ; Rds(on)=4.2m ohm(typical)
Ilimit_min=(8.366K*9uA)/(5.0m*1.2)=15.058A
Ilimit_max=(8.535K*11uA)/(4.2m*1.2)=22.352A
Iocp=Ilimit+1/2Delta I=15.79A-23.09A
Iocp(min)>1.2Ipeak
    
```

2011/9/19

OVP=110% 115% 120%

+0.675VSP

+VTT_REFP

+1.35VP

+1.35VP

+5VALW

+1.35VP

+1.35VP

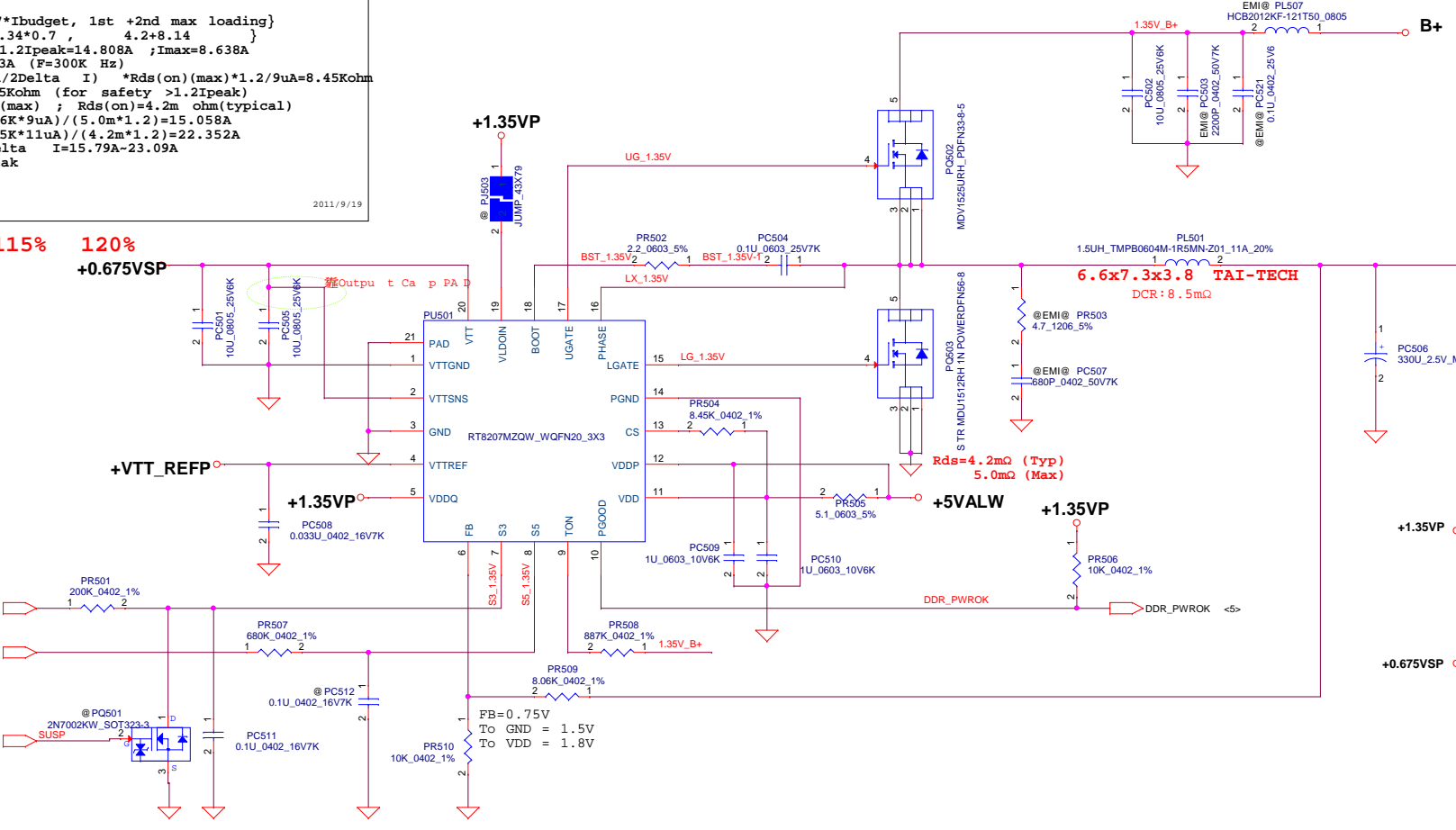
+1.35VP

+1.35VP

+0.675VSP

+0.675VSP

- <26,30,33,34> SUSP#
- <23> SYSON
- <26> SUSP

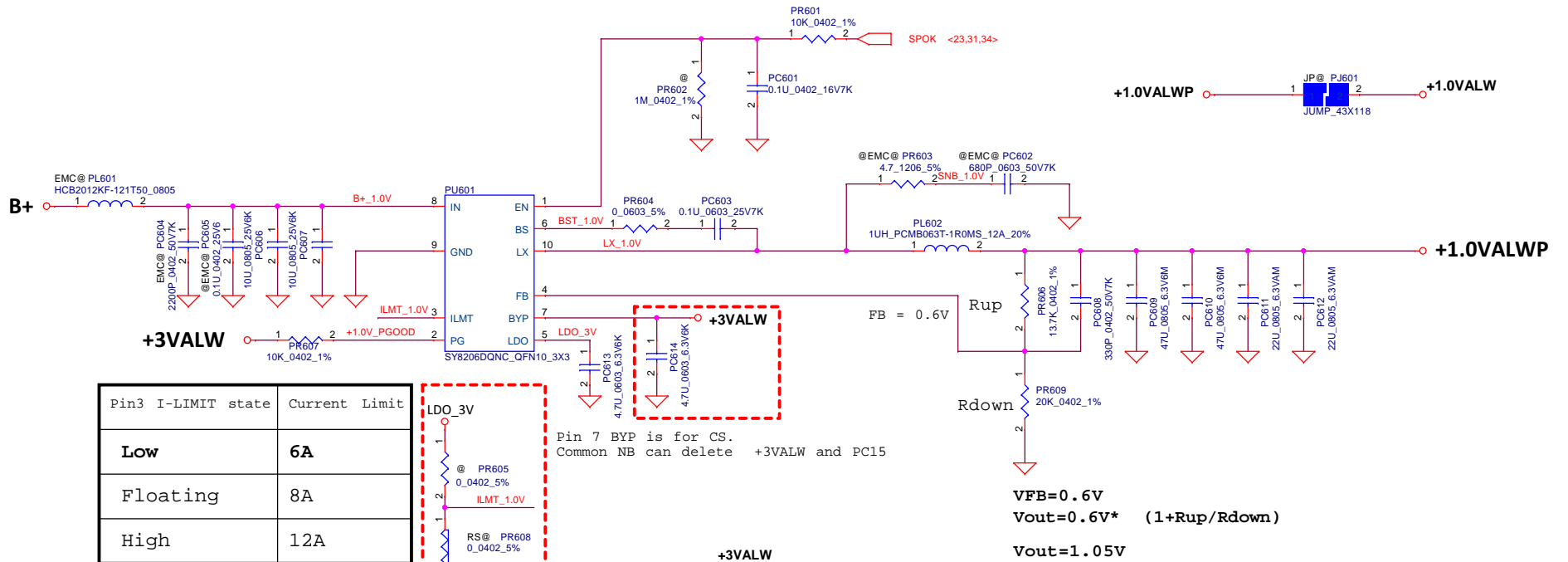


STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

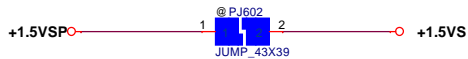
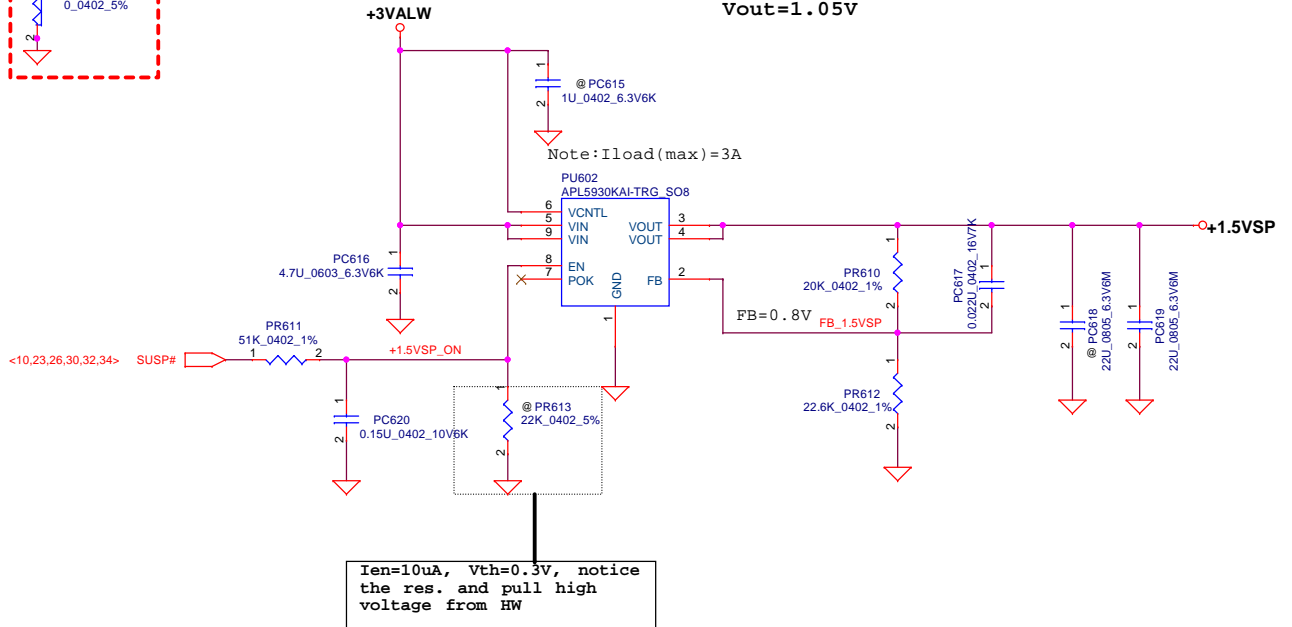
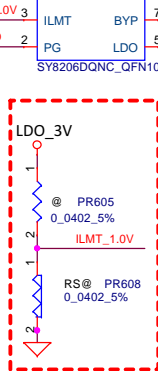
Note: S3 - sleep ; S5 - power off

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				1.35VP/0.675VSP	
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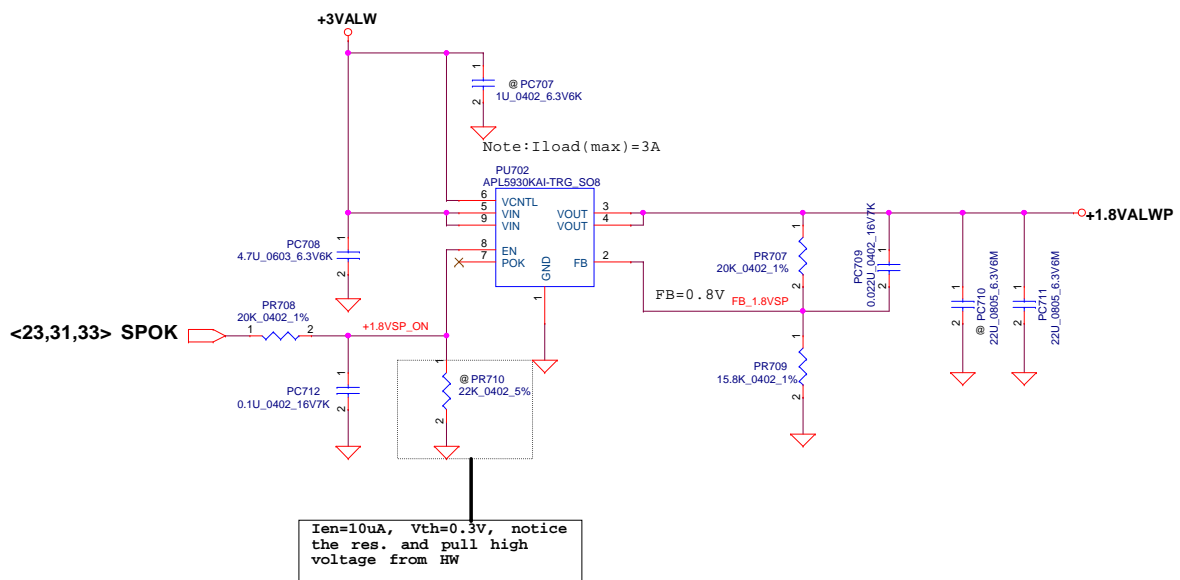
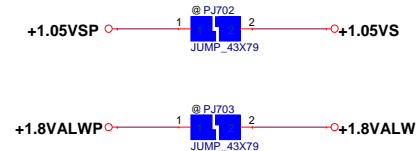
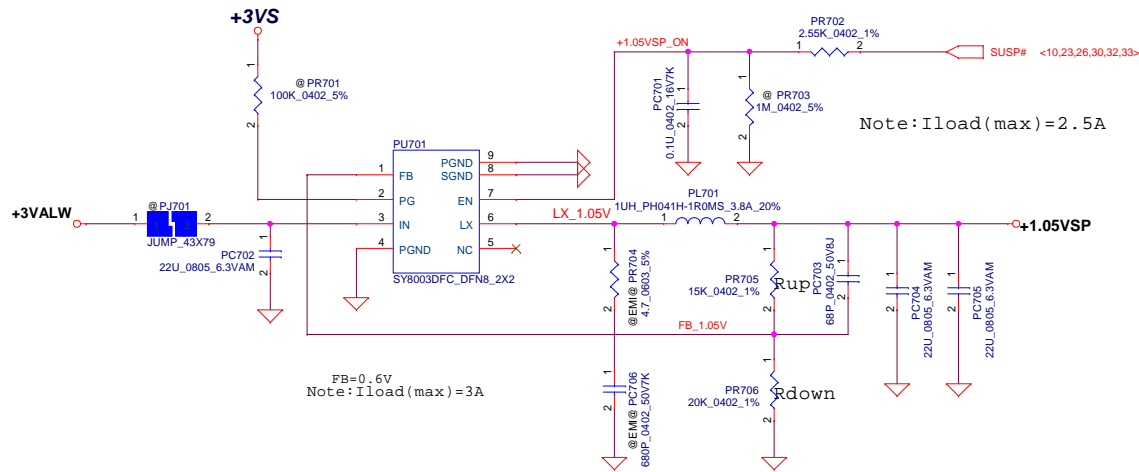
Note: Use U3C931 SPI to switch High & Low Level for VDD11



Pin3 I-LIMIT state	Current Limit
Low	6A
Floating	8A
High	12A



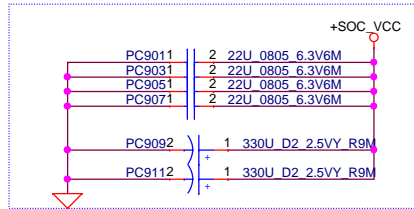
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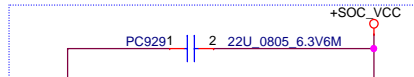
Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

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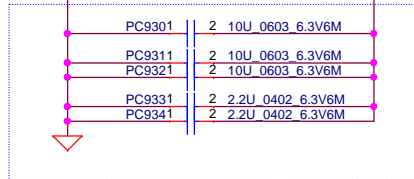
Output Cap



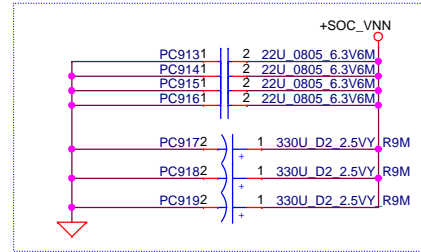
Package Edge Cap



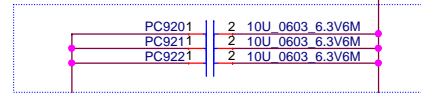
Back Side Cap



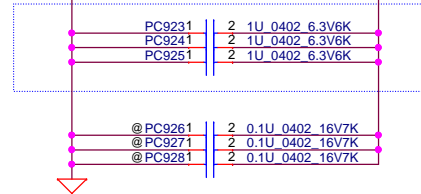
Output Cap



Package Edge Cap



Back Side Cap



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Tune Power sequence by HW request	1.05VS & 1.5VS sequence meet SPEC			Change PR702 to 2.5K, PR611 to 51K, PC620 to 150nF	07/05	DVT
2		Change 1.35V voltage close to 1.35		32	Change PR509 to 7.68K	07/05	DVT
3	EMI request	Cut-in EMI solution		30	Change PR310 to 2.2	07/05	DVT
4		Approve CPU transient		CPU	Change PC931, PC932 from 4.7uF to 10uF Change PR839 from 240 to 232 Add PR808 to 20.5K Change PC812 from 330pF to 1000pF Change PC828 from 470pF to 680pF	07/24	DVT
5							
6					Add PR411, PR413	12/22	DVT2
7	+1.05V ripple close upper and mean too low	Adjust output voltage and add Cff			Add PC609 into 4700P Change PR608 from 133K to 127K	12/22	DVT2
8		Improve CPU transient character		40	Unpop PC926	01/09	DVT2
9		Tune sequence		35	Change PC428 from 4700p to 10n, PC427 from 0.047u to 6.8n	02/04	PVT
10		0 ohm reduce			Change PR507, PR513, PR523 to R-pad	02/22	PVT
11		Provide 3/5V PG signal to EC		35	Add PR416	02/22	PVT
12	ESD request			32	Add PC101 into 0.1uF	02/26	PVT
13	ESD request			36	Add PC521, PR503, PC507	02/26	PVT
14		Use HW to control VCIN1 function		33	Add PR204	03/05	PVT
15							
16							
17							

Delete 08/14

12
13
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16
17

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