

# COMPAL CONFIDENTIAL

MODEL NAME : Goliad MLK 12 UMA ENTRY

PCB NO : LA-A972P

BOM P/N : 4319RK31LXX

GPIO MAP: 3.3b

## Goliad MLK 12" UMA ENTRY

Broadwell U Processor

2013-12-23

REV : 0.2 (X01)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

VPRO@ : Vpro Component


NVPRO@ : Non-Vpro Component



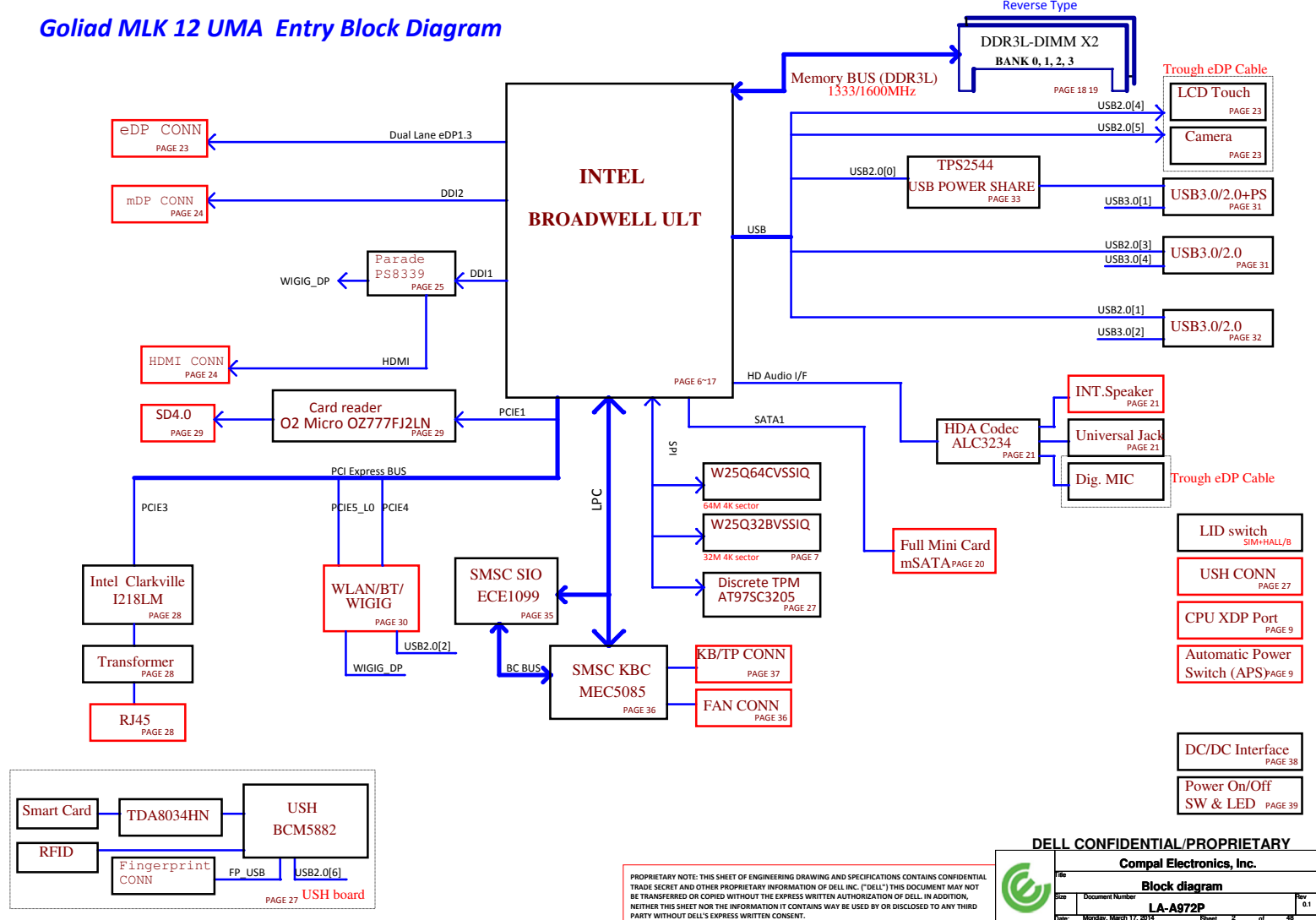
MB PCB	
Part Number	Description
D480002800	PCB 14A LA-A972P REV0 MB W/O DOCKING 2

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Title		<b>Cover Sheet</b>	
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# Goliad MLK 12 UMA Entry Block Diagram



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**Block diagram**

File: \_\_\_\_\_

Doc: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: 0.1

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**POWER STATES**

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

**PM TABLE**

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	NA
		SATA 2	NA
		SATA 1	JMINI3
		SATA 0	NA

BDW ULT	USB PORT#	DESTINATION
	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
7	WWAN	

USH	0	BIO
	1	NA

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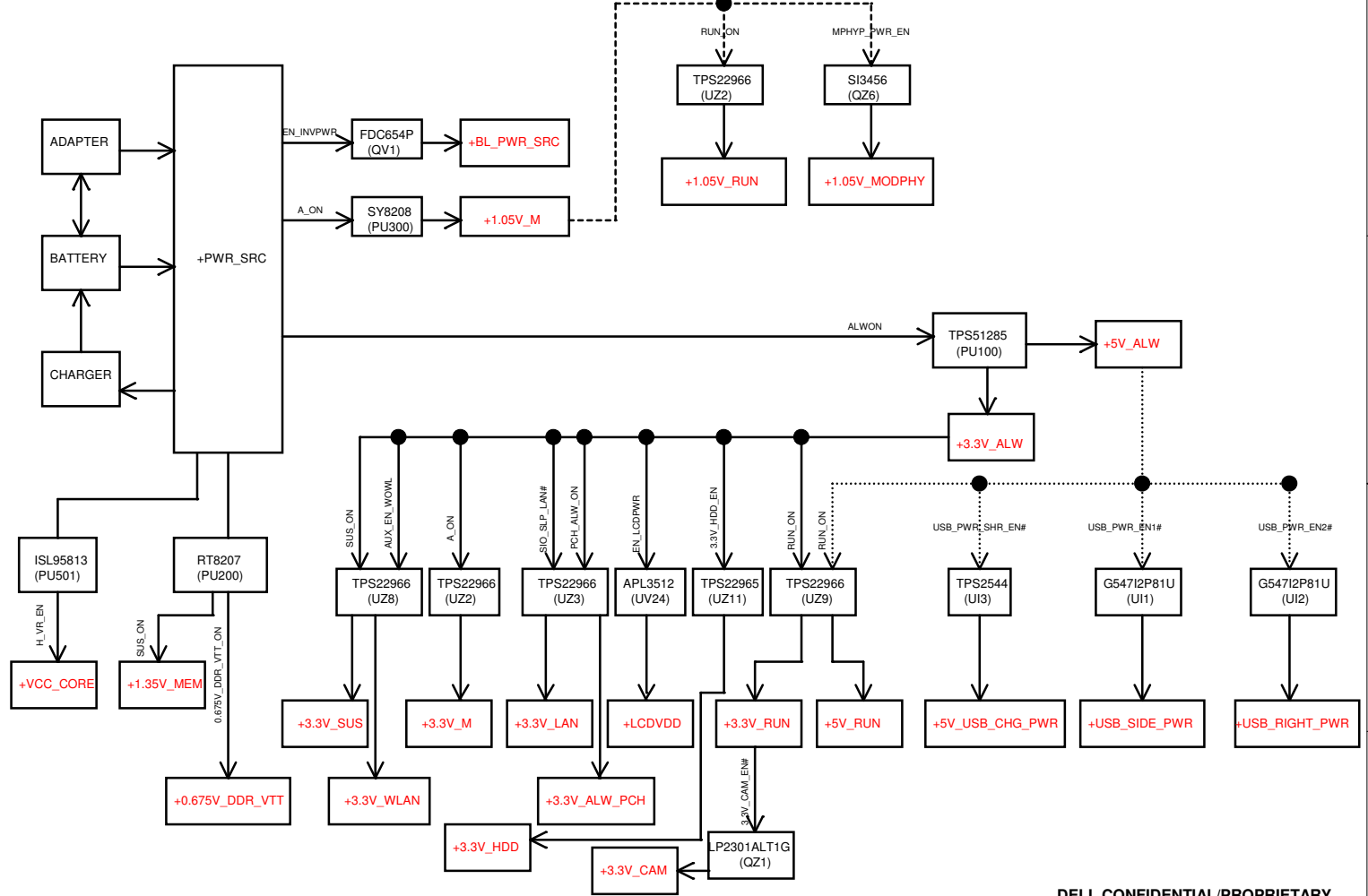
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File: **Port assignment**

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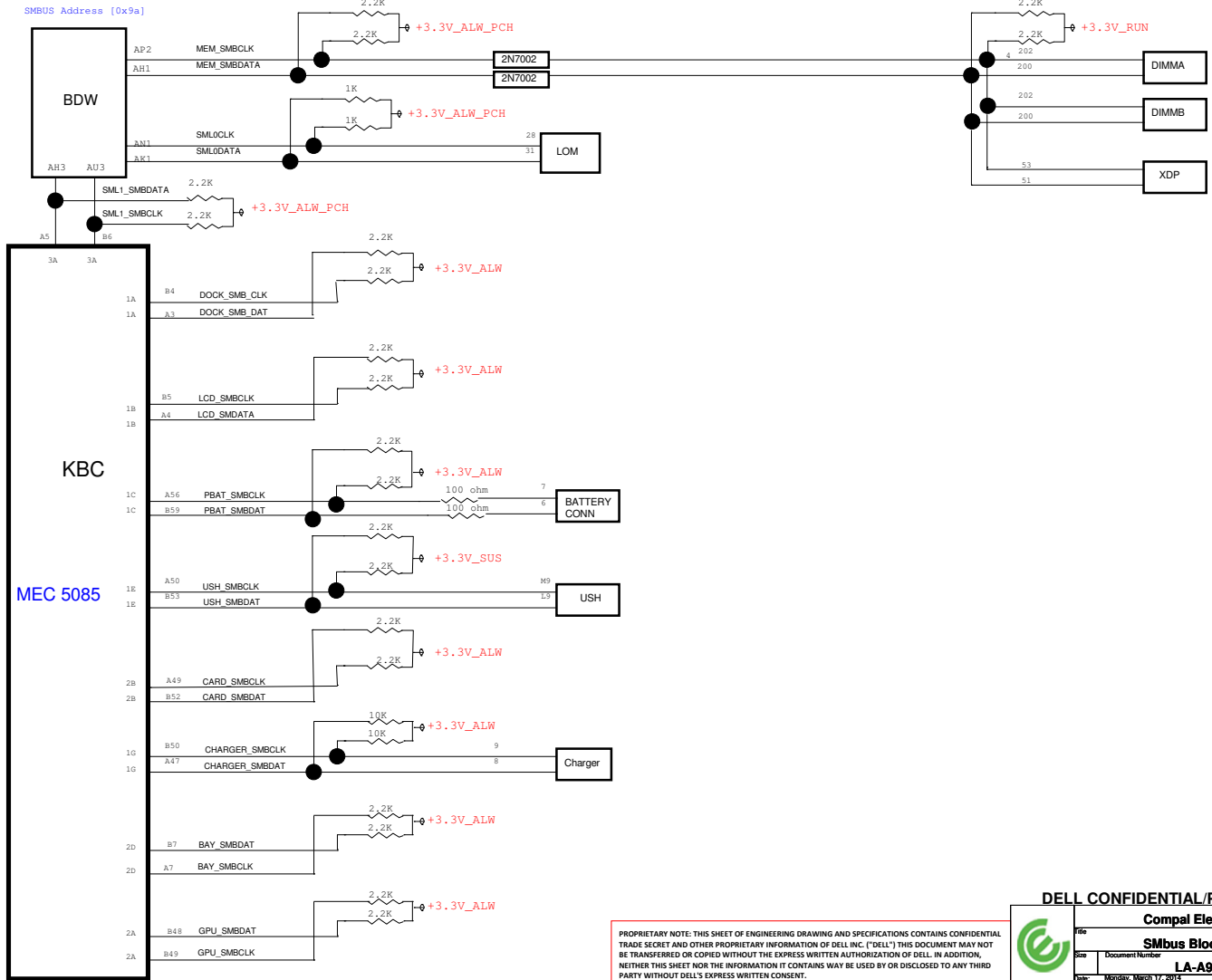
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SMBUS Address [0x9a]



MEC 5085

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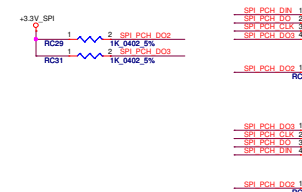
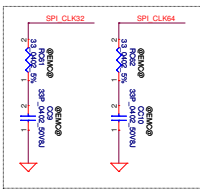
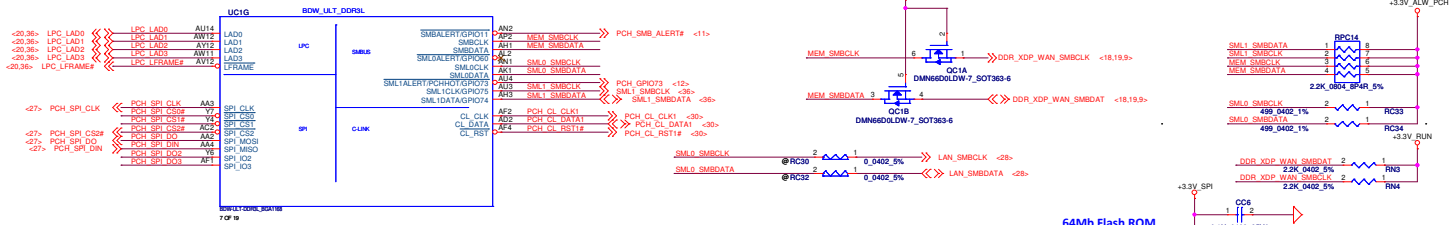
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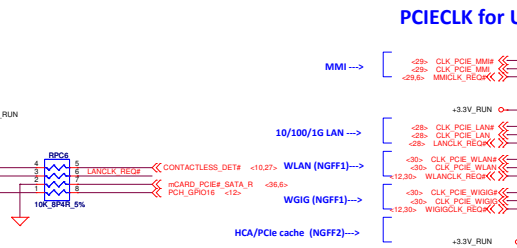
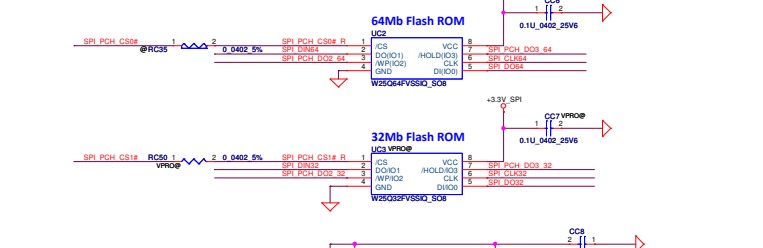
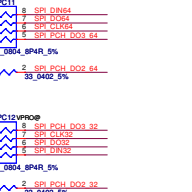
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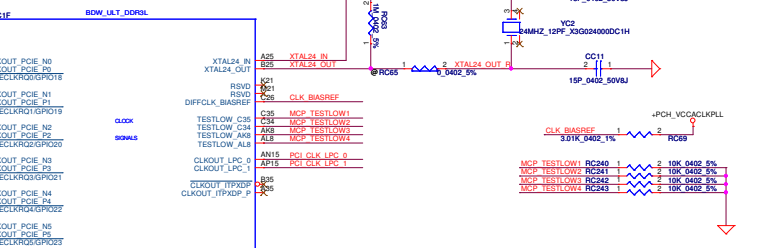
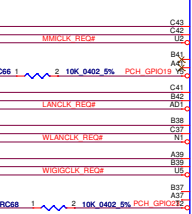




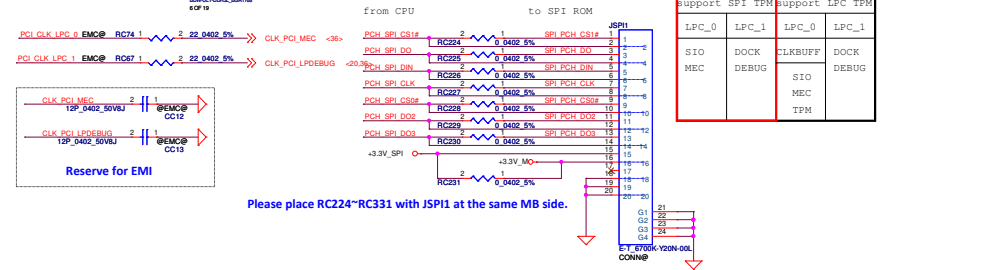
**SOFTWARE TAA**



**PCIEMK for UMA**



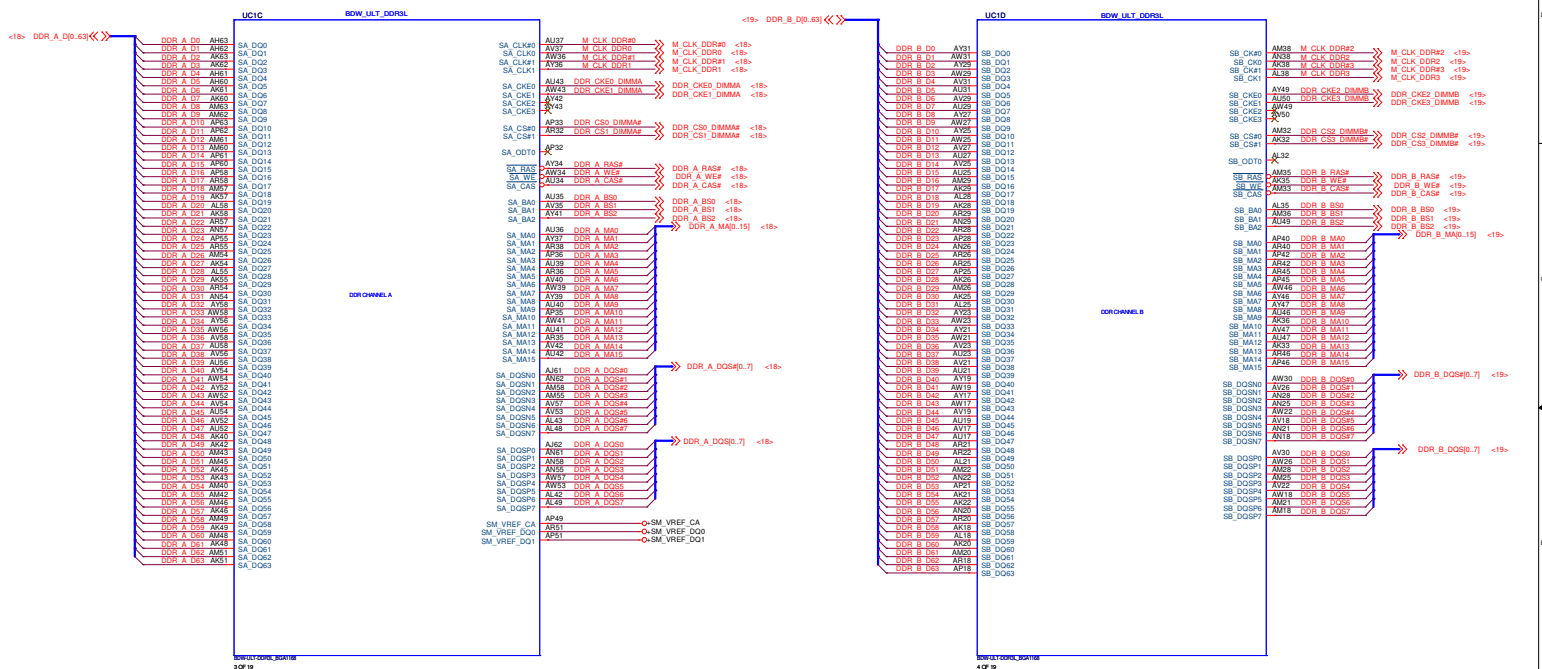
PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14U_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA



support SPI TPM		support LPC TPM	
LPC_0	LPC_1	LPC_0	LPC_1
SIO	DOCK	CLKBUFF	DOCK
MEC	DEBUG	SIO	MEC
		TPM	DEBUG

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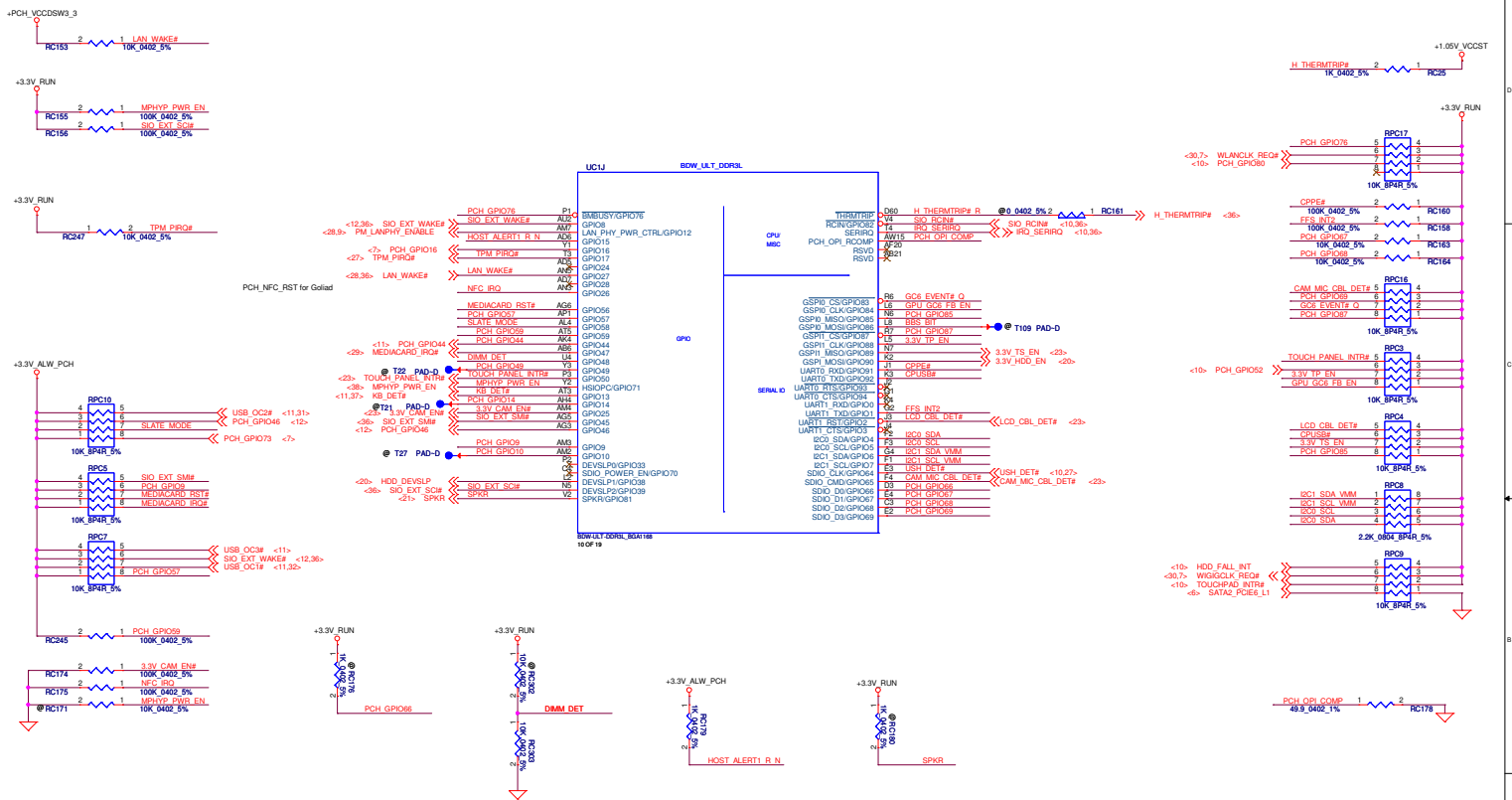
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TOP-BLOCK SWAP OVERRIDE		DIMM Detect		TLS CONFIDENTIALITY		No Reboot on TCO Timer expiration	
HIGH	ENABLE	HIGH	1 DIMM	HIGH	ENABLE	HIGH	ENABLE
LOW(DEFAULT)	DISABLE	LOW	2 DIMM	LOW(DEFAULT)	DISABLE	LOW(DEFAULT)	DISABLE

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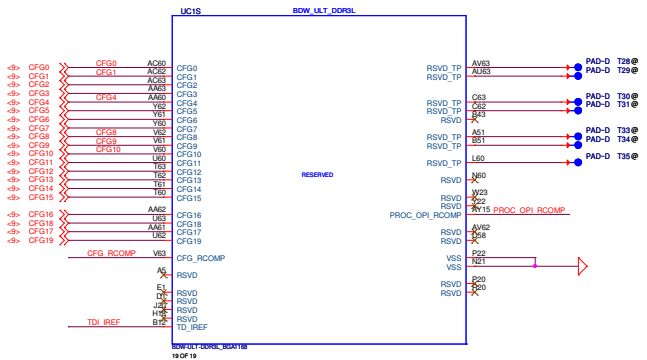
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**CPU (7/12)**

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### CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked 0:Disable Noa will be available pegrardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

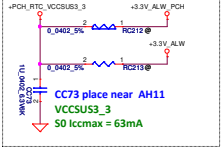
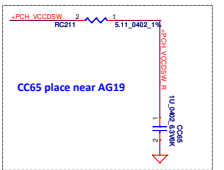
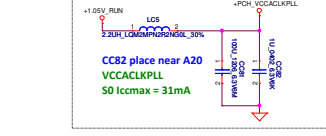
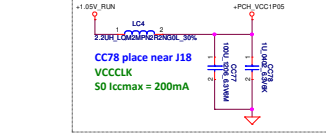
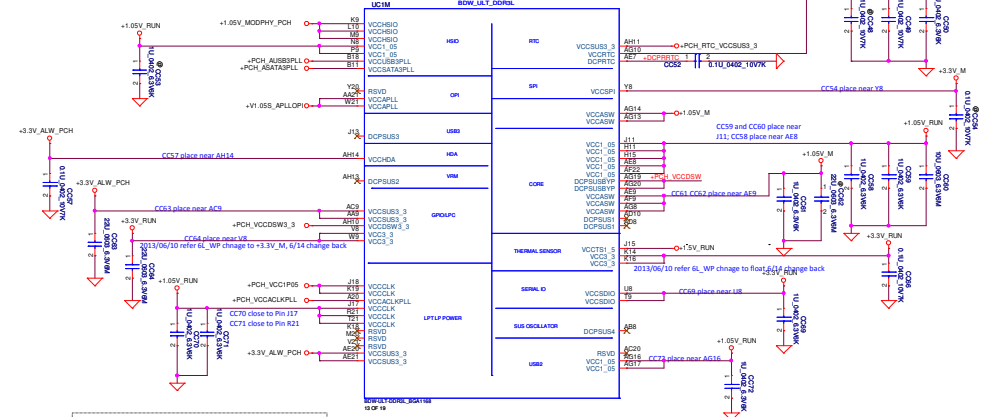
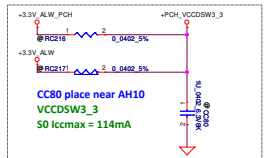
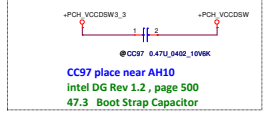
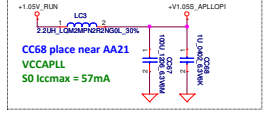
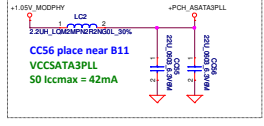
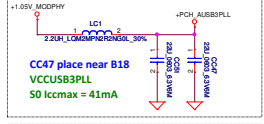
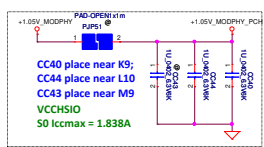
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Voltage Rail	Voltage (V)	S0 Iccmax Current (A)	Sx Iccmax Current (A)	Deep Sx Iccmax (A)	G3
VCCIO5 (Internal Suspend VR mode using HTVRMEN)	1.05	1.741	0	0	0
VCCIO3 (Internal Suspend VR mode using HTVRMEN)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCCLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.290	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCSUS3_3	1.5	0.003	0	0	0
VCCSUS2_3	3.3	0.041	0	0	0
VCCSUS1_3	3.3	0.017	0	0	0
VCCSUS0_3	1.05	0.658	0	0	0
VCCSUS3_3 (External Suspend VR mode using HTVRMEN)	3.3	0.058	0	0	0
VCCSUS2_3 (External Suspend VR mode using HTVRMEN)	3.3	0.011	<1 mA	0	0
VCCSUS1_3 (External Suspend VR mode using HTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS0_3 (External Suspend VR mode using HTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1*	1.05	0.109	0.014	0	0
DcpSus2*	1.05	0.025	0.001	0	0
DcpSus3*	1.05	0.010	0.001	0	0
DcpSus4*	1.05	0.001	0.001	0	0
VCCDSW2_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	8 $\mu$ A See notes 1, 2

**Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.**

**Power Rail Isolation**

Voltage Supply	Interface (power rail isolation required)	PCH Pins sharing power rail
V1.05v	Core	Z11, H11, H15, A81, AF22
	DIE	FA21, W21
	HSD	K9, L10, M1, P9, B18, B11, M9
	USB2	AG16, AG17
	CLKA(L)	A20
V3.3v	CLK(A)	B21, Y21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3v	LPOD	ACE, A85, AE20, AE21
	RTC	AH11
	HDA	AH14
V3.3v	GPOD	W8, W9
	USDD	U8, T9
	Thermal Sensor	K14, K15

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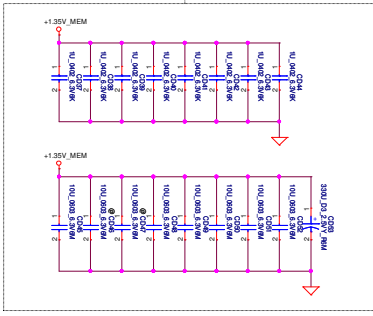


H=4mm  
Reverse Type

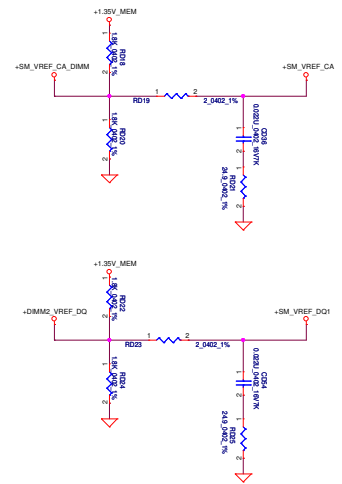
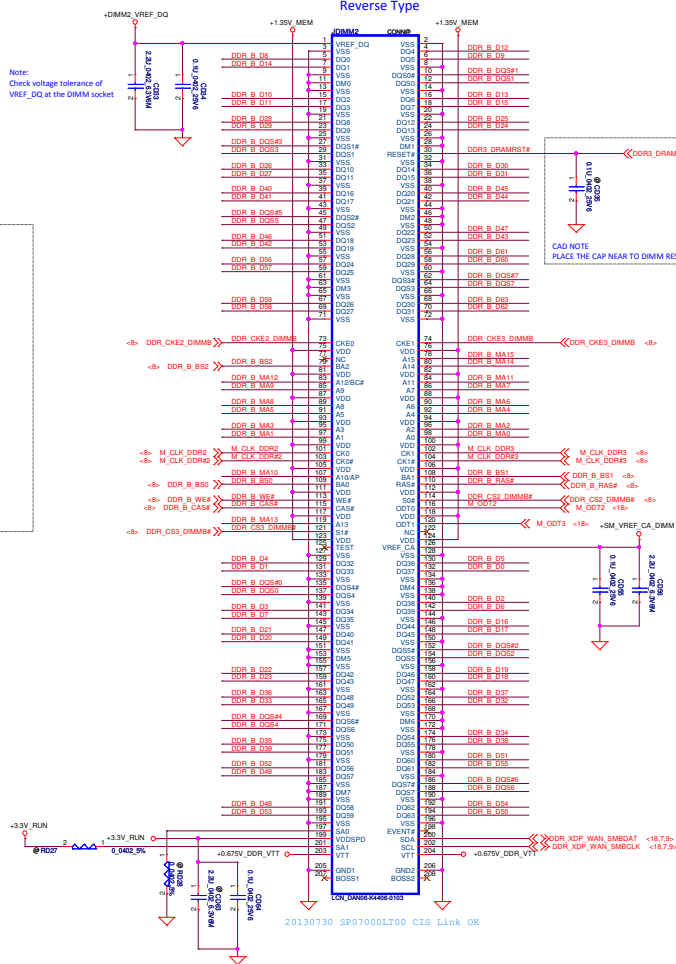
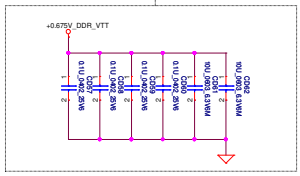
- <-> DDR\_B\_D0S4E.7
- <-> DDR\_B\_D0E.4S
- <-> DDR\_B\_D0S0.7
- <-> DDR\_B\_MAP.1S

Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

Layout Note:  
Place near JDIMM2



Layout Note:  
Place near  
JDIMM2.203,204

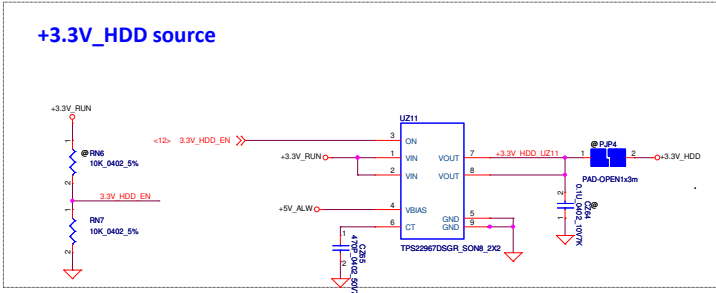


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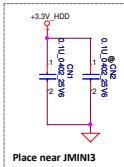
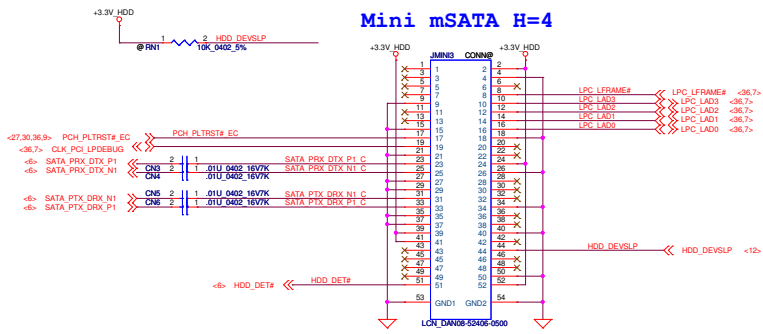
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### +3.3V\_HDD source



### Mini mSATA H=4



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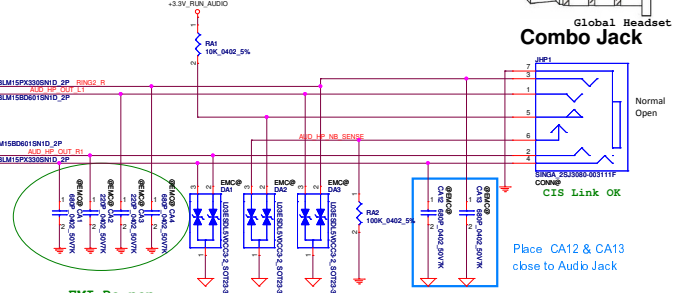
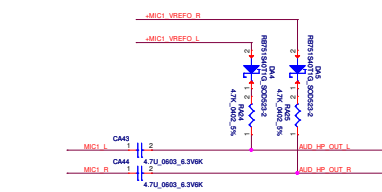
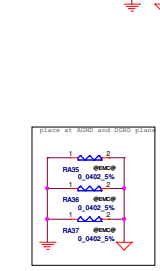
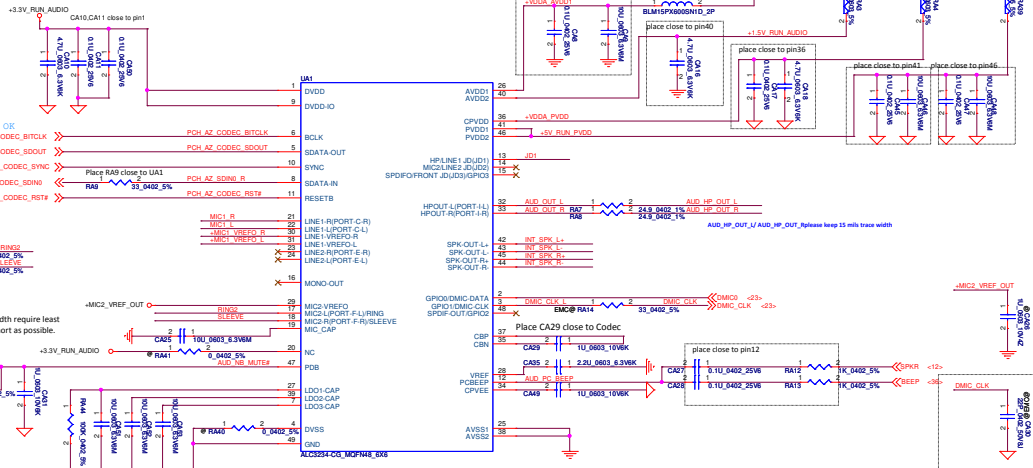
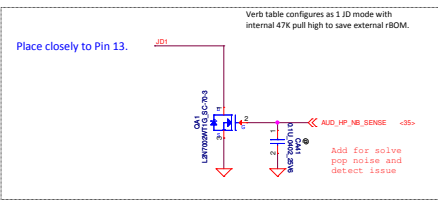
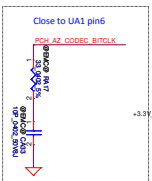
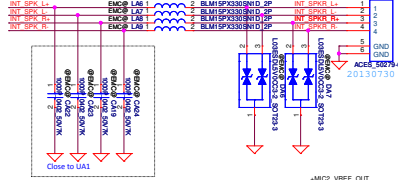
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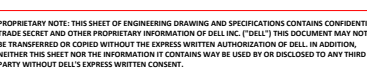
1W x 1oh, 4ohm (Transformer spec is 8ohm) 500mV per unit, there are two transducer units in one speaker box)

### Internal Speakers Header

40 mils trace Keep 20 mils spacing



### EMI De-pop



Realtek feedback  
Prevent the Noise from Combo Jack  
while system entry into S3 / S4 / S5

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**Compal Electronics, Inc.**

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Rev: 1.1

Date: Monday, March 17, 2014

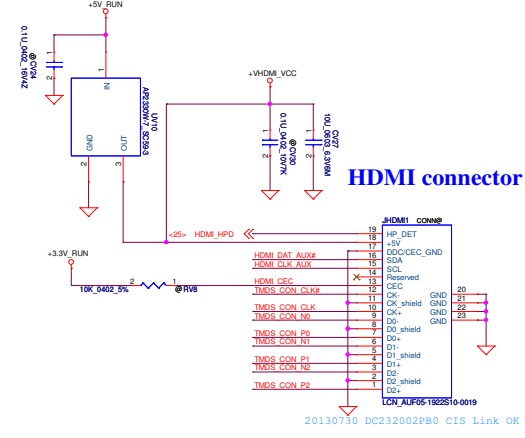
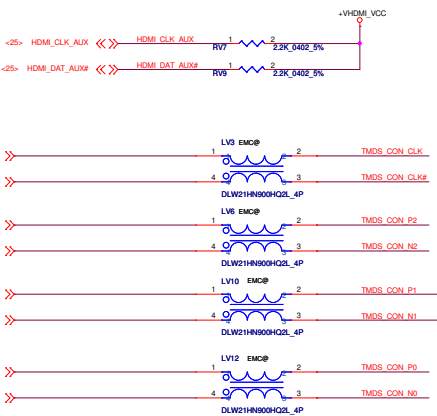
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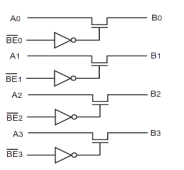
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Compal Electronics, Inc.	
DP 1.2 MST HUB	
Doc Number	LA-A972P
Date	Monday, March 17, 2014
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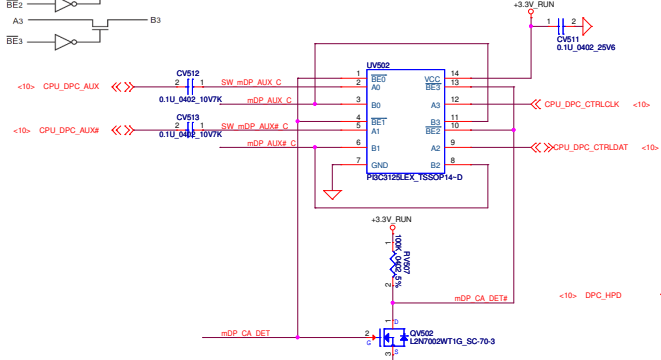




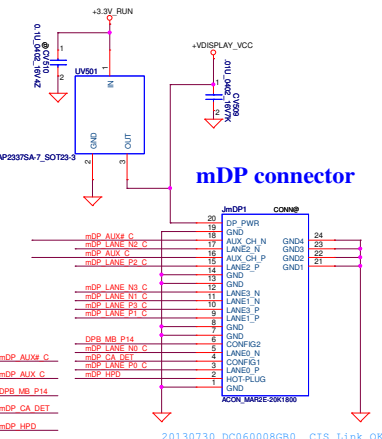
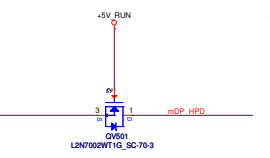
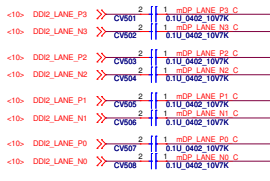
20130730 DC232002P80 CIS Link OK  
 LCN\_AU051922510-0019



**AUX/DDC SW for DDI2 to Mini DP**



mDP_CA_DET	Function
1	mDP
0	BIOS



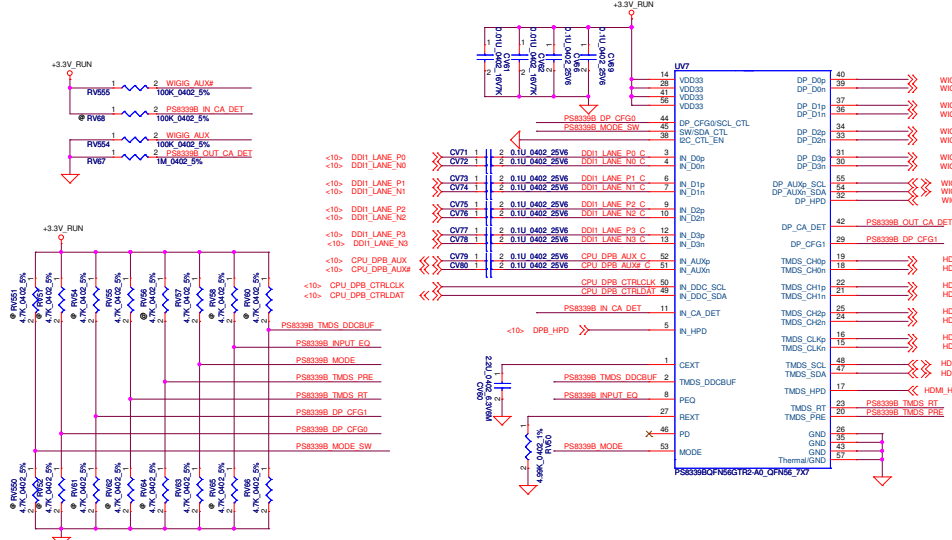
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 ACOM\_MAREE20K1800

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		<b>Compal Electronics, Inc.</b> <b>HDMI CONN</b>	
		Title: <b>LA-A972P</b>	Rev: <b>0.1</b>
Doc Number:	Date: <b>Monday, March 17, 2014</b>	Sheet: <b>24</b>	of: <b>48</b>

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PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



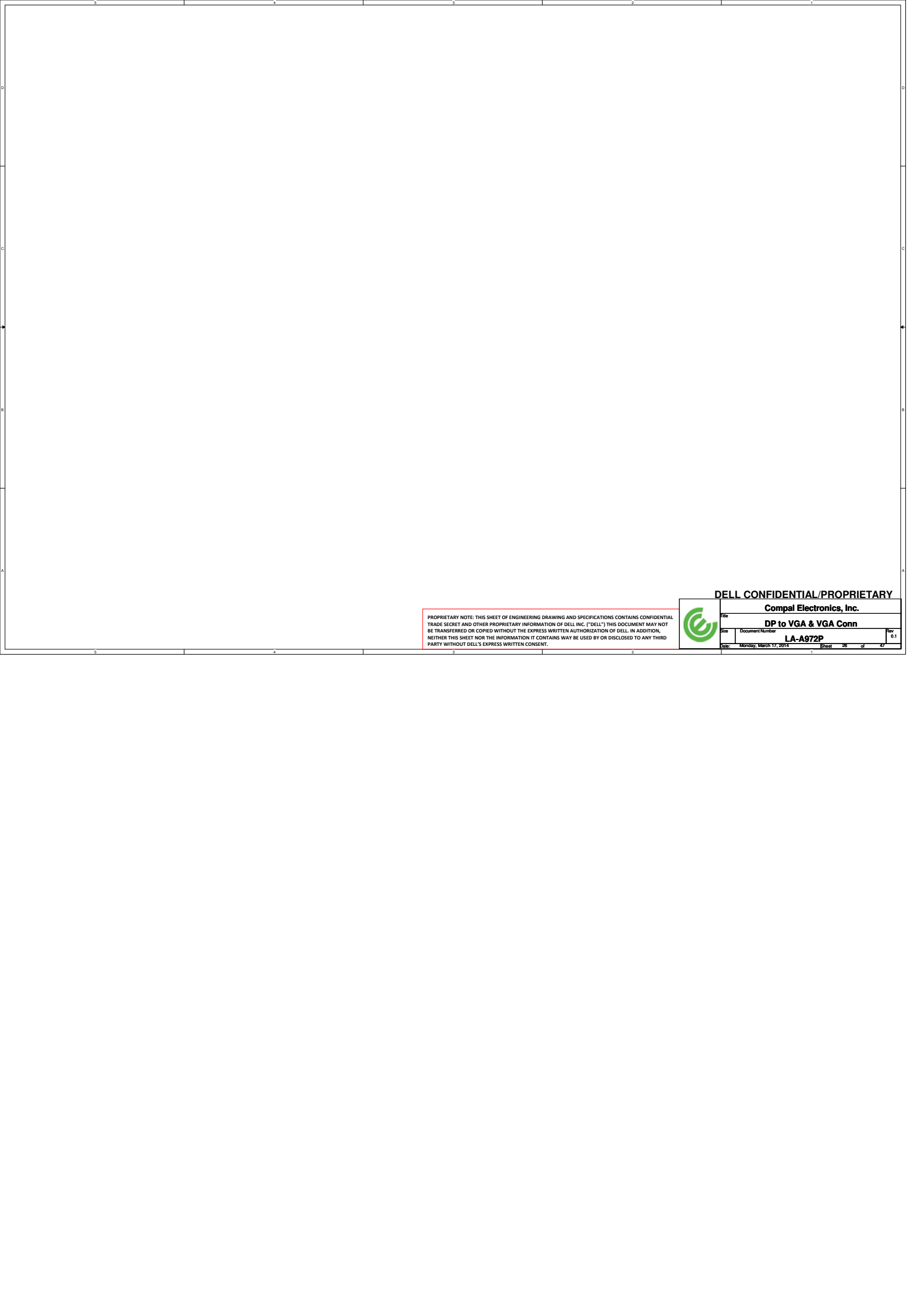
- MODE = L: Control Switching Mode, HDMI ID disable  
= H: Automatic Switching Mode, HDMI ID disable  
= M: Automatic Switching Mode, HDMI ID enable
- TMDS\_PRE = L: no pre-emphasis  
= H: 1.5dB pre-emphasis  
= M: 3.0dB pre-emphasis
- TMDS\_RT = L: Standard open drain driver  
= H: Open drain driver with termination resistors
- TMDS\_DDCBUF = L: DDC pass through  
= H: DDC active buffer  
= M: DDC pass through with 40 kohm pull up resistor
- PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
= H: HEQ, compensate channel loss up to 15dB @ HBR2  
= M: LLEQ, compensate channel loss up to 5dB @ HBR2
- DP\_CFG1 = L: default, auto test disable & input offset cancellation enable  
= H: auto test enable & input offset cancellation enable  
= M: auto test disable & input offset cancellation disable
- DP\_CFG0 = L: default, automatic EQ enable & AUX interception enable  
= H: automatic EQ disable & AUX interception enable  
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

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**Compal Electronics, Inc.**

<b>DP SW</b>	
Doc Number	Rev
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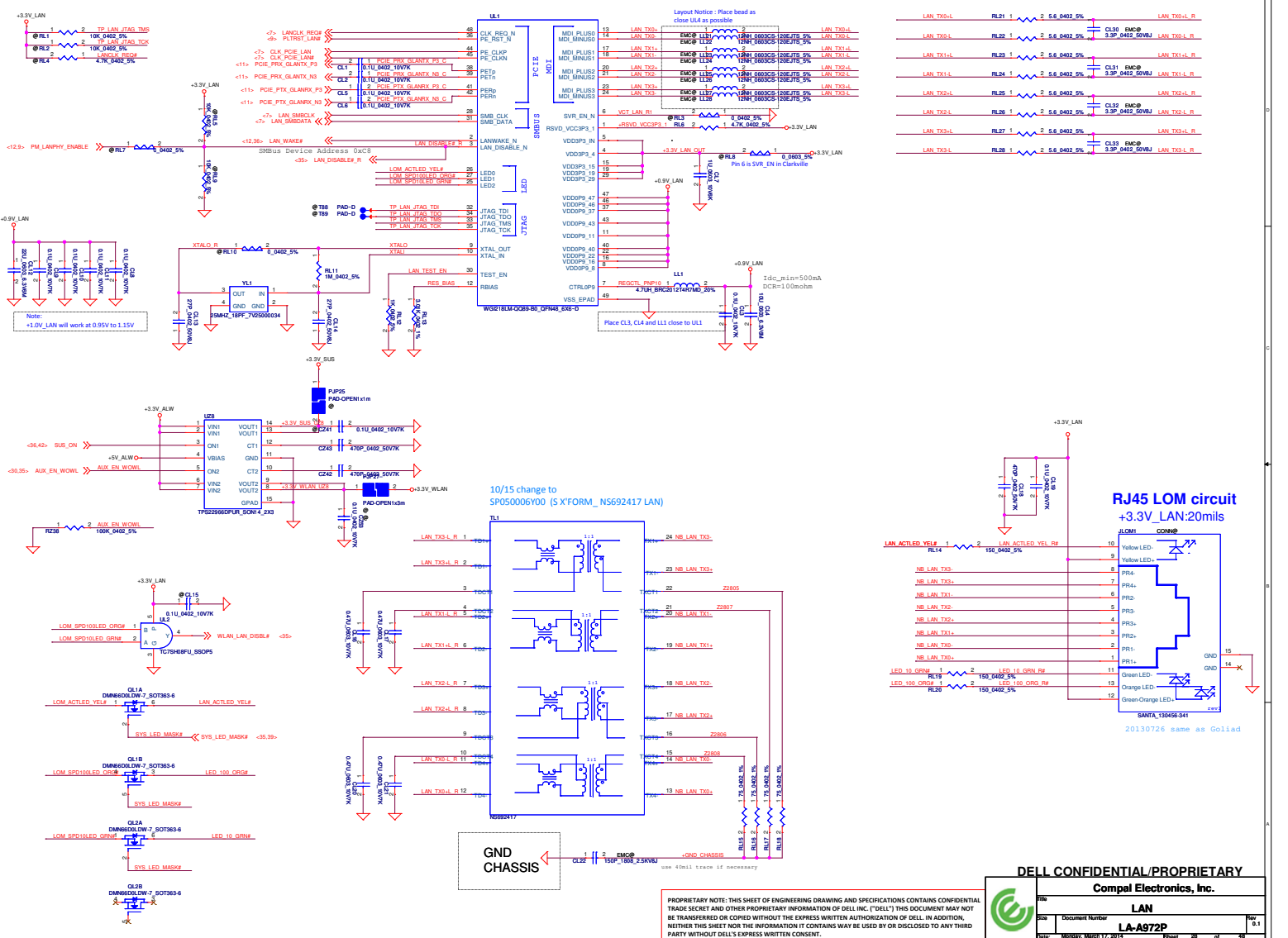


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	<b>Compal Electronics, Inc.</b>	
	<b>DP to VGA &amp; VGA Conn</b>	
	<b>LA-A972P</b>	Rev 0.1
Date:	Monday, March 17, 2014	Sheet 25 of 47





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**Compal Electronics, Inc.**

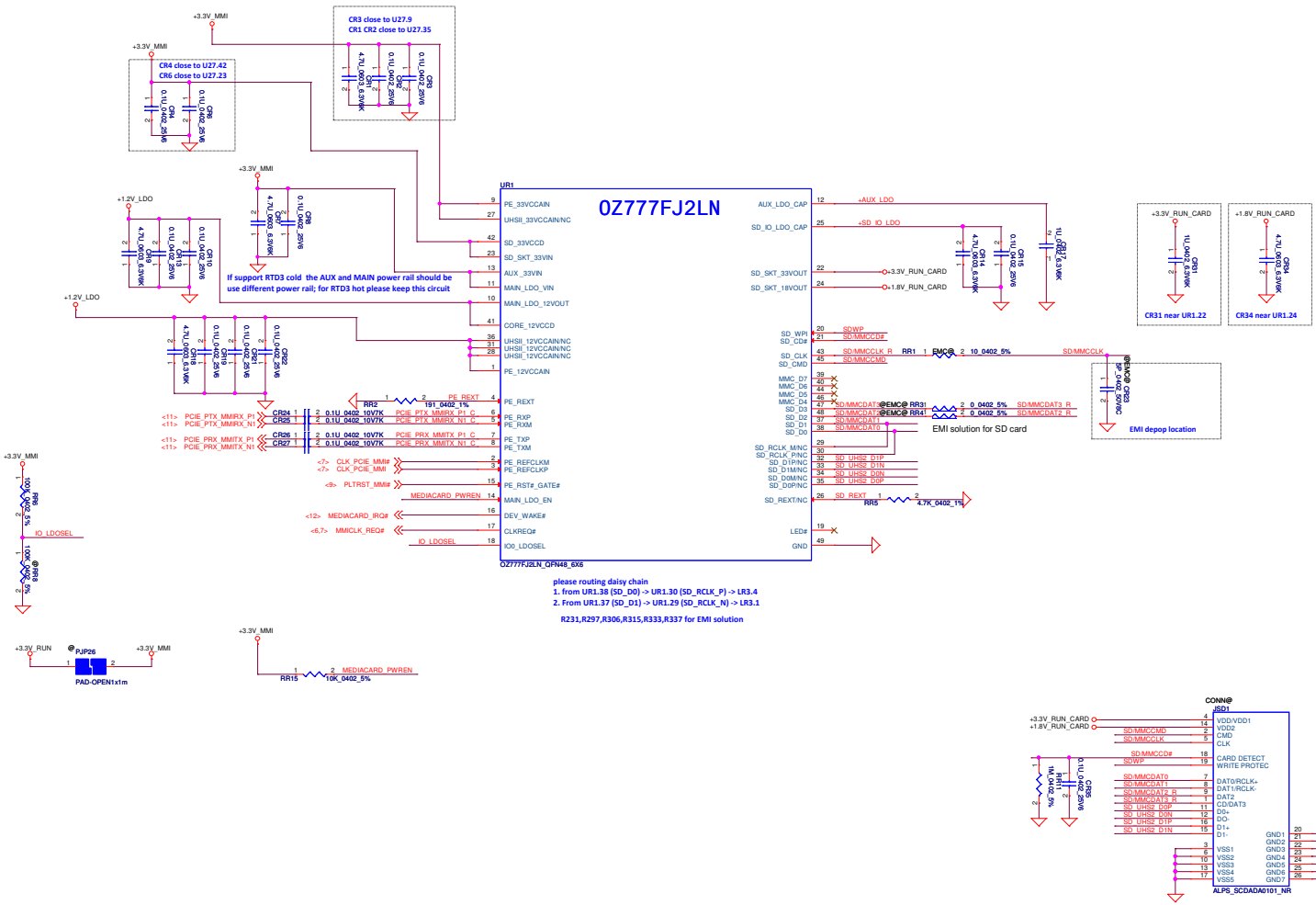
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Doc: Document Number **LA-A972P**

Date: Monday, March 17, 2014

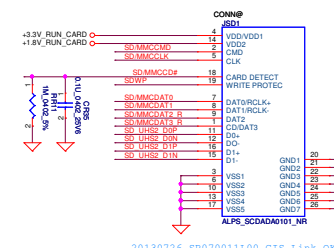
Sheet: 39 of 45

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please routing deaisy chain  
 1. from UR1.38 (SD\_D0) -> UR1.30 (SD\_RCLK\_P) -> LR3.4  
 2. From UR1.37 (SD\_D1) -> UR1.29 (SD\_RCLK\_N) -> LR3.1

R231, R297, R306, R315, R333, R337 for EMI solution



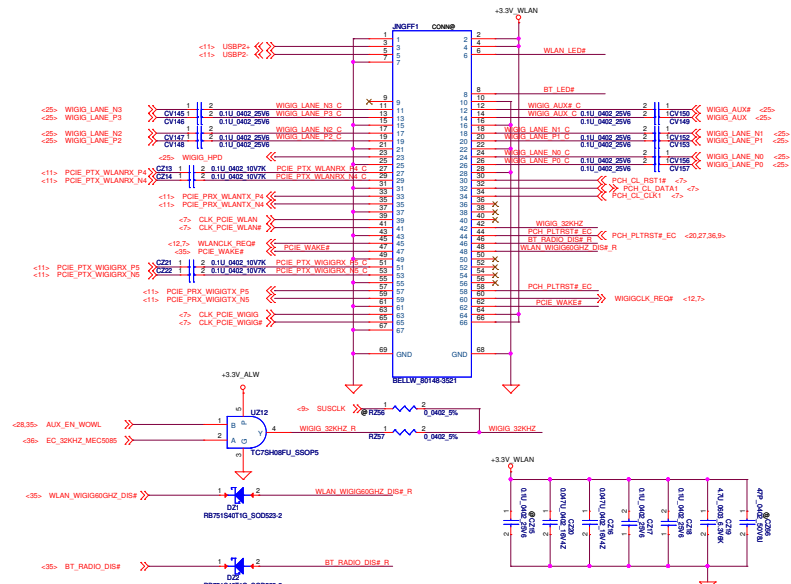
20130726 SP07001100 CIS Link OK

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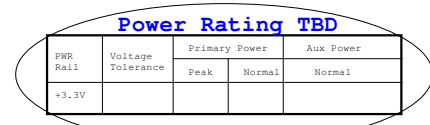
Compal Electronics, Inc.

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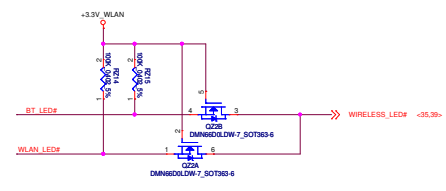
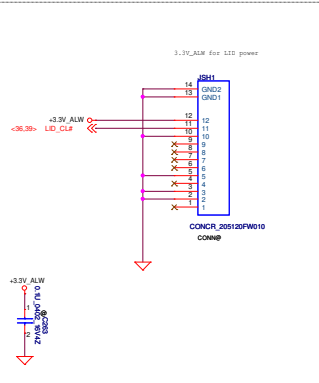
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STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIe
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIe
15	HIGH	HIGH	HIGH	HIGH	NA



LED control circuit



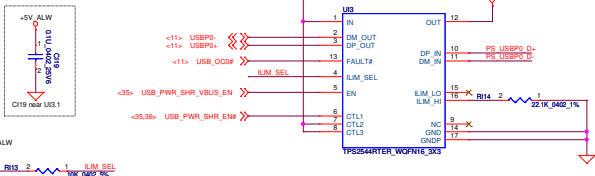
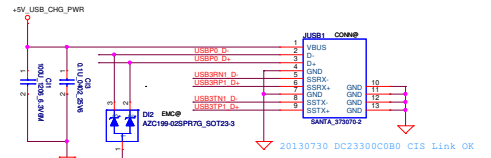
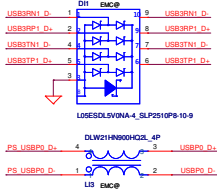
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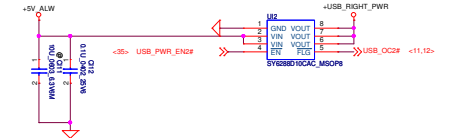
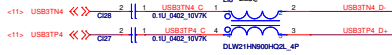
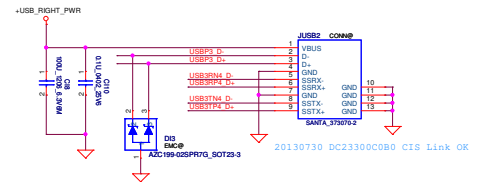
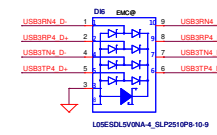
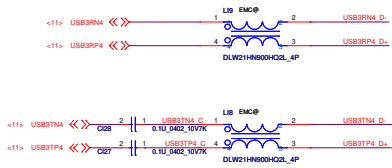


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PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA



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USB3.0		Rev
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# NFC on USH/B

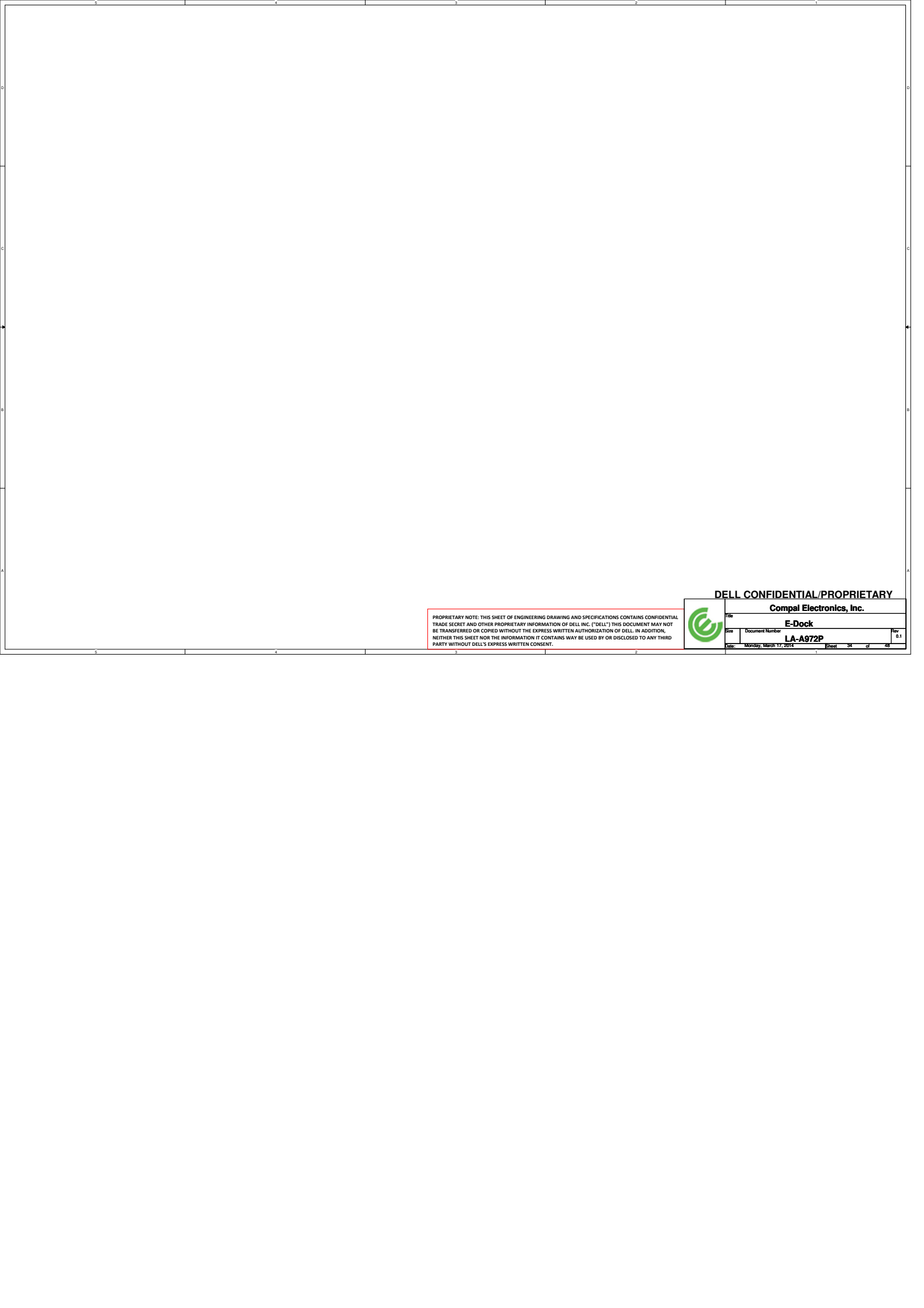
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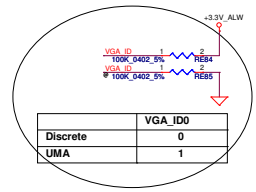
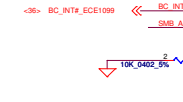
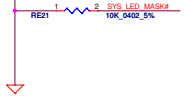
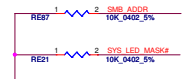
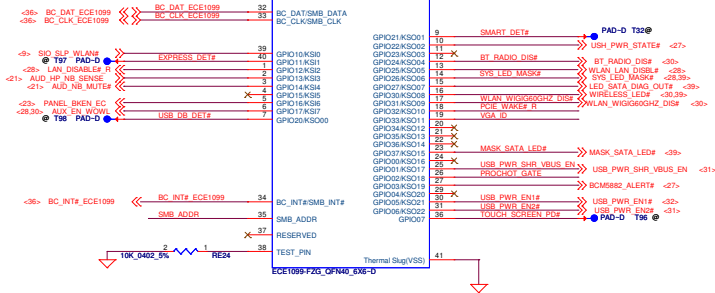
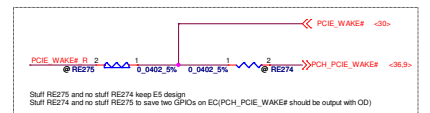
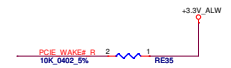
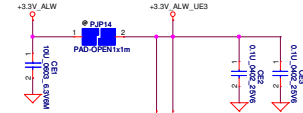
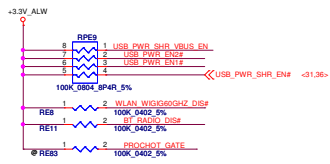
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Size	Document Number	Rev
	<b>LA-A972P</b>	<b>0.1</b>
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Title		<b>E-Dock</b>	
Size	Document Number	<b>LA-A972P</b>	
Date		Monday, March 17, 2014	Rev 0.1
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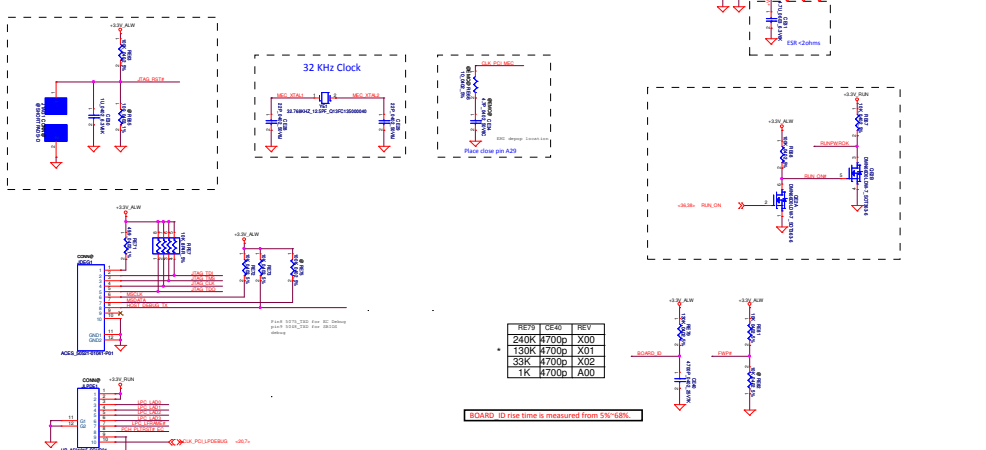
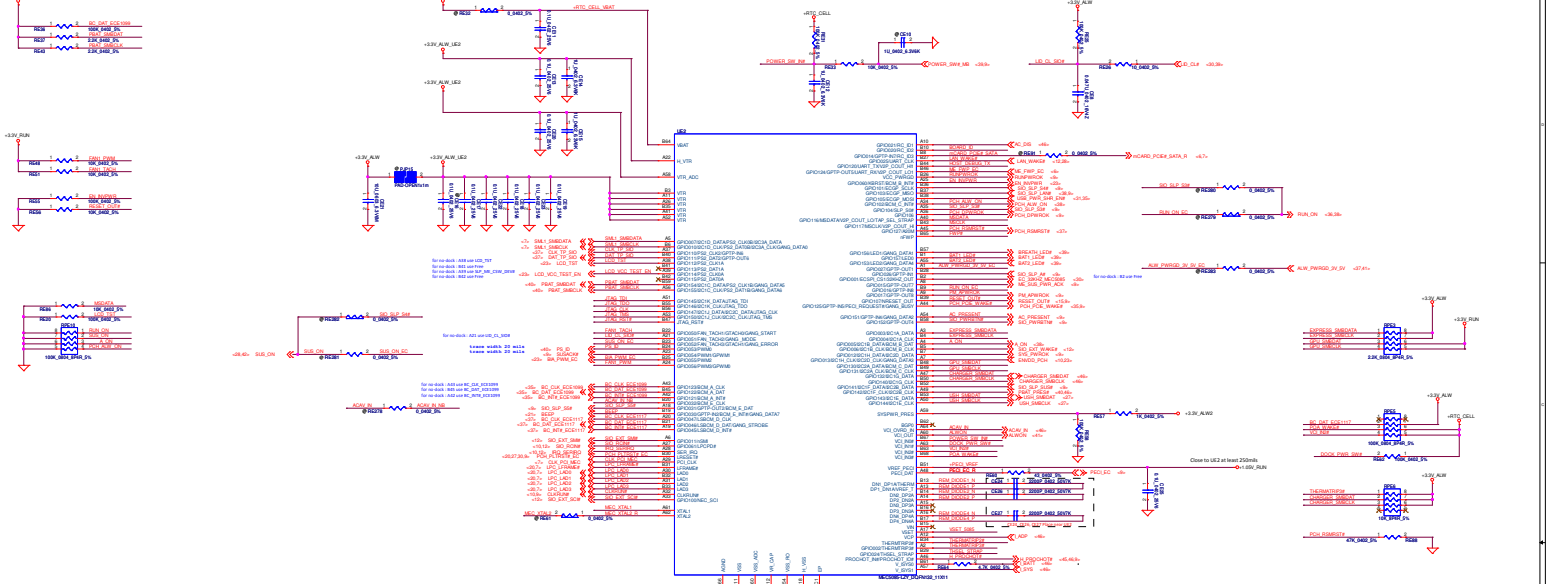


	VGA_ID0
Discrete	0
UMA	1

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### Setting for Thermal Design

Thermal diode mapping

SMS Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DP3/DN3	VGA
DP4/DN4	V.R

Place under CPU  
Place QES close to the QES as possible

DP2/DN2 for SODIMM on QES, place QES close to SODIMM and QES close to QES

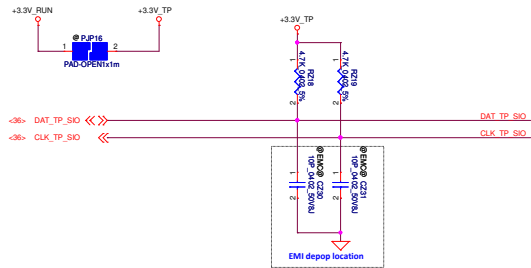
DP3/DN3 for VGA on QES, place QES close to VGA/ALAN and QES close to QES

DP4/DN4 for V.R on QES, place QES close to V.R. check.

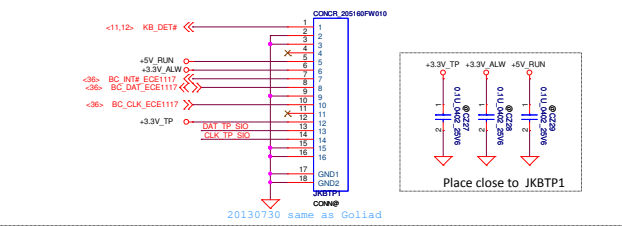
Channel 1  
Thermal Diode Mapping: DP1/DN1, DP2/DN2, DP3/DN3, DP4/DN4  
Thermal Diode Mapping: QES  
Thermal Diode Mapping: QES

Keep 1.58K, 7p-56 degree

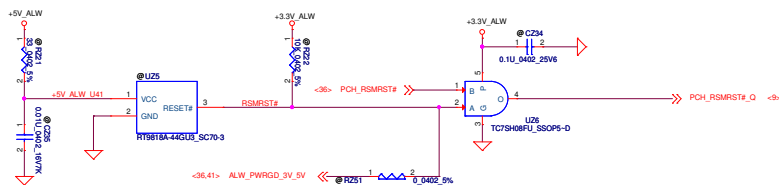
### Touch Pad



### Keyboard



### RSMRST circuit



#### @P Cable

Part Number	Description
DCS1057P00	8-COMM SET 14A MB-ESP-LED-CAMERA

#### @P TS Cable

Part Number	Description
DCS1007P00	8-COMM SET 14A MB-ESP-LED-CAMERA-TS

#### @DC-IN Cable

Part Number	Description
DCS1006P00	COMM SET 09N DC3ACR-MB 22W1003-038110P

#### @RTC BATT

Part Number	Description
DCS1006P00	COMM SET 09N DC3ACR-MB 22W1003-038110P

#### @FAN

Part Number	Description
DC28A005800	FAN SET DAQ25 DC5V AB74058B-MB3 A20A

#### @USH Board FFC

Part Number	Description
HBK00018200	FFC 50P G P0.5 PAD=0.3 4786 MB-USH

#### @VTP FFC

Part Number	Description
HBK00018200	FFC 50P G P0.5 PAD=0.3 4786 MB-USH

#### @NFC Board FFC

Part Number	Description
HBK00018200	FFC 50P G P0.5 PAD=0.3 40,386 MB-HPF

#### @FP FFC

Part Number	Description
HBK00018200	FFC 50P F P0.5 PAD=0.3 22,386 MB-FP

#### @SM-HMB FFC

Part Number	Description
HBK00018200	FFC 12P G P0.5 PAD=0.3 73,386 MB-S1H-BALL

#### @Spk

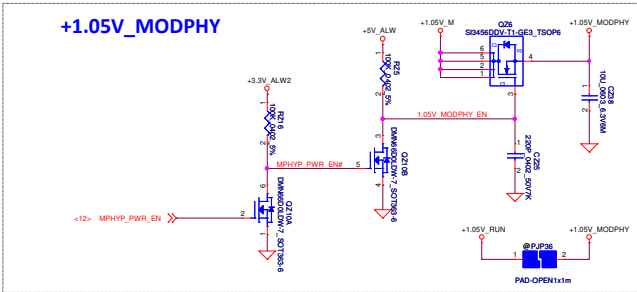
Part Number	Description
PK230053Q01	SPK PACK 2.5X 2.0X 4 OHM PD

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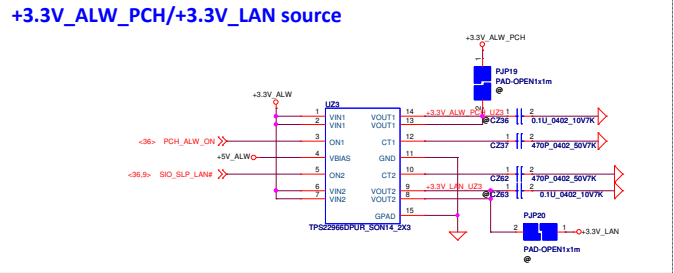
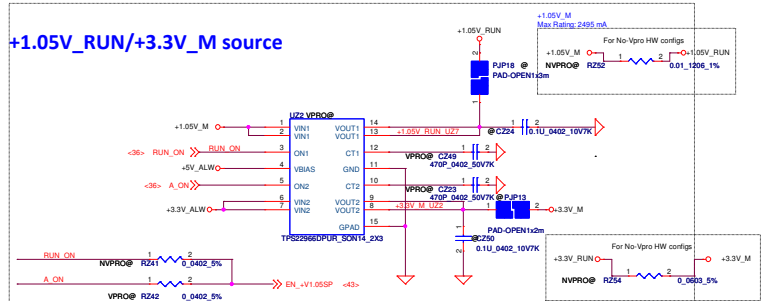
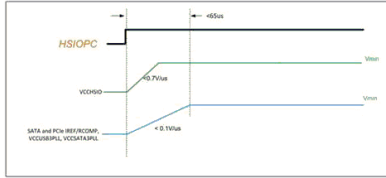
File	Keyboard
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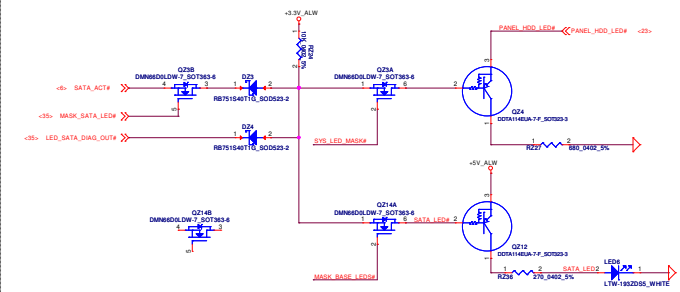


if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

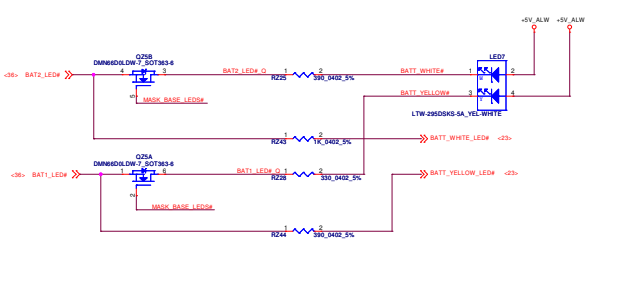
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



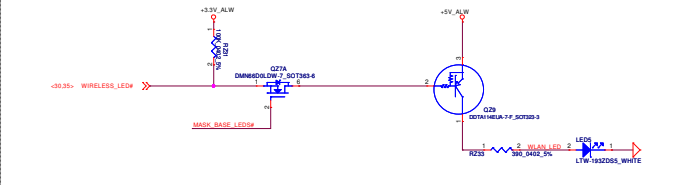
### HDD LED solution for White LED



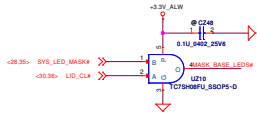
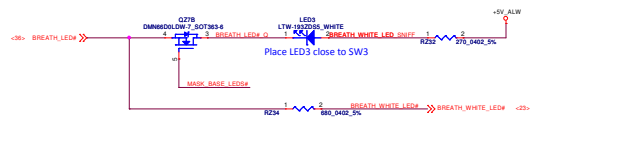
### Battery LED



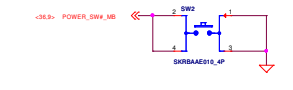
### WLAN LED solution for White LED



### Breath LED

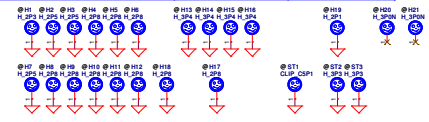


### POWER & INSTANT ON SWITCH



	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

- Fiducial Mark**
- ⊙ F01
  - ✕ F02
  - F03
  - ⊙ F04



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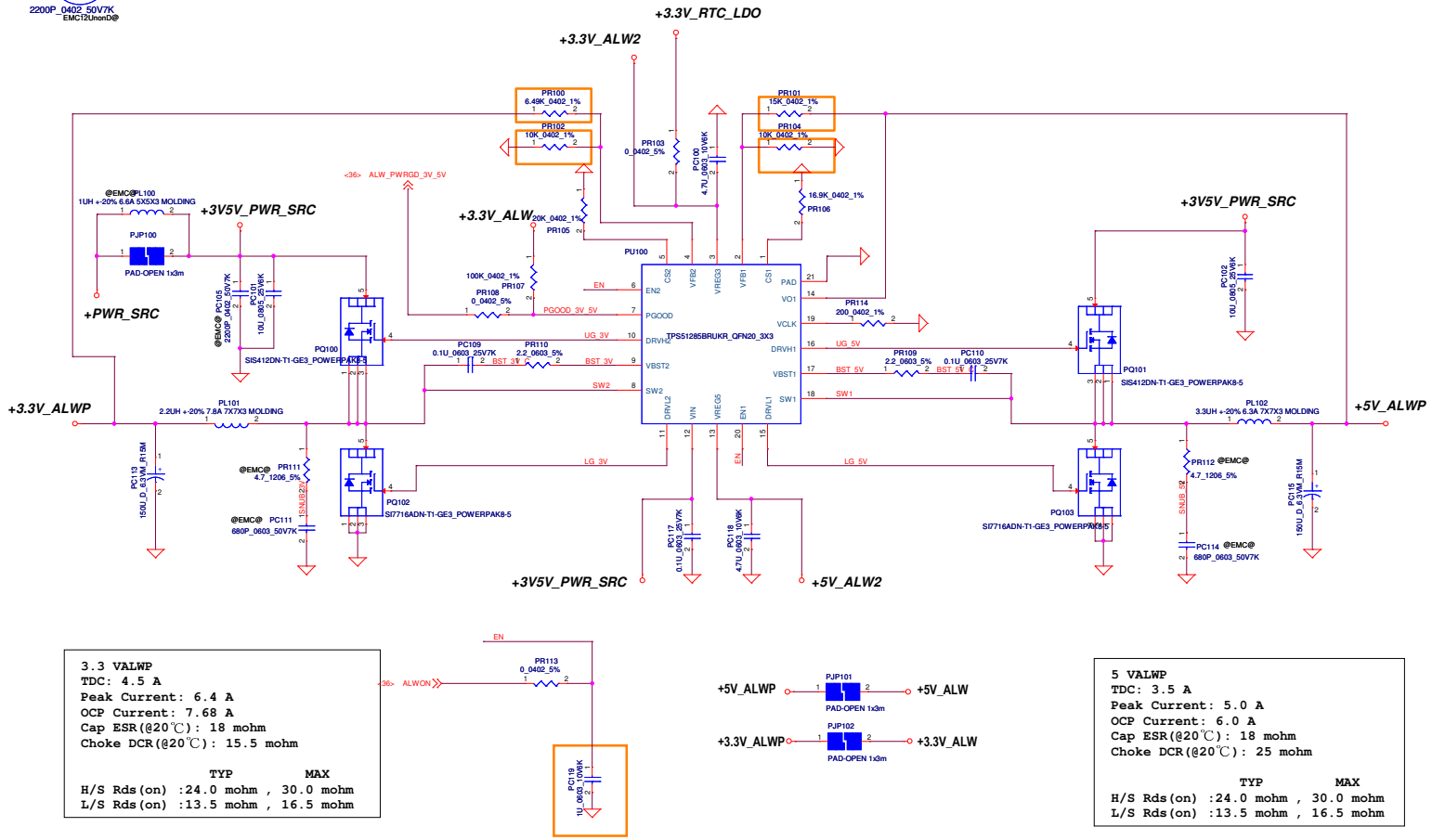
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**PAD\_LED**

Doc# Document Number: **LA-A972P**

Date: Monday, March 17, 2014





3.3 VALWP

TDC: 4.5 A

Peak Current: 6.4 A

OCF Current: 7.68 A

Cap ESR (@20°C): 18 mohm

Choke DCR (@20°C): 15.5 mohm

	TYP	MAX
H/S Rds (on)	:24.0 mohm	30.0 mohm
L/S Rds (on)	:13.5 mohm	16.5 mohm

5 VALWP

TDC: 3.5 A

Peak Current: 5.0 A

OCF Current: 6.0 A

Cap ESR (@20°C): 18 mohm

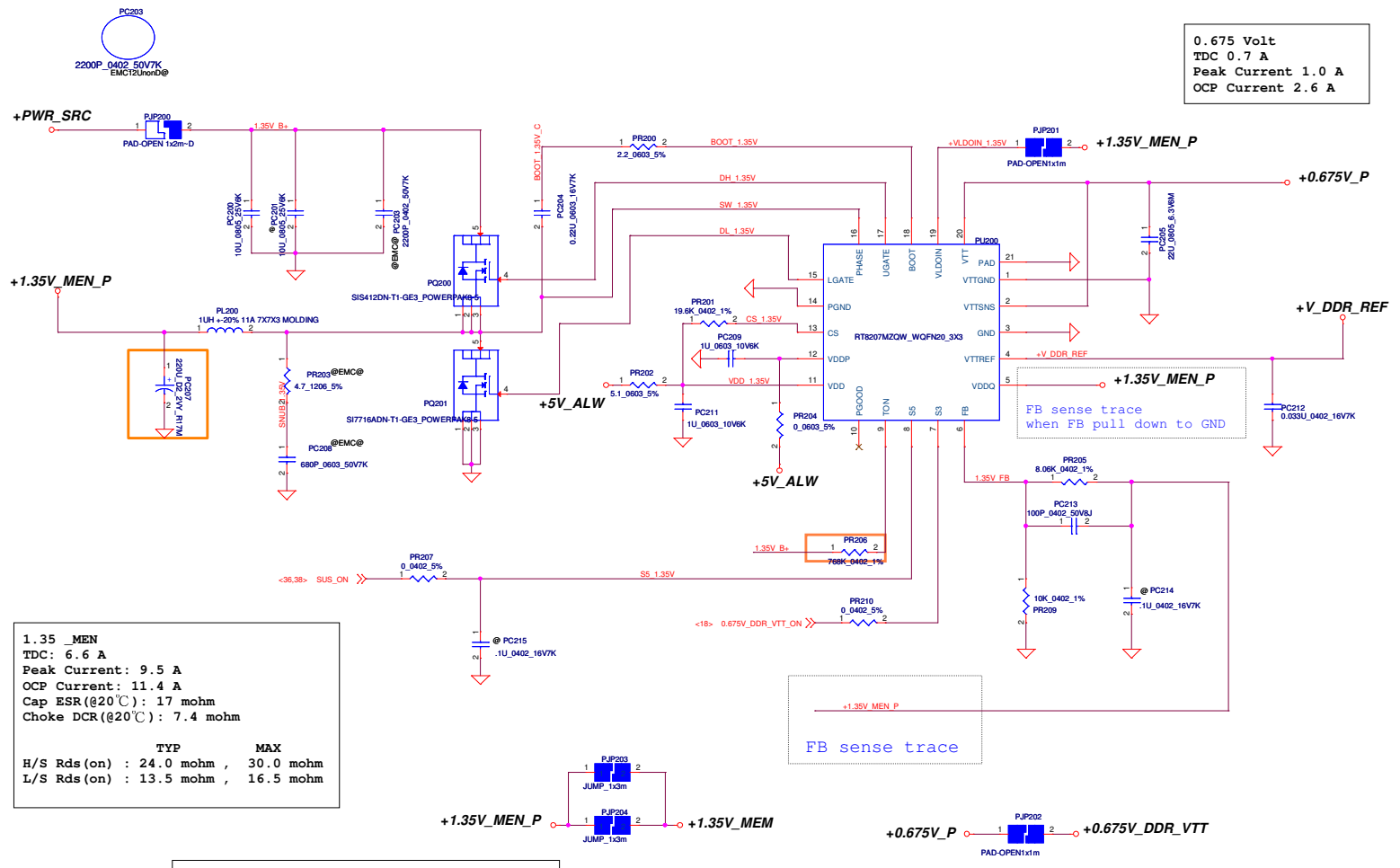
Choke DCR (@20°C): 25 mohm

	TYP	MAX
H/S Rds (on)	:24.0 mohm	30.0 mohm
L/S Rds (on)	:13.5 mohm	16.5 mohm

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0.675 Volt  
 TDC 0.7 A  
 Peak Current 1.0 A  
 OCP Current 2.6 A



1.35\_MEN  
 TDC: 6.6 A  
 Peak Current: 9.5 A  
 OCP Current: 11.4 A  
 Cap ESR (@20°C): 17 mohm  
 Choke DCR (@20°C): 7.4 mohm

	TYP	MAX
H/S Rds (on)	24.0 mohm	30.0 mohm
L/S Rds (on)	13.5 mohm	16.5 mohm

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

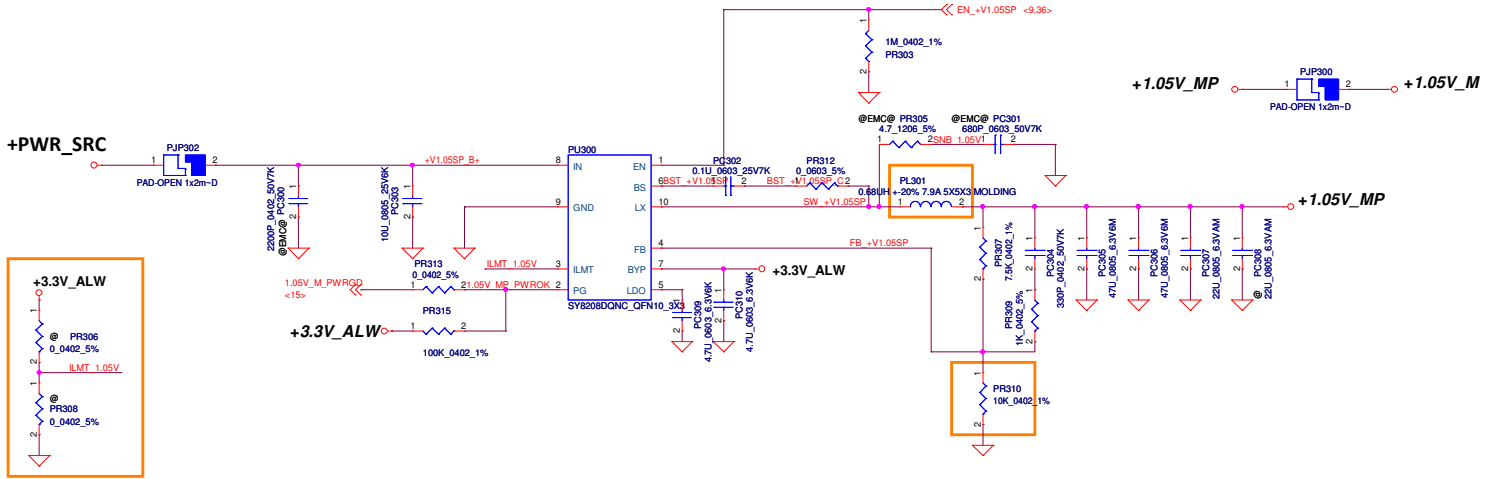
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File	<b>+1.35V_MEN+0.675V_DDR_VTT</b>		
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+1.05V\_MEN  
 TDC: 5.7 A  
 Peak Current: 8.1 A  
 OCP Current: 9.7 A fix by IC  
 Choke DCR(@20°C): 14.0 mohm

PC300  
 2200P\_0402\_50V7K  
 EMC12UhorD@

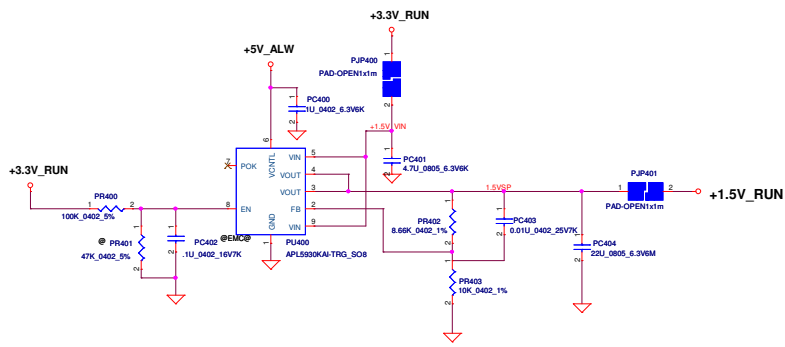


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+1.5V\_RUN  
 TDC: 0.47 A  
 Peak Current: 0.67 A



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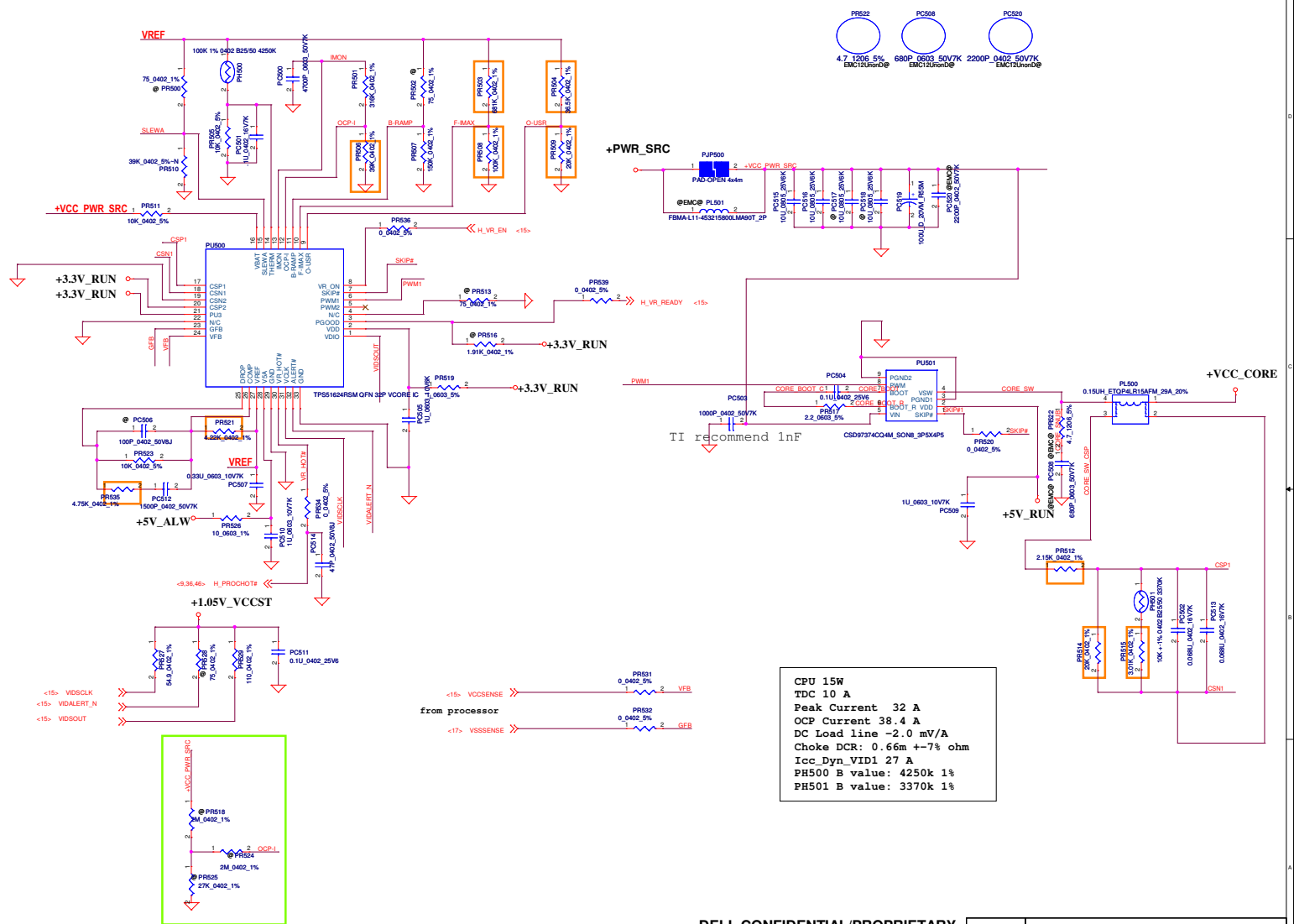
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+1.5VSP

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CPU 15W  
 TDC 10 A  
 Peak Current 32 A  
 OCP Current 38.4 A  
 DC Load line -2.0 mV/A  
 Choke DCR: 0.66m +-7% ohm  
 Icc\_Dyn\_VID1 27 A  
 PH500 B value: 4250k 1%  
 PH501 B value: 3370k 1%

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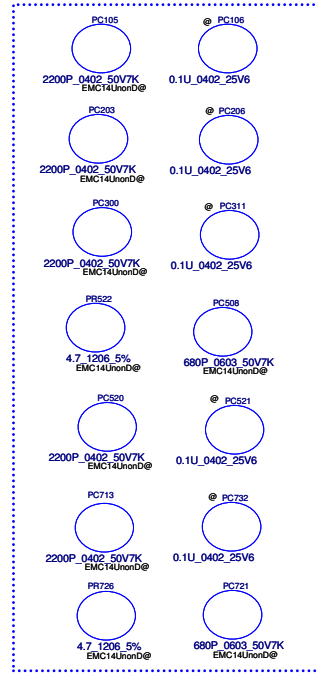
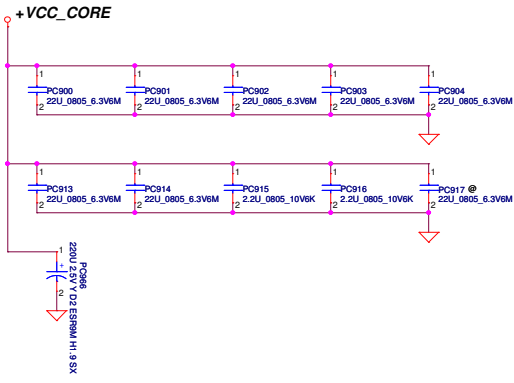
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+VCC CORE	
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Based on \_RF Cheng. Hill  
 鄭智仁 (11257) for PT 20131107

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
2	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
3	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR715, PR729 to 154k	X01
4	41, 43, 44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
5	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
6	ALL	ALL	10/31	Compal	RF request	Pop PR522, PC508, PR726, PC721, PC713, PL501, PC520	X01
7	46	Charger	12/05	Compal	Has the same behavior with dock circuit	Add PQ711	X01
8	46	Charger	12/05	Compal	To add 2nd source	Remove PQ702 Add PQ709, PQ710	X01
9	46	Charger	12/05	Compal	To reduce leakage current	Remove PD701 Add PD704, PD705	X01
10	46	Charger	3/03	Compal	To set OVP level	Remove PR729	X02
11	46	Charger	3/03	Compal	To set IC function	Remove PC720 Add PR788, PR799	X02
12	40	DCIN	3/03	Compal	For ME change request	Change PBATT1	X02
13	40	DCIN	3/03	Compal	For EMC change request	Add PD5 PC20 PC21 PC22 Remove PC11	X02

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<b>PWR P.I.R (1/1)</b>	
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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL			0.2 (X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2 (X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_MURATA DLW21HN900HQ2L)	0.2 (X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2 (X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
9	24	HW	2013/10/9	COMPAL	SATA circuit issue	Swap mSATA P & N	0.2 (X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDL05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2 (X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)

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EE P.I.R (1/3)

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2 (X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 -- SUS_ON_EC , RPE10.2 -- SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 -- RUN_ON_EC	0.2 (X01)
17	12	HW	2013/10/24	COMPAL			0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 & CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL			0.2 (X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop Q26, Q210, RZ16, RZ5, C225, C238	0.2 (X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN36RN4 pull high to +3.3V_RUN for DDR_XDF_WAN_SMBDAT/SMBCLK	0.2 (X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
39	21	HW	2013/12/17	COMPAL			0.3 (X01)
40	22	HW	2013/12/17	COMPAL			0.3 (X01)

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EE P.I.R (2/3)

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