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ZAWBA/ZAWBB
DIS M/B Schematics Document

AMD Beema SOC with DDR3L

AMD Jet LE

2014-03-03

LA-B291P

REV：1.0

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Title	Cover Page	
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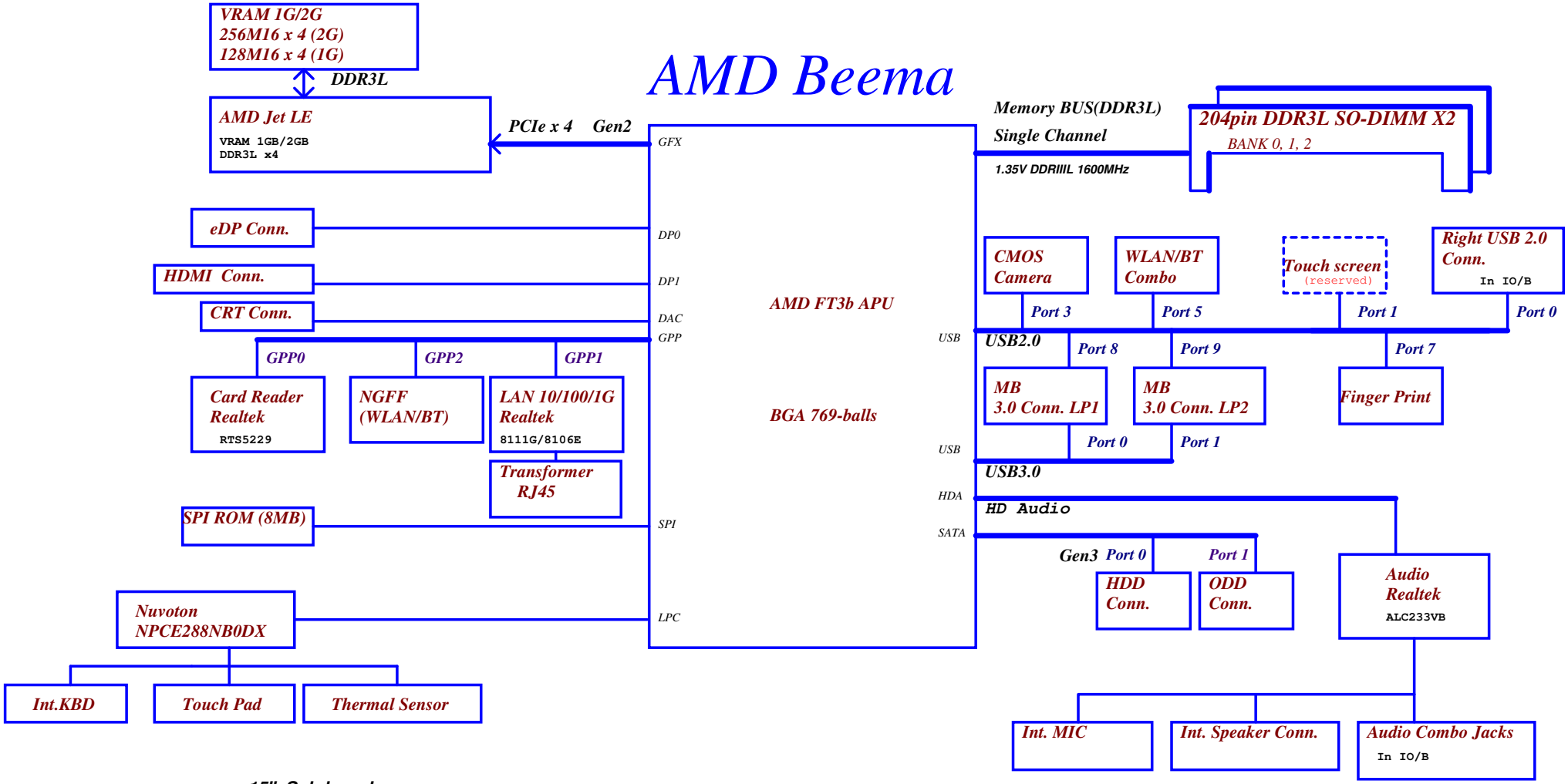
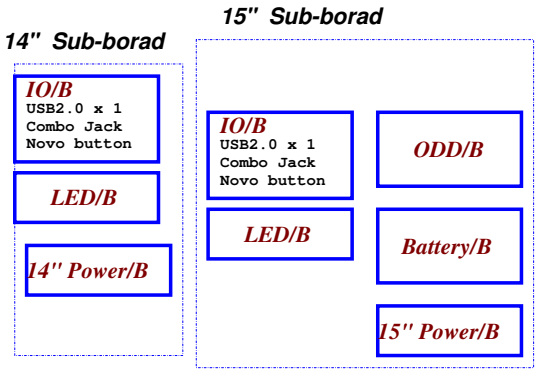
AMD Beema





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Title: Block Diagram

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VGS	1.35V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
R1562	100K +/- 5%

Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

USB OC MAPPING

OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

BOM Structure Table

BOM Structure	BTO Item
45@	for HDMI Logo
14@	for 14" componect
15@	for 15" componect
B5@	15W 2.4GHz BGA APU
B4@	15W 1.8GHz BGA APU
B3@	15W 1.5GHz BGA APU
B2@	10W 1.5GHz BGA APU
B1@	10W 1.35GHz BGA APU
UMA@	UMA part
PX@	Common VGA circuit
JET@	Jet LE GPU
TOPAZ@	Topaz XT GPU
CMOS@	CMOS Camera part
HDMI@	HDMI part
8106ELDO@	Realtek RTL8106E with LDO mode
8106ESW@	Realtek RTL8106E with SWR mode
8111GLDO@	Realtek RTL8111G with LDO mode
8111GSW@	Realtek RTL8111G with SWR mode
TS@	Touch Screen
ZODD@	Zero Power ODD part
NOZODD@	Non-Zero Power ODD part
CHG@	USB Charger function
NOCHG@	Non-USB Charger function
FHD@	Full HD Panel
DR@	VRAM Dual Rank
SR@	VRAM Single Rank
USB2@	USB 2.0
USB3@	USB 3.0
233VB@	Realtek ALC233-VB Audio IC
ME@	ME part
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
GIGAEMIP@	EMI Un pop for LAN GIGA function
@	Unpop

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	288N +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	288N +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

APU PCIE PORT LIST

Port	Device
0	Card Reader
1	LAN
2	WLAN
3	

USB Port Table

USB 2.0	USB 3.0		Port	3 External USB Port
			0	Touch Screen
			1	RIGHT USB
			2	
			3	Camera
			4	
			5	WLAN/BT Combo
			6	
			7	Finger Print
	XHCI	0	8	LEFT USB3.0
		1	9	LEFT USB3.0

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

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Jet LE VRAM STRAP

		X76@ Vendor UV5, UV6, UV7, UV8	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV21	X76@ R_pd RV24
1GBytes	ZZZ09 JH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ10 JM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
1GBytes	ZZZ11 JS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	2	0	1	0	4.53K	2K
2GBytes	ZZZ12 JH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ13 JS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ14 JM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
2GBytes	ZZZ08 JM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	6	1	1	0	3.4K	10K
1GBytes	ZZZ16 JM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	7	1	1	1	4.75K	NC

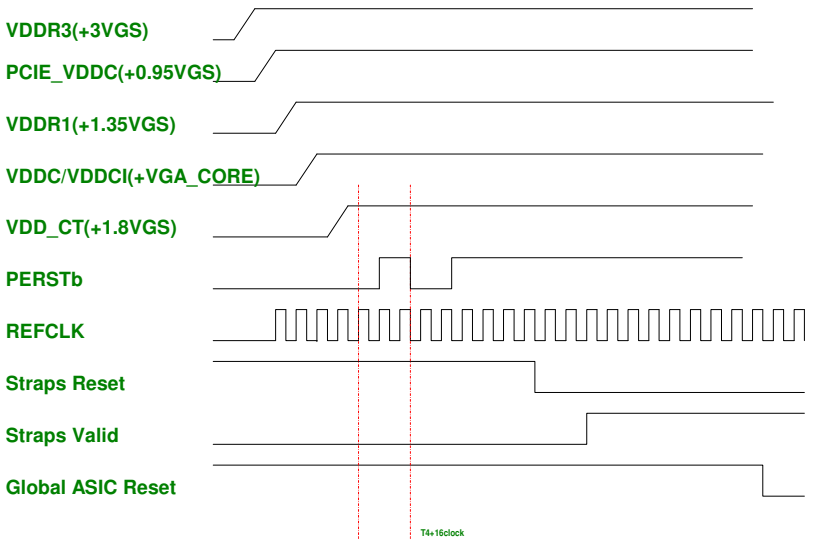
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Power-Up/Down Sequence

"Jet" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- It is recommended that the 3.3-V rail ramp up frist.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpressTM idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≦ 50mV/us)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



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HDMI & LVDS should be reverse in KABINI:
APU TX0 to Connector TX2 ; APU TX1 to Connector TX1
APU TX2 to Connector TX0 ; APU TX3 to Connector CLK

EDP use 2 Lane for FHD

MEMORY VREF

HDT+

PU +3VS

PU +1.8VS

PU +1.8VS + PD

PD

RP11, RP6 will @ when MP

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Title: FT3 DDR3/DISP/MISC//HDT

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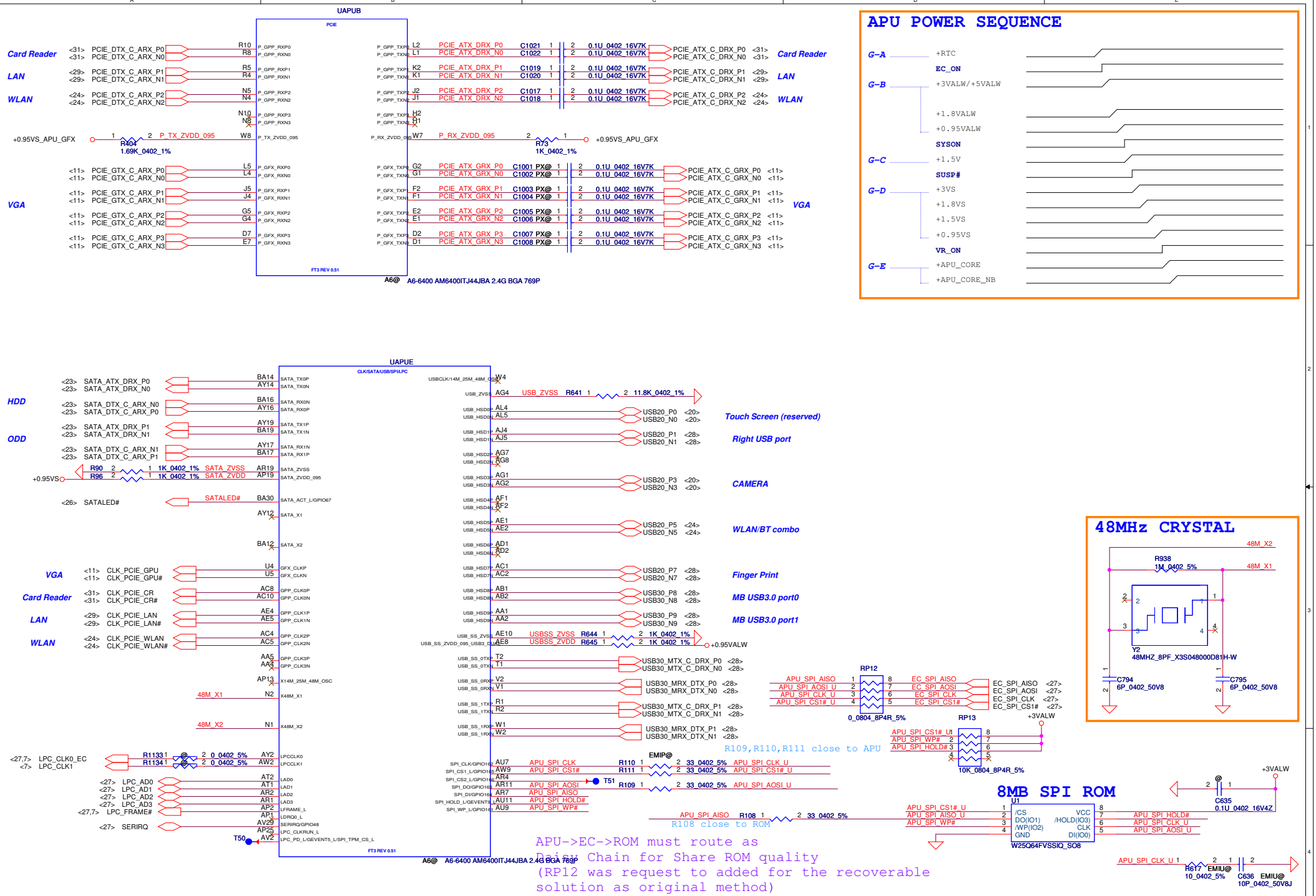

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Title	FT3 PCIE/SATA/CLK/USB/SPI		
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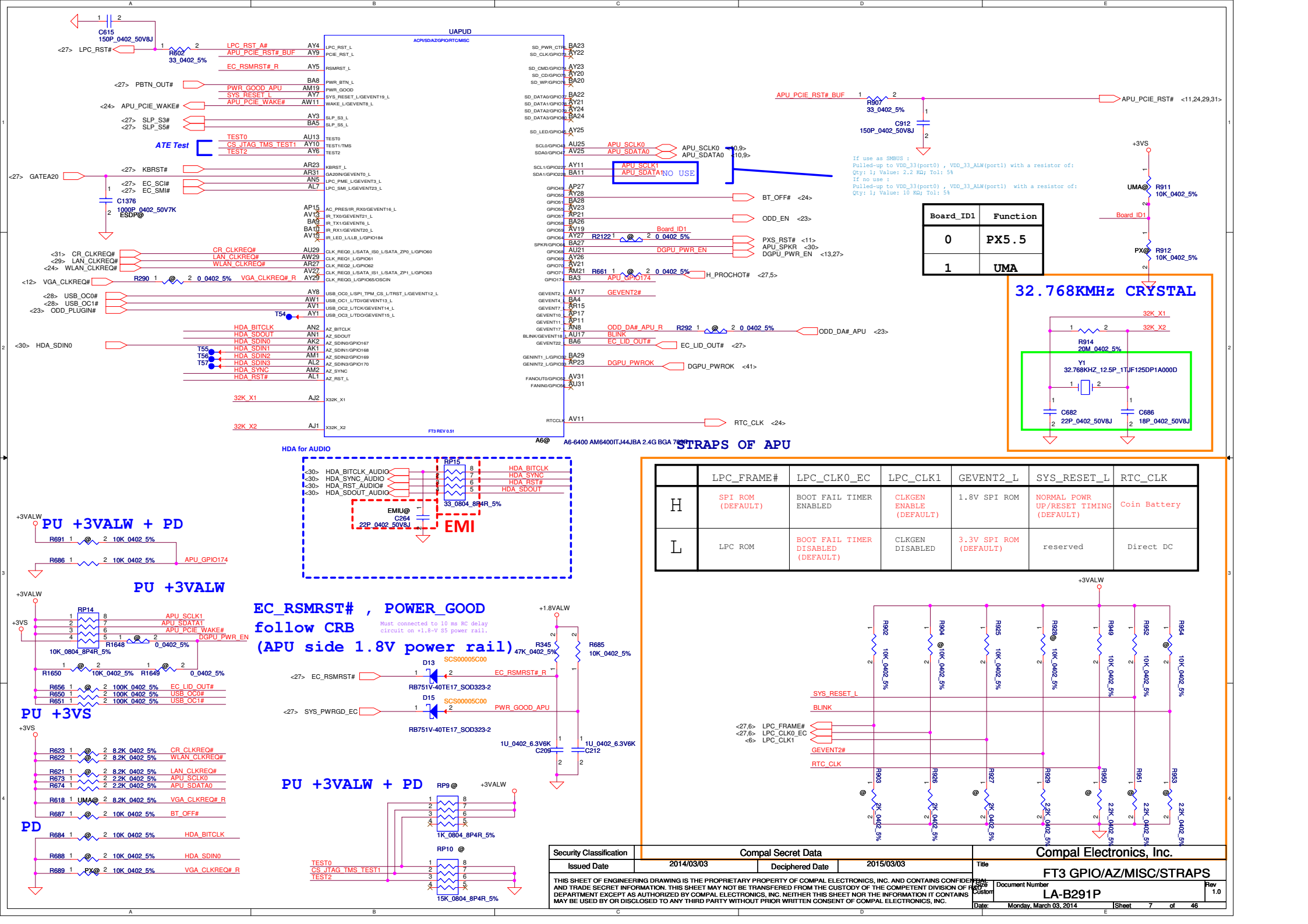

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	SYS_RESET_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)	Coin Battery
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	reserved	Direct DC

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Title	FT3 GPIO/AZ/MISC/STRAPS		
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CORE POWER OF APU

+APU_CORE — VDDCR_CPU

C1179 C1180 C1181 C1182 C1183 C1184 C1186 C1187 C1188 C1189 C1190
1U_0402_6.3V6K ×10, 180P_0402_50V8J

RTC OF APU

VDDBT_RTC_G — VDDBT_RTC_G

+RTCBATT_R — W=20mils — R93 10K_0402_5%

C1365 0.22U_0402_10V6K

CLRP1 @ SHORT PADS — Need OPEN

for Clear CMOS

+RTCBATT需過LDO轉1.5V, 20130930 added

+RTCBATT — U102 AP2138N-1.5TRG1_SOT23-3 (Vout, GND, Vin) — +RTCBATT_3V

C811 0.1U_0603_25V7K

C810 680P_0603_50VK

Need use+3.3V transfer to +1.5V LDO to APU side for Beema

INTEGRATED GPU POWER OF APU

+APU_CORE_NB — VDDCR_NB

C1200 C1201 C1202 C1192 C1191 C1193 C1194 C1197
1U_0402_6.3V6K ×7, 180P_0402_50V8J

+3VALW/+3VS OF APU

+3VS — C1249 1U_0402_6.3V6K; C1257 180P_0402_50V8J; C1252 C1253 1U_0402_6.3V6K

VDD_33 — VDD_33_ALW

+3VALW — +3VALW_APU — R582 0_0603_5%

VDDIO_AZ_ALW
(Could be S0 or S5 power rail)

+1.35V — VDDIO_MEM_S — PLANE SPLIT

C824 C825 C949 C823 C826 C827 C828 C829 C831 C830 C832 C1211 C1210 C1208 C1207 C1230 C1231 C1258 C1259 C1372 C1373
10U_0603_6.3V6M ×2, 1U_0402_16V7K ×9, 180P_0402_50V8J ×8, 0.1U_0402_16V7K_ESD@ ×2

+1.5VS — C1161 4.7U_0603_6.3V6K; C1255 C1254 C1255 C1256 1U_0402_6.3V6K ×4, 180P_0402_50V8J

+0.95VALW/+0.95VS OF APU

VDD_095_GFX

+0.95VS — VDD_095 — L22 FBMA-L11-201209-121LMA50T_0805 — +0.95VS_APU_GFX

C1198 C1199 C1205 C1204 C1206 C1250 C1213 C1203
10U_0603_6.3V6M ×2, 1U_0402_6.3V6K ×5, 180P_0402_50V8J

+0.95VALW

C1214 C1221 C1218
1U_0402_6.3V6K ×2, 180P_0402_50V8J

C1216 C1217 C1219 C1222
1U_0402_6.3V6K ×3, 180P_0402_50V8J

VDD_095_USB3_DUAL — VDD_095_ALW

+1.8VALW/+1.8VS OF APU

+1.8VS — VDD_18

C1236 C1237 C1238 C1239 C1240 C1233
10U_0603_6.3V6M ×2, 1U_0402_6.3V6K ×4, 180P_0402_50V8J

+1.8VALW

C1244 C1250 C1246 C1245
1U_0402_6.3V6K ×3, 180P_0402_50V8J

VDD_18_ALW

TEMPINRETUNE — R131 KABINI@ 0_0402_5%

UAPUF (POWER)

+1.35V — VDDIO_MEM_S_1 … VDDIO_MEM_S_23 (J35, L32, L37, N35, R31, R37, U32, U35, W31, W32, W37, AA31, AA35, AC32, AC37, AE31, AE35, AG32, AG37, AJ35, AL32, AL37, AR35)

+APU_CORE — VDDCR_CPU_1 … VDDCR_CPU_26 (L21, L23, L25, L27, L29, N21, N23, N27, R21, R23, R27, U21, U23, U27, W21, W23, W27, AA21, AA23, AA27, AC21, AC23, AC27, AE21, AE23, AE27)

+APU_CORE_NB — VDDCR_NB_1 … VDDCR_NB_21 (L13, L17, N11, N13, N17, R11, R13, R17, U13, U17, W13, W17, AA13, AA17, AC13, AC17, AE15, AE17, AE19, AG17, AG21)

+1.5VS — AL10 VDDIO_AZ_ALW_1, AL11 VDDIO_AZ_ALW_2

+1.8VALW — B1 VDD_18_ALW_1, B2 VDD_18_ALW_2

VDD_18_1 … VDD_18_4 (A2, A3, B3, C3) — +1.8VS

+3VALW_APU — AL13 VDD_33_ALW_1, AM13 VDD_33_ALW_2

VDD_33_1, VDD_33_2 (AM15, AM17) — +3VS

+0.95VALW — AR5 VDD_095_USB3_DUAL_1, AU4 VDD_095_USB3_DUAL_2, AV7 VDD_095_USB3_DUAL_3, AW5 VDD_095_USB3_DUAL_4

VDD_095_1 … VDD_095_8 (AG23, AG27, AJ21, AJ27, AL21, AL23, AL27, AM23, AM25) — +0.95VS

+0.95VALW — AE11 VDD_095_ALW_1, AE13 VDD_095_ALW_2, AJ11 VDD_095_ALW_3, AJ13 VDD_095_ALW_4

VDD_095_GFX_1 … VDD_095_GFX_3 (U10, W10, AA10) — +0.95VS_APU_GFX

+RTCBATT_R — AN4 VDDBT_RTC_G

FT3 REV 0.51 — A6@ — A6-6400 AM6400ITJ44JBA 2.4G BGA 769P

UAPUG (GND)

A8 A13 A23 A31 A35 A39 B8 B13 B23 B31 B39 C1 C2 C5 C7 C9 C11 C13 C15 C17 C19 C21 C23 C25 C27 C29 C31 C33 C35 C37 C39 C41 D9 D11 D13 E3 E4 E9 E11 E13 E27 E31 E35 E38 E39 G3 G7 G11 G13 G15 G17 G21 G25 G29 G35 G37 G39 G41 H11 H13 H23 H31 J3 J7 J8 J39 K11 K13 K17 K19 K21 K23 K25 K27 K29 K31 L3 L7 L8 L10 L11 L15 L19 L31 L39 L41 M1 M2 N3 N7 N15 N19 N25 N29 N31 N39 P1 P2 R3 R7 R15 R19 R25 R29 R39 R41 U1 U2 U3 U7 U8 U11 U15 U19 U25 U29 U31 U39 W3 W5 W11 W15 W19 W25 — VSS_1 … VSS_187

FT3 REV 0.51 — A6@ — A6-6400 AM6400ITJ44JBA 2.4G BGA 769P

UAPUH (GND)

W29 W39 W41 Y1 Y2 AA3 AA7 AA8 AA11 AA15 AA19 AA25 AA29 AA39 AC3 AC7 AC11 AC15 AC19 AC25 AC29 AC31 AC39 AC41 AE3 AE7 AE25 AE29 AE32 AE39 AG3 AG5 AG10 AG11 AG13 AG15 AG19 AG25 AG29 AG31 AG39 AG41 AH1 AH2 AJ3 AJ7 AJ15 AJ17 AJ19 AJ23 AJ25 AJ29 AJ31 AJ32 AJ39 AL3 AL8 AL15 AL17 AL19 AL25 AL29 — VSS_125 … VSS_186

AL39 AL41 AM11 AM27 AM31 AN3 AN7 AN39 AP31 AR3 AR13 AR17 AR21 AR25 AR29 AR39 AR41 AU1 AU2 AU3 AU15 AU19 AU23 AU27 AU39 AV9 AW3 AW7 AW13 AW15 AW17 AW19 AW21 AW23 AW25 AW27 AW31 AW33 AW35 AW37 AW39 AY13 AY15 AY18 AY30 BA2 BA7 BA13 BA15 BA18 BA21 BA25 BA31 BA35 BA39 A15 AL31 AM29 — VSS_187 … VSS_242, VSSBG_DAC, VBUF, PSEN

FT3 REV 0.51 — A6@ — A6-6400 AM6400ITJ44JBA 2.4G BGA 769P

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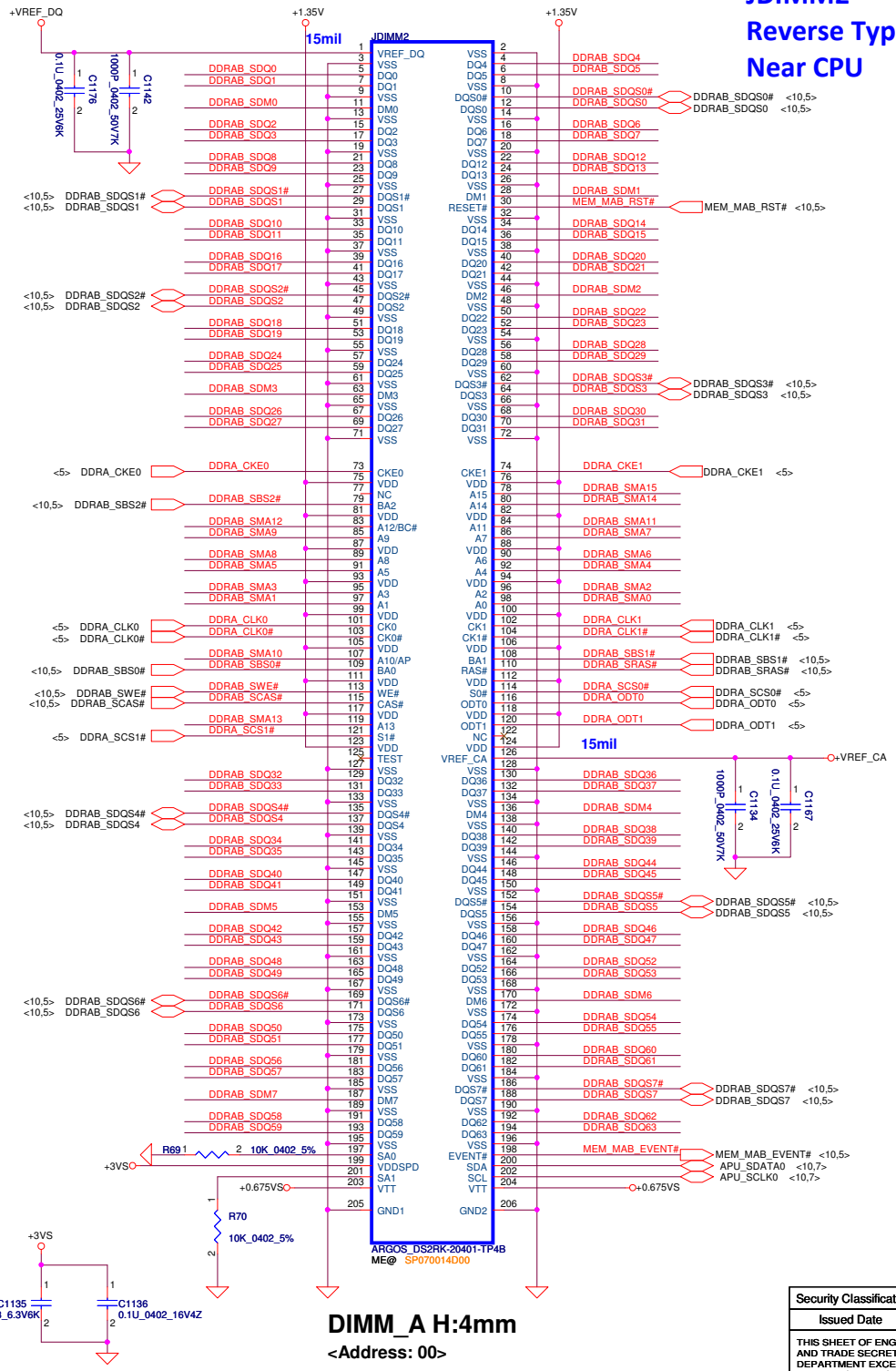
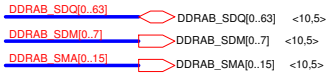
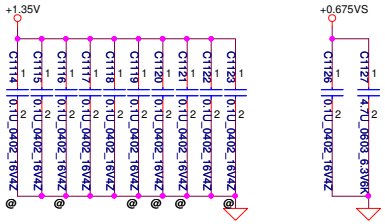
JDIMM2
Reverse Type
Near CPU

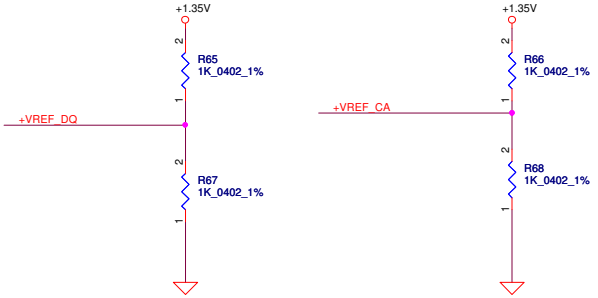




+1.35V/+0.675VS OF DIMM1



VREF for DIMM1,2



DIMM_A H:4mm

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Title: DDR3 SODIMM-I Socket

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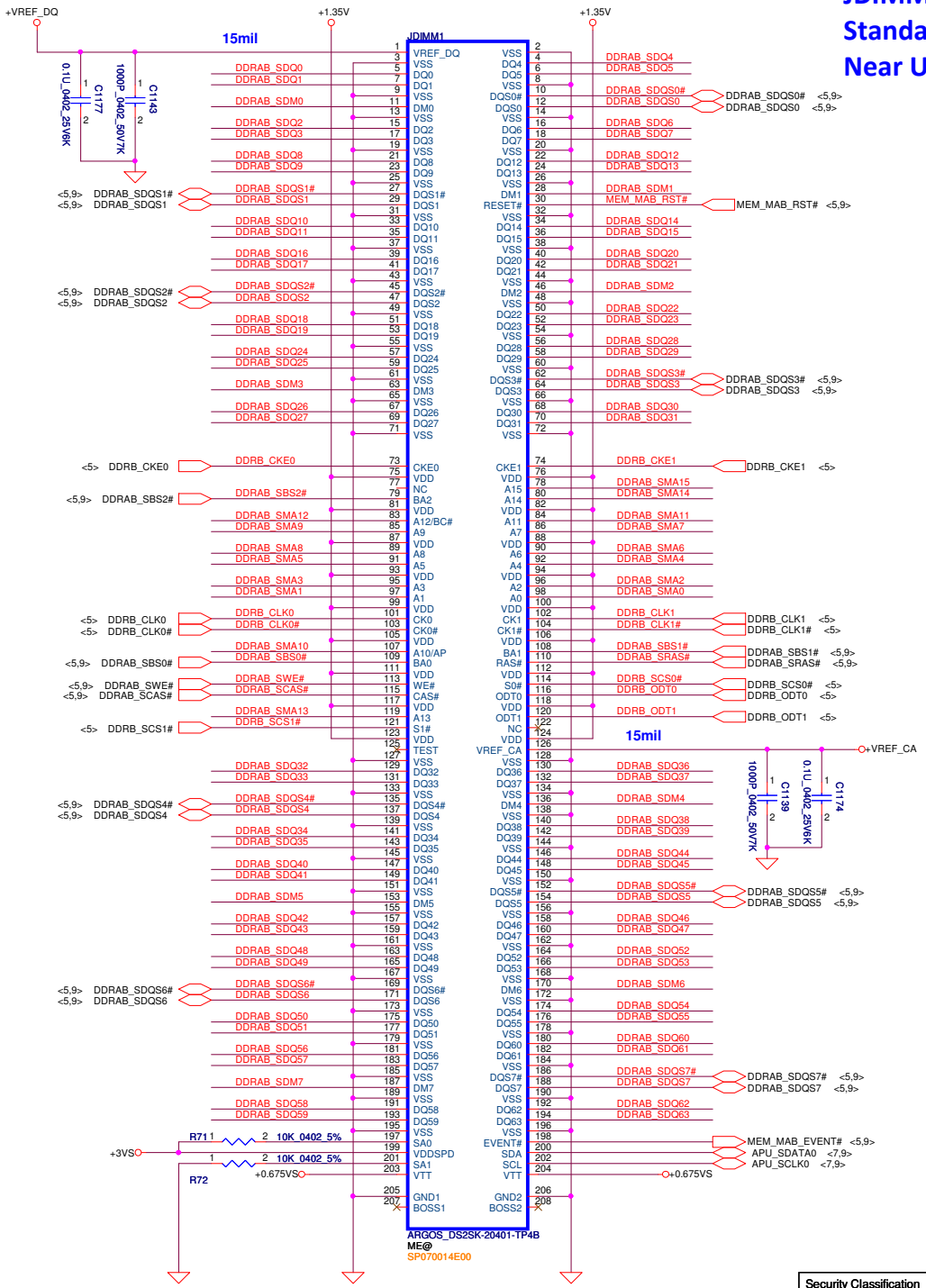
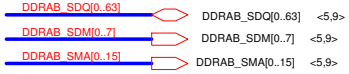
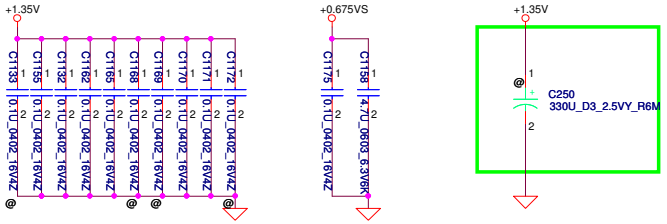
JDIMM1
Standard Type
Near User





+1.35V/+0.675VS OF DIMM2



DIMM_B H:4mm

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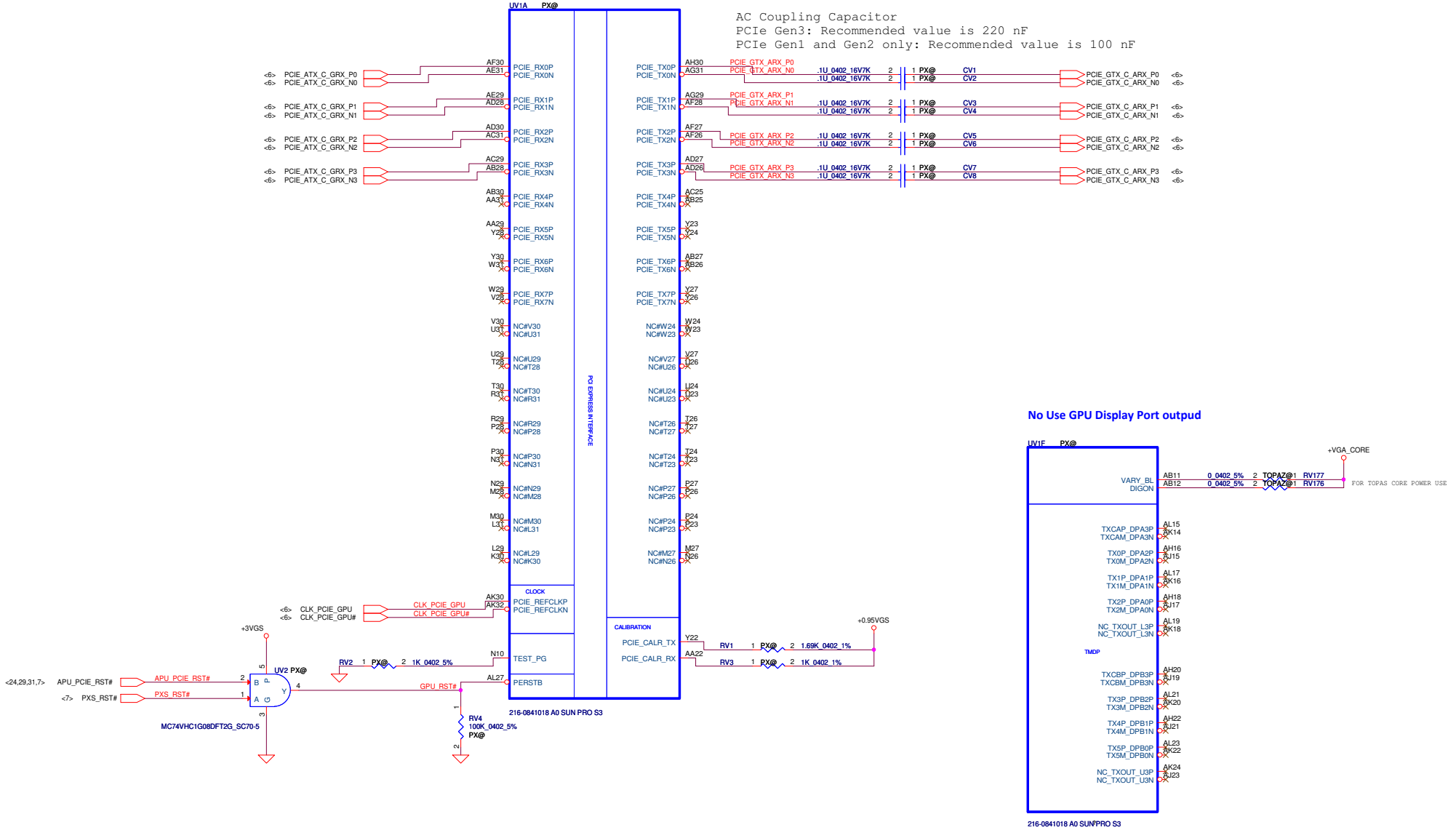

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL(1/5)_PCIE/DP

Size	Document Number	Rev
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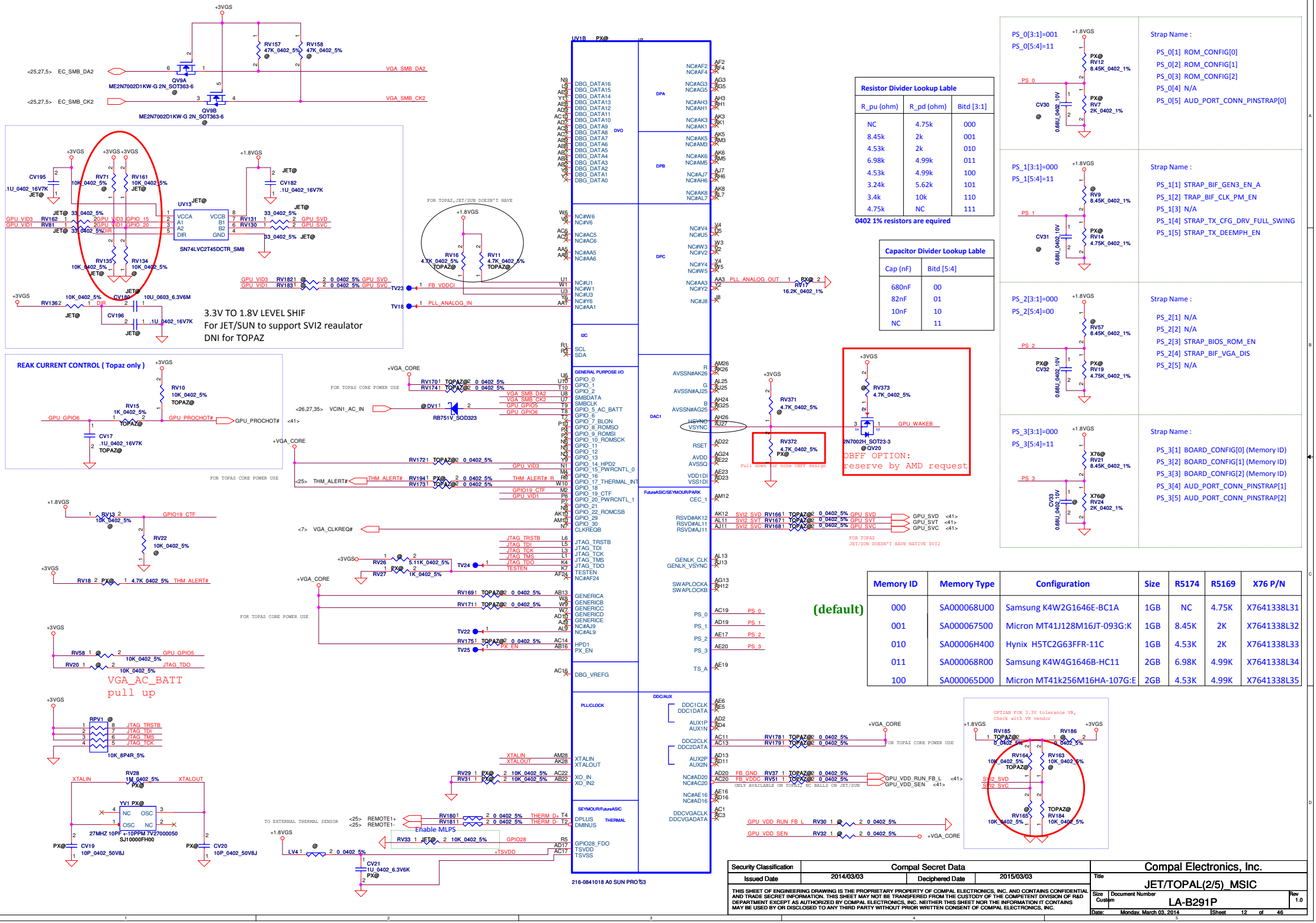

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB	NC	4.75K	X7641338L31
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB	8.45K	2K	X7641338L32
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7641338L33
011	SA000068R00	Samsung K4W4G1646B-HC11	2GB	6.98K	4.99K	X7641338L34
100	SA000065D00	Micron MT41k256M16HA-107G:E	2GB	4.53K	4.99K	X7641338L35

(default)

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL(2/5)_MSIC

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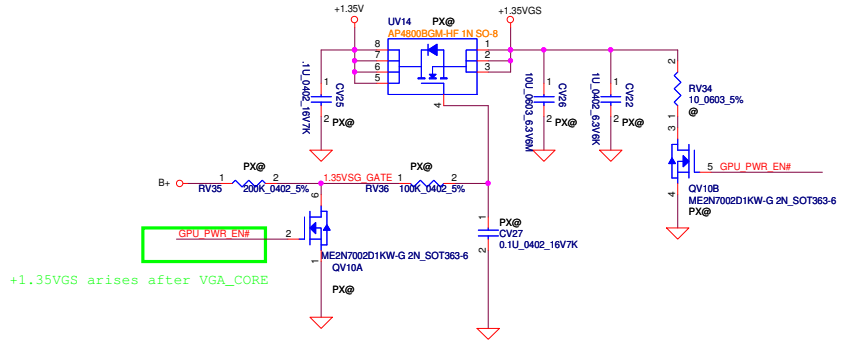
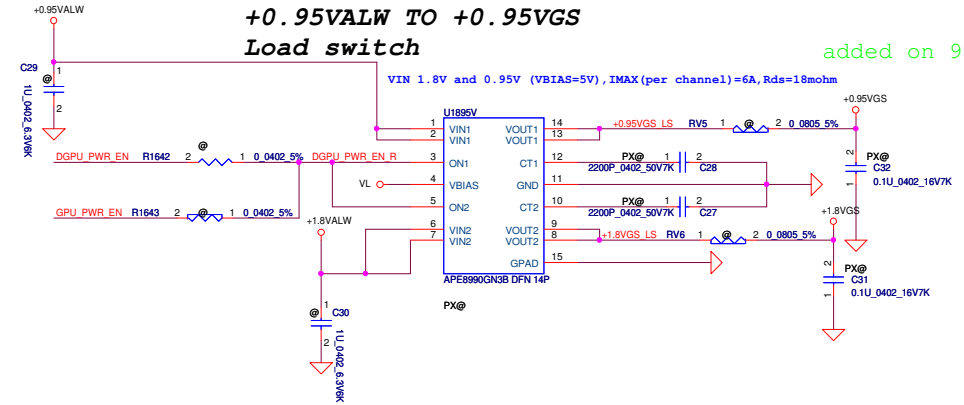
+1.35VS to +1.35VGS

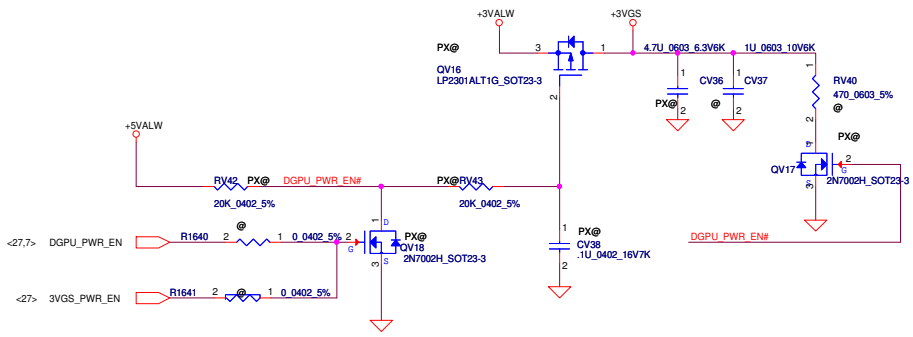


+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch

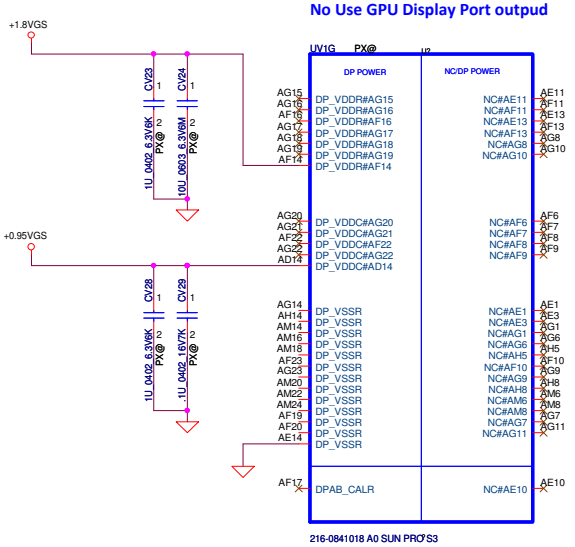
added on 9/28



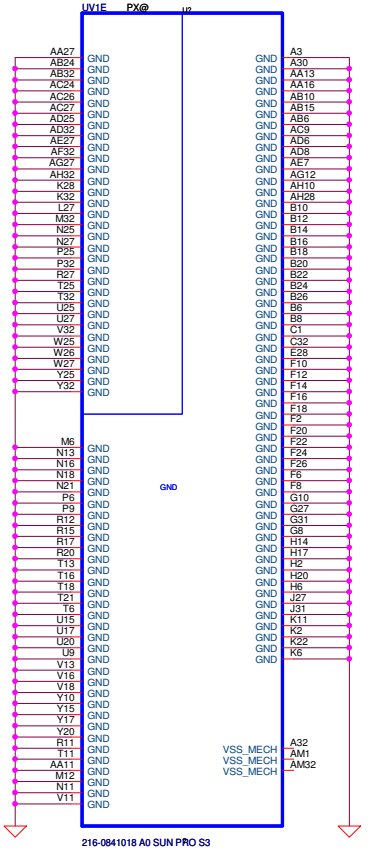
+3VS to +3VS_VGA



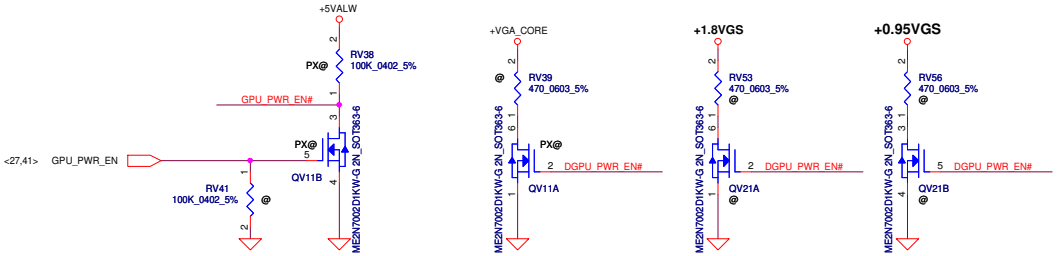
No Use GPU Display Port outpud



216-0841018 A0 SUN PRO S3



216-0841018 A0 SUN PRO S3



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL(3/5)_PWR/GND

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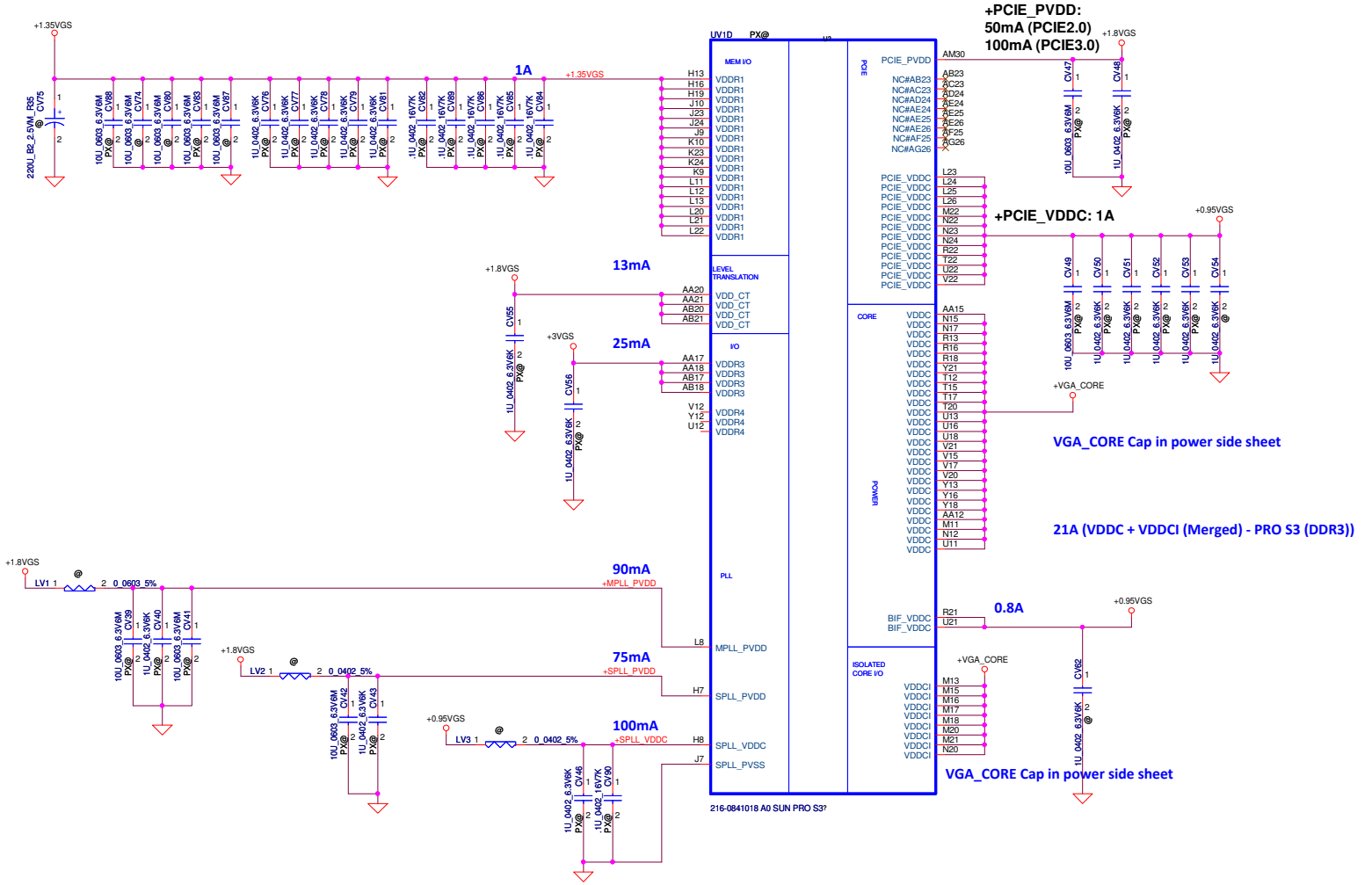
+VGA_CORE		10uF	2.2uF	1uF	0.1uF
VDDC	TBD	7	16	4	3
VDDCI	3.5A				

+0.95VGS		10uF	1uF	0.1uF
PCIE_VDDC	1A	1	5(1@)	0
BIF_VDDC	0.8A	0	1(1@)	0
SPLL_VDDC	100mA	0	1	1

+1.35VGS		10uF	1uF	0.1uF	0.01uF
VDDR1	1.5A	5(3@)	5	5	0

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	0
MPLL_PVDD	130mA	2	1	0
SPLL_PVDD	75mA	0	1	0
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	0	1	0
+TSVDD	13mA	0	1	0
+DP_VDDR		1	1	0
+DP_VDDC		0	1	1

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	1	0



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL(4/5)_PWR

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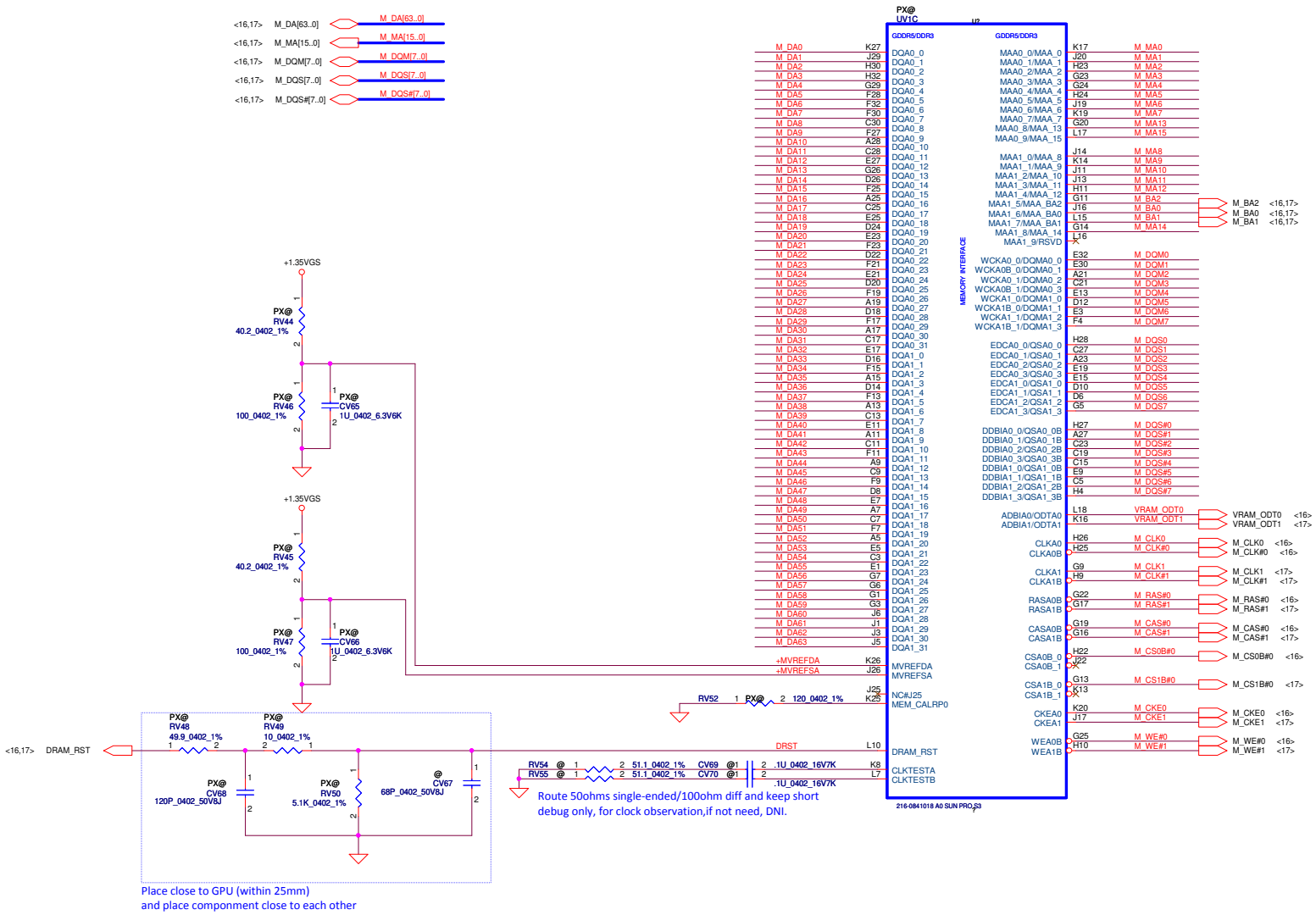

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL(5/5)_MEM

Size	Document Number	Rev
Custom	LA-B291P	1.0

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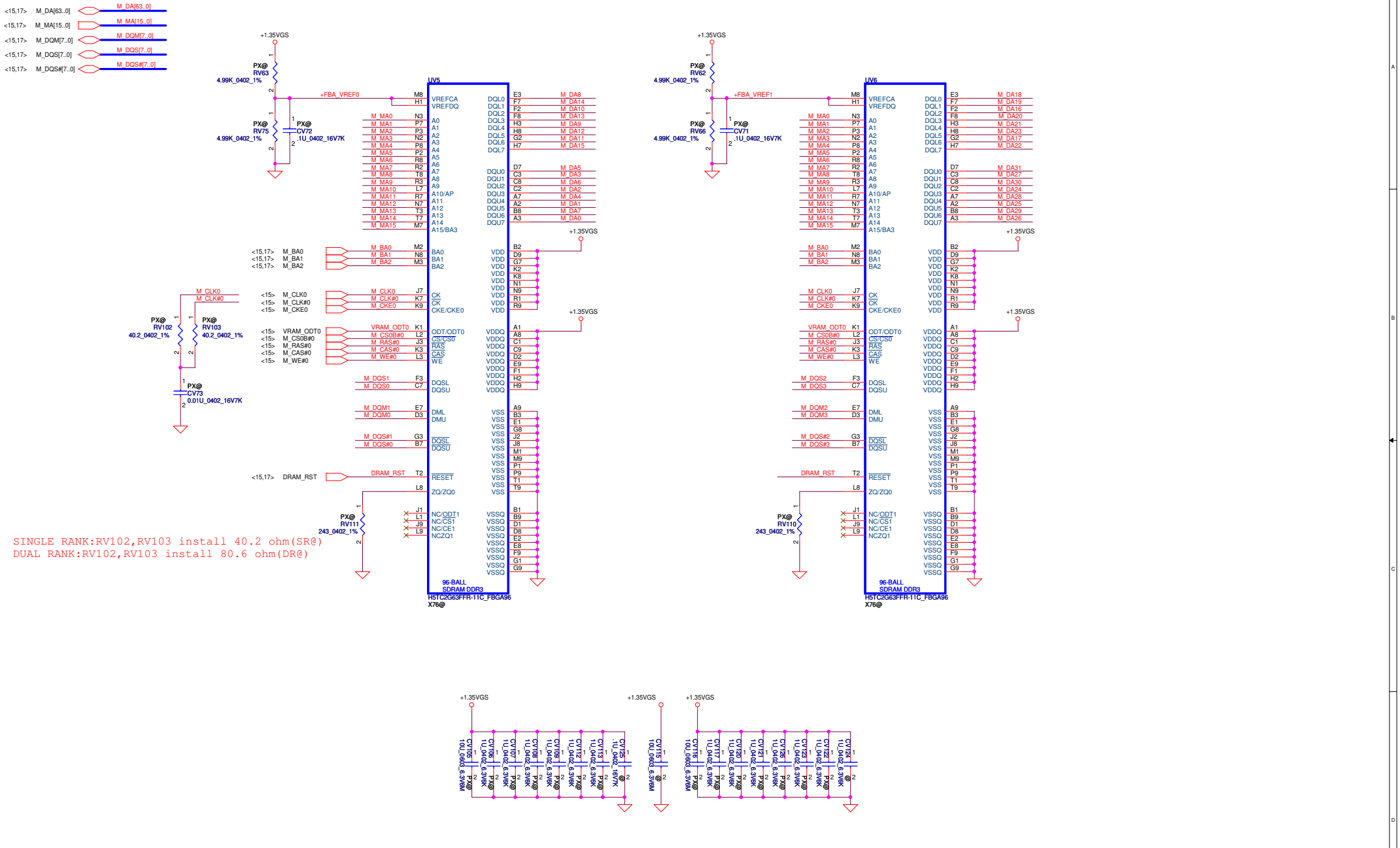
DDR3L Memory Channel Rank 0:A0



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL_DDR3L_A1 Rank 0

Size	Document Number	Rev
Custom	LA-B291P	1.0

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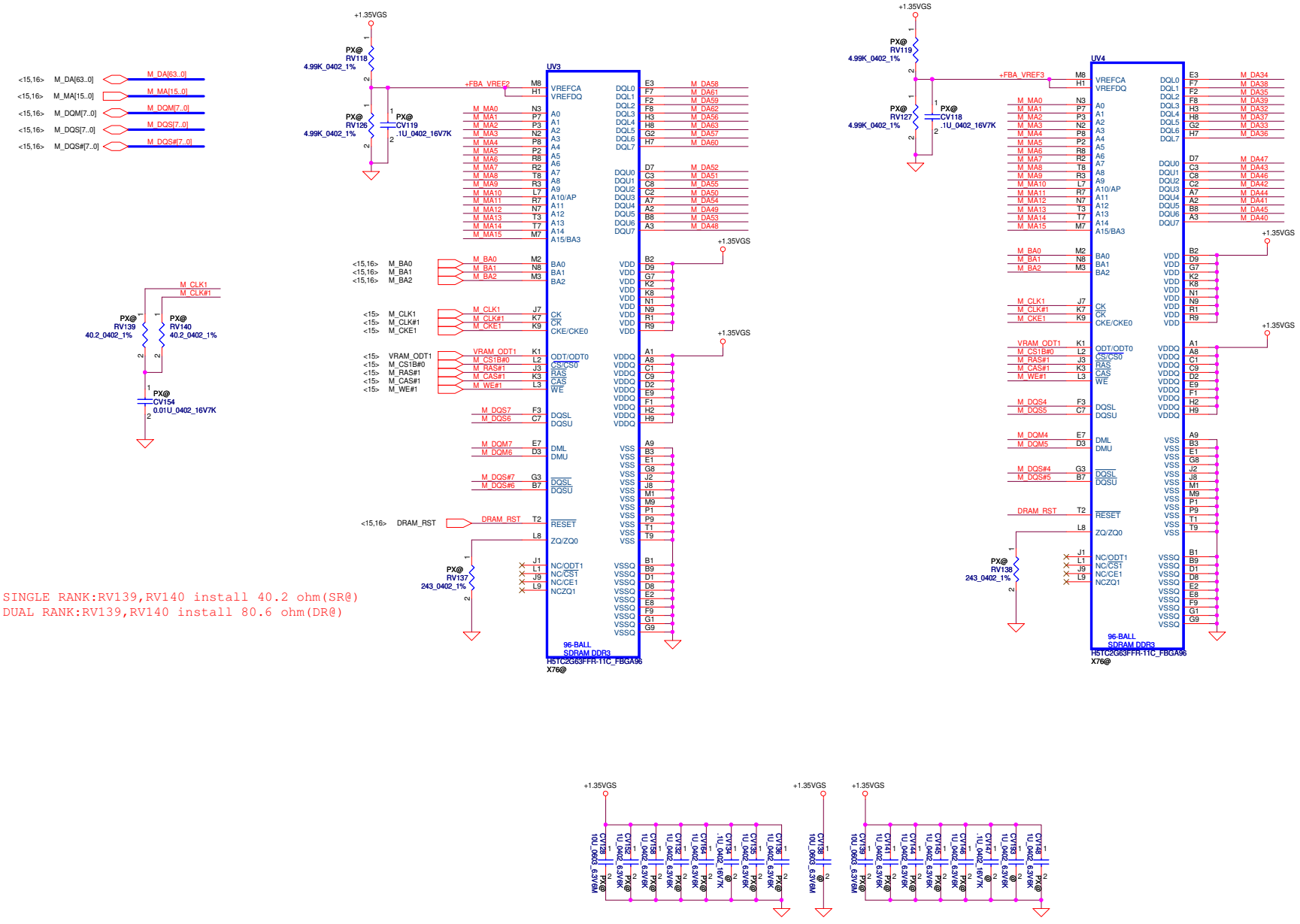
DDR3L Memory Channel Rank 0:A1



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: JET/TOPAL_DDR3L_A2 Rank 0

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Custom	LA-B291P	1.0

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Title	Reserved
Size	A
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Title	Reserved
Size	A
Document Number	LA-B291P
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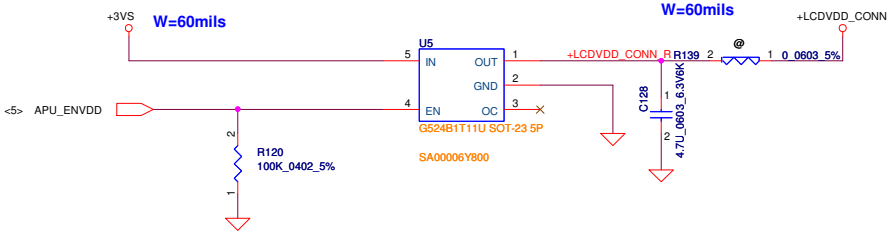
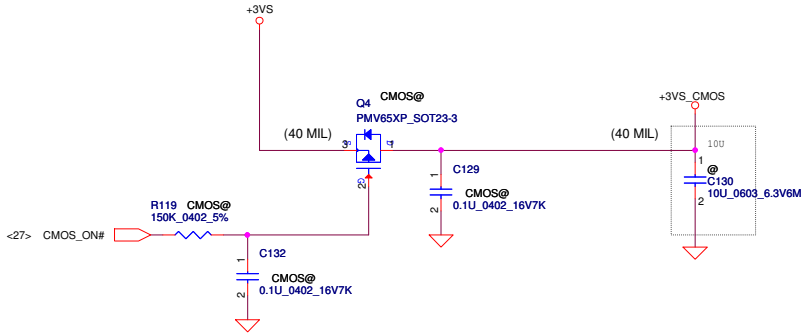
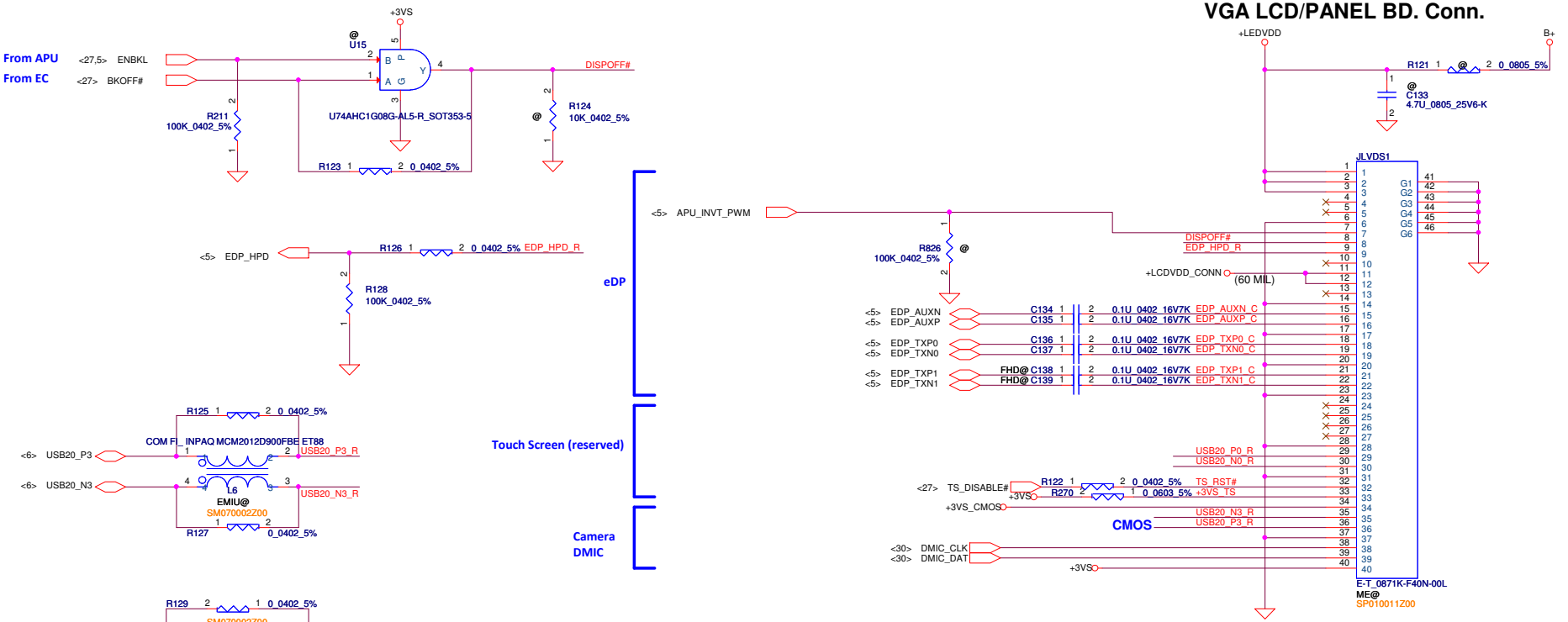
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title: EDP CONN / Camera			
Size: B	Document Number: LA-B291P		Rev: 1.0
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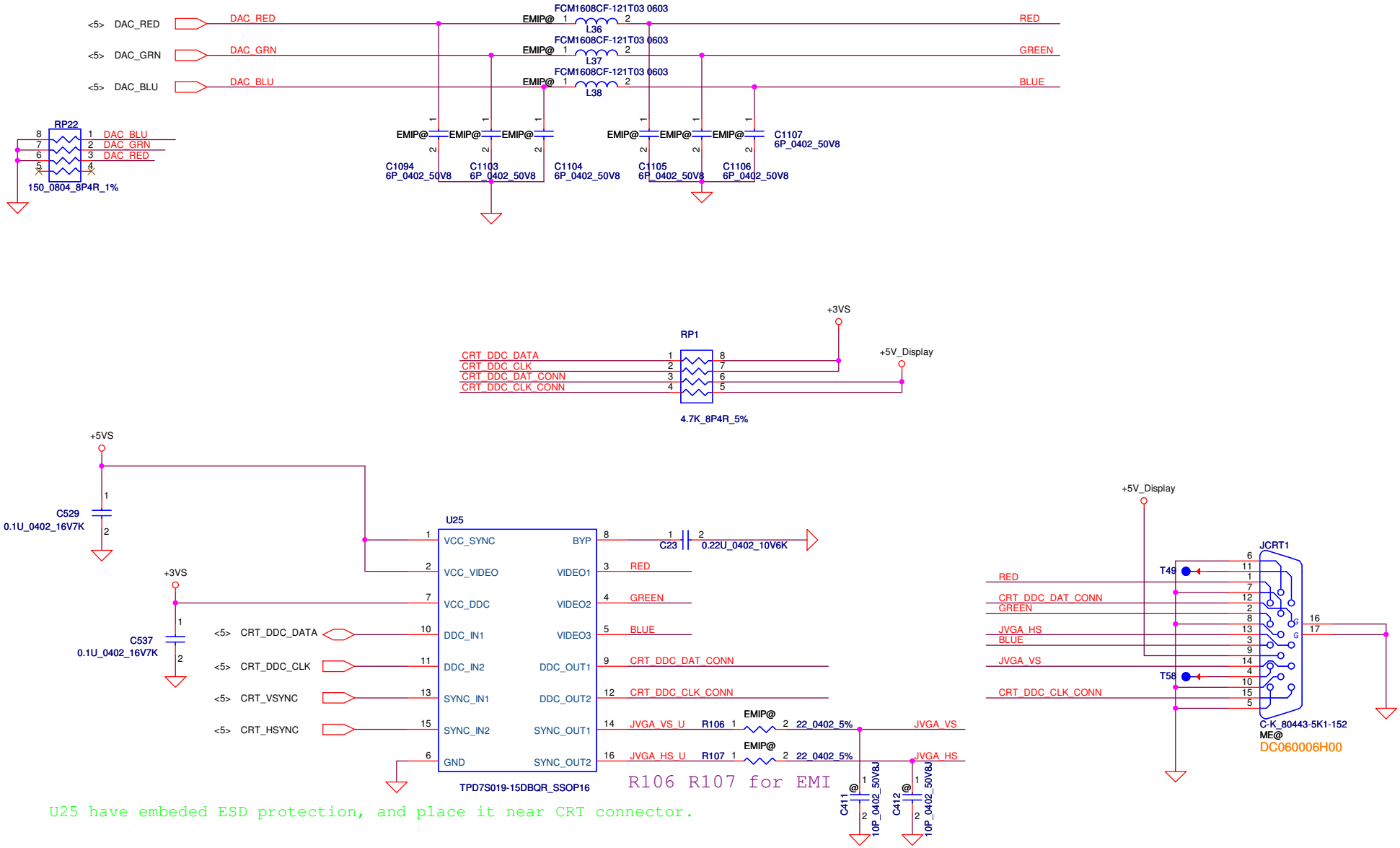
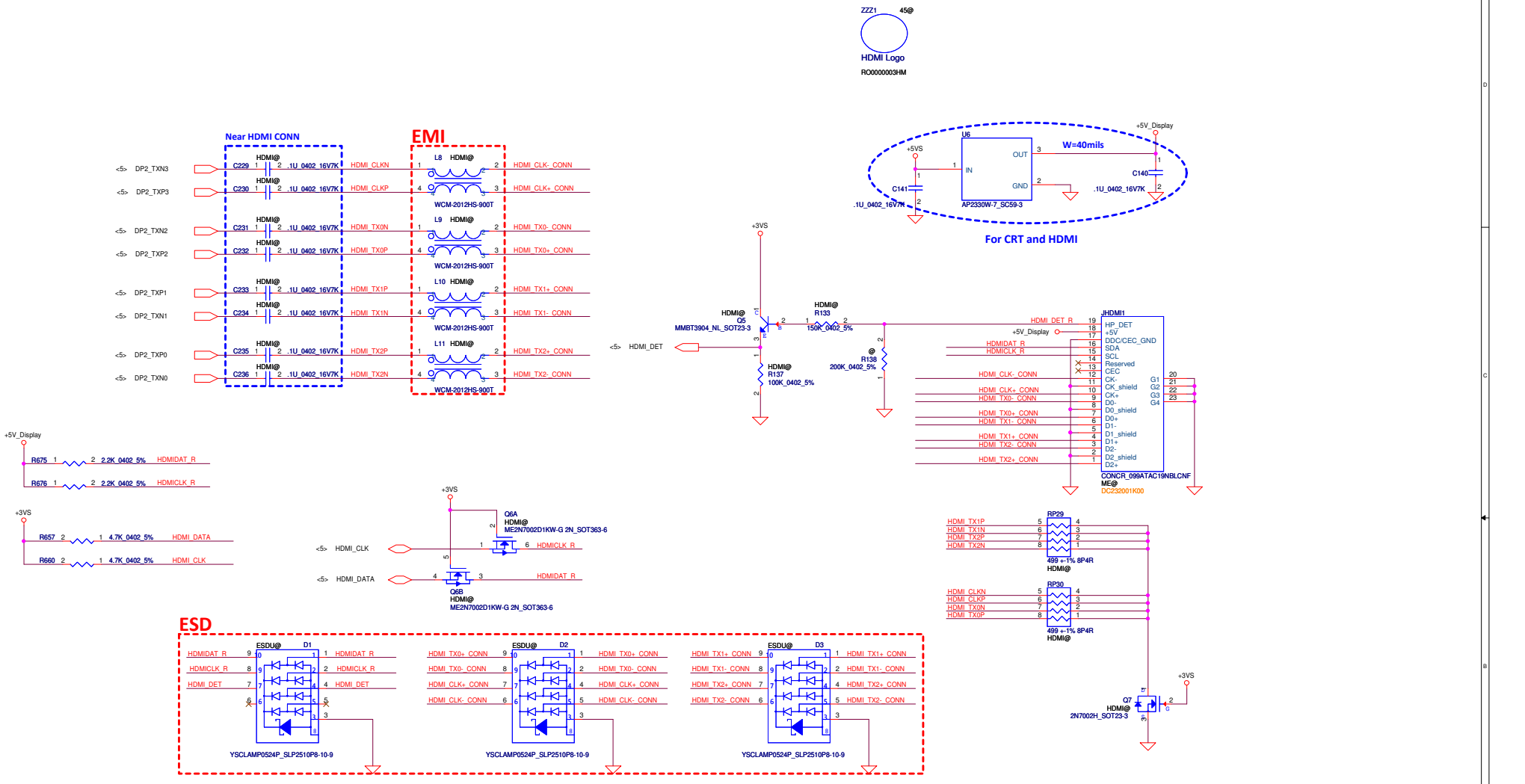


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Title	CRT CONN		
Size B	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 21 of 46		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	HDMI CONN		
Size C	Document Number LA-B291P		Rev 1.0
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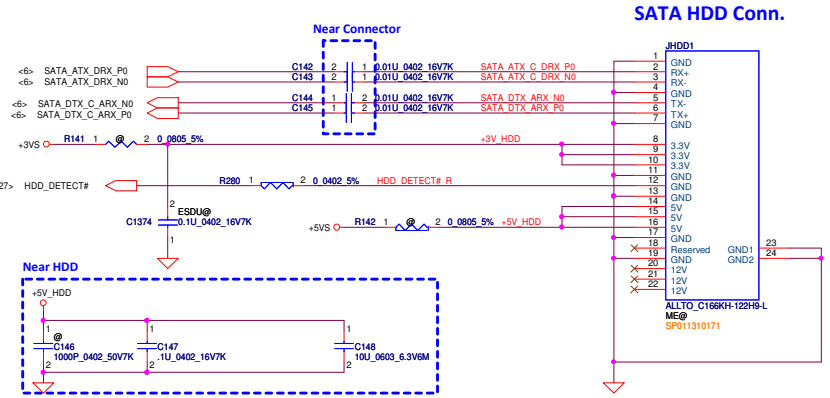
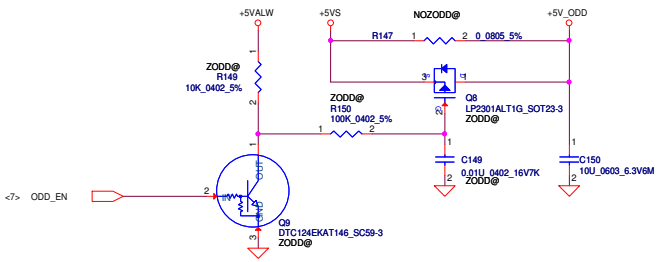
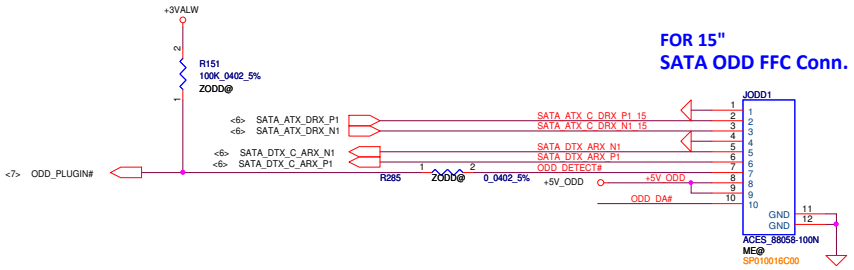
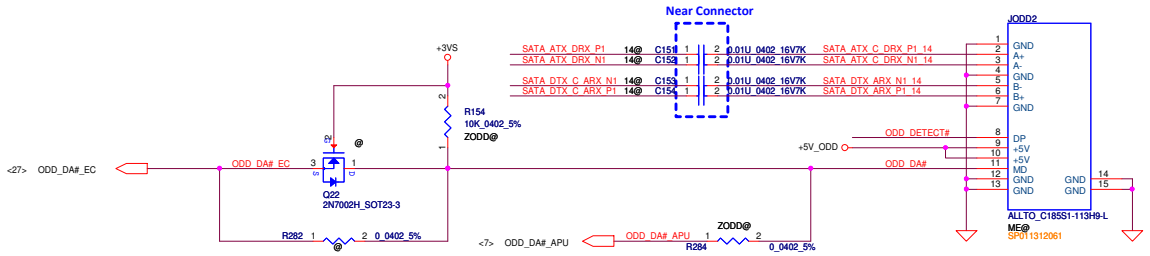
HDD



ODD







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date 2015/03/03	Title: HDD/ODD
Size: C	Document Number: LA-B291P		Rev: 1.0
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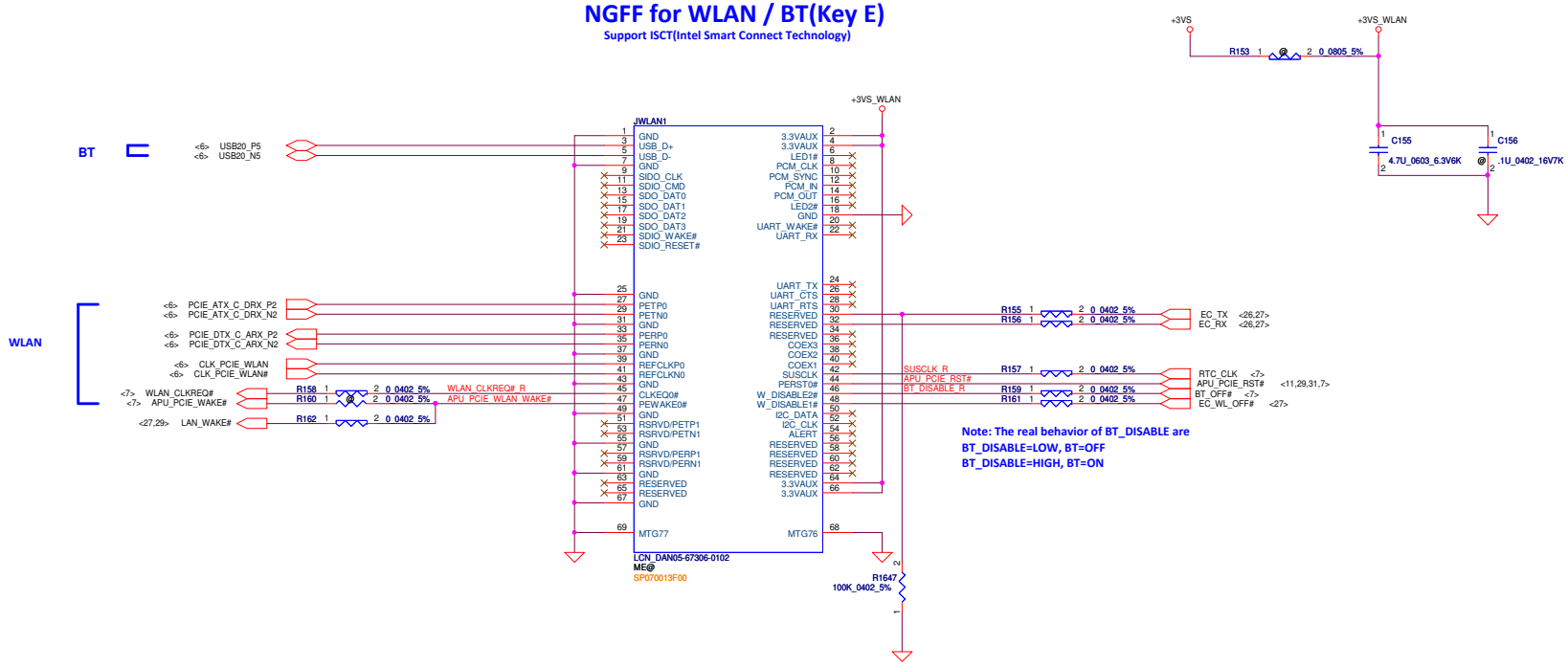
NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	NGFF WLAN/BT		
Size C	Document Number LA-B291P		Rev 1.0
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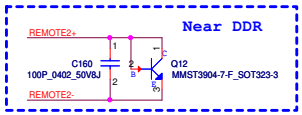
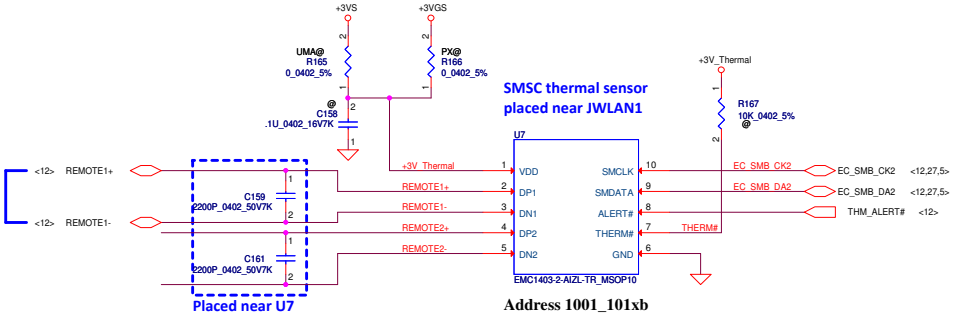
3 Channel

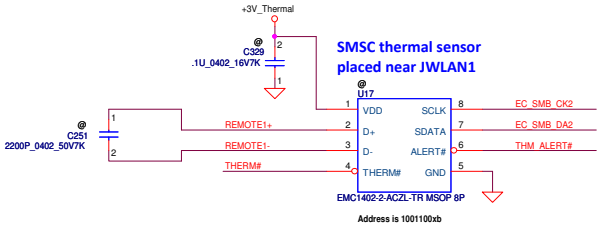


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

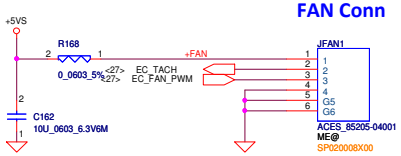
GPU

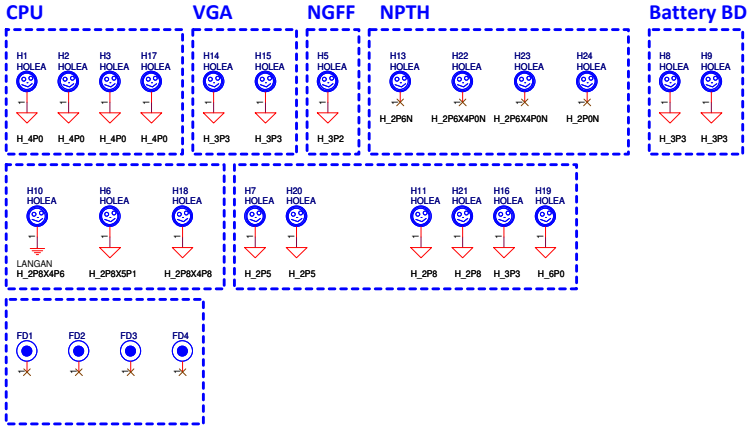


2 Channel

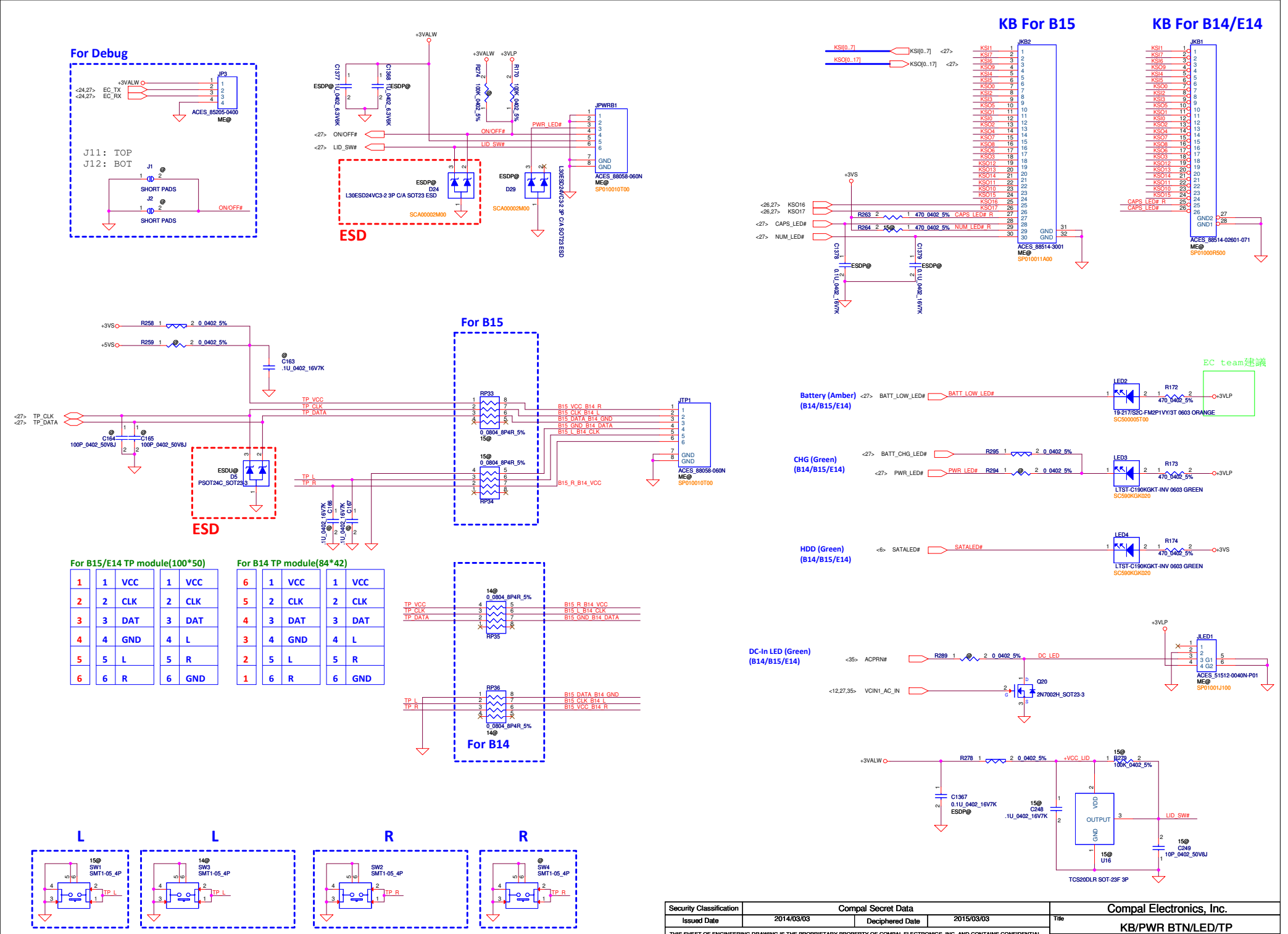


FAN Conn





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	EMC1403-2/FAN/Screw Hole		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 25 of 46		



1	1	VCC	1	VCC	6	1	VCC
2	2	CLK	2	CLK	5	2	CLK
3	3	DAT	3	DAT	4	3	DAT
4	4	GND	4	L	3	4	GND
5	5	L	5	R	2	5	L
6	6	R	6	GND	1	6	R

Security Classification	Compal Secret Data	
Issued Date	2014/03/03	Deciphered Date 2015/03/03

Compal Electronics, Inc.

Title: KB/PWR BTN/LED/TP

Size	Document Number	Rev
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Vcc	3.3V +/- 5%				
R1562	100K +/- 5%				
Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

NPCE288NB0DX_LQFP128_14X14
Part Number = SA000079Y00

For GPU

ESD

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.

Title: EC-Nuvoton 288N

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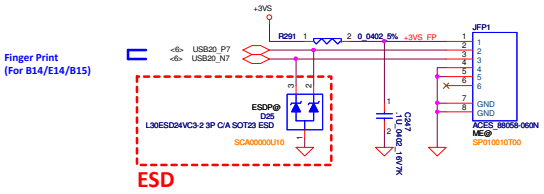
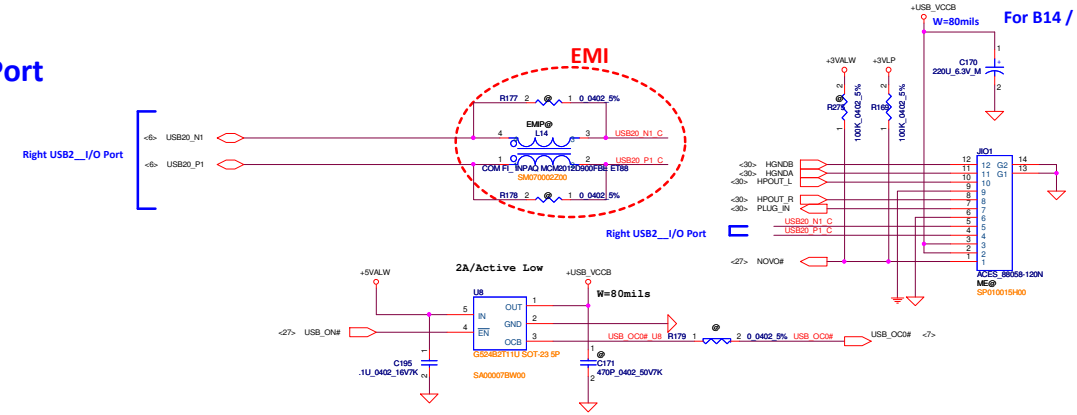
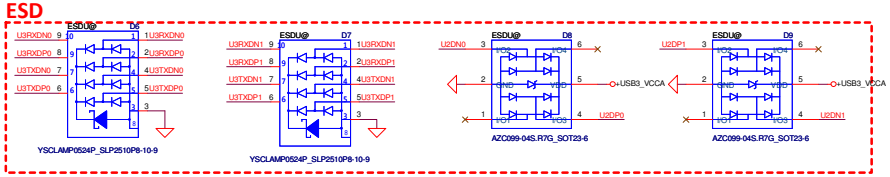
Finger Print



USB2.0_Port

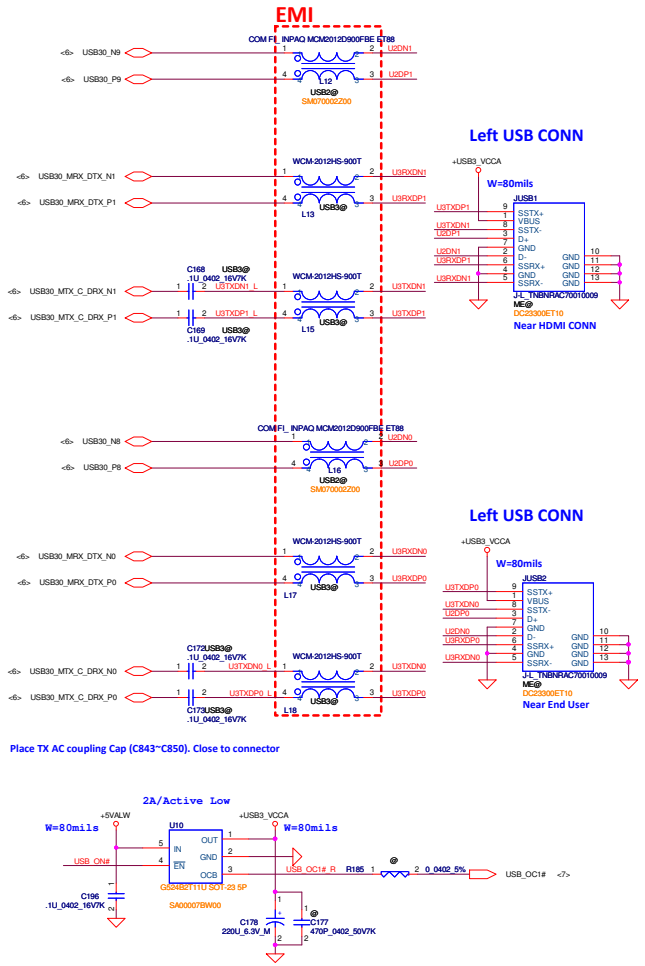


ESD

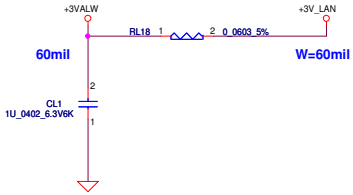


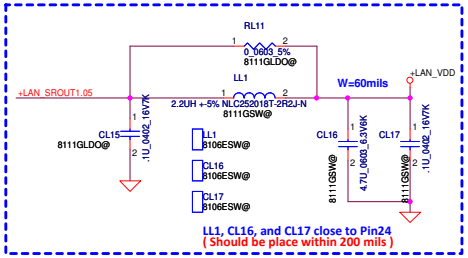
ESD protection needs to be placed near connector side

USB3.0_Port



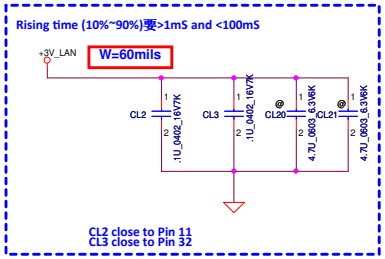
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03
Title	USB Port/FP		
Size	Document Number		Rev
Custom	LA-B291P		1.0
Date:	Monday, March 03, 2014	Sheet	28 of 46

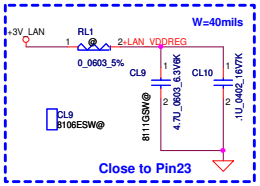


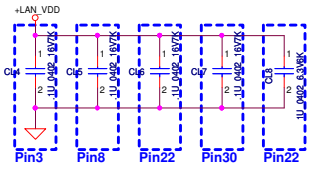


		1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005V700	RTL8111G	LDO	X	X	X	O	O
	~~RTL8111G~~	~~External~~	~~X~~	~~X~~	~~X~~	~~X~~	~~O~~
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA00006SY00	RTL8106E	LDO	X	X	X	X	X

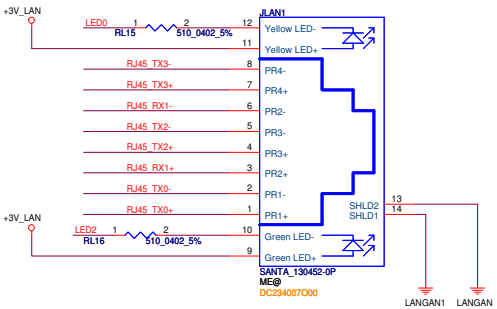
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.



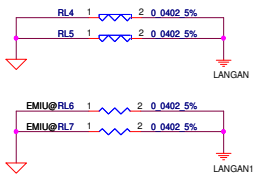


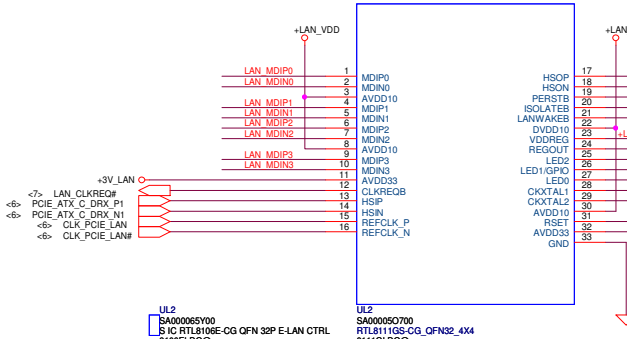


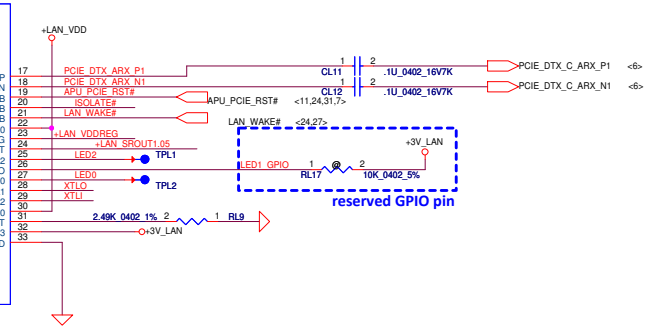
RJ-45 CONN.

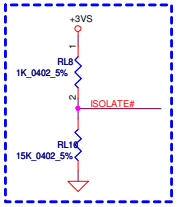


EMI





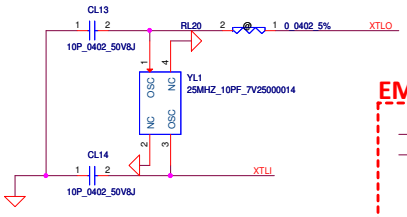




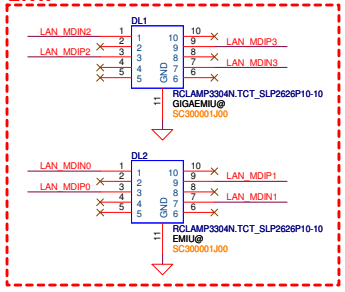
UL2
SA00006S910
S IC RTL8106E-CG QFN 32P E-LAN CTRL
8106ELDO@

UL2
SA00006N910
S IC RTL8106EUL-CG QFN 32P E-LAN CTRL
8106ESW@

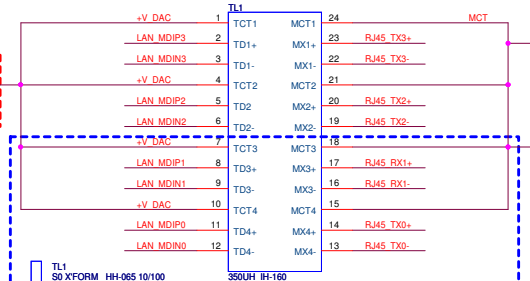
UL2
SA00006ML10
S IC RTL8111GUL-CG QFN 32P E-LAN CTRL
8111GSW@



EMI



EMI



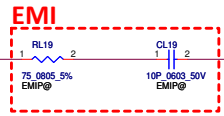
TL1
S0 XFORM_ HH-065 10/100
8106ELDO@

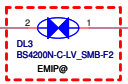
FOR 10/100 data transferring 2013/08/27

TL1
S0 XFORM_ HH-065 10/100
8106ESW@

TL1
S0 XFORM_ 350UH_IH-160
8111GSW@

EMI





EMI

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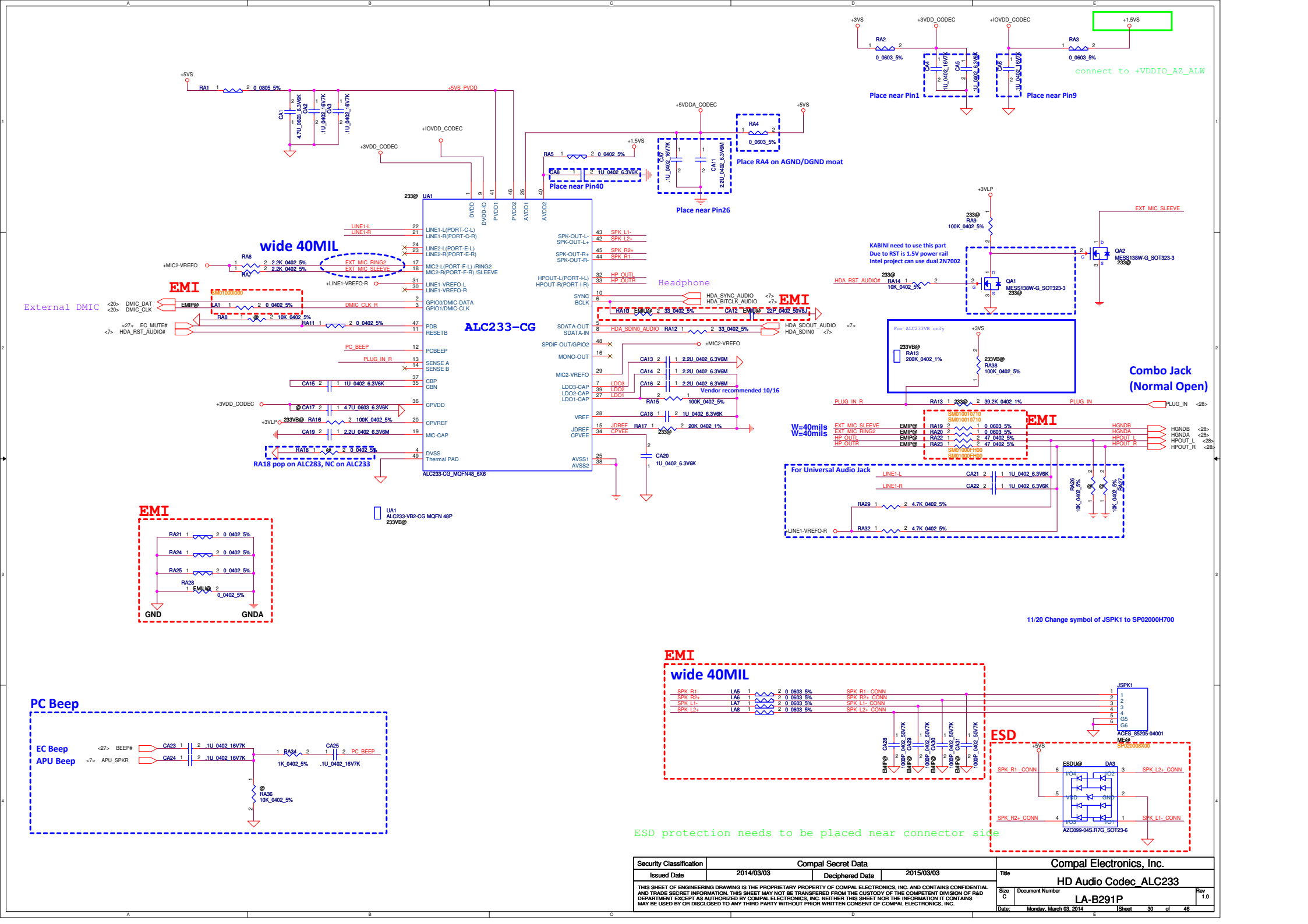
Title	LAN_RTL8111G/RTL8106E		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014		Sheet 29 of 46	


+3VS
+3VDD_CODEC
+IOVDD_CODEC
+1.5VS
RA2 0_0603_5%
RA3 0_0603_5%
CA4 1U_0402_16V7K
CA5 1U_0402_6.3V6K
CA6 1U_0402_16V7K
connect to +VDDIO_AZ_ALW
Place near Pin1
Place near Pin9
+5VS
RA1 0_0805_5%
+5VS_PVDD
CA1 4.7U_0603_6.3V6K
CA2 .1U_0402_16V7K
CA3 .1U_0402_16V7K
+5VDDA_CODEC
RA4 0_0603_5%
RA5 0_0402_5%
CA8 1U_0402_6.3V6K
CA9 .1U_0402_16V7K
CA11 2.2U_0402_6.3V6M
Place RA4 on AGND/DGND moat
Place near Pin40
Place near Pin26
233@ UA1
DVDD
DVDD-IO
PVDD1
PVDD2
AVDD1
AVDD2
wide 40MIL
LINE1-L
LINE1-R
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
+MIC2-VREFO
RA6 2.2K_0402_5%
RA7 2.2K_0402_5%
EXT_MIC_RING2
EXT_MIC_SLEEVE
MIC2-L(PORT-F-L) /RING2
MIC2-R(PORT-F-R) /SLEEVE
+LINE1-VREFO-R
LINE1-VREFO-L
LINE1-VREFO-R
EMI
SM070000000
External DMIC
EMIP@
LA1 0_0402_5%
DMIC_DAT
DMIC_CLK
DMIC_CLK_R
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
RA8 @ 10K_0402_5%
RA11 0_0402_5%
EC_MUTE#
HDA_RST_AUDIO#
PDB
RESETB
ALC233-CG
PC_BEEP
PCBEEP
PLUG_IN_R
SENSE A
SENSE B
CA15 1U_0402_6.3V6K
CBP
CBN
+3VDD_CODEC
@CA17 4.7U_0603_6.3V6K
CPVDD
+3VLP
233VB@ RA16 100K_0402_5%
CPVREF
CA19 2.2U_0402_6.3V6M
MIC-CAP
RA18 @ 0_0402_5%
DVSS
Thermal PAD
RA18 pop on ALC283, NC on ALC233
ALC233-CG_MQFN48_6X6
SPK-OUT-L-
SPK-OUT-L+
SPK-OUT-R+
SPK-OUT-R-
SPK_L1-
SPK_L2+
SPK_R2+
SPK_R1-
HPOUT-L(PORT-I-L)
HPOUT-R(PORT-I-R)
HP_OUTL
HP_OUTR
Headphone
SYNC
BCLK
HDA_SYNC_AUDIO
HDA_BITCLK_AUDIO
EMI
RA10 EMIP@ 33_0402_5%
CA12 EMIP@ 22P_0402_50V8J
SDATA-OUT
SDATA-IN
HDA_SDOUT_AUDIO
HDA_SDIN0
HDA_SDIN0_AUDIO
RA12 33_0402_5%
SPDIF-OUT/GPIO2
+MIC2-VREFO
MONO-OUT
MIC2-VREFO
CA13 2.2U_0402_6.3V6M
CA14 2.2U_0402_6.3V6M
CA16 2.2U_0402_6.3V6M
Vendor recommended 10/16
LDO3-CAP
LDO2-CAP
LDO1-CAP
LDO3
LDO2
LDO1
RA15 100K_0402_5%
VREF
CA18 1U_0402_6.3V6K
JDREF
CPVEE
RA17 20K_0402_1%
CA20 1U_0402_6.3V6K
AVSS1
AVSS2
UA1
ALC233-VB2-CG MQFN 48P
233VB@
KABINI need to use this part
Due to RST is 1.5V power rail
Intel project can use dual 2N7002
+3VLP
233@ RA9 100K_0402_5%
EXT_MIC_SLEEVE
QA2 MESS138W-G_SOT323-3 233@
HDA_RST_AUDIO#
RA14 10K_0402_5%
QA1 MESS138W-G_SOT323-3 233@
For ALC233VB only
233VB@ RA13 200K_0402_1%
233VB@ RA38 100K_0402_5%
Combo Jack
(Normal Open)
PLUG_IN_R
RA13 39.2K_0402_1%
PLUG_IN
SM010010710
SM010010710
EMI
W=40mils
W=40mils
EXT_MIC_SLEEVE
EXT_MIC_RING2
HP_OUTL
HP_OUTR
RA19 0_0603_5%
RA20 0_0603_5%
RA22 47_0402_5%
RA23 47_0402_5%
SM070000FH00
SM070000FH00
HGNDB
HGNDA
HPOUT_L
HPOUT_R
For Universal Audio Jack
LINE1-L
LINE1-R
CA21 1U_0402_6.3V6K
CA22 1U_0402_6.3V6K
RA29 4.7K_0402_5%
RA32 4.7K_0402_5%
LINE1-VREFO-R
RA26 10K_0402_5%
RA27 10K_0402_5%
EMI
RA21 0_0402_5%
RA24 0_0402_5%
RA25 0_0402_5%
RA28 @ 0_0402_5%
GND
GNDA
11/20 Change symbol of JSPK1 to SP02000H700
EMI
wide 40MIL
SPK_R1-
SPK_R2+
SPK_L1-
SPK_L2+
LA5 0_0603_5%
LA6 0_0603_5%
LA7 0_0603_5%
LA8 0_0603_5%
SPK_R1- CONN
SPK_R2+ CONN
SPK_L1- CONN
SPK_L2+ CONN
CA28 1000P_0402_50V7K EMIP@
CA29 1000P_0402_50V7K EMIP@
CA30 1000P_0402_50V7K EMIP@
CA31 1000P_0402_50V7K EMIP@
JSPK1
ACES_85205-04001
ME@
SP02000BA00
ESD
ESDU@
DA3
AZC099-04S.R7G_SOT23-6
PC Beep
EC Beep
APU Beep
<27> BEEP#
<7> APU_SPKR
CA23 .1U_0402_16V7K
CA24 .1U_0402_16V7K
RA34 1K_0402_5%
CA25 .1U_0402_16V7K
PC_BEEP
@ RA36 10K_0402_5%
ESD protection needs to be placed near connector side
Security Classification
Compal Secret Data
Issued Date
2014/03/03
Deciphered Date
2015/03/03
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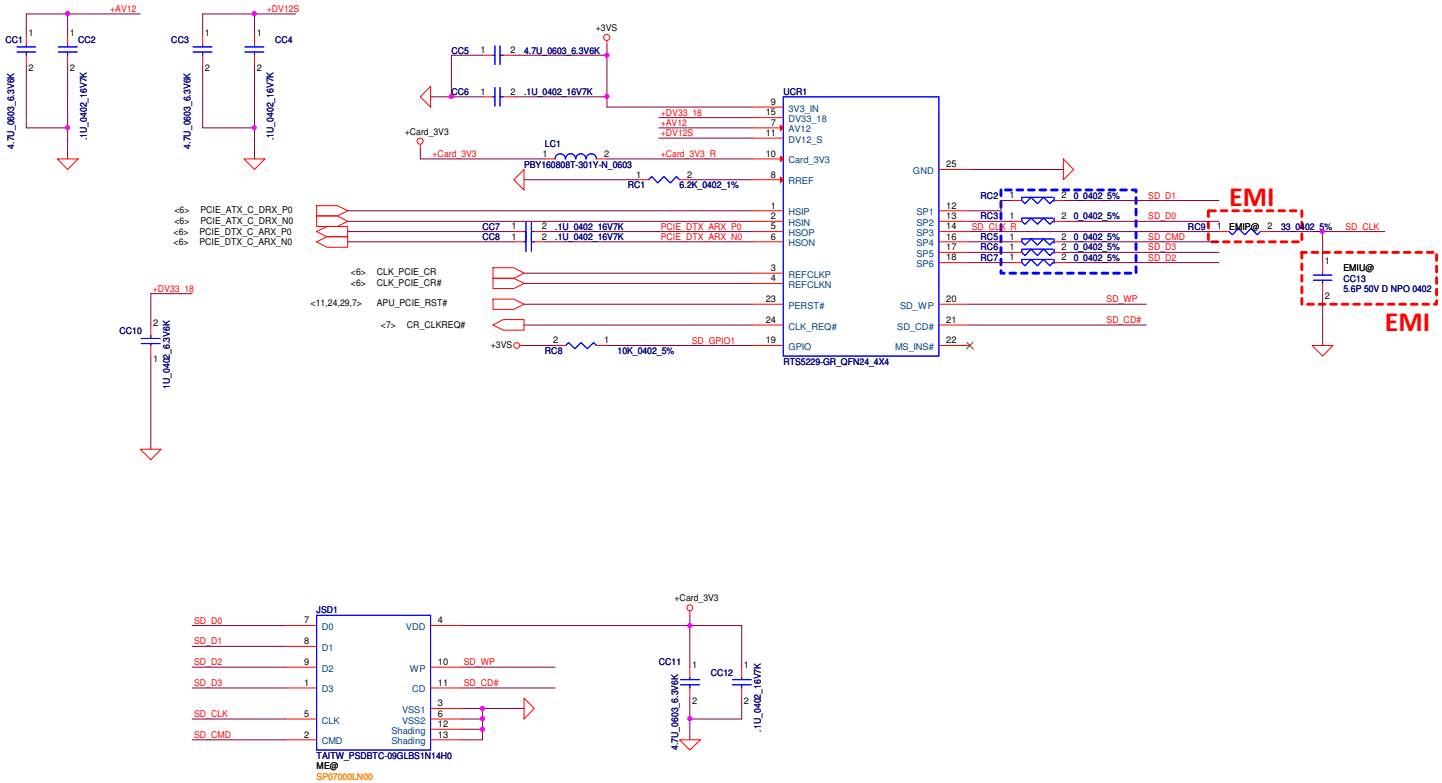
Compal Electronics, Inc.
Title
HD Audio Codec_ALC233
Size C
Document Number
LA-B291P
Rev 1.0
Date: Monday, March 03, 2014
Sheet 30 of 46



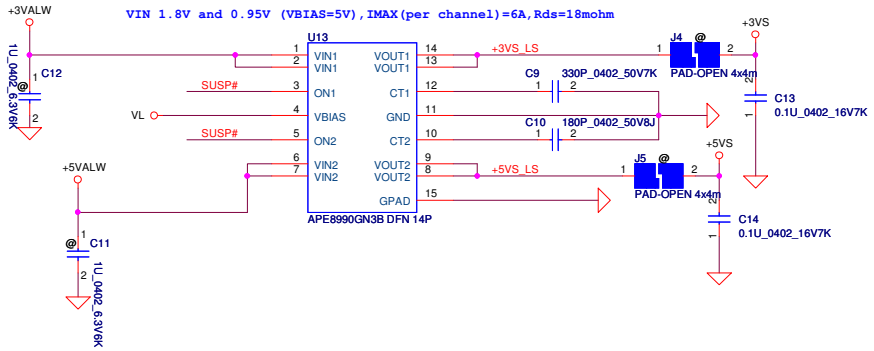
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Title	Card Reader RTS5229		
Size C	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 31 of 46		

+5VALW TO +5VS
+3VALW TO +3VS
Load switch

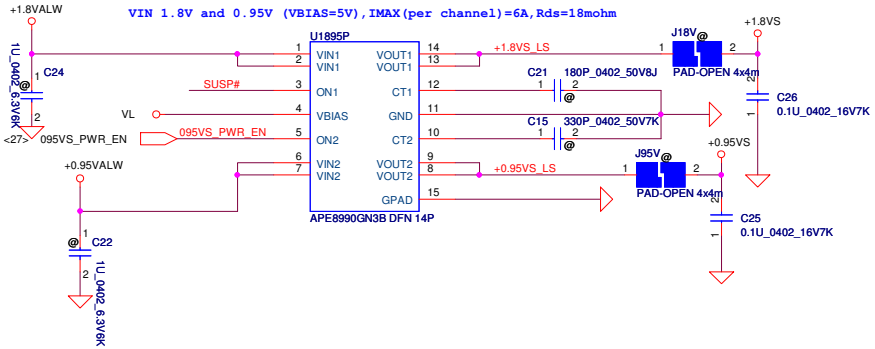
VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

VIN 1.8V and 0.95V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm



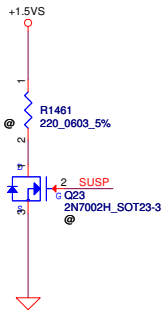
+1.8VALW TO +1.8VS
+0.95VALW TO +0.95VS
Load switch

VIN 1.8V and 0.95V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

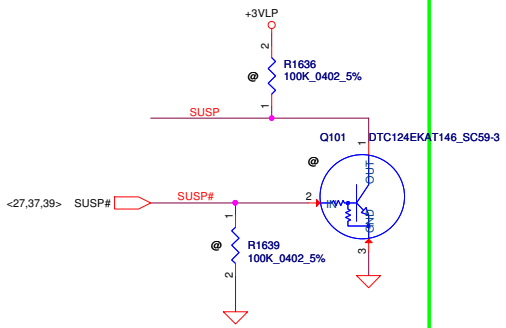


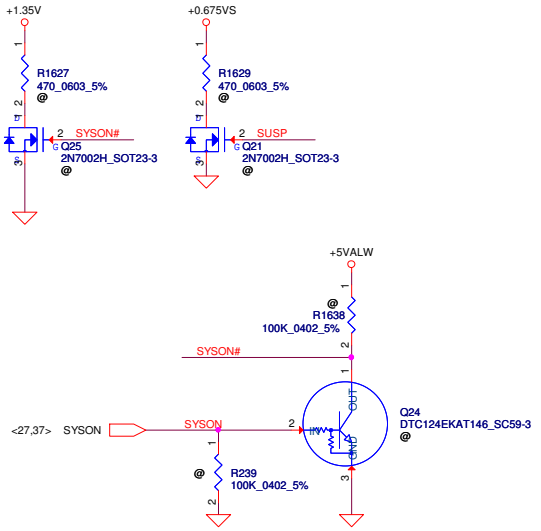
+1.5VS discharge circuit only for Beema

only 1.5VS from PWR



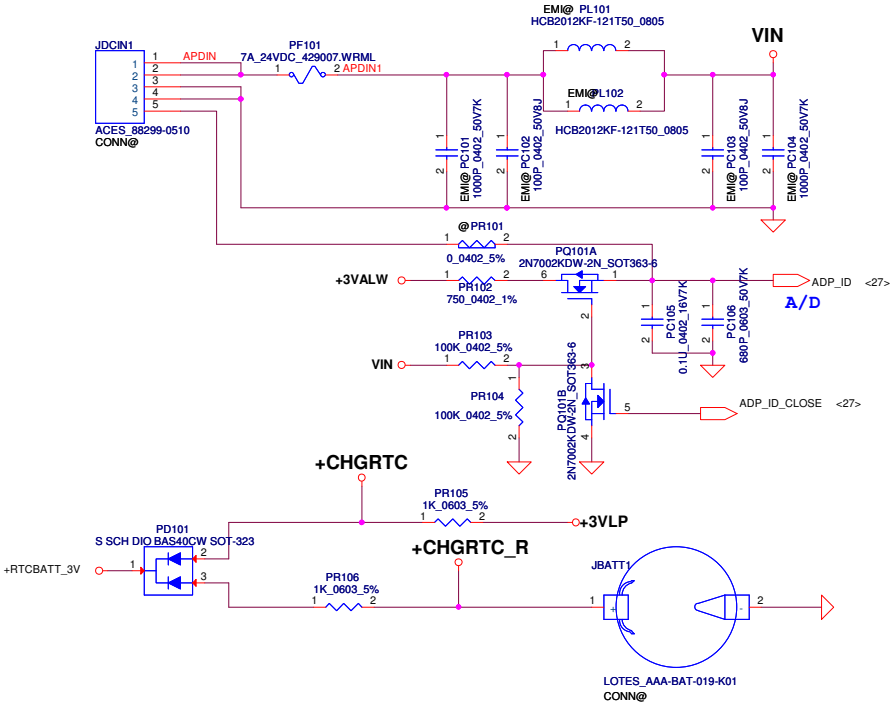
only for Beema





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title: DC Interface

Size: B	Document Number: LA-B291P		Rev: 1.0
Date: Monday, March 03, 2014	Sheet 32 of 46		



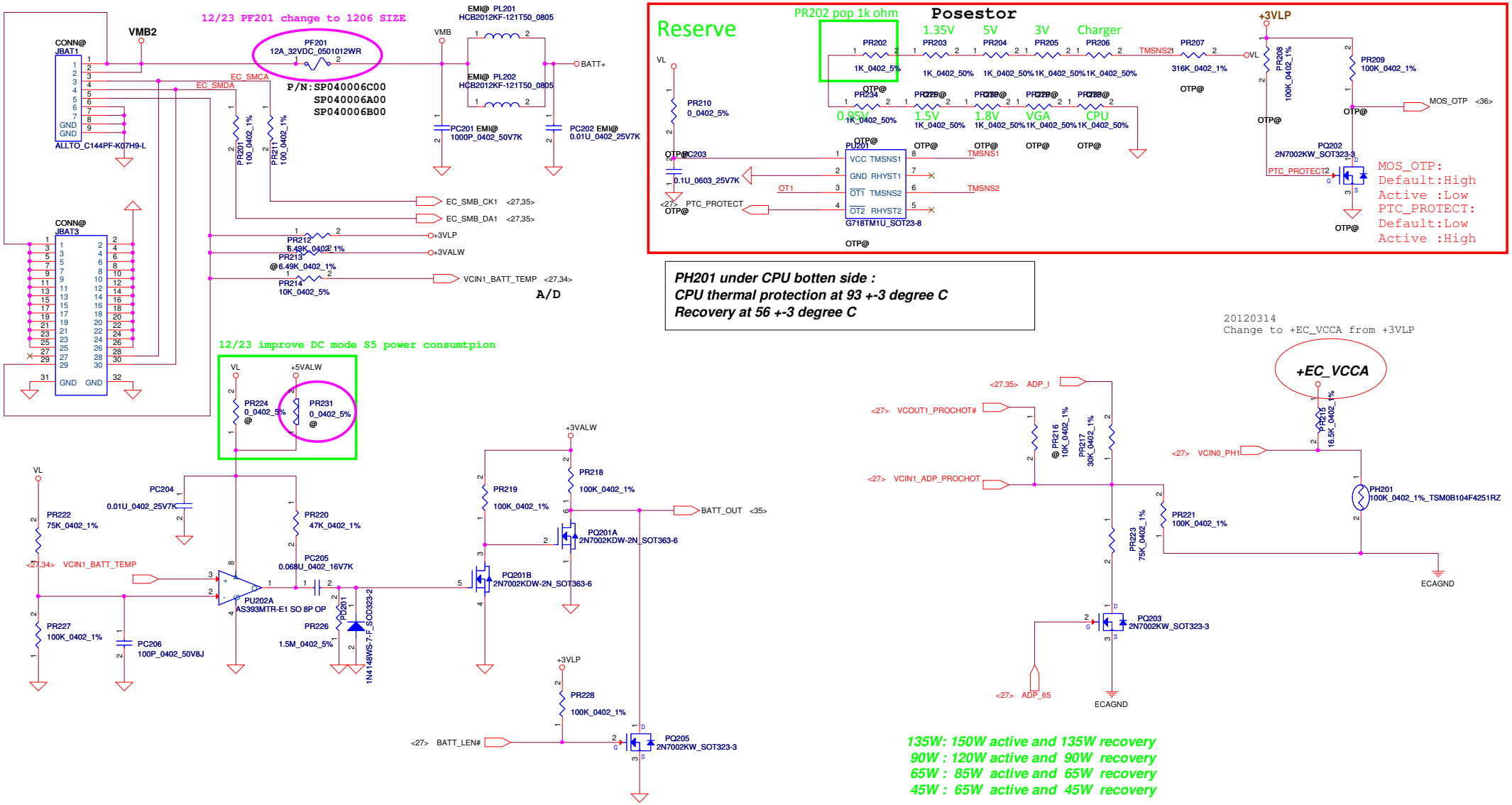
RTC Battery

ADP_ID

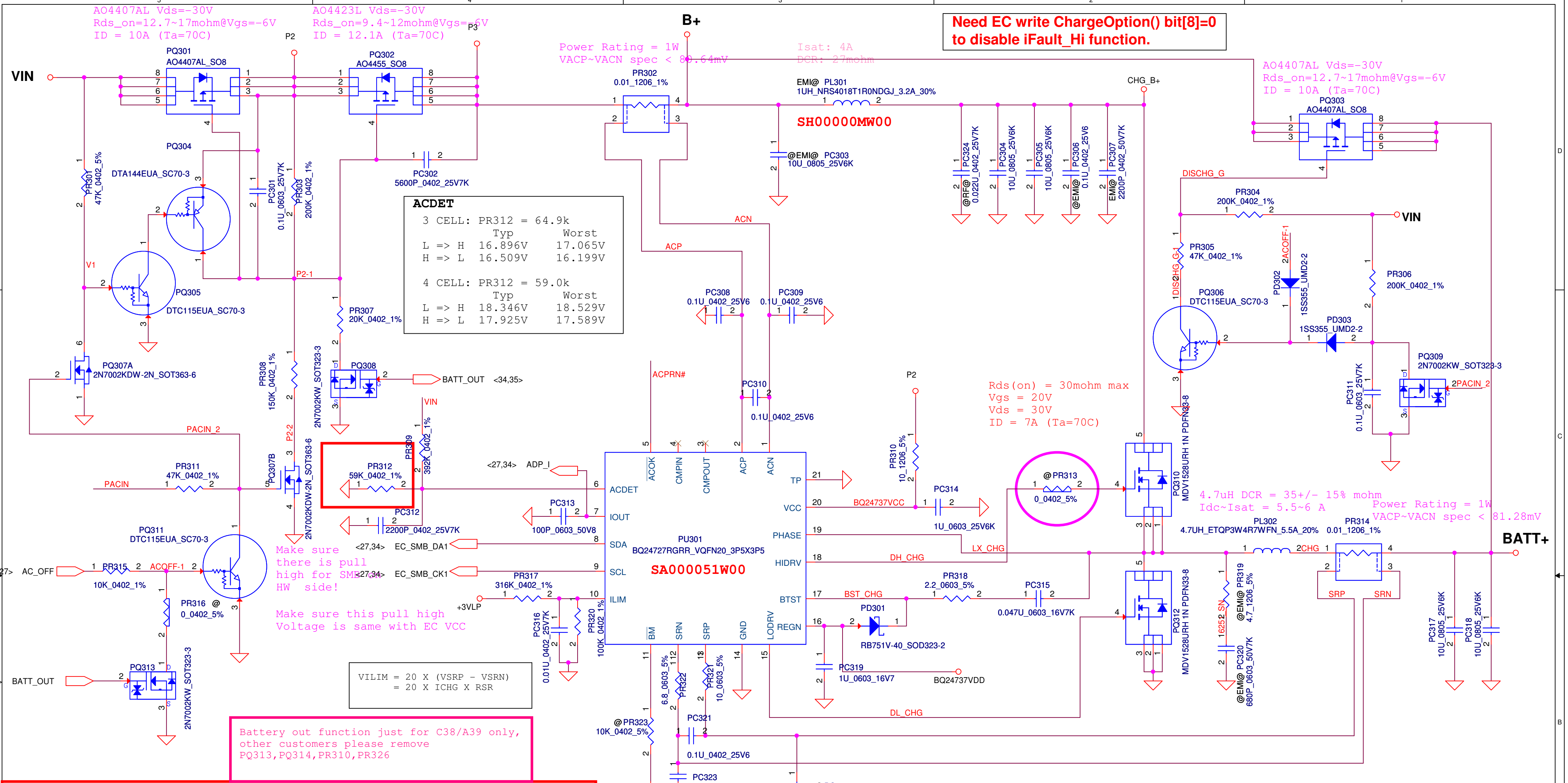
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date 2015/03/03	Title: Power Map

Size: Custom	Document Number: LA-B291P		Rev: 1.0
Date: Monday, March 03, 2014	Sheet 33 of 46		



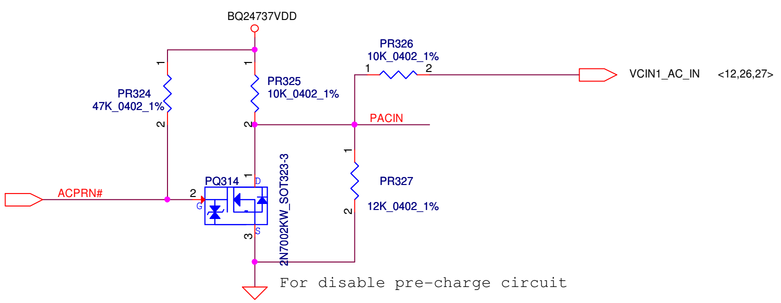
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date 2015/03/03	Title PWR- BATTERY CONN/OTP
Size Custom	Document Number LA-B291P		Rev 1.0
Date: Monday, March 03, 2014	Sheet 34 of 46		



Design Notes
Maximum Charging current 2.0A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. 0X12 bit[12:11] set 00 (default 11) to set BAT
Depletion Comparator Threshold
Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell)
4. Disable turbo when AC only
#Circuit Design
1. Make sure there is pull high for SMB on HW side
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 2.0A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)
4. For hybrid design, need double check PQ301,PQ302,PQ303,PQ309 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.15V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 104%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 135mV (default)

Module model information

BQ24737_V1.mdd for dual layer



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title: PWR- CHARGER BQ24727

Size | Document Number: LA-B291P | Rev 1.0

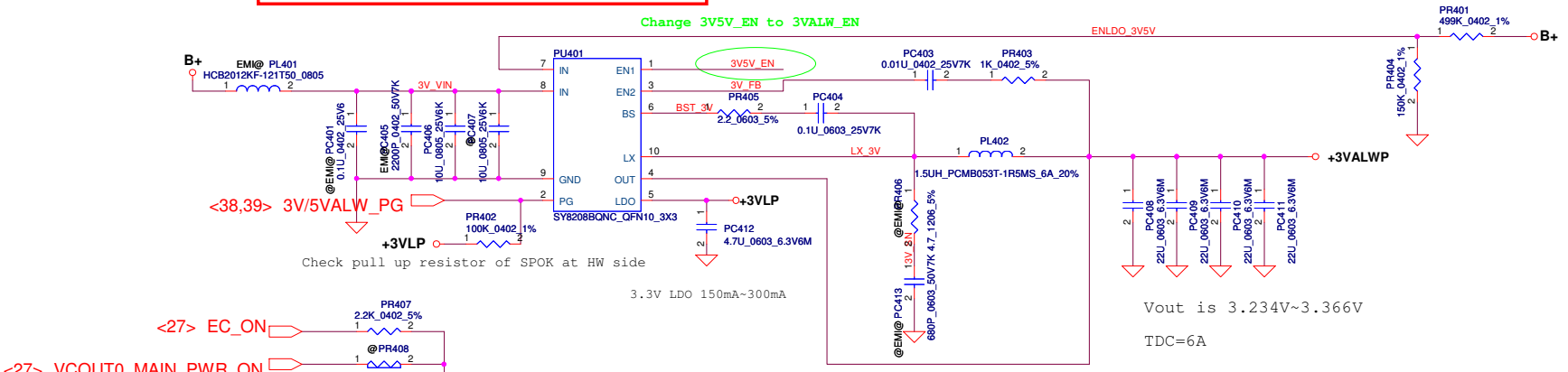
Date: Monday, March 03, 2014 |

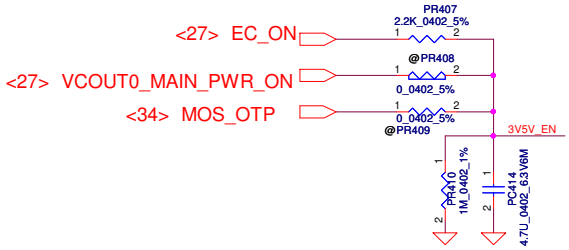
Module model information

SY8208B_V2.mdd

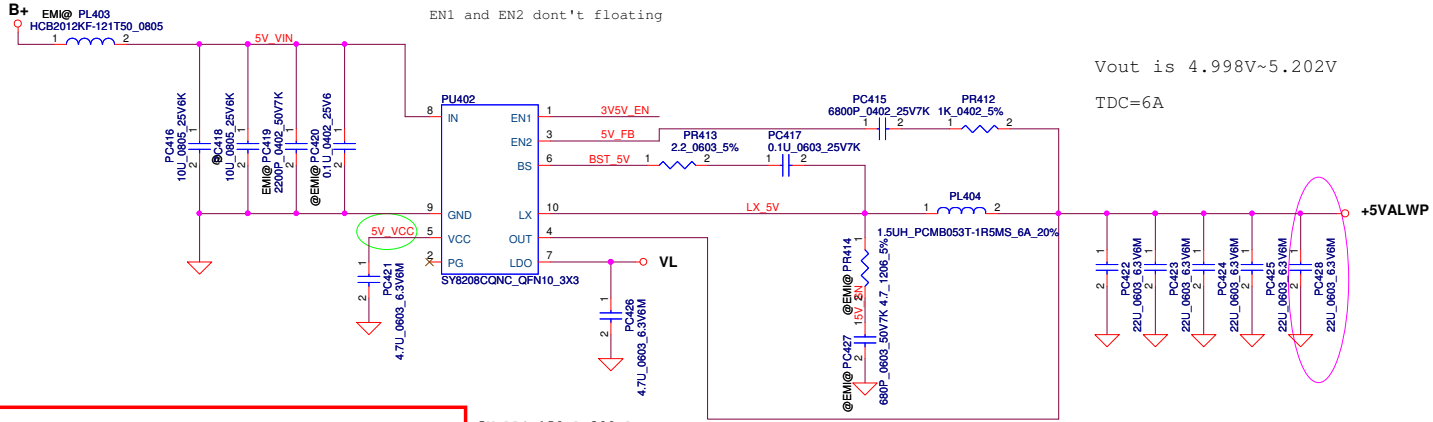
EN1 and EN2 dont't floating

Change 3V5V_EN to 3VALW_EN





EN1 and EN2 dont't floating



Module model information

SY8208C_V2.mdd

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

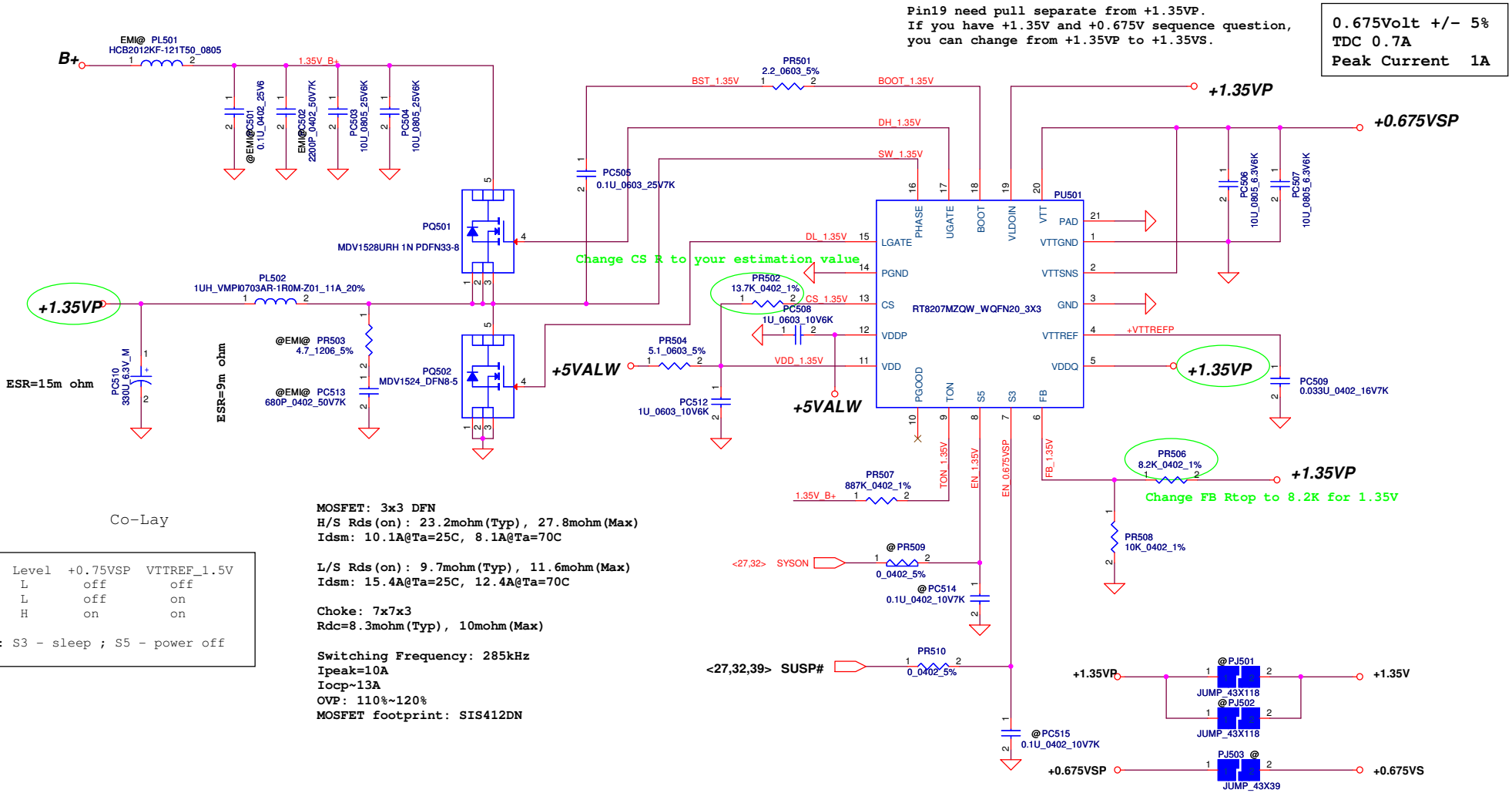
Title: PWR- 3VALW/5VALW-SY8208B/C

Size: Custom | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 36 of 46

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer



Co-Lay

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 9.7mohm(Typ), 11.6mohm(Max)
Idsm: 15.4A@Ta=25C, 12.4A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: PWR-+1.35VP/ +0.675VS

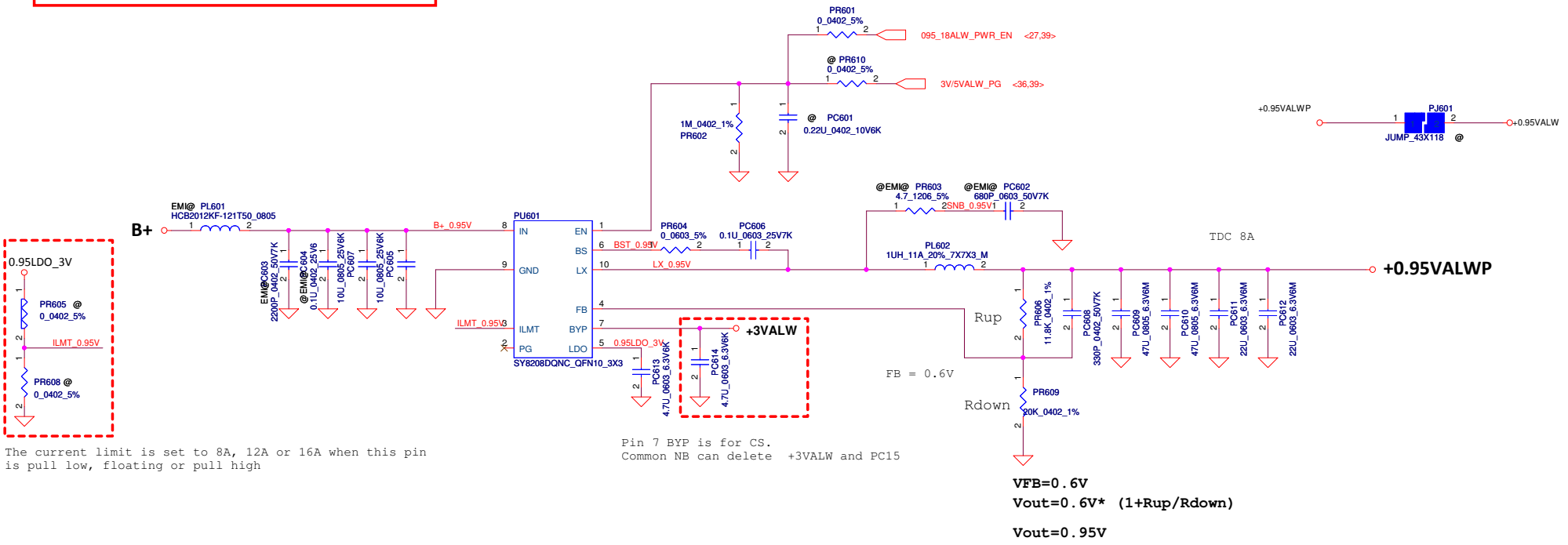
Size: Custom | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 37 of 46

Module model information

SY8208D_V2.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=0.95V

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	PWR- +0.95VALW		
Size: Custom	Document Number: LA-B291P		Rev: 1.0
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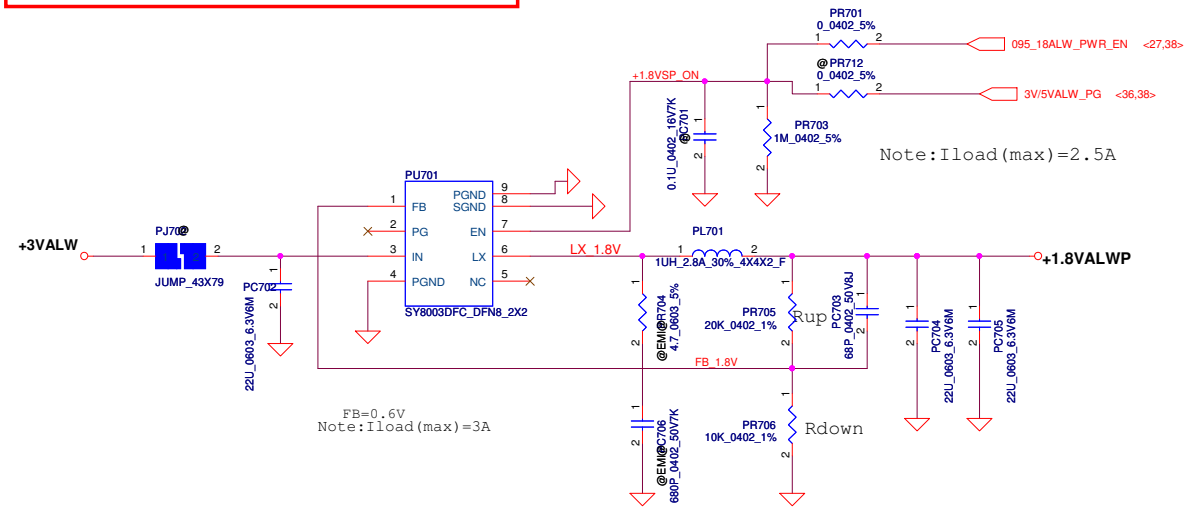
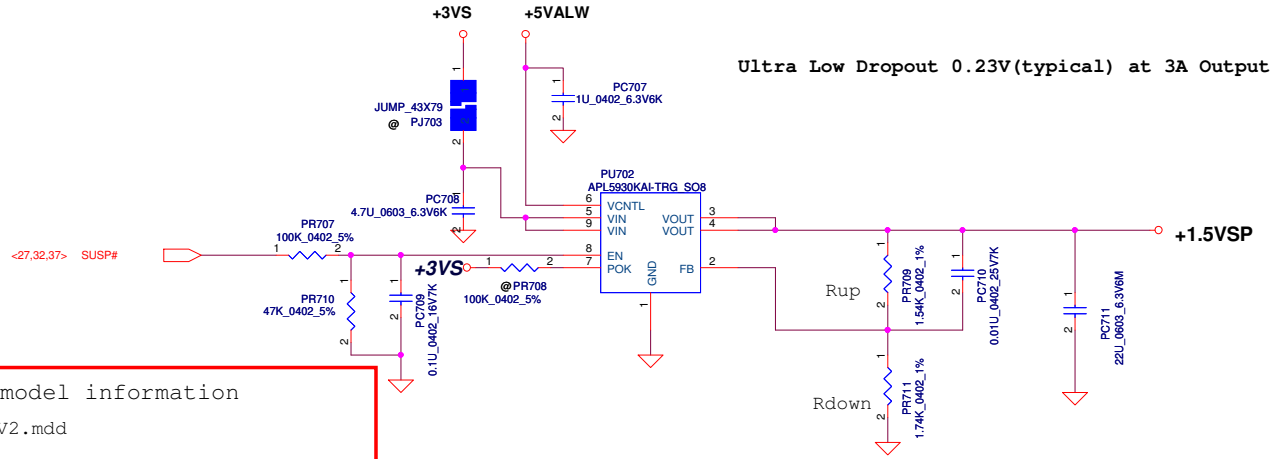
Module model information

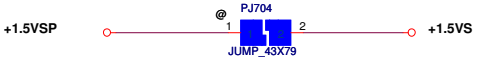
SY8003_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)





Ultra Low Dropout 0.23V(typical) at 3A Output Current

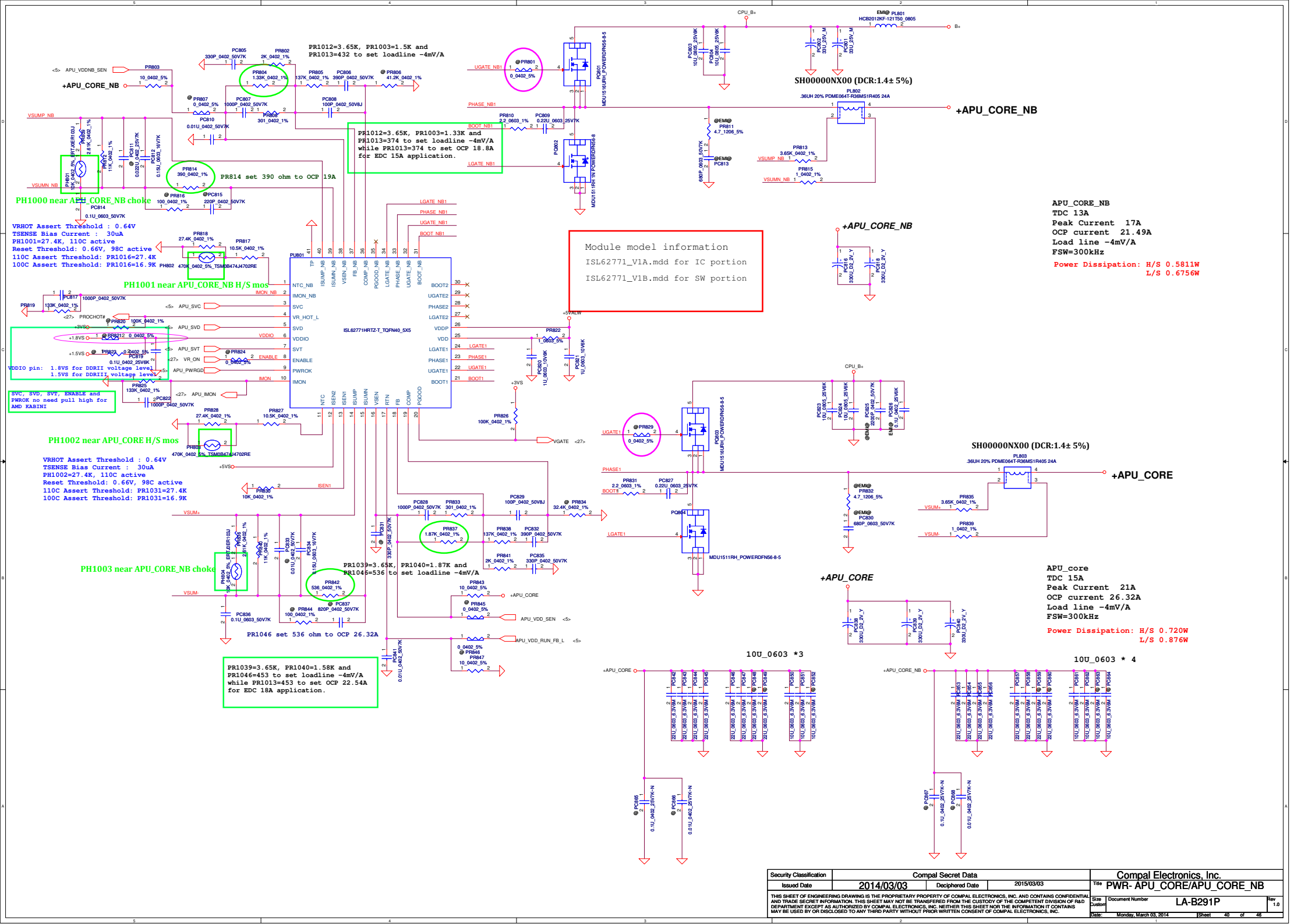
Vout=0.8V* (1+Rup/Rdown)

Module model information

APL5930_V2.mdd

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	PWR- +1.8VALW/ +1.5VS		
Size: Custom	Document Number: LA-B291P		Rev: 1.0
Date: Monday, March 03, 2014	Sheet 39 of 46		



Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

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Compal Electronics, Inc.	
Title	PWR- APU_CORE/APU_CORE_NB
Size: Custom	Document Number: LA-B291P
Rev	1.0
Date: Monday, March 03, 2014	Sheet 40 of 46

Module model information

ISL62771_V1A.mdd for IC portion

ISL62771_V1B.mdd for SW portion

+VGA_CORE
AMD JET LE
TDC 20A
EDC 30A

Fsw=400K Hz

VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1001=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1016=27.4K
100C Assert Threshold: PR1016=16.9K

SVC, SVD, SVI, ENABLE and PWROK no need pull high for AMD KABINI

VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

25W

15W

GPU 15W setting

PR931=536 ohm, PR924=1K ohm, PC925=0.1uF,
PR944 =0 ohm, PR920=10K ohm,
PC961 @, PC962 @, PR938 @ and PR939 @
while PR931=536 ohm to set OCP for GPU 15W application.

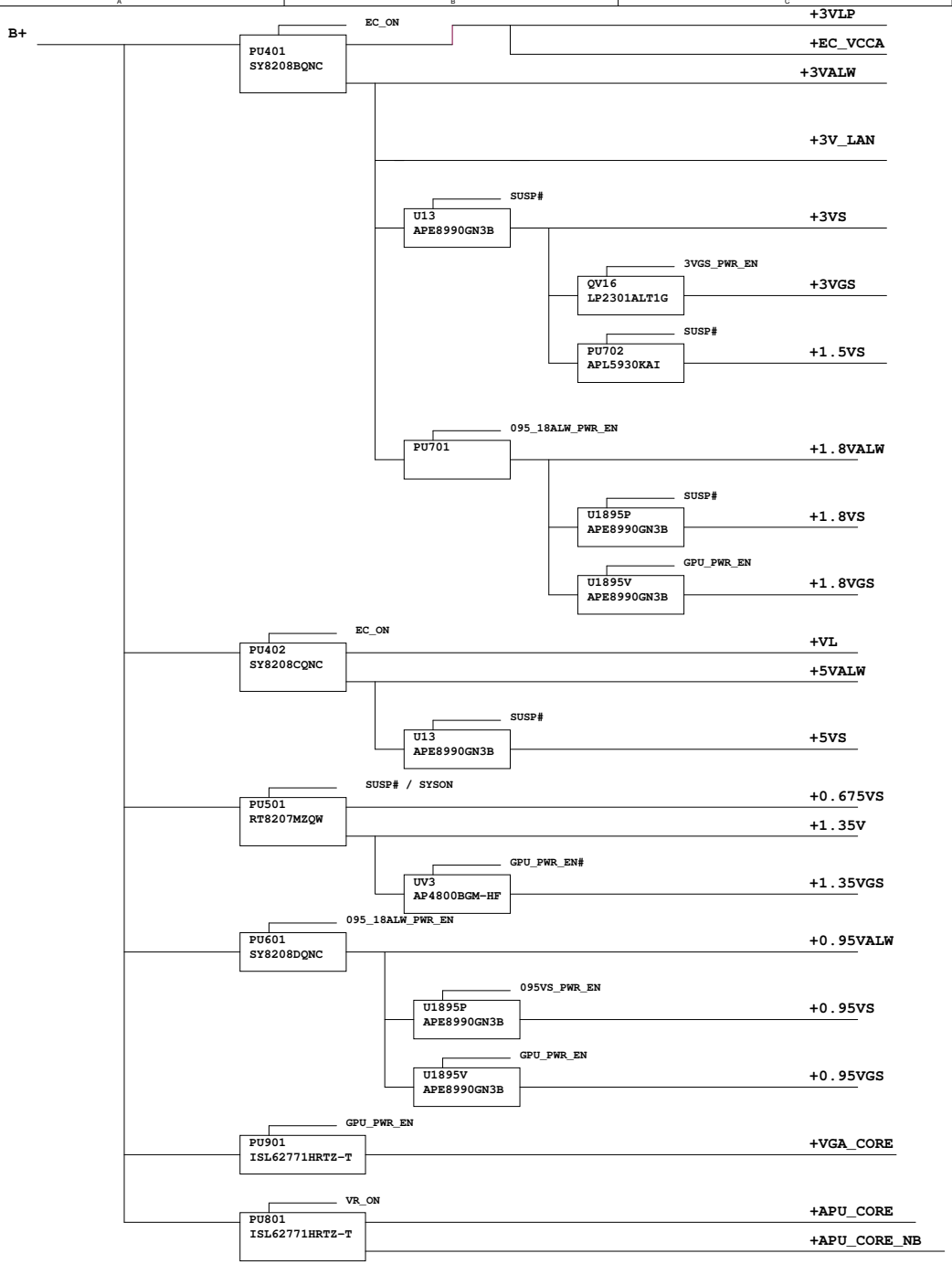
SH00000NX00 (DCR:1.4± 5%)

1/7 change to H=6 CAP_SF000002000

Power Dissipation: H/S 0.720W
L/S 0.876W

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.			
Title	PWR- +VGA_CORE		
Size: Custom	Document Number: LA-B291P		Rev: 1.0
Date: Monday, March 03, 2014	Sheet 41 of 46		



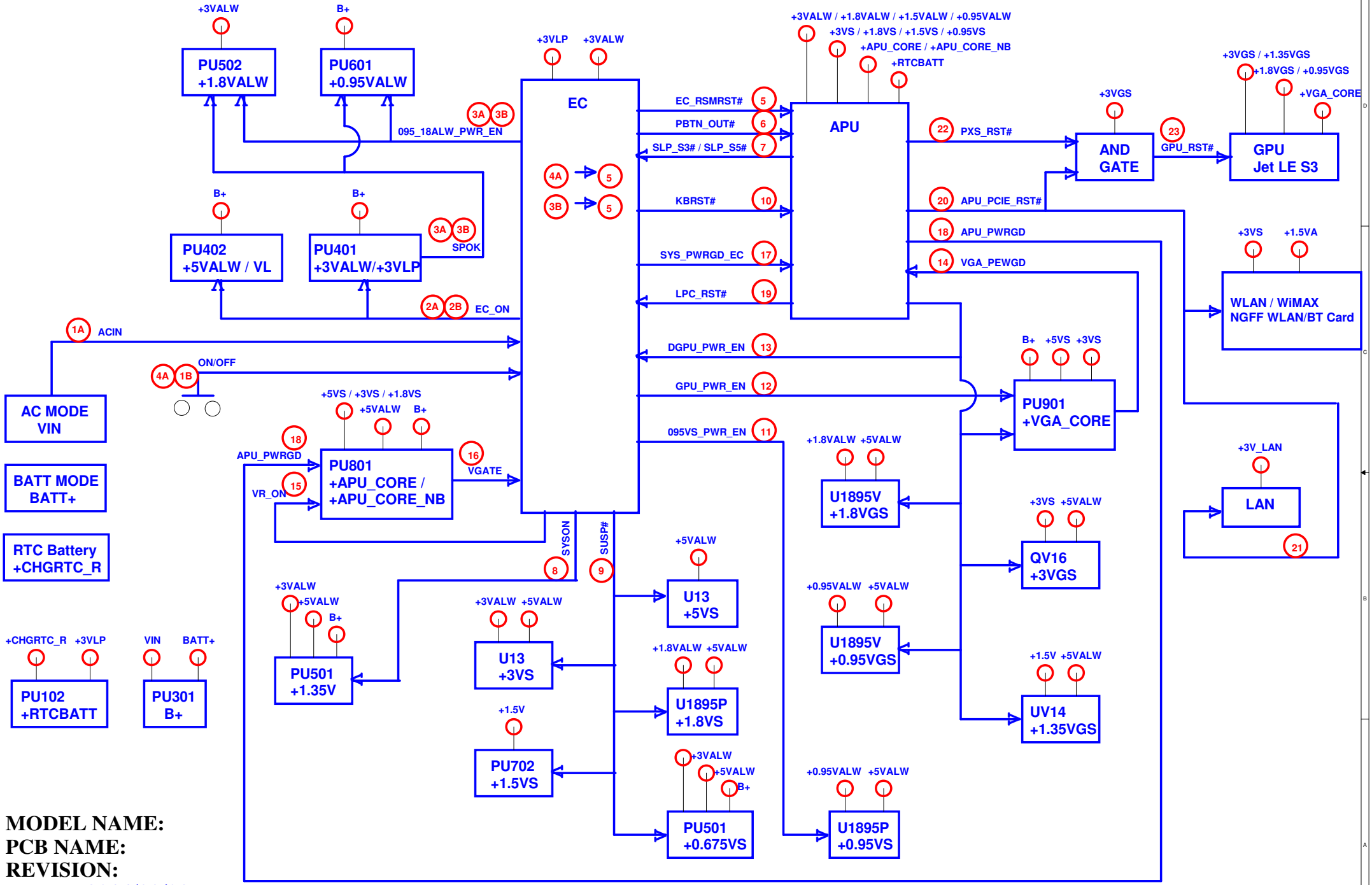
Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: LA-B291P | Rev: 1.0

Date: Monday, March 03, 2014 | Sheet 42 of 46



MODEL NAME:
PCB NAME:
REVISION:
DATE: *2014/03/03*

COMPAL CONFIDENTIAL

Security Classification	Compal Secret Data		
Issued Date	2014/03/03	Deciphered Date	2015/03/03

Compal Electronics, Inc.

Title: Power Sequence Block

Size: Custom | Document Number: LA-B291P | Rev: 1.0

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