
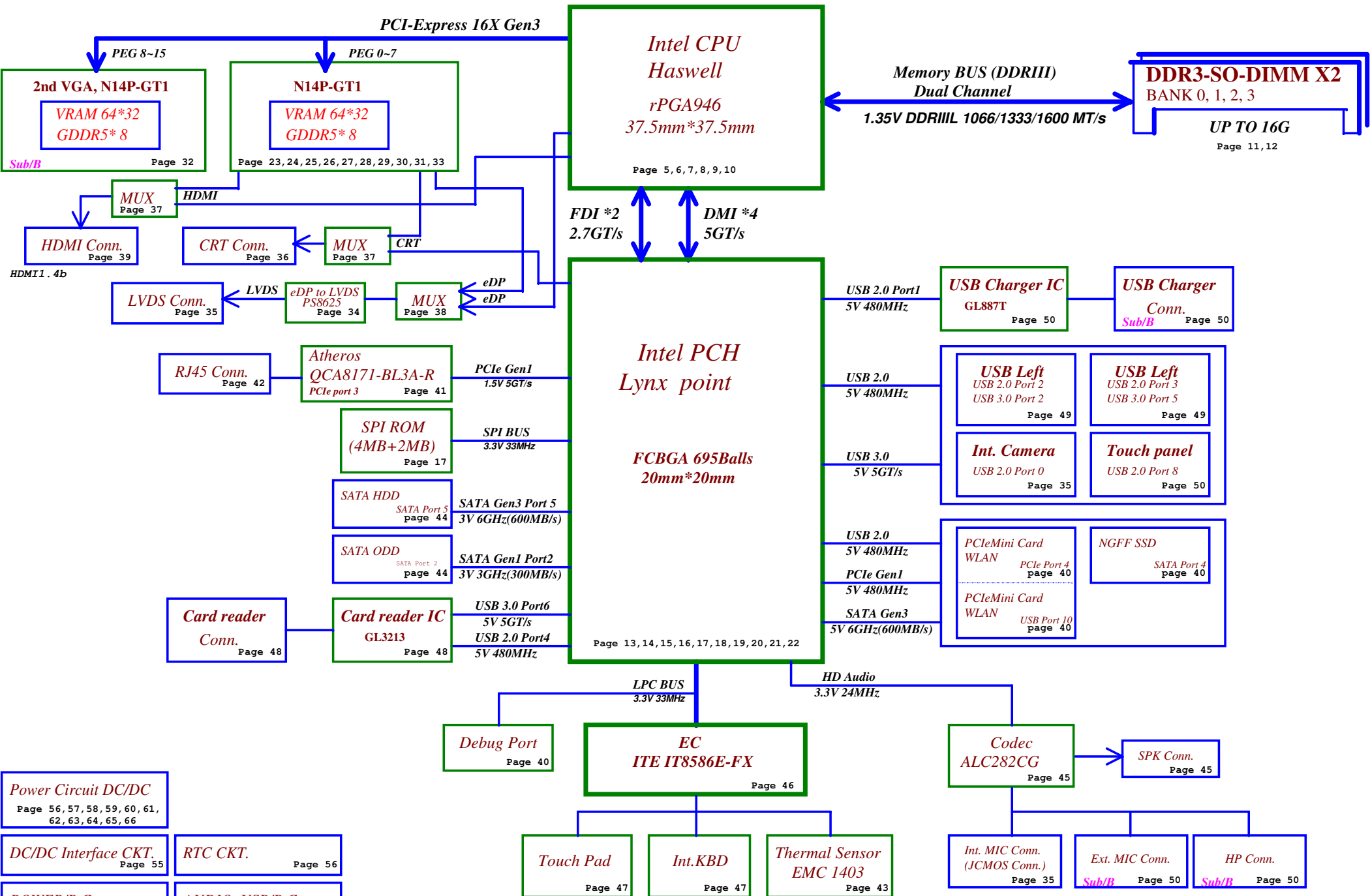


VIQY1 (Y510)

NM_A032 Rev1.0 Schematic

***Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P GT + 2nd VGA N14P GT
2013-03-19 Rev1.0***

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				Y501 NM-A032	

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
		0	Camera
	XHCI	1	USB Port (Right Side)
	EHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
		4	Card Reader
		5	
		6	
		7	
	EHCI2	8	Touch panel
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	

BOM Structure Table

BOM Structure	BTO Item
GT@	NV GT750M
GT1@	NV GT755M
CMOS@	CMOS Camera part
SURGE@	QCA8171 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
@	Unpop
DS3@	Deep S3 support part
daul@	Support daul channel panel function
887T@	GENESYS 887T USB charger solution
887@	GENESYS 887 USB charger solution
TI@	TI USB charger solution
EDP@	Support EDP panel function
SLI@	For SLI function part
47W@	For 47W CPU part
37W@	For 37W CPU part

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIe PORT LIST

Port	Device
1	
2	
3	
4	LAN
5	WLAN
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



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VGA and GDDR5 Voltage Rails (N14Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	IN	-	FB_CLAMP_MON
GPIO1	OUT	-	NA
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	NA
GPIO6	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO7	OUT	-	NA
GPIO8	OUT	-	OVERT#
GPIO9	OUT	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	NVVDV PWM_VID
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	DPRSLPVR_VGA
GPIO14	OUT	-	NA
GPIO15	IN	-	NA
GPIO16	OUT	-	NA
GPIO17	IN	-	VGA_EDP_HP
GPIO18	IN	-	DGPU_HDMI_HP
GPIO19	IN	-	NA

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

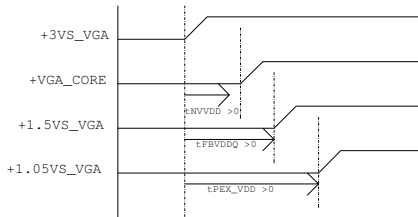
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

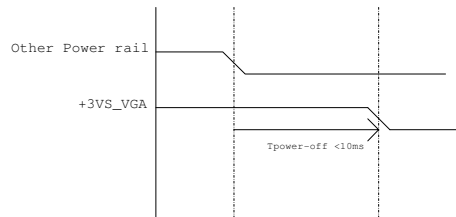
Device ID	setting	I2C Slave addresses ID
N13P-GT (28nm)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N14P-GT 28nm	PU 10K	PD 15K	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU	N14P-GT	N14P-GT1
FB Memory (GDDR5)	ROM_SI	ROM_SI
Samsung 3000MHz	K4G20325FD-FC03	
	64Mx32	PD 30K
Hynix 3000MHz	H5GQ2H24AFR-R0C	
	64Mx32	PD 25K
Samsung 2500MHz	K4G20325FD-FC04	
	64Mx32	PD 30K
Hynix 2500MHz	H5GQ2H24AFR-T2C	
	64Mx32	PD 25K

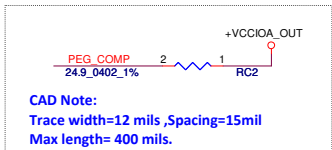


1. all power rail ramp up time should be larger than 40us

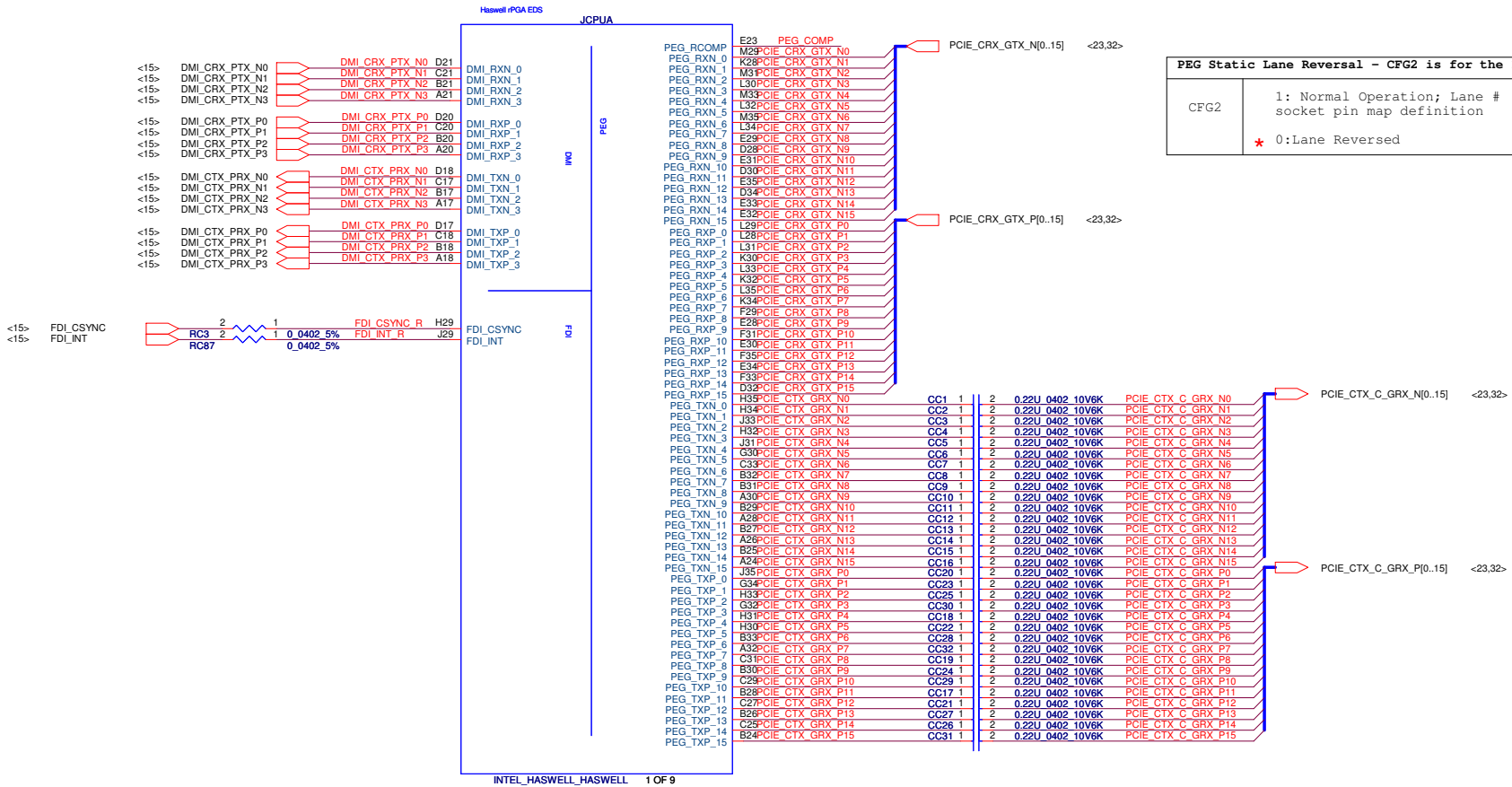


1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

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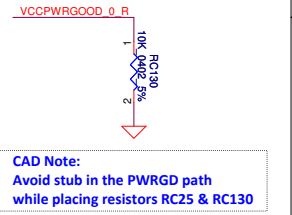
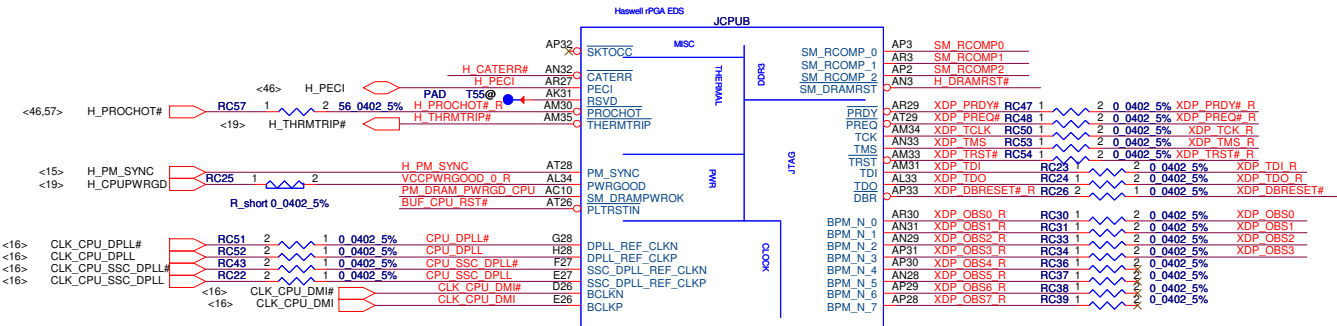
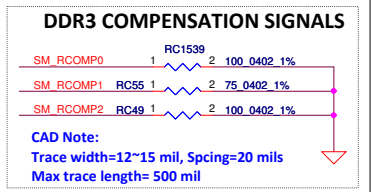
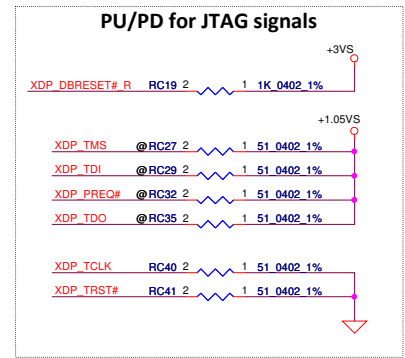
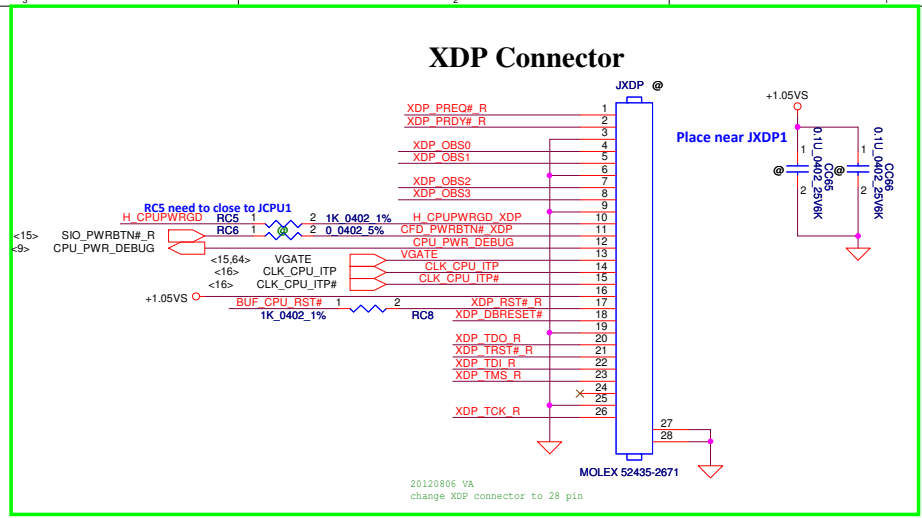
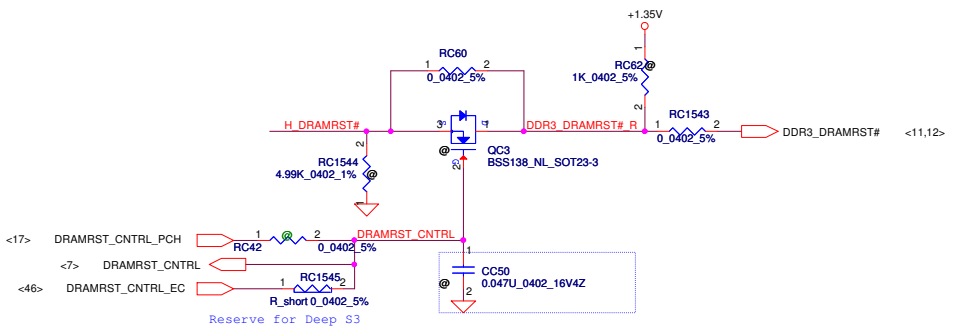


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

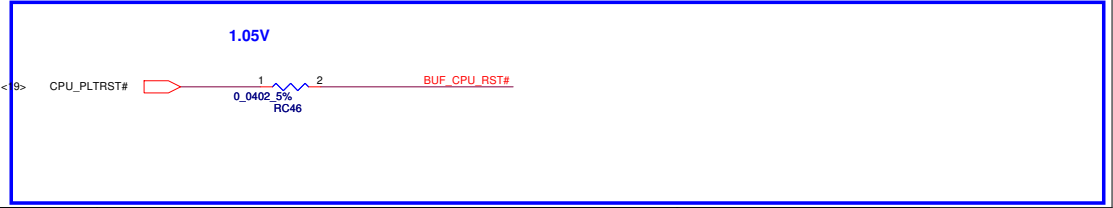
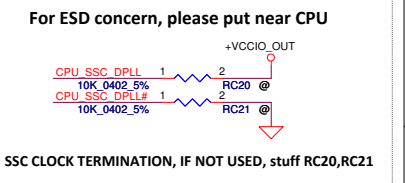
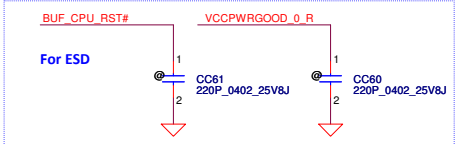
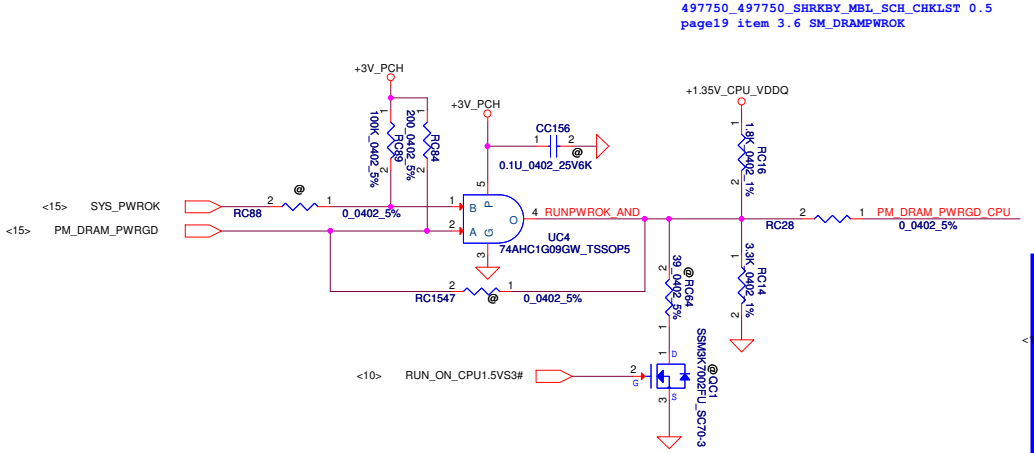


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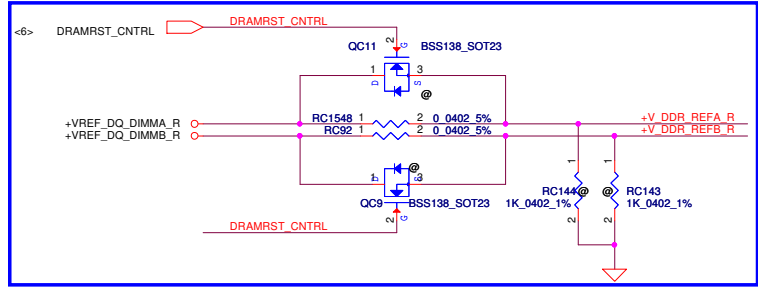
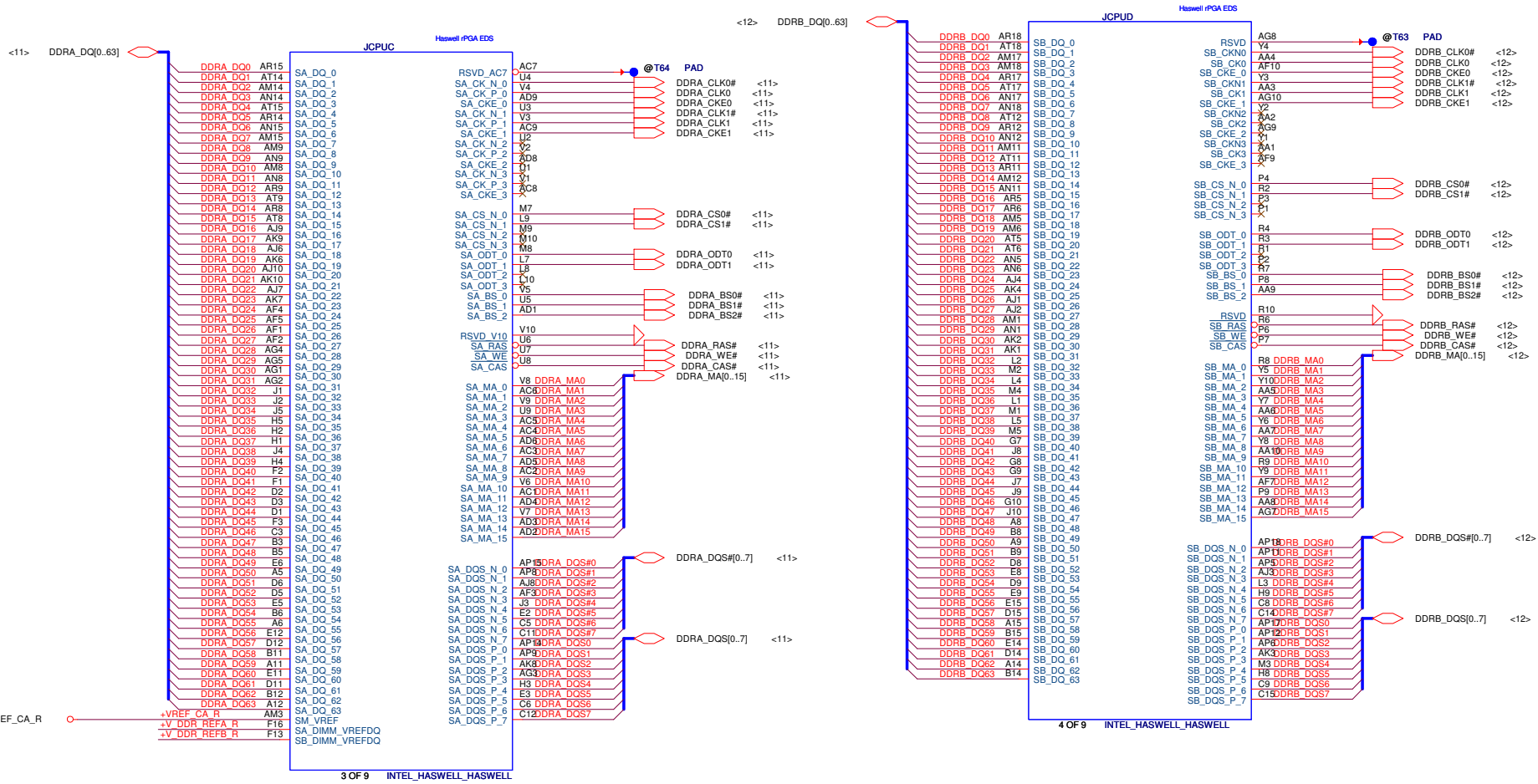
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SM_DRAMPWRK with DDR Power Gating Topology



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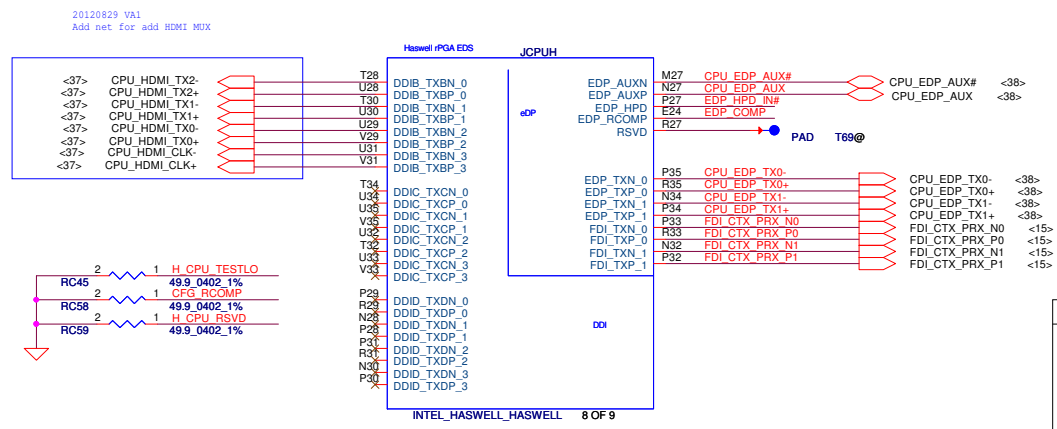
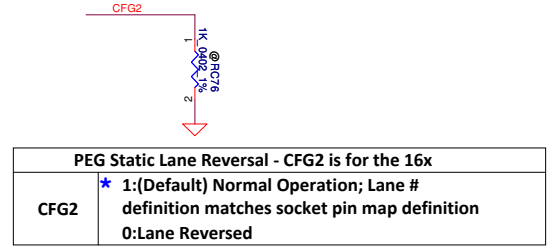
6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

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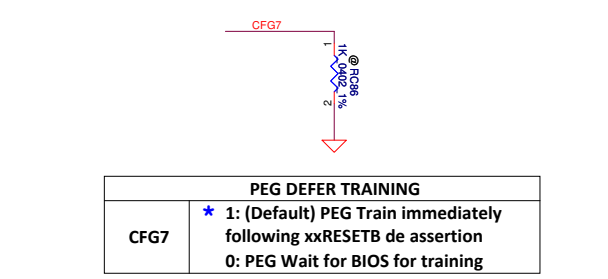
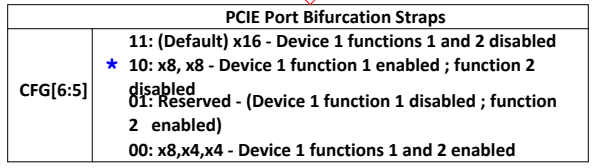
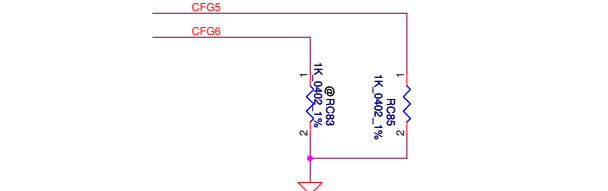
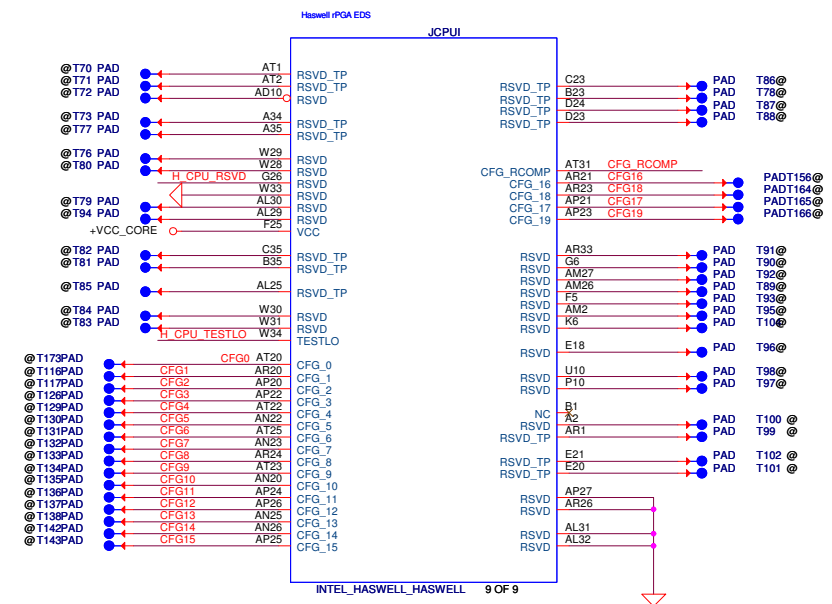
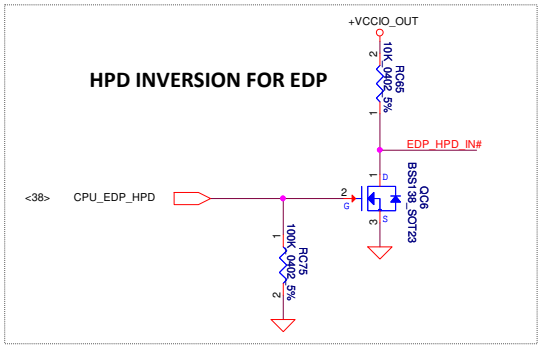
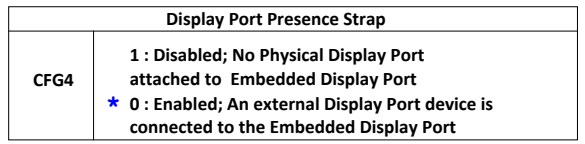
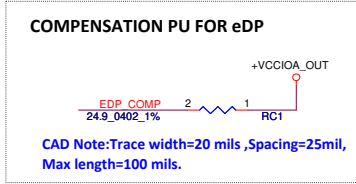


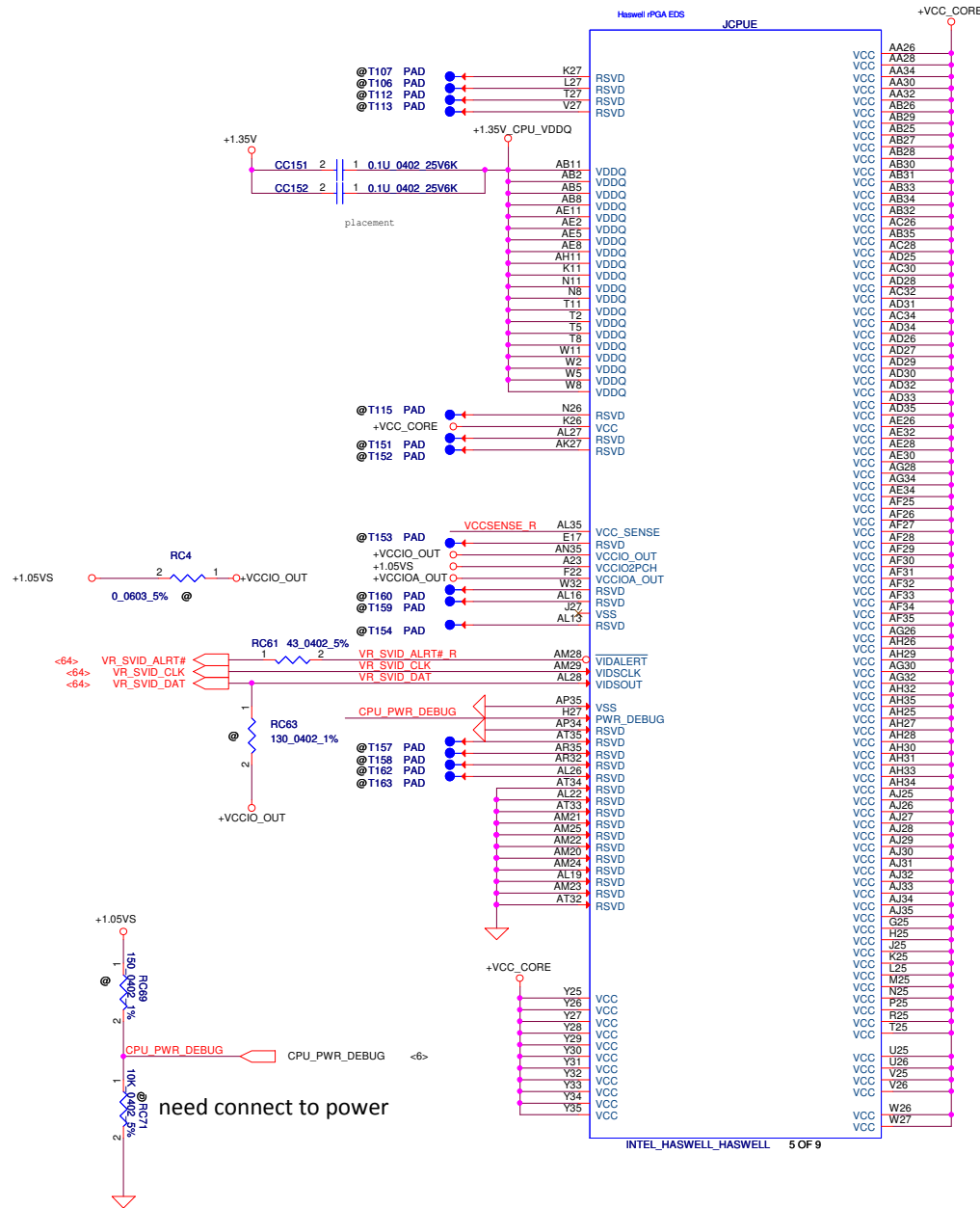
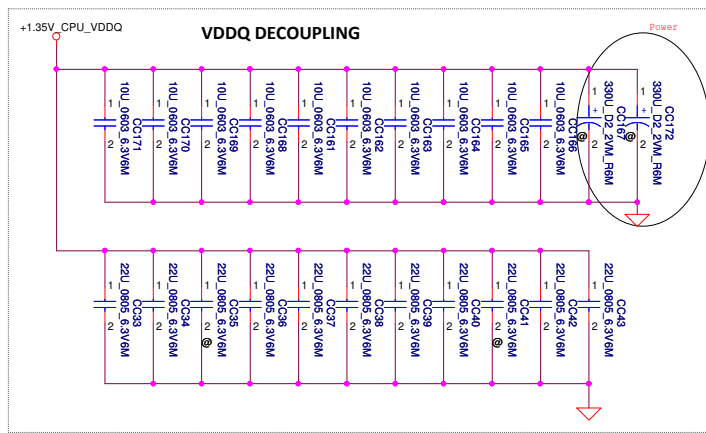
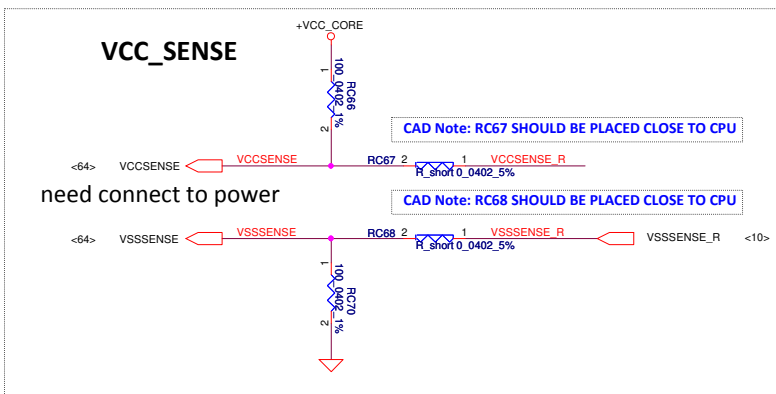
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CFG STRAPS for CPU



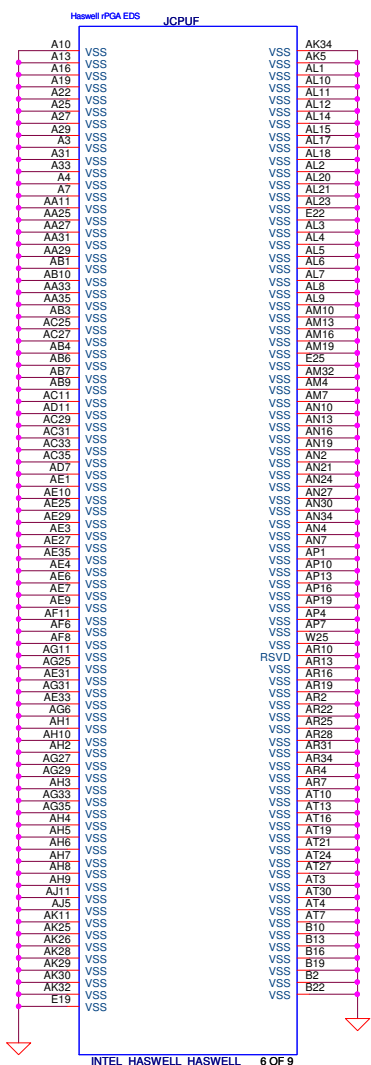
check CLK item



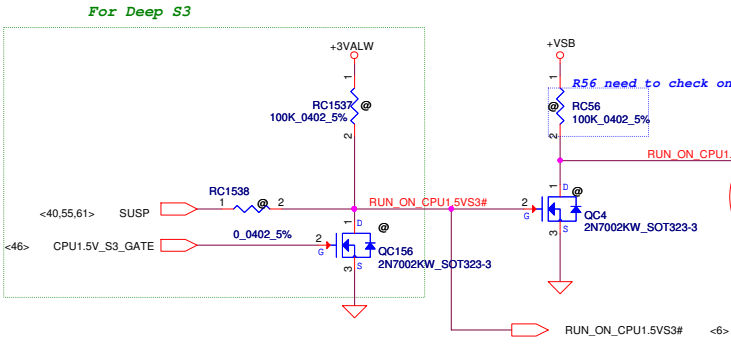
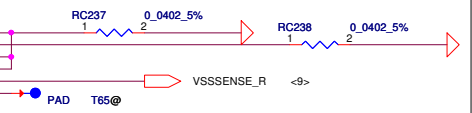
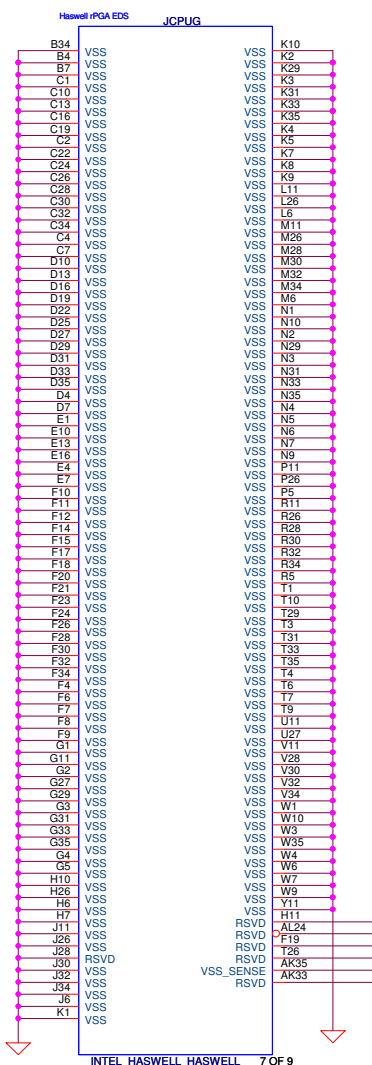
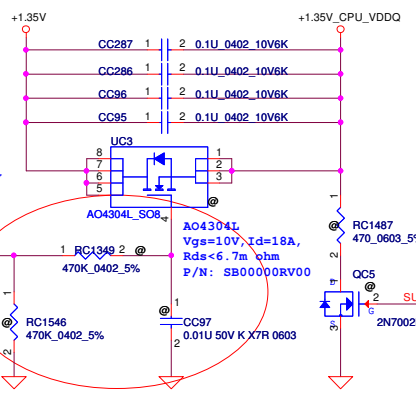


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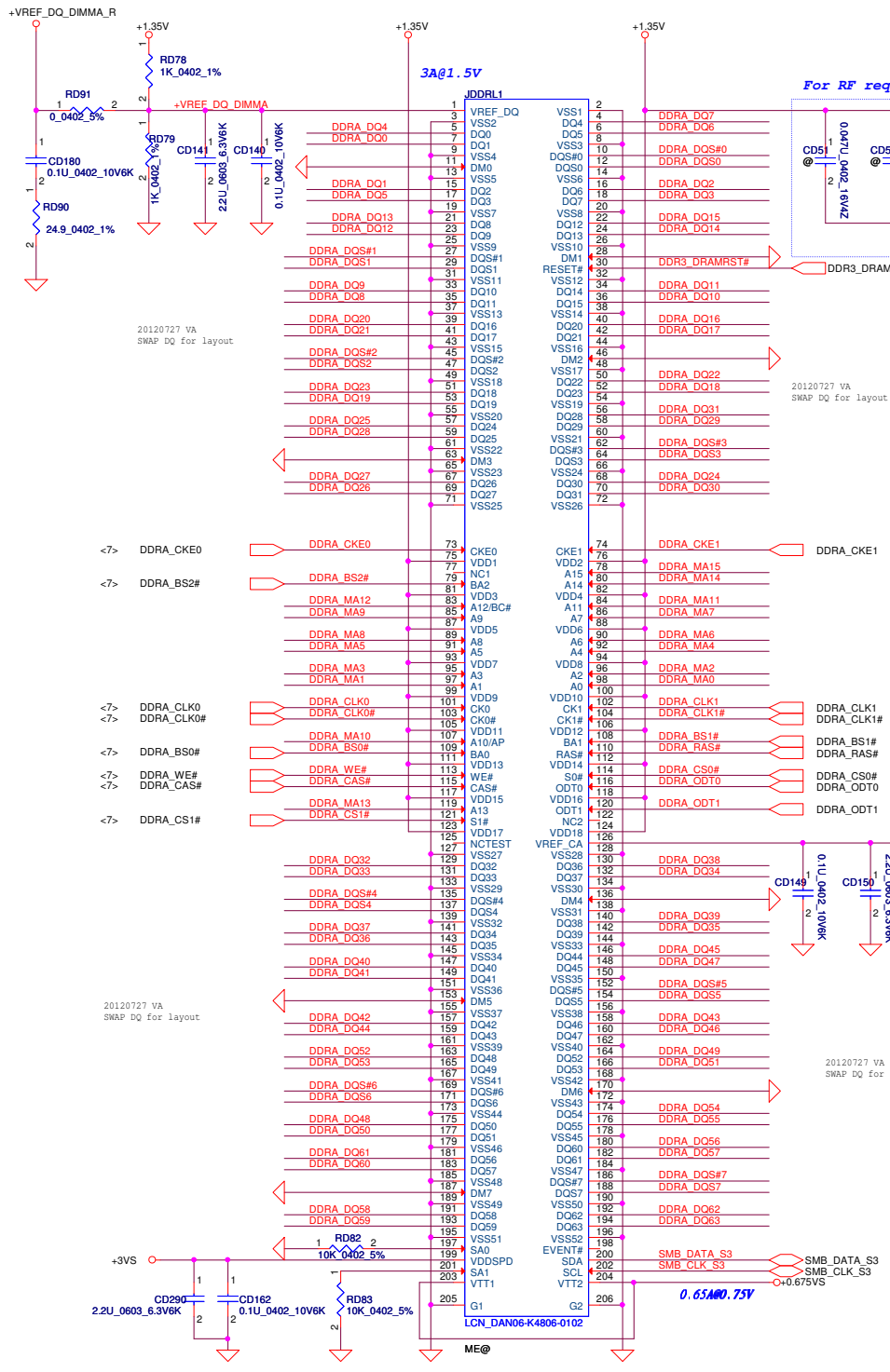
+1.35V_CPU_VDDQ



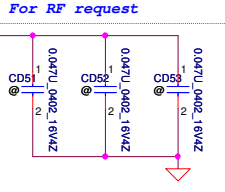
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CPU (6/7) PWR			
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DDR3 SO-DIMM A

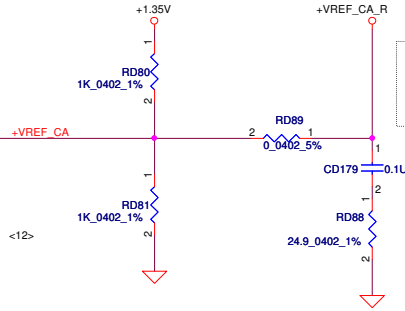
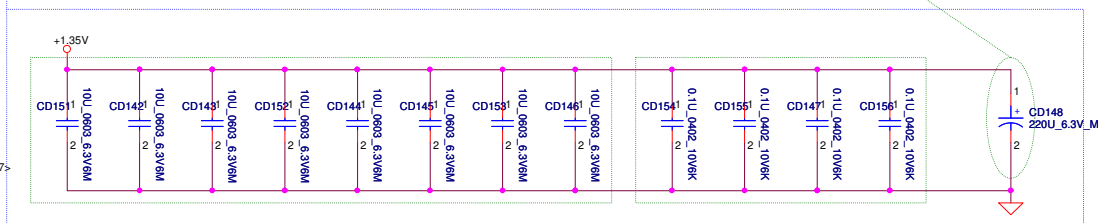


- DDRA_DQ[0..63] <7>
- DDRA_DQS[0..7] <7>
- DDRA_DQS#0[0..7] <7>
- DDRA_MA[0..15] <7>



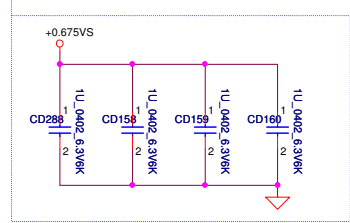
Layout Note:
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OSCON (220uF_6.3V_4.2L_ESR17m) *1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4



Layout Note:
Place near DIMM

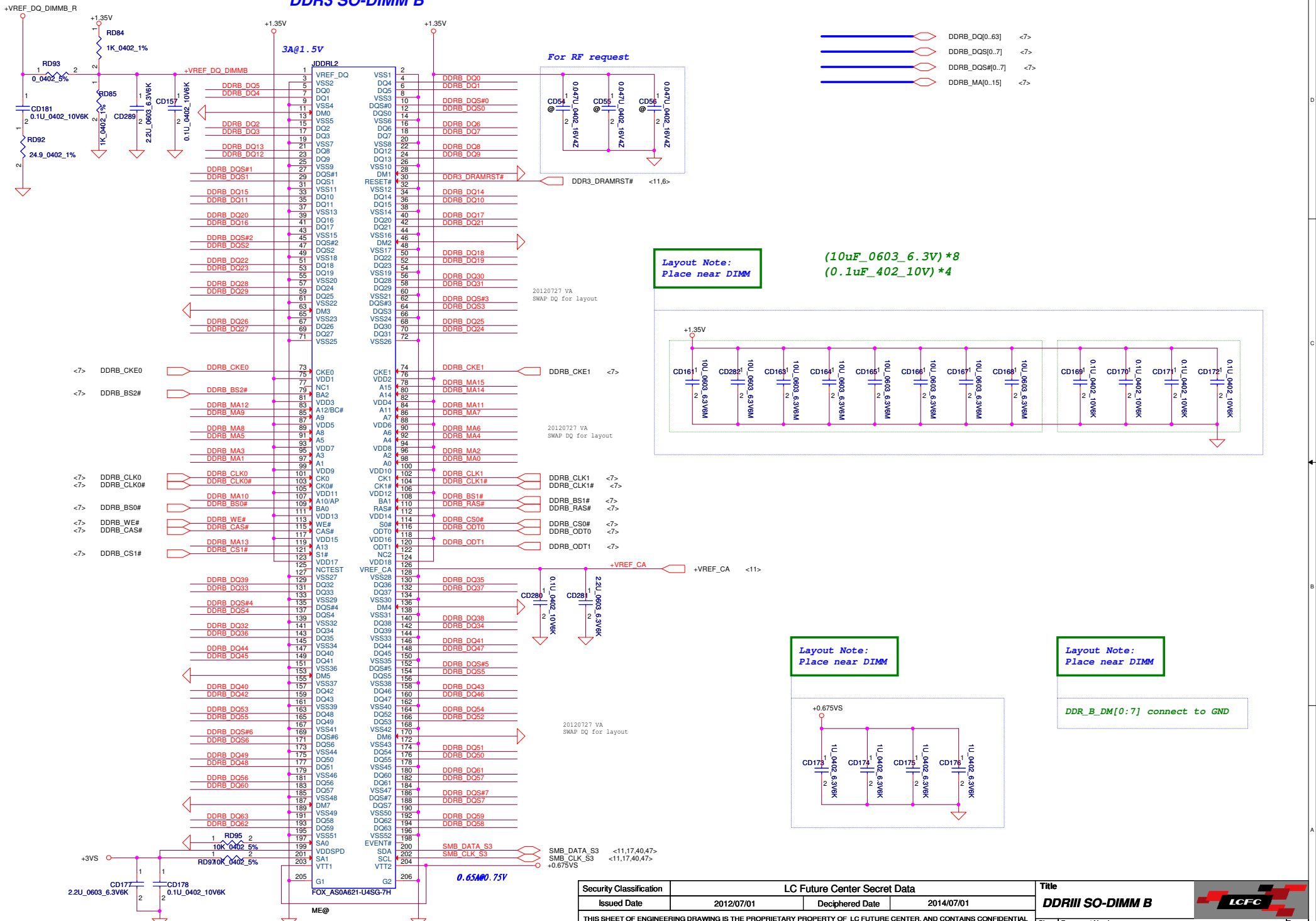
Layout Note:
Place near DIMM



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Title		LCFC	
DDRIII SO-DIMM A			
Size	Document Number	Y501 NM-A032	
Customer			
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DDR3 SO-DIMM B

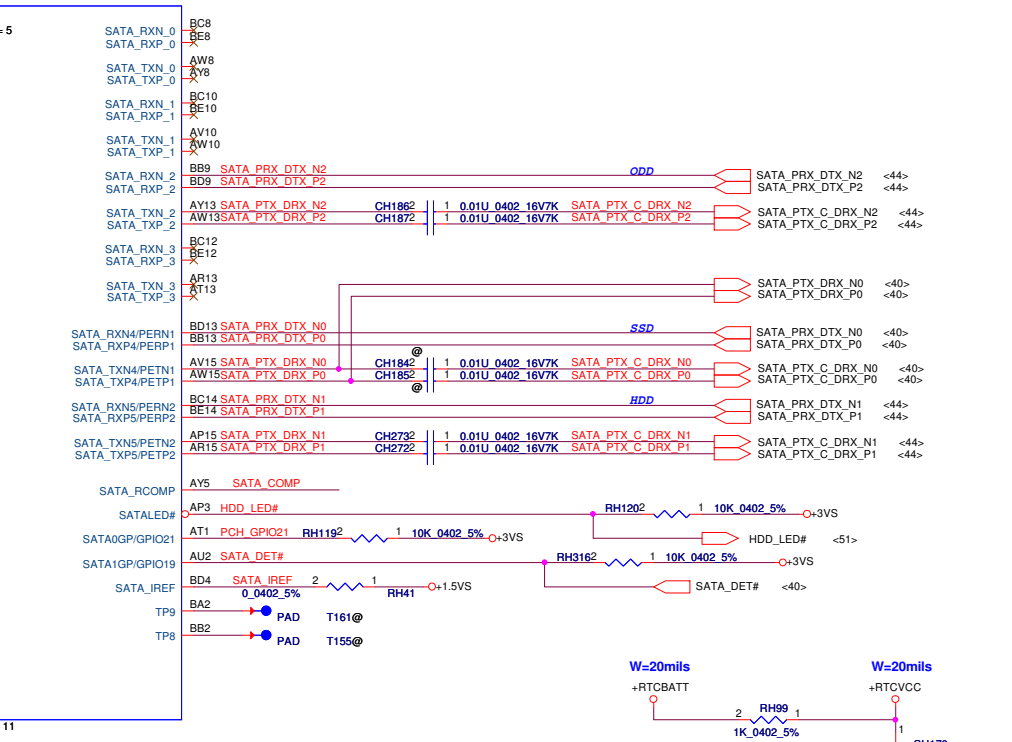
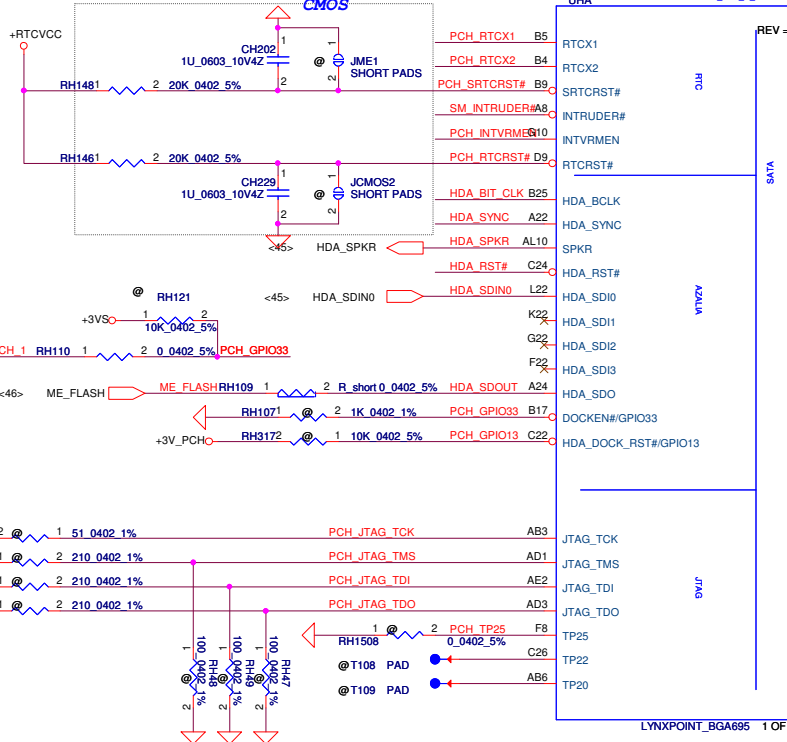


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Title DDRIII SO-DIMM B	
Size Custom	Document Number Y501 NM-A032
Date Wednesday, March 27, 2013	Rev 1.0
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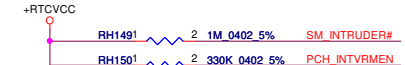
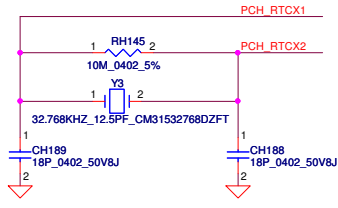
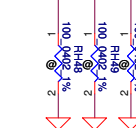
Place JUMPER under RAM door



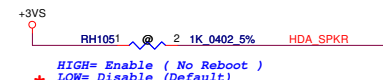
<37> CRT_SWITCH_1

<46> ME_FLASH

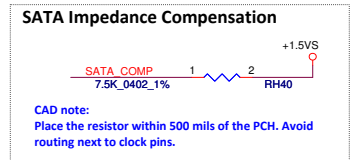
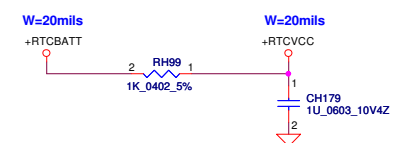
+3V_PCH



INTVRMEN
 * H : Integrated VRM enable (Default)
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)

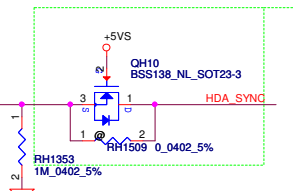
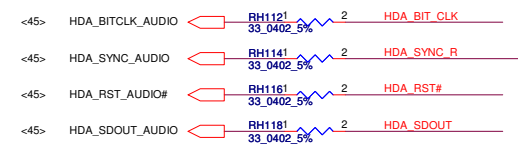


* HIGH = Enable (No Reboot)
 * LOW = Disable (Default)

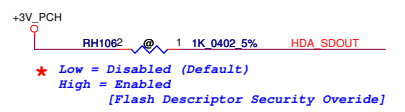


SATA Impedance Compensation
 CAD note:
 Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

HDA AUDIO

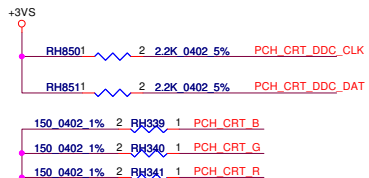


<Intel update spec>
 If RH1509 = stuff
 RH1353 = @
 QH10 = @
 RH108 = @
 This signal has a weak internal pull-down
 On Die PLL VR Select is supplied by
 1.5V when sampled high (Default)
 1.8V when sampled low
 Needs to be pulled High for Chief River platform

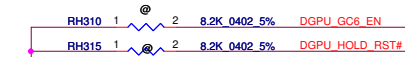
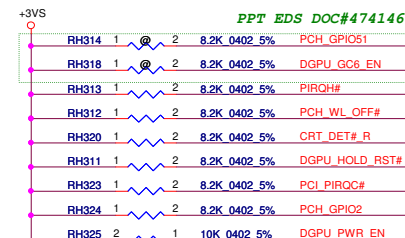
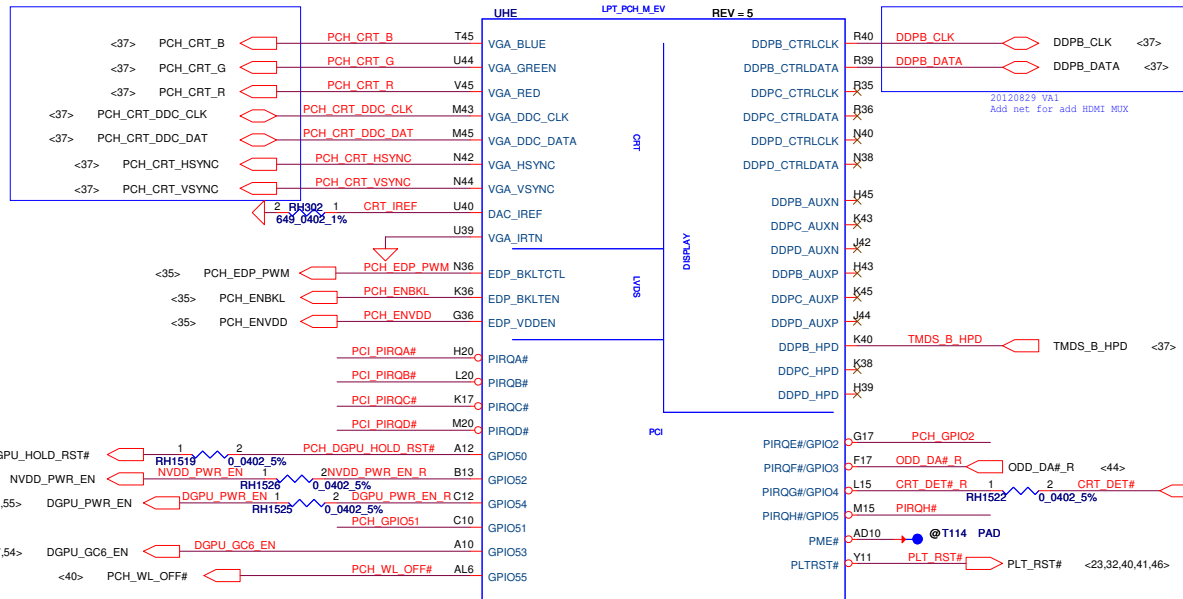


* Low = Disabled (Default)
 * High = Enabled
 [Flash Descriptor Security Override]

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Date:	Wednesday, March 27, 2013	Sheet	13	of 69

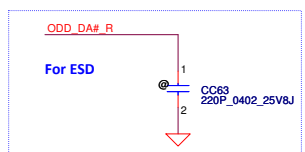
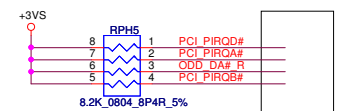
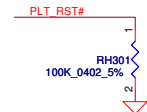


20120829 VAL
Add net for add CRT MIX



A16 swap override Strap/Top-Block Swap Override jumper

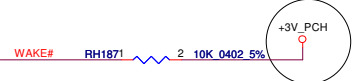
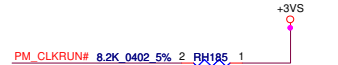
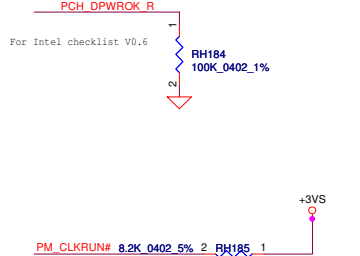
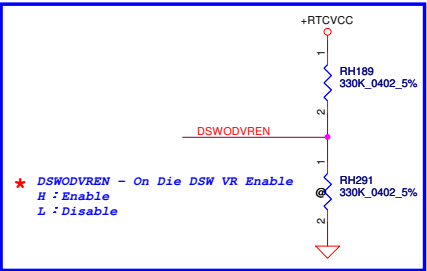
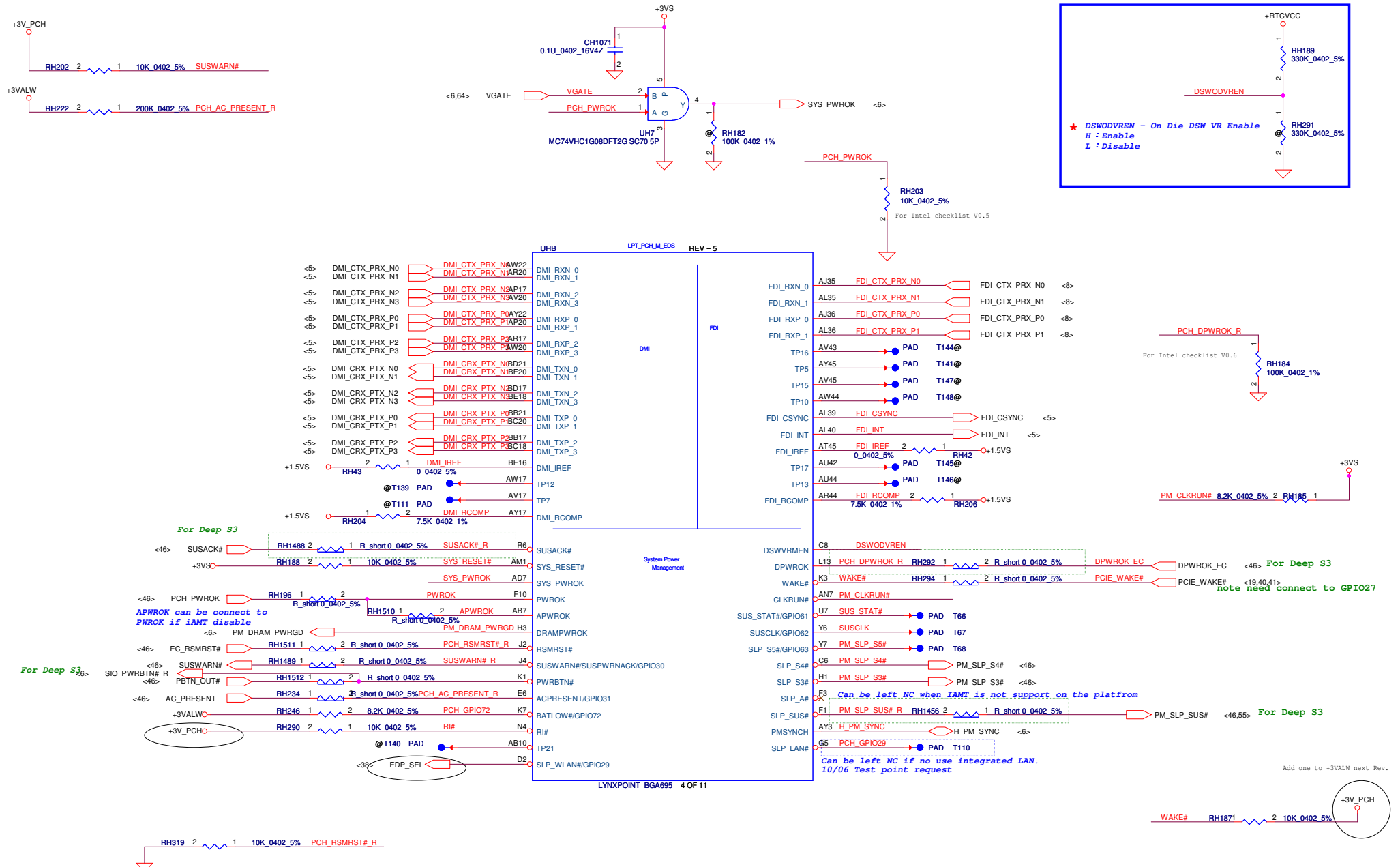
PCI_GNT3#	<p>Low = A16 swap override/Top-Block Swap Override enabled</p> <p>**High=Default</p>
------------------	---



PCH_GPIOS1 RH307 1 @ 2 1K 0402 5%

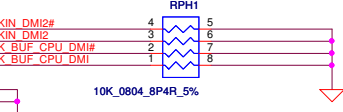
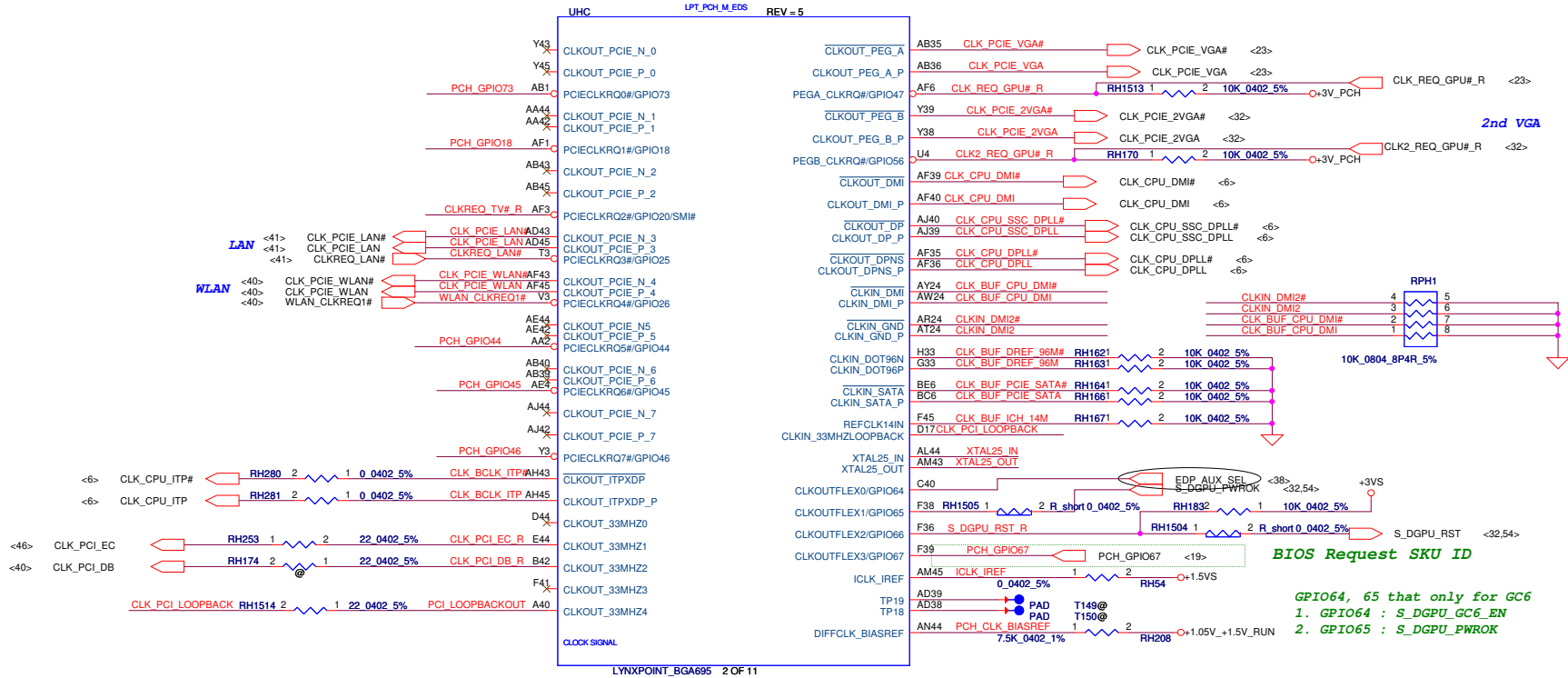
Boot BIOS Strap

BBS_BIT1 (GPIOS1)	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
*	1	SPI



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Size	Document Number	Rev	
Custom	Y501 NM-A032	1.0	
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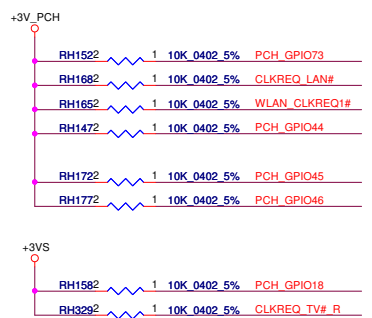
Add one to +3VALW next. Rev.



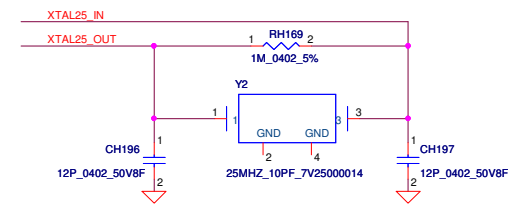
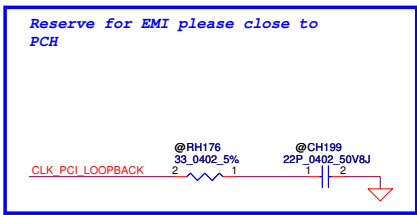
BIOS Request SKU ID

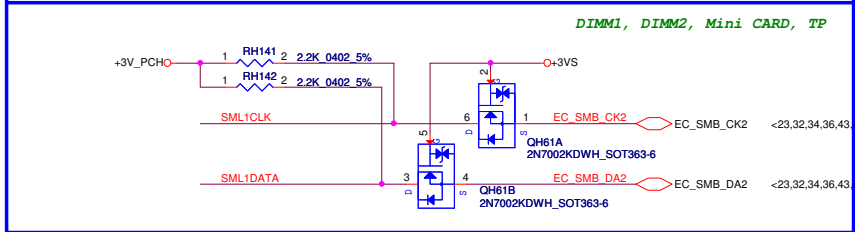
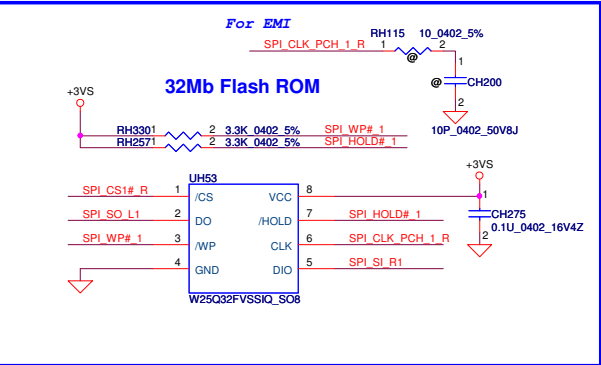
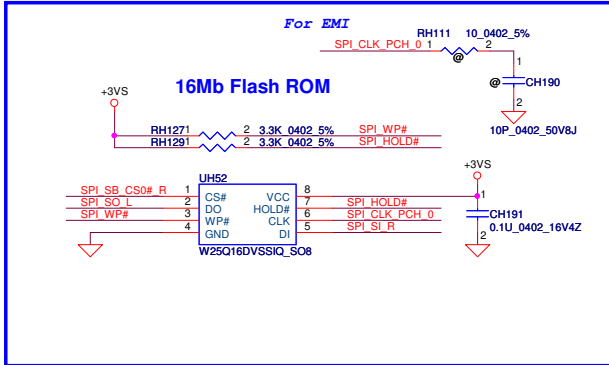
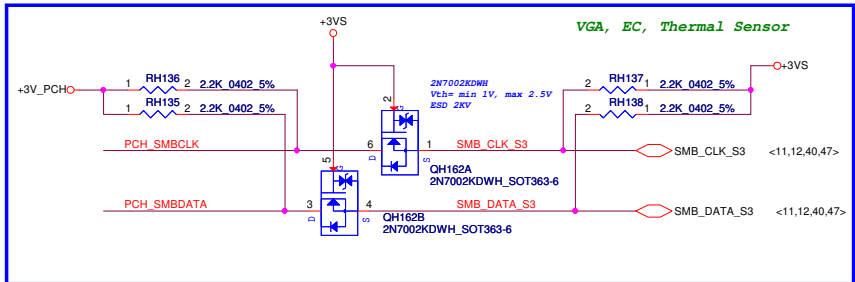
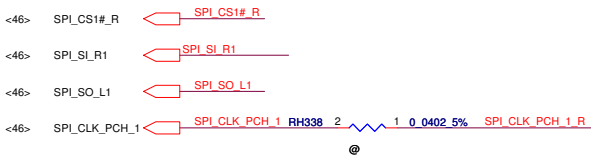
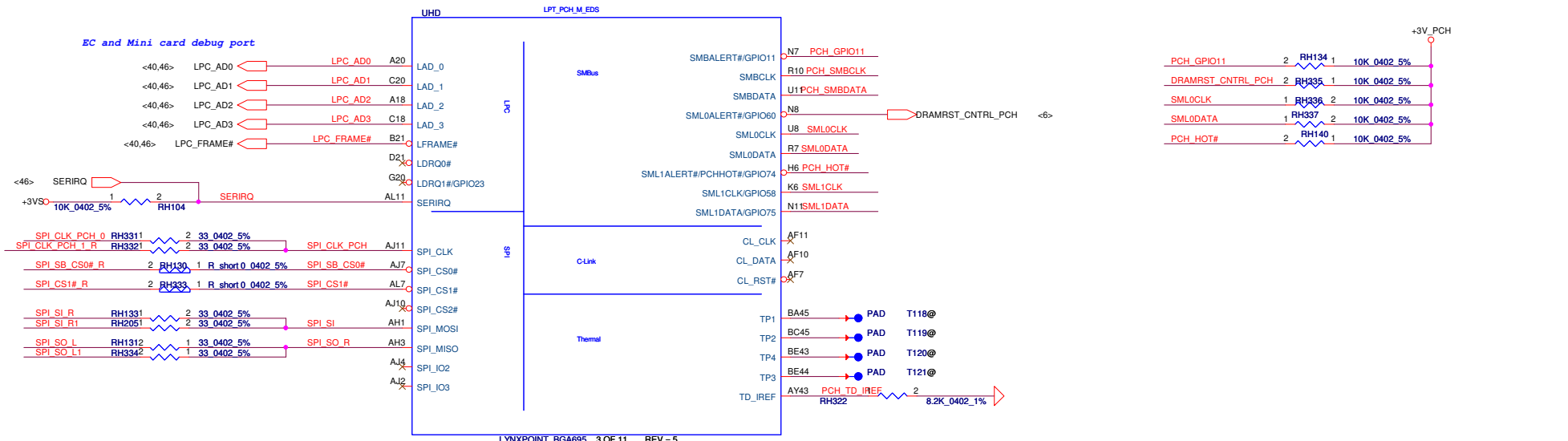
GPIO64, 65 that only for GC6

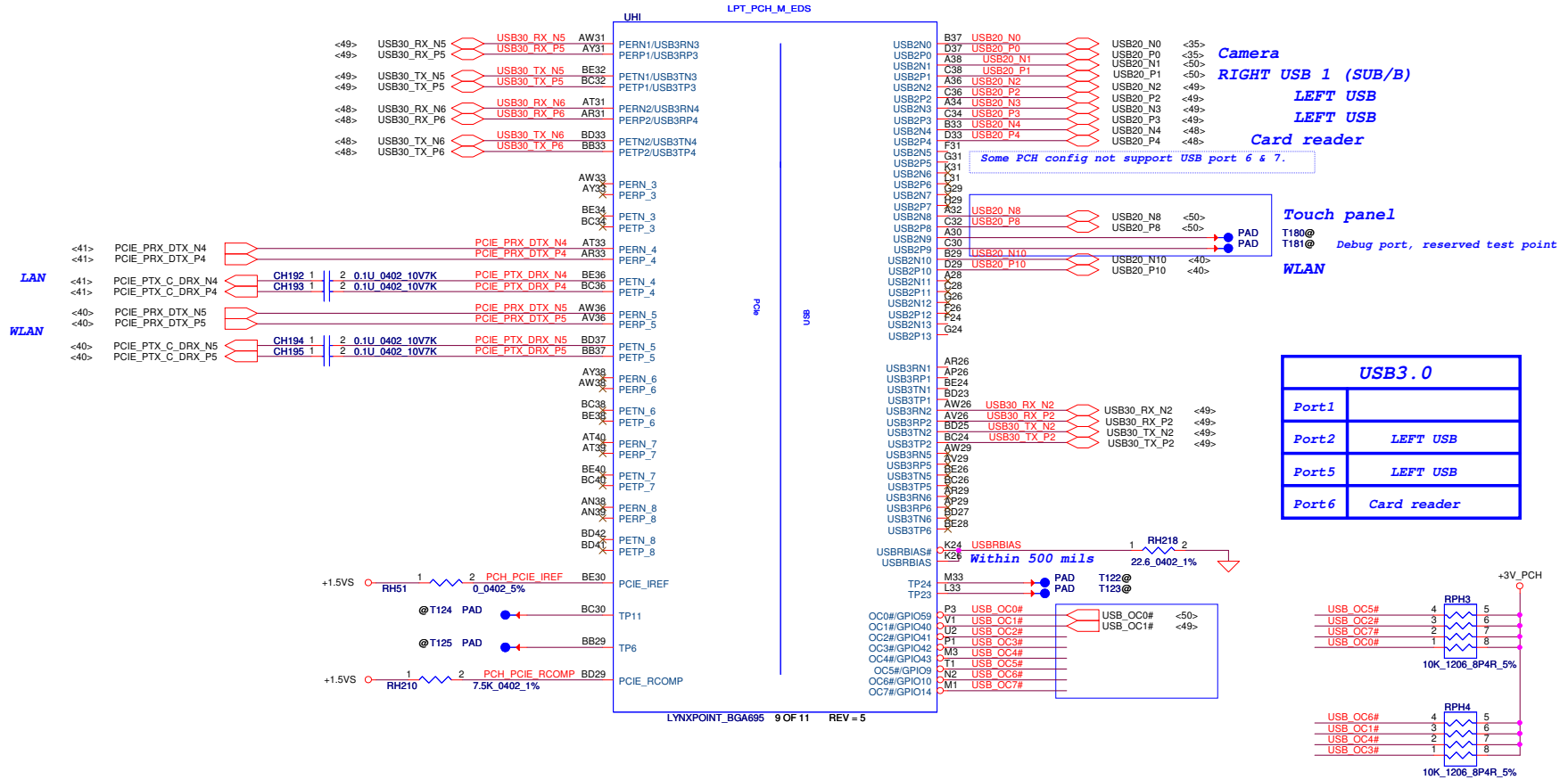
- GPIO64 : S_DGPU_GC6_EN
- GPIO65 : S_DGPU_PWROK



Change C196, C197 value of Cap from 33pF to 10pF for TXC recommend

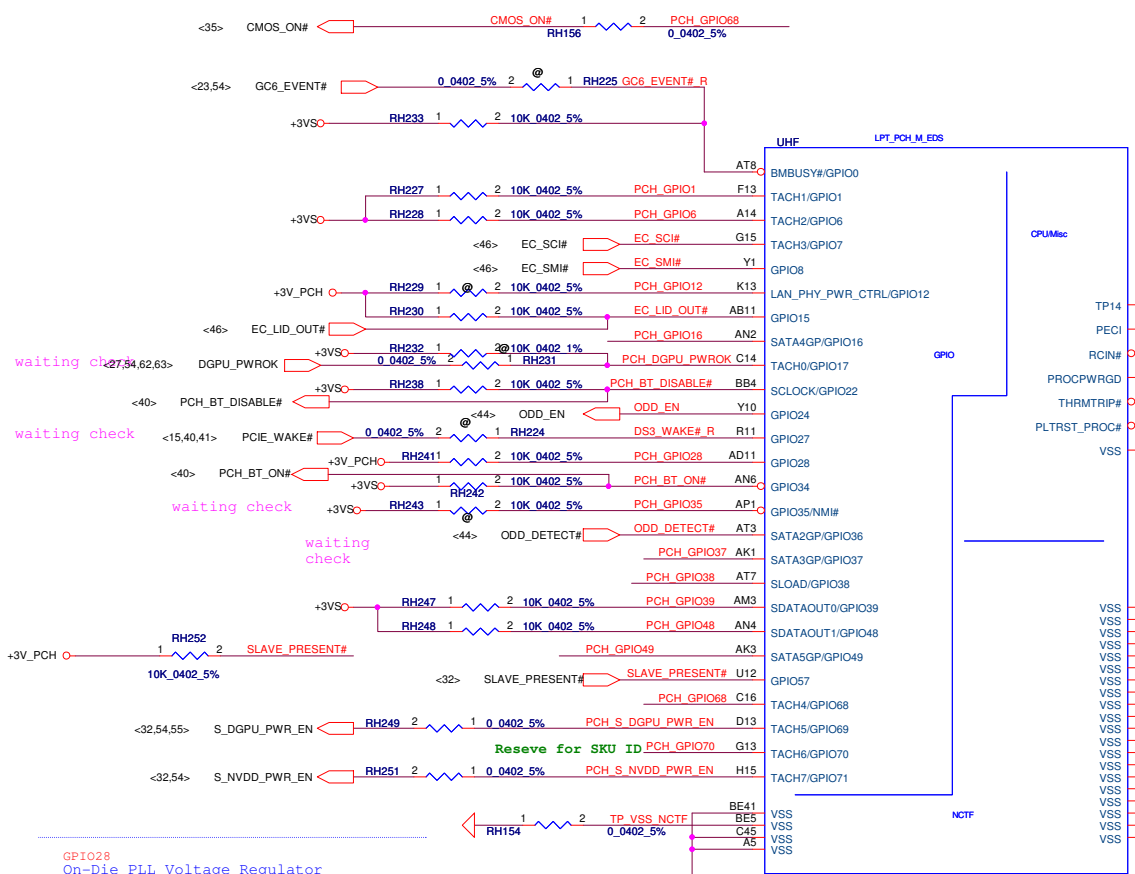






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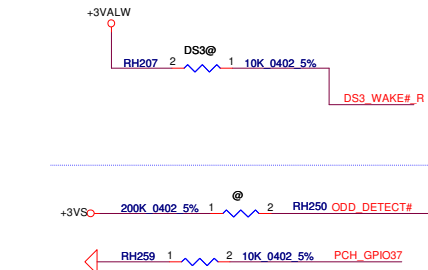




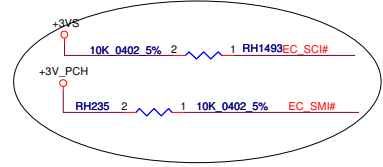
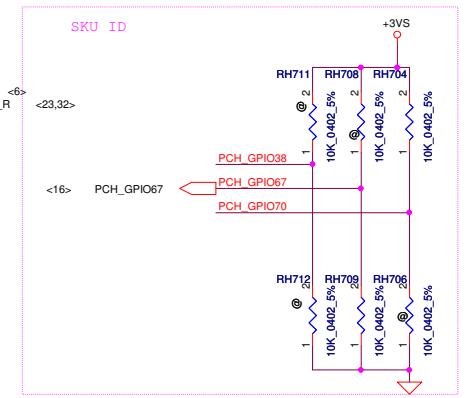
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

- H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



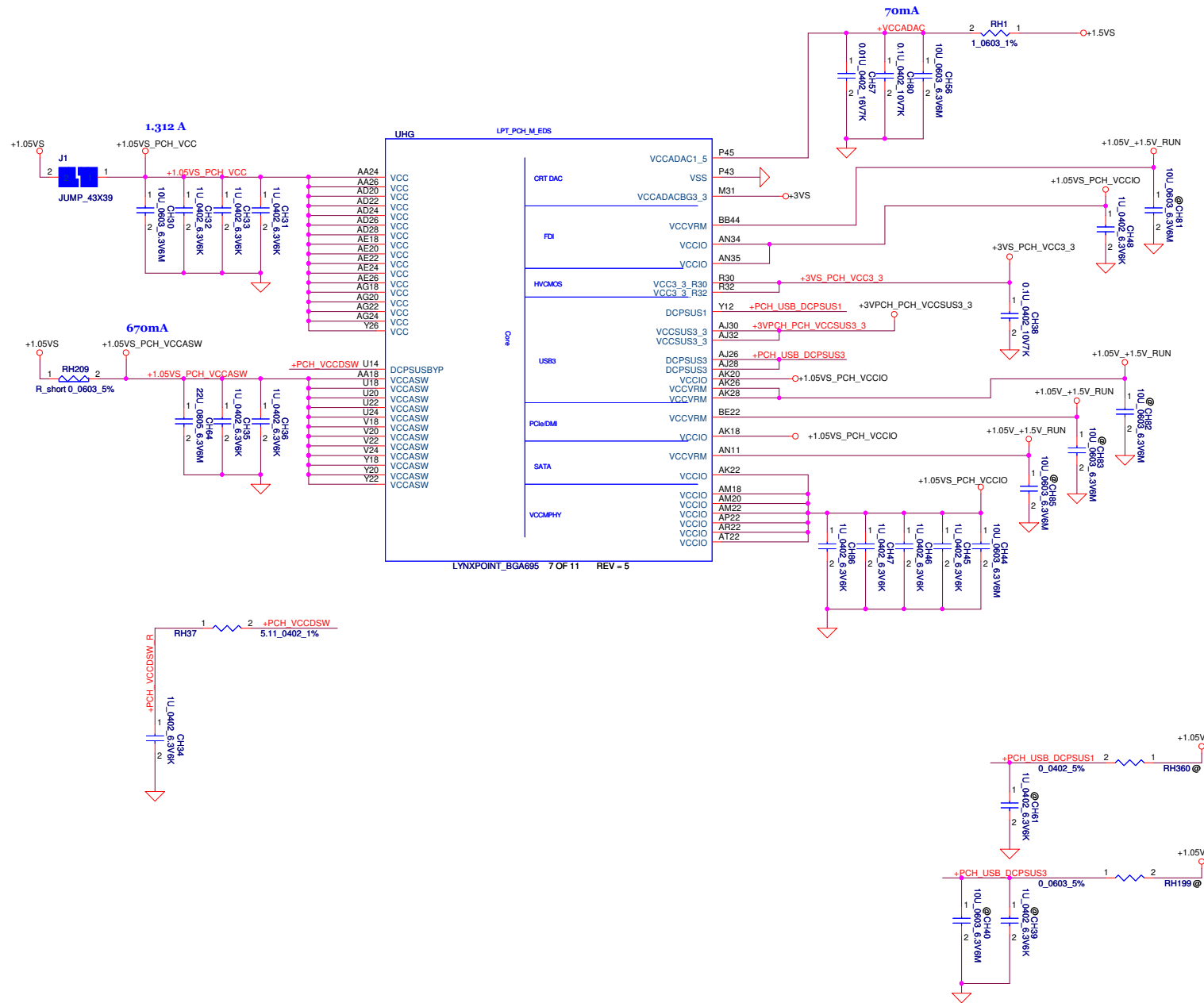
Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
			X
			X
			X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1



Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

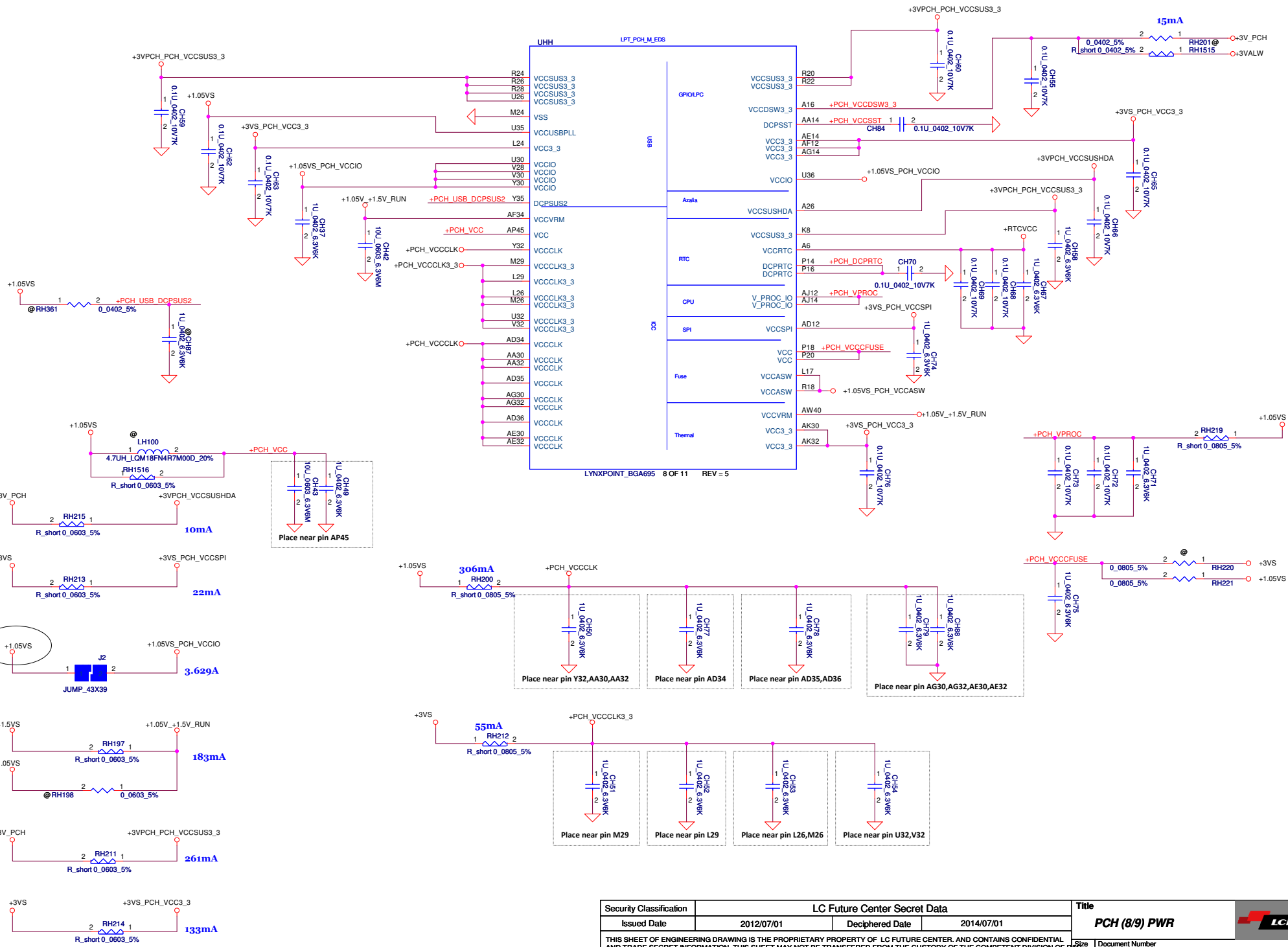
Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals					
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	PCIE 9	PCIE 10	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)									(00)	(00)						
				USB3 3	USB3 4									PCIE 1	PCIE 2						
				(01)	(01)									(01)	(01)						

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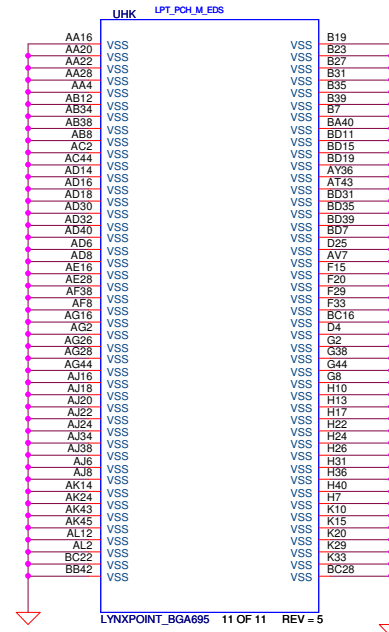
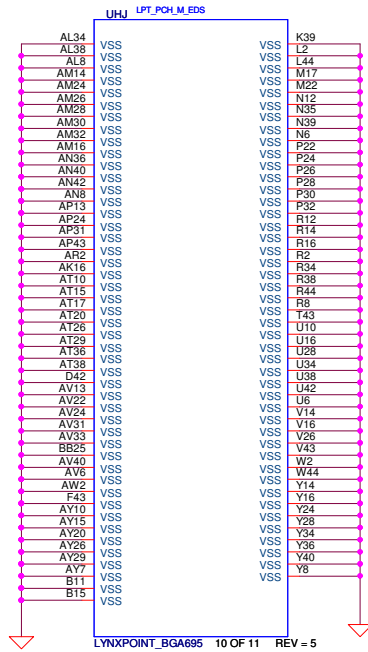
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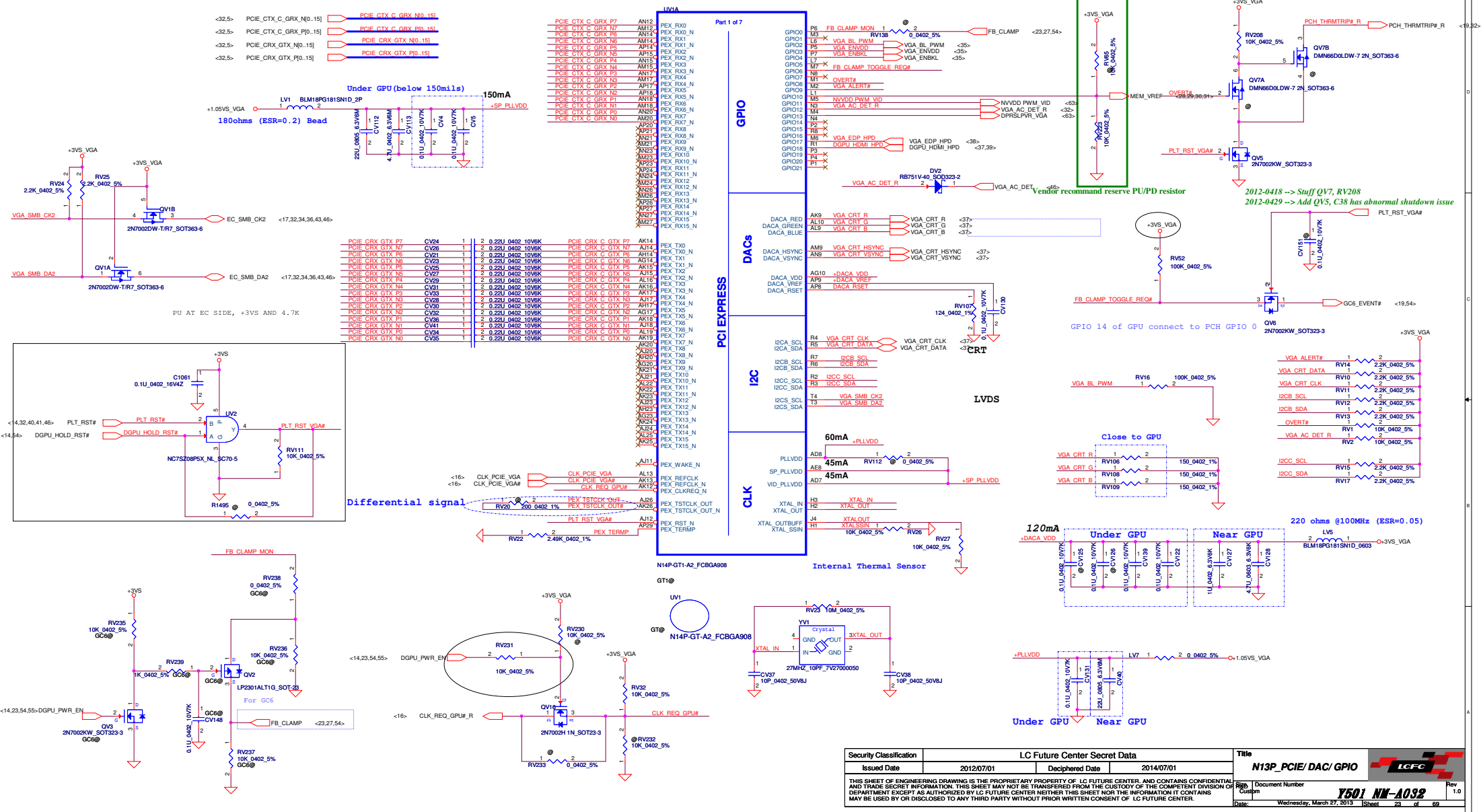
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						Y501 NM-A032	Rev 1.0
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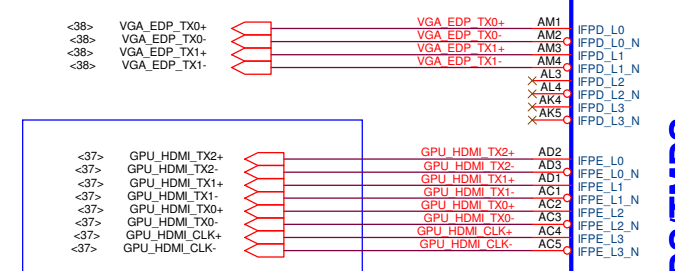
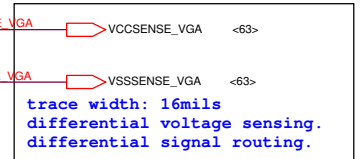
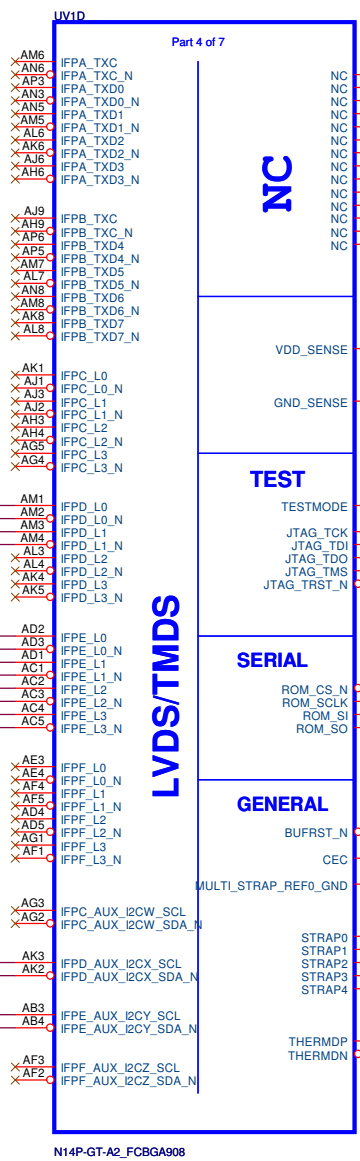


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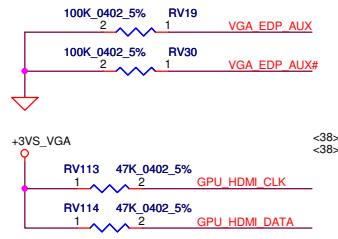




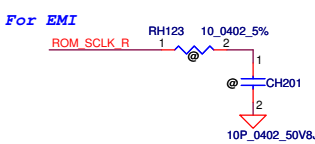
Security Classification	LC Future Center Secret Data		Title	 N13P_PCIE/ DAC/ GPIO
Issued Date	2012/07/01	Deciphered Date	2014/07/01	
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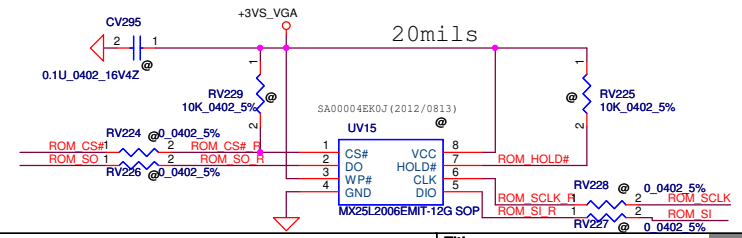
20120829 VA1
Change net name for add HDMI MUX



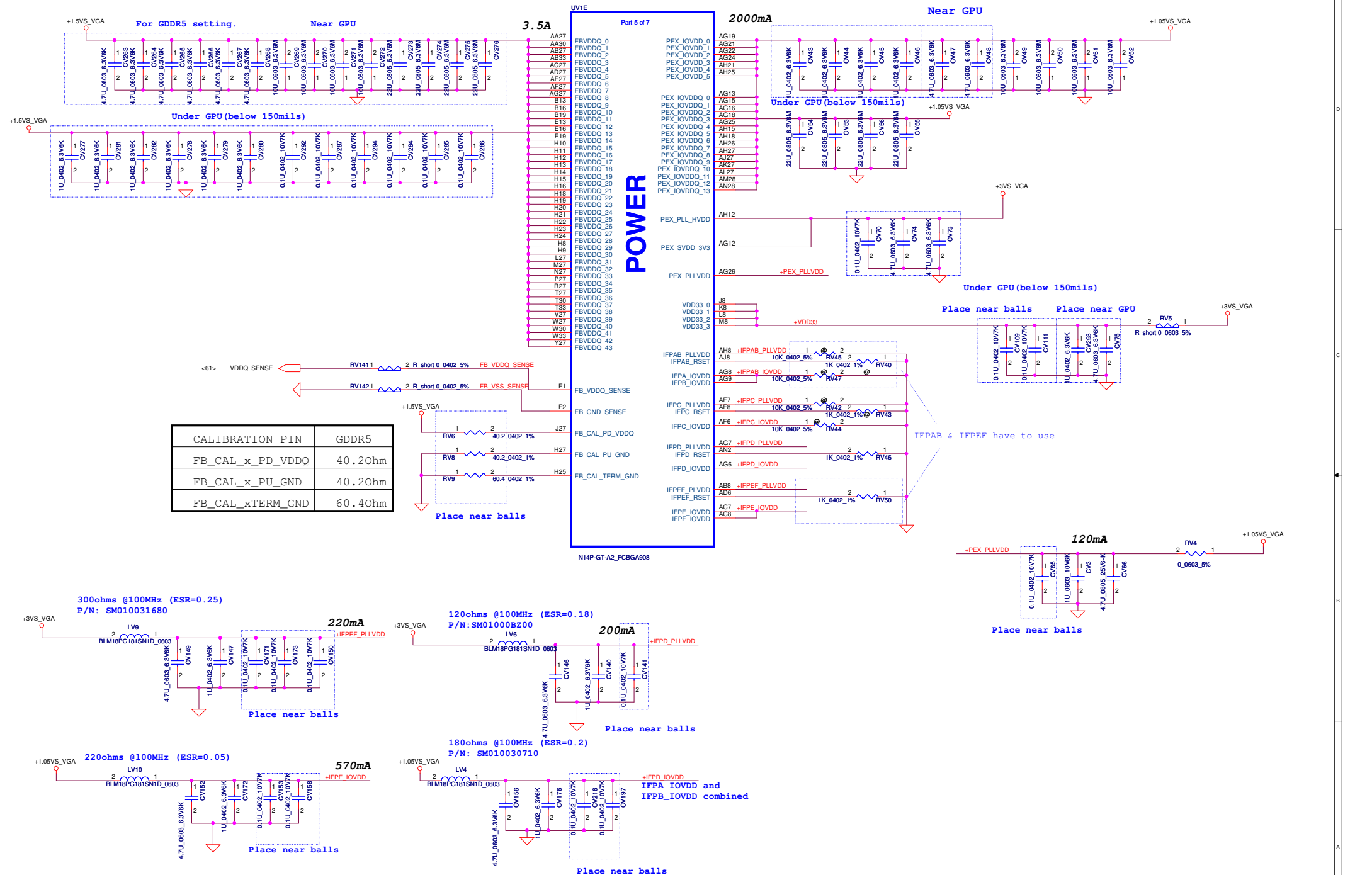
HDMI
20120829 VA1
Change net name for add HDMI MUX



1MB SPI ROM FOR VBIOS ROM (SLI)

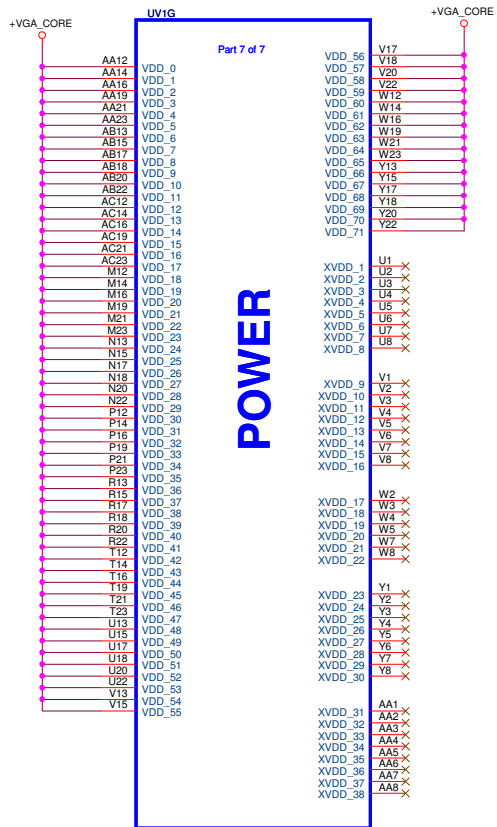


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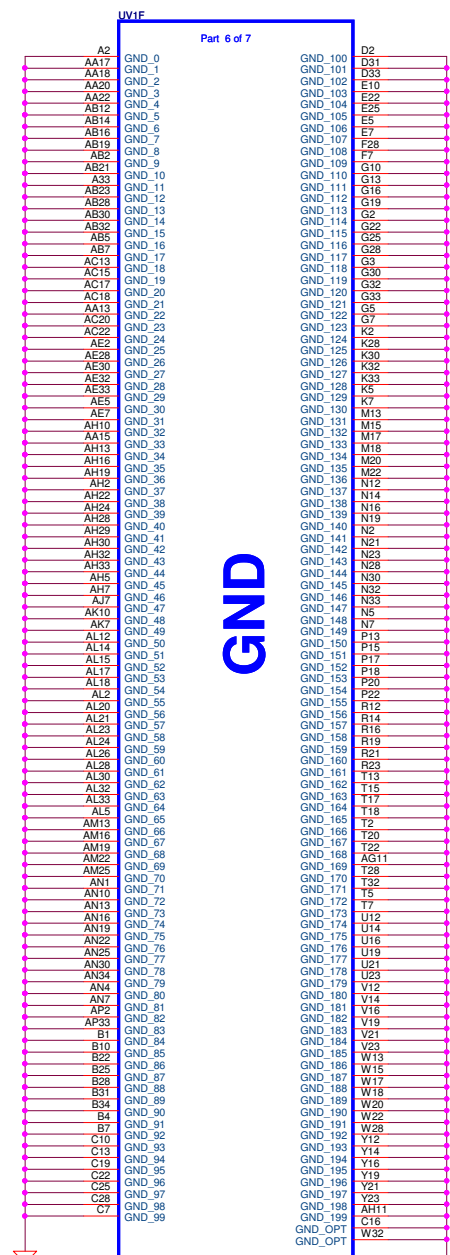



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.20ohm
FB_CAL_x_PU_GND	40.20ohm
FB_CAL_x_TERM_GND	60.40ohm

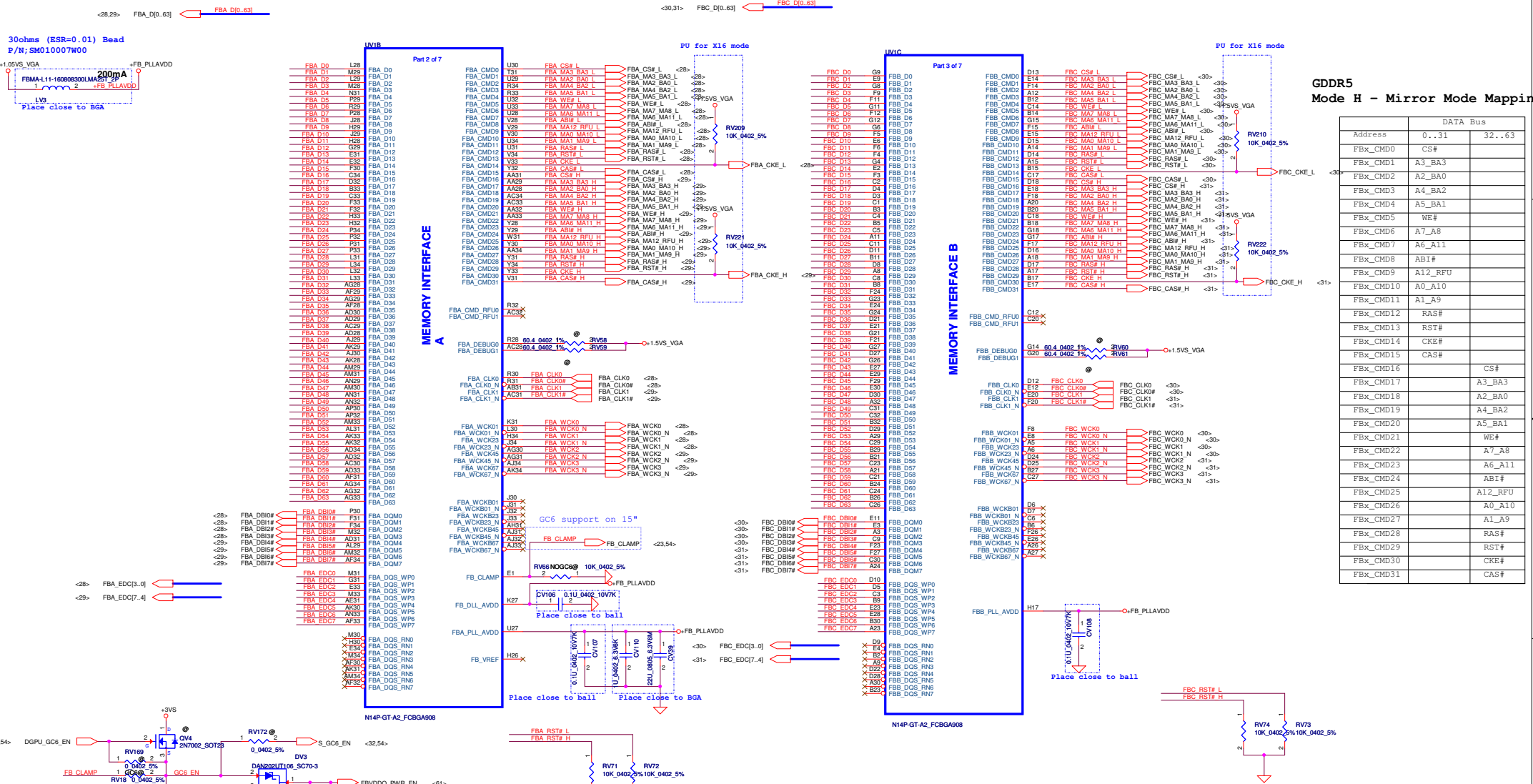
Security Classification	LC Future Center Secret Data		Title	 N13P_Power
Issued Date	2012/07/01	Deciphered Date	2014/07/01	
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N13P-GT1-A2_FCBGA908



Security Classification	LC Future Center Secret Data		Title	N13P-GT1-A2_FCBGA908
Issued Date	2012/07/01	Deciphered Date	2014/07/01	N13P-GT1-A2_FCBGA908
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Size	Document Number	Y501 NM-A032		Rev 1.0
Date:	Wednesday, March 27, 2013	Sheet	26	of 69

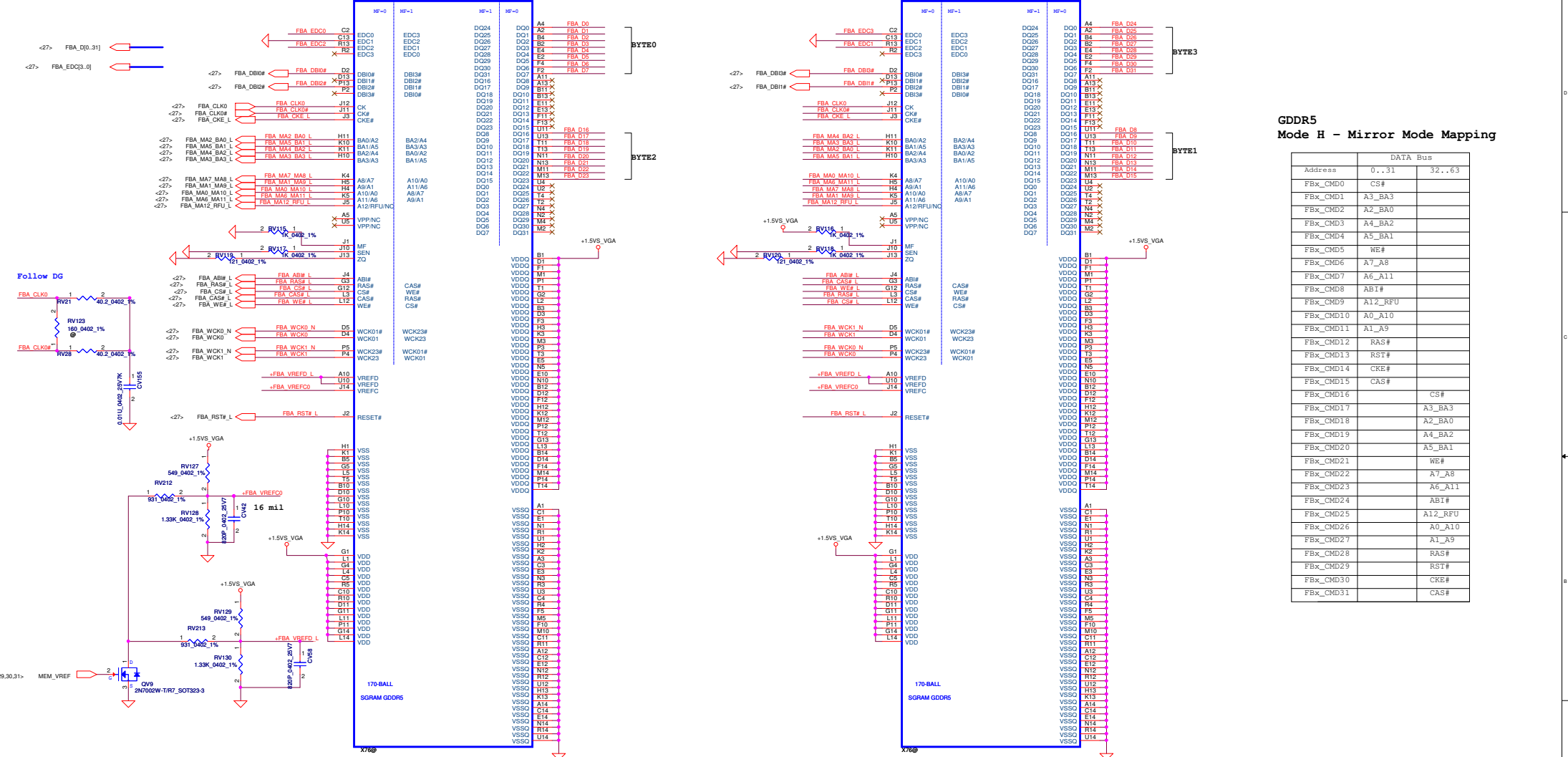


GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus
Fbx_CMD0	CS#
Fbx_CMD1	A3_BA3
Fbx_CMD2	A2_BA0
Fbx_CMD3	A4_BA2
Fbx_CMD4	A5_BA1
Fbx_CMD5	WE#
Fbx_CMD6	A7_A8
Fbx_CMD7	A6_A11
Fbx_CMD8	AB1#
Fbx_CMD9	A12_RFU
Fbx_CMD10	A0_A10
Fbx_CMD11	A1_A9
Fbx_CMD13	RAS#
Fbx_CMD15	CAS#
Fbx_CMD16	CS#
Fbx_CMD17	A3_BA3
Fbx_CMD18	A2_BA0
Fbx_CMD19	A4_BA2
Fbx_CMD20	A5_BA1
Fbx_CMD21	WE#
Fbx_CMD22	A7_A8
Fbx_CMD23	A6_A11
Fbx_CMD24	AB1#
Fbx_CMD25	A12_RFU
Fbx_CMD26	A0_A10
Fbx_CMD27	A1_A9
Fbx_CMD28	RAS#
Fbx_CMD29	RST#
Fbx_CMD30	CKE#
Fbx_CMD31	CAS#

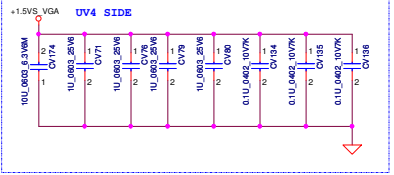
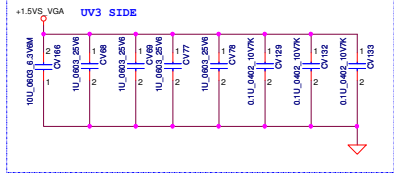
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Issued Date	2012/07/01	Deciphered Date	2014/07/01
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Memory - Lower 32 bits



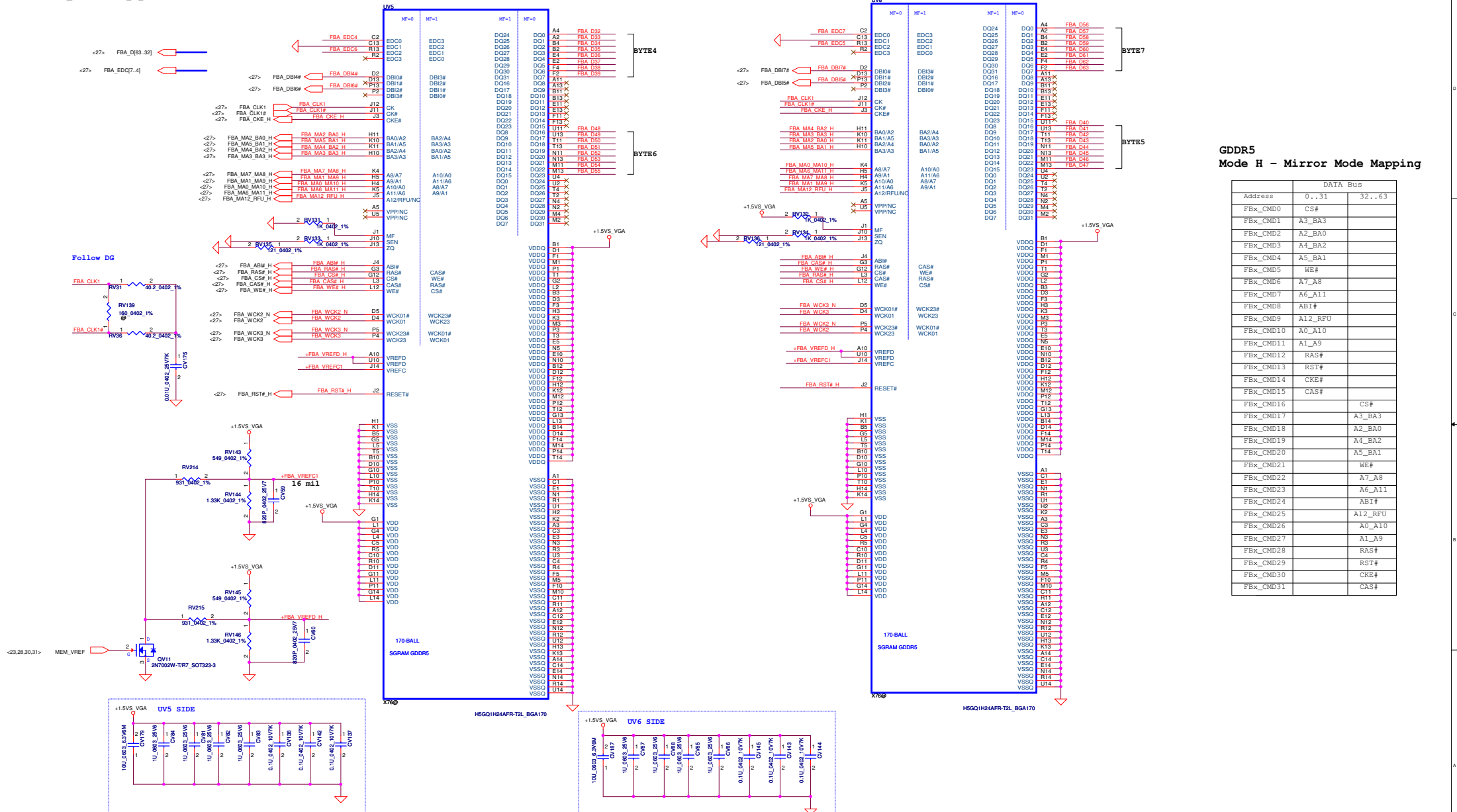
GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus
0..31	32..63
FBx_CMD0	CS#
FBx_CMD1	A3_BA3
FBx_CMD2	A2_BA0
FBx_CMD3	A4_BA2
FBx_CMD4	A5_BA1
FBx_CMD5	WE#
FBx_CMD6	A7_A8
FBx_CMD7	A6_A11
FBx_CMD8	AB1#
FBx_CMD9	A12_RFU
FBx_CMD10	A0_A10
FBx_CMD11	A1_A9
FBx_CMD12	RAS#
FBx_CMD13	RST#
FBx_CMD14	CKE#
FBx_CMD15	CAS#
FBx_CMD16	
FBx_CMD17	A3_BA3
FBx_CMD18	A2_BA0
FBx_CMD19	A4_BA2
FBx_CMD20	A5_BA1
FBx_CMD21	WE#
FBx_CMD22	A7_A8
FBx_CMD23	A6_A11
FBx_CMD24	AB1#
FBx_CMD25	A12_RFU
FBx_CMD26	A0_A10
FBx_CMD27	A1_A9
FBx_CMD28	RAS#
FBx_CMD29	RST#
FBx_CMD30	CKE#
FBx_CMD31	CAS#



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Memory - Upper 32 bits

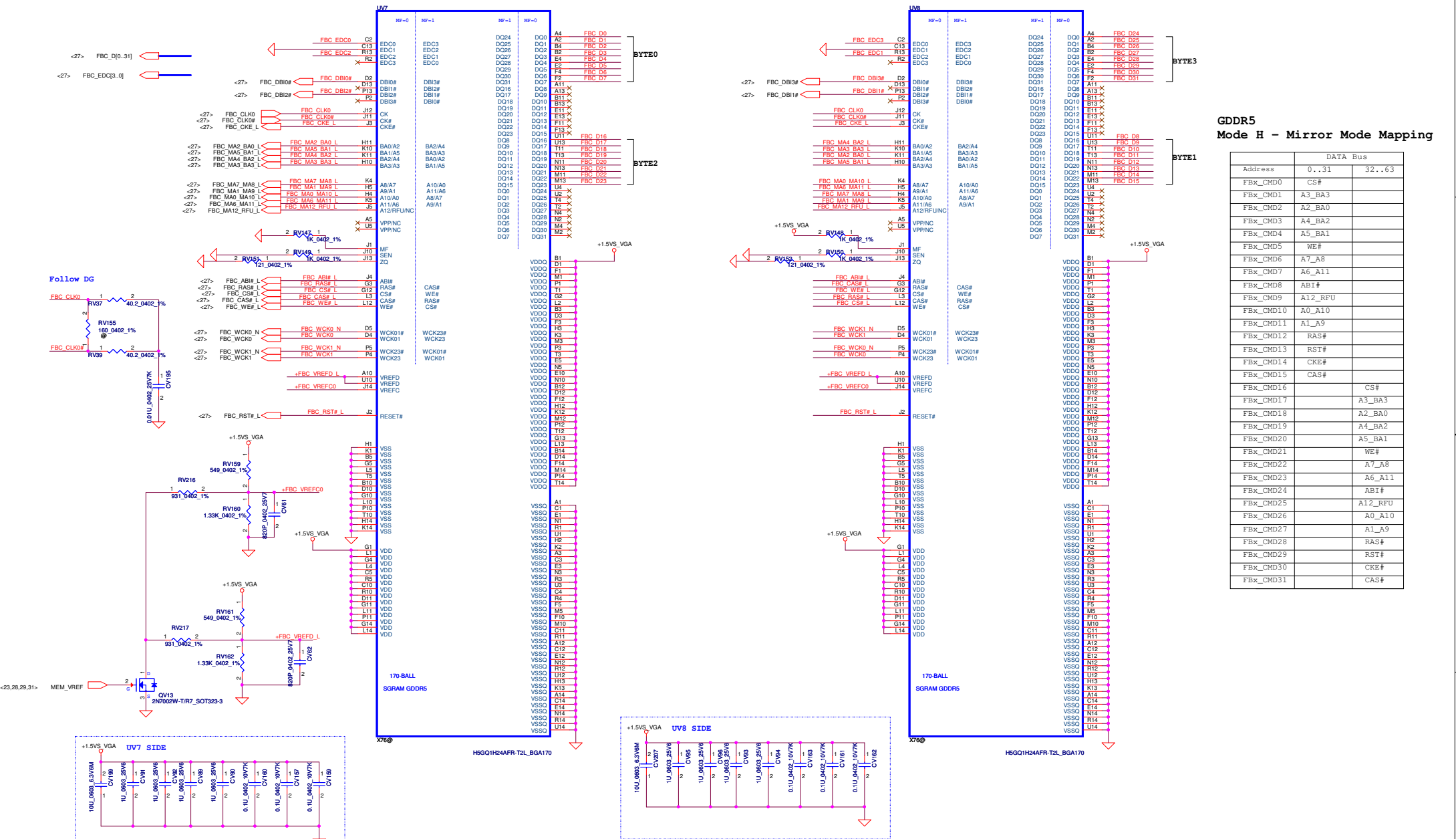


GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus
Fbx_CMD0	CS#
Fbx_CMD1	A3_BA3
Fbx_CMD2	A2_BA0
Fbx_CMD3	A4_BA2
Fbx_CMD5	A5_BA1
Fbx_CMD6	A7_A8
Fbx_CMD7	A6_A11
Fbx_CMD8	AB1#
Fbx_CMD9	A12_RFU
Fbx_CMD10	A0_A10
Fbx_CMD11	A1_A9
Fbx_CMD12	RAS#
Fbx_CMD13	RST#
Fbx_CMD14	CKE#
Fbx_CMD15	CAS#
Fbx_CMD16	CS#
Fbx_CMD17	A3_BA3
Fbx_CMD18	A2_BA0
Fbx_CMD19	A4_BA2
Fbx_CMD20	A5_BA1
Fbx_CMD21	WE#
Fbx_CMD22	A7_A8
Fbx_CMD23	A6_A11
Fbx_CMD24	AB1#
Fbx_CMD25	A12_RFU
Fbx_CMD27	A1_A9
Fbx_CMD28	RAS#
Fbx_CMD29	RST#
Fbx_CMD30	CKE#
Fbx_CMD31	CAS#

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Memory Partition C - Lower 32 bits

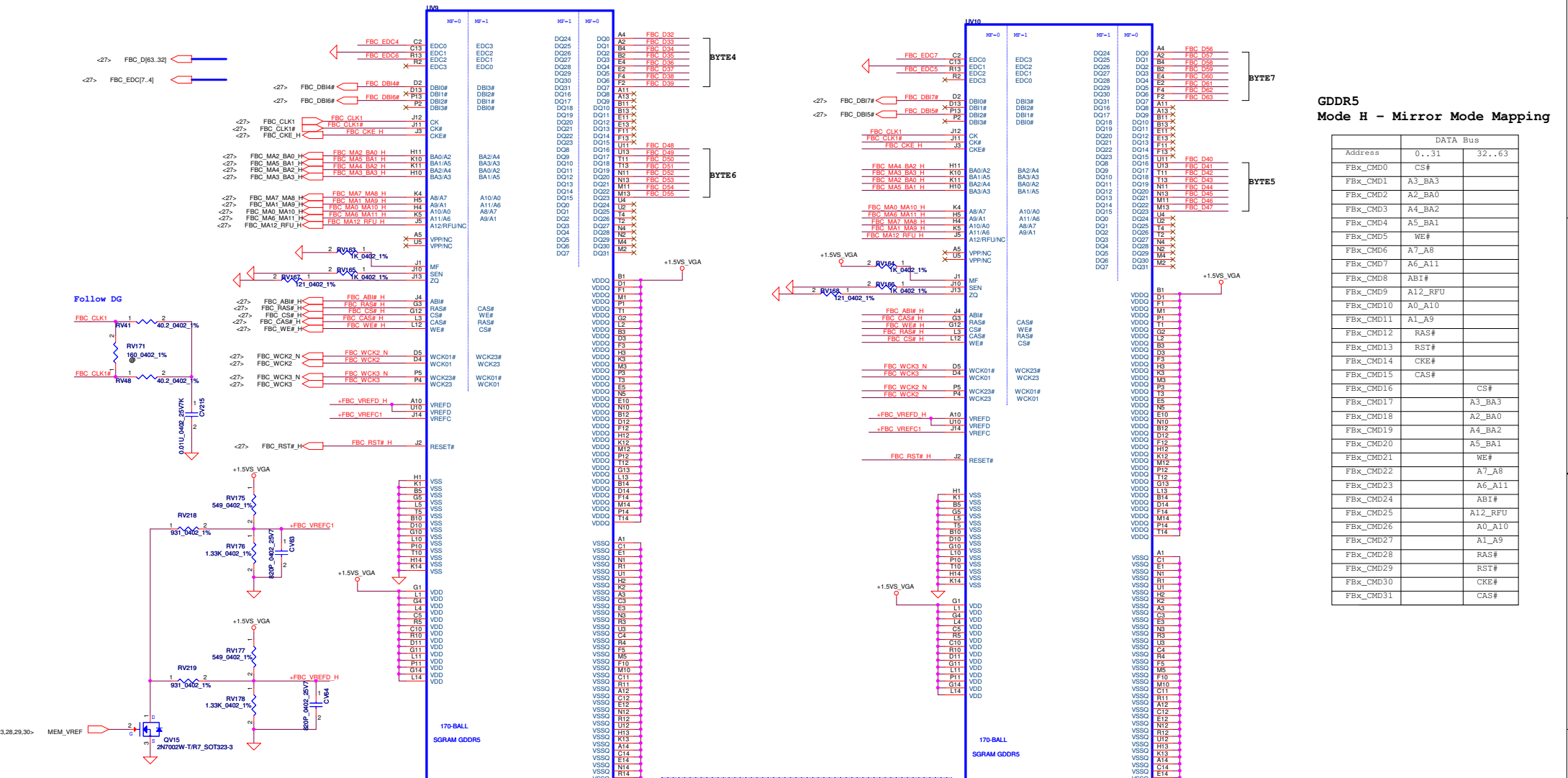


GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus	
FBX_CMD0	0..31	32..63
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	AB1#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		AB1#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

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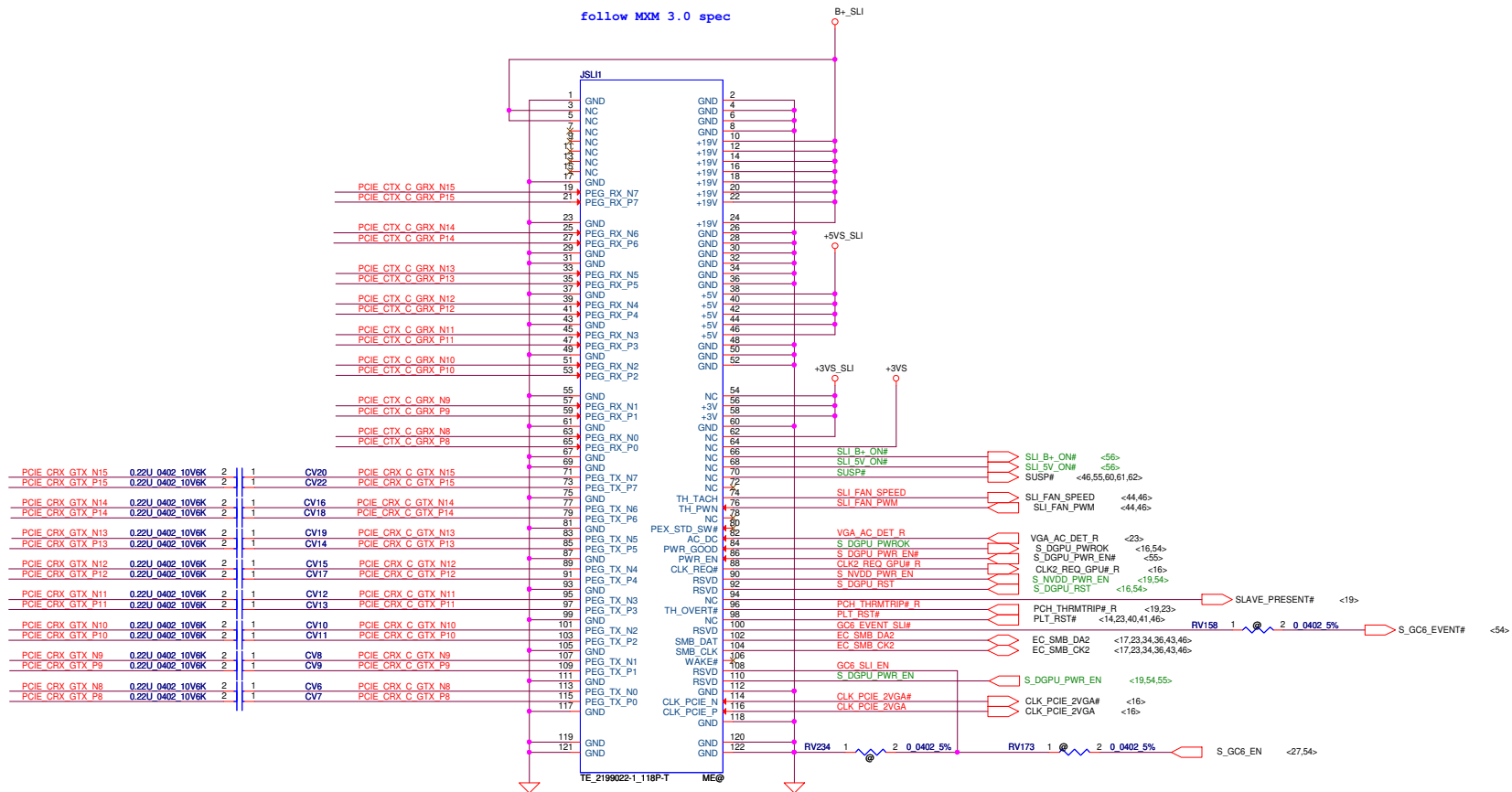
Memory Partition C - Upper 32 bits



GDDR5 Mode H - Mirror Mode Mapping

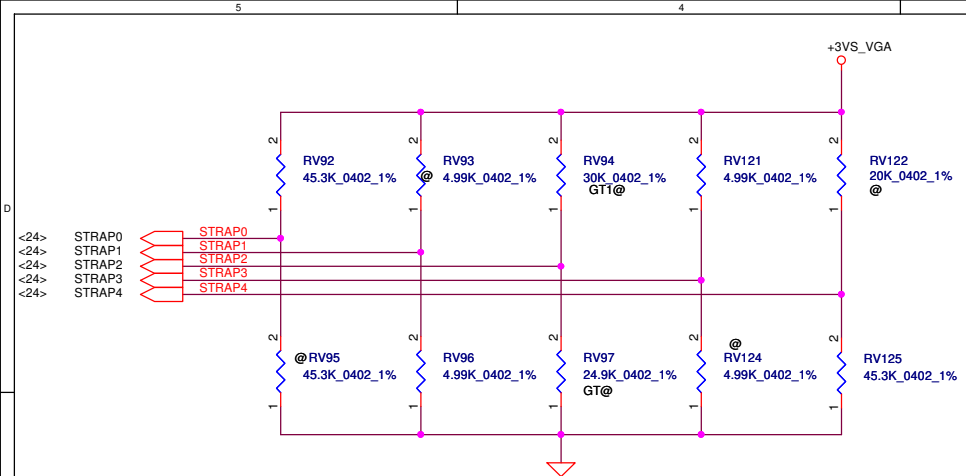
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RA5#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RA5#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		Title
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- 11/11 for 2nd VGA fan need to notice EC
- <23,5> PCIE_CTX_C_GRX_N[0..15] PCIE_CTX_C_GRX_N[0..15]
 - <23,5> PCIE_CTX_C_GRX_P[0..15] PCIE_CTX_C_GRX_P[0..15]
 - <23,5> PCIE_CRX_GTX_N[0..15] PCIE_CRX_GTX_N[0..15]
 - <23,5> PCIE_CRX_GTX_P[0..15] PCIE_CRX_GTX_P[0..15]

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	VGA MXM	
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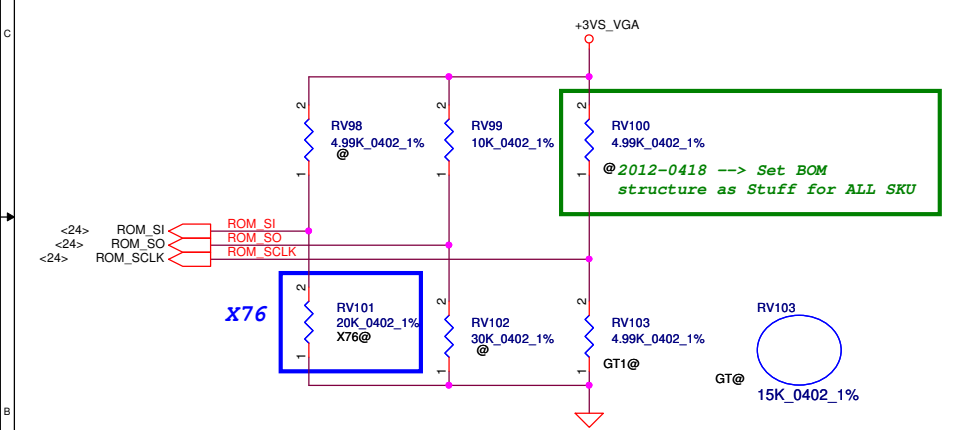


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present



3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

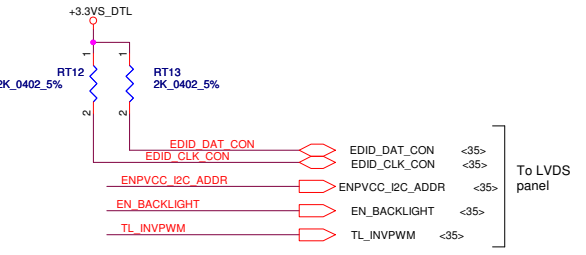
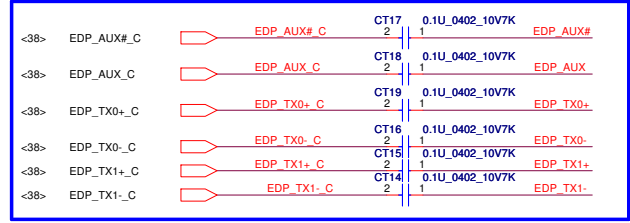
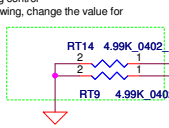
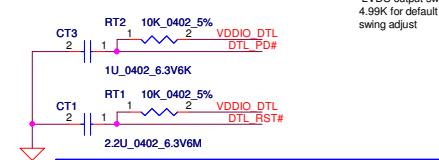
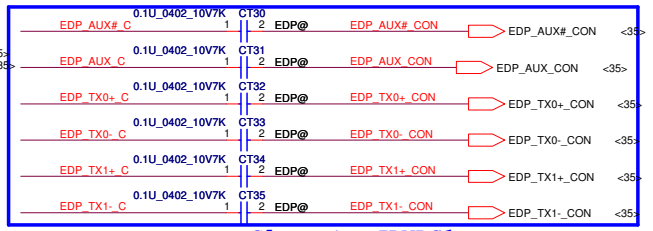
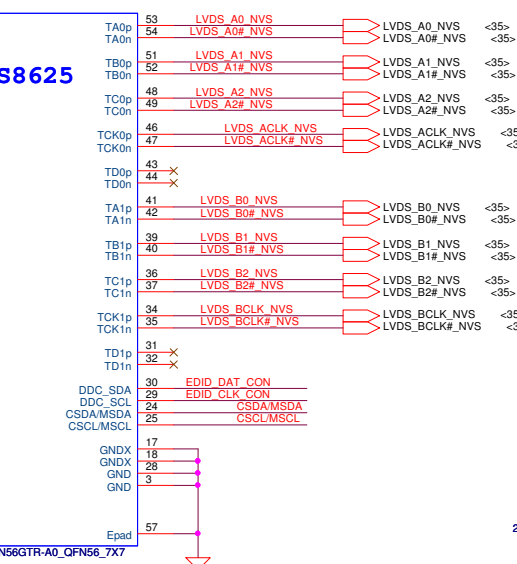
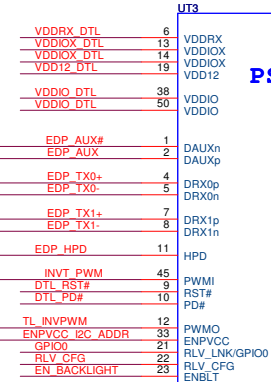
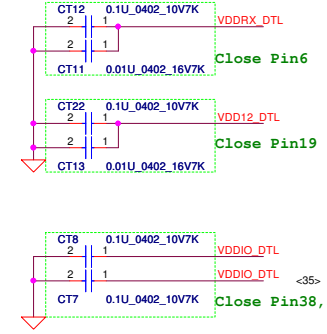
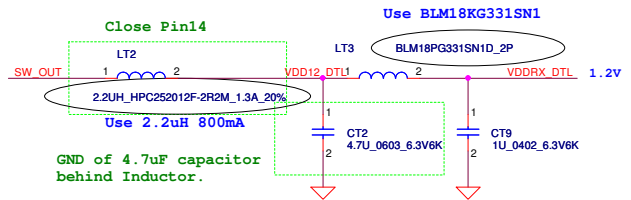
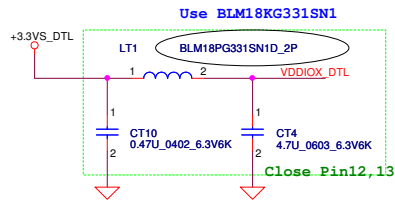
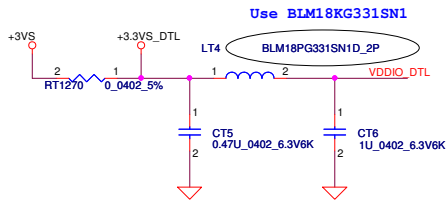
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	FB Memory (GDDR5)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K PD 15K (ROM not present) PD 35K (ROM present)	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K
		K4G10325FG-HC04 1G 32Mx32	PD 45K						
	H5GQ2H24MFR-T2C 2G 64Mx32	PD 25K							
	H5GQ1H24BFR-T2C 1G 32Mx32	PD 20K							
	H5GQ2H24AFR-T2C 2G 64Mx32	PD 25K							

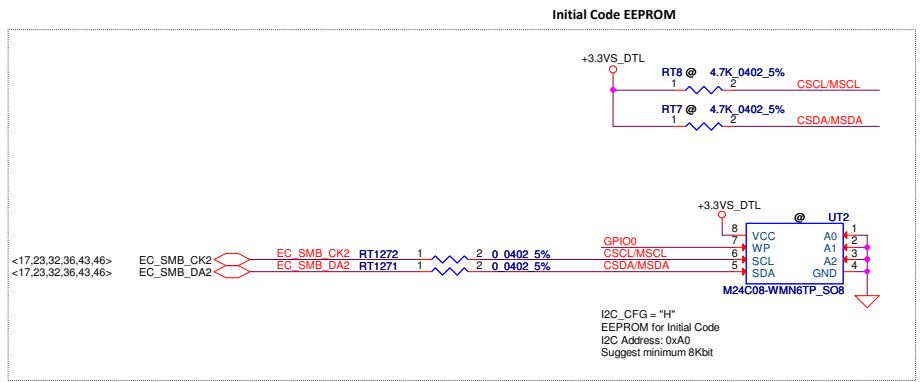
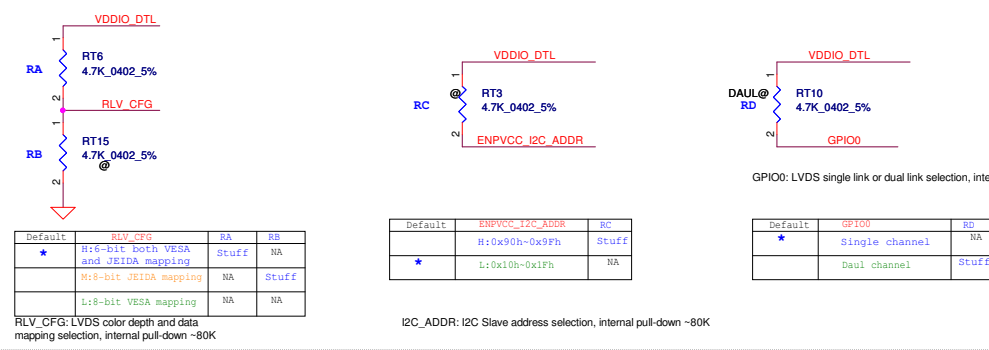
VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
	X76409JVL51 (1G 32Mx16)	SA00003RS0J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J EOL
	X76409JVL02 (2G 64Mx32)	SA00004GD1J
	X76409JVL52 (1G 32Mx16)	SA00003WL1J

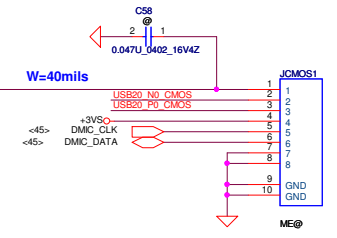
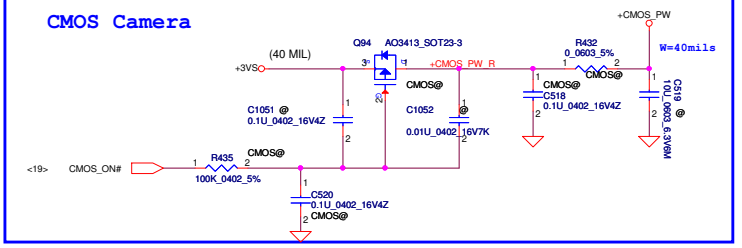
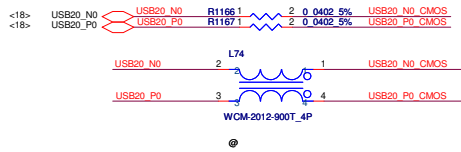
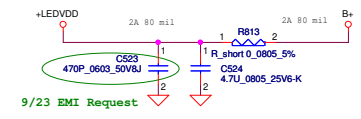
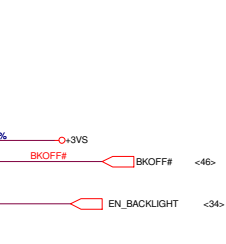
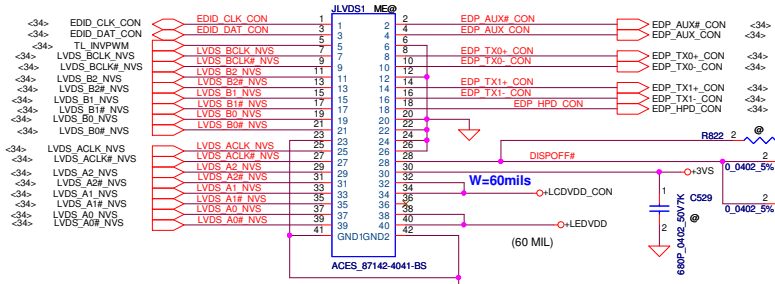
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Title: N13P_MISC
 Size: Custom
 Document Number: Y501 NM-A032
 Date: Wednesday, March 27, 2013
 Sheet: 33 of 69
 Rev: 1.0

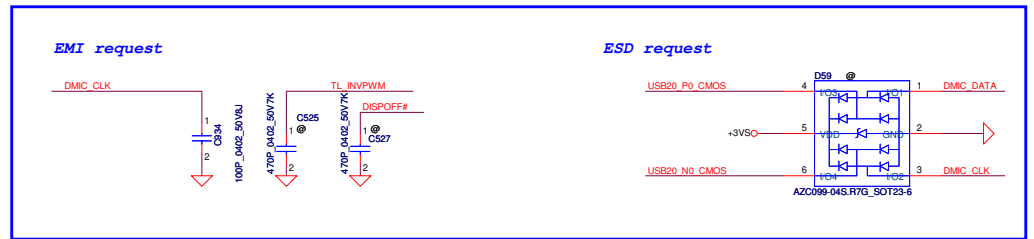
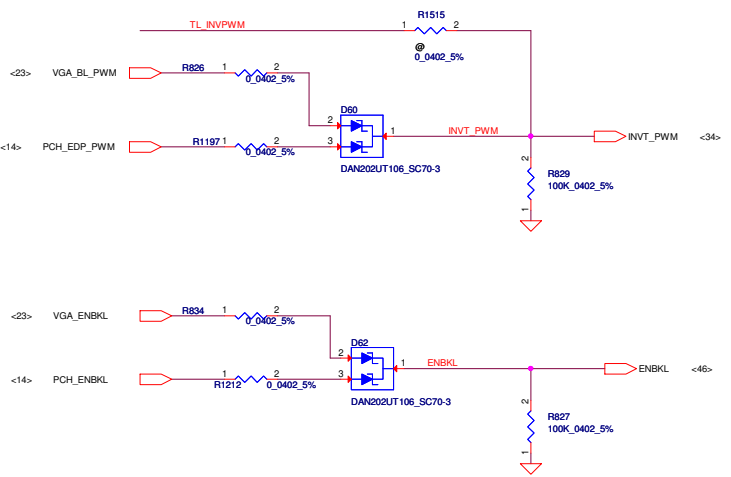
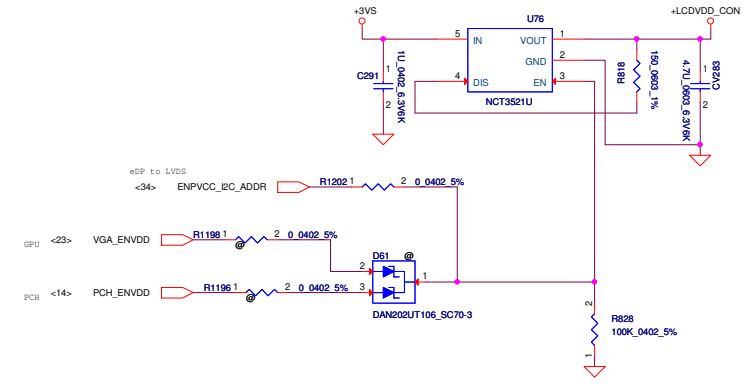


Power On Configuration





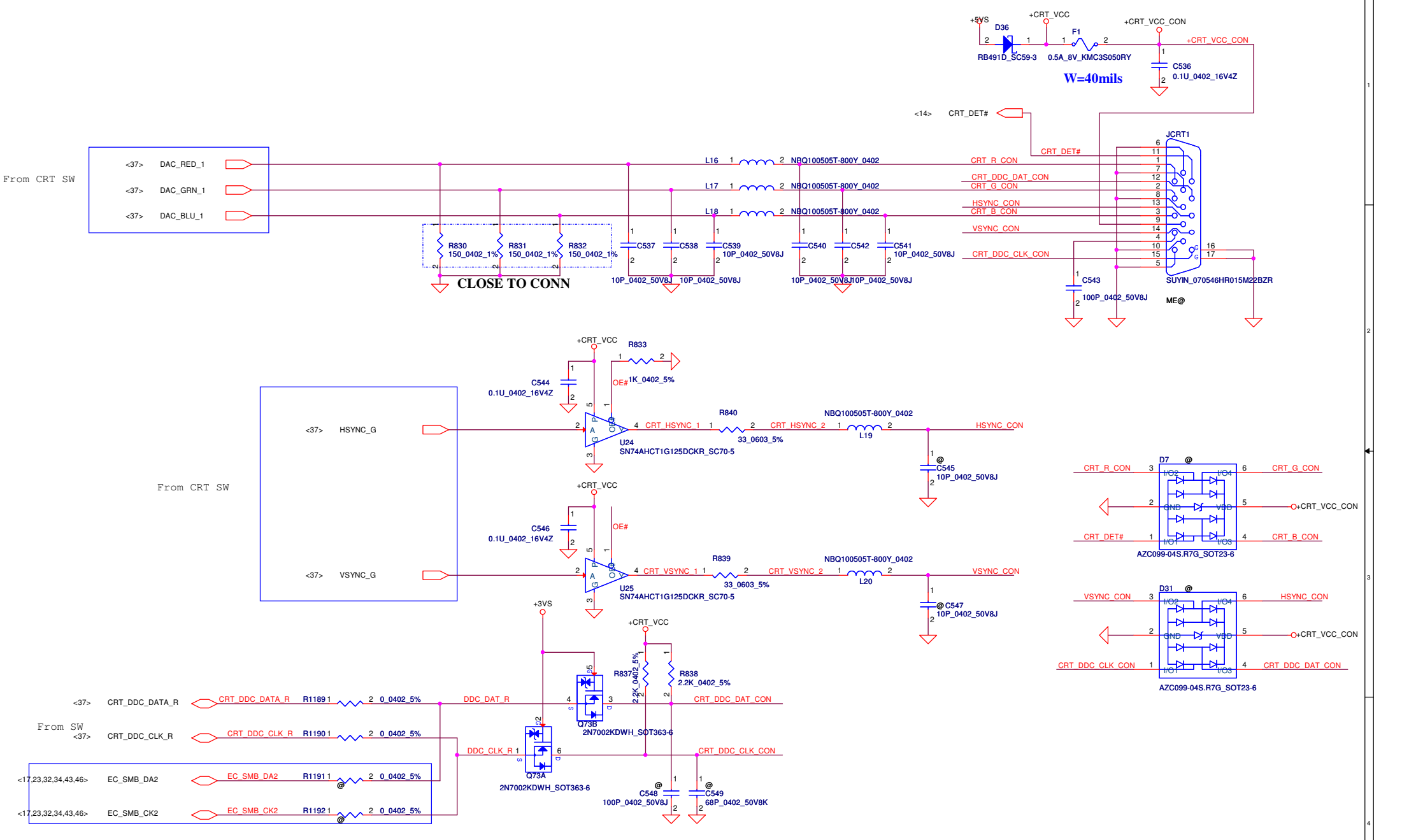
LCDVDD



LVDS LOAD SWITCH
1.9mS Typical Rise time, R_{ds} on 80m ohm

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Issued Date		2012/07/01		Deciphered Date	
		2014/07/01		Title	
				LVDS/ CMOS/ USB-ReDriver	
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				Date: Wednesday, March 27, 2013	
				Sheet 35 of 69	

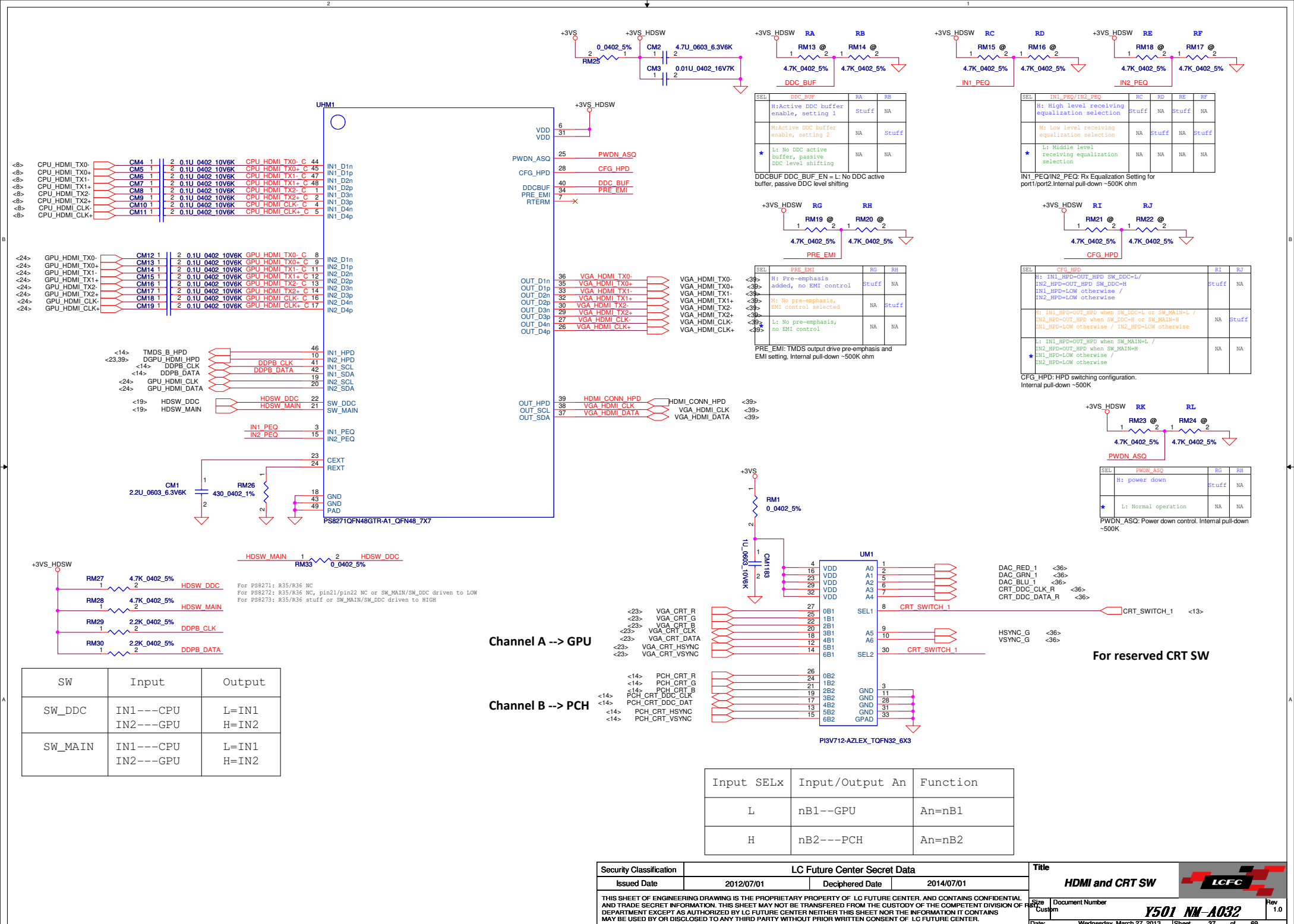
CRT Connector



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Issued Date	2012/07/01	Deciphered Date
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Title	CRT Connector	
Size	Document Number	Rev
Custom	Y501 NM-A032	1.0
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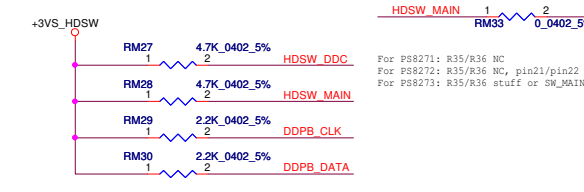
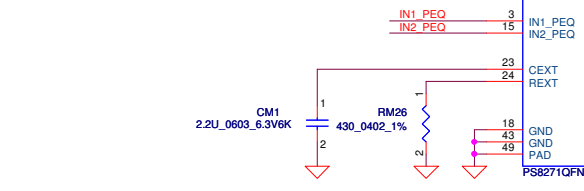




Pin	Component	Value	Function
<8>	CPU_HDMI_TX0+	CM4 1	2 0.1U 0402 10V6K CPU HDMI TX0+ C 44
<8>	CPU_HDMI_TX0+	CM5 2	2 0.1U 0402 10V6K CPU HDMI TX0+ C 45
<8>	CPU_HDMI_TX1+	CM6 1	2 0.1U 0402 10V6K CPU HDMI TX1+ C 47
<8>	CPU_HDMI_TX1+	CM7 2	2 0.1U 0402 10V6K CPU HDMI TX1+ C 48
<8>	CPU_HDMI_TX2+	CM8 1	2 0.1U 0402 10V6K CPU HDMI TX2+ C 1
<8>	CPU_HDMI_TX2+	CM9 2	2 0.1U 0402 10V6K CPU HDMI TX2+ C 2
<8>	CPU_HDMI_CLK+	CM10 1	2 0.1U 0402 10V6K CPU HDMI CLK+ C 4
<8>	CPU_HDMI_CLK+	CM11 2	2 0.1U 0402 10V6K CPU HDMI CLK+ C 5

Pin	Component	Value	Function
<24>	GPU_HDMI_TX0+	CM12 1	2 0.1U 0402 10V6K GPU HDMI TX0+ C 8
<24>	GPU_HDMI_TX0+	CM13 2	2 0.1U 0402 10V6K GPU HDMI TX0+ C 9
<24>	GPU_HDMI_TX1+	CM14 1	2 0.1U 0402 10V6K GPU HDMI TX1+ C 11
<24>	GPU_HDMI_TX1+	CM15 2	2 0.1U 0402 10V6K GPU HDMI TX1+ C 12
<24>	GPU_HDMI_TX2+	CM16 1	2 0.1U 0402 10V6K GPU HDMI TX2+ C 13
<24>	GPU_HDMI_TX2+	CM17 2	2 0.1U 0402 10V6K GPU HDMI TX2+ C 14
<24>	GPU_HDMI_CLK+	CM18 1	2 0.1U 0402 10V6K GPU HDMI CLK+ C 16
<24>	GPU_HDMI_CLK+	CM19 2	2 0.1U 0402 10V6K GPU HDMI CLK+ C 17

Pin	Component	Value	Function
<14>	TMDS_B_HPD		IN1_HPD 46
<23,39>	DGPU_HDMI_HPD		IN2_HPD 10
<14>	DDPB_CLK		IN2_HPD 41
<14>	DDPB_DATA		IN1_SDA 42
<24>	GPU_HDMI_CLK		IN1_SDA 19
<24>	GPU_HDMI_DATA		IN2_SCL 20
<24>	GPU_HDMI_DATA		IN2_SDA 19
<19>	HDSW_DDC		SW_DDC 22
<19>	HDSW_MAIN		SW_MAIN 21



SW	Input	Output
SW_DDC	IN1---CPU IN2---GPU	L=IN1 H=IN2
SW_MAIN	IN1---CPU IN2---GPU	L=IN1 H=IN2

Channel A --> GPU

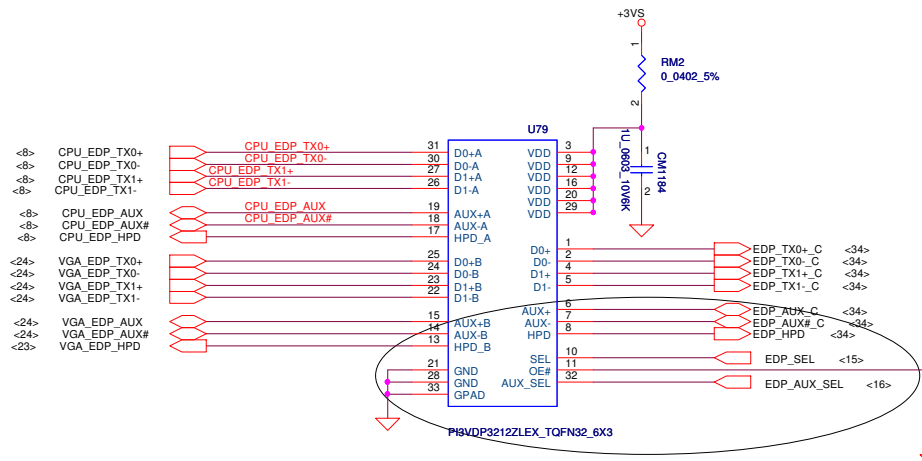
Channel B --> PCH

Pin	Component	Value	Function
<23>	VGA_CRT_R		SEL1 8 CRT_SWITCH_1
<23>	VGA_CRT_G		SEL1 9 CRT_SWITCH_1
<23>	VGA_CRT_B		SEL1 10 CRT_SWITCH_1
<23>	VGA_CRT_CLK		SEL1 11 CRT_SWITCH_1
<23>	VGA_CRT_DATA		SEL1 12 CRT_SWITCH_1
<23>	VGA_CRT_HSYNC		SEL1 13 CRT_SWITCH_1
<23>	VGA_CRT_VSYNC		SEL1 14 CRT_SWITCH_1
<14>	PCH_CRT_R		SEL2 26 CRT_SWITCH_1
<14>	PCH_CRT_G		SEL2 27 CRT_SWITCH_1
<14>	PCH_CRT_B		SEL2 28 CRT_SWITCH_1
<14>	PCH_CRT_DDC_CLK		SEL2 29 CRT_SWITCH_1
<14>	PCH_CRT_DDC_DAT		SEL2 30 CRT_SWITCH_1
<14>	PCH_CRT_HSYNC		SEL2 31 CRT_SWITCH_1
<14>	PCH_CRT_VSYNC		SEL2 32 CRT_SWITCH_1



For reserved CRT SW

Input SELx	Input/Output An	Function
L	nB1--GPU	An=nB1
H	nB2---PCH	An=nB2



OE#	SEL	AUX_SEL	FUNCTION
L	L	L	PORT A
L	L	H	PORT A-HS, PORT B-HPD/AUX
L	H	L	PORT B-HS, PORT A-HPD/AUX
L	H	H	PORT B
H	X	X	IC POWER DOWN

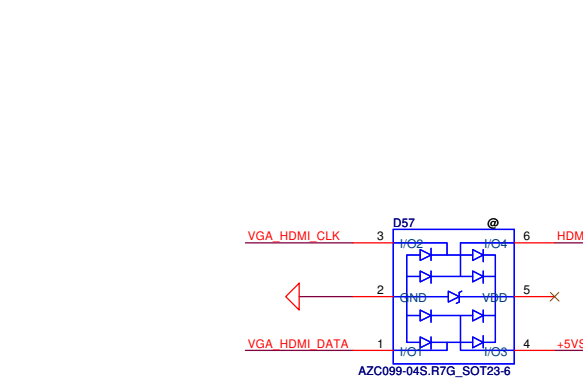
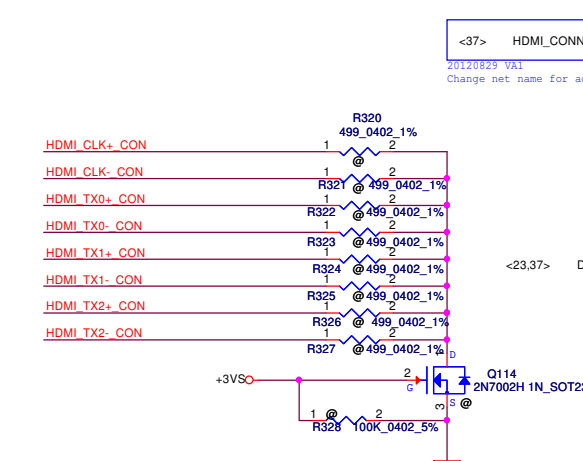
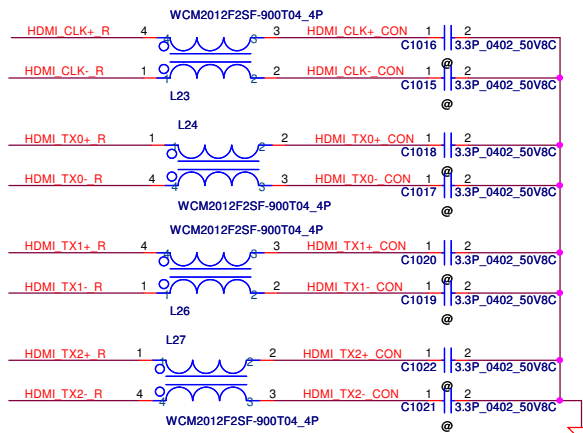
Security Classification: LC Future Center Secret Data

Issued Date: 2012/07/01

Deciphered Date: 2014/07/01

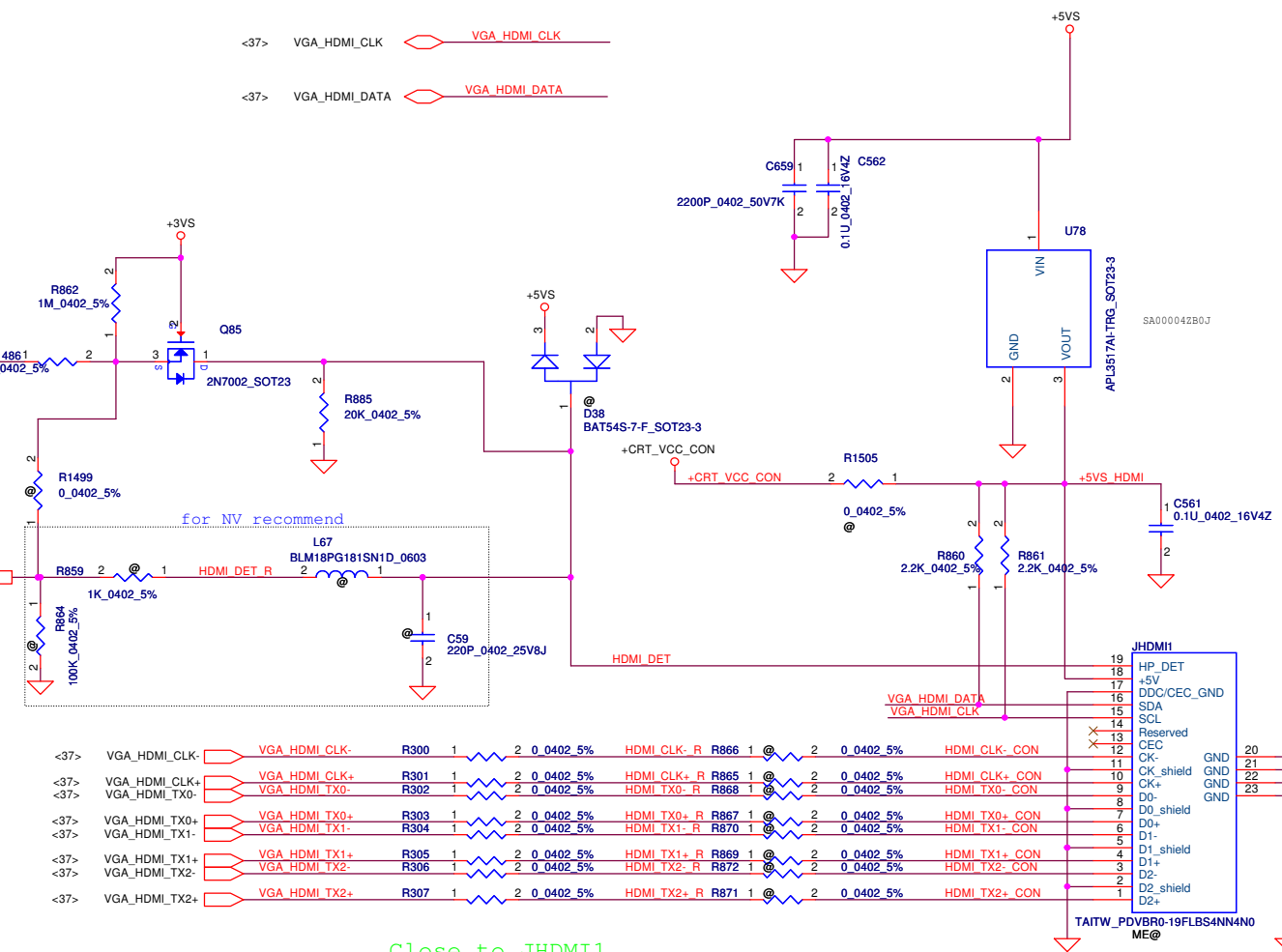
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Title		
LVDS/ CMOS/ USB-ReDriver		
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Custom		
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Rev	1.0	



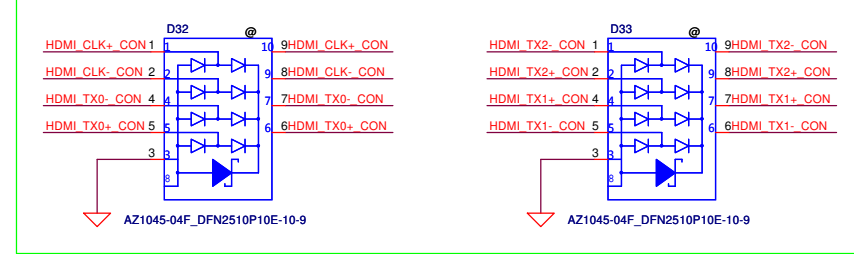
<37> VGA_HDMI_CLK VGA_HDMI_CLK

<37> VGA_HDMI_DATA VGA_HDMI_DATA



<37>	VGA_HDMI_CLK-	VGA_HDMI_CLK-	R300	1	2	0.0402_5%	HDMI_CLK- R	R866	1	@	2	0.0402_5%	HDMI_CLK- CON
<37>	VGA_HDMI_CLK+	VGA_HDMI_CLK+	R301	1	2	0.0402_5%	HDMI_CLK+ R	R865	1	@	2	0.0402_5%	HDMI_CLK+ CON
<37>	VGA_HDMI_TX0-	VGA_HDMI_TX0-	R302	1	2	0.0402_5%	HDMI_TX0- R	R868	1	@	2	0.0402_5%	HDMI_TX0- CON
<37>	VGA_HDMI_TX0+	VGA_HDMI_TX0+	R303	1	2	0.0402_5%	HDMI_TX0+ R	R867	1	@	2	0.0402_5%	HDMI_TX0+ CON
<37>	VGA_HDMI_TX1-	VGA_HDMI_TX1-	R304	1	2	0.0402_5%	HDMI_TX1- R	R870	1	@	2	0.0402_5%	HDMI_TX1- CON
<37>	VGA_HDMI_TX1+	VGA_HDMI_TX1+	R305	1	2	0.0402_5%	HDMI_TX1+ R	R869	1	@	2	0.0402_5%	HDMI_TX1+ CON
<37>	VGA_HDMI_TX2-	VGA_HDMI_TX2-	R306	1	2	0.0402_5%	HDMI_TX2- R	R872	1	@	2	0.0402_5%	HDMI_TX2- CON
<37>	VGA_HDMI_TX2+	VGA_HDMI_TX2+	R307	1	2	0.0402_5%	HDMI_TX2+ R	R871	1	@	2	0.0402_5%	HDMI_TX2+ CON

Close to JHDMI1

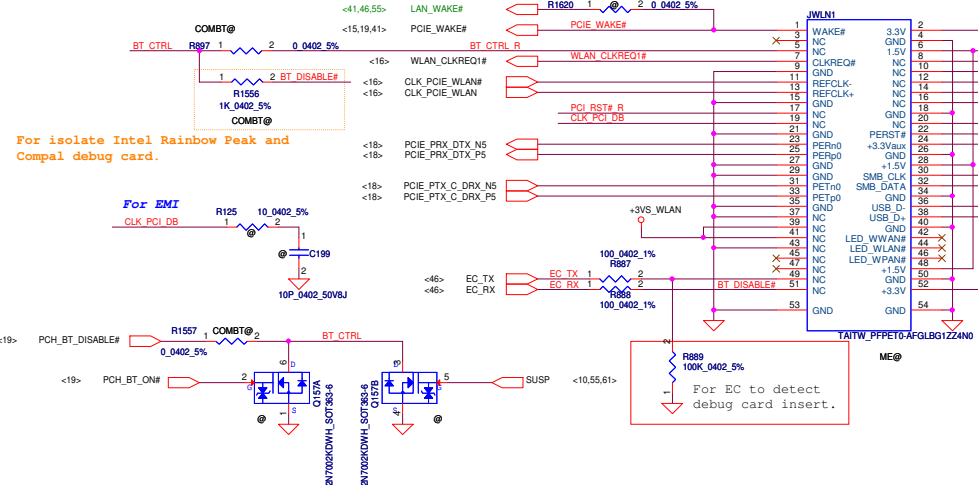
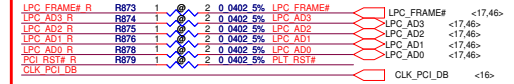


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			69	

Mini-Express Card(WLAN/WiMAX)

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



WLAN&BT Combo module circuits

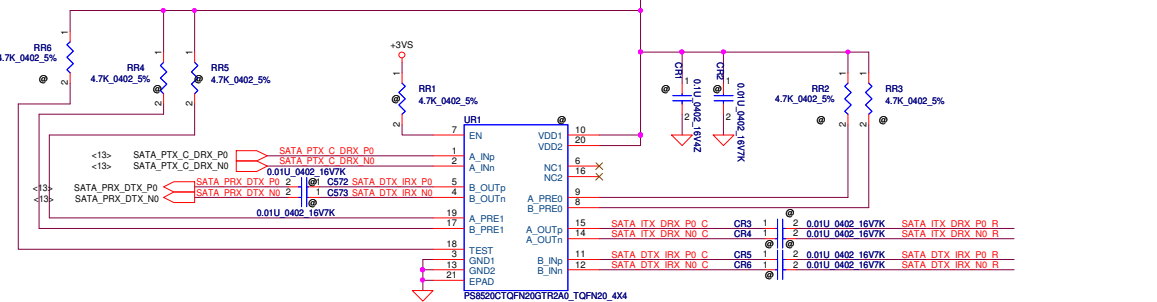
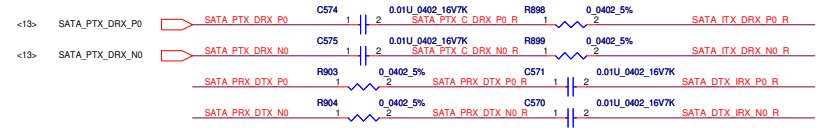
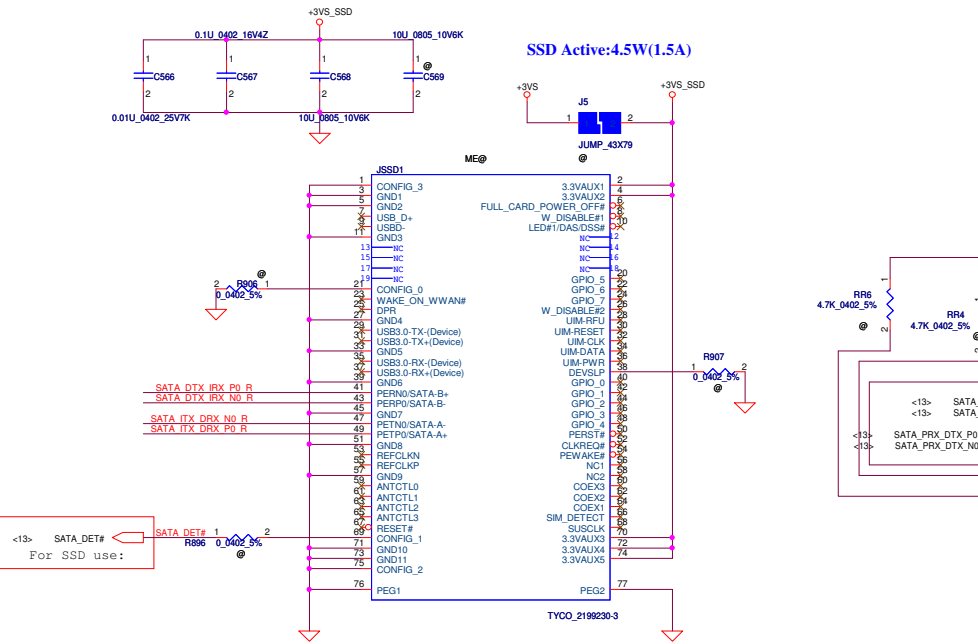
	BT on module Enable	BT on module Disable
* BT_CRTL (GPIO22)	H	L
PCH_BT_ON#	L	H



softstart (RC) will check on EVT PCB

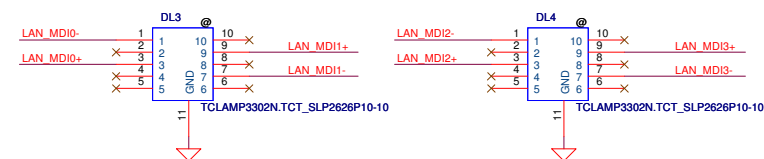
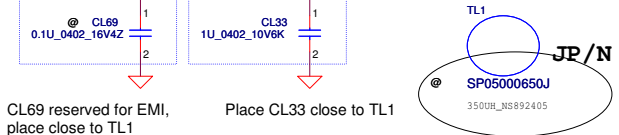
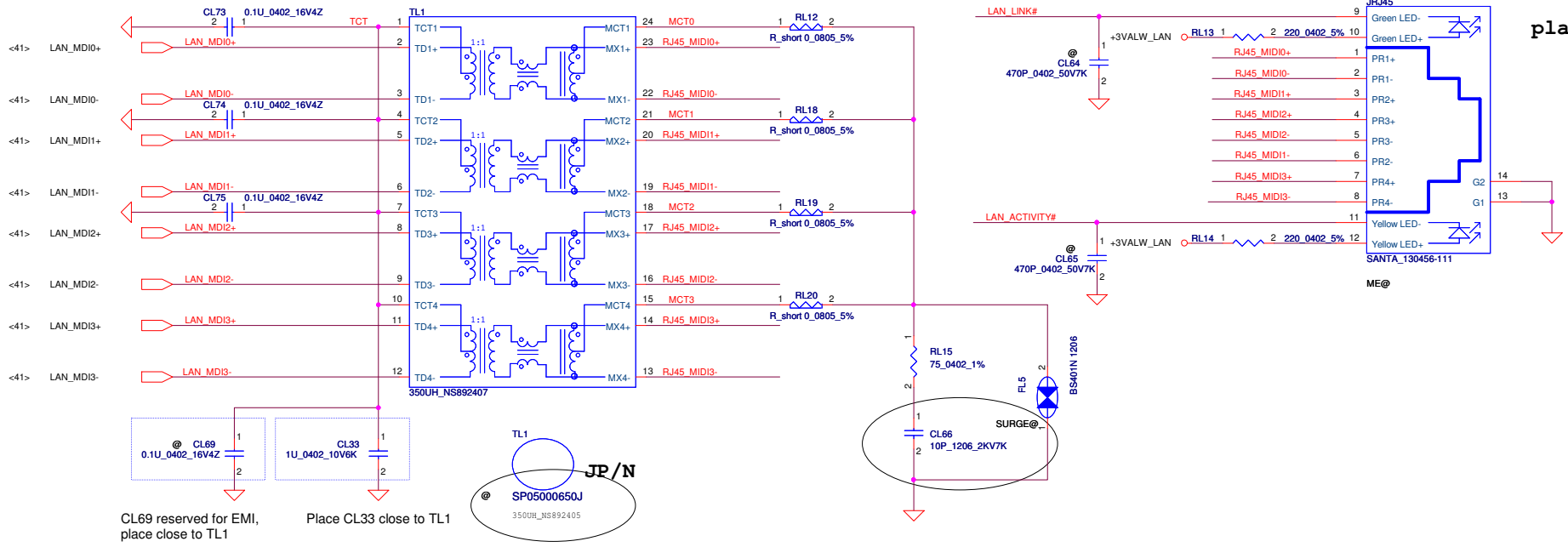
9/18 Increase for Intel AOAC function

NGFF(SSD)

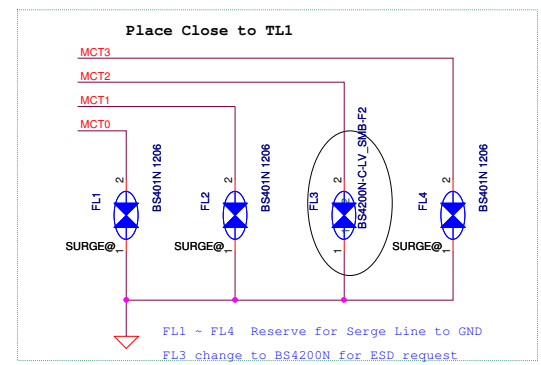
SSD Active:4.5W(1.5A)



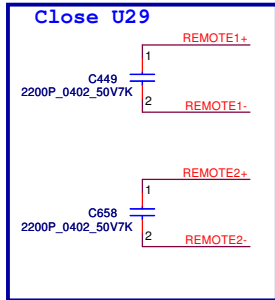
<41> LAN_LINK#  LAN_LINK#
 <41> LAN_ACTIVITY#  LAN_ACTIVITY#



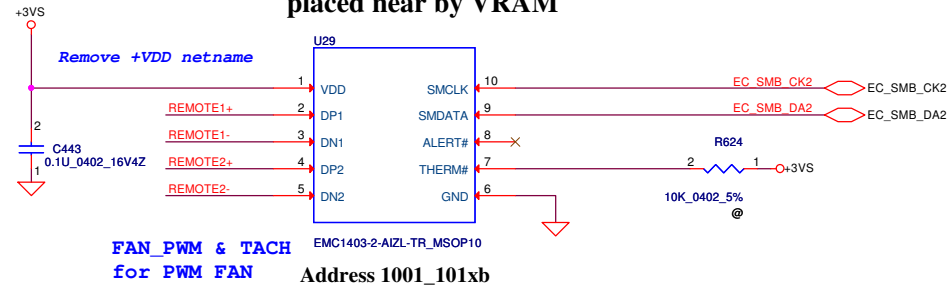
DL3, DL4 Reserve for Surge



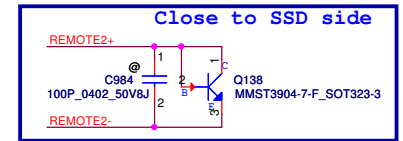
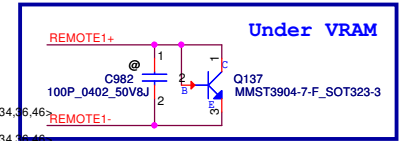
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**SMSC thermal sensor
placed near by VRAM**

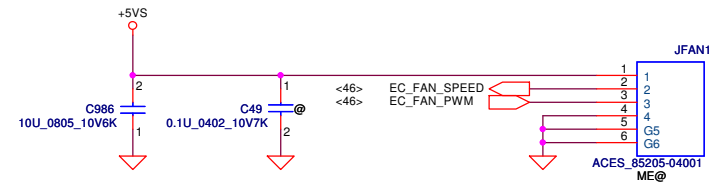


internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp



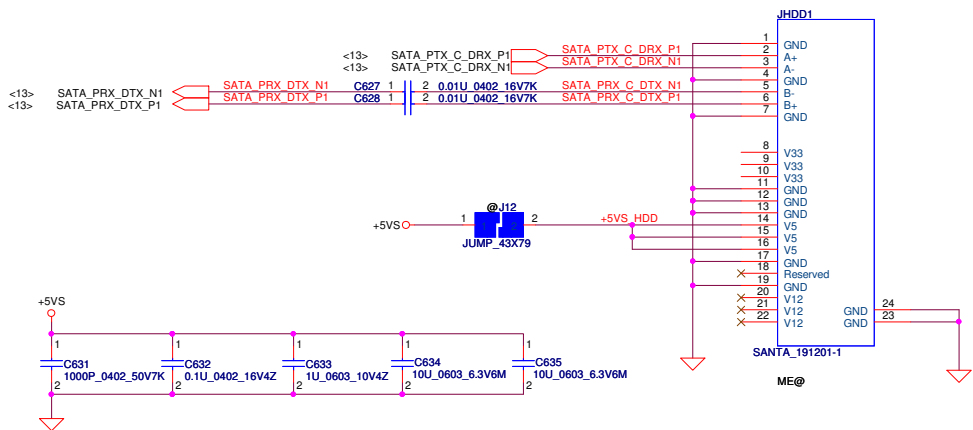
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

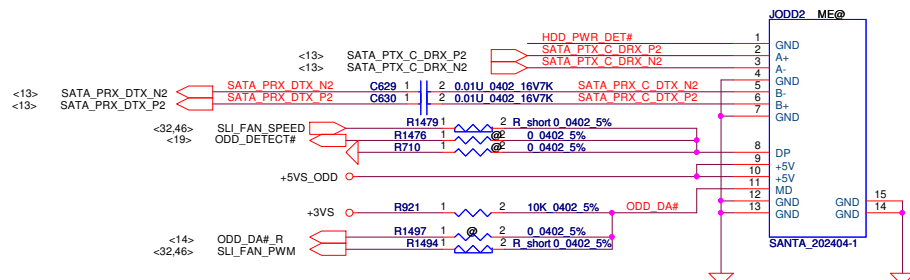


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Size	Document Number	Date		Rev
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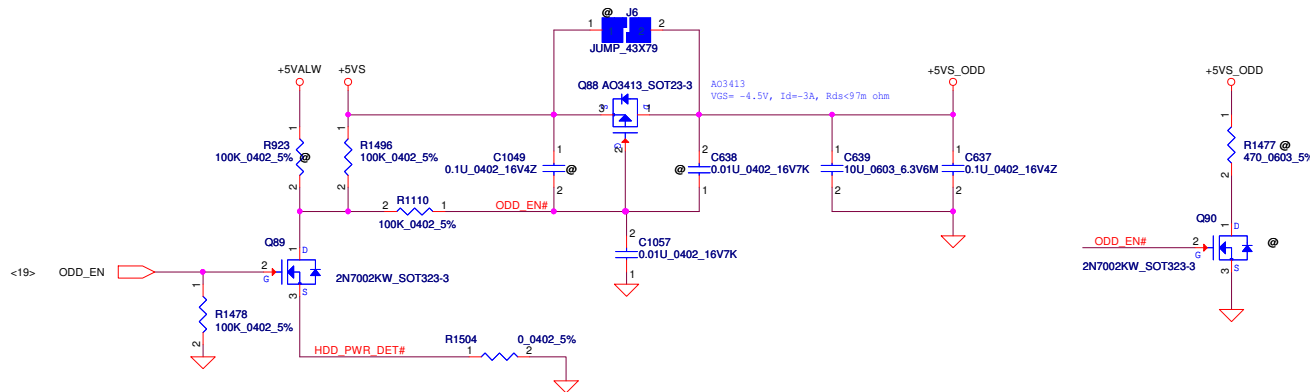
SATA HDD Conn.




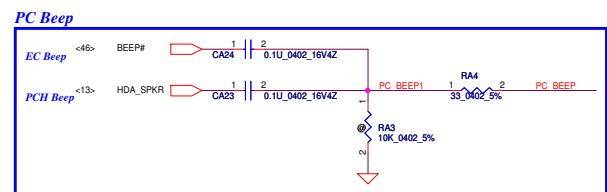
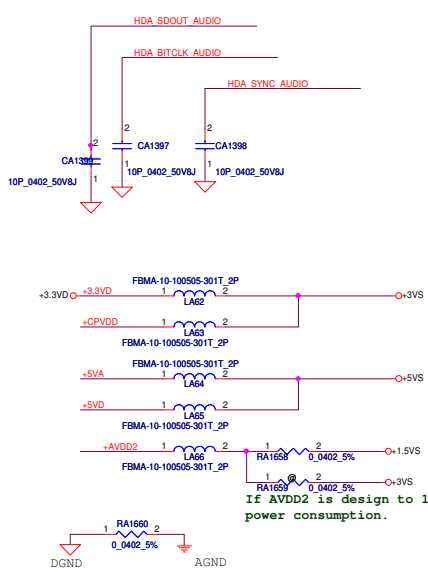
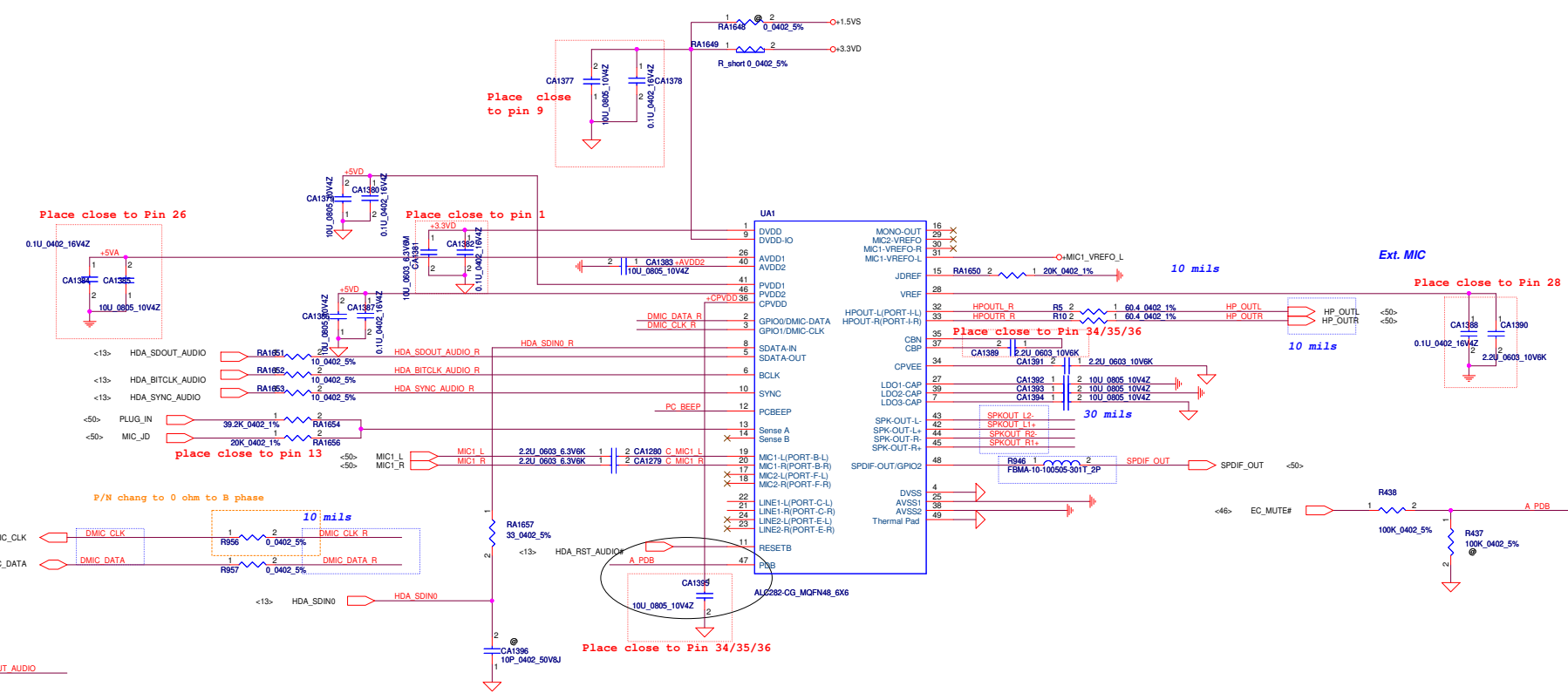
SATA ODD Conn.



ODD Power Control

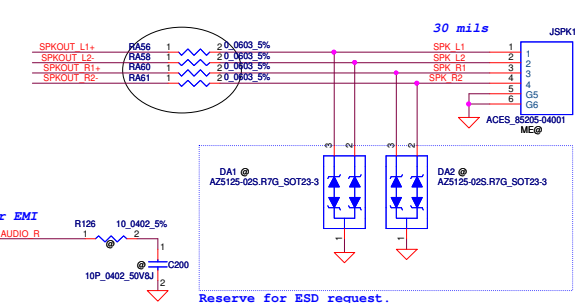
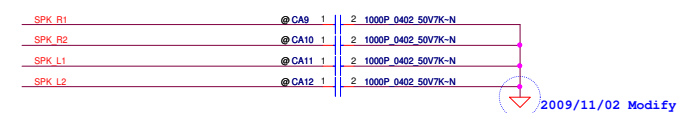


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				Rev: 1.0



ALC282 Configuration - example
 4 external jacks: Line-in / Mic-in / Hp-out / SPDIF-OUT
 Internal speaker
 Internal Stereo DMIC

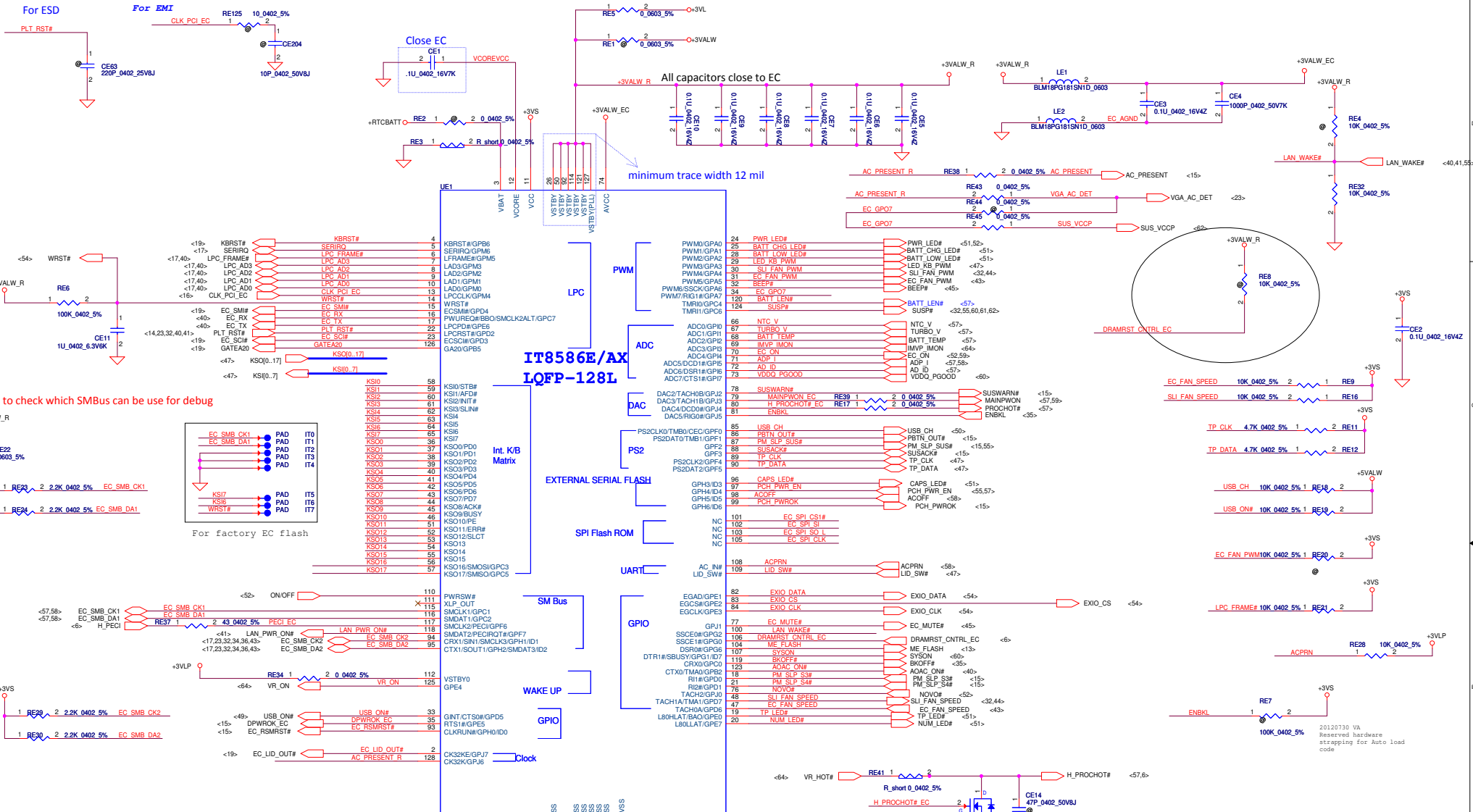
Pin Assignment	Location	Function
SPEAKER-OUT (pin-43/44/45/46_Port D)	Internal	Internal Speaker
Cap-Saving HP-OUT (pin-32/33_Port I)	External	Headphone out
LINE1 (pin-21/22_Port C)	External	Line in
MIC1 (pin-19/20_Port B)	External	Mic in
MONO-OUT (pin-16)		
MIC2 (pin-17/18_Port F)		
DMIC1/2 (pin-2/3)		



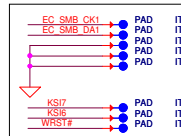
Tied at one point only under the codec or near the codec

If AVDD2 is design to 1.5V, you will get better power consumption.

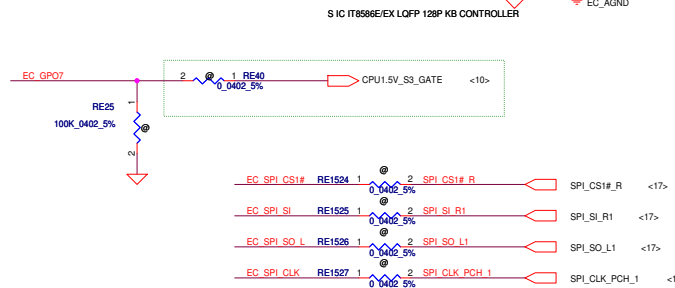
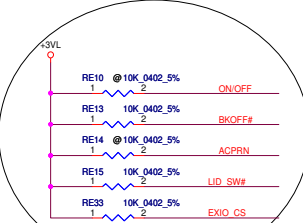
Security Classification		LC Future Center Secret Data		Title	
NC	Issued Date	2012/05/02	Deciphered Date	2012/05/02	Audio Codec
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Need to check which SMBus can be use for debug

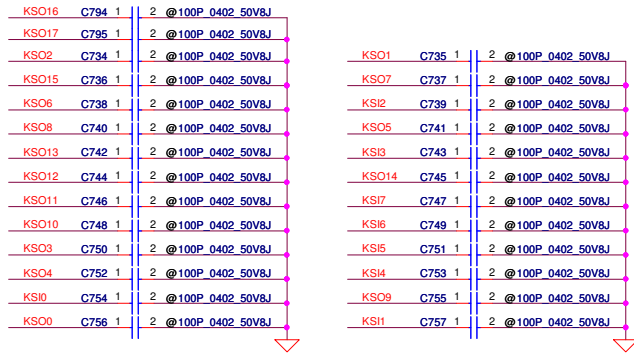
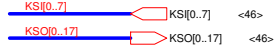


For factory EC flash

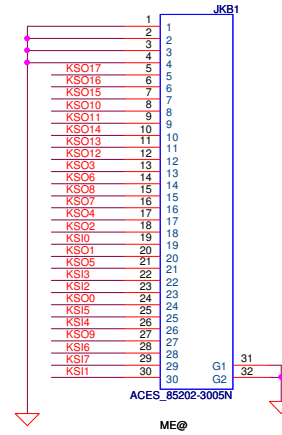


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				Y501	NW-A092
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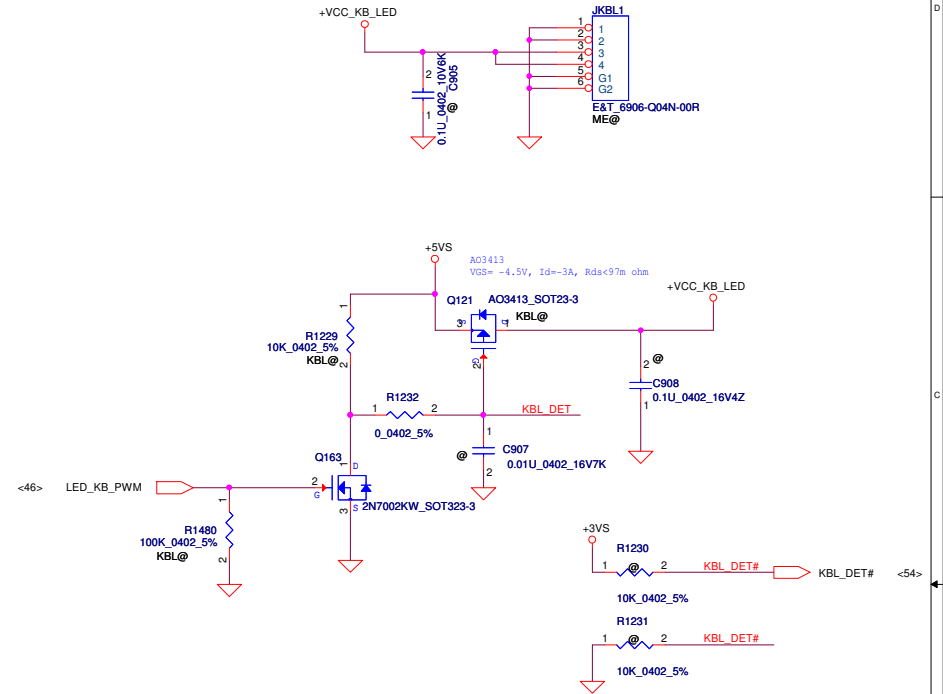
15" INT_KBD Conn.



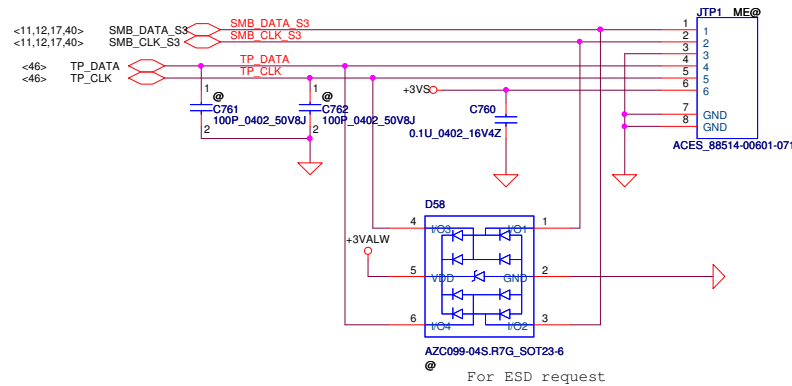
CONN PIN define need double check



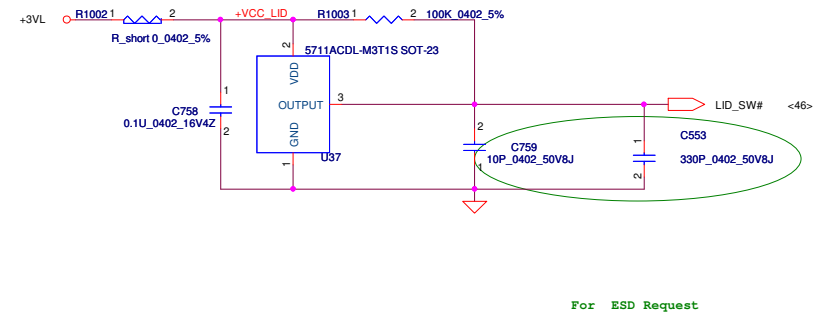
KB Lighting CONN.4pin



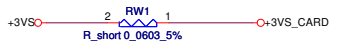
To TP/B Conn.



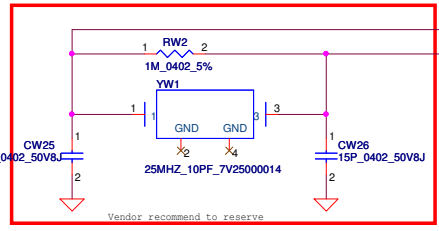
Lid Switch



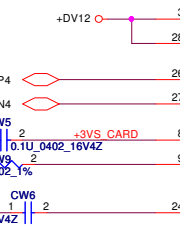
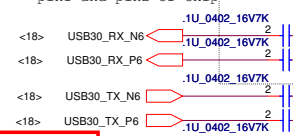
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	
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				Rev 1.0



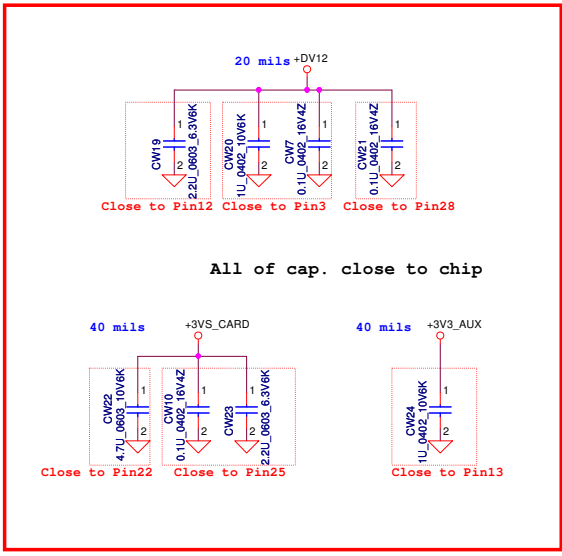
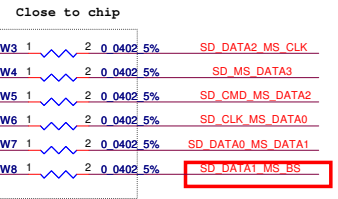
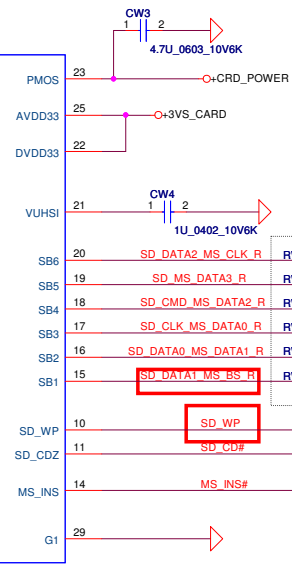
1.2V Power Source Selection: (Optional)



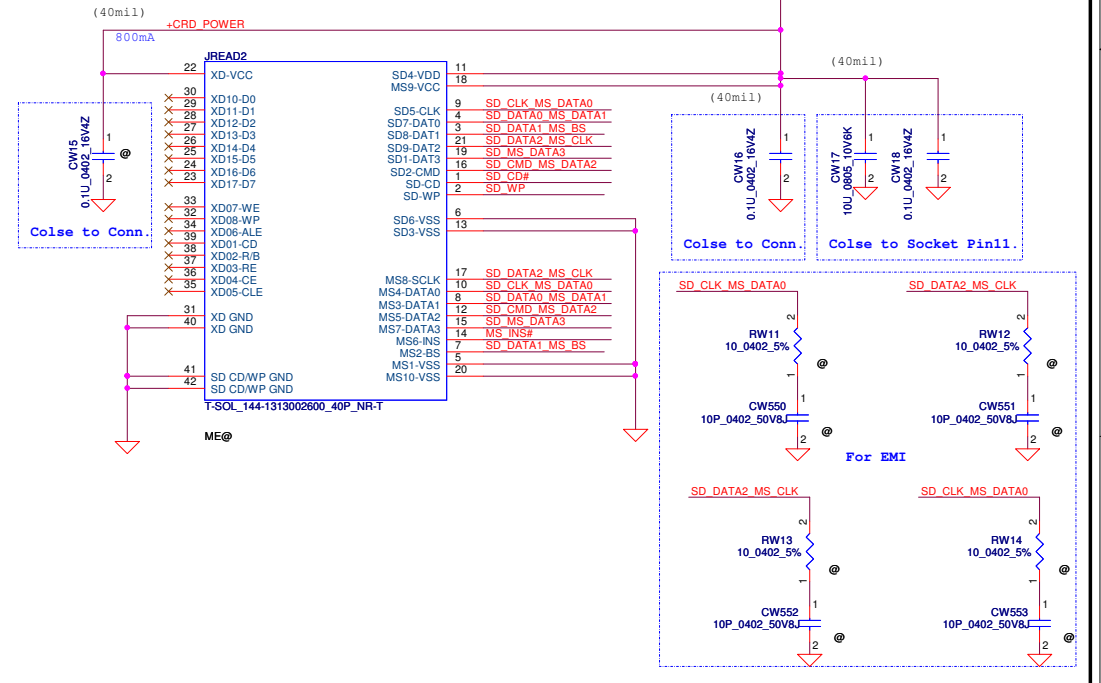
AC Coupling close to pin1 and pin2 of Chip



GL3213-OHY03_QFN28_5X5



< 4 in 1 Card Reader Connector >

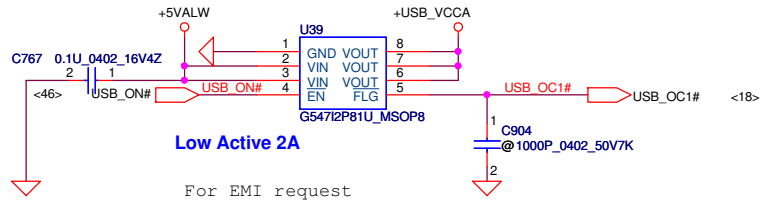


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Title	
Card reader GL3213	
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LEFT SIDE USB3.0 PORT X1

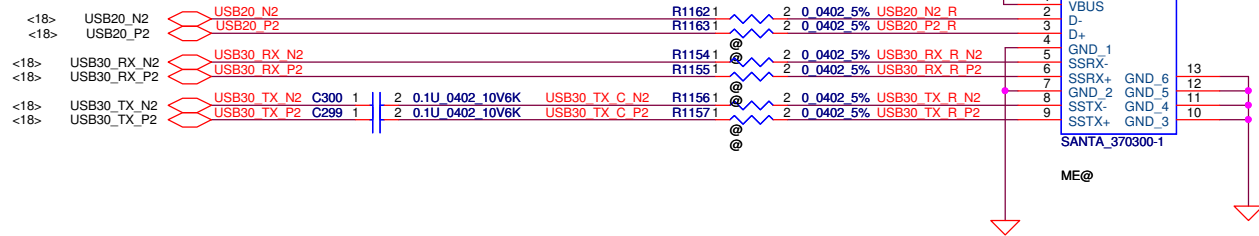
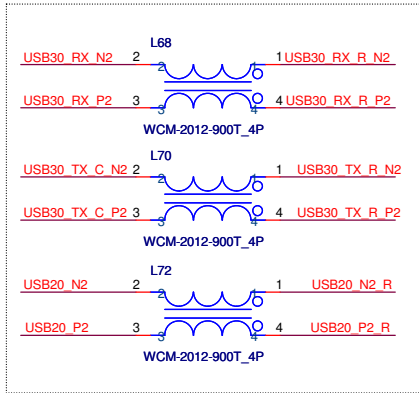


Low Active 2A

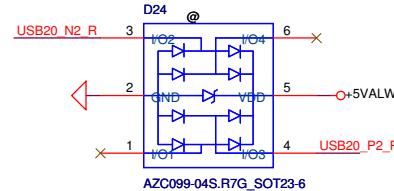
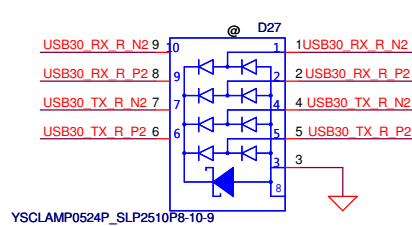
For EMI request

USB2.0 choke --> SM070001S0J

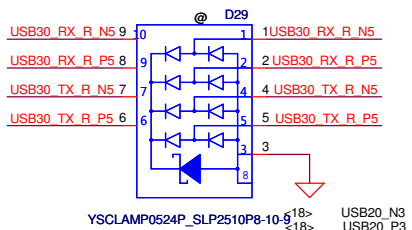
USB3.0 Choke --> SM070001S0J



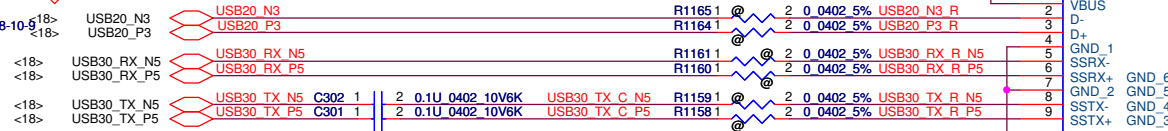
For ESD request



For ESD request



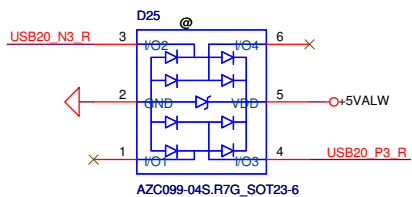
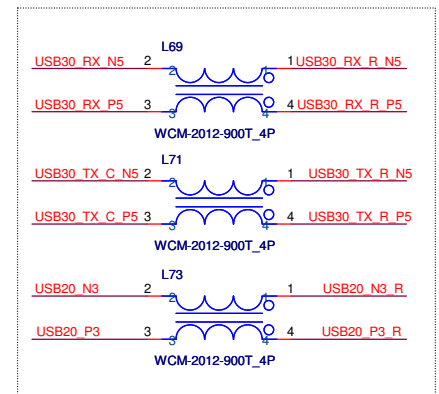
YSCLAMP0524P_SLP2510P8-10-9



For EMI request

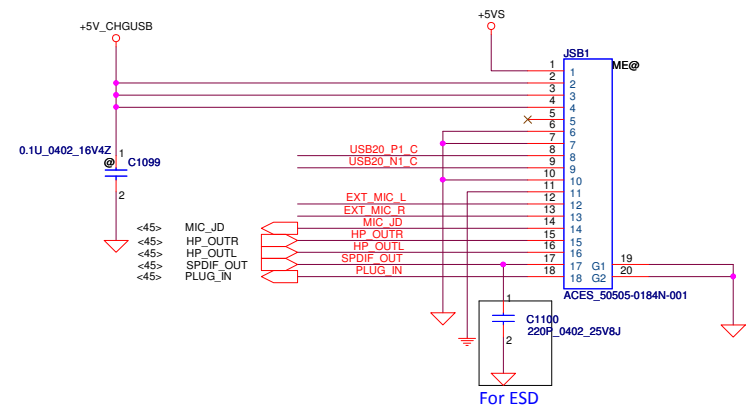
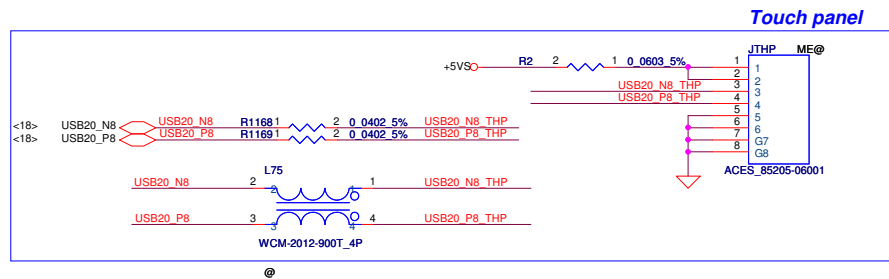
USB2.0 choke --> SM070000I00

USB3.0 Choke --> SM070001U00

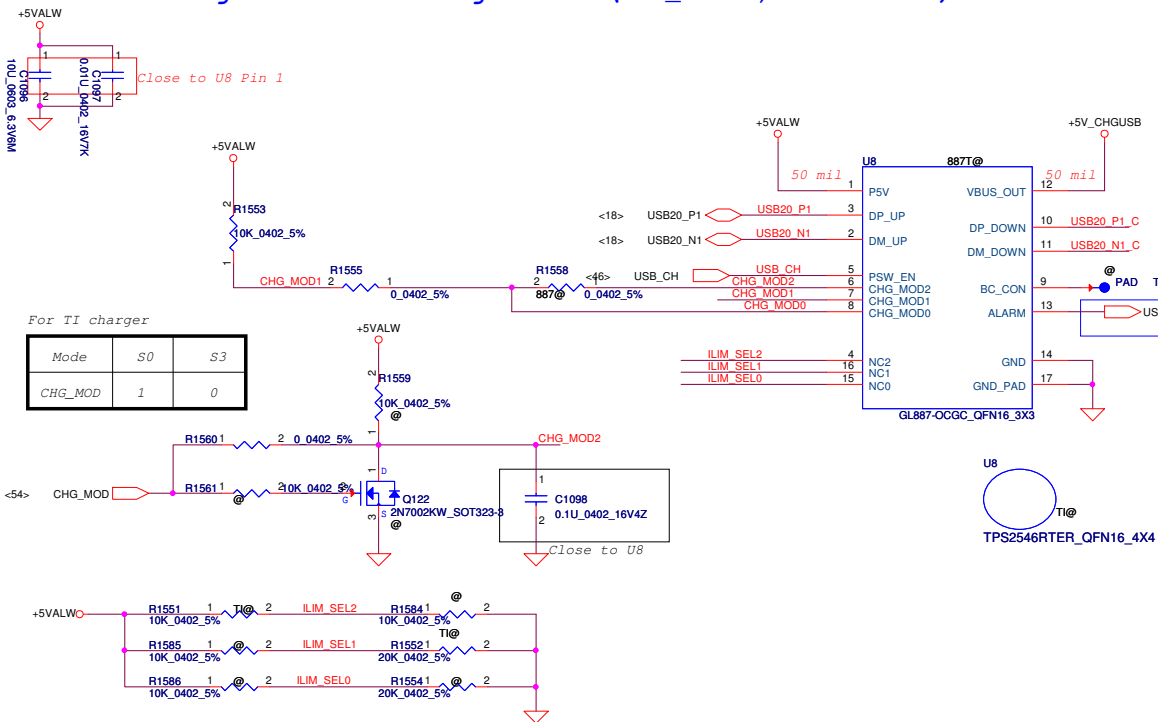


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Title	USB 3.0 PORT (LEFT)	
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Sleep & Charge Right side USB Charger Port (USB Port5, near JMC1)



For TI charger

Mode	S0	S3
CHG_MOD	1	0

Genesys GL887

CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
0	0	0	Charge Disable
0	1	0	CDP mode
0	1	1	DCP mode
1	0	0	Apple 1A mode
1	0	1	Apple 2A mode
1	1	0	Auto mode (DCP and Apple 1A)
1	1	1	Auto mode (DCP and Apple 2A)

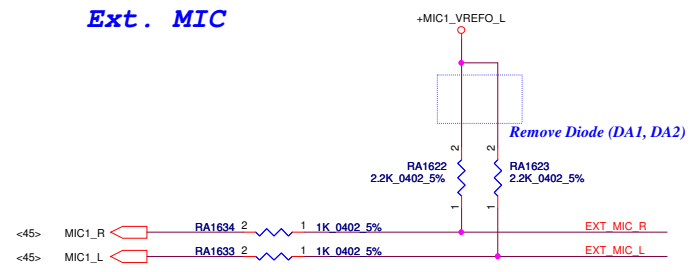
Genesys GL887T

CHG_MOD2	CHG_MOD1	CHG_MOD0	Charge Mode
0	0	0	Power down mode
0	0	1	Auto 2A mode without wake up function
X	1	0	BC1.2 SDP mode
0	1	1	Auto 2A mode with wake up function
1	0	0	BC1.2 DCP mode
1	0	1	Apple 2A mode
1	1	1	BC1.2 CDP mode with Smart CDP

TI TPS2543

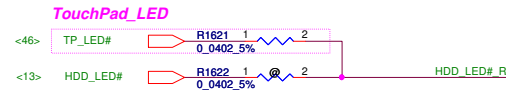
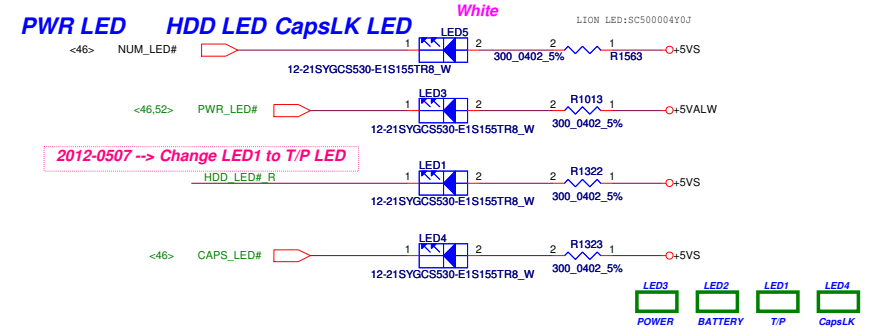
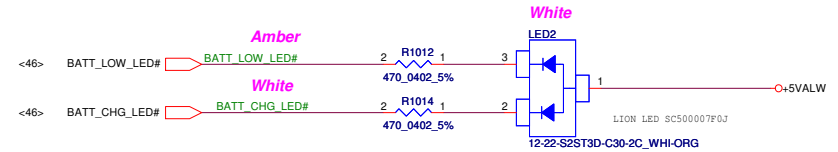
CHG_MOD2	CHG_MOD1	CHG_MOD0	ILIM_SEL2	MODE
0	0	0	X	DCH_OUT held low /Data lines disconnected
1	1	1	1	CDP Data connected and Load detect active
1	1	1	0	SDP2 Data connected
1	1	0	X	SDP1 Data connected
0	1	0	X	SDP1 Data connected
1	0	0	X	DCP_Short Stay in DCP BC1.2 Charging mode
1	0	1	X	DCP_Divider Stay in DCP Divider1 Charging mode
0	1	1	X	DCP_Auto Data disconnected and Load detect active
0	0	1	X	DCP_Auto Data disconnected and Load detect active

Ext. MIC



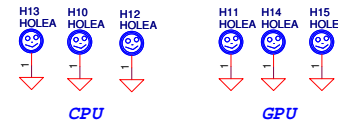
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	
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Date:	Wednesday, March 27, 2013	Sheet	50	Rev 1.0

BATT CHARGE/LOW LED

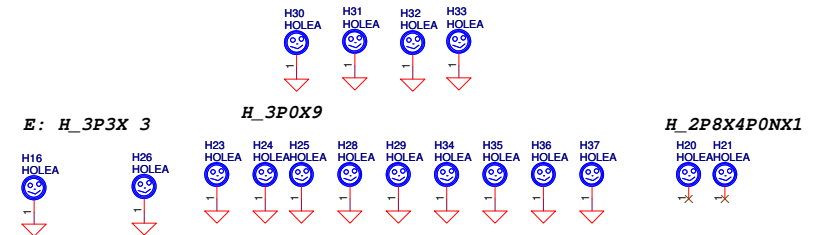


Screw Hole

CPU and GPU: H_3P8X 6
 C: H_3P8X 3 B: H_3P8X 3
 MIN PCIE: H_3P3 X 1
 E: H_3P3X 1



ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1
 A: H_2P8X 8

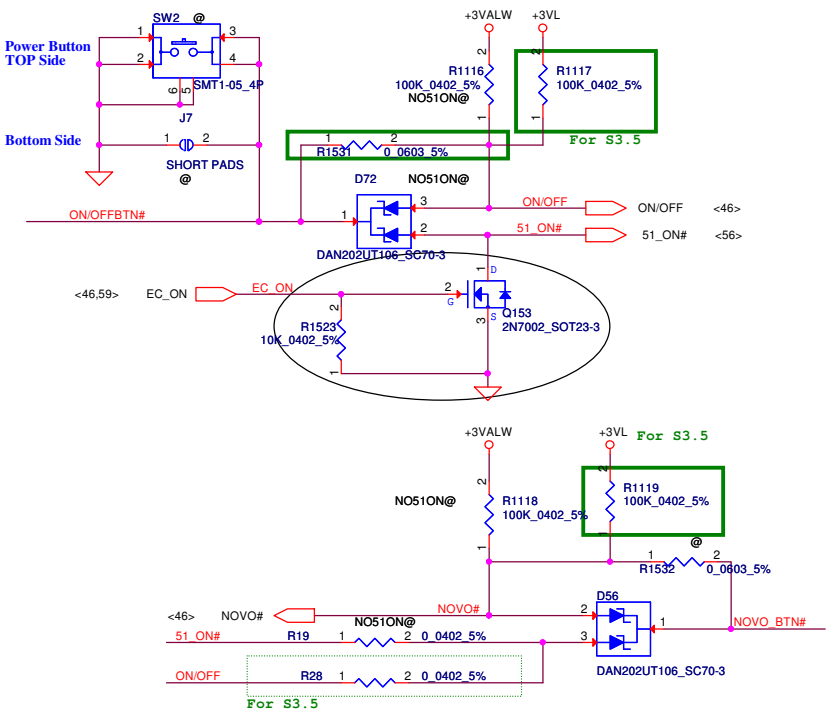


PCB Fedical Mark PAD

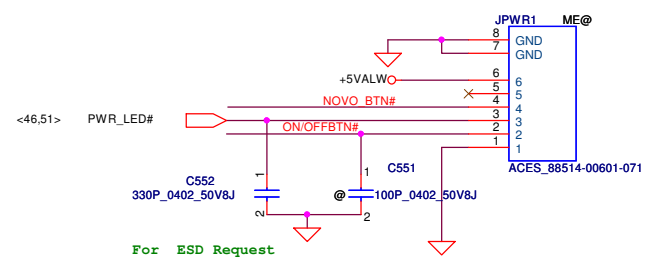


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ON/OFF switch



Power Button/B link to Function/B Conn. 10pin



**EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00**

NO51ON@ default reserved

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Title		
ONOFF SW/ PWR-B CONN/ ISPD		
Size	Document Number	Rev
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5

4

3

2

1

D

D

C

C

B

B

A

A

Security Classification	Compal Secret Data		Title
Issued Date	2011/07/21	Deciphered Date	2012/12/31
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Size	C	Rev	1.0
Date: Wednesday, March 27, 2013		Sheet	53 of 69

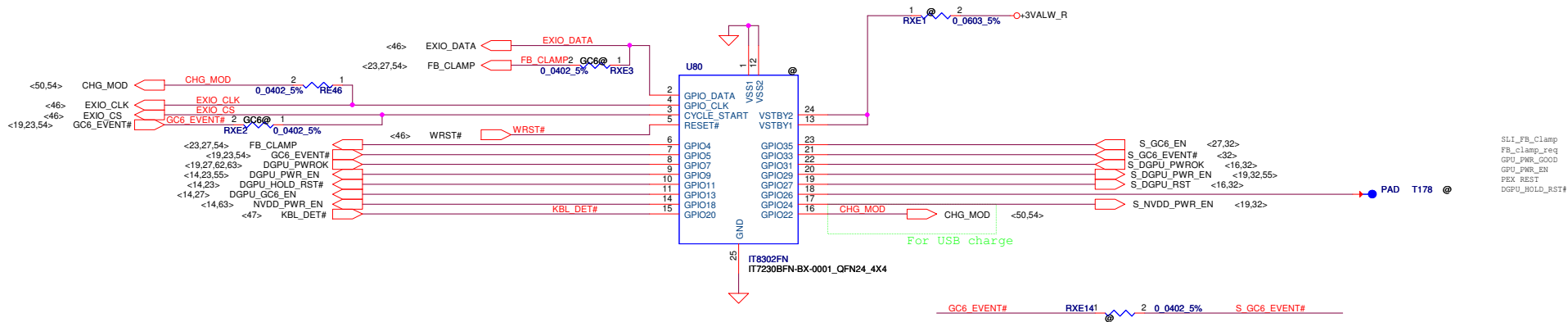
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4

3

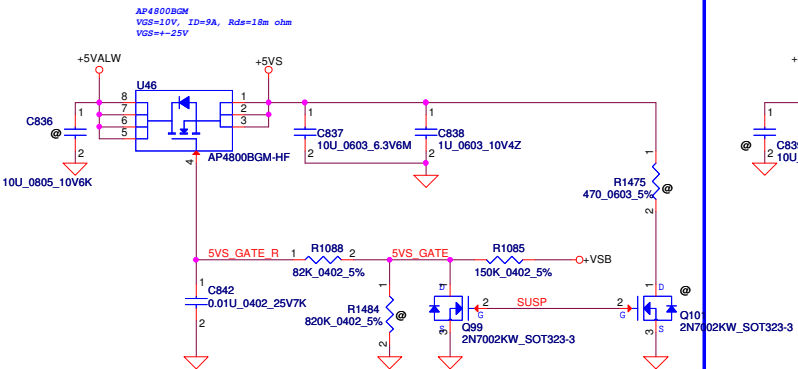
2

1

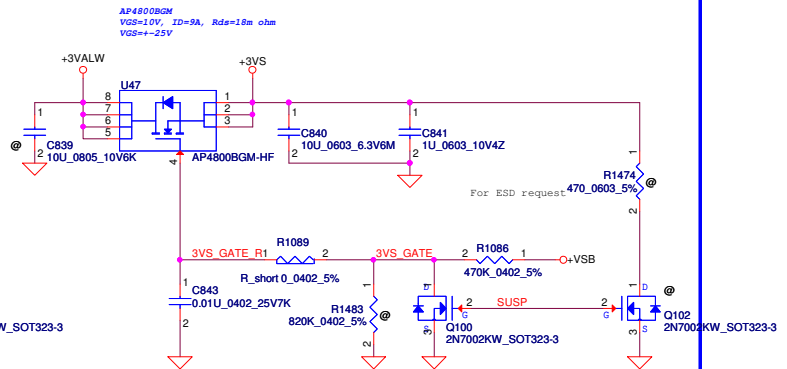


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				Y501 NM-A032
				Rev 1.0
				Date: Wednesday, March 27, 2013 Sheet 54 of 69

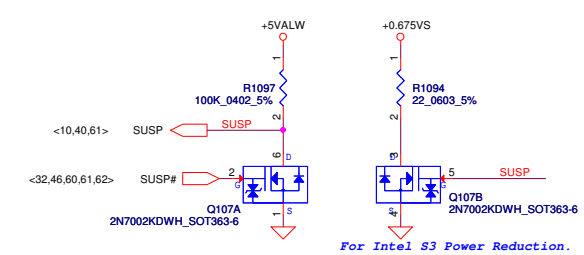
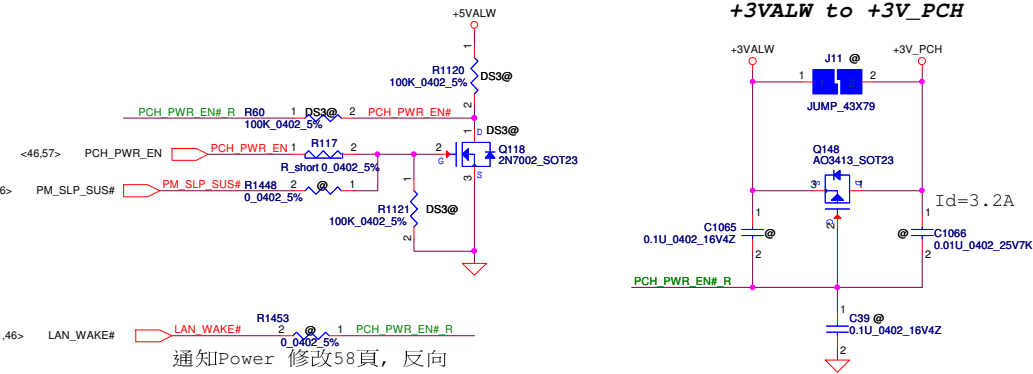
+5VALW to +5VS



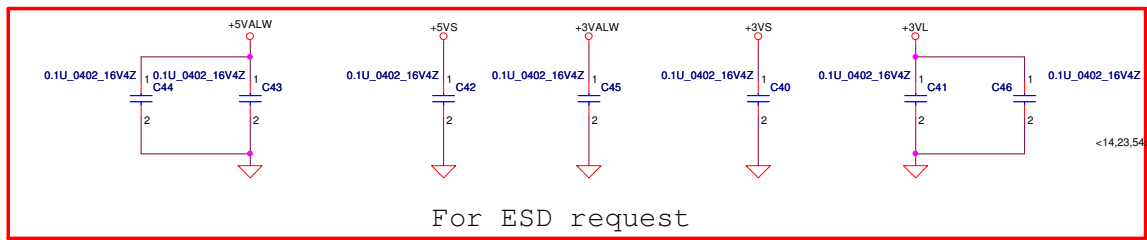
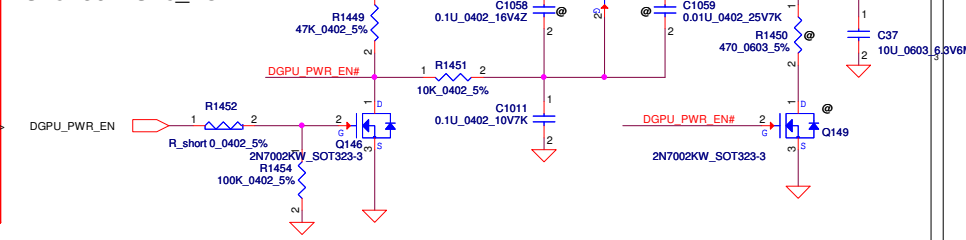
+3VALW to +3VS



+3VALW to +3V_PCH

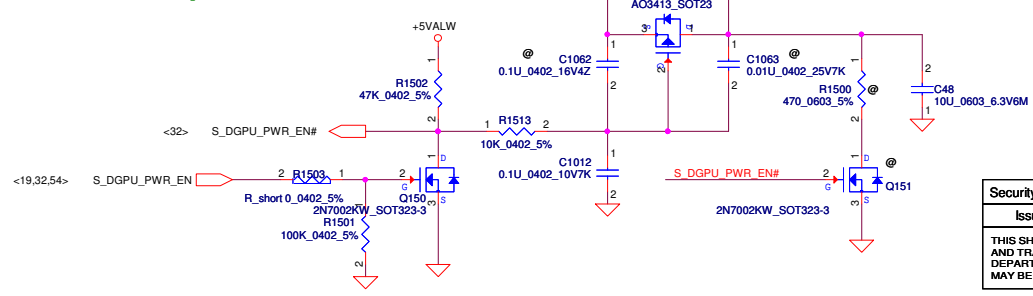



+3VS to +3VS_VGA



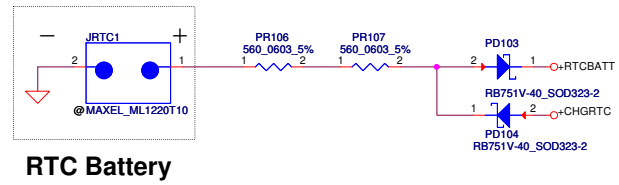
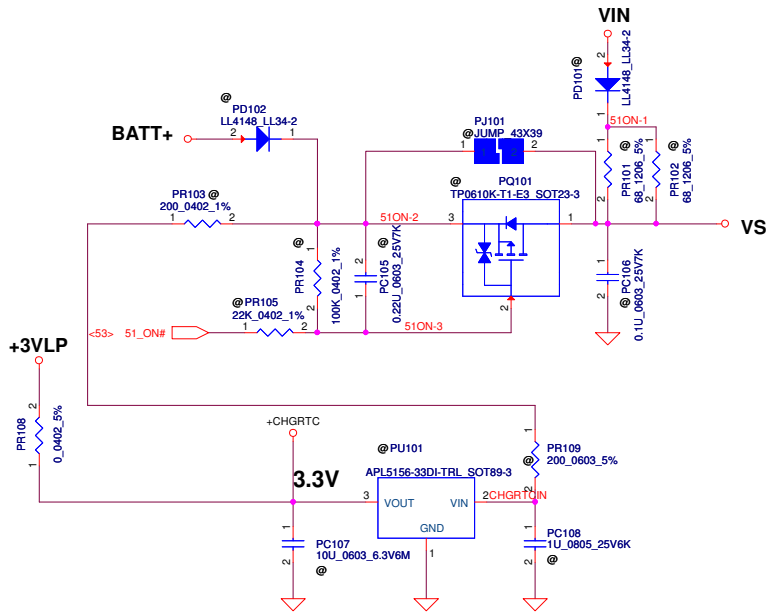
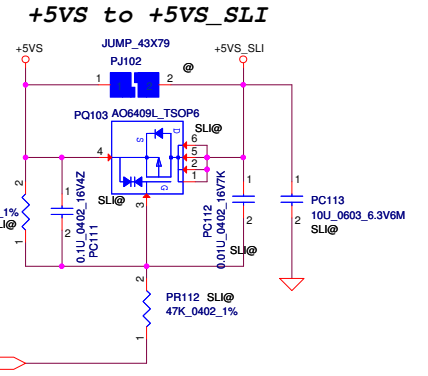
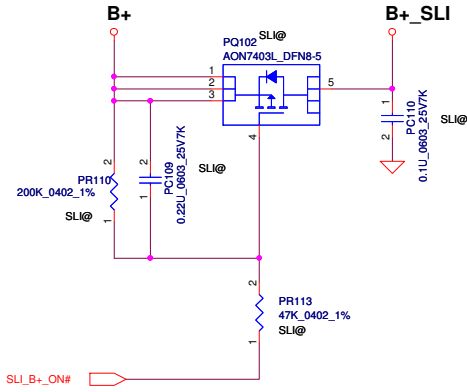
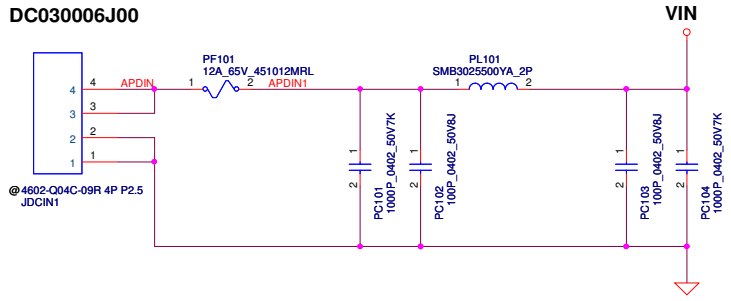
+3VS to +3VS_SLI

2012-0419 --> modify +3VS_SLI BOM structure to "SLI@"



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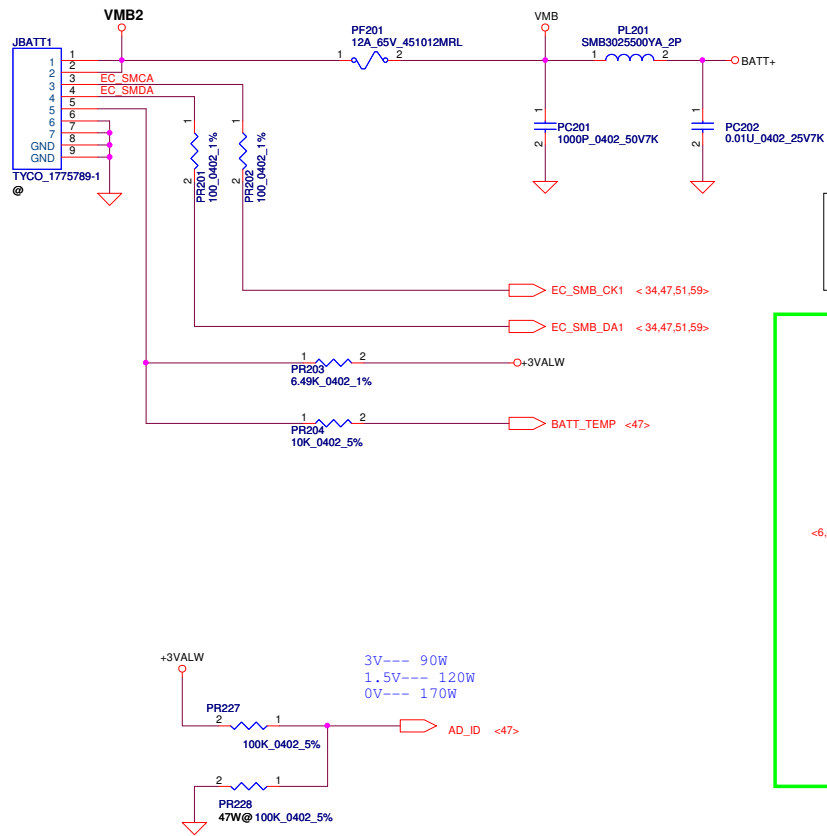
DC030006J00



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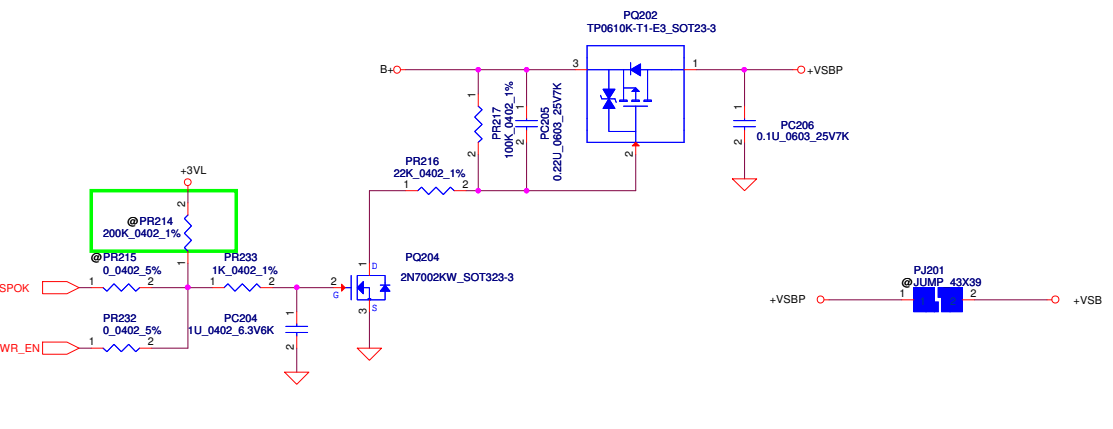
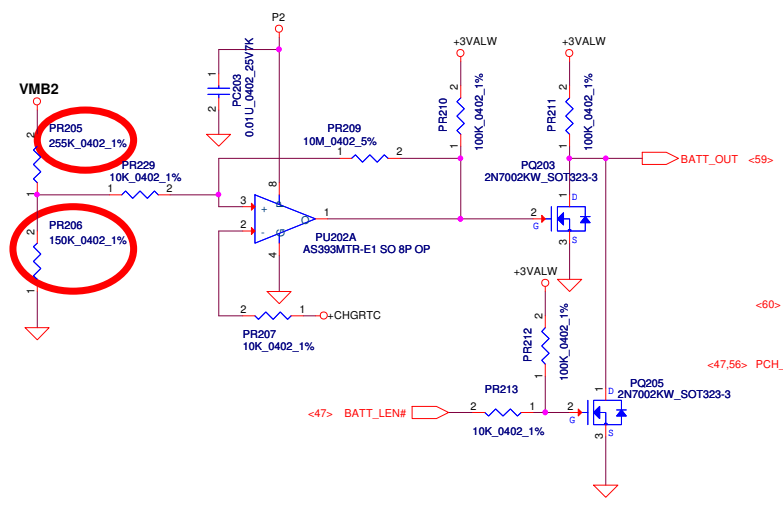
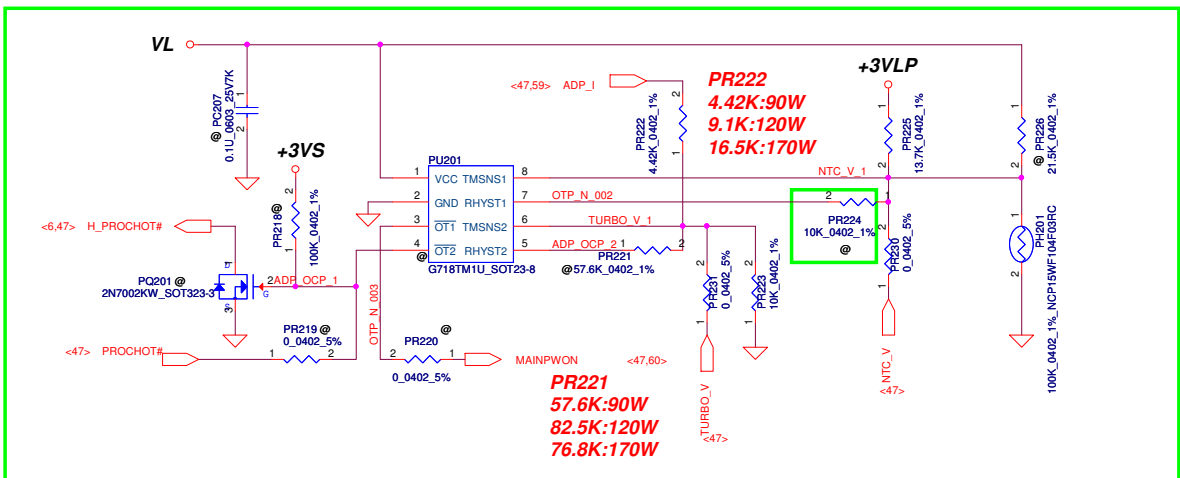
Title	Vin Detector
Size	Custom
Document Number	Y510 NM-A032
Date	Wednesday, March 27, 2013
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Rev	1.0





PH1 under CPU bottom side :
 CPU thermal protection at 92+-3 degree C
 Recovery at 56 +-3 degree C

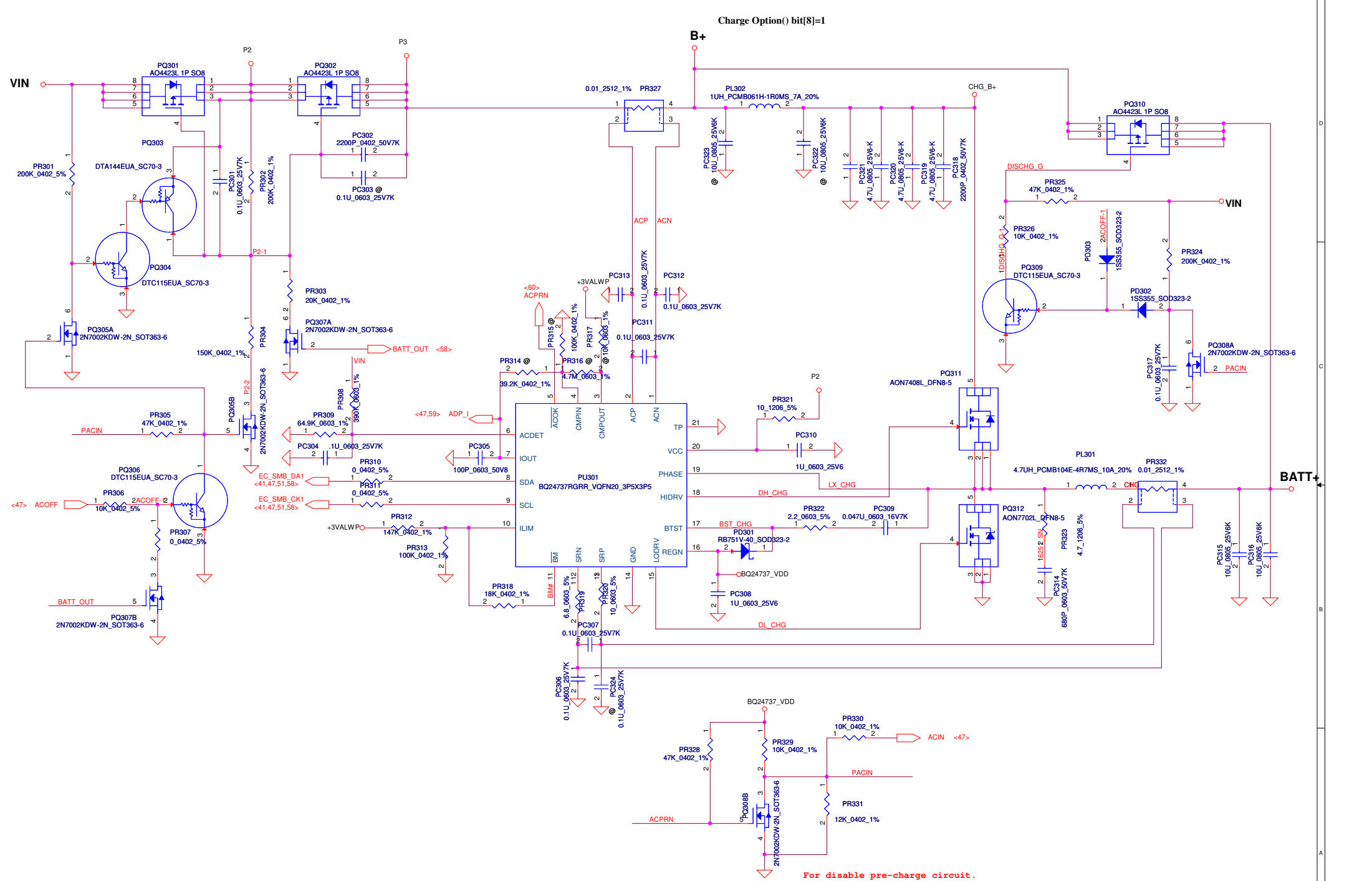
For KB930 --> Keep PU1 circuit
 (Vth = 0.825V)
 For KB912 (Red square) --> Remove PU201 circuit, but keep PR206
 PH201, PR205, PR211, PQ201, PR208, PR212



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Title	BATTERY CONN/OTP	
Size	Document Number	Rev
Custom	Y510 NM-A032	1.0
Date:	Wednesday, March 27, 2013	Sheet 57 of 69

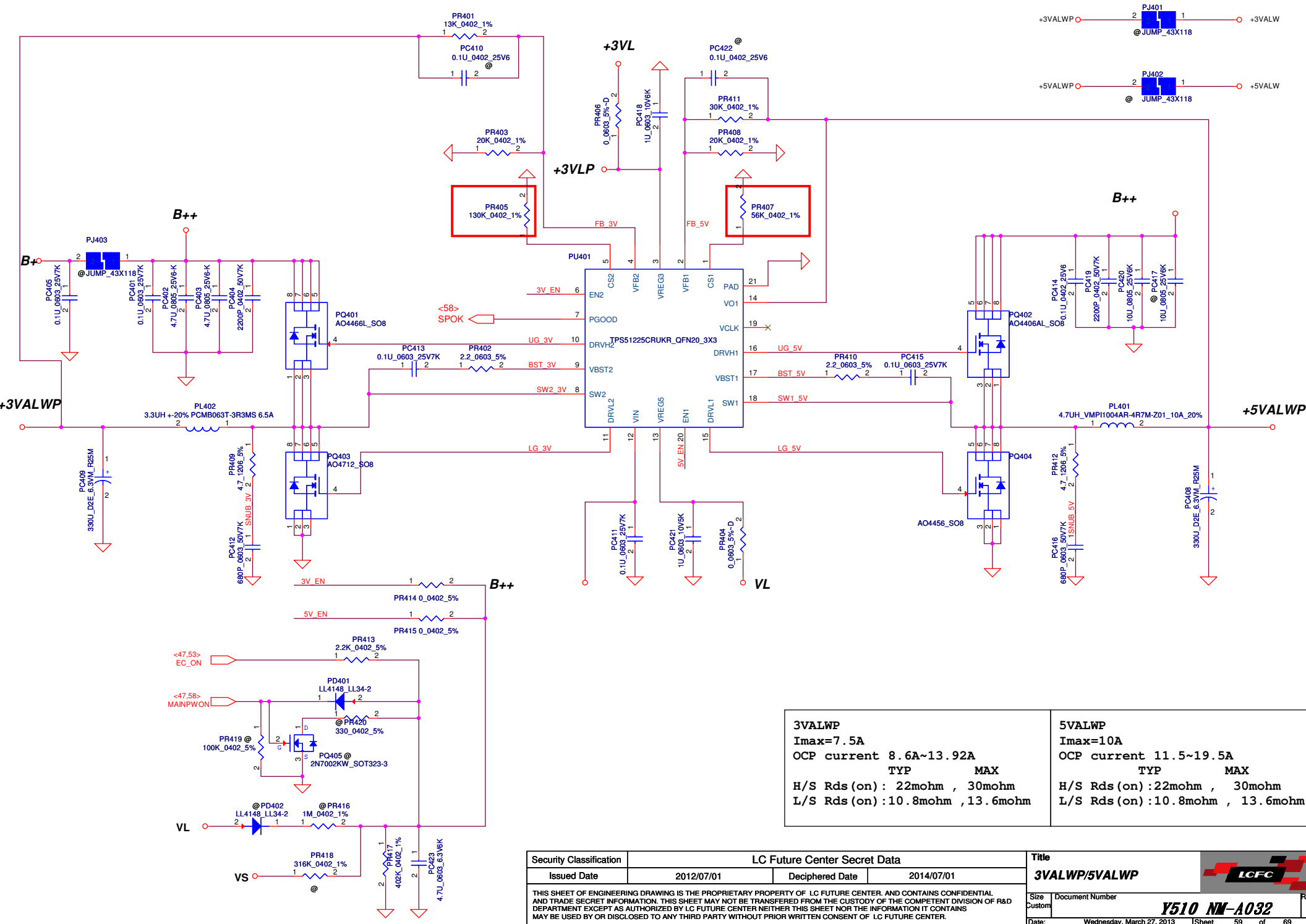




For disable pre-charge circuit.

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Title		
CHARGER		
Size	Document Number	Y510 NM-A032
Custom		
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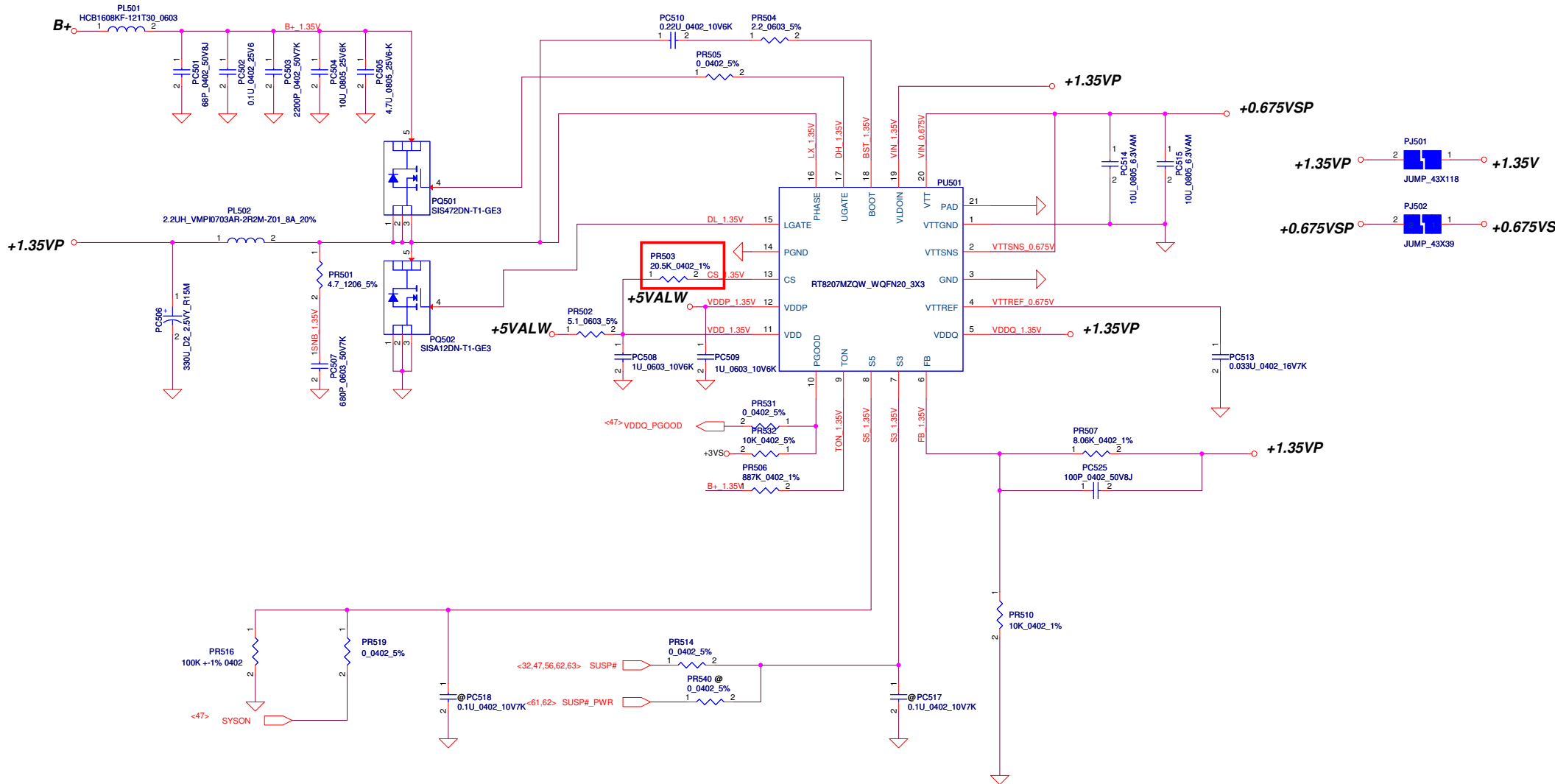
3VALWP $I_{max}=7.5A$ OCP current 8.6A~13.92A TYP MAX H/S Rds (on) : 22mohm , 30mohm L/S Rds (on) : 10.8mohm , 13.6mohm	5VALWP $I_{max}=10A$ OCP current 11.5~19.5A TYP MAX H/S Rds (on) : 22mohm , 30mohm L/S Rds (on) : 10.8mohm , 13.6mohm
--	--

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Title		3VALWP/5VALWP	
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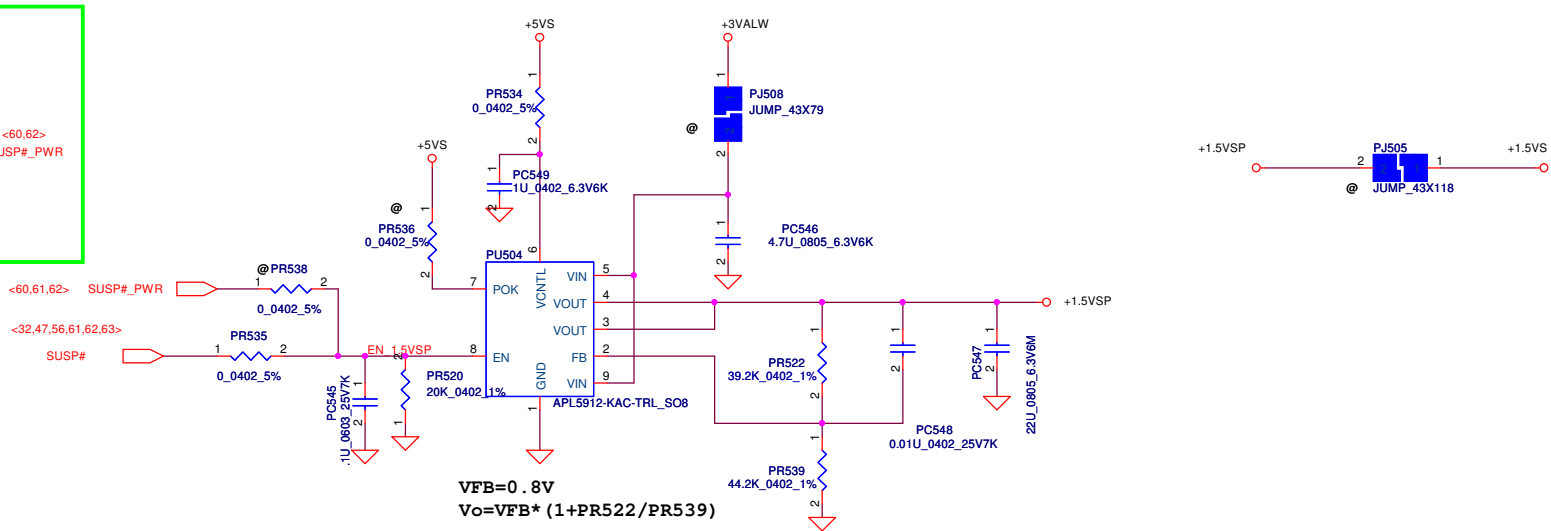
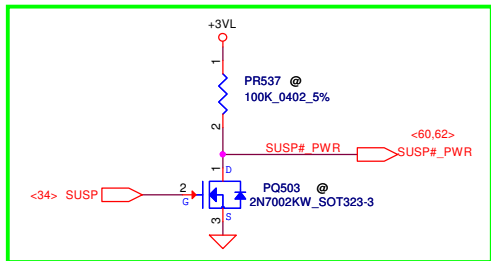
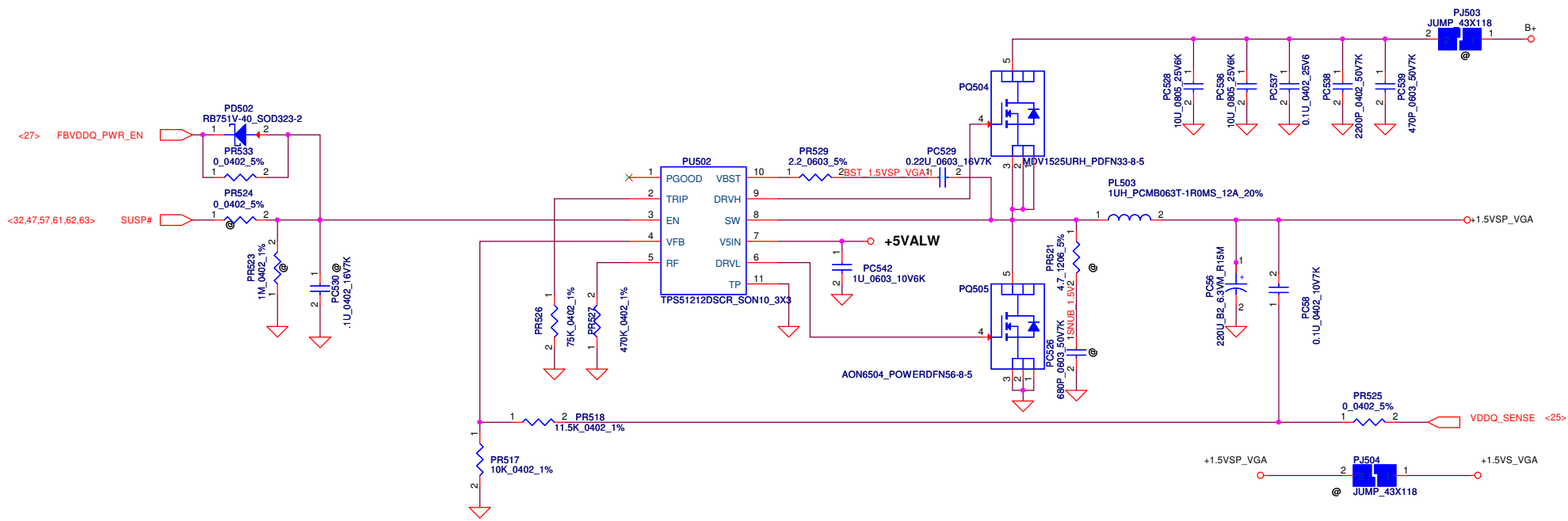
Rev 1.0



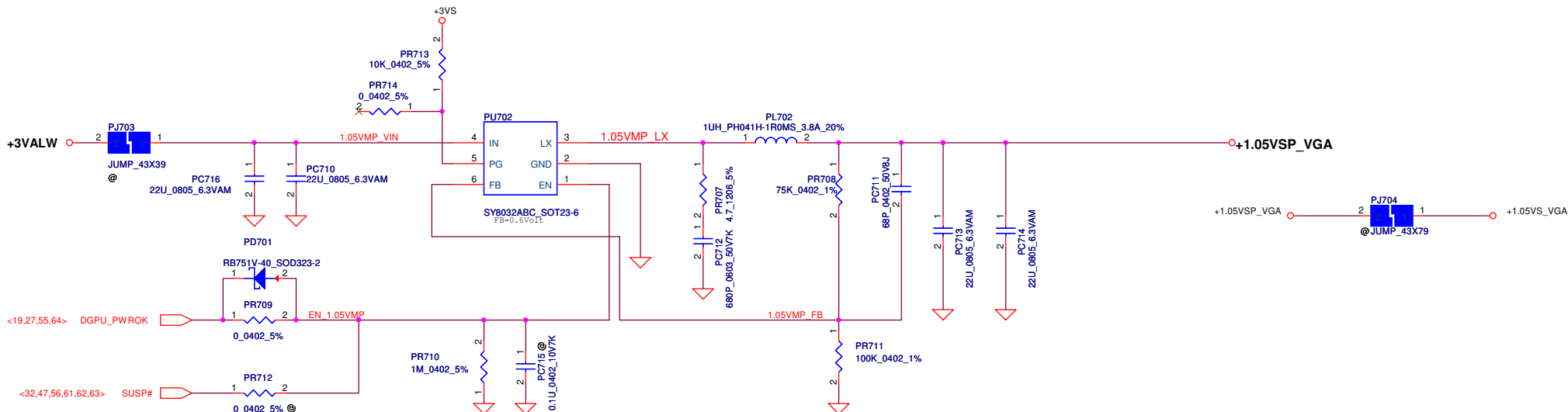
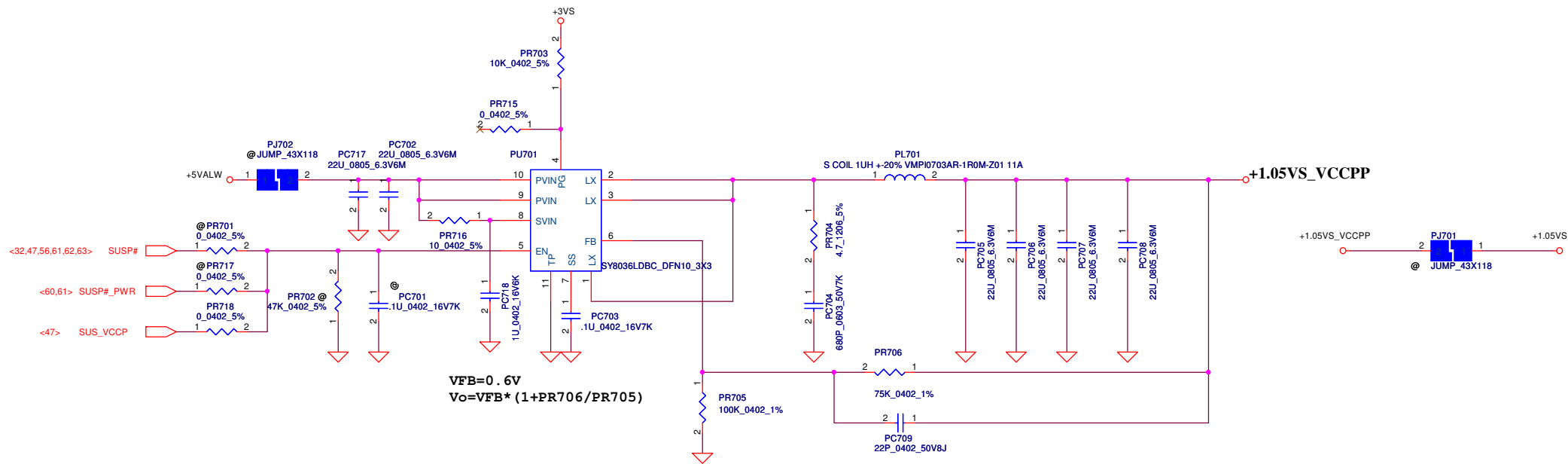
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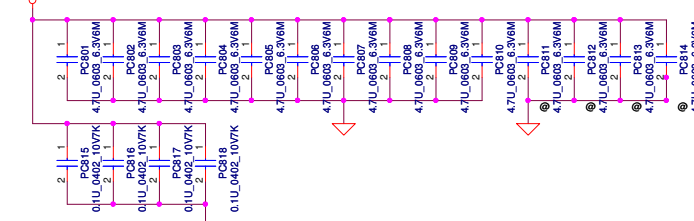


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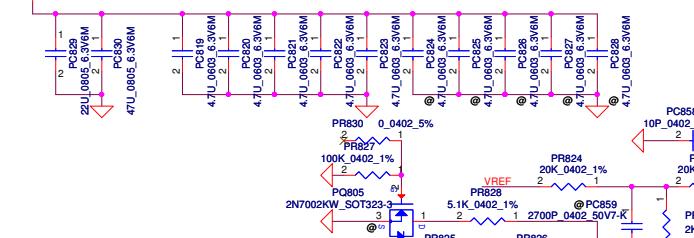


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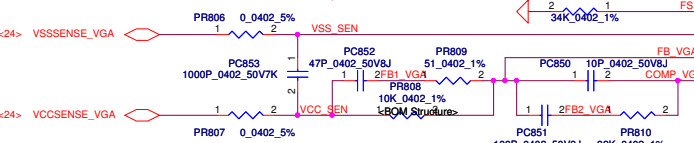
+VGA_CORE Under VGA Core GB4-128 package



+VGA_CORE Near VGA Core



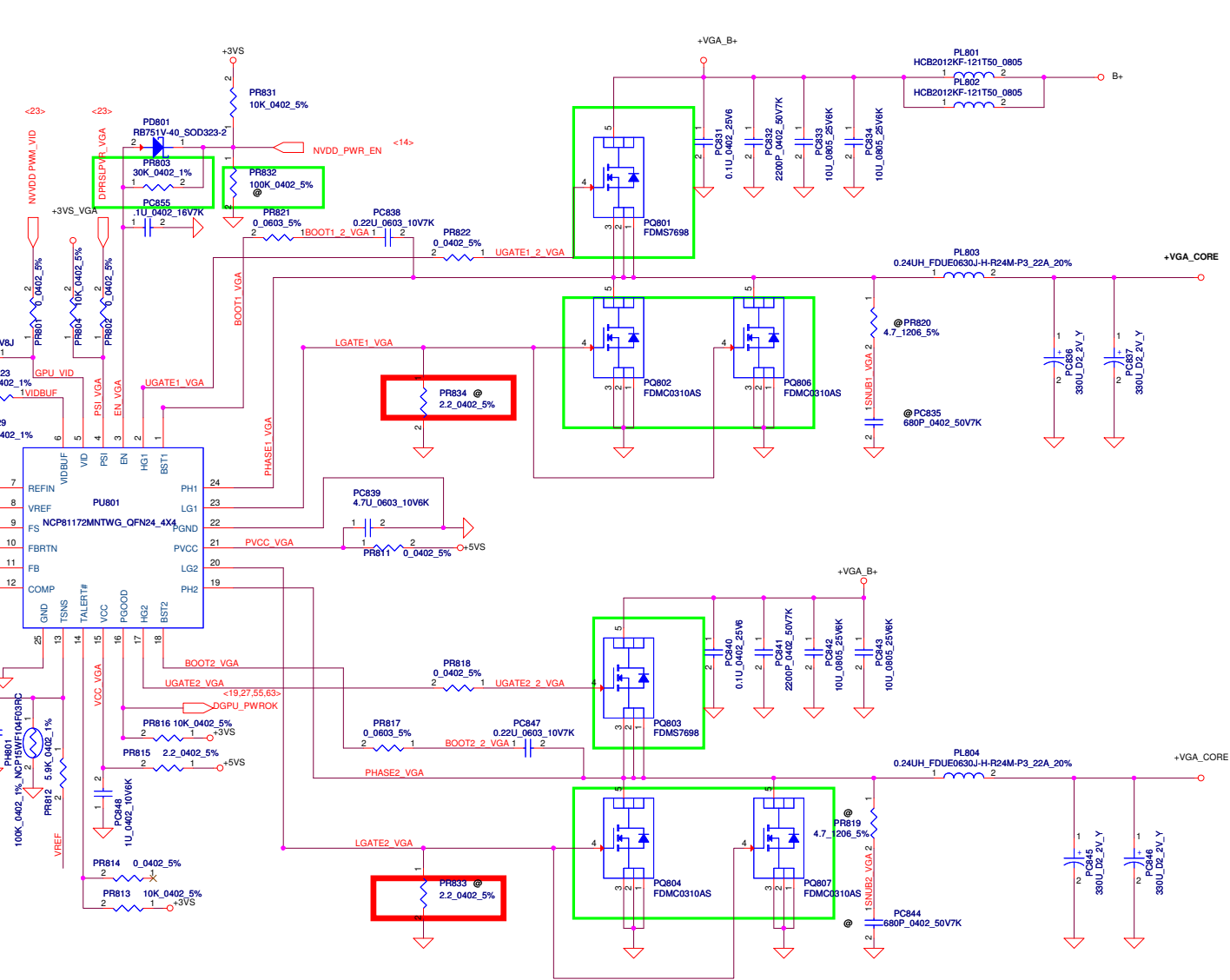
PR805 = 34K ==> Fsw = 450KHz



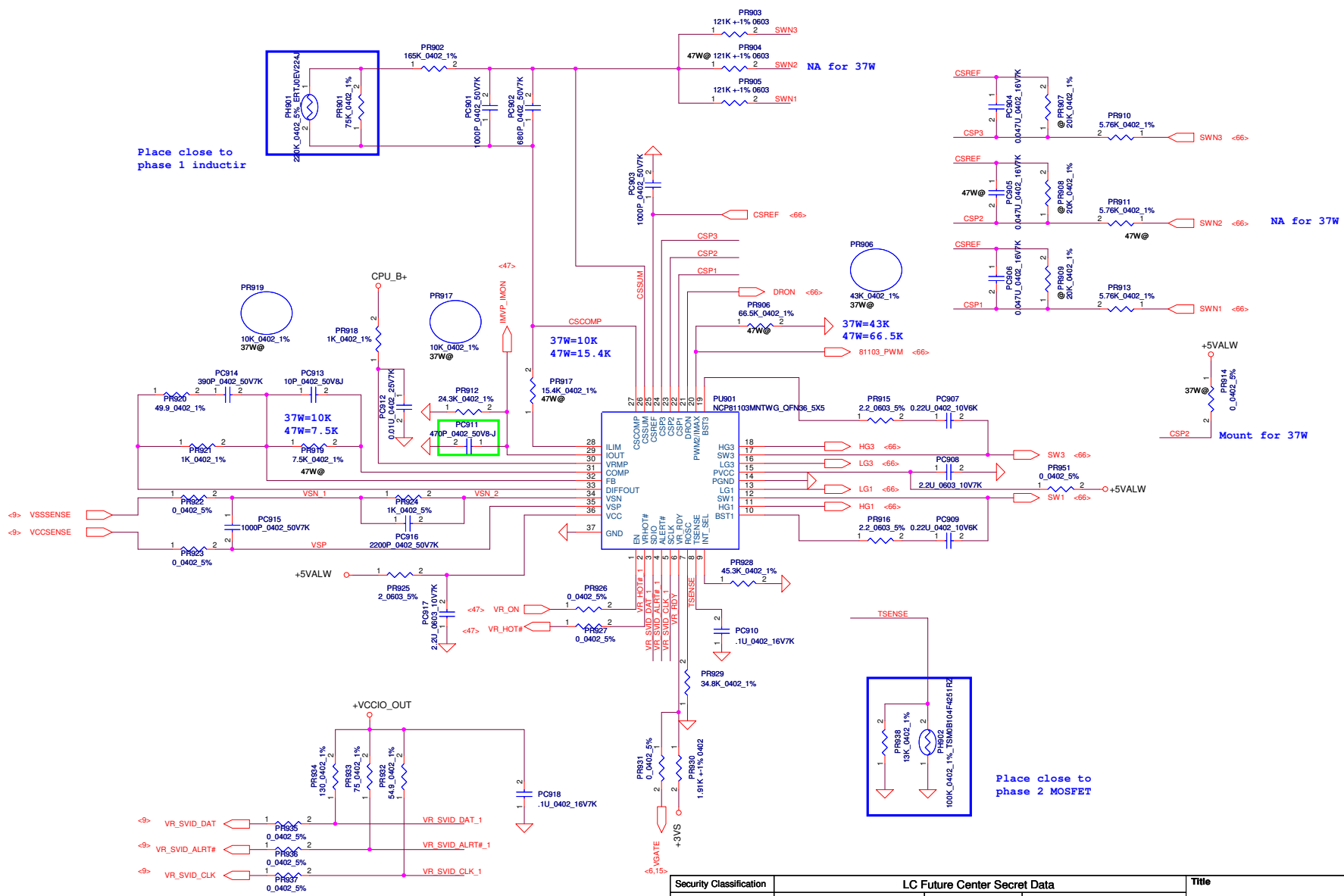
N14P-GT 35W
Ipeak=50A
Imax=35A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *5

N14P-GS 25W
Ipeak=36A
Imax=25A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *3

Thermistor near MOSFET trigger point 97 degree C.



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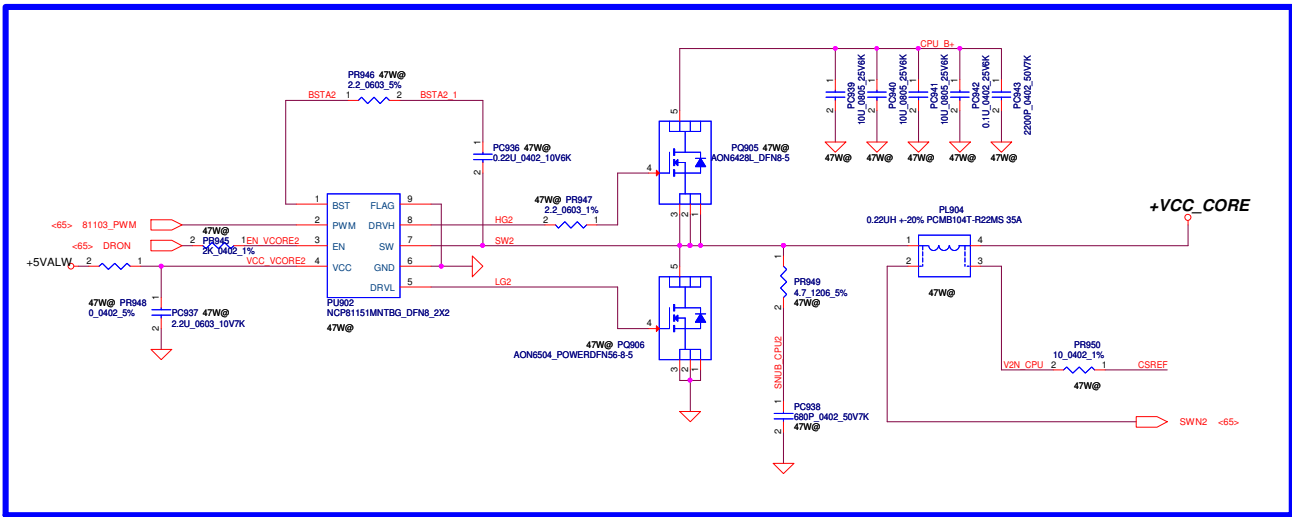
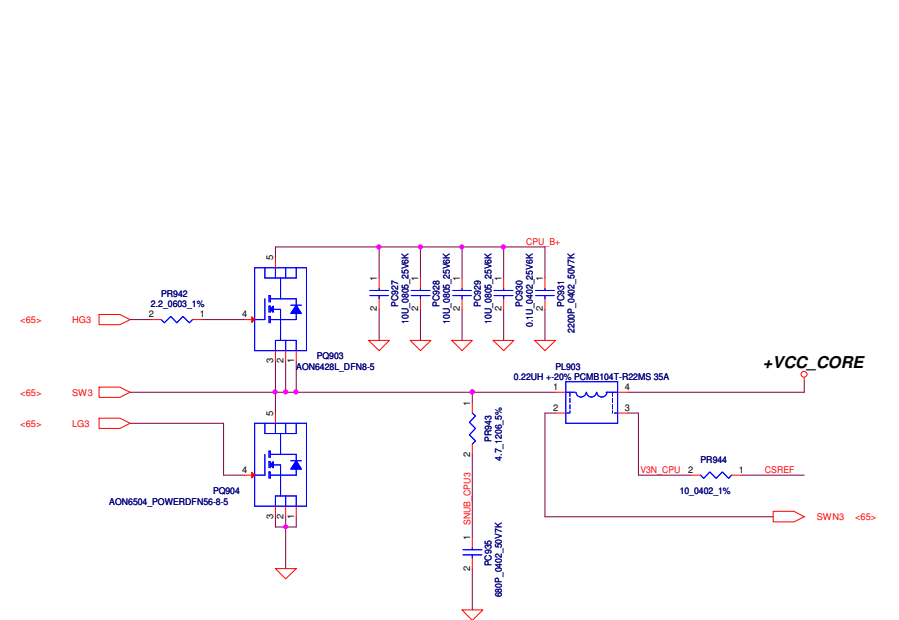
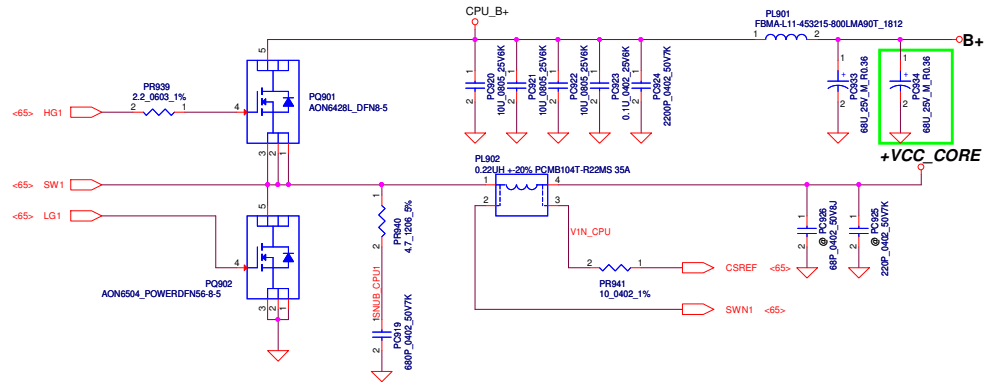
Place close to phase 1 inductor

Mount for 37W

Place close to phase 2 MOSFET

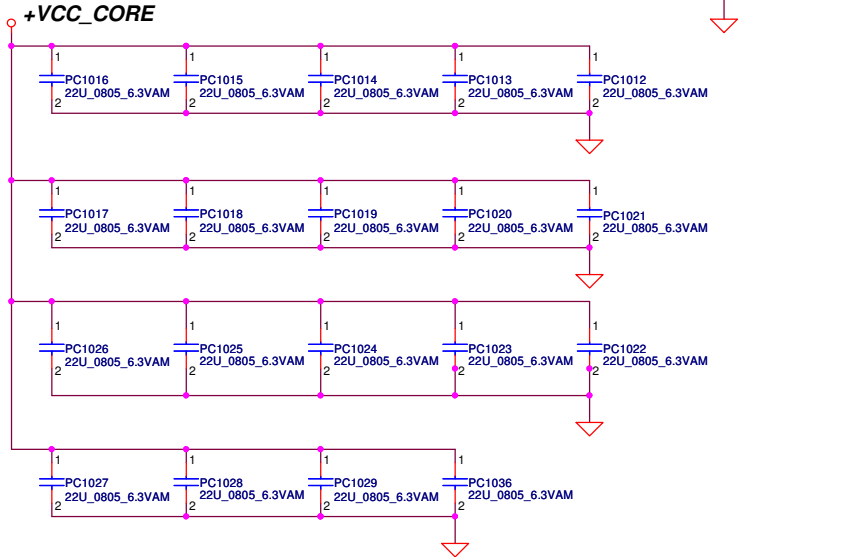
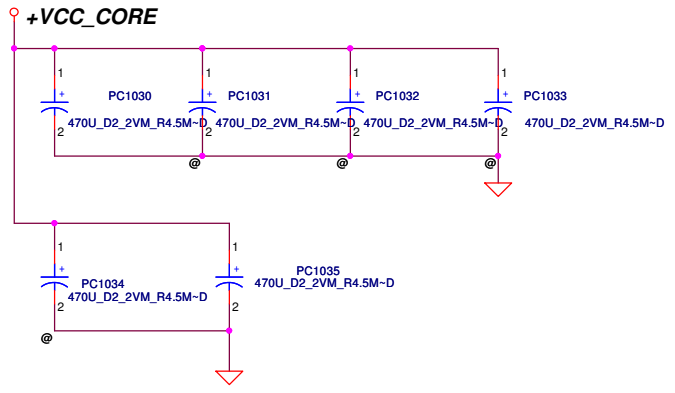
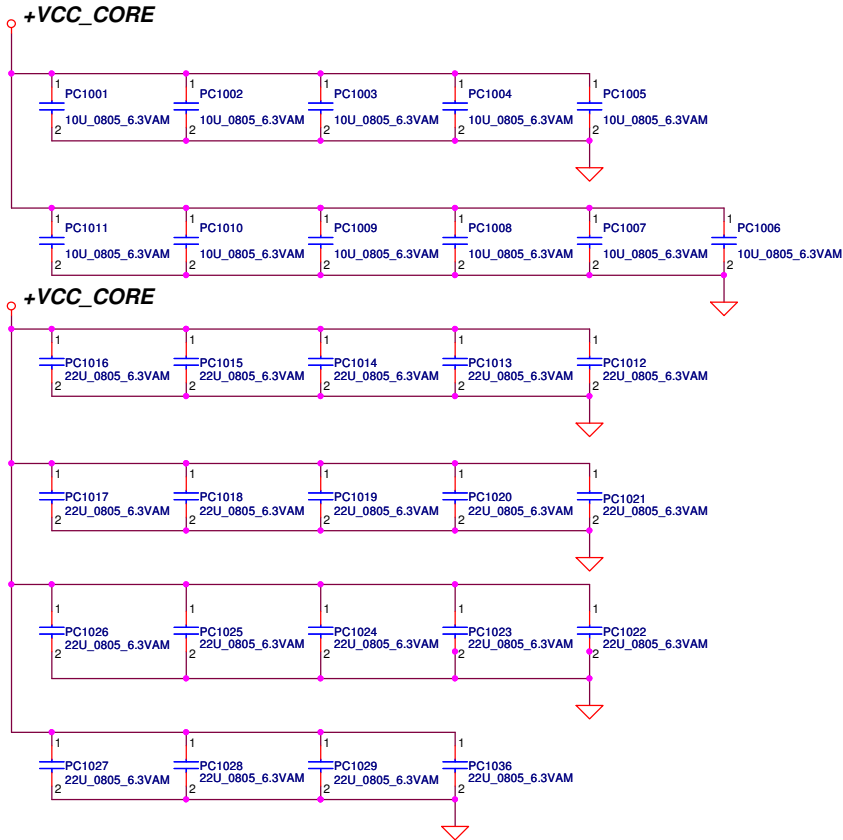
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CPU_CORE		
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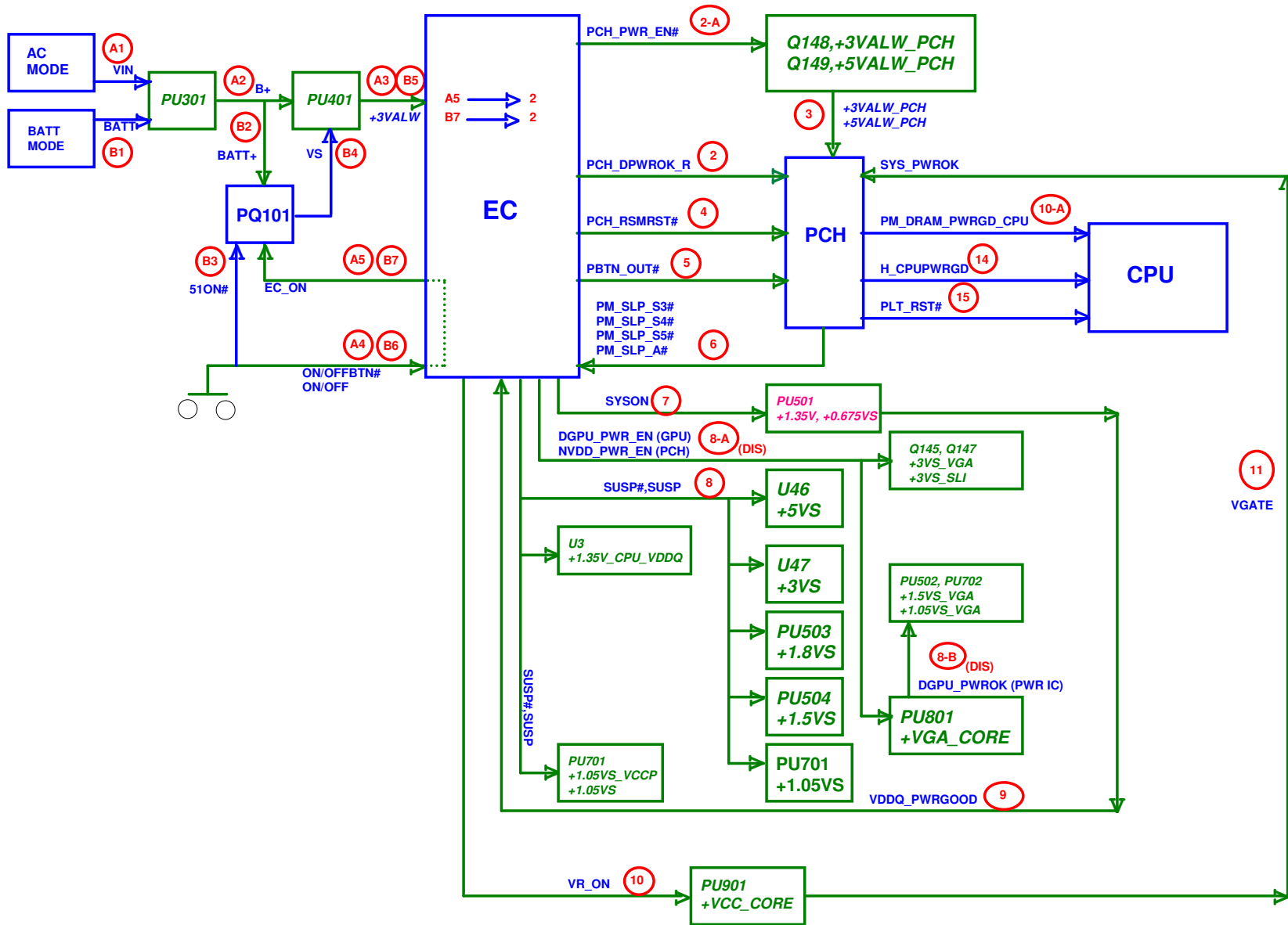
Mount for 47W

Based on PDDG rev 0.7 Table 5-1.



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Title		
PROCESSOR DECOUPLING		
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HW PIR (Product Improve Record)


QIQY5 LA-8691P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.2
 GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

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Issued Date	2012/07/01	Deciphered Date	2014/07/01	HW PIR		
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR PIR	
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