Embedded Systems Conference San Francisco

Conference: **March 6-10, 2005**
Exhibition: **March 8-10, 2005**

Moscone Convention Center San Francisco, CA

www.embedded.com/esc/sf

<THE LARGEST SYSTEMS DESIGN EVENT IN NORTH AMERICA >

300 leading experts presenting

250 hardware and software sessions

at the most comprehensive educational forum in North America

NEW TO THE EMBEDDED SYSTEMS CONFERENCE PROGRAM IN 2005

Design Seminars
Seminars focused on information across emerging technology sectors and enabling technologies **<see page 34>**

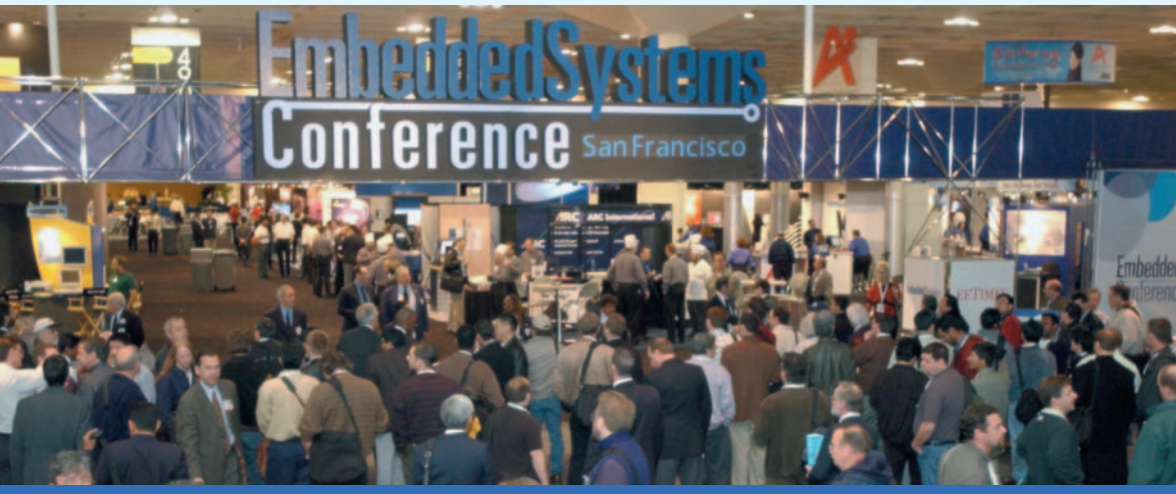
- Analog and Power Design Seminar
- DSP Performance Design Seminar
- Easy Paths to Silicon Design Seminar
- Consumer Systems Design Seminar
- 3G Cellular System Design Seminar
- Network Systems Design Seminar
- Wireless Networking Design Seminar

Microprocessor Summit
Chip companies announce their new plans and talk competitively about today's chips for embedded systems of all types. **<see page 9>**

Register by January 11, 2005
to receive the best conference rates!

UPDATED AS OF 11/18/2004

» The Most Comprehensive Educational Forum at



As an engineer or technology manager today, you face a host of complex challenges. One of these challenges is to expand your knowledge base within your specialization. The **2005 Embedded Systems Conference San Francisco** is an ideal forum to **learn** relevant new technical skills and the latest technologies; to **network** with industry experts, vendors and your peers; and to **discover** cutting-edge products from leading companies—**all under one roof, at one time.**

The Most Robust Technical Program Ever Offered at an Embedded Systems Conference

» 250 Sessions taught by 300 Industry Experts «

Embedded Training Program—the 17th year of this esteemed training program features 148 classes (a 12% increase over 2004) taught by industry experts on topics including embedded software development, hardware/software integration, debugging, real-time development, programmable logic design, wireless, and security. » See page 10 for session descriptions.

New in 2005: Design Seminar Series—seven seminars that address the needs of design engineers and technology managers for in-depth, future-looking, and vital design information. The seminars focus on design issues in emerging technology sectors including consumer, cellular, and networking, and enabling technologies such as field programmable gate arrays, digital signal processors, and analog design. » See page 34 for session descriptions.

New in 2005: Microprocessor Summit—a one-day forum for the introduction of new embedded processor, microcontroller, and digital signal processor architectures. A panel of industry experts offers evaluations of the new products, helping systems designers sort through their options in order to make better purchasing decisions. » See page 9 for more information.

Design matters, and quality design relies on cutting-edge information. The Embedded Systems Conference is the premier training opportunity for anyone involved in electronics design. **Cost-effective** and **time-efficient**, there is no better place to get the information and skills you need to succeed in today's challenging market.

We'll see you in San Francisco!

the Largest System Design Event in North America

"This is the must-attend event for systems design engineers. The best systems designers in the industry teach the technical sessions—it's invigorating to meet the authors of the books on my shelves that I reference regularly. I walked away with knowledge and ideas that I could implement immediately at work."

David Miller, Engineer, Cat Electronics, Software Center of Excellence, Caterpillar Inc.

Make the Most of Your Training Budget

Best Conference Value ePass

The ePass allows you to make an a-la-carte conference package customized to your individual needs. Choose from 250 sessions across the Embedded Training Program, Design Seminars, and Microprocessor Summit.

Pass Dates	Features		Register by Jan 11	Register by Feb 8	Register by March 3	Onsite Pricing
ePass [BEST VALUE] S M T W T ● ● ● ● ●	• Access to ALL of the 250 sessions offered in the Embedded Training Program, seven Design Seminars and Microprocessor Summit • Exhibition • Exhibit floor receptions	• Exhibitor workshops • Special events & networking • Downloadable class notes • Proceedings CD-ROMs • Conference bag • EEQuorum Portal	$1,795 **SAVE $400**	$1,945 **SAVE $250**	$2,045 **SAVE $150**	$2,195

Bring Your Whole Team Group Discount

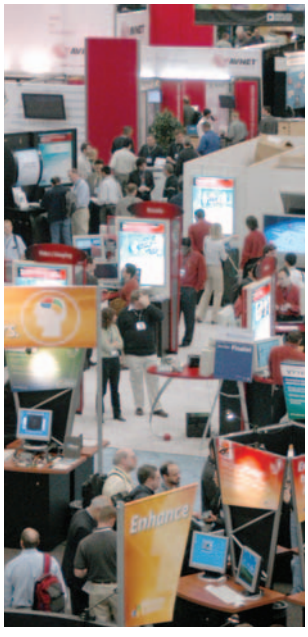
The more people you bring, the more you save. Discounts range from 15% to 35%. For more information call the registration team at 800 /441-8826.

Go To Page 48 for complete pricing and registration package information.

»THE LARGEST SYSTEMS DESIGN

"I liked the ease of browsing many potential vendors and products all in one location, without searching for hours on the Internet.."

—Graeme Coakley
Computer Engineer
Idean Robotics



Exhibitor List (as of 11/3/04)

A | AAEON Electronics, Inc.
AccelChip, Inc.
Accelerated Technology, a Division of Mentor Graphics
ACCES I/O Products, Inc.
Acrosser USA
Actel
ADLINK Technology, Inc.
Adtron Corporation
Advanced Digital Logic, Inc.
Advantech Embedded Computing
Agilent Technologies
Allegro Software Development Corp.
Alliance Semiconductor
American Arium
Ampro Computers, Inc.
Amulet Technologies, LLC
Analog Devices, Inc.
Aonix
Applied Data Systems
ARC International
ARM
ATI Technologies, Inc.
Atmel Corp.
Avnet Electronics Marketing
AVX Corporation
AXIOMTEK

B | BDTI-Berkeley Design Technology, Inc.
Beganto, Inc.
Beta Layout Ltd.
BiTMICRO Networks
Blackhawk
BP Microsystems, Inc.

C | Celoxica, Ltd.
Certicom Corp.
Chip Supply, Inc.
ChipX, Inc.
CMP Media LLC
CMX Systems, Inc.
Connect Tech, Inc.
Corelis, Inc.
Cosmic Software, Inc.
Cradle Technology, Inc.
Crossbow Technology, Inc.
CSM Computer Systems
Messtechnik GmbH

D | Dallas Semiconductor/MAXIM
Datakey Electronics
Datalight, Inc.
Derivation Systems, Inc.
DFI Technologies, Inc.
Digi International
Diversified Technology, Inc.

E | Earth Computer Technologies
EBSnet, Inc.
Echelon Corp.
eCosCenric Limited
eeProductCenter.com
EE Times
Electronics Supply and Manufacturing
Embedded Systems Programming
EMJ Embedded Systems
Emulation Technology, Inc.
Enea Embedded Technology
Enova Technology Corporation
esd electronics
Evalue Technology, Inc.
Express Logic, Inc.
Extended Systems

F | Feller US Corp.
FieldServer Technologies
First Silicon Solutions
Freescale Semiconductor
Fujitsu Microelectronics America
Future Electronics

G | GDA Technologies, Inc.
GE Fanuc Embedded Systems
Grammatech
Green Hills Software, Inc.

H | Harry Krantz Company
HI-TECH Software LLC
Hyperstone Electronics GmbH

» See the latest hardware, software, and development tool solutions from leading vendors in the electronics industry

» Watch product demonstrations and hear about new product launches

» Speak to product experts, compare products side-by-side and share experiences with your peers

» Hear first-hand about tomorrow's technology today

Exhibition Hours:

Tuesday, March 8	1:00pm – 8:00pm
Wednesday, March 9	10:00am – 7:00pm
Thursday, March 10	9:00am – 2:00pm

Register for a FREE exhibits pass today at www.embedded.com/esc/sf

EXHIBITION IN NORTH AMERICA

I | IAR Systems
ICP America, Inc.
I-Logix
Indesign, LLC
Infineon Technologies
InHand Electronics, Inc.
Intel Corporation
Interface Corporation
International Rectifier
Ironwood Electronics
iSystem
Ixxat, Inc.

J | Jungo Software Technologies

K | Keil Software
Kent Displays, Inc.
Kontron America
KUKA Controls, GmbH
Kyocera Industrial Ceramics Corp.

L | Lantronix
Lauterbach, Inc.
Leopard Logic, Inc.
Logic Product Development
LynuxWorks, Inc.

M | The MathWorks, Inc.
Matrix Orbital
MaxStream, Inc.
McObject LLC
MCC Micro Computer Control Corp.
Medical Electronics Manufacturing
Megatel Computer (1986) Corp.
Memec
MEN Micro, Inc.
Micrium
Microcross
Microsoft Corporation
MontaVista Software
Motorola
Moxa Technologies, Inc.
M-Systems, Inc.
Multi-Tech Systems, Inc.

N | National Instruments
NCI Logic Analyzers
NEC Electronics America, Inc.
NetBurner, Inc.
Newark InOne
Newport Electronics, Inc.
Nohau Corporation

O | Objective Interface Systems, Inc.
Octagon Systems
Okaya Electric
Oki Semiconductor
Open Interface North America, Inc.

P | Parvus Corporation
Perforce Software
PHYTEC America, LLC
Phyton, Inc.
pls Development Tools
PLX Technology, Inc.
Polyspace
Power Factor One, Inc.
Protech Systems
Purcell Brackets, Inc.

Q | QNX Software Systems
Quadros Systems, Inc.
QuickLogic Corp.

R | Rabbit Semiconductor
Reach Technology, Inc.
Renesas Technology
RICOH Electronics, Inc.
RSI, Inc

S | SBE
SBS Technologies, Inc.
Segger Microcontroller Systeme GmbH
Sharp Microelectronics of the Americas
Signum Systems
Silicon Labs
SMA Computers
SMSC
SNMP Research International
Softier, Inc.
Spectrum Digital, Inc.
StarGen, Inc.
STMicroelectronics
Stretch
SureSoft Technologies, Inc.
Synertron Technology, Inc.
Synopsys, Inc.

T | Tektronix, Inc.
Tern, Inc.
Texas Instruments
Texas Instruments Third Party Pavilion
TimeSys Corporation
Toronto Microelectronics, Inc.
Toshiba America Electronic Components, Inc. (TAEC)
TQ Components
TransDimension, Inc.
Transmeta Corporation
Treck, Inc.
Tri-M Systems and Engineering
Trimble
TriplePoint, Inc.
TSMC

V | Vanteon Corporation
Varta Microbattery, Inc.
VaST Systems Technology
Vector CANtech, Inc.
VersaLogic Corp.
VIA Technologies, Inc.
Vibren Technologies
Virtio
Virtual Silicon
Virtutech, Inc.
Vytek

W | Wasabi Systems
Western Design Center, Inc.
White Electronic Designs
WinSystems, Inc.
Wintec Industries, Inc.

X | XILINX, Inc.

Y | Yokogawa Corp. of America

Z | Z-World

"The presenters were interesting and energetic people. I have a better view of the industry and learned a lot from the presentations."

- Teo Chiang Mei
Engineer
Agilent Technologies Malaysia

Exhibitor Workshops

These free workshops are open to ALL attendees and will be held in the mezzanine area. Attend an exhibitor workshop to learn about specific solutions for your unique design challenges.

Workshops presented by:

Actel XILINX®

Visit www.embedded.com/esc/sf for more information and to register for an exhibitor workshop.

Pre-registration for exhibitor workshops is required.

Register for a FREE exhibits pass today at www.embedded.com/esc/sf

KEYNOTES

Embedded Systems Conference Keynote
From Cubicles to Comics

Dilbert Cartoonist, Scott Adams

Tuesday, March 8
12:00 pm – 1:00 pm

Dilbert cartoonist, Scott Adams, will describe his strange journey from corporate cubicles to the comic pages, show the comics that got him in the most trouble, and share some tips for success that you won't hear anyplace else.

Dilbert is published in over 2,000 newspapers, in 65 countries. Scott Adams has 29 books in print—over 10 million sold—including two number one New York Times best sellers.

Scott Adams was born and raised in Windham, New York, in the Catskill Mountains. He has lived and worked in California since 1979. He holds a BA in economics from Hartwick College, Oneonta, New York, and an MBA from the University of California at Berkeley. He's also a certified hypnotist.

Design Seminar Keynote
Software Defined Radio—Business, Market, and Social Ramifications

Stephen M. Blust, Chair of the SDR Forum

Mark Cummings, Chairman of the Board, SDR Forum

Wednesday, March 9, 3:45 pm – 4:45 pm

Today, SDR products are emerging in every sector of the wireless industry. And it's not just engineers and technologists who are working to harness the power of this disruptive technology. SDR is now a top priority with regulators, public safety and defense decision-makers, commercial business strategists, and venture capitalists around the world. This keynote will address SDR from an international perspective—from the viewpoint of the wireless carrier and the end user.

PANELS

Embedded Systems Conference Panel
The Future for Signal Processing Applications

Moderator: Jeff Bier, General Manager, Berkeley Design Technology, Inc.

Monday, March 7, 6:00 pm – 7:00 pm

This panel discussion explores how processors are evolving to meet the changing demands of signal processing applications. Panelists will confront questions such as whether digital signal processors can remain competitive with increasingly capable general-purpose processors, FPGAs, and other processor options.

View from C-Level Live: After the Storm. How the Industry's Changed Forever

Moderator: Brian Fuller, Editor-in-Chief, *EE Times*

Wednesday, March 9, 1:00 pm – 2:00 pm

Not only did electronics companies weather the storm of '01-'03, but they emerged Phoenix-like from the ashes of the worst-ever recession. But not all is well in Silicon Valley. Consolidation and the looming uncertainty of the rise of Asia weigh heavily on executives used to a fairly predictable cycle. How do some of the leading semiconductor and software executives view the changed nature of our business?

Engineering Humanity: Managing the Chaos

Moderator: Brian Fuller, Editor-in-Chief, *EE Times*

Thursday, March 10, 10:00 am – 11:00 am

The American engineer is under increasing pressure as the nature of the electronics business changes. Not only are engineers grappling with the offshoring trend but many baby boomer-generation members who signed on in the heady days of the space race are finding job security uncertain as they near retirement. How can engineers not only cope in a world of uncertainty but thrive in this new paradigm?

Additional Panel Discussions

Please review the Design Seminars on pages 36-47 for additional panels open to all attendees.

» Moving Beyond 3G: Where Do We Go From Here?

» The Transformation of the TV

» Silicon Support at Layer 7: XML, SOAP, and Vertical Protocols

» The Future of Wireless Networking

Shop Talks and Brown Bag Lunches

7:15 am and 1:00 pm daily, Tuesday - Thursday

Moderated by leading speakers from the Embedded Systems Conference programs, these free-form discussions are a great opportunity to swap ideas with your colleagues about common development problems and design challenges. Sessions are limited to the first fifty attendees. Please check the web site for a list of speakers. Note: no food or refreshments are provided for Brown Bag lunches.

Special events and networking opportunities are open to all attendees.*
For additional information on all these sessions, please visit www.embedded.com/esc/sf

Visit the web site for more information about all the special events and networking opportunities: www.embedded.com/esc/sf

ONLINE NETWORKING

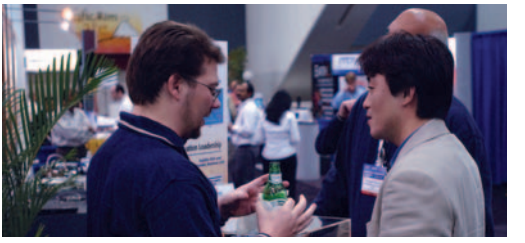
EEQUORUM

Super-charge your event networking experience with EEQuorum™ powered by BDMetrics, an online matching system that connects you with colleagues and vendors who offer the tools you need for your designs, and connects you to other engineers working in your field so you can share ideas and solutions. You will receive a FREE personalized EEQuorum event networking portal once you register for the Embedded Systems Conference San Francisco. The earlier you register, the earlier you can begin forging new business relationships using this innovative technology. Personalized portals will go live January 14, 2005, so don't miss out on this opportunity for pre-event networking.

RECEPTIONS

Tuesday, March 8, 7:00 pm – 8:00 pm
Wednesday, March 9, 5:45 pm – 6:45 pm

Enjoy beverages and tasty food on the exhibits floor on Tuesday and Wednesday evening. Meet with hundreds of exhibitors and network with thousands of your colleagues, peers, and industry experts from across the electronics industry.



AWARDS

EE TIMES ACE AWARDS

EE Times' Annual Creativity in Electronics Awards Gala

Wednesday, March 9, 7:00 pm – 9:00 pm

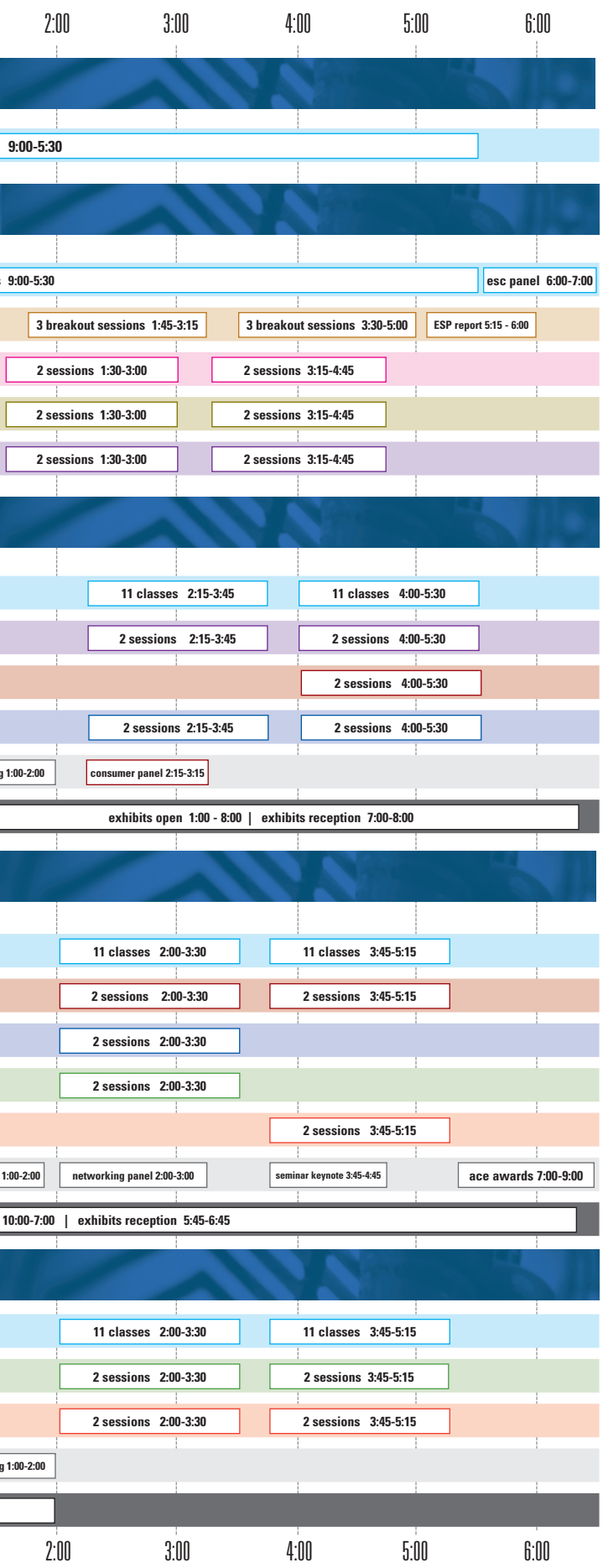
EE Times will recognize and honor the people, companies, and products that demonstrate leadership in the electronics industry at their first Annual Creativity in Electronics Awards. To purchase a ticket or to nominate your product, company, or executive for the 2005 *EE Times* ACE Awards visit www.eetimes.com/ace. Nomination deadline is December 31, 2004.

*ticket required for ACE Awards

"I made good new contacts in my related industry and caught up with former colleagues."

—Rod Kirk, Applications Engineering Manager, AMCC


8:00
9:00
10:00
11:00
12:00
1:00
Sunday : March 6
Embedded Training
8 full day tutorials
Monday : March 7
Embedded Training
8 full day tutorials
Microprocessor Summit
1 morning general session 8:30-12:00
luncheon 12:00-1:30
Analog and Power
2 sessions 8:30-10:00
2 sessions 11:00-12:30
DSP Performance
2 sessions 8:30-10:00
2 sessions 11:00-12:30
Easy Paths to Silicon Seminar
2 sessions 8:30-10:00
2 sessions 11:00-12:30
Tuesday : March 8
Embedded Training
11 classes 8:30-10:00
11 classes 10:15-11:45
Easy Paths to Silicon Seminar
2 sessions 8:30-10:00
2 sessions 10:15-11:45
Consumer Systems
2 sessions 8:30-10:00
2 sessions 10:15-11:45
3G Cellular Systems
2 sessions 8:30-10:00
General
shop talk 7:15-8:15
3G cellular panel 10:15-11:15
ESC keynote 12:00-1:00
brown bag
Exhibits
Wednesday : March 9
Embedded Training
11 classes 8:30-10:00
11 classes 11:00-12:30
Consumer Systems
2 sessions 8:30-10:00
2 sessions 11:00-12:30
3G Cellular Systems
2 sessions 8:30-10:00
2 sessions 11:00-12:30
Wireless Networking
2 sessions 8:30-10:00
2 sessions 11:00-12:30
Network Systems
2 sessions 8:30-10:00
2 sessions 11:00-12:30
General
shop talk 7:15-8:15
C-level live
Exhibits
exhibits open
Thursday : March 10
Embedded Training
11 classes 8:30-10:00
11 classes 11:00-12:30
Wireless Networking
2 sessions 8:30-10:00
Network Systems
2 sessions 8:30-10:00
2 sessions 11:00-12:30
General
shop talk 7:15-8:15
humanity panel 10:00-11:00
wireless panel 11:15-12:15
brown bag
Exhibits
exhibits open : 9:00-2:00
8:00
9:00
10:00
11:00
12:00
1:00



Special Events

[open to all attendees]

Embedded Systems Conference Keynote

From Cubicles to Comics

Scott Adams
Dilbert Cartoonist
Tuesday, March 8 12:00 pm–1:00 pm

Design Seminar Keynote Address

Software Defined Radio—Business, Market, and Social Ramifications

Stephen Blust
Chair of the SDR Forum

Mark Cummings
Chairman of the Board
SDR Forum

Wednesday, March 9 3:45 pm–4:45 pm

Embedded System Conference Panel

The Future of Signal Processing Applications

Moderator: Jeff Bier
General Manager
Berkeley Design Technology, Inc.
Monday, March 7 6:00 pm–7:00 pm

View from C-Level Live: After the Storm. How the Industry's Changed Forever

Moderator: Brian Fuller, Editor-in-Chief, *EE Times*
Wednesday, March 9 1:00 pm–2:00 pm

Engineering Humanity Panel: Managing the Chaos

Moderator: Brian Fuller, Editor-in-Chief, *EE Times*
Thursday, March 10 10:00 am–11:00 am

Exhibits Floor Receptions

Tuesday, March 8 7:00 pm–8:00 pm
Wednesday, March 9 5:45 pm–6:45 pm

Check-in/Registration Hours

Sunday, March 6 7:30 am–4:00 pm
Monday, March 7 7:30 am–5:30 pm
Tuesday, March 8 7:30 am–8:00 pm
Wednesday, March 9 7:30 am–7:00 pm
Thursday, March 10 8:00 am–4:00 pm

Exhibition Hours

Tuesday, March 8 1:00 pm–8:00 pm
Wednesday, March 9 10:00 am–7:00 pm
Thursday, March 10 9:00 am–2:00 pm

Lindsey Vereen
Conference Director
Embedded Group Editorial Director

The Embedded Systems Conference San Francisco Advisory Board is made up of industry experts who provide invaluable aid in identifying important topics and trends in the embedded industry. Their expertise guides the content of the technical program and keeps it current and educational for conference attendees.

Michael Barr
President
Netrino Consultants Network

Bruce Powel Douglass
Chief Evangelist
I-Logix

Larry Mittag
Lead Consultant
Mittag Enterprises

Jeff Bier
General Manager
BDTI

Jack Gannsle
Chief Engineer
The Ganssle Group

Dan Saks
President
Saks & Associates

John Canosa
Chief Scientist
Questra

Bill Gatliff
Independent Consultant

Tom Starnes
Chief Analyst
Gartner Dataquest

Tom Cantrell
Editor
Circuit Cellar

Jean Labrosse
President
Micrium, Inc.

Jim Turley
Editor-in-Chief
Embedded Systems Programming

Christopher Leidligh
Director of Embedded Communications
American Power Conversion

AFFILIATED COMPANIES

Industry companies affliated with the technical program include:

Actel
Altera
American Power Conversion
Analog Devices
Artesyn Communication Products
Atheros Communications
Atmel
Avnet
BDTI
Ericsson
Freescale Semiconductor, Inc.
Green Hills Software
Hewlett-Packard Co.
Hughes Network Systems
IBM
IDT
I-Logix
Intel Corp.
Linear Technology Corp.
Linley Group
Lynux Works, Inc.
Mentor Graphics
Microchip Technology
National Instruments
National Security Agency
National Semiconductor
NEC Electronics
Nokia
Nortel Networks
OSE Systems
Philips Semiconductors
PMC-Sierra
Portelligent
QNX Software Systems
Qualcomm Incorporated
QuickLogic
Raytheon Company
SafeNet
Saks & Associates
Sharp Microelectronics
Skyworks Solutions
STMicroelectronics
Synopsys
Teja Technologies
Tektronix
Tensilica
TeraChip
Texas Instruments
The MathWorks
Thomson
TimeSys
Toyota Motor
Vector CANtech
Wind River Systems
Xilinx

For a complete list of faculty, please visit www.embedded.com/esc/sf

Attend the Microprocessor Summit, held at the Argent Hotel, by purchasing the one-day Microprocessor Summit Pass or the ePass. See page 48 for all pass options.

NEW! **Microprocessor Summit presented by *Embedded Systems Programming***

The Microprocessor Summit, the newest part of the Embedded Systems Conference (ESC), provides a forum for major semiconductor companies to talk about their near-future plans—as well as current chips. The one-day program starts with a morning of juried announcements of new products by leading and upcoming chip vendors. Each presentation is coupled with piercing discussion led by an editorial moderator.

The afternoon sessions focus on today's shipping processors and is intended for buyers and decision makers. It's organized in three parallel tracks along product-specific lines, with each track led by industry analysts Jim Turley, Linley Gwennap, and Jeff Bier. They'll cover embedded processors, network processors, and media/signal processors, respectively.

The day concludes with the first release of survey results from the 2005 ESP Embedded Survey to the audience of embedded designers, chip architects, executives from the chip industry, analysts, press, and venture capitalists.

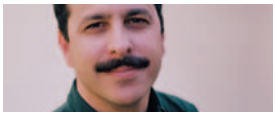
The new one-day Microprocessor Summit, moderated by Jim Turley, provides a forum to introduce new embedded processors, microcontrollers, or digital signal processors, and to talk about the pros and cons of today's processors. The program includes both new and existing variants of architectures and product families. A panel of industry experts offers evaluations of the products, helping systems designers sort through their options in order to make better purchasing decisions.

Program Highlights

- Geared toward working engineers evaluating real products
- Moderated and/or juried presentations by independent editors (No marketing fluff)
- Real chips for real designers—Price, performance, software, and support are all considered
- Fun!—No long-winded presentations or sales pitches, but a lively day with useful material

Event Chair:
Jim Turley
Editor-in-Chief,
Embedded Systems Programming

Session Chair:
Jeff Bier
General Manager,
Berkeley Design Technology, Inc.



Session Chair:
Linley Gwennap
Principal Analyst,
The Linley Group, Inc.

Copper Sponsor: **MIPS Technologies, Inc.**

Due to the late-breaking nature of the content for the Microprocessor Summit, the program was not finalized when this catalog went to print. Program details will be finalized and live on our web site at the end of January. Please check the site for complete session and speaker information: www.embedded.com/esc/sf

Program Chair: Lindsey Vereen, Conference Director, Embedded Group Editorial Director

Now in its 17th year, the Embedded Systems Conference training program has a strong reputation for offering high-caliber, solutions-oriented technical sessions. The technical program is a fundamental educational tool offering practical, how-to classes designed to meet the needs of engineers developing embedded systems. The classes offered are designed to provide knowledge of methodologies, processes, and techniques. Topics covered include embedded software development, hardware/software integration, debugging, real-time development, programmable logic design, wireless and wired connectivity, and security. New in 2005, you will find more classes and an additional full day of tutorial content, see below.

9:00 am – 5:30 pm

UPDATED! ETP-100 From CPLDs to FPGAs to ASICs

Bob Zeidman

Key Takeaways Attendees will learn how to determine which technologies and architectures of ASICs and programmable devices are suitable and how to design them.

Introductory: Understanding of digital hardware design required.

Complex Programmable Logic Devices (CPLDs), Field Programmable Gate Arrays (FPGAs), Application Specific Integrated Circuits (ASICs). What are they? What are their underlying architectures? How do you design one and what are the advantages and tradeoffs? What potential problems do you need to be aware of? How do you plan a project that incorporates one or more of these chips? These are the questions that this tutorial will answer.

NEW! ETP-101 User Interface Design

Niall Murphy

Key Takeaways The process of designing the user interaction by performing task analysis and usability trials as well as how to identify properties in an interface.

Introductory

This tutorial teaches the skills required to design a new user interface or recognize where an existing interface can be improved. It strikes a balance between concrete topics such as menus and icons, and providing the attendee with general principles for good design, such as direct manipulation. The tutorial examines the process of developing a user interface by task analysis and how it is evaluated in user trials. Both graphical and non-graphical interfaces are considered, and examples discussed include industrial equipment, medical equipment and consumer devices.

NEW! ETP-102 Migrating from a Legacy RTOS to Embedded Linux

Michael Anderson

Key Takeaways How the embedded Linux environment compares to the legacy RTOS in terms of features, memory model, scheduling algorithms, threading models and I/O systems.

Intermediate: Familiarity with an RTOS such as VxWorks(TM) or pSOS(TM) recommended.

As Linux continues to gain strength in the embedded marketplace, many companies are considering moving their existing, or developing new applications, for an embedded Linux environment. However, there is a considerable investment in both legacy code base as well as engineering talent that is focused on the legacy RTOS. This tutorial is targeted at dispelling much of the fear, uncertainty and doubt being put forward by the RTOS companies by showing the similarities and differences between Linux and the RTOSes. A strategy for migrating applications will also be presented.

NEW! ETP-103 Scaling System Design

Stephen J. Mellor

Key Takeaways How to build models, select model compilers, meet performance criteria, and modify rules.

Intermediate

As system complexity rises to the point we can no longer cope, a major problem is maintaining a single overarching architecture that ties the system into a coherent whole. In addition, piecemeal implementation causes testing and integration problems. By applying off-the-shelf model compilers consisting of modifiable rules to a model of an application, we can be assured of a complete consistent implementation. This tutorial shows how to build application models and select an appropriate model compiler, to ensure that performance is adequate, and modify model compilation rules as necessary to get code that screams.

ETP-104 Embedded Linux Jumpstart

William Gatliff

Key Takeaways A headstart on using GNU tools and Linux for embedded applications.

Intermediate: Fundamental embedded programming concepts and prior programming experience required; Linux experience a plus.

This tutorial provides a complete introduction to using Linux as an embedded operating system and is delivered by a real embedded Linux programmer, using real embedded Linux hardware. The tutorial begins with a brief overview of Linux and its suitability for certain types of embedded applications, along with a discussion of how the GNU licenses (under which Linux is provided) actually do permit using Linux in some kinds of proprietary embedded applications. The instructor then demonstrates how to build, install and use Linux on a commercially available single board computer.

ETP-105 Embedded C Programming

Michael Barr

Key Takeaways Everything you ever wanted to know about developing real-time embedded software and device drivers in C.

Introductory: Familiarity with C required.

This tutorial covers a large number of key concepts associated specifically with real-time and embedded systems programming. Topics include C startup code and the world before main; writing, installing, and debugging interrupt service routines; making code reentrant; and the correct use of C's volatile keyword. The development of device drivers that interact with peripheral control and status registers through memory-mapped I/O, overlayed structs, and bitfields is demonstrated. Bitmasks and bitfields are compared and contrasted.

NEW! ETP-106 Introduction to Real-Time Operating Systems

David Kalinsky

Key Takeaways How to select and use the appropriate kind of RTOS for an embedded system that has tight real-time response deadlines.

Introductory: Some background in developing embedded system software or firmware (with or without any real-time operating system).

Embedded systems developers use many different kinds of real-time operating systems (RTOSes), ranging from simple do-it-yourself cyclic software schedulers, to full-featured, off-the-shelf RTOS kernels containing priority-based preemptive schedulers and mechanisms for intertask communication and synchronization. This tutorial shows their features, and also takes a peek into the future of RTOSes. It begins with a survey of task schedulers and suggests when to abandon home-grown schedulers and consider using a commercial RTOS. It surveys intertask communication and synchronization mechanisms, including message queues, semaphores, and mutexes. The tutorial covers dynamic memory allocation techniques and concludes with examples of how to exploit an RTOS in embedded designs.

ETP-107 Real-Time UML

Bruce Powel Douglass

Key Takeaways How to apply the semantics and notations of the UML to software and systems designs, requirements modeling, with an emphasis on UML 2.0 and real-time concepts.

Introductory

The Unified Modeling Language can be effectively applied to all kinds of software systems including real-time embedded systems (RTES). This tutorial focuses on the key aspects of the UML relevant to RTES, including capturing functional and performance requirements, identifying objects and classes within RTES, and tying requirements to class models, concurrency, and distribution design. It also discusses behavioral descriptions using sequence diagrams and statecharts and the role of objects in high-reliability and safety-critical RTES design. The discussion includes the new UML 2.0.

"I enjoyed the ability to move between multiple conferences and courses, allowing me to speak with people and gain knowledge from areas I would normally never be exposed to."

Aaron Linsdau
Sr. Electrical Engineer
Callaway Golf

9:00 am – 5:30 pm

UPDATED! ETP-110 Real-Time Kernels

Jean Labrosse

Key Takeaways What a kernel is, how a kernel works, and how to use a kernel specifically in embedded products.

Intermediate: Knowledge of C and some assembly language required.

This tutorial explains what a real-time kernel is using the proper amount of code, graphics, animations, and running examples on an actual target CPU. It gives an understanding of real-time kernels by going into the internals of a scheduler, showing the steps involved in a context switch, and examining how semaphores, message queues, and many other common kernel services are typically implemented. This tutorial helps determine whether a real-time kernel can be used and if so, provides the knowledge to help make a selection from the many commercial real-time kernels currently available.

NEW! ETP-111 System Architecting and Tradeoffs

Kim Fowler

Key Takeaways The basic subsystems, architectural choices, processes, and tradeoffs in designing and developing a product.

Introductory

None of the systems we design exist in isolation. Consequently, there are no optimal solutions, but there are tradeoffs that we can make to improve the situation. This tutorial covers many aspects of preparing, designing, and developing a product including systems engineering, architecture, interface choices, review and testing, documentation, the human interface, packaging, power, cooling, problems, and buy vs. build.

UPDATED! ETP-112 Managing Embedded Projects

Jack Ganssle

Key Takeaways To run an embedded project in an efficient and effective manner, using practical no-nonsense methods.

Intermediate: Any assembly language and C required.

For all of the talk about technology, there is much too little said about managing the technology and managing the process of bringing an embedded system from concept to production. This tutorial covers managing schedules, dealing with difficult developers, creating and managing project specifications and expectations, creating an environment where developers will thrive, managing bugs to dramatically reduce development time, fixing the feature/schedule/quality conflict, and learning from mistakes and successes.

NEW! ETP-113 Real-Time Design Guidelines and Rules of Thumb

Dave Stewart

Key Takeaways Rules of thumb and tricks that will enable you to quickly make good decisions relating to the design and implementation of software.

Introductory

When you start the design of embedded software, do you have any of the following questions? Should my system include preemption? Should it be periodic or event driven? Should I use a commercial RTOS? Which real-time scheduling algorithm is best? How do I set up the schedule? How fast should I sample my sensors, or set the control rate? How can I eliminate priority inversion? What errors or "gotchas" am I not aware of that I should be? What is the best way to debug my real-time problems? This tutorial presents guidelines for making these decisions.

NEW! ETP-114 Embedded GNU Jumpstart

William Gatliff

Key Takeaways How to use GNU tools for embedded development.

Intermediate: Prior programming experience required.

This tutorial introduces the use of GNU tools for embedded development, using lectures combined with demonstrations and real-world examples. The materials are taken from the author's ten years of experience in producing embedded systems using GNU tools.

ETP-115 Crafting Embedded Systems in C++

Dan Saks

Key Takeaways To use C++ to write low-level device drivers as readable, yet efficient, abstractions.

Intermediate: Familiarity with basic constructs and some C++ experience required.

C++ offers the same low-level language facilities as C, including bitfields, bitwise operators, and casts. Therefore, you can use C++ to write device drivers that are every bit as efficient as they would be in C. However, such low-level code is often hard to write and maintain, and it's rarely portable. Using higher level features of C++, you can implement low-level device drivers that are much easier to read and maintain. Moreover, if you exploit C++ really well, you can write drivers that are almost, if not just, as efficient as they would be in C. This tutorial illustrates techniques involving nested constants and types, the const and volatile type qualifiers, overloading, unions and templates. It also provides a look "under the hood" to see how compilers and linkers implement C++ language features, giving you the insight you need to avoid many performance pitfalls.

UPDATED! ETP-116 Architectural Design of Device Drivers

David Kalinsky

Key Takeaways How to select an appropriate device driver design pattern, and architect the device driver.

Introductory: Some experience in software/firmware development at the software/hardware interface required.

While the focus in writing I/O device drivers is often at a nuts-and-bolts level of bit-bashing and register-twiddling, it's also possible to take a higher architectural-level view of device input/output driver software. This tutorial begins with the fundamental driver architectural issues of mutual exclusion in device access, and synchronous vs. asynchronous relations between application tasks and hardware devices. Then it gives examples of driver architectures of increasing complexity, followed by examples of synchronous and asynchronous device drivers. The tutorial includes a session on queueing theory as it applies to device drivers.

UPDATED! ETP-117 TCP/IP Networking

Christopher Leidigh

Key Takeaways Knowledge of the TCP/IP suite from the link layer through the application layer.

Introductory

This tutorial focuses on the internal workings of the TCP/IP network stack. It covers base protocols of IP, UDP, and TCP as well as application layer protocols that use TCP/IP. While no code is included, the tutorial will gives a basis of understanding of the mechanics and schemes used within the stack and protocols, which is critical for embedded designers using TCP/IP. The tutorial will work through the stack from the link layer to the application layer. The tutorial presents an overview of the protocols at each layer and covers application layer protocols such as DNS, SNMP, and HTTP.

8:30 am – 10:00 am

UPDATED! ETP-200 Designing with Real-Time Kernels, Part 1

Jean Labrosse

Key Takeaways Whether you can use a kernel in your embedded system and how to use some of the most common services provided by commercial kernels.

Intermediate: Knowledge of C Programming required.

Does your next embedded system needs a real-time kernel (also known as an RTOS)? This class examines the costs associated with an RTOS, whether you can actually use one, how to set task priorities, how to use some of the most common services provided by a kernel, how some can reduce priority inversions, and more. This class uses a combination of code, graphics, animations, and running examples on an actual target CPU to show you what a kernel can do. This is the first class in a two-part series.

ETP-201 Linux 101

Doug Abbott

Key Takeaways Insight into what Linux is, how it fits into the embedded space, and why you should care.

Introductory: Fluency in C and basic computer architecture knowledge required.

A large number of engineers grew up in the embedded world writing assembly language or C programs without reference to an operating system. Today Linux, a "free" operating system with full source code, looms large on the embedded horizon. Protected mode memory, the root filesystem, the Unix process model, device drivers—these are just some of the issues covered to give embedded engineers the tools they need to understand Linux and to use it effectively.

UPDATED! ETP-202 Principles of High Availability Embedded Systems Design, Part 1

David Kalinsky

Key Takeaways How to design embedded systems, including hardware and software, that are required to continue providing service despite the occurrence of internal and external faults.

Introductory

High availability systems design is based on a combination of redundant hardware components and software to manage fault detection and correction. This must be done without human intervention to achieve "five-nines" (99.999%) or greater availability, equivalent to less than 1 second of downtime per day. This class discusses basic hardware N-plexing and voting issues, as well as software and system fault tolerance techniques appropriate for embedded systems, starting with the static method of N-version programming. A number of dynamic software/system fault tolerance techniques are surveyed and the class ends with a forward error recovery technique. This is the first class in a two-part series.

NEW! ETP-203 Programmable Embedded Peripherals Simplify Complex Tasks

Murugavel Raju

Key Takeaways How a second processor can handle complex tasks in low-power embedded applications, leaving less intensive functions to the main processor.

Intermediate

Today's measurement world requires complex measurements that smart peripherals can't accommodate. One solution is programmable peripherals. CPLDs are one alternative but another approach is to have another set of CPU and memory attached to the smart peripheral. Changing the embedded software of the peripheral changes its function. This class describes this approach, and describes an electricity energy measurement meter as an application that can benefit from the approach.

NEW! ETP-204 Measuring Execution Time and Real-Time Performance, Part 1

Dave Stewart

Key Takeaways Techniques for measuring the real execution time of embedded programs, including advantages and disadvantages.

Intermediate: Knowledge of C or C++ and basic operating system concepts required.

Many embedded systems require hard or soft real-time execution. This class presents a variety of techniques, at both coarse-grain and fine-grain levels, to measure the execution time of both user code and operating system overhead. The measurements can then be used as the basis for accurate real-time scheduling analysis, for identifying timing problems, or to know what code needs to be optimized. This is the first class in a two-part series.

ETP-205 Embedded Programming 101, Part 1

Michael Barr

Key Takeaways How to write software that interfaces directly to hardware, including how to handle interrupts and access peripheral control and status registers through pointers, structures, and bitfields.

Introductory: Familiarity with C required.

This class covers a number of key concepts associated specifically with real-time embedded programming. Core topics include writing reentrant code, using the volatile keyword, and interacting with peripheral control and status registers through memory-mapped I/O. In addition, issues such as interrupt latency, watchdog timers, endianness, and determinism will be discussed. The class also uncovers subtle features of the firmware development process, including C startup code, cross-compilation, relocation, and remote debugging. This is the first class in a two-part series.

ETP-206 Implementing Downloadable Firmware with Flash Memory

William Gatliff

Key Takeaways A microprogrammer-based approach to flash memory reprogramming, and how this provides for safe and flexible field updates of embedded firmware.

Intermediate: C programming experience required.

This class presents several approaches to implementing field reprogrammability in embedded systems that use flash memory. The discussion includes source code, descriptions of the imitations and advantages of each approach, and ways to avoid common mistakes associated with downloadable firmware capabilities.

UPDATED! ETP-207 RTL Design Practices that Will Improve Firmware Development

Gary Stringham

Key Takeaways RTL design and style practices that will significantly help when writing firmware to control the chips.

Intermediate: Understanding of chip design helpful.

Too often, designs of FPGAs, ASICs, ASSPs, and other chips have negative impact on firmware development, causing schedule delays and lower quality in the embedded products being developed for market. Once a chip is in silicon form, it is generally too late to make RTL changes, causing the engineer to attempt workarounds in firmware to salvage the chip. This class teaches design practices in several areas of RTL design, such as documentation, registers, interrupts, aborts, and test hooks and makes it possible to more quickly develop the code, especially while debugging the interaction between the chip and firmware.

NEW! ETP-208 Debugging Elusive Digital Problems Quickly

David Haworth

Key Takeaways How to use the sophisticated trigger engine of modern logic analyzers to capture and analyze unusual circuit anomalies.

Intermediate

Debugging a digital system depends on being able to capture and analyze unique signal and event anomalies that are causing problems. These anomalies can be hard to find and capture. This class shows logic analyzer triggering techniques to find and capture these problems. Attendees learn how to trigger on errors such as clock glitches, crosstalk, termination errors, setup/hold violations, missing pulses, too narrow pulses, too long interrupt response times, power up configuration error, etc. These techniques will help capture bugs that threaten development schedule.

ETP-209 Short-Range Wireless Data Communications

Charles Knutson

Key Takeaways An understanding of short-range wireless technologies that are currently available and the trade-offs inherent to each.

Introductory

A plethora of short-range wireless data communication solutions now vie for the attention of embedded designers. The current crop includes IrDA, Bluetooth, 802.11b, Ultra Wideband, HomeRF and more. These technologies cover a wide range of capabilities and constraints. Sometimes they compete and other times they complement. Who will win? Who will lose? Do there have to be winners and losers? This class provides a survey of the broad range of short-range wireless data communication technologies currently available for embedded devices.

ETP-210 Noise and Shielding

Kim Fowler

Key Takeaways How to define, analyze, and select techniques for shielding circuits and subsystems from electrical noise.

Intermediate: Basic understanding of electromagnetic propagation, magnetic coupling, electrostatic forces, current flow and impedance required.

This class covers electromagnetic noise and how to design circuits and shielding to avoid it. It will present the sources of noise and the mechanisms for noise energy transmission and coupling. These mechanisms include conductive, inductive, capacitive, and electromagnetic couplings. The class includes methods for shielding and filtering noise. The topics include grounding, shielding, electrostatic discharge (ESD), general diagnostics, layout of signal traces, cables, and enclosures.

10:15 am – 11:45 am

UPDATED! ETP-220 Designing with Real-Time Kernels, Part 2
Jean Labrosse

This is the second class in a two-part series. Please see class ETP-200 for abstract.

UPDATED! ETP-221 Effective Use Cases for Real-Time Systems
Bruce Powel Douglass

Key Takeaways How use cases can structure requirements and how clear, unambiguous requirements can lead to robust testable designs.

Introductory

In the real-time and embedded domain, there are few references for how to effectively capture both the functional and quality of service requirements, so engineers in this domain are having a very difficult time effectively capturing requirements at the right level of detail. This class presents the approach the author has introduced at NASA/JPL for the capturing of the requirements for complex space mission requirements. This approach uses use cases, actors, sequence diagrams, and statecharts to capture requirements and then provides a means to track these requirements forward into the design of the system.

UPDATED! ETP-222 Principles of High Availability Embedded Systems Design, Part 2
David Kalinsky

This is the second class in a two-part series. Please see class ETP-202 for abstract.

UPDATED! ETP-223 TCP/IP for Embedded Engineers
Thomas Herbert

Key Takeaways Preparation for making the choices faced in deploying TCP/IP in an embedded project.

Intermediate: Basic understanding of programming techniques required.

This class explains TCP/IP, using the OSI model. The physical, data link, network, and transport layers are introduced including the TCP and UDP transport protocols. Specific requirements for TCP/IP are discussed for common intended uses in embedded systems. Linux sources are widely available and it is free from license costs and includes a stable tested TCP/IP stack proven in server class machines. The class examines Linux and compares it to other implementations of TCP/IP often used in embedded systems. This class also covers IPv6 and security.

NEW! ETP-224 Measuring Execution Time and Real-Time Performance, Part 2
Dave Stewart

This is the second class in a two-part series. Please see class ETP-204 for abstract.

ETP-225 Embedded Programming 101, Part 2
Michael Barr

This is the second class in a two-part series. Please see class ETP-205 for abstract.

UPDATED! ETP-226 Introduction to Posix Threads
Doug Abbott

Key Takeaways An appreciation for the features of Posix threads as a tool for building robust and efficient programs.

Introductory: Fluency in C required.

The heavyweight "process model," historically used by Unix systems, including Linux, to split a large system into smaller, more tractable pieces, doesn't always lend itself to embedded environments owing to substantial computational overhead. POSIX threads, also known as Pthreads, is a multithreading API that looks more like what embedded programmers are used to but runs in a Unix/Linux environment. This class introduces Posix Threads and shows you how to use threads to create more efficient, more responsive programs.

NEW! ETP-227 Basic Control Theory for the Software Engineer
Tim Wescott

Key Takeaways Use the z transform to perform basic control systems analysis and design tasks.

Advanced: Some experience with closed-loop control systems recommended. Working knowledge of simple controllers, ability to read C code, and advanced algebra required.

The z transform is an essential part of a structured control system design. This class describes the basics of using the z transform to develop control systems, using the sort of math that is familiar to the accomplished embedded system designer.

NEW! ETP-228 Introduction to the ANSI/EIA/CEA-709.1 Control Networking Protocol
Rich Blomseth

Key Takeaways Apply the ANSI/EIA/CEA-709.1 protocol to embedded applications that require network communication

Introductory

The ANSI/EIA/CEA-709.1 control networking protocol is in use in more than 40 million devices that have been installed in homes, buildings, factories, trains, and other embedded systems worldwide. Key features of the protocol are described at each of the seven OSI reference model layers. The EIA-709.1 protocol is compared to TCP/IP. A free API for embedded system developers is presented that can be used to create EIA-709.1 applications for any embedded microcontroller. The API functions are described, as well as the effort required to port the API to a new processor and to add control networking to existing embedded applications.

UPDATED! ETP-229 Wireless Protocol Stacks
Larry Mittag

Key Takeaways The strengths and weaknesses of a variety of wireless protocols to make more informed decisions about designing wireless systems.

Advanced: Solid understanding of communications protocol stacks and General understanding of how wireless communications work.

This class concentrates on the details of wireless protocol stacks that are useful to engineers that need to dig deeper into the technology than the typical application programmer. The goal is to allow you to use these stacks to their fullest potential in the specialized systems you are designing.

NEW! ETP-230 Top Ten Usability Mistakes

Niall Murphy

Key Takeaways How to identify end remove the most common mistakes made in the design of the user interface of an embedded device.

Introductory

In embedded user interfaces, the same mistakes appear again and again. A device with multiple modes confuses the user, or a screen times out just when the user is about to press a key. The text of the display uses terms that make sense to the engineer that designed the device but baffle the ordinary user. This class addresses these problems and looks at a set of examples of real products to identify the most common and easily eliminated usability mistakes.

2:15 pm – 3:45 pm

ETP-240 Inside Real-Time Kernels, Part 1

Jean Labrosse

Key Takeaways What a kernel is and how it works.

Intermediate: Knowledge of C and some knowledge of assembly language required.

This class examines the inner workings of a real-time kernel. Also known as an RTOS, it is software that manages the time of a microprocessor, microcontroller or DSP, allows multitasking, and provides valuable services to embedded applications. By understanding internals, you will have a better grasp on the issues involved when using a kernel. This class shows how a kernel works. You will experience the inner workings of a scheduler, see what's involved in a context switch, and examine how semaphores, message queues, and many other common kernel services are typically implemented. This is the first class in a two-part series.

UPDATED! ETP-241 Design Patterns for Tasks in Real-Time Systems

Michael Grischy

Key Takeaways Guidelines for partitioning an embedded application into tasks under a real-time operating system.

Intermediate: Familiarity with RTOS operation and knowledge of C required.

This class presents design patterns that are commonly used for partitioning an embedded systems application that run under a real-time operating system into tasks, with the goal of enabling programmers to apply them to their own work. These design patterns fall into three major groups: desynchronizing patterns, which partition the design into tasks that operate asynchronously to one another so that tasks can be prioritized; synchronizing patterns, which are used for controlling access to shared resources; and architectural patterns, which are used for implementing commonly occurring functional themes.

NEW! ETP-242 SysML: The New Systems Modeling Language

Bruce Powel Douglass

Key Takeaways The basic semantic and notational elements in the upcoming SysML language for modeling systems requirements and designs.

Introductory: Some basic familiarity with the UML required.

SysML is a new modeling language, heavily based on the UML 2.0 but significantly adding to and extending the UML. SysML provides continuous behavioral modeling and adds a number of new semantics concepts, such as parametric modeling, and several new diagram types. This standard is currently under development and will be released as a standard this year. This class reveals the internals of the SysML and how it can be used for effective systems development, as well as how systems designs can be efficiently passed on to software developers.

NEW! ETP-243 Embedded Systems Programming using DSPs

Robert Oshana

Key Takeaways A familiarity with the concepts, techniques, and processes for developing DSP-based applications.

Introductory

Developing embedded digital signal processing (DSP) applications is a complex task influenced by many parameters. But by using a systematic approach, the result can be an efficient implementation. This class provides an overview of application development techniques associated with DSPs in embedded systems. Topics include differences between DSPs and other general purpose processors, choosing a DSP for an embedded application, survey of DSP architectures, summary of tools for DSP application development, and real-time application development techniques using DSPs.

UPDATED! ETP-244 The 25 Most Common Mistakes with Real-Time Software Development, Part 1

Dave Stewart

Key Takeaways Recognize the most common problems encountered when building real-time systems and obtain an overview of methods and solutions to avoid making mistakes.

Introductory

This class presents the most common mistakes and pitfalls associated with developing embedded real-time software. The origin, causes, and hidden dangers of these mistakes are highlighted. Methods ranging from better education to using new technology and recent research results are also discussed. The mistakes vary from problems with the high-level project management methodologies to poor decisions on low-level technical issues relating to the design and implementation. This is the first class in a two-part series.

ETP-245 Embedded Linux Startup Code

William Gatliff

Key Takeaways Linux's startup procedure, and how to modify that procedure when porting Linux to an embedded platform.

Advanced: Prior experience with the Linux operating system and programming in C required.

This class is a walk-through of the startup-related portions of the Linux kernel source code, from the point the kernel begins running until the kernel is ready to run user programs.

ETP-246 Memory Management, Part 1

Niall Murphy

Key Takeaways How to evaluate the memory management options available to decide if malloc and free is appropriate for a project.

Intermediate: Knowledge of C programming required.

Use of memory in embedded systems must be measured to ensure the resources available are sufficient. The general purpose allocation mechanism available with most compilers can suffer from fragmentation, regardless of how carefully it is used. This is not acceptable for systems that have to run for long periods. Also a general purpose allocation scheme usually has undeterministic real-time properties as it may have to perform a search for memory of the appropriate size. This class looks at some custom alternatives that eliminate fragmentation and searches, such as fixed size pools. This is the first class in a two-part series.

NEW! ETP-247 PID without a PhD

Tim Wescott

Key Takeaways Design a closed-loop PID (Proportional, Integral, Derivative) controller.

Intermediate: Ability to read C required.

The PID controller is a common control strategy used in many control loops in the world today. This class teaches how to design and implement a PID controller in software. It uses practical examples to show how the various elements of a PID controller affect system performance, it gives methods for implementing PID controllers including how to avoid some common pitfalls, and it gives the designer guidance in designing the controller up-front to help estimate the processor load and insure the hardware design is adequate to the task.

NEW! ETP-248 Managing Power, Ground, and Noise in Microcontroller and Analog Applications

Bonnie Baker

Key Takeaways Good layout practices, their impact on noise, and the theory behind them.

Intermediate

Microcontroller applications often have low-level sensor signals and moderate power drive circuitry, in addition to the microcontrollers. A peaceful co-existence with these three extremes requires careful power and ground distribution design. This class discusses sources of noise in all three areas and the paths where the noise travels around. It also discusses the proper selection and placement of noise isolating and limiting components to keep digital and power noise out of sensitive input circuits.

UPDATED! ETP-249 Understanding and Using the 802.11 Standards

Larry Mittag

Key Takeaways What standards are in process and what they mean to engineers creating wireless systems.

Intermediate: Solid understanding of communications protocol stacks and a general understanding of how wireless LANs work.

This class examines the IEEE standards relating to wireless communications. The emphasis will be on what each standard means to working engineers creating embedded systems around wireless communications.

NEW! ETP-250 Fantastic Failures

Kim Fowler

Key Takeaways Understanding the place of failure in designing new products.

Introductory

Failure can be the source of useful information. This class presents several case studies of failures and illustrates what went wrong, what we can learn, and what we can do to avoid them. The case studies include Comet – the first jet-engine airliner that tested the limits of human knowledge; Therac-25 – a development nightmare in system design; Chernobyl – a study in human expertise, experience, and arrogance; Apple Lisa – great ideas before their time, a marketing miscue; Product recalls; and Sidewinder missile – innovative development practices that led to a system that is still useful 50 years later.

4:00 pm – 5:30 pm

ETP-260 Inside Real-Time Kernels, Part 2
Jean Labrosse

This is the second class in a two-part series. Please see class ETP-240 for abstract.

ETP-261 Executable UML
Stephen J. Mellor

Key Takeaways The components of executable UML, how they fit together, translation into code, what decisions need to be made, and at what time during the process.

Introductory: Familiarity with UML required.

Executable UML is here. When using the traditional approach of adding code to UML, a series of implementation decisions are made that may not be correct, appropriate, or even knowable. Executable UML changes all that by allowing for early verification through simulation of an UML. The model, once verified, can be translated directly into efficient code using an openly accessible, tunable model compiler.

NEW! ETP-262 Leveraging Bit-Stream Encryption to Protect IP and Proprietary Designs
Jie Feng

Key Takeaways How to implement an encryption scheme using programmable logic to protect against threats to proprietary IP and designs.

Intermediate

Now that FPGAs offer performance and costs comparable to ASICs and ASSPs, with the additional advantages of low development risk, faster time to market and flexibility, they are increasingly being used for critical system functions. Protecting designs implemented in FPGAs is becoming more important. The latest generations of SRAM-based FPGAs use configuration bitstream encryption to secure designer's intellectual property (IP). This class discusses the various types of security threats to programmable logic devices and details encryption methodologies that can be used to protect proprietary designs and IP implemented in FPGAs.

NEW! ETP-263 Embedded Systems Development: A Cookbook Approach
Thomas A. Bullinger

Key Takeaways Practical methods for architecting, designing, and developing embedded systems in a repeatable, reliable manner without introducing unwieldy process.

Intermediate

Building on previous presentations of SEEM, this class offers a detailed step-by-step approach for analyzing, designing and implementing an embedded system. A "cookbook" is presented that clearly delineates the sequence of SEEM artifact creation from problem description through implementation. The cookbook also describes tracking the dependencies among the artifacts, and the manner in which iteration is embraced in order to handle discovered bugs and changing requirements. SEEM's main hallmark—namely, traceability from an unambiguous problem definition to the implementation—is explicitly described.

NEW! ETP-264 The 25 Most Common Mistakes with Real-Time Software Development, Part 2
Dave Stewart

This is the second class in a two-part series. Please see class ETP-244 for abstract.

ETP-265 Embedded Linux Interrupt Code
William Gatliff

Key Takeaways An understanding of Linux's interrupt handling mechanism, and how to adapt that mechanism to an embedded platform.

Advanced: C programming and some experience with the Linux operating system required.

This class is a walkthrough of the interrupt-related portions of the Linux kernel source code, from the point an interrupt is asserted to the point the associated interrupt handler begins running. A brief look at how Linux interacts manipulates interrupt controller hardware is also provided.

ETP-266 Memory Management, Part 2
Niall Murphy

This is the second class in a two-part series. Please see class ETP-246 for abstract.

NEW! ETP-267 Building Signaling Platforms with ATCA
James Darroch

Key Takeaways How to construct scaleable signaling platforms, using the modularity of ATCA and well-structured protocol stacks.

Intermediate

The Advanced Telecom Computing Architecture (ATCA) defines a managed platform for building modular, flexible, scaleable platforms for Telecom applications. The ATCA specification includes the Advanced Mezzanine Card (AMC), hot-swappable modules that provide I/O (from T1/E1 up to Optical OC3/OC12 interfaces) or processing capability. Signaling and other networking protocols may be implemented on the I/O modules. Upper layers or call processing applications may be implemented on processing modules. Even voice processing is possible. This class describes how to construct scaleable signaling platforms with ATCA.

UPDATED! ETP-268 An Introduction to eCos
Nick Garnett

Key Takeaways A basic understanding of eCos, how to configure it for different platforms and how to write and build programs that use it.

Intermediate: Understanding the role of system software in embedded systems and familiarity with embedded hardware assumed.

eCos is an open source, royalty free operating system for embedded and real-time applications. It is highly configurable to allow only those features of the OS that are required for an application to be built into the executable. eCos attempts to fill the gap between buying a commercial RTOS and building it yourself. The class includes an introduction to the features supported by eCos and a demonstration of the configuration and building of an eCos system.

UPDATED! ETP-269 802.11 Security
Larry Mittag

Key Takeaways The strengths and weaknesses of a variety of security options for wireless communciations and just how secure wireless communications can be.

Advanced: Understanding of communications protocol stacks and how wireless LANs work required.

This class examines the options for securing wireless communciations. Special attention will be paid to the evolving standards for wireless LANs, including AES and 802.11i.

UPDATED! ETP-270 Mission-Critical and Safety-Critical Development

Kim Fowler

Key Takeaways The standards, processes, and documentation needed for developing safety-critical and mission-critical systems.

Introductory

This class covers issues in designing mission-critical and safety-critical systems. It provides the general processes used in design and development and illustrates them with two case studies: a satellite subsystem and a medical device. The topics cover the various aspects: the phases of development, documentation, plans, procedures, reviews, and reports. The class also addresses concerns over version control, archiving, traceability, and audits.

8:30 am – 10:00 am

ETP-300 Secure Embedded OS: A Technology Overview

Arun Subbarao

Key Takeaways Understand security problems in embedded operating systems and how to evaluate the security capabilities of an OS.

Intermediate: Basic understanding of RTOS internals and familiarity with processor architecture and software life-cycle & process methodology required.

One of the critical components involved in ensuring the security of embedded devices is the embedded OS. The security of an embedded device is extremely dependent on the ability of the OS to provide a secure environment for applications. This class provides an overview of the technology issues involved in designing a "Secure Embedded OS," and the implications of using it in secure embedded applications. Conformance to open standards is reviewed as well as process methodologies needed for secure OS development.

NEW! ETP-301 Writing Your First WinCE USB Device Driver

Joe Tykowski

Key Takeaways The basic information required to implement a WinCE 5.0 USB device driver.

Introductory: Basic understanding of C required.

The information required to write a USB device driver is plentiful, if you have the time and patience to find it. This class demonstrates, through the use of a practical example, a simple approach to writing a WinCE 5.0 USB device driver. The example includes the basic structure and requirements for implementing a device driver for a commercially available USB fingerprint sensor. The approach details how to write a WinCE stream driver, how to communicate via USB bus, how to install the driver on a platform, and how to ensure proper communication between the application and the device driver.

NEW! ETP-302 DODAF and the UML

Bruce Powel Douglass

Key Takeaways The basic concepts of the DODAF standard and the set of products specified in the standard, and how each may be represented with the UML.

Intermediate: Some basic familiarity with the UML required.

The Department of Defense Architecture Framework (DODAF) is a new standard, based upon the older C4ISR standard and specifies a semantic framework for representing architectures in a consistent way. The UML is a general modeling language but is particularly adept at clearly showing architectures, system structures, and behavior—all vital aspects of any DODAF-compliant product. The class demonstrates how useful and appropriate the UML is at creating both the required and supporting DODAF products.

NEW! ETP-303 Automated Coin Validation with Programmable Analog

Ian Macbeth and Jon Goldfinch

Key Takeaways How to dynamically reconfigure signal chains to make a hardware platform work across multiple sensors and tie them together into a automated coin validation system.

Intermediate

Embedded designs must access information from analog sensors. A common implementation for embedded systems is with analog sensors, fixed analog circuitry for signal conditioning and conversion into the digital realm, and a digital processing unit for processing and decision making. This class presents an architecture using analog circuitry that is dynamically changeable under software control. It describes this analog design methodology and its deployment in software-based systems using as an example a coin validation device that measures several different physical characteristics of the coins to determine their authenticity.

NEW! ETP-304 Implementing High Availability with the SA Forum Specifications

Steven Dake

Key Takeaways How systems using the Service Availability Forum specification are implemented.

Intermediate

The Service Availability Forum has published specifications for common APIs and methods for ensuring services remain available in an environment where uptime must be maintained at least at levels of 99.999% capacity. The SA Forum specifications cover the interfaces between the hardware layer and upper layers and the interfaces providing high availability services to the applications, application services and other middleware, referred to as the Application Interface Specification (AIS). An open source software implementation of AIS services is examined to understand how the specifications are applied in real applications.

UPDATED! ETP-305 C and C++ Gotchas, Part 1

Dan Saks

Key Takeaways How to anticipate and avoid gotchas in C and C++ programs.

Intermediate: C and C++ programming experience required.

Static checking in C catches many potential errors at translation time that might otherwise become run-time errors. C++ applies even stricter checks to weed out more errors at translation time. Nonetheless, C and C++ programs can still have "gotchas"—constructs that compile and link without diagnostics, yet produce unintended, and often disastrous, run-time results. This class explains why gotchas are an inherent part of C and C++. It presents numerous platform-independent C and C++ programming examples containing gotchas and, when possible, recommends ways to avoid them. This is the first class in a two part-series.

UPDATED! ETP-306 Optimizing C for Embedded Systems

Ted Schleich

Key Takeaways Optimization of embedded software applications for maximum performance and minimum memory requirements.

Intermediate: A good understanding of hardware/software interactions required.

This class presents several techniques used for optimizing software in embedded systems. The focus is on embedded systems programmed using the C language, however, the techniques presented are applicable to any software development in any software language. The topics presented are: optimization trade-offs, rules of optimization, generic optimization techniques for embedded systems, and compiler optimizations.

NEW! ETP-307 Internet Messaging and Mail Protocols

Christopher Leidigh

Key Takeaways The fundamentals of the primary mail protocols SMTP, POP and IMAP and how these protocols can be leveraged in embedded devices.

Intermediate

While SMTP, The Simple Mail Transfer Protocol, is the most widely used messaging protocol, there are others that can be used. This class presents the fundamentals of SMTP as well the the POP (Post Office Protocol) and IMAP (Interactive Mail Access Protocol) used in user mail handling. Two message protocols, SYSLOG and SNMP Traps are also presented which provide devices with the ability to send machine to machine messages. Understanding the variety of methods available for asynchronous message delivery will enable designers to chose the methods appropriate for their systems.

UPDATED! ETP-308 IP Version 6 and the Dual Stack

Christian Legare

Key Takeaways An understanding of IP version 6 features, benefits and new protocols, their interactions and inter-relations.

Intermediate: Binary and hexadecimal notation system, IP version 4 addressing scheme and Ethernet LAN required.

Internet Protocol version 6 (IPv6) improves on IPv4 by greatly increasing the number of available addresses and by enabling more efficient routing, simpler configuration, built-in IP security, better support for real-time data delivery, and other essential enhancements. Almost all of the transition mechanisms from IPv4 to IPv6 require the need for a host to run a dual stack: IPv4 and IPv6 together. Attendees are exposed to the challenges an embedded system engineer designing an IP enabled device faces when implementing an IPv6 or dual stack in terms of resources and performance.

NEW! ETP-309 Designing with Soft Processor Cores in FPGAs, Part 1

RC Cofer and Ben Harding

Key Takeaways Soft processor core architectures, benefits, costs, design flow, design challenges and mitigations, current vendor offerings and system requirement allocation for efficient design evaluation.

Introductory

This class presents an overview of Soft Processor Core (SpC) technology, vendors, choices, performance, toolsets and design flows for programmable logic. An overview of the architectural elements of RISC processors provides the required foundation for the comparison of current vendor SpC offerings. SpC design flows are presented along with common design challenges and potential solutions. The advantages, disadvantages, flexibility and performance of soft vs. hard processors is discussed. Analysis and system requirement prioritization is reviewed to help designers perform efficient trade-off evaluations of potential SpC implementations. This is the first class in a two-part series.

NEW! ETP-310 How to Streamline Embedded Systems Development with Eclipse

Jason Wilson and Steven Greffenius

Key Takeaways Learn how to integrate the tools required for MDA and deploy a simple embedded system from the Eclipse framework.

Introductory

Model Driven Architecture offers big gains for embedded systems developers, but the problem of integrating the tools required for MDA has not yielded a simple solution. Developers need a UML editor, a transformation engine, a compiler, and a code debugger. A model-level debugger and hardware simulators also aid the process. Eclipse, an open source framework, can solve some of these integration problems and streamline the development process. This class explains how Eclipse helps embedded systems developers with design, model transformation, debugging, and system deployment.

11:00 am – 12:30 pm

NEW! ETP-320 Designing Applications for Symmetric Multi-Processing Systems

Robert Craig and Sebastien Marineau-Mes

Key Takeaways An understanding of SMP hardware architectures, operating system support for SMP, and design of applications.

Intermediate

This class presents the design issues you face when porting an existing application to an SMP system or designing a new application to take advantage of SMP hardware. It covers hardware constraints, including bandwidth limits and I/O subsystem performance, with examples of how these constraints can be removed or minimized with specialized hardware elements. A discussion follows on how the operating system and applications can be architected to maximize performance on an SMP system. Specific examples of application re-architecting using optimization tools will be shown.

NEW! ETP-321 AVR Microcontroller for Control Application Developments

Joe-Ming Cheng

Key Takeaways Ability to formulate quick HW/SW prototyping solutions for sensing, motion control, lab automation, and equipment/instrument control.

Intermediate: Basic understanding of digital hardware interface, ADC/DAC, real-time timer/counter, and RISC architecture/instruction set required.

Typical AVR microcontroller applications are sensing, motion control, lab automation, and equipment/instrument controls. Mechanical systems typically have less than 10-khz bandwidth. AVR microcontrollers, clocking at 4 to 16 MHz, can facilitate fairly extended and robust real-time control for these systems. This class presents an overview of an AVR-based application prototyping and development environment and process. It then describes the AVR architecture, instruction set, C and assembly coding introduction. The class covers simulation and hardware emulation, with examples.

UPDATED! ETP-322 Understanding Compilers and Optimizations for Embedded Systems

Robert Oshana

Key Takeaways Various techniques used to improve embedded application performance using a combination of tools, algorithms, and architectures.

Introductory: Basic understanding of software build tools required.

Embedded systems are increasingly being programmed in higher level languages like C/C++ and Java. The benefits include portability, maintainability and productivity, but there can also be drawbacks. It is useful to understand how a high level language program is translated into instructions and when you cannot rely on the compiler! This class overviews the compilation process, discusses some basic compiler optimization techniques that can help you meet your performance goals, and reviews some of the more advanced techniques that allow you to perform more global or program level optimizations.

NEW! ETP-323 Wireless Embedded Networks: Connectivity for Everyday Objects

Robert Poor

Key Takeaways Embedded network architectures and how they differ from conventional wireless LAN systems, including the benefits gained by a self-organizing, self-healing mesh architecture.

Intermediate

The ever-decreasing cost and increasing performance of silicon Radio Frequency Integrated Circuits (RFICs) makes it practical to manufacture wireless communication capabilities into everyday goods. With the addition of appropriate control software, simple RFICs can become store-and-forward nodes in device networks, giving rise to a new category of wireless embedded networking, to add sensing and control to everyday devices. This class covers the technology that makes wireless embedded networks possible, and how it will help drive the RFIC market in the future.

UPDATED! ETP-324 Web Services in Embedded Systems

John Canosa

Key Takeaways An understanding of what Web Services are, and how they can be implemented in systems ranging from 8-bit to 32-bit.

Introductory

Web Services are key to the harnessing of the power of Internet connected embedded devices. They are the preferred method of calling remote procedures and enabling distributed computing for both embedded and business systems. This class provides an introduction to Web Services—what they are, the standards behind them (XML, SOAP, WSDL and UDDI) and their advantages and disadvantages for the embedded world. Some real world examples of Web Services are discussed.

UPDATED! ETP-325 C and C++ Gotchas, Part 2

Dan Saks

This is the second class in a two-part series. Please see class ETP-305 for abstract.

NEW! ETP-326 Modeling and Simulation Using UML, Part 1

Raetta Towers

Key Takeaways A preview of the anticipated OMG standard on System UML and how the standard relates to executable UML.

Intermediate: Knowledge of UML and simulation concepts required.

As programming languages turn into modeling languages, projects are being able to model systems at a high enough level of absraction that allows for architecture validation using simulation. The ability to perform architecture validation and simulation is key to the success of current large programs that tend to span across multiple sites and companies. Standards such as the OMG's UML 2.0 and SysML are enabling technologies that allow organizations to effectively deploy simulation stratigies that bridge across system and software teams. This is the same technology allows for team in differnt companies or locations to use a standard notation and delay implementation decisions until later in the program. An understanding of how to generate production level software from the same models that the systems engineers use for architecture, validation, and simulation. This is the first class in a two-part series.

UPDATED! ETP-327 The Ten Secrets of Debugging Embedded Systems

Lori Fraleigh

Key Takeaways How to identify and test for ten common issues in embedded and real-time systems such as memory leaks, performance bottlenecks, and API misuse.

Intermediate: Knowledge of C or C++ required.

Developers of embedded software face unique challenges, including devices that must run for months without crashing, extreme reliability, and limited memory and processing power. To build cost-effective systems, embedded programmers must squeeze performance and find errors before they reach the field. From seeking the needles in the haystack to understanding where CPU cycles are truly wasted, this class will summarize years of experience with thousands of real-world systems into ten simple rules for building better real-time software.

NEW! ETP-328 Networking Technologies for Low-Level Embedded Systems

Ted Schleich

Key Takeaways How to evaluate networking technologies for inclusion into low-level embedded systems.

Intermediate

There are a very large number of networking technologies suitable for networking embedded systems. The focus of this class is to narrow down the choices by examining five networking technologies (serial, Bluetooth, LonWorks, Ethernet, and wireless Ethernet) relative to low-level embedded systems. The class presents overviews, definitions, evaluation metrics, networking technologies, and conclusions.

NEW! ETP-329 Designing with Soft Processor Cores in FPGAs, Part 2

RC Cofer and Ben Harding

This is the second class in a two-part series. Please see class ETP-309 for abstract.

ETP-330 Really Real-Time Systems

Jack Ganssle

Key Takeaways Structuring code to meet performance requirements.

Intermediate: Any assembly language and C required.

Most smaller embedded systems meet their real-time requirements only by luck. We have few techniques that help us design a system that will be timely and predictable. This class shares practical (no UML, no academic proofs) ways to include time in your design, to help you produce a system that meets its deadlines, rather than beating a slow system into submission late in the debug stage. We examine the real speeds of common C constructs on various 8- and 16-bit CPUs, as well as faster alternatives to some compiler-supplied library routines.

"The Embedded Systems Conference San Francisco provides an excellent variety of topics presented in tutorials/classes. Lots to choose from."

Mel King
Senior Systems Engineer
Scientific Research Corporation

2:00 pm – 3:30 pm

NEW! ETP-340 Introduction to Distributed Embedded Systems

Bruce Emaus

Key Takeaways Technical fundamentals and related business aspects that surround the development of a distributed embedded system.

Introductory

This class introduces the basic technical (and a few business) concepts behind developing a distributed embedded system in contrast to the typical centralized or single processor approach. The primary focus is at the architectural or product application level with an emphasis on the distributed function, partitioning, transfer dialogs, and the choice of communication protocol. Many real world examples in the automotive electronics industry are shown. The class also examines the business aspects of "going distributed," the basic process of developing a distributed product, and the importance of systems engineering.

NEW! ETP-341 Case Example: Implementing DSPs in Biometric Systems

Ram Sathappan

Key Takeaways How to maximize the capabilities of a DSP for image enhancement and minimize power consumption without sacrificing performance.

Introductory: Basic understanding of DSPs, semiconductors and Biometrics market a plus.

This class discusses the design decisions behind the development of a self-contained fingerprint-authentication device based on a digital signal processor. The discussion evaluates the selection of an appropriate processor and sensor, as well as the necessary verification software.

NEW! ETP-342 Production Code Generation

Tom Erkkinen

Key Takeaways How to design, implement, and deploy embedded systems using a modeling environment and automatic code generation.

Introductory

With production code generation, code is automatically generated from executable models and deployed in embedded system products. Automotive and aerospace companies are quickly incorporating production code generation into their mainstream development processes for embedded control systems. Other industries and applications are assessing if production code generation is suitable for them. This class introduces model-based design and production code generation with emphasis on best practices and lessons learned from industry adopters. Topics detailed include code efficiency optimizations, data management, style guidelines, software integration, and verification and validation.

NEW! ETP-343 FPGA Design for Firmware Engineers, Part 1

RC Cofer and Ben Harding

Key Takeaways The required foundation for designing with FPGAs, from evaluating and selecting an FPGA manufacturer to understanding the software tools.

Introductory

Many of today's fast turn embedded projects can benefit from the flexibility of FPGA technology. FPGA design flows are evolving and are increasingly similar to traditional software development flows. Hardware Description Languages (HDLs) are being used in place of schematic capture to define, simulate and verify design functionality. This class details an HDL-based FPGA design flow to engineers without an extensive hardware background. It presents an overview of FPGA technology and covers design decisions, including evaluation and selection of FPGA supplier, family, package and component. This is the first class in a two-part series.

NEW! ETP-344 Measurement and Improvement of Processor Utilization in a Real-Time Application

Vitaliy Slobotskoy

Key Takeaways How to accurately measure processor utilization for each task or thread and how to use the maximum available amount of CPU cycles for actual data processing.

Intermediate

Accurate measurement of processor utilization for each task can be critical for successful development of a complex network application. This class gives an overview of available profilers (commercially available and under GPL) and presents a convenient method for benchmarking, which includes program source code markup and post-execution analysis, and which does not involve an external profiler. This method is especially convenient when software simulator is available for the platform. A few coding tricks are shown that allow to decrease processor utilization and make more processor cycles available for increased robustness or enhanced functionality.

UPDATED! ETP-345 Representing and Manipulating Hardware in Standard C and C++

Dan Saks

Key Takeaways How to write data declarations that accurately model hardware registers, and using the const and volatile qualifiers to improve the correctness and efficiency of device drivers.

Intermediate: C and some C++ programming experience required.

In addition to being used to develop highly portable applications, C and C++ can be used to write hardware-specific code. This class examines the features of standard C and C++ that can be used to represent hardware as data structures. It describes the common idioms for controlling typical devices, focusing on what can be done using only standard language features. It suggests platform-specific extensions that may be needed to complete the job. It also explores techniques for packaging hardware as abstractions.

NEW! ETP-346 Modeling and Simulation Using UML, Part 2

Raetta Towers

This is the second class in a two-part series. Please see class ETP-326 for abstract.

ETP-347 **Slow Process Control: A Modeling/Simulation Approach**

Ugo Ruggeri

Key Takeaways How to speed up the design and tune process and prediction of the behavior of the controlled process before having a controller prototype.

Advanced: System control theory and matrix algebra required.

Running a numeric simulation on a process model may accelerate the tuning of slow control systems: computer simulations with different controller architectures and/or with different parameters can be easily and quickly performed. Another advantage is the ability to predict the behavior of the controlled process before having a controller prototype to tune and test. This class provides some generalities on system modeling and model identification, and then focuses on a model structure especially suitable for the digital control of single-input/single-output linear systems. An identification algorithm is detailed.

UPDATED! ETP-348 **Embedding SSL: Internet Security for 8-bit Systems**

Timothy Stapko

Key Takeaways Attendees will learn about cryptography as it applies to SSL, the basics of the SSL protocol and the issues involved in implementing SSL for embedded systems.

Intermediate: Understanding of network programming and TCP/IP, and the role of network security in embedded systems required.

This class discusses the basics of SSL and Transport Layer Security (TLS, the IETF standard for SSL) and the problems inherent in constructing an SSL implementation for a system with limited resources, including processing requirements for encryption, digital certificate management, memory management issues, and seamless API integration with existing networking protocols. Real-world issues are illustrated by covering a working implementation of an SSL server for the Rabbit microprocessor.

NEW! ETP-349 **Pervasive Computing Applications and Wireless Sensor Networks**

Dave Stewart

Key Takeaways The many trade-offs that need to be considered when putting together a wireless sensor network or a pervasive computing application.

Introductory

A new generation of applications that consist of dozens to thousands of tiny processing units is emerging, called pervasive computing. Potential applications include machine health and diagnostics, physiological monitoring, environmental monitoring, asset and inventory management, smart agriculture, and many more. The key enabling technology for these applications is the advent wireless sensor networks that merge ultra-low-power communication with miniaturization of sensors and actuators. In this class both the benefits and the many new challenges for embedded system engineers are discussed.

ETP-350 **Learning from Disaster**

Jack Ganssle

Key Takeaways Attendees will learn the most common mistakes that lead to product failures in the field.

Intermediate

Civil engineers have learned how to avoid failure from their rich history of bridge collapses, tunnel floodings, and building disintegrations. The firmware world is quite different; it seems we all make the same mistakes, repeatedly. Yet most problems have similar root causes. In this class a number of embedded disasters are examined, large and small, and lessons we must learn to improve our code are extracted.

"The Embedded Systems Conference San Francisco gave me the opportunity to hear from experienced embedded designers on various subjects that pertain to projects that I am working on. The different points of view and ideas provided me with new avenues for further study."

Scott Wheeler
Senior Staff Electronics Engineering
Lockheed Martin

3:45 pm – 5:15 pm

ETP-360 Verification and Validation for Embedded Software

Charles Knutson

Key Takeaways The fundamental principles of verification and validation and the positive role they can play in the creation of high quality software systems.

Introductory: Understanding of software development and quality issues required.

Building quality into software during development is far more effective than trying to test it in after it's been built. Verification and validation techniques can be applied throughout the process lifecycle to help assure that the right product is being built, and the product is being built right. This class introduces the fundamental theory and techniques of verification and validation and discusses how these techniques have been successfully applied in the creation of high-quality embedded software.

NEW! ETP-361 Rapidly Assessing Alternative Execution Topologies via MDA

Peter Fontana

Key Takeaways Optimization of run-time performance through the specification of and rapid deployment to multiple execution topology alternatives.

Intermediate: Familiarity with developing and assessing embedded software architecture alternatives required.

To achieve system execution performance goals, initial implementation architectures often need to be reworked and new execution topologies tried to find the optimal deployment allocation. With rising system feature complexity combining with sophisticated multitask and multiprocessor execution topologies, specific architectural allocation techniques and automation are required to facilitate this effort. This class introduces and outlines key aspects of the Model Driven Architecture (MDA) approach that directly support the specification of multiple alternative execution topologies, and the rapid deployment of MDA systems to these implementation alternatives.

NEW! ETP-362 Programming Frameworks for Embedded Multimedia Applications

David Katz, Rick Gentile, and Tomasz Lukasiak

Key Takeaways Different multimedia system frameworks and strategies for partitioning processor resources in single-core and dual-core media processors.

Intermediate: Basic understanding of embedded processor architectures required, emphasizing memory and DMA subsystems.

With the availability of high-performance embedded media processors, software engineers must port media-based algorithms from the PC environment to a realm where memory size and data bandwidth are important considerations. This class discusses programming frameworks that allow software developers to achieve the highest performance for a given application without increasing the complexity of the programming model. It also presents strategies for partitioning processor resources in single-core and dual-core media processors.

NEW! ETP-363 FPGA Design for Firmware Engineers, Part 2

RC Cofer and Ben Harding

This is the second class in a two-part series. Please see class ETP-343 for abstract.

NEW! ETP-364 Guidelines for Writing Portable Code

Greg Davis

Key Takeaways How to write portable C or C++ code.

Intermediate: Basic knowledge of C required.

Today's fastest, lowest power processor may be outdated tomorrow, leaving the developer locked into obsolete technology, unable to move to a new processor. Writing portable code can help minimize the risk by making the migration to newer processor or software technology as painless as possible. This class focuses on coding guidelines that take nothing for granted, leaving the programmer with a portable code base, ensuring access to the latest technology.

UPDATED! ETP-365 Writing ISRs in C++

Dan Saks

Key Takeaways How to implement an ISR framework in C++ and evaluate tradeoffs between performance and flexibility, particularly regarding choices between static and dynamic binding.

Intermediate: Basic knowledge of writing device drivers in C++ required.

Writing hardware interrupt service routines (ISRs) entirely in Standard C++ is practically impossible. ISR calling conventions rarely, if ever, match normal C++ function calling conventions. When writing ISRs in C++, you must either dip into assembly language or use platform-specific language extensions. (Standard C is equally inadequate for writing ISRs.) This class shows you how to write much (just not all) of your ISR code in Standard C++. Attendees learn to use language linkage (e.g., extern "C") when interfacing C++ with hardware resources and assembly language code.

NEW! ETP-366 Building and Implementing Concurrent Specifications

Stephen J. Mellor

Key Takeaways How to express requirements so they can be mapped easily to a multi-tasking/multi-threaded RTOS.

Introductory

Many requirements documents are described in a linear manner, which makes for "interesting times" when the system is highly concurrent and multi-threaded. Any attempt to take concurrency and distribution into account when expressing requirements can easily lead to premature design and difficulties in retargeting the application to a different environment. This class describes an approach to capturing concurrency in requirements as models and providing rules to sequentialize and sequence them in an implementation on an RTOS.

NEW! ETP-367 FPGA Embedded Processors: Revealing True System Performance

Bryan Fletcher

Key Takeaways Advantages and disadvantages of designing with an FPGA embedded processor; specifically, the tradeoffs between cost, memory architecture, peripheral set, and performance.

Intermediate

This class investigates the performance and cost trade-offs for several FPGA embedded processor systems and gives an overview of the available peripherals and memory controllers. Several case studies examine the effects of various embedded processor memory structures and peripheral sets. The results from these case studies are used to draw conclusions regarding the performance and cost penalty incurred by using specific peripherals and memory architectures. After this class, attendees will understand how to interpret the manufacturers published benchmarks and how that translates into an actual system design.

NEW! ETP-368 **Power Optimization Techniques for Embedded Systems Programmers**

Robert Oshana

Key Takeaways Practical power optimization techniques the process to follow when developing power efficient applications.

Introductory: Basic understanding of processor architectures and a high level programming language such as C/C++ required.

Relatively little emphasis has been placed on power optimization techniques that can be applied to embedded system applications. This class provides an overview of basic static and dynamic power optimization techniques that can be used to reduce power consumption in portable embedded applications. The power optimization process is discussed to show how to select the right device, how to build an application to optimize power consumption, and how to measure and optimize for power after the application is built.

NEW! ETP-369 **Using ZigBee Technology for Low Power Device Designs**

Jon Adams

Key Takeaways How to utilize the ZigBee protocol and other enabling technologies to design mobile devices.

Intermediate

ZigBee is a standards-based, low cost, low power technology that will enable the broad-based deployment of wireless networks in home, enterprise and industrial settings. The ZigBee protocol was designed to facilitate long-life battery applications. Devices can be powered either by battery or line, though ZigBee has always highlighted its battery-powered capabilities. This class describes the ZigBee specification and tells how to integrate ZigBee technology into various mobile device designs for low power functionality.

NEW! ETP-370 **CANopen-Based Transducer Network**

Cyrilla Jane Menon

Key Takeaways How to build simple and cascaded embedded networks, depending on the requirements, as proposed by IEEE 1451.

Introductory

In order to reduce the integration effort that is necessary especially in sensor-intensive applications, the CAN in Automation (CiA) international users' and manufacturers' group has developed a CANopen device profile (DS 404) for transducers and closed-loop controllers that can be used to describe multi-sensor devices. Using this profile, the system designer can design cascaded networks. The multi-channel CANopen transducer module may use embedded communication links as defined in IEEE 1451. The CANopen devices provide compatibility to the Transducer Electronic Data Sheet (TEDS) as defined in IEEE 1451.

"The classes this year were excellent. Very on-topic, very apropos to today's design decisions.

I loved the coverage of UML and software project management instead of just classes on today's hot new CPU/bus/components."

David Poole
Sr. Software Engineer
Mobility

8:30 am – 10:00 am

NEW! ETP-400 Multiprocessing in Embedded Systems

Tracy Thomas

Key Takeaways Basic multiprocessing concepts to use when deciding whether to implement a multiprocessing system for a project.

Introductory: Familiarity with C useful.

Embedded systems are constantly demanding more of the CPUs within them, and one way to efficiently design complex systems is by utilizing multiple CPU cores. This class provides an introduction to multiprocessing topics and covers both hardware and software requirements, with an emphasis on software development. Topics include different models of parallel programming, communication, synchronization, and a discussion of what is required of software engineers to utilize a multiprocessor system. The class also provides a survey of some currently available technologies.

NEW! ETP-401 Model Driven Development of Resource Constrained Embedded Applications

Ton Janssen

Key Takeaways UML for modeling resource constrained embedded systems, and how to minimize resource demands of the system under development while still using a model driven approach.

Intermediate: Programming experience in C required, UML experience a plus.

Many embedded systems are constrained in the amount of memory and computational processing power available. The use of models to generate embedded applications requires thoughtful attention to these constraints. This class investigates the use of the Unified Modeling Language (UML) modeling tools for the generation of resource constrained applications. A small case study of an embedded system is used. Trade-offs in using high-level abstractions such as active objects are investigated. Productivity and quality gains from using models for embedded development are discussed.

ETP-402 Fundamentals of Digital Imaging, Part 1

John Canosa

Key Takeaways An understanding of digital imaging devices, how to interact with image capture and output components, and the basics of optimizing image processing.

Introductory

Digital imaging knowledge is important for devices with graphical displays and hard copy output capability. This class explores the fundamentals from capture to image processing through output. Topics covered include CCD/CMOS sensor interfacing, basic image processing, color spaces, and working with output devices such as display controllers and printers. Attendees will be able to answer the age old question "Why does it look so good on my screen and so bad when I print it out?" This is the first class in a two-part series.

NEW! ETP-403 The Perils of FPGA Timing Closure

Carl Christensen

Key Takeaways Achieve timing closing by studying various techniques used on three large FPGA designs.

Intermediate: Understanding of digital hardware design including hardware description languages, knowledge of FPGA features and architecture, and exposure to FPGA tool flows required.

Looking into the struggles to get large designs to closure can provide valuable insight to others using large FPGAs. This class describes a project involving three large FPGA designs, two in Xilinx V2 3000 parts, and one in a Xilinx V2 Pro 50, in which timing closure was not expected to be a problem. But it was. Techniques to be examined include area constraints, synthesis options, physical synthesis, par switches, "secret" par switches, and hierarchical floor planning.

NEW! ETP-404 Selecting Linux as an Embedded Operating System

Paul Knot

Key Takeaways How to evaluate whether Linux might be a suitable operating system to use in a future product.

Introductory

There are significant tradeoffs to be made when selecting a suitable OS for any particular device. This class looks at the considerations when evaluating Linux as an embedded operating system, and shares some insights gained on a real project, during which, the promise of being able to use completely free, mainly open-source software and development tools was put to the test with a good measure of success. Attendees learn the issues associated with using Linux and other open source software in an embedded system.

NEW! ETP-405 C++: Inheritance, Interfaces and Thunks

Niall Cooling

Key Takeaways The memory and performance impact of using C++ multiple inheritance in an embedded system, the need for "thunks," and how to minimize overheads.

Advanced

Since its standardization in 1998, C++ has grown as a plausable alternative to C as an embedded programming langauge. To date, many programmers have not used C++ Multiple Inhertiance (MI) because it is not supported (e.g. Embedded C++) or because of concerns over the performance impact. However, with the acceptance of UML 2.0, the concept of multiple interfaces will play a much greater roll in design, thus forcing the use of MI. This class looks at the real impact of using MI in an embedded design.

UPDATED! ETP-406 **Practical Statecharts for Embedded Systems, Part 1**

Miro Samek

Key Takeaways How to apply statecharts to construct more robust and maintainable event-driven software and how to practically code statecharts in C or C++.

Intermediate: Fluency in C required, familiarity with inheritance in C++ a plus. Part 2 requires general understanding of preemptive multitasking, mutual exclusion, and blocking.

This class shows practical ways to use UML statecharts in designs, to help produce efficient and maintainable systems with well-understood behavior, rather than creating "spaghetti" code littered with convoluted ifs and elses. Part 1 presents the essence of statecharts, why are they fundamental, and how to practically code them directly in C or C++ without sophisticated CASE tools. Part 2 shows how to combine concurrent state machines into applications, presents a lightweight, portable event-driven framework for real-time embedded systems, and teaches how to build and use a minimal statechart-based application framework. This is the first class in a two-part series.

UPDATED! ETP-407 **Extreme Programming and Embedded Software Development**

Robert Martin

Key Takeaways How extreme programming and agile development can improve how you specify and develop software.

Introductory

Extreme Programming (XP) made its debut in 1999. The topic is still a hot bed of discussion; much of that discussion is mired in rumor and misinformation. XP is an Agile software development methodology, iterative at its core and reducing development process overhead. This class explores the efficient and effective practices of XP and how to use it to develop embedded software. A team using XP makes concrete progress in embedded software development early in the development cycle, even prior to hardware availability.

NEW! ETP-408 **Meeting RTCA/DO-178B/12B and ARINC 653 Safety Requirements for Critical Systems**

Joe Wlad

Key Takeaways Five levels of software defined by DO-178B, data documents required by DO-178B, and the requirements for an operating system to meet reusable software components approval.

Advanced: Familiarity with DO-178B and ARINC 653 standards helpful but not required.

This class reviews the DO-178B guidelines for software in airborne systems and equipment and discusses how equipment makers can bypass the labor-intensive certification process with commercial-off-the-shelf (COTS) solutions that use the standard ARINC 653 interface platform. It examines the typical architecture of a federated avionics system, analyzes the ARINC layer, and explains the advantages of integrated modular avionics (IMA). The class proposes a platform for software certification reuse that provides comprehensive software vulnerability analysis, is ARINC compliant and meets DO-178B certification evidence requirements.

NEW! ETP-409 **Hardware As Software: Designing with Configurable Processors**

Albert Wang

Key Takeaways Configurable architectures and the impact this technology will have in future processor development.

Intermediate: Familiarity with C and Assembly a plus.

This class examines configurable architectures which marry the flexibility of software programmability with the performance capabilities of ASIC designs in applications where SoC and ASIC design are economically infeasible and general purpose software processors can't meet minimum performance requirements. Software-configurable architectures blur the distinction between hardware and software. Key topics to be discussed include hardware/software partitioning issues, abstracting hardware as software, definition and use of custom instructions, designing for parallelism, dynamic adaptation to computational hotspots, and the management and optimization of simultaneous hardware/software design.

NEW! ETP-410 **Establishing Great Software Development Process(es) for Your Organization**

Dale Mayes

Key Takeaways The elements that comprise a very formal software process and the ability to wisely select the pieces that are pertinent to your project.

Introductory

There are many correlations between good software designs and good software development processes. It takes multiple views to adequately describe both software architectures and software development processes. One of the process views this class examines is a swim lane chart. This view highlights another parallel; good software designs limit the number of dependencies and interaction points between modules. The class introduces the traditional waterfall, incremental and iterative development models. A quick overview of a classic formal process (DoD-2167a) establishes a common reference for what artifacts are typically created under a formal process and touches on other factors that add to a project's complexity.

> "I liked the offerings/topics, the expertise, and professional experience that the speakers displayed and expressed during the presentations."
>
> Nick Olivas
> Electronics Technician
> LANL

11:15 am – 12:45 pm

ETP-420 Real-Time Architectures: Past, Present, and Future, Part 1
Doug Locke and Mark Gerhardt

Key Takeaways Fundamental real-time architecture styles, and the impact of using object-oriented architectures in embedded real-time systems.

Introductory

The architecture of response-time critical embedded systems is usually chosen early in the system's lifecycle. There are only four fundamental real-time architectural styles, each having its strengths and weaknesses. It is now known that a set of fundamental real-time architectural principles exists that govern these styles, and that can be exploited to successfully navigate this minefield throughout the system lifecycle. This class illustrates these four fundamental architectures, describes their strengths and weaknesses, and deals with the fundamental architectural concepts that could have strengthened them. This is the first class in a two-part series.

NEW! ETP-421 Real-Time Programming in Java
Steve Furr

Key Takeaways How to take advantage of the Real-Time Specification for Java.

Intermediate: Experience writing application software in Java required.

By using the Real-time Specification for Java (RTSJ), developers can eliminate unpredictable latencies introduced by the garbage collector, exercise full control over thread priorities, and handle asynchronous events with ease. This class identifies the drawbacks of deploying conventional Java in a real-time system and how the RTSJ solves them. Using working code examples, we explore all the new classes that a Java Virtual Machine (JVM) supporting the RTSJ must provide. The class also examines how real-time behavior can be achieved via the Java Native Interface (JNI).

ETP-422 Fundamentals of Digital Imaging, Part 2
John Canosa

This is the second class in a two-part series. Please see class ETP-402 for abstract.

UPDATED! ETP-423 Hardware/Software Codesign for Platform FPGAs
Don Davis

Key Takeaways How to develop platform FPGAs using a high-level software-centric flow.

Introductory

System-on-a-chip FPGAs including embedded processors, busses, memory, and hardware accelerators provide an opportunity to develop high performance, optimal systems. To realize the promise of this vision, a complete tool chain from concept to implementation is required. An automated design framework is described that allows development of hardware/software platform FPGA systems starting with a pure C design specification. Profiling, verification and advanced compilation technologies, including an optimized C to hardware compiler, provide a full push-button implementation flow.

NEW! ETP-424 Bringing up a Custom Linux BSP
Michael Anderson

Key Takeaways Knowledge of the Linux boot sequence and the role of boot firmware.

Intermediate: Fluency in C required, understanding of CPU initialization techniques and make file syntax recommended.

Typical Linux makes extensive use of hardware MMUs and hardware services that were used only sparingly in legacy RTOS environments. In addition, Linux does not provide for boot firmware as part of the standard distribution. This class outlines the requirements for boot firmware interaction with the BSP as well as the steps required to get your board ready to start the Linux kernel. Strategies for building the BSP, placement of BSP-specific files, and the integration of that custom BSP into the Linux kernel sources are presented.

NEW! ETP-425 High Assurance Java for Mission-Critical Systems, Part 1
Kelvin Nilsen

Key Takeaways Create architectures using the safety-critical specification for Java, and combine safety-critical components with traditional Java components in high assurance mission-critical systems.

Intermediate

The safety-critical specification for Java (SCSJ) is designed to provide the high performance, small memory footprint, hard real-time determinism, and simplicity required for the development of DO-178B certified software in commercial and military avionics applications. Many of the special capabilities of the SCSJ are also well suited to development of high-assurance mission-critical software. This includes device drivers; interfaces to legacy software components written in C, C++, and Ada; and any software components that have demanding performance, footprint, or hard real-time determinism constraints. This is the first class in a two-part series.

UPDATED! ETP-426 Practical Statecharts for Embedded Systems, Part 2
Miro Samek

This is the second class in a two-part series. Please see class ETP-406 for abstract.

NEW! ETP-427 Debugging Embedded Linux Systems
Darcy Wronkiewicz

Key Takeaways Techniques for debugging multi-threaded embedded Linux applications, the Linux kernel, and device drivers.

Intermediate

Despite their limitations, the simple flat-memory models of legacy home grown and commercial embedded operating systems are usually easy to debug. Debugging an embedded Linux system, where MMU translations are enabled and context switches across user modes are permitted at any time, requires new methods. This class discusses the challenges of debugging multi-threaded embedded Linux applications as well as the Linux kernel and device drivers. Techniques for debugging individual threads, processes, loadable kernel modules, and new hardware are presented.

NEW! ETP-428 Safety-Relevant Communication in Embedded Control Systems

Cyrilla Jane Menon

Key Takeaways How to realize safety-relevant communication on top of non-safety-relevant bus systems like CAN and CANopen.

Intermediate: Understanding of digital hardware design required. General understanding of CAN networks a plus.

The class introduces the CANopen Safety Protocol (CiA DS 304) and discusses the concept of serial redundancy transmitting safety-relevant data in two continuous messages with bit-wise inverted content. It also describes several implementation possibilities including a single-processor implementation done by a consortium of device manufacturers and system designers as well as configuration possibilities and restrictions. Using the generic profiles (I/O, motion control, encoder, and hydraulics) and some specific application profiles (e.g. lift and door control) in conjunction with the CANopen Safety protocol is covered.

NEW! ETP-429 Integrating the Trusted Platform Module into Embedded Systems

Kevin Schutz

Key Takeaways Trusted Platform Module specification, capabilities for embedded systems, and integration.

Intermediate

This class introduces the Trusted Platform Module (TPM), its capabilities, the Message Communication protocol, RSA basics, and details the TPM Key Hierarchy. The class details a methodology that enables successful integration of the TPM into a design and provides the methodology for verifying the TPM's operation on a specific platform.

UPDATED! ETP-430 A Skills List for Developing Embedded Software

Dale Word

Key Takeaways Skills necessary to transition from traditional software development to embedded development.

Introductory

Developing software for embedded systems is inherently different than developing software for desktop or server environments. In this era of point-and-click, automated development, embedded development skills are becoming less common. This class helps traditionally trained software developers transition into embedded development, by giving an overview of the topics that they may need to spend time reviewing or learning. It provides a "study list" for engineers transitioning to the embedded realm, and also a "qualifications list" for managers looking to hire embedded developers.

"Presenters shared real life events that happened to them. One of my presenters even stayed after the class for a Q&A session."

Robert Huber
Software Engineer
Baker Hughes Inteq

2:00 pm – 3:30 pm

UPDATED! ETP-440 Real-Time Architectures: Past, Present, and Future, Part 2
Doug Locke and Mark Gerhardt

This is the second class in a two-part series. Please see class ETP-420 for abstract.

NEW! ETP-441 Measuring and Tuning Real-Time Performance of Embedded Systems
Russell Klein and Rajat Moona

Key Takeaways Techniques to measure and improve the overall real-time performance of embedded systems.

Intermediate: Familiarity with real-time hardware design issues helpful.

Embedded systems often have performance bottlenecks, which prevent them from meeting their performance requirements. This class explores techniques to profile the system and presents data that can be extracted from the profiles allowing designers to identify bottlenecks and modify the design. The class presents real life examples. One of the case studies will be low bit rate speech encoders. We walk our audience through several changes in the design and their impact. Finally we show the tuned design achieving much lower frequency, saving power and cost.

NEW! ETP-442 Software Defined Radio with Reconfigurable Hardware and Software
Peter Ryser

Key Takeaways Development process for hardware/software platform, including tools and target platforms.

Introductory

This class presents a step-by-step walk through of the implementation of a Software Defined Radio (SDR) system running on embedded Linux in a single FPGA. We discuss aspects of hardware and software partitioning between the FPGA fabric and the embedded processors as well as between the processors themselves and show the advantages of Software Defined Radio on reconfigurable computing systems over existing solutions. The result is a working SDR application using hardware, software, and a full embedded operating system.

NEW! ETP-443 Model-Based Design of Closed Loop Control for Embedded Systems Using Fixed Point Controllers
Arefeen Mohommad

Key Takeaways Achievement of system-level optimizations which can be difficult to realize using only C or HDL-based tools.

Intermediate

This class shows the application of Model-based design to the development of a closed-loop, real-time motor control application. The system was modeled as a block diagram; different pieces of the system are simulated to validate algorithms using 32-bit fixed-point operations. Automatic code generation was used to verify performance on a fixed point DSP controller. The algorithms are presented in detail, and the accuracy of 32-bit fixed-point operations is compared with 16-bit fixed point and floating-point operations. The comparison results show that proper 32-bit fixed-point operations provide excellent performance for any embedded system implementations.

NEW! ETP-444 Power Management Strategies in Embedded Applications, Part 1
Gordon Mortensen

Key Takeaways Understanding of low-power options and techniques to maximize portable designs.

Intermediate

Low-power techniques are increasingly important for portable embedded applications. This class introduces software and hardware approaches for aggressively managing the power budget. Implementation of a range of reduced-power modes between fully on and fully off is discussed, with reference to support for these modes in communication protocols and embedded controller silicon. This is the first class in a two-part series.

NEW! ETP-445 High Assurance Java for Mission-Critical Systems, Part 2
Kelvin Nilsen

This is the second class in a two-part series. Please see class ETP-425 for abstract.

NEW! ETP-446 Data Management for Highly Available Embedded Systems
Ali Paasimaa

Key Takeaways Selecting an appropriate database product, choosing between alternative high-availability database technologies, and the Service Availability Forum's AIS (Application Interface Specification.)

Intermediate

The class introduces the field of highly available databases (HA DBs). The required availability level of contemporary telecom systems is around "5 nines," that is 99.999% availability. A special challenge of HA DB systems is that the pure availability of the service is not sufficient—the integrity of the data has to be maintained over any failure scenario. An overview of commercially available architectures is given, together with guidelines to various trade-offs achieved with the technology. The criteria for and behavior of a HA DB compliant with the SA Forum's specifications is described.

NEW! ETP-447 Covering Multiple Embedded Networking Technologies with CANopen
Olaf Pfeiffer and Christian Keydel

Key Takeaways How CANopen can be used on multiple network technologies, including I2C, UART, LIN, CAN and Ethernet.

Intermediate: General knowledge about embedded networking required.

This class explains how embedded communication methods can share a common network protocol, providing a transparent network protocol covering several layers in an embedded networking system. The hardware layers unified by this method include UART, LIN, I2C, CAN and Ethernet. The general, shared CANopen functionality required for such a hardware-independent implementation is summarized in this class followed by a review of how this technology is adapted for the different hardware layers. The class ends with an overview of the general requirements that other physical layers must meet to be usable for CANopen.

NEW! ETP-448 Building Internet Applications with Microsoft's .NET Compact Framework

Robert Burdick

Key Takeaways Ability to create Internet-enabled applications for a variety of Windows CE devices and platforms using the Microsoft .NET Compact Framework.

Intermediate: Some experience with Windows or Windows CE application programming and C or C++ programming required. C# or vb.NET programming a plus.

This class describes the benefits of writing Internet-enabled mobile and wireless applications for Windows CE using the Microsoft .NET Compact Framework. The .NET Compact Framework and the tools available for building applications using the framework are explained. The Microsoft .NET Compact Framework is compared to the traditional Win32 approach to writing such applications for Windows CE. Attendees will be able to start writing their own web applications for platforms such as the Pocket PC and Smart Phone immediately.

NEW! ETP-449 Application Development for ZigBee Wireless Networking

Drew Gislason

Key Takeaways ZigBee basics, including the PHY and MAC layers, and the ZigBee stack.

Introductory

ZigBee addresses networking among devices with low-data rate exchange needs, such as lighting, HVAC, security, medical and other monitoring and control applications using sensors and actuators. This class covers the basics about the ZigBee wireless networking standard, including the various layers of the stack, and the application framework and profiles, which assure interoperability and form an application foundation. Considerations in writing a ZigBee application are discussed while examining C source code for a simple application. A ZigBee wireless network will demonstrate the application in use.

NEW! ETP-450 The Hardware/Software Co-design for Road Vehicle Control System

Ryuji Okamura

Key Takeaways System designers and software engineers will learn how to apply co-design to vehicle control system applications.

Intermediate

In vehicle control systems electric control unit (ECU) as software content grows, appropriate MCU loading becomes difficult to maintain. One path to successful development is to use co-design for the control system. In this class we focus on how to apply the co-design to the problem. We propose a co-design environment, applying high-level synthesis. By applying co-design to the engine ECU, we succeeded in transforming part of the software into custom hardware, thus reducing the load on the target MCU.

3:45 pm – 5:15 pm

ETP-460 Complementing DSPs with FPGAs

Paul Ekas

Key Takeaways Confidence in suggesting a DSP + FPGA solution when customers run into roadblocks using a DSP by itself.

Intermediate

A new generation of low-cost FPGAs can be used to resolve system-level challenges without significantly impacting overall system costs. These FPGAs can be used to implement peripherals, replace hard-to-find components, connect high-speed analog-to-digital and digital-to-analog converters, streamline data transfers, act as co-processors or fill any other gap between the end application and the system designer's DSP of choice. This class describes real-world situations where system-level challenges require a solution involving more than just a DSP. In each example, the benefits of partitioning the system between a DSP and an FPGA are detailed.

NEW! ETP-461 Scalable and Platform Agnostic Device Driver Architecture

Matthew Sottek

Key Takeaways Learn the importance of strong software engineering principles like modularity, reusability, and scalability.

Intermediate: Devide driver programming experience and fluency in C required. Graphics driver knowledge a plus.

As new operating systems and hardware platforms emerge, device driver development and validation becomes more demanding. Duplicate efforts appear in device drivers that support a combination of software/hardware platforms. Good modularization and layered functional abstraction practices help produce scalable and portable device drivers that reduce the maintenance costs while improving the adaptability for future OS and hardware platforms. This class discusses the pros and cons of a modular driver framework vs. a traditional device driver development model.

NEW! ETP-462 MCUs for Motor Control

John Pocs

Key Takeaways Basic MCU features and the implementations of various speed and torque control methods for more energy efficient appliances.

Intermediate: Basic understanding of microcontroller architecture and digital electronics required. Knowledge about motors and motor control a plus.

This class introduces 3-phase electric motor basics and describes the various speed and torque control methods used to tackle the need for fast and precise motor response. Special peripherals such as 6-phase PWM timers, synchronized fast ADC, encoder timers and high performance CPUs with programmer friendly architectures are key features for modern motor-control MCUs. They can greatly reduce the software overhead and allow real-time processing of sensor signals, as well as the implementation of sophisticated control algorithms, yet leave enough room for other system tasks such as managing communication or human interface.

NEW! ETP-463 Integrating DSP Design and Test for Rapid Product Development

Mike Trimborn

Key Takeaways Decrease time to market by testing software and hardware earlier in the design process.

Intermediate

Due to the complexity and variety of DSP applications, testing DSP algorithms with various parameters can be challenging. LabVIEW graphical development provides a rapid platform to develop, debug, and test applications through RTDX. Furthermore, the LabVIEW DSP Test Integration toolkit provides a plug-in to the Texas Instruments Code Composer Studio IDE to debug DSP algorithms without needing to program. This class walks through how companies in automotive and aerospace are using LabVIEW and Code Composer Studio to reduce the development time for their audio, video, and control applications.

NEW! ETP-464 Power Management Strategies in Embedded Applications, Part 2

Gordon Mortensen

This is the second class in a two-part series. Please see class ETP-444 for abstract.

UPDATED! ETP-465 Secure Safety-Critical Distributed Embedded Systems

Bill Beckwith, Joseph Jacob, and Mark Vanfleet

Key Takeaways The architecture of MILS systems and the design goals behind MILS, MILS Middleware and MILS Systems.

Intermediate: Working understanding of computer systems required.

To address the need for security in embedded and real-time systems, an architecture based on a small separation, or partitioning, kernel has been proposed termed the MILS (Multiple Independent Levels of Security). The architecture classifies the components of a system into three layers; the partitioning kernel, the middleware, and the application layer. The class discusses the MILS architecture, its impact upon current and future embedded system development, and the certification process.

ETP-466 Introduction to the PowerPC Programming Model

Paul Gramann

Key Takeaways PowerPC architecture from a programming perspective, along with its components and instructions.

Intermediate: Some assembler or C programming experience required.

As CISC programmers transition from legacy processors to RISC architectures such as the PowerPC, they are faced with a steep learning curve. This class presents an overview of the PowerPC programming model for engineers and programmers who are new to the PowerPC architecture. The class discusses the PowerPC storage model, registers, instruction types and formats, memory management, interrupt handling, debug facilities, and provides suggestions for maintaining code compatibility across different PowerPC implementations.

NEW! ETP-467 Emerging Landscape of High Speed Serial Interconnect Standards

Harpinder Matharu

Key Takeaways Technological strengths and weaknesses of the high speed interconnect standards.

Introductory

To alleviate the problems of high cost, long lead times, and lack of interoperability of proprietary high speed interconnects, several industry forums have sprung up to unleash new serial high speed interconnect standards and protocols. The contenders include: Serial Rapid IO, PCI Express, Advanced Switching (an extension of PCI Express), and Backplane Ethernet. Latencies, congestion management, quality of service, redundancy, and high availability are some of the features that will play decisive roles in this competition. This class discusses and compares the strengths and weaknesses of the underlying technology and ecosystem of the competing high speed interconnect standards to understand their future prospects.

NEW! ETP-468 Bridging Embedded Network Technologies

Axel Wolf

Key Takeaways What to pay attention to when using a single microcontroller to bridge multiple communication networks including I2C, UART, LIN, CAN and others.

Intermediate: General knowledge about embedded networking and/or CANbus required.

This class summarizes common communication methods used and focuses on the requirements for a bridge application, where multiple communication methods and layers come together in a single chip. The different network layers typically used in embedded applications are summarized and evaluated. Network technologies covered include I2C, UART, LIN, CAN and Ethernet. The evaluation also includes a comparison of regular implementations versus smart implementation of these technologies. Using a Philips LPC2000 ARM7TDMI microcontroller, a real-world bridge example is demonstrated.

NEW! ETP-469 The Joy of Real-Time Artificial Intelligence

Mikel Cvetanovic

Key Takeaways Understanding the problems inherent in combining AI and real-time systems.

Introductory

Combining real-time systems with AI is like combining chocolate ice cream with onions. They just doesn't mix well together. The purpose of this class is to explore the problems of applying AI techniques to real-time systems, or, applying real-time requirements to AI systems. A historical perspective will be given which will carry through to the present to show the evolution of real-time AI systems. Real-world examples will be given.

NEW! ETP-470 Safety Critical Software Verification: Lessons From the DO-178B Approach

Nat Hillary

Key Takeaways Improve software quality by studying code quality standards and guidelines used by the FAA to certify safety critical avionics systems.

Intermediate: C, C++ or Ada programming experience required, software test experience a plus.

Published by Requirements and Technical Concepts for Aviation Inc., the DO-178B Software Considerations in Airborne Systems and Equipment Certification document offers guidelines that are unique relative to other quality processes, because they state that the verification activities used for a given system should be determined by how safety critical the system is. This class looks at what is meant by the term "software quality," and then reviews validation and verification activities. Finally, we describe three powerful software verification lessons and a golden rule that you can start implementing today.

NEW! ONE-AND-TWO DAY DESIGN FOCUSED SEMINARS

Attend one seminar or choose from multiple programs to build your own custom program with the ePass, see page 48 for all pass options.

Analog and Power
design seminar

March 7, 2005

This program explains the use of analog components such as amplifiers, data converters, power management devices, and high-speed interface components. It provides insight into the role played by analog, mixed-signal and power technology in a world increasingly dominated by digital engineering.

Key Takeaways

- Understanding some of the tradeoffs that need to be considered in providing power to the newest embedded systems
- Grasping the differing requirements for popular data converter applications such as audio, video, radio communications and controls
- Meeting the experts on amplification and sensor signal conditioning techniques

Program Chair:
Stephan Ohr

Editorial Director, Analog and DSP; Editor-in-Chief, *Planet Analog*
CMP Media LLC

DSP Performance
design seminar

March 7, 2005

This program updates designers on DSP architectural trends and software design issues. Speakers here link DSP concepts like precision, clock rates, and code space to the specific requirements of next-generation high-speed data communications, wireless signal processing and consumer electronic systems.

Key Takeaways

- Understanding the differences between microprocessors and DSPs, as well as the DSP architectures that enable military precision or low-power consumption (but not both)
- Choosing hardware architectures to support the next embedded system
- Learning about new-generation programming tools
- Understanding the efficiencies obtained (power and performance) in applying those tools correctly

Program Chair:
Stephan Ohr

Editorial Director, Analog and DSP; Editor-in-Chief, *Planet Analog*
CMP Media LLC

Easy Paths to Silicon
design seminar

March 7-8, 2005

This seminar looks at ways to implement applications or algorithms in hardware that don't involve a traditional ASIC flow. Aimed at systems and software engineers, it will provide an introduction to FPGAs, configurable array architectures, and algorithm-to-silicon EDA tools and flows.

Key Takeaways

- Understanding when to consider placing algorithms or applications into silicon
- Finding the easiest and most cost-effective silicon implementations that fit your requirements
- Learning how to design with FPGAs, including processor cores, operating systems and IP
- Learning how EDA tools can bring algorithms into silicon

Program Chair:
Richard Goering

Editorial Director, Design Automation, CMP Media LLC

Consumer Systems
design seminar

March 8-9, 2005

An historic shift from analog to digital music and video is giving rise to a new generation of digital TVs and media servers, MP3 players of all sorts and home networks capable of streaming and storing digital media. This seminar explores design issues in analog, DSP, compression, display and other technologies that are the key enablers for this sector.

Key Takeaways

- Receiving detailed design insights from engineers who have designed and analyzed top brand digital TVs, set-top boxes, and MP3 players
- Hearing up-to-date information about how to handle thorny issues such as copyright protection, digital rights management, and systems interoperability
- Learning the latest software techniques in Linux and user-interface programming for consumer systems
- Meeting other working engineers in leading consumer companies

Program Chair:
Rick Merritt

Editorial Editor-at-Large, *EE Times*

3G Cellular System

design seminar

March 8-9, 2005

This seminar will look at the system-level design engineering challenges related to the development of infrastructure and mobile devices that operate on third-generation (3G) wireless networks. The seminar will look at technology issues, such as DSP power management, and RF design, as well as emerging standards and regulatory issues that will impact the design of 3G systems and equipment.

Key Takeaways

- Learning tips and techniques for supporting the delivery of video and 3D gaming capabilities to mobile phones
- Gaining insights into key 3G cellular specifications being deployed and under development
- Understanding software-radio and other advanced RF architectures and their impact on mobile phone and base station designs
- Learning RF and baseband techniques that will be needed to deliver broadcast video to a mobile phone

Program Chair:
Robert Keenan
Editor-in-Chief,
CommsDesign.com

Wireless Networking

design seminar

March 9-10, 2005

This seminar will focus on resolving the problems facing wireless network designers as they tackle issues such as ultrawideband, Wi-Fi/cellular integration, ZigBee and other short-range wireless networking technologies.

Key Takeaways

- Evaluating and selecting the optimum wireless sensor network
- Designing ultrawideband antennas and systems
- Incorporating QoS, security, smart antennas and mesh networking into their next system design
- Understanding international regulatory issues and the various WLAN and wireless personal area networking standards

Program Chair:
Patrick Mannion
Wireless & DSP Editor;
CommWeek & In Focus Section Editor,
EE Times

Network Systems

design seminar

March 9-10, 2005

This seminar will spotlight the convergence of all traffic to the Internet Protocol by showing how voice traffic, data traffic, and video rides on a common backbone of IP and Ethernet. Both days of the Network Systems Design seminar will try to achieve a balance of hardware and software, as they are key to all aspects of internetworking. On day one, workshops will be held on IPv 6 and on Linux standards in software. Hardware sessions will include a workshop on interoperability led by Intel, and paper sessions on switching fabrics, network security, and network processors. Additionally, a panel session will address chip-level support for the XML language. On day two, software sessions will include workshops on symmetric multiprocessing and on Session Initiation Protocol (critical for Voice over IP), while a software paper session will address real-time operating systems. Hardware sessions on day two include workshops on 10-Gigabit Ethernet and on modular communications, and paper sessions on traffic management, line cards, and Voice Over IP.

Key Takeaways

- Understanding practical design techniques for Voice Over IP systems
- Gigabit Ethernet switches and routers, and future common-chassis systems based on the ATCA backplane standard
- Learning about Linux in telecom, new trends in IP protocols, symmetric multiprocessing, and real-time kernels

Program Chair:
Loring Wirbel
Editorial Director,
Communications Initiative,
CMP Media LLC

Design Seminars

8:30 am – 10:00 am

APD-500 **Data Converter Architectures**
Walt Kester, Corporate Staff Applications Engineer, Analog Devices, Inc.

This class examines the three most popular ADC architectures: sigma-delta, successive approximation, and pipelined. The basics of each architecture are discussed, with emphasis on interface, and timing implications. Practical application examples of each architecture are shown, along with overall selection guidelines.

APD-501 **Linear Regulator and Switching Mode Power Supply Basics**
Henry Zhang, Power Application Section Leader, Linear Technology Corp.

This class provides a fundamental understanding of linear regulator (LR) and switching mode power supply (SMPS) to the system designers who do not have strong power electronics backgrounds. It covers basic operating principles and differences of LR and SMPS, the advantages and disadvantages of each solution, and how to determine the right solution for your application.

11:00 am – 12:30 pm

APD-520 **Op Amps and Op Amp Applications**
Ronald Mancini, Staff Scientist, Texas Instruments, Inc.

Michael Steffes, Strategic Marketing Manager, Texas Instruments, Inc.

The proliferation of amplifiers presents a selection problem for even the most experienced analog designers. Selection criterion based on key specifications, such as bandwidth, dynamic range, and costs can help. For ADC input interface circuits, noise performance (such as spurious-free dynamic range, SFDR) is explained, and, for power op amps, load resistance and pulse width modulation (PWM) techniques.

APD-521 **Matching power MOSFETs and Pulse Width Modulators**
Carl Blake, Director of Technical Marketing for the Computing and Communications Sector, International Rectifier

The variety of MOSFETs has expanded exponentially since the 1980s, when peak voltage and Rdson were once the primary selection criteria. This class provides insight into how secondary parameters affect in-circuit performance. Focusing upon the latest characterization techniques, this selection process includes discussions into the difference between data sheet specifications and actual in-circuit performance.

1:30 pm – 3:00 pm

APD-540 **Designing for Digital Audio**
Don Dapkus, Applications Engineering Manager, Texas Instruments, Inc.

This class discusses the trade-offs made during two designs that use class-D amplifiers. The first design is for a speaker system used with LCD monitors and TVs, and the second design is for a mobile phone that makes use of a class-D amplifier.

APD-541 **Application Requirements Drive Voltage Regulator Selection in Portable Systems**
David Brown, Manager of Application Engineering, Advanced Analogic Technologies

Portable system designers must maximize battery life while offering an extensive array of features at the lowest cost and with the least amount of design complexity. This class compares the attributes of low dropout (LDO) linear voltage regulators, capacitive charge pump switching regulators, and inductive DC/DC switching regulators.

3:15 pm – 4:45 pm

APD-560 **High Speed Interface Considerations**
Moderator: Stephan Ohr, Editorial Director, eeProductCenter and Editor-In-Chief, *Planet Analog*

Differential Signal Processing in High-Performance Data Acquisition Systems
James Karki, Systems Engineering Manager, Texas Instruments, Inc.

Trends in Digital Interfaces for High-Speed ADCs
Robbie Shergill, Applications Manager, Data Conversion, National Semiconductor

Upgrading a 1-Gbps System to Support Data Rates of 4 Gbps
Falk Alicke, System Engineer, Texas Instruments, Inc.

Select the Right Operational Amplifier for your Filtering Circuits
Bonnie Baker, Analog Applications Engineering Manager, Microchip Technology, Inc.

APD-561 **Specialized Power Management Applications and Techniques**
Moderator: Paul O'Shea, Senior Technology Editor, *EE Times*' Power Management DesignLine

Powering FPGAs
Ajit Jain, Strategic Marketing Manager, National Semiconductor

Setpoint Accuracy and Temperature Effects in Communications Equipment
Tom DeLurio, Director of Applications Engineering, Summit Microelectronics, Inc.

8:30 am – 10:00 am

DSP-502 Microprocessors vs. Digital Signal Processors

Jeff Bier, General Manager, Berkeley Design Technology, Inc.

As more and more applications incorporate signal-processing features, an increasing number of system designers must decide whether a MPU or a DSP is the best choice for their systems. This class highlights the special requirements of signal processing applications, introduces the differences between low-end and high-performance MPUs and DSPs, and explores criteria for deciding when to use a MCU and when to use a DSP.

DSP-503 Efficient Coding Techniques for High-Performance Embedded Applications

David Katz, Senior DSP Applications Engineer, Analog Devices, Inc.

Rick Gentile, Senior DSP Applications Engineer, Analog Devices, Inc.

Tom Lukasiak, Senior DSP Applications Engineer, Analog Devices, Inc.

Today's digital signal processors (DSPs) have achieved such an attractive mix of performance, peripheral mix, power dissipation and pricing that many system designers are eager to explore their benefits over the processors with which they've traditionally designed. This class discusses programming strategies and techniques for DSPs in today's development environment.

11:00 am – 12:30 pm

DSP-522 Evaluating the DSP Processor Options

Jeff Bier, General Manager, Berkeley Design Technology, Inc.

This class explains the architectural approaches used in the latest crop of DSP processors. It includes the evaluation of several recently introduced processors such as Texas Instruments' TMS320C64x, Analog Devices' Blackfin, and Freescale's MSC711x in terms of speed, cost, energy efficiency, development tools, and other considerations.

DSP-523 C-Compilers for DSP Programming

Moderator: Stephan Ohr, Editorial Director, eeProductCenter and Editor-In-Chief, *Planet Analog*

Advanced Compiler Optimizations for the Smallest, Fastest Code
Greg Davis, Engineering Manager, Compiler Development, Green Hills Software

Tuning DSP Compilers
George Mock, Software Engineer, Texas Instruments

Using Embedded-C for High Performance DSP Programming
Marcel Beemster, Senior Software Engineer, ACE Associated Compiler Experts

1:30 pm – 3:00 pm

DSP-542 Mixed Controller and DSP Architectures

Moderator: Marty Gold, Executive Editor, eeProductCenter and EE Times' ProductWeek

The Advantages of Hybrid Controllers in Design
Scott Lynch, Operations Manager, Freescale Semiconductor, Inc.

DSP Performance Improvements in General Purpose Processors
Steve Steele, Applications Engineer, ARM Ltd.

Look Under the Hood of the dsPIC DSC
Richard Fischer, Manager, Digital Signal Controller Applications, Microchip Technology, Inc.

DSP-543 Multimedia Programming Issues

Moderator: Lindsey Vereen, Editorial Director, *Embedded Systems Programming* and embedded.com

DSPs: The Backbone of the Digital Video Migration
Yvonne Cager, Manager, DSP Video Solutions, Texas Instruments, Inc.

FPGA Design of Video/Imaging Filters
Chang Choo, Technologist, Silicon DSP

Harnessing Parallelism for Video Processing Applications
Amit Gulati, Applications Engineering Manager, Cradle Technologies

3:15 pm – 4:45 pm

DSP-562 DSP Algorithm Implementations

Moderator: Henry Davis, DSP Consultant, Henry Davis Associates

Lowering the Barrier to DSP Design
Mike Trimborn, LabVIEW FPGA Product Manager, National Instruments

Optimizing Performance of DSP Systems through Block-Level Design
Tom Cesear, Director, IP Development and Consulting Services, AccelChip Inc.

DSP-563 Specialized Applications

Moderator: Jim Lipman, Vice President Client Services, Cain Communications

Boosting the Performance and Quality of Safety Critical Software
Nat Hillary, Field Applications Engineer, MetroWerks

Building Complex GUIs for Low-End Embedded Systems
Michael Juran, President, Altia

Designing and Optimizing Software for Symmetric Multiprocessing
Sebastien Marineau-Mes, Senior OS Manager & Architect, QNX Software Systems

6:00 pm – 7:00 pm

Panel The Future of Processors for Signal Processing Applications

Moderator: Jeff Bier, General Manager, Berkeley Design Technology, Inc.

Please see page 4 for further details.

< open to all attendees >

8:30 am – 10:00 am

EPD-504 Introduction to Programmable SoCs

Bob Zeidman, President, Zeidman Consulting

This class examines various programmable SoCs and their underlying architectures and technologies. It discusses tradeoffs between different FPGA families and explores new architectures, particularly with respect to SoCs.

EPD-505 Choosing the Right Semiconductor Platform for Your Design

Phillip LoPresti, Associate Vice President and General Manager, Custom LSI SBU, NEC Electronics America

This class looks at cost, time-to-market and performance advantages and disadvantages of cell-based ASICs, ASSPs, FPGAs and structured ASICs to help designers select the design platform that best fits their custom application's needs.

11:00 am – 12:30 pm

EPD-524 Designing with Embedded Processor Cores in FPGAs

R.C. Cofer, Field Applications Engineer, Avnet

Ben Harding, Field Applications Engineer, Avnet

This class presents an overview of hard and soft FPGA Embedded Processor Cores (EPCs). EPC technology, vendors, choices, performance, toolsets and design flows for programmable logic will be discussed. It covers advantages, disadvantages, design tradeoffs, design estimation, implementation, debug and potential problems, and mitigations for designing with soft processor cores within FPGAs.

EPD-525 Real-Time Operating Systems for SoCs

Bob Zeidman, President, Zeidman Consulting

This class examines different options for putting an RTOS on an SoC. It will examine tradeoffs between three options: writing your own RTOS, purchasing an off-the-shelf RTOS, and using a software synthesis tool to automatically generate an RTOS.

1:30 pm – 3:00 pm

EPD-544 Designing with IP in FPGAs

RC Cofer, Field Applications Engineer, Avnet

Ben Harding, Field Applications Engineer, Avnet

This class presents the process of evaluating, selecting and implementing IP blocks within FPGAs. FPGA design flow for implementing IP, questions to answer when evaluating IP providers, common IP support models, IP licensing and evaluation models, terminology, and documentation are discussed along with an overview of available IP categories and offerings for FPGA providers.

EPD-545 Hardware/Software Co-Design for FPGAs Using C

David Pellerin, CTO, Impulse Accelerated Technologies, Inc.

Embedded systems designers have new options to rapidly develop, simulate and implement high computational throughput algorithms for FPGAs using standard C and popular C development environments. This class demonstrates the path from C to hardware, including debugging, automatic parallelizing, hardware/software partitioning, and FPGA synthesis.

3:15 pm – 4:45 pm

EPD-564 FPGAs - Tools and Flows: An Overview for the Beginner

Mike Dini, President, The DINI Group

This class provides an overview of the tools and flows necessary to do FPGA design today. Topics covered include: What is an FPGA; What tools and resources are needed to do FPGA design; What are the languages; VHDL/verilog/other; What is the controversy; How does the flow work, and What does the future look like?

EPD-565 FPGA Design Evaluation: Using a Starter Kit to go from Soup to Nuts

Martin Mason, Director of Flash FPGA Product Apps, Actel Corp.

This class examines the productivity gains that can be realized by using a starter kit with step-by-step instructions that show users how to take a design rapidly from concept to completion while getting the most from the tools and silicon. It also examines how the starter kit can subsequently be integrated into a more complex system for rapid prototyping.

8:30 am – 10:00 am

EPD-604 Implementing DSPs in FPGAs

RC Cofer, Field Applications Engineer, Avnet Design Services

Ben Harding, Field Applications Engineer, Avnet

This class addresses the architectural features developed for implementing DSP functions and evaluation of which algorithms can be efficiently implemented with these features. Design flow, critical design decisions, terminology, numeric representation, and arithmetic operations are presented along with performance and implementation cost tradeoffs, available DSP Intellectual Property (IP) and design verification and debug approaches.

EPD-605 Processors, Coprocessors, Accelerators: Synthesizing Algorithms into Hardware

Moderator: Daya Nadamuni, Principal Analyst, Gartner Dataquest

Creating Performance And Power-Efficient Algorithms for C-to-RTL Application Engine Synthesis
Craig Gleason, Director of Hardware, Synfora, Inc.

A Methodology and Tooling Enabling Application-Specific Processor Design
Andreas Hoffmann, Engineering Director, CoWare Inc.

Using Coprocessor Synthesis to Accelerate Embedded Software
Richard Taylor, CTO, CriticalBlue

10:15 am – 11:45 am

EPD-624 Taking the HARD out of Hardware Design by Using a MATLAB-Based Design Flow

Eric Cigan, Product Manager, AccelChip Inc.

Yanbing Li, Senior Corporate Application Engineering Manager, Synopsys

This class explains how algorithmic synthesis connects MATLAB modeling to hardware implementation for DSP algorithms. Attendees learn the tool flow that makes this connection, and how to automate today's manual steps in DSP design, increase knowledge of hardware design to improve design specifications, and convert a high-level model into a form that can end up in a chip.

EPD-625 Behavioral Synthesis from C Language Algorithms

Moderator: Richard Goering, Editorial Director, Design Automation, CMP Media LLC

C-Based Algorithm Design and Synthesis to FPGA
Stephen Chappell, Director of Applications Engineering, Celoxica

Implementation Independent Design of a Digital Imaging Algorithm Using Behavioral Synthesis
David Pursley, Technical Marketing Manager, Forte Design Systems

2:15 pm – 3:45 pm

EPD-644 Model-Based Design of High-Speed Signal Processing Hardware for Software Radio

Brian Ogilvie, Principal Engineer, The MathWorks, Inc.

Paul Pacheco, Senior Engineer, The MathWorks, Inc.

This class describes the application of model-based design to accelerate the development of signal processing hardware. The concepts are illustrated through step-by-step design, simulation, code generation, and verification of a high-speed digital down conversion "front end" for a software-defined radio application.

EPD-645 Using FPGAs for Peripheral Expansion and Acceleration

Moderator: Ron Wilson, Semiconductor Editor, *EE Times*

Implementing Hardware Acceleration in Embedded Systems
Mike Alford, CTO, QuickLogic

Solving the Interface Challenges for FPGA-Based Peripherals and Algorithm Accelerators
Joe Hanson, Director of System Level Tools Marketing, Altera

4:00 pm – 5:30 pm

EPD-664 Approaches in FPGA Design

Moderator: Nancy Wu, Principal Analyst, Gartner Dataquest

Hardware/Software Co-Design for Platform FPGAs
Tim Tripp, Advanced System Tools Product Marketing, Xilinx

Protecting Intellectual Property In FPGA Devices
Tom Barraza, Senior Staff IP Solutions Engineer, Actel Corp.

Using FPGA-Based Design to Deliver Embedded Solutions Customized to Specific System Needs
Bob Garrett, Senior Marketing Manager, Altera

EPD-665 Configurable Architectures Bring Algorithms into Silicon

Moderator: Richard Goering, Editorial Director, Design Automation, CMP Media LLC

Easily Translating C Algorithms into Hardware with Configurable Processors
Dror Mayden, Director of Software Development, Tensilica

Software Defined ICs Ease Design and System Integration
Paul Master, CTO, QuickSilver Technology

8:30 am — 10:00 am

CSD-600 Intro to Video Compression

Jeff Bier, General Manager, Berkeley Design Technology, Inc.

This class explains basic video compression algorithms, including still-image compression, motion estimation, artifact reduction, and color conversion. The demands these codecs make on processors and the consequences of these demands are discussed.

CSD-601 GUIs for CE Systems

Moderator: Seamus McAteer, Analyst, Zelos Group

Powerful User Interfaces for Consumer Devices Using Web Technology

Barry Merrick, Software Architect and Engineering Manager, ANT Ltd.

10:15 am — 11:45 am

CSD-620 Processors for Consumer Audio/Video Applications

Jeff Bier, General Manager, Berkeley Design Technology, Inc.

This class explores the types of processors used in consumer audio/video applications, including general-purpose CPUs, DSPs, media processors, and application-specific standard products. It will characterize the strengths and weaknesses of each type of device, and evaluate leading processors in terms of performance, efficiency, development infrastructure, and vendor strategies.

CSD-621 Design Issues for Linux in CE Devices

Moderator: Kevin Dankwardt, Principal, K Computing, and member of the Embedded Linux Consortium

More Power to You: Embedded Linux Technologies for Dynamic Power Management in Consumer Devices

John Mehaffey, Architect, MontaVista

Time and Space: Optimizing Boot Up and Footprint in Linux-Based CE Devices

Bill Weinberg, Open Source Architecture Specialist, OSDL

What You Need to Know About the CELF Specifications for Linux in Consumer Devices

John Mehaffey, Architect, MontaVista

2:15 pm — 3:15 pm

CSD Panel The Transformation of the TV

Moderator: Nikhil Balram, CTO of Displays Division, National Semiconductor

Panelists from leading display companies, semiconductor companies, and consumer electronics companies discuss some of the dramatic new innovations that are combining to effect a dramatic transformation of the respectable middle-aged 20th century TV set into a wild and exciting 21st century teenager.

< open to all attendees >

4:00 pm — 5:30 pm

CSD-660 Issues in Video Design

Moderator: Peter Glaskowsky, Editor-in-Chief, Microprocessor Report

Designing and Implementing Low Cost Portable Media Devices on Resource Limited Systems

Kevin Wells, 32-bit Applications Engineer, Sharp Microelectronics

Overcoming the Bit-Rate Barrier: Encoding Techniques for Delivering High-Quality Video over Low-Bandwidth Networks

Indra Laksano, Vice President, Research & Development, ViXS Systems

CSD-661 FCC Certification for Digital TV Devices

Gopal Miglani, President, BitRouter

This class focuses on software design issues for today's Digital TV receives including CableCARD, EIA-708-B, Advanced Television Systems Committee (ATSC) PSIP and Cable out-of-band SI data. It also addresses issues for future receivers which will need to include IEEE 1394, two-way and multi-stream CableCARD and the Open Cable Applications Platform (OCAP).

8:30 am – 10:00 am

CSD-700 Digital Video Recording and Video-On-Demand Servers

Mike Ficco, Chief Architect, Hughes Network Systems

This class is designed to help embedded developers deliver the long promised dream of Video-On-Demand. It focuses on important design considerations for efficient acquisition, storage, and presentation of digital multimedia.

CSD-701 Multimedia Home Networking Design

Moderator: John Antonchick, Consultant, NCN Associates

Networking with Coaxial Media
Ladd Wardani, President MOCA and VP Business Development, Entropic Communications

Networking with HomePlug (Powerline) Technology
Arnaud Perrier, Product Manager, INTELLON Corp.

Networking with Ultra Wide Band RF Technology
Rajeev Krishnamoorthy, CEO and Founder, TZero Technologies, Inc.

Streaming Video Issues
Mike Luby, CTO, Digital Fountain

11:00 am – 12:30 pm

CSD-720 Embedded Streaming Media Servers

Mike Ficco, Chief Architect, Hughes Network Systems

The convergence of new technologies and economical extremely large hard drives has enabled relatively economical embedded platforms to perform as household and multi-dwelling-unit video servers. This class presents methods of efficiently storing and distributing multimedia. It focuses on delivering the media to local and remote clients.

CSD-721 Evolution of the iPod and Beyond: Silicon Rocks

David Carey, President, Portelligent

This class tracks the Apple iPod family in detail, examining the electronics architecture and changes therein. Along with electronics, focus is on system design, which must bring together an increasingly commodity set of components to stand apart from the crowd.

2:00 pm – 3:30 pm

CSD-740 Design Issues in Digital Television

Bill Burnett, President, D2M

This class gives practical guidance on designing compelling flat-screen and digital television products. The presenter is from a leading digital TV design house that has developed DTV products for several leading brand OEMs.

CSD-741 Design Issues in Digital Rights Management

Moderator: Peter Hoddie, Principal, Kinoma

Managing Digital Content Rights in Embedded Devices
Niels Rump, Senior Consultant, Rightscom

Profiling and Binary Encoding of the MPEG REL for Embedded DRM Systems
Xin Wang, Chief Scientist, ContentGuard, Inc.

3:45 pm – 5:15 pm

CSD-760 Home Networked Device Interoperability Guidelines

Jim Edwards, Co-editor, Interoperability Guidelines, Digital Living Network Alliance

This class presents the latest version of the home networked device interoperability guidelines from the Digital Living Network Alliance. The guidelines establish a technical platform that enables consumer electronics, personal computers and wireless devices to seamlessly share content through a wired or wireless network, bringing the industry one-step closer to the realization of truly digital living.

CSD-761 Copyright Protection in Consumer Systems

Content Protection in Networks of 1394 CE Devices
Michael Johas Teener, System Architect, PlumbLinks

How to Handle Copyright Protection over the HDMI Interconnect
Brett Gaines, Chairman, Panelink LLC

8:30 am — 10:00 am

3GC-602 Inside the 3GPP and 3GPP2 Specs

The transition from existing second generation (2G) and 2.5G networks to third generation (3G) wireless networks is in full swing. And, during the transition, ETSI-backed 3GPP and ITU-backed 3GPP2 have played and will continue to play a key role in developing the specifications that will shape the design and development of 3G systems and eq1uipment. In this class, presenters from both standards bodies examine the key specifications that have been defined to date while also examining future specs under development and their impact on the development of cellular phones, base stations, and other 3G systems.

Moderator: Robert Keenan, Editor-in-Chief, CommsDesign.com

3GPP

Asok Chatterjee, Vice President, Ericsson Inc.

3GPP2

Edward Tiedemann, Senior Vice President of Engineering, Qualcomm

3GC-603 The Direction of Advanced Voice Codecs

Huan-yu Su, Executive Director, Speech Processing, Mindspeed Technologies, Inc.

With increasing demands for voice quality and additional new services that require large bandwidth, advanced speech compression will play an important role in the future of 3G networks. This class discusses how advanced voice codecs are changing, and what needs to be done to make it happen.

10:15 am — 11:15 am

3GC Panel Moving Beyond 3G: Where Do We Go From Here?

Moderator: Robert Keenan, Editor-in-Chief, CommsDesign.com

With 3G deployments slated to increase dramatically in 2005, wireless system designers must now start laying the ground work for its next evolution path. But, the big question is: Where do we go from here? This panel will draw on technical experts from all corners of wireless to look at the technologies that will shape the future of cellular design. Topics discussed will include, broadcast video, increased uplink/downlink speeds, cognitive radio, WiMAX, and the impact of OFDM and the move to all-IP networks.

< open to all attendees >

2:15 pm — 3:45 pm

3GC-642 Increasing Cellular Uplink Speeds with HSUPA

Fabricio Velez, Solution Development Manager, Nokia

The 3GPP committee has defined the high-speed uplink packet data access (HSUPA) concept to increase uplink performance. This class examines the main technological improvements provided by the HSUPA and their impact on system performance. The class also looks at the capacity increases provided by HSDPA and provides a general overview of an HSUPA implementation in a RAN and mobile design.

3GC-643 Managing Power in Mobiles

Moderator: Robert Keenan, Editor-in-Chief, CommsDesign.com

Backlighting the Low Power, Low Cost Way with Charge Pumps

Tom Karpus, Applications Engineering Manager, Handhelds, Semtech Corp.

Designing for Low Power in 3G/Dual-Mode Mobiles

Michael Barkway, 3G Silicon Technology Product Manager, TTPcom

RT-OS Run Time Power Management for Mobile Terminals

Roberto Zafalon, Low Power System Design Manager, STMicroelectronics

4:00 pm — 5:30 pm

3GC-662 Broadband-Enabling Cellular Nets

Moderator: Craig Mathias, Principal Analyst, Farpoint Group

IEEE 802.20: Maximizing Spectrum Efficiency for Mobile Data Services

Lars Johnsson, Senior Director of Product Management, Flarion Technologies

Understanding HSDPA's Impact on W-CDMA Designs

Chaitali Sengupta, Senior Menber of Technical Staff, Texas Instruments, Inc.

Equipping WiMAX for Mobile Designs

Sai Subramanian, Vice President of Product Management, Navini Networks

3GC-663 Digital Television to your Cell Phone: DVB-H Markets, Technology and Testing

Paul Robinson, Director of Tektronix Cambridge Ltd, Tektronix, Inc.

Digital Video Broadcast for Handheld (DVB-H), the technology that brings digital video to handheld portable and mobile devices, has many implications for the next generation network and network operator. This class looks at DVB-H in terms of market demographics, implementation technologies, worldwide deployment plans and new test methodologies for the developer and network operator.

8:30 am – 10:00 am

3GC-702 **Tailoring Security for Mobile Designs**
Moderator: Victor Tsai, Senior Manager of Market Development, Renesas Technology America

Building Secure Applications on a Wireless Platform
Dan Kaplan, Manager, Software Development, SafeNet, Inc.

ECC: The Next Gen Crypto Step for Securing Mobiles
Robert Gallant, Cryptographic Engineer, Certicom Corp

Securing Smartphones from the Inside Out
Leonid Smolyansky, Systems & Architecture Manager, Freescale Semiconductor Israel Ltd.

3GC-703 **Standardizing Base Station Design Using OBSAI and CPRI**
Gerry Leavey, Technical Advisor, PMC-Sierra

New standards from the Open Base Station Initiative (OBSAI) and the Common Public Radio Interface (CPRI) promise a radical shift toward modular base station design using open interfaces. This compare-and-contrast class introduces designers to both standards and offers practical insight into developing compliant systems

11:00 am – 12:30 pm

3GC-722 **Advanced Radio Design Techniques**
Moderator: Doug Grant, Business Development Director, Analog Devices

Advanced RF Design Issues For Multimedia Applications in Mobile Handsets
Mohy Abdelgany, Vice President, RF Solutions, Skyworks Solutions, Inc.

Designing a Multi-Antenna, MC-CDMA SoC for 4G Apps
Friedbert Berens, Group Manager, STMicroelectronics

Making Antennas Smarter Inside a Mobile Phone
Jan Klein, Chief Strategist, Magnolia Broadband Inc.

3GC-723 **Digital Video and 3D Graphics Processing in Mobiles**
Moderator: Bill Krenik, Advanced Architectures Manager, Wireless Terminals Business Unit, Texas Instruments, Inc.

Developing Handsets for Graphically Intensive 3G Applications
Gaël Rosset, CTO, TTPCom Danmark

Digital Video Coding Standards in Handheld Systems
Bruce Flinchbaugh, Research Manager, Texas Instruments

Mobile Video: Meeting the Design Challenges of DSP + RISC
David Murray, Applications Group Manager, CEVA

2:00 pm – 3:30 pm

3GC-742 **The SDR-Enabled Handset—What It Is, Why It's Needed, and How to Build It**
Andre Kruetzfeldt, Member at Large, SDR Forum
Mark Cummings, Chairman of the Board, SDR Forum

This class examines the market needs for a software defined radio (SDR)-enabled handset and the technical challenges and solutions to building it. Emphasis will be placed on the importance of creating specific guidelines to help promote the globalization of the SDR-enabled handset.

3GC-743 **Building Reconfigurable Base Stations**
Alan Gatherer, Member of Technical Staff, Texas Instruments, Inc.

Many factors have pushed wireless operators and OEM business managers towards technical gurus who promise a world where a single radio can cope with almost any scenario. This class casts a bright light on the murky world of reconfiguration and examines why we need it, what can actually be done, and how far along the path we have come.

3:45 pm – 5:15 pm

Communications Keynote **SDR-Business, Market, and Social Ramifications**
Stephan Blust, Director of Wireless Standards, Cingular Wireless, and Chair of the SDR Forum
Mark Cummings, Managing General Partner, enVia, and Chairman of the Board, SDR Forum

Please see page 4 for further details.

< open to all attendees >

8:30 am — 10:00 am

WND-704 **Overview of Wireless Regulations**
Carl Stevenson, President and CTO, WK3C Wireless LLC

With a very innovative and proactive policy with respect to spectrum use, the Federal Communications Commission has put itself at the forefront of wireless development, particularly with initiatives such as ultrawideband signaling and the freeing up of more spectrum in the 5-GHz band for unlicensed use. More recently, the FCC has cast its eye toward ad-hoc spectrum reuse initiatives in the TV bands and has cast light on what many believe will be the next big thing—cognitive radio. This class looks at these and other pending FCC and global spectrum and regulatory initiatives with an emphasis on interpreting their impact on future wireless designs.

WND-705 **Personal Area Wireless Sensor Networks**
Moderator: Bob Heile, Chair, IEEE 802.15 Working Group on Wireless Personal Area Networks and Chair, ZigBee Alliance

Building Low Power into Wireless Sensor Networks Using ZigBee
Jon Adams, Director of Radio Technology, Freescale Semiconductor

How 802.11b/g WLAN and Bluetooth Can Coexist
Olaf Hirsch, Senior Principal Engineer and System Architect, Philips Semiconductors

Making Sense of the Sensor Network Value Chain
Jay Werb, Vice President of Technology, Sensicast Systems, Inc.

11:00 am — 12:30 pm

WND-724 **Standards 802.11 and 802.15**
Al Petrick, Vice-Chairman of IEEE 802.11 Working Group, Vice President of Business Development, IceFyre Semiconductor

From quality of service extensions and fast hand-off issues to next-generation wireless LAN architectures delivering higher data rates beyond 54-Mbps, the 802.11 working group is by no means resting on its laurels, despite its on-going success. So too with the 802.15 working group, which continues to develop wireless personal area networks, most notably those based on ultrawideband (802.15.3a) and 802.15.4, upon which ZigBee is based. This class rapidly takes attendees up to date on the latest developments within these two groups and lay out the path ahead for future improvements.

WND-725 **Ultra-Wideband Antenna Modeling and Design**
William Davis, Professor, Virginia Tech

This class presents an overview of antenna modeling and design for ultra-wideband (UWB) applications. Frequency independent, narrowband, and UWB antennas will be reviewed and compared from the perspective of size and bandwidth based on the concept of fundamental limits. Concepts of link budget and analysis are also presented.

2:00 pm — 3:30 pm

WND-744 **Next-Gen Wireless LAN Design**
Moderator: Craig Mathias, Principal Analyst, Farpoint Group

Mobile Data Handoff: Wireless LAN to a Fully Mobile WAN
Jim Durcan, Director of Product Management, Flarion Technologies

Multiple-Input, Multiple Output (MIMO) Antenna Design
VK Jones, Chief Scientist, Airgo Networks, Inc.

WLAN Receiver Architectures
Jung Yee, CTO, IceFyre Semiconductor

WND-745 **UWB Design**
Moderator: Jeff Reed, Professor, Bradley Department of Electrical and Computer Engineering, Mobile and Portable Radio Research Group (MPRG), Virginia Tech

Practical Techniques for Interference Rejection for UWB Systems
R. Michael Buehrer, Professor, Virginia Tech

Realizing the Promise of Ultrawideband through CMOS
Roberto Aiello, Founder and CEO, Staccato Communications, Inc.

Using DS-UWB for Optimized Convergence
Jerry Lynch, Director of Applications Engineering, Freescale Semiconductor, Inc.

3:45 pm — 4:45 pm

Communications Keynote: **SDR-Business, Market, and Social Ramifications**
Stephan Blust, Director of Wireless Standards, Cingular Wireless, and Chair of the SDR Forum

Mark Cummings, Managing General Partner, enVia, and Chairman of the Board, SDR Forum

Please see page 4 for further details.

8:30 am – 10:00 am

WND-804 QoS and Effective Voice-over-Wi-Fi Design

Moderator: Al Petrick, Vice-Chairman of IEEE 802.11 Working Group, Vice President of Business Development, IceFyre Semiconductor

Engineering for VoIP with 802.11
Greg Chesson, Director of Protocol Engineering, Atheros Communications

UWB: Approaches to Quality of Service
Peter Johanssen, Chair, 1394 TA Wireless Working Group, Congruent Software, Inc.

VoWLAN Challenges and Solutions for Today's Network
Prapaul Shivnani, VoIP Technical Staff, Texas Instruments, Inc.

WND-805 Wireless Network and Cellular Convergence

Moderator: Doug Grant, Business Development Director, Analog Devices, Inc.

Low-Cost Multi-Mode Technology for Converged Cellular and Data Mobile Handsets
Lon Christensen, CTO, Quorum Systems, Inc.

Signal Processing in Future Wireless Systems
Ahmad Bahai, CTO of Wireless Division, National Semiconductor

Unlicensed Mobile Access Lays Path to Cellular/WLAN Convergence
Rajeev Gupta, Director of Engineering, Kineto Wireless

11:15 am – 12:15 pm

WND Panel The Future of Wireless Networking

Moderator: Patrick Mannion, Wireless & DSP Editor, and CommWeek and In-Focus Section Editor, EE Times

With myriad wireless connectivity schemes already deployed and many more in the works, designers face the unenviable task of picking which—or how many—wireless interfaces to include in their next design. While the standard response is to "look at your usage model, then decide," that's an oversimplification in the light of ever-improving performance, cost, power and space characteristics of the newer interfaces being proposed. To answer the burning question as to where the future of wireless connectivity is headed—and how long will it take us get there—this panel probes some of the finest minds from industry, academia, and the venture capital and analyst communities.

< open to all attendees >

2:00 pm – 3:30 pm

WND-844 Securing Wi-Fi Networks

Jesse Walker, Security Architect, Communications Architecture Lab, Intel Corp.

This class on next generation security for Wi-Fi (802.11 wireless LANs) Robust Security Networks (RSN) will discuss how the latest security schemes work, what are their strengths and weaknesses and what is involved in their implementation. It will provide an overview of 802.11i, and hints about the ways to deploy it to get the most out of its security.

WND-845 Improving Wireless Networks with Antennas

Jack Winters, Chief Scientist, Motia, Inc.

This class discusses the use of smart antennas in WLANs. MIMO systems are described, as will the impact of smart antennas on mesh networking. Performance results and extensions are included and future applications (beyond Wi-Fi to areas such as WiMax) of smart antenna technology are discussed.

3:45 pm – 5:15 pm

WND-864 WiMAX Demystified

Mohammad Shakouri, Associate Vice President of Business Development, Alvarion

This class provides an educational, objective overview of the WiMAX solution as it applies to different operators such as fixed, wireless Internet service providers (WISPs) and cellular. It highlights the timeline for conformance and interoperability testing and certification, and details the opportunities for service providers to leverage WiMAX in their network service offerings.

WND-865 Mesh Network Design and Implementation

Moderator: Patrick Mannion, Wireless & DSP Editor, and CommWeek and In-Focus Section Editor, EE Times

Issues on Robustness and Scalability of Wireless Mesh Networks
Sokwoo Rhee, CTO, Millennial Net

Mesh Networking Contains the Tools for Overcoming its Own Weaknesses
Zachary Smith, Chief Software Architect, Ember Corp.

Mesh Networks: A Solution for Mobile Data
Peter Stanforth, CTO, MeshNetworks

8:30 am – 10:00 am

NSD-706 Linux as an Embedded Operating System and Development Environment

Ed Bizari, Director of Business Planning, Performance Technologies

The ongoing growth and maturity of Linux as a fully functional and flexible operating system environment is key to advances in embedded software. This class discusses the performance and integrated benefits of contemporary silicon devices coupled with the functionality and cost benefits of Linux that are providing embedded developers with options never before available.

NSD-707 Switching Fabrics at Layers 1 and 2

Moderator: To Be Determined

An Area-Efficient, Scalable, High Speed Serial Full Mesh Switch Fabric Design for FPGA
Hamish Fallside, Senior Manager Networking Systems Solutions, Xilinx, Inc.

ATCA Platform for High End Core/Edge Switch
Reuven Segev, Director of Marketing, TeraChip

Blade-Level Switching: A Key to Upgradeable L4-7 Services
Uri Cummings, Co-Founder & Vice President of Product Development, Fulcrum Microsystems

11:00 am – 12:30 pm

NSD-726 Seamless Networking

Alan Crouch, Director, Performance Networking Lab, Intel Corp.
Dan Dahle, Senior Strategic Architect, Intel Corp.

The convergence of computing and communications is driving the global demand for always-on wireless connectivity—anytime, anywhere, any device. This class provides an overview of Intel's work with the industry to lay the foundation for an end-to-end architecture that enables seamless and simple wireless connectivity.

NSD-727 Network Security

Moderator: Loring Wirbel, Editorial Director, Communications Initiative, CMP Media LLC

Moving Security Services to the Service Provider Network Edge
Mark Orthodoxou, Product Manager, IDT, Inc.

Third-Party Software for Security, VoIP and Wireless Networking Equipment
Srinivasa Rao Addepalli, CTO and Chief Architect, Intoto, Inc.

WLAN Security: VPNs vs. 802.1X
Matthew Gast, Corporate Systems Engineer, Trapeze Networks

2:00 pm – 3:00 pm

NSD Panel Silicon Support at Layer 7: XML, SOAP, and Vertical Protocols

Moderator: Loring Wirbel, Editorial Director, Communications Initiative, CMP Media LLC

Chip-level acceleration for network protocols has slowly and sequentially climbed up the seven layers of the Open Systems Interconnect protocol stack. Many skeptics questioned whether silicon acceleration would ever be possible at the application layer, Layer 7. The advent of XML, the eXtensible Markup Language, has silenced the skeptics. XML and the Microsoft-derived Simple Object Access Protocol has spurred a development community into designing hardware that switches and routes content at the application layer. Three leading startups in the XML acceleration feature will discuss optimizing programmable processors for Layer 7, and developing dedicated chips to speed applications.

< open to all attendees >

3:45 pm – 5:15 pm

NSD-766 SIP-Based Applications

Subhash Verma, VP of Engineering, BayPackets

SIP has proven to be the signaling protocol for next generation telecom networks. This class discusses the various mechanisms SIP provides for the implementation of advanced SIP services in telecom networks, including session establishment, mobility, presence and instant messaging capabilities.

NSD-767 Control Plane and Data Path—New Processing Concepts

Moderator: To Be Determined

Advanced Managed Platforms: Solving Mission Impossible
Jim Medeiros, General Manager, Computing Products Group, Performance Technologies

Developing Endian Neutral Code for Embedded Applications
Lori Matassa, Staff Technical Marketing Engineer, Intel Corp.

New Model for Networking Solutions: One Device/Any Application
Peder Jungck, Founder and CTO, CloudShield Technologies, Inc.

8:30 am – 10:00 am

NSD-806 Using Symmetric Multiprocessing (SMP) to Build Highly Scalable Network Elements

Sebastien Marineau-Mes, Senior OS Manager & Architect, QNX Software Systems

SMP can offer enormous scaling benefits for applications such IP and MPLS route calculation, Layer 3 packet forwarding, storage caching, and call-processing encryption. This class explores recent advantages in SMP technology and provides engineers with practical techniques for designing and optimizing their SMP systems.

NSD-807 Traffic Management Using Advanced Protocols

Moderator: Loring Wirbel, Editorial Director, Communications Initiative, CMP Media LLC

Traffic Management Design and Applications in Modern Routers

Bidyut Parruck, CTO & Founder, Azanda Network Devices

Triple-Play Services Model—Technical Challenges

Paul Chopelas, Director of Applications Engineering, Bay Microsystems

11:15 am – 12:45 pm

NSD-826 Modular Communications Platforms: Driving Server Economics to create the Next Generation Network

Howard Bubb, Vice President, Intel Corp. and General Manager, Network Processing Group

Modular architectures provide telecommunications equipment manufacturers (TEMs) and carriers the option to purchase standard components from vendors, giving them the ability to deploy lower cost, scalable network equipment quickly and efficiently. This class will discuss how to deploy lower cost, scalable network equipment more quickly and efficiently.

NSD-827 Software Interaction: RTOS, Protocol Stacks, Services

Moderator: To Be Determined

Making Better Build vs. Buy Networking Equipment Development Choices

John Brandte, Vice President of Marketing and Business Development, NComm, Inc.

Optimized Integration of Real-Time Network Protocols into an RTOS

Charlie Grandgent, Sr. Software Engineer, CMX Systems Inc.

Tool Options: Maximizing Software Performance in Multi-Core Processors

Akash Deshpande, CTO and Founder, Teja Technologies

2:00 pm – 3:30 pm

NSD-846 IPv6 Trends in 2005

Susan Hares, CTO, NextHop

2004 has seen the US Government and Asian countries (China, Japan and Korea) committing money to build IPv6 networks and carriers and carrier exchange points are currently supporting IPv6 traffic at commercial levels. This class discusses what indicators should be watched to track IPv6 in 2005.

NSD-847 10Gigabit Ethernet over Copper Robust: Cost-Effective Connectivity in the Data Center

Mike McConnell, Co-Founder, KeyEye Communications

10Gigabit Ethernet over copper reduces the cost of adding bandwidth to data center applications. This class decribes the requirements and challenges of implementing 10Gigabit Ethernet over copper cabling, followed by a comparison of architectures and standards.

3:45 pm – 5:15 pm

NSD-866 How to Create IP Video Telephony Systems

Pradeep Bardia, Video Telephony Solutions Manager, Texas Instruments, Inc.

The growth of video telephony markets means that design engineers will need to be able understand how to integrate the needed system components. This class addresses the system considerations and how to build them to accommodate the demand for new products in home and in corporate environments.

NSD-867 Integrating Electronics and Optics in Multi-Gigabit Line Cards

Moderator: To Be Determined

Chip-to-Chip Flow Control on Line Cards

Jeremy Bicknell, Packet Exchange Product Manager, IDT

Managing the Risk of Embedding SerDes for High-Speed Network Applications

Vadim Shain, Systems Application Engineering Manager, Custom LSI Strategic Business Unit, NEC Electronics America

REGISTER TODAY!

1) Online: www.embedded.com/esc/sf

2) Fax: 415.947.6020 (a PDF of the registration form is available at www.embedded.com/esc/sf)

3) Phone: 800.441.8826
415.947.6130 outside US (m-f 9am-4pm pacific time)

Onsite Check-in and Registration Hours:

Sunday, March 6	7:30am – 4:00pm
Monday, March 7	7:30am – 5:30pm
Tuesday, March 8	7:30am – 8:00pm
Wednesday, March 9	7:30am – 7:00pm
Thursday, March 10	8:00am – 4:00pm

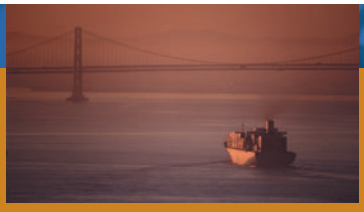
More Options Than Ever Before—For best conference rates, early registration is encouraged. No need to decide now which sessions you would like to attend. Use the priority code, located on the back of the catalog. **Use Priority code "IEEE"**

Pass Dates	Features		Register by Jan 11	Register by Feb 8	Register by March 3	Onsite Pricing
ePass [BEST VALUE] S M T W T ● ● ● ● ●	• Access to ALL of the 250 sessions offered in the Embedded Training Program, Design Seminars and the Microprocessor Summit • Exhibition 3/8–3/10 • Exhibit floor receptions	• Exhibitor workshop • Special events & networking • Downloadable class notes • Proceedings CD-ROMs • Conference bag • EEQuorum Portal	$1,795 SAVE $400	$1,945 SAVE $250	$2,045 SAVE $150	$2,195
Embedded Training Program 5-Day Pass S M T W T ● ● ● ● ●	• All Embedded Training Program sessions Sunday through Thursday • Exhibition 3/8–3/10 • Exhibit floor receptions • Exhibitor workshop	• Special events & networking • Downloadable class notes • Proceedings CD-ROM • Conference bag • EEQuorum Portal	$1,545 SAVE $450	$1,695 SAVE $300	$1,845 SAVE $150	$1,995
Embedded Training Program 3-Day Pass S M T W T ○ ○ ● ● ●	• Embedded Training Program classes Tuesday through Thursday • Exhibition 3/8–3/10 • Exhibit floor receptions • Exhibitor workshop	• Special events and networking • Downloadable class notes • Proceedings CD-ROM • Conference bag • EEQuorum Portal	$1,245 SAVE $250	$1,395 SAVE $100	$1,445 SAVE $50	$1,495
All Tutorials Pass S M T W T ● ● ○ ○ ○	• Embedded Training Program Sunday and Monday tutorials • Exhibition 3/8–3/10 • Exhibit floor receptions	• Exhibitor workshop • Special events & networking • Downloadable tutorial notes • Conference bag • EEQuorum Portal	$995 SAVE $300	$1,095 SAVE $200	$1,195 SAVE $100	$1,295
Sunday Tutorials Only Pass S M T W T ● ○ ○ ○ ○	• Embedded Training Program Sunday tutorials • Exhibition 3/8–3/10 • Exhibit floor receptions • Exhibitor workshop	• Special events & networking • Downloadable tutorial notes • Conference bag • EEQuorum Portal	$645 SAVE $300	$795 SAVE $150	$895 SAVE $50	$945
Monday Tutorials Only Pass S M T W T ○ ● ○ ○ ○	• Embedded Training Program Monday tutorials • Exhibition 3/8–3/10 • Exhibit floor receptions • Exhibitor workshop	• Special events & networking • Downloadable tutorial notes • Conference bag • EEQuorum Portal	$645 SAVE $300	$795 SAVE $150	$895 SAVE $50	$945
Design Seminar 2-Day Pass S M T W T ○ ● ● ○ ○ ○ ○ ● ● ○ ○ ○ ● ● ○ ○ ○ ○ ● ● ○ ○ ○ ● ●	*Choose one of the following 2-day seminars:* **Easy Paths to Silicon Design Seminar** **Consumer Systems Design Seminar** **3G Cellular Systems Design Seminar** **Network Systems Design Seminar** **Wireless Networking Design Seminar**	• Exhibition 3/8–3/10 • Exhibit floor receptions • Exhibitor workshop • Special events & networking • Downloadable proceedings • Downloadable class notes • Conference bag • EEQuorum Portal	$495 SAVE $300	$595 SAVE $200	$695 SAVE $100	$795
Design Seminar 1-Day Pass S M T W T ○ ● ○ ○ ○	*Choose one:* **Analog and Power Design Seminar** **DSP Performance Design Seminar** • Exhibition 3/8–3/10 • Exhibit floor receptions	• Exhibitor workshop • Special events & networking • Downloadable class notes • Downloadable proceedings • Conference bag • EEQuorum Portal	$295 SAVE $300	$395 SAVE $200	$495 SAVE $100	$595
Microprocessor Summit Pass S M T W T ○ ● ○ ○ ○	• All Microprocessor Summit sessions • Exhibition 3/8–3/10 • Lunch • Exhibit floor receptions	• Exhibitor workshop • Special events & networking • Proceedings binder • Conference bag • EEQuorum Portal	$695	$795	$895`	$995
Exhibits Plus Pass S M T W T ○ ○ ● ● ●	• Exhibition 3/8–3/10 • Exhibit floor receptions • Exhibitor workshop	• Special events & networking • Proceedings CD-ROMs* • Conference bag • EEQuorum Portal	$295	$295	$295	N/A
			*Must be purchased in advance. CD-ROMs must be picked up onsite.			
Exhibits Pass S M T W T ○ ○ ● ● ●	• Exhibition 3/8–3/10 • Exhibit floor receptions	• Exhibitor workshop • Special events & networking • EEQuorum Portal	$0 SAVE $50	$0 SAVE $50	$0 SAVE $50	$50

Group Discount Offer Bring your whole team! The more people you bring, the more you save. Discounts range from 15% to 35%. For more information call the registration team at 800/441-8826.

Online registration will be open until March 3, 2005. After March 3, you may register onsite at the Moscone South Convention Center on March 6-10, 2005. See web site for updates on registration.

Cancellations, Substitutions, Downgrades & Upgrades: If you need to cancel, you may do so for a 75% refund until Friday, February 4, 2005. Attendees who register prior to or after the deadline date who do not cancel in writing by the deadline date are liable for the pass cost and will be charged for the full registration fee. Sorry, no refunds or letters of credit are available after this date. Please fax your cancellation request to (415) 947-6020, or mail your request to: ESC Registration Department | CMP Media LLC | 600 Harrison Street, 6th Floor | San Francisco, CA 94107. Substitutions are allowed only with the written permission of the original registrant. Please mail your substitution request to the above address, or fax to (415) 947-6020. Written requests for a downgraded pass must be received no later than Friday, February 4, 2005 for a full refund on the difference of registration fees between the value of the original and downgraded pass. Requests received after February 4, 2005 will receive a letter of credit for the 2006 ESC issued for the difference in value of the pass downgraded from. Upgrade pass requests must be submitted in writing and faxed to (415) 947-6020 along with payment information for the difference in value.



Book your hotel early and save!

Embedded Systems Conference San Francisco has negotiated discounted hotel rates for our attendees and exhibitors. Reserve a room at participating hotels today.

To receive these special rates:

> Mention Embedded Systems Conference San Francisco when calling the hotel to make a reservation

> Make your reservation by Friday, February 11, 2005

All hotels are located in San Francisco. Rooms are limited and discounted rates are based on availability. Discounted rates apply for dates arriving on Saturday, March 5, 2005 and departing Friday, March 11, 2005. A seventy-two (72) hour individual cancellation policy applies to all of the hotels.

Groups of 8 or more: please contact the conference or convention services department at each hotel to receive a sub-block contract.

Participating Hotel	Address	Reservations	Rates
Argent Hotel	50 Third Street	877-222-6699 415-974-6400	$179 single/double
Best Western Americana	121 Seventh Street	415-626-0200 800-444-5816	$99 single/double
Grand Hyatt	345 Stockton Street	800-233-1234 415-398-1234	$165 single/double
Hotel Milano	55 Fifth Street	800-398-7555 415-543-8555	$119 single/double
Hotel Palomar	12 Fourth Street	866-373-4941 415-448-1111	$189 single/double
Marriott Courtyard	299 Second Street	800-321-2211 415-947-0700	$159 single/double
Marriott Hotel	55 Fourth Street	800-228-9290 415-796-1600	$209 single/double
The Mosser Hotel	54 Fourth Street	800-227-3804 415-986-4400	$129 single/double
Palace Hotel	2 New Montgomery Street	888-627-7196 415-512-1111	$189 single/double
Pickwick Hotel	85 Fifth Street	800-437-4824 415-421-7500	$119 single/double
Renaissance Parc 55	55 Cyril Magnin Street	800-697-3103 415-392-800	$159 single/double
W San Francisco	181 Third Street	877-946-8357 415-777-5300	$239 single/double
Westin St. Francis	335 Powell Street	800-937-8461 415-397-7000	$179 single/double

Check the web site for updated travel information at www.embedded.com/esc/sf

Embedded Systems Conference San Francisco

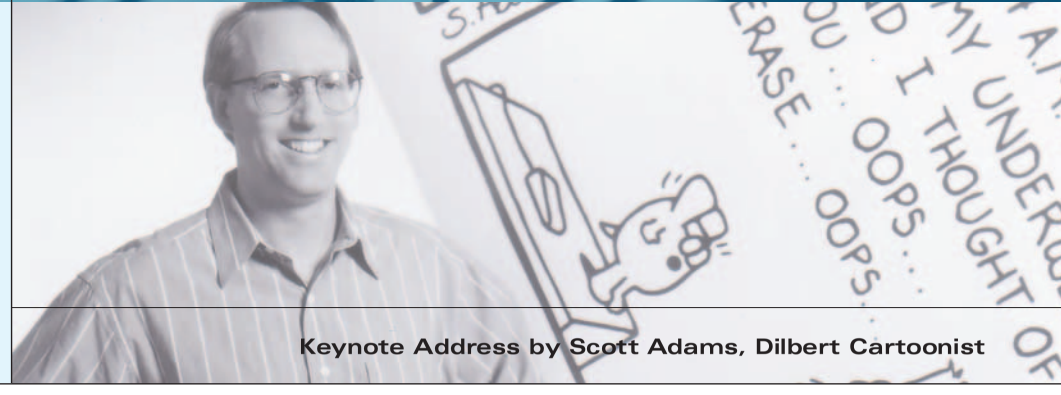
March 6-10, 2005

www.embedded.com/esc/sf

THE LARGEST SYSTEMS DESIGN EVENT IN NORTH AMERICA

The Embedded Systems Conference San Francisco is the premier training opportunity for anyone involved in electronics design.

- » **LEARN** relevant skills and how-to design techniques from 300 leading experts presenting 250 hardware and software sessions
- » **CONNECT** with industry experts, vendors, and your peers at a series of insightful keynotes, stimulating panel discussions, and multi-faceted networking opportunities
- » **DISCOVER** cutting-edge hardware, software, tools, and system components from 350 leading vendors who can provide solutions to your toughest design challenges



Keynote Address by Scott Adams, Dilbert Cartoonist

Embedded Systems Conference San Francisco
P.O. Box 45
Ferdinand, IN 47532

Media Sponsors: Embedded Systems Programming, EE Times

Use Priority Code "**IEEE**" to receive the lowest conference fees!