First International Computer,Inc

Protable Computer Group HW Department

Board name : Mother Board Schematic

Project : AT11

Version : 0.2

Initial Date : September 24 , 2004

1. Schematic Page Description :
2. PCI & IRQ & DMA Description :
3. Block Diagram :
4. Nat name Description :
5. Board Stack up Description :
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9. switch setting

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Title: AT11 < Dothan + 915GM + ICH6-M >

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1. Schematic Page Description :

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)
AD23	CardBus (TI 4510)
AD24	LAN 82562EZ

PCIINT	CHIP
IRQA	MiniPCI/CardBus
IRQB	MiniPCI/CardBus
IRQC	VGA/LAN
IRQD	ICH6-M Embeded USB2.0

BUSMASTER

REQ	CHIP
REQ0 / GNT0	MiniPCI
REQ1 / GNT1	CardBus
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ4 / GNT4	LAN(82562EZ)

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	~~FLOPPY DISK~~
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	MODEM/LAN
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	~~ECP~~
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

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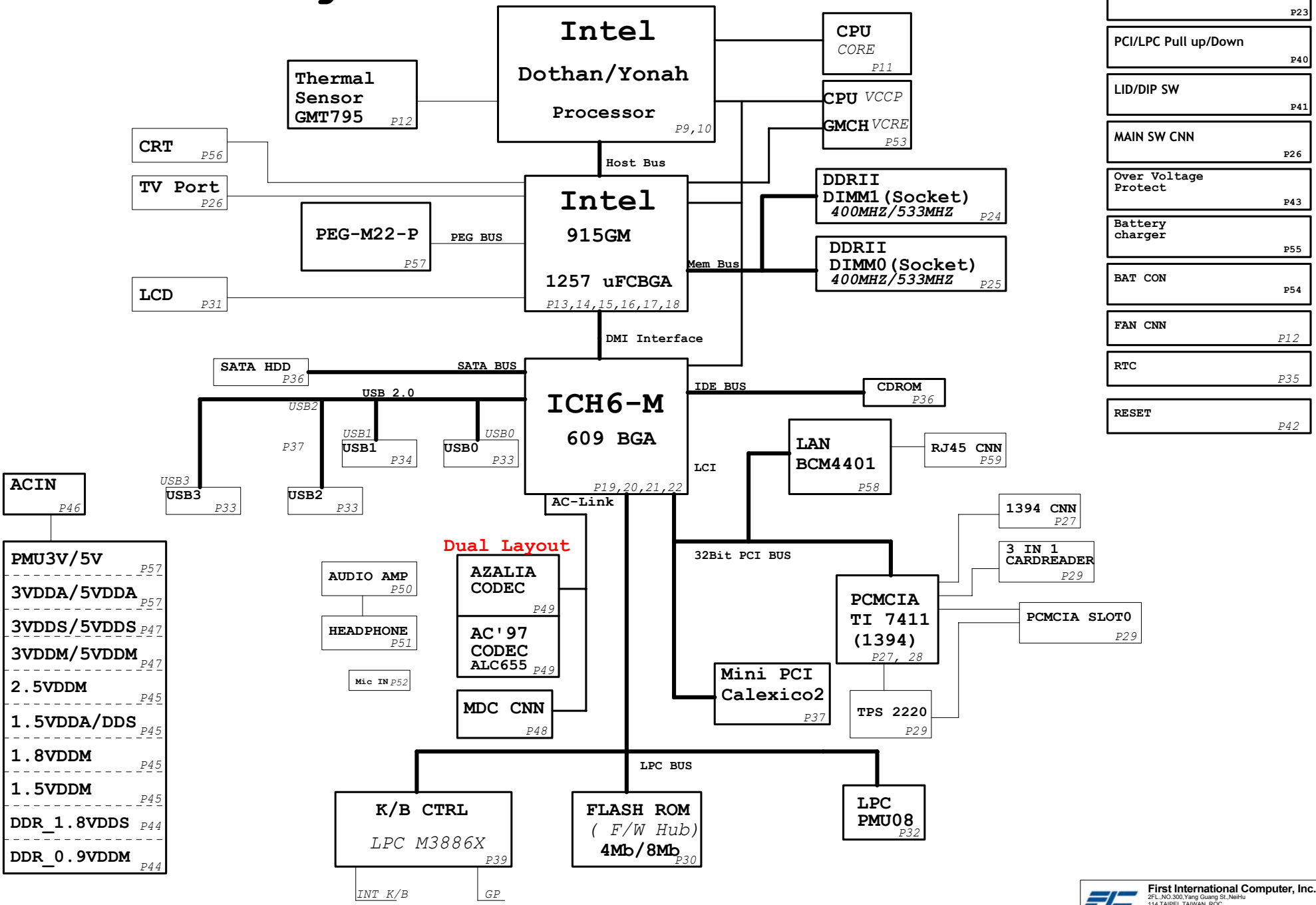
3. Block Diagram :



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4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage 1.468V~0.956V for CPU
VCCP	1.05V for AGTL+ Termination Voltage
Vcore_MGCH	1.05V or 1.5V for ALVISO core
1.8VDDM	1.8V for CPU PLL Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDM	2.5V power rail for GMCH GIO
DDR_1.8VDDS	1.8V power rail for DDRII
DDR_0.9VDDM	0.9V DDRII Termination Voltage

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(High Speed)
Layer 4		Stripline Layer(High Speed)
Layer 5		Power Plane
Layer 6		Stripline Layer(High Speed)
Layer 7		Ground Plane
Layer 8		Solder Side,Microstrip signal Layer

Layers : 8 Depth 1.2mm Impence 55 ohms +/- 10%

POWER RAIL	DESTINATION	VOLTAGE	S0 CURRENT
VCORE_CPU	Dothan	0.956~1.308V	27A
VCCP	Dothan	1.05V	2.5A
VCCP_MGCH	ALVISO	1.05V	0.85A
VCORE_MGCH	ALVISO	1.05V	4A
1.8VDDM/1.5VDDM	Dothan (PLL)	1.8V	0.2A
DDR_1.8VDDS	ALVISO (DDR2) DDR2 MODULE	1.8V	2.7A
1.5VDDM	ALVISO (LVDS, TVDAC,PCIE)(VCCASM) ICH6M (CORE)(PLL)(DMI)	1.5V	1.8A 2.95A
1.5VDDS	ICH6M (SUS/LAN)	1.5V	
1.5VDDA	ICH6M (SUS)	1.5V	
2.5VDDM	ALVISO (PCIE_A,LVDSIO,CRTDAC,HV)	2.5V	0.15A
0.9VDDM	DDR RAM	0.9V	
3VDDM	ICH6M (IO) ALVISO (TV DAC) TI4510 MiniPCI FWH BIOS LPC KBC AC97 CODEC CLK GEN LVDS	3.3V	0.2A 0.13A 0.6A (Evaluation) 0.024A (Evaluation) 0.0461A (Idle) 0.36A 0.4A
3VDDS	TI4510 MiniPCI PCMCIA VCCA	3.3V	0.36A
3VDDA	ICH6M (SUS)	3.3V	0.4A
5VDDM	AMP2020 CDROM HDD INT KB/ INT MS INVERTER		0.0615A (Idle) 0.338A (Run) 0.0461A (Idle) 0.677~0.8A(Run) 0.0461A (Idle) 0.52A (Run) 0.0615A (Idle) 0.569A (Run)
5VDDS	PCMCIA VCCA		
5VDDA	ICH6M USB		7mA
PMU3V	PMU08		0.0615A
PMU5V	PMU08		0.0615A

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6.Schematic modify Item and History :

	BUG	ROOT CAUSE	SOLUTION	PHASE IN
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				

HISTORY:

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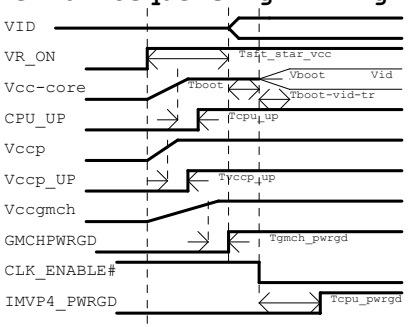
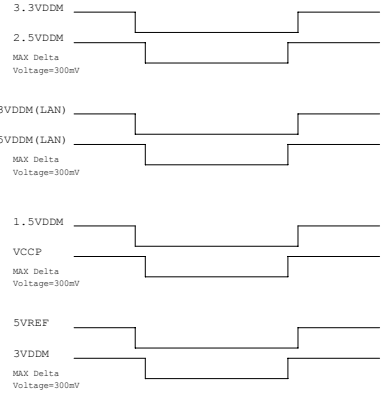
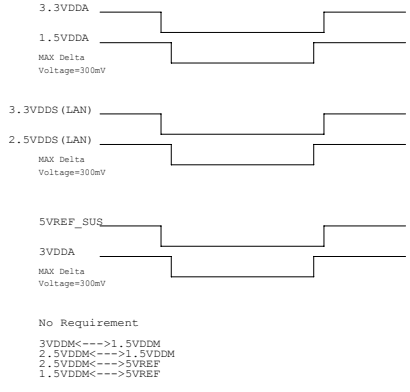
7. power on & off & S3 Sequence :

Power On Sequencing Timing Diagram

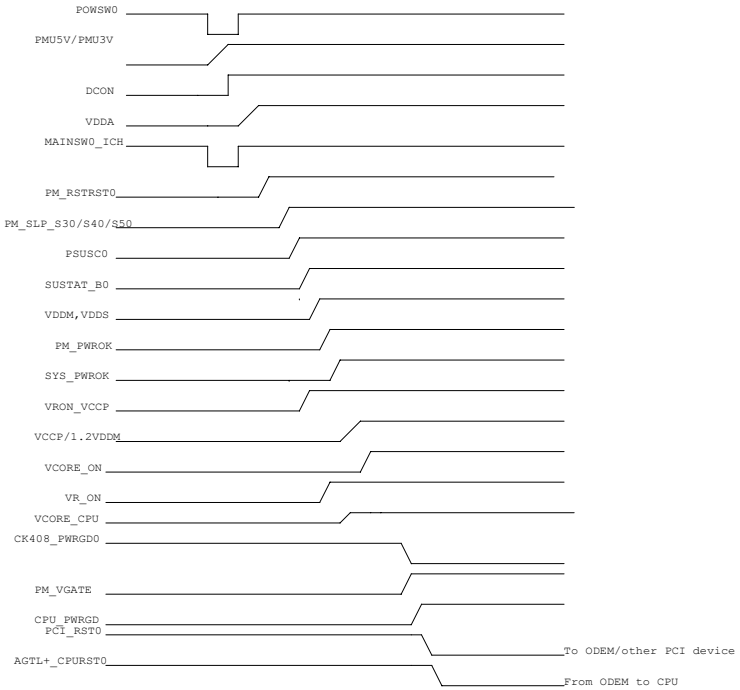


ICH6M Timing

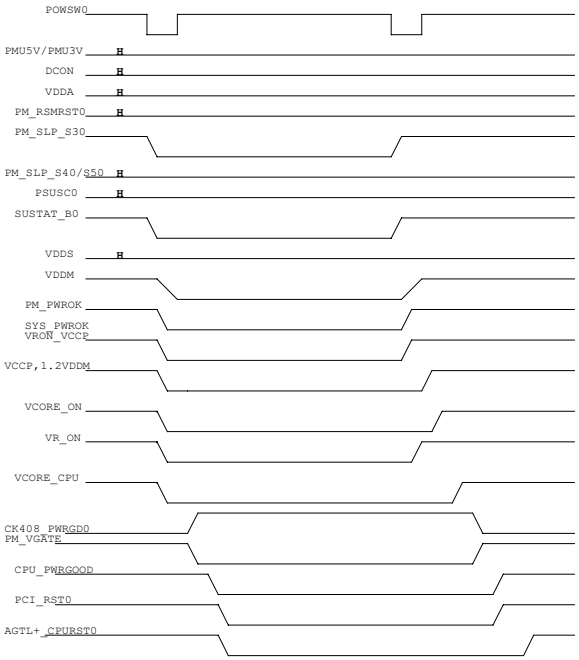




BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



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Size: C | Document Number: Timing Diagram | Rev: 0.1

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8. Layout Guideline :

System Bus Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer) Micro-strip(Ext. Layer)	1.0 ~ 6.5 inch	55+/-10%	4 & 8(Int. Layer) 5 & 10(Ext. Layer)

Source Synchronous DATA :

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

Topology1:

DATA#[63..0] , DINV#[3..0] , DSTBN#[3..0] , DSTBP#[3..0]						
Signal Names	Transmission Line Type	Total Trace Length		Normal Impedance	Spacing (mils)	
		Min (inches)	Max (inches)		Data to Data Strobe to Strobe	Strobe to Data
DATA#[63..0]	Strip-line	0.5	5.5	55+/-10%	4 & 8	NA
DINV#[3..0]	Strip-line	0.5	5.5	55+/-10%	4 & 8	NA
DSTBN#[3..0]	Strip-line	0.5	5.5	55+/-10%	4 & 12	4 & 8
DSTBP#[3..0]	Strip-line	0.5	5.5	55+/-10%	4 & 12	4 & 8

NOTE: No trace witdth to trace space ratio requirement relaxation allowedcomplementary strobes.
The only recommended trace spacing ratio is 3:1

Topology2:

DATA#[63..0] , DINV#[3..0] , DSTBN#[3..0] , DSTBP#[3..0]						
Signal Names	Transmission Line Type	Total Trace Length		Normal Impedance	Spacing (mils)	
		Min (inches)	Max (inches)		Data to Data Strobe to Strobe	Strobe to Data
DATA#[63..0]	Strip-line	0.5	3.0	55+/-10%	4 & 6	NA
DINV#[3..0]	Strip-line	0.5	3.0	55+/-10%	4 & 6	NA
DSTBN#[3..0]	Strip-line	0.5	3.0	55+/-10%	4 & 12	4 & 6
DSTBP#[3..0]	Strip-line	0.5	3.0	55+/-10%	4 & 12	4 & 6

NOTE: No trace witdth to trace space ratio requirement relaxation allowedcomplementary strobes.
The only recommended trace spacing ratio is 3:1

Topology3:

DATA#[63..0] , DINV#[3..0] , DSTBN#[3..0] , DSTBP#[3..0]						
Signal Names	Transmission Line Type	Total Trace Length		Normal Impedance	Spacing (mils)	
		Min (inches)	Max (inches)		Data to Data Strobe to Strobe	Strobe to Data
DATA#[63..0]	Strip-line	0.5	5.5	55+/-10%	4 & 8	NA
DINV#[3..0]	Strip-line	0.5	5.5	55+/-10%	4 & 8	NA
DSTBN#[3..0]	Strip-line	0.5	5.5	55+/-10%	4 & 12	4 & 8
DSTBP#[3..0]	Strip-line	0.5	5.5	55+/-10%	4 & 12	4 & 8

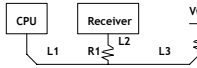
NOTE: No trace witdth to trace space ratio requirement relaxation allowedcomplementary strobes.
The only recommended trace spacing ratio is 3:1

Source Synchronous ADDRESS :

Address#[31..3] , REQ#[4..0] , ADSTB#[1..0]			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	0.5 ~ 6.5 inch	55+/-10%	4 & 8

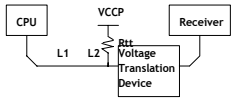
Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17	+/- 200 mils	ADSTB1#	+/- 200 mils

Topology : IERR# , FERR#



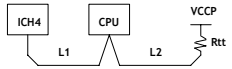
L1	L2	L3	R1	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Strip-line

Topology : PROCHOT#



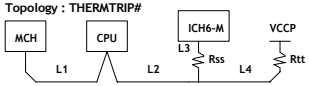
L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line

Topology : PWRGOOD



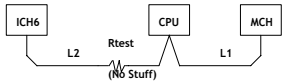
L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	330 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	330 +/-5%	Strip-line

Topology : THERMTRIP#



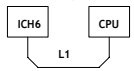
L1	L2	Rtt	Rss	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	75 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	75 +/-5%	Strip-line

Topology : CPUSLP#



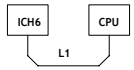
L1	L2	Rtest	Transmission Line
0.5" - 12"	0.5" -12.0"	0	Micro-strip
0.5" - 12"	0.5" - 12.0"	0	Strip-line

Topology : LINT1 / NMI , LINT0 / INTR , A20M# , IGNNE# , DPSLP# , SMI# , STPCLK#



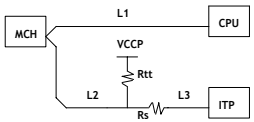
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPU RESET# without ITP



L1	Transmission Line
1" - 6.5"	Micro-strip
1" - 6.5"	Strip-line

Topology : CPU RESET# with ITP



L1	L2 + L3	L3	Rs	Rtt
1.0" - 6.0"	6.0" max	0.5" max	22.6 +/-1%	54.9 +/-1%

Differential Impedance Targets for Routing :

Signal Type	Routing Geometry	Impedance	Signal Matching
Host Clock	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 20 mils
DMI	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 5 mils
EXT-PCI	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 20 mils
SDVO	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 20 mils
LVDS	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 20 mils
SATA	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 10 mils
USB2.0	4 -mil trace width on 7- mil spacing	90 Ω +/- 15 %	+/- 75 mil
PCI EXPRESS	5 -mil trace width on 7- mil spacing	100 Ω +/- 15 %	+/- 37 mils
DDR2	5 -mil trace width on 7- mil spacing	85 Ω +/- 15 %	+/- 20 mil

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ALVISO DDR2 Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

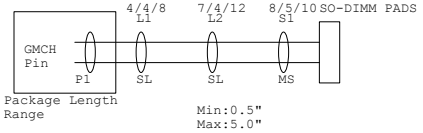
DDR2 Signal Groups

Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SA_DQ[63:0] ; SB_DQ[63:0] SA_DQS[7:0] ; SA_DQS[7:0] SA_DM[7:0] ; SB_DM[7:0]
Control	SCKE[3:0] SCS#[3:0] SM_ODT[3:0]
Command	SA_MA[13:0] ; SB_MA[13:0] SA_BA[1:0] ; SB_BA[1:0] SA_RAS# ; SB_RAS# SA_CAS# ; SB_CAS# SA_WE# ; SB_WE#
Compensation	SMRCOMPN ; SMRCOMPP SMSLEWIN ; SMSLEWOUT SMVREF[1:0]
Feedback	SA_RCVENOUT# ; SB_RCVENOUT# SA_RCVENIN# ; SB_RCVENIN#

Length Matching Formulas

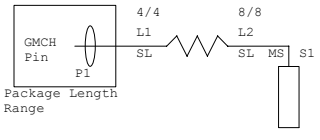
Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerence within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 10 mils
Minimum Pair to Pair Spacing : ? mils
Minimum Spacing to other DDR Signals : 12 mils
Minimum Spacing to other non-DDR Signals : 20 mils
Trace Length L1 : Max 0.5", S1 : Max 200 mils
Total Length --L1+L2+S1: Min 0.5" , Max 5.0"

Data Signals Topologies and Routing Guidelines

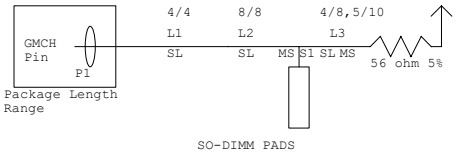


Minimum Spacing to other DDR Signals : 12 mils
Minimum Spacing to other non-DDR Signals : 20 mils
Trace Width : 4mils
- inner layerL2 Segment : 4 mils,Total Length < /= 3000 mils
- inner layerL2 Segment : 8 mils,Total Length > 3000 mils
- outer layerL2 Segment : 5 mils

Trace Spacing : 6mils
- inner layerL2 Segment : 6 mils,Total Length < /= 3000 mils
- inner layerL2 Segment : 8 mils,Total Length > 3000 mils
- outer layerL2 Segment : 10 mils

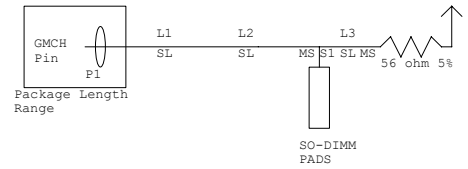
Total Length --L1+L2+S1: Min 0.5" , Max 4.5"
Trace Length L1 : Max 0.5", S1 : Max 200 mils
DQ/DM to DQSLength Matching : +/- 10 mils

Control Signals Topologies and Routing Guidelines



Minimum CTRL trace Spacing : 8 mils
Minimum Spacing to other DDR Signals : 12 mils
Minimum Spacing to other non-DDR Signals : 20 mils
Trace Length L1 : Max 0.5"
L3 : Max 1.5"
Total Length --L1+L2+S1: Min 0.5" , Max 4.5"
CTRL to SCK/SCK# Length Matching : (CTRL-1.5")
</= CTRL </= (CLK 1.0")

Command Signals Topologies and Routing Guidelines



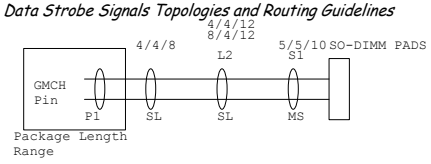
Minimum Spacing to other DDR Signals : 12 mils
Minimum Spacing to other non-DDR Signals : 20 mils
Trace Width : 4mils
- inner layerL2 Segment : 4 mils,Total Length < /= 3000 mils
- inner layerL2 Segment : 8 mils,Total Length > 3000 mils
- outer layerL2 Segment : 5 mils

Trace Spacing : 6mils
- inner layerL2 Segment : 6 mils,Total Length < /= 3000 mils
- inner layerL2 Segment : 8 mils,Total Length > 3000 mils
- outer layerL2 Segment : 10 mils

Total Length --L1+L2+S1: Min 0.5" , Max 4.5"
Trace Length L1 : Max 0.5", S1 : Max 200 mils
Trace Length L3 : Max 1.5"

Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.5" , Max : Clock -1.0"

Data Strobe Signals Topologies and Routing Guidelines

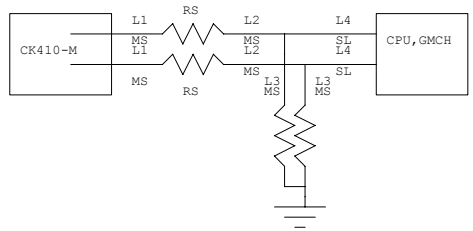


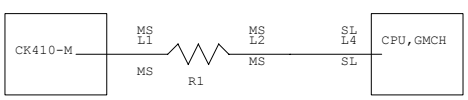
Minimum Spacing to other DDR Signals : 12 mils
Minimum Spacing to other non-DDR Signals : 20 mils
Trace Width : 4mils
- inner layerL2 Segment : 4 mils,Total Length < /= 3000 mils
- inner layerL2 Segment : 8 mils,Total Length > 3000 mils
- outer layerL2 Segment : 5 mils

DQS to DQS# Spacing : 4mils
- outer layerL2 Segment : 5 mils

Minmun DQS to DQ Spacing :
- inner layerL2 Segment : 6 mils,Total Length < /= 3000 mils
- inner layerL2 Segment : 8 mils,Total Length > 3000 mils
- outer layerL2 Segment : 10 mils

Total Length --L1+L2+S1: Min 0.5" , Max 4.5"
Trace Length L1 : Max 0.5", S1 : Max 200 mils





Length Matching : DQS to SCK/SCK#
(Clock - 1.0") </= DQS </= (Clock + 0.5")

CLOCKS	LENGTH	TRACE / SPACE	TRACE MUTCHING	Rs	Rt	IMPEDANCE	SKEW	NOTES
HCLKCPU[1..0] **HCLKNB[1..0]** **HCLKITP[1..0]**	L1 : Max 0.5" L2 : Max 200mils L3 : Max 0.5" L4 : Min 2" Max 8 "	**4 / 7 mils**	L1+/L1- : +/- 10 mils L2+/L2- : +/- 10 mils L3+/L3- : +/- 10 mils L1+L2+L3 /L1- + L2- + L3- : +/- 10 mils L4+/L4- : 200 +/- 10 mils (for PGA Topology) L4+/L4- : 500 +/- 10 mils (for BGA Topology)	33 ohms +/- 5%	49.9 ohms +/- 1%	100 ohms +/- 15% differential mode 55 ohms +/- 15% single mode	350ps Total Budget 100ps for flight skew 100ps for pin to pin skew 150ps for jitter	Differentials pairs with the same length 1.(within 10 mil) 2.CPU & NB trace mismatch within 450 mil * 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
SRC CLK	L1 : Max 0.5" L2 : Max 200mils L3 : Max 200 mils L4 : Min 200 mils Max 12"	**4 / 7 mils 50 mils (spacing to other)**	L1+L2+L4 /L1- + L2- + L4- : +/- 25 mils	22 ohms +/- 5% to 33 ohms +/- 5%	49.9 ohms +/- 1%	55 ohms +/- 15%	NA	1.Making PCI length with minimum various **2.Max skew = 1ns**
DOT CLK	L1 : Max 0.5" L2 : Max 200mils L3 : Max 200 mils L4 : Min 4" Max 10"	**4 / 7 mils 25 mils (spacing to other)**	+/- 10 mils	33 ohms +/- 5%	49.9 ohms +/- 1%	100 ohms +/- 15%		

CLOCKS	LENGTH	TRACE / SPACE	TRACE MUTCHING	R1	Rt	IMPEDANCE	SKEW	NOTES
USB (48MHZ) **CLK**	L1 : Max 0.5" L2 : Min 2" Max 20"	**4 mils (stripline)** **20 mils (spacing to other)**	NA	33 ohms +/- 5%		55 ohms +/- 15%	NONE	
PCI/PCIF **CLK** **PCLKICH** **PCLKFWH** **PCLKSIO** **PCLKLAN**	L1 : Max 0.5" L2 : Min 2" Max 20" L2 : Z +(0" to 10") ,Max 20" L2 : Z +(0" to 6") ,Max 20"	**4 mils (stripline)** **10 mils (spacing to other)**	NA	12.1 ohms +/- 1% 33 ohms +/- 5%		55 ohms +/- 15%	NONE	
14MCLK_SIO **14MCLK_ICH** **14MCLK_AC97**	L1 : Max 0.5" L2 : Max 18"	**4 mils (stripline)** **10 mils (spacing to other)**	(L1+L2) to ICH6-M must be within 500 nils to (L1+L2) to SIO/AC97	12.1 ohms +/- 1%		55 ohms +/- 15%		

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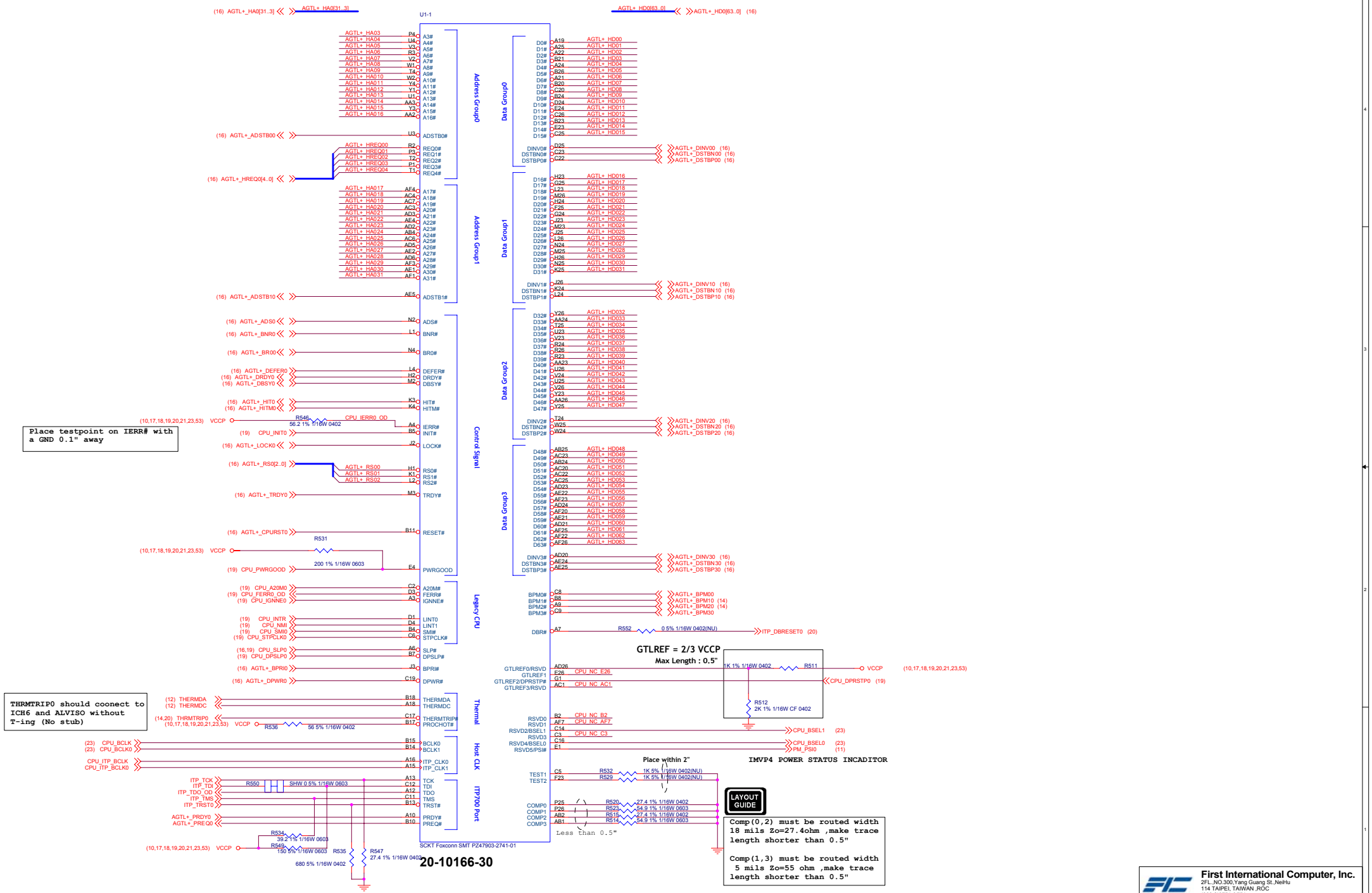
Title: **AT11 < Dothan + 915GM + ICH6-M >**

Size: C | Document Number: **DDRII/CLK Gen Layout Guideline** | Rev: 0.1

Date: Wednesday, February 16, 2005 | Sheet 8 of 63



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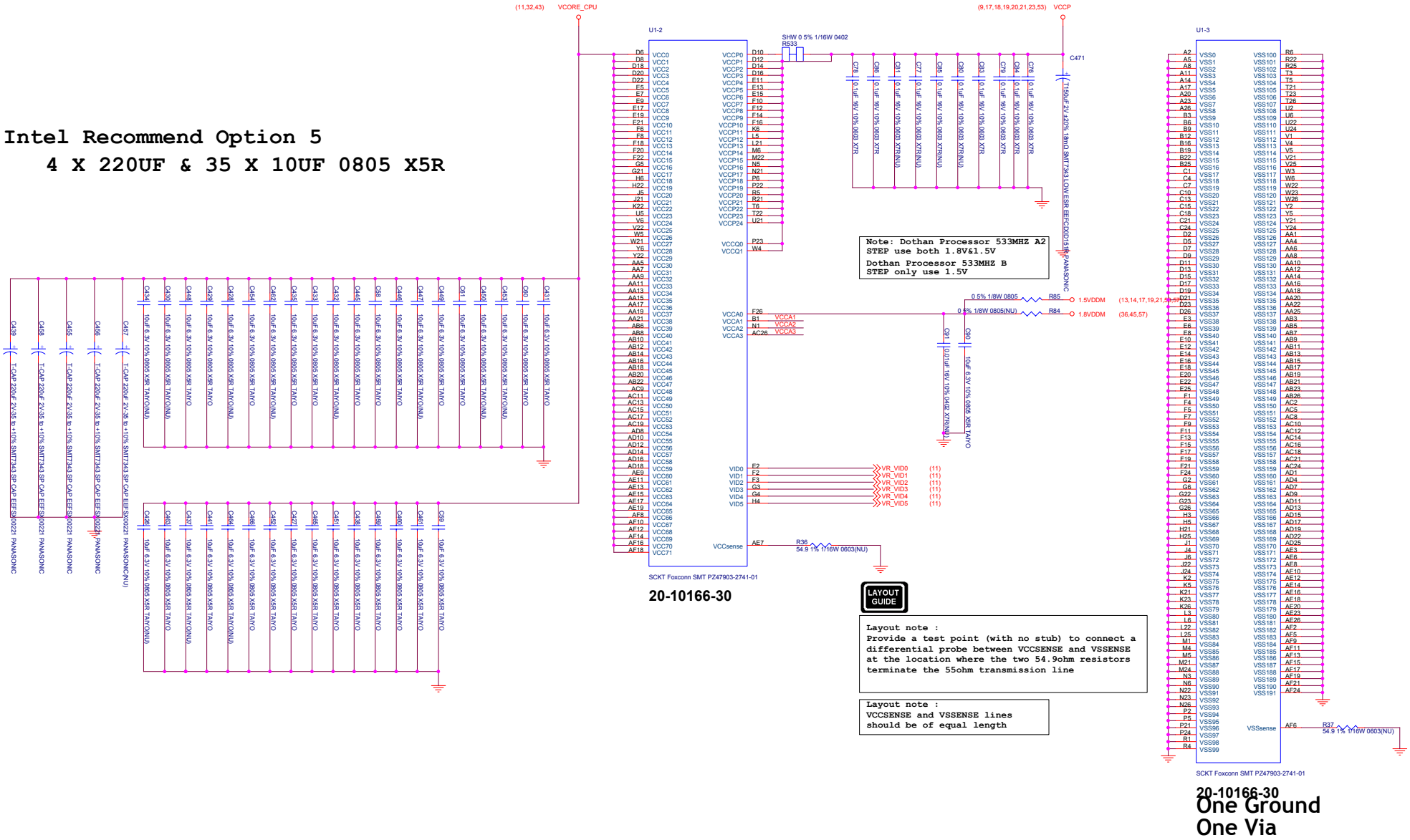
Title	AT11 < Dothan + 915GM + ICH6-M >
Size C	Document Number CPU (Dothan) 1/2 Rev 0.1
Date: Thursday, April 14, 2005	Sheet 9 of 63



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Title	AT11 < Dothan + 915GM + ICH6-M >	
Size C	Document Number CPU (Dothan) 2/2	Rev 0.1
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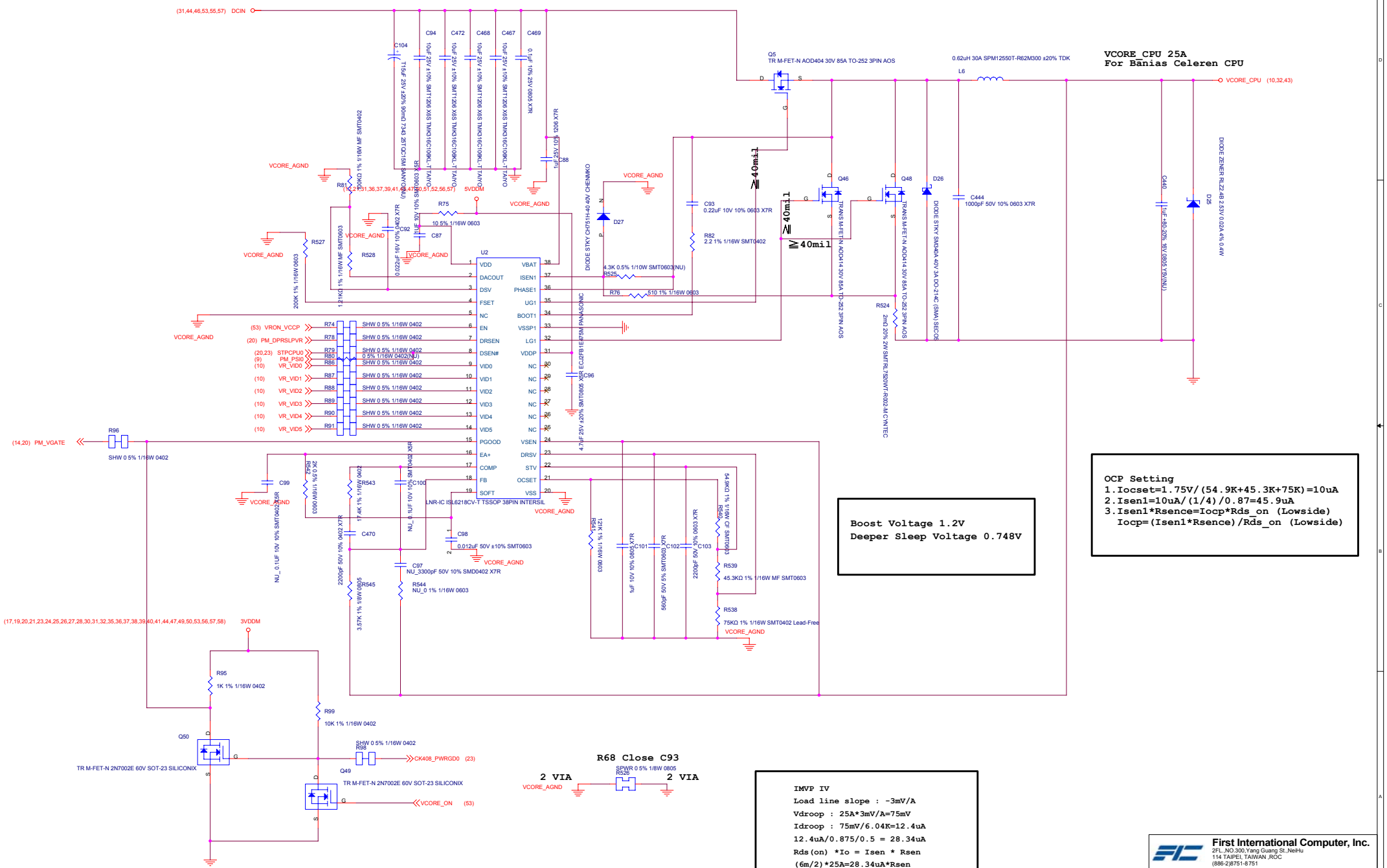
VCORE_CPU



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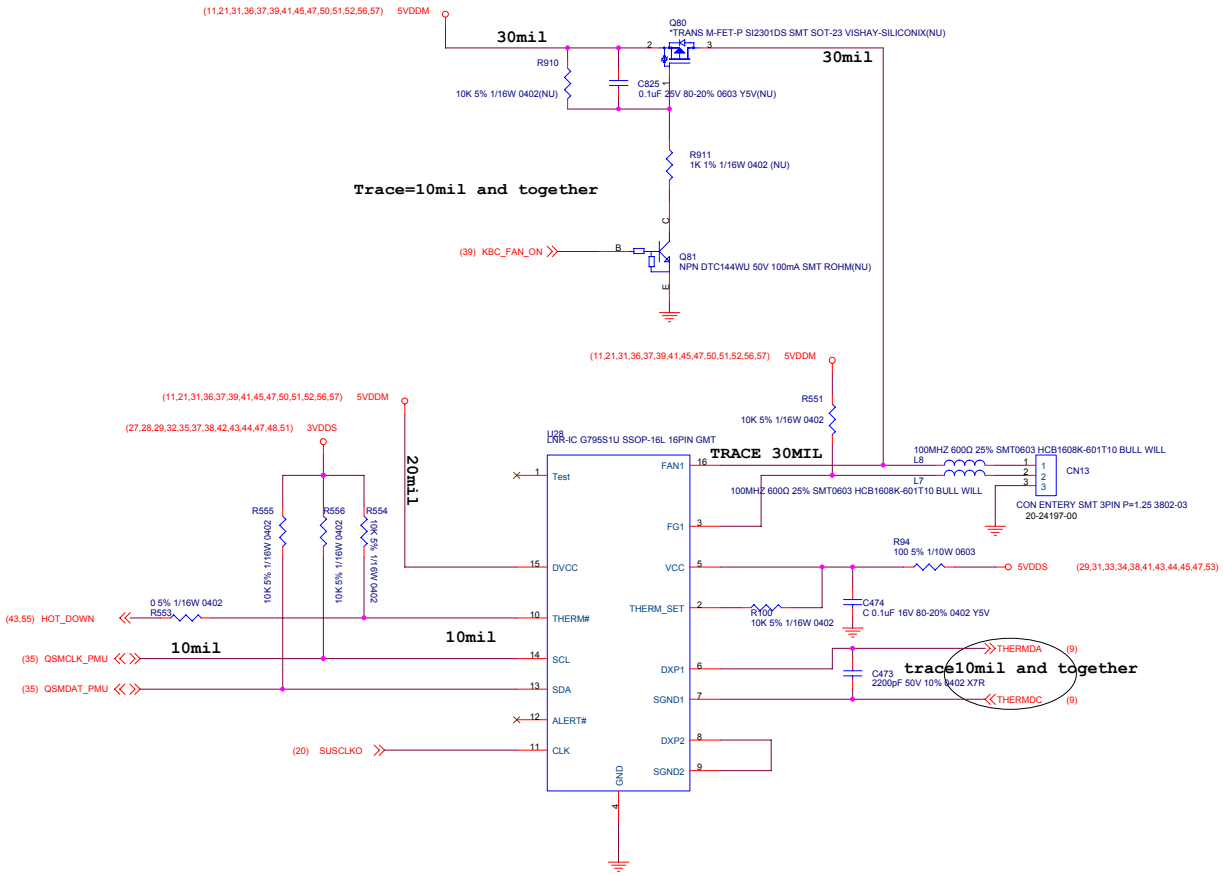
Size C	Document Number Vcore	Rev 0.1
Date: Thursday, April 14, 2005	Sheet 11 of 63	

THERMAL SENSOR



LAYOUT GUIDE

1.Far away the CRT,clock generator,memory bus,PCI bus.
2.As close CPU as possible.

	10 mil	GND
10 mil	MINIMUM	THERMDA
10 mil	10 mil	THERMDC
		GND

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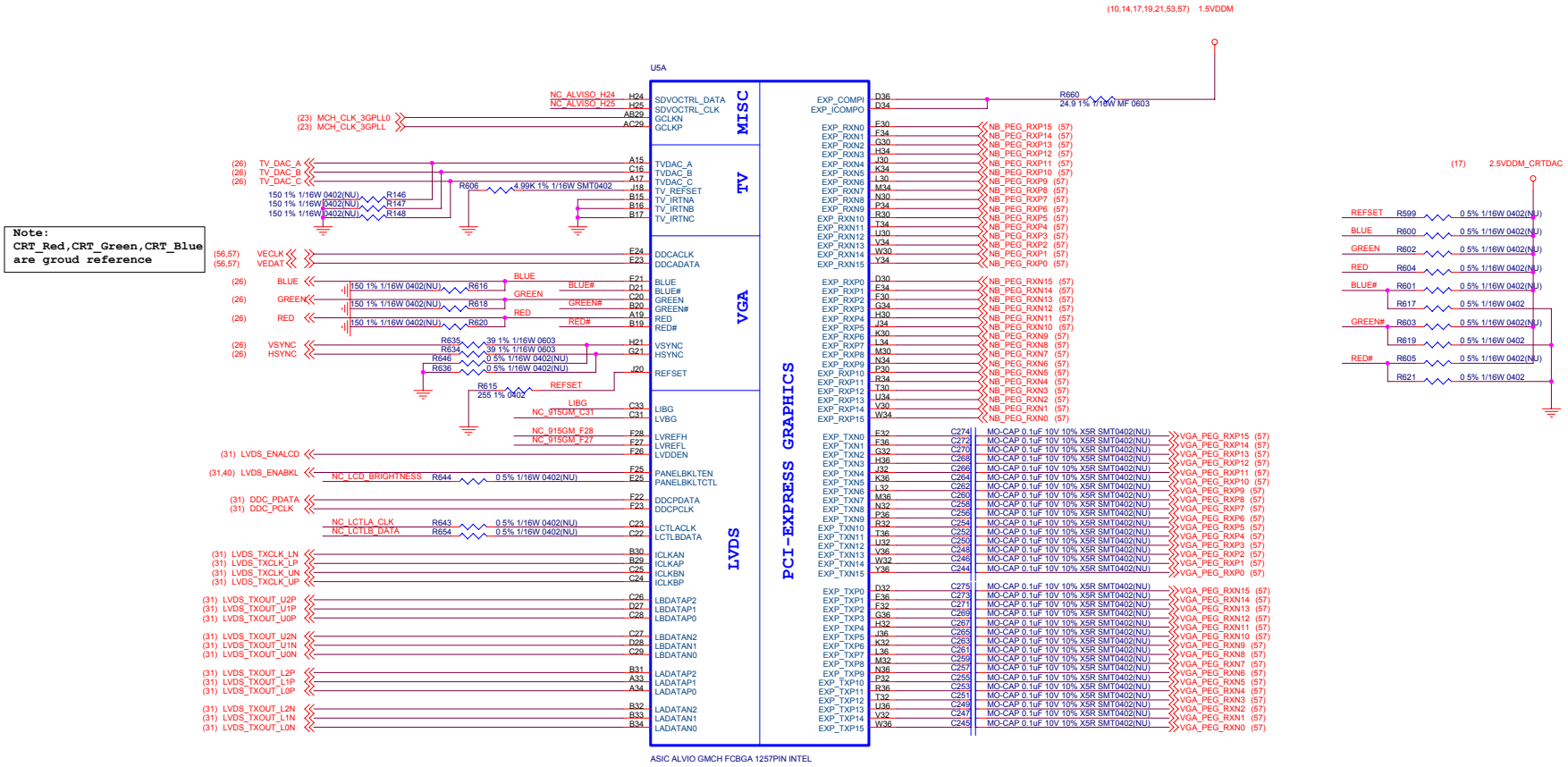
Title: AT11 < Dothan + 915GM + ICH6-M >		
Size: C	Document Number: Thermal / FAN CNN	Rev: 0.1
Date: Thursday, April 14, 2005	Sheet 12 of 63	



PM BOM:

R606, R146, R147, R148	0ohm 0402
R616, R618, R620	(NU)
R599, R600, R602, R604	0ohm 0402
R601, R603, R605	0ohm 0402
R617, R619, R621, R615	(NU)
R658	(NU)

GM BOM:

R146, R147, R148	150ohm 1%
R606	4.99K 1%
R599, R600, R602, R604	(NU)
R601, R603, R605	(NU)
R617, R619, R621	0ohm 0402
R634, R635	39ohm 1%
R636, R646	(NU)
R616, R618, R620	150ohm 1%
R658	1.5Kohm 1%

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Title: AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	ALVISO(LVDS/PCIE/VGA/TV/MISC)	0.1

Date: Thursday, April 14, 2005 Sheet 13 of 63

For ITP Port used only

AGTL+_BPM20 (9)
AGTL+_BPM10 (9)

(16,17,18) VCCP_GMCH

R572 10K 5% 1/16W 0402

R563 0 5% 1/16W 0402(NU)

R564 0 5% 1/16W 0402(NU)

MCH_BSEL1 (23)
MCH_BSEL0 (23)

CFG[2:0] 10k ohms pull up or pull down or direct connect form processor

U5B

(19) DMI_TXN[3..0]
DMI_TXN0 AA31
DMI_TXN1 AB35
DMI_TXN2 AC31
DMI_TXN3 AD35

(19) DMI_TXP[3..0]
DMI_TXP0 Y31
DMI_TXP1 AA35
DMI_TXP2 AB31
DMI_TXP3 AC35

(19) DMI_RXN[3..0]
DMI_RXN0 AA33
DMI_RXN1 AB37
DMI_RXN2 AC33
DMI_RXN3 AD37

(19) DMI_RXP[3..0]
DMI_RXP0 Y33
DMI_RXP1 AA37
DMI_RXP2 AB33
DMI_RXP3 AC37

DMI

DMIRXN0
DMIRXN1
DMIRXN2
DMIRXN3

DMIRXP0
DMIRXP1
DMIRXP2
DMIRXP3

DMITXN0
DMITXN1
DMITXN2
DMITXN3

DMITXP0
DMITXP1
DMITXP2
DMITXP3

CFG/RSVD

CFG0 G16
CFG1 H13
CFG2 G14
CFG3 F16
CFG4 F15
CFG5 G15
CFG6 E16
CFG7 D17
CFG8 J16
CFG9 D15
CFG10 E15
CFG11 D14
CFG12 E14
CFG13 H12
CFG14 C14
CFG15 H15
CFG16 J15
CFG17 H14
CFG18 G22
CFG19 G23
CFG20 D23
RSVD21 G25
RSVD22 G24
RSVD23 J17
RSVD24 A31
RSVD25 A30
RSVD26 D26
RSVD27 D25

T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T23 T24 T25 T26 T27 T28

C497 MO-CAP 0.1uF 10V 10% X5R SMT0402

INTEL SUGGESTED

GM BOM:
R1519, R1520, R1521, R1522 (NU)

PM BOM:
R1519, R1520, R1521, R1522 0ohm 0402

(10,13,17,19,21,53,57) 1.5VDDM

MCH_SSCLK
MCH_DREFCLK

R641 0 5% 1/16W 0402(NU)
R642 0 5% 1/16W 0402(NU)

DDR MUXING

(24) MGH_SMCLK_DDR0 AM33
(24) MGH_SMCLK_DDR1 AL1
NC_ALVISO_AE11 AE11
(25) MGH_SMCLK_DDR3 AJ34
(25) MGH_SMCLK_DDR4 AF6
NC_ALVISO_AC10 AC10

SM_CK0
SM_CK1
SM_CK2
SM_CK3
SM_CK4
SM_CK5

(24) MGH_SMCLK_DDR00 AN33
(24) MGH_SMCLK_DDR10 AK1
NC_ALVISO_AE10 AE10
(25) MGH_SMCLK_DDR30 AJ33
(25) MGH_SMCLK_DDR40 AF5
NC_ALVISO_AD10 AD10

SM_CK0#
SM_CK1#
SM_CK2#
SM_CK3#
SM_CK4#
SM_CK5#

(24) MGH_SM_CKE0 AP21
(24) MGH_SM_CKE1 AM21
(25) MGH_SM_CKE2 AH21
(25) MGH_SM_CKE3 AK21

SM_CKE0
SM_CKE1
SM_CKE2
SM_CKE3

(24) MGH_SM_CS00 AN16
(24) MGH_SM_CS10 AM14
(24,25) MGH_SM_CS20 AH15
(25) MGH_SM_CS30 AG16

SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#

M_OCDCOMP0 AF22
M_OCDCOMP1 AF16

SM_OCDCOMP0
SM_OCDCOMP1

(24) MCH_ODT0 AP14
(24) MCH_ODT1 AL15
(25) MCH_ODT2 AM11
(25) MCH_ODT3 AN10

SM_ODT0
SM_ODT1
SM_ODT2
SM_ODT3

MGH_RCOMP0 AK10
MGH_RCOMP AK11

SMRCOMPN
SMRCOMPP

(24,25,41) DDR_VREF AF37
AD1

SMVREF0
SMVREF1

MGH_SMXSLEW AE27
AE28

SMXSLEWIN
SMXSLEWOUT

MGH_SMYSLEW AF9
AE10

SMYSLEWIN
SMYSLEWOUT

R624 40.2 1% 1/16W 0603

R625 40.2 1% 1/16W 0603

Laout note:
Route as short as possible

Laout note:
Route as short as possible

PM

BM_BUSY# J23
EXT_TS0# J21
EXT_TS1# H22
THRMTRIP# F5
PWROK AD30
RSTIN# AE29

PM_EXTTS00
PM_EXTTS10

PM_BMBUSY0 (20)
PM_EXTTS00
THRMTRIP0 (9,20)
PM_VGATE (11,20)
PLT_RST0 (19,30,36,57)

R664 100 1% 1/16W 0402

CLKS

DREFCLKN A24
DREFCLKP A23
DREF_SSCLKN C37
DREF_SSCLKP D37

MCH_DREFCLK0 (23)
MCH_DREFCLK (23)
MCH_SSCLK0 (23)
MCH_SSCLK (23)

MCH_DREFCLK0
MCH_SSCLK0

R633 0 5% 1/16W 0402(NU)
R640 0 5% 1/16W 0402(NU)

NC

NC0 AP37 NC_ALVISO_AP37
NC1 AN37 NC_ALVISO_AN37
NC2 AP36 NC_ALVISO_AP36
NC3 AP2 NC_ALVISO_AP2
NC4 AP1 NC_ALVISO_AP1
NC5 AN1 NC_ALVISO_AN1
NC6 B1 NC_ALVISO_B1
NC7 A2 NC_ALVISO_A2
NC8 B37 NC_ALVISO_B37
NC9 A36 NC_ALVISO_A36
NC10 A37 NC_ALVISO_A37

ASIC ALVIO GMCH FCBGA 1257PIN INTEL

(17,21,31,45,56,57) 2.5VDDM

R656 10K 5% 1/16W 0402 PM_EXTTS00
R657 10K 5% 1/16W 0402 PM_EXTTS10

CFG5

CFG5	LOW=DMIx2 HIGH=DMIx4

R570 2.2K 5% 1/16W 0402(NU)

CFG6

R145 2.2K 5% 1/16W 0402

CFG6 (DDR Strap) LOW=DDR2 NC=DDR

CFG16

R595 2.2K 5% 1/16W 0402(NU)

(17,21,31,45,56,57) 2.5VDDM

CFG18 (VCC_SEL)	LOW=1.05V HIGH=1.5V

R655 1K 5% 1/16W 0402(NU)

CFG18

(17,24,43,44,45) DDR_1.8VDDS

R565 80.6 1% 0603

MGH_RCOMP0

MGH_RCOMP

R566 80.6 1% 0603

CFG7

CFG9 PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation

R162 2.2K 5% 1/16W 0402(NU)

CFG9

R571 2.2K 5% 1/16W 0402

CFG16 (FSB Dynamic ODT)	LOW=DT/Transportable CPU HIGH=Mobile CPU

CFG7 (CPU Strap)	LOW=DT/Transportable CPU HIGH=Mobile CPU

(17,21,31,45,56,57) 2.5VDDM

CFG19 (VTT SEL)	LOW=1.05V HIGH=1.2V

R645 1K 5% 1/16W 0402(NU)

CFG19

CFG[17:3] have internal pullup resistors
CFG[19:18] have internal pulldwon resistors

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Title: AT11 < Dothan + 915GM + ICH6-M >

Size: C | Document Number: ALVISO(DMI/CLK/PM) | Rev: 0.1

Date: Thursday, April 14, 2005 | Sheet 14 of 63

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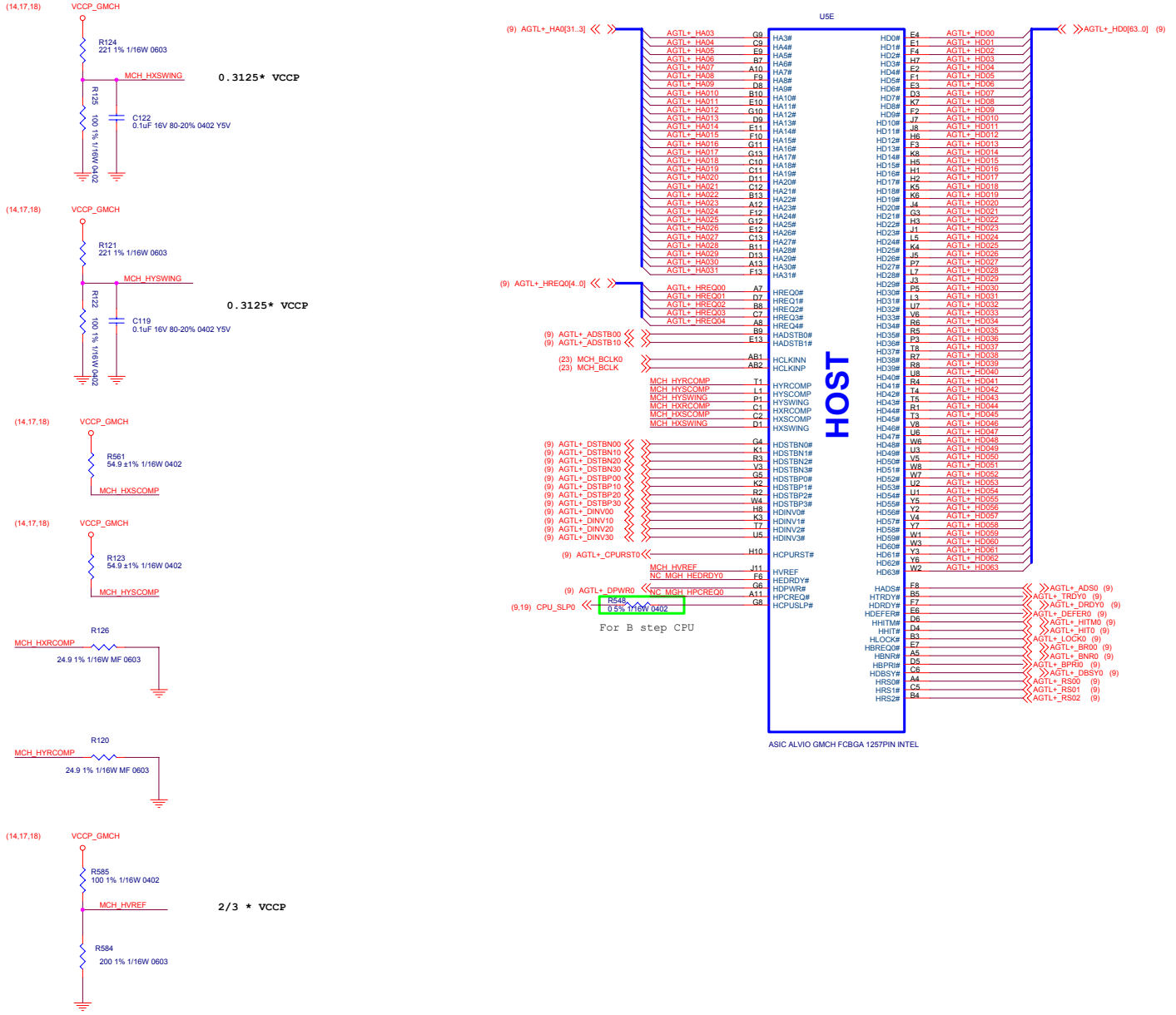
Title

AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	ALVISO(DUAL DDR)	0.1

Date: Thursday, April 14, 2005 Sheet 15 of 63



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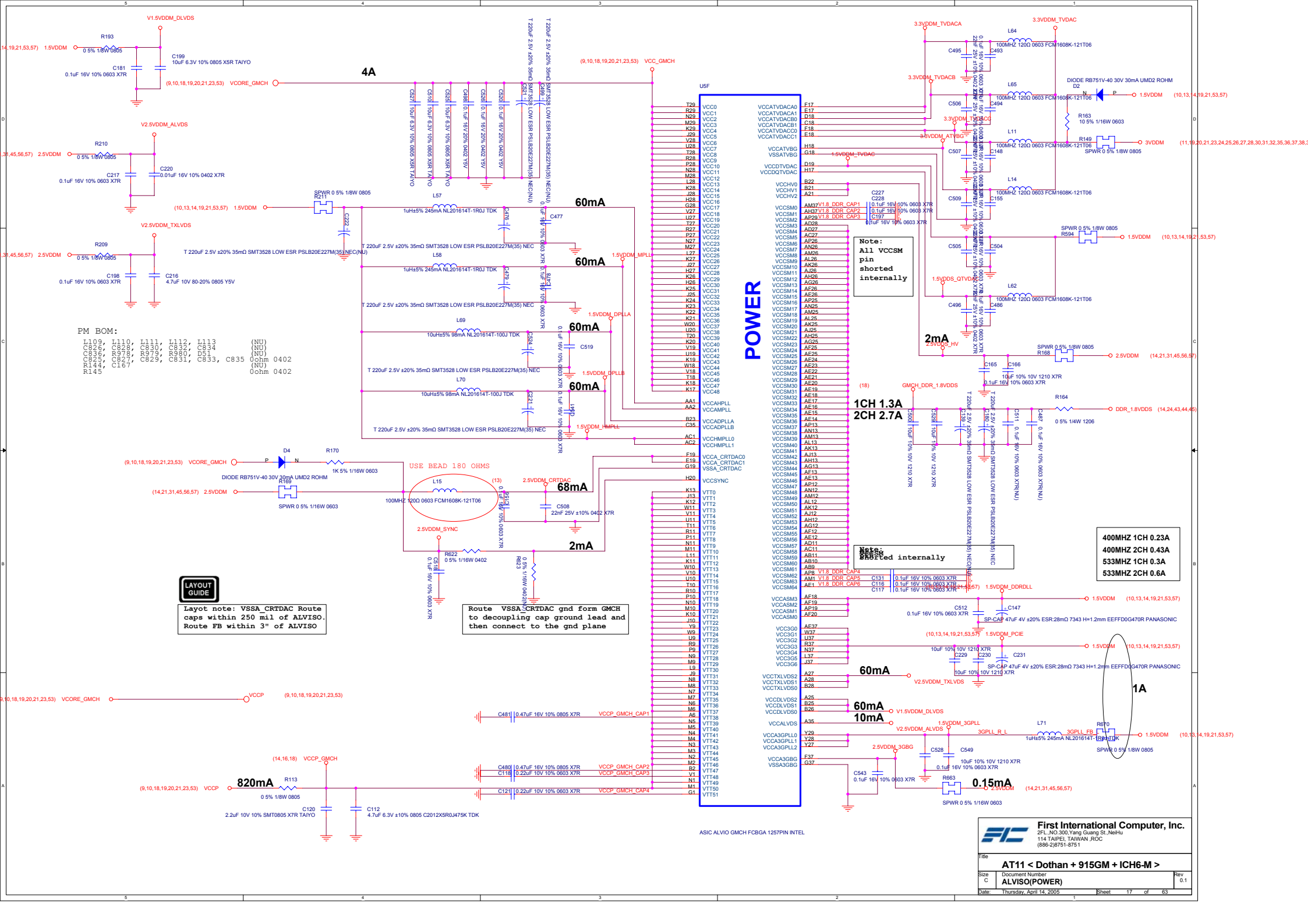
Title

AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	ALVISO(HOST)	0.1

Date: Thursday, April 14, 2005 Sheet 16 of 63



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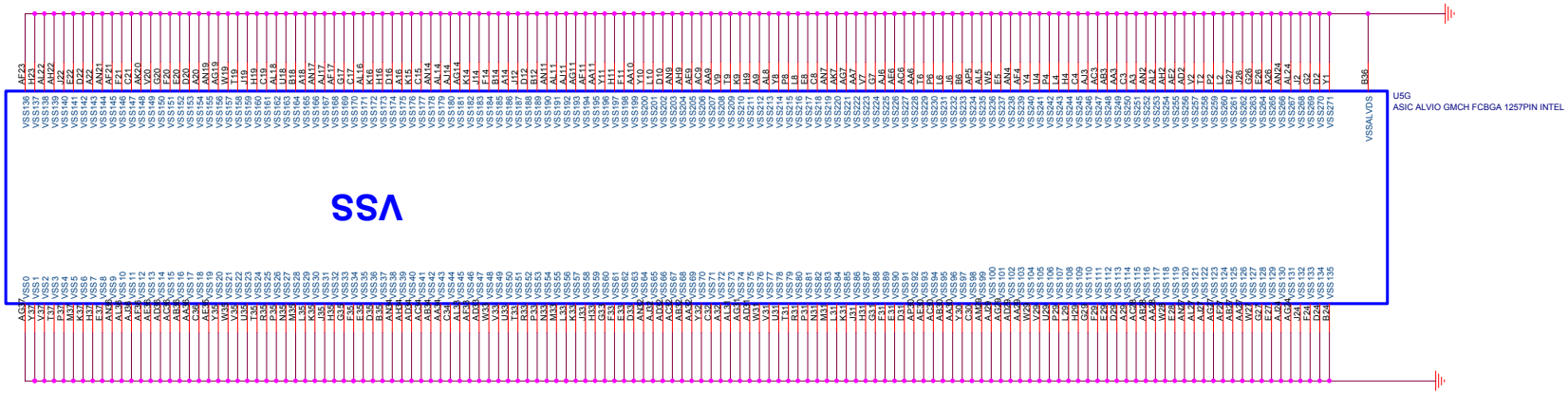
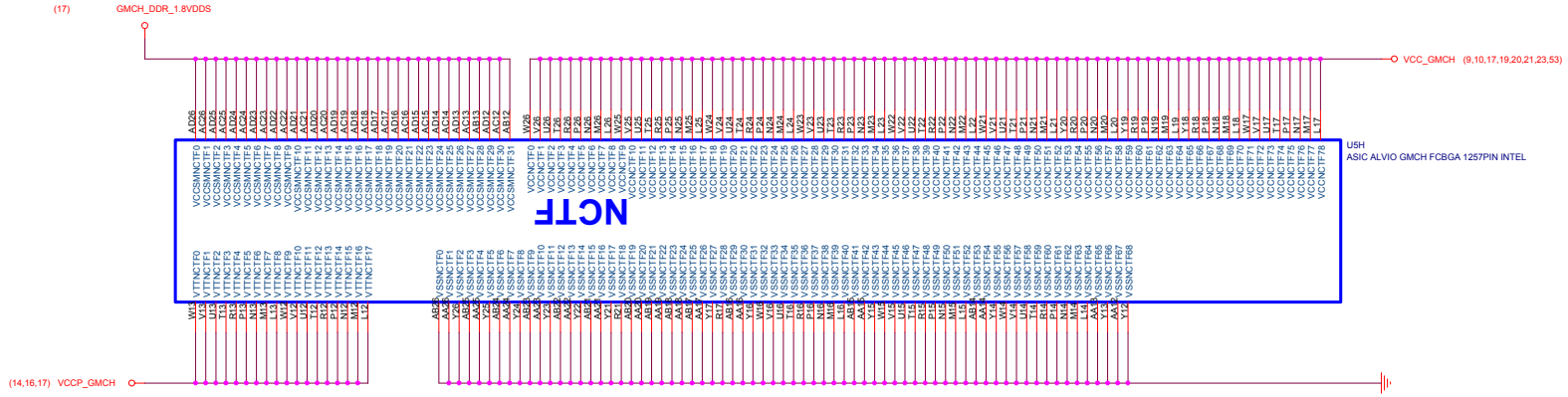
Title	AT11 < Dothan + 915GM + ICH6-M >
Size C	Document Number ALVISO(POWER) Rev 0.1
Date: Thursday, April 14, 2005	Sheet 17 of 63





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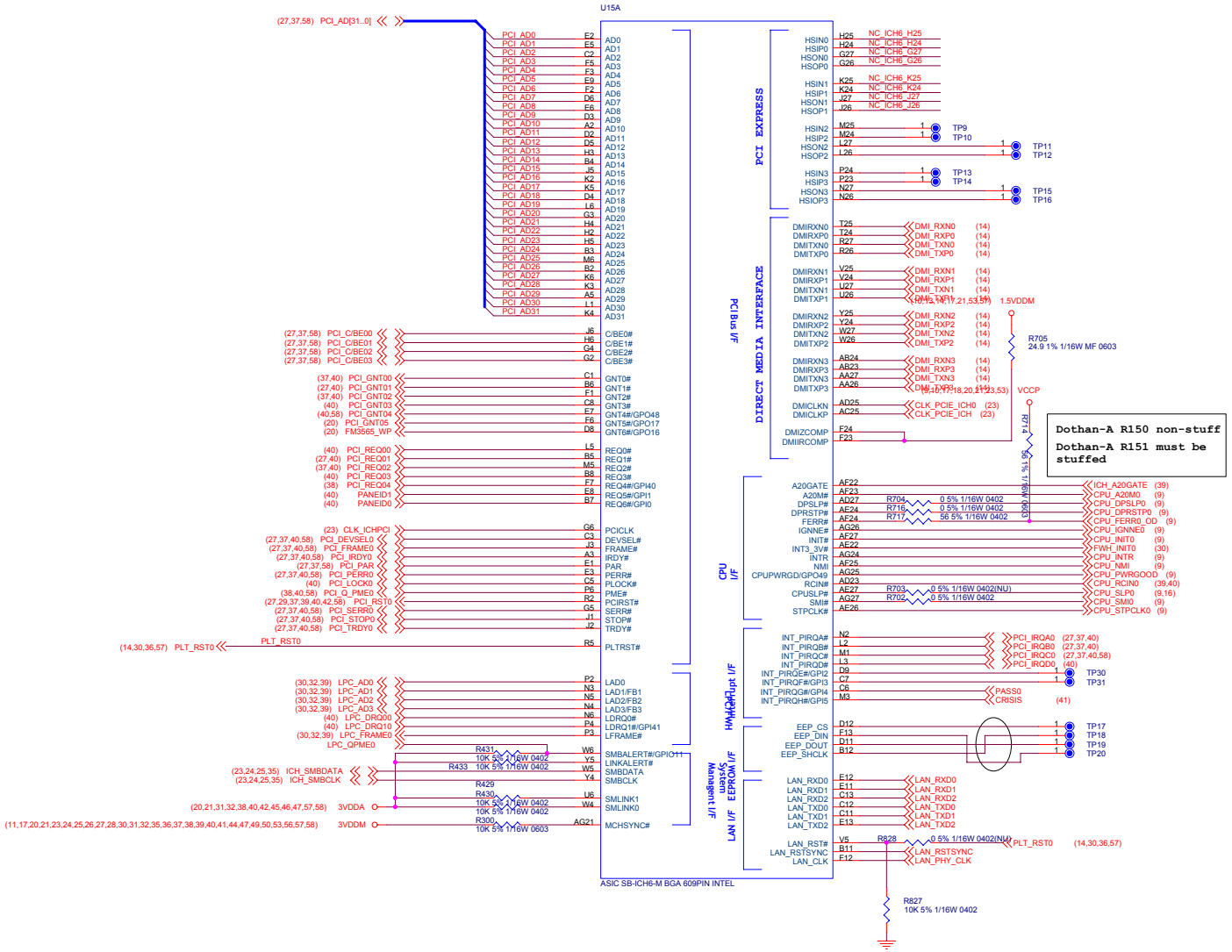
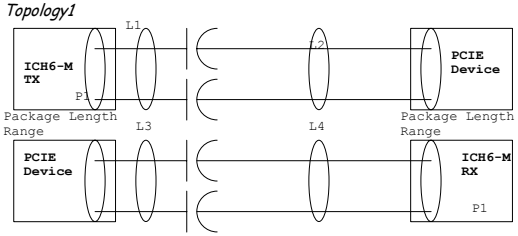
Title	AT11 < Dothan + 915GM + ICH6-M >		
Size C	Document Number ALVISO(VSS/NCTF)		Rev 0.1
Date: Thursday, April 14, 2005	Sheet 18 of 63		



PCIE Signal Topologies and Routing Guidelines

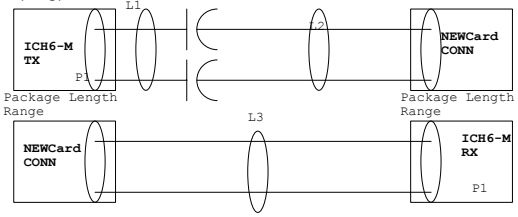
Signal	TRACE WIDTH	SPACE	TRACE MUTCHING	Impedance
PCIE	4 mils (stripline) 5 mils (microstrip)	7 mils (differential) 20 mils (pair to pair)	+/- 5 mils	100 ohms +/-20%

Topology1



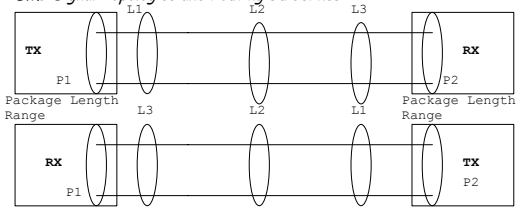
L1	L2	L3	L4	Cap
Min 0.25" Max 19.25"	Max 19.25" - L1	Min 0.25" Max 19.25"	Max 19.25" - L1	75nF ~200nF +/-20% 0402 or 0603

Topology2



L1	L2	L3	Cap
Min 0.25" Max 14.75"	Max 14.75" - L1	Min 0.25" Max 15"	75nF ~200nF +/-20% 0402 or 0603

DMI Signal Topologies and Routing Guidelines



Signal	TRACE WIDTH	SPACE	TRACE MUTCHING	Impedance
DMI	4 mils (stripline) 5 mils (microstrip)	7 mils (differential) 20 mils (pair to pair) 20 mils (non-PCIE signal)	+/- 5 mils	100 ohms +/-20%

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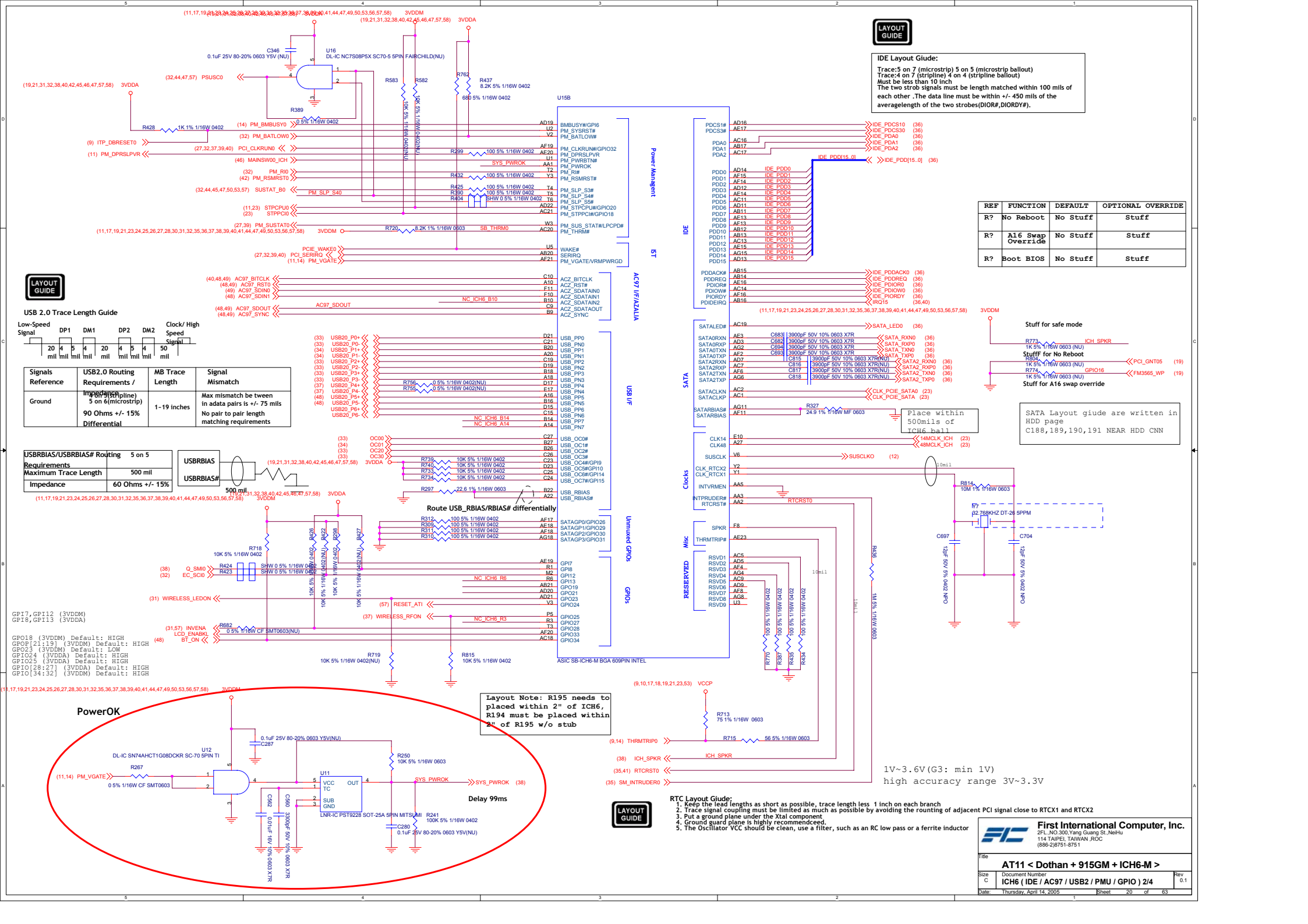
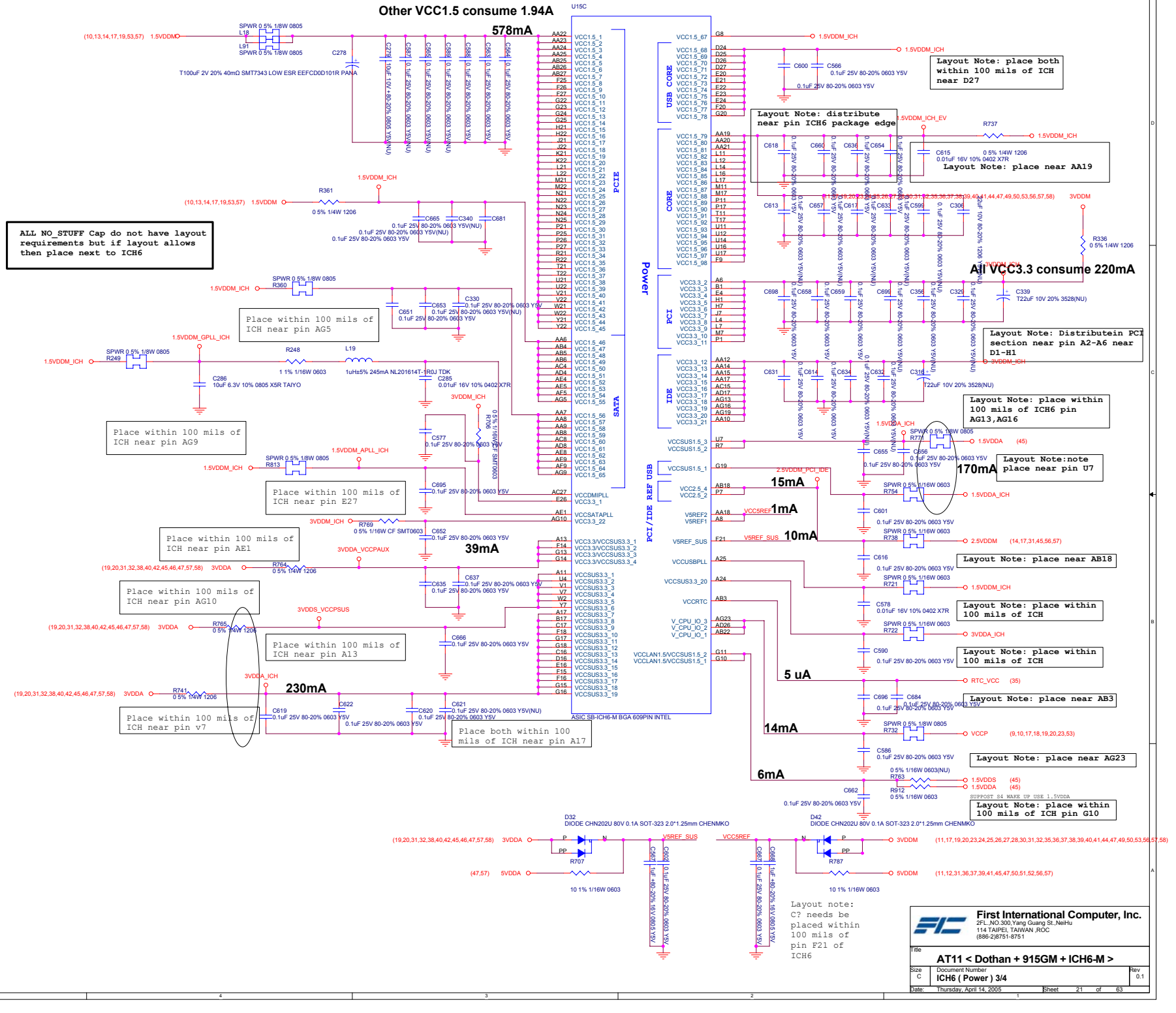
Title	AT11 < Dothan + 915GM + ICH6-M >	
Size C	Document Number: ICH6 (PCI / PCIE / CPU / IRQ / Lan) 1/4	Rev 0.1
Date: Thursday, April 14, 2005	Sheet 19 of 63	


LAYOUT GUIDE
IDE Layout Giude:
Trace:5 on 7 (microstrip) 5 on 5 (microstrip ballout)
Trace:4 on 7 (stripline) 4 on 4 (stripline ballout)
Must be less than 10 inch
The two strob signals must be length matched within 100 mils of each other .The data line must be within +/- 450 mils of the averagelength of the two strobes(DIOR#,DIORDY#).
REF | FUNCTION | DEFAULT | OPTIONAL OVERRIDE
R? | No Reboot | No Stuff | Stuff
R? | A16 Swap Override | No Stuff | Stuff
R? | Boot BIOS | No Stuff | Stuff
USB 2.0 Trace Length Guide
Low-Speed Signal
DP1
DM1
DP2
DM2
Clock/ High Speed Signal
20 mil
4 mil
5 mil
4 mil
20 mil
4 mil
5 mil
4 mil
50 mil
Signals Reference | USB2.0 Routing Requirements / Impedance | MB Trace Length | Signal Mismatch
Ground | 4 on 5(stripline) 5 on 6(microstrip) 90 Ohms +/- 15% Differential | 1-19 inches | Max mismatch be tween in adata pairs is +/- 75 mils No pair to pair length matching requirements
USBRBIAS/USBRBIAS# Routing Requirements 5 on 5
Maximum Trace Length 500 mil
Impedance 60 Ohms +/- 15%
USBRBIAS
USBRBIAS#
500 mil
Route USB_RBIAS/RBIAS# differentially
Layout Note: R195 needs to placed within 2" of ICH6, R194 must be placed within 2" of R195 w/o stub
PowerOK
Delay 99ms
RTC Layout Giude:
1. Keep the lead lengths as short as possible, trace length less 1 inch on each branch
2. Trace signal coupling must be limited as much as possible by avoiding the rounting of adjacent PCI signal close to RTCX1 and RTCX2
3. Put a ground plane under the Xtal component
4. Ground guard plane is highly recommendceed.
5. The Oscillator VCC should be clean, use a filter, such as an RC low pass or a ferrite inductor
Stuff for safe mode
StuffF for No Reboot
Stuff for A16 swap override
SATA Layout giude are written in HDD page
C188,189,190,191 NEAR HDD CNN
Place within 500mils of ICH6 ball
1V~3.6V(G3: min 1V)
high accuracy range 3V~3.3V
GPI7,GPI12 (3VDDM)
GPI8,GPI13 (3VDDA)
GPO18 (3VDDM) Default: HIGH
GPOP[21:19) (3VDDM) Default: HIGH
GPO23 (3VDDM) Default: LOW
GPIO24 (3VDDA) Default: HIGH
GPIO25 (3VDDA) Default: HIGH
GPIO[28:27) (3VDDA) Default: HIGH
GPIO[34:32] (3VDDM) Default: HIGH
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
Title
AT11 < Dothan + 915GM + ICH6-M >
Size C
Document Number
ICH6 (IDE / AC97 / USB2 / PMU / GPIO) 2/4
Rev 0.1
Date: Thursday, April 14, 2005
Sheet 20 of 63


Other VCC1.5 consume 1.94A
578mA
U15C
ALL NO_STUFF Cap do not have layout requirements but if layout allows then place next to ICH6
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near pin E27
Place within 100 mils of ICH near pin AE1
Place within 100 mils of ICH near pin AG10
Place within 100 mils of ICH near pin A13
Place within 100 mils of ICH near pin v7
Place both within 100 mils of ICH near pin A17
39mA
230mA
All VCC3.3 consume 220mA
170mA
15mA
1mA
10mA
5 uA
14mA
6mA
Layout Note: place both within 100 mils of ICH near D27
Layout Note: distribute near pin ICH6 package edge
Layout Note: place near AA19
Layout Note: Distributein PCI section near pin A2-A6 near D1-H1
Layout Note: place within 100 mils of ICH6 pin AG13,AG16
Layout Note:note place near pin U7
Layout Note: place near AB18
Layout Note: place within 100 mils of ICH
Layout Note: place within 100 mils of ICH
Layout Note: place near AB3
Layout Note: place near AG23
Layout Note: place within 100 mils of ICH pin G10
Layout note: C? needs be placed within 100 mils of pin F21 of ICH6
ASIC SB-ICH6-M BGA 609PIN INTEL
D32 DIODE CHN202U 80V 0.1A SOT-323 2.0*1.25mm CHENMKO
D42 DIODE CHN202U 80V 0.1A SOT-323 2.0*1.25mm CHENMKO
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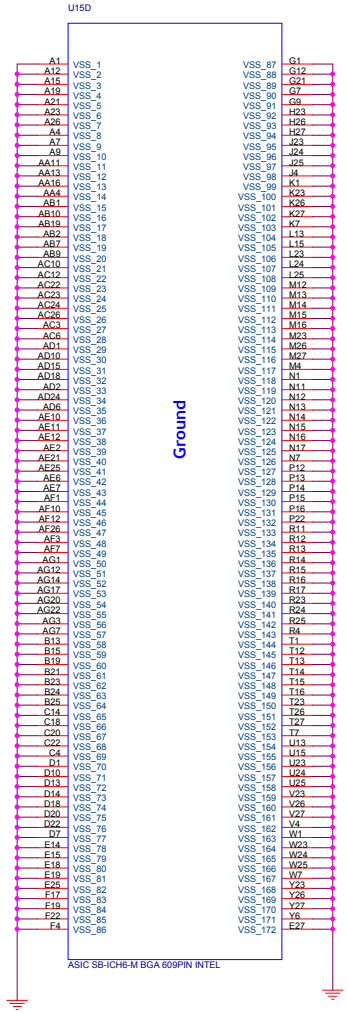
AT11 < Dothan + 915GM + ICH6-M >
Size C
Document Number ICH6 (Power) 3/4
Rev 0.1
Date: Thursday, April 14, 2005
Sheet 21 of 63



A1	VSS_1	VSS_87	G1
A12	VSS_2	VSS_88	G12
A15	VSS_3	VSS_89	G21
A19	VSS_4	VSS_90	G7
A21	VSS_5	VSS_91	G9
A23	VSS_6	VSS_92	H23
A26	VSS_7	VSS_93	H26
A4	VSS_8	VSS_94	H27
A7	VSS_9	VSS_95	J23
A9	VSS_10	VSS_96	J24
AA11	VSS_11	VSS_97	J25
AA13	VSS_12	VSS_98	J4
AA16	VSS_13	VSS_99	K1
AA4	VSS_14	VSS_100	K23
AB1	VSS_15	VSS_101	K26
AB10	VSS_16	VSS_102	K27
AB19	VSS_17	VSS_103	K7
AB2	VSS_18	VSS_104	L13
AB7	VSS_19	VSS_105	L15
AB9	VSS_20	VSS_106	L23
AC10	VSS_21	VSS_107	L24
AC12	VSS_22	VSS_108	L25
AC22	VSS_23	VSS_109	M12
AC23	VSS_24	VSS_110	M13
AC24	VSS_25	VSS_111	M14
AC26	VSS_26	VSS_112	M15
AC3	VSS_27	VSS_113	M16
AC6	VSS_28	VSS_114	M23
AD1	VSS_29	VSS_115	M26
AD10	VSS_30	VSS_116	M27
AD15	VSS_31	VSS_117	M4
AD18	VSS_32	VSS_118	N1
AD2	VSS_33	VSS_119	N11
AD24	VSS_34	VSS_120	N12
AD6	VSS_35	VSS_121	N13
AE10	VSS_36	VSS_122	N14
AE11	VSS_37	VSS_123	N15
AE12	VSS_38	VSS_124	N16
AE2	VSS_39	VSS_125	N17
AE21	VSS_40	VSS_126	N7
AE25	VSS_41	VSS_127	P12
AE6	VSS_42	VSS_128	P13
AE7	VSS_43	VSS_129	P14
AF1	VSS_44	VSS_130	P15
AF10	VSS_45	VSS_131	P16
AF12	VSS_46	VSS_132	P22
AF26	VSS_47	VSS_133	R11
AF3	VSS_48	VSS_134	R12
AF7	VSS_49	VSS_135	R13
AG1	VSS_50	VSS_136	R14
AG12	VSS_51	VSS_137	R15
AG14	VSS_52	VSS_138	R16
AG17	VSS_53	VSS_139	R17
AG20	VSS_54	VSS_140	R23
AG22	VSS_55	VSS_141	R24
AG3	VSS_56	VSS_142	R25
AG7	VSS_57	VSS_143	R4
B13	VSS_58	VSS_144	T1
B15	VSS_59	VSS_145	T12
B19	VSS_60	VSS_146	T13
B21	VSS_61	VSS_147	T14
B23	VSS_62	VSS_148	T15
B24	VSS_63	VSS_149	T16
B25	VSS_64	VSS_150	T23
C14	VSS_65	VSS_151	T26
C18	VSS_66	VSS_152	T27
C20	VSS_67	VSS_153	T7
C22	VSS_68	VSS_154	U13
C4	VSS_69	VSS_155	U15
D1	VSS_70	VSS_156	U23
D10	VSS_71	VSS_157	U24
D13	VSS_72	VSS_158	U25
D14	VSS_73	VSS_159	V23
D18	VSS_74	VSS_160	V26
D20	VSS_75	VSS_161	V27
D22	VSS_76	VSS_162	V4
D7	VSS_77	VSS_163	W1
E14	VSS_78	VSS_164	W23
E15	VSS_79	VSS_165	W24
E18	VSS_80	VSS_166	W25
E19	VSS_81	VSS_167	W7
E25	VSS_82	VSS_168	Y23
F17	VSS_83	VSS_169	Y26
F19	VSS_84	VSS_170	Y27
F22	VSS_85	VSS_171	Y6
F4	VSS_86	VSS_172	E27

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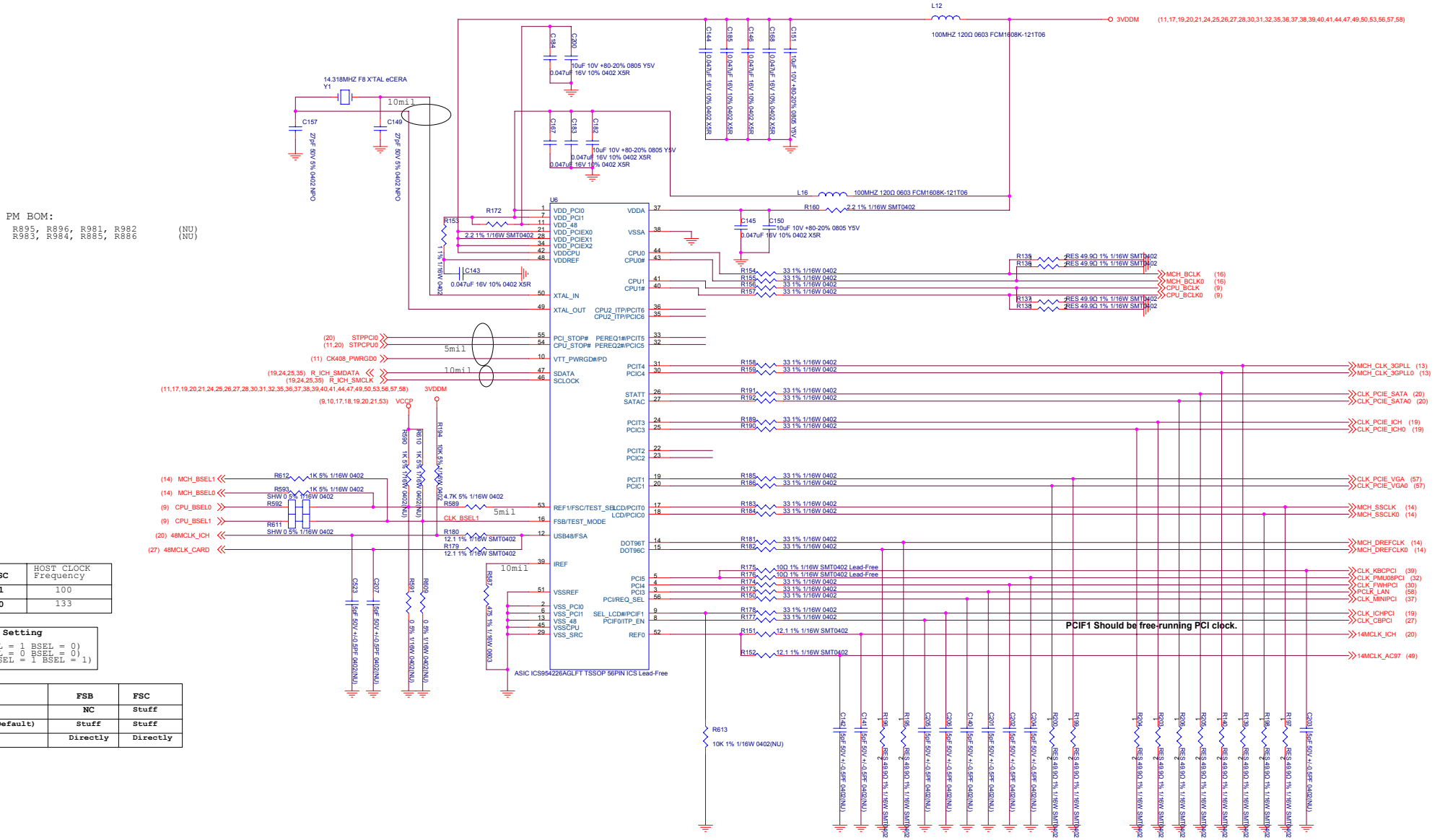
Title

AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	**ICH6 (Ground) 4/4**	0.1

Date: Wednesday, February 16, 2005 Sheet 22 of 63



FSA	FSB	FSC	HOST CLOCK Frequency
1	0	1	100
1	0	0	133

CK-410 BSEL Setting

10 = PSB400 (BSEL = 1 BSEL = 0)
00 = PSB533 (BSEL = 0 BSEL = 0)
11 = Reserved (BSEL = 1 BSEL = 1)

	FSB	FSC
Dothan-A PSB400	NC	Stuff
Dothan-A PSB533(Default)	Stuff	Stuff
Dothan-B1	Directly	Directly

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

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Title: AT11 < Dothan + 915GM + ICH6-M >

Size: C | Document Number: Clock Generator (ICS 954206AG) | Rev: 0.1

Date: Thursday, April 14, 2005 | Sheet 23 of 63

Place near So-Dimm1

CN32

SCKT KEYLINK SMT 200PIN 5662-2-131 DDR2 H=5.2mm NOR

20-25013-00

SO DIMM 1

LAYOUT GUIDE

Other signal — 20mil
DDR_VREF — 20mil — 20mil
Other signal — 20mil

SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0

LAYOUT GUIDE

Place one cap close to every 2 pullup resistors terminated to 0.9vddm

400 mils

56 5% 0402X2 1/16W 4P2R

Place these resistors near So-Dimm1

120mil

Place these Hi-Freq decoupling caps near GMCH

Place these 2.2uF caps near So-Dimm1

Place these 0.1uF caps near So-Dimm1

Title	AT11 < Dothan + 915GM + ICH6-M >
Size C	Document Number DDR2 SODIMM 1
Rev	0.1
Date:	Thursday, April 14, 2005
Sheet	24 of 63

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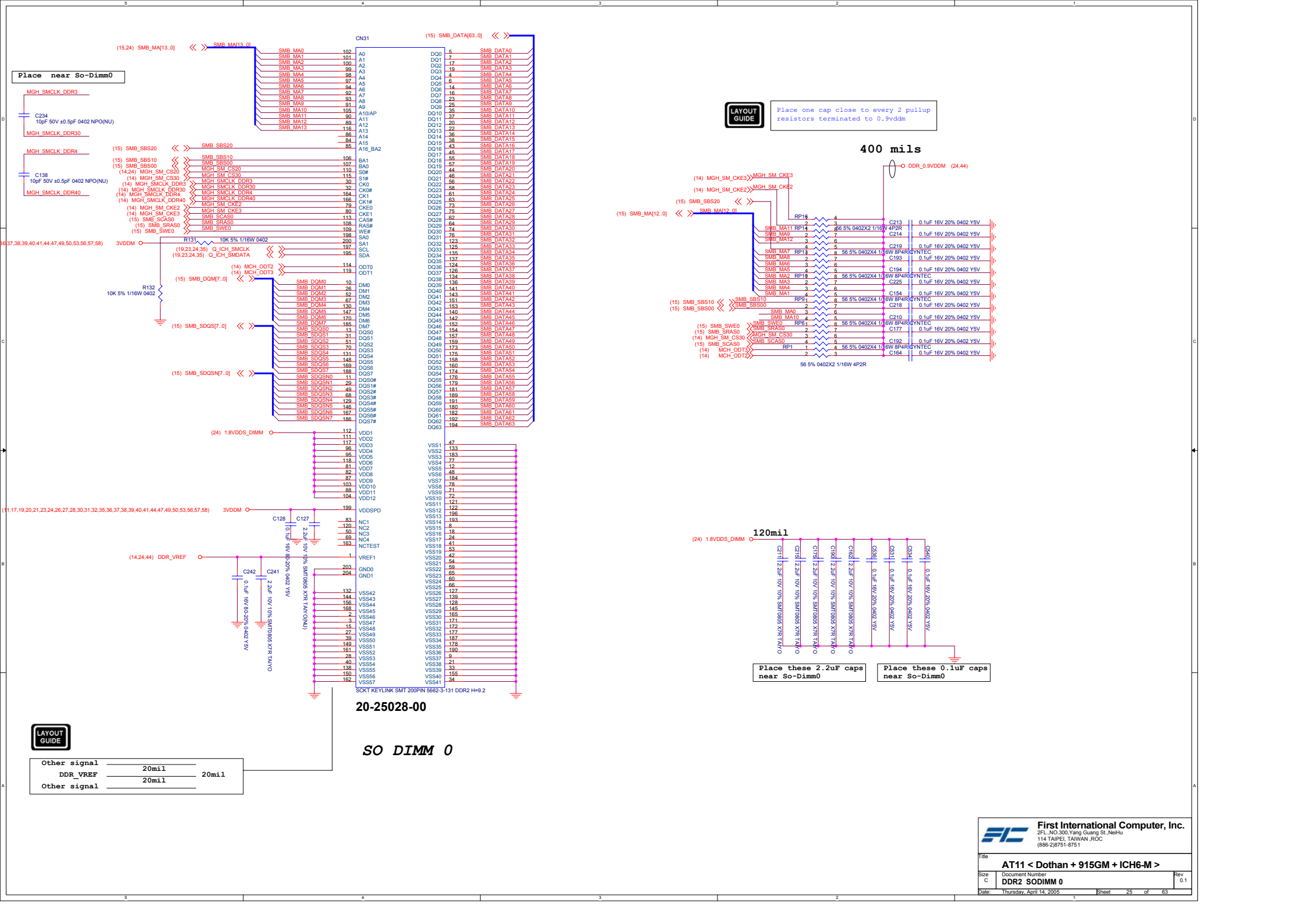
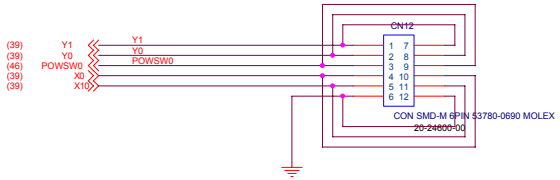
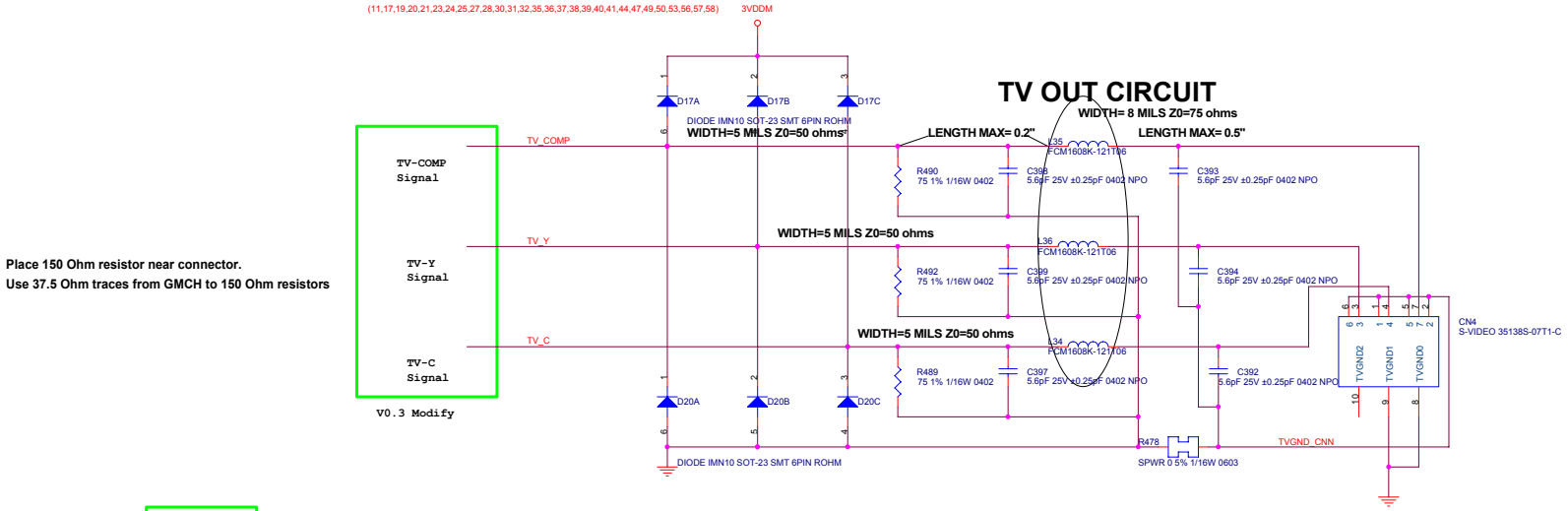
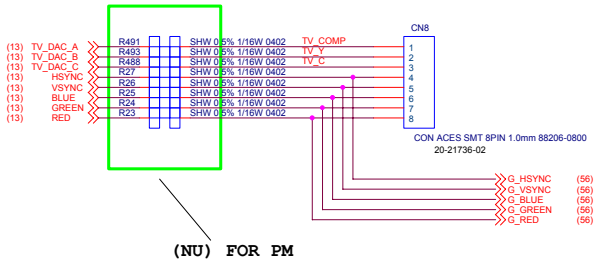


Company	First International Computer, Inc.
Address	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC
Phone	(886-2)8751-8751
Title	AT11 < Dothan + 915GM + ICH6-M >
Size	C
Document Number	DDR2 SODIMM 0
Rev	0.1
Date	Thursday, April 14, 2005
Sheet	25 of 63







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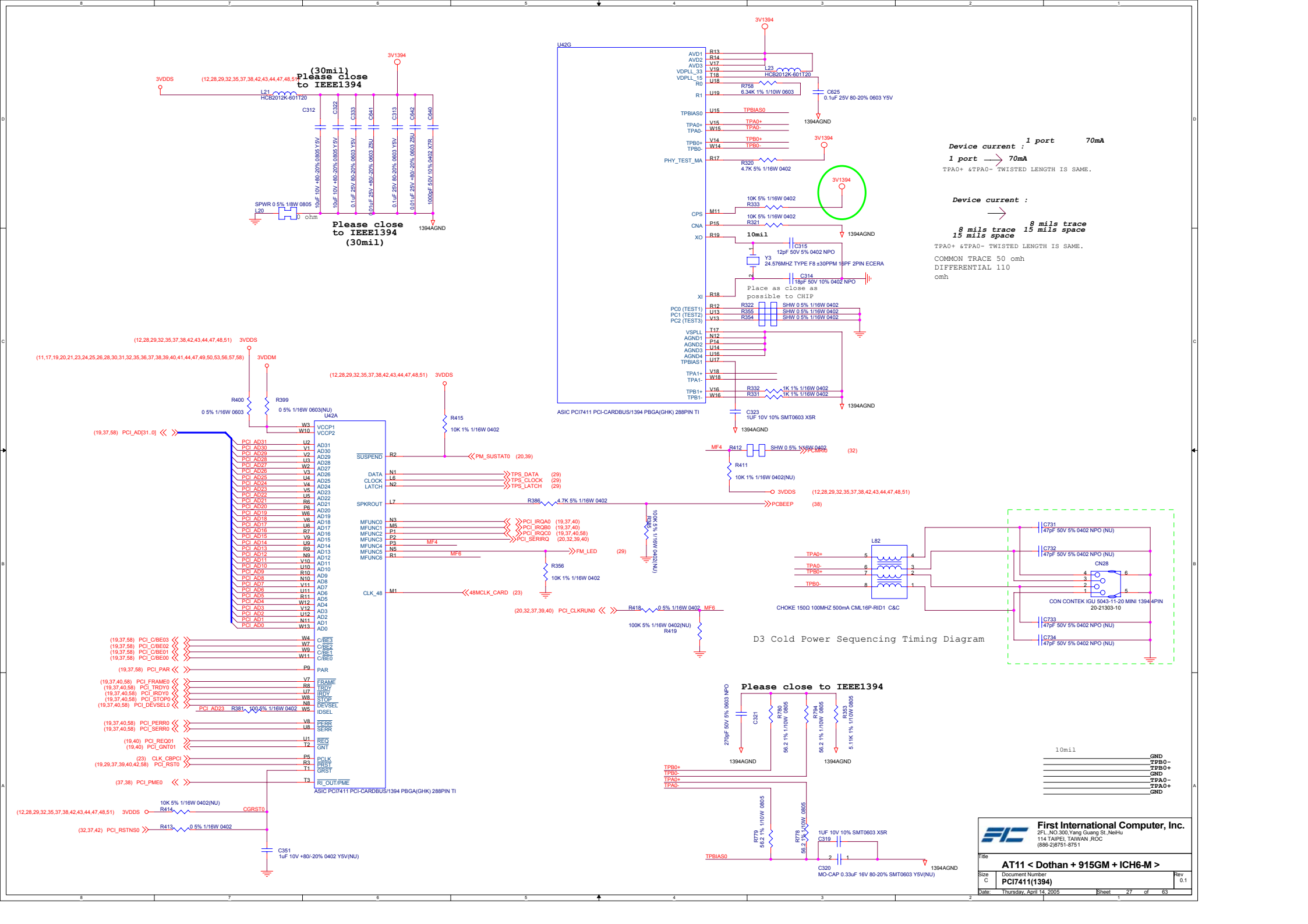
Title: AT11 < Dothan + 915GM + ICH6-M >

Size: C | Document Number: SWITCH & TV-OUT | Rev: 0.1

Date: Thursday, April 14, 2005 | Sheet 26 of 63


(30mil)
Please close to IEEE1394
3VDDS
3V1394
L21 HCB2012K-601T120
C312 10uF 10V +80/-20% 0805 Y5V
C322 10uF 10V +80/-20% 0805 Y5V
C333 0.1uF 25V 80/-20% 0603 Y5V
C641 0.01uF 25V +80/-20% 0603 Z5U
C313 0.1uF 25V 80/-20% 0603 Y5V
C642 0.01uF 25V +80/-20% 0603 Z5U
C640 1000pF 50V 10% 0402 X7R
SPWR 0 5% 1/8W 0805
L20 0 ohm
1394AGND
Please close to IEEE1394 (30mil)
U42G
AVD1 AVD2 AVD3 VDPLL_33 VDPLL_15 R0 R1
R758 6.34K 1% 1/10W 0603
L23 HCB2012K-601T120
C625 0.1uF 25V 80-20% 0603 Y5V
TPBIAS0 TPA0+ TPA0- TPB0+ TPB0-
PHY_TEST_MA
R320 4.7K 5% 1/16W 0402
CPS CNA XO XI
10K 5% 1/16W 0402 R333
10K 5% 1/16W 0402 R321
10mil
C315 12pF 50V 5% 0402 NPO
Y3 24.576MHZ TYPE F8 ±30PPM 18PF 2PIN ECERA
C314 18pF 50V 10% 0402 NPO
Place as close as possible to CHIP
PC0 (TEST1) PC1 (TEST2) PC2 (TEST3)
R322 R355 R354 SHW 0.5% 1/16W 0402
VSPLL AGND1 AGND2 AGND3 AGND4 TPBIAS1
TPA1+ TPA1- TPB1+ TPB1-
R332 1K 1% 1/16W 0402
R331 1K 1% 1/16W 0402
C323 1UF 10V 10% SMT0603 X5R
ASIC PCI7411 PCI-CARDBUS/1394 PBGA(GHK) 288PIN TI
Device current : 1 port 70mA
1 port → 70mA
TPA0+ &TPA0- TWISTED LENGTH IS SAME.
Device current :
8 mils trace 15 mils space
8 mils trace 15 mils space
TPA0+ &TPA0- TWISTED LENGTH IS SAME.
COMMON TRACE 50 omh
DIFFERENTIAL 110 omh
(12,28,29,32,35,37,38,42,43,44,47,48,51) 3VDDS
(11,17,19,20,21,23,24,25,26,28,30,31,32,35,36,37,38,39,40,41,44,47,49,50,53,56,57,58) 3VDDM
R400 0 5% 1/16W 0603
R399 0 5% 1/16W 0603(NU)
U42A
VCCP1 VCCP2
(19,37,58) PCI_AD[31..0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
(19,37,58) PCI_C/BE03 PCI_C/BE02 PCI_C/BE01 PCI_C/BE00
C/BE3 C/BE2 C/BE1 C/BE0
(19,37,58) PCI_PAR
PAR
(19,37,40,58) PCI_FRAME0 (19,37,40,58) PCI_TRDY0 (19,37,40,58) PCI_IRDY0 (19,37,40,58) PCI_STOP0 (19,37,40,58) PCI_DEVSEL0
FRAME TRDY IRDY STOP DEVSEL
PCI_AD23 R381 100 5% 1/16W 0402
IDSEL
(19,37,40,58) PCI_PERR0 (19,37,40,58) PCI_SERR0
PERR SERR
(19,40) PCI_REQ01 (19,40) PCI_GNT01
REQ GNT
(23) CLK_CBPCI (19,29,37,39,40,42,58) PCI_RST0
PCLK PRST GRST
(37,38) PCI_PME0
RI_OUT/PME
ASIC PCI7411 PCI-CARDBUS/1394 PBGA(GHK) 288PIN TI
10K 5% 1/16W 0402(NU) R414
(12,28,29,32,35,37,38,42,43,44,47,48,51) 3VDDS
CGRST0
(32,37,42) PCI_RSTNS0
R413 0 5% 1/16W 0402
C351 1uF 10V +80/-20% 0402 YSV(NU)
(12,28,29,32,35,37,38,42,43,44,47,48,51) 3VDDS
R415 10K 1% 1/16W 0402
SUSPEND R2 (PM_SUSTAT0 (20,39))
DATA N1 (TPS_DATA (29))
CLOCK L6 (TPS_CLOCK (29))
LATCH N2 (TPS_LATCH (29))
SPKROUT L7
R386 4.7K 5% 1/16W 0402
PCBEEP (38)
R385 100K 5% 1/16W 0402(NU)
MFUNC0 N3 (PCI_IRQA0 (19,37,40))
MFUNC1 M5 (PCI_IRQB0 (19,37,40))
MFUNC2 P1 (PCI_IRQC0 (19,37,40,58))
MFUNC3 P2 (PCI_SERIRQ (20,32,39,40))
MFUNC4 P3 MF4
MFUNC5 N5
MFUNC6 R1 MF6
FM_LED (29)
R356 10K 1% 1/16W 0402
CLK_48 M1 (48MCLK_CARD (23))
(20,32,37,39,40) PCI_CLKRUN0
R418 0 5% 1/16W 0402 MF6
100K 5% 1/16W 0402(NU) R419
MF4 R412 SHW 0.5% 1/16W 0402 PCMRI0 (32)
R411 10K 1% 1/16W 0402(NU)
3VDDS (12,28,29,32,35,37,38,42,43,44,47,48,51)
L82
TPA0+ TPA0- TPB0+ TPB0-
CHOKE 150Ω 100MHZ 500mA CML16P-RID1 C&C
C731 47pF 50V 5% 0402 NPO (NU)
C732 47pF 50V 5% 0402 NPO (NU)
CN28
CON CONTEK IGU 5043-11-20 MINI 1394 4PIN 20-21303-10
C733 47pF 50V 5% 0402 NPO (NU)
C734 47pF 50V 5% 0402 NPO (NU)
D3 Cold Power Sequencing Timing Diagram
Please close to IEEE1394
C321 270pF 50V 5% 0603 NPO
R780 56.2 1% 1/10W 0805
R784 56.2 1% 1/10W 0805
R353 5.11K 1% 1/10W 0805
1394AGND
TPB0+ TPB0- TPA0+ TPA0-
R779 56.2 1% 1/10W 0805
R778 56.2 1% 1/10W 0805
1UF 10V 10% SMT0603 X5R C319
TPBIAS0
C320 MO-CAP 0.33uF 16V 80-20% SMT0603 Y5V(NU)
10mil
GND TPB0- TPB0+ GND TPA0- TPA0+ GND
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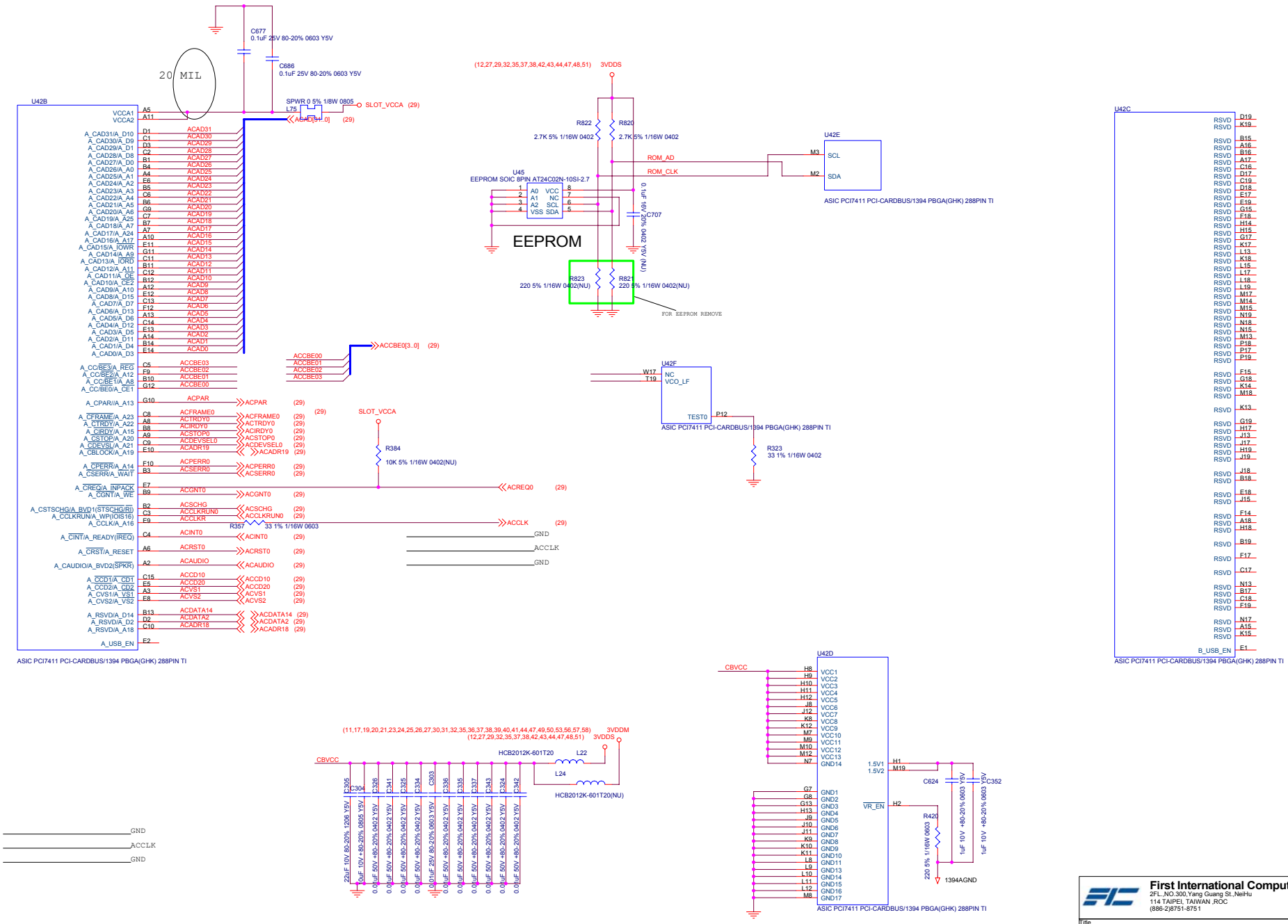
Title
AT11 < Dothan + 915GM + ICH6-M >
Size C
Document Number PCI7411(1394)
Rev 0.1
Date: Thursday, April 14, 2005
Sheet 27 of 63



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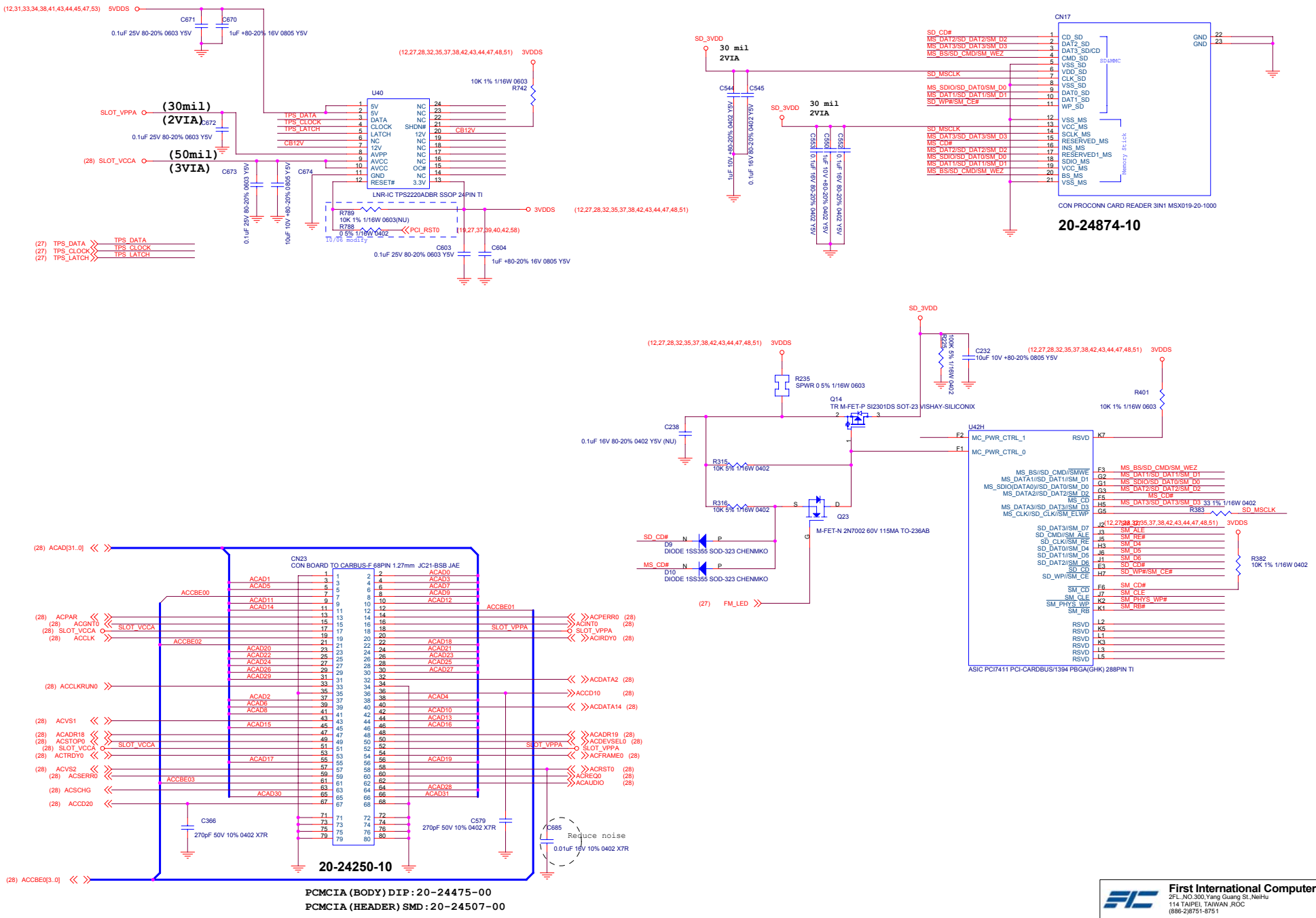
Title	AT11 < Dothan + 915GM + ICH6-M >		
Size C	Document Number PCI7411(CardBus)		Rev 0.1
Date: Thursday, April 14, 2005	Sheet 28 of 63		



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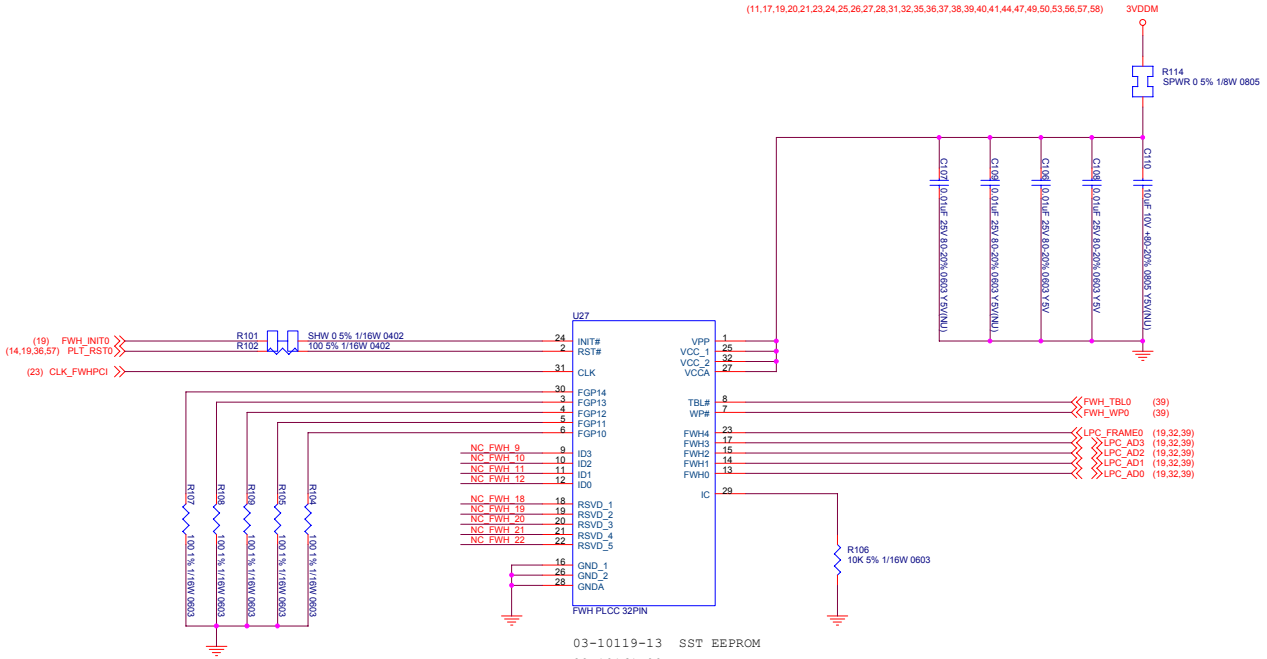
Title: **AT11 < Dothan + 915GM + ICH6-M >**

Size	Document Number	Rev
C	Cardbus Power/CNN	0.1

Date: Thursday, April 14, 2005 Sheet 29 of 63



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Title

AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	**FirmWare Hub**	0.1

Date: Thursday, April 14, 2005 Sheet 30 of 63

LCD brightness control

(11,12,21,36,37,39,41,45,47,50,51,52,56,57) 5VDDM

VBRIGHTNESS 0.5V - 4.0V

(38) Q_BLADJ

FROM PMU07

BLADJ label signal
BLADJ: 1.6V - 2.6V

R9 1K 5% 1/16W 0402

Q2 TRANS NPN MMBT3904 SOT SOT-23 FAIRCHILD

C15 0.1uF 16V 80-20% 0402 Y5V

R28 4.7K 5% 1/16W 0402

C414 10uF 10V +80-20% 0805 Y5V

BRIGHTNESS >> BRIGHTNESS

LED indicator control logic

Trace:5mil, Spacing:5mil

Q47

(12,29,33,34,38,41,43,44,45,47,53) 5VDDS

LED_AMBER >> LED_AMBER (57)

(32) LED_A

R522 1K 5% 1/16W 0402

TR IMD2 50V 30mA 6PIN SC-59 ROHM

Q44

(12,29,33,34,38,41,43,44,45,47,53) 5VDDS

LED_GREEN >> LED_GREEN (57)

(32) LED_G

R517 1K 5% 1/16W 0402

TR IMD2 50V 30mA 6PIN SC-59 ROHM

Q45

(54,57) PMU5V

CHG_LED >> CHG_LED (57)

(32) CHGLED

R519 1K 5% 1/16W 0402

TR IMD2 50V 30mA 6PIN SC-59 ROHM

(57) WIRELESS_RFON01

(11,12,21,36,37,39,41,45,47,50,51,52,56,57) 5VDDM

Q3 PNP DTA144EU UMT 50V 30mA ROHM

(11,17,19,20,21,23,24,25,26,27,28,29,32,35,36,37,38,39,40,41,44,47,49,50,53,56,57,58)

(20) WIRELESS_LEDON

TR NPN DTC144EUA(UMT3) 50V 100mA ROHM Q1

Q38A TRANS M-FET-P FDS6875 2.5V SOP-8 8PIN FAIRCHILD

(19,20,21,32,38,40,42,45,46,47,57,58) 3VDDA

ICC_MAX=2A
PATTERN
WIDTH=MIN.
2MM(80MIL)

C391 0.1uF 25V 80-20% 0603 Y5V

R477 47K 5% 1/16W 0603

Q38B TRANS M-FET-P FDS6875 2.5V SOP-8 8PIN FAIRCHILD

L33 HCB2012K-121T30

F5 FUSE 2A 32V TR/3216FF SMD

Min : 80 MIL or Power Plane

2003.03.12 modify mlcc
2003.03.14 change 0805

C12 10uF 20% 1206 Y5V

C11 0.1uF 25V 80-20% 0603 Y5V

5mil

R476 4.7K 5% 1/16W 0603

(13) LVDS_ENALCD

5mil

Q39 NPN PDTC144EU SOT-323 PHILIPS

R495 100K 1% 1/16W MF 0402 PANA

(11,17,19,20,21,23,24,25,26,27,28,30,32,35,36,37,38,39,40,41,44,47,49,50,53,56,57,58) 3VDDM

(11,44,46,53,55,57) DCIN

HCB1608K-601T10 L47

HCB1608K-601T10 L48

Min : 60 MIL

C13

C14 1uF 25V 20% 0805 Y5V

(11,12,21,36,37,39,41,45,47,50,51,52,56,57) 5VDDM

BRIGHTNESS >> BRIGHTNESS
(20,57) INVENA >> INVENA

(39,57) CAPS0
(39,57) NUM0
(39,57) SRLL0
(36,57) HDD_LED0
(57) LED_GREEN >> LED_GREEN
(57) LED_AMBER >> LED_AMBER
(57) CHG_LED >> CHG_LED

3VDDM

R60 2.2K 1% 1/16W 0603

R59 2.2K 1% 1/16W 0603

LCD_DDC_CLK

LCD_DDC_DATA

(13) LVDS_TXCLK_LN
(13) LVDS_TXCLK_UP
(13) LVDS_TXCLK_LP
(13) LVDS_TXCLK_UN

(13) LVDS_TXOUT_L2N
(13) LVDS_TXOUT_U2P
(13) LVDS_TXOUT_L2P
(13) LVDS_TXOUT_U2N

(13) LVDS_TXOUT_L1N
(13) LVDS_TXOUT_U1P
(13) LVDS_TXOUT_L1P
(13) LVDS_TXOUT_U1N

(13) LVDS_TXOUT_L0N
(13) LVDS_TXOUT_U0P
(13) LVDS_TXOUT_L0P
(13) LVDS_TXOUT_U0N

CN9

NP2 NPTH2 GP2 GP1 NPTH1 NP1

GP6 GP5 GP4 GP3

CON 50PIN 88028-500N ACE

20-25085-00

C74 0.1uF 16V 20% 0402 Y5V(NU)

(NU) FOR PM

(14,17,21,45,56,57) 2.5VDDM

R83 2.2K 1% 1/16W 0603

Q6

(13) DDC_PDATA

LCD_DDC_DATA

M-FET-N 2N7002 60V 115MA TO-236AB

(14,17,21,45,56,57) 2.5VDDM

R71 2.2K 1% 1/16W 0603

Q4

(13) DDC_PCLK

LCD_DDC_CLK

M-FET-N 2N7002 60V 115MA TO-236AB

(12,29,33,34,38,41,43,44,45,47,53) 5VDDS

(57) G_LVDS_ENABKL

R669 0 5% 1/16W 0402(NU)

(13,40) LVDS_ENABKL

R668 0 5% 1/16W 0402

U32 DL-IC SN74AHCT1G08DCKR SC-70 5PIN TI

(32,41) LID0

INVENA >> INVENA (20,57)

LVDS Interface

The trace length of TXOUT0- should be equal to TXOUT0+
The trace length of TXOUT1- should be equal to TXOUT1+
The trace length of TXOUT2- should be equal to TXOUT2+
The trace length of TXCLK- should be equal to TXCLK+

Mismatch between TXLCK+/- and TXOUT+/- not exceed 25 mil

MUST HAVE VIA HOLE
GND
15mil
TXOUT0- 5mil
5mil
TXOUT0+ 5mil
15mil
GND
MUST HAVE VIA HOLE
20 mil area must clean no any trace and via hole
MUST HAVE VIA HOLE
GND
15mil
TXOUT1- 5mil
5mil
TXOUT1+ 5mil
15mil
GND
MUST HAVE VIA HOLE

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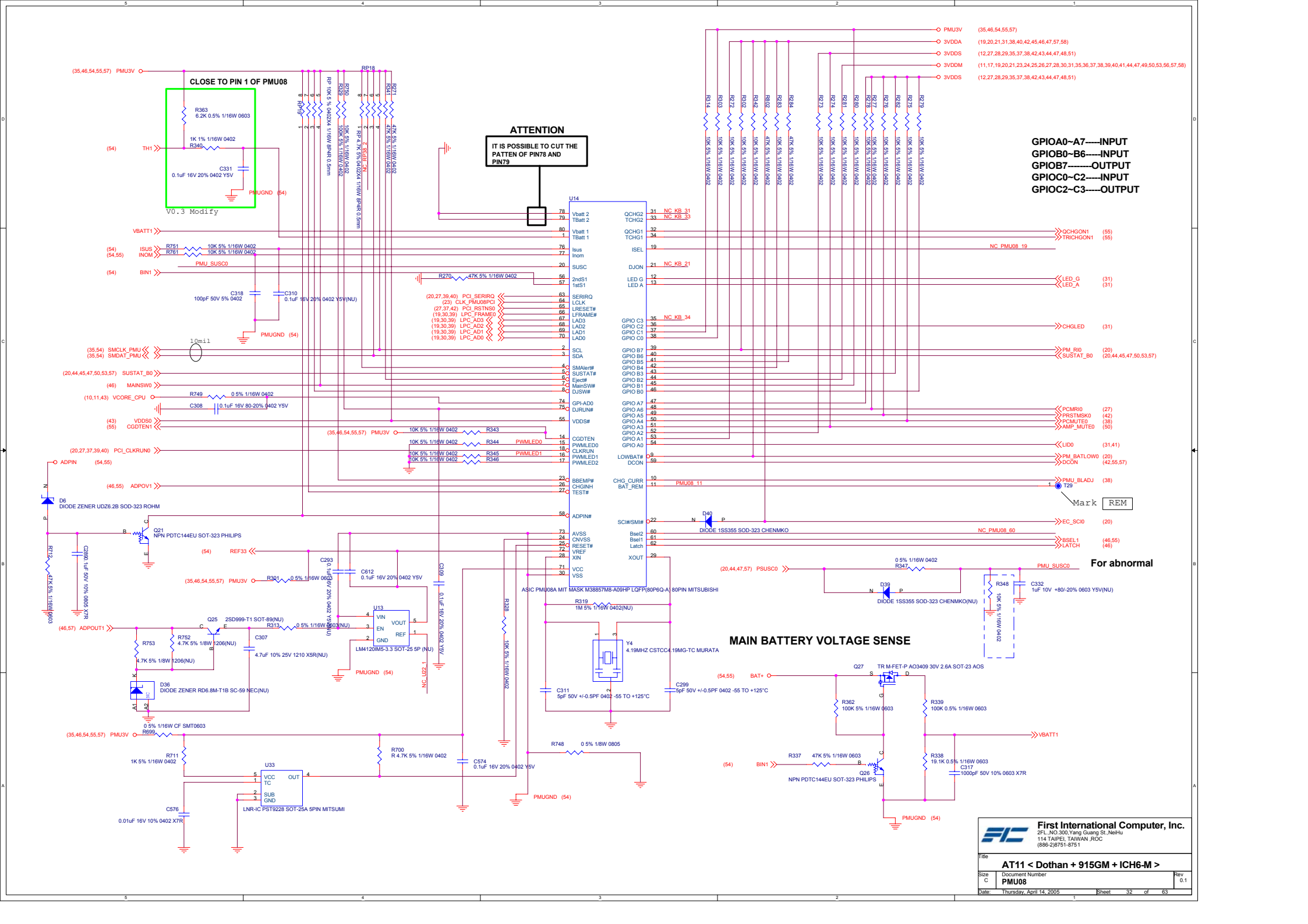
(886-2)2600-8818

Title: AT11 < Dothan + 915GM + ICH6-M >

Size: C | Document Number: LCD CNN | Rev: 0.2

Date: Thursday, April 14, 2005 | Sheet 31 of 63


CLOSE TO PIN 1 OF PMU08
V0.3 Modify
ATTENTION
IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79
GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT
ASIC PMU08A MIT MASK M38857M8-A09HP LQFP(80P6Q-A) 80PIN MITSUBISHI
MAIN BATTERY VOLTAGE SENSE
For abnormal
Mark
REM
First International Computer, Inc.
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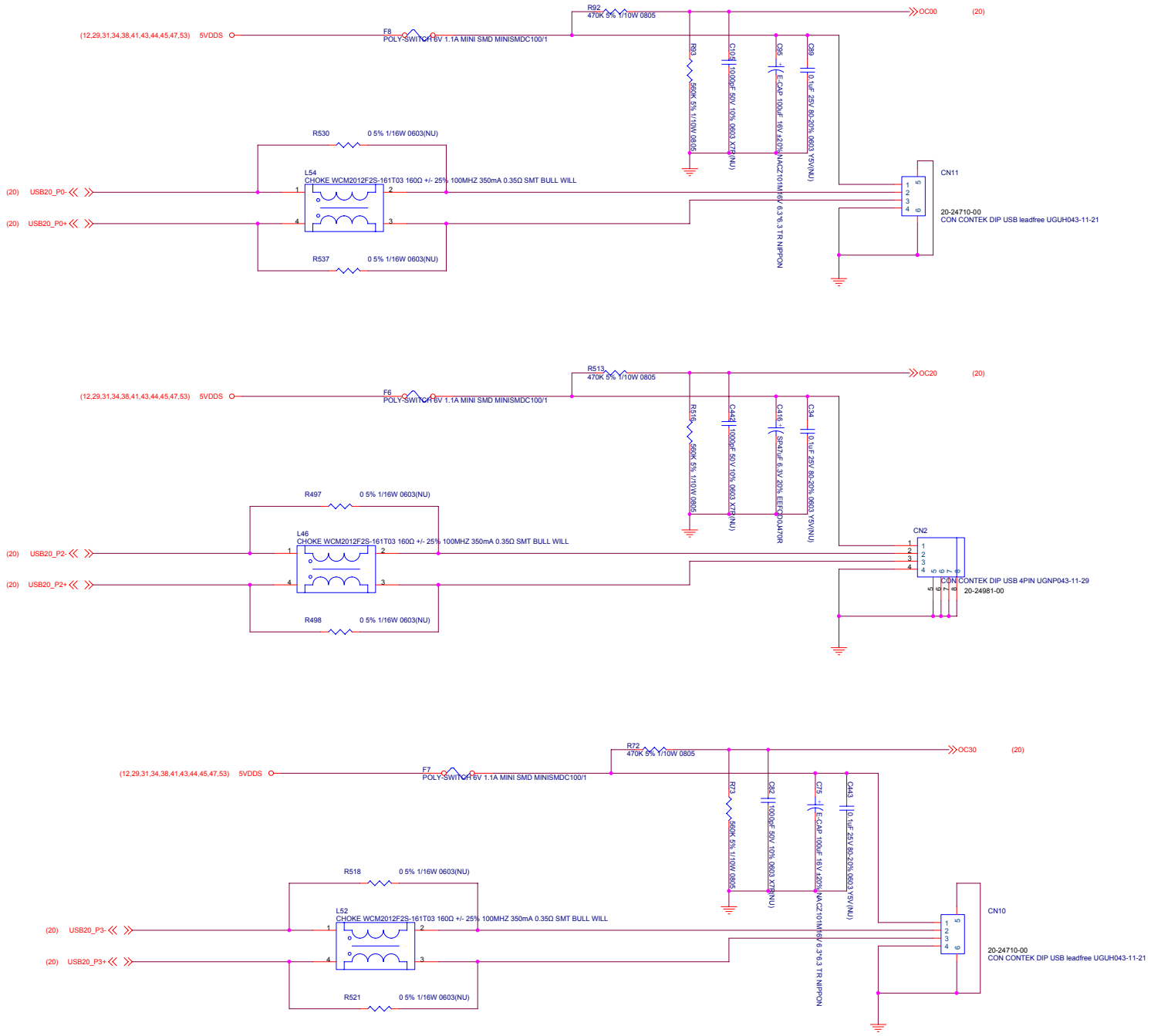
AT11 < Dothan + 915GM + ICH6-M >
PMU08
Thursday, April 14, 2005
Sheet 32 of 63



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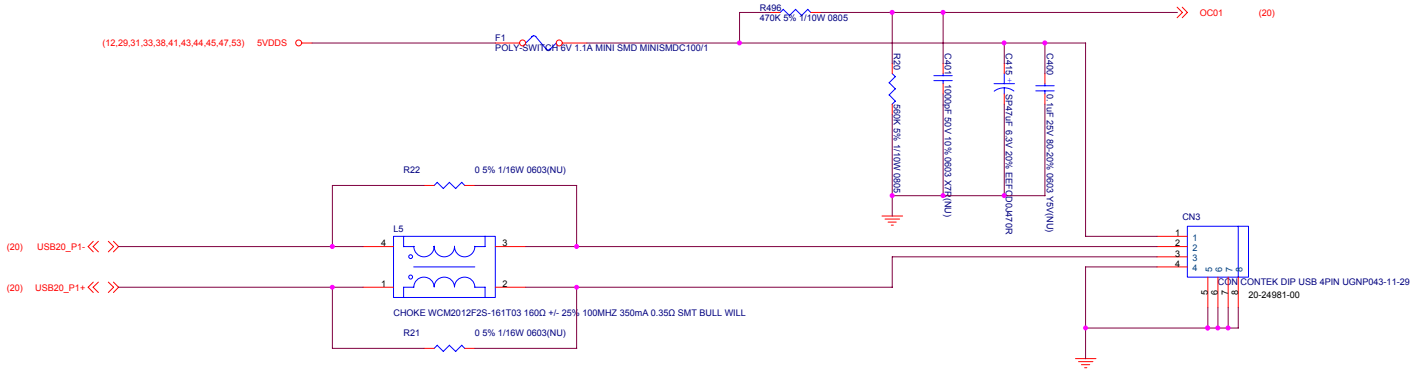
Title

AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	**USB CNN 1**	0.1

Date: Thursday, April 14, 2005 Sheet 33 of 63



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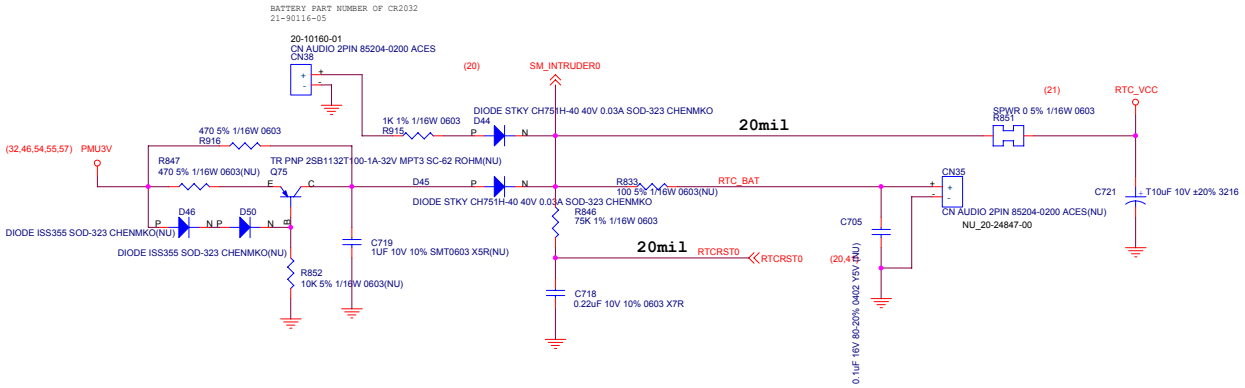
Title

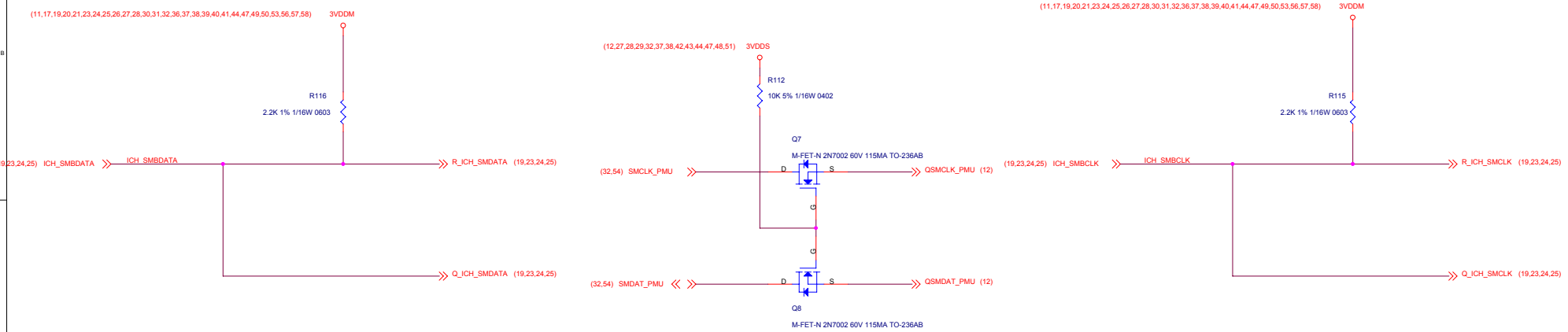
AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	**USB CNN2**	0.1

Date: Thursday, April 14, 2005 Sheet 34 of 63

RTC Discharge Circuit





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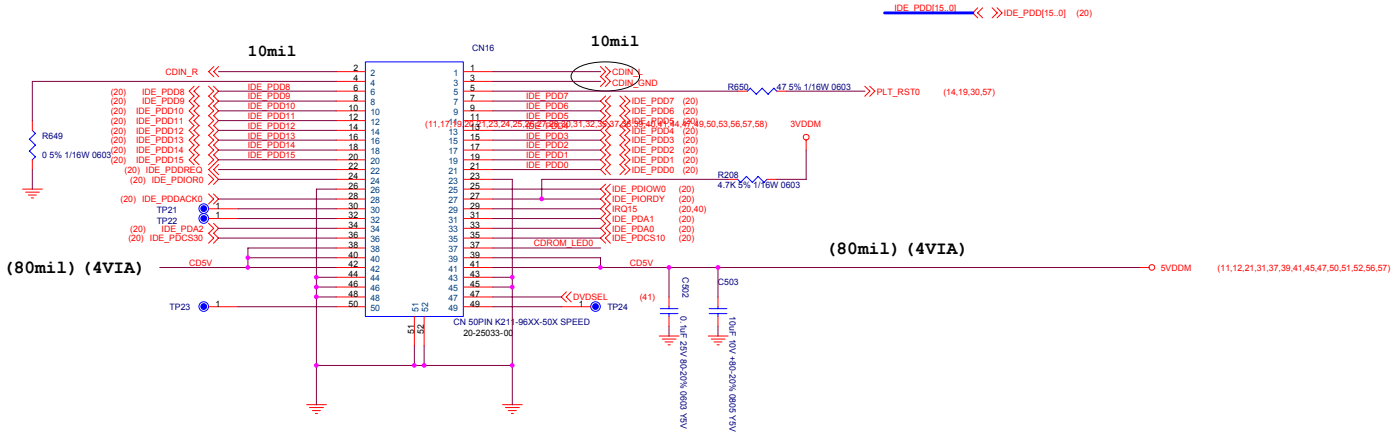
Title: **AT11 < Dothan + 915GM + ICH6-M >**

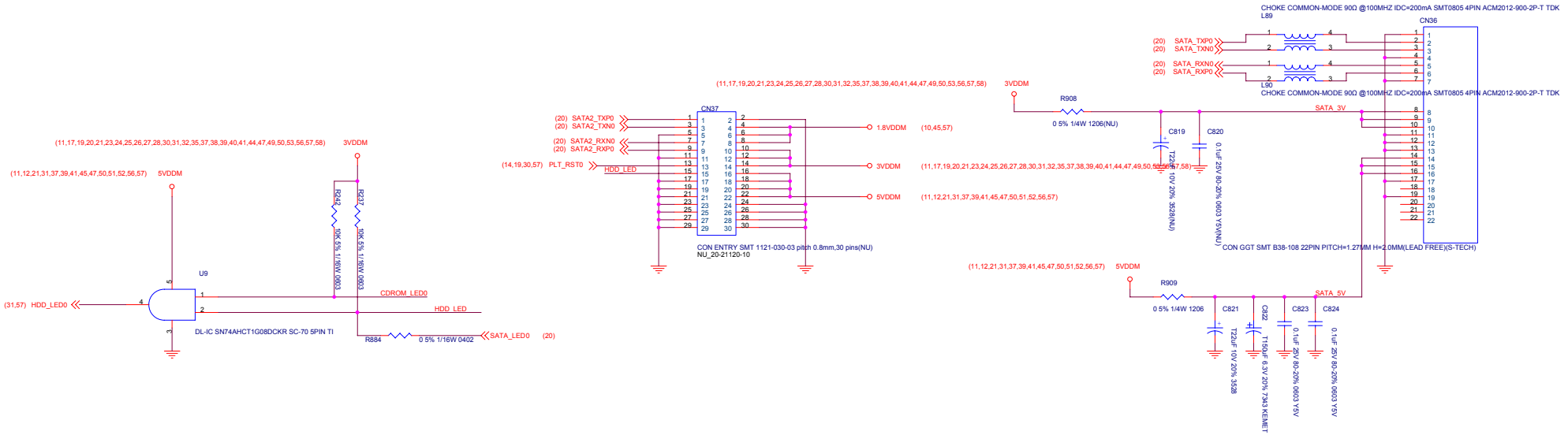
Size	Document Number	Rev
C	RTC / SMBUS	0.1

Date: Thursday, April 14, 2005 Sheet 35 of 63

CD-ROM CNN



HDD I/F



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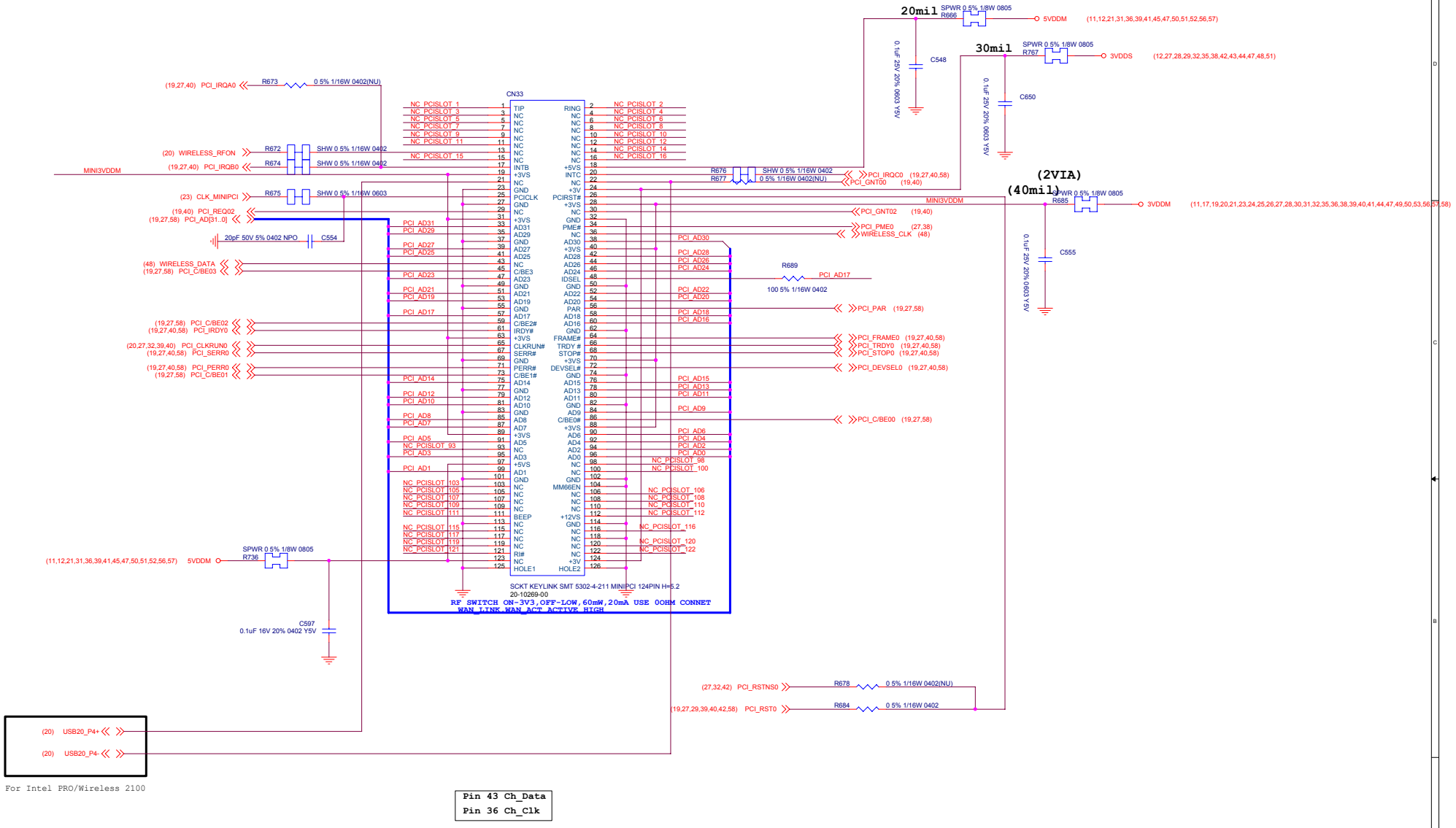
Title: **AT11 < Dothan + 915GM + ICH6-M >**

Size	Document Number	Rev
C	SATA /CD-ROM CNN	0.1

Date: Thursday, April 14, 2005 Sheet 36 of 63



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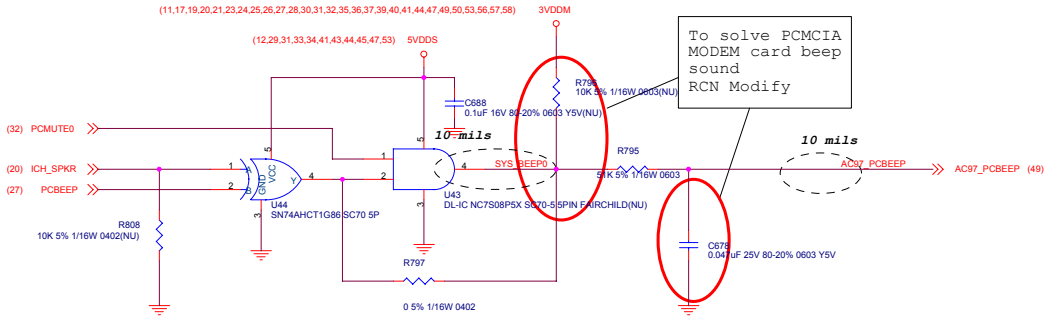
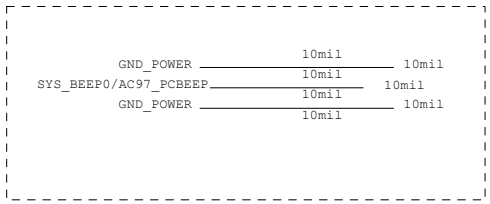
Title: AT11 < Dothan + 915GM + ICH6-M >

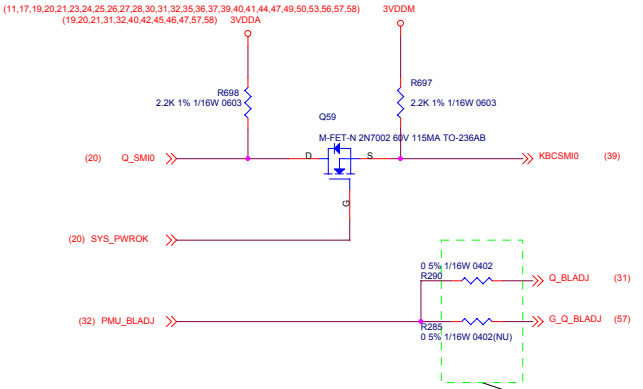
Size	Document Number	Rev
C	Calexico MINI PCI	0.1

Date: Thursday, April 14, 2005 Sheet 37 of 63

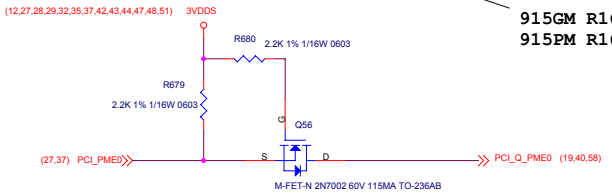
PCBEEP

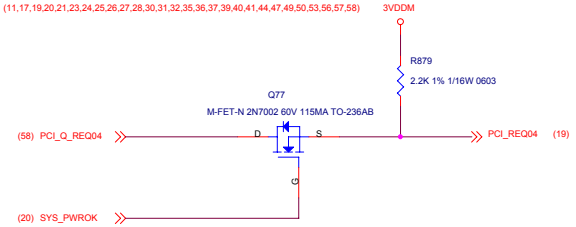






915GM R1630 0ohm; R1631 (NU)
915PM R1630 (NU); R1631 0ohm





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Title: AT11 < Dothan + 915GM + ICH6-M >

Size: C | Document Number: PCBEEP/SWITCH | Rev: 0.1

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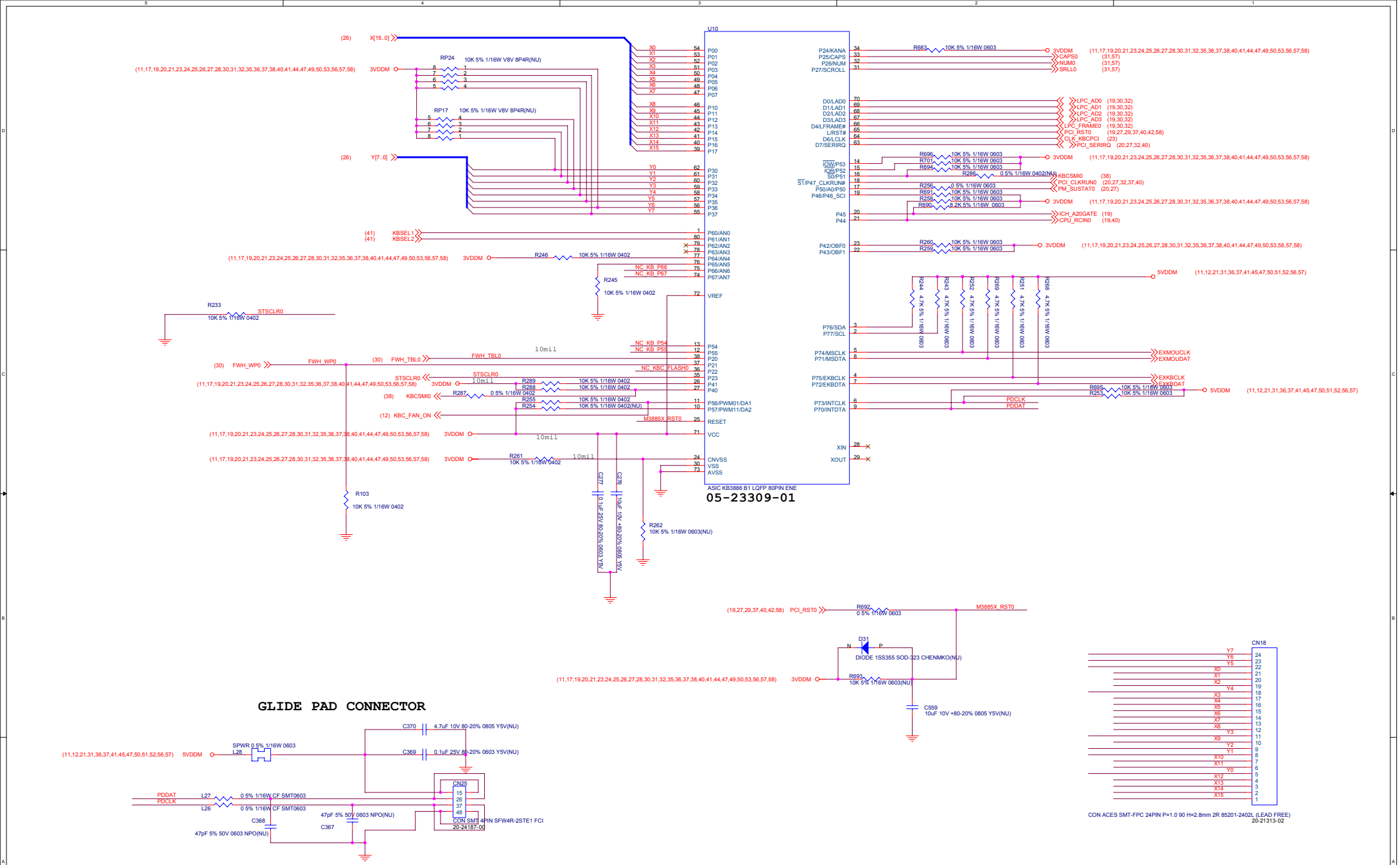

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Title: **AT11 < Dothan + 915GM + ICH6-M >**

Size	Document Number	Rev
C	**KBC M38869**	0.1

Date: Thursday, April 14, 2005 Sheet 39 of 63

PCI Pull Up/Down

(11,17,19,20,21,23,24,25,26,27,28,30,31,32,35,36,37,38,39,41,44,47,49,50,53,56,57,58) 3VDDM

RP20
1 8 PCI_FRAME0 (19,27,37,58)
2 7 PCI_STOP0 (19,27,37,58)
3 6 PCI_IRDY0 (19,27,37,58)
4 5 PCI_TRDY0 (19,27,37,58)
*RP 8.2KΩ 5% SMT3216 1/16W IE 8P4R

RP25
1 8 PCI_DEVSEL0 (19,27,37,58)
2 7 PCI_PERR0 (19,27,37,58)
3 6 PCI_SERR0 (19,27,37,58)
4 5 PCI_LOCK0 (19)
*RP 8.2KΩ 5% SMT3216 1/16W IE 8P4R

R840 8.2K 1% 1/16W 0603 PCI_RST0 (19,27,29,37,39,42,58)

R416 10K 5% 1/16W 0402 PCI_SERIRQ (20,27,32,39)

RP23
1 8 PCI_IRQB0 (19,27,37)
2 7 PCI_IRQD0 (19)
3 6 PCI_IRQC0 (19,27,37,58)
4 5 PCI_IRQA0 (19,27,37)
*RP 8.2KΩ 5% SMT3216 1/16W IE 8P4R

RP22
1 8 PCI_GNT04 (19,58)
2 7 PCI_GNT03 (19)
3 6 PCI_GNT01 (19,27)
4 5 PCI_GNT02 (19,37)
*RP 8.2KΩ 5% SMT3216 1/16W IE 8P4R(NU)

RP21
1 8 PCI_REQ01 (19,27)
2 7 PCI_REQ03 (19)
3 6 PCI_REQ02 (19,37)
4 5 PCI_REQ00 (19)
10K 5 % 0402X4 1/16W 8P4R

R667 10K 5% 1/16W 0402 LVDS_ENABKL (13,31)

R207 8.2K 5% 1/16W 0402 IRQ15 (20,36)

R421 8.2K 1% 1/16W 0603(NU) PCI_GNT00 (19,37)

LPC Pull Up

(11,17,19,20,21,23,24,25,26,27,28,30,31,32,35,36,37,38,39,41,44,47,49,50,53,56,57,58) 3VDDM

R830 10K 5% 1/16W 0603(NU) LPC_DRQ00 (19)
R829 10K 5% 1/16W 0603(NU) LPC_DRQ10 (19)

PCI PMU Pull Up

(19,20,21,31,32,38,42,45,46,47,57,58) 3VDDA

R681 10K 5% 1/16W 0603(NU) PCI_Q_PME0 (19,38,58)

(11,17,19,20,21,23,24,25,26,27,28,30,31,32,35,36,37,38,39,41,44,47,49,50,53,56,57,58) 3VDDM

R417 8.2K 1% 1/16W 0603 PCI_CLKRUN0 (20,27,32,37,39)
R257 10K 5% 1/16W 0402 CPU_RCIN0 (19,39)

AC97 Pull Down

R143 10K 5% 1/16W 0603(NU) AC97_BITCLK (20,48,49)

(11,17,19,20,21,23,24,25,26,27,28,30,31,32,35,36,37,38,39,41,44,47,49,50,53,56,57,58) 3VDDM

GPIO Pull Up

R326 8.2K 1% 1/16W 0603 PANEID0 (19)
R325 8.2K 1% 1/16W 0603 PANEID1 (19)

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Title: AT11 < Dothan + 915GM + ICH6-M >

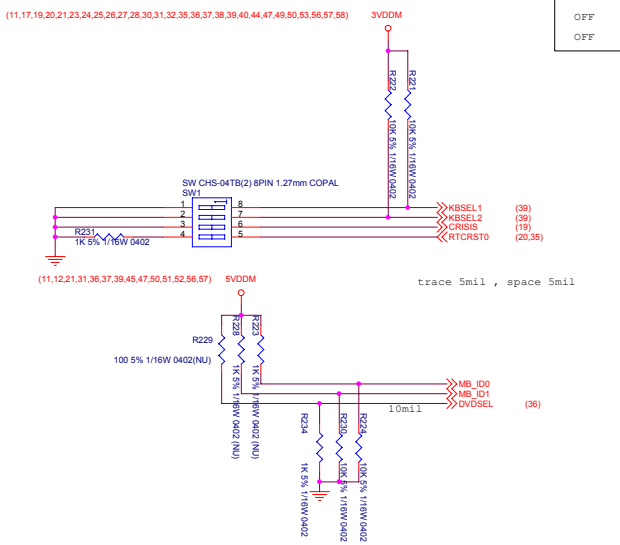
Size: C | Document Number: PCI / LPC / GPIO Pull Up/Down | Rev: 0.1

Date: Thursday, April 14, 2005 | Sheet 40 of 63

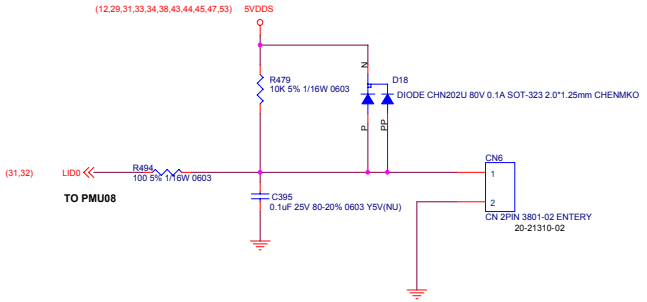
DIP SWITCH

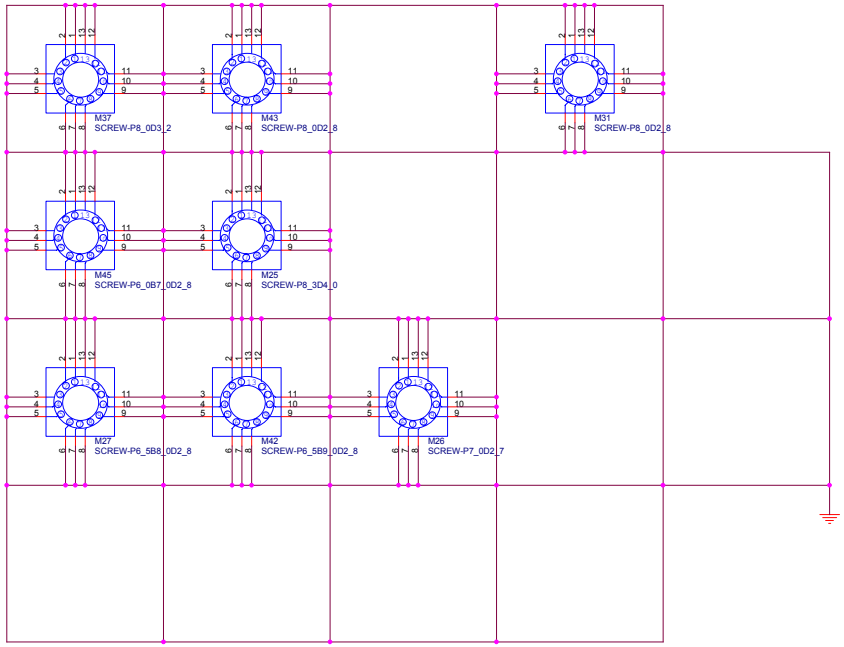
KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

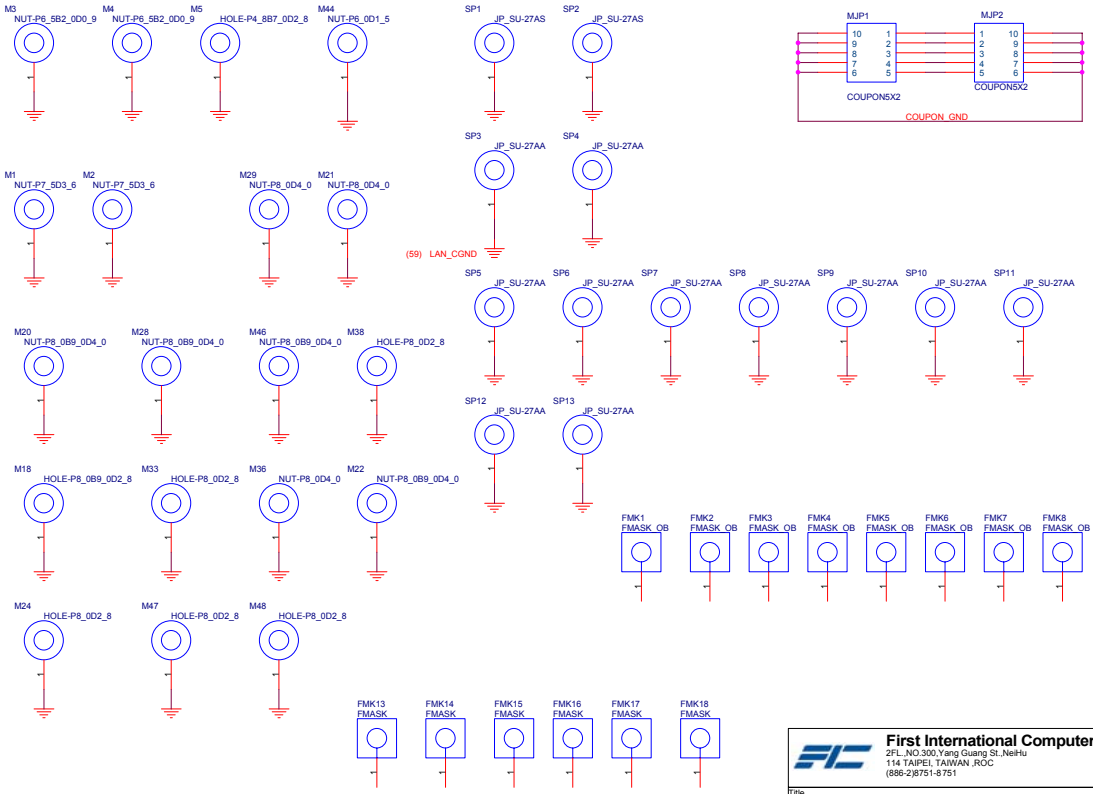
MB_ID0	ON	Reserved
	OFF	Reserved
LOGSEL	ON	Reserved
	OFF	Reserved
PASS0	ON	Override
	OFF	Available
DVDSEL	ON	CD-ROM
	OFF	DVD
CMOS_CLEAR	ON	Reset RTC
	OFF	NONE



LID Switch







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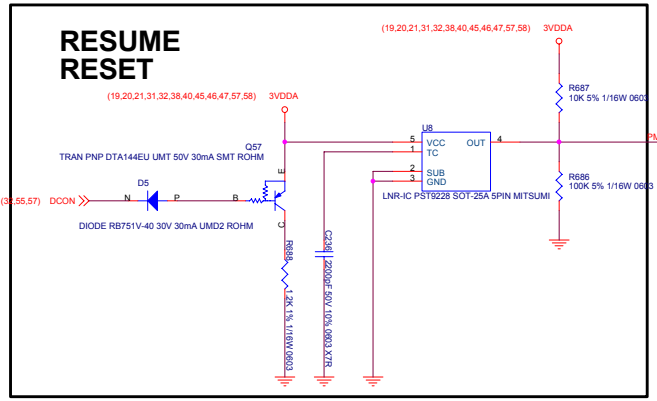
Title: **AT11 < Dothan + 915GM + ICH6-M >**

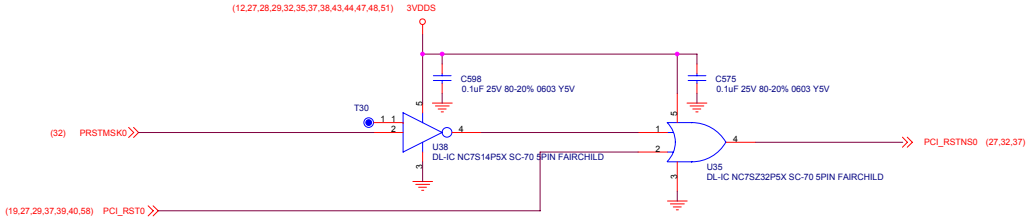
Size: C | Document Number: **DIP/LID SW; SCREW** | Rev: 0.1

Date: Thursday, April 14, 2005 | Sheet 41 of 63



WORKAROUND FOR POWER CONTROL SIGNAL

PCI RESET & PCI NON RESET



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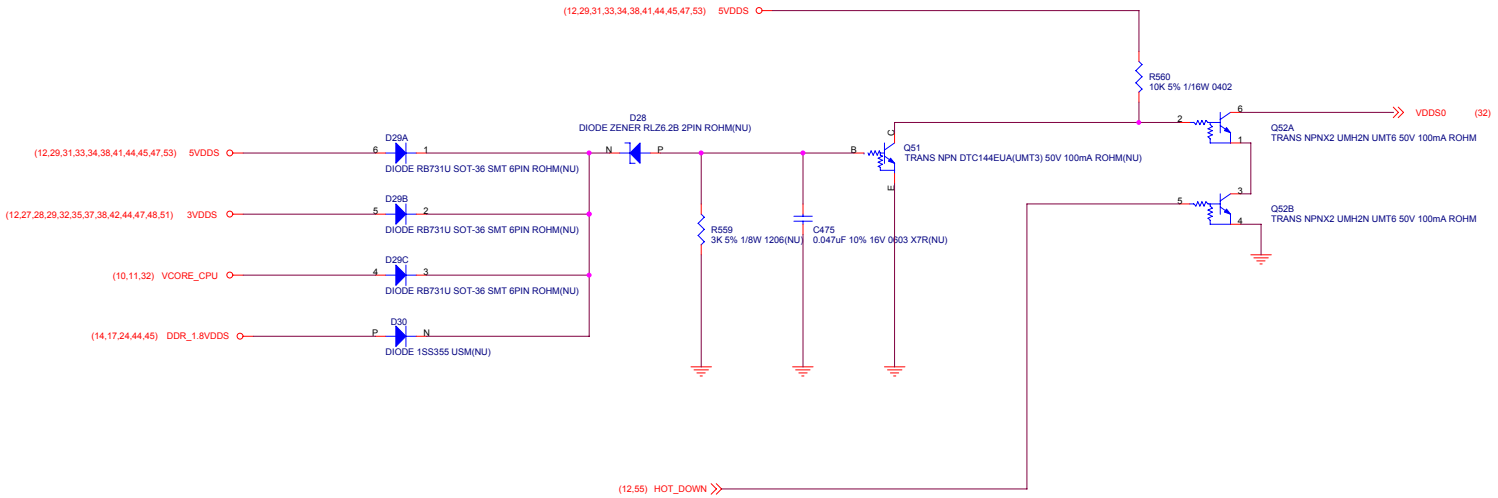
Title: AT11 < Dothan + 915GM + ICH6-M >

Size: C | Document Number: Reset Control Logic | Rev: 0.1

Date: Thursday, April 14, 2005 | Sheet 42 of 63

SYSTEM POWER OVP



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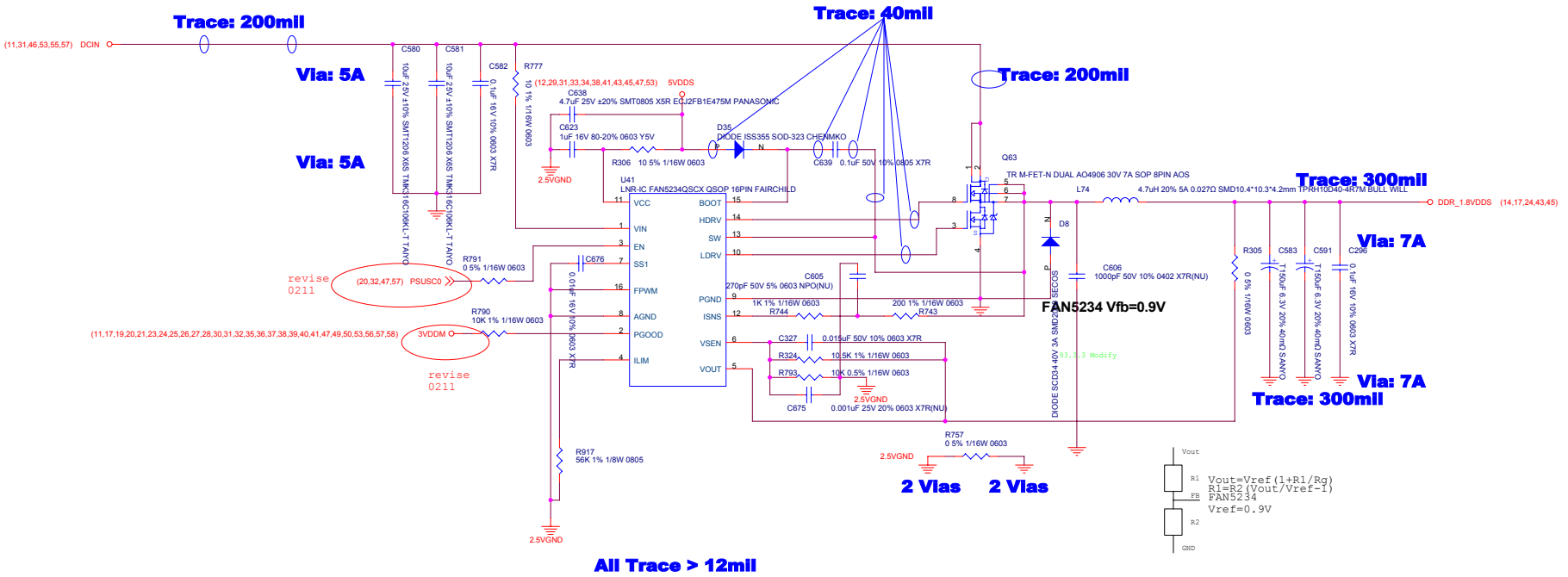
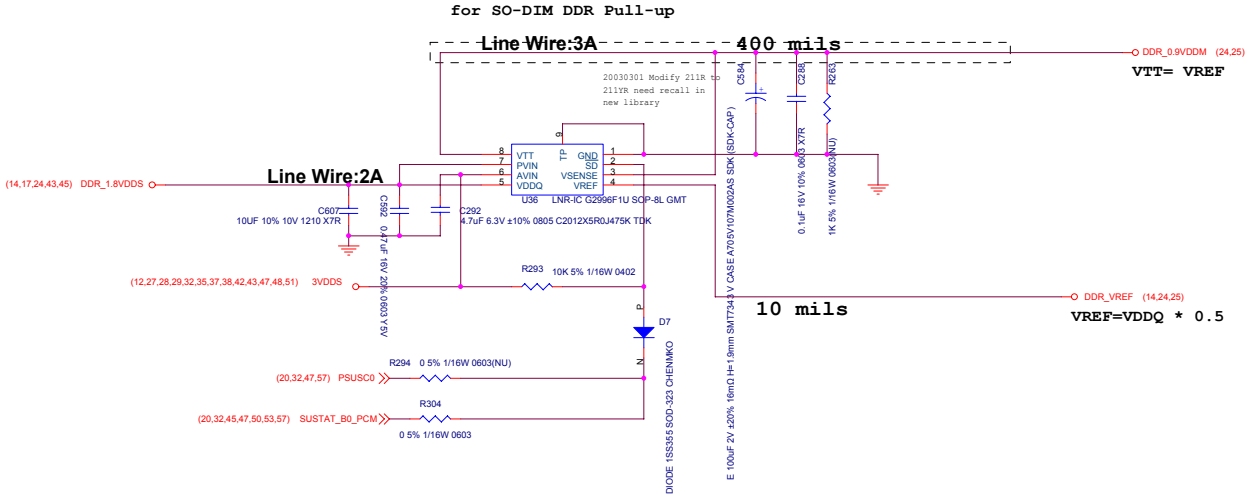
Title
AT11 < Dothan + 915GM + ICH6-M >

Size	Document Number	Rev
C	**Over Voltage Protect**	0.1

Date: Thursday, April 14, 2005 Sheet 43 of 63

DDR POWER





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Title: AT11 < Dothan + 915GM + ICH6-M >		
Size: C	Document Number: DDR2 POWER	Rev: 0.1
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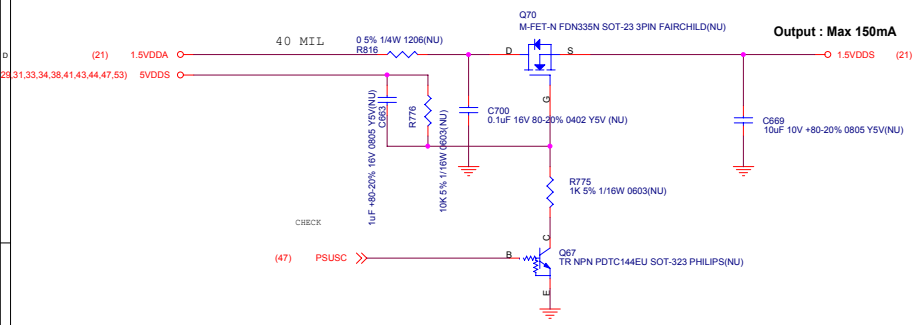
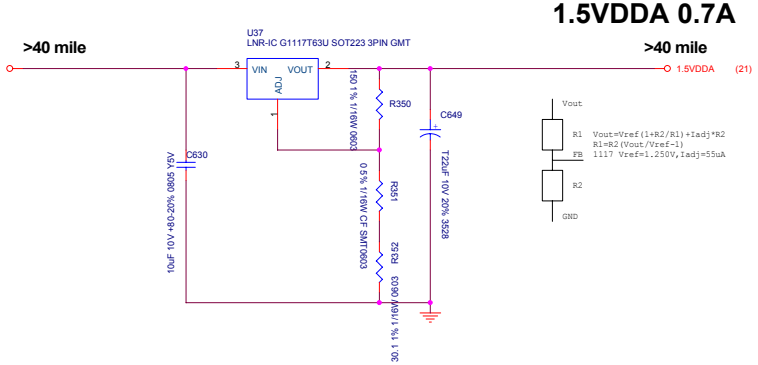
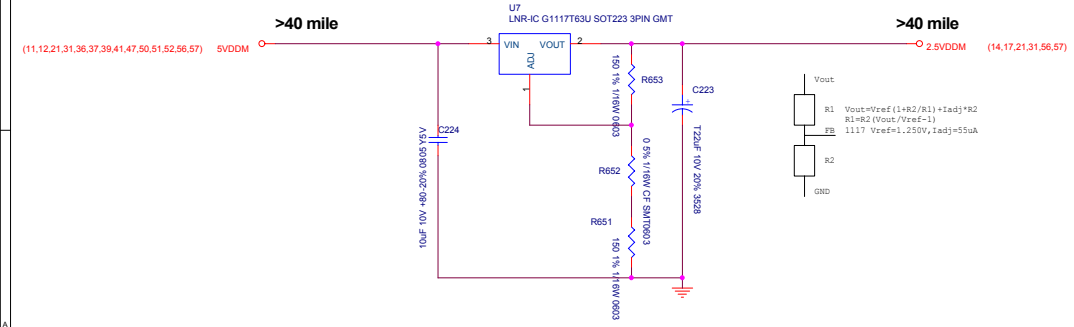
1.5VDDS 0.2A



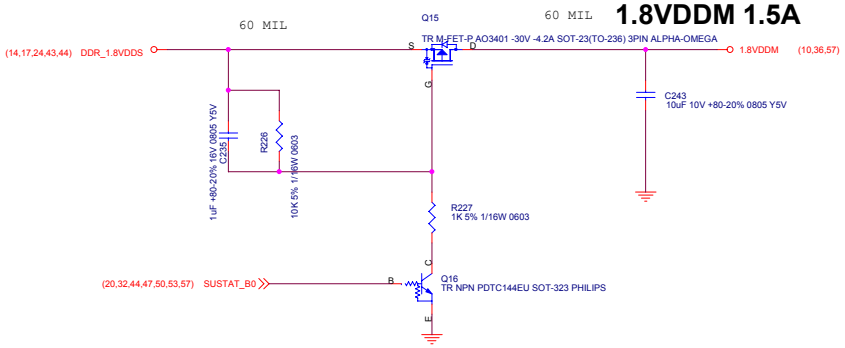
1.5VDDA 0.7A



2.5VDDM 0.6A



1.8VDDM 1.5A



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Size: C | Document Number: 1.5VDDA/S/M,1.8VDDM,2.5VDDM | Rev: 0.1

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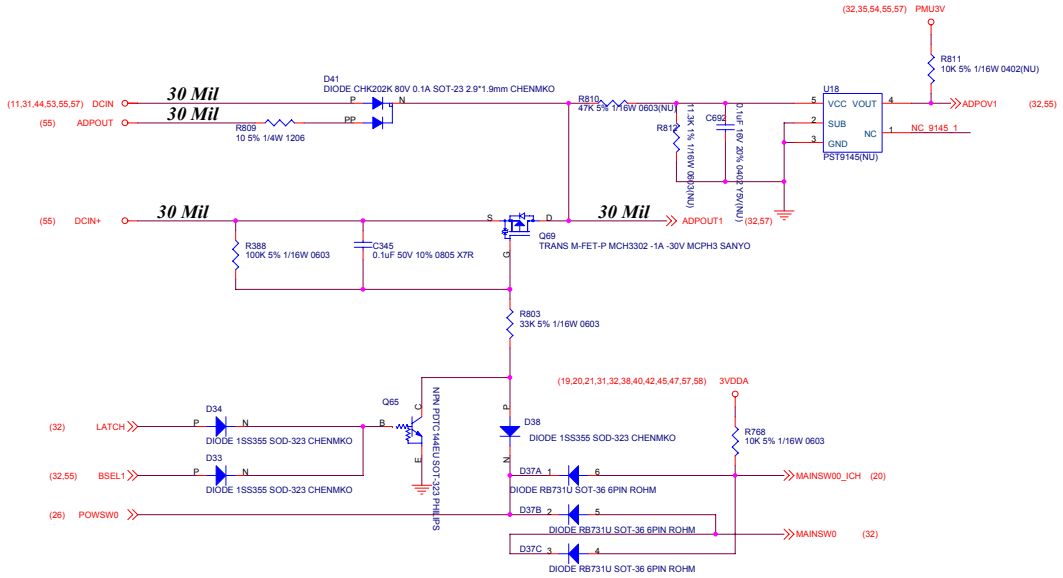

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Title
AT11 < Dothan + 915GM + ICH6-M >

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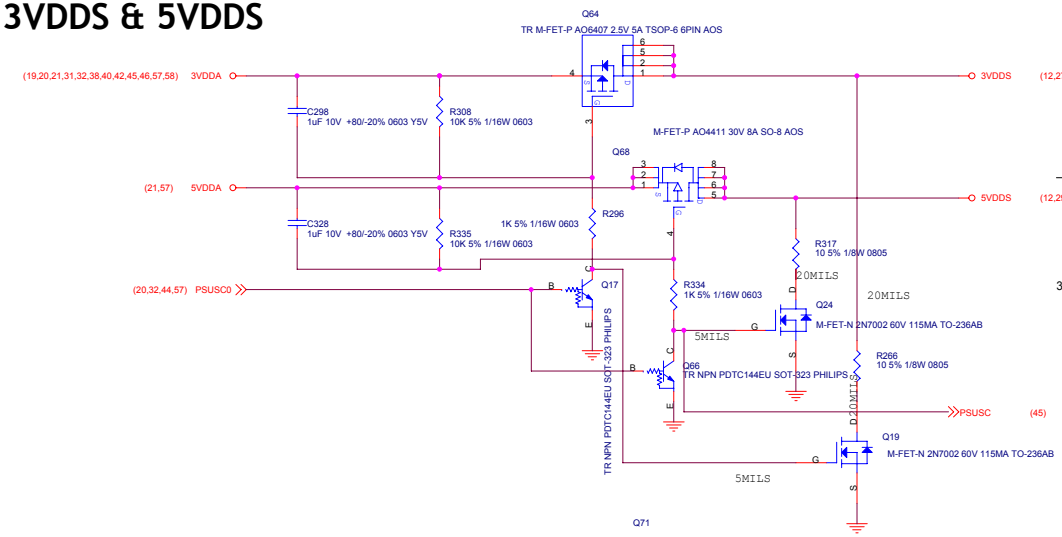
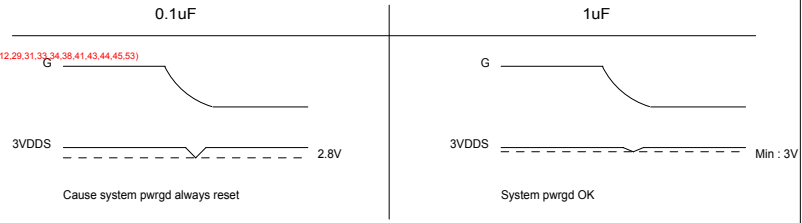
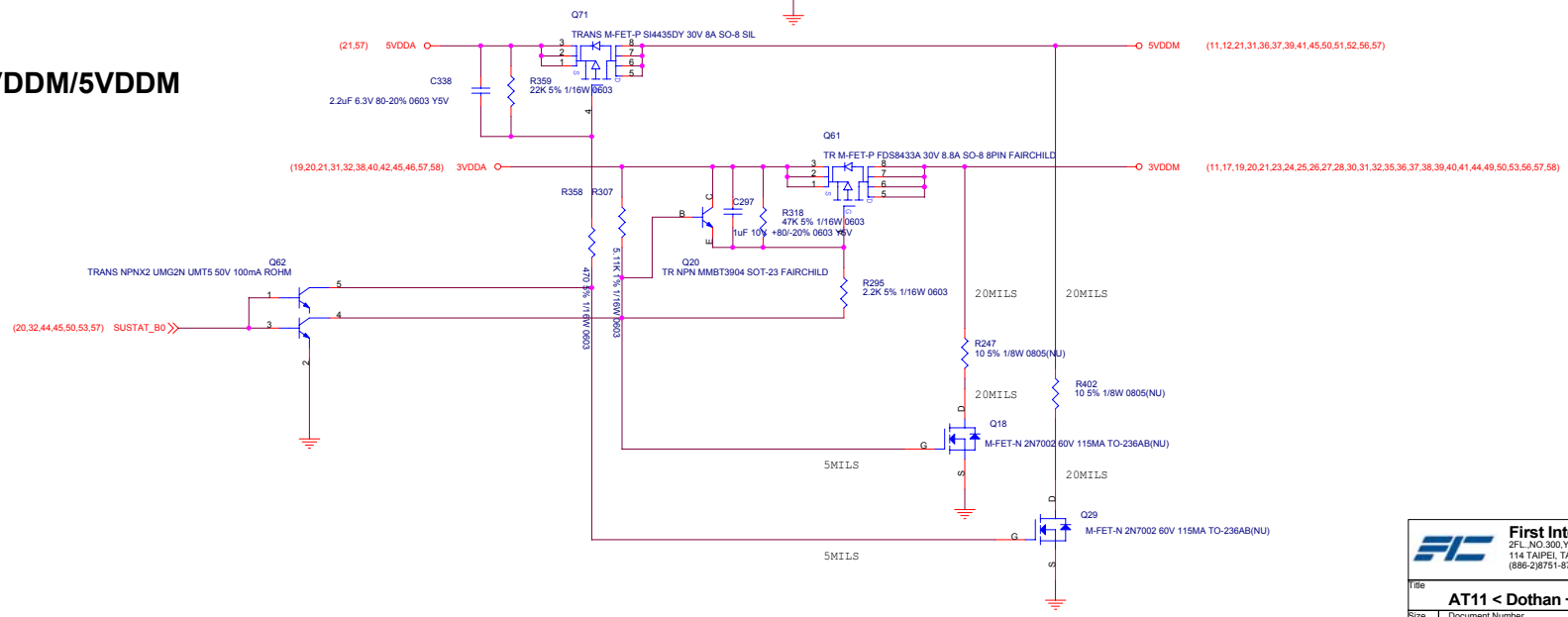
3VDDS & 5VDDS





3VDDM/5VDDM



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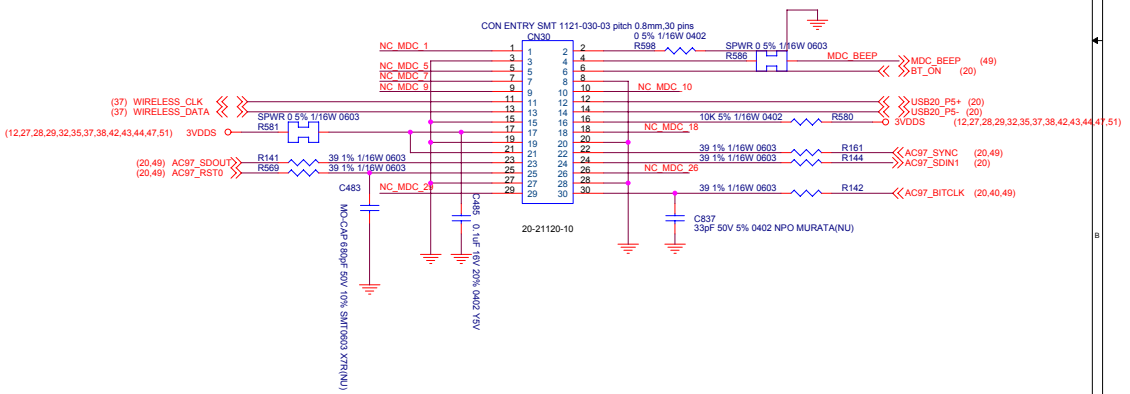
MDC CNN



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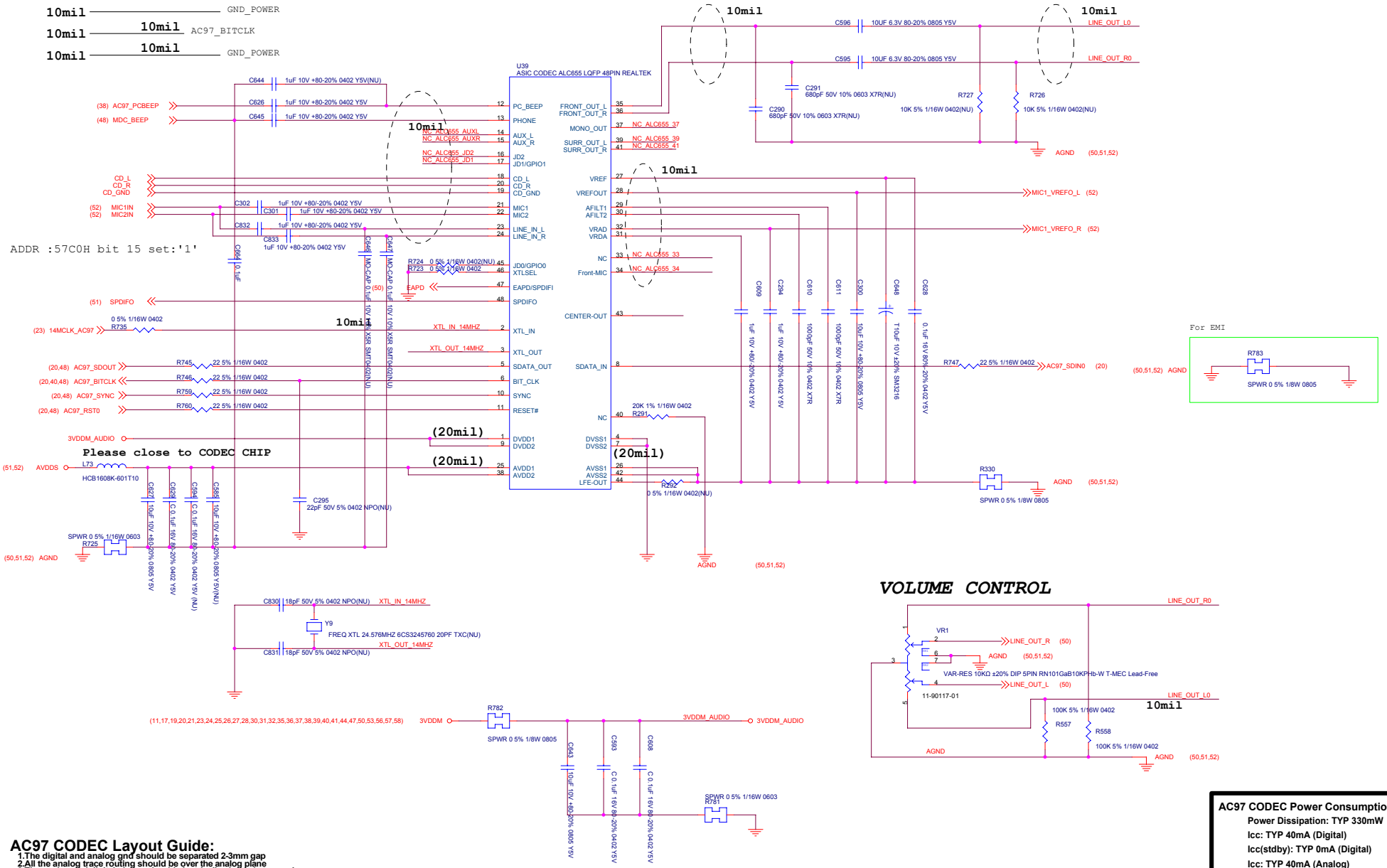
AC97/AZALIA CODEC DUAL LAYOUT

AC97 USE ALC655 / AZALIA(RESERVE)

10mil GND_POWER
10mil AC97_PCBEEP 10mil
10mil GND_POWER 10mil
10mil GND_POWER
10mil 14MCLK_AC97 10mil
10mil GND_POWER 10mil
10mil GND_POWER
10mil AC97_BITCLK 10mil
10mil GND_POWER 10mil



AC97 CODEC Layout Guide:

1. The digital and analog gnd should be separated 2-3mm gap
2. All the analog trace routing should be over the analog plane
3. The analog and digital planes should electrically shorted at one place
4. All supply high frequency decoulping ,reference high freguency decoulp and filter caps must be routed on the same layer as the codec
5. Analog I/O routing should be kept a short as possible
6. Analog I/O routing should be shielding with analog ground traces
7. Use of ground plane fill and the copper fill should be shorted to the analog ground plane
8. The AC-link signal should be as short as possible
9. AC-link clock signal should have a series resistor close to the codec
10. The AC-link signal should be shielding with ground
11. Split analog and digital ground planes and 2-3mm
12. Analog signals only over analog ground plane
13. Digital signals only over digital ground plane
14. Locate analog section away from high speed digital circuits
15. Place smallest bypass capacitor closest to IC pin
16. Use metal film resistors and NPO capacitors in analog path
17. The Audio signals trace width is 12mil or more

AC97 CODEC Power Consumption:

- Power Dissipation: TYP 330mW
- Icc: TYP 40mA (Digital)
- Icc(stdby): TYP 0mA (Digital)
- Icc: TYP 40mA (Analog)
- Icc(stdby): TYP 0.13mA (Analog)

A_GND 10mil 10mil
LINE_OUT_L 10mil 10mil
A_GND 10mil 10mil
LINE_OUT_R 10mil 10mil
A_GND 10mil 10mil

CD_GND 10mil 10mil
CD_L 10mil 10mil
CD_GND 10mil 10mil
CD_R 10mil 10mil
CD_GND 10mil 10mil

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Size	Document Number	Rev
C	AC97 CODEC (ALC655)	0.1

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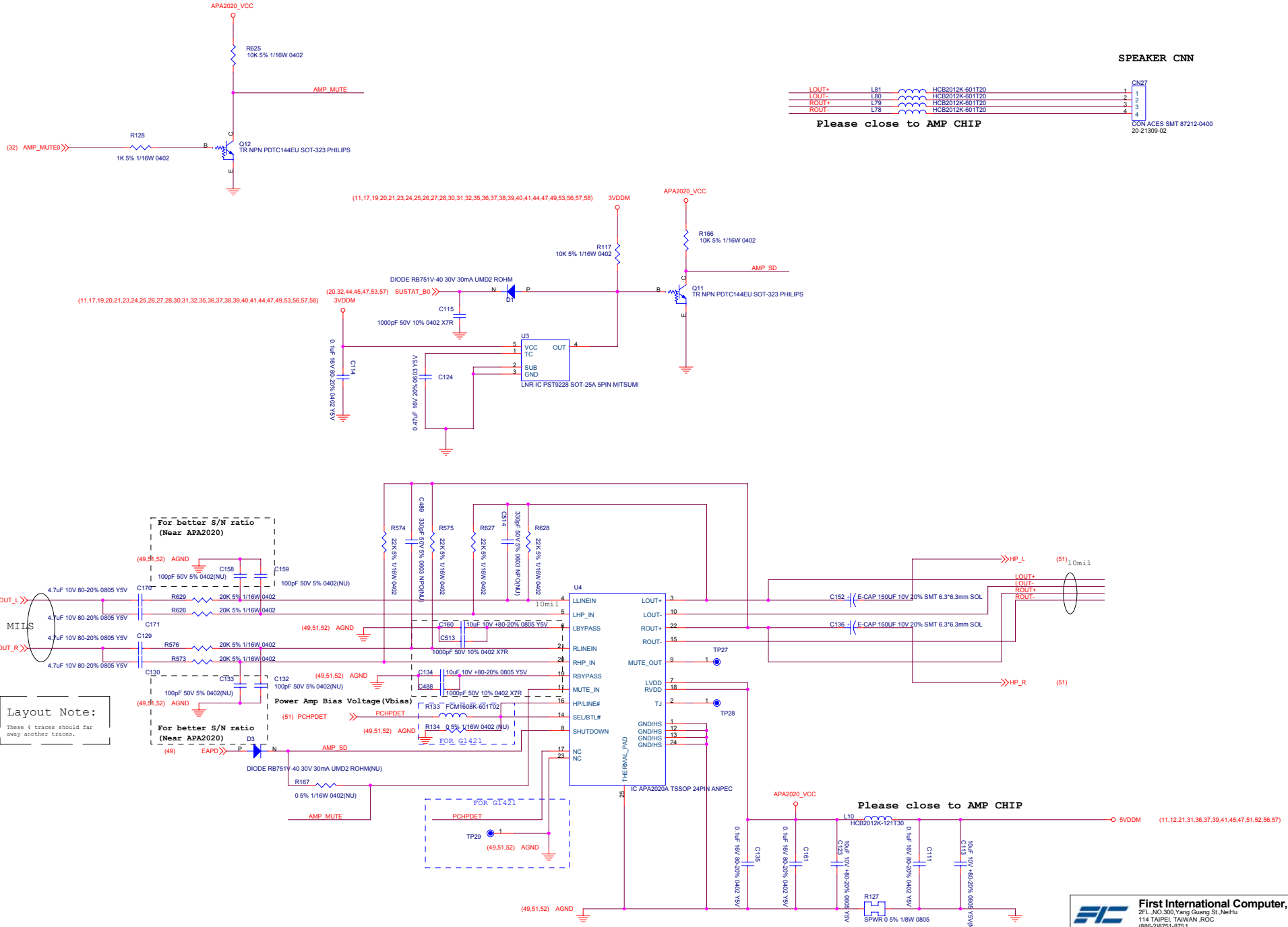

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Title	AT11 < Dothan + 915GM + ICH6-M >	
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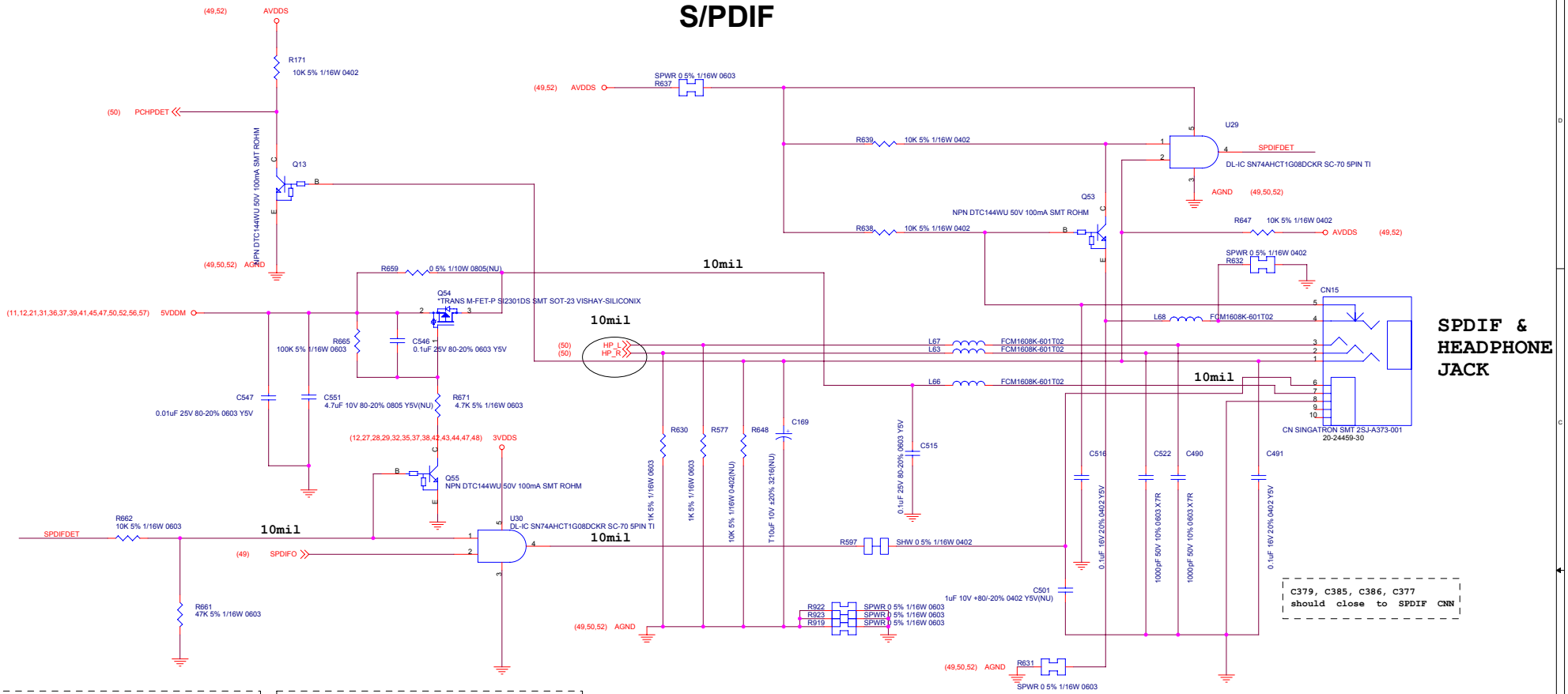
S/PDIF



SPDIF & HEADPHONE JACK

C379, C385, C386, C377 should close to SPDIF CNN

10mil

AGND
LOUT+
AGND
LOUT-
AGND

10mil

AGND
LINE_OUT_L
AGND
LINE_OUT_R
AGND

10mil

AGND
ROUT+
AGND
ROUT-
AGND

10mil

AGND
A_HP_L
AGND
A_HP_R
AGND

10mil

GND_POWER
SYS_BEEP0/AC97_PCBEEP
GND_POWER

10mil

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Size: C | Document Number: Headphone / SPDIF | Rev: 0.1

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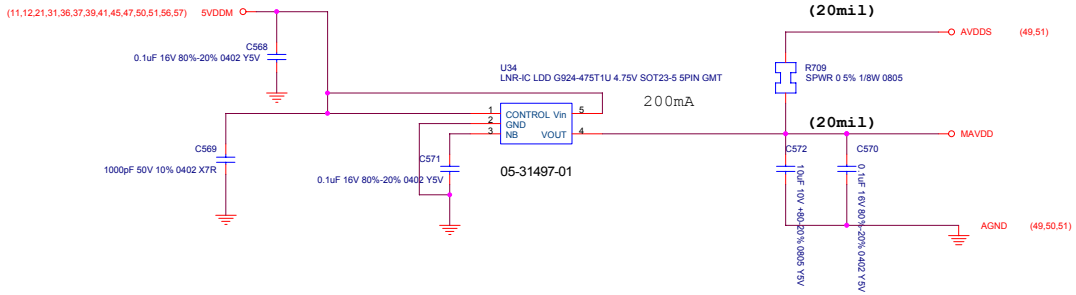

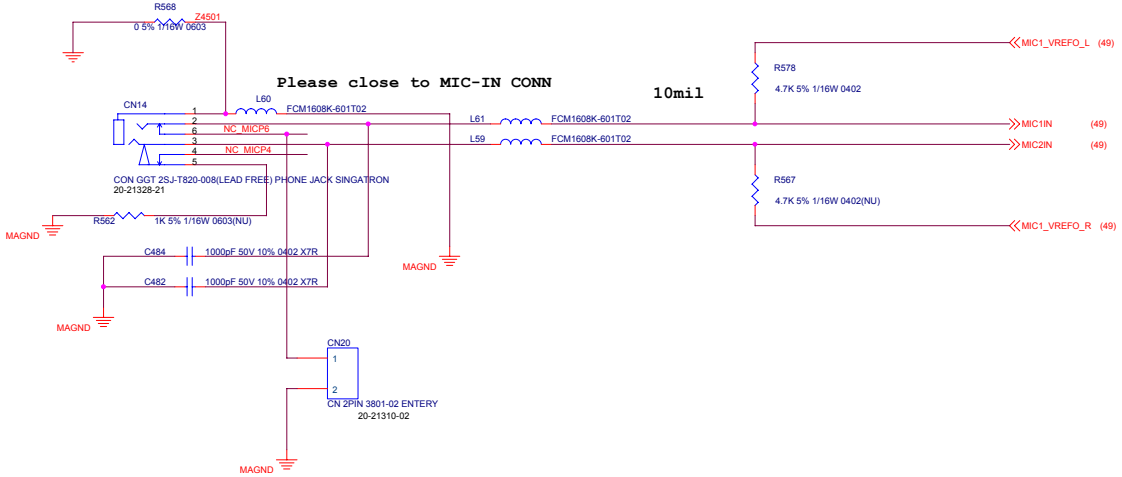

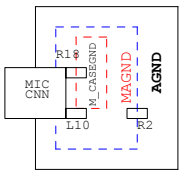

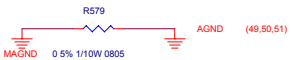

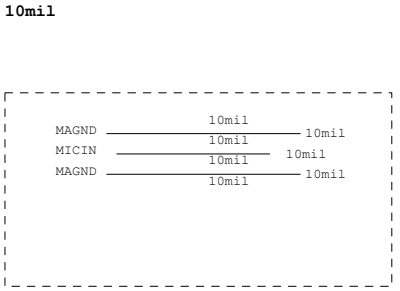

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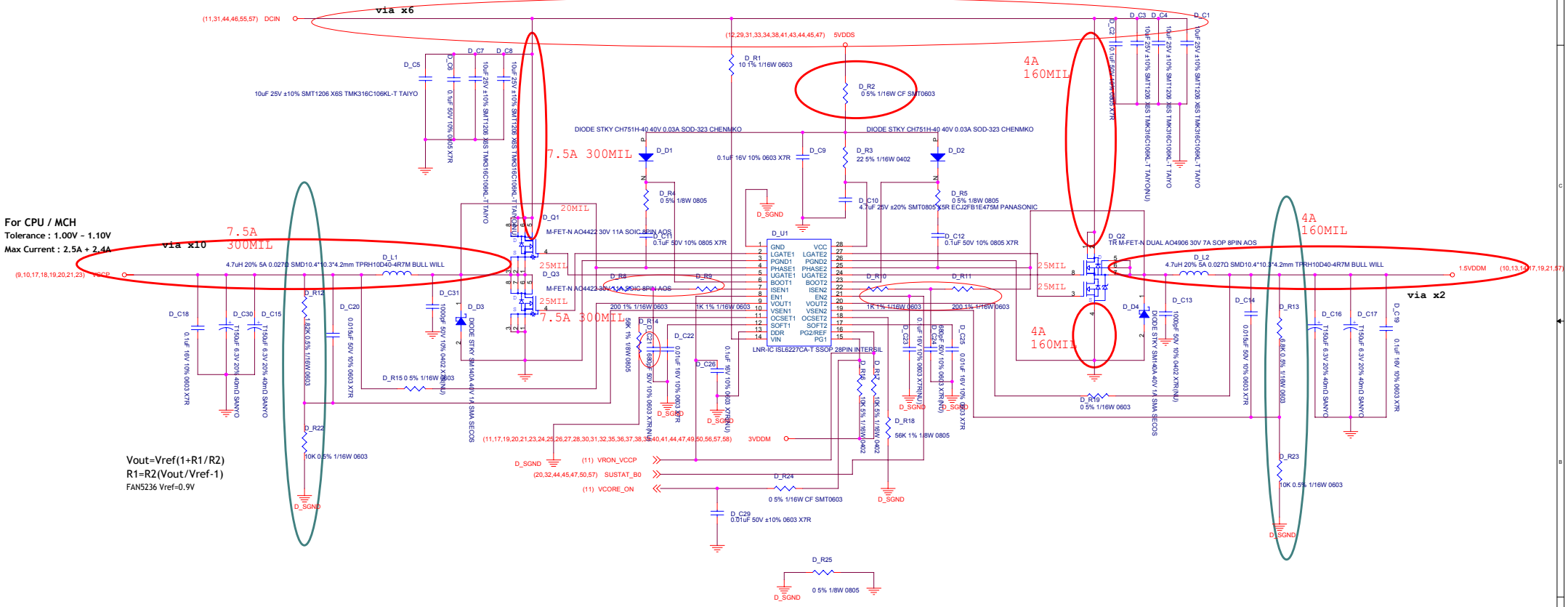
VCCP ,VORE_GMCH

25mil



DDR_1.8VDDS Setting
RDS(on)=32m ,I(max)=3A
1. Rsense={[Iload(max)*RDS(on)]/[150uA]}-100
=[[3A*32m]/150uA]-100
=640
2. Ilimit=1.2*1.25*1.6*3A=7.2A
3. Rlimit=[11.2*(100+Rsense)]/[Ilimit*RDS(on)]
=[11.2*(100+640)]/[7.2*32m]
=35.9K

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Size: C	Document Number: VCCP/1.5VDDM	Rev: 0.1
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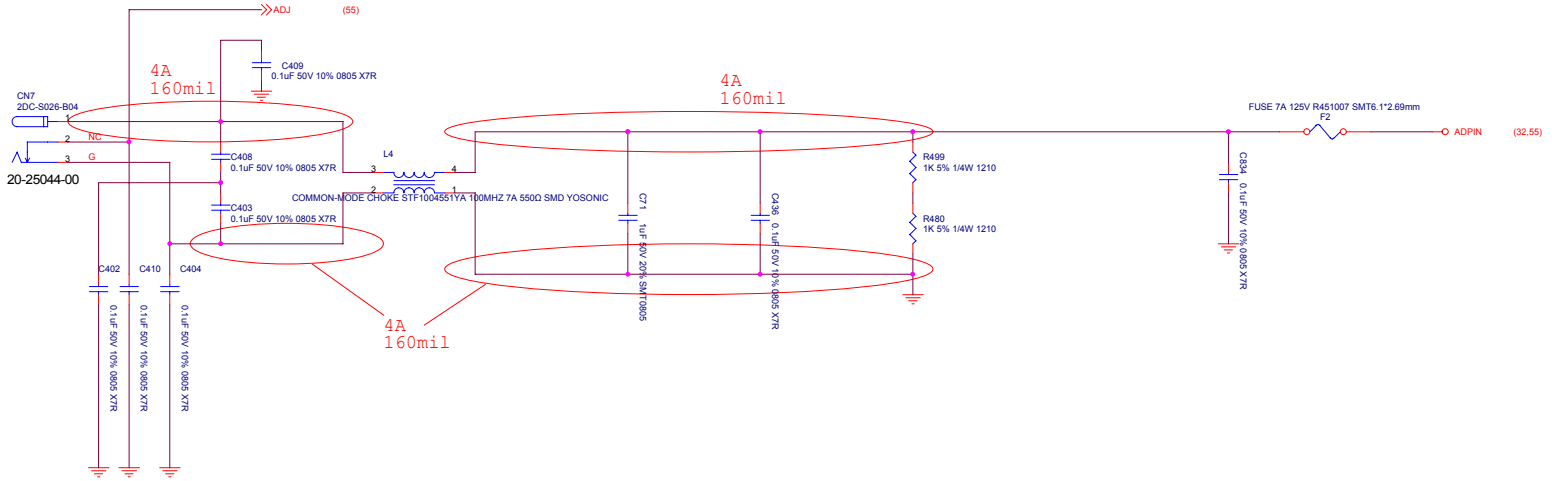
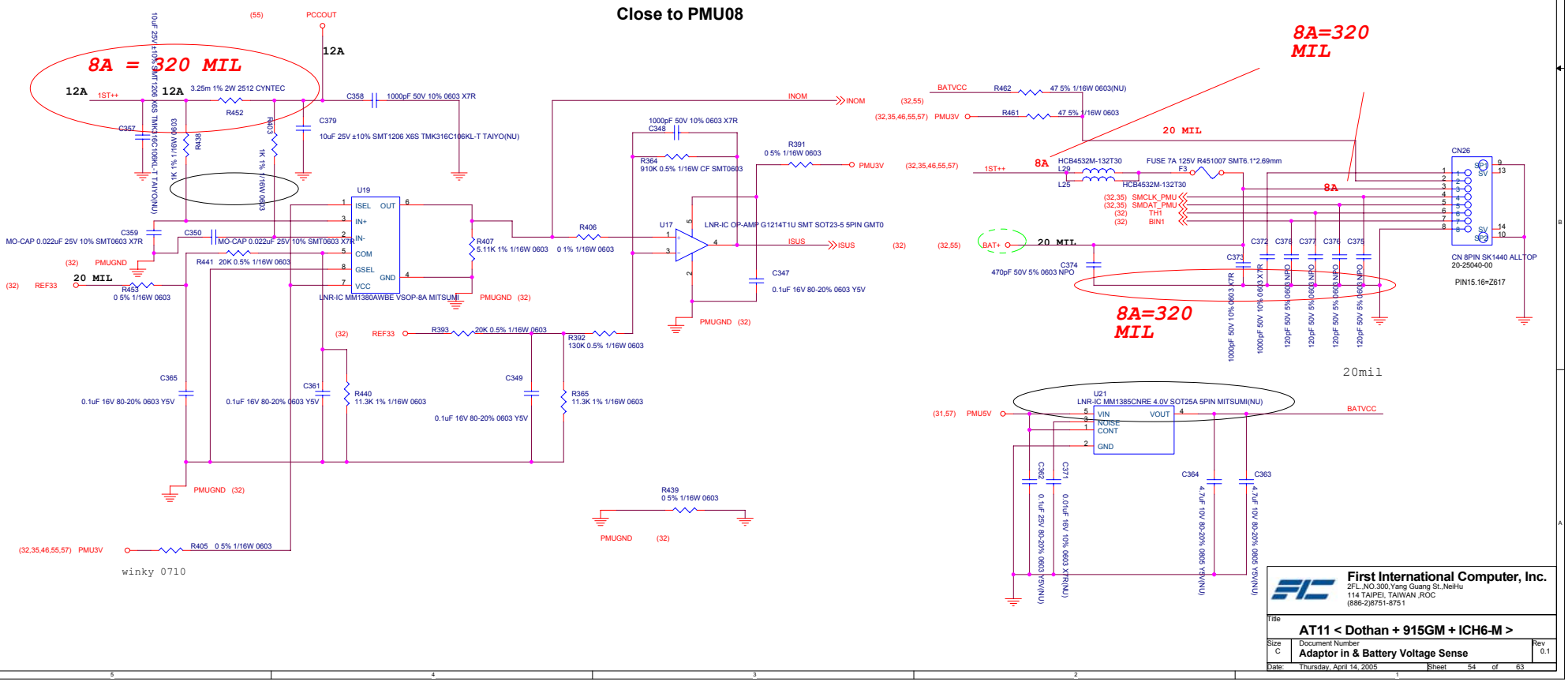


CHR Board BATTERY IN



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Title	AT11 < Dothan + 915GM + ICH6-M >	
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V_+INE2

0422 MODIFY TO 1000P X 3 EMI

CGDTEN point 115W and 300mA

Charge CGDTEN normal H Over Power L

5A 200mil

2A 80mil

5A 200mil

MB3887 Vref=5V
Charge current
= R27/(R1+R2)*5

Total power setting
V_+INE2 = Rsys * Isys * 20

12A 480mil

12A 480mil

(40mil)
2.5V 150mA

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Title	AT11 < Dothan + 915GM + ICH6-M >
Size	C
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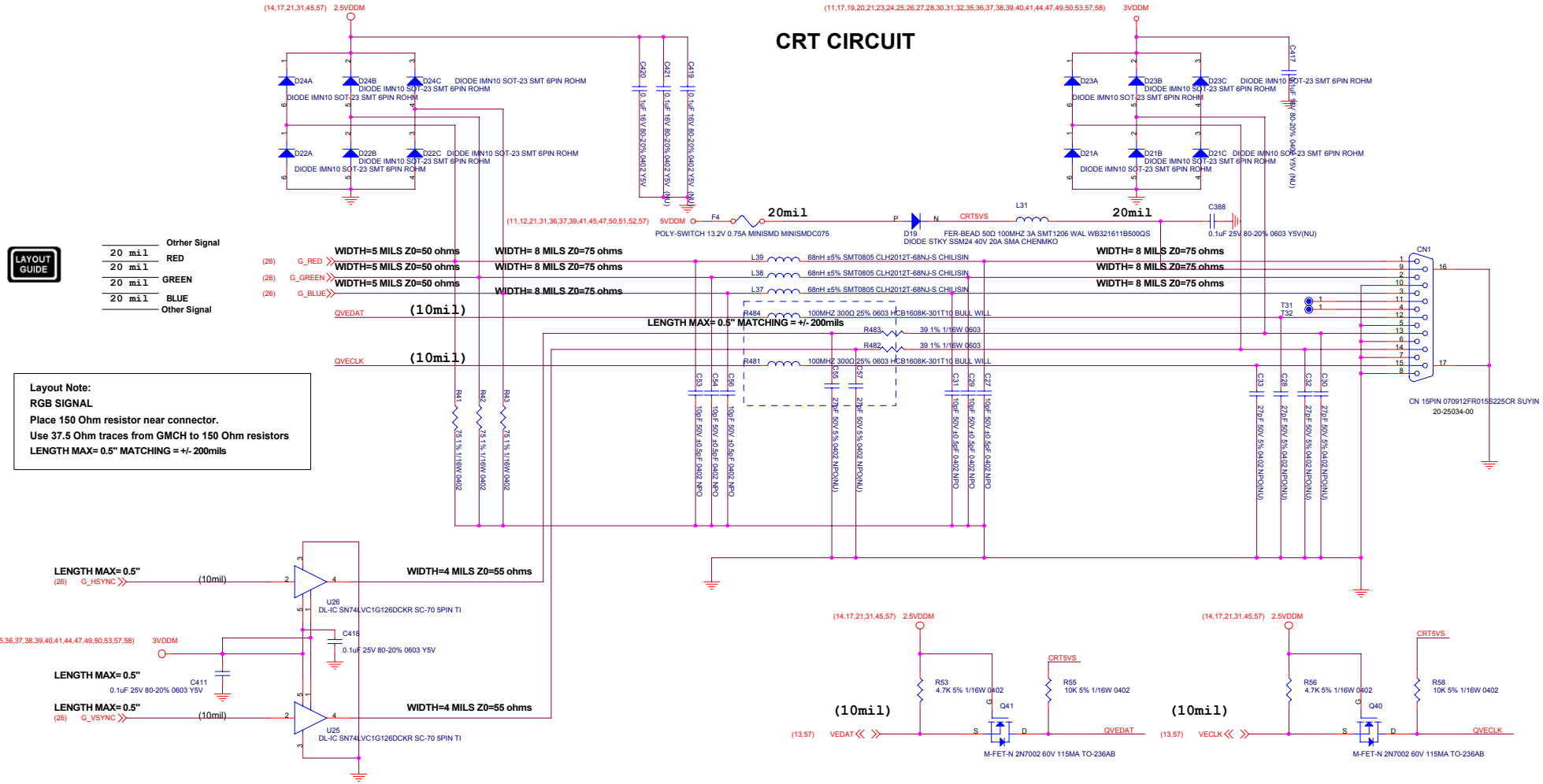
CRT CIRCUIT



Layout Note:

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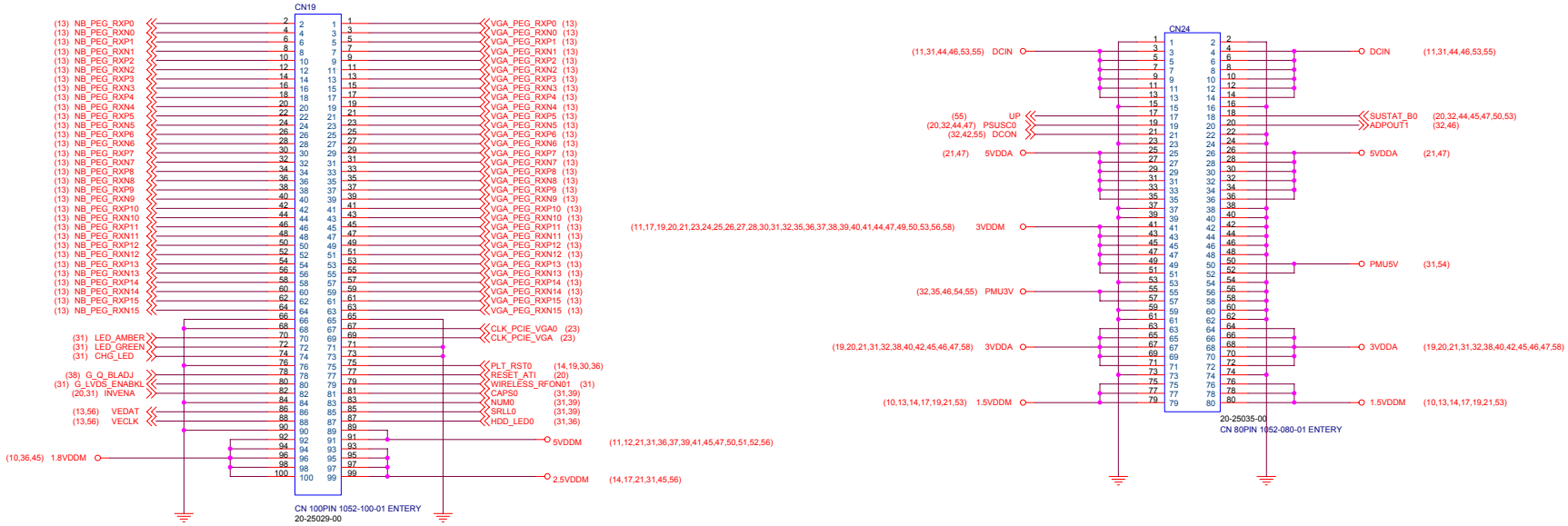
Strobe to Strobe 8 mils



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(886-2)2600-8818

Title: **AT11 (DOTHAN + 915PM + ICH6-M)**

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Option mark:
R991: Populated for BCM5702C/BCM5705/BCM5705M
R992: Populated for BCM4401
R993: Populated for 3.3V PCI tolerance
R994: Populated for 5V PCI tolerance

BCM4401==>VESD(1,3) connect to VAUX power
BCM570x ==>VESD(1,3) connect to normal power

Note: For BCM5702, BCM5705 and BCM5705M, a serial FLASH can be used in stead of the serial EEPROM. Here are the configurations:

R1010	R1011	Descriptions
OFF	OFF	EEPROM Mode
OFF	ON	Illegal Configuration
ON	ON	Flash

Mode(AT45DB011B)

Note: CSTSCHG for 5705M only, NC for 4401,5702 and 5705

Note: If CLKRUN# not used please pull down

Note: Populate R1000 and depopulate R1002 when CLKRUN# is not required.

Note: Place PLLVDD filters as close to chip as possible.

PLACE CAPS AS CLOSE TO POWER PINS AS POSSIBLE

Note: Place BIASVDD filter close to pins.

PLACE CAPACITORS AS CLOSE TO POWER PINS AS POSSIBLE

For BCM570X Only

Note: Place Resistor close to pins.

1.24K 1% for BCM570x
1.27K 1% for BCM4401

Note:
This design default configured for FLASH (BCM5702/BCM5705/BCM5705M)

Note:
For the BCM4401, populate SPROM 93C46 and depopulate FLASH (U61) and EEPROM (U60) and their corresponding components.

Note: Place power plane.

fine tune this resistor for depopulate noise and ripple

Note: Place these component close to pins.

PLACE CAPACITORS AS CLOSE TO POWER PINS AS POSSIBLE

populate Q77,Q78 for BCM5705M (GIGA)

ASIC BCM4401 LAN FBGA 196PIN BROADCOM

EEPROM AT24C64AN-10SI-2.7 64K SOIC 8PIN ATMEL(NU)

EEPROM AT93C46-10SI-2.7 1Kbit(64*16) SOP 8PIN ATMEL

Company	FIC International Computer, Inc.
Author	7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC (886-2)2600-8818
Title	AT11 (DOTHAN + 915PM + ICH6-M)
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LAN Layout Guide

1.Each signal trace between the PHY and the RJ45 should have a controlled impedance of 50 ohms.

2.The distance between each pair coming from the same BCM5705M device should be 50 mils minimum.

3.Differential pairs from different BCM5705M devices should have 200 mils spacing between them.

4. Route differential pairs such that the + and - signals are matched in length.(as short as possible)

5.Place the series termination resistors close to the source.

6.If any two traces must cross each other on different layers,always cross them at or near 90 degree to minimize potential crosstalk.

7.To place the power transistors a minimum distance of 1.5 inches away from the BCM5705M device.

8.The BCM5705M clock source needs to be placed as close as possible to the BCM5705M device.

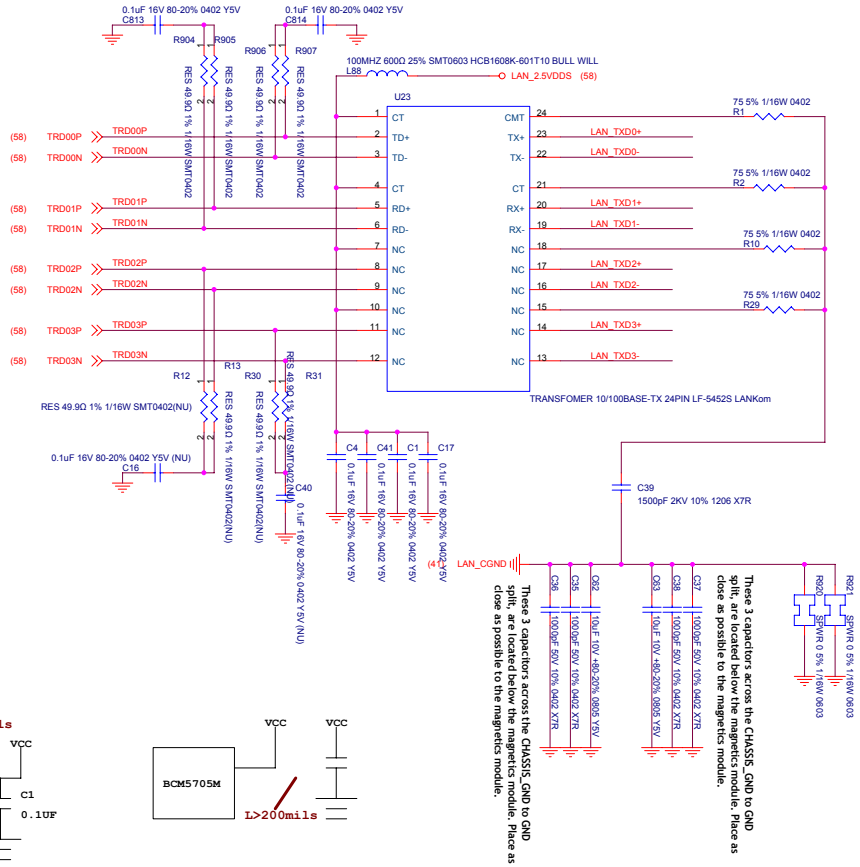
9.Locate the resistor as close to the RDAC pin as possible,and keep the trace between them as short as possible.

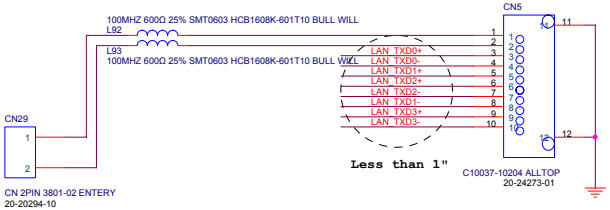
Avoid routing any high -speed signal traces in this area.

If vias cannot be placed next to the pins,then use 20 mils traces.

11.If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.

12.Place the filtering circuit as close to the pin as possible.





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Title: AT11 (DOTHAN + 915PM + ICH6-M)

Size: C | Document Number: 10/100 LAN TRANSFER | Rev: 0.1

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