First International Computer,Inc

Portable Computer Group HW Department

Board name : Mother Board Schematic

Project : LM10W

Version : 0.7

Initial Date : Feb 21 , 2006

1. Schematic Page Description :
2. PCI & IRQ & DMA Description :
3. Block Diagram :
4. Nat name Description :
5. Board Stack up Description :
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7. power on & off & S3 Sequence :
8. Layout Guideline :
9. switch setting

Manager Sign by:

Drawing by :

Total confirm by: Jack Chen

LAN Circuit check by:

Audio Circuit check by:

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Title: LM10W < VIA VN896 + VT8237A >

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1. Schematic Page Description :

LM10W Schematic Ver : 0.7

1. Title
2. Schematic Page Description
3. Block Diagram
4. ANNOTATIONS
5. Schematic Modify
6. Timing Diagram
7. DDR Layout Guideline
8. Yonah processor (1/2)
9. Yonah processor (2/2)
10. POWER (CPU CORE)
11. Thermal / VR_PWRGD
12. Clock Generator
13. Clock Buffer
14. VN896 (1/4)
15. VN896 (2/4)
16. VN896 (3/4)
17. VN896 (4/4)
18. DDR SO-DIMM1
19. DDR SO-DIMM0
20. VT1634AL LVDS Transmitter
21. LCD Connector
22. CRT Connector
23. VT8237A (1/3)
24. VT8237A (2/3)
25. VT8237A (3/3)
26. Power Good & Fan Controller
27. EXPRESS CARD
28. RTC
29. MINI PCI
30. VT6103L PHY
31. USB CNN
32. S-ATA HD / CD-ROM CNN
33. LPC PMU08
34. LPC KBC M38827
35. INT KBC / GP Connector
36. MDC Connector
37. DIP Switch & LED
38. Firm Ware Hub / LID Switch
39. Reset Circuit
40. OVP / SCREW
41. CX20549 Audio Codec
42. G1432+1410 Audio Amplifier
43. H.P. Out / Audio CNN
44. DDR PWR
45. 1.5VDDA/S , 1.8/2.5VDDM/A
46. 3VDDM / 5VDDM
47. VCCP/1.5VDDM
48. 3VDDA / 5VDDA / PMU3/5V
49. POW-ON Controller
50. ADIN / Battery CNN
51. Charge Circuit / DCIN
52. Inverter Controller
53. Audio board
54. Switch transfer board
55. MDC circuit

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)

PCIINT	CHIP		
IRQA	NB		
IRQB	MiniPCI		
IRQC	MiniPCI		
IRQD		IRQH	PCI-E

BUSMASTER

REQ	CHIP
REQ0 / GNT0	
REQ1 / GNT1	
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Desciption	
IRQ0	System timer	
IRQ1	Keyboard	
IRQ2	(Casacde)	
IRQ3	LAN / MODEM	
IRQ4	~~Serial Port~~	
IRQ5	AUDIO / VGA / USB	
IRQ6	~~FLOPPY DISK~~	
IRQ7	~~LPT~~	
IRQ8	RTC	
IRQ9	ACPI	
IRQ10	FIR (Disable by default)	(MODEM/LAN)
IRQ11	Cardbus	
IRQ12	PS/2 mouse	
IRQ13	FPU	
IRQ14	HDD	
IRQ15	CDROM	

DMA Channel	Device	
DMA0	FIR (disable by default)	(MODEM / LAN)
DMA1	~~ECP~~	
DMA2	~~FLOPPY DISK~~	
DMA3	AUDIO	
DMA4	(Cascade)	
DMA5	Unused	
DMA6	Unused	
DMA7	Unused	

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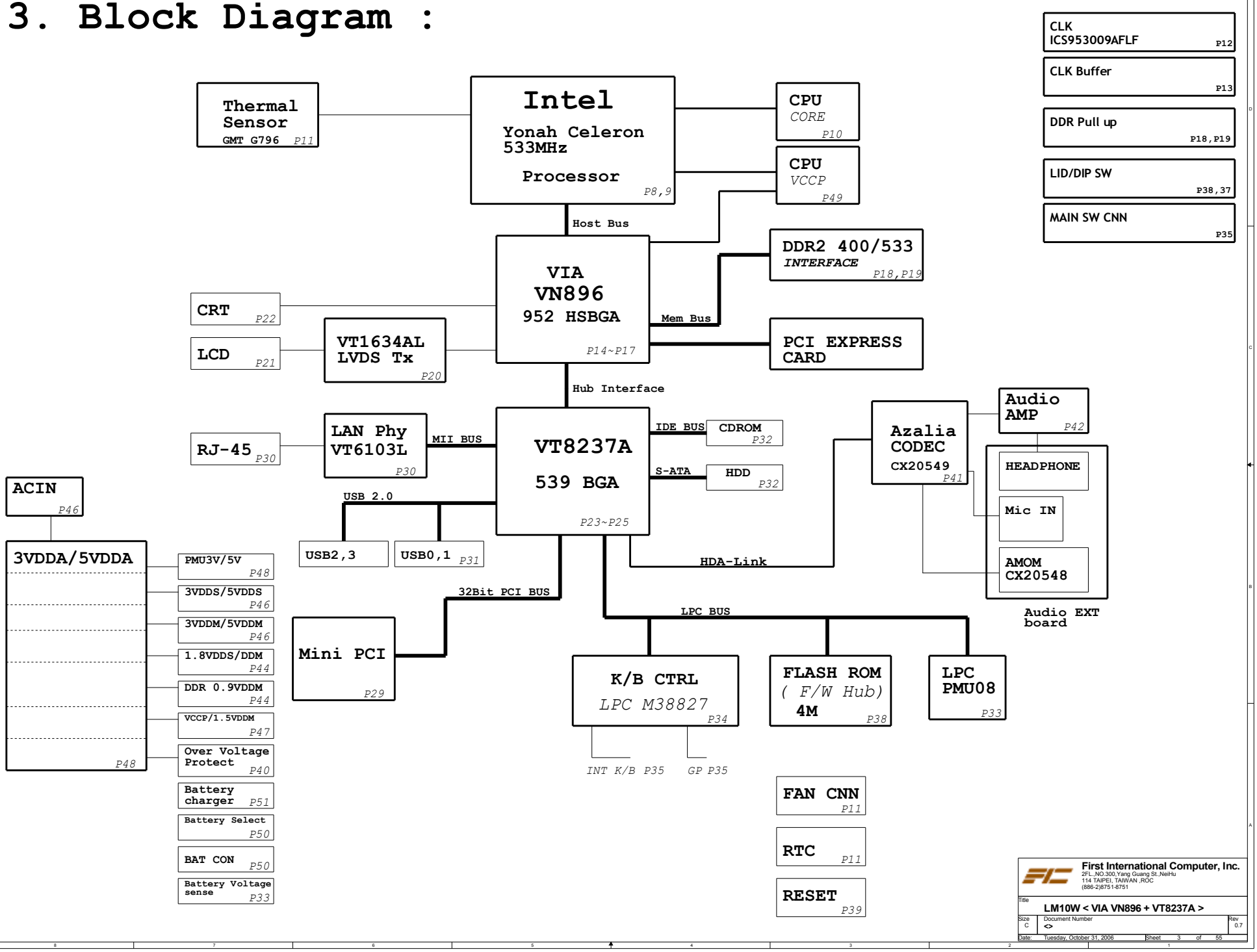
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR_0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(AGTL,CLOCK,DDR)
Layer 4		Stripline Layer(Analog,LVDS,other)
Layer 5		Power Plane
Layer 6		Solder Side,Microstrip signal Layer

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6.Schematic modify Item and History :

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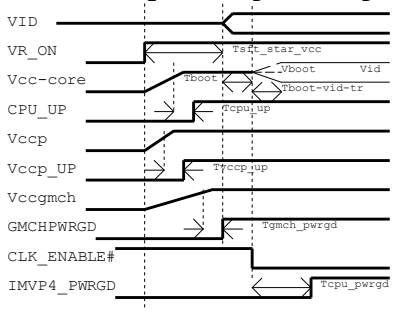
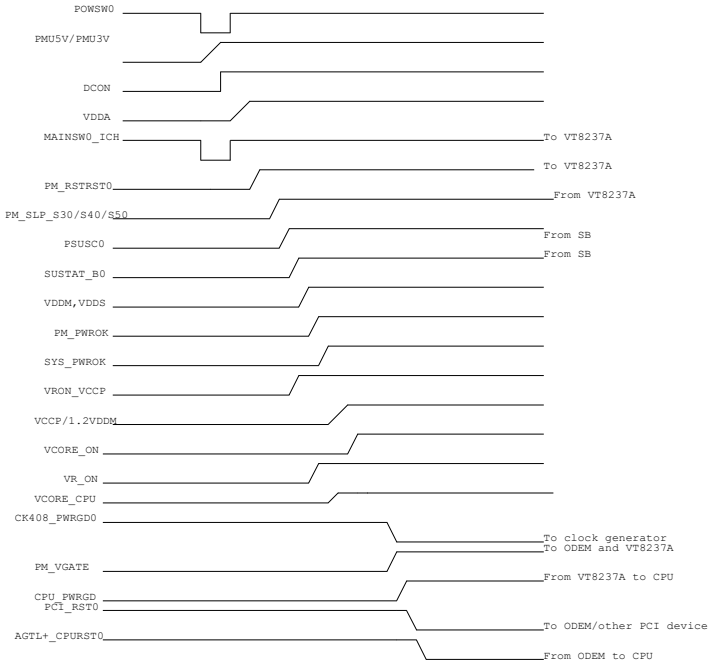
7. power on & off & S3 Sequence :

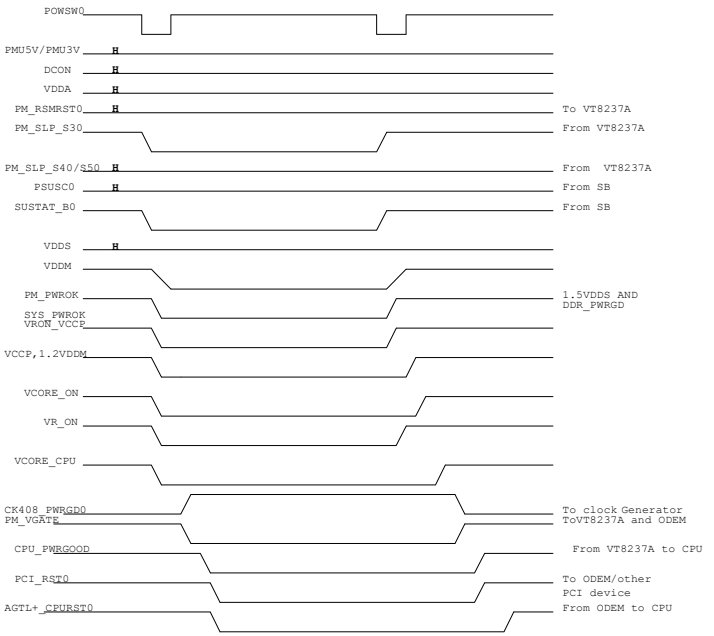
Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



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8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

DDR Signal Groups

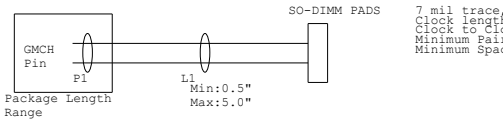
Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS#[3:0]
Command	SMA[12:6,3:0] SBA[1:0] SRAS# SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

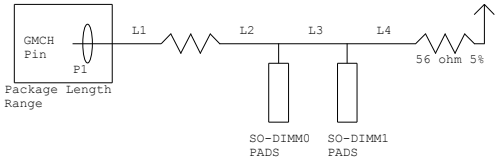
CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between + & -)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH	4.5" ~ 9.0 "	5 / 20 mils	* 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
AGPCLK_ATI	MAX : 8.5"		
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2.Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5"~9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" ~ 12.5"	5 / 20 mils	

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerehve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

Data Signals Topologies and Routing Guidelines

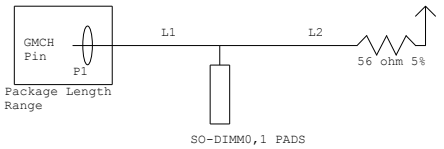


Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5", Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0 "
Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 0.5"
SDQ/SDM to SDQS : +/-'25 mils

SDQ/SDM to SDQS Mapping

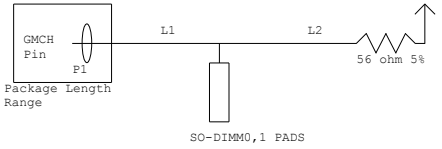
Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

Control Signals Topologies and Routing Guidelines



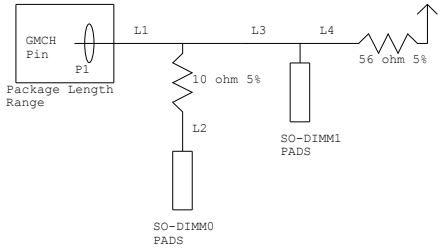
Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

CPC Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

Command Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.0"
L3 : Max 2.0"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"

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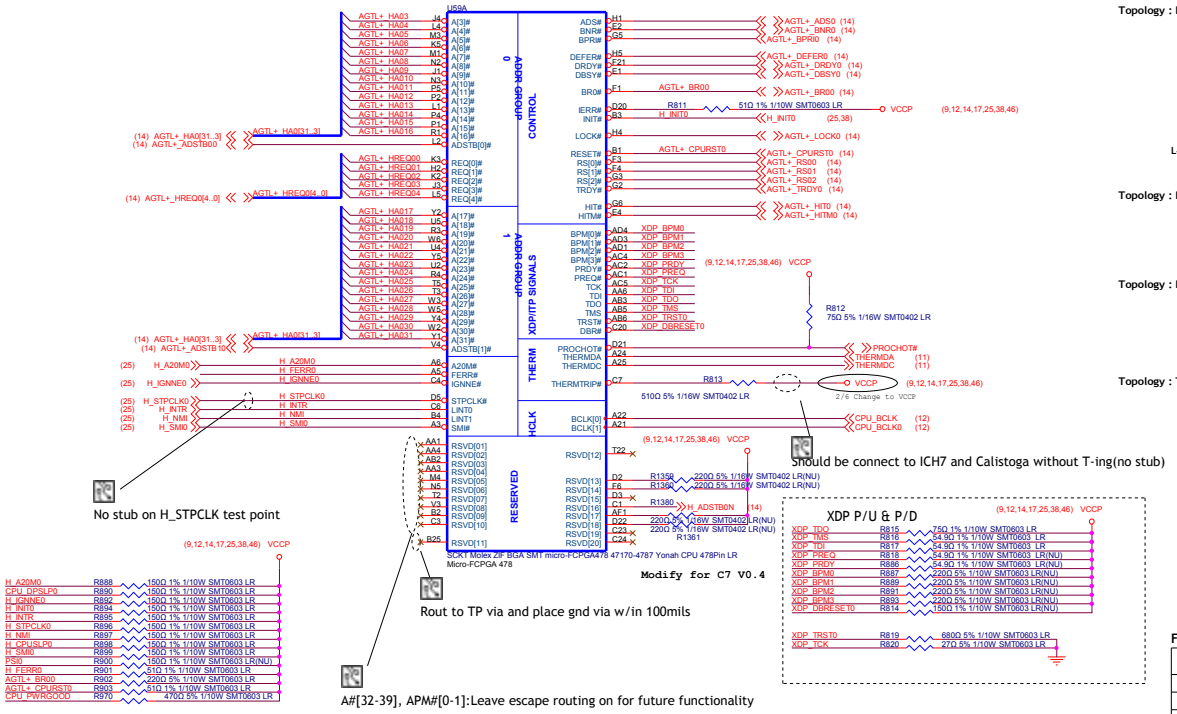
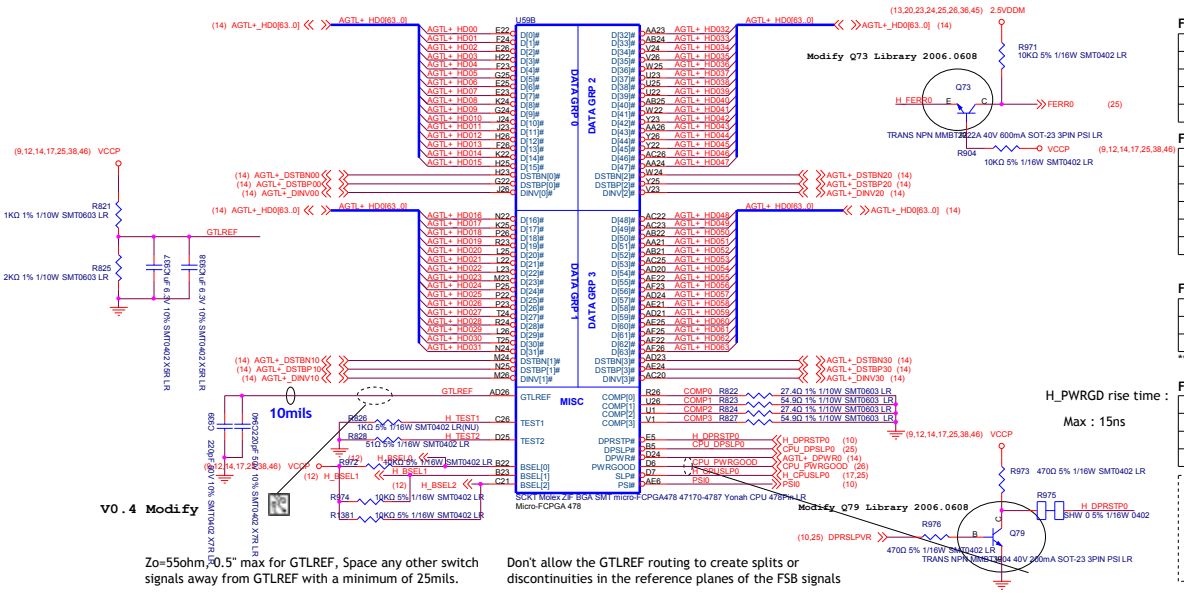
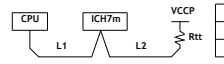




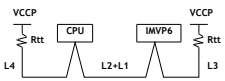
Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.

Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

Topology : FERR#

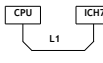


L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line



L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Strip-line

Topology : PWRGOOD

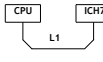


L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# SMI# , STPCLK#

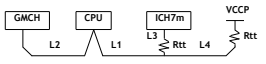


L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#

L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#



L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

FSB Common Clock Signal Layout Guide :

ADS# , BNR# , BPR# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Address#[31..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

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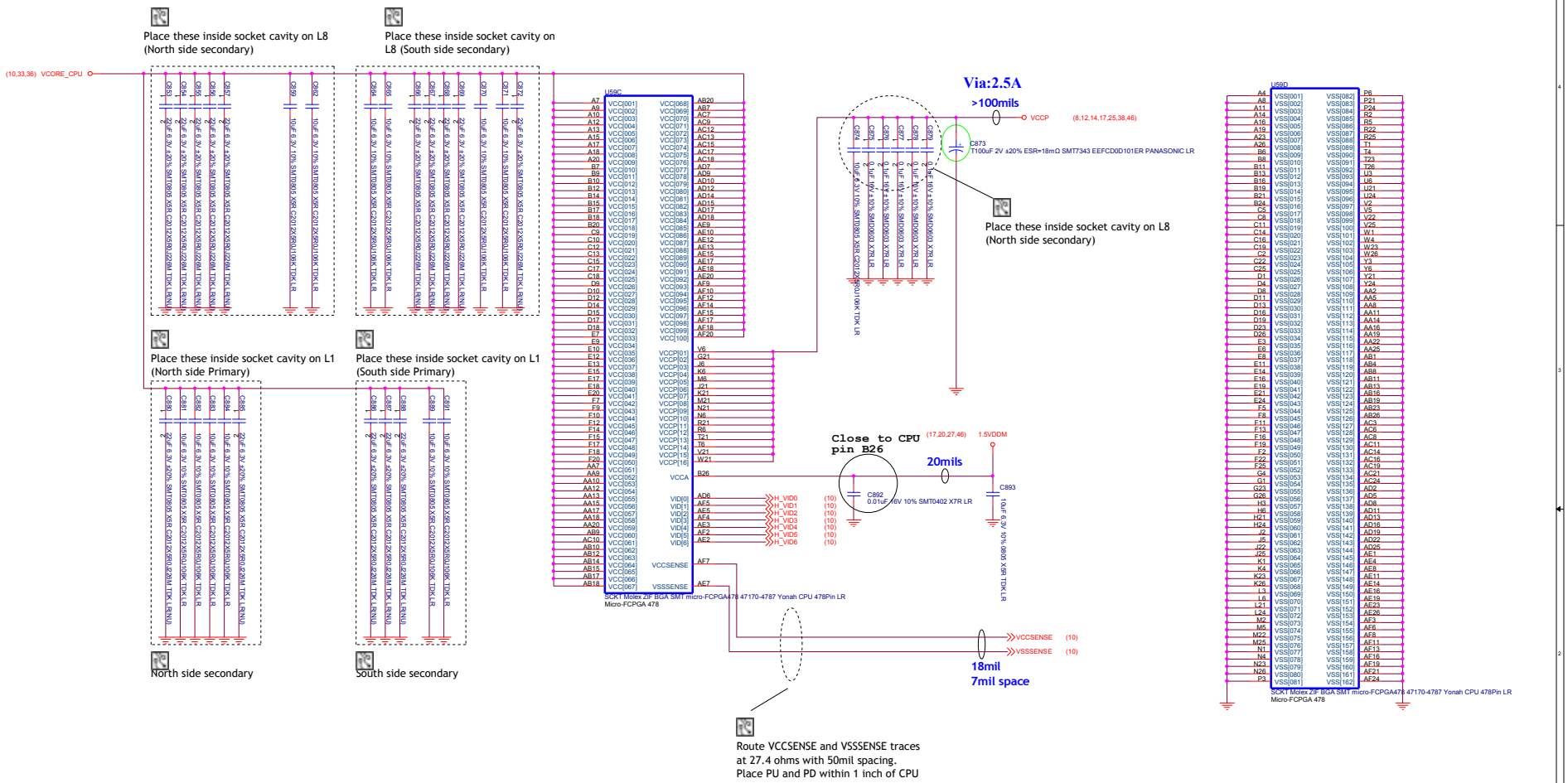

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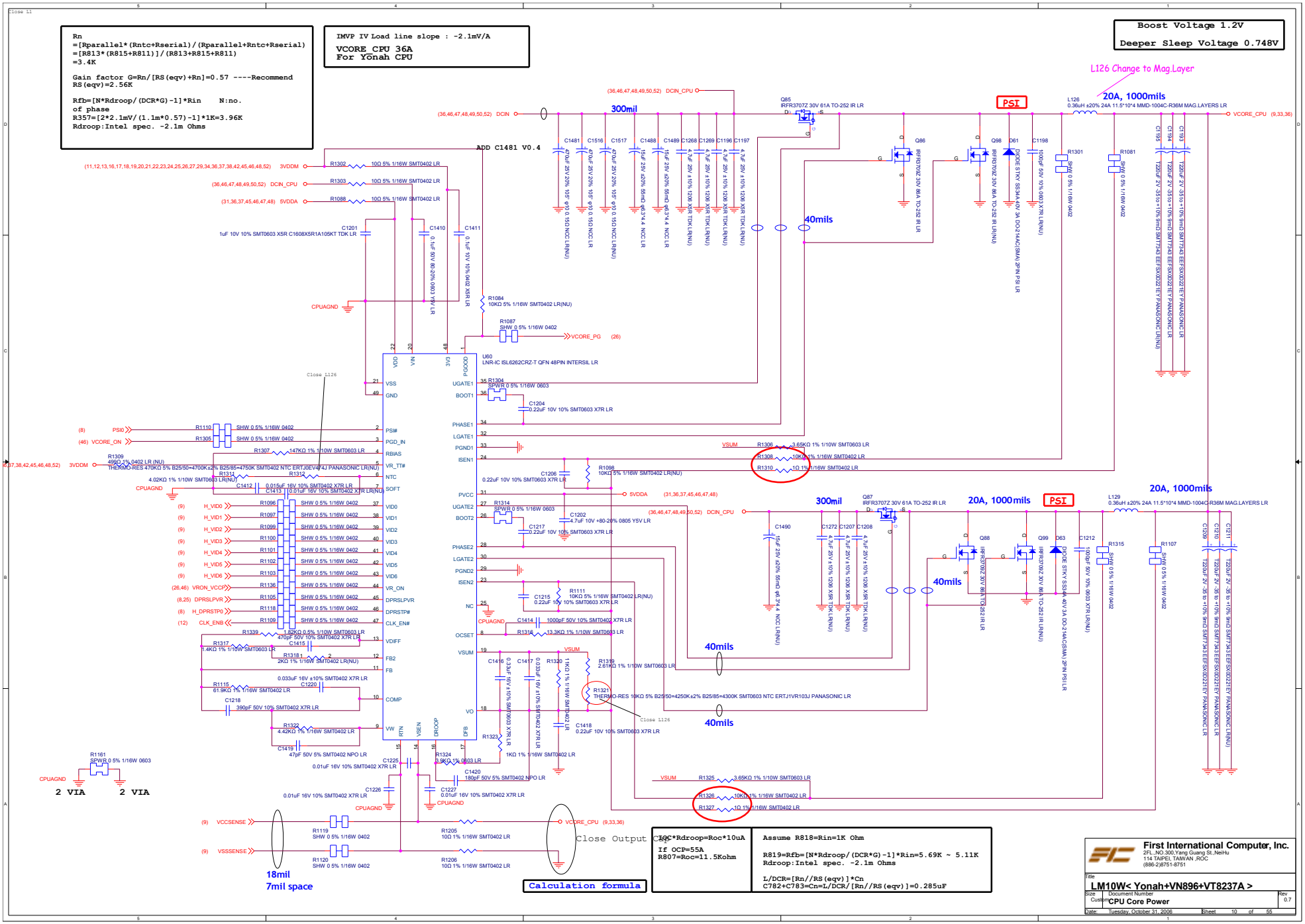
Rn
=[Rparallel*(Rntc+Rserial)/(Rparallel+Rntc+Rserial)
=[R813*(R815+R811)]/(R813+R815+R811)
=3.4K
Gain factor G=Rn/[RS(eqv)+Rn]=0.57 ----Recommend
RS(eqv)=2.56K
Rfb=[N*Rdroop/(DCR*G)-1]*Rin N:no. of phase
R357=[2*2.1mV/(1.1m*0.57)-1]*1K=3.96K
Rdroop:Intel spec. -2.1m Ohms
IMVP IV Load line slope : -2.1mV/A
VCORE_CPU 36A
For Yonah CPU
Boost Voltage 1.2V
Deeper Sleep Voltage 0.748V
L126 Change to Mag.Layer
ADD C1481 V0.4
300mil
40mils
20A, 1000mils
PSI
U60
LNR-IC ISL6262CRZ-T QFN 48PIN INTERSIL LR
2 VIA
2 VIA
18mil
7mil space
Close Output Cap
Calculation formula
Assume R818=Rin=1K Ohm
R819=Rfb=[N*Rdroop/(DCR*G)-1]*Rin=5.69K ~ 5.11K
Rdroop:Intel spec. -2.1m Ohms
L/DCR=[Rn//RS(eqv)]*Cn
C782+C783=Cn=L/DCR/[Rn//RS(eqv)]=0.285uF
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LM10W< Yonah+VN896+VT8237A >
CPU Core Power
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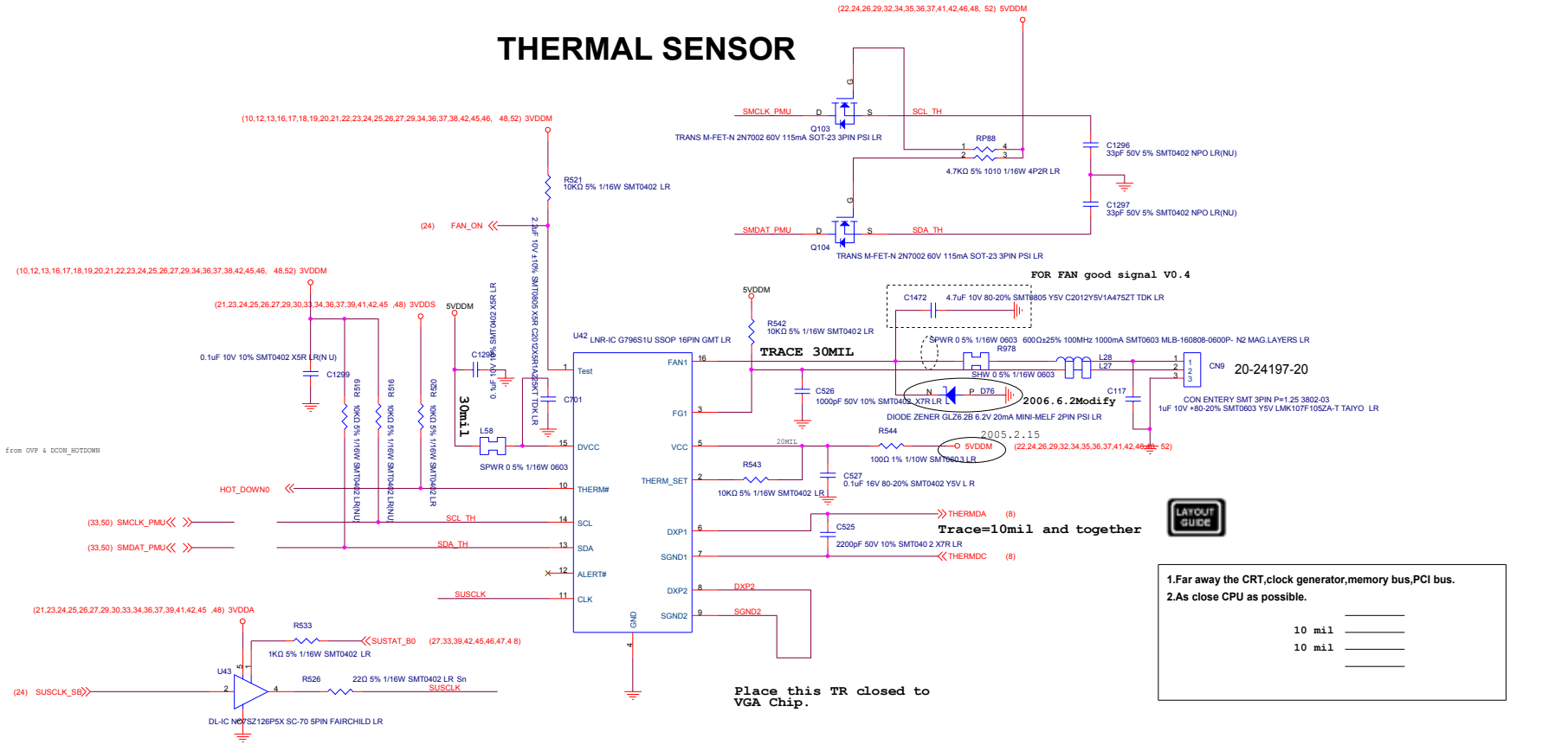
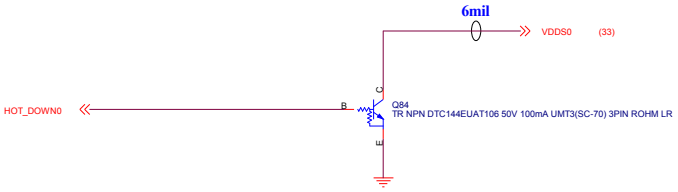
THERMAL SENSOR





(22,24,26,29,32,34,35,36,37,41,42,46,48, 52) 5VDDM
5VDDM
(21,23,24,25,26,27,29,30,33,34,36,37,39,41,42,45, 48) 3VDDS
3VDDS

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Title: LM10W < VIA VN896 + VT8237A >

Size: C | Document Number: <Thermal / RTC> | Rev: 0.7

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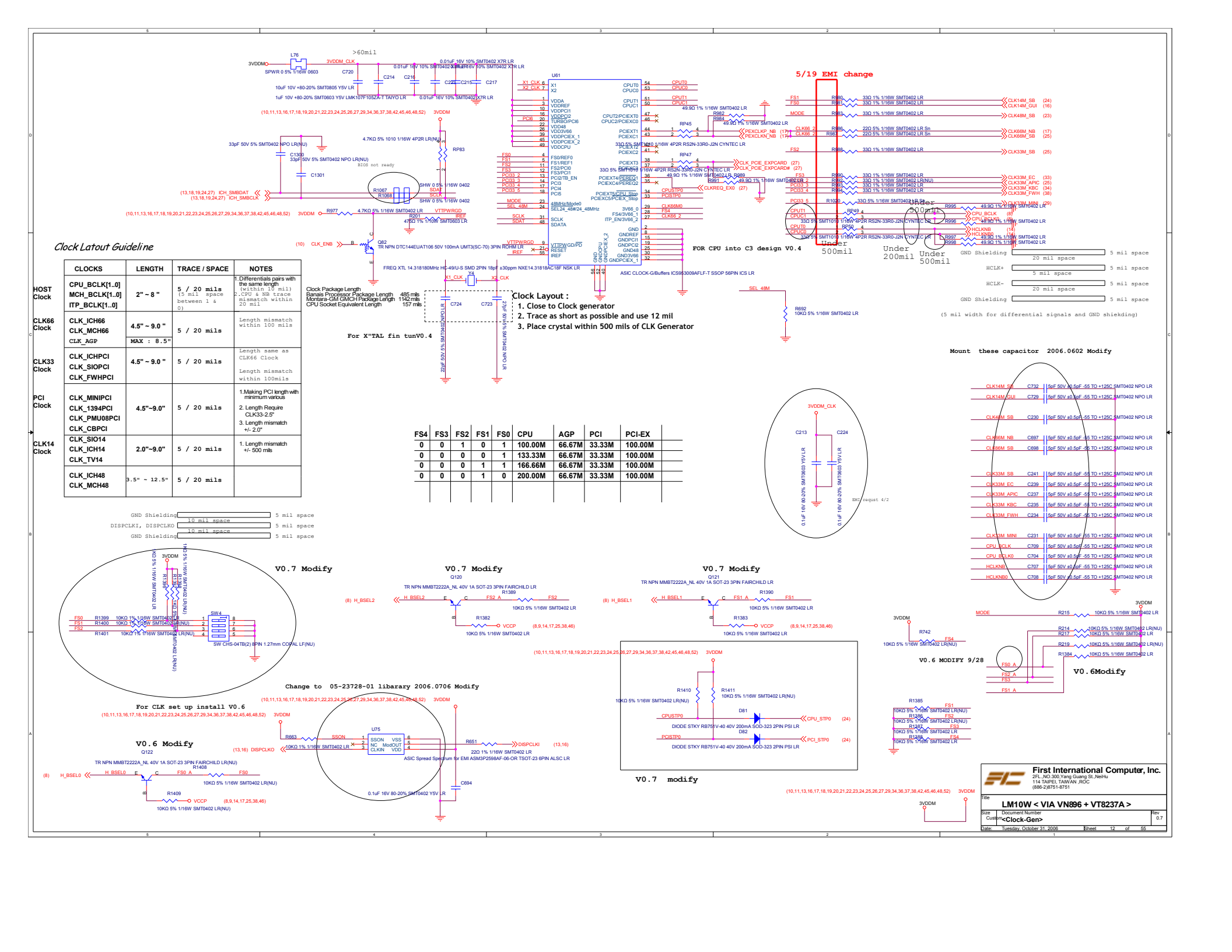
5/19 EMI change
FOR CPU into C3 design V0.4
For X"TAL fin tunV0.4
Clock Layout :
1. Close to Clock generator
2. Trace as short as possible and use 12 mil
3. Place crystal within 500 mils of CLK Generator
Clock Package Length
Banais Processor Package Length 495 mils
Montara-GM GMCH Package Length 1142 mils
CPU Socket Equivalent Length 157 mils
Clock Latout Guideline
HOST Clock
CLK66 Clock
CLK33 Clock
PCI Clock
CLK14 Clock
CLOCKS
LENGTH
TRACE / SPACE
NOTES
CPU_BCLK[1..0]
MCH_BCLK[1..0]
ITP_BCLK[1..0]
2" ~ 8 "
5 / 20 mils
1.Differentials pairs with the same length (within 10 mil)
2.CPU & NB trace mismatch within 20 mil
CLK_ICH66
CLK_MCH66
CLK_AGP
4.5" ~ 9.0 "
MAX : 8.5"
5 / 20 mils
Length mismatch within 100 mils
CLK_ICHPCI
CLK_SIOPCI
CLK_FWHPCI
4.5" ~ 9.0 "
5 / 20 mils
Length same as CLK66 Clock
Length mismatch within 100mils
CLK_MINIPCI
CLK_1394PCI
CLK_PMU08PCI
CLK_CBPCI
4.5"~9.0"
5 / 20 mils
1.Making PCI length with minimum various
2. Length Require CLK33-2.5"
3. Length mismatch +/- 2.0"
CLK_SIO14
CLK_ICH14
CLK_TV14
2.0"~9.0"
5 / 20 mils
1. Length mismatch +/- 500 mils
CLK_ICH48
CLK_MCH48
3.5" ~ 12.5"
5 / 20 mils
FS4 FS3 FS2 FS1 FS0 CPU AGP PCI PCI-EX
0 0 1 0 1 100.00M 66.67M 33.33M 100.00M
0 0 0 0 1 133.33M 66.67M 33.33M 100.00M
0 0 0 1 1 166.66M 66.67M 33.33M 100.00M
0 0 0 1 0 200.00M 66.67M 33.33M 100.00M
Mount these capacitor 2006.0602 Modify
V0.7 Modify
V0.7 Modify
V0.7 Modify
V0.6 MODIFY 9/28
V0.6Modify
V0.6 Modify
V0.7 modify
Change to 05-23728-01 libarary 2006.0706 Modify
For CLK set up install V0.6
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LM10W < VIA VN896 + VT8237A >
Clock-Gen
Tuesday, October 31, 2006
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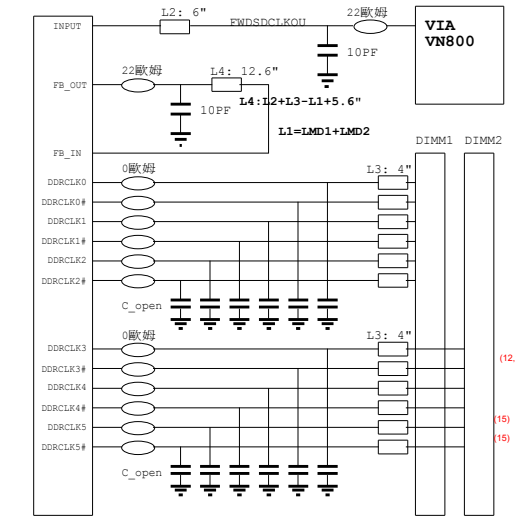
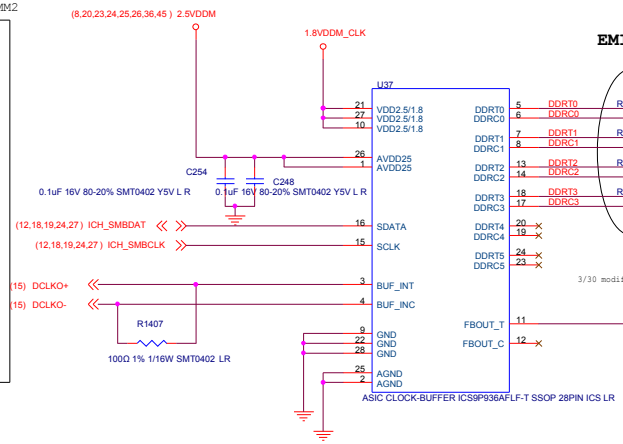
DDR CLOCK BUFFER

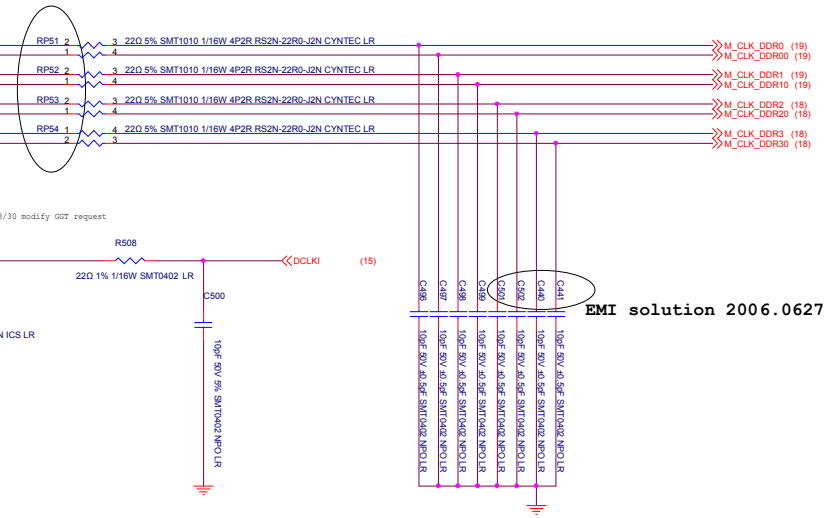


DDR Clock Buffer



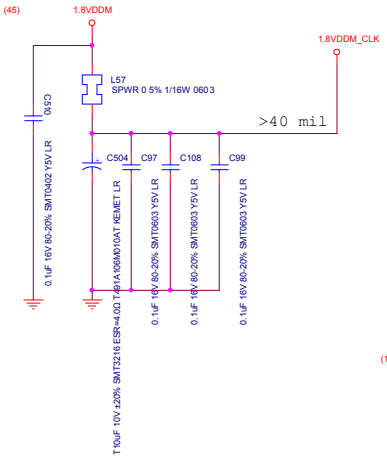
V0.7 modify del L145,L146

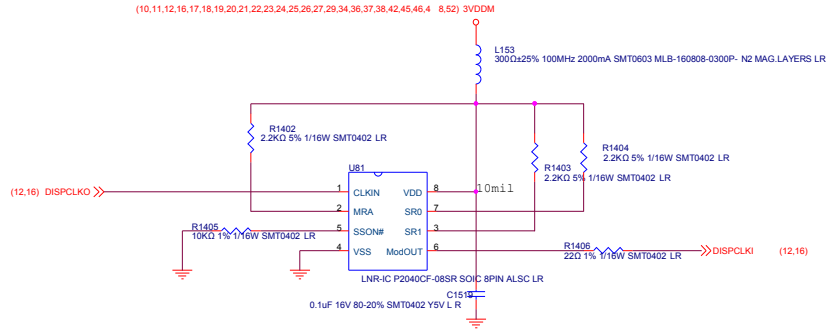
EMI solution 2006.0627



EMI solution 2006.0627

Mount these capacitor 2006.0602 Modify





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Title: LM10W < VIA VN896 + VT8237A >

Size: C | Document Number: <clock buffer> | Rev: 0.7

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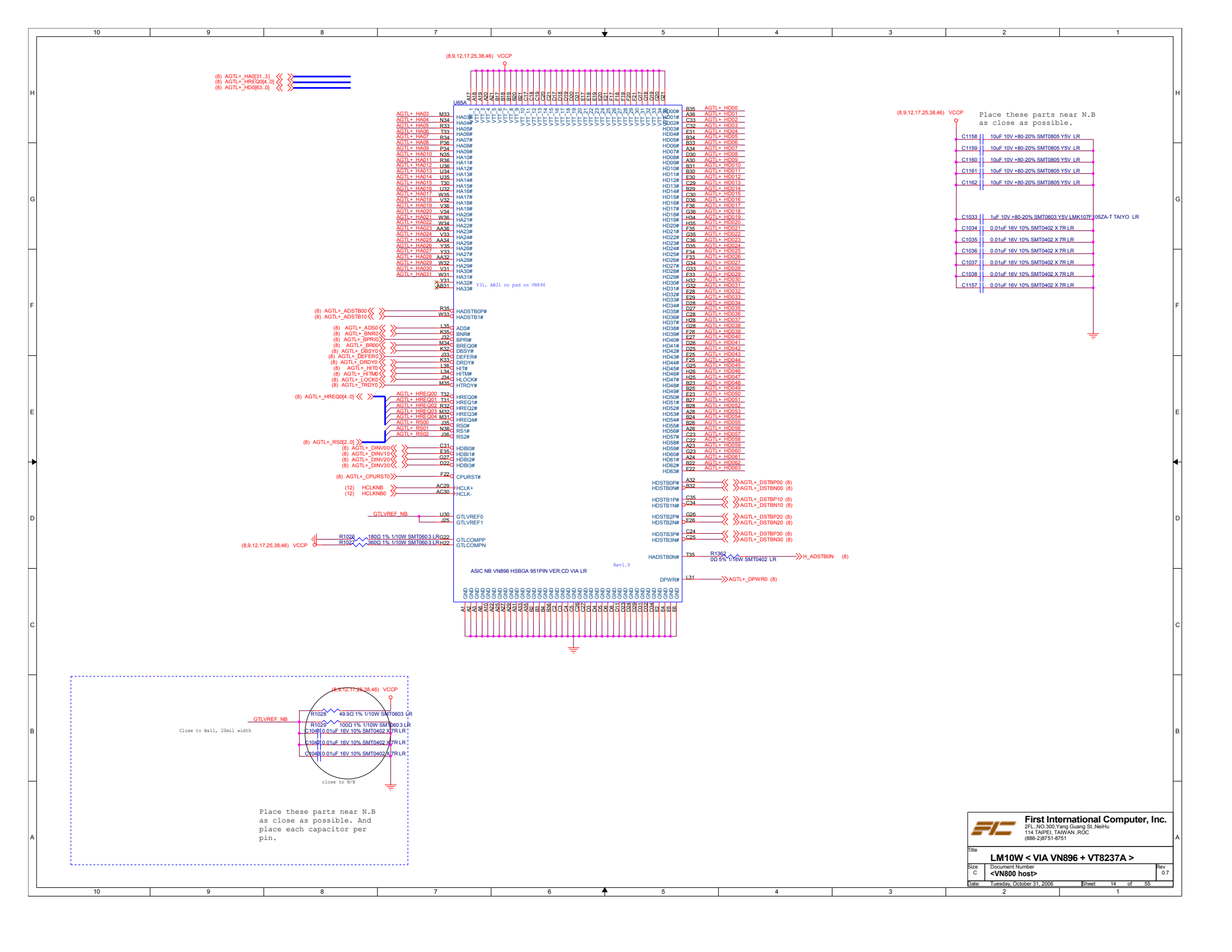
(8,9,12,17,25,38,46) VCCP
(8) AGTL+_HA0[31..3]
(8) AGTL+_HREQ0[4..0]
(8) AGTL+_HD0[63..0]
U65A
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
Rev1.9
Y31, AB31 no pad on VN896
Place these parts near N.B as close as possible.
C1158 10uF 10V +80-20% SMT0805 Y5V LR
C1159 10uF 10V +80-20% SMT0805 Y5V LR
C1160 10uF 10V +80-20% SMT0805 Y5V LR
C1161 10uF 10V +80-20% SMT0805 Y5V LR
C1162 10uF 10V +80-20% SMT0805 Y5V LR
C1033 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1034 0.01uF 16V 10% SMT0402 X 7R LR
C1035 0.01uF 16V 10% SMT0402 X 7R LR
C1036 0.01uF 16V 10% SMT0402 X 7R LR
C1037 0.01uF 16V 10% SMT0402 X 7R LR
C1038 0.01uF 16V 10% SMT0402 X 7R LR
C1157 0.01uF 16V 10% SMT0402 X 7R LR
R1026 180Ω 1% 1/10W SMT0603 LR
R1027 360Ω 1% 1/10W SMT0603 LR
R1362 0Ω 5% 1/16W SMT0402 LR
GTLVREF_NB
R1028 49.9Ω 1% 1/10W SMT0603 LR
R1029 100Ω 1% 1/10W SMT0603 LR
C1040 0.01uF 16V 10% SMT0402 X 7R LR
C1041 0.01uF 16V 10% SMT0402 X 7R LR
C1042 0.01uF 16V 10% SMT0402 X 7R LR
Close to Ball, 20mil width
close to N/B
Place these parts near N.B as close as possible. And place each capacitor per pin.
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LM10W < VIA VN896 + VT8237A >
Size C
Document Number <VN800 host>
Rev 0.7
Date: Tuesday, October 31, 2006
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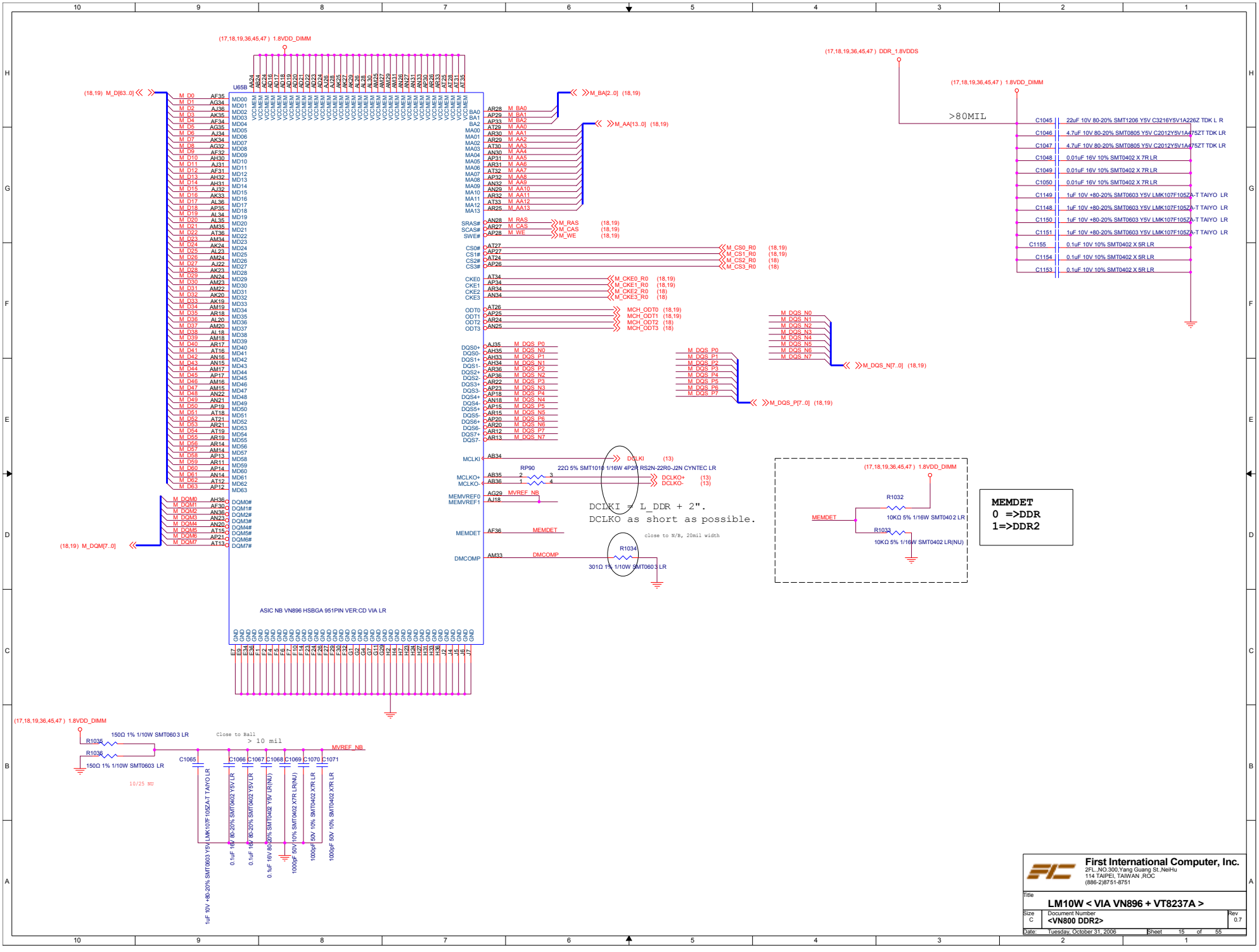

MEMDET
0 =>DDR
1=>DDR2

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Title: **LM10W < VIA VN896 + VT8237A >**

Size	Document Number	Rev
C	<VN800 DDR2>	0.7

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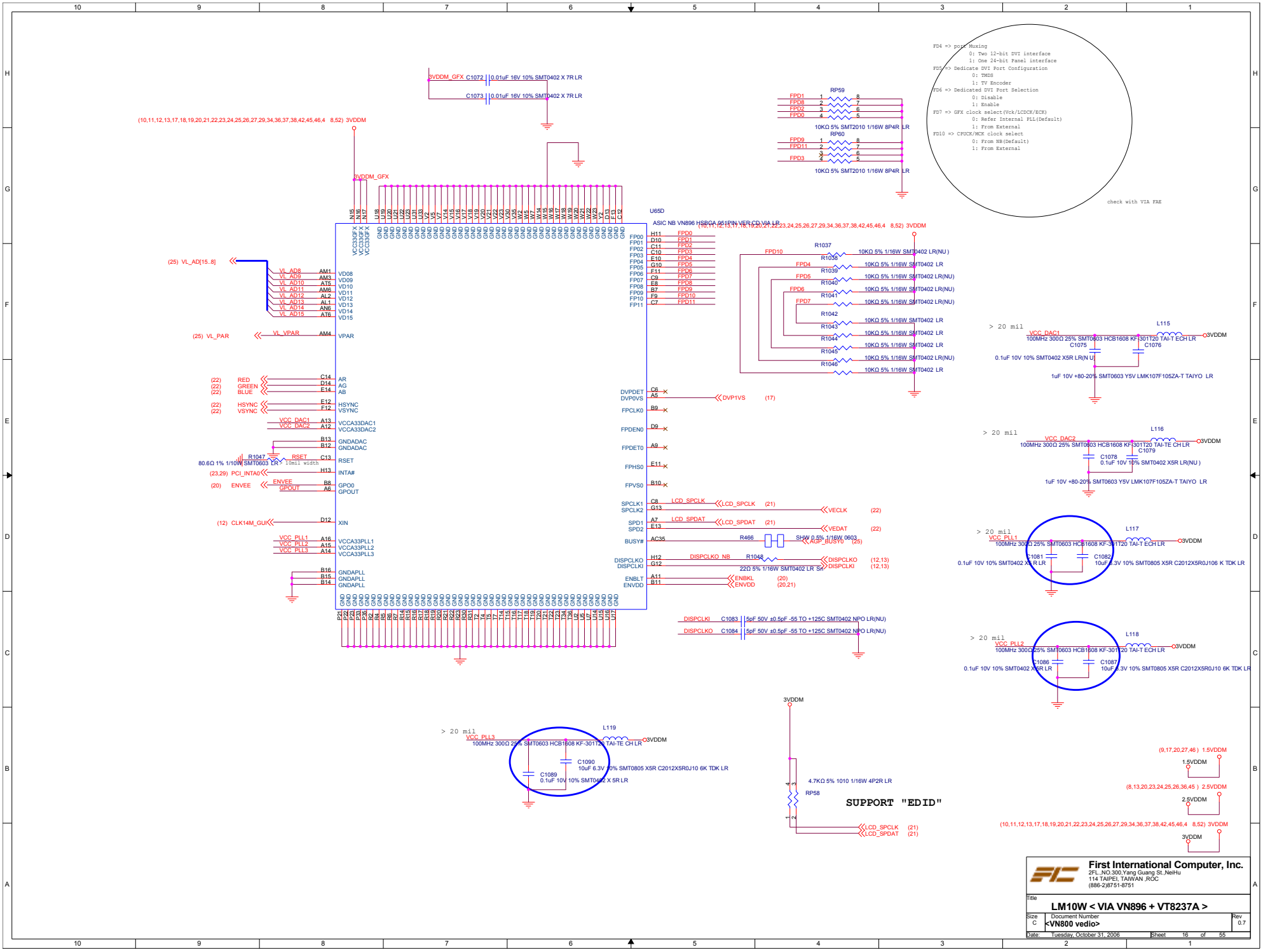
3VDDM_GFX C1072 0.01uF 16V 10% SMT0402 X 7R LR
C1073 0.01uF 16V 10% SMT0402 X 7R LR
(10,11,12,13,17,18,19,20,21,22,23,24,25,26,27,29,34,36,37,38,42,45,46,4 8,52) 3VDDM
3VDDM_GFX
U65D
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
RP59
FPD1 FPD8 FPD2 FPD0
10KΩ 5% SMT2010 1/16W 8P4R LR
RP60
FPD9 FPD11 FPD3
10KΩ 5% SMT2010 1/16W 8P4R LR
FD4 => port Muxing
0: Two 12-bit DVI interface
1: One 24-bit Panel interface
FD5 => Dedicate DVI Port Configuration
0: TMDS
1: TV Encoder
FD6 => Dedicated DVI Port Selection
0: Disable
1: Enable
FD7 => GFX clock select(Vck/LCDCK/ECK)
0: Refer Internal PLL(Default)
1: From External
FD10 => CPUCK/MCK clock select
0: From NB(Default)
1: From External
check with VIA FAE
(25) VL_AD[15..8]
VL_AD8 VL_AD9 VL_AD10 VL_AD11 VL_AD12 VL_AD13 VL_AD14 VL_AD15
(25) VL_PAR
VL_VPAR
(22) RED (22) GREEN (22) BLUE
(22) HSYNC (22) VSYNC
VCC_DAC1 VCC_DAC2
R1047 80.6Ω 1% 1/10W SMT0603 LR
RSET
10mil width
(23,29) PCI_INTA0
(20) ENVEE
ENVEE GPOUT
(12) CLK14M_GUI
VCC_PLL1 VCC_PLL2 VCC_PLL3
FPD10 FPD4 FPD5 FPD6 FPD7
R1037 R1038 R1039 R1040 R1041 R1042 R1043 R1044 R1045 R1046
10KΩ 5% 1/16W SMT0402 LR(NU)
10KΩ 5% 1/16W SMT0402 LR
10KΩ 5% 1/16W SMT0402 LR(NU)
DVP1VS (17)
LCD_SPCLK (21)
VECLK (22)
LCD_SPDAT (21)
VEDAT (22)
R466 SHW 0.5% 1/16W 0603
AGP_BUSY0 (25)
DISPCLKO_NB R1048
22Ω 5% 1/16W SMT0402 LR Sn
DISPCLKO (12,13)
DISPCLKI (12,13)
ENBKL (20)
ENVDD (20,21)
DISPCLKI C1083 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
DISPCLKO C1084 5pF 50V ±0.5pF -55 TO +125C SMT0402 NPO LR(NU)
> 20 mil
L115
VCC_DAC1
100MHz 300Ω 25% SMT0603 HCB1608 KF-301T20 TAI-T ECH LR
3VDDM
C1075 0.1uF 10V 10% SMT0402 X5R LR(N U
C1076 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
L116
VCC_DAC2
C1078 0.1uF 10V 10% SMT0402 X5R LR(NU)
C1079 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
L117
VCC_PLL1
C1081 0.1uF 10V 10% SMT0402 X5R LR
C1082 10uF 6.3V 10% SMT0805 X5R C2012X5R0J106 K TDK LR
L118
VCC_PLL2
C1086 0.1uF 10V 10% SMT0402 X5R LR
C1087 10uF 6.3V 10% SMT0805 X5R C2012X5R0J10 6K TDK LR
L119
VCC_PLL3
C1089 0.1uF 10V 10% SMT0402 X 5R LR
C1090 10uF 6.3V 10% SMT0805 X5R C2012X5R0J10 6K TDK LR
4.7KΩ 5% 1010 1/16W 4P2R LR
RP58
SUPPORT "EDID"
(9,17,20,27,46) 1.5VDDM
(8,13,20,23,24,25,26,36,45) 2.5VDDM
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Title
LM10W < VIA VN896 + VT8237A >
Size C
Document Number
<VN800 vedio>
Rev 0.7
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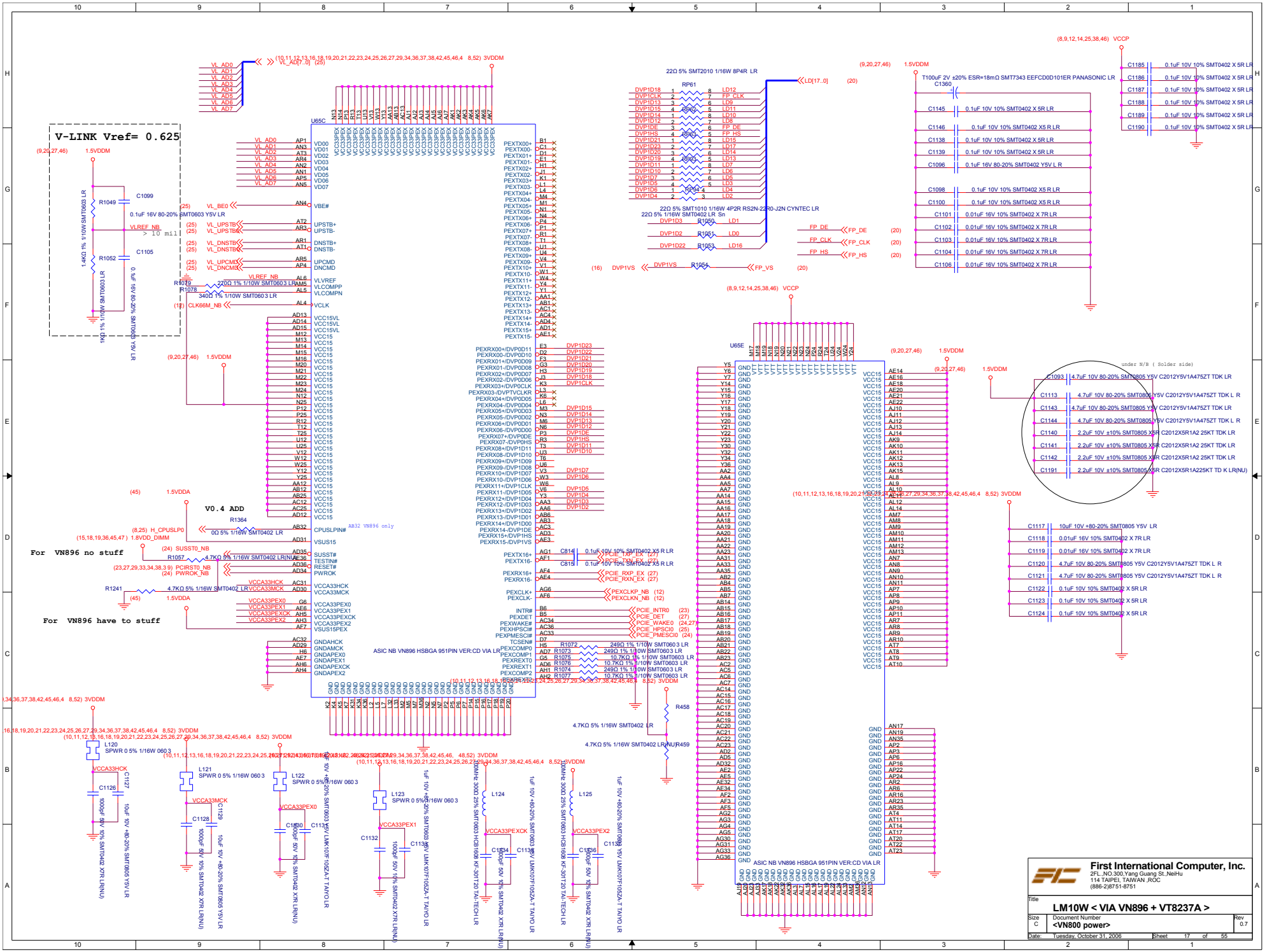
V-LINK Vref= 0.625
V0.4 ADD
For VN896 no stuff
For VN896 have to stuff
ASIC NB VN896 HSBGA 951PIN VER:CD VIA LR
First International Computer, Inc.
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LM10W < VIA VN896 + VT8237A >
<VN800 power>
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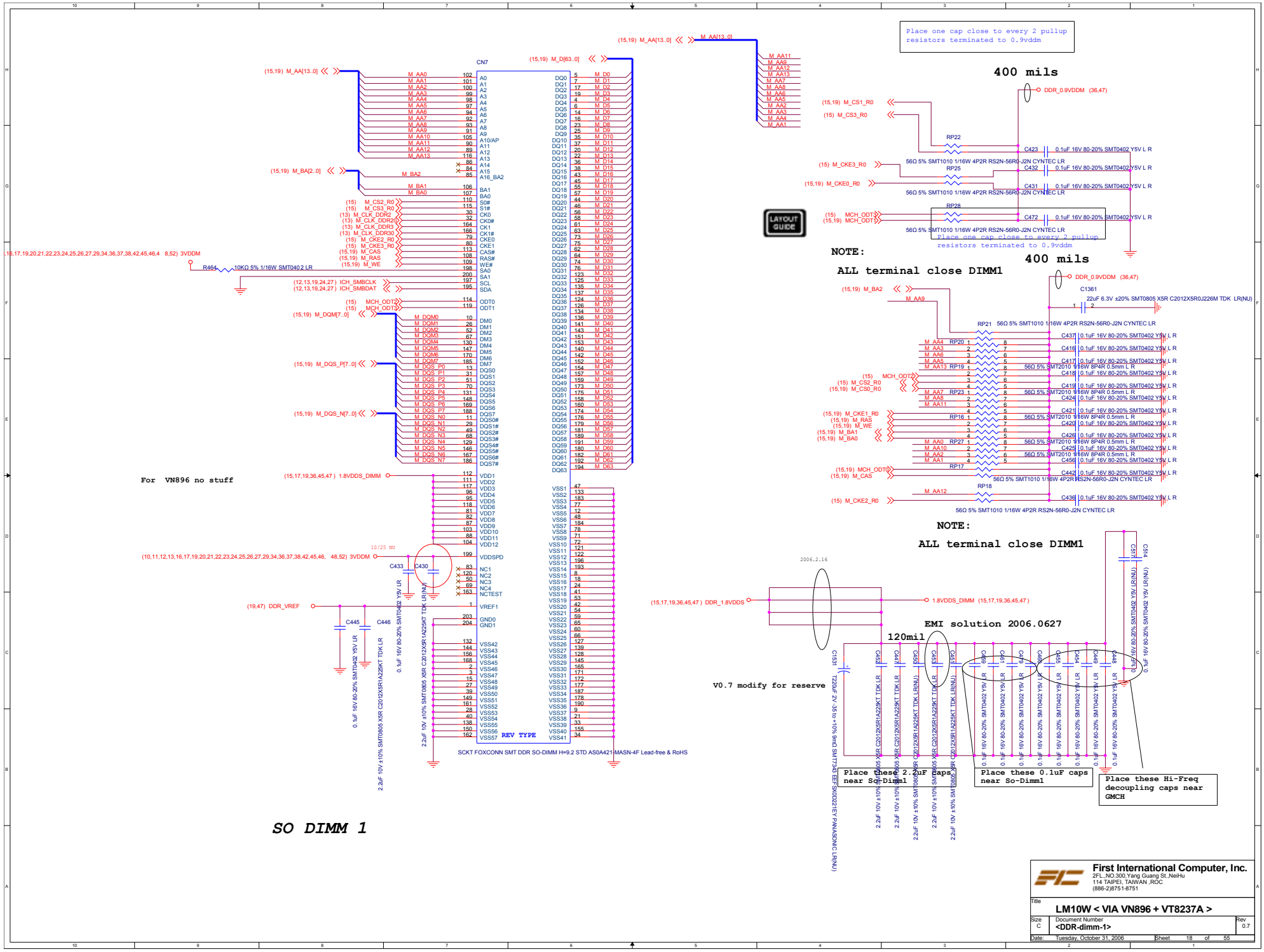
CN7
SO DIMM 1
For VN896 no stuff
Place one cap close to every 2 pullup resistors terminated to 0.9vddm
400 mils
NOTE:
ALL terminal close DIMM1
EMI solution 2006.0627
120mil
V0.7 modify for reserve
Place these 2.2uF caps near So-Dimm1
Place these 0.1uF caps near So-Dimm1
Place these Hi-Freq decoupling caps near GMCH
SCKT FOXCONN SMT DDR SO-DIMM H=9.2 STD AS0A421-MASN-4F Lead-free & RoHS
REV TYPE
First International Computer, Inc.
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LM10W < VIA VN896 + VT8237A >
<DDR-dimm-1>
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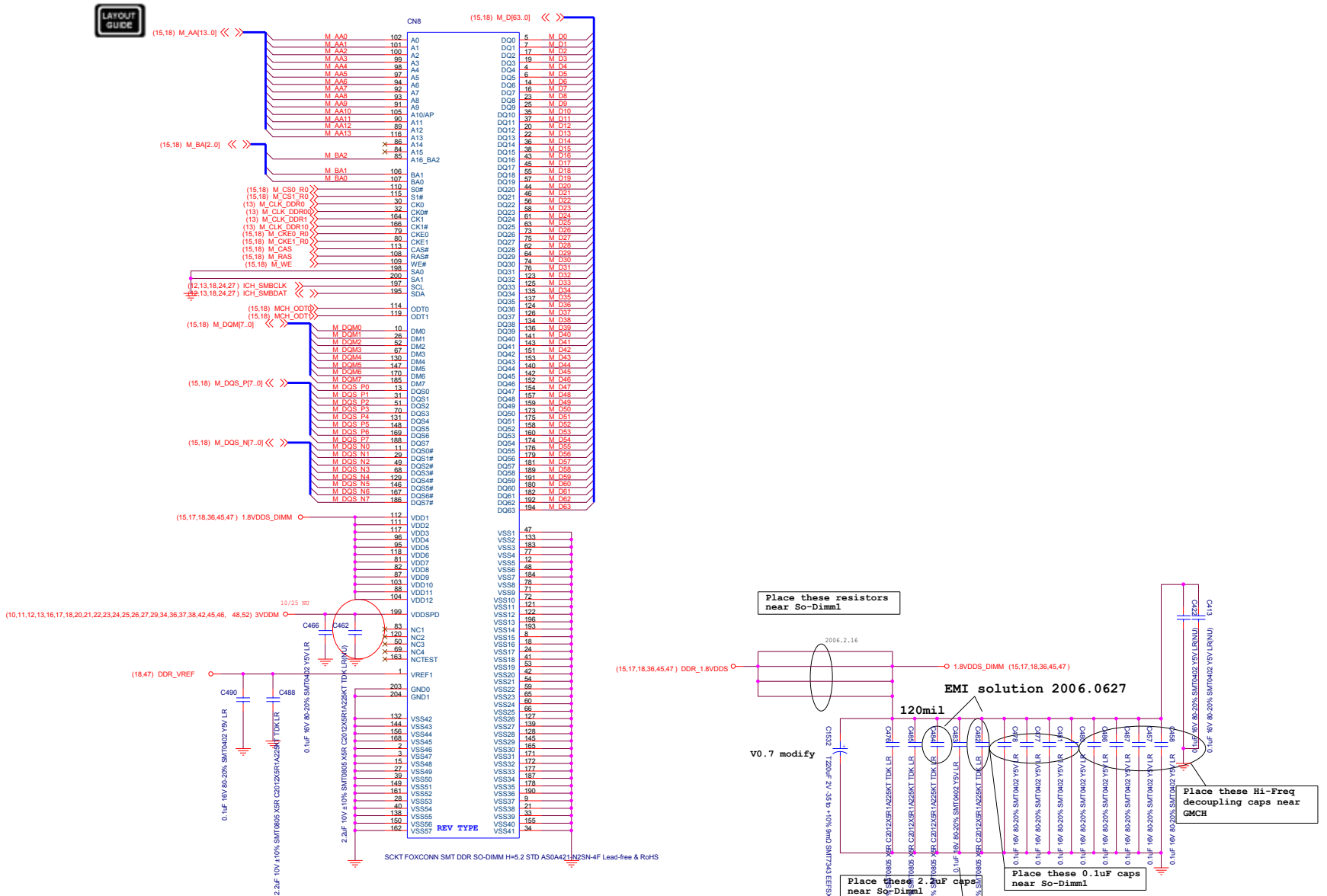
LAYOUT GUIDE
CN8
(15,18) M_AA[13..0]
(15,18) M_BA[2..0]
(15,18) M_D[63..0]
(15,18) M_DQM[7..0]
(15,18) M_DQS_P[7..0]
(15,18) M_DQS_N[7..0]
(15,17,18,36,45,47) 1.8VDDS_DIMM
(10,11,12,13,16,17,18,20,21,22,23,24,25,26,27,29,34,36,37,38,42,45,46, 48,52) 3VDDM
(18,47) DDR_VREF
(12,13,18,24,27) ICH_SMBCLK
(12,13,18,24,27) ICH_SMBDAT
(13) M_CLK_DDR0
(13) M_CLK_DDR0#
(13) M_CLK_DDR1
(13) M_CLK_DDR1#
(15,18) M_CS0_R0
(15,18) M_CS1_R0
(15,18) M_CKE0_R0
(15,18) M_CKE1_R0
(15,18) M_CAS
(15,18) M_RAS
(15,18) M_WE
(15,18) MCH_ODT0
(15,18) MCH_ODT1
REV TYPE
SCKT FOXCONN SMT DDR SO-DIMM H=5.2 STD AS0A421-N2SN-4F Lead-free & RoHS
SO DIMM 0
Place these resistors near So-Dimm1
(15,17,18,36,45,47) DDR_1.8VDDS
1.8VDDS_DIMM (15,17,18,36,45,47)
EMI solution 2006.0627
120mil
V0.7 modify
Place these 2.2uF caps near So-Dimm1
Place these 0.1uF caps near So-Dimm1
Place these Hi-Freq decoupling caps near GMCH
V0.4 EMI Modify
First International Computer, Inc.
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LM10W < VIA VN896 + VT8237A >
<DDR-dimm-2>
Tuesday, October 31, 2006
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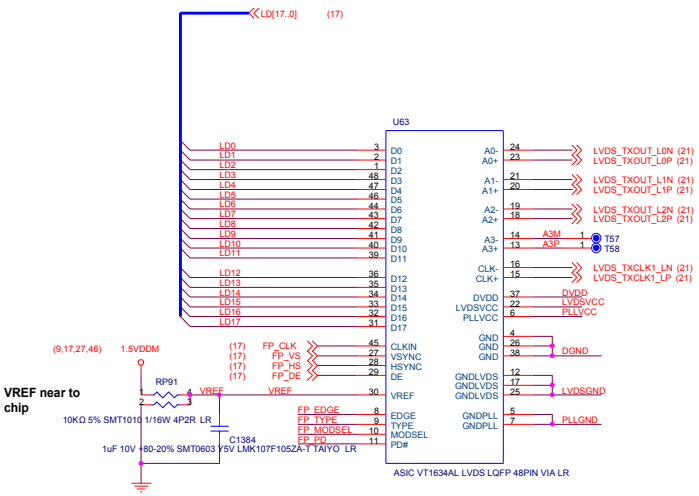
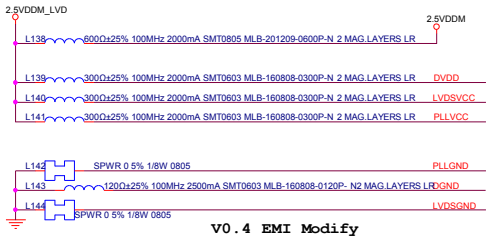
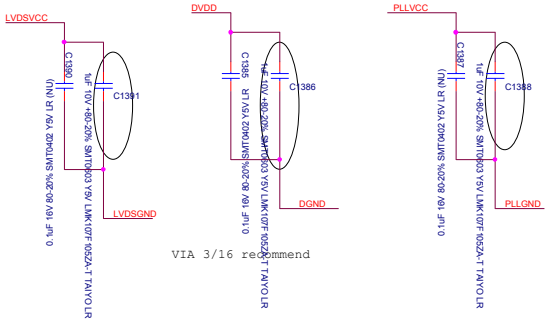
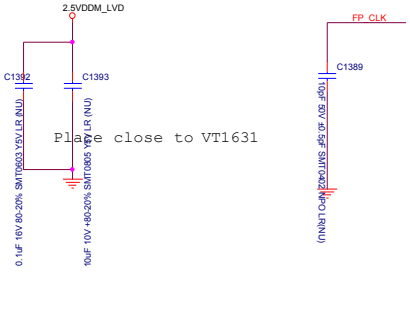




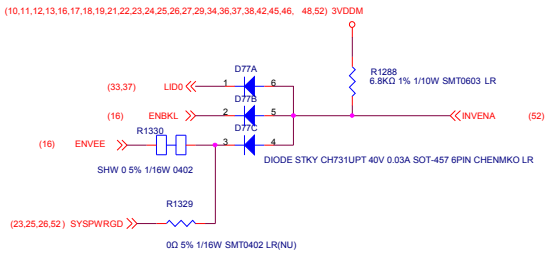
V0.4 EMI Modify

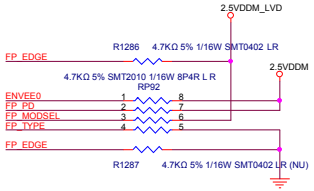
V0.4 EMI Modify

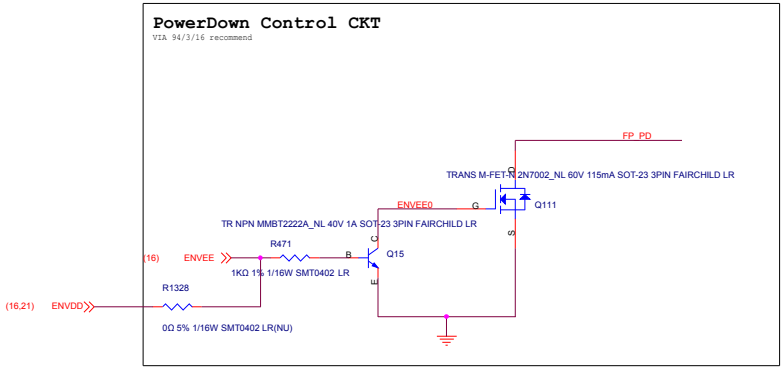


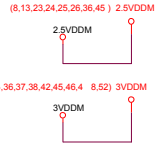


STRAPPING	PULL-UP	PULL-DOWN
FP_EDGE	**Falling edge**	Rising edge
FP_TYPE	MSB color mapping	**LSB color mapping**
FP_MODSEL	**18 bit**	12 bit









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Title: **LM10W< VIA VN896 + VT8237A+ >**

Size: C | Document Number: **<LVDS 1634AL>** | Rev: 0.7

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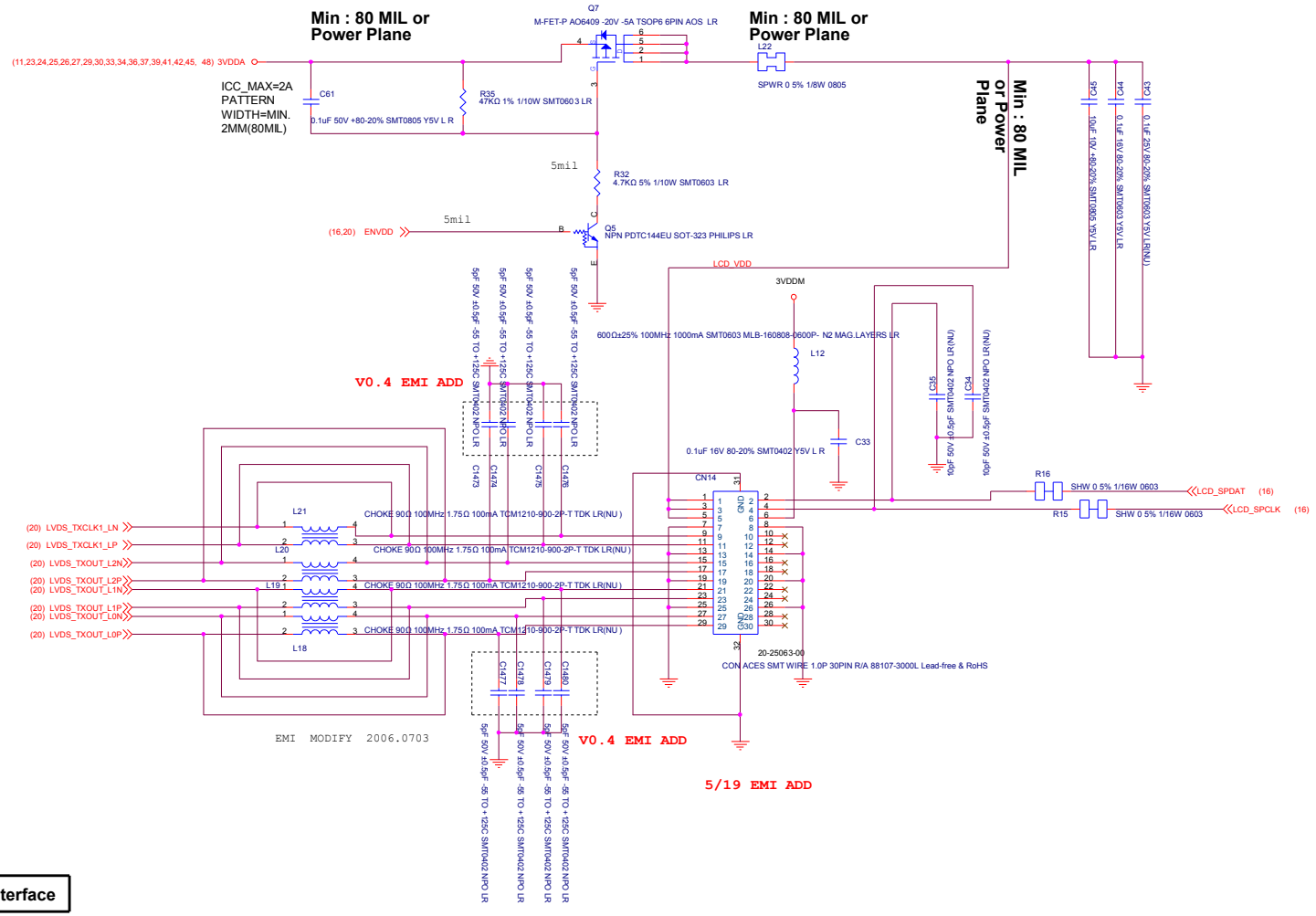

LVDS Interface

Signal	LENGTH	TRACE	SPACE	TRACE MUTCHING	Impedance	Note
LVDS	10" Cable MAX 16"	4 mils (stripline) 6 mils (microstrip)	20 mils 7 mils (edge to edge) 20 mils (pair to pair) 20 mils (to non LVDS signal)	+/-20 mils (data to data) +/-20 mils (with a clock pair) X +/-20 mils (clock to clock)	100 ohms +/-15%	Breakout region from NB should be less than 500 mils

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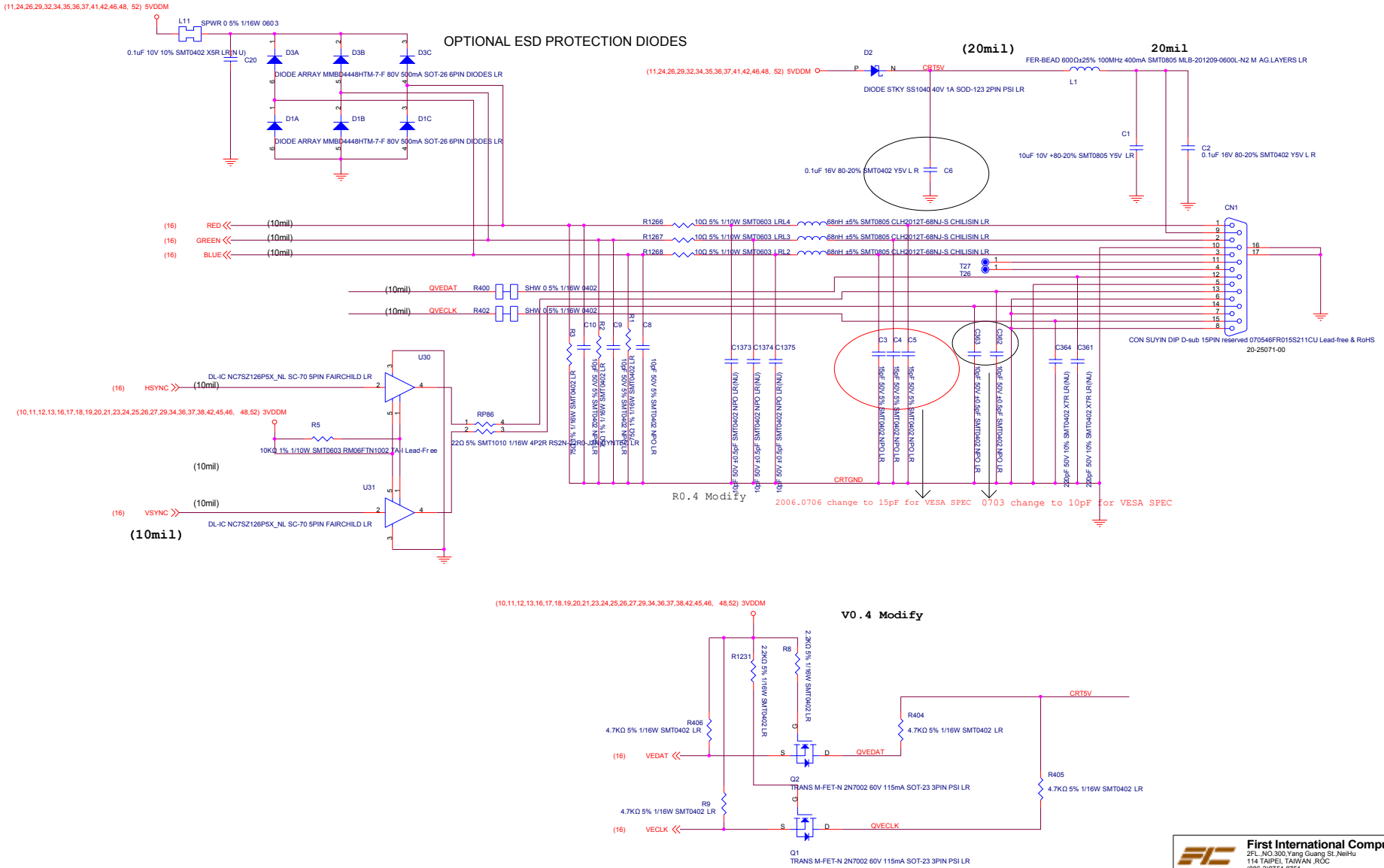
Title: LM10W < VIA VN896 + VT8237A >

Size: C | Document Number: <LCD connecter> | Rev: 0.7

Date: Tuesday, October 31, 2006 | Sheet 21 of 55



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Size: C | Document Number: <CRT connector> | Rev: 0.7

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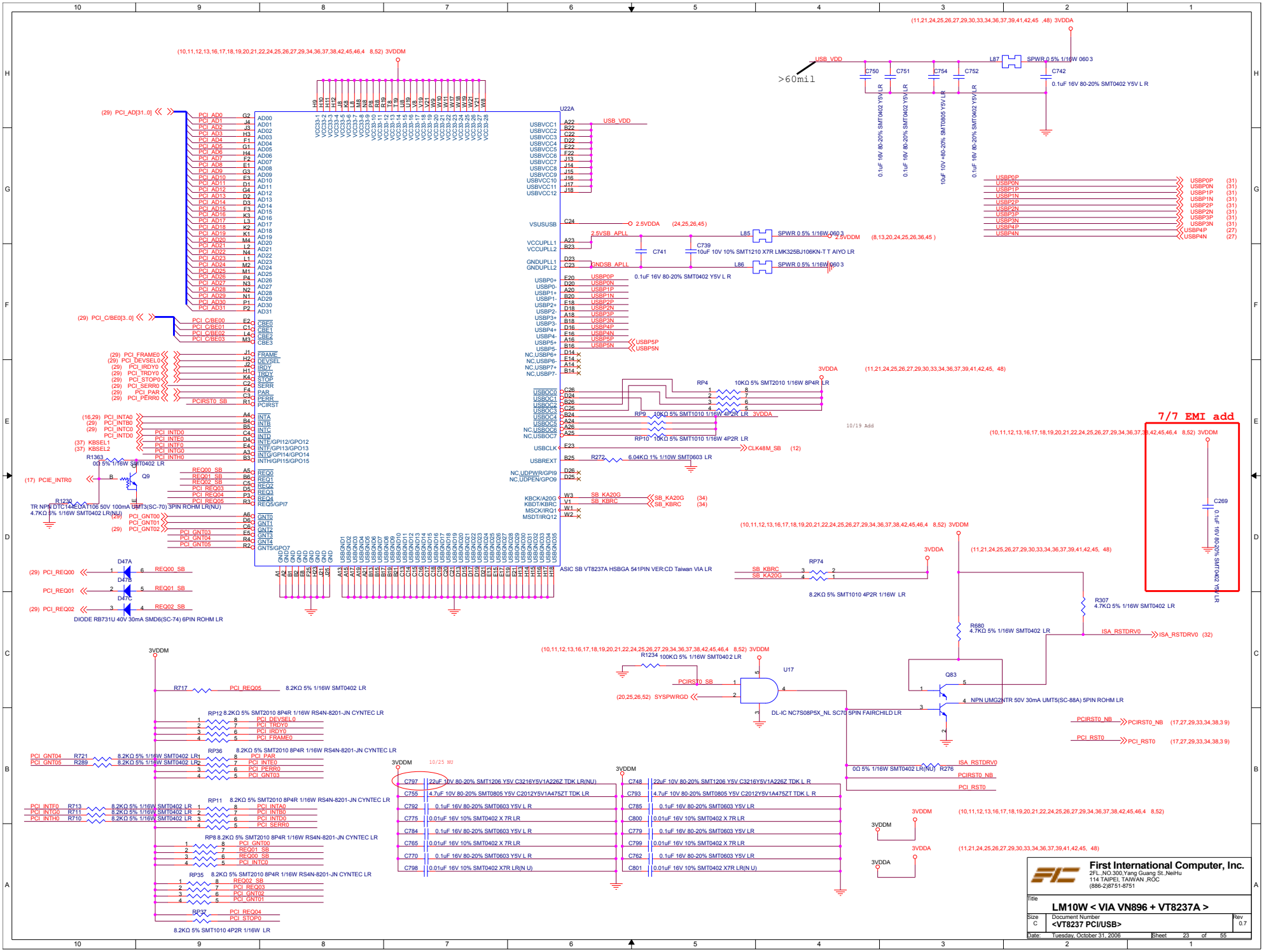
U22A
ASIC SB VT8237A HSBGA 541PIN VER:CD Taiwan VIA LR
U17
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR
DIODE RB731U 40V 30mA SMD6(SC-74) 6PIN ROHM LR
TR NPN DTC144EUA T106 50V 100mA UMT3(SC-70) 3PIN ROHM LR(NU)
NPN UMG2NTR 50V 30mA UMT5(SC-88A) 5PIN ROHM LR
7/7 EMI add
10/19 Add
10/25 NU
First International Computer, Inc.
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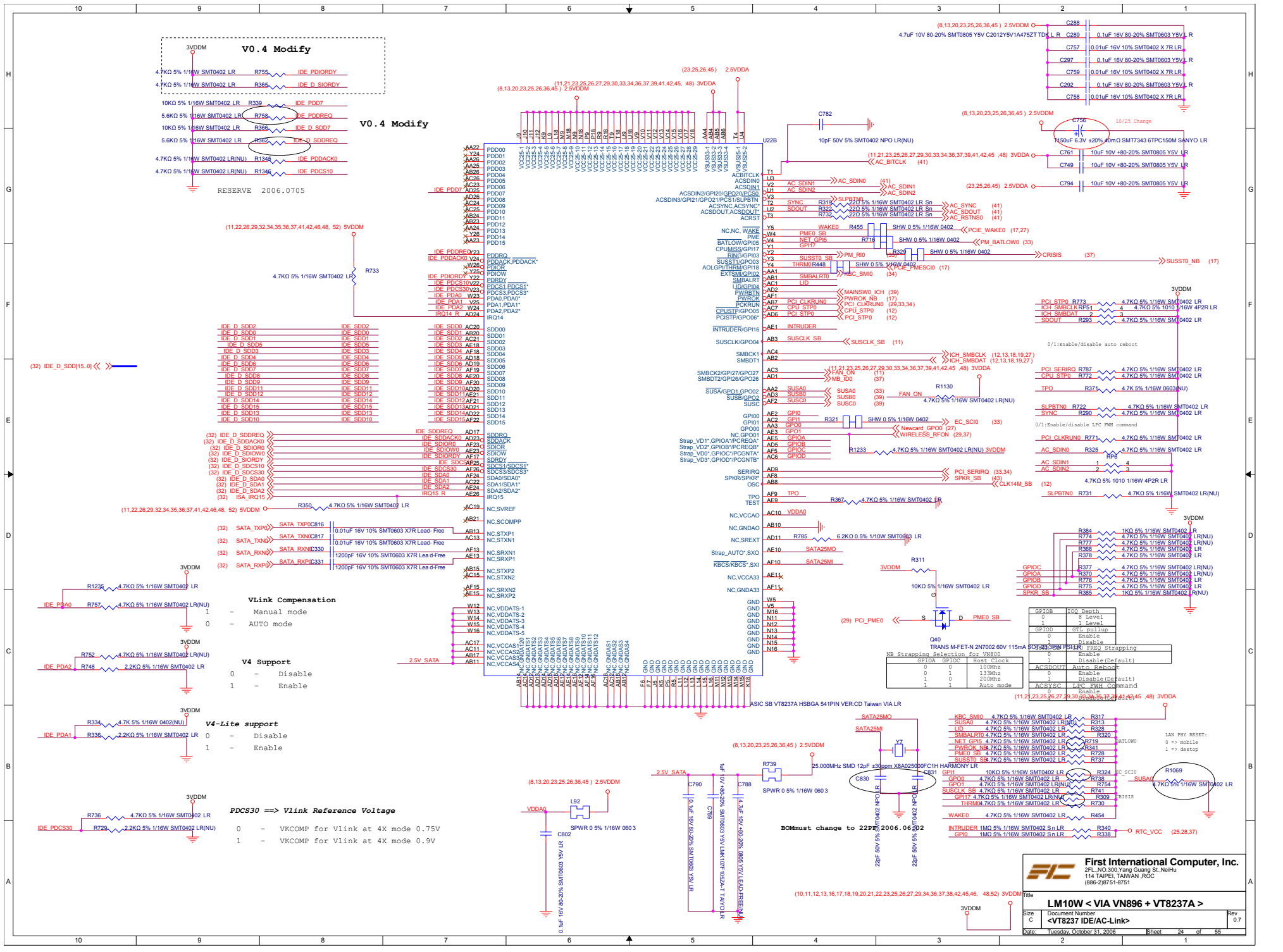
LM10W < VIA VN896 + VT8237A >
<VT8237 PCI/USB>
Tuesday, October 31, 2006
Sheet 23 of 55


V0.4 Modify
V0.4 Modify
RESERVE 2006.0705
VLink Compensation
V4 Support
V4-Lite support
PDCS30 ==> Vlink Reference Voltage
ASIC SB VT8237A HSBGA 541PIN VER:CD Taiwan VIA LR
BOMmust change to 22PF 2006.06.02
First International Computer, Inc.
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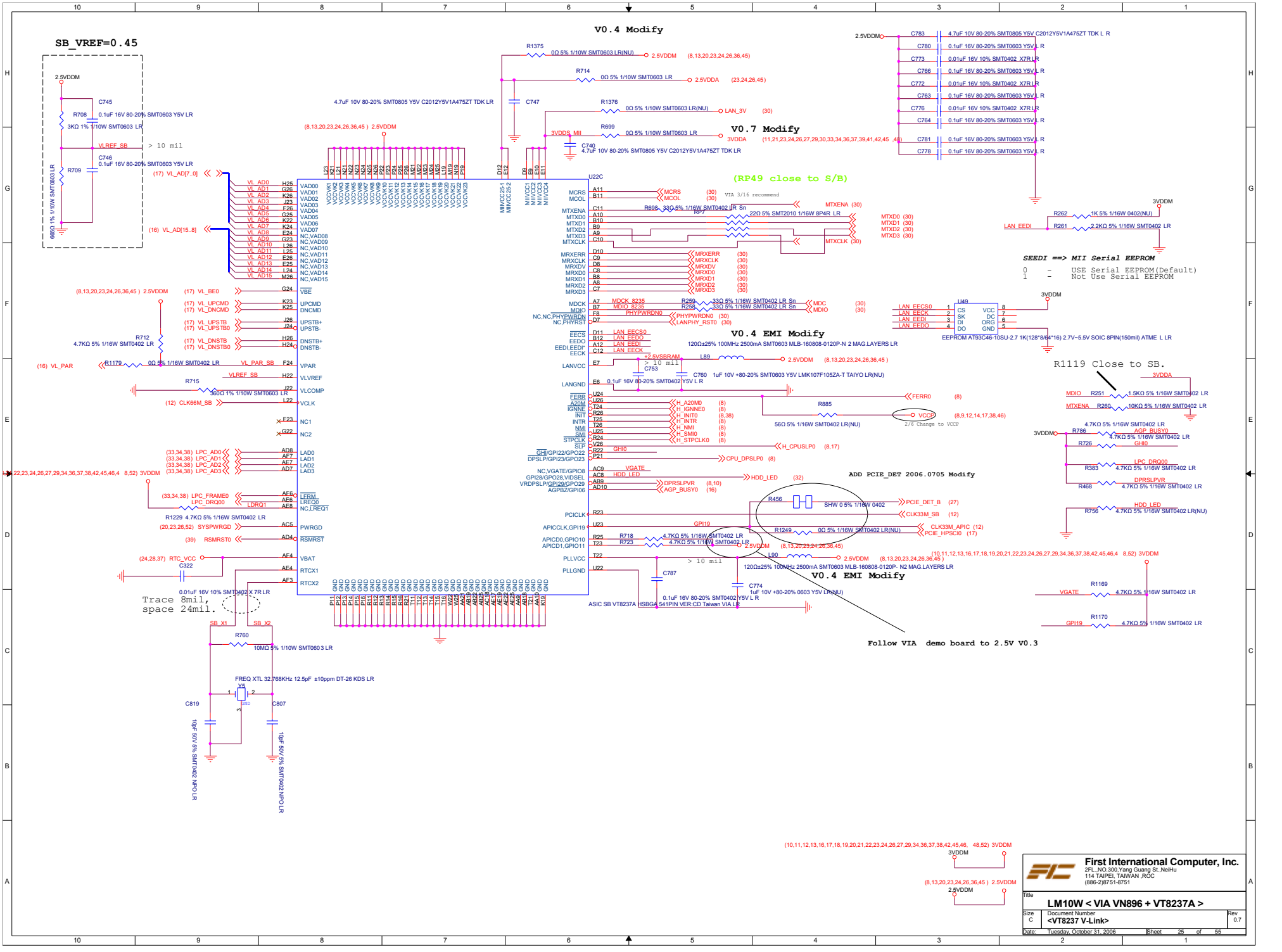
LM10W < VIA VN896 + VT8237A >
<VT8237 IDE/AC-Link>
Tuesday, October 31, 2006


SB_VREF=0.45
V0.4 Modify
V0.7 Modify
(RP49 close to S/B)
V0.4 EMI Modify
V0.4 EMI Modify
ADD PCIE_DET 2006.0705 Modify
R1119 Close to SB.
SEEDI ==> MII Serial EEPROM
0 - USE Serial EEPROM(Default)
1 - Not Use Serial EEPROM
Trace 8mil, space 24mil.
Follow VIA demo board to 2.5V V0.3
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LM10W < VIA VN896 + VT8237A >
<VT8237 V-Link>
Rev 0.7
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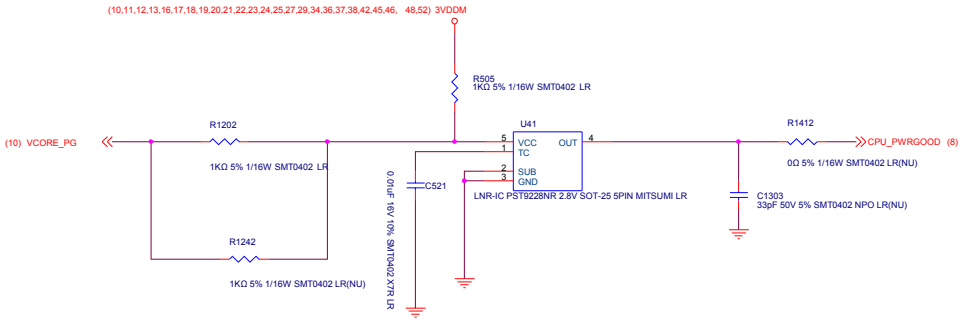
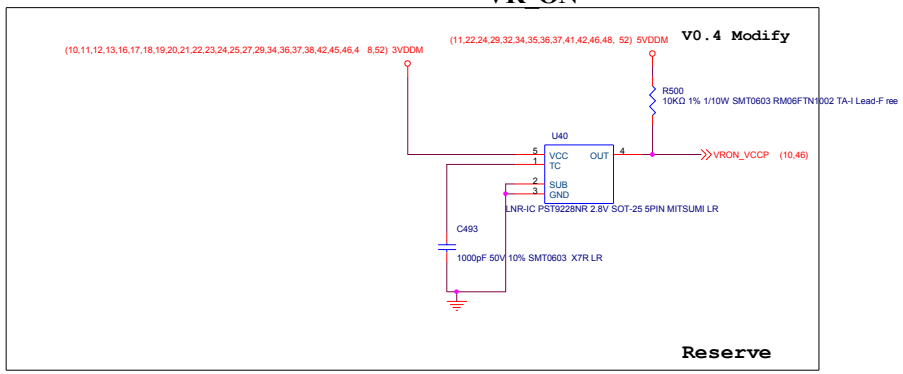
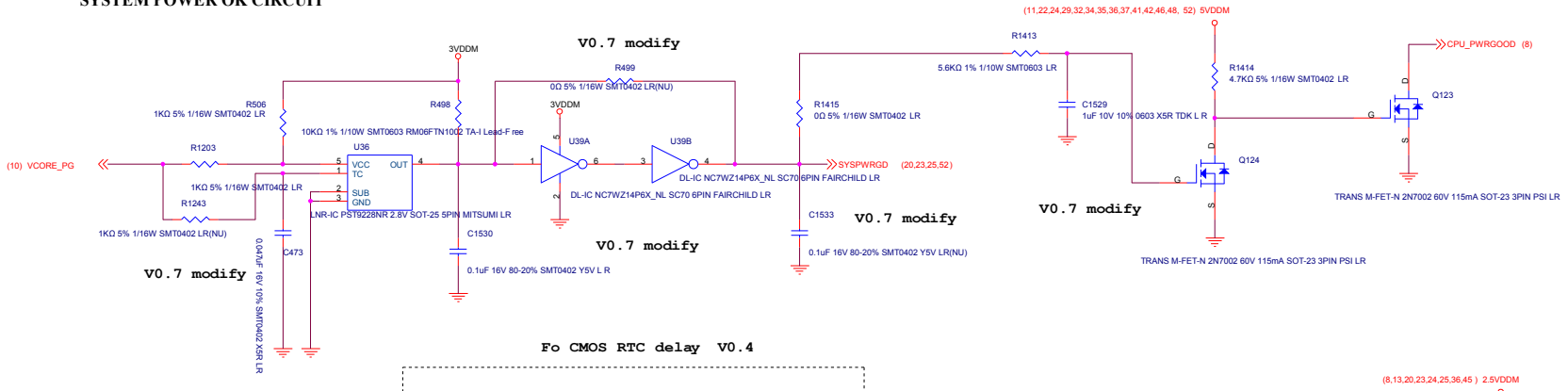
CPU POWER OK CIRCUIT

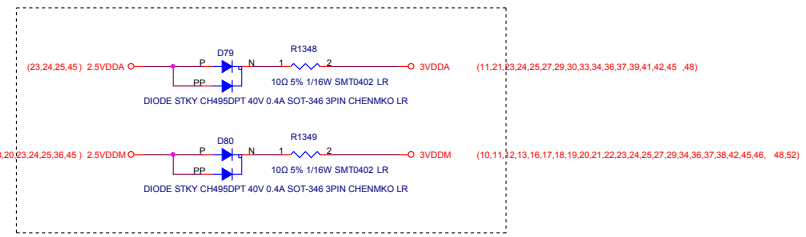


VR_ON



SYSTEM POWER OK CIRCUIT





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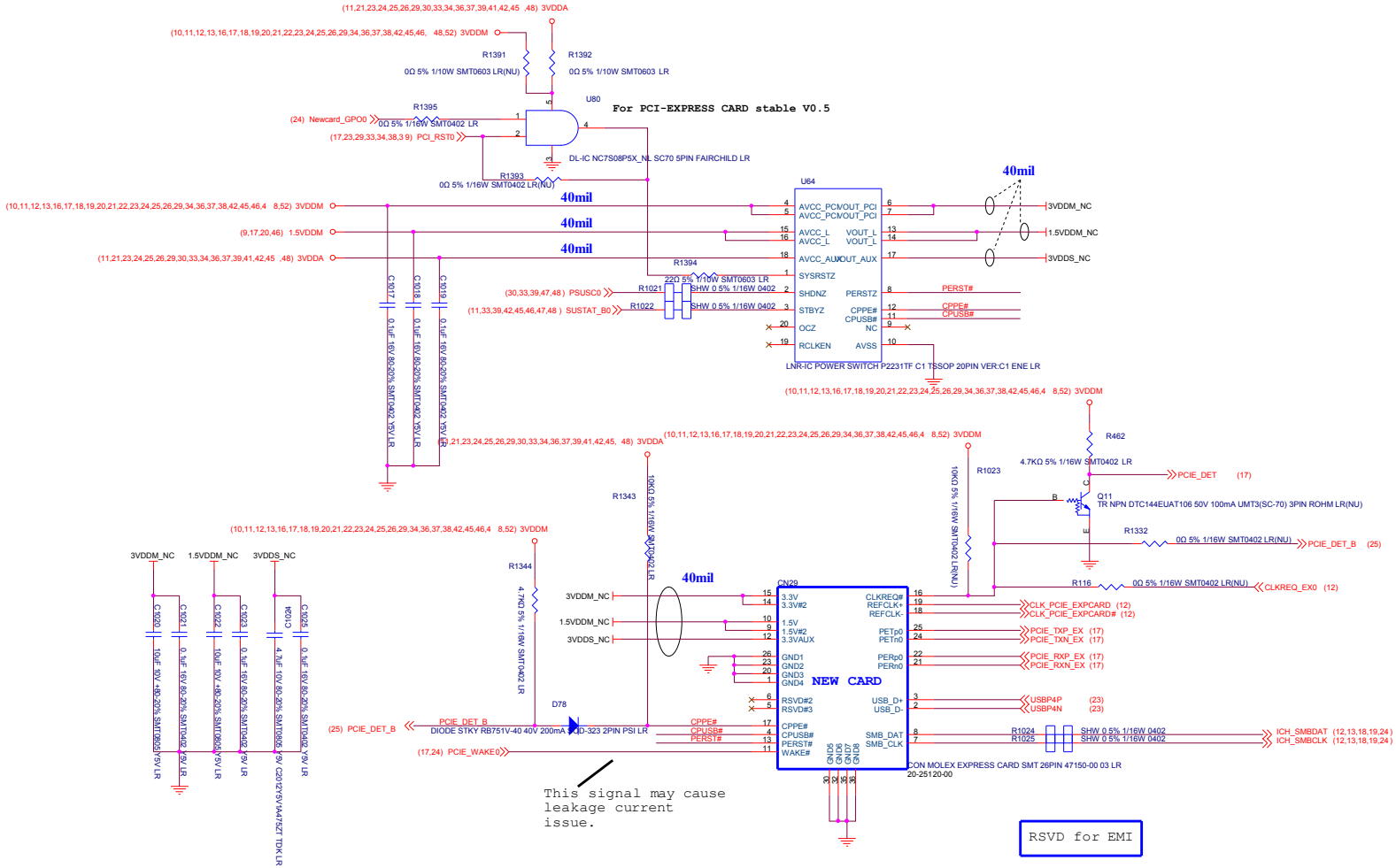
Title: LM10W < VIA VN896 + VT8237A >

Size: C | Document Number: <POWER Good> | Rev: 0.7

Date: Tuesday, October 31, 2006 | Sheet 26 of 55



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Title	LM10W < VIA VN896 + VT8237A >	
Size C	Document Number < CardBus Controller >	Rev 0.7
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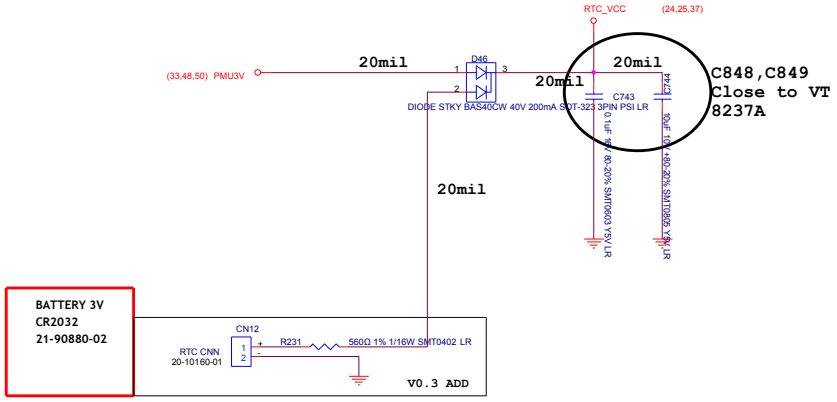
RTC Discharge Circuit



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Size: C	Document Number: < CardBus Power/CNN >	Rev: 0.7
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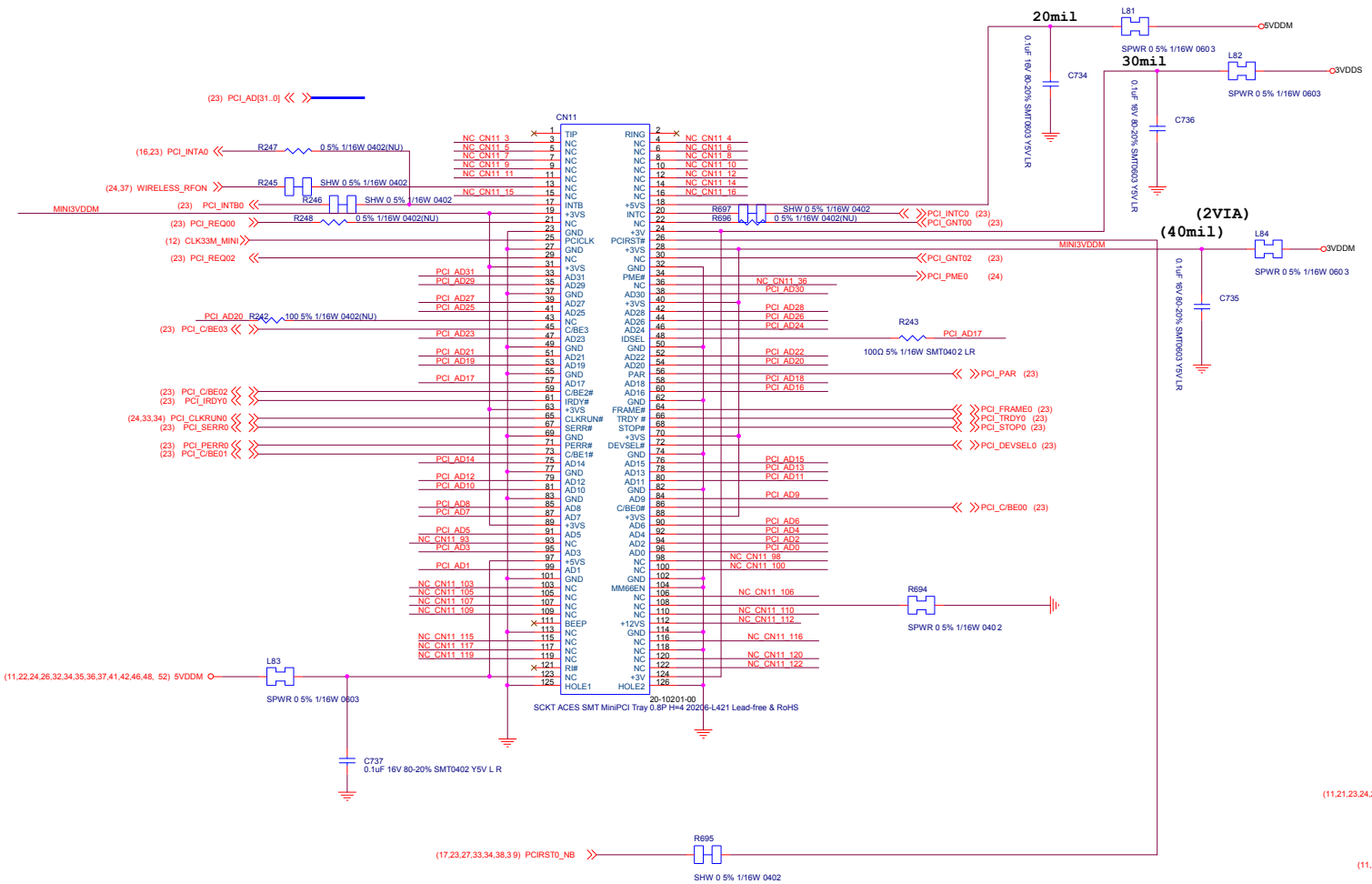
TYPE III MODEM / LAN CONNECTOR



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Title	LM10W < VIA VN896 + VT8237A >	
Size C	Document Number <Mini-PCI>	Rev 0.7
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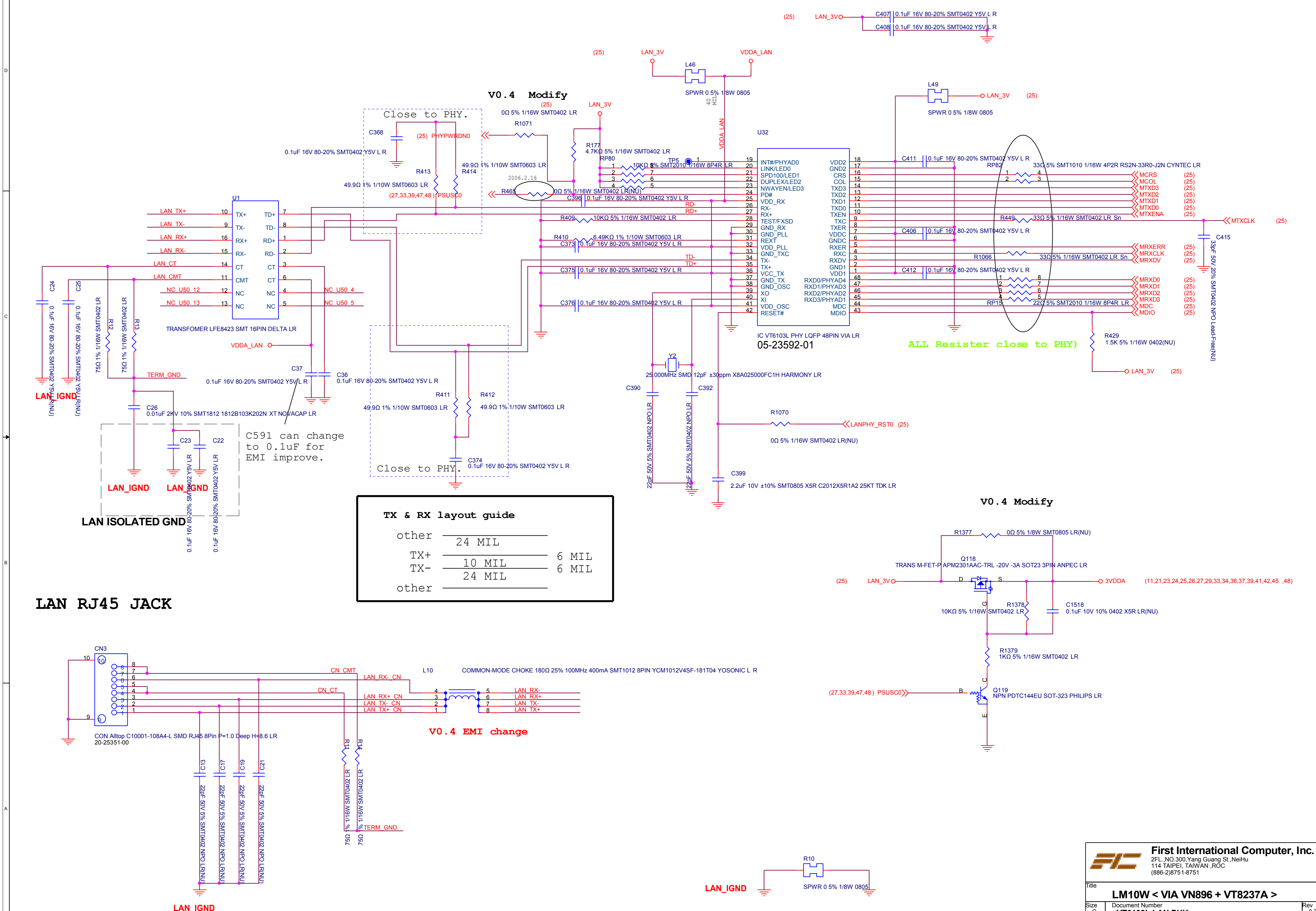

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Title	LM10W < VIA VN896 + VT8237A >	
Size C	Document Number <VT6103L LAN PHY>	Rev 0.7
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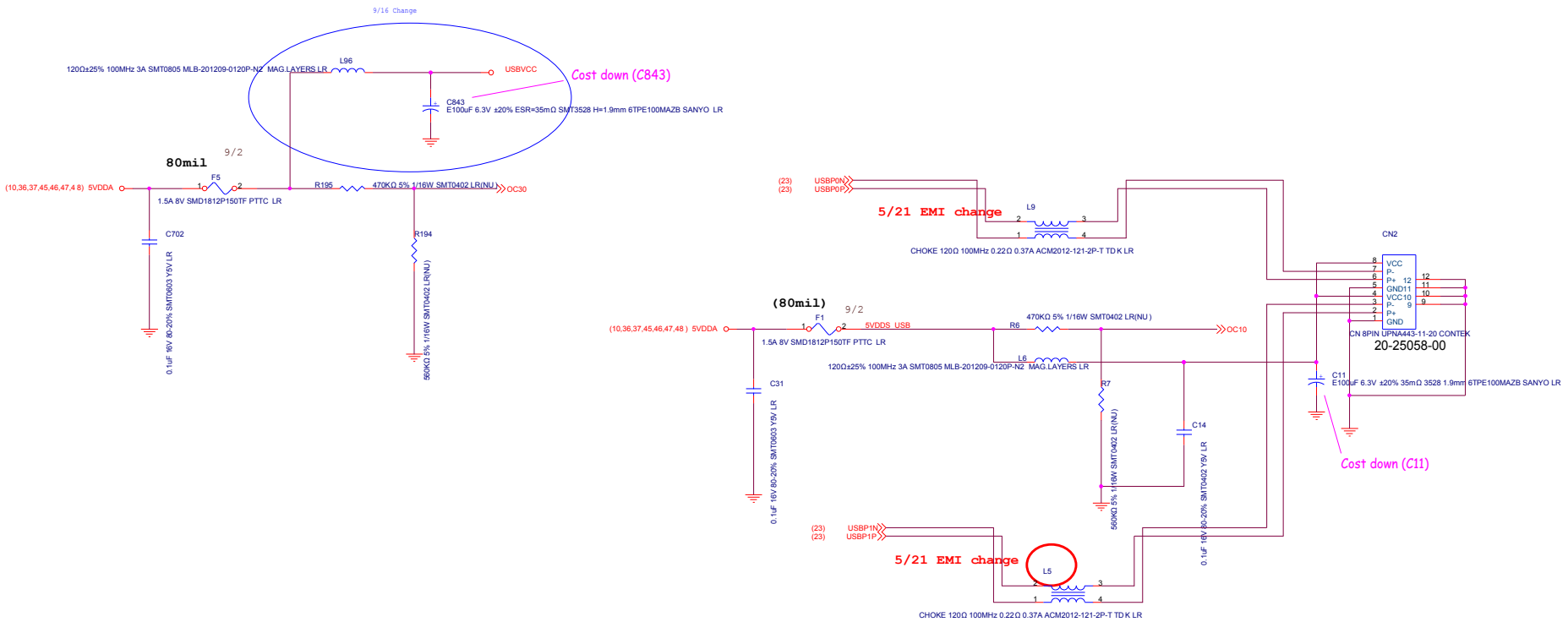

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Title	**LM10W < VIA VN896 + VT8237A >**	
Size: C	Document Number: **<USB CNN>**	Rev: 0.7
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SATA Layout Note:

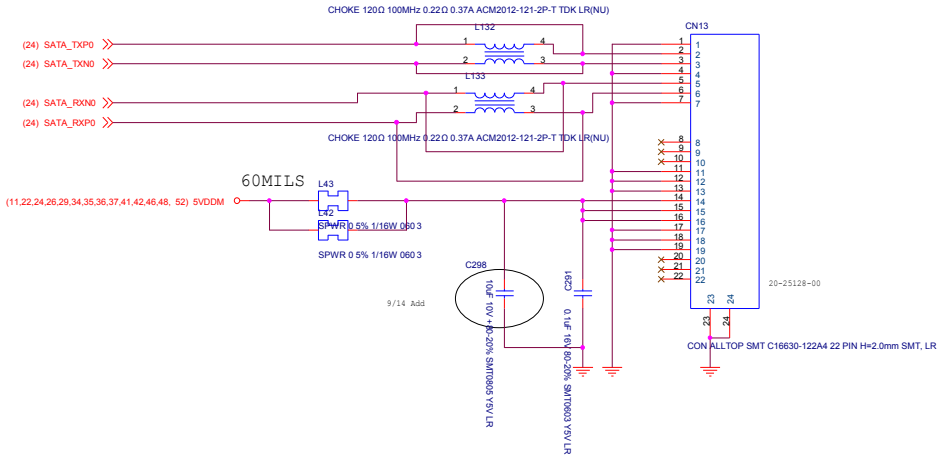
MS or SL:

20mils	+	6mils	−	20mils	−	6mils	+	20mils
		TX				RX		

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

NOTE

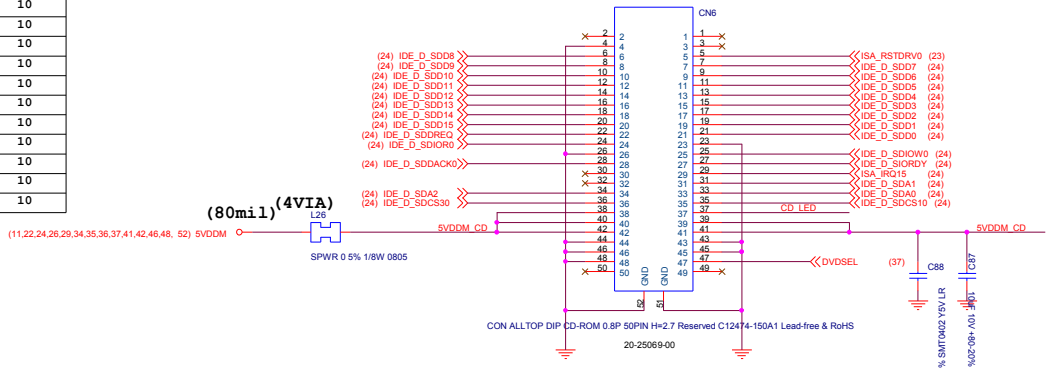
SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

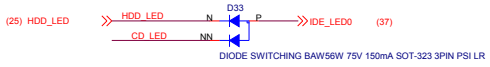


IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN





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Title: LM10W < VIA VN896 + VT8237A >
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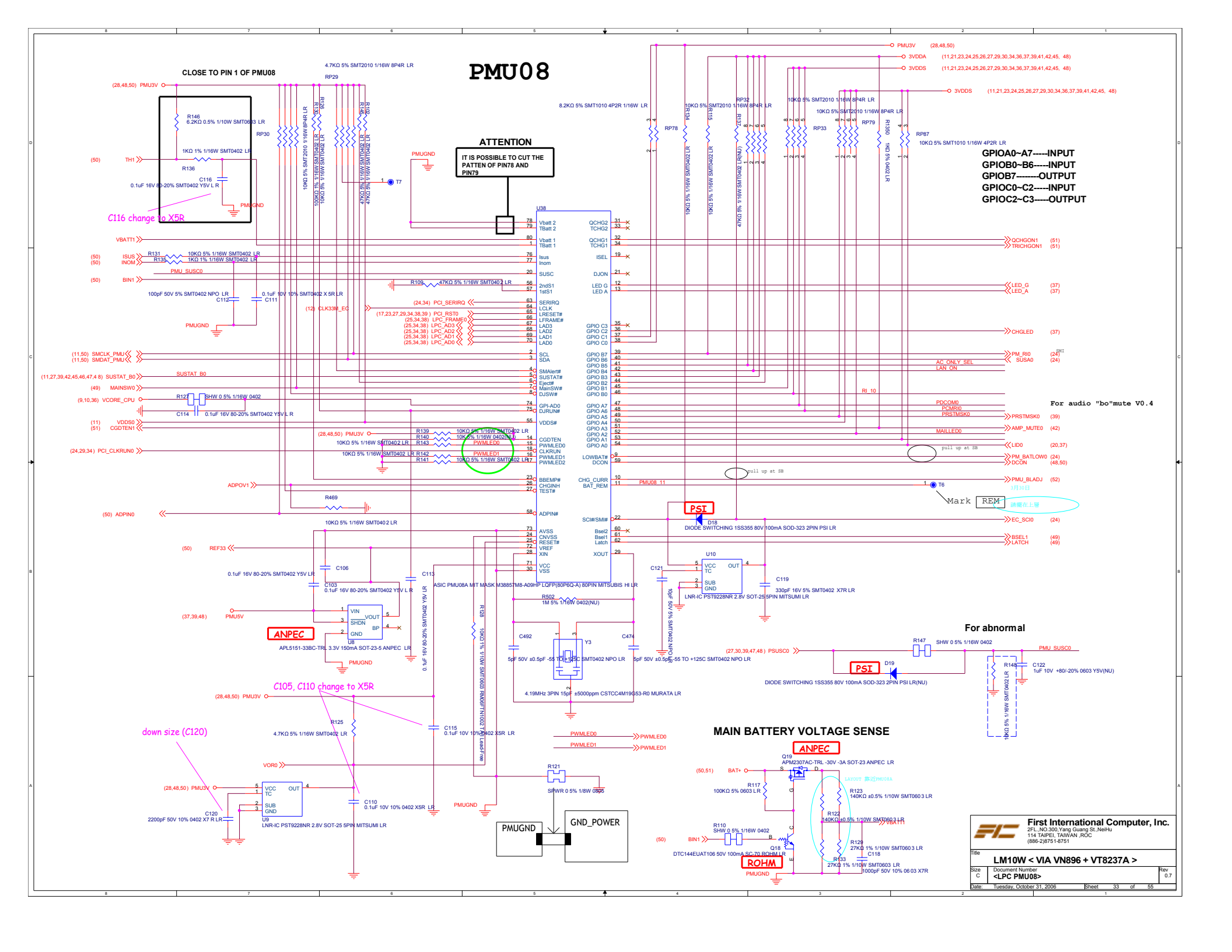
PMU08
CLOSE TO PIN 1 OF PMU08
ATTENTION
IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79
GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT
C116 change to X5R
C105, C110 change to X5R
down size (C120)
For audio "bo"mute V0.4
For abnormal
MAIN BATTERY VOLTAGE SENSE
ASIC PMU08A MIT MASK M38857M8-A09HP LQFP(80P6Q-A) 80PIN MITSUBIS HI LR
4.19MHz 3PIN 15pF ±5000ppm CSTCC4M19G53-R0 MURATA LR
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
APL5151-33BC-TRL 3.3V 150mA SOT-23-5 ANPEC LR
LNR-IC PST9228NR 2.8V SOT-25 5PIN MITSUMI LR
APM2307AC-TRL -30V -3A SOT-23 ANPEC LR
DTC144EUAT106 50V 100mA SC-70 ROHM LR
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LM10W < VIA VN896 + VT8237A >
<LPC PMU08>
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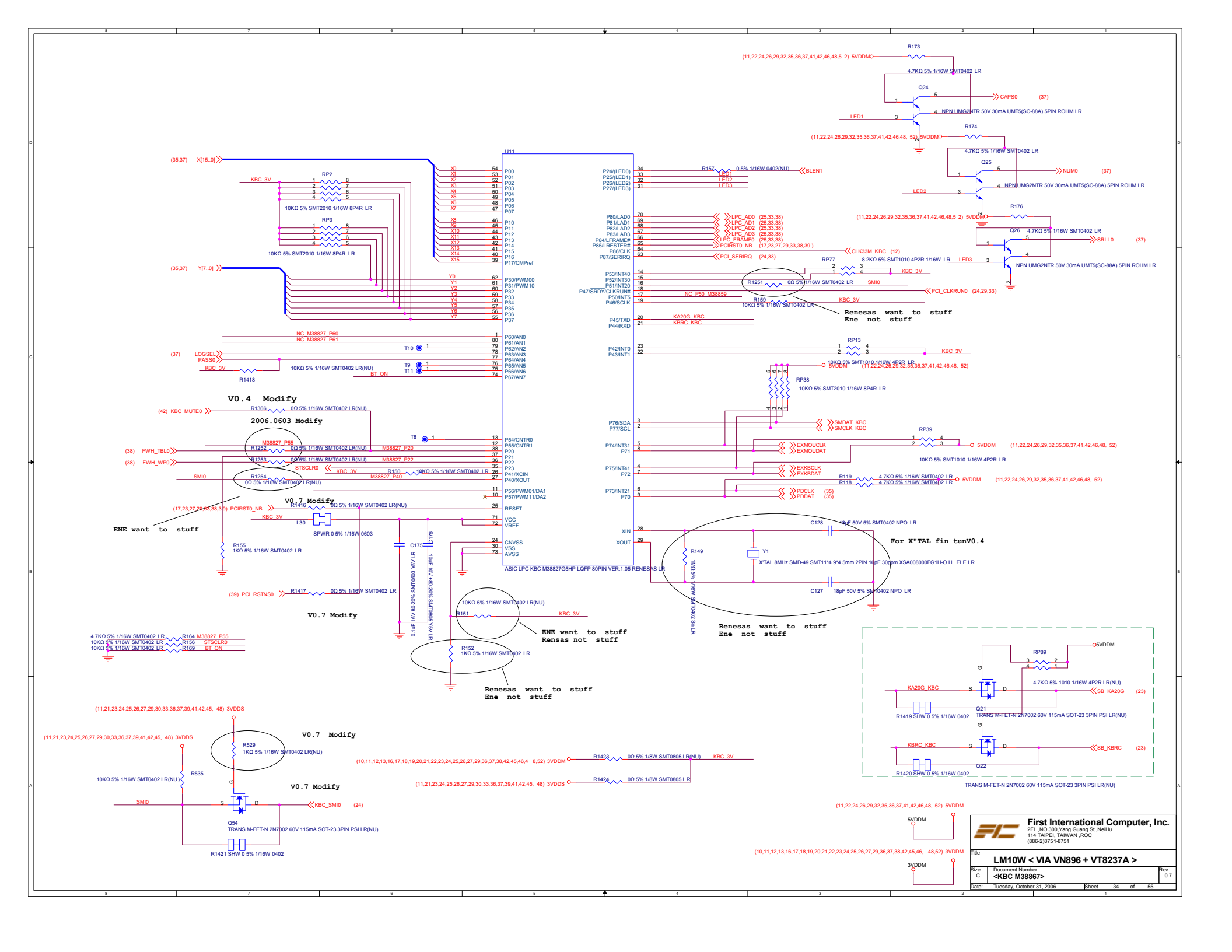
U11
ASIC LPC KBC M38827G5HP LQFP 80PIN VER:1.05 RENESAS LR
V0.4 Modify
2006.0603 Modify
V0.7 Modify
ENE want to stuff
Renesas want to stuff
Ene not stuff
For X"TAL fin tunV0.4
XTAL 8MHz SMD-49 SMT11*4.9*4.5mm 2PIN 16pF 30ppm XSA008000FG1H-O H .ELE LR
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU)
First International Computer, Inc.
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LM10W < VIA VN896 + VT8237A >
Document Number
<KBC M38867>
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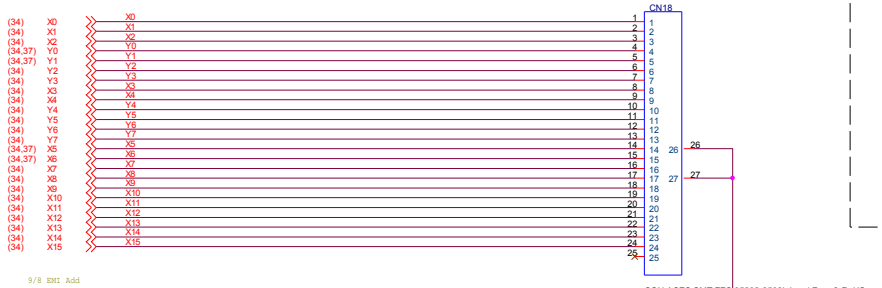
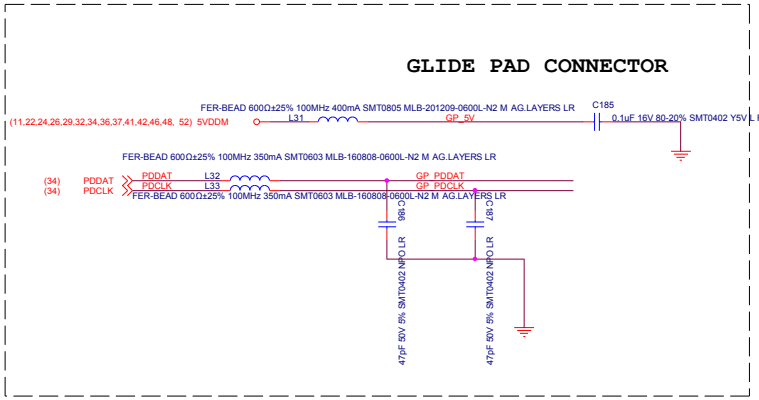
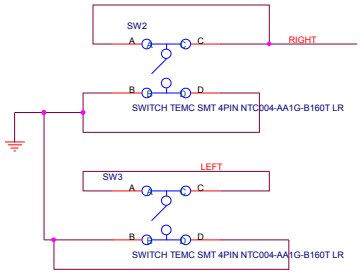
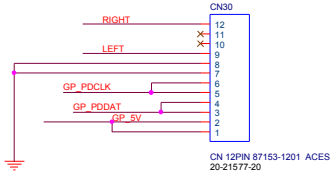
INT KB CNN

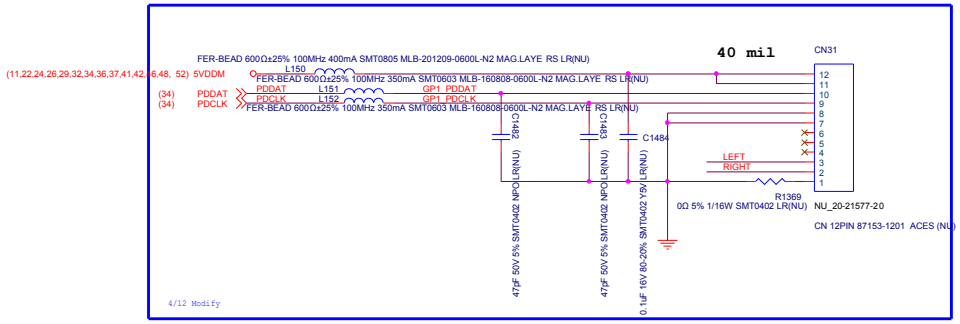








V0.4 Modify Reserve



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Title	LM10W < VIA VN896 + VT8237A >	
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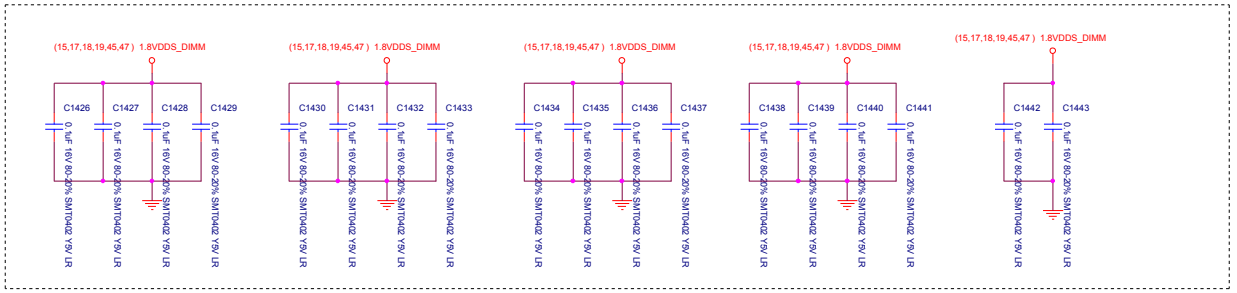
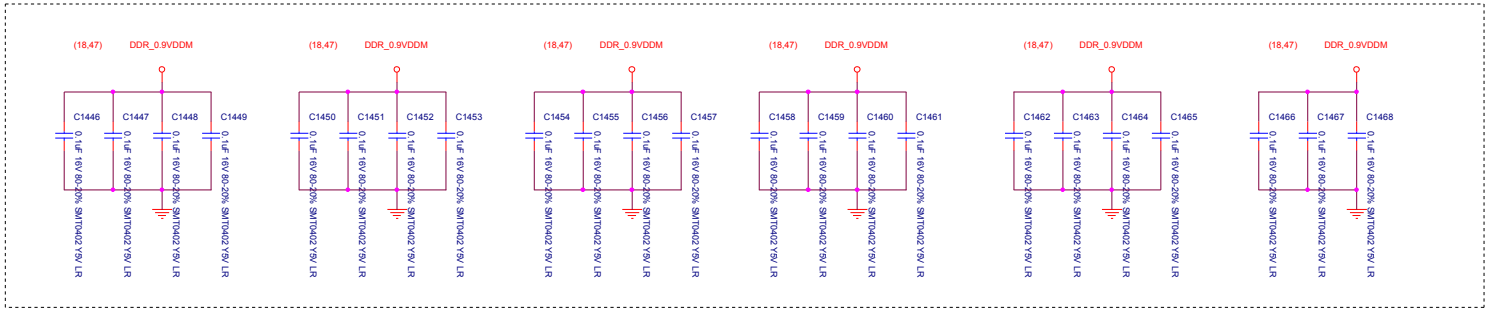
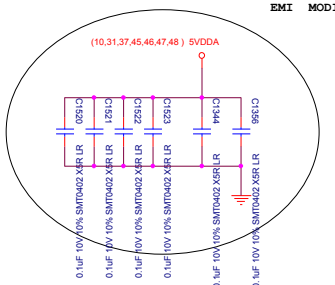
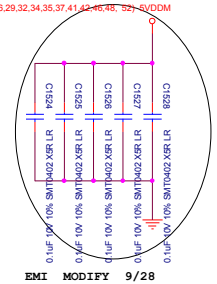
EMI MODIFY 9/28



EMI solution 2006.0627

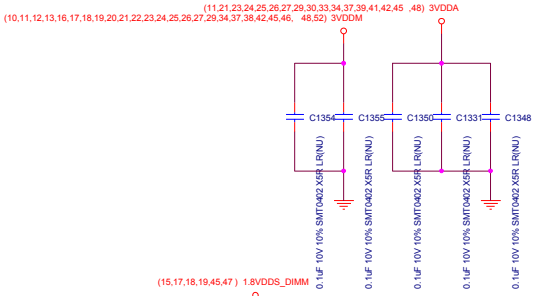


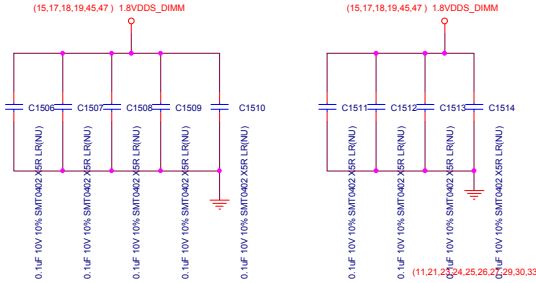




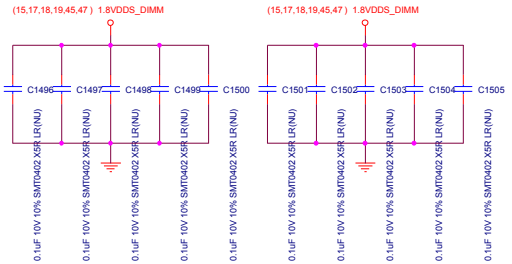
EMI MODIFY 9/28

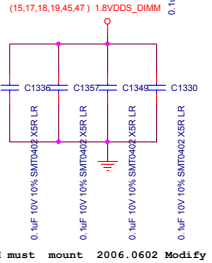
EMI solution V0.7



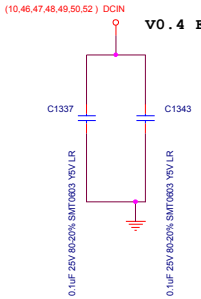


EMI V0.4 Modify

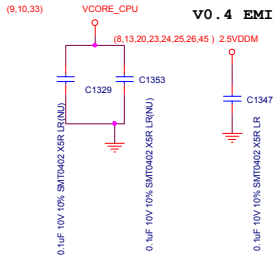




BOM must mount 2006.0602 Modify

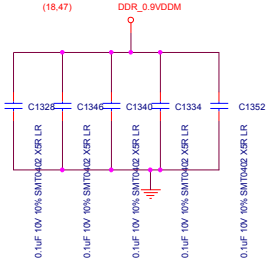


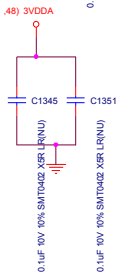
V0.4 EMI Modify

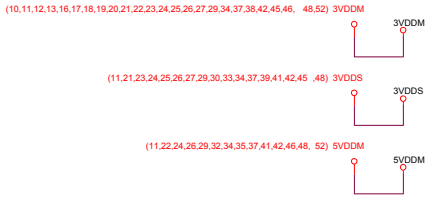


V0.4 EMI Modify

BOM must mount 2006.0602 Modify







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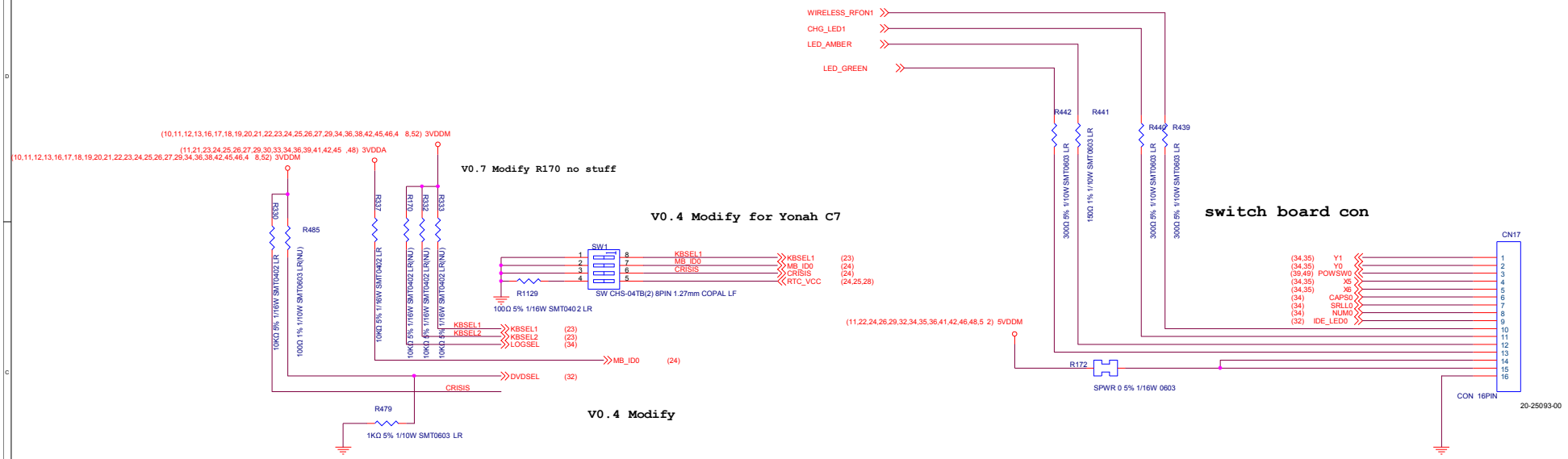
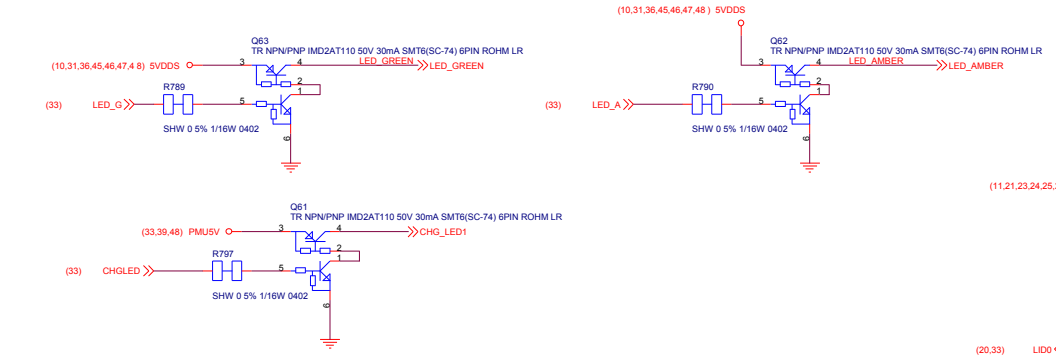
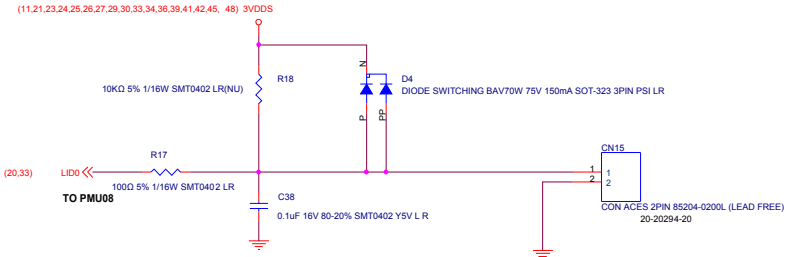
DIP SWITCH



LED indicator control logic



LID Switch



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Title	LM10W < VIA VN896 + VT8237A >	
Size: C	Document Number: <DIP SW/ LED>	Rev: 0.7
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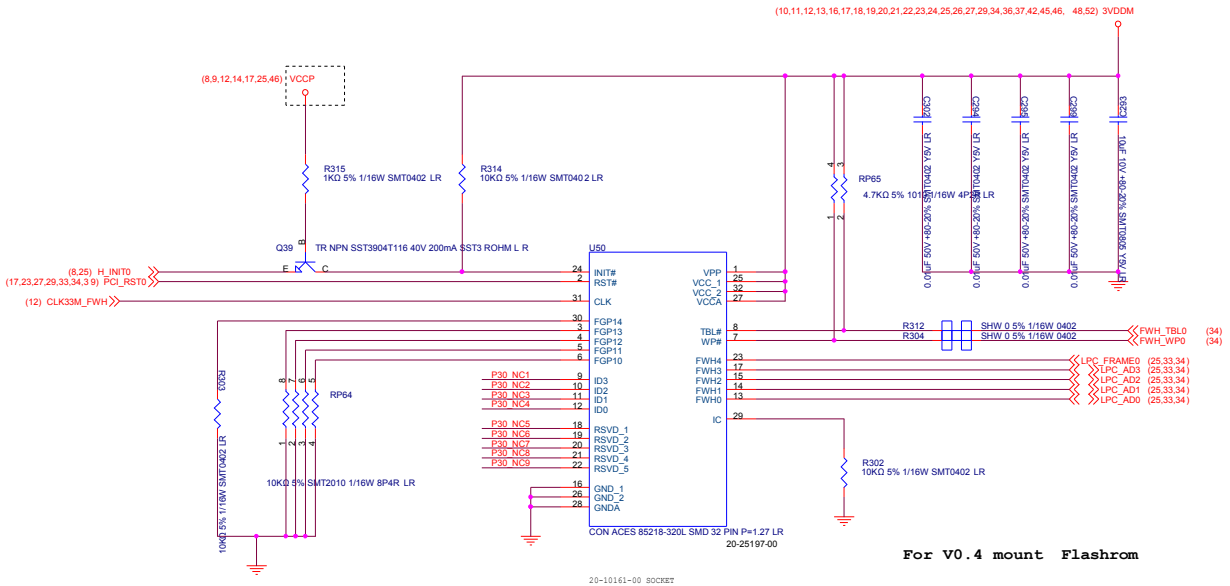
4M FLASH ROM



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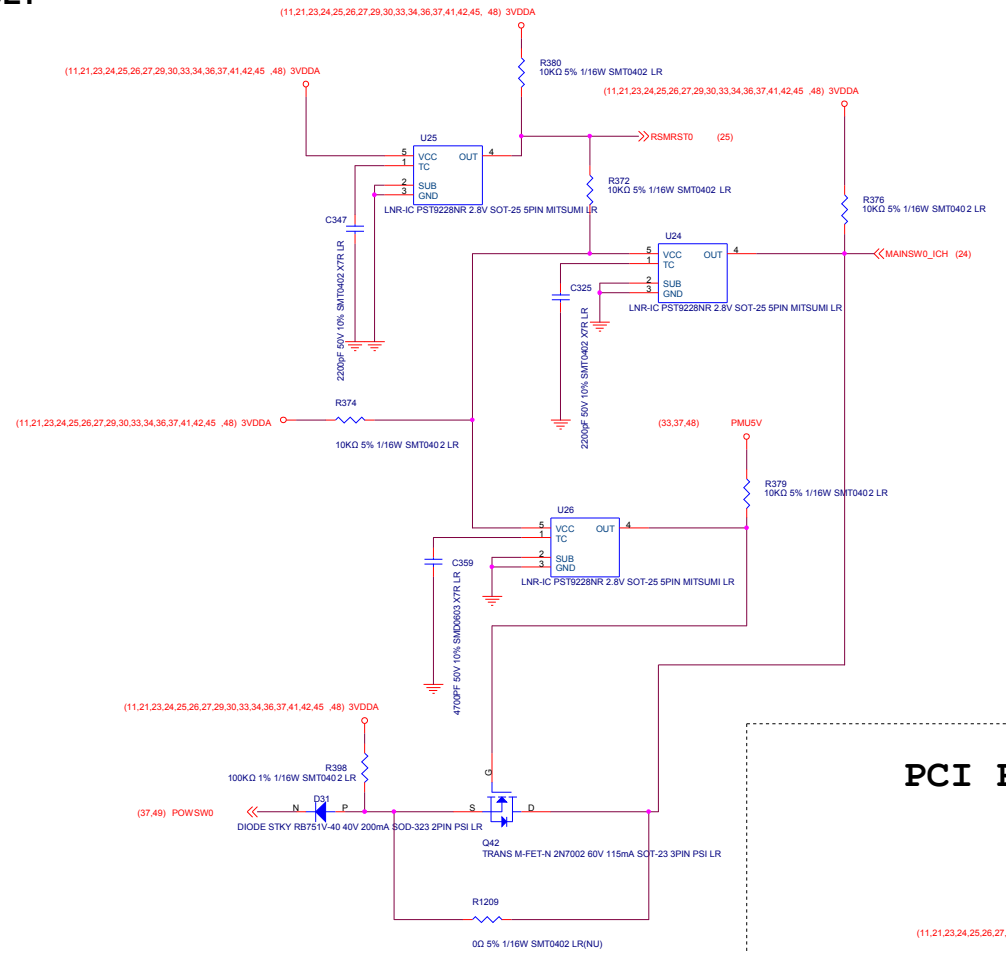
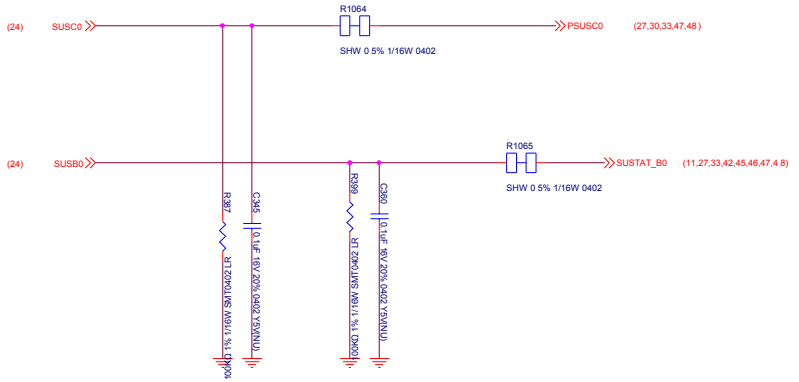
(886-2)8751-8751

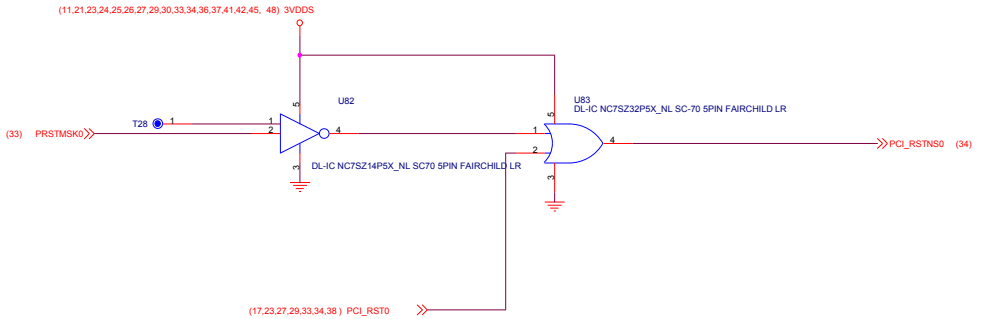
Title	LM10W < VIA VN896 + VT8237A >	
Size C	Document Number <LID SW/ BIOS>	Rev 0.7
Date: Tuesday, October 31, 2006	Sheet 38 of 55	

RESUME RESET





PCI RESET & PCI NON RESET



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Title	LM10W < VIA VN896 + VT8237A >	
Size C	Document Number <Reset Circuit>	Rev 0.7
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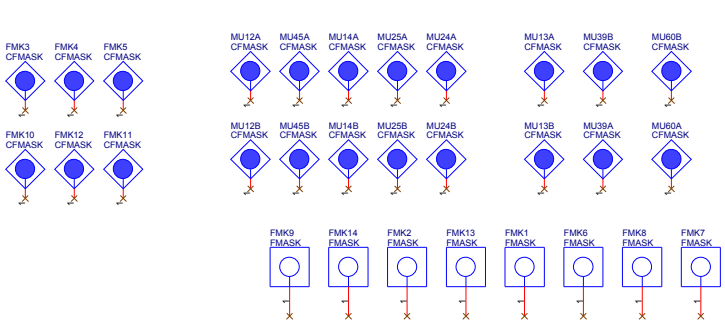
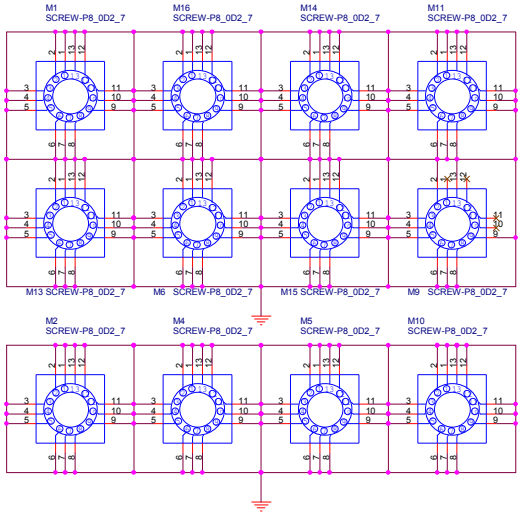
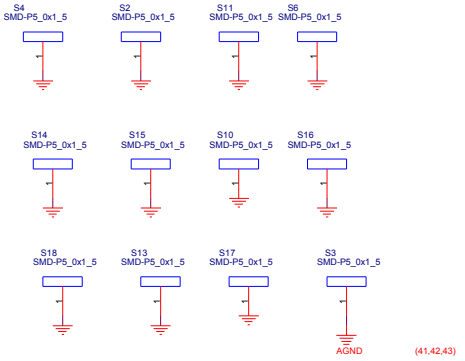
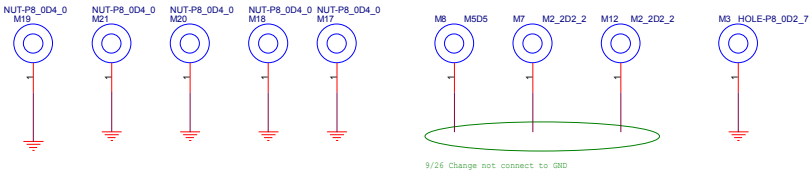
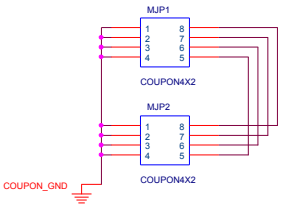








COUPON4X2



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Title: **LM10W < VIA VN896 + VT8237A >**

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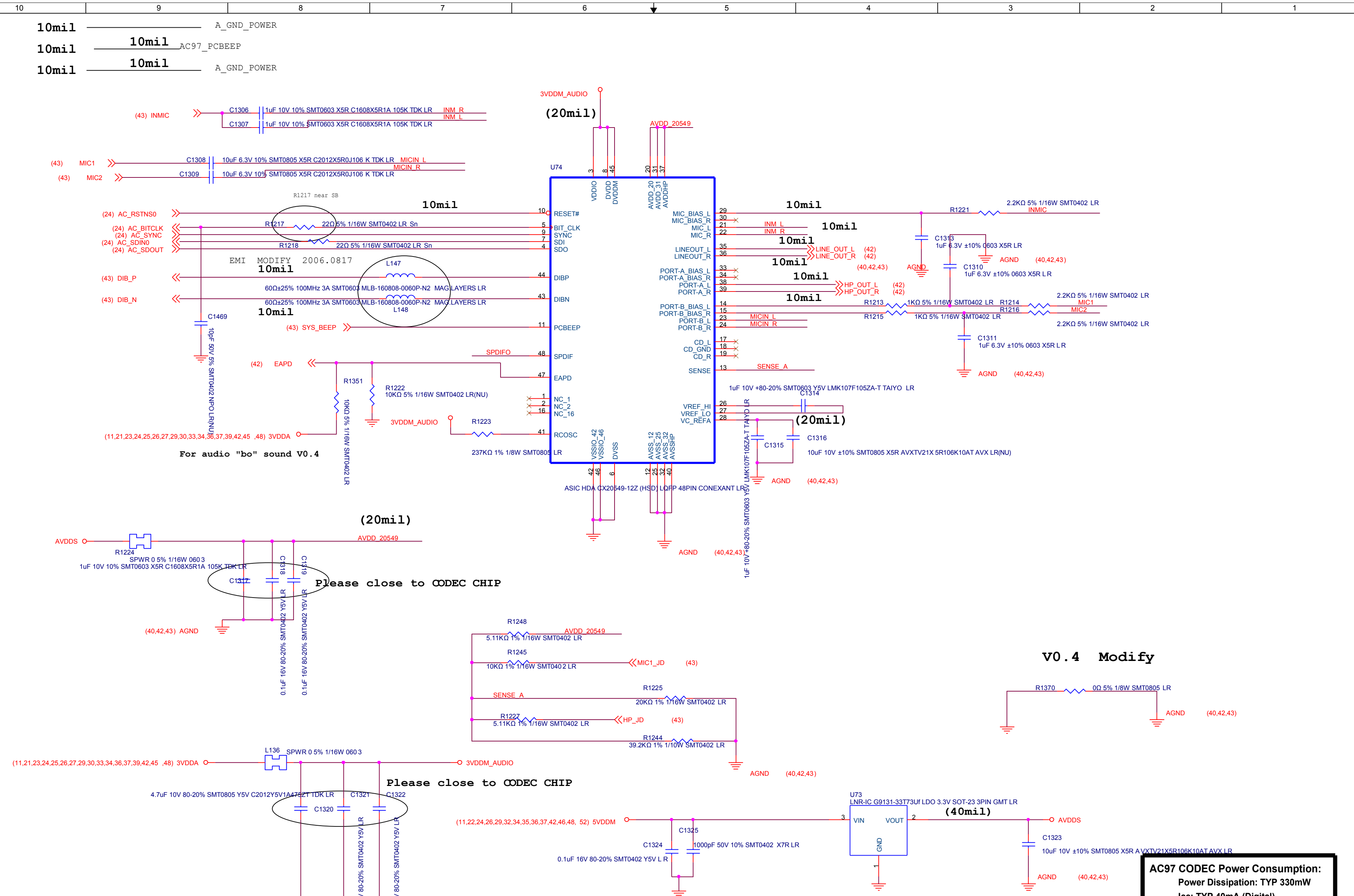
10mil A_GND_POWER
10mil AC97_PCBEEP
10mil A_GND_POWER
3VDDM_AUDIO
(20mil)
AVDD_20549
U74
(43) INMIC
C1306 1uF 10V 10% SMT0603 X5R C1608X5R1A 105K TDK LR INM_R
C1307 1uF 10V 10% SMT0603 X5R C1608X5R1A 105K TDK LR INM_L
(43) MIC1 C1308 10uF 6.3V 10% SMT0805 X5R C2012X5R0J106 K TDK LR MICIN_L
(43) MIC2 C1309 10uF 6.3V 10% SMT0805 X5R C2012X5R0J106 K TDK LR MICIN_R
R1217 near SB
(24) AC_RSTNS0
(24) AC_BITCLK
(24) AC_SYNC
(24) AC_SDIN0
(24) AC_SDOUT
R1217 22Ω 5% 1/16W SMT0402 LR Sn
R1218 22Ω 5% 1/16W SMT0402 LR Sn
EMI MODIFY 2006.0817
L147
(43) DIB_P
(43) DIB_N
60Ω±25% 100MHz 3A SMT0603 MLB-160808-0060P-N2 MAG LAYERS LR
L148
C1469 10pF 50V 5% SMT0402 NPO LR(NU)
(43) SYS_BEEP
SPDIFO
(42) EAPD
R1351 10KΩ 5% 1/16W SMT0402 LR
R1222 10KΩ 5% 1/16W SMT0402 LR(NU)
3VDDM_AUDIO R1223 237KΩ 1% 1/8W SMT0805 LR
(11,21,23,24,25,26,27,29,30,33,34,36,37,39,42,45 ,48) 3VDDA
For audio "bo" sound V0.4
RESET# BIT_CLK SYNC SDI SDO DIBP DIBN PCBEEP SPDIF EAPD NC_1 NC_2 NC_16 RCOSC
VDDIO DVDD DVDDM AVDD_20 AVDD_31 AVDDHP
VSSIO_42 VSSIO_46 DVSS AVSS_12 AVSS_25 AVSS_32 AVSSHP
MIC_BIAS_L MIC_BIAS_R MIC_L MIC_R LINEOUT_L LINEOUT_R PORT-A_BIAS_L PORT-A_BIAS_R PORT-A_L PORT-A_R PORT-B_BIAS_L PORT-B_BIAS_R PORT-B_L PORT-B_R CD_L CD_GND CD_R SENSE VREF_HI VREF_LO VC_REFA
ASIC HDA CX20549-12Z (HSD) LQFP 48PIN CONEXANT LR
R1221 2.2KΩ 5% 1/16W SMT0402 LR INMIC
C1313 1uF 6.3V ±10% 0603 X5R LR
C1310 1uF 6.3V ±10% 0603 X5R LR
AGND (40,42,43)
LINE_OUT_L (42)
LINE_OUT_R (42)
HP_OUT_L (42)
HP_OUT_R (42)
R1213 1KΩ 5% 1/16W SMT0402 LR
R1215 1KΩ 5% 1/16W SMT0402 LR
R1214 2.2KΩ 5% 1/16W SMT0402 LR MIC1
R1216 2.2KΩ 5% 1/16W SMT0402 LR MIC2
C1311 1uF 6.3V ±10% 0603 X5R LR
SENSE_A
C1314 1uF 10V +80-20% SMT0603 Y5V LMK107F105ZA-T TAIYO LR
C1315 C1316 10uF 10V ±10% SMT0805 X5R AVXTV21X5R106KAT AVX LR(NU)
(20mil)
AVDDS R1224 SPWR 0 5% 1/16W 060 3
AVDD_20549
C1317 1uF 10V 10% SMT0603 X5R C1608X5R1A 105K TDK LR
C1318 C1319 0.1uF 16V 80-20% SMT0402 Y5V LR
Please close to CODEC CHIP
R1248 5.11KΩ 1% 1/16W SMT0402 LR
R1245 10KΩ 1% 1/16W SMT0402 LR MIC1_JD (43)
SENSE_A R1225 20KΩ 1% 1/16W SMT0402 LR
R1227 5.11KΩ 1% 1/16W SMT0402 LR HP_JD (43)
R1244 39.2KΩ 1% 1/10W SMT0402 LR
V0.4 Modify
R1370 0Ω 5% 1/8W SMT0805 LR
L136 SPWR 0 5% 1/16W 060 3
(11,21,23,24,25,26,27,29,30,33,34,36,37,39,42,45 ,48) 3VDDA
3VDDM_AUDIO
4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR
C1320 C1321 C1322 0.1uF 16V 80-20% SMT0402 Y5V LR
U73 LNR-IC G9131-33T73Uf LDO 3.3V SOT-23 3PIN GMT LR
VIN VOUT GND
(40mil)
(11,22,24,26,29,32,34,35,36,37,42,46,48, 52) 5VDDM
C1324 0.1uF 16V 80-20% SMT0402 Y5V L R
C1325 1000pF 50V 10% SMT0402 X7R LR
C1323 10uF 10V ±10% SMT0805 X5R A VXTV21X5R106K10AT AVX LR

AC97 CODEC Power Consumption:
Power Dissipation: TYP 330mW
Icc: TYP 40mA (Digital)
Icc(stdby): TYP 0mA (Digital)
Icc: TYP 40mA (Analog)
Icc(stdby): TYP 0.13mA (Analog)

HDA CODEC Layout Guide:

1. The digital and analog gnd should be separated 2-3mm gap
2. All the analog trace routing should be over the analog plane
3. The analog and digital planes s hould electrically shorted at one place
4. All supply high frequency decoupling ,reference high frequency decoulp and filter caps must be routed on the same layer as the codec
5. Analog I/O routing should be kept a short as possible
6. Analog I/O routing should be shielding with analog ground traces
7. Use of ground plane fill and the copper fill should be shorted to the analog ground plane
8. The AC-link signal should be as short as possible
9. AC-link clock signal should have a se ries resistor close to the codec
10. The AC-link signal should be shielding with ground
11. Split analog and digital ground planes and 2-3mm
12. Analog signals only over analog ground plane
13. Digital signals only over digital ground plane
14. Locate analog section away from high speed digital circuits
15. Place smallest bypass capacitor c losest to IC pin
16. Use metal film resistors and NPO capacitors in analog path
17. The Audio signals trace wid th is 12mil or more

A_GND	10mil
A_LINE_OUT_L	10mil
A_GND	10mil
A_LINE_OUT_R	10mil
A_GND	10mil

A_CD_GND	10mil
A_CD_L	10mil
A_CD_GND	10mil
A_CD_R	10mil
A_CD_GND	10mil

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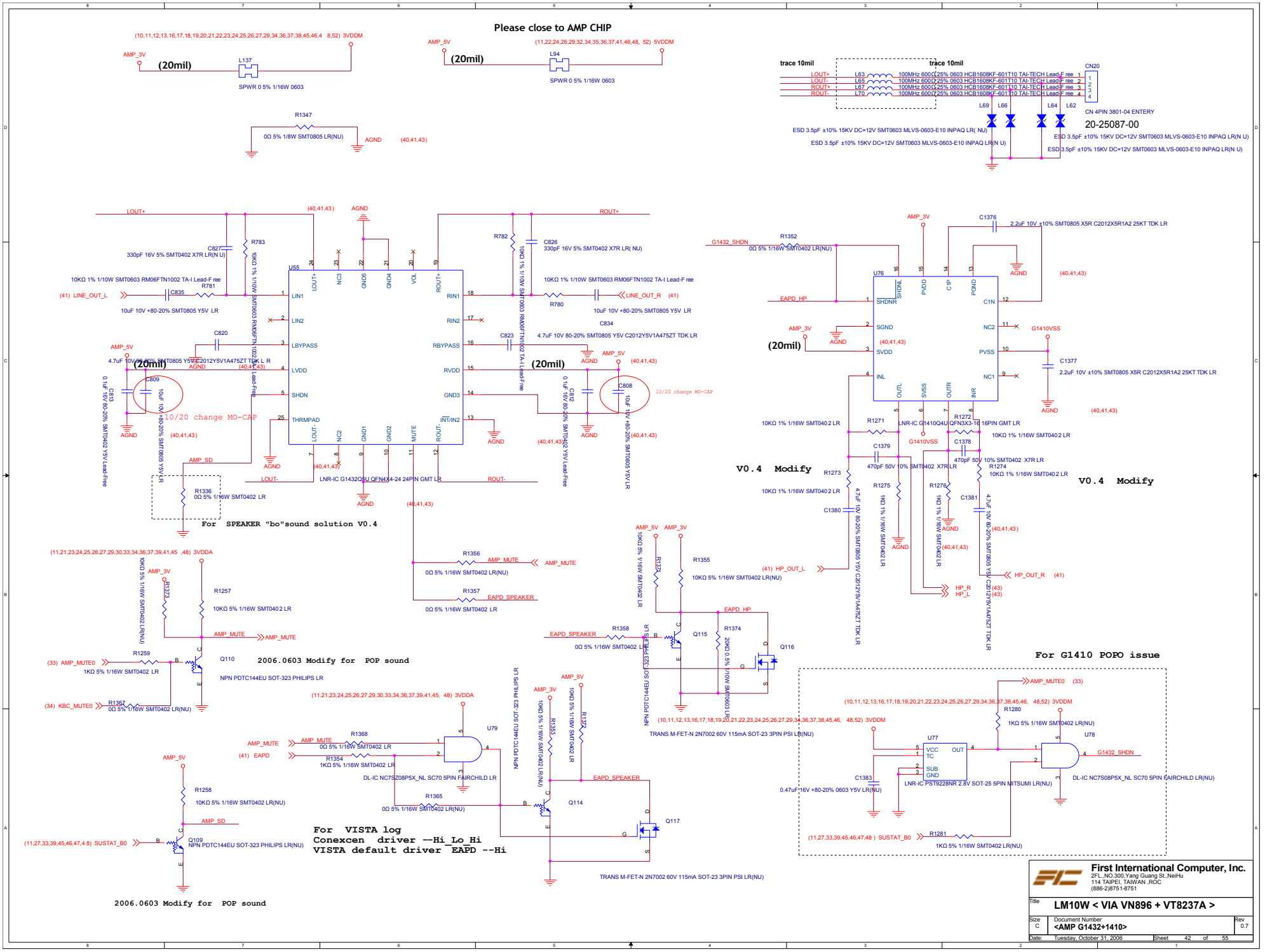
Title: LM10W < VIA VN896 + VT8237A >

Size: C | Document Number: <CX20549 codec> | Rev: 0.7


Please close to AMP CHIP
(10,11,12,13,16,17,18,19,20,21,22,23,24,25,26,27,29,34,36,37,38,45,46,4 8,52) 3VDDM
AMP_3V
(20mil)
L137
SPWR 0 5% 1/16W 0603
AMP_5V
(11,22,24,26,29,32,34,35,36,37,41,46,48, 52) 5VDDM
(20mil)
L94
SPWR 0 5% 1/16W 0603
R1347
0Ω 5% 1/8W SMT0805 LR(NU)
AGND
(40,41,43)
trace 10mil
trace 10mil
LOUT+
LOUT-
ROUT+
ROUT-
L63
L65
L67
L70
100MHz 600Ω 25% 0603 HCB1608KF-601T10 TAI-TECH Lead-F ree
CN20
CN 4PIN 3801-04 ENTERY
20-25087-00
L69
L66
L64
L62
ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR(NU)
ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR(N U)
LOUT+
C827
330pF 16V 5% SMT0402 X7R LR(N U)
R783
10KΩ 1% 1/10W SMT0603 RM06FTN1002 TA-I Lead-F ree
10KΩ 1% 1/10W SMT0603 RM06FTN1002 TA-I Lead-F ree
R781
(41) LINE_OUT_L
C835
10uF 10V +80-20% SMT0805 Y5V LR
U55
LIN1
LIN2
LBYPASS
LVDD
SHDN
THRMPAD
LOUT+
NC3
GND5
GND4
VOL
ROUT+
RIN1
RIN2
RBYPASS
RVDD
GND3
INT/IN2
LOUT-
NC2
GND1
GND2
MUTE
ROUT-
LNR-IC G1432GSU QFN4X4-24 24PIN GMT LR
C820
4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK L R
C809
10uF 10V +80-20% SMT0805 Y5V LR
C813
0.1uF 16V 80-20% SMT0402 Y5V Lead-Free
10/20 change MO-CAP
AMP_SD
R1336
0Ω 5% 1/16W SMT0402 LR
For SPEAKER "bo"sound solution V0.4
R782
C826
330pF 16V 5% SMT0402 X7R LR(NU)
10KΩ 1% 1/10W SMT0603 RM06FTN1002 TA-I Lead-F ree
R780
LINE_OUT_R (41)
10uF 10V +80-20% SMT0805 Y5V LR
C834
4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR
C823
C808
10uF 10V +80-20% SMT0805 Y5V LR
C812
0.1uF 16V 80-20% SMT0402 Y5V Lead-Free
10/20 change MO-CAP
R1356
AMP_MUTE
0Ω 5% 1/16W SMT0402 LR(NU)
R1357
EAPD_SPEAKER
0Ω 5% 1/16W SMT0402 LR
G1432_SHDN
R1352
0Ω 5% 1/16W SMT0402 LR(NU)
U76
SHDNR
SGND
SVDD
INL
SHDNL
PVDD
C1P
PGND
C1N
NC2
PVSS
NC1
OUTL
SVSS
OUTR
INR
EAPD_HP
G1410VSS
C1376
2.2uF 10V ±10% SMT0805 X5R C2012X5R1A2 25KT TDK LR
C1377
2.2uF 10V ±10% SMT0805 X5R C2012X5R1A2 25KT TDK LR
R1271
R1272
LNR-IC G1410Q4U QFN3X3-16 16PIN GMT LR
C1379
470pF 50V 10% SMT0402 X7R LR
C1378
470pF 50V 10% SMT0402 X7R LR
R1273
R1274
R1275
R1276
C1380
C1381
4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR
(41) HP_OUT_L
HP_OUT_R (41)
HP_R (43)
HP_L (43)
V0.4 Modify
V0.4 Modify
For G1410 POPO issue
(11,21,23,24,25,26,27,29,30,33,34,36,37,39,41,45 ,48) 3VDDA
R1373
R1257
10KΩ 5% 1/16W SMT0402 LR
AMP_MUTE
R1259
(33) AMP_MUTE0
1KΩ 5% 1/16W SMT0402 LR
Q110
NPN PDTC144EU SOT-323 PHILIPS LR
R1367
(34) KBC_MUTE0
0Ω 5% 1/16W SMT0402 LR(NU)
2006.0603 Modify for POP sound
R1372
R1355
10KΩ 5% 1/16W SMT0402 LR(NU)
EAPD_HP
R1358
0Ω 5% 1/16W SMT0402 LR
Q115
2N7002 60V 115mA SOT-323 PHILIPS LR
R1374
20KΩ 0.5% 1/10W SMT0603 LR
Q116
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU)
(10,11,12,13,16,17,18,19,20,21,22,23,24,25,26,27,29,34,36,37,38,45,46, 48,52) 3VDDM
R1280
1KΩ 5% 1/16W SMT0402 LR(NU)
U77
VCC
TC
OUT
SUB
GND
LNR-IC PST9228NR 2.8V SOT-25 5PIN MITSUMI LR(NU)
C1383
0.47uF 16V +80-20% 0603 Y5V LR(NU)
U78
G1432_SHDN
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR(NU)
(11,27,33,39,45,46,47,48) SUSTAT_B0
R1281
1KΩ 5% 1/16W SMT0402 LR(NU)
(11,21,23,24,25,26,27,29,30,33,34,36,37,39,41,45, 48) 3VDDA
U79
AMP_MUTE
R1368
0Ω 5% 1/16W SMT0402 LR
(41) EAPD
R1354
1KΩ 5% 1/16W SMT0402 LR
DL-IC NC7SZ08P5X_NL SC70 5PIN FAIRCHILD LR
R1365
0Ω 5% 1/16W SMT0402 LR(NU)
R1353
10KΩ 5% 1/16W SMT0402 LR(NU)
R1371
10KΩ 5% 1/16W SMT0402 LR
EAPD_SPEAKER
Q114
Q117
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR(NU)
R1258
10KΩ 5% 1/16W SMT0402 LR(NU)
AMP_SD
(11,27,33,39,45,46,47,4 8) SUSTAT_B0
Q109
NPN PDTC144EU SOT-323 PHILIPS LR(NU)
For VISTA log
Conexcen driver --Hi_Lo_Hi
VISTA default driver EAPD --Hi
2006.0603 Modify for POP sound
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(886-2)8751-8751
Title
LM10W < VIA VN896 + VT8237A >
Size C
Document Number
<AMP G1432+1410>
Rev 0.7
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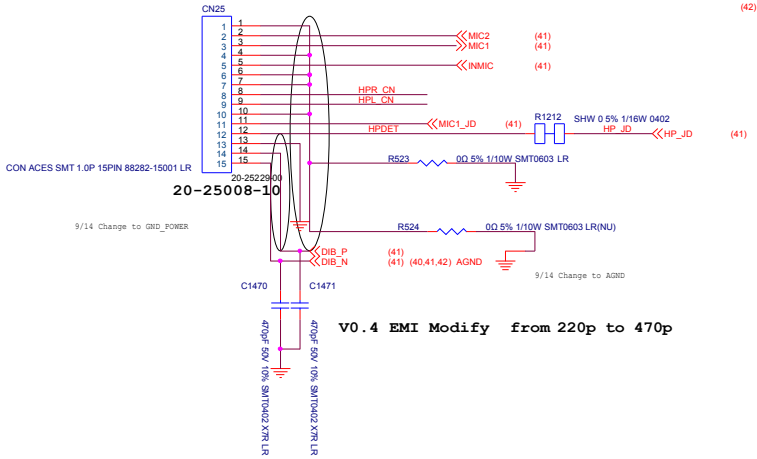

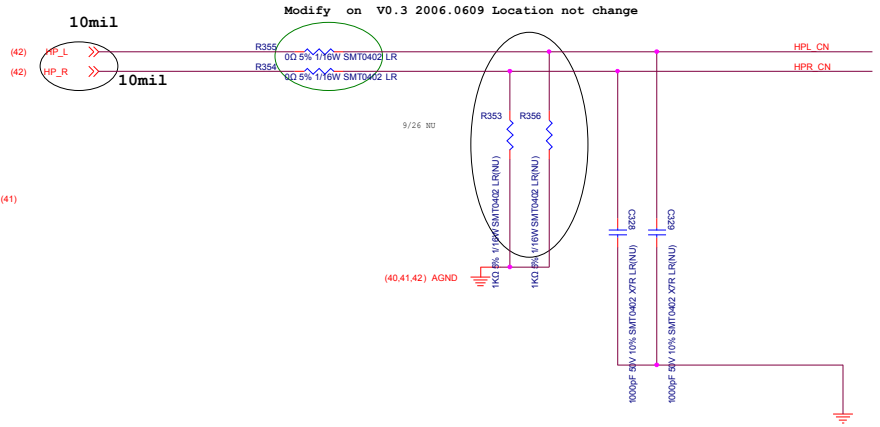

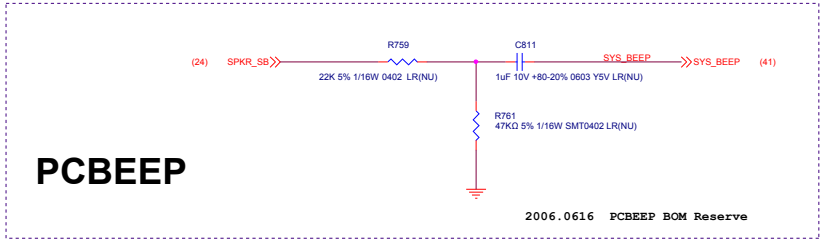

(11,22,24,26,29,32,34,35,36,37,41,42,46,48, 52) 5VDDM

5VDDM

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Title: LM10W < VIA VN896 + VT8237A >		
Size: C	Document Number: <SPDIF / HP OUT / Audio CN>	Rev: 0.7
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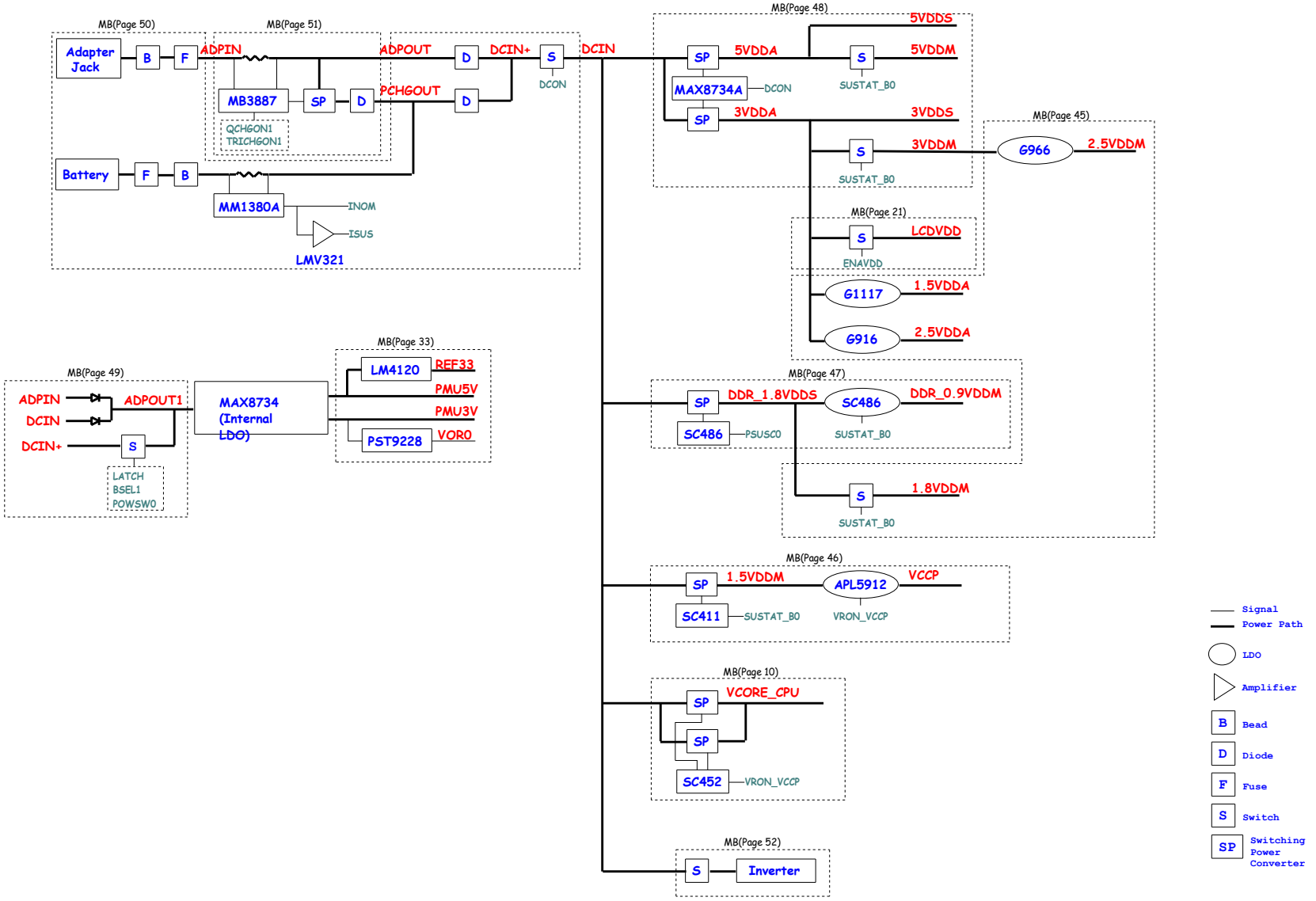
LM10W Power Block



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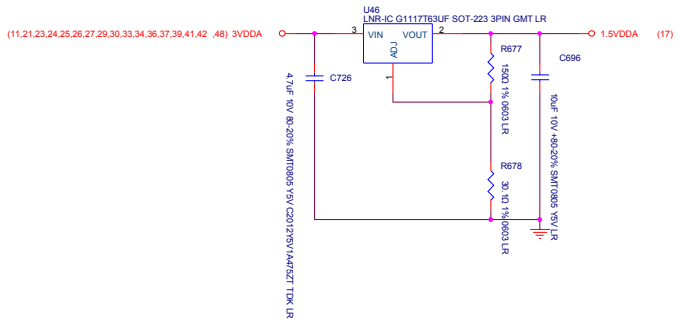
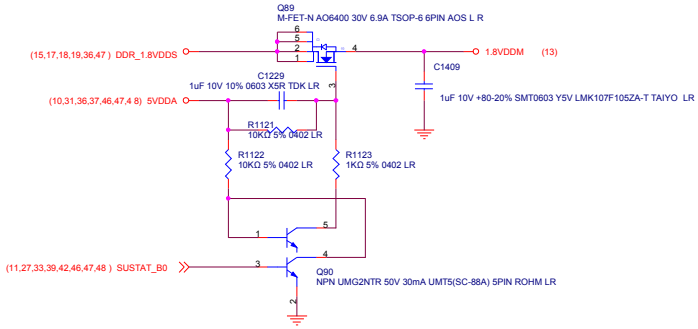
Title	LM10W < VIA VN896 + VT8237A >	
Size: C	Document Number: <DDR2 POWER>	Rev: 0.7
Date: Tuesday, October 31, 2006	Sheet 44 of 55	

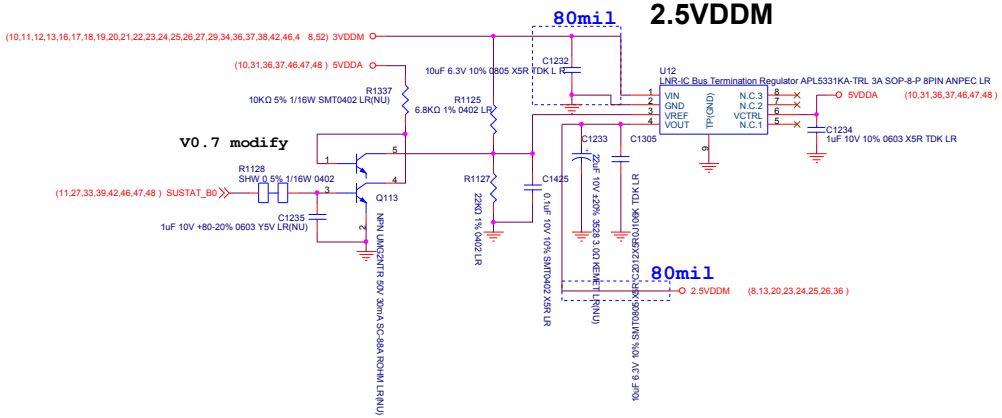
1.5VDDA 0.5A



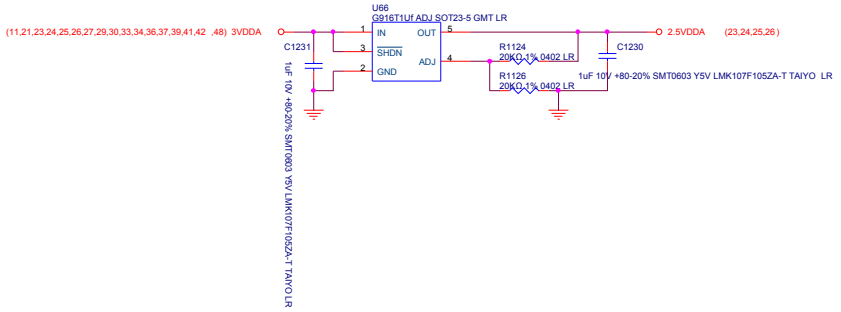
1.8VDDM 1.5A



2.5VDDM



2.5VDDA 0.5A



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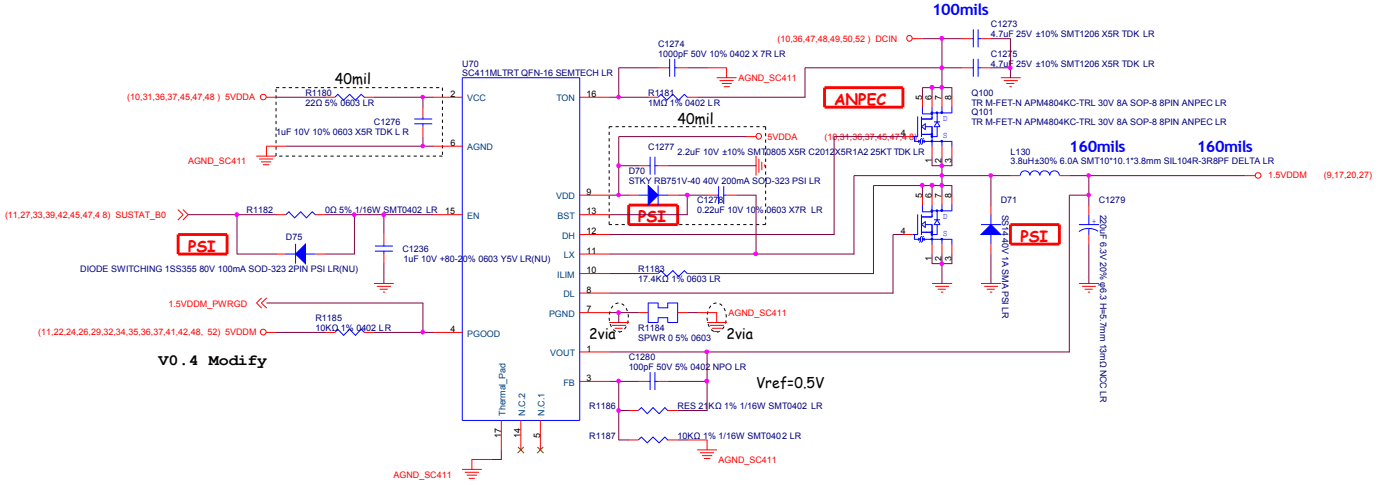
Title: **LM10W < VIA VN896 + VT8237A >**

Size	Document Number	Rev
C	<1.5V / 2.5V /1.8V>	0.7

Date: Tuesday, October 31, 2006 Sheet 45 of 55

1.5VDDM



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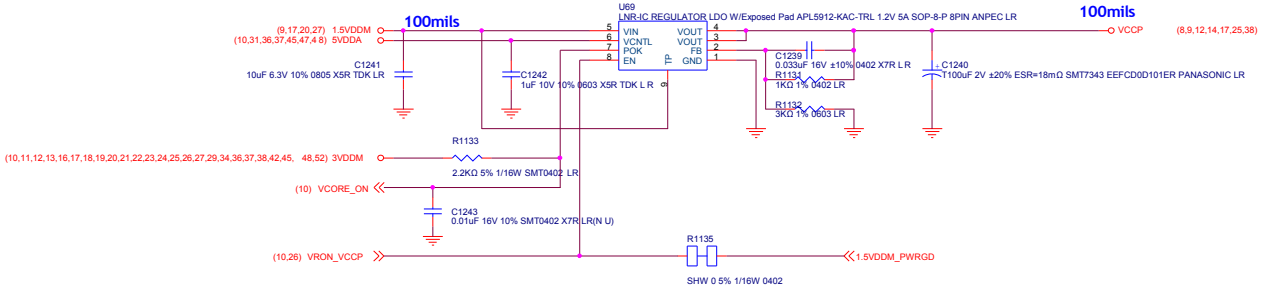

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Size C	Document Number <POWER 3/5 VDDS/VDDM>	Rev 0.7
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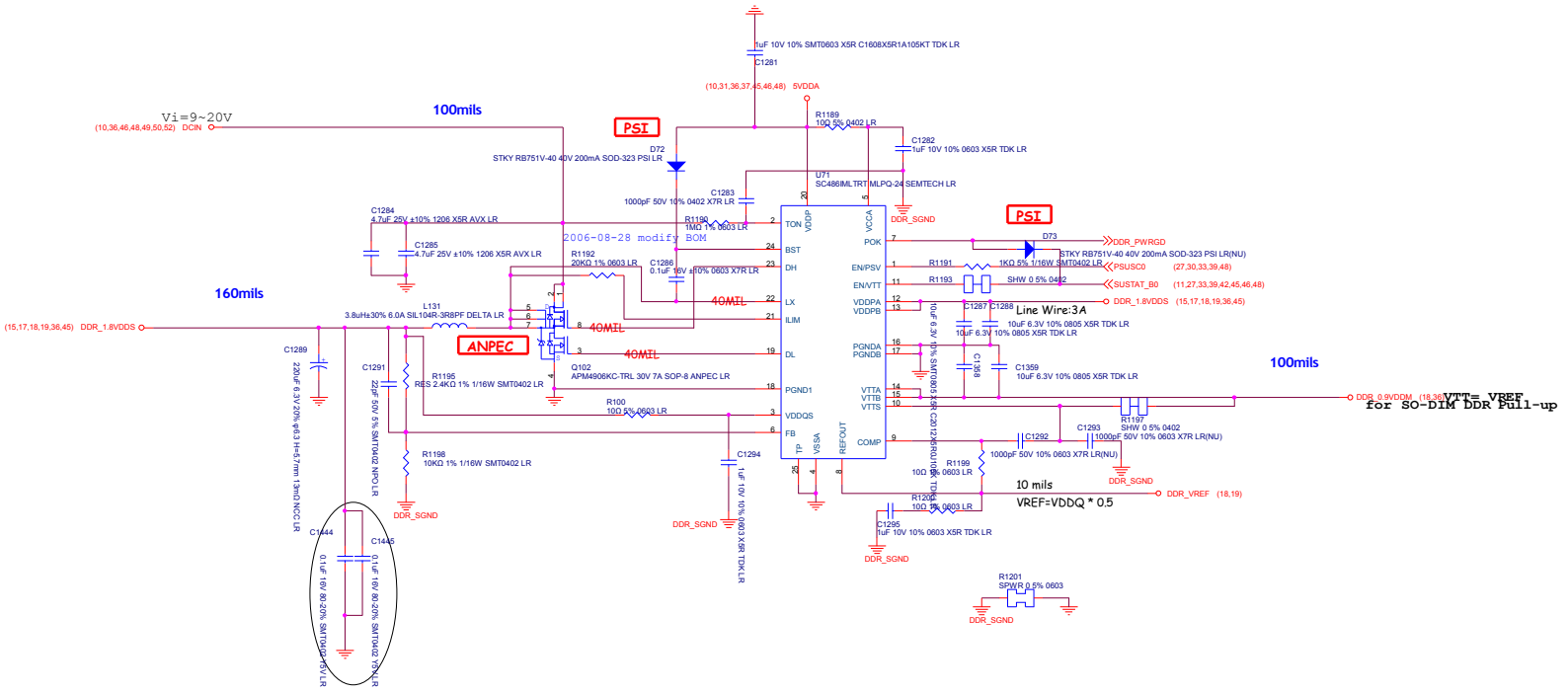

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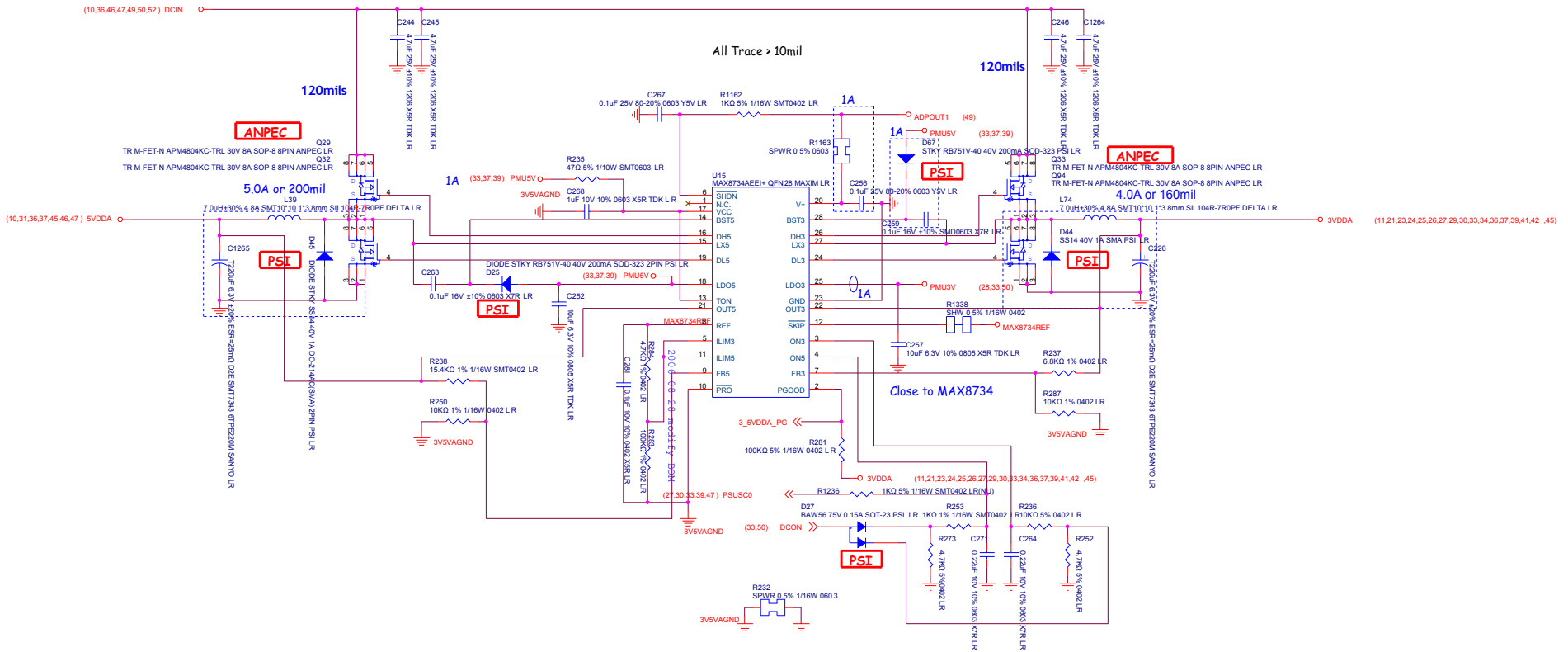
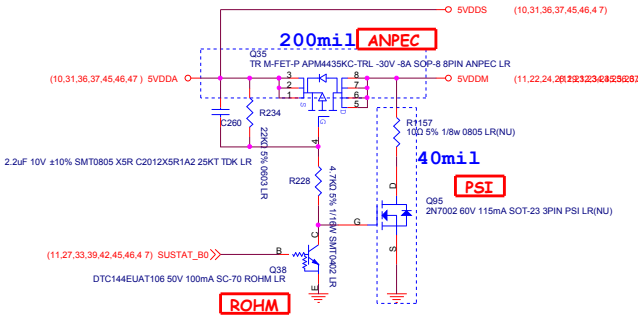
5VDDA/S/M, 3VDDA/S/M



5VDDS/5VDDM



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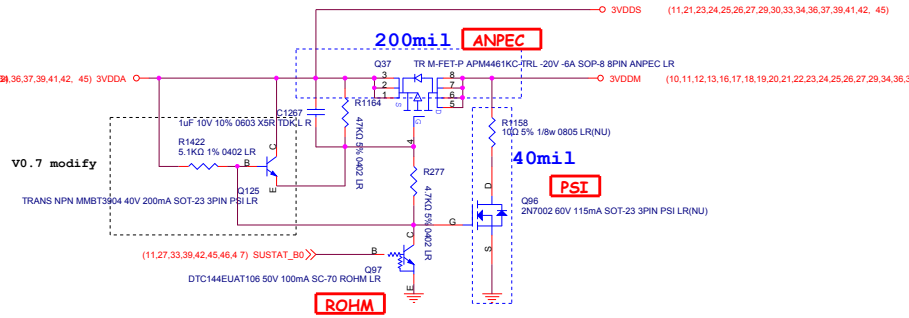

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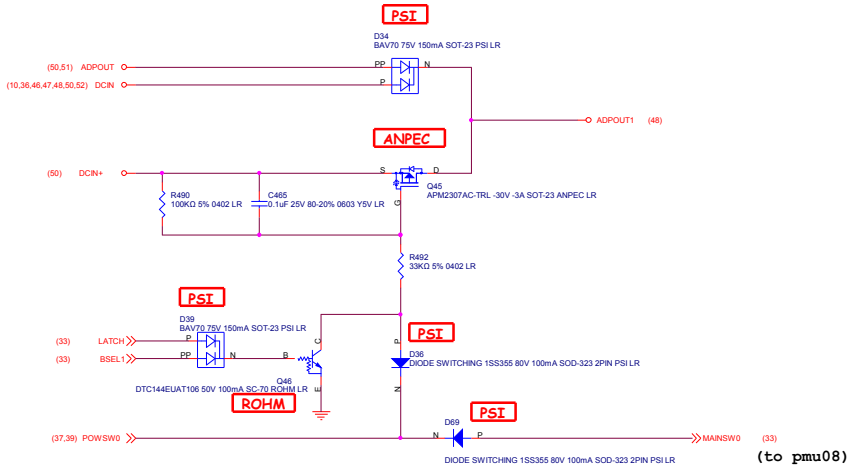

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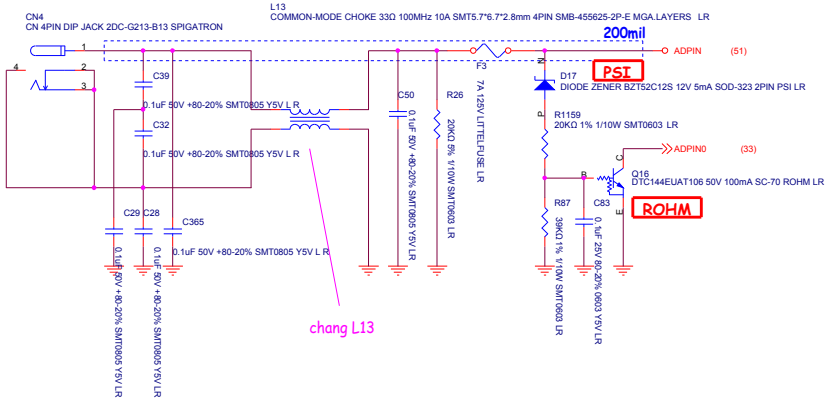
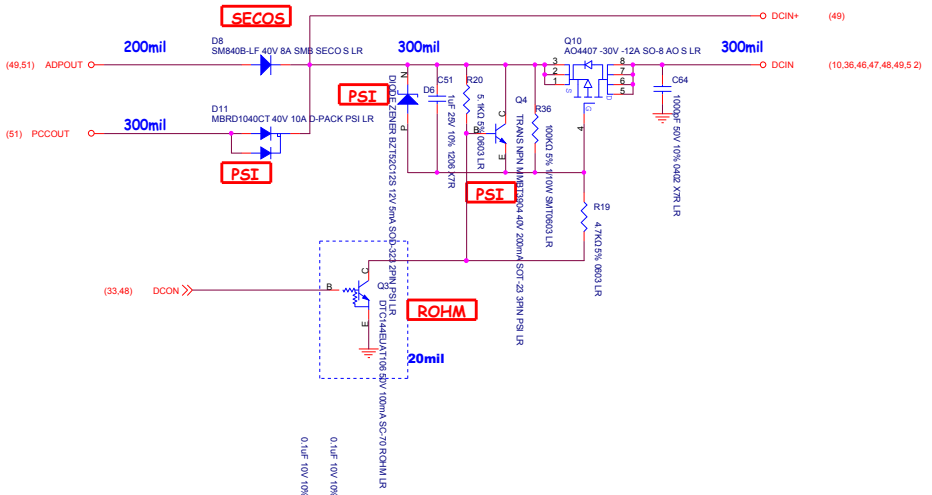
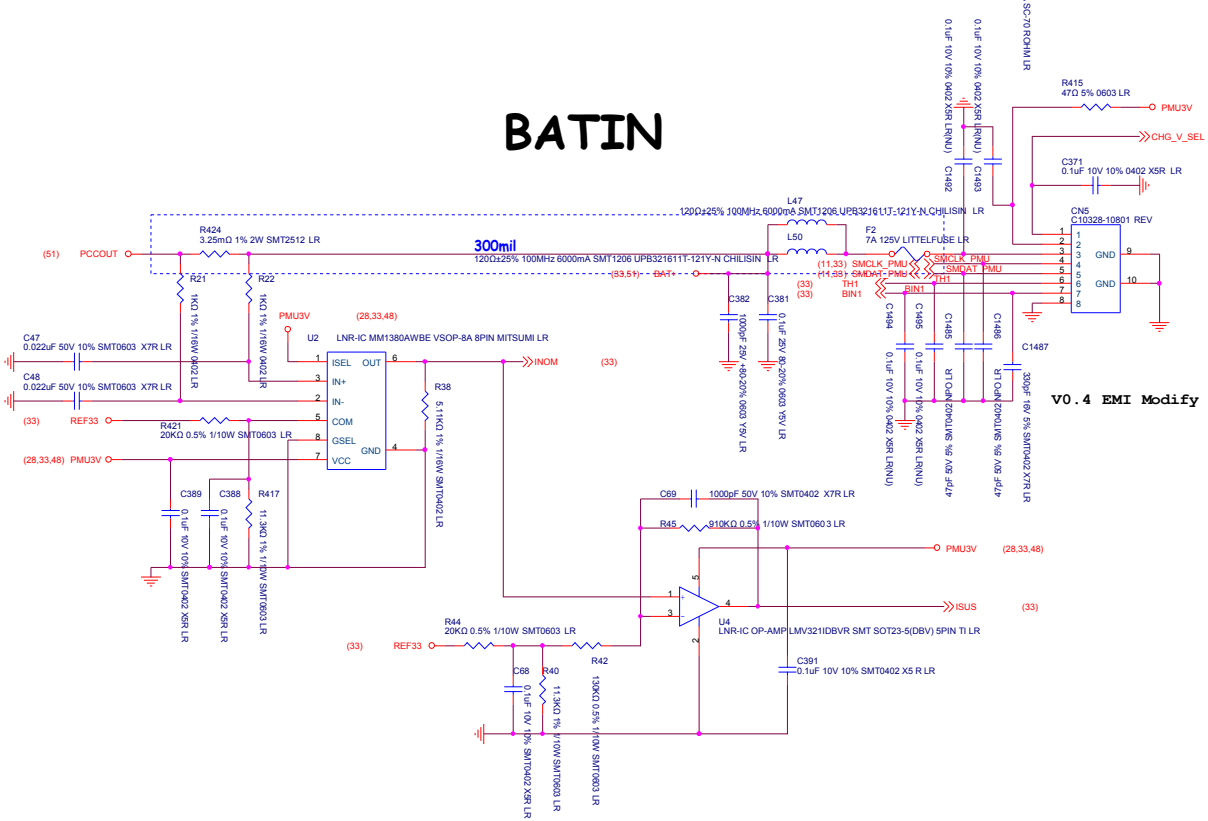
ADPIN



DCIN



BATIN



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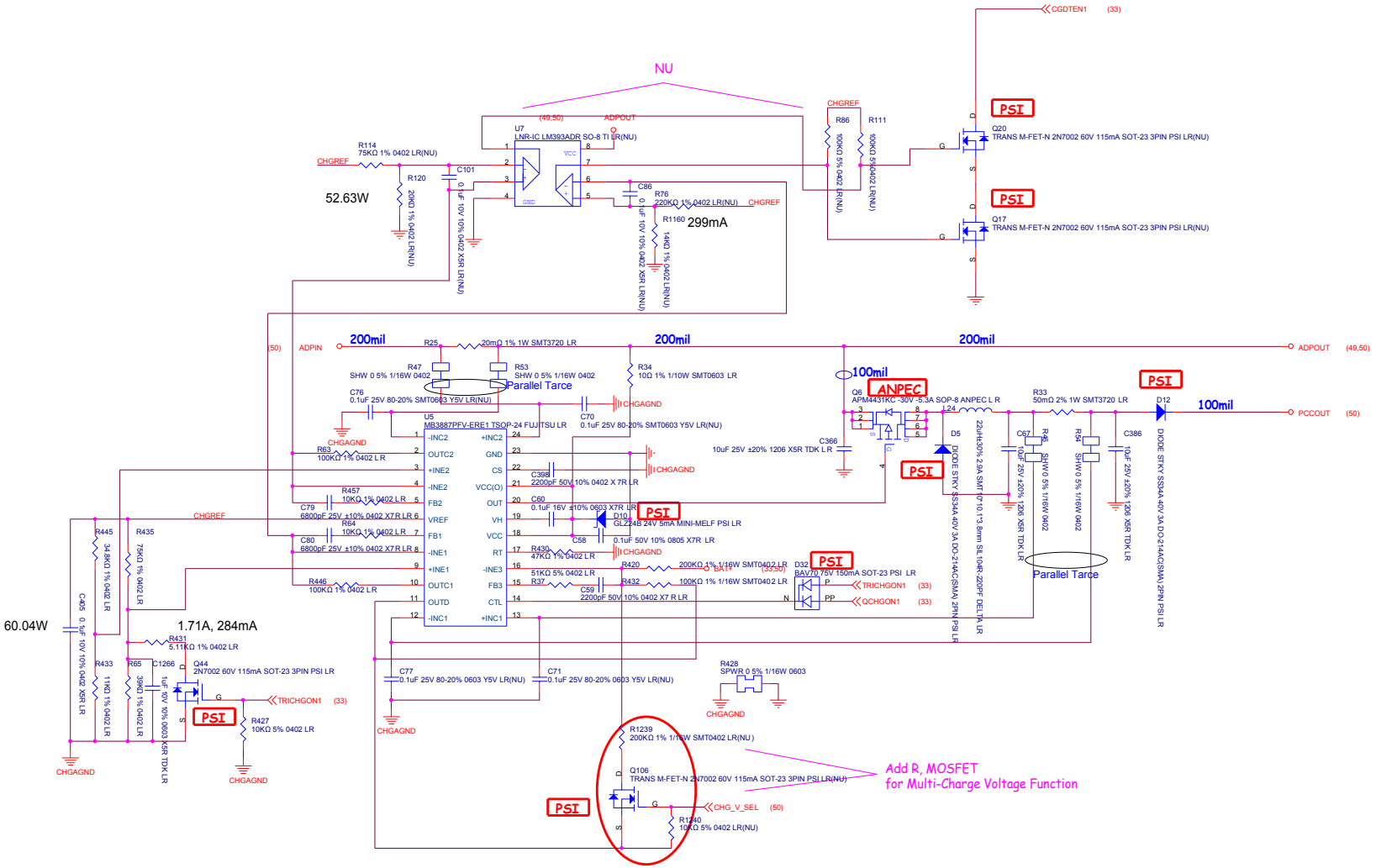
Charger



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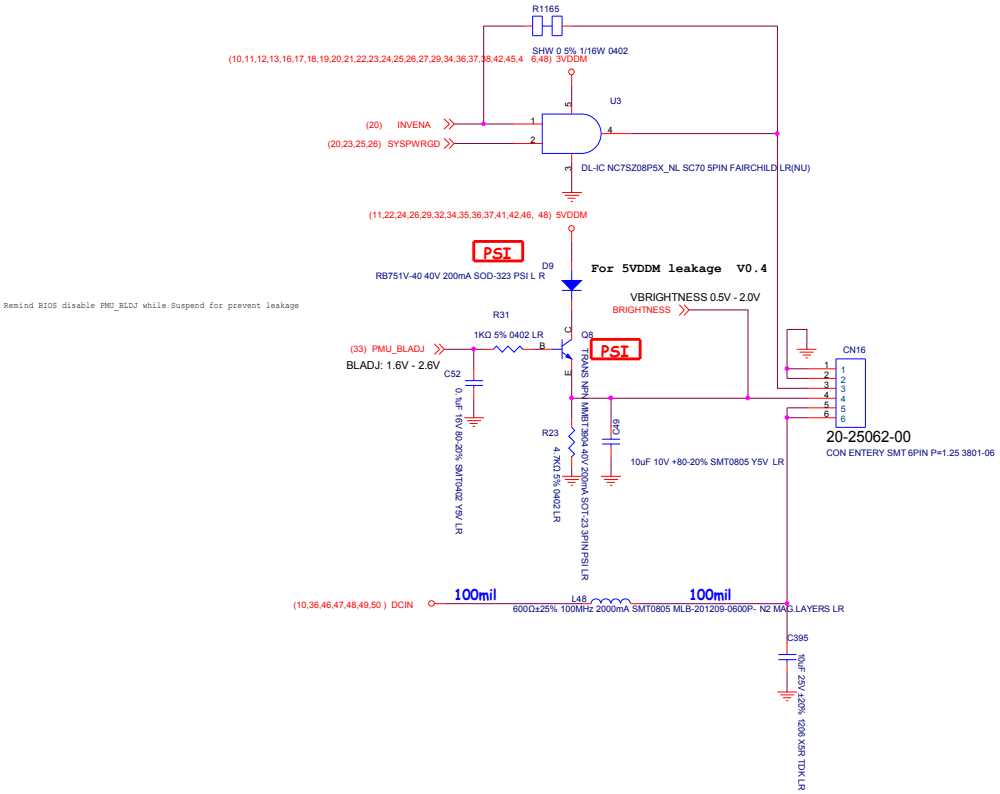
Inverter Connector



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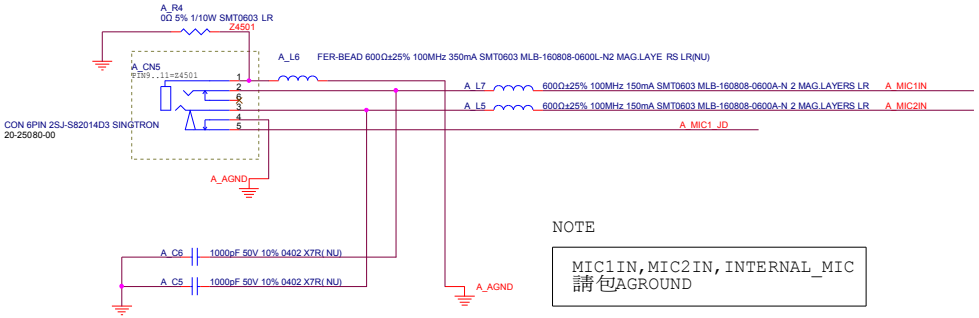
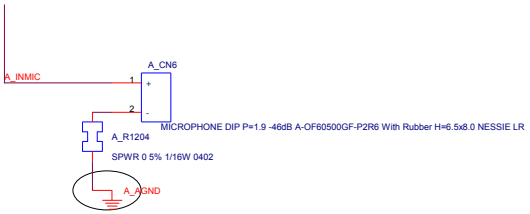
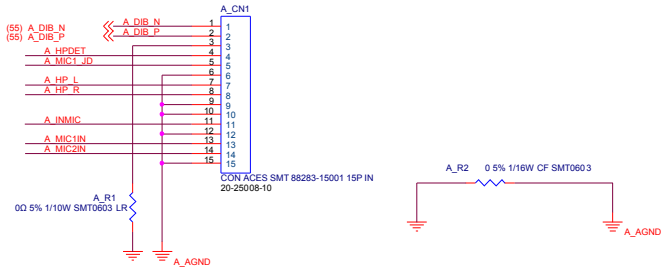


NOTE

MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND

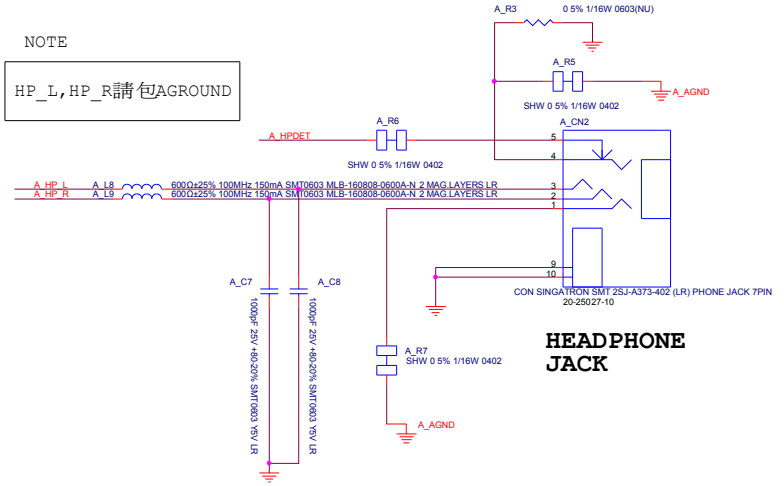
9/16 Cancel USB CON



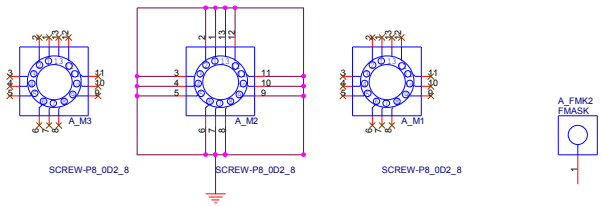


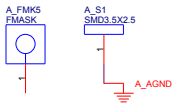
NOTE

HP_L,HP_R請包AGROUND



HEADPHONE JACK





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Title: **LM10W < VIA VN896 + VT8237A >**

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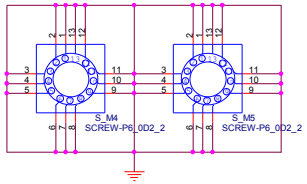

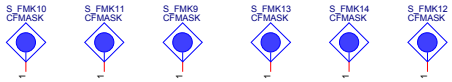

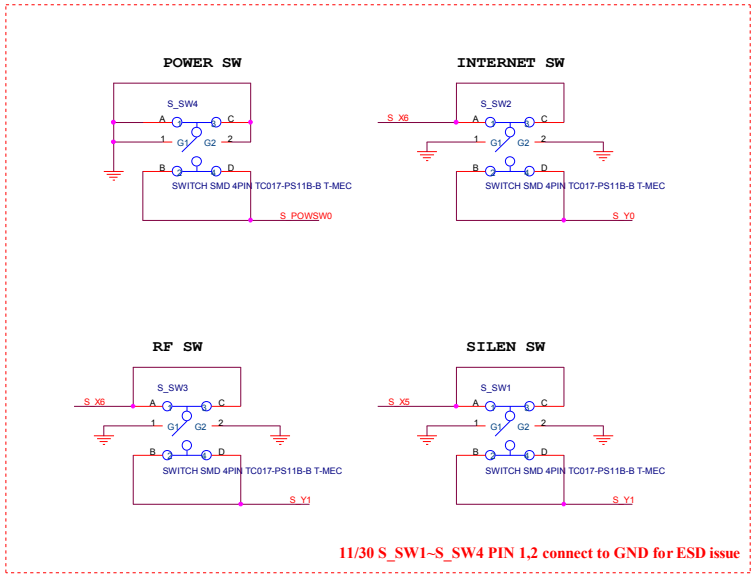

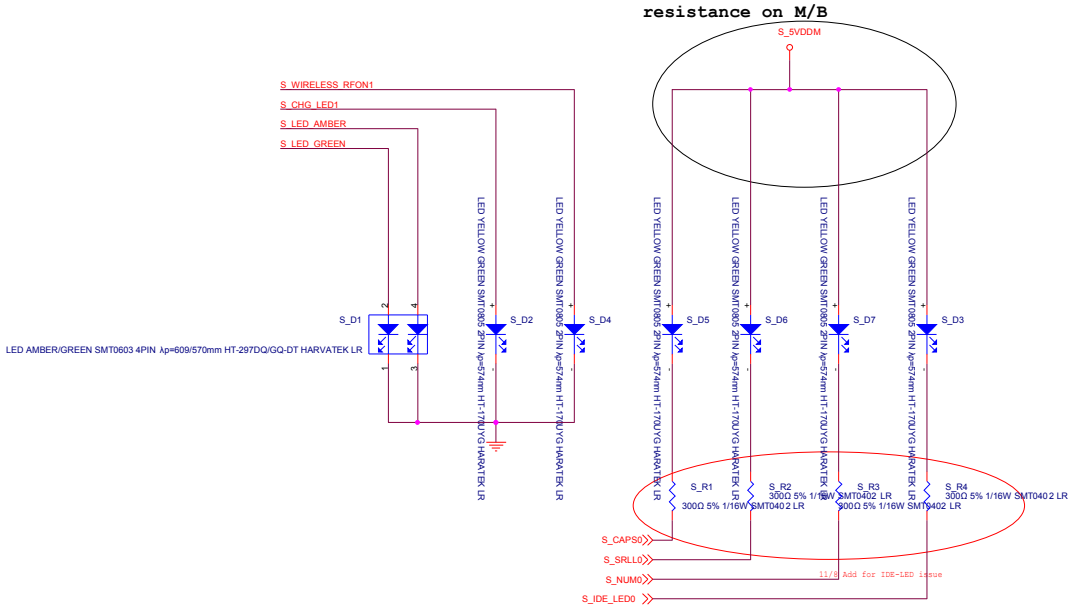

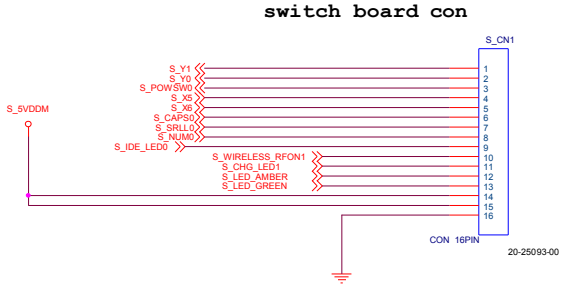

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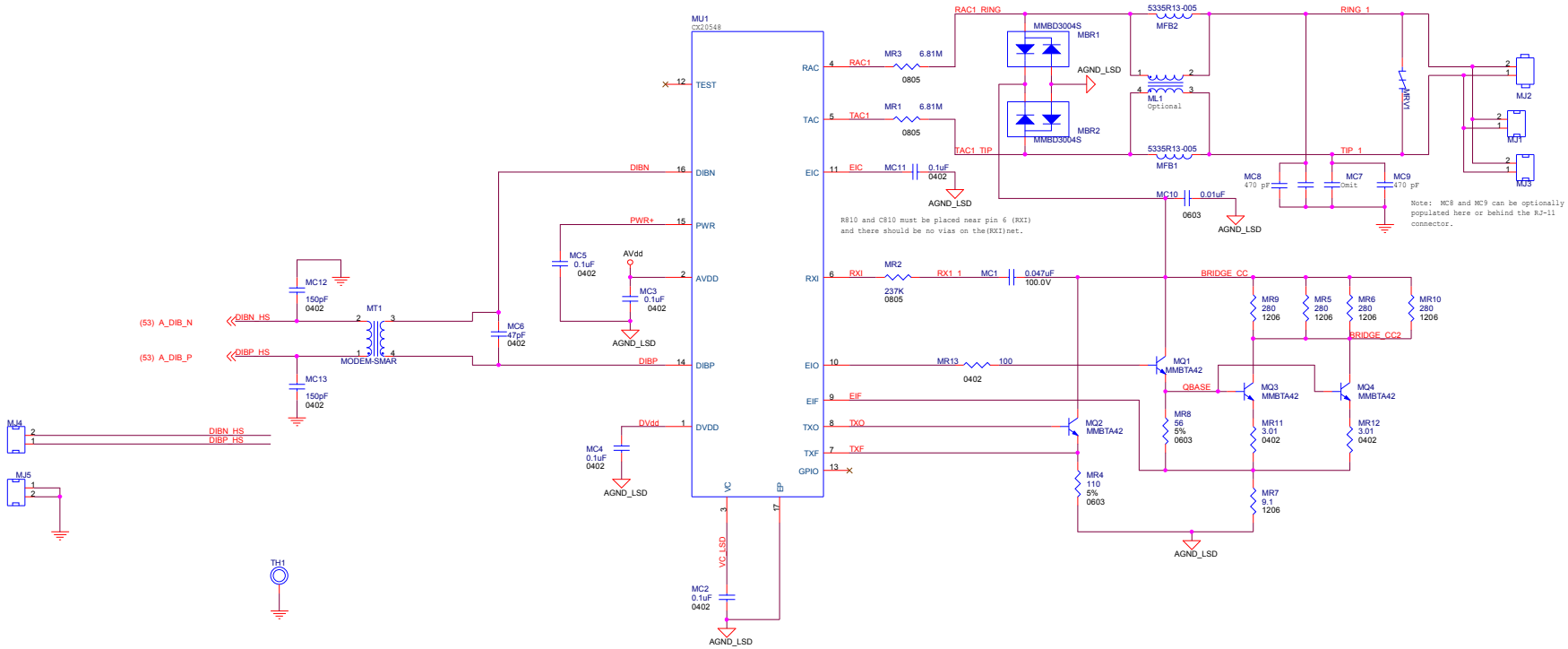

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