First International Computer,Inc

Protable Computer Group HW Department

Board name : Mother Board Schematic

Project : LM7R

Version : 0.1

Initial Date : March 1 , 2005

1. Schematic Page Description :
2. PCI & IRQ & DMA Description :
3. Block Diagram :
4. Nat name Description :
5. Board Stack up Description :
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8. Layout Guideline :
9. switch setting

Manager Sign by:

Drawing by : AHARRY_HUANG

Total confirm by: CC_TSAO

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Audio Circuit check by:

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Title: LM7R < VIA VN800 + VT8237R>

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1. Schematic Page Description :

LM7 Schematic Ver : 0.1

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI(Wireless LAN)
AD23	CardBus

PCIINT	CHIP
IRQA	MiniPCI/NB
IRQB	MiniPCI/CardBus
IRQC	MiniPCI
IRQD	

BUSMASTER

REQ	CHIP
REQ0 / GNT0	MiniPCI
REQ1 / GNT1	CardBus
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Desciption	
IRQ0	System timer	
IRQ1	Keyboard	
IRQ2	(Casacde)	
IRQ3	LAN / MODEM	
IRQ4	~~Serial Port~~	
IRQ5	AUDIO / VGA / USB	
IRQ6	~~FLOPPY DISK~~	
IRQ7	~~LPT~~	
IRQ8	RTC	
IRQ9	ACPI	
IRQ10	FIR (Disable by default)	(MODEM/LAN)
IRQ11	Cardbus	
IRQ12	PS/2 mouse	
IRQ13	FPU	
IRQ14	HDD	
IRQ15	CDROM	

DMA Channel	Device	
DMA0	FIR (disable by default)	(MODEM / LAN)
DMA1	~~ECP~~	
DMA2	~~FLOPPY DISK~~	
DMA3	AUDIO	
DMA4	(Cascade)	
DMA5	Unused	
DMA6	Unused	
DMA7	Unused	

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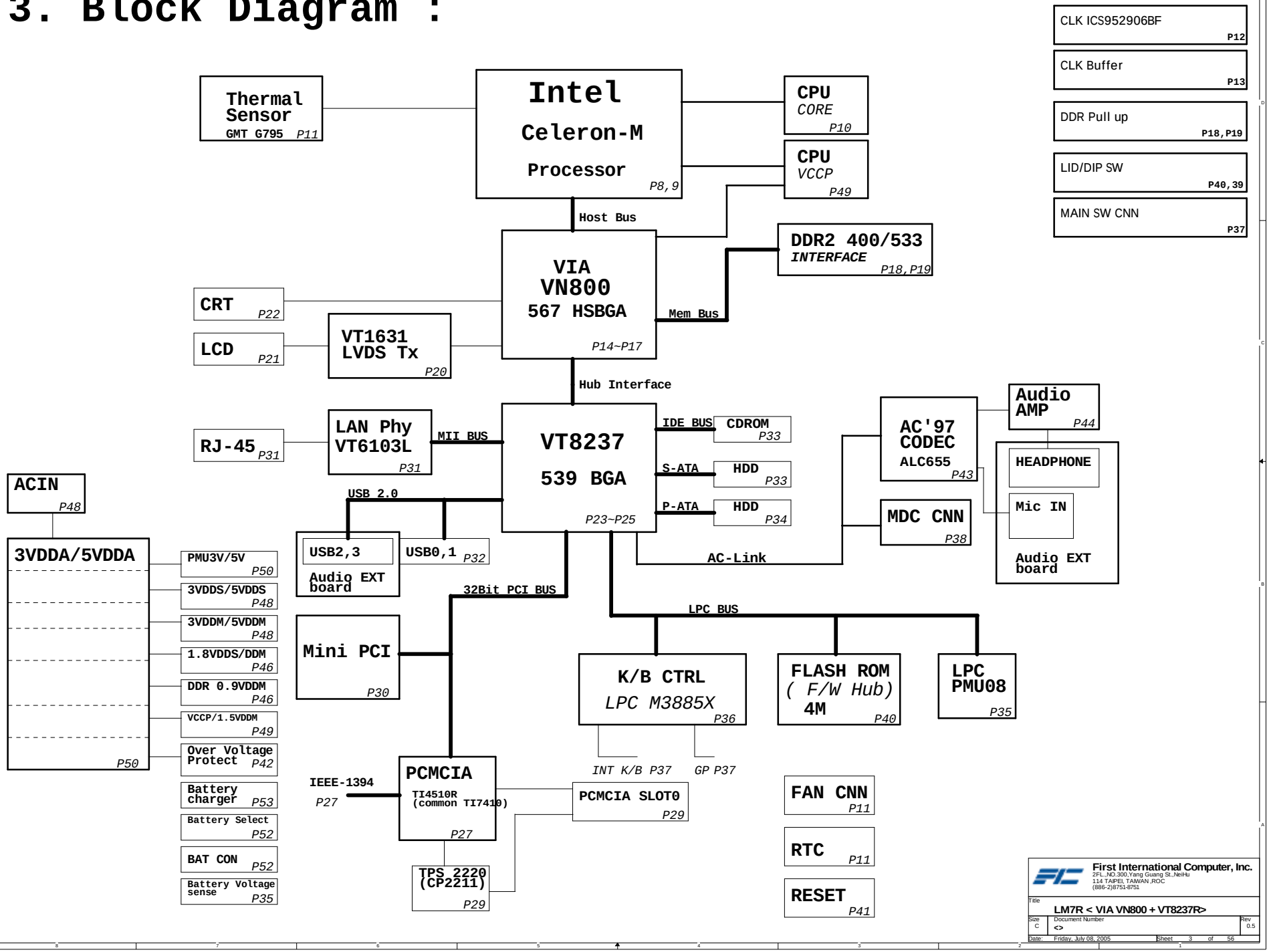
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
3VDDS	3.3V power rail
5VDDS	5.0V power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
Vcore_CPU	Core Voltage for CPU
VCCP	1.05V for AGTL+ Termination Voltage
1.8VDDM	1.8V for CPU PLL Voltage
DDR_0.9VDDM	0.9V DDR Termination Voltage
1.5VDDM	1.5V switched power rail
1.5VDDS	1.5V power rail
1.5VDDA	1.5V always on power rail
2.5VDDS	2.5V power rail for DDR

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Stripline Layer(AGTL,CLOCK,DDR)
Layer 4		Stripline Layer(Analog,LVDS,other)
Layer 5		Ground Plane
Layer 6		Solder Side,Microstrip signal Layer

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6.Schematic modify Item and History :

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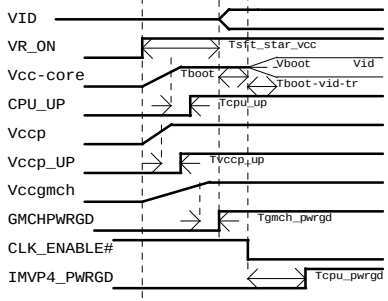
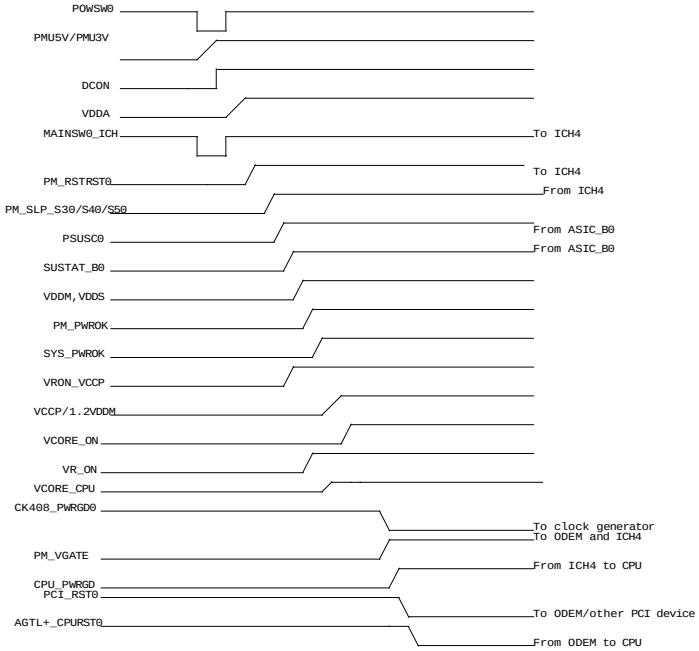
7. power on & off & S3 Sequence :

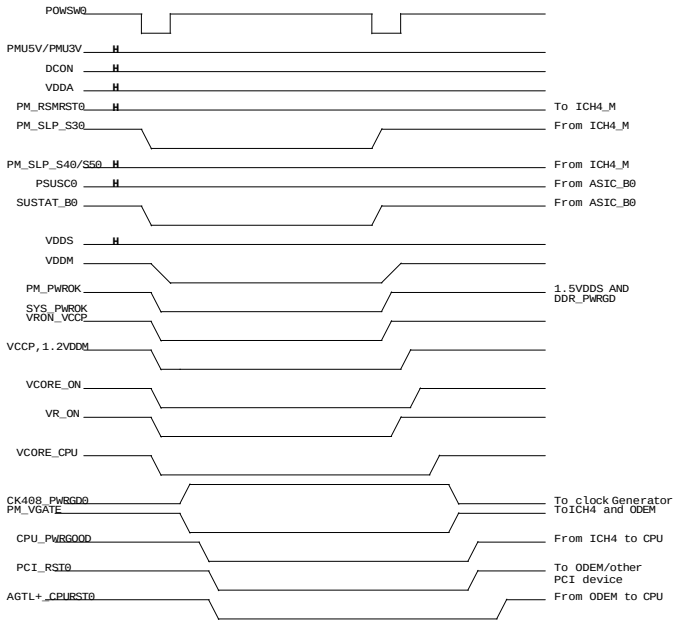
Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



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8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

DDR Signal Groups

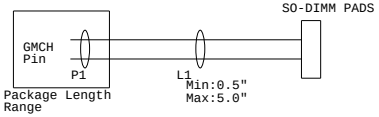
Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS#[3:0]
Command	SMA[12,6,3:0] SBA[1:0] SRAS# SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

Length Matching Formulas

Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

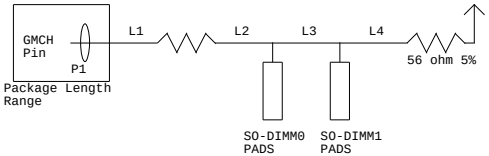
CLOCKS	LENGTH	TRACE / SPACE	NOTES
HCLKCPU[1..0] HCLKNB[1..0] HCLKITP[1..0]	2" ~ 8"	5 / 20 mils (5 mil space between + & -)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 450 mil
66MCLK_ICH 66MCLK_GMCH AGPCLK_ATI	4.5" ~ 9.0 " MAX : 8.5"	5 / 20 mils	* 66MCLK_ICH & AGPCLK_GMCH AGPCLK_ATI Length mismatch within 100 mils
PCLKICH PCLKCB PCLK1394 PCLKUSB20 PCLKOP PCLKFWH PCLKSIO PCLKLAN	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2.Max skew = 1ns
14MCLK_SIO 14MCLK_ICH 14MCLK_AC97	4.5"~9.0"	5 / 10 mils	
48MCLK_ICH 48MCLK_CB	3.5" ~ 12.5"	5 / 20 mils	

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerenve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

Data Signals Topologies and Routing Guidelines



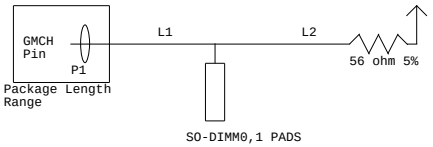
Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0 "

Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 0.5"
SDQ/SDM to SDQS : +/- 25 mils

SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

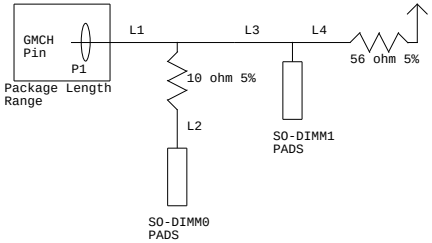
Control Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"

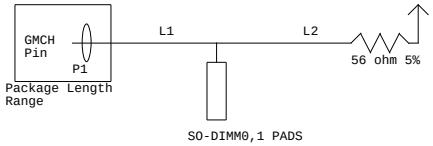
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

Command Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.0"
L3 : Max 2.0"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"

CPC Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"

Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

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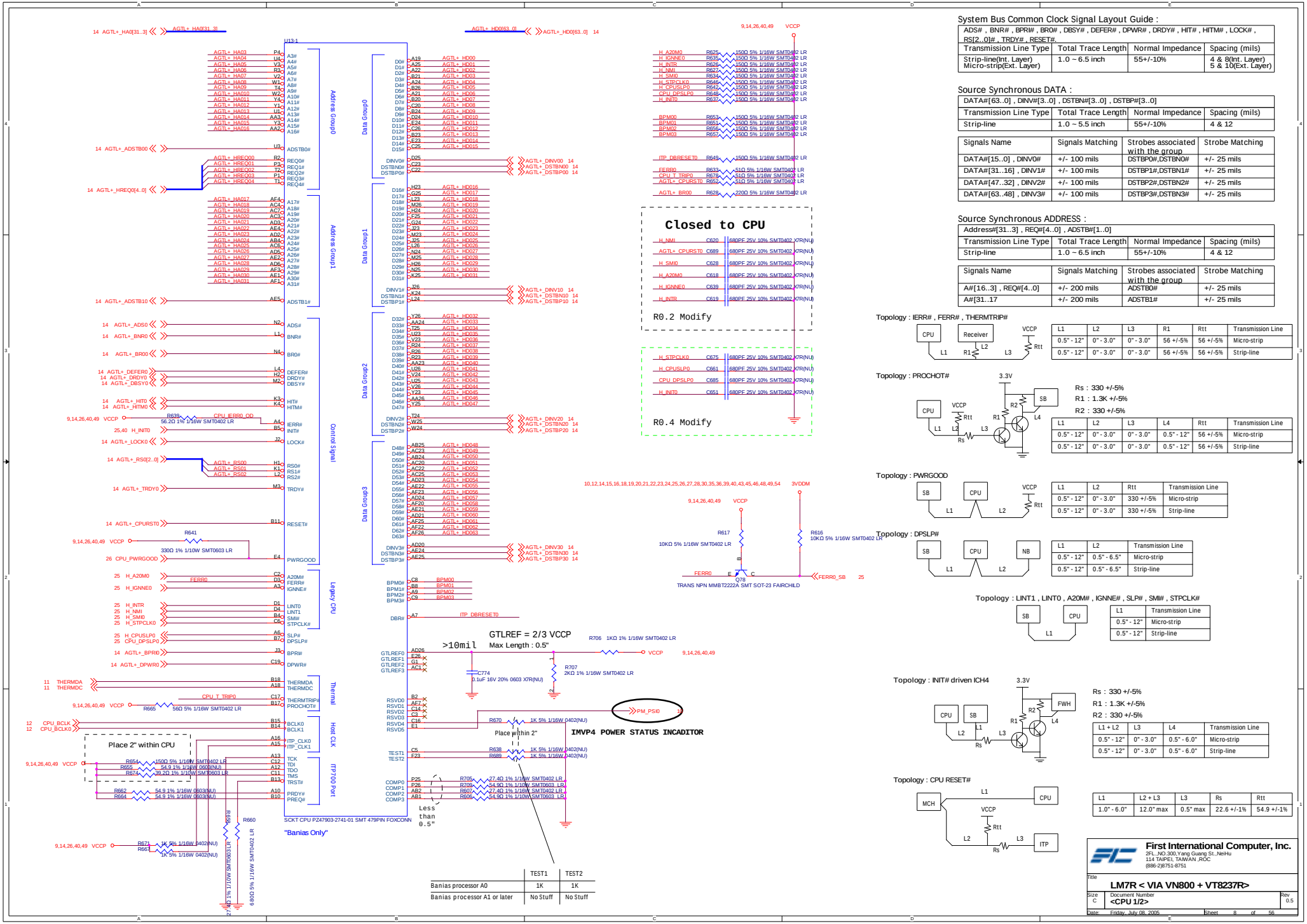

System Bus Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer) Micro-strip(Ext. Layer)	1.0 ~ 6.5 inch	55+/-10%	4 & 8(Int. Layer) 5 & 10(Ext. Layer)

Source Synchronous DATA :

DATA#[63..0] , DINV#[3..0] , DSTBN#[3..0] , DSTBP#[3..0]

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	1.0 ~ 5.5 inch	55+/-10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

Source Synchronous ADDRESS :

Address#[31..3] , REQ#[4..0] , ADSTB#[1..0]

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	1.0 ~ 6.5 inch	55+/-10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 25 mils
A#[31..17	+/- 200 mils	ADSTB1#	+/- 25 mils

Topology : IERR# , FERR# , THERMTRIP#

L1	L2	L3	R1	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Strip-line

Topology : PROCHOT#

Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	0.5" - 12"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	0.5" - 12"	56 +/-5%	Strip-line

Topology : PWRGOOD

L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	330 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	330 +/-5%	Strip-line

Topology : DPSLP#

L1	L2	Transmission Line
0.5" - 12"	0.5" - 6.5"	Micro-strip
0.5" - 12"	0.5" - 6.5"	Strip-line

Topology : LINT1 , LINT0 , A20M# , IGNNE# , SLP# , SMI# , STPCLK#

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INIT# driven ICH4

Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

L1 + L2	L3	L4	Transmission Line
0.5" - 12"	0" - 3.0"	0.5" - 6.0"	Micro-strip
0.5" - 12"	0" - 3.0"	0.5" - 6.0"	Strip-line

Topology : CPU RESET#

L1	L2 + L3	L3	Rs	Rtt
1.0" - 6.0"	12.0" max	0.5" max	22.6 +/-1%	54.9 +/-1%

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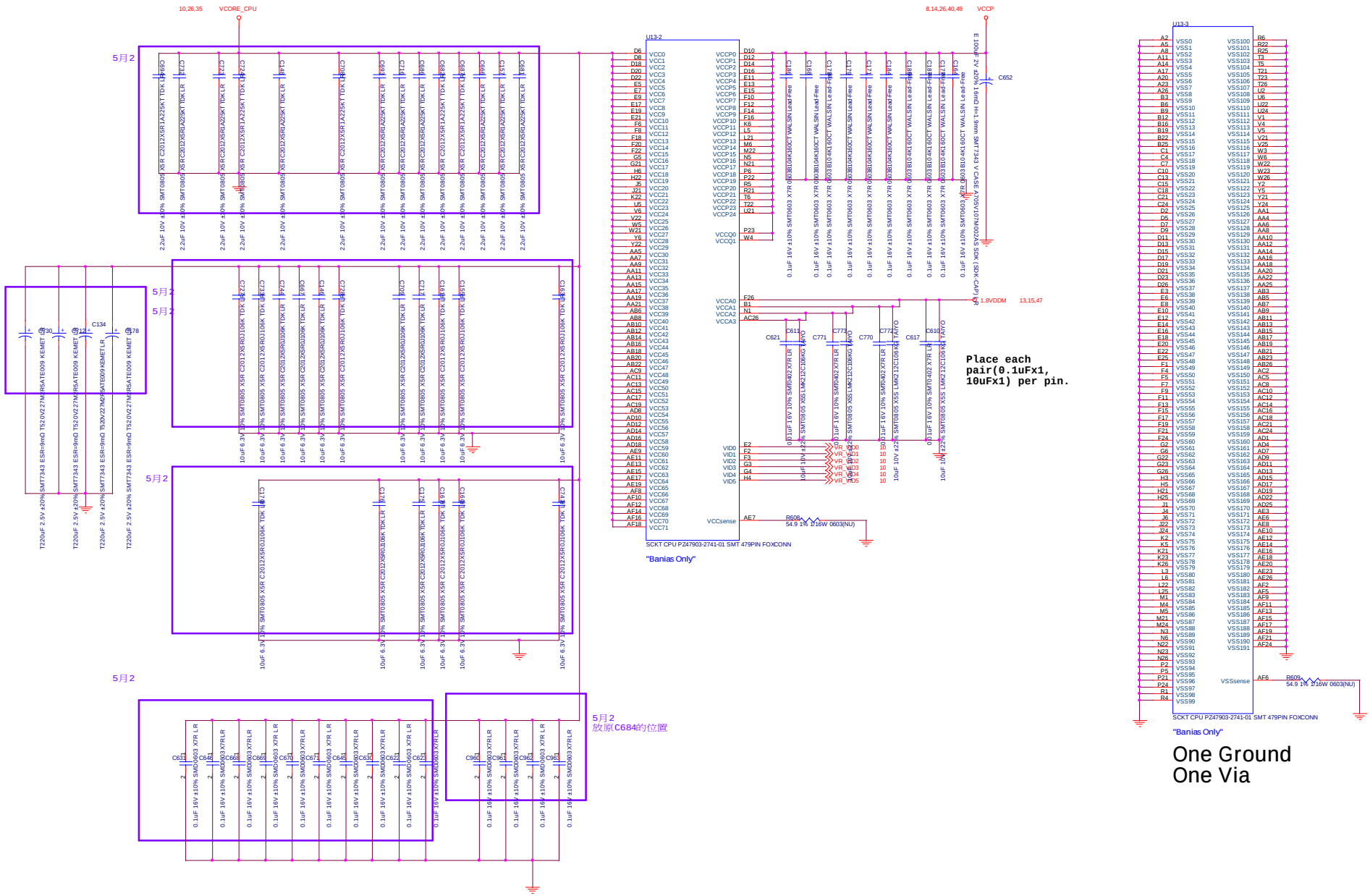

Company	First International Computer, Inc.
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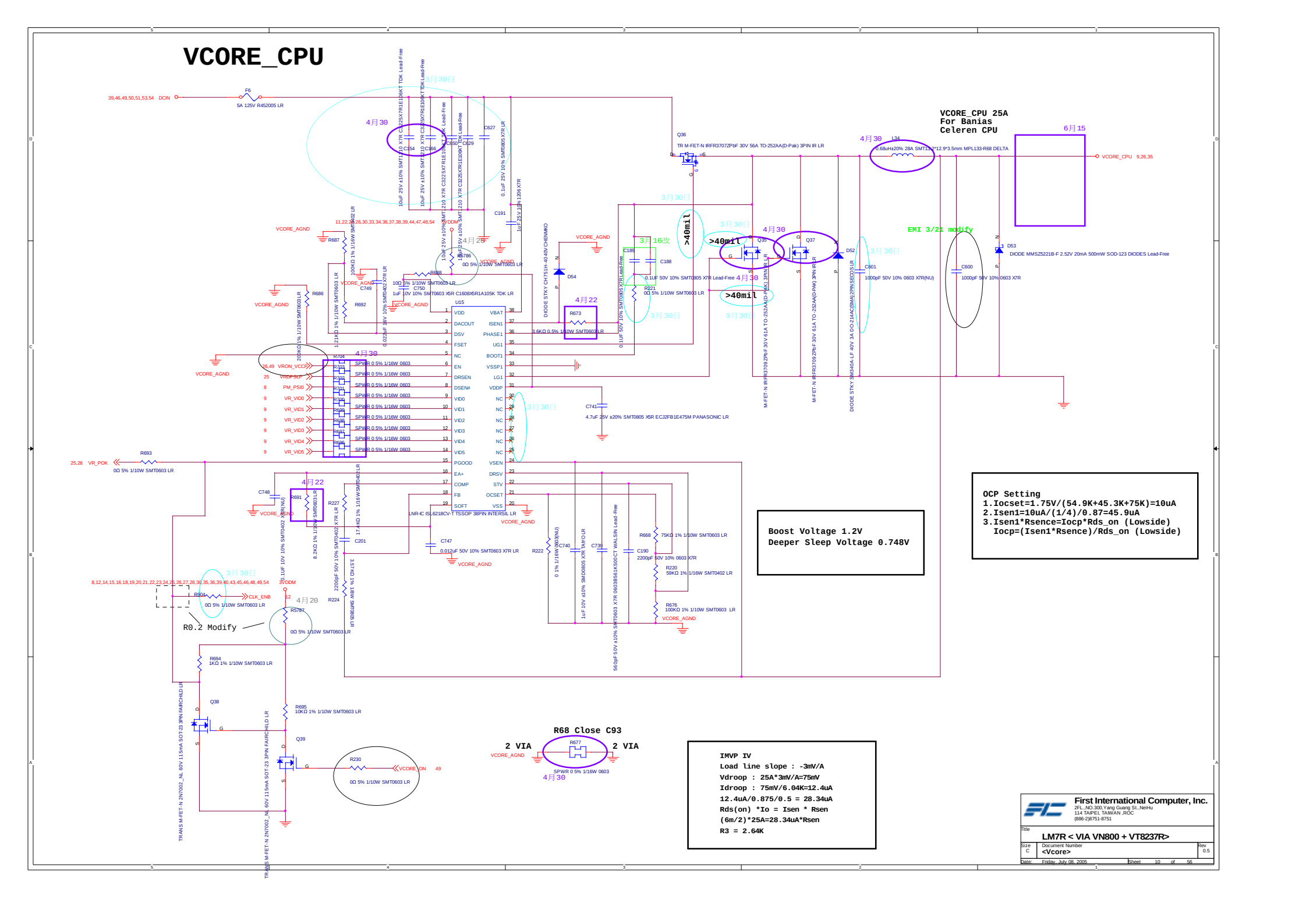
VCORE_CPU
VCORE_CPU 25A
For Banias
Celeren CPU
EMI 3/21 modify
>40mil
>40mil
>40mil
OCP Setting
1.Iocset=1.75V/(54.9K+45.3K+75K)=10uA
2.Isen1=10uA/(1/4)/0.87=45.9uA
3.Isen1*Rsence=Iocp*Rds_on (Lowside)
Iocp=(Isen1*Rsence)/Rds_on (Lowside)
Boost Voltage 1.2V
Deeper Sleep Voltage 0.748V
R0.2 Modify
R68 Close C93
2 VIA
2 VIA
IMVP IV
Load line slope : -3mV/A
Vdroop : 25A*3mV/A=75mV
Idroop : 75mV/6.04K=12.4uA
12.4uA/0.875/0.5 = 28.34uA
Rds(on) *Io = Isen * Rsen
(6m/2)*25A=28.34uA*Rsen
R3 = 2.64K
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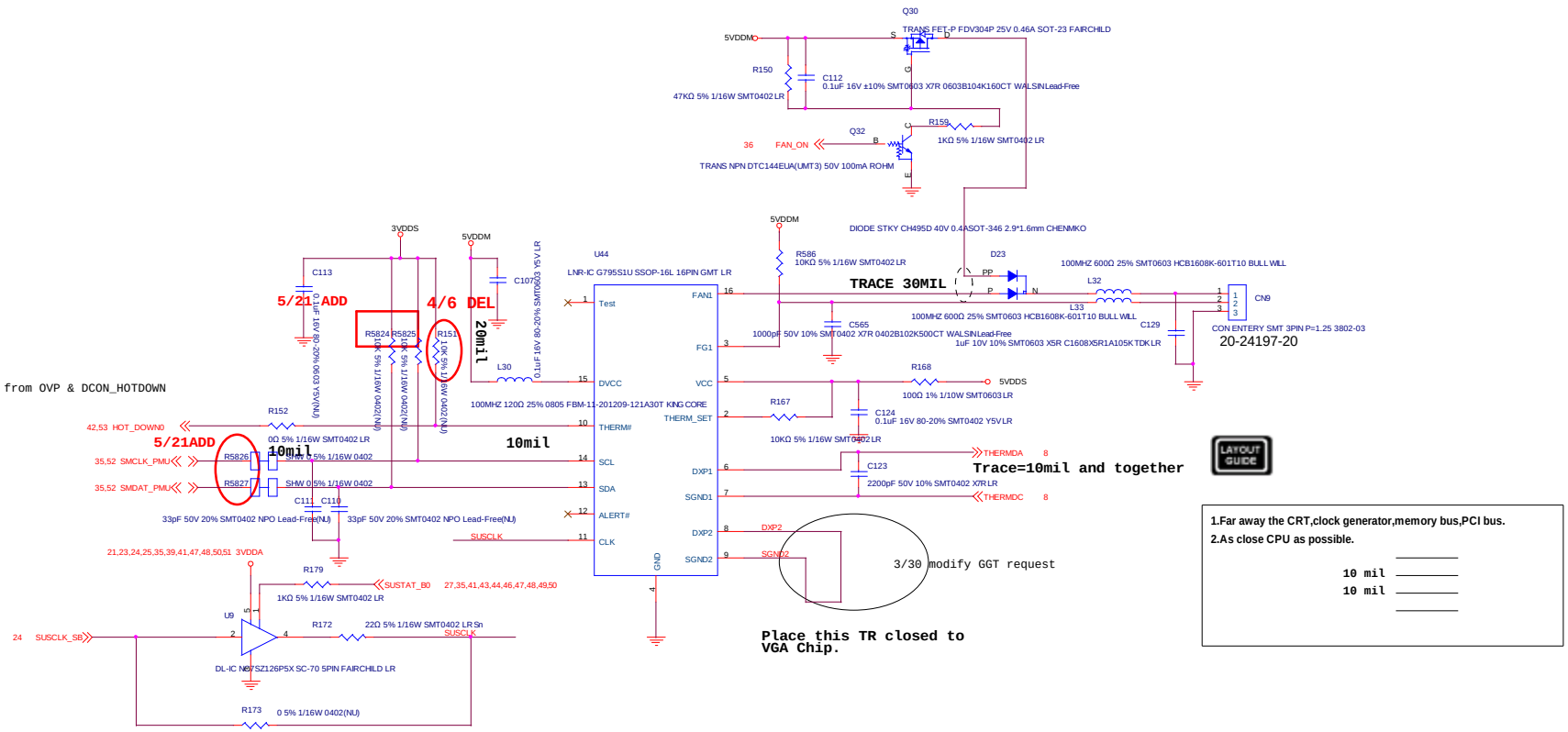
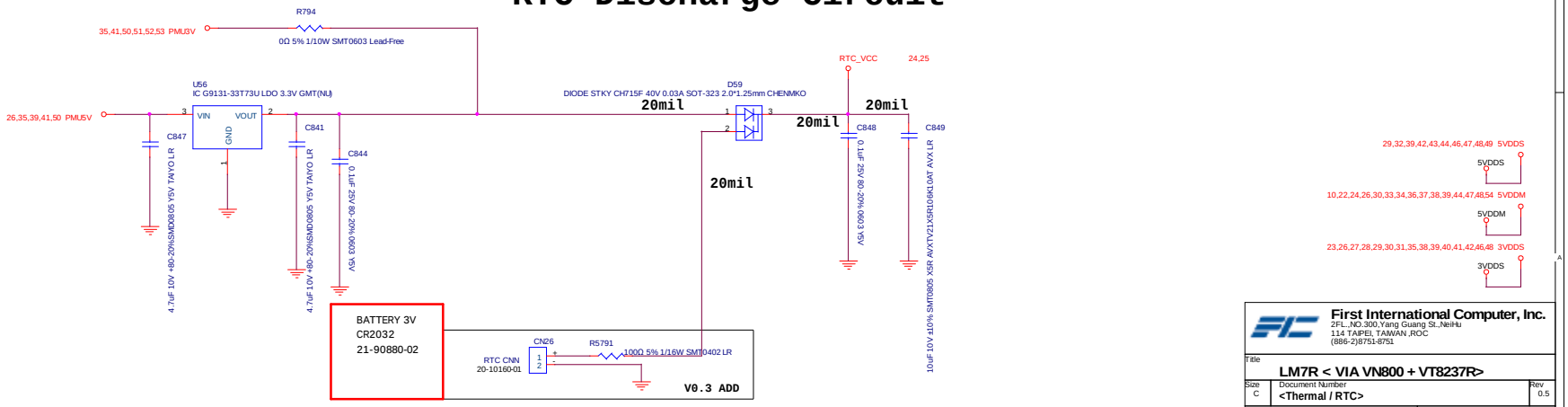
<Vcore>
Friday, July 08, 2005

THERMAL SENSOR



RTC Discharge Circuit



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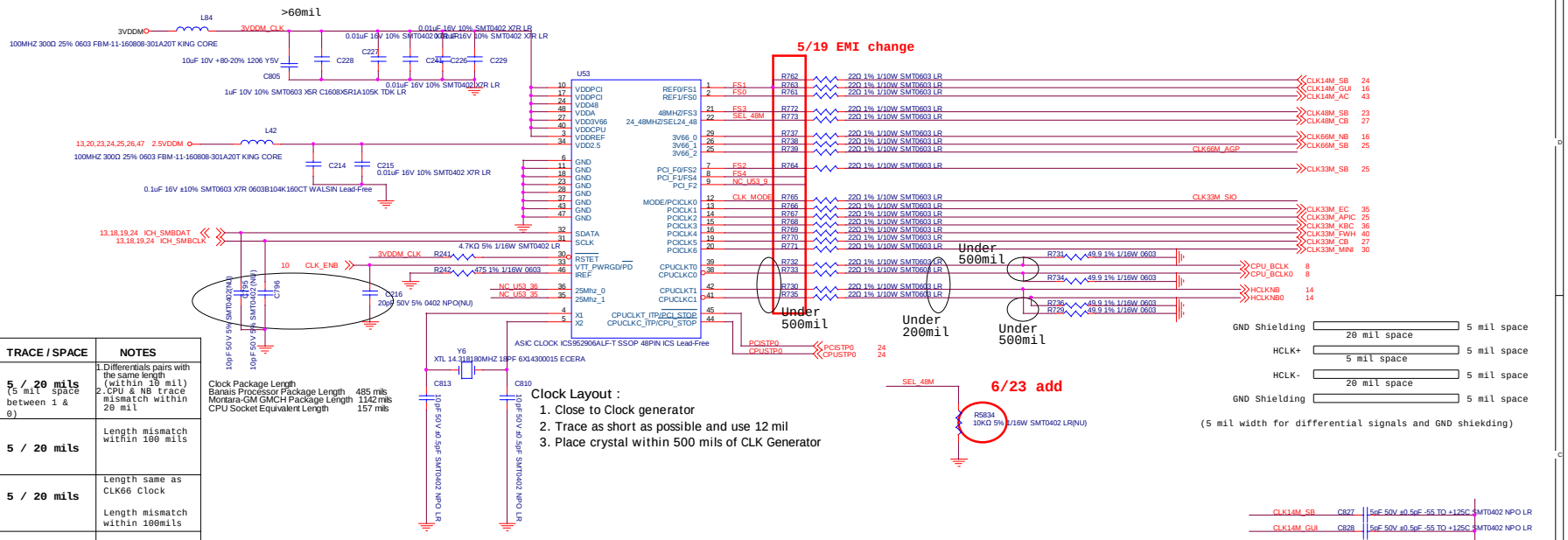


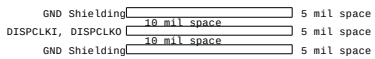
Clock Latout Guideline

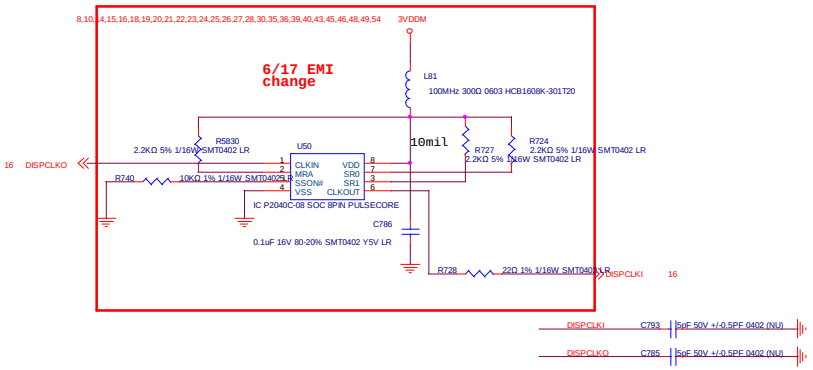
	CLOCKS	LENGTH	TRACE / SPACE	NOTES
HOST Clock	CPU_BCLK[1..0] MCH_BCLK[1..0] ITP_BCLK[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between 1 & 0)	1.Differentials pairs with the same length (within 10 mil) 2.CPU & NB trace mismatch within 20 mil
CLK66 Clock	CLK_ICH66 CLK_MCH66	4.5" ~ 9.0 "	5 / 20 mils	Length mismatch within 100 mils
	CLK_AGP	MAX : 8.5"		
CLK33 Clock	CLK_ICHPCI CLK_SIOPCI CLK_FWHPCI	4.5" ~ 9.0 "	5 / 20 mils	Length same as CLK66 Clock Length mismatch within 100mils
PCI Clock	CLK_MINIPCI CLK_1394PCI CLK_PMU08PCI CLK_CBPCI	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2. Length Require CLK33-2.5" 3. Length mismatch +/- 2.0"
CLK14 Clock	CLK_SIO14 CLK_ICH14 CLK_TV14	2.0"~9.0"	5 / 20 mils	1. Length mismatch +/- 500 mils
	CLK_ICH48 CLK_MCH48	3.5" ~ 12.5"	5 / 20 mils	

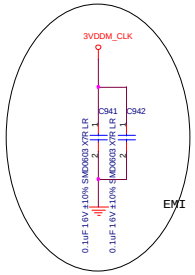
Clock Package Length
Banais Processor Package Length 485 mils
Montara-GM GMCH Package Length 1142 mils
CPU Socket Equivalent Length 157 mils

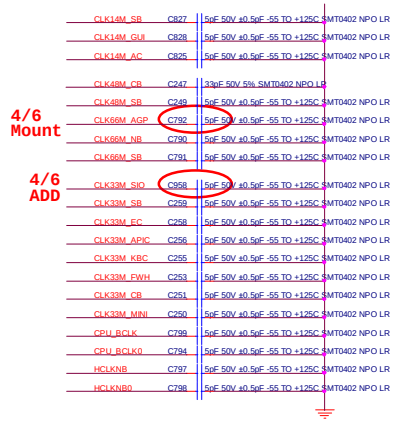
Clock Layout :
1. Close to Clock generator
2. Trace as short as possible and use 12 mil
3. Place crystal within 500 mils of CLK Generator

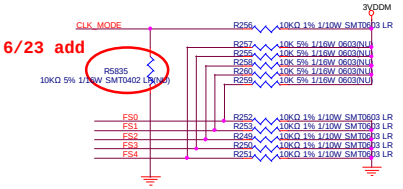
FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	REF
0	0	0	0	0	100.00M	66.67M	33.33M	14.318M
0	0	0	0	1	200.00M	66.67M	33.33M	14.318M
0	0	0	1	0	133.33M	66.67M	33.33M	14.318M
0	0	0	1	1	166.67M	66.67M	33.33M	14.318M
0	0	1	0	1	400.00M	66.67M	33.33M	14.318M











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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <Clock-Gen> | Rev: 0.5

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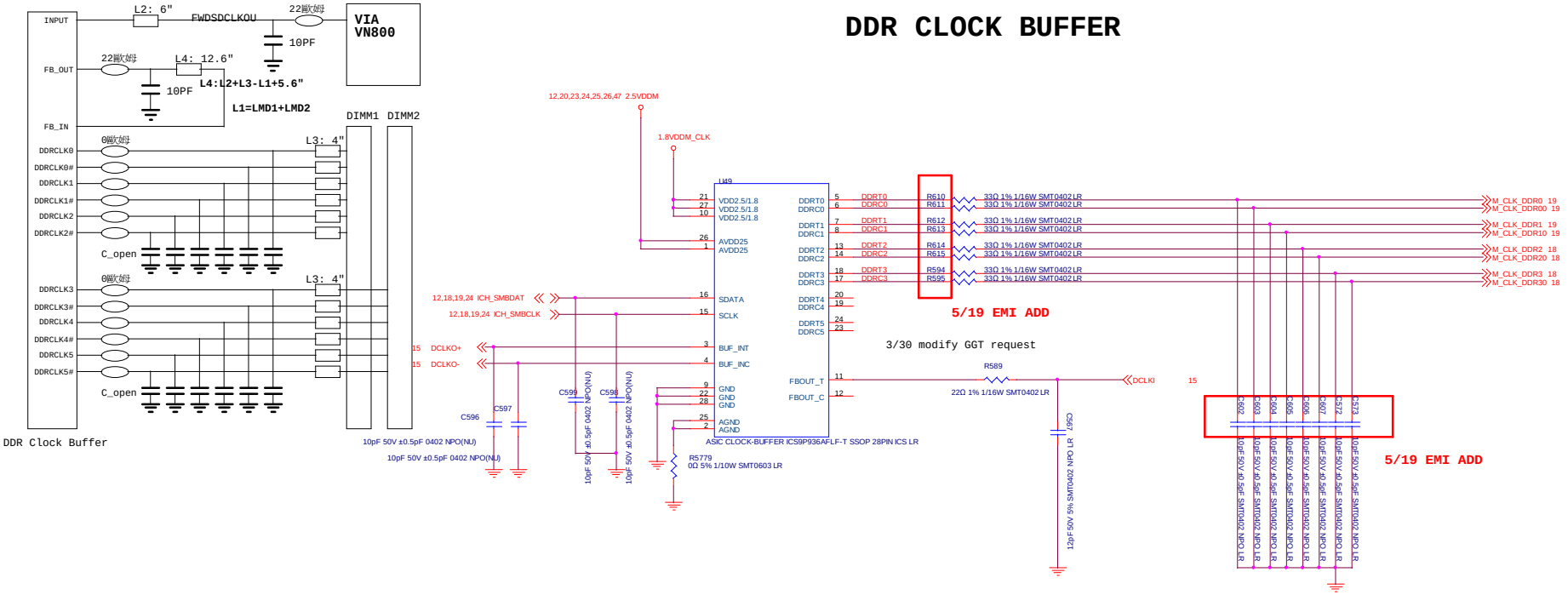
DDR CLOCK BUFFER



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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <clock buffer> | Rev: 0.5

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HOST CPU INTERFACE

U14A
ASIC NB VN800 HSBGA 567PIN VIA

Place these parts near N.B as close as possible.

Place these parts near N.B as close as possible. And place each capacitor per pin.

make sure??

Title	LM7R < VIA VN800 + VT8237R>
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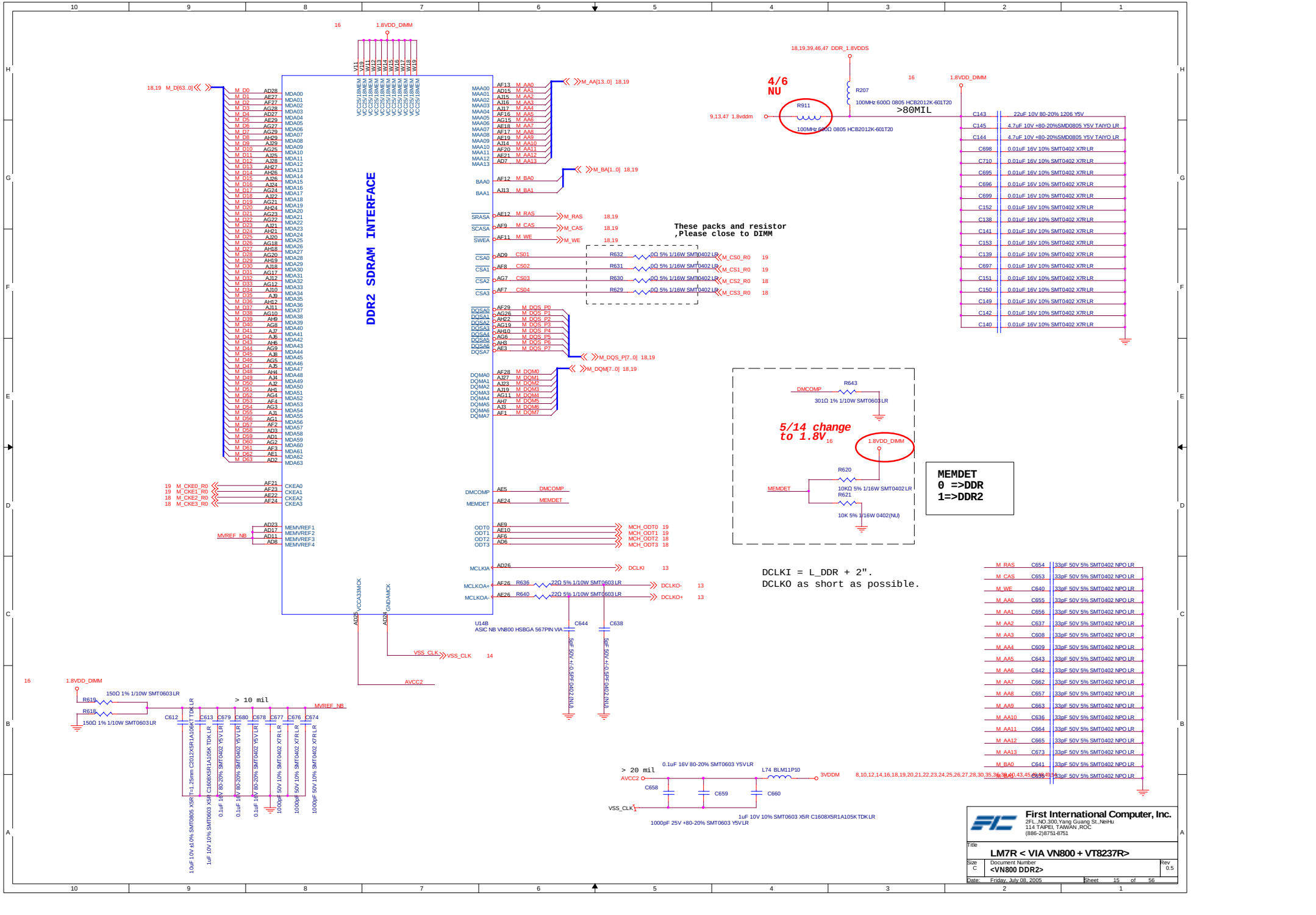
DDR2 SDRAM INTERFACE
18,19 M_D[63..0]
M_D0 AD28 MDA00
M_D1 AE27 MDA01
M_D2 AE27 MDA02
M_D3 AG28 MDA03
M_D4 AD27 MDA04
M_D5 AE29 MDA05
M_D6 AG27 MDA06
M_D7 AG29 MDA07
M_D8 AH29 MDA08
M_D9 AJ29 MDA09
M_D10 AG25 MDA10
M_D11 AJ25 MDA11
M_D12 AJ28 MDA12
M_D13 AH27 MDA13
M_D14 AH26 MDA14
M_D15 AJ26 MDA15
M_D16 AJ24 MDA16
M_D17 AG24 MDA17
M_D18 AJ22 MDA18
M_D19 AG21 MDA19
M_D20 AH24 MDA20
M_D21 AG23 MDA21
M_D22 AG22 MDA22
M_D23 AJ21 MDA23
M_D24 AH21 MDA24
M_D25 AJ20 MDA25
M_D26 AG18 MDA26
M_D27 AH18 MDA27
M_D28 AG20 MDA28
M_D29 AH19 MDA29
M_D30 AJ18 MDA30
M_D31 AG17 MDA31
M_D32 AJ12 MDA32
M_D33 AG12 MDA33
M_D34 AJ10 MDA34
M_D35 AJ9 MDA35
M_D36 AH12 MDA36
M_D37 AJ11 MDA37
M_D38 AG10 MDA38
M_D39 AH9 MDA39
M_D40 AG8 MDA40
M_D41 AJ7 MDA41
M_D42 AJ5 MDA42
M_D43 AH6 MDA43
M_D44 AG9 MDA44
M_D45 AJ8 MDA45
M_D46 AG5 MDA46
M_D47 AJ5 MDA47
M_D48 AH4 MDA48
M_D49 AJ4 MDA49
M_D50 AJ2 MDA50
M_D51 AH1 MDA51
M_D52 AG4 MDA52
M_D53 AF4 MDA53
M_D54 AG3 MDA54
M_D55 AJ1 MDA55
M_D56 AG1 MDA56
M_D57 AF2 MDA57
M_D58 AD3 MDA58
M_D59 AD1 MDA59
M_D60 AG2 MDA60
M_D61 AF3 MDA61
M_D62 AE1 MDA62
M_D63 AD2 MDA63
16 1.8VDD_DIMM
VC25/18MEM
MAA00 AF13 M_AA0
MAA01 AD15 M_AA1
MAA02 AJ15 M_AA2
MAA03 AJ16 M_AA3
MAA04 AJ17 M_AA4
MAA05 AF16 M_AA5
MAA06 AG15 M_AA6
MAA07 AE18 M_AA7
MAA08 AF17 M_AA8
MAA09 AE19 M_AA9
MAA10 AJ14 M_AA10
MAA11 AF20 M_AA11
MAA12 AE21 M_AA12
MAA13 AD7 M_AA13
M_AA[13..0] 18,19
BAA0 AF12 M_BA0
BAA1 AJ13 M_BA1
M_BA[1..0] 18,19
SRASA AE12 M_RAS M_RAS 18,19
SCASA AF9 M_CAS M_CAS 18,19
SWEA AF11 M_WE M_WE 18,19
These packs and resistor ,Please close to DIMM
CSA0 AD9 CS01 R632 0Ω 5% 1/16W SMT0402 LR M_CS0_R0 19
CSA1 AF8 CS02 R631 0Ω 5% 1/16W SMT0402 LR M_CS1_R0 19
CSA2 AG7 CS03 R630 0Ω 5% 1/16W SMT0402 LR M_CS2_R0 18
CSA3 AF7 CS04 R629 0Ω 5% 1/16W SMT0402 LR M_CS3_R0 18
DQSA0 AF29 M_DQS_P0
DQSA1 AG26 M_DQS_P1
DQSA2 AH22 M_DQS_P2
DQSA3 AG19 M_DQS_P3
DQSA4 AH10 M_DQS_P4
DQSA5 AG6 M_DQS_P5
DQSA6 AH3 M_DQS_P6
DQSA7 AE3 M_DQS_P7
M_DQS_P[7..0] 18,19
DQMA0 AF28 M_DQM0
DQMA1 AJ27 M_DQM1
DQMA2 AJ23 M_DQM2
DQMA3 AJ19 M_DQM3
DQMA4 AG11 M_DQM4
DQMA5 AH7 M_DQM5
DQMA6 AJ3 M_DQM6
DQMA7 AF1 M_DQM7
M_DQM[7..0] 18,19
19 M_CKE0_R0 AF21 CKEA0
19 M_CKE1_R0 AF23 CKEA1
18 M_CKE2_R0 AF22 CKEA2
18 M_CKE3_R0 AF24 CKEA3
DMCOMP AE5 DMCOMP
MEMDET AE24 MEMDET
MVREF_NB AD23 AD17 AD11 AD8 MEMVREF1 MEMVREF2 MEMVREF3 MEMVREF4
ODT0 AE9 MCH_ODT0 19
ODT1 AE10 MCH_ODT1 19
ODT2 AF6 MCH_ODT2 18
ODT3 AD6 MCH_ODT3 18
MCLKIA AD26 DCLKI 13
MCLKOA+ AF26 R636 22Ω 5% 1/10W SMT0603 LR DCLKO- 13
MCLKOA- AE26 R640 22Ω 5% 1/10W SMT0603 LR DCLKO+ 13
AD25 VCCA33MCK
AD24 GNDAMCK
VSS_CLK VSS_CLK 14
AVCC2
U14B
ASIC NB VN800 HSBGA 567PIN VIA
C644 C638 56pF 50V +-0.5pF 0402 CNJ
18,19,39,46,47 DDR_1.8VDDS
4/6 NU
R207 100MHz 600Ω 0805 HCB2012K-601T20
>80MIL
9,13,47 1.8vddm
R911 100MHz 600Ω 0805 HCB2012K-601T20
16 1.8VDD_DIMM
C143 22uF 10V 80-20% 1206 Y5V
C145 4.7uF 10V +80-20%SMD0805 Y5V TAIYO LR
C144 4.7uF 10V +80-20%SMD0805 Y5V TAIYO LR
C698 C710 C695 C696 C699 C152 C138 C141 C153 C139 C697 C151 C150 C149 C142 C140 0.01uF 16V 10% SMT0402 X7R LR
DMCOMP R643 301Ω 1% 1/10W SMT0603 LR
5/14 change to 1.8V
16 1.8VDD_DIMM
MEMDET R620 10KΩ 5% 1/16W SMT0402 LR
R621 10K 5% 1/16W 0402(NU)
MEMDET 0 =>DDR 1=>DDR2
DCLKI = L_DDR + 2".
DCLKO as short as possible.
M_RAS C654 M_CAS C653 M_WE C640 M_AA0 C655 M_AA1 C656 M_AA2 C637 M_AA3 C608 M_AA4 C609 M_AA5 C643 M_AA6 C642 M_AA7 C662 M_AA8 C657 M_AA9 C663 M_AA10 C636 M_AA11 C664 M_AA12 C665 M_AA13 C673 M_BA0 C641 M_BA1 C635 33pF 50V 5% SMT0402 NPO LR
16 1.8VDD_DIMM
R619 150Ω 1% 1/10W SMT0603 LR
R618 150Ω 1% 1/10W SMT0603 LR
> 10 mil
MVREF_NB
C612 C613 C679 C680 C678 C677 C676 C674
10uF 10V +1.0% SMT0805 X5R
1uF 10V 10% SMT0603 X5R C1608X5R1A105K TDK LR
0.1uF 10V 80-20% SMT0402 Y5V LR
1000pF 50V 10% SMT0402 X7R LR
> 20 mil
AVCC2
0.1uF 16V 80-20% SMT0603 Y5V LR
L74 BLM11P10
3VDDM
8,10,12,14,16,18,19,20,21,22,23,24,25,26,27,28,30,35,36,38,40,43,45,46,48,49,54
C658 C659 C660
VSS_CLK
1uF 10V 10% SMT0603 X5R C1608X5R1A105K TDK LR
1000pF 25V +80-20% SMT0603 Y5V LR
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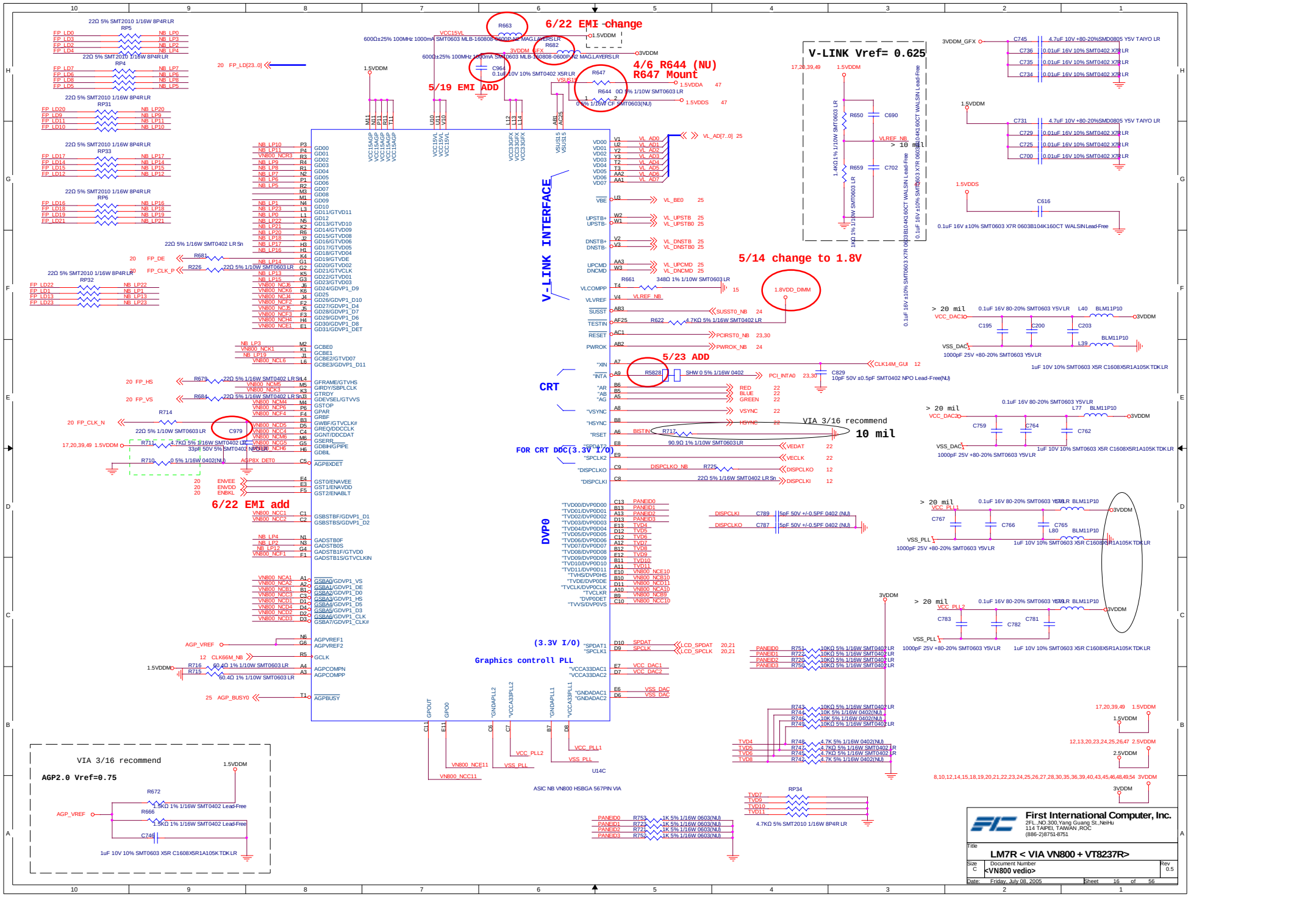
Title
LM7R < VIA VN800 + VT8237R>
Size C
Document Number <VN800 DDR2>
Rev 0.5
Date: Friday, July 08, 2005
Sheet 15 of 56


6/22 EMI change
4/6 R644 (NU)
R647 Mount
5/19 EMI ADD
V-LINK Vref= 0.625
5/14 change to 1.8V
5/23 ADD
V-LINK INTERFACE
CRT
DVP0
Graphics controll PLL
(3.3V I/O)
FOR CRT DDC(3.3V I/O)
6/22 EMI add
VIA 3/16 recommend
10 mil
AGP2.0 Vref=0.75
ASIC NB VN800 HSBGA 567PIN VIA
U14C
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LM7R < VIA VN800 + VT8237R>
<VN800 vedio>
Size C
Rev 0.5
Date: Friday, July 08, 2005
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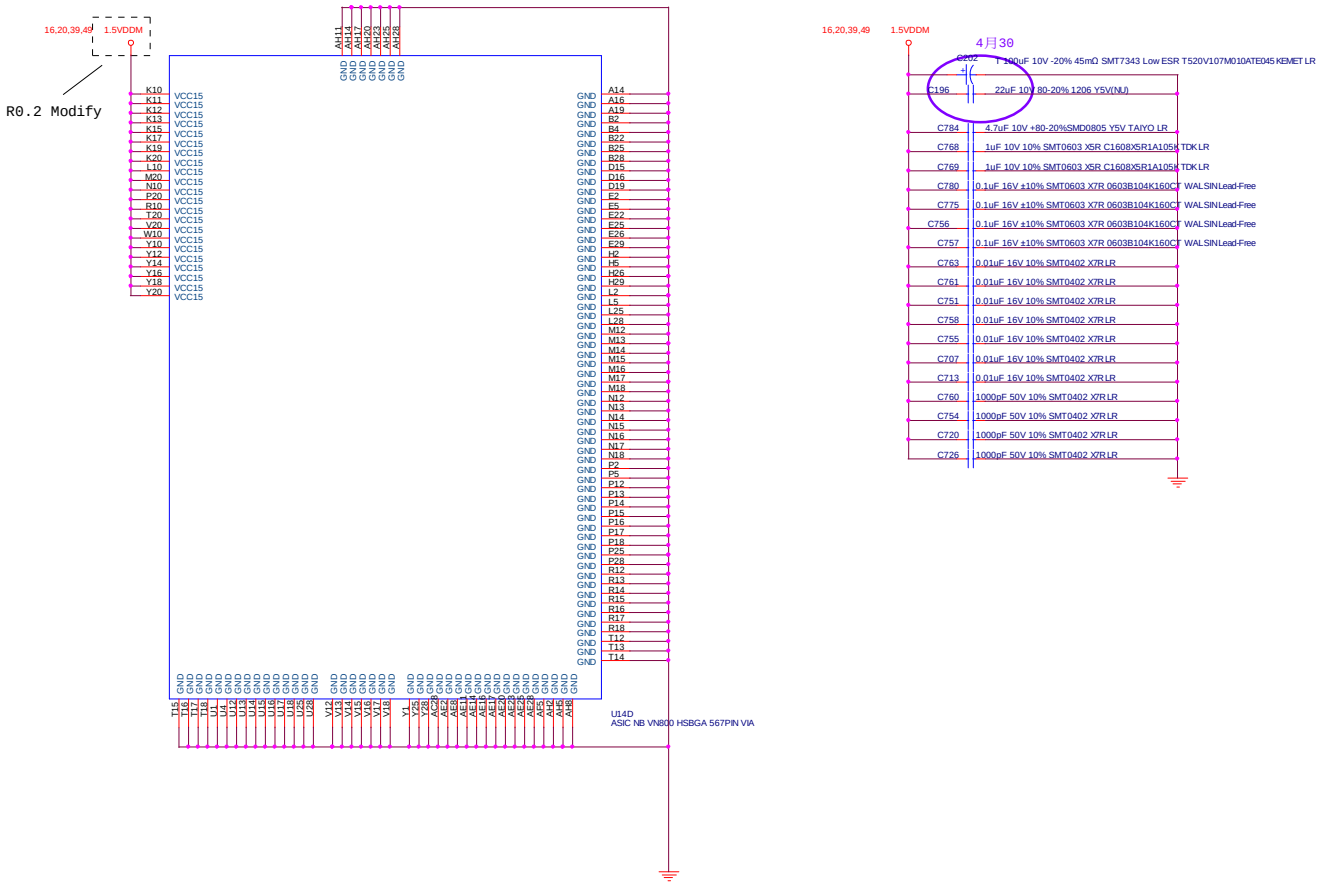

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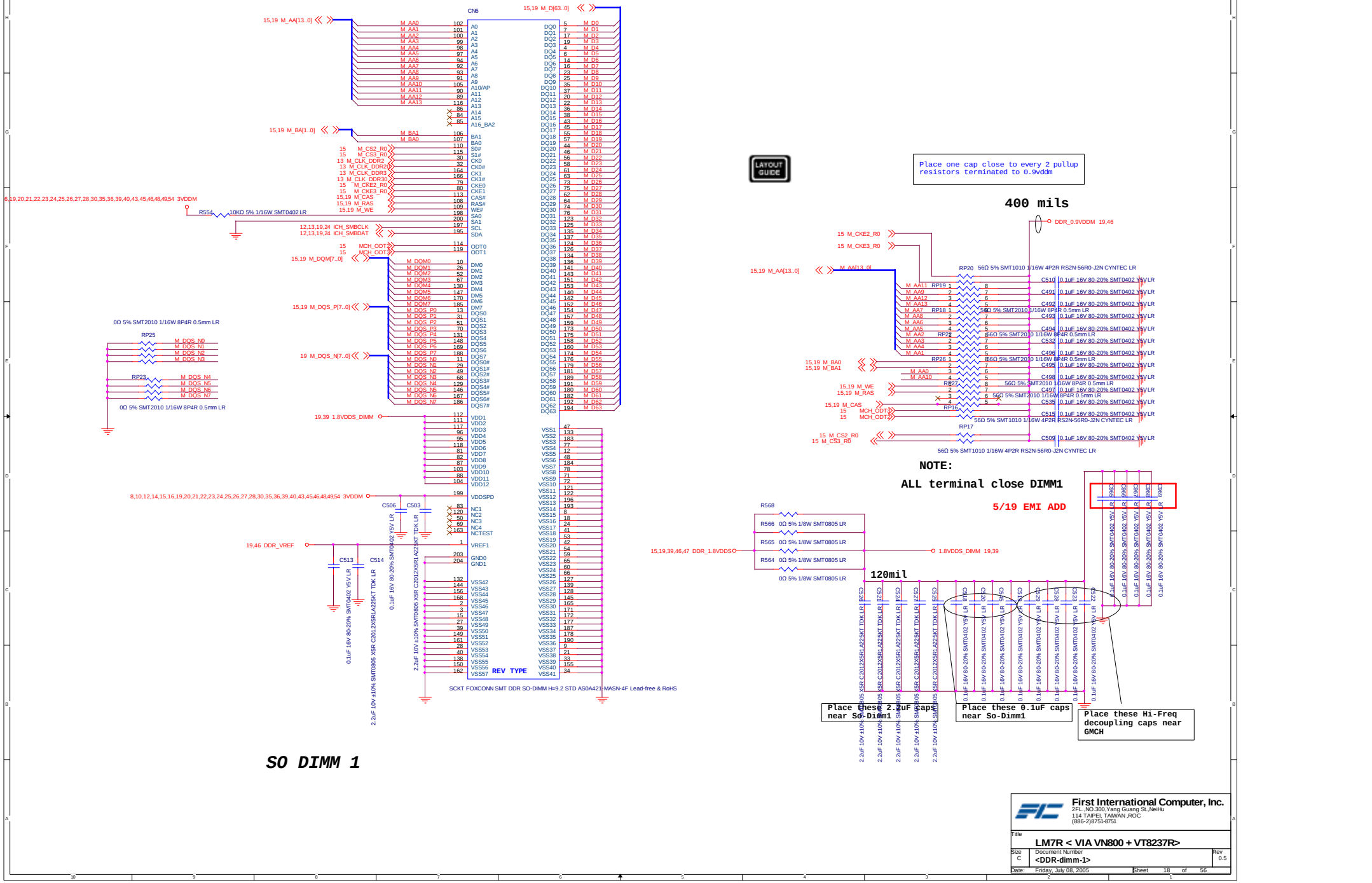
Title: **LM7R < VIA VN800 + VT8237R>**

Size	Document Number	Rev
C	<VN800 power>	0.5

Date: Friday, July 08, 2005 Sheet 17 of 56


CN6
SCKT FOXCONN SMT DDR SO-DIMM H=9.2 STD AS0A421-MASN-4F Lead-free & RoHS
REV TYPE
SO DIMM 1
LAYOUT GUIDE
Place one cap close to every 2 pullup resistors terminated to 0.9vddm
400 mils
NOTE:
ALL terminal close DIMM1
5/19 EMI ADD
120mil
Place these 2.2uF caps near So-Dimm1
Place these 0.1uF caps near So-Dimm1
Place these Hi-Freq decoupling caps near GMCH
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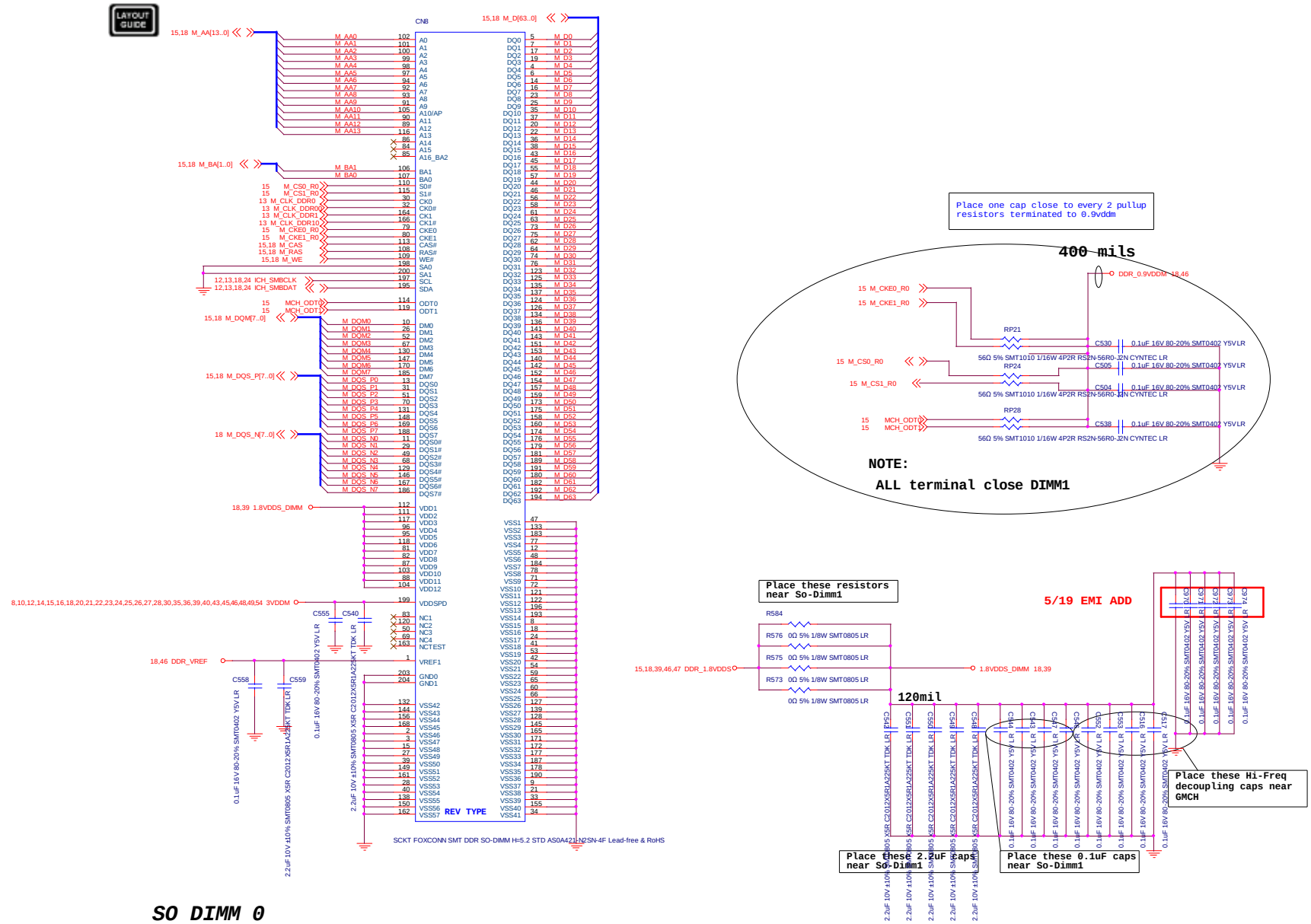
LM7R < VIA VN800 + VT8237R>
<DDR-dimm-1>
Friday, July 08, 2005



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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <DDR-dimm-2> | Rev: 0.5

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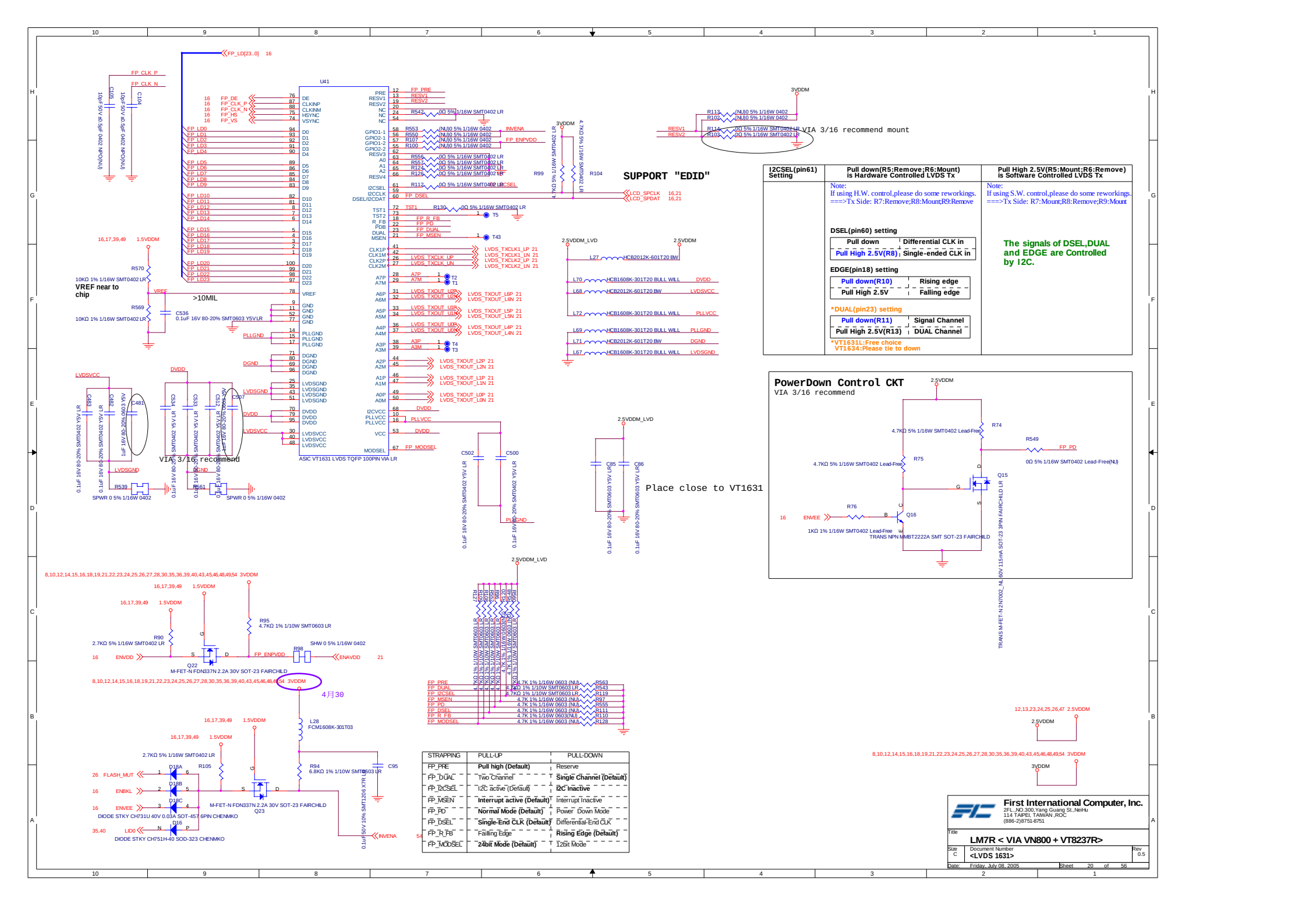
U41
ASIC VT1631 LVDS TQFP 100PIN VIA LR
SUPPORT "EDID"
VIA 3/16 recommend mount
VREF near to chip
>10MIL
VIA 3/16 recommend
Place close to VT1631
SPWR 0 5% 1/16W 0402
SPWR 0 5% 1/16W 0402
DIODE STKY CH731U 40V 0.03A SOT-457 6PIN CHENMKO
DIODE STKY CH751H-40 SOD-323 CHENMKO
M-FET-N FDN337N 2.2A 30V SOT-23 FAIRCHILD
M-FET-N FDN337N 2.2A 30V SOT-23 FAIRCHILD
TRANS M-FET-N 2N7002_NL 60V 115mA SOT-23 3PIN FAIRCHILD LR
TRANS NPN MMBT2222A SMT SOT-23 FAIRCHILD
4月30
I2CSEL(pin61) Setting
Pull down(R5:Remove;R6:Mount) is Hardware Controlled LVDS Tx
Pull High 2.5V(R5:Mount;R6:Remove) is Software Controlled LVDS Tx
Note:
If using H.W. control,please do some reworkings.
===>Tx Side: R7:Remove;R8:Mount;R9:Remove
Note:
If using S.W. control,please do some reworkings.
===>Tx Side: R7:Mount;R8:Remove;R9:Mount
DSEL(pin60) setting
Pull down
Differential CLK in
Pull High 2.5V(R8)
Single-ended CLK in
EDGE(pin18) setting
Pull down(R10)
Rising edge
Pull High 2.5V
Falling edge
*DUAL(pin23) setting
Pull down(R11)
Signal Channel
Pull High 2.5V(R13)
DUAL Channel
*VT1631L:Free choice
VT1634:Please tie to down
The signals of DSEL,DUAL and EDGE are Controlled by I2C.
PowerDown Control CKT
VIA 3/16 recommend
STRAPPING
PULL-UP
PULL-DOWN
FP_PRE
Pull high (Default)
Reserve
FP_DUAL
Two Channel
Single Channel (Default)
FP_I2CSEL
I2C active (Default)
I2C Inactive
FP_MSEN
Interrupt active (Default)
Interrupt Inactive
FP_PD
Normal Mode (Default)
Power Down Mode
FP_DSEL
Single-End CLK (Default)
Differential-End CLK
FP_R_FB
Failing Edge
Rising Edge (Default)
FP_MODSEL
24bit Mode (Default)
12bit Mode
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Title
LM7R < VIA VN800 + VT8237R>
Size C
Document Number <LVDS 1631>
Rev 0.5
Date: Friday, July 08, 2005
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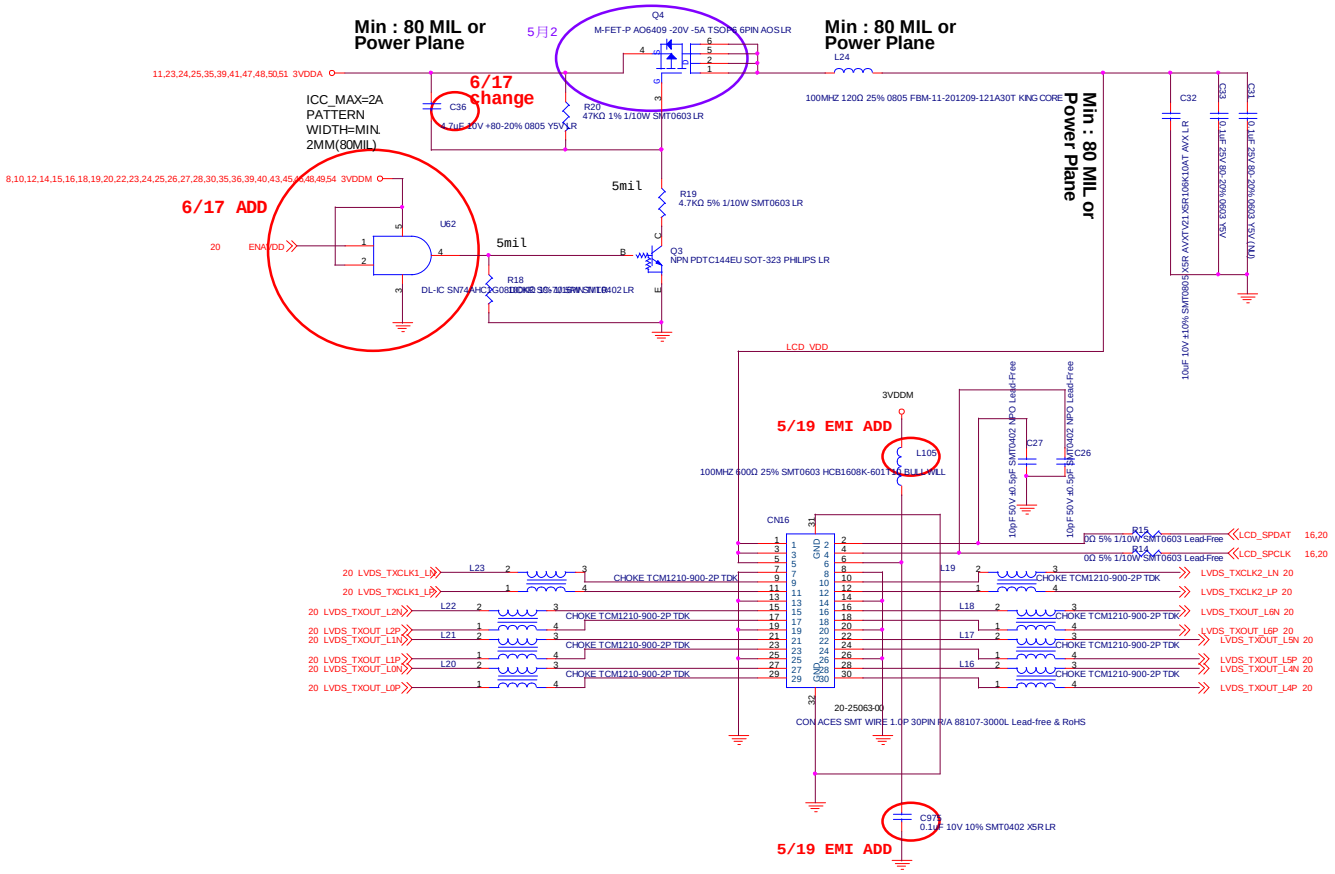

LVDS Interface

Signal	LENGTH	TRACE	SPACE	TRACE MUTCHING	Impedance	Note
LVDS	10" Cable MAX 16"	4 mils (stripline) 6 mils (microstrip)	20 mils 7 mils (edge to edge) 20 mils (pair to pair) 20 mils (to non LVDS signal)	+/-20 mils (data to clock) +/-20 mils (with a clock pair) X +/-20 mils (clock to clock)	100 ohms +/-15%	Breakout region from NB should be less than 500 mils

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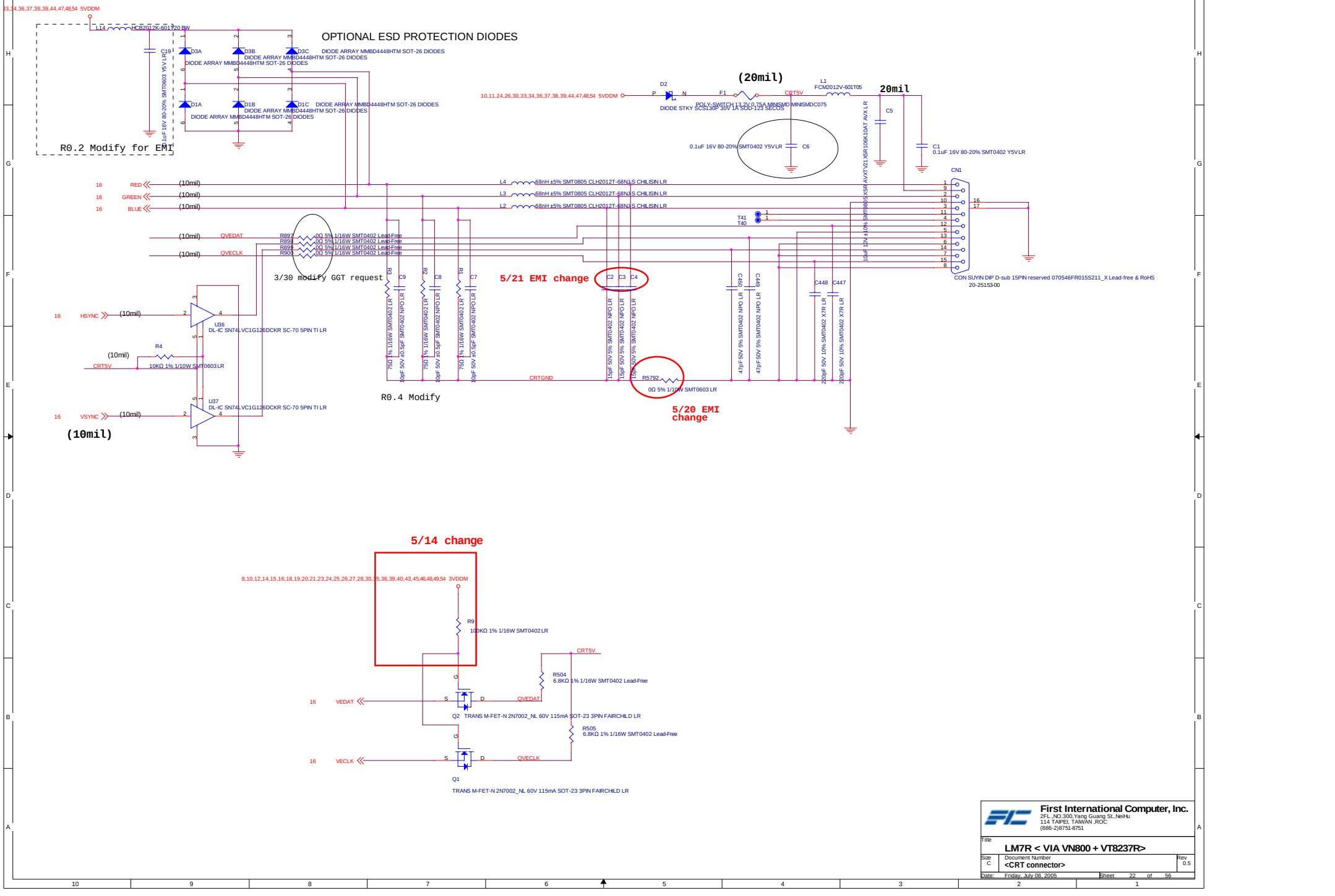
Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <LCD connecter> | Rev: 0.5

Date: Friday, July 08, 2005 | Sheet 21 of 56



Company	First International Computer, Inc.
Address	2FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC
Phone	(886-2)8751-8751
Title	LM7R < VIA VN800 + VT8237R>
Size	C
Document Number	<CRT connector>
Rev	0.5
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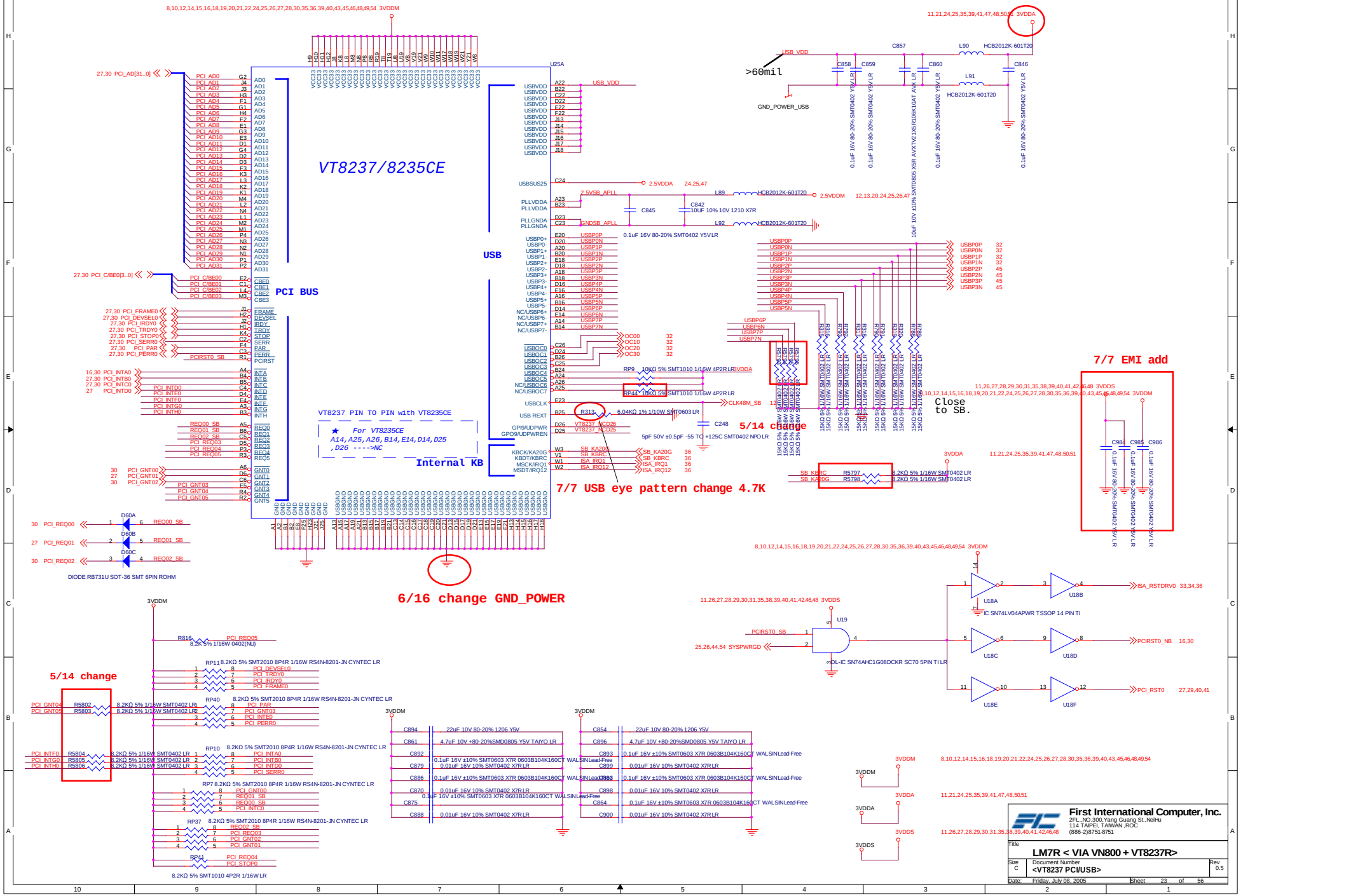
VT8237/8235CE
PCI BUS
USB
Internal KB
VT8237 PIN TO PIN with VT8235CE
★ For VT8235CE
A14, A25, A26, B14, E14, D14, D25
, D26 ----->NC
7/7 USB eye pattern change 4.7K
5/14 change
7/7 EMI add
Close to SB.
6/16 change GND_POWER
DIODE RB731U SOT-36 SMT 6PIN ROHM
IC SN74LV04APWR TSSOP 14 PIN TI
DL-IC SN74AHC1G08DCKR SC70 5PIN TI LR
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LM7R < VIA VN800 + VT8237R>
<VT8237 PCI/USB>
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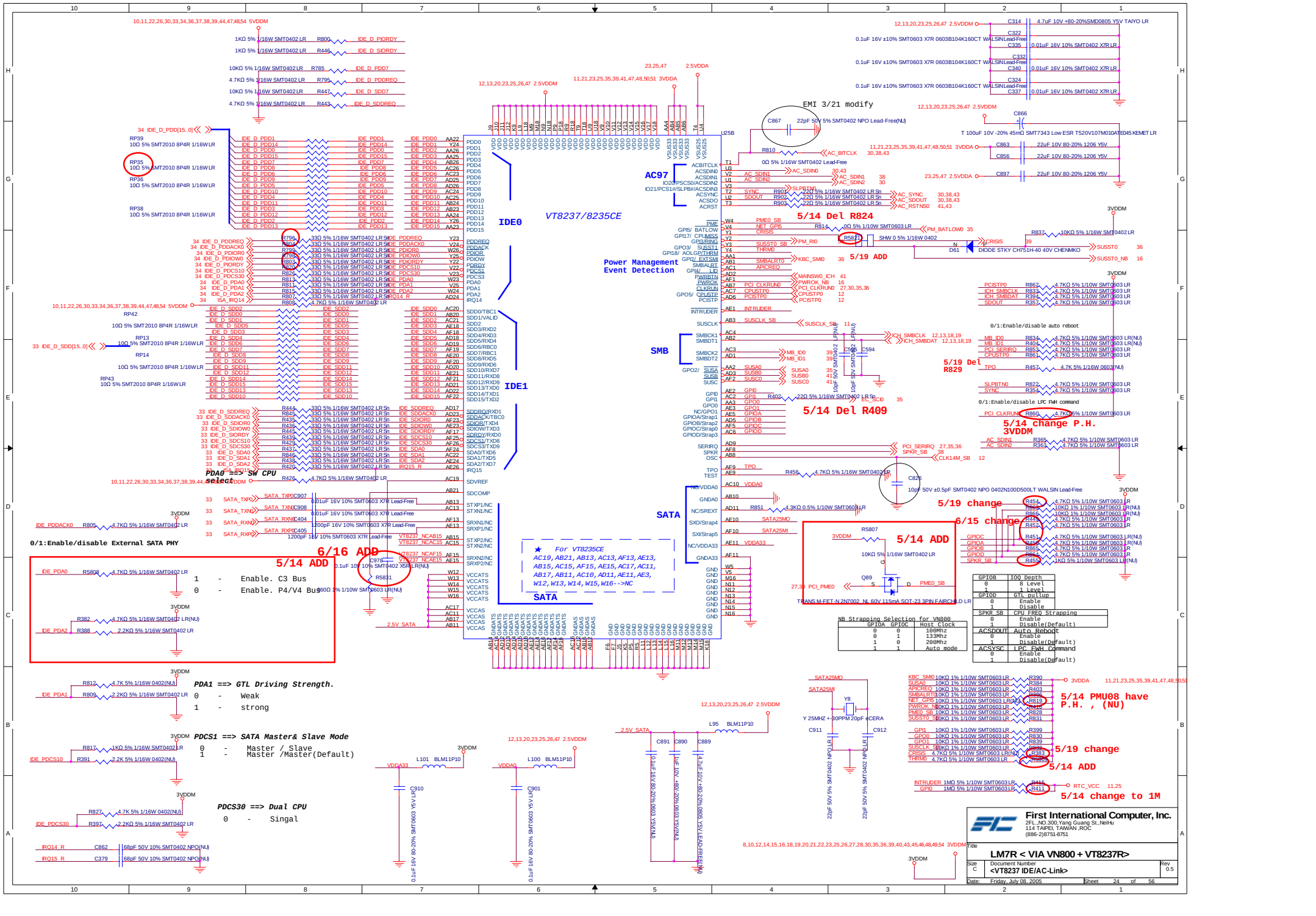
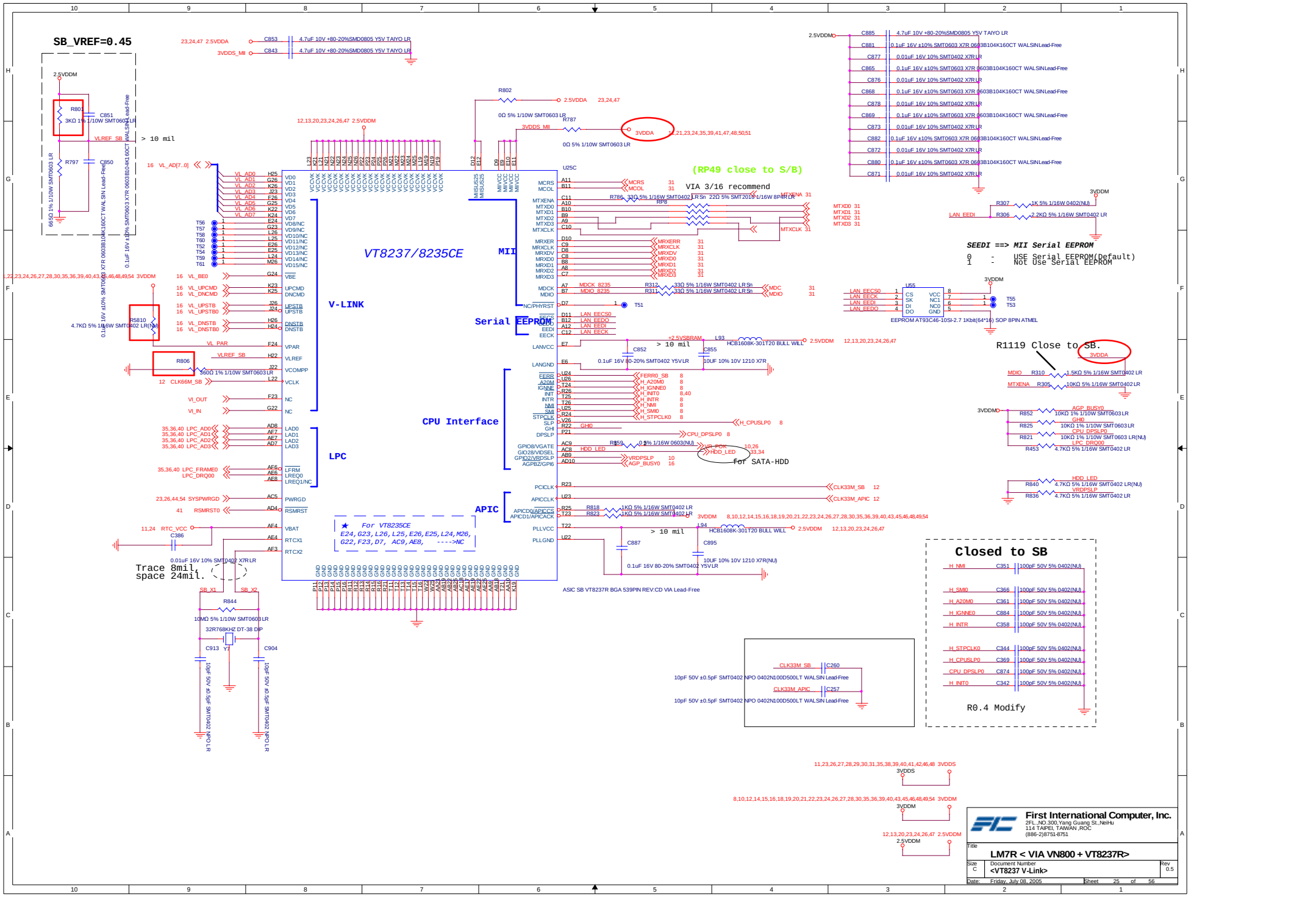

VT8237/8235CE
IDE0
IDE1
SMB
SATA
AC97
Power Management
Event Detection
EMI 3/21 modify
5/14 Del R824
5/19 ADD
5/14 Del R409
5/19 Del R829
5/14 change P.H. 3VDDM
5/19 change
6/15 change
5/14 ADD
6/16 ADD
PDA0 ==> SW CPU select
0/1:Enable/disable External SATA PHY
PDA1 ==> GTL Driving Strength.
PDCS1 ==> SATA Master& Slave Mode
PDCS30 ==> Dual CPU
5/14 PMU08 have P.H. , (NU)
5/14 change to 1M
First International Computer, Inc.
LM7R < VIA VN800 + VT8237R>
<VT8237 IDE/AC-Link>


SB_VREF=0.45
VT8237/8235CE
V-LINK
MII
Serial EEPROM
CPU Interface
LPC
APIC
(RP49 close to S/B)
VIA 3/16 recommend
SEEDI ==> MII Serial EEPROM
0 - USE Serial EEPROM(Default)
1 - Not Use Serial EEPROM
EEPROM AT93C46-10SI-2.7 1Kbit(64*16) SOP 8PIN ATMEL
R1119 Close to SB.
Closed to SB
H_NMI C351 100pF 50V 5% 0402(NU)
H_SMI0 C366 100pF 50V 5% 0402(NU)
H_A20M0 C361 100pF 50V 5% 0402(NU)
H_IGNNE0 C884 100pF 50V 5% 0402(NU)
H_INTR C358 100pF 50V 5% 0402(NU)
H_STPCLK0 C344 100pF 50V 5% 0402(NU)
H_CPUSLP0 C369 100pF 50V 5% 0402(NU)
CPU_DPSLP0 C874 100pF 50V 5% 0402(NU)
H_INIT0 C342 100pF 50V 5% 0402(NU)
R0.4 Modify
Trace 8mil,
space 24mil.
★ For VT8235CE
E24, G23, L26, L25, E26, E25, L24, M26,
G22, F23, D7, AC9, AE8, ---->NC
ASIC SB VT8237R BGA 539PIN REV:CD VIA Lead-Free
First International Computer, Inc.
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(886-2)8751-8751
LM7R < VIA VN800 + VT8237R>
<VT8237 V-Link>
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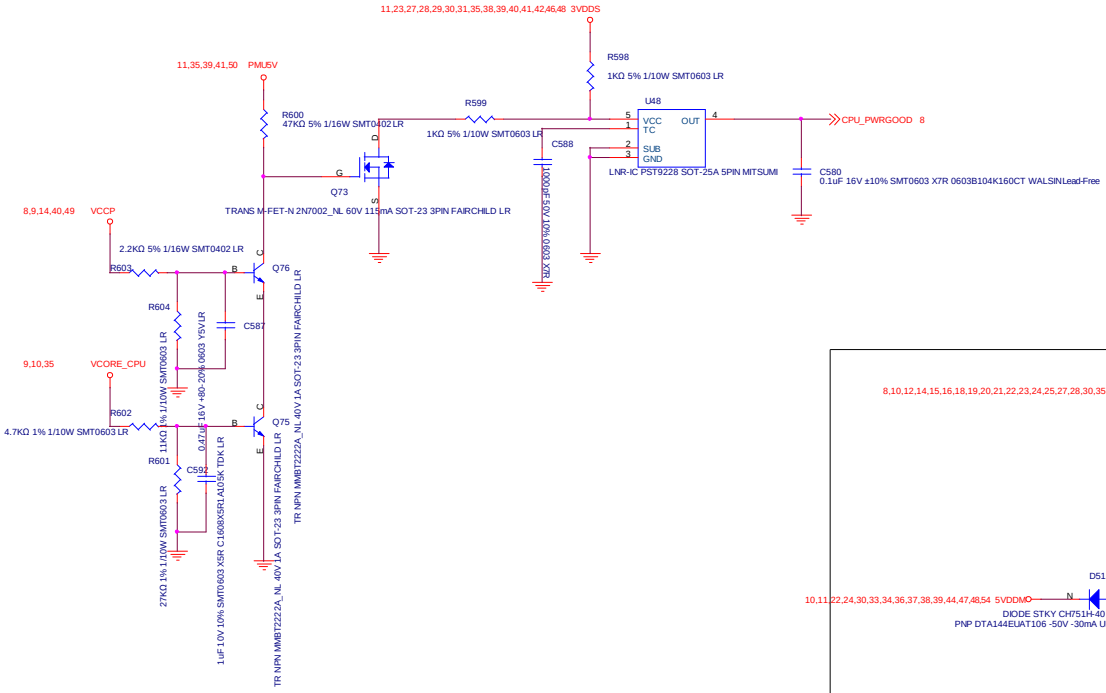
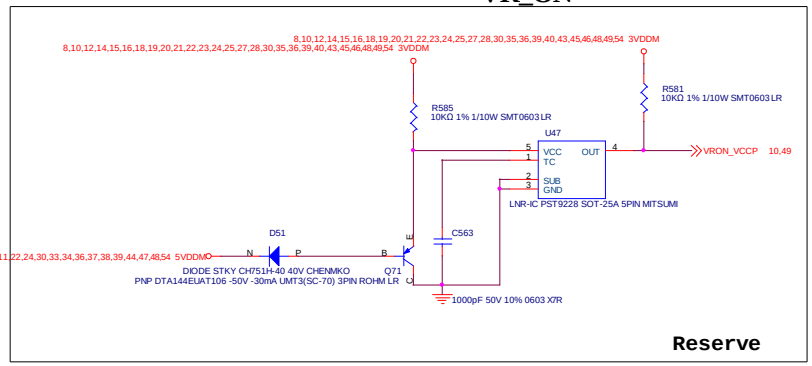
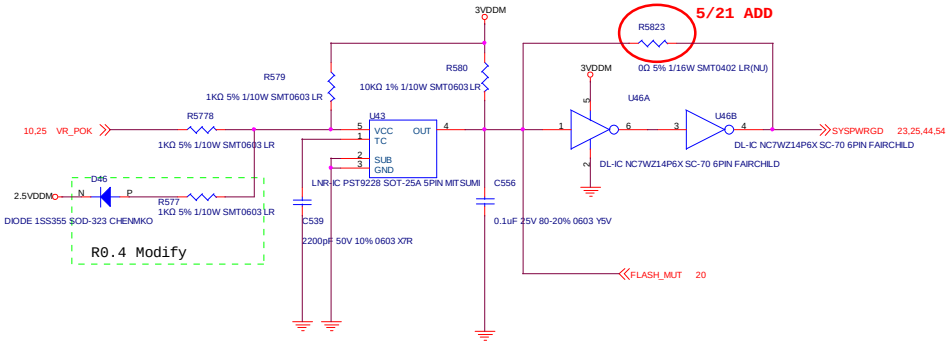
CPU POWER OK CIRCUIT

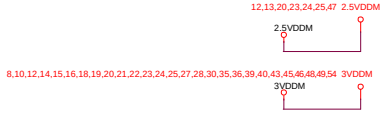


VR_ON



SYSTEM POWER OK CIRCUIT





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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <POWER Good> | Rev: 0.5

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Please close to 7411 IC

(30mil)
Please close to IEEE1394

Please close to IEEE1394 (30mil)

5/14 change

Device current :
1 port ⟶ 70mA
TPA0+ &TPA0- TWISTED LENGTH IS SAME.

Device current :
⟶
8 mils trace 15 mils space

TPA0+ &TPA0- TWISTED LENGTH IS SAME.
COMMON TRACE 50 omh
DIFFERENTIAL 110 omh

Place as close as possible to CHIP

For 4510R
T18,T19=>filter0,filter1

5/21 EMI ADD

7/5 Modify

7/5 Modify

6/17 ADD

Check with TI FAE if CLK_48 needed while suspend

5/14 change

Please closely 7411 IC

Layout Guide:
trace width: 4 mils
pair spacing: 8 mils
nominal diff .impedance: 110ohm
spacing to others: 20 mils

change to SRC1394-121 bull will

GND
TPB0-
TPB0+
GND
TPA0-
TPA0+
GND

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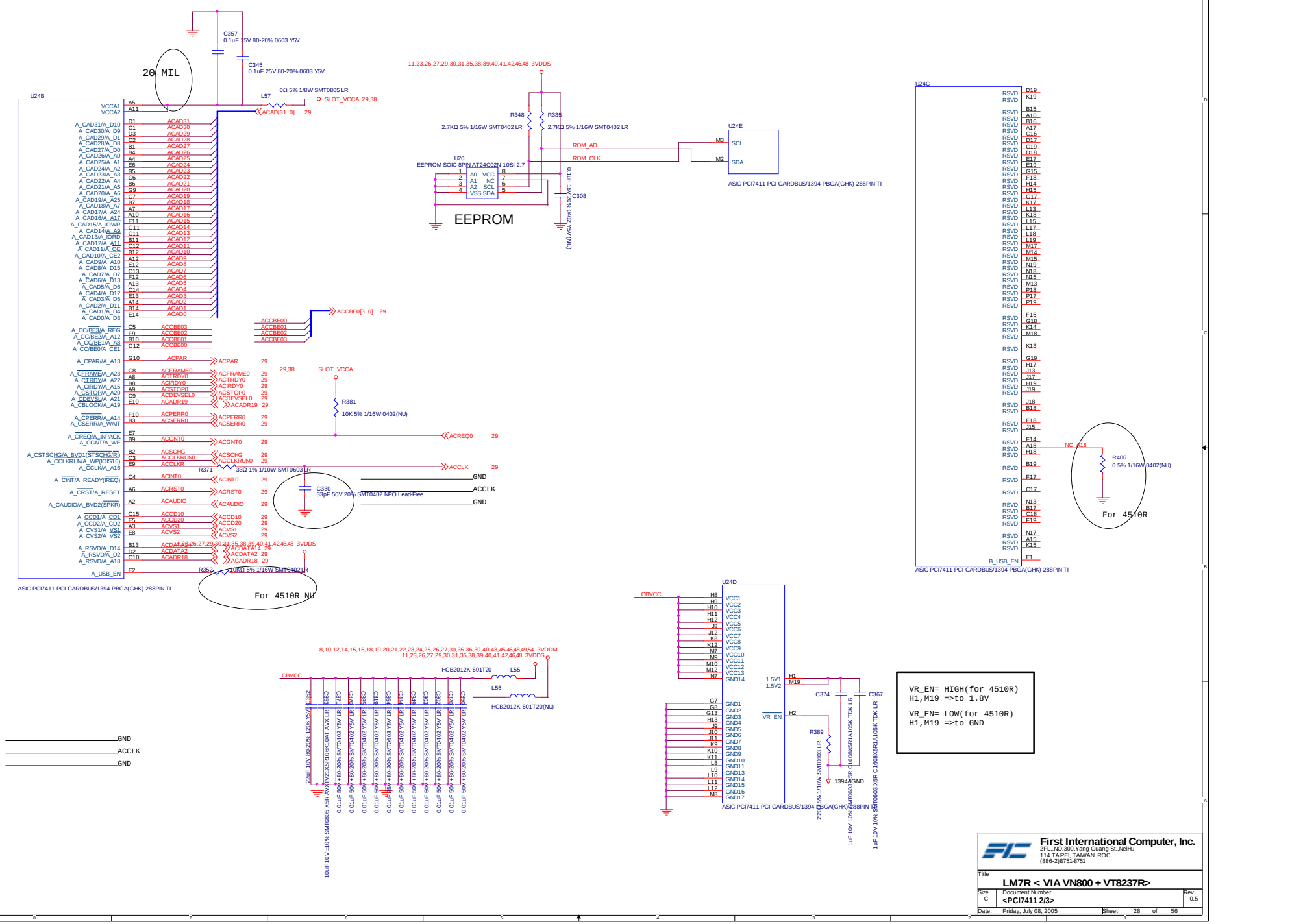
Title: LM7R < VIA VN800 + VT8237R>

Size	Document Number	Rev
C	<PCI7411 1/3>	0.5

Date: Friday, July 08, 2005 Sheet 27 of 56


U24B
ASIC PCI7411 PCI-CARDBUS/1394 PBGA(GHK) 288PIN TI
20 MIL
C357
0.1uF 25V 80-20% 0603 Y5V
C345
0.1uF 25V 80-20% 0603 Y5V
L57
0Ω 5% 1/8W SMT0805 LR
SLOT_VCCA 29,38
ACAD[31..0] 29
ACCBE0[3..0] 29
ACPAR 29
ACFRAME0 29
ACTRDY0 29
ACIRDY0 29
ACSTOP0 29
ACDEVSEL0 29
ACADR19 29
ACPERR0 29
ACSERR0 29
ACREQ0 29
ACGNT0 29
ACSCHG 29
ACCLKRUN0 29
ACCLK 29
ACINT0 29
ACRST0 29
ACAUDIO 29
ACCD10 29
ACCD20 29
ACVS1 29
ACVS2 29
ACDATA14 29
ACDATA2 29
ACADR18 29
R371 33Ω 1% 1/10W SMT0603 LR
R352 10KΩ 5% 1/16W SMT0402 LR
For 4510R NU
C330
33pF 50V 20% SMT0402 NPO Lead-Free
R381
10K 5% 1/16W 0402(NU)
GND
ACCLK
GND
11,23,26,27,29,30,31,35,38,39,40,41,42,46,48 3VDDS
U20
EEPROM SOIC 8PIN AT24C02N-10SI-2.7
EEPROM
R348
2.7KΩ 5% 1/16W SMT0402 LR
R335
2.7KΩ 5% 1/16W SMT0402 LR
ROM_AD
ROM_CLK
C308
0.1uF 16V 10% 0402 Y5V (NU)
U24E
SCL
SDA
ASIC PCI7411 PCI-CARDBUS/1394 PBGA(GHK) 288PIN TI
U24C
ASIC PCI7411 PCI-CARDBUS/1394 PBGA(GHK) 288PIN TI
NC_418
R406
0 5% 1/16W 0402(NU)
For 4510R
8,10,12,14,15,16,18,19,20,21,22,23,24,25,26,27,30,35,36,39,40,43,45,46,48,49,54 3VDDM
11,23,26,27,29,30,31,35,38,39,40,41,42,46,48 3VDDS
CBVCC
HCB2012K-601T20
L55
L56
HCB2012K-601T20(NU)
U24D
ASIC PCI7411 PCI-CARDBUS/1394 PBGA(GHK) 288PIN TI
1.5V1
1.5V2
VR_EN
H1
M19
H2
C374
C367
R389
2.2Ω 5% 1/10W SMT0603
1394AGND
1uF 10V 10% SMT0603 X5R C1608X5R1A105K TDK LR
VR_EN= HIGH(for 4510R)
H1,M19 =>to 1.8V
VR_EN= LOW(for 4510R)
H1,M19 =>to GND
GND
ACCLK
GND
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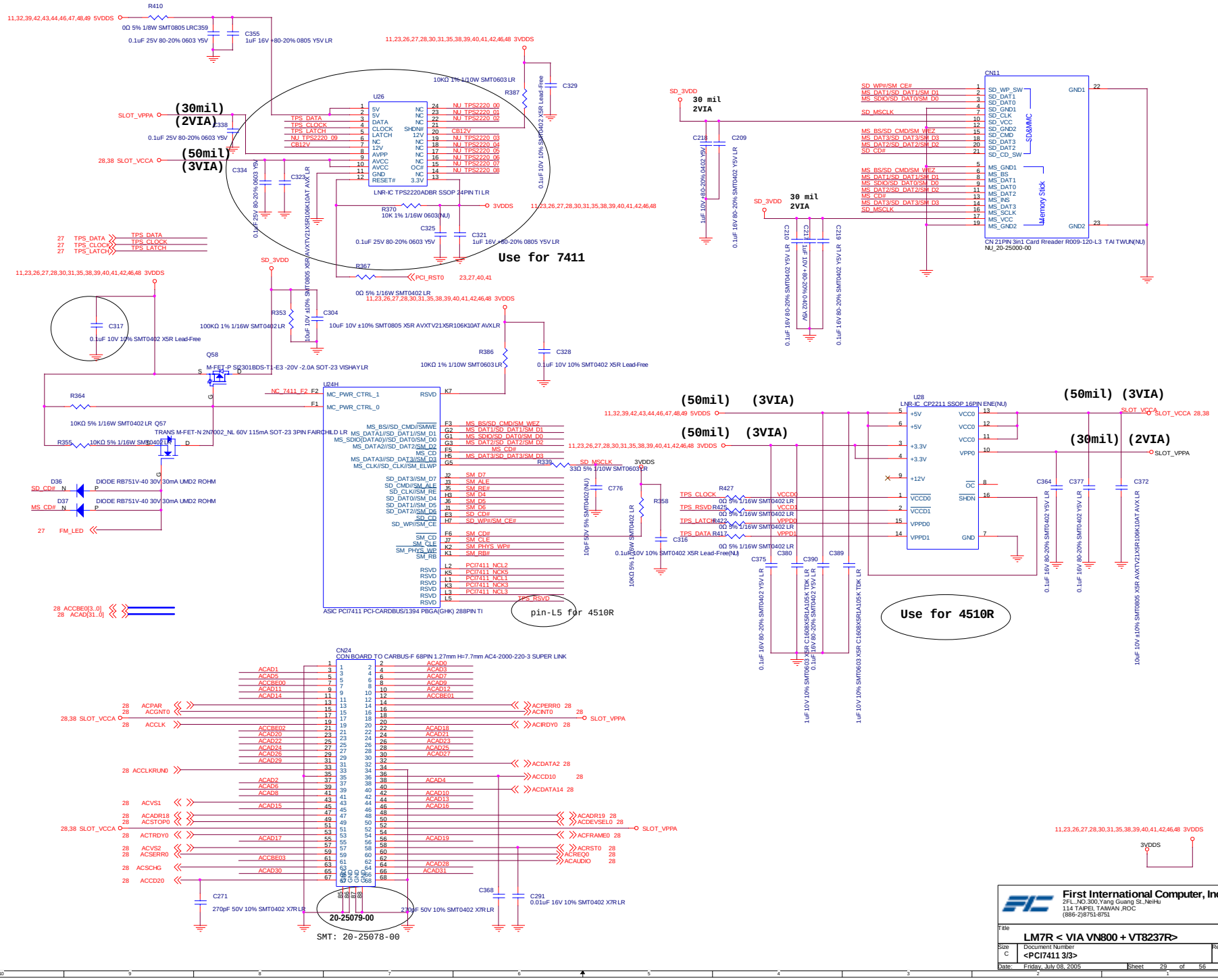
Title
LM7R < VIA VN800 + VT8237R>
Size C
Document Number
<PCI7411 2/3>
Rev 0.5
Date: Friday, July 08, 2005
Sheet 28 of 56


Use for 7411
Use for 4510R
pin-L5 for 4510R
(30mil) (2VIA)
(50mil) (3VIA)
30 mil 2VIA
20-25079-00
SMT: 20-25078-00
First International Computer, Inc.
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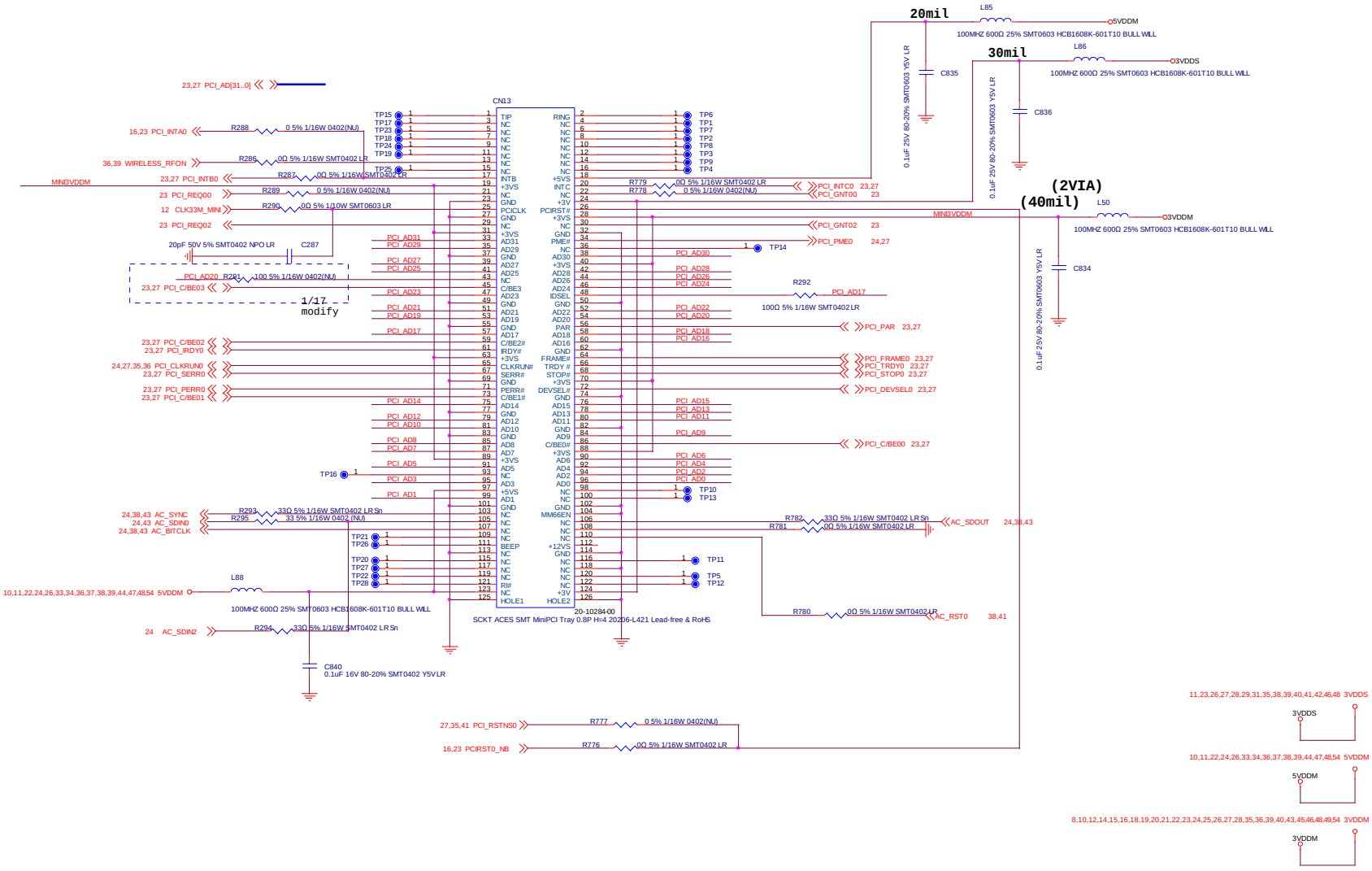
<PCI7411 3/3>
Friday, July 08, 2005

TYPE III MODEM / LAN CONNECTOR



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Size: C	Document Number: <Mini-PCI>	Rev: 0.5
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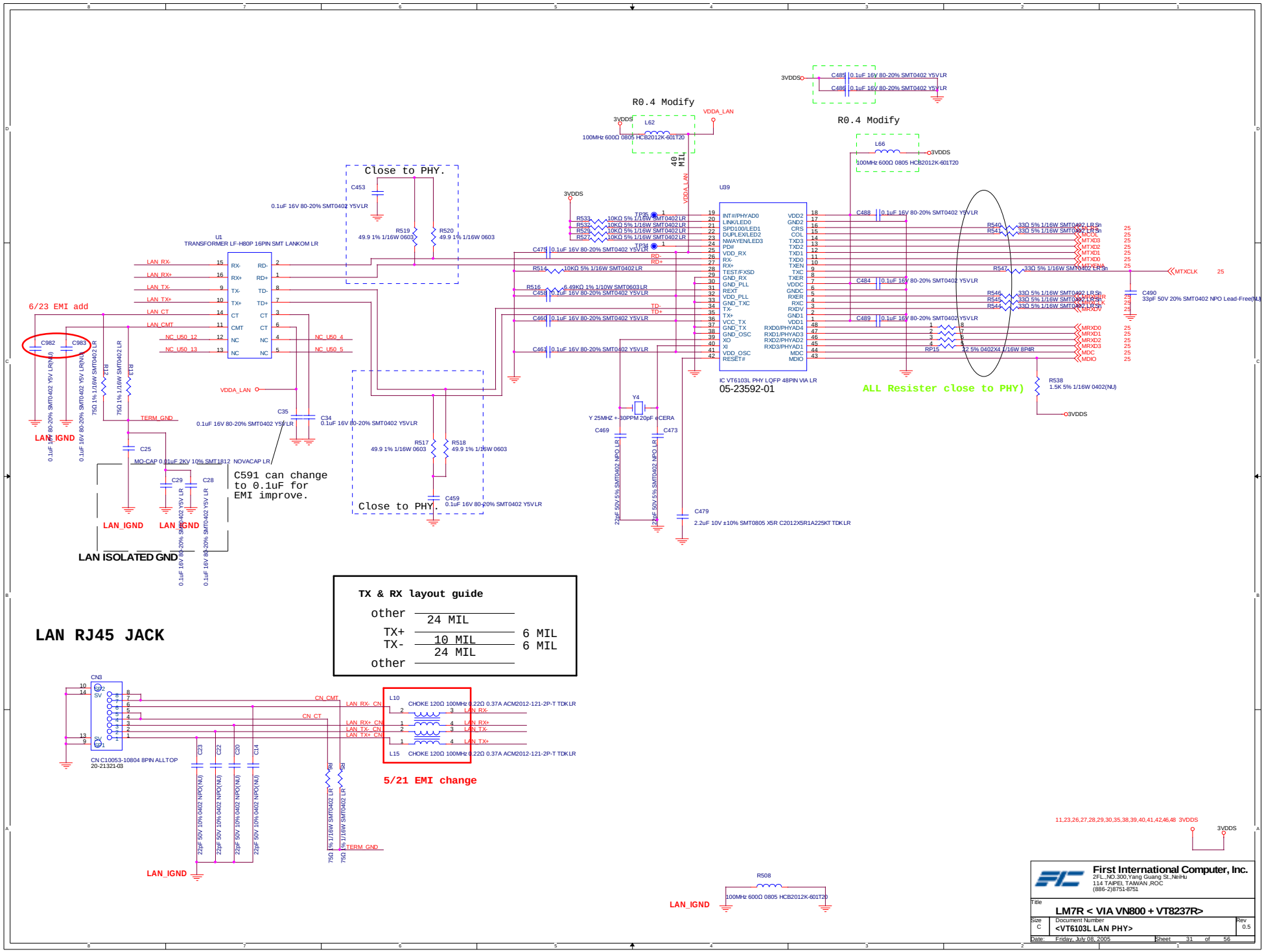
R0.4 Modify
R0.4 Modify
Close to PHY.
Close to PHY.
6/23 EMI add
C591 can change to 0.1uF for EMI improve.
ALL Resister close to PHY)
IC VT6103L PHY LQFP 48PIN VIA LR
05-23592-01
LAN RJ45 JACK
TX & RX layout guide
other 24 MIL
TX+ 10 MIL 6 MIL
TX- 24 MIL 6 MIL
other
5/21 EMI change
LAN ISOLATED GND
LAN_IGND
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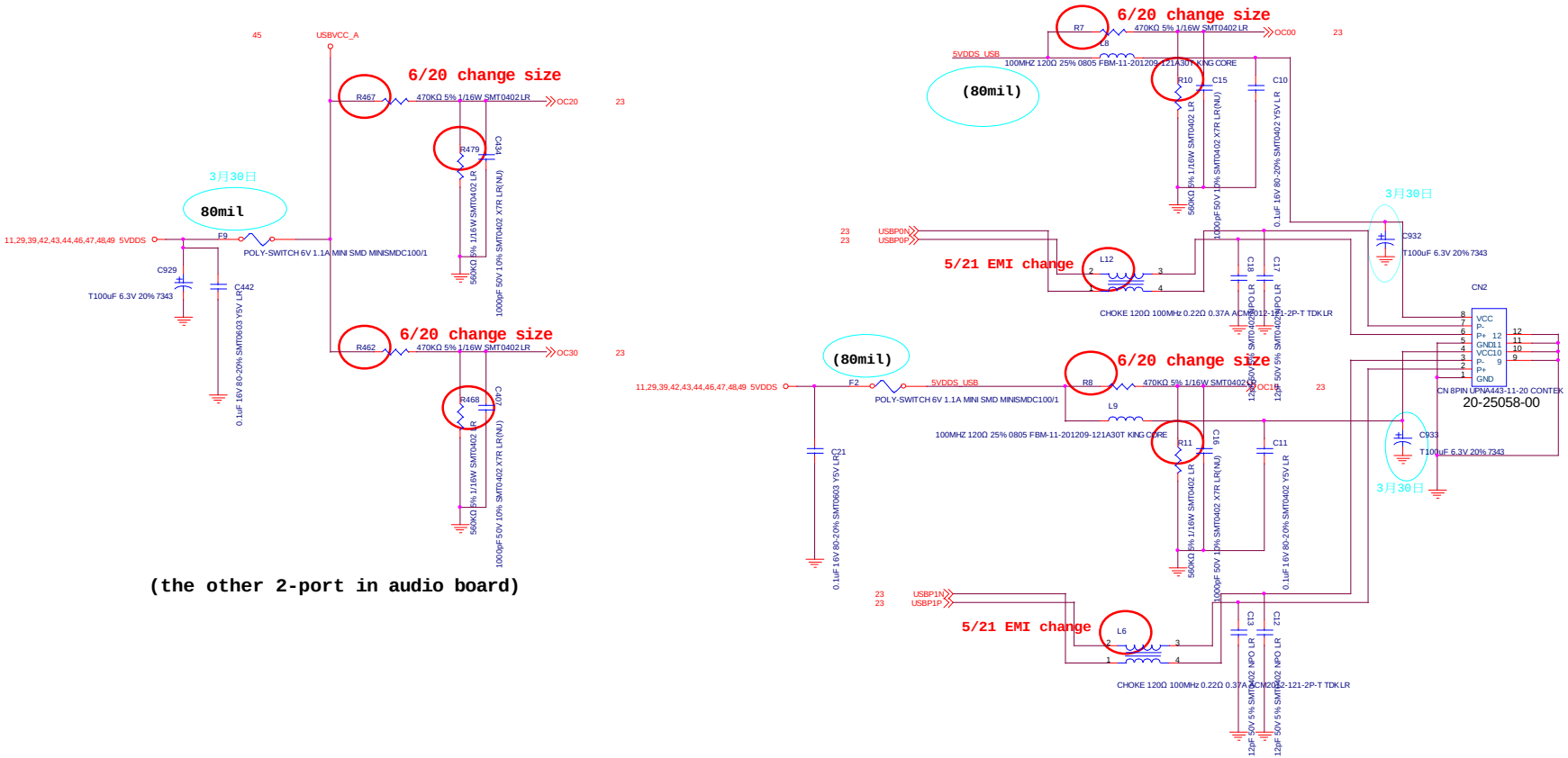
<VT6103L LAN PHY>
Date: Friday, July 08, 2005
Sheet 31 of 56



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Title: **LM7R < VIA VN800 + VT8237R>**

Size	Document Number	Rev
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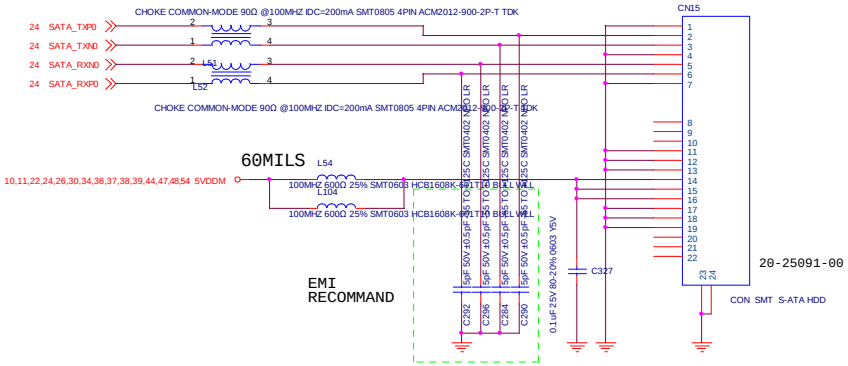
SATA Layout Note:

MS or SL:

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

NOTE

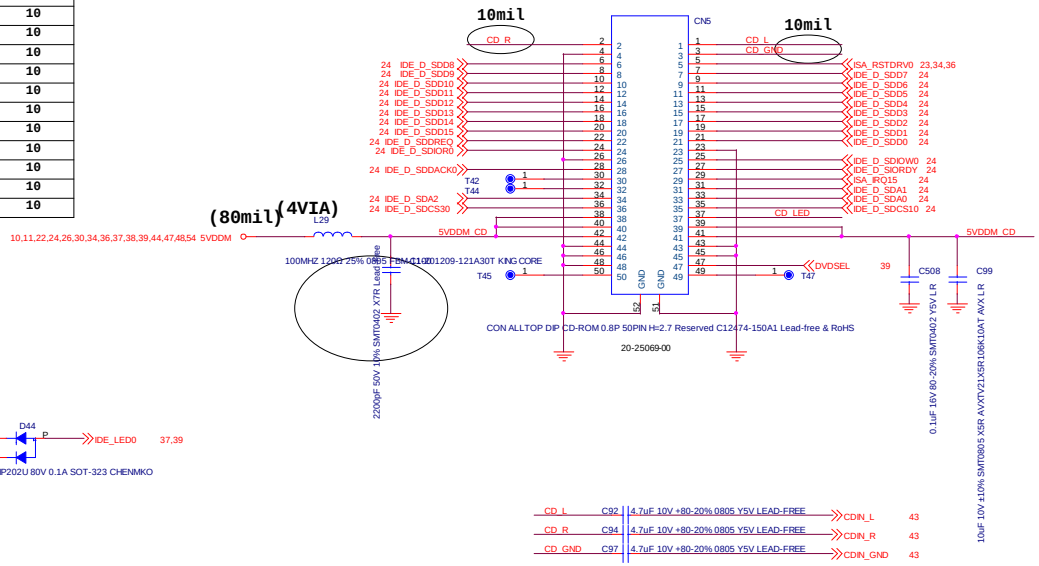
SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

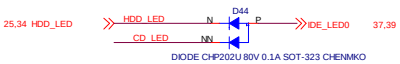


IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

CDROM CNN





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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <IDE connector> | Rev: 0.5

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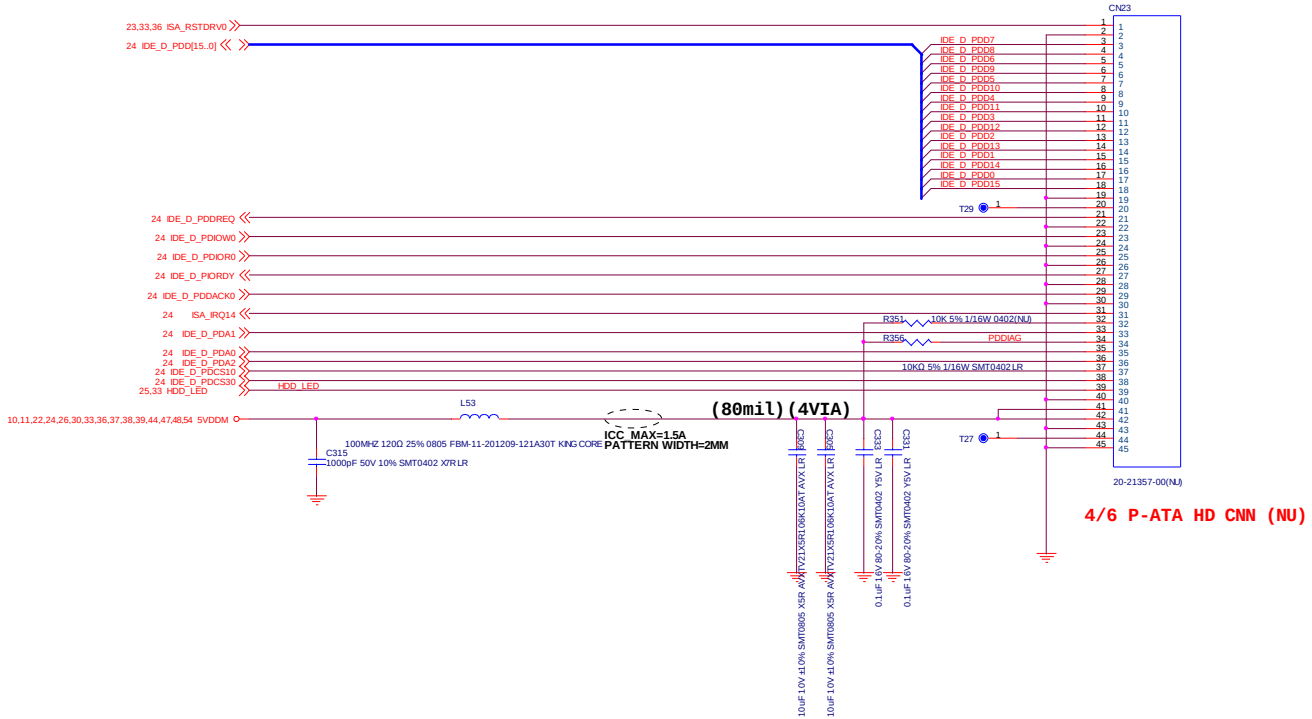
IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10

PATA-HDD SWITCH CNN(option)



4/6 P-ATA HD CNN (NU)

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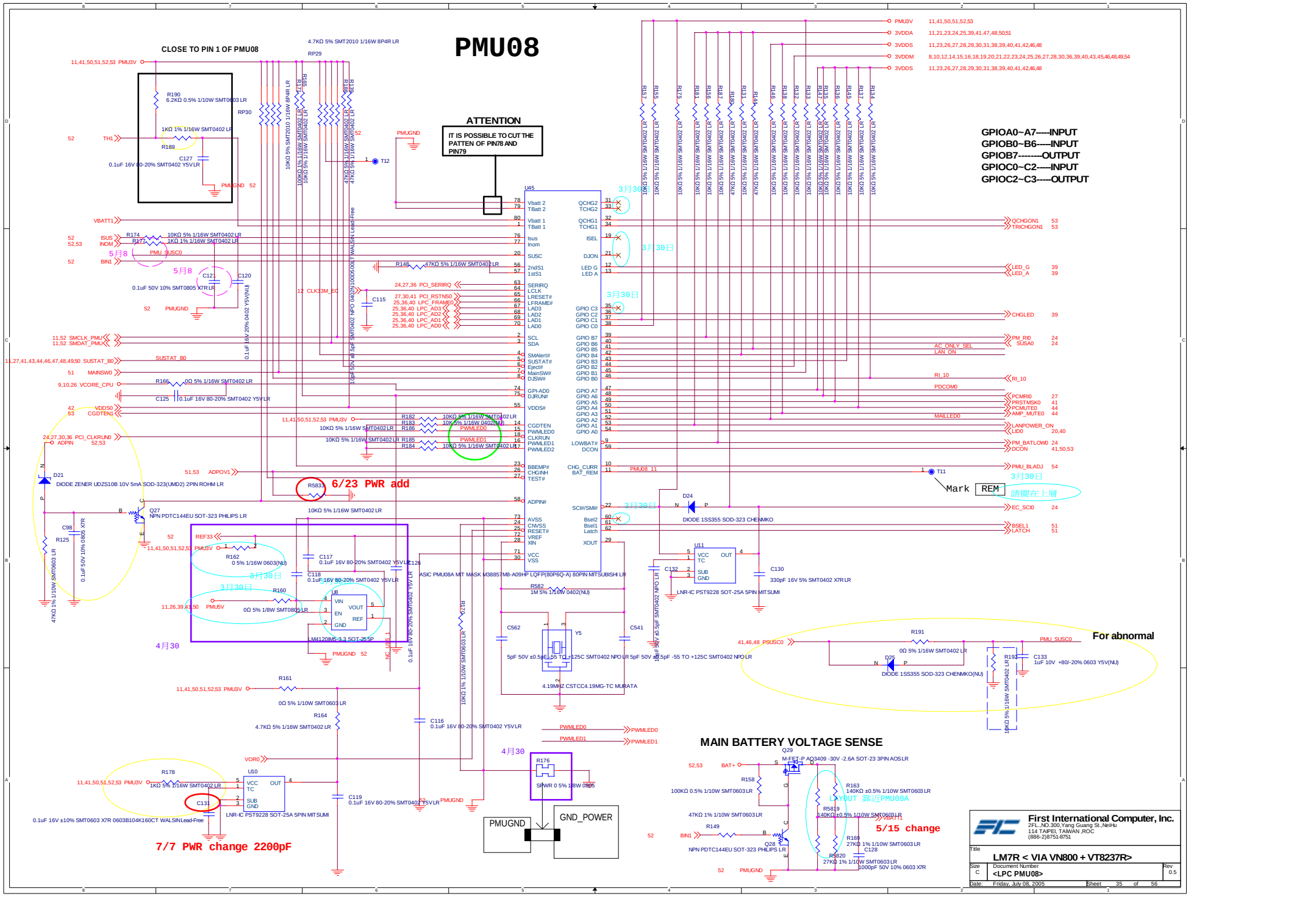
PMU08


CLOSE TO PIN 1 OF PMU08
4.7KΩ 5% SMT2010 1/16W 8P4R LR
RP29
RP30
R190 6.2KΩ 0.5% 1/10W SMT0603 LR
1KΩ 1% 1/16W SMT0402 LR
R189
C127 0.1uF 16V ±0-20% SMT0402 Y5V LR
PMUGND
ATTENTION
IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79
U45
GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT
PMU3V 11,41,50,51,52,53
3VDDA 11,21,23,24,25,39,41,47,48,50,51
3VDDS 11,23,26,27,28,29,30,31,38,39,40,41,42,46,48
3VDDM 8,10,12,14,15,16,18,19,20,21,22,23,24,25,26,27,28,30,36,39,40,43,45,46,48,49,54
3VDDS 11,23,26,27,28,29,30,31,38,39,40,41,42,46,48
Mark
REM
請擺在上層
6/23 PWR add
7/7 PWR change 2200pF
5/15 change
MAIN BATTERY VOLTAGE SENSE
For abnormal
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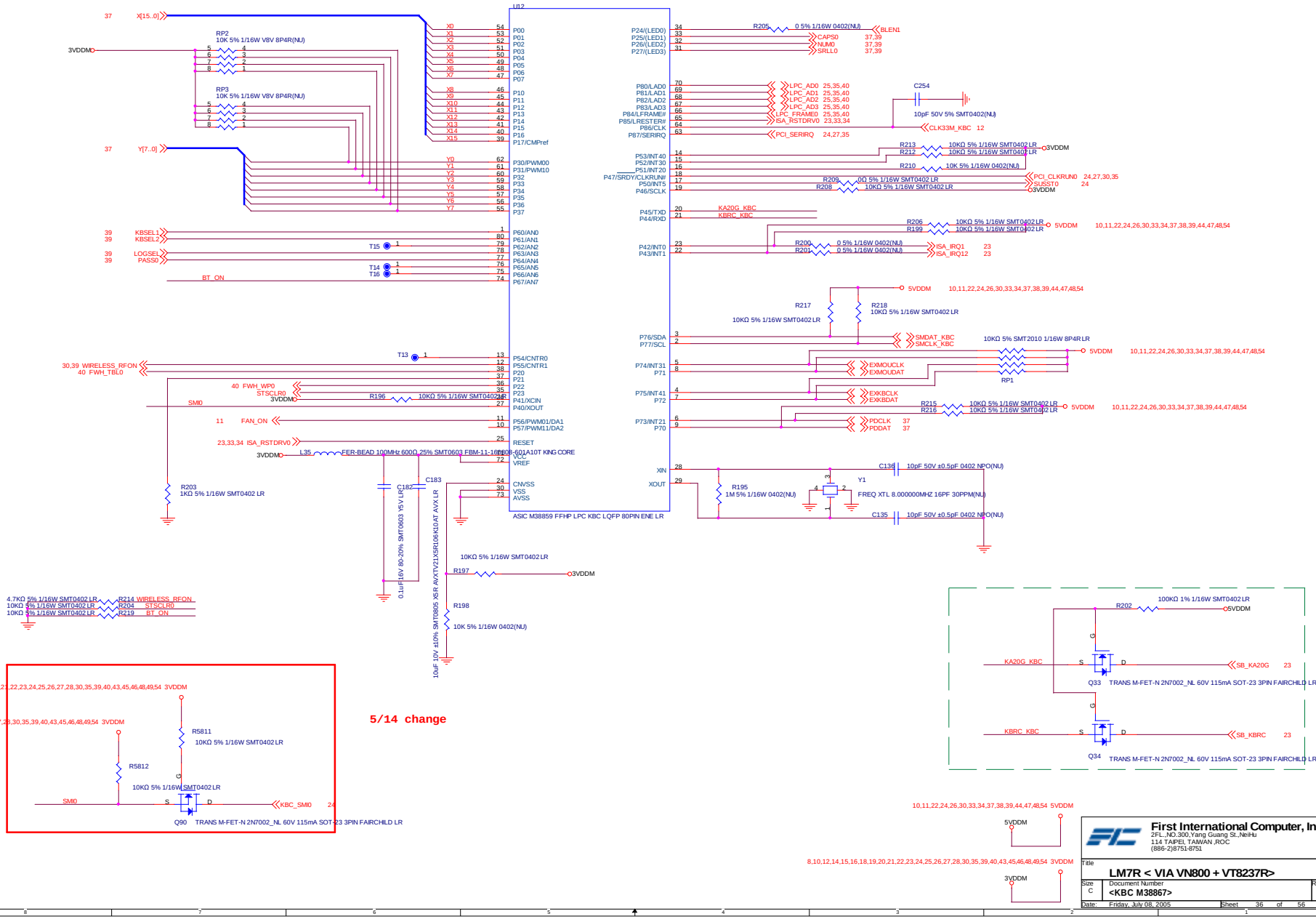
LM7R < VIA VN800 + VT8237R>
<LPC PMU08>
Friday, July 08, 2005


U12
ASIC M38859 FFHP LPC KBC LQFP 80PIN ENE LR
RP2
10K 5% 1/16W V8V 8P4R(NU)
RP3
10K 5% 1/16W V8V 8P4R(NU)
R205 0 5% 1/16W 0402(NU)
C254
10pF 50V 5% SMT0402(NU)
R213 10KΩ 5% 1/16W SMT0402 LR
R212 10KΩ 5% 1/16W SMT0402 LR
R210 10K 5% 1/16W 0402(NU)
R209 0Ω 5% 1/16W SMT0402 LR
R208 10KΩ 5% 1/16W SMT0402 LR
R206 10KΩ 5% 1/16W SMT0402 LR
R199 10KΩ 5% 1/16W SMT0402 LR
R200 0 5% 1/16W 0402(NU)
R201 0 5% 1/16W 0402(NU)
R217 10KΩ 5% 1/16W SMT0402 LR
R218 10KΩ 5% 1/16W SMT0402 LR
SMT2010 1/16W 8P4R LR
RP1
R215 10KΩ 5% 1/16W SMT0402 LR
R216 10KΩ 5% 1/16W SMT0402 LR
R196 10KΩ 5% 1/16W SMT0402 LR
R203 1KΩ 5% 1/16W SMT0402 LR
L35 FER-BEAD 100MHz 600Ω 25% SMT0603 FBM-11-160808-601A10T KING CORE
C182
C183
0.1uF 16V 80-20% SMT0603 X5V LR
C136 10pF 50V ±0.5pF 0402 NPO(NU)
C135 10pF 50V ±0.5pF 0402 NPO(NU)
Y1
FREQ XTL 8.000000MHZ 16PF 30PPM(NU)
R195 1M 5% 1/16W 0402(NU)
R197 10KΩ 5% 1/16W SMT0402 LR
R198 10K 5% 1/16W 0402(NU)
10uF 10V ±10% SMT0805 X5R AVX TVZ1X5R106K10AT AVX LR
4.7KΩ 5% 1/16W SMT0402 LR
10KΩ 5% 1/16W SMT0402 LR
10KΩ 5% 1/16W SMT0402 LR
R214 WIRELESS_RFON
R204 STSCLR0
R219 BT_ON
R5811 10KΩ 5% 1/16W SMT0402 LR
R5812 10KΩ 5% 1/16W SMT0402 LR
Q90 TRANS M-FET-N 2N7002_NL 60V 115mA SOT-23 3PIN FAIRCHILD LR
5/14 change
R202 100KΩ 1% 1/16W SMT0402 LR
Q33 TRANS M-FET-N 2N7002_NL 60V 115mA SOT-23 3PIN FAIRCHILD LR
Q34 TRANS M-FET-N 2N7002_NL 60V 115mA SOT-23 3PIN FAIRCHILD LR
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LM7R < VIA VN800 + VT8237R>
<KBC M38867>
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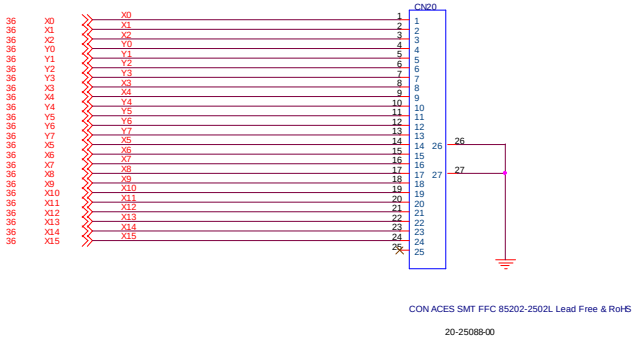
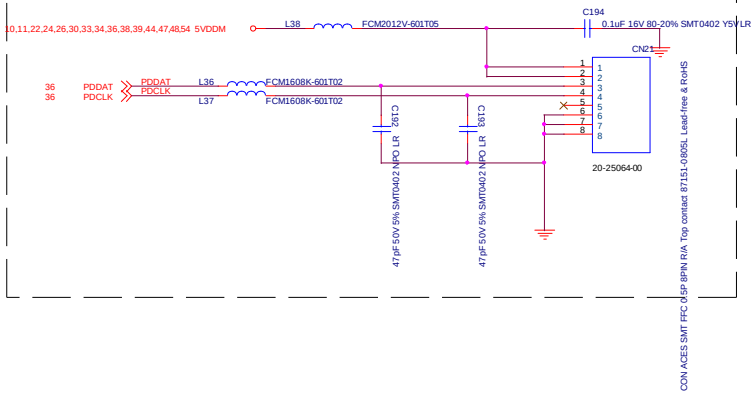
INT KB CNN



CON ACES SMT FFC 85202-2502L Lead Free & RoHS

20-25088-00

GLIDE PAD CONNECTOR

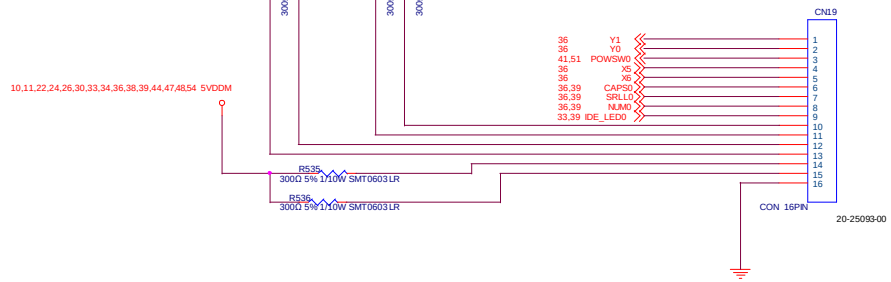


39 WIRELESS_RFON1
39 CHG_LED1
39 LED_AMBER
39 LED_GREEN

6月15

R888 300Ω 5% 1/10W SMT0603 LR
R889 150Ω 1% 1/10W SMT0603 LR
R892 300Ω 5% 1/10W SMT0603 LR
R884 300Ω 5% 1/10W SMT0603 LR

switch board con



20-25093-00

11,23,26,27,28,29,30,31,35,38,39,40,41,42,46,48 3VDDS
3VDDS
8,10,12,14,15,16,18,19,20,21,22,23,24,25,26,27,28,30,35,36,39,40,43,45,46,48,49,54 3VDDM
3VDDM

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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <INT K/B /GP/SW CNN> | Rev: 0.5

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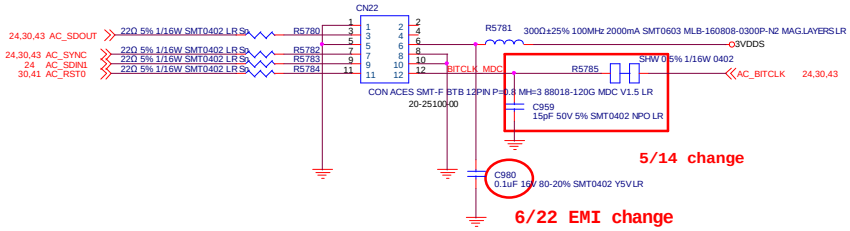
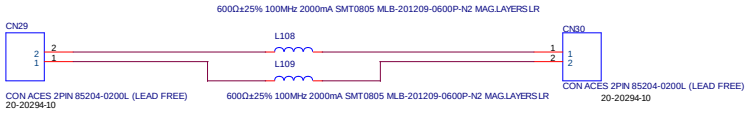
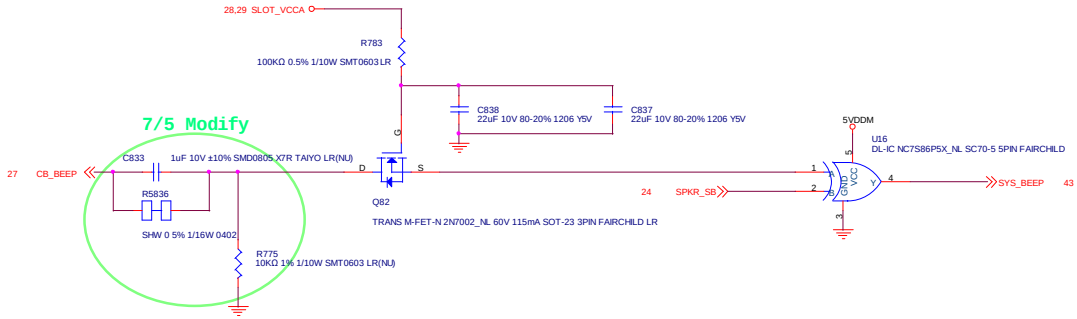
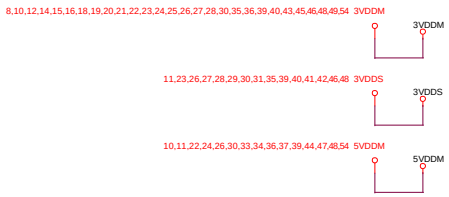
MDC 1.5 CNN









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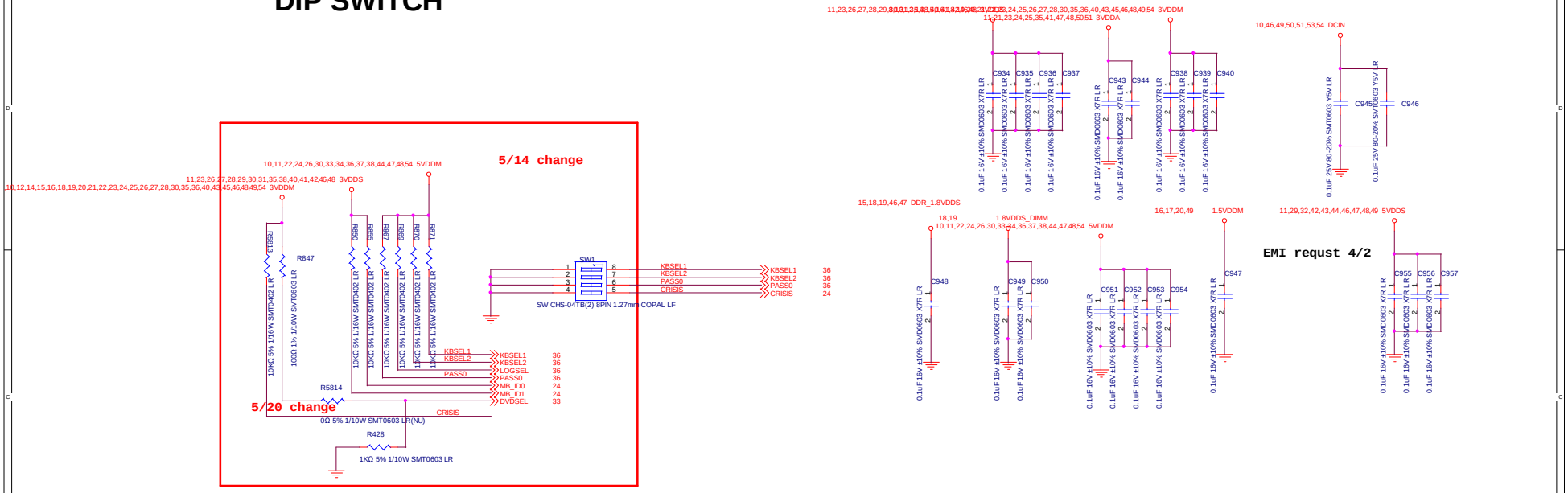
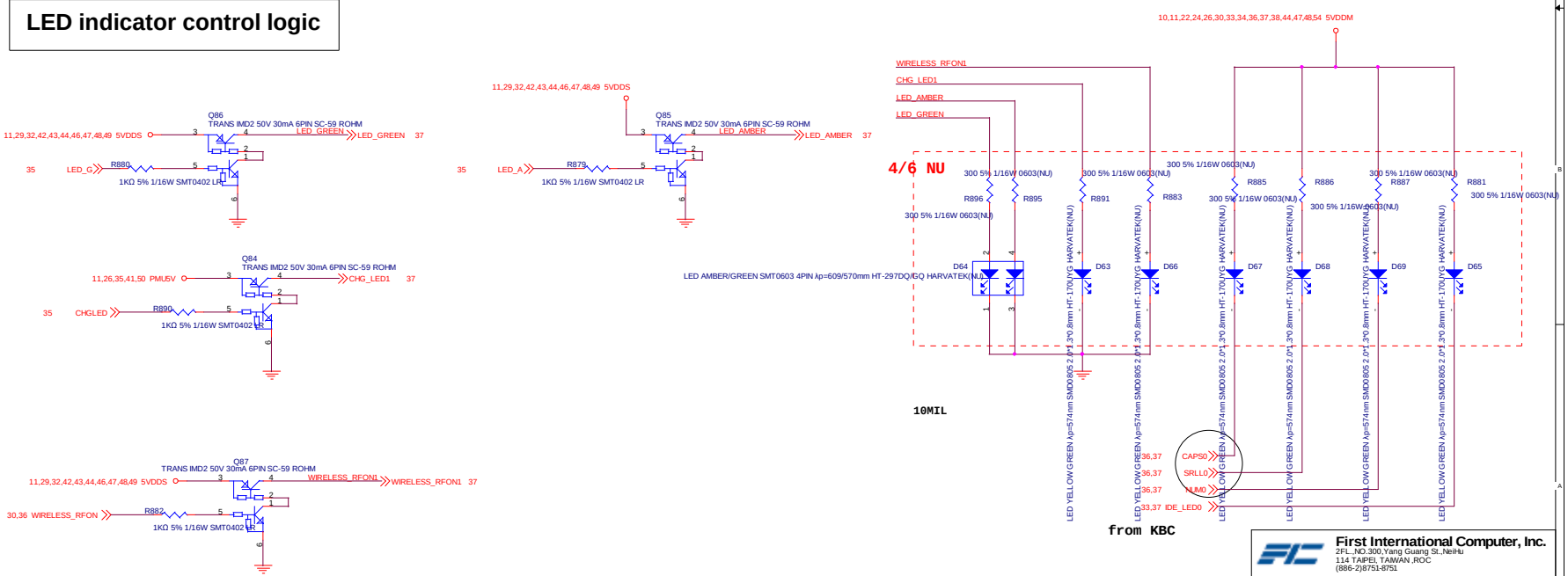
Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <MDC CNN>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 38 of 56	

DIP SWITCH



LED indicator control logic



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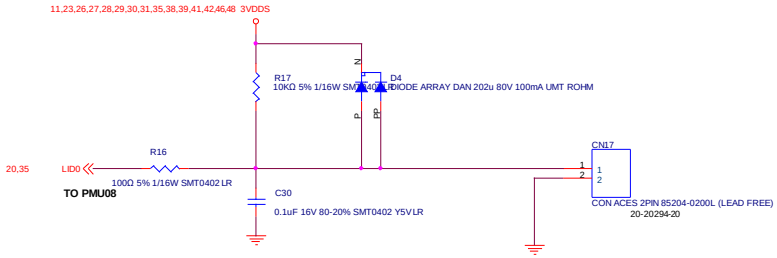
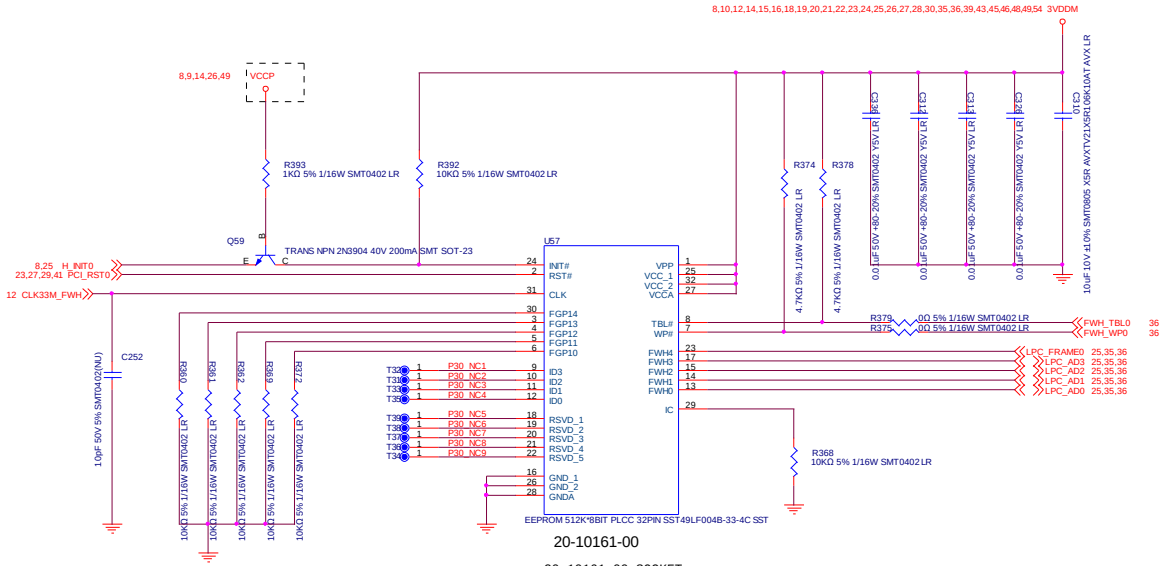
Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <DIP SW/ LED>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 39 of 56	

LID Switch



4M FLASH ROM



20-10161-00

20-10161-00 SOCKET

03-10119-15 Atmel Flash

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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <LID SW/ BIOS> | Rev: 0.5

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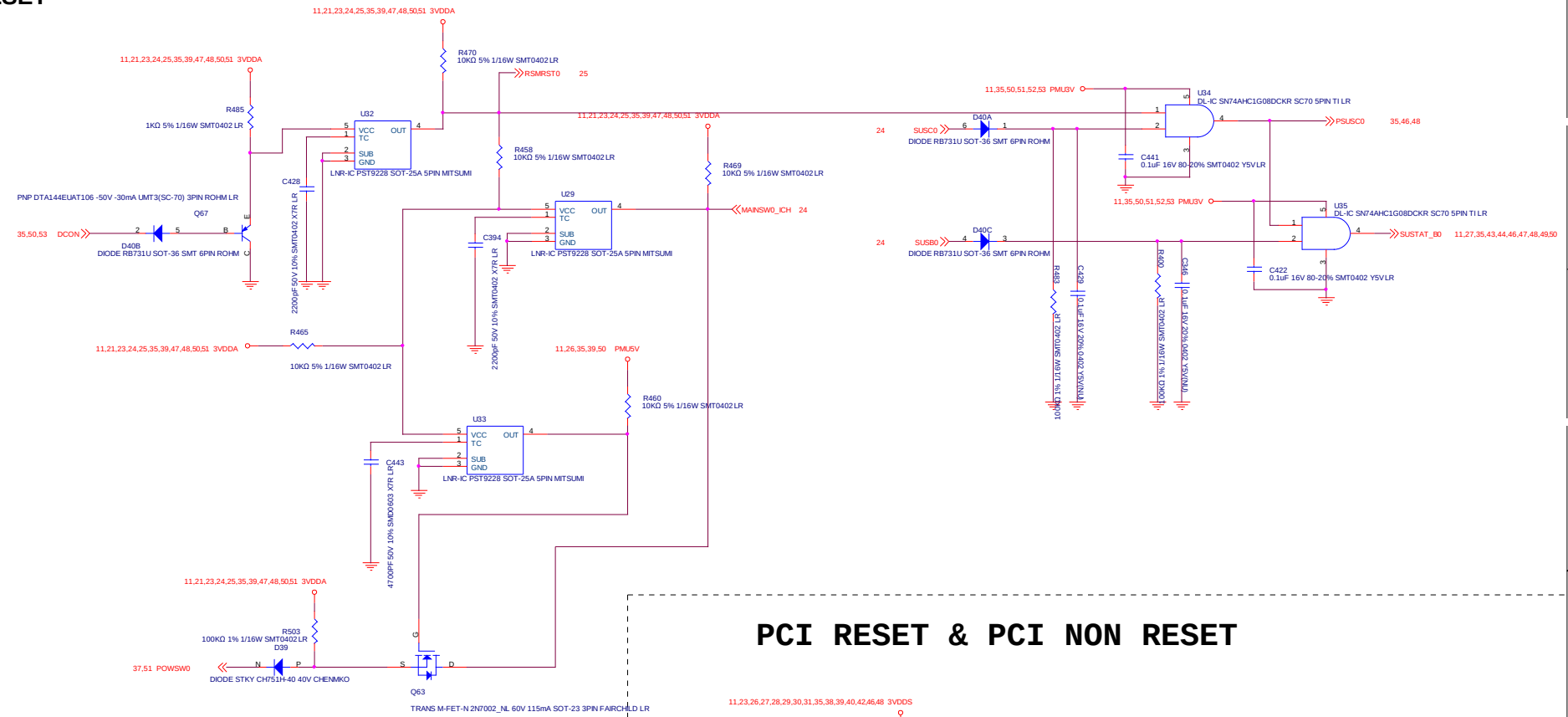
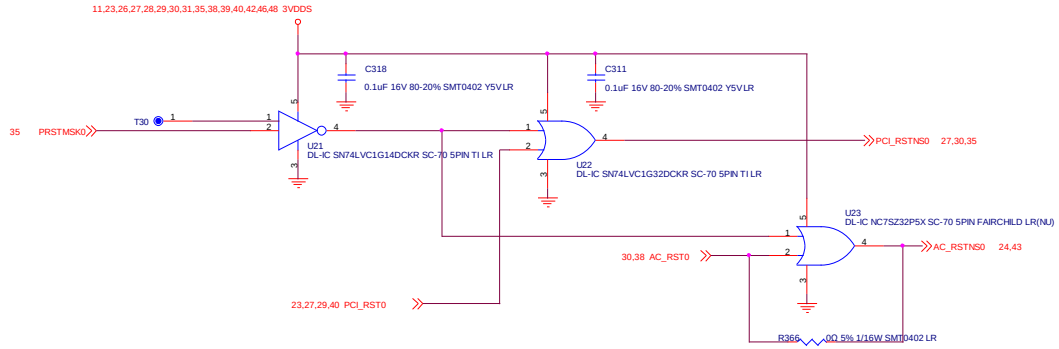
RESUME RESET



PCI RESET & PCI NON RESET



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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <Reset Circuit> | Rev: 0.5

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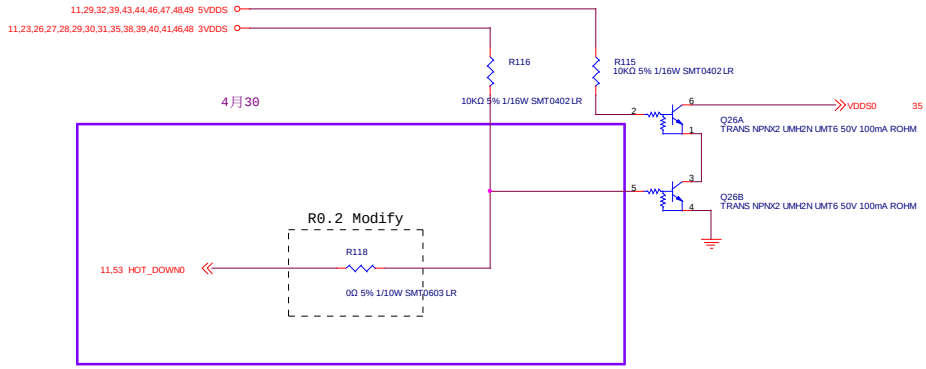
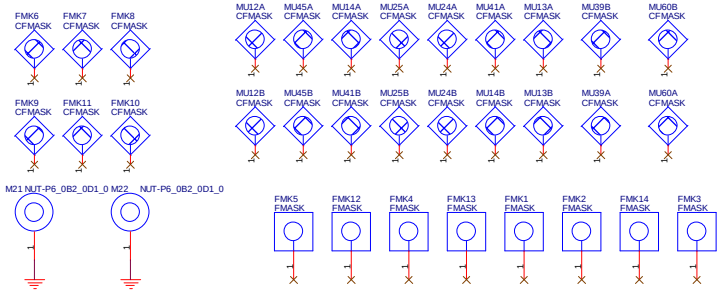
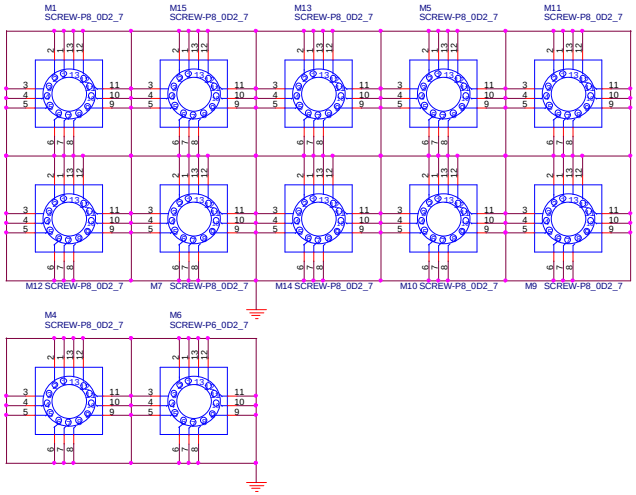
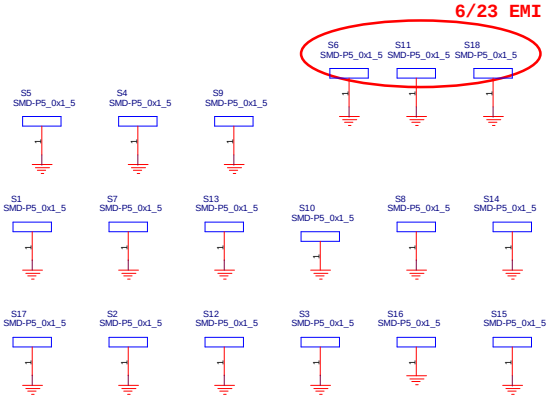
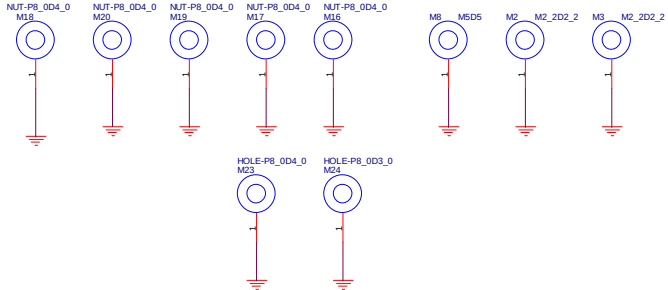




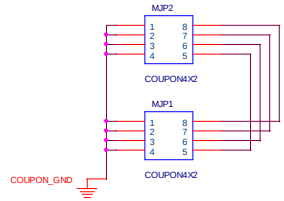


6/23 EMI change





COUPON4X2



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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <OVP CKT> | Rev: 0.5

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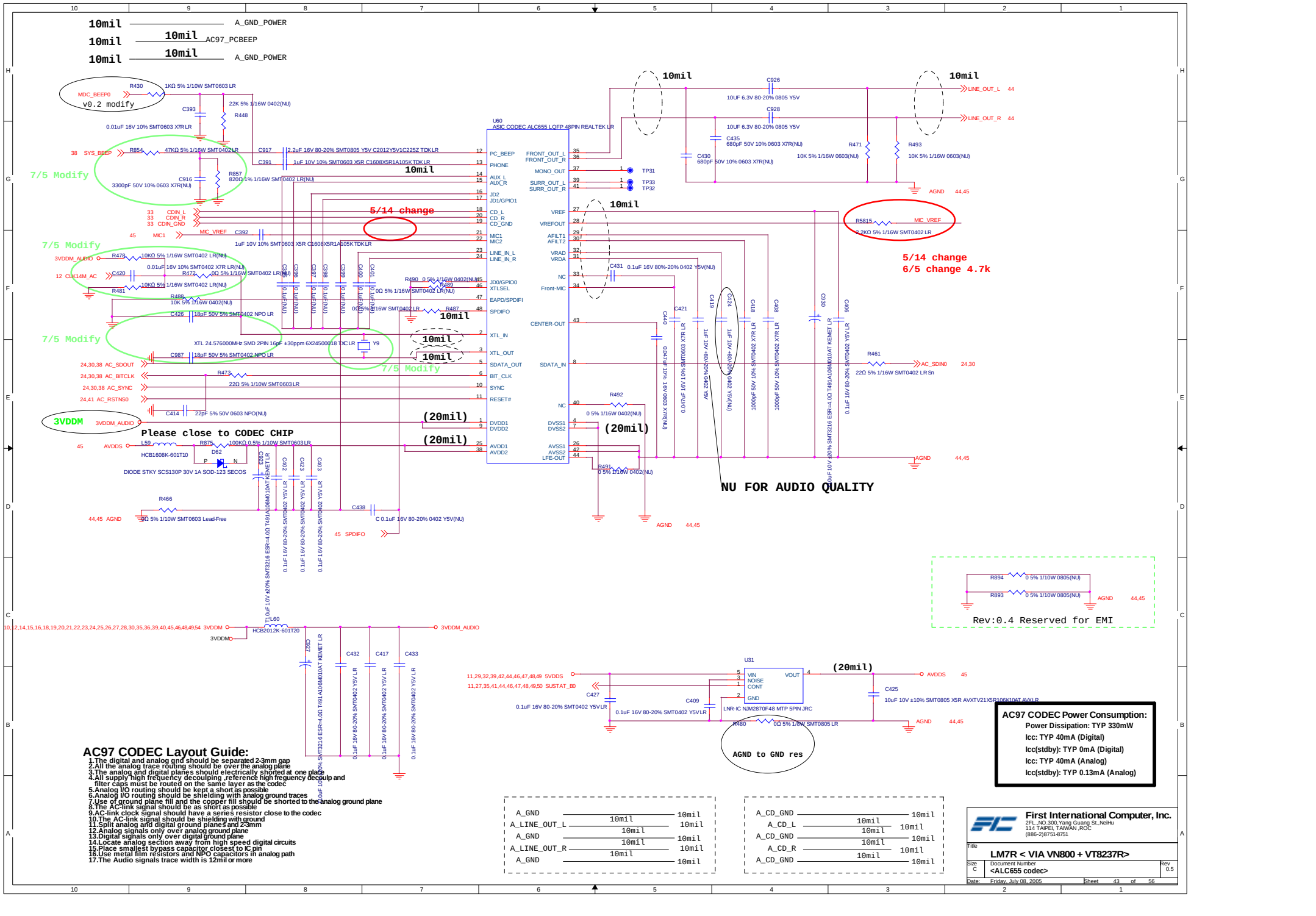
10mil A_GND_POWER
10mil 10mil AC97_PCBEEP
10mil 10mil A_GND_POWER
U60
ASIC CODEC ALC655 LQFP 48PIN REALTEK LR
v0.2 modify
7/5 Modify
5/14 change
6/5 change 4.7k
NU FOR AUDIO QUALITY
Please close to CODEC CHIP
3VDDM
AGND to GND res
Rev:0.4 Reserved for EMI
U31
LNR-IC NJM2870F48 MTP 5PIN JRC
AC97 CODEC Layout Guide:
1.The digital and analog gnd should be separated 2-3mm gap
2.All the analog trace routing should be over the analog plane
3.The analog and digital planes should electrically shorted at one place
4.All supply high frequency decoupling ,reference high freguency decouip and filter caps must be routed on the same layer as the codec
5.Analog I/O routing should be kept a short as possible
6.Analog I/O routing should be shielding with analog ground traces
7.Use of ground plane fill and the copper fill should be shorted to the analog ground plane
8.The AC-link signal should be as short as possible
9.AC-link clock signal should have a series resistor close to the codec
10.The AC-link signal should be shielding with ground
11.Split analog and digital ground planes and 2-3mm
12.Analog signals only over analog ground plane
13.Digital signals only over digital ground plane
14.Locate analog section away from high speed digital circuits
15.Place smallest bypass capacitor closest to IC pin
16.Use metal film resistors and NPO capacitors in analog path
17.The Audio signals trace width is 12mil or more
AC97 CODEC Power Consumption:
Power Dissipation: TYP 330mW
Icc: TYP 40mA (Digital)
Icc(stdby): TYP 0mA (Digital)
Icc: TYP 40mA (Analog)
Icc(stdby): TYP 0.13mA (Analog)
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LM7R < VIA VN800 + VT8237R>
<ALC655 codec>
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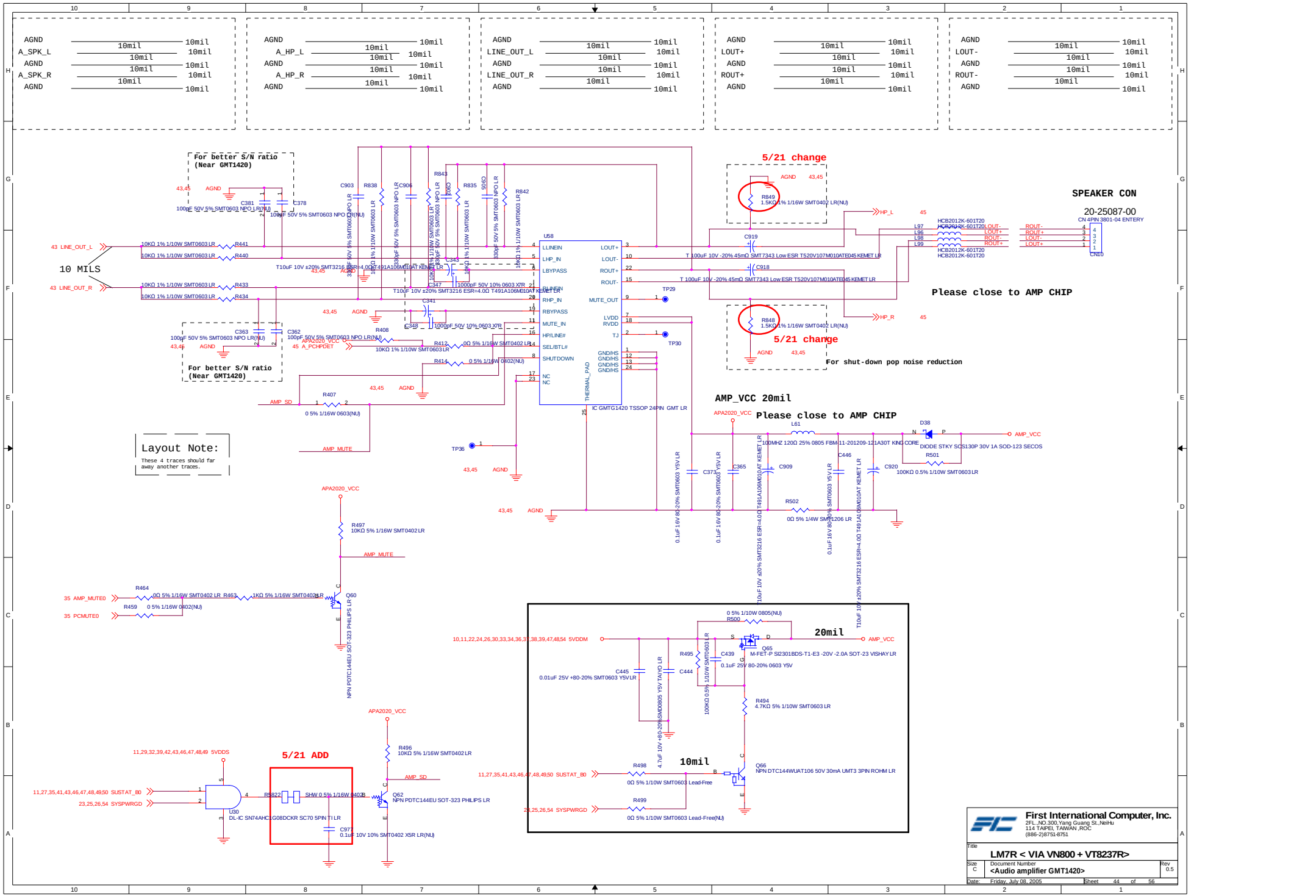
AGND 10mil 10mil
A_SPK_L 10mil 10mil
AGND 10mil 10mil
A_SPK_R 10mil 10mil
AGND 10mil 10mil
AGND 10mil 10mil
A_HP_L 10mil 10mil
AGND 10mil 10mil
A_HP_R 10mil 10mil
AGND 10mil 10mil
AGND 10mil 10mil
LINE_OUT_L 10mil 10mil
AGND 10mil 10mil
LINE_OUT_R 10mil 10mil
AGND 10mil 10mil
AGND 10mil 10mil
LOUT+ 10mil 10mil
AGND 10mil 10mil
ROUT+ 10mil 10mil
AGND 10mil 10mil
AGND 10mil 10mil
LOUT- 10mil 10mil
AGND 10mil 10mil
ROUT- 10mil 10mil
AGND 10mil 10mil
For better S/N ratio (Near GMT1420)
For better S/N ratio (Near GMT1420)
5/21 change
5/21 change
SPEAKER CON
20-25087-00
CN 4PIN 3801-04 ENTERY
Please close to AMP CHIP
For shut-down pop noise reduction
10 MILS
AMP_VCC 20mil
Please close to AMP CHIP
IC GMTG1420 TSSOP 24PIN GMT LR
Layout Note:
These 4 traces should far away another traces.
5/21 ADD
20mil
10mil
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LM7R < VIA VN800 + VT8237R>
<Audio amplifier GMT1420>
Size C
Rev 0.5
Date: Friday, July 08, 2005
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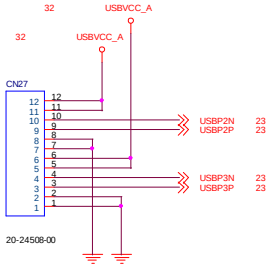
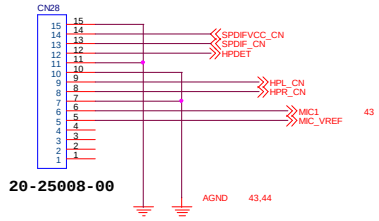
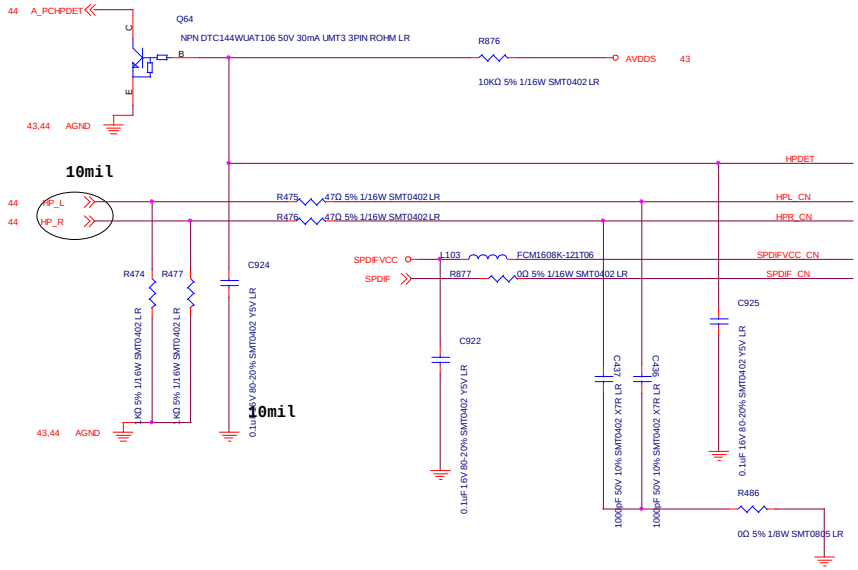


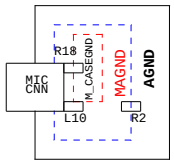
5/19 ME change , 20-24508-10 LF



5/19 ME change , 20-25008-10 LF

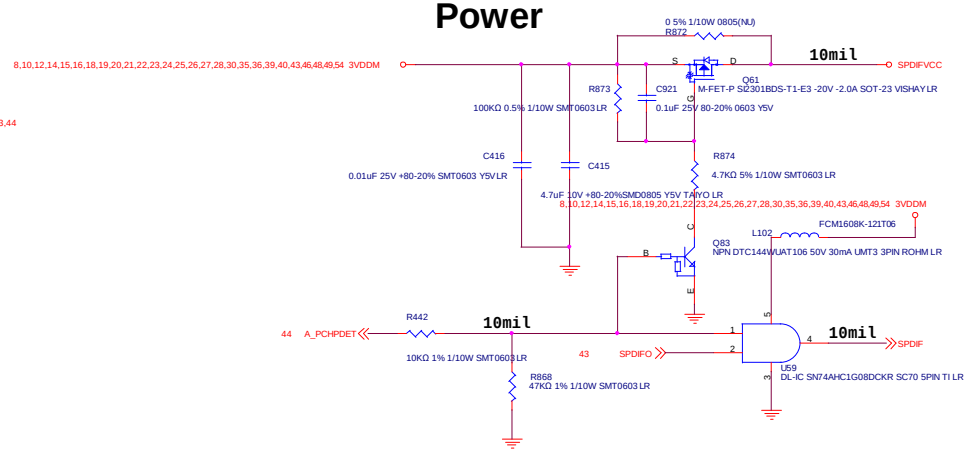
Normal=LOW
Headphone insert=High





7/7 EMI change baed

S/PDIF Power



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Size: C | Document Number: <SPDIF / HP OUT / Audio CN> | Rev: 0.5

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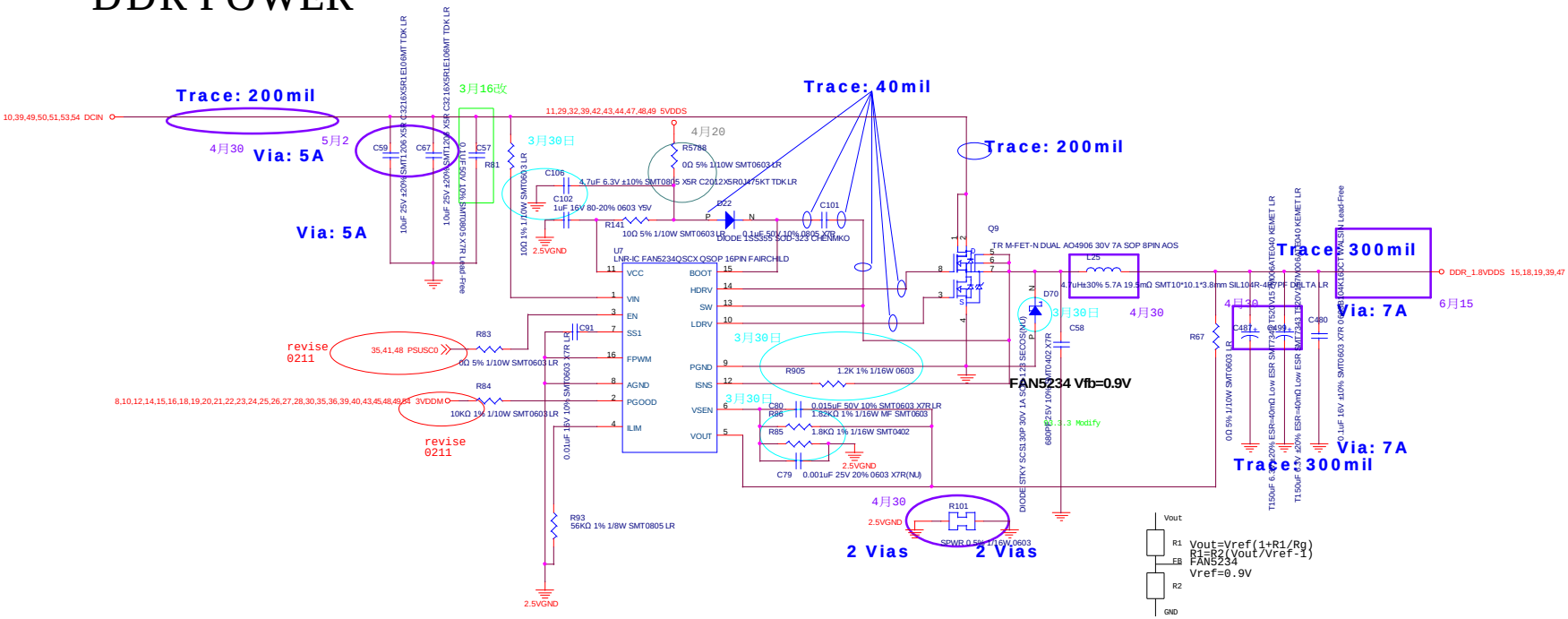
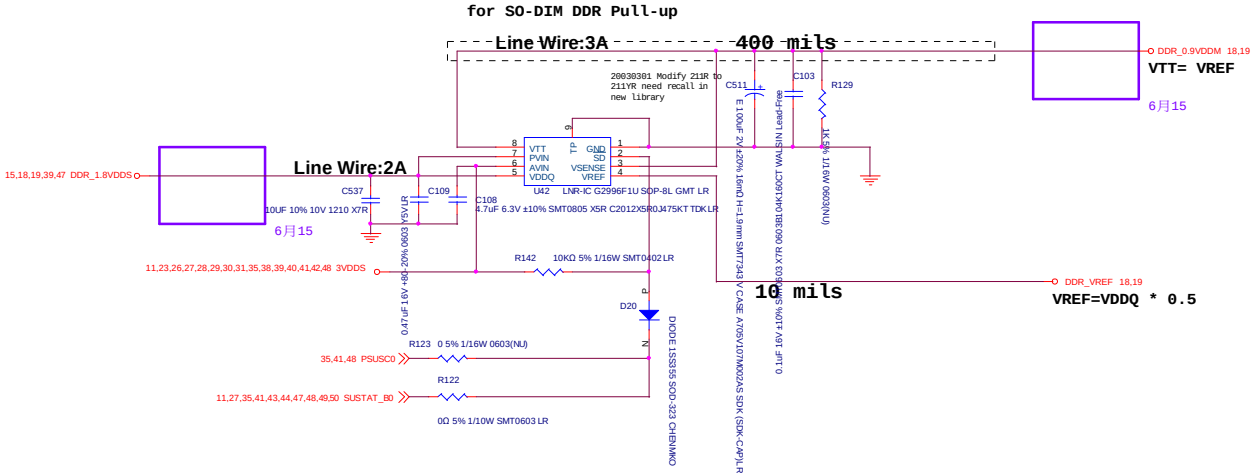
DDR POWER





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Title: LM7R < VIA VN800 + VT8237R>		
Size: C	Document Number: <DDR2 POWER>	Rev: 0.5
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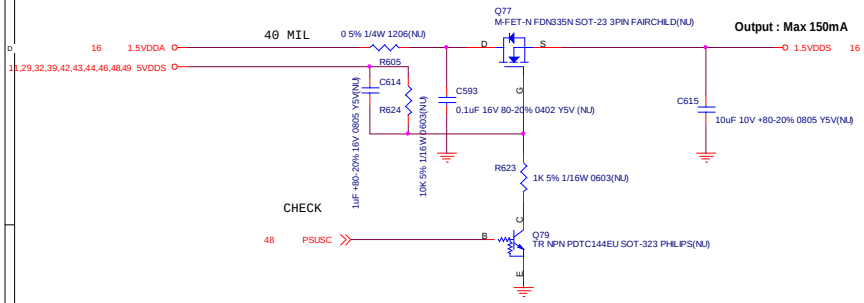
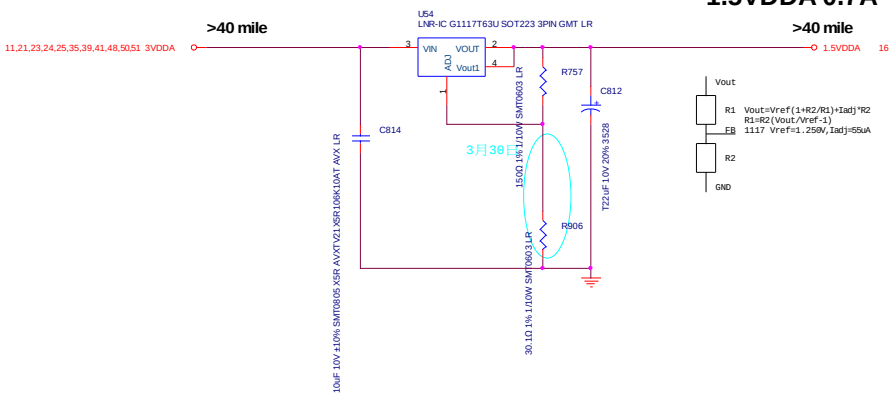
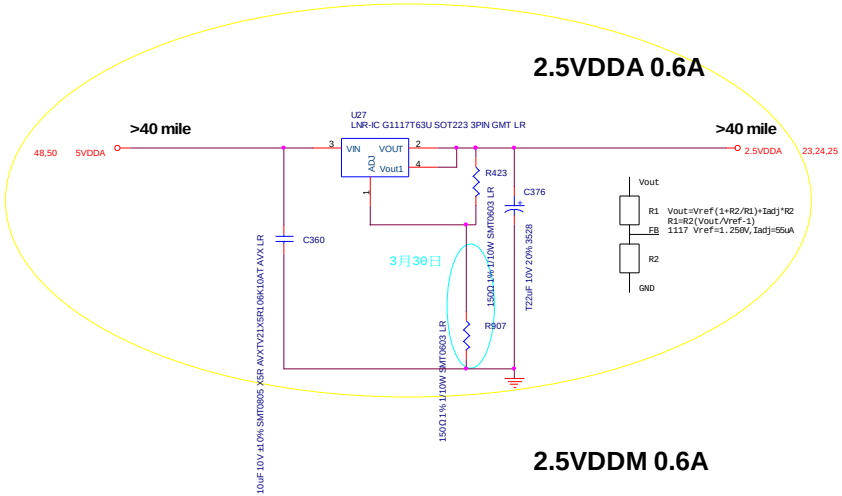
1.5VDDS 0.2A



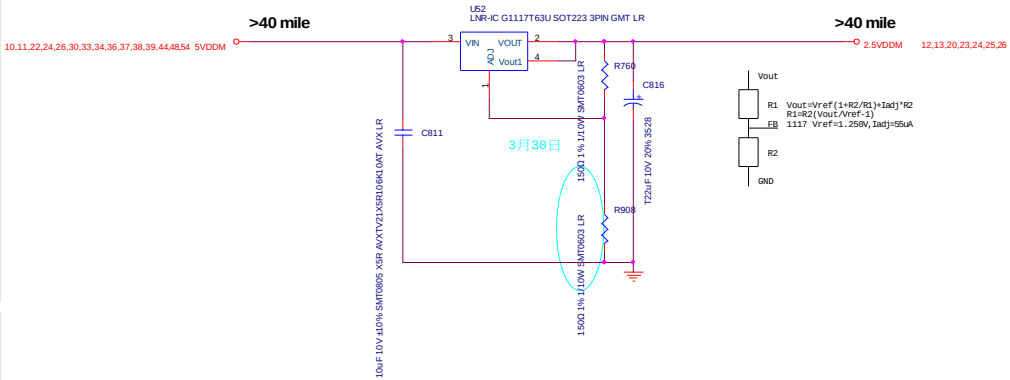
1.5VDDA 0.7A



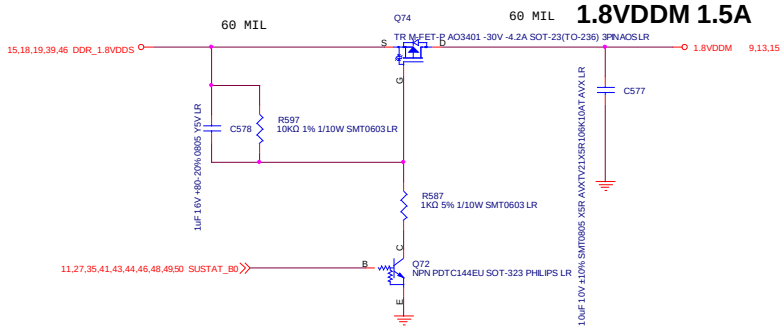
2.5VDDA 0.6A



2.5VDDM 0.6A



1.8VDDM 1.5A



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Title	LM7R < VIA VN800 + VT8237R>	
Size C	Document Number <1.5V / 2.5V /1.8V>	Rev 0.5
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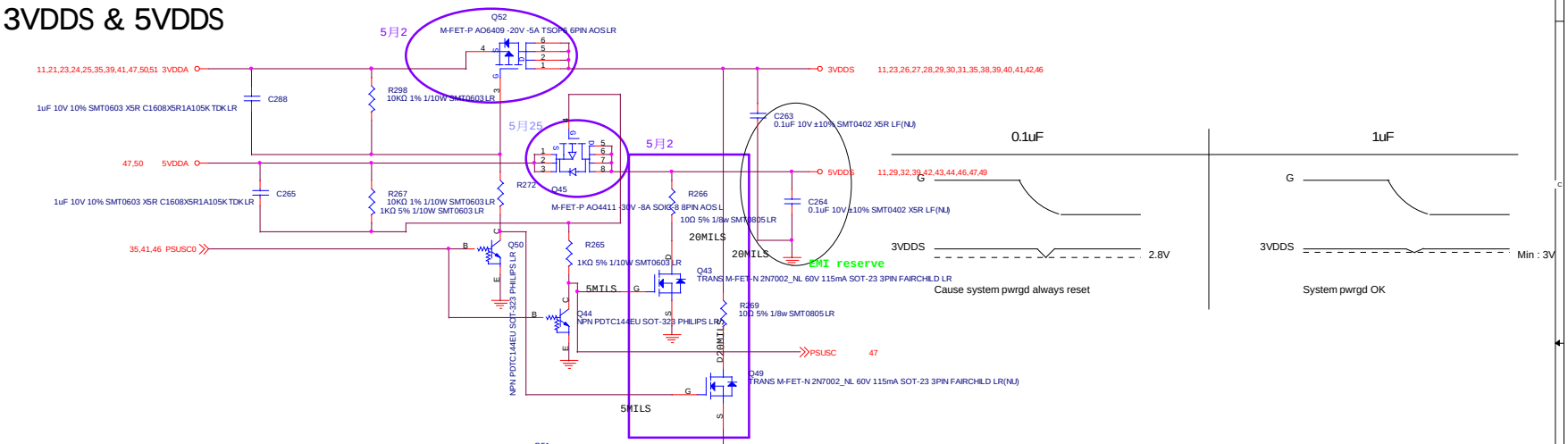
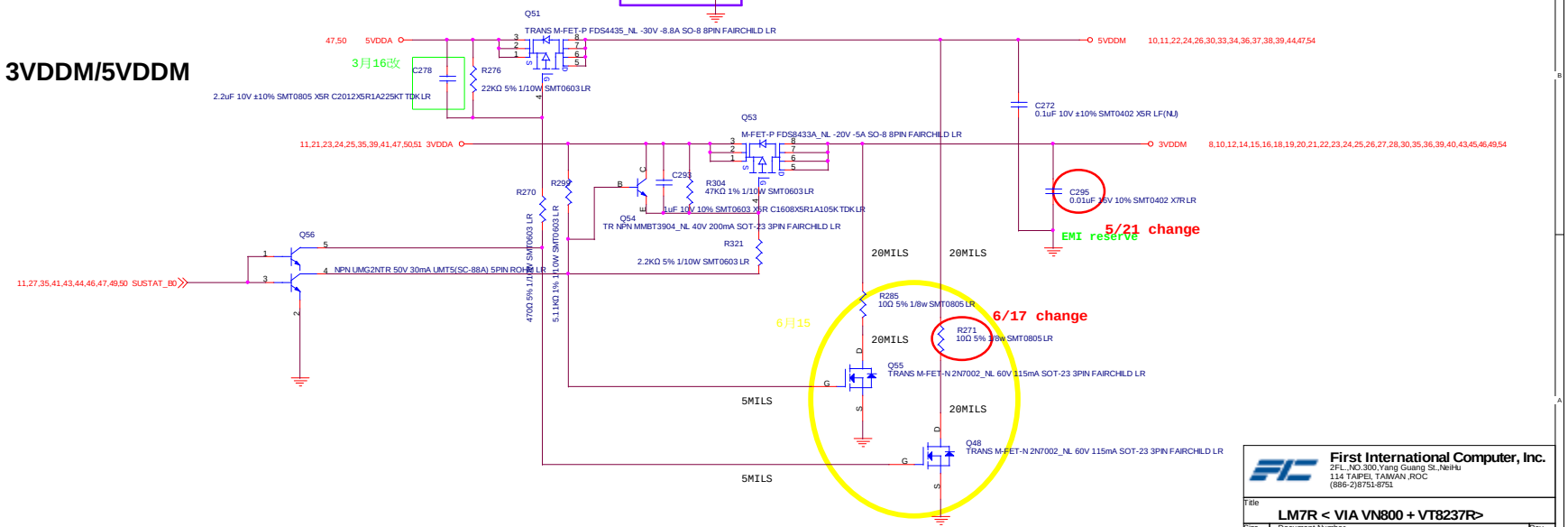
3VDDS & 5VDDS



3VDDM/5VDDM



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Title: LM7R < VIA VN800 + VT8237R>

Size: C | Document Number: <POWER 3/5 VDDS/VDDM> | Rev: 0.5

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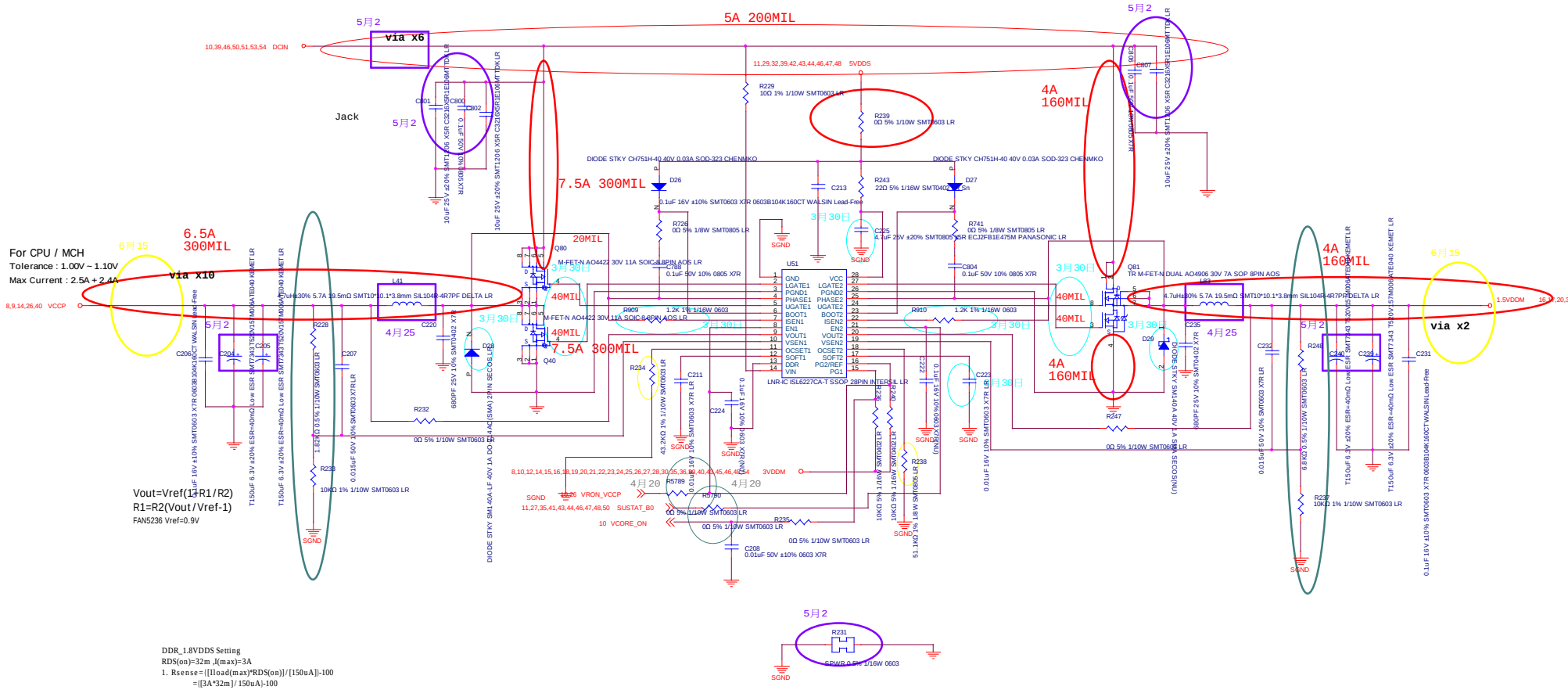
VCCP ,VORE_GMCH



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Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <VCCP & 1.5VDDM>	Rev: 0.5
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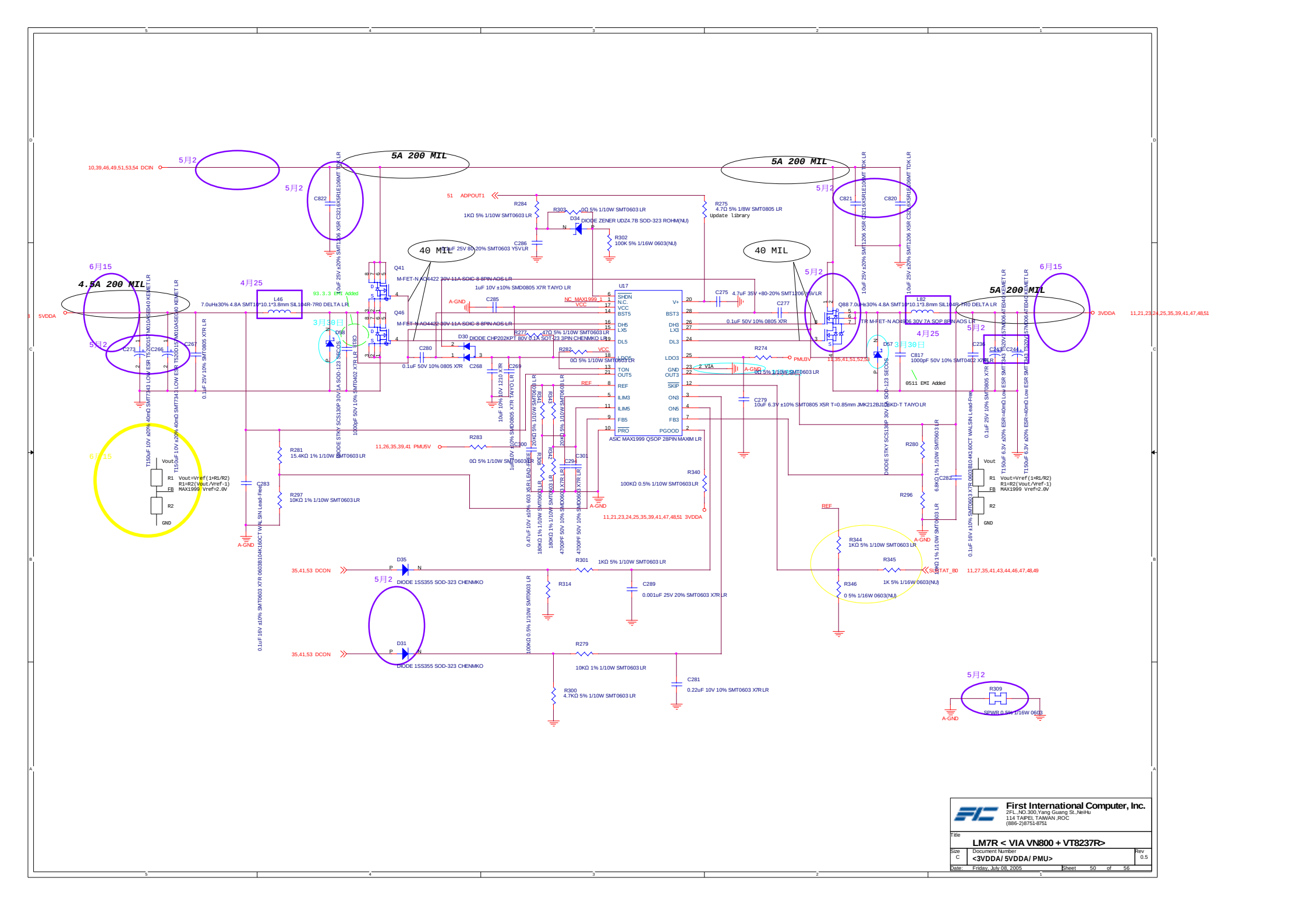

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Title	LM7R < VIA VN800 + VT8237R>
Size: C	Document Number: <3VDDA/ 5VDDA/ PMU>
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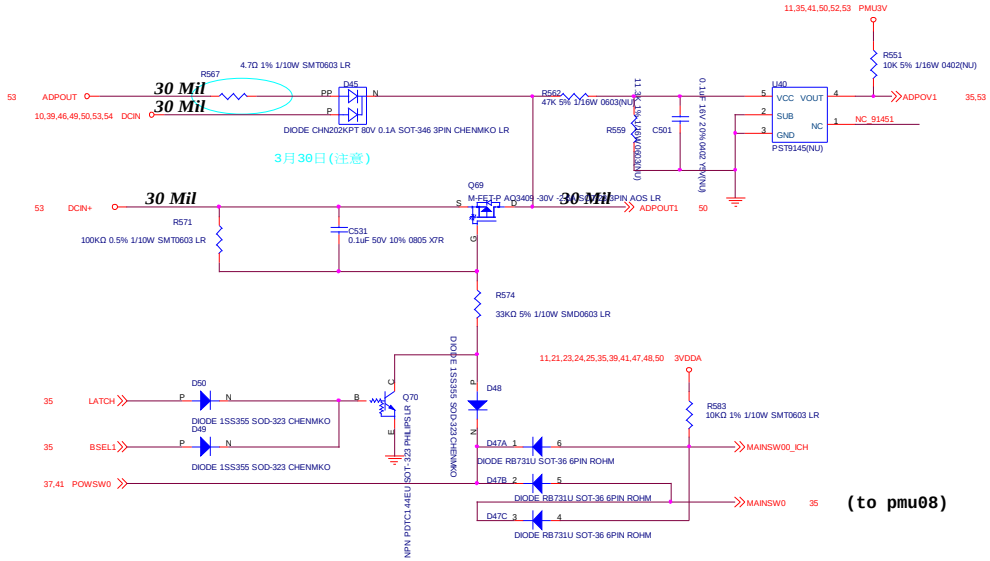

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Title	LM7R < VIA VN800 + VT8237R>	
Size C	Document Number <power-on switch control>	Rev 0.5
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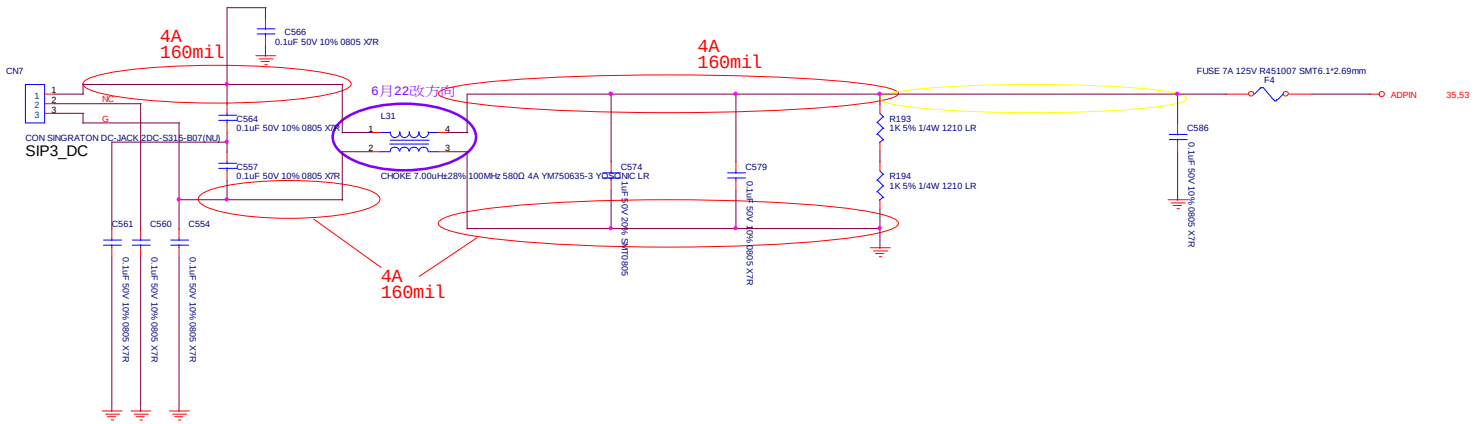
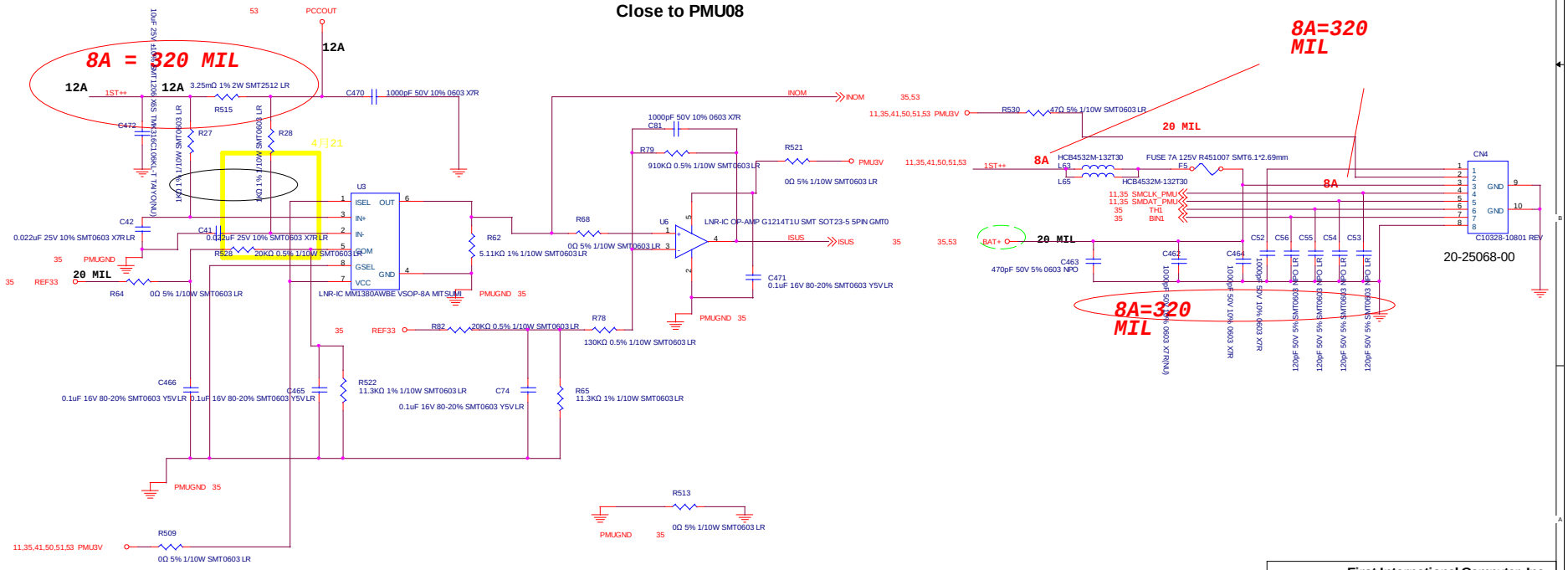


CHR BATTERY IN

Close to PMU08



winky 0710

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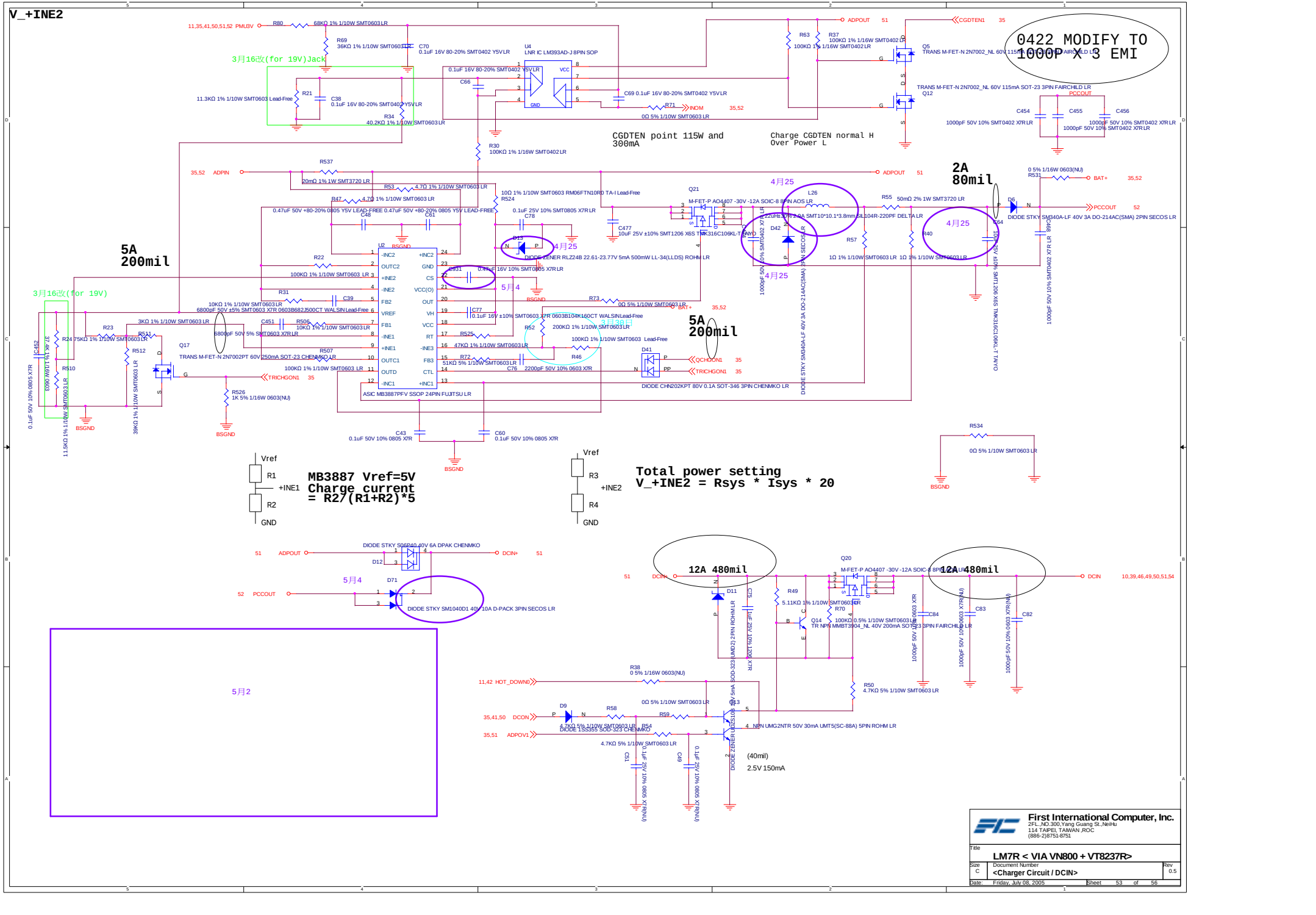
Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <AC-IN / Battery CNN>	Rev: 0.5
Date: Friday, July 08, 2005	Sheet 52 of 56	


V_+INE2
0422 MODIFY TO
1000P X 3 EMI
3月16改(for 19V)Jack
CGDTEN point 115W and
300mA
Charge CGDTEN normal H
Over Power L
2A
80mil
5A
200mil
3月16改(for 19V)
5A
200mil
4月25
5月4
MB3887 Vref=5V
Charge current
= R27(R1+R2)*5
Total power setting
V_+INE2 = Rsys * Isys * 20
12A 480mil
12A 480mil
5月2
(40mil)
2.5V 150mA
First International Computer, Inc.
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(886-2)8751-8751
LM7R < VIA VN800 + VT8237R>
<Charger Circuit / DCIN>
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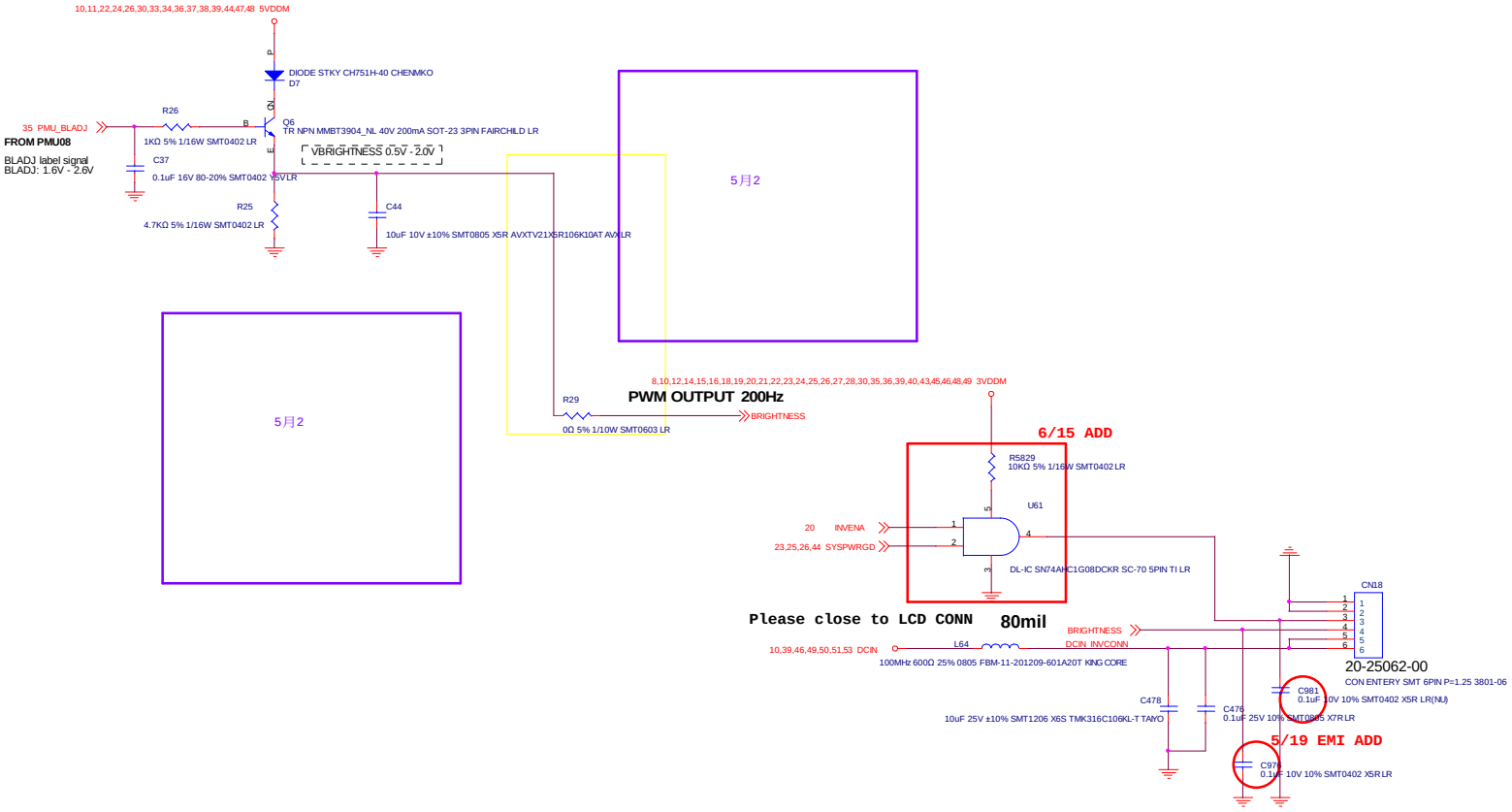
Inverter Control

LCD brightness control



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Title	LM7R < VIA VN800 + VT8237R>	
Size: C	Document Number: <Inverter>	Rev: 0.5
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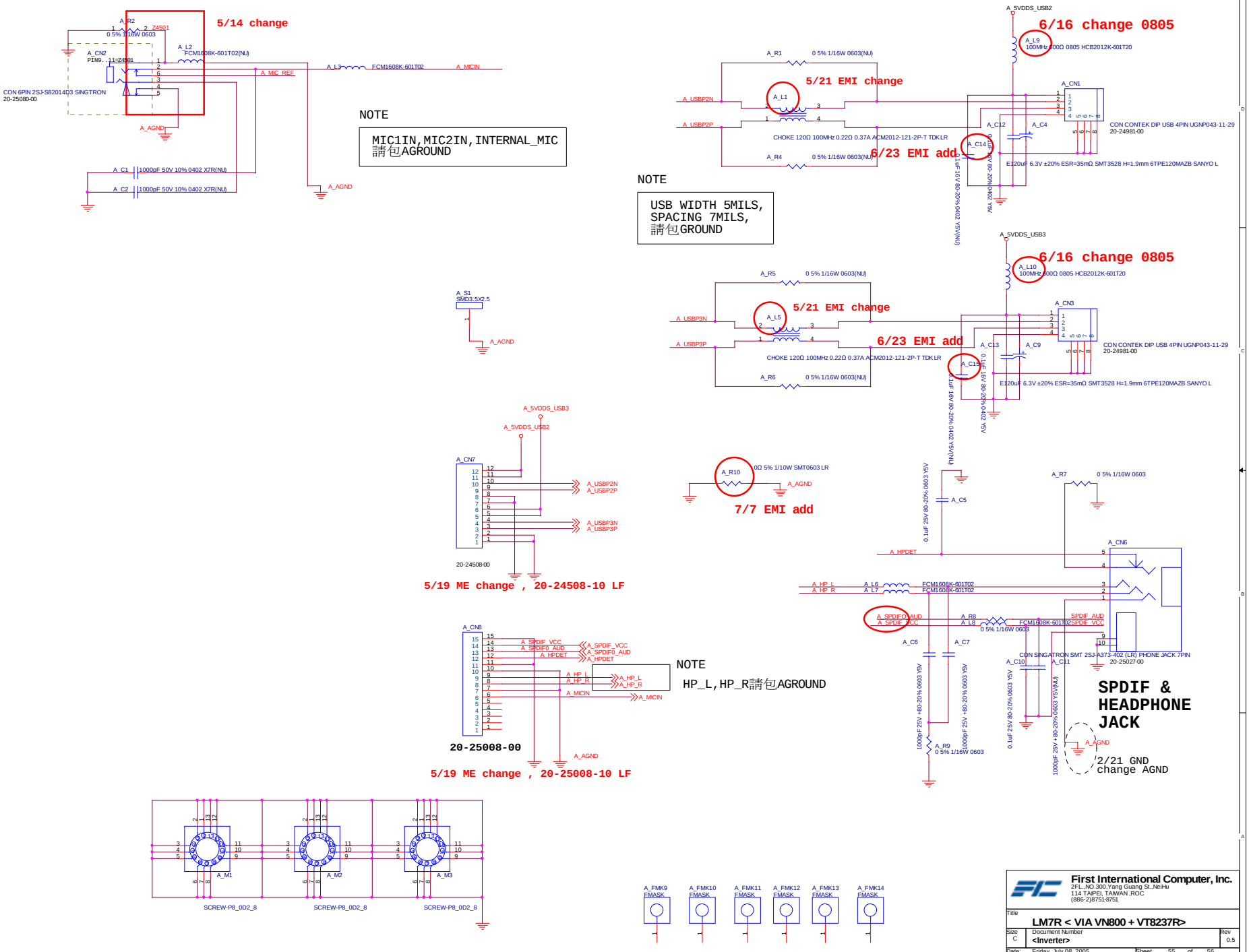
5/14 change
A_R2
Z4501
0 5% 1/16W 0603
A_CN2
PIN9..11=Z4501
A_L2
FCM1608K-601T02(NU)
A_MIC_REF
A_L3
FCM1608K-601T02
A_MICIN
CON 6PIN 2SJ-S82014D3 SINGTRON
20-25080-00
A_AGND
A_C1
1000pF 50V 10% 0402 X7R(NU)
A_C2
1000pF 50V 10% 0402 X7R(NU)
NOTE
MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND
A_5VDDS_USB2
6/16 change 0805
A_L9
100MHz 600Ω 0805 HCB2012K-601T20
A_R1
0 5% 1/16W 0603(NU)
5/21 EMI change
A_USBP2N
A_USBP2P
A_L1
CHOKE 120Ω 100MHz 0.22Ω 0.37A ACM2012-121-2P-T TDK LR
A_R4
0 5% 1/16W 0603(NU)
6/23 EMI add
A_CN1
CON CONTEK DIP USB 4PIN UGNP043-11-29
20-24981-00
A_C12
A_C4
A_C14
E120uF 6.3V ±20% ESR=35mΩ SMT3528 H=1.9mm 6TPE120MAZB SANYO L
0.1uF 16V 80-20% 0402 Y5V(NU)
NOTE
USB WIDTH 5MILS,
SPACING 7MILS,
請包GROUND
A_5VDDS_USB3
6/16 change 0805
A_L10
100MHz 600Ω 0805 HCB2012K-601T20
A_R5
0 5% 1/16W 0603(NU)
5/21 EMI change
A_USBP3N
A_USBP3P
A_L5
CHOKE 120Ω 100MHz 0.22Ω 0.37A ACM2012-121-2P-T TDK LR
A_R6
0 5% 1/16W 0603(NU)
6/23 EMI add
A_CN3
CON CONTEK DIP USB 4PIN UGNP043-11-29
20-24981-00
A_C13
A_C9
A_C15
E120uF 6.3V ±20% ESR=35mΩ SMT3528 H=1.9mm 6TPE120MAZB SANYO L
0.1uF 16V 80-20% 0402 Y5V(NU)
A_S1
SMD3.5X2.5
A_AGND
A_5VDDS_USB3
A_5VDDS_USB2
A_CN7
A_USBP2N
A_USBP2P
A_USBP3N
A_USBP3P
20-24508-00
5/19 ME change , 20-24508-10 LF
A_R10
0Ω 5% 1/10W SMT0603 LR
7/7 EMI add
0.1uF 25V 80-20% 0603 Y5V
A_C5
A_R7
0 5% 1/16W 0603
A_HPDET
A_CN6
A_HP_L
A_HP_R
A_L6
A_L7
FCM1608K-601T02
A_SPDIFO_AUD
A_SPDIF_VCC
A_R8
A_L8
FCM1608K-601T02
SPDIF_AUD
SPDIF_VCC
0 5% 1/16W 0603
A_C6
A_C7
1000pF 25V +80-20% 0603 Y5V
A_R9
0 5% 1/16W 0603
A_C10
A_C11
CON SINGATRON SMT 2SJ-A373-402 (LR) PHONE JACK 7PIN
20-25027-00
A_CN8
A_SPDIF_VCC
A_SPDIFO_AUD
A_HPDET
A_HP_L
A_HP_R
A_MICIN
20-25008-00
A_AGND
5/19 ME change , 20-25008-10 LF
NOTE
HP_L,HP_R請包AGROUND
SPDIF &
HEADPHONE
JACK
2/21 GND
change AGND
A_M1
A_M2
A_M3
SCREW-P8_0D2_8
SCREW-P8_0D2_8
SCREW-P8_0D2_8
A_FMK9
FMASK
A_FMK10
FMASK
A_FMK11
FMASK
A_FMK12
FMASK
A_FMK13
FMASK
A_FMK14
FMASK
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