First International Computer, Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : AMD S1 + MCP67MD + NB8M-SE

Version : 0.4

Initial Date : 10/25/2006

Confidential

Manager Sign by : Avery Lee

Drawing by : Ahsing Huang

Total confirm by :Adam Cho

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Title: PTT50 (FIC)

Size: C | Document Number: TITLE | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 1 of 57

1. Schematic Page Description :

FIC Schematic Ver : 0.1

2. PCI BUS Description :

IDSEL	CHIP
AD22	1394 VIA VT6311S

PCIINT	CHIP
IRQA	——
IRQB	——
IRQC	1394 VIA VT6311S
IRQD	——

BUSMASTER

REQ	CHIP
REQ0 / GNT0	——
REQ1 / GNT1	1394 VIA VT6311S
REQ2 / GNT2	——
REQ3 / GNT3	——
REQ4 / GNT4	——

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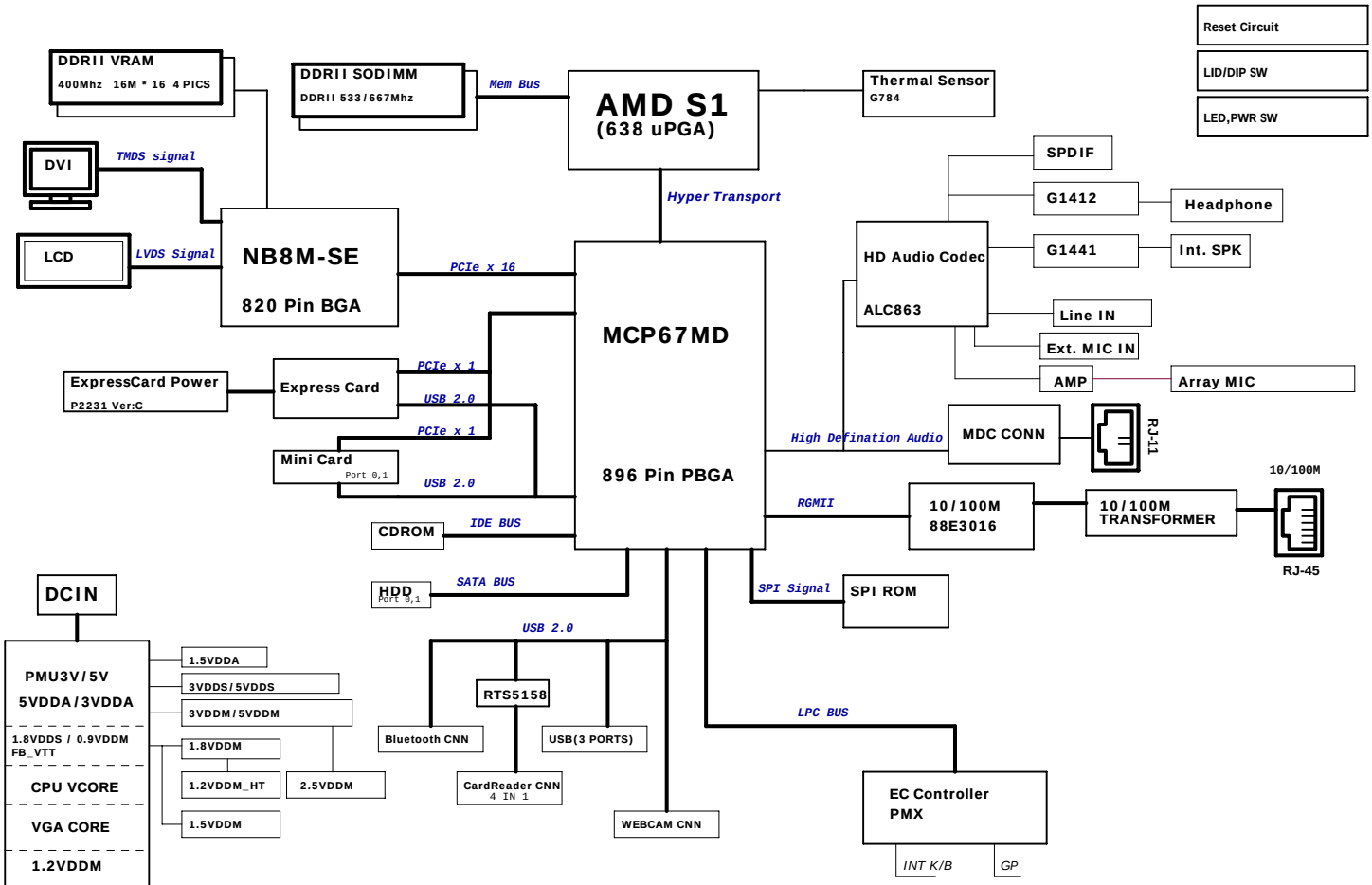
Title: PTT50 (FIC)

Size: C | Document Number: Schematic Page DESCR | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 2 of 57



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Size: C | Document Number: Block Diagram | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 3 of 57

4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
1.5VDDA	1.5V always on power rail by DCON or PSUSC0
1.8VDDS	1.8V power rail
1.2VDDA	1.2V always on power rail by 3VDDA
0.9VDDM	0.9V DDR Termination Voltage
5VDDM	5.0V suspend power rail
3VDDM	3.3V suspend power rail
2.5VDDM	2.5V suspend power rail
1.5VDDM	1.5V suspend power rail
VDD_CORE	Core Voltage for VGA
VCPU_CORE	Core Voltage for CPU
1.2VDDM	VCC For CPU & NB
+1.2VHT	VCC For CPU & NB Hyper Transport

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

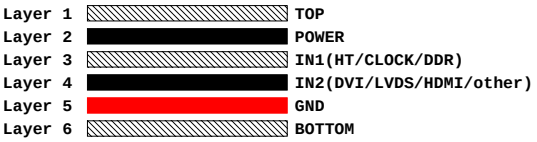
0 = Active Low signal

Signal Conditioning

_D_ = Damped (by a resistor)
_Q_ = Isolated (by a Q-switch)
_L_ = Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers



Impedance Based On a Six-Layer Stack-Up

Interface	Impedance
PCI-Express HT signals	60 Ohm +/- 10% SE 93 Ohm +/- 10% differential
RGMII, SATA, IFP/TMDS, HDMI	55 Ohm +/- 10% SE 100 Ohm +/- 10% differential
USB	50 Ohm +/- 10% SE 90 Ohm +/- 10% differential
All other interfaces	60 Ohm +/- 10% SE

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Title: PTT50 (FIC)
Size: C
Document Number: ANNOTATIONS
Rev: 0.1
Date: Tuesday, July 03, 2007
Sheet 4 of 57

6.Schematic modify Item and History :

V0.1 --> V0.2

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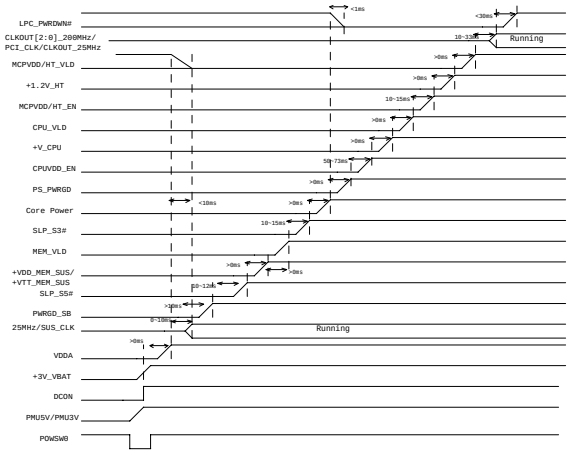
Title: PTT50 (FIC)

Size: C | Document Number: Schematic History | Rev: 0.1

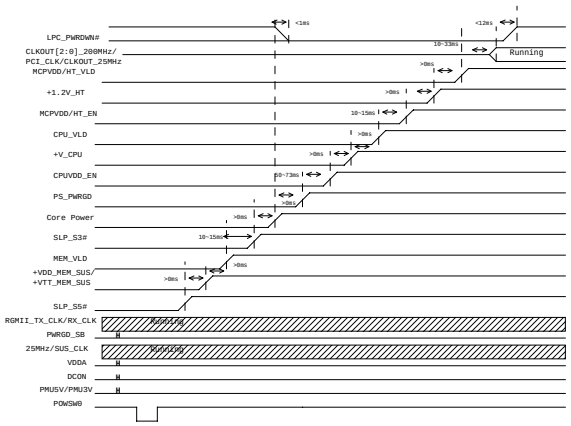
Date: Tuesday, July 03, 2007 | Sheet 5 of 57

7. power on & off & S3 Sequence :

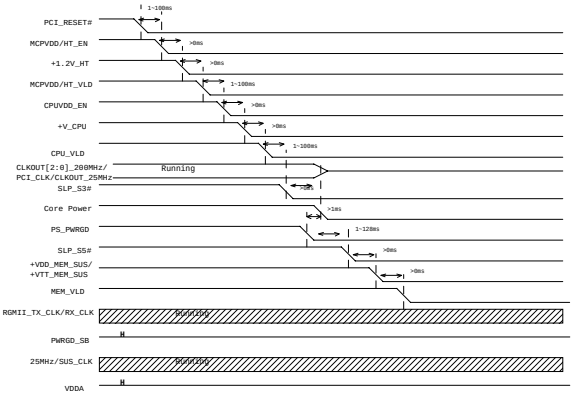
G3-to-S0 Power-Up Sequence



S3/S4/S5 to S0 Resume Sequence



S3/S4/S5 Power-Down Sequence



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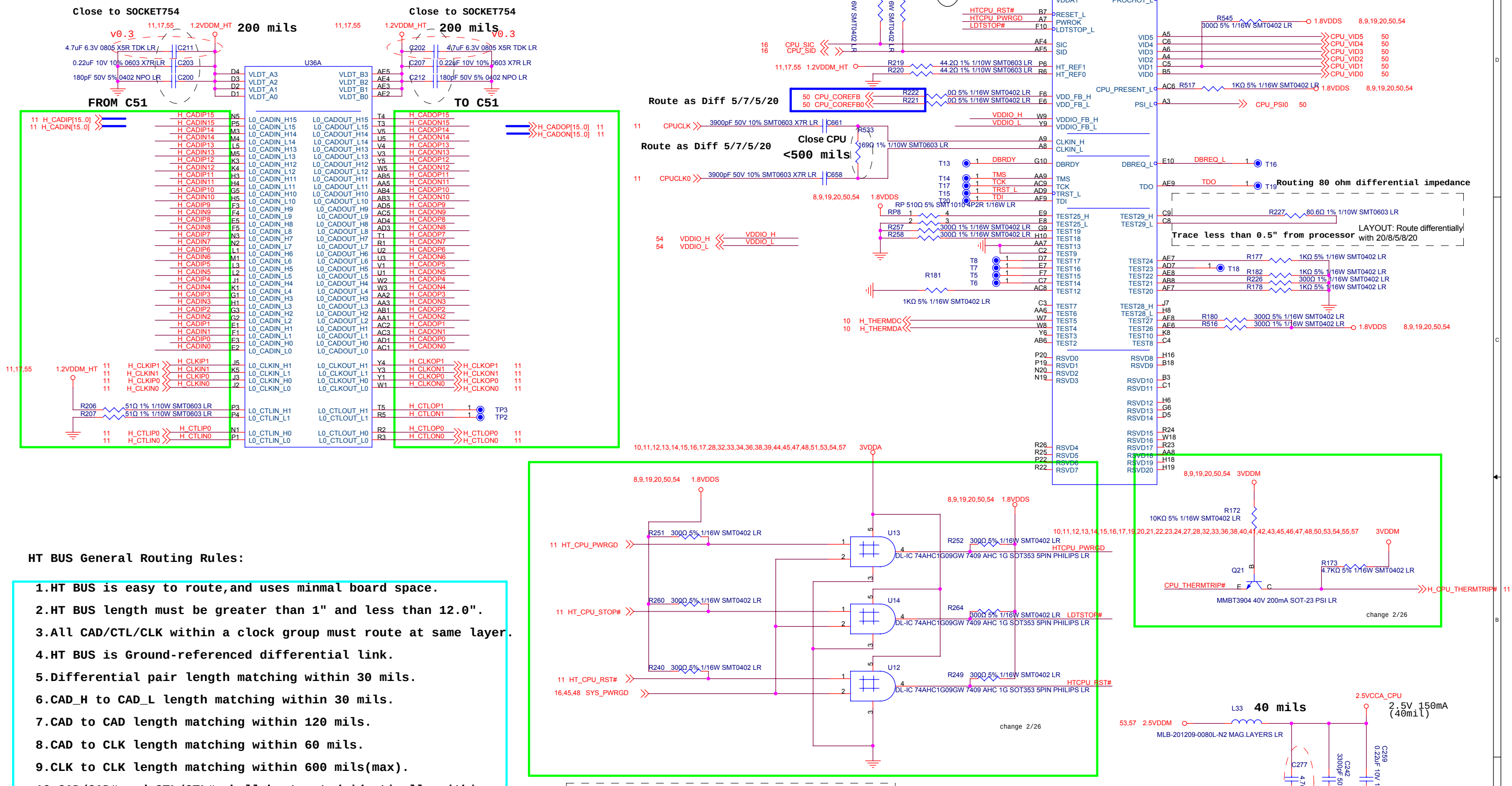
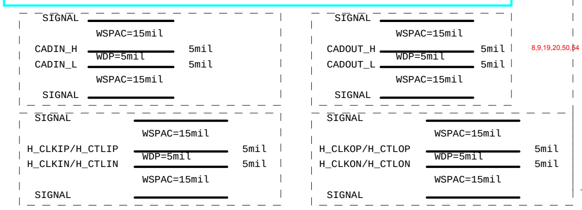
Title	PTT50 (FIC)	
Size: C	Document Number: Timing Diagram	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 6 of 57	

ClawHammer HT Interface



HT BUS General Routing Rules:

1. HT BUS is easy to route,and uses minmal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 600 mils(max).
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.



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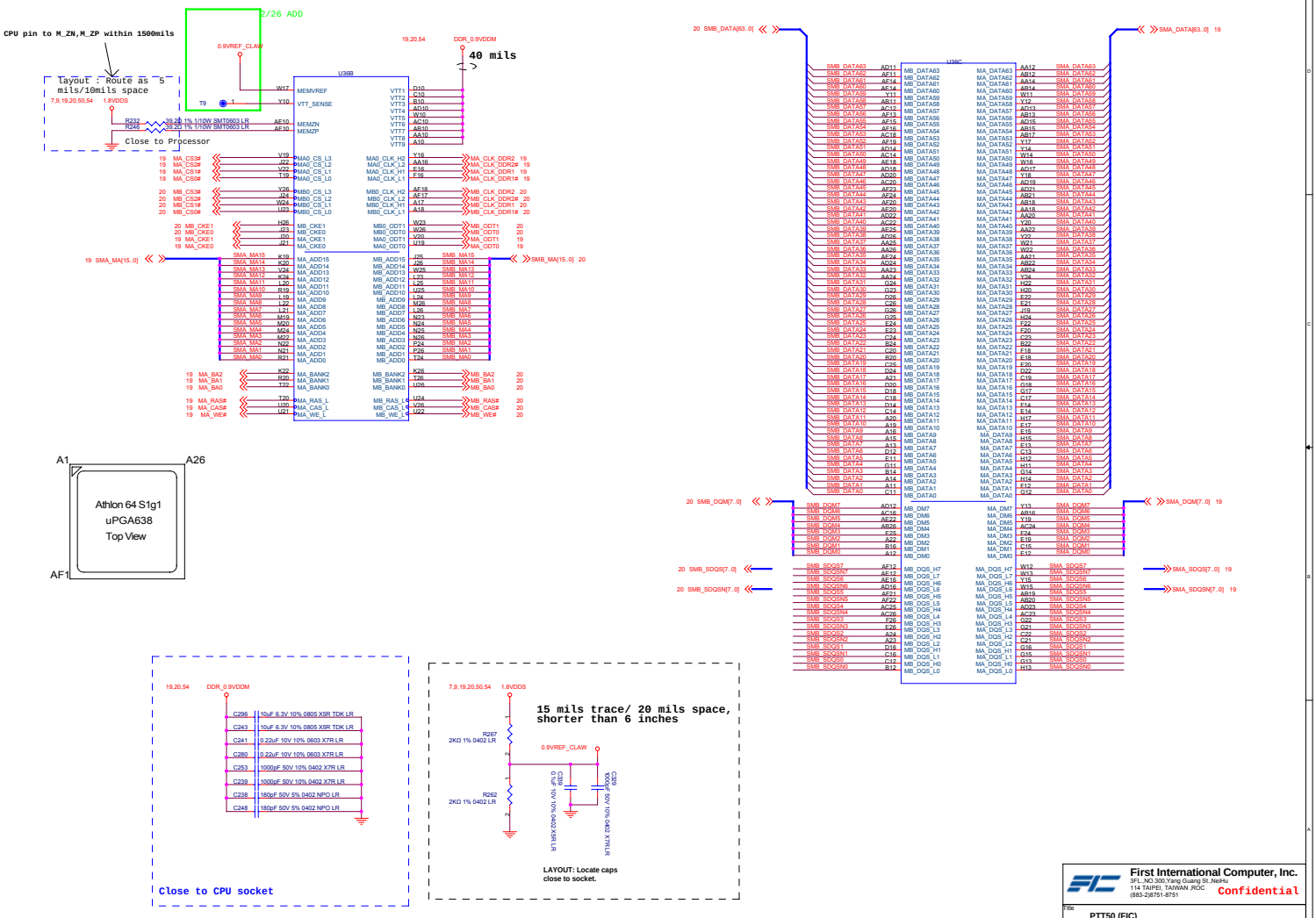
Size C	Document Number AMD S1 HT(1/3)	Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 7 of 57	

Clawhammer DDR Interface



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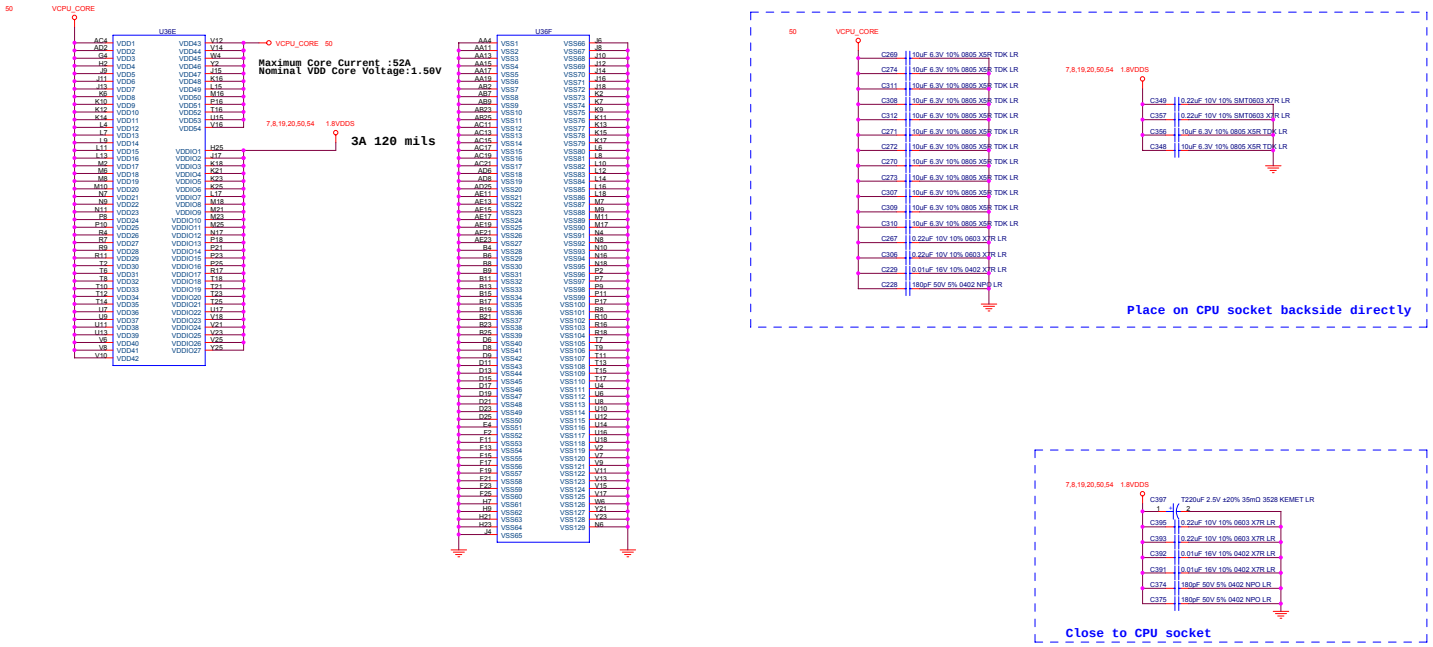
Size: C	Document Number: AMD S1 DDR(2/3)		Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 8 of 57		



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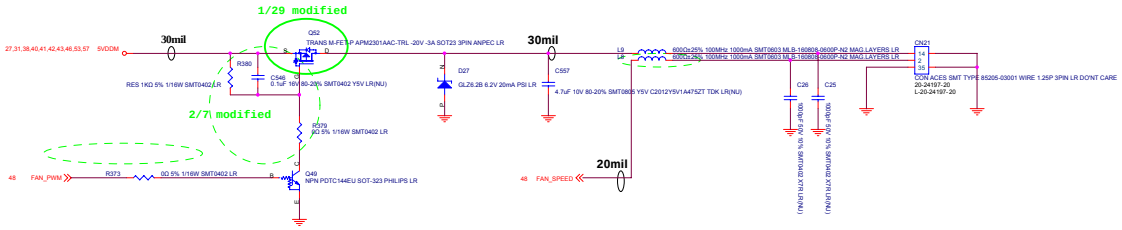
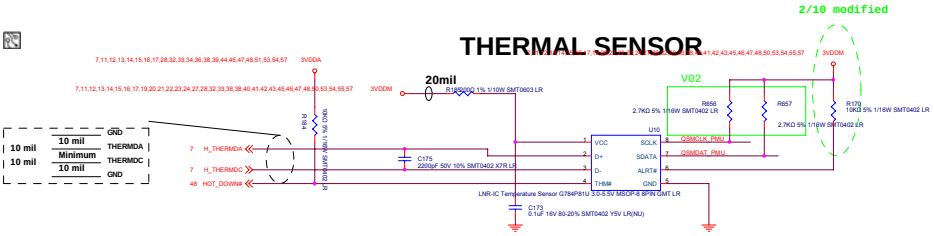
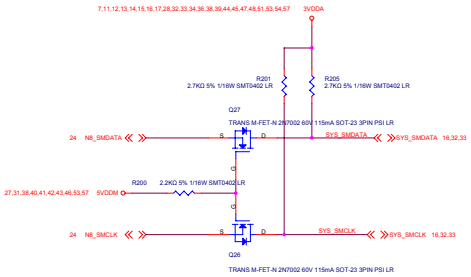
Size C	Document Number AMD S1 POWER(3/3)		Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 9	of	57

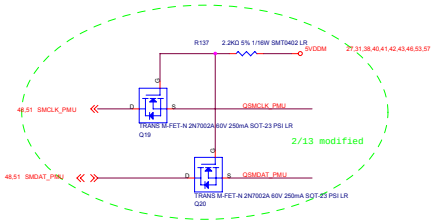
FAN Control



THERMAL SENSOR







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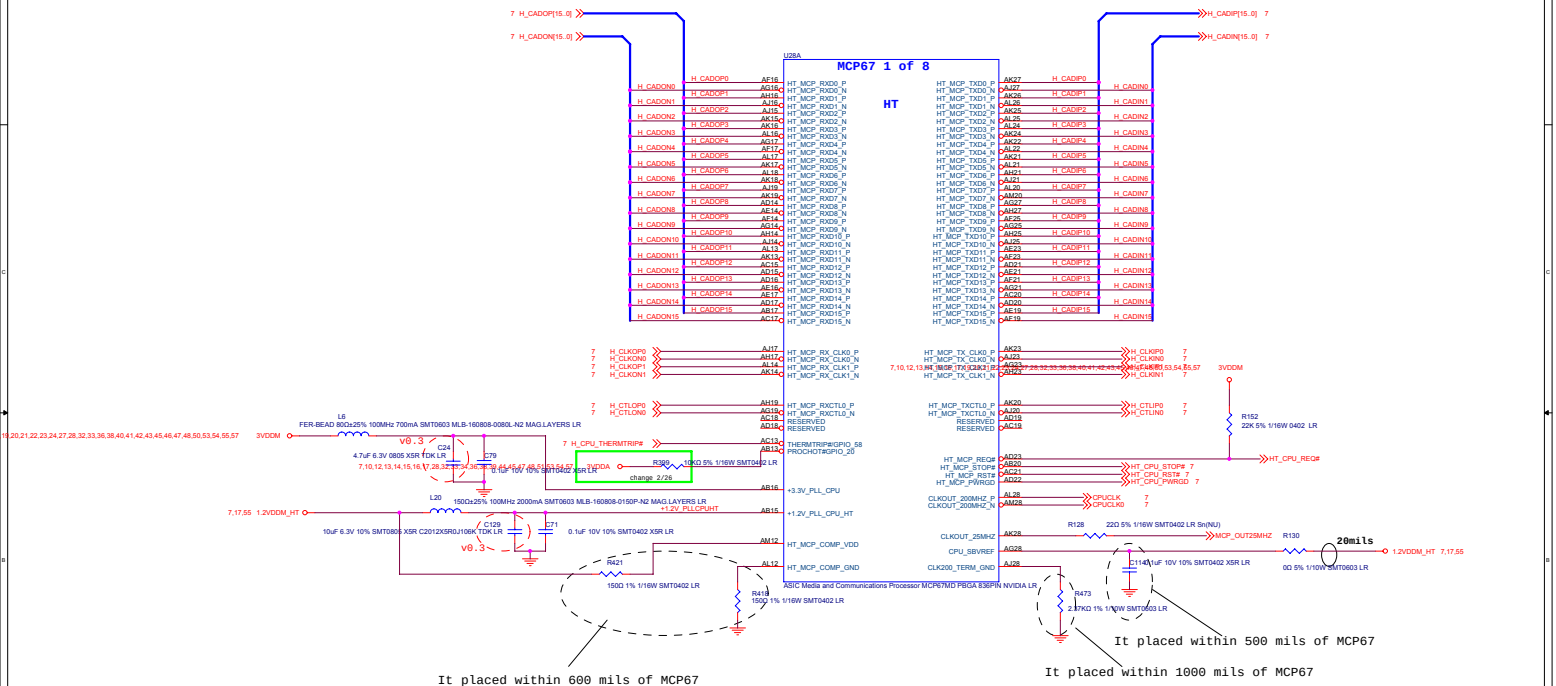
File: PTT50 (FIC)			
Size: C	Document Number: CPU Thermal/Fan CNN		Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 10 of 57		



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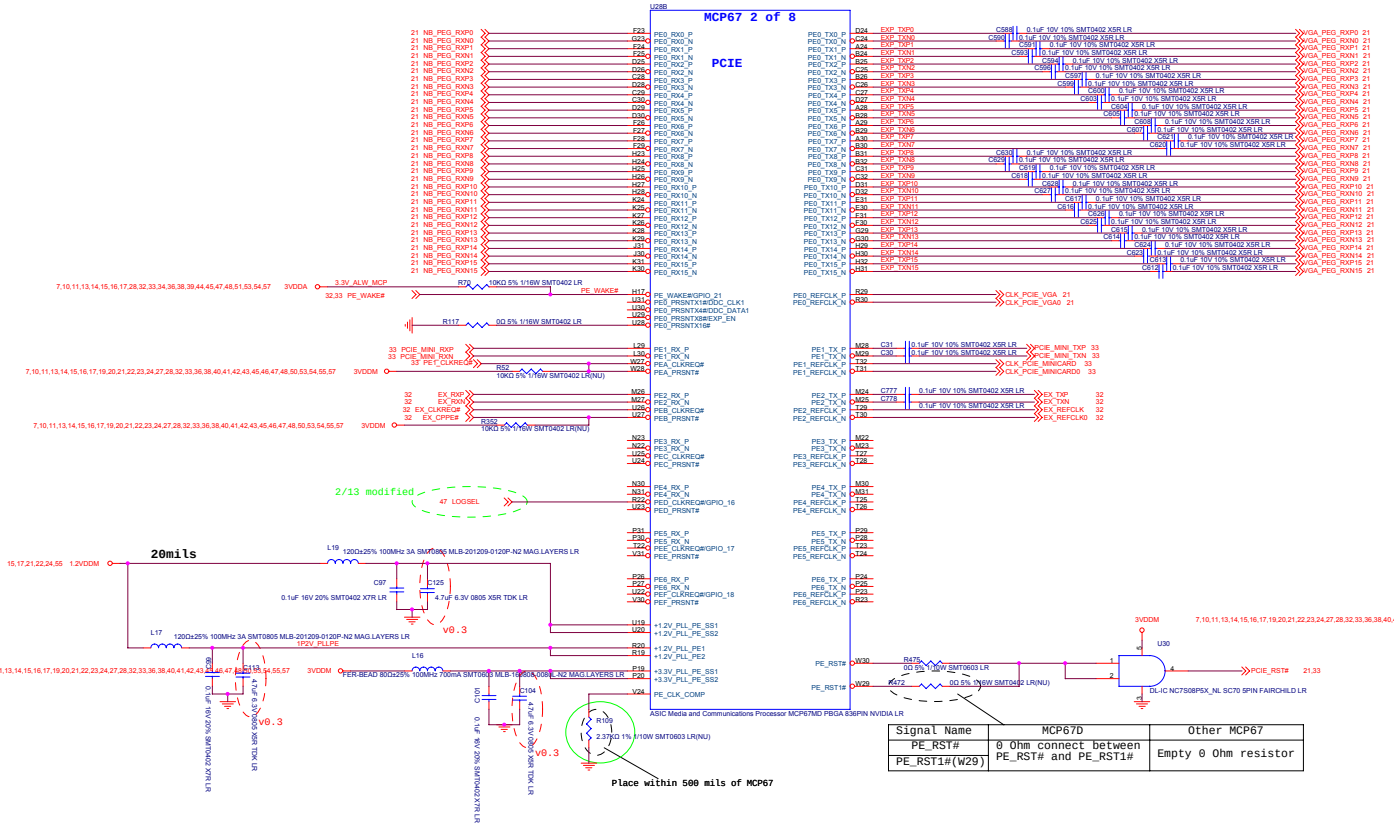
Title	PTT50 (FIC)	
Size: C	Document Number: MCP67 HT (1/8)	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 11 of 57	



Signal Name	MCP67D	Other MCP67
PE_RST#	0 Ohm connect between PE_RST# and PE_RST1#	Empty 0 Ohm resistor
PE_RST1#(W29)		

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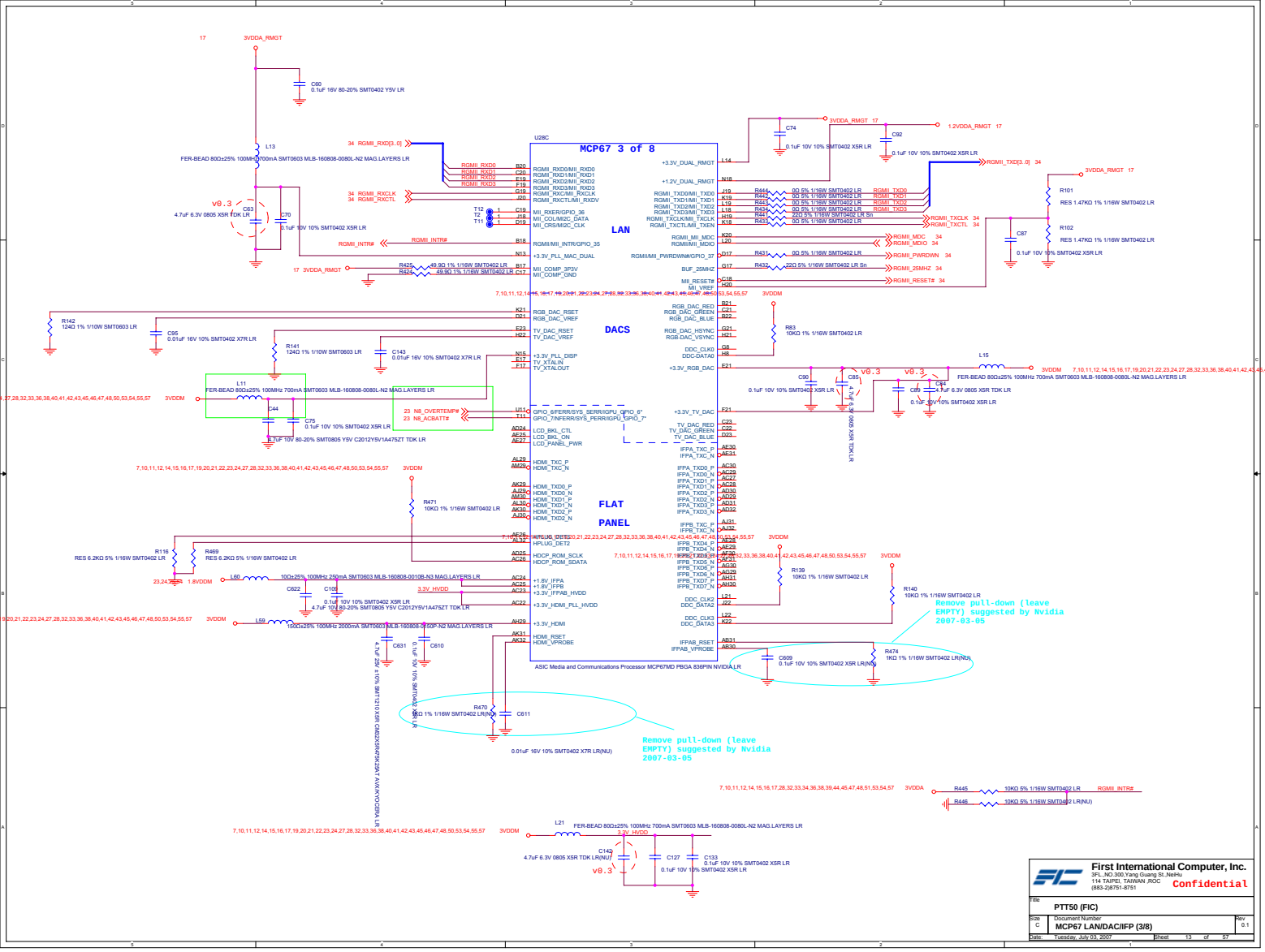
Size: C	Document Number: MCP67 PCIE (2/8)	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 12 of 57	



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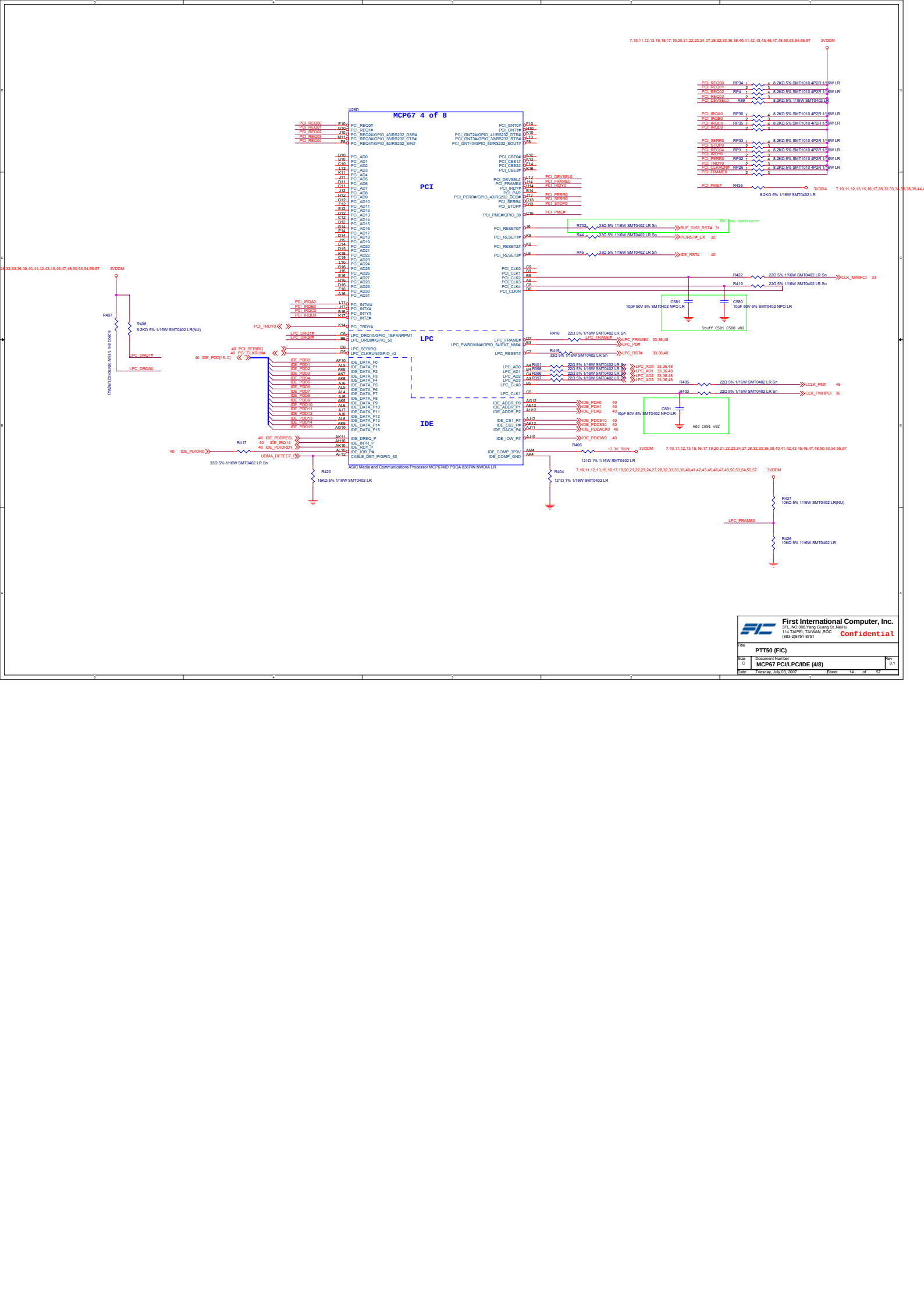
Title	PTT50 (FIC)
Size	C
Document Number	MCP67 LAN/DAC/IFP (3/8)
Rev	0.1
Date	Tuesday, July 03, 2007
Sheet	13 of 57


MCP67 4 of 8
U28D
PCI
LPC
IDE
PCI_REQ00
PCI_REQ01
PCI_REQ02
PCI_REQ03
PCI_REQ04
PCI_GNT0#
PCI_GNT1#
PCI_GNT2#/GPIO_41/RS232_DTR#
PCI_GNT3#/GPIO_39/RS232_RTS#
PCI_GNT4#/GPIO_53/RS232_SOUT#
PCI_CBE0#
PCI_CBE1#
PCI_CBE2#
PCI_CBE3#
PCI_DEVSEL#
PCI_FRAME#
PCI_IRDY#
PCI_PAR
PCI_PERR#/GPIO_43/RS232_DCD#
PCI_SERR#
PCI_STOP#
PCI_PME#/GPIO_30
PCI_RESET0#
PCI_RESET1#
PCI_RESET2#
PCI_RESET3#
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK3
PCI_CLK4
PCI_CLKIN
PCI_IRQA0
PCI_IRQB0
PCI_IRQC0
PCI_IRQD0
PCI_INTW#
PCI_INTX#
PCI_INTY#
PCI_INTZ#
PCI_TRDY0
PCI_TRDY#
LPC_DRQ1#/GPIO_19/FANRPM1
LPC_DRQ0#/GPIO_50
LPC_SERIRQ
LPC_CLKRUN#/GPIO_42
LPC_FRAME#
LPC_PWRDWN#/GPIO_54/EXT_NMI#
LPC_RESET#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_CLK0
LPC_CLK1
IDE_DATA_P0
IDE_DATA_P1
IDE_DATA_P2
IDE_DATA_P3
IDE_DATA_P4
IDE_DATA_P5
IDE_DATA_P6
IDE_DATA_P7
IDE_DATA_P8
IDE_DATA_P9
IDE_DATA_P10
IDE_DATA_P11
IDE_DATA_P12
IDE_DATA_P13
IDE_DATA_P14
IDE_DATA_P15
IDE_DREQ_P
IDE_INTR_P
IDE_RDY_P
IDE_IOR_P#
CABLE_DET_P/GPIO_63
IDE_ADDR_P0
IDE_ADDR_P1
IDE_ADDR_P2
IDE_CS1_P#
IDE_CS3_P#
IDE_DACK_P#
IDE_IOW_P#
IDE_COMP_3P3V
IDE_COMP_GND
ASIC Media and Communications Processor MCP67MD PBGA 836PIN NVIDIA LR
7,10,11,12,13,15,16,17,19,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57
3VDDM
3VDDA
8.2KΩ 5% 1/16W SMT0402 LR
8.2KΩ 5% 1/16W SMT0402 LR(NU)
33Ω 5% 1/16W SMT0402 LR Sn
22Ω 5% 1/16W SMT0402 LR Sn
10pF 50V 5% SMT0402 NPO LR
121Ω 1% 1/16W SMT0402 LR
15KΩ 5% 1/16W SMT0402 LR
10KΩ 5% 1/16W SMT0402 LR
10KΩ 5% 1/16W SMT0402 LR(NU)
for new cardreader
Stuff C581 C580 v02
Add C891 v02
BUF_5158_RST#
PCIRST#_EX
IDE_RST#
CLK_MINIPCI
CLK_FWHPCI
LCLK_FMX
LPC_FRAME#
LPC_PD#
LPC_RST#
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDCS10
IDE_PDCS30
IDE_PDDACK0
IDE_PDIOW0
+3.3V_RUN
UDMA_DETECT
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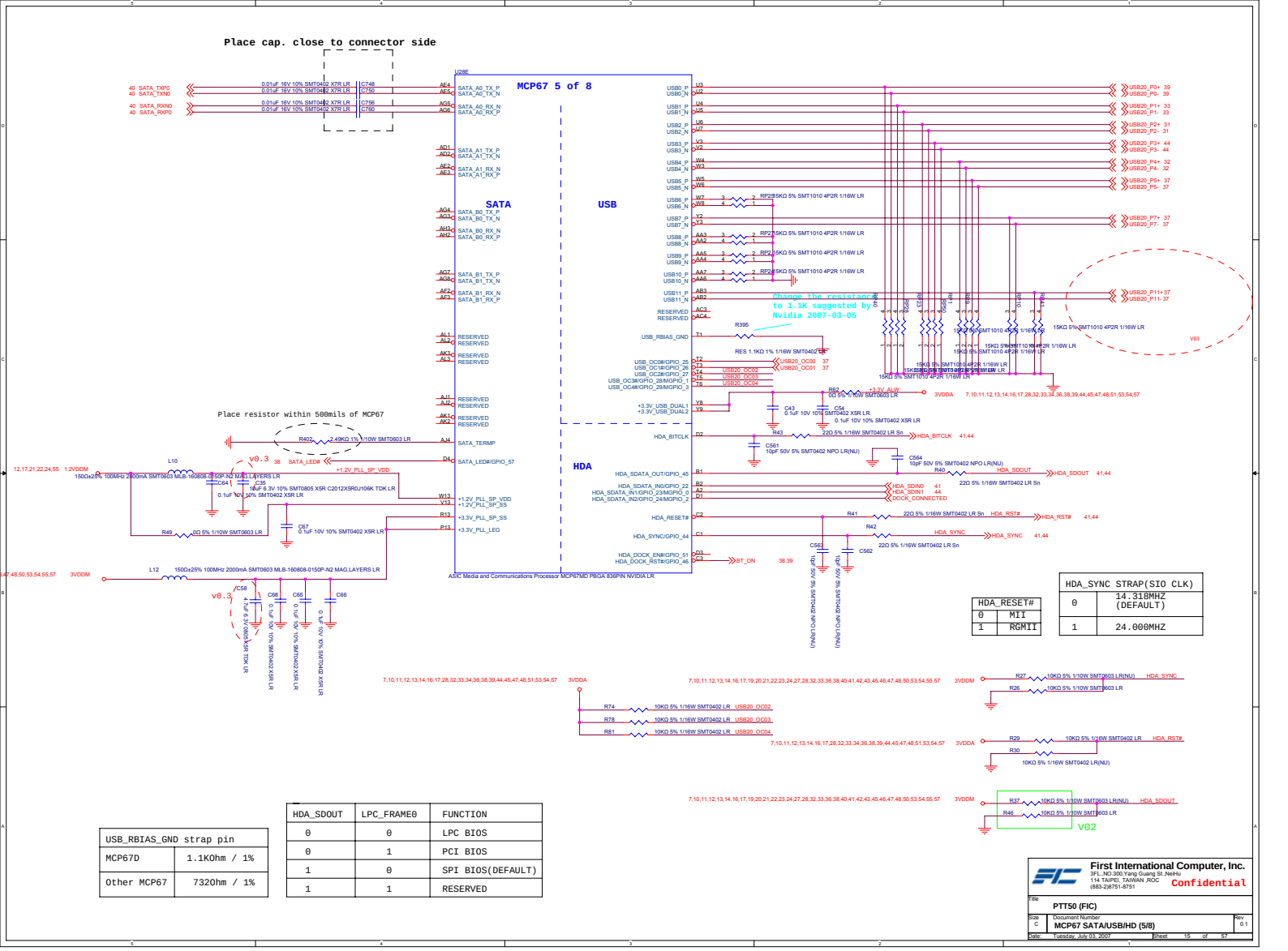
PTT50 (FIC)
MCP67 PCI/LPC/IDE (4/8)
Rev 0.1
Tuesday, July 03, 2007
Sheet 14 of 57



USB_RBIAS_GND strap pin	
MCP67D	1.1KOhm / 1%
Other MCP67	732Ohm / 1%

HDA_SDOUT	LPC_FRAME0	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS(DEFAULT)
1	1	RESERVED

HDA_RESET#	
0	MII
1	RGMII

HDA_SYNC STRAP(SIO CLK)	
0	14.318MHZ (DEFAULT)
1	24.000MHZ

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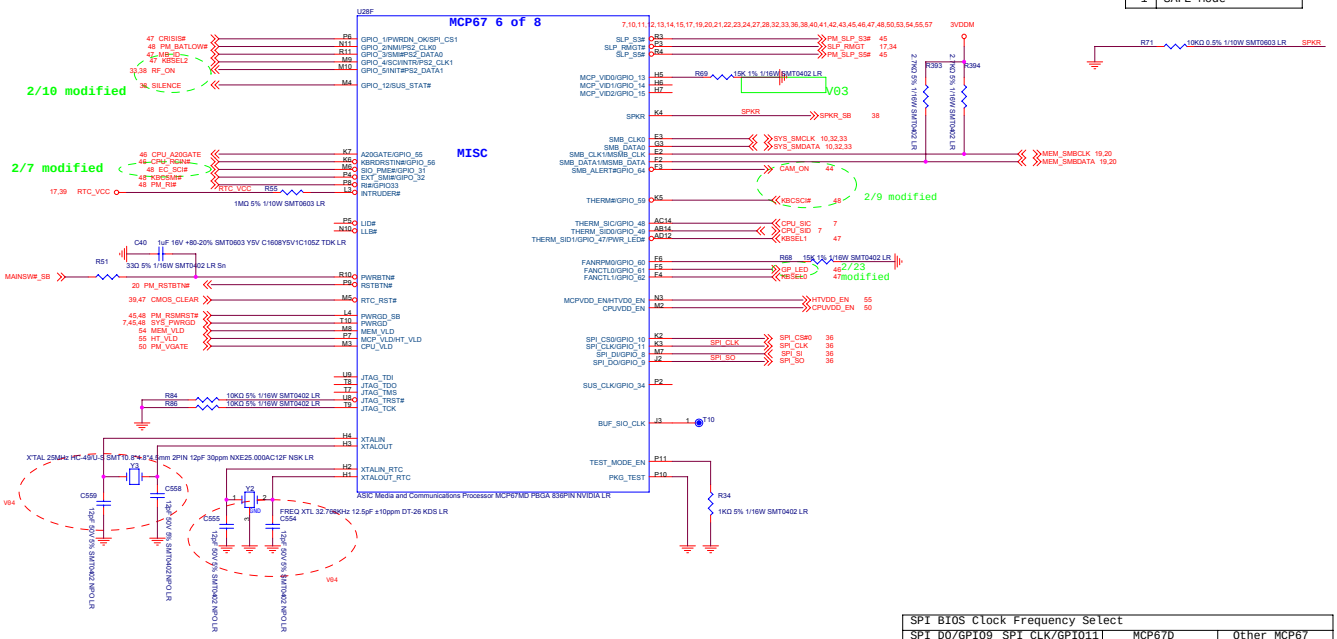
Size: C | Document Number: MCP67 SATA/USB/HD (5/8) | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 15 of 57

Boot Mode Select : SPKR	
0	USER Mode (DEFAULT)
1	SAFE Mode



SPI BIOS Clock Frequency Select		
SPI_DO/GPIO9 SPI_CLK/GPIO11	MCP67D	Other MCP67
00	500KHz	31MHz(default)
01	1.8MHz	42MHz
10	2.5MHz	25MHz
11	25MHz(default)	1MHz

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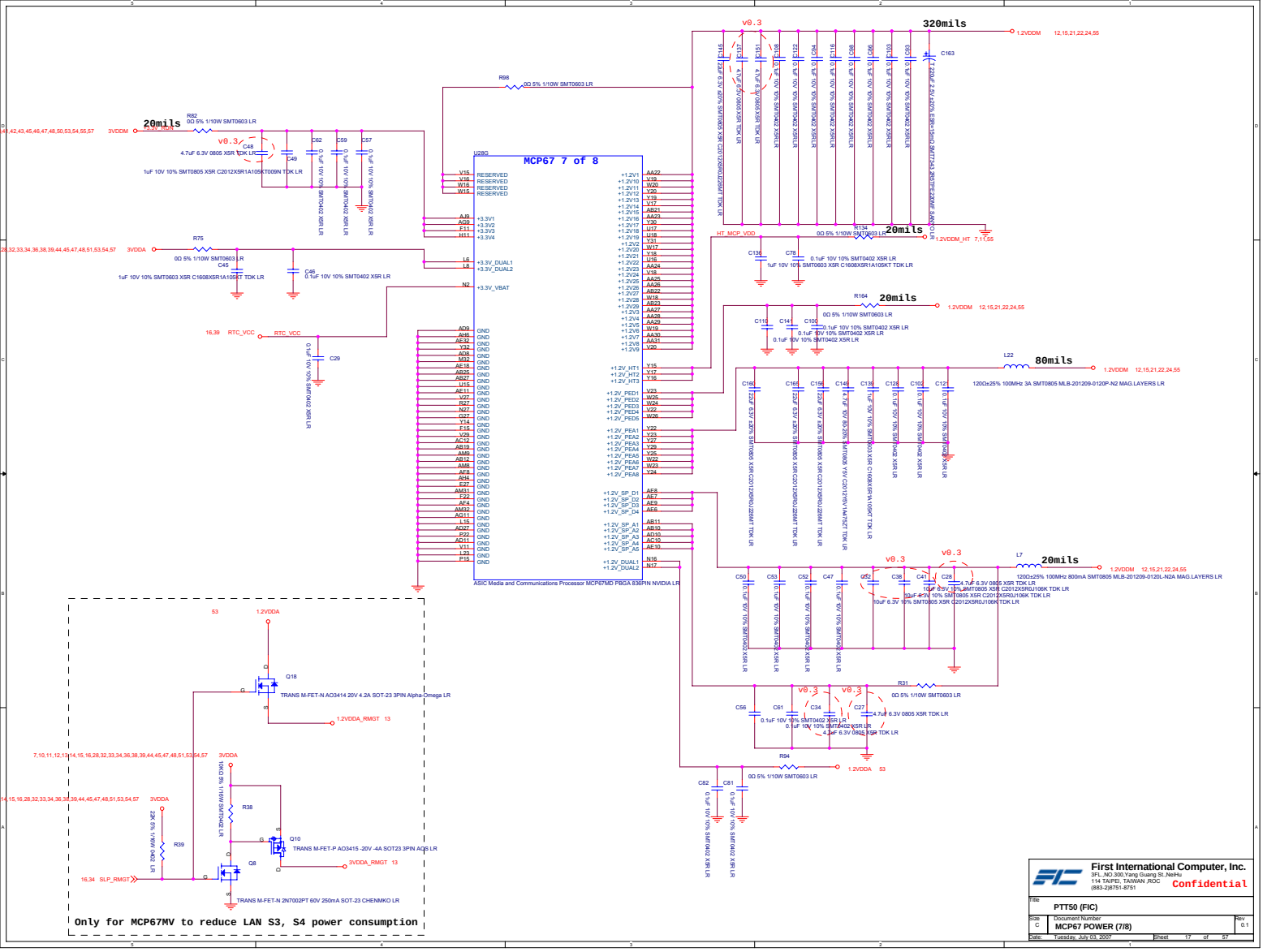
Size C	Document Number MCP67 MISC (6/8)	Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 16 of 57	


MCP67 7 of 8
ASIC Media and Communications Processor MCP67MD PBGA 836PIN NVIDIA LR
Only for MCP67MV to reduce LAN S3, S4 power consumption
320mils
20mils
80mils
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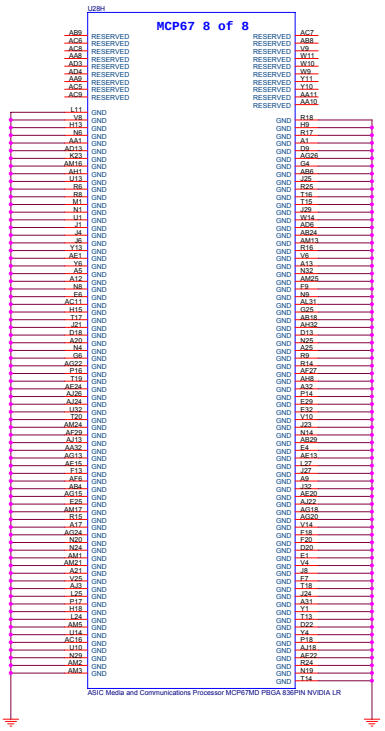
PTT50 (FIC)
MCP67 POWER (7/8)
Tuesday, July 03, 2007
Sheet 17 of 57



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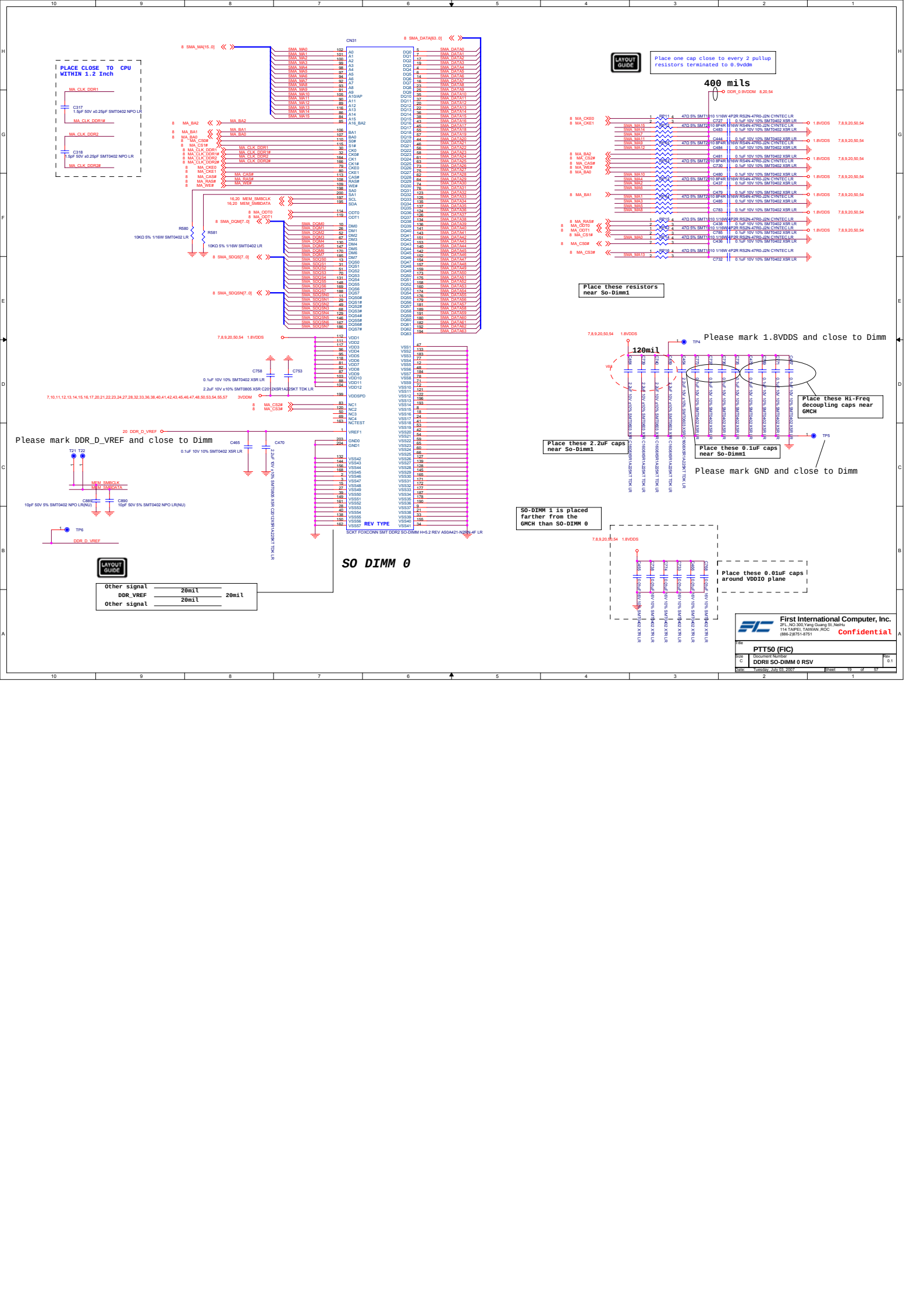
Size: C | Document Number: MCP67 GND (8/8) | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 18 of 57


PLACE CLOSE TO CPU WITHIN 1.2 Inch
MA_CLK_DDR1
C317 1.5pF 50V ±0.25pF SMT0402 NPO LR
MA_CLK_DDR1#
MA_CLK_DDR2
C318 1.5pF 50V ±0.25pF SMT0402 NPO LR
MA_CLK_DDR2#
CN31
8 SMA_MA[15..0]
8 SMA_DATA[63..0]
R580 10KΩ 5% 1/16W SMT0402 LR
R581 10KΩ 5% 1/16W SMT0402 LR
8 SMA_DQM[7..0]
8 SMA_SDQS[7..0]
8 SMA_SDQSN[7..0]
7,8,9,20,50,54 1.8VDDS
C758 0.1uF 10V 10% SMT0402 XSR LR
C753 2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR
7,10,11,12,13,14,15,16,17,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57 3VDDM
Please mark DDR_D_VREF and close to Dimm
20 DDR_D_VREF
C465 0.1uF 10V 10% SMT0402 XSR LR
C470 2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR
T21 T22
MEM_SMBCLK
MEM_SMBDATA
C889 10pF 50V 5% SMT0402 NPO LR(NU)
C890 10pF 50V 5% SMT0402 NPO LR(NU)
TP6
DDR_D_VREF
LAYOUT GUIDE
Other signal
DDR_VREF 20mil
Other signal 20mil
REV TYPE
SCKT FOXCONN SMT DDR2 SO-DIMM H=5.2 REV AS0A421-N28N-4F LR
SO DIMM 0
SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0
LAYOUT GUIDE
Place one cap close to every 2 pullup resistors terminated to 0.9vddm
400 mils
DDR_0.9VDDM 8,20,54
Place these resistors near So-Dimm1
Please mark 1.8VDDS and close to Dimm
120mil
TP4
TP5
Place these 2.2uF caps near So-Dimm1
Place these 0.1uF caps near So-Dimm1
Place these Hi-Freq decoupling caps near GMCH
Please mark GND and close to Dimm
Place these 0.01uF caps around VDDIO plane
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PTT50 (FIC)
DDRII SO-DIMM 0 RSV
Rev 0.1
Tuesday, July 03, 2007
Sheet 19 of 57

PLACE CLOSE TO CPU WITHIN 1.2 Inch

MB_CLK_DDR1

C334 1.5pF 50V ±0.25pF SMT0402 NPO LR

MB_CLK_DDR1#

MB_CLK_DDR2

C333 1.5pF 50V ±0.25pF SMT0402 NPO LR

MB_CLK_DDR2#

CN32

8 SMB_MA[15..0] → SMB_MA0 … SMB_MA15

8 SMB_DATA[63..0] → SMB_DATA0 … SMB_DATA63

8 MB_BA2 → MB_BA2

8 MB_BA1 → MB_BA1

8 MB_BA0 → MB_BA0

8 MB_CS0# → MB_CS0#

8 MB_CS1# → MB_CS1#

8 MB_CLK_DDR1 → MB_CLK_DDR1

8 MB_CLK_DDR1# → MB_CLK_DDR1#

8 MB_CLK_DDR2 → MB_CLK_DDR2

8 MB_CLK_DDR2# → MB_CLK_DDR2#

8 MB_CKE0 → MB_CKE0

8 MB_CKE1 → MB_CKE1

8 MB_CAS# → MB_CAS#

8 MB_RAS# → MB_RAS#

8 MB_WE# → MB_WE#

7,10,11,12,13,14,15,16,17,19,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57 3VDDM

R591 10KΩ 5% 1/16W SMT0402 LR

16,19 MEM_SMBCLK

16,19 MEM_SMBDATA

8 MB_ODT0 → ODT0

8 MB_ODT1 → ODT1

8 SMB_DQM[7..0] → SMB_DQM0 … SMB_DQM7

R595 10KΩ 5% 1/16W SMT0402 LR

8 SMB_SDQS[7..0] → SMB_DQS0 … SMB_DQS7

8 SMB_SDQSN[7..0] → SMB_DQSN0 … SMB_DQSN7

7,8,9,19,50,54 1.8VDDS

C742 C741

0.1uF 10V 10% SMT0402 X5R LR

2.2uF 10V ±10% SMT0603 X5R C1608X5R1A225KT TDK LR

7,10,11,12,13,14,15,16,17,19,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57 3VDDM

8 MB_CS2# → NC1

8 MB_CS3# → NC2

NC3 NC4 NCTEST

VREF1

GND0 GND1

VSS42 … VSS57

VDD1 … VDD12 VDDSPD

VSS1 … VSS41

STD TYPE

SCKT Foxconn Soft tray AS0A421-N2SN-4F DDR2 H5.2mm STD

19 DDR_D_VREF

T24 T23

54 DDR_VREF

JP20 0Ω 5% 1/10W SMT0603 LR

C446 0.1uF 10V 10% SMT0402 X5R LR

C448 2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

16,19 MEM_SMBCLK

16,19 MEM_SMBDATA

7,8,9,19,50,54 1.8VDDS

R303 10KΩ 1% 1/16W SMT0402 LR(NU)

T1

R302 10KΩ 1% 1/16W SMT0402 LR(NU)

16 PM_RSTBTN#

FOR DDR TEST (Near DDR Door)

LAYOUT GUIDE

Other signal	20mil	
DDR_VREF		20mil
Other signal	20mil	

LAYOUT GUIDE

Place one cap close to every 2 pullup resistors terminated to 0.9vddm

400 mils

DDR_0.9VDDM 8,19,54

RP18 RP17 RP16 RP15 RP14 RP19 RP20 RP21 RP22

47Ω 5% SMT1010 1/16W 4P2R RS2N-47R0-J2N CYNTEC LR

8 MB_CKE1 8 MB_CKE0 8 MB_BA2 8 MB_CS2# 8 MB_CS1# 8 MB_WE# 8 MB_CS0# 8 MB_ODT1 8 MB_CS3# 8 MB_BA0 8 MB_CAS# 8 MB_BA1 8 MB_RAS#

SMB_MA9 SMB_MA12 SMB_MA15 SMB_MA14 SMB_MA13 SMB_MA7 SMB_MA6 SMB_MA4 SMB_MA5 SMB_MA0 SMB_MA8 SMB_MA10 SMB_MA11 SMB_MA1 SMB_MA3

C442 C782 C445 C482 C729 C435 C441 C728 C781 C439 C731 C434 C443 C784

0.1uF 10V 10% SMT0402 X5R LR

1.8VDDS 7,8,9,19,50,54

120mil

7,8,9,19,50,54 1.8VDDS

C453 C411 C460 C779 C778 C458 C772 C456 C774

2.2uF 10V ±10% SMT0603 X5R C1608X5R1A225KT TDK LR

0.1uF 10V 10% SMT0402 X5R LR

Place these 2.2uF caps near So-Dimm0

Place these 0.1uF caps near So-Dimm0

SO DIMM 1

7,10,11,12,13,14,15,16,17,19,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57 3VDDM

Place cloase to DIMMs

D44 D43

16,19 MEM_SMBCLK

16,19 MEM_SMBDATA

MEM_SMBCLK

MEM_SMBDATA

DIODE SWITCHING BAV99 75V 150mA SOT-23 3PIN PSI LR

DIODE SWITCHING BAV99 75V 150mA SOT-23 3PIN PSI LR

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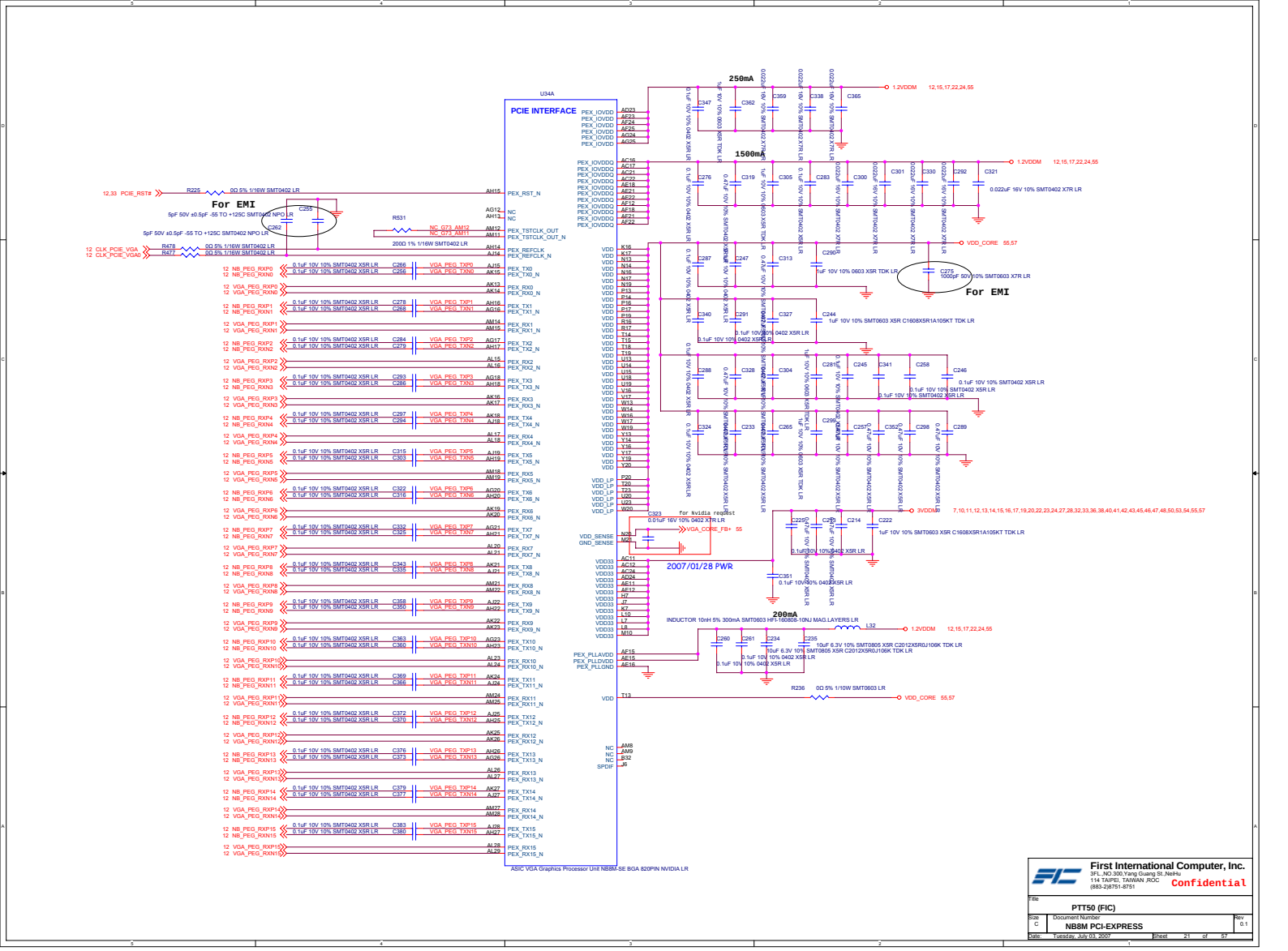
Title	PTT50 (FIC)	
Size C	Document Number DDRII SO-DIMM 1 STD	Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 20 of 57	


U34A
PCIE INTERFACE
ASIC VGA Graphics Processor Unit NB8M-SE BGA 820PIN NVIDIA LR
250mA
1500mA
200mA
1.2VDDM
VDD_CORE
3VDDM
For EMI
2007/01/28 PWR
for Nvidia request
INDUCTOR 10nH 5% 300mA SMT0603 HFI-1608S-10NJ MAG.LAYERS LR
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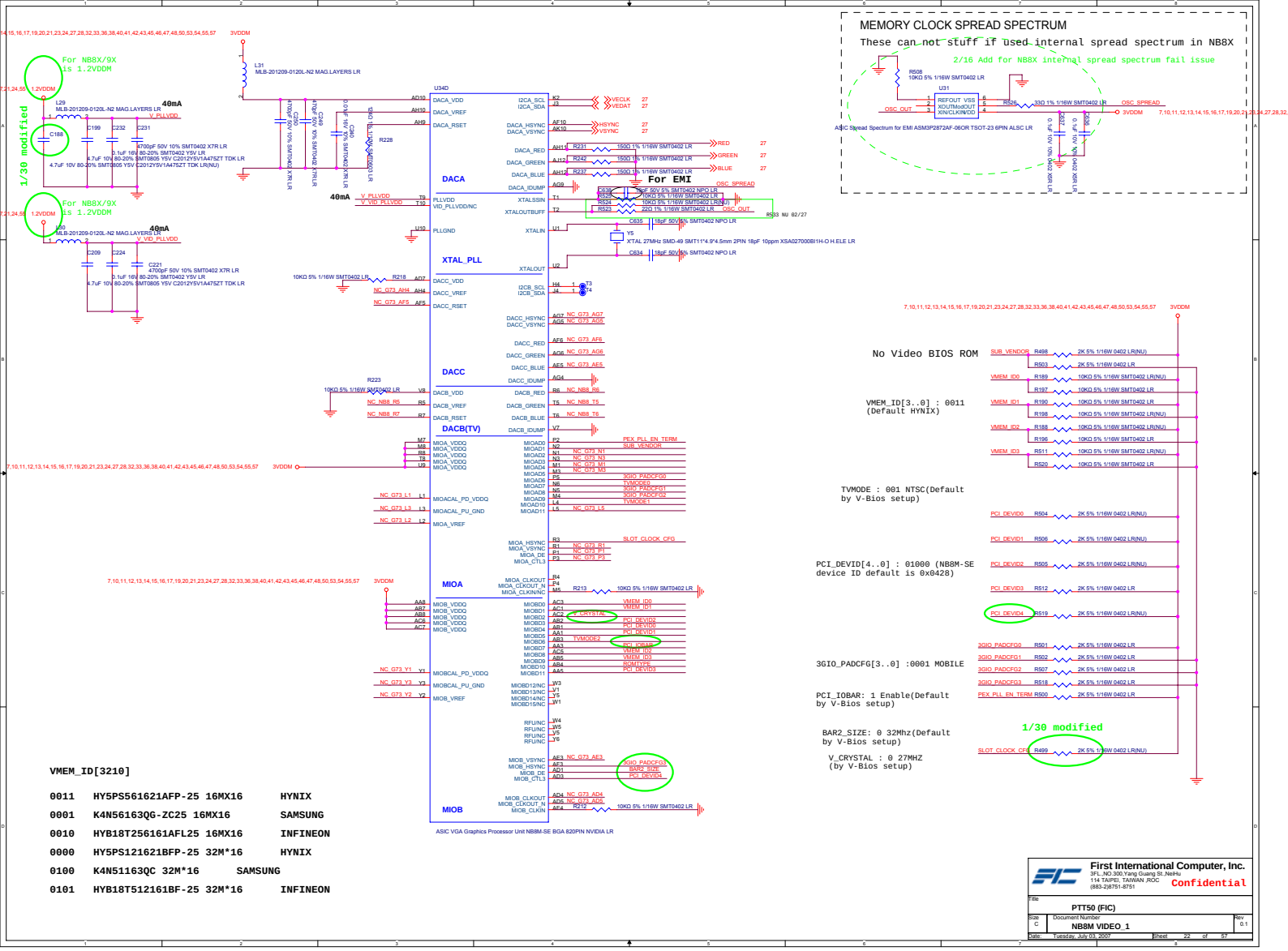
PTT50 (FIC)
NB8M PCI-EXPRESS
Tuesday, July 03, 2007
Sheet 21 of 57


MEMORY CLOCK SPREAD SPECTRUM
These can not stuff if used internal spread spectrum in NB8X
2/16 Add for NB8X internal spread spectrum fail issue
ASIC Spread Spectrum for EMI ASM3P2872AF-06OR TSOT-23 6PIN ALSC LR
For NB8X/9X is 1.2VDDM
1/30 modified
40mA
For EMI
XTAL 27MHz SMD-49 SMT11*4.9*4.5mm 2PIN 18pF 10ppm XSA027000BI1H-O H.ELE LR
ASIC VGA Graphics Processor Unit NB8M-SE BGA 820PIN NVIDIA LR
No Video BIOS ROM
VMEM_ID[3..0] : 0011
(Default HYNIX)
TVMODE : 001 NTSC(Default
by V-Bios setup)
PCI_DEVID[4..0] : 01000 (NB8M-SE
device ID default is 0x0428)
3GIO_PADCFG[3..0] :0001 MOBILE
PCI_IOBAR: 1 Enable(Default
by V-Bios setup)
BAR2_SIZE: 0 32Mhz(Default
by V-Bios setup)
V_CRYSTAL : 0 27MHZ
(by V-Bios setup)
1/30 modified
VMEM_ID[3210]
0011 HY5PS561621AFP-25 16MX16 HYNIX
0001 K4N56163QG-ZC25 16MX16 SAMSUNG
0010 HYB18T256161AFL25 16MX16 INFINEON
0000 HY5PS121621BFP-25 32M*16 HYNIX
0100 K4N51163QC 32M*16 SAMSUNG
0101 HYB18T512161BF-25 32M*16 INFINEON
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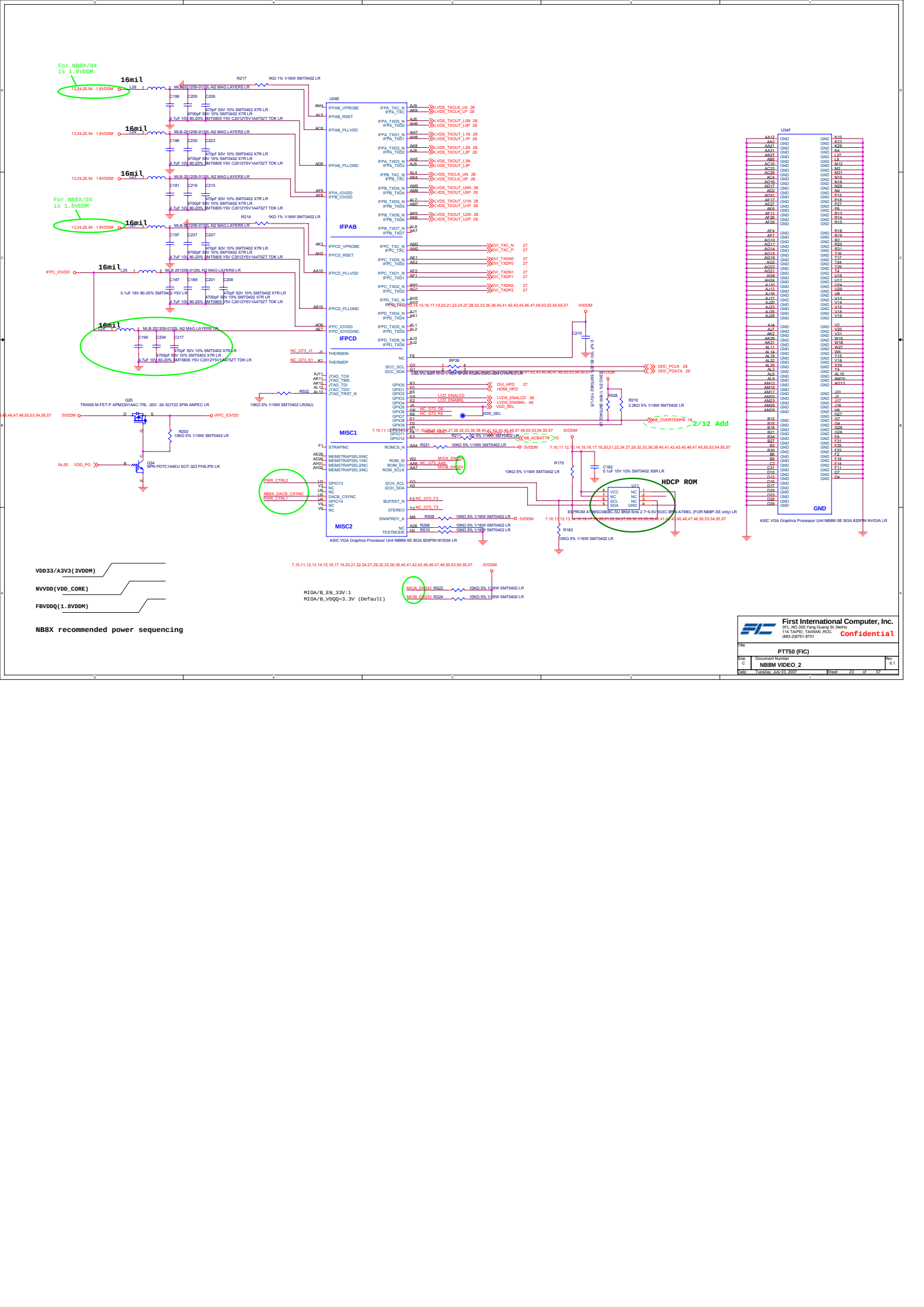
PTT50 (FIC)
NB8M VIDEO_1
Tuesday, July 03, 2007



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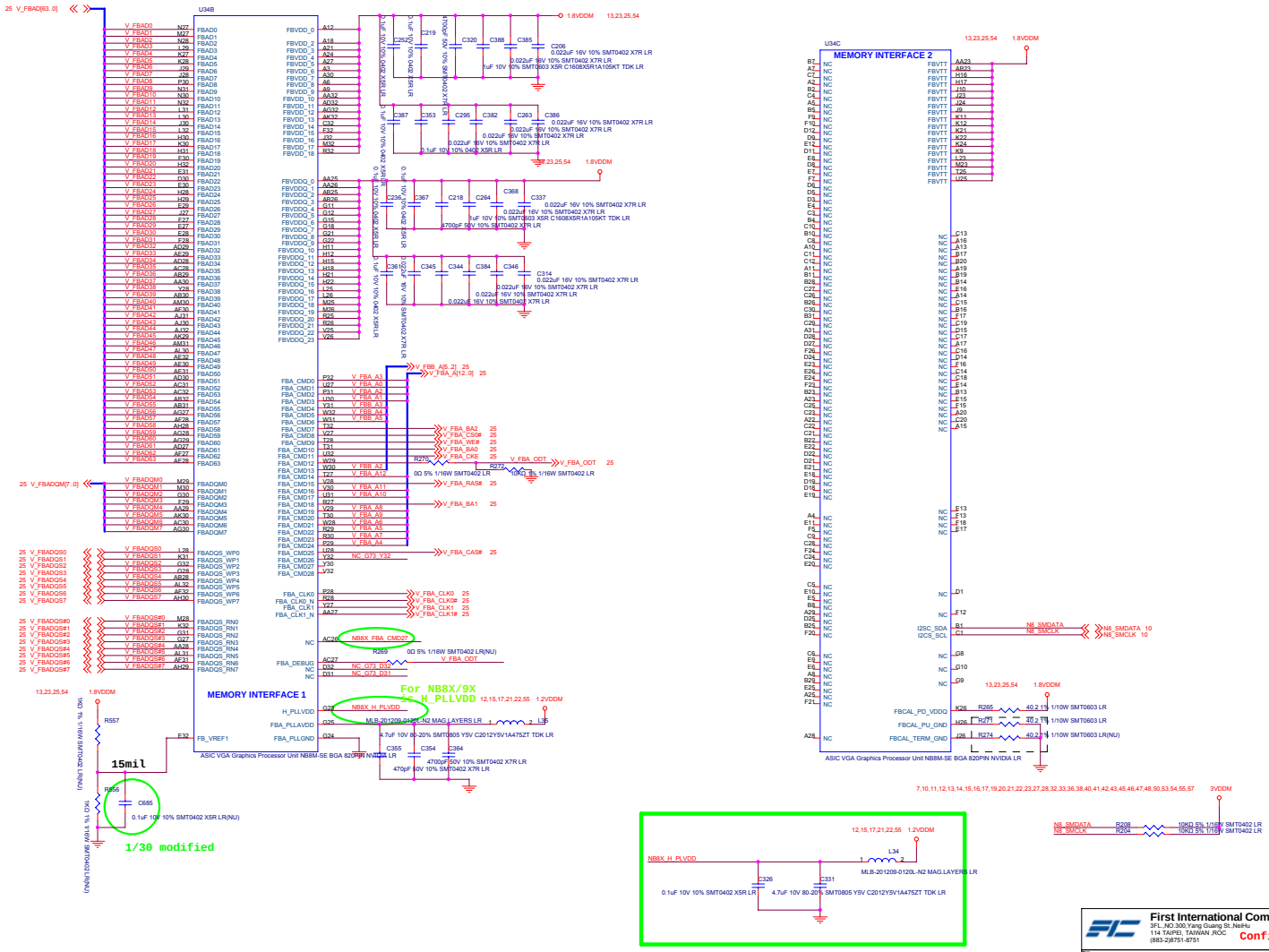
Title	PTT50 (FIC)		
Size C	Document Number NB8M VIDEO_2		Rev 0.1
Date: Tuesday, July 03, 2007		Sheet 23 of 57	


U34B
MEMORY INTERFACE 1
ASIC VGA Graphics Processor Unit NB8M-SE BGA 820PIN NVIDIA
U34C
MEMORY INTERFACE 2
ASIC VGA Graphics Processor Unit NB8M-SE BGA 820PIN NVIDIA
For NB8X/9X
H_PLLVDD
15mil
1/30 modified
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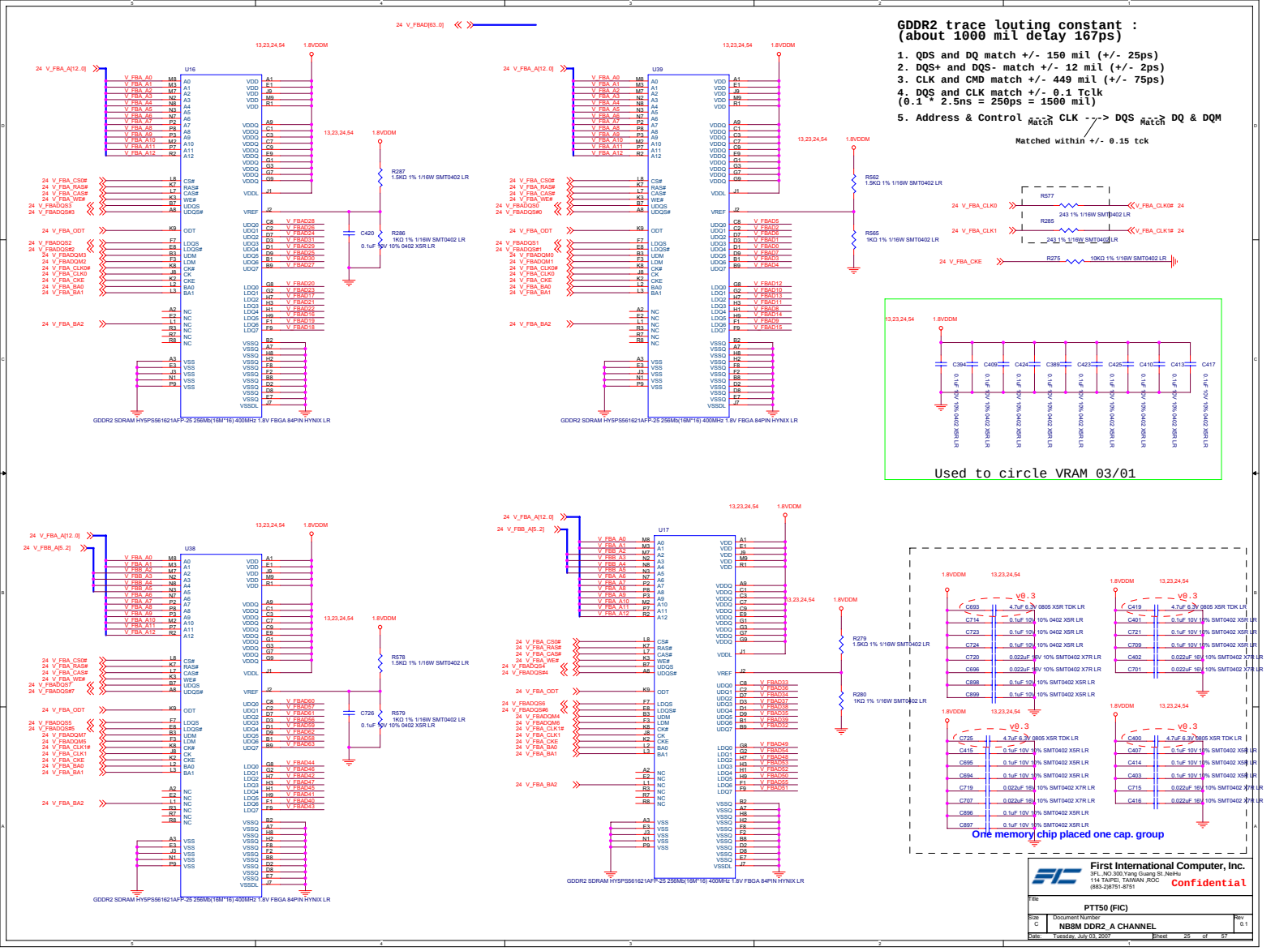
PTT50 (FIC)
NB8M MEM CHANEL
Tuesday, July 03, 2007



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Title	PTT50 (FIC)		
Size: C	Document Number: NB8M DDR2_A CHANNEL		Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 25 of 57		

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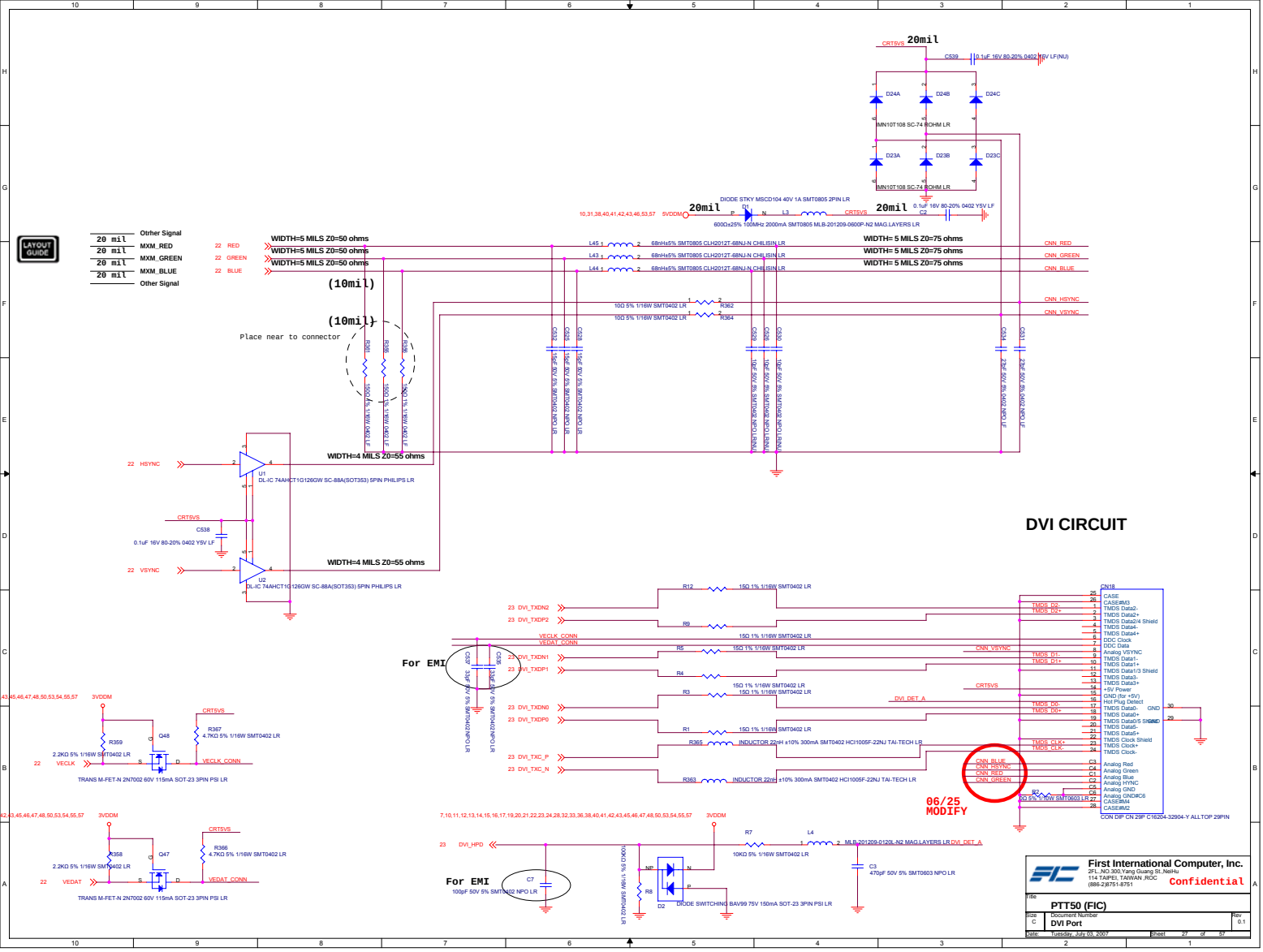
Title

PTT50 (FIC)

Size	Document Number	Rev
Custom	NB8M DDR2_C CHANNEL	0.1

Date: Tuesday, July 03, 2007 Sheet 26 of 57


DVI CIRCUIT
LAYOUT GUIDE
20 mil Othrer Signal
20 mil MXM_RED
20 mil MXM_GREEN
20 mil MXM_BLUE
20 mil Other Signal
22 RED
22 GREEN
22 BLUE
WIDTH=5 MILS Z0=50 ohms
WIDTH=5 MILS Z0=50 ohms
WIDTH=5 MILS Z0=50 ohms
(10mil)
(10mil)
Place near to connector
WIDTH=4 MILS Z0=55 ohms
WIDTH=4 MILS Z0=55 ohms
22 HSYNC
22 VSYNC
U1
U2
DL-IC 74AHCT1G126GW SC-88A(SOT353) 5PIN PHILIPS LR
CRT5VS
C538
0.1uF 16V 80-20% 0402 Y5V LF
20mil
C539
0.1uF 16V 80-20% 0402 Y5V LF(NU)
D24A
D24B
D24C
MMN10T108 SC-74 8OHM LR
D23A
D23B
D23C
MMN10T108 SC-74 8OHM LR
DIODE STKY MSCD104 40V 1A SMT0805 2PIN LR
10,31,38,40,41,42,43,46,53,57 5VDDM
L3
C2
600Ω±25% 100MHz 2000mA SMT0805 MLB-201209-0600P-N2 MAG LAYERS LR
WIDTH= 5 MILS Z0=75 ohms
WIDTH= 5 MILS Z0=75 ohms
WIDTH= 5 MILS Z0=75 ohms
CNN_RED
CNN_GREEN
CNN_BLUE
CNN_HSYNC
CNN_VSYNC
L45
L43
L44
68nH±5% SMT0805 CLH2012T-68NJ-N CHILISIN LR
10Ω 5% 1/16W SMT0402 LR
R362
R364
For EMI
R12
R9
R5
R4
R3
R1
R365
R363
15Ω 1% 1/16W SMT0402 LR
INDUCTOR 22nH ±10% 300mA SMT0402 HCI1005F-22NJ TAI-TECH LR
23 DVI_TXDN2
23 DVI_TXDP2
23 DVI_TXDN1
23 DVI_TXDP1
23 DVI_TXDN0
23 DVI_TXDP0
23 DVI_TXC_P
23 DVI_TXC_N
VECLK_CONN
VEDAT_CONN
CRT5VS
DVI_DET_A
CN18
CON DIP CN 29P C16204-32904-Y ALLTOP 29PIN
TMDS_D2-
TMDS_D2+
TMDS_D1-
TMDS_D1+
TMDS_D0-
TMDS_D0+
TMDS_CLK+
TMDS_CLK-
CNN_BLUE
CNN_HSYNC
CNN_RED
CNN_GREEN
R2
2Ω 5% 1/16W SMT0603 LR
06/25
MODIFY
43,45,46,47,48,50,53,54,55,57 3VDDM
R359
2.2KΩ 5% 1/16W SMT0402 LR
Q48
R367
4.7KΩ 5% 1/16W SMT0402 LR
22 VECLK
VECLK_CONN
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
42,43,45,46,47,48,50,53,54,55,57 3VDDM
R358
2.2KΩ 5% 1/16W SMT0402 LR
Q47
R366
4.7KΩ 5% 1/16W SMT0402 LR
22 VEDAT
VEDAT_CONN
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57 3VDDM
23 DVI_HPD
For EMI
C7
100pF 50V 5% SMT0402 NPO LR
R7
10KΩ 5% 1/16W SMT0402 LR
L4
MLB-201209-0120L-N2 MAG LAYERS LR
C3
470pF 50V 5% SMT0603 NPO LR
R8
D2
DIODE SWITCHING BAV99 75V 150mA SOT-23 3PIN PSI LR
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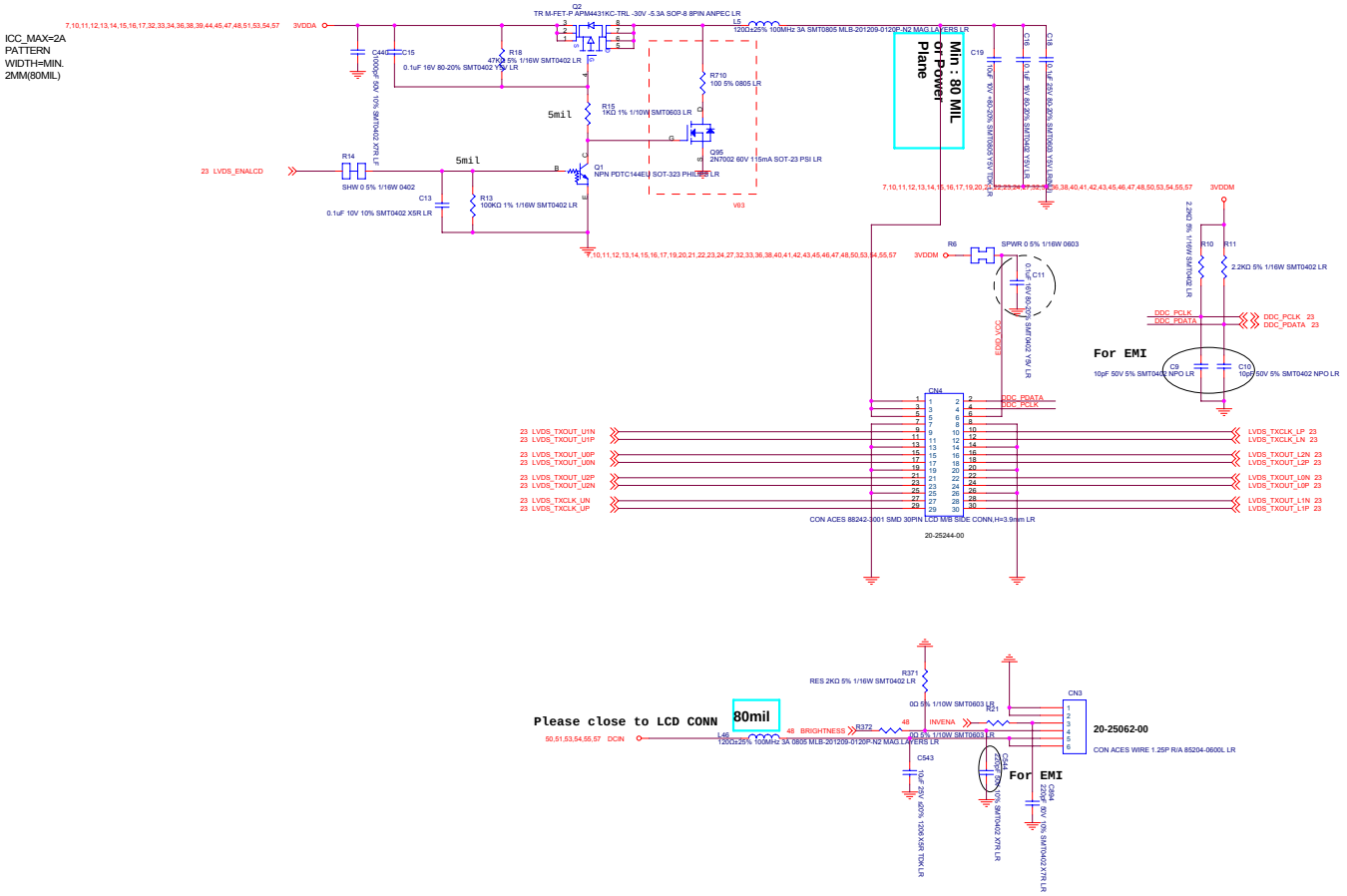
PTT50 (FIC)
DVI Port
Tuesday, July 03, 2007
Sheet 27 of 57



First International Computer, Inc.		
3FL, NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)8751-8751	Confidential	
Title: Orion A/AM(PB) MTN70/PTB72(FIC)		
Size: C	Document Number: LCD CNN	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 28 of 57	

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Title

PTT50 (FIC)

Size	Document Number	Rev
C	HDMI CNN	0.1

Date: Tuesday, July 03, 2007 Sheet 29 of 57

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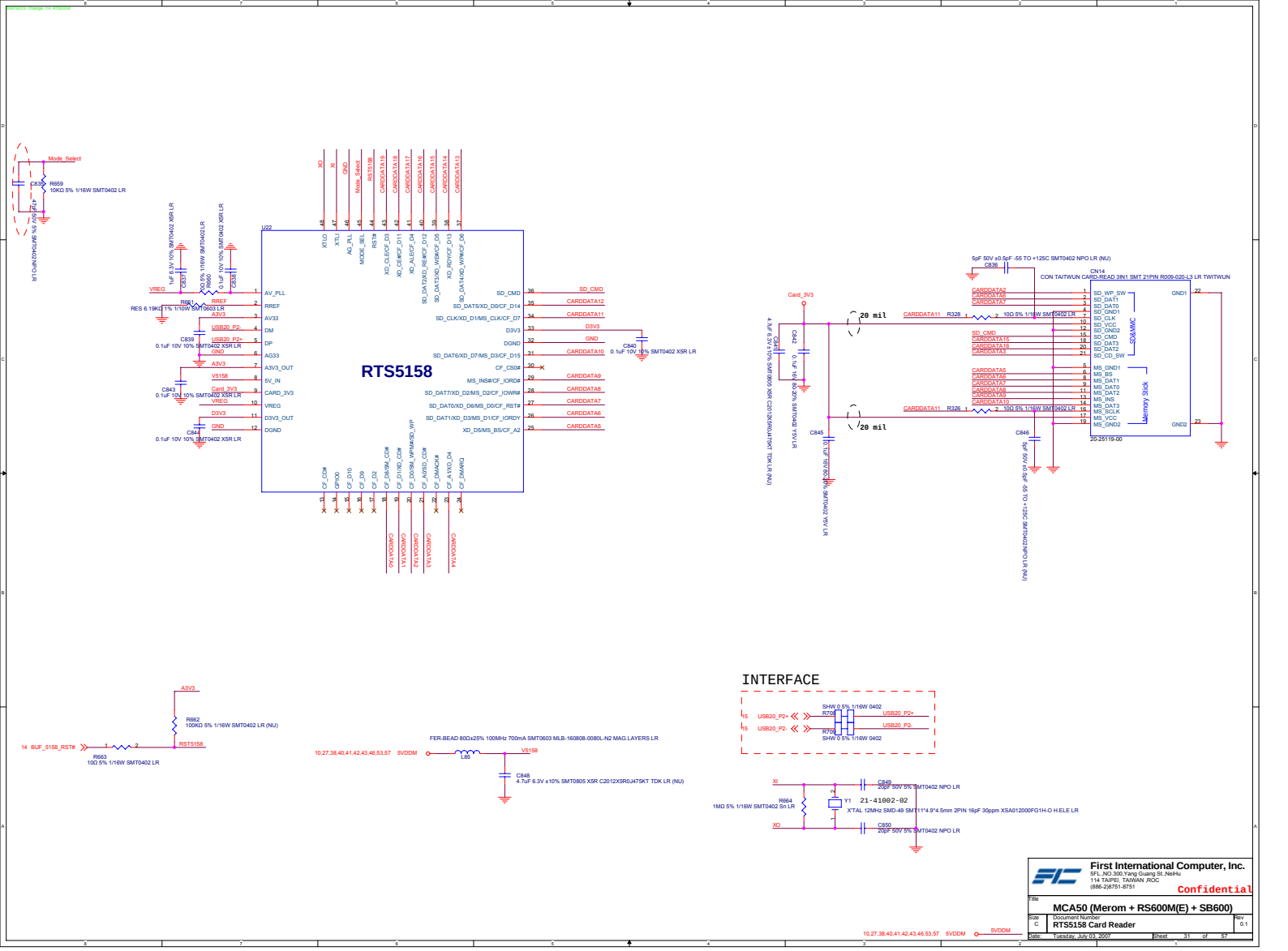
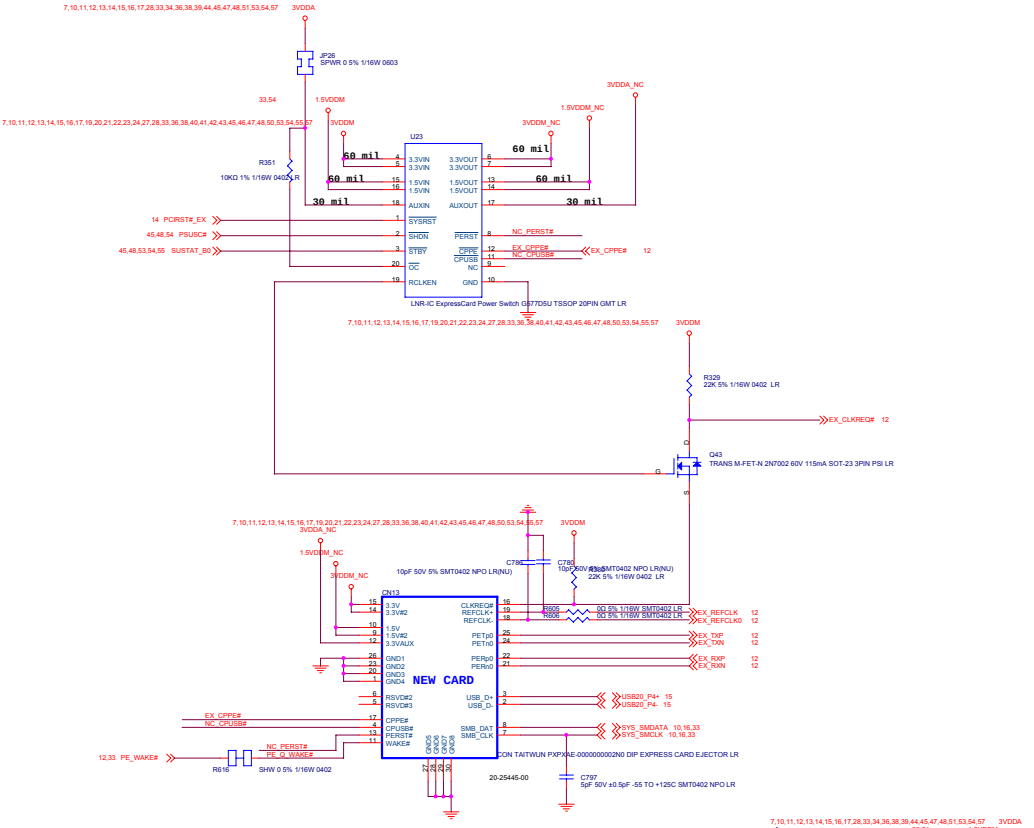
Title: PTT50 (FIC)

Size	Document Number	Rev
C	VIA VT6311S(1394)	0.1

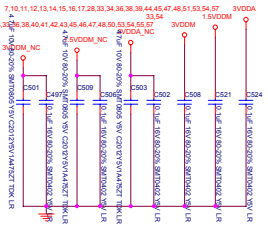
Date: Tuesday, July 03, 2007 Sheet 30 of 57


RTS5158
INTERFACE
CN14
CON TAITWUN CARD-READ 3IN1 SMT 21PIN R009-020-L3 LR TWITWUN
20-25119-00
First International Computer, Inc.
Confidential
MCA50 (Merom + RS600M(E) + SB600)
RTS5158 Card Reader
Tuesday, July 03, 2007



Express Card Ejector : 20-25445-00

Express Card Header : 20-25446-00



First International Computer, Inc.		
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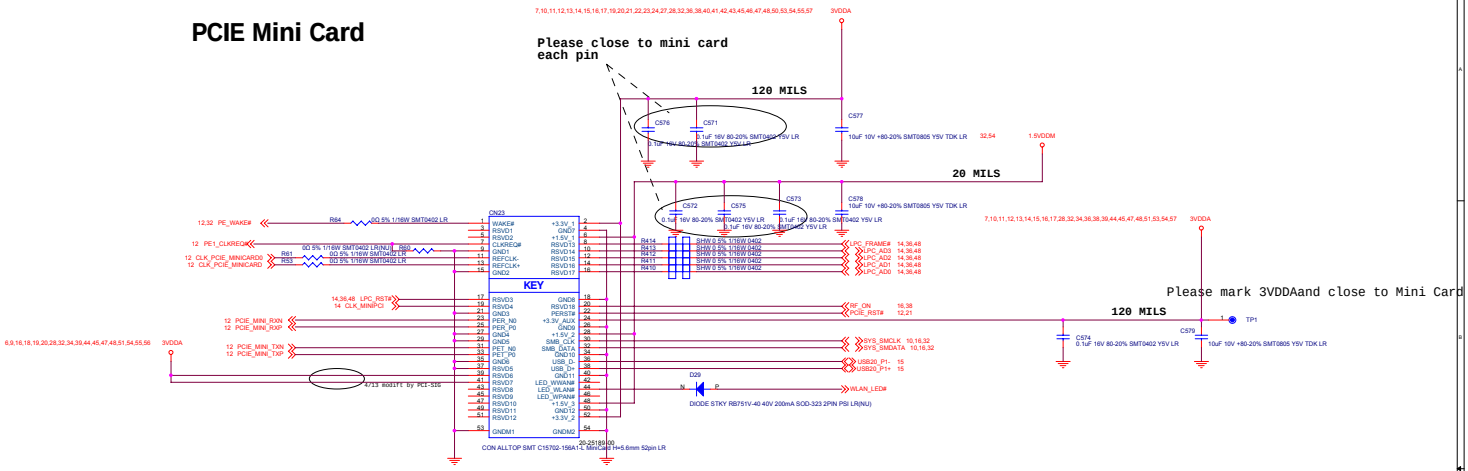
Title: PTT50 (FIC)		
Size: C	Document Number: New Card(express card)	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 32 of 57	

PCIE Mini Card



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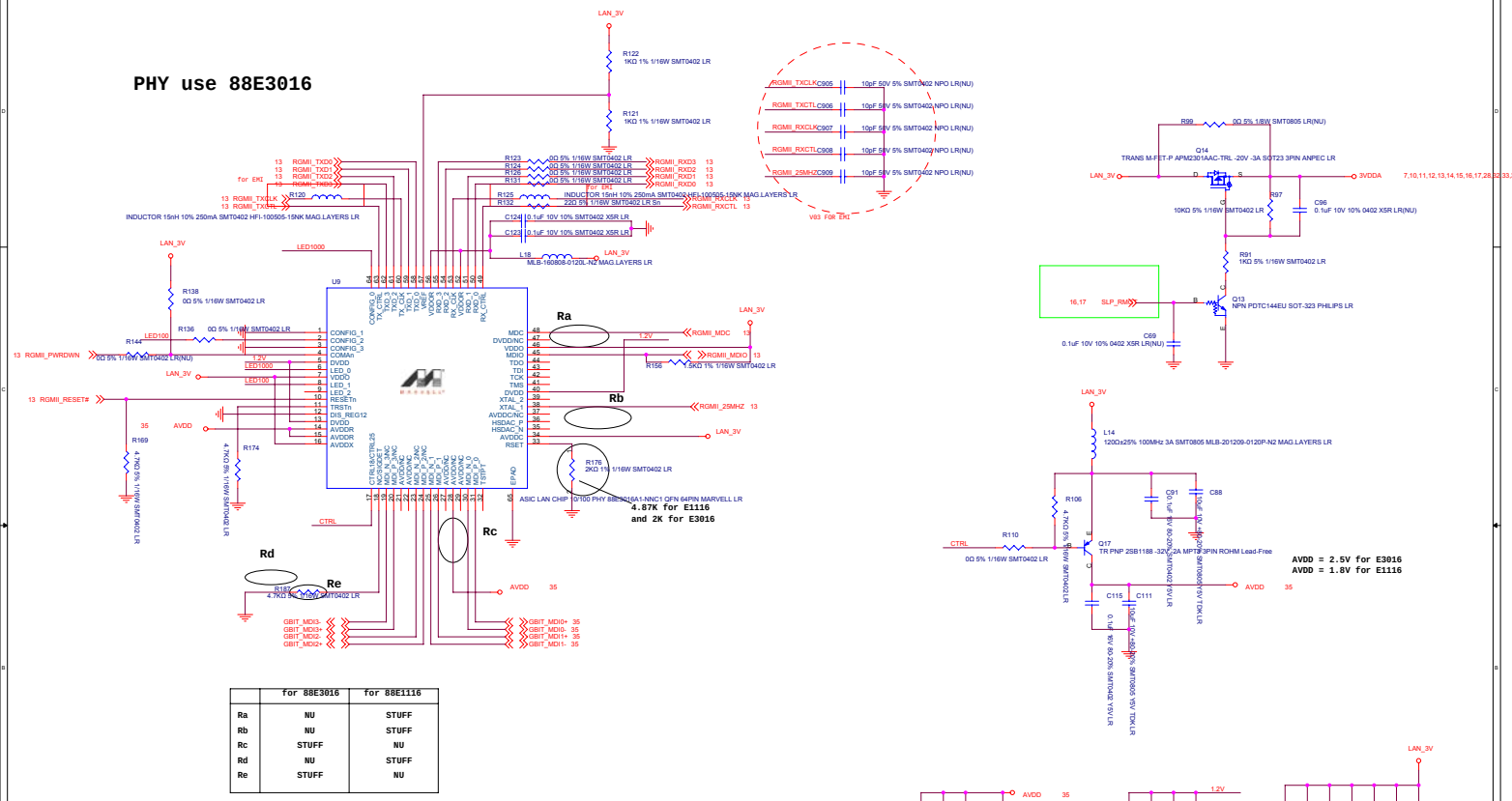
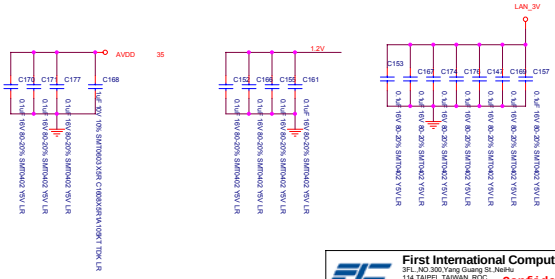
File: PTT50 (FIC)

Size	Document Number	Rev
C	PCIE Mini Card	0.1

Date: Tuesday, July 03, 2007 Sheet 33 of 57

PHY use 88E3016





	for 88E3016	for 88E1116
Ra	NU	STUFF
Rb	NU	STUFF
Rc	STUFF	NU
Rd	NU	STUFF
Re	STUFF	NU

Layout Guide

1. The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip,and away from signal traces(ex:MDI0+/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. The termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as possible to the power pins,such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer,and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum lenghth between Lan Chip and transfer is achievable only when there's no interferences around.
9. All 4 pairs of the differential resister(49.9k) must close to Lan Chip,and make them(4pairs) as same as distant.
10. PLACE GND PLANE AS LARGE AS POSSIBLE
11. If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.
12. It's important to separate digital signals from analog signals.If it is unavoidable to cross digtal signals with analong power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15. The Lan Chip pin 1 facing the transformer,then you can make the signal shorter.

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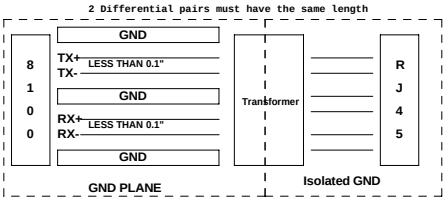
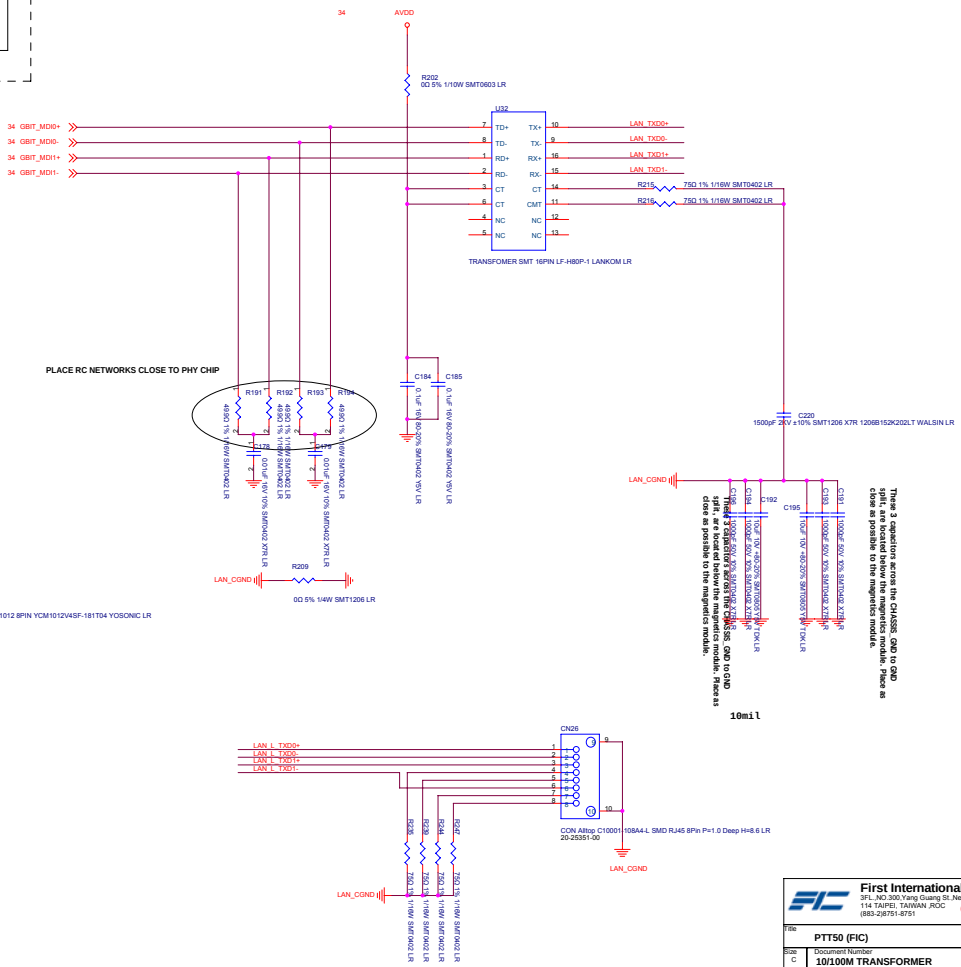
Title	PTT50 (FIC)	
Size C	Document Number 10/100M PHY 88E3016	Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 34 of 57	

TX
RX

100 ohm ---> trace 4 mil , space 10 mil
50 mil space from other signals
Total Tace Length no more thans 4.8"
2 Differential pairs must have the same length





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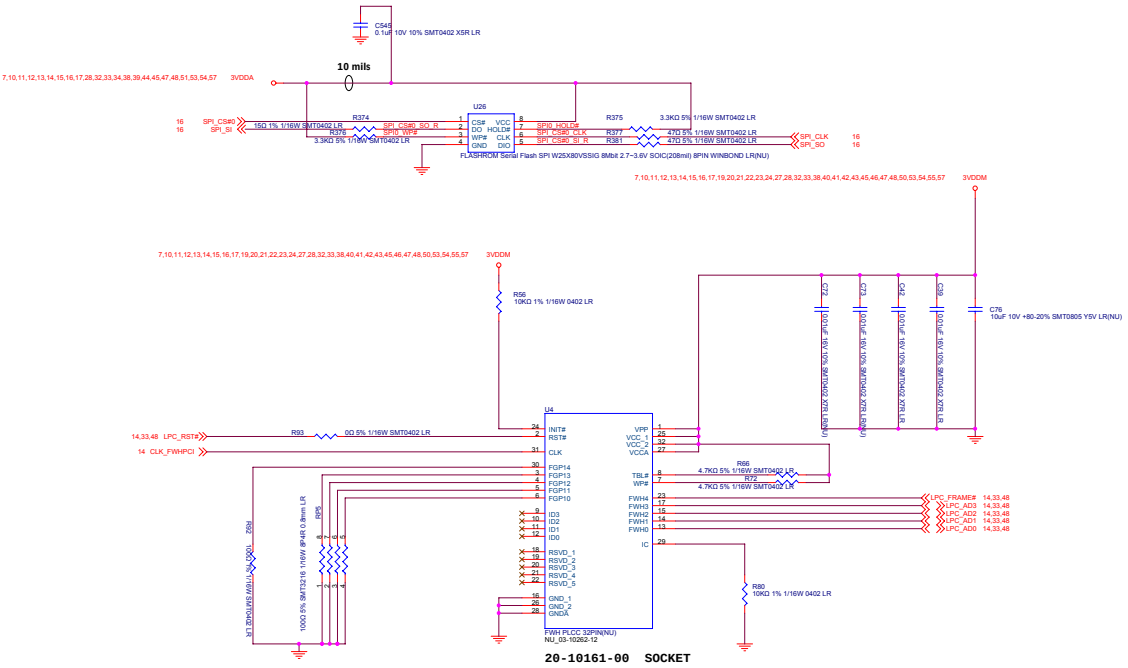
Title: PTT50 (FIC)

Size: C | Document Number: 10/100M TRANSFORMER | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 35 of 57

SPI Interface



20-10161-00 SOCKET

03-10262-12 Flash ROM PM49FL004TL-33JCE
4Mbit(512K*8) PMC LR

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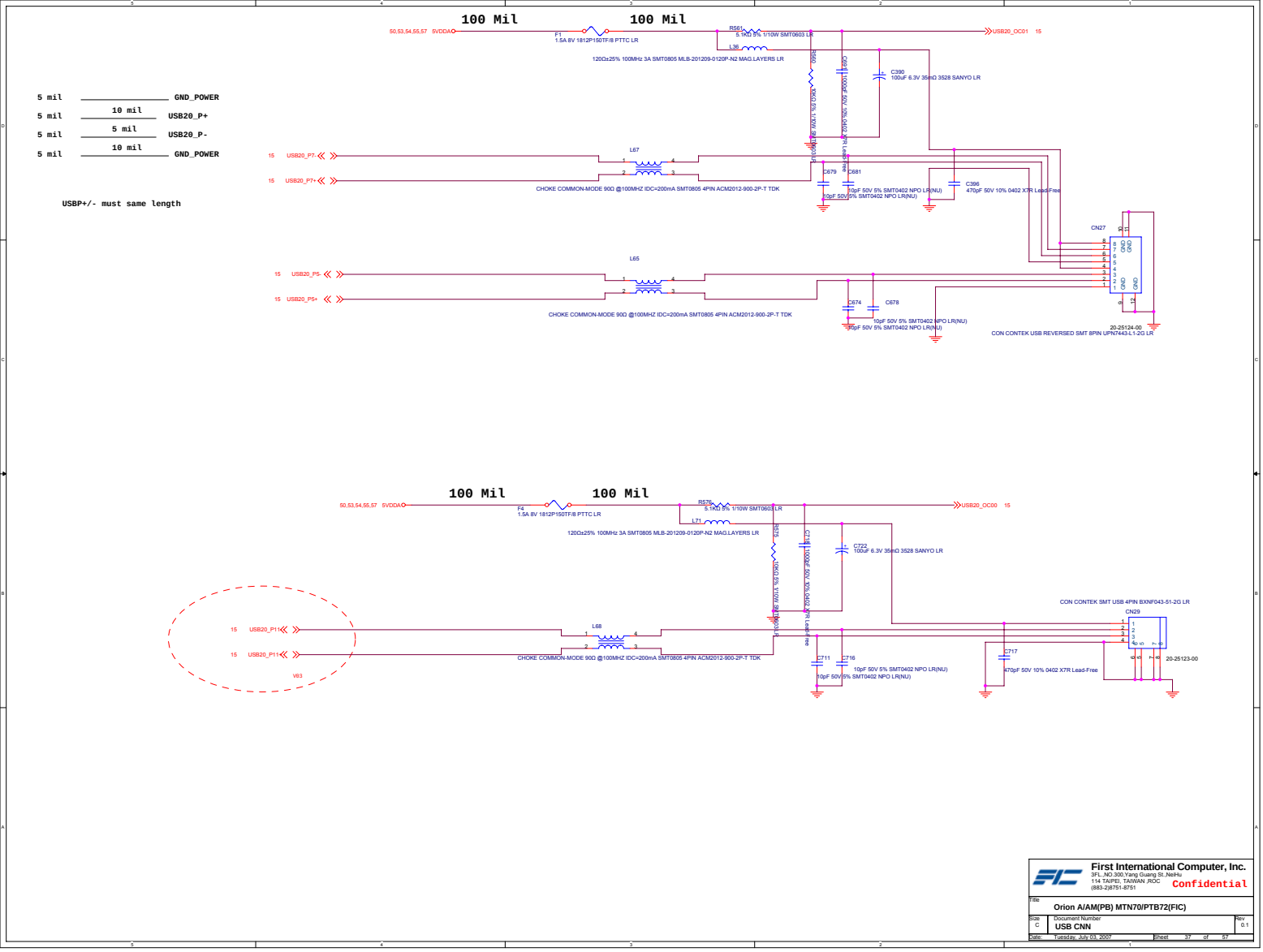
Title	PTT50 (FIC)	
Size C	Document Number: SPI FLASH ROM	Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 36 of 57	



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Title	Orion A/AM(PB) MTN70/PTB72(FIC)	
Size: C	Document Number: USB CNN	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 37 of 57	

LED indicator control logic

CN5
CN 18PIN 88296-1801 ACES 88503-1801

BUZZR
Q30 TRANS NPN MMBT2222A 40V 600mA SOT-23 3PIN PSI LR
BUZZER 30.0±4.5Ω 5V KSTG954RP/HA KINGSTATE LR

Wireless indicator
v0.3
direction changed
LED Amber/Blue SMT0603 λp=609/468nm HT-297UD/CB HARVATEK LR
PDTC144EU SOT-323 PHILIPS LR
PS355NS 80V 100mA SMT0805 2PIN PSI LR
BAV70 75V 150mA SOT-23 PSI LR
LED BLUE λp=470nm SMT0603 HT-19NB8/HARVATEK LR
SWITCH 3PIN NSS507-212F-FAAG1T T-MEC LR

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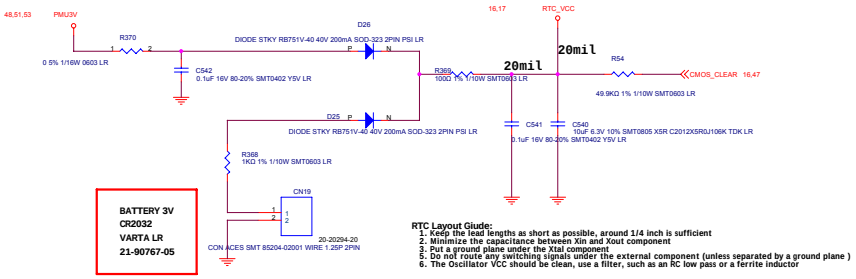
Title	PTT50 (FIC)	
Size: C	Document Number: LED / SW CN	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 38 of 57	

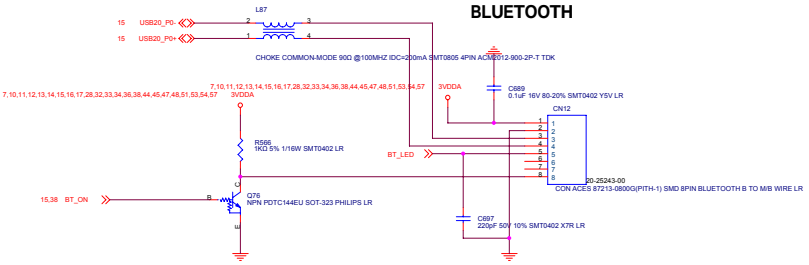
RTC Discharge Circuit



RTC Layout Giude:

1. Keep the lead lengths as short as possible, around 1/4 inch is sufficient
2. Minimize the capacitance between Xin and Xout component
3. Put a ground plane under the Xtal component
5. Do not route any switching signals under the external component (unless separated by a ground plane)
6. The Oscillator VCC should be clean, use a filter, such as an RC low pass or a ferrite inductor

BLUETOOTH



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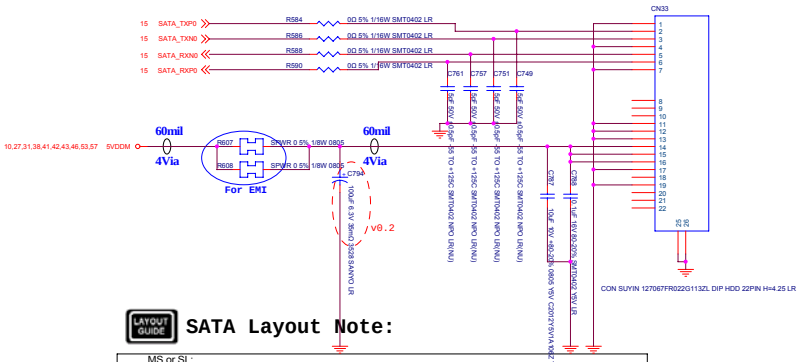
Size: C	Document Number: RTC/ Bluetooth CNN	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 39 of 57	

HDD I/F



SATA Layout Note:

MS or SL:

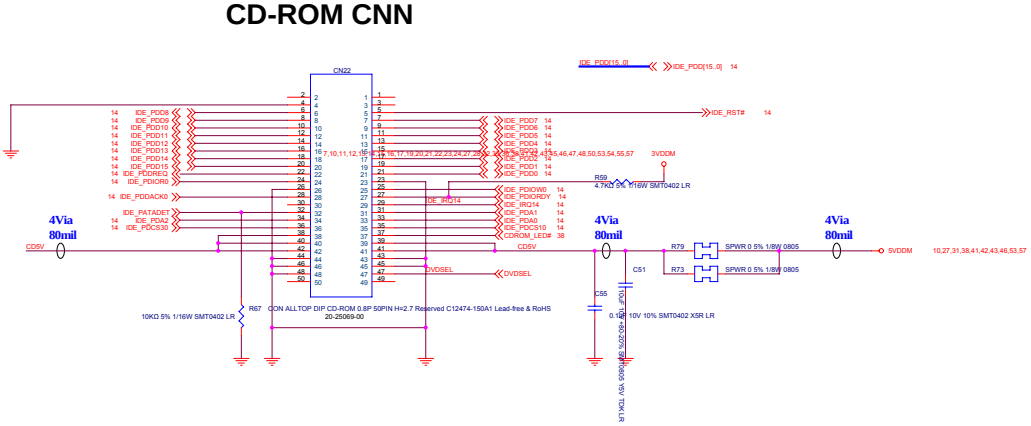
5mils 5mils 5mils 5mils

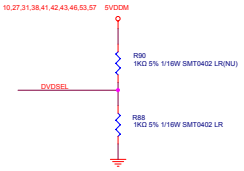
20mils 8mils 20mils 8mils 20mils

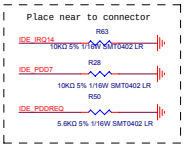
TX RX

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

CD-ROM CNN







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Title	PTT50 (FIC)	
Size: C	Document Number: SATA HD / CD-ROM CNN	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 40 of 57	

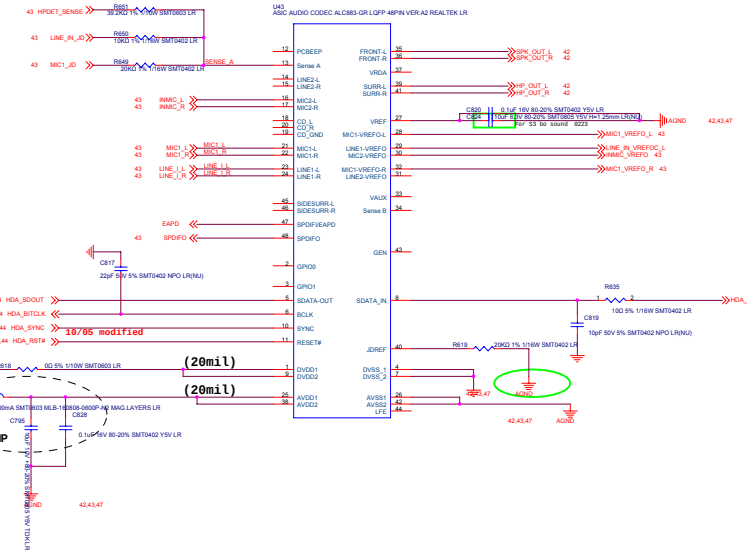
10mil GND_POWER
10mil 10mil AZALIA_PCBEEP
10mil 10mil GND_POWER

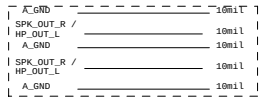
10mil GND_POWER
10mil 10mil AZALIA_BITCLK
10mil 10mil GND_POWER

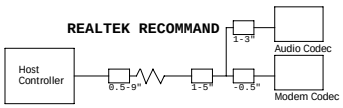
10mil GND_POWER
10mil 10mil 14MCLK_AZALIA
10mil 10mil GND_POWER

Layout guide :

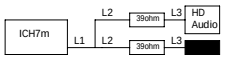
1. Close to codec.
2. Realtek suggested that layout trace of the sense pin should away form any analog trace because sensing current might distorts the audio performance (The bottom lay is best choice).







HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#



Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.5"~2.5" L2 <= 0.1" L3 = 1"~8"

*** L3 can be extened up to 15" if HD Audio docking is not used

HD Audio-ACZ_SDIN

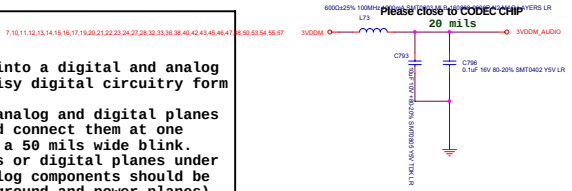
Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.1"~15" L2 <= 0.5"

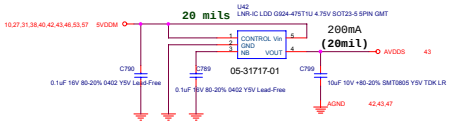
*** Breakout can be routed 4 on 4 up to 500 mils

AZALIA CODEC POWER

Layout guide :

1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry form quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.





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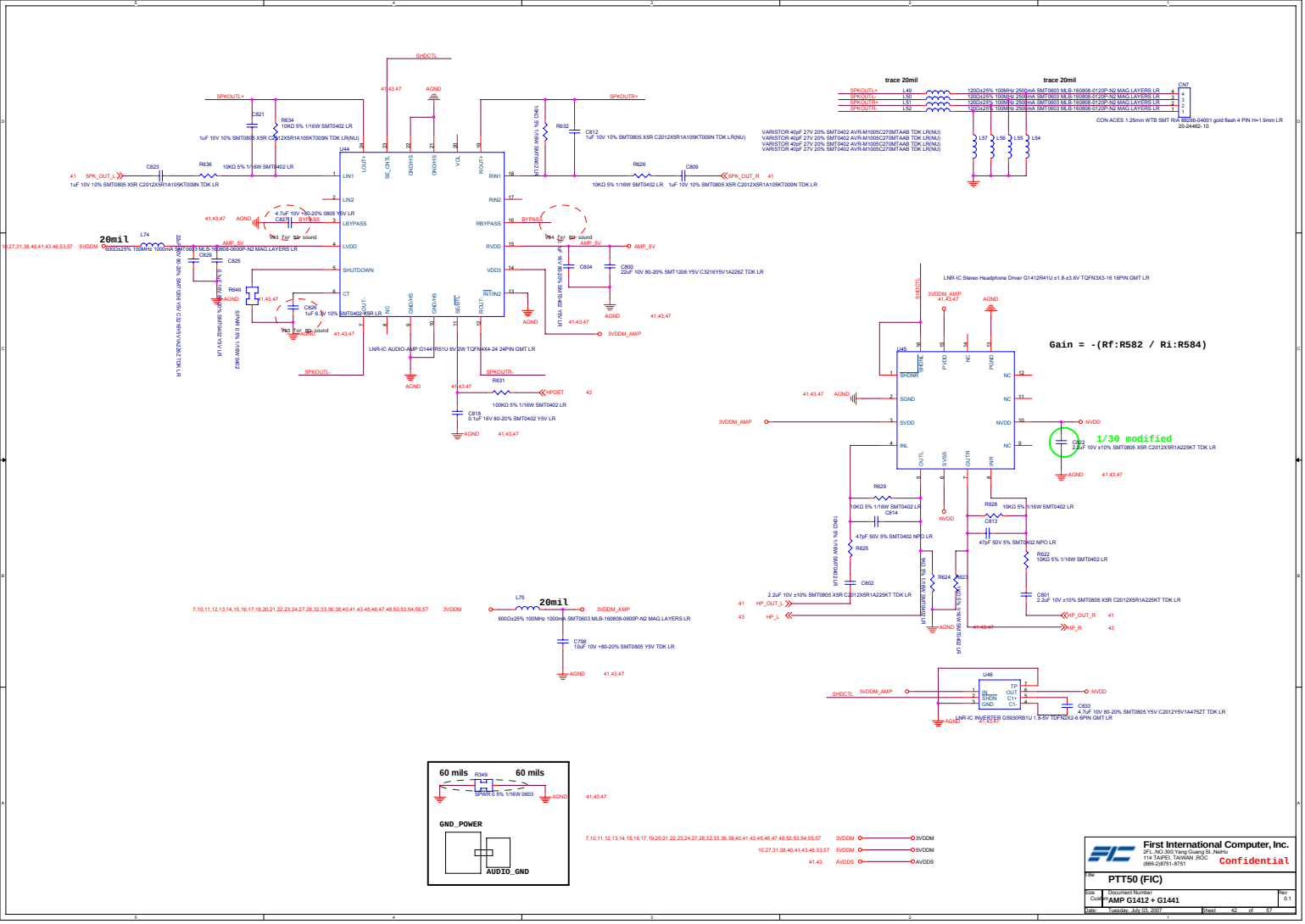
File	PTT50 (FIC)	
Size C	Document Number Azalia ALC268 Codec	Rev 0.1
Date: Tuesday, July 03, 2007	Sheet 41 of 57	



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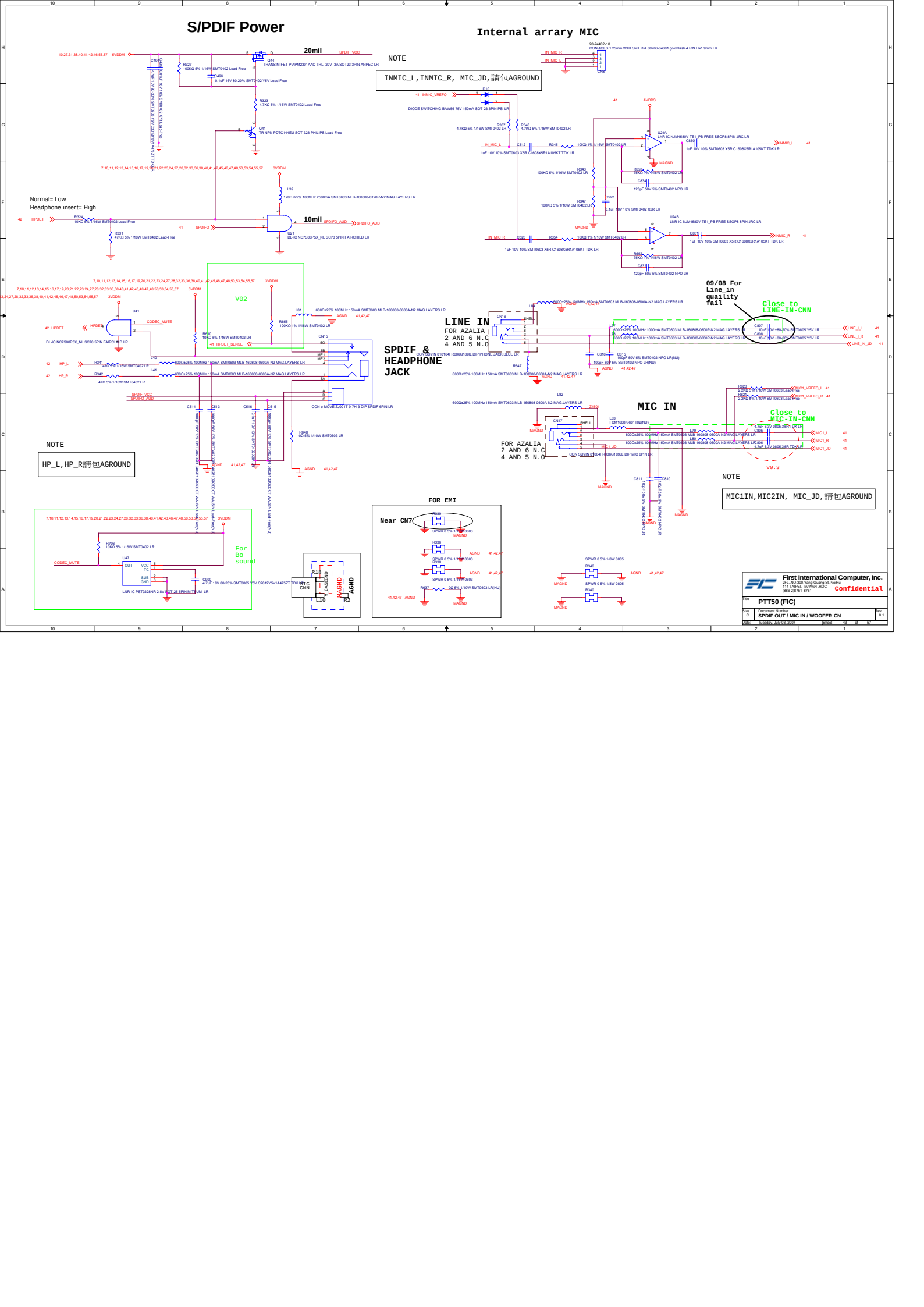
Size	Document Number: AMP G1412 + G1441
Rev	0.1
Date	Tuesday, July 03, 2007
Sheet	42 of 57


S/PDIF Power
Internal arrary MIC
20mil
10mil
NOTE
INMIC_L,INMIC_R, MIC_JD,請包AGROUND
Normal= Low
Headphone insert= High
V02
LINE IN
FOR AZALIA
2 AND 6 N.C
4 AND 5 N.O
SPDIF &
HEADPHONE
JACK
09/08 For
Line_in
quaility
fail
Close to
LINE-IN-CNN
MIC IN
Close to
MIC-IN-CNN
FOR AZALIA
2 AND 6 N.C
4 AND 5 N.O
v0.3
NOTE
HP_L,HP_R請包AGROUND
NOTE
MIC1IN,MIC2IN, MIC_JD,請包AGROUND
FOR EMI
Near CN7
For
Bo
sound
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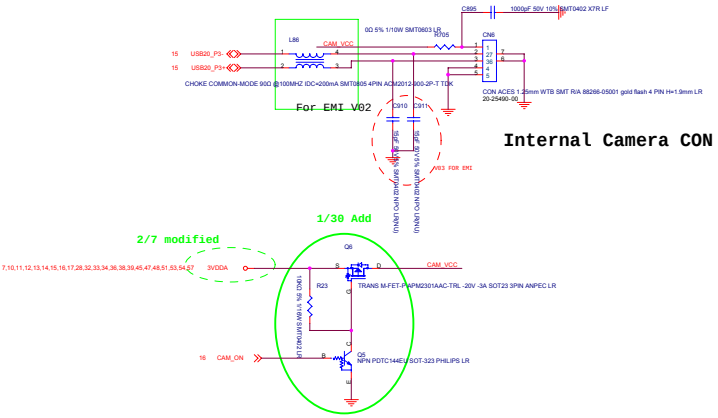
PTT50 (FIC)
SPDIF OUT / MIC IN / WOOFER CN



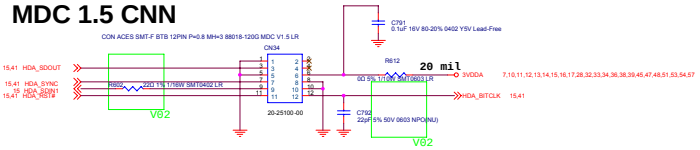
HD Audio-ACZ_SDIN (MDC Connector)

ICH7m	L1	MDC Conn	L2	39ohm	L3	HD Audio

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline)	L1 = 0.1"~15" L2 = 0.5"~1.5" L3 = 0.5"

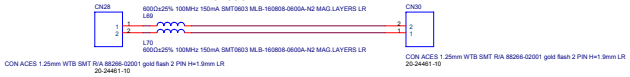
*** Breakout can be routed 4 on 4 up to 400 mils

MDC 1.5 CNN



FOR EMI Solution

Close



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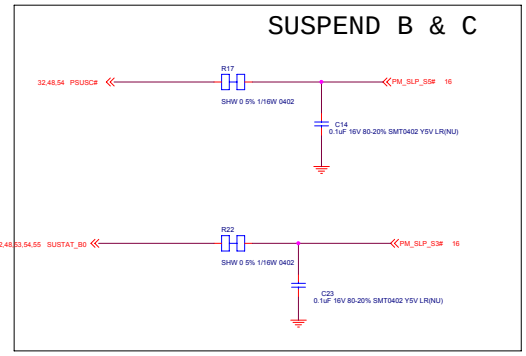
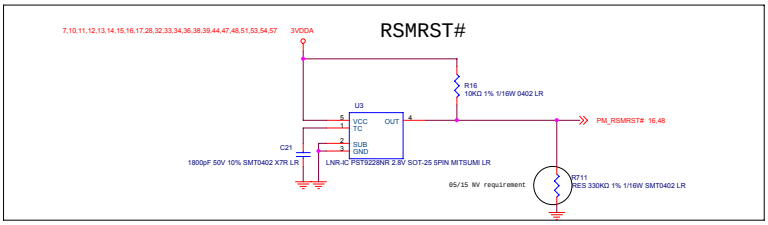
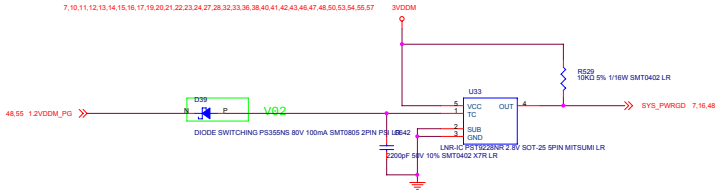
Size	Document Number	Rev
C	Camera + MIC CNN/MDC CNN	0.1

Date: Tuesday, July 03, 2007 Sheet 44 of 57



RESUME RESET





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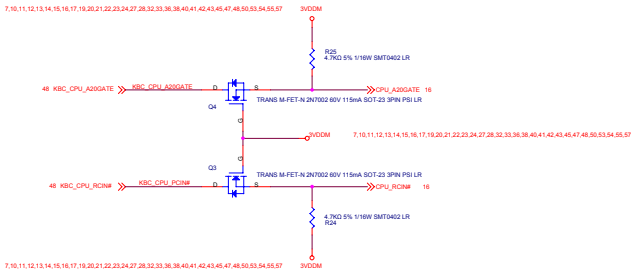
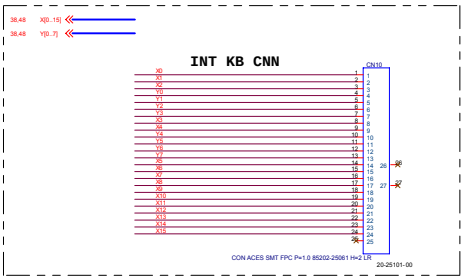
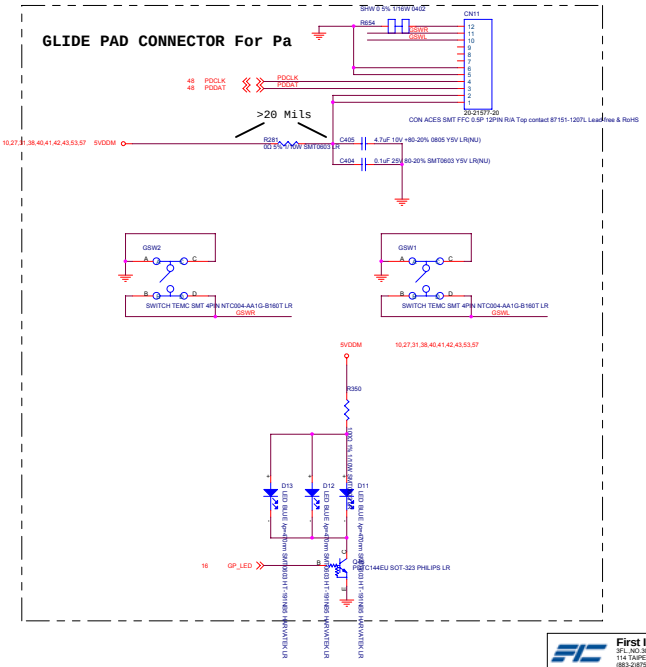
Title	PTT50 (FIC)	
Size: C	Document Number: Reset Circuit	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 45 of 57	







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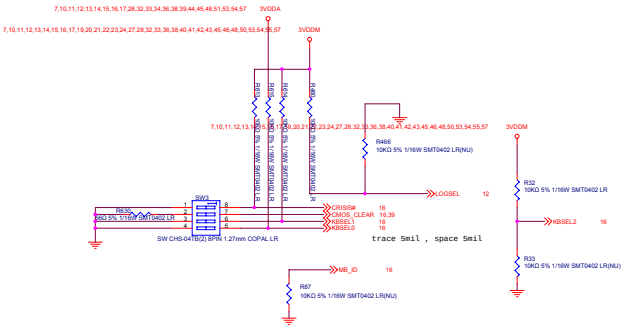
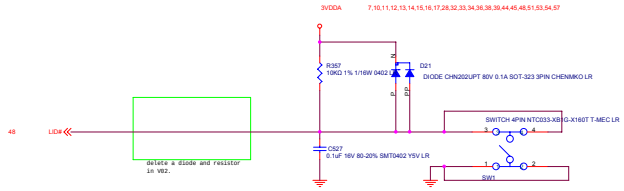
Size	Document Number	Rev
C	KB CNN/GP CNN	0.1

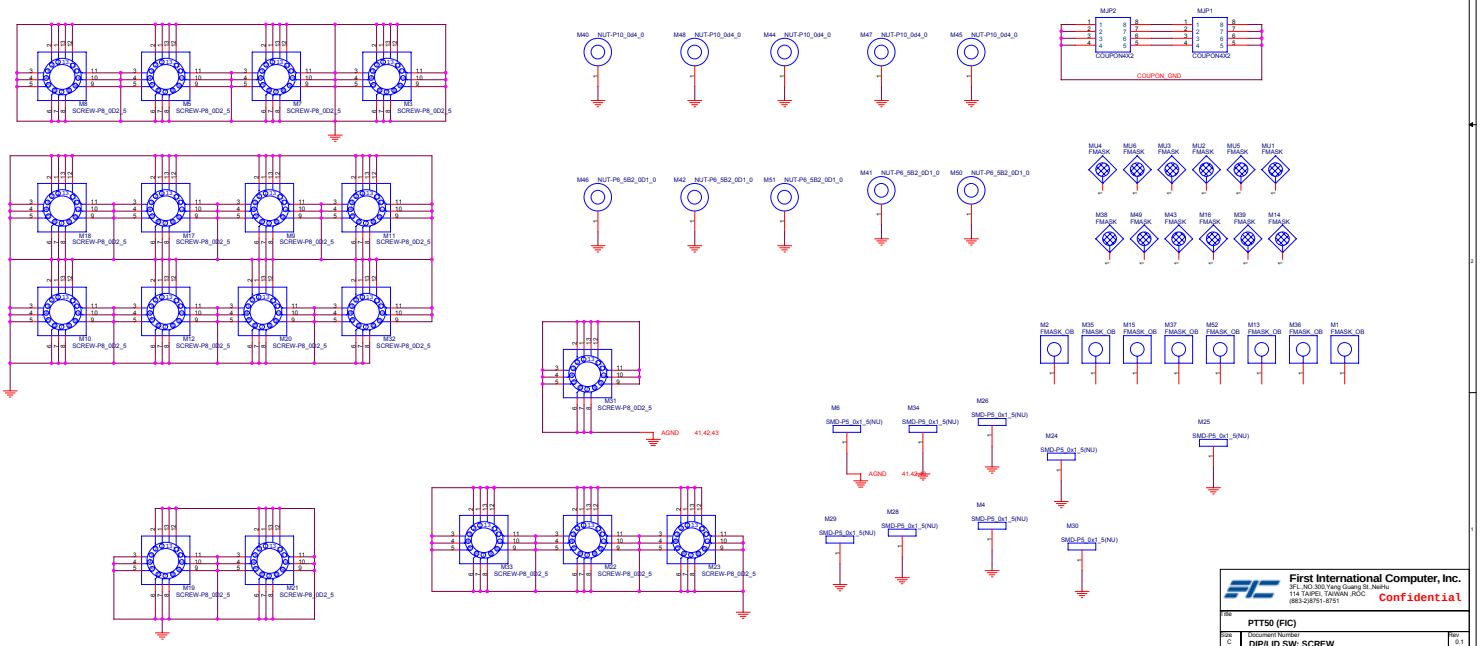
Date: Tuesday, July 03, 2007 Sheet 48 of 57

DIP SWITCH



LID Switch





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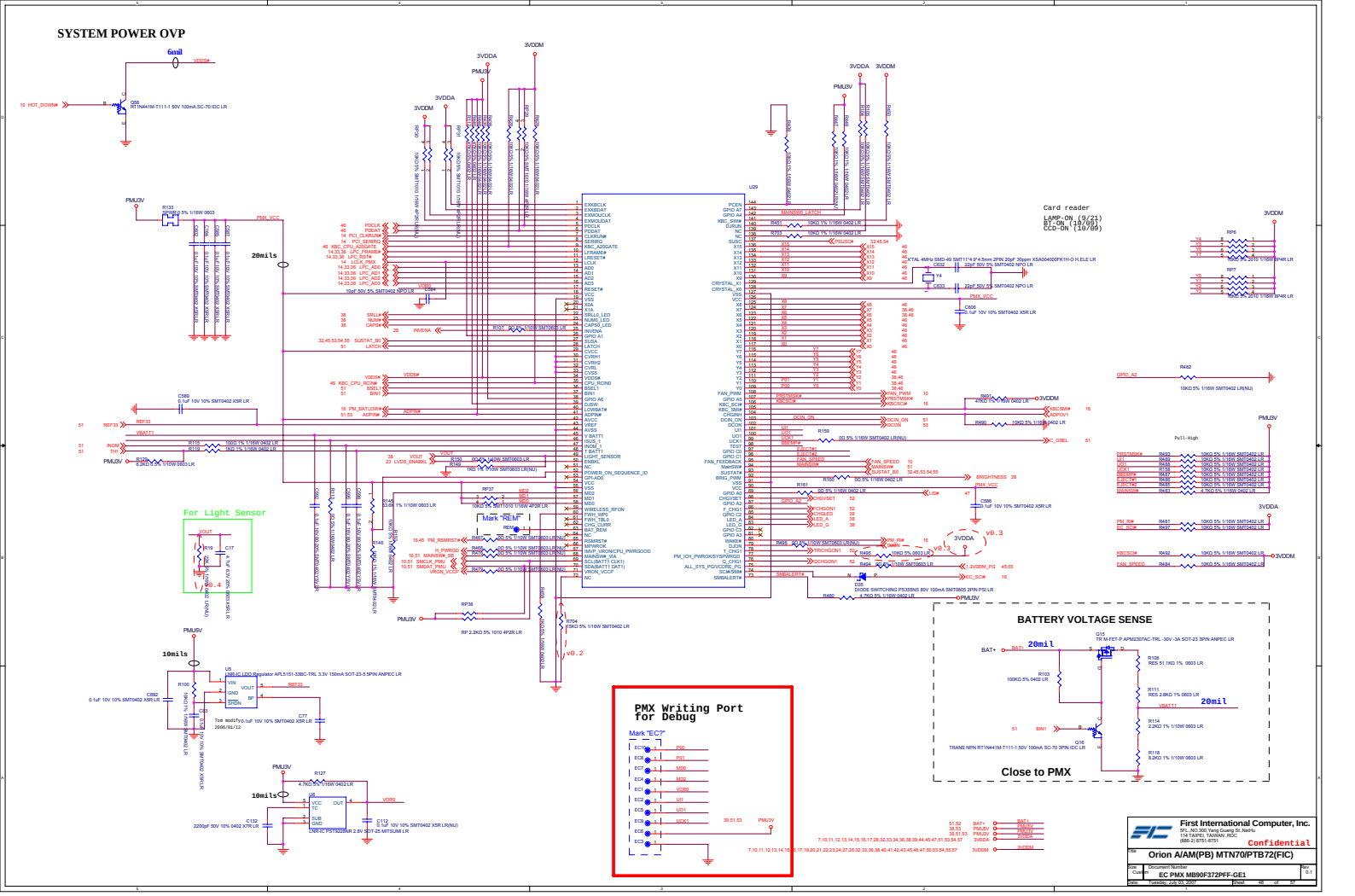
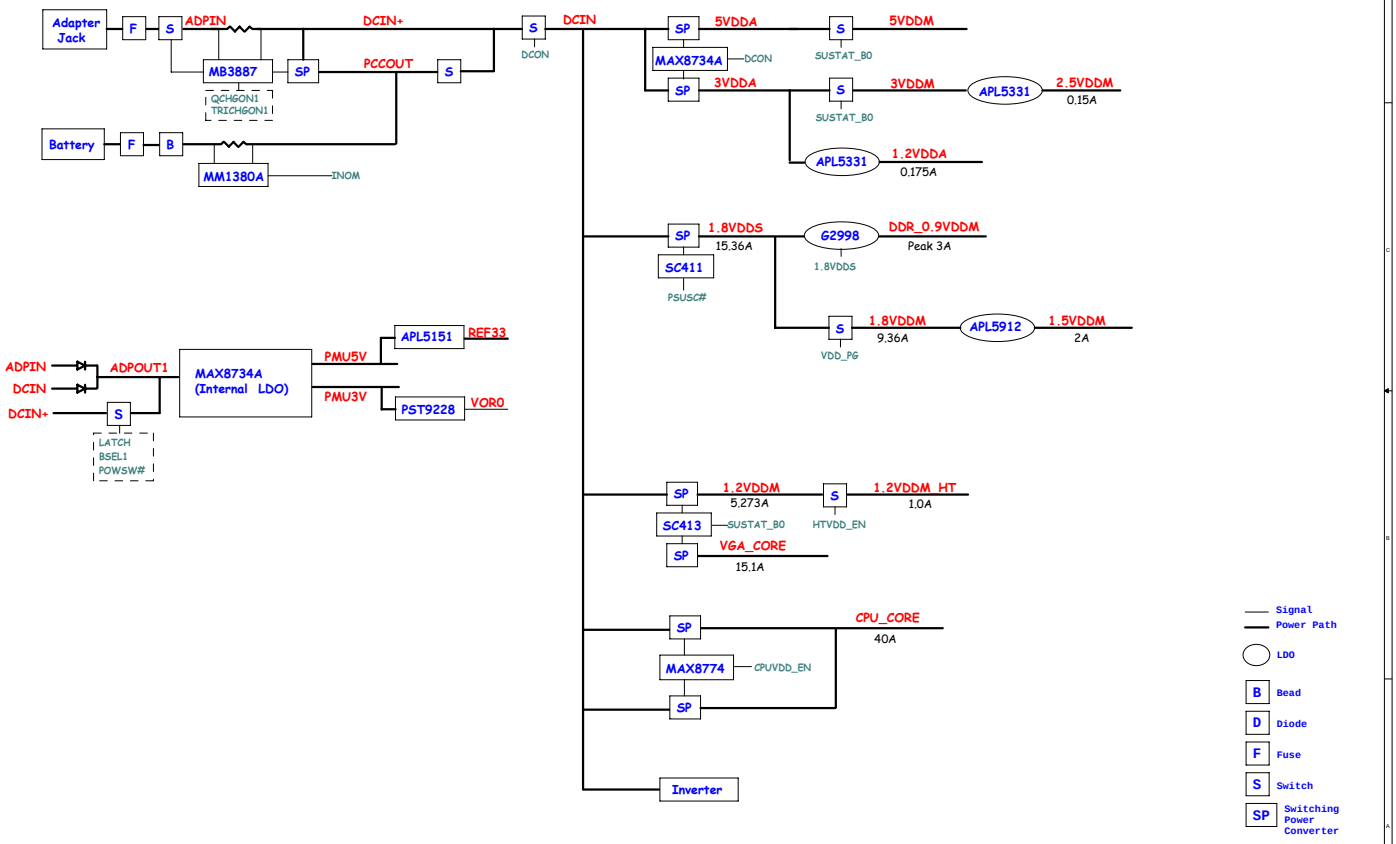
Size	Document Number	Rev
C	DIP/LID SW; SCREW	0.1

Date: Tuesday, July 03, 2007 Sheet 47 of 57

SYSTEM POWER OVP



PTT50 Power Block Diagram



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Title: Orion A/AM(PB) MTN70/PTB72(FIC)

Size: C | Document Number: Power Block Diagram | Rev: 0.1

Date: Tuesday, July 03, 2007 | Sheet 49 of 57

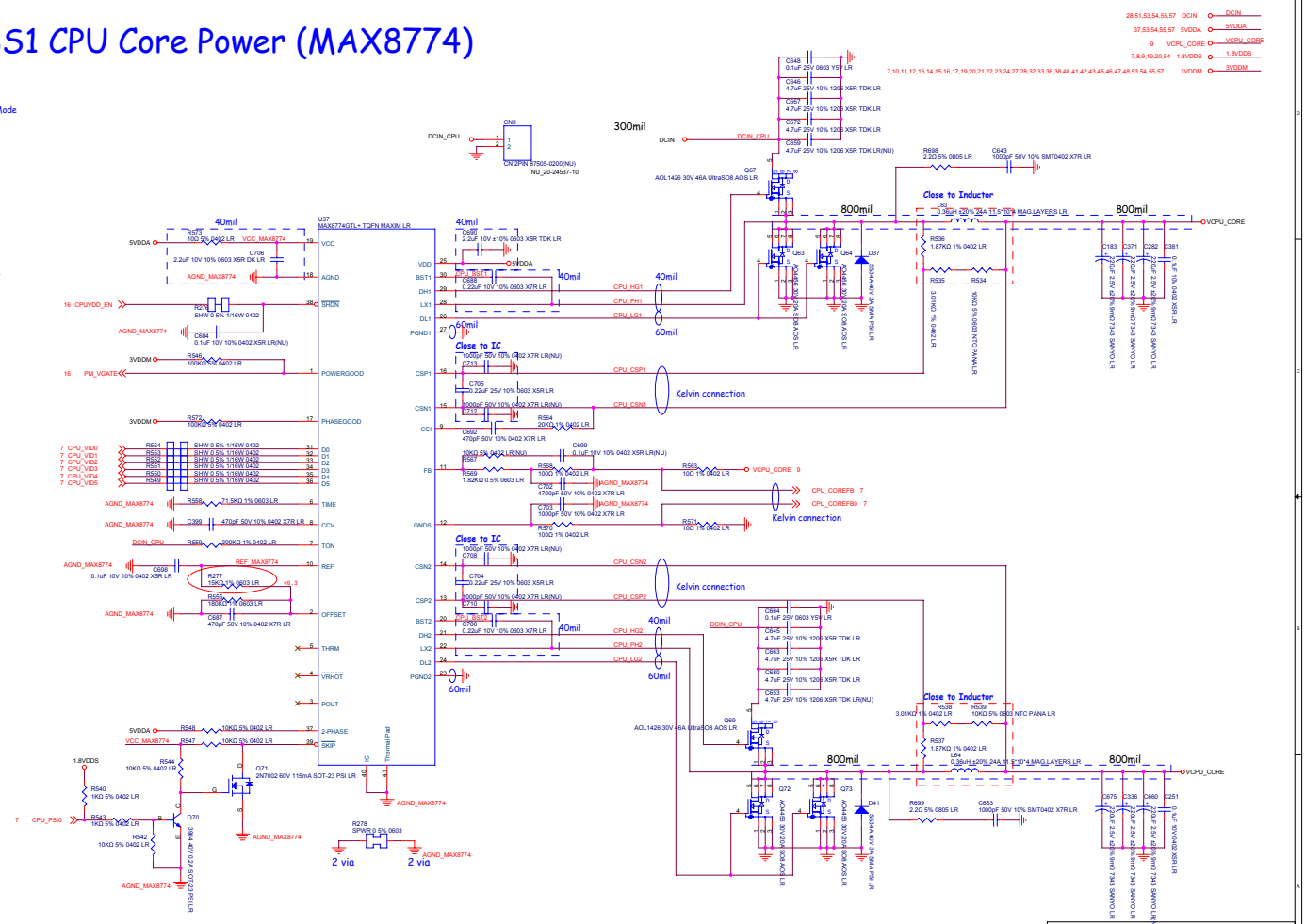
AMD K8S1 CPU Core Power (MAX8774)

#SKIP:
VCC: Dual Phase Force PWM Mode
REF: Dual Phase Skip Mode
GND: One Phase Skip Mode

#Switching frequency (Ton):
= 1/(16.26pF * (Rton+6.5k))
Rton = 200k → 300kHz

#REF(2V):
1uF MLCC
maximum
to GND

#FB:
RFB=Rdroop/(Rsense*Gm(FB))
Gm(FB) Typ=600uS



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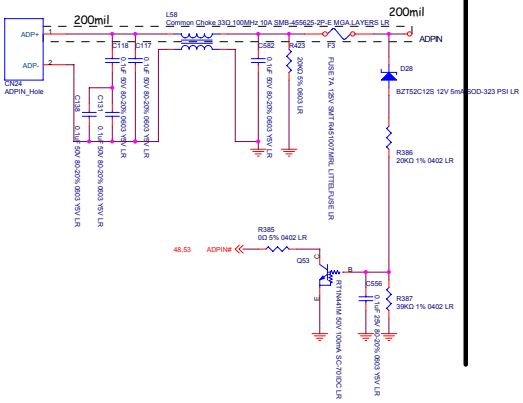
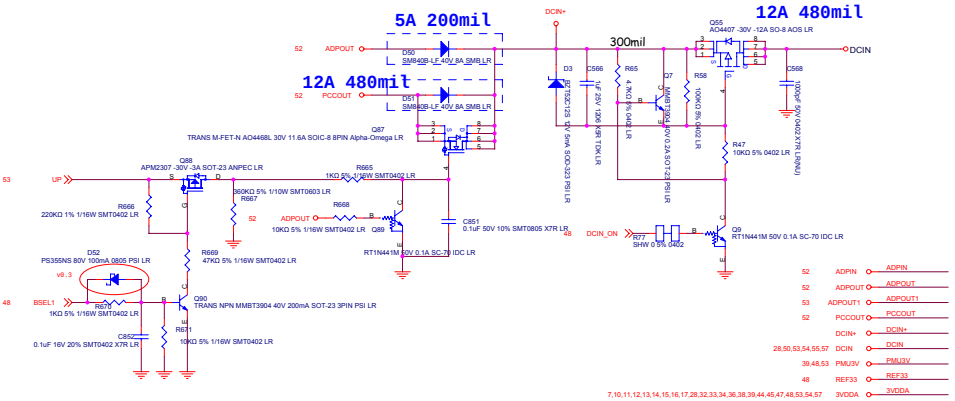
Title	PTT50	
Size / Custom	Document Number: CPU CORE (MAX8774)	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 50 of 57	

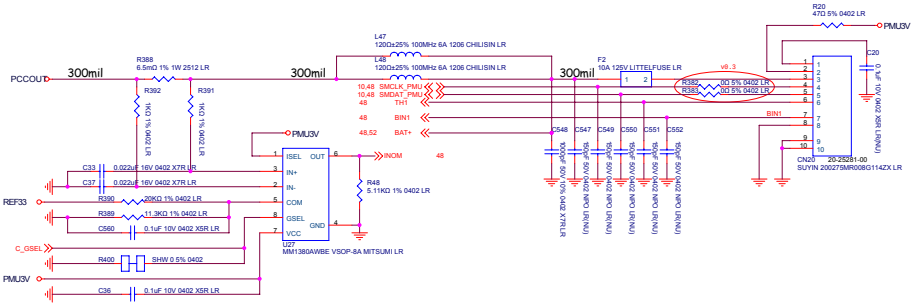
ADPIN



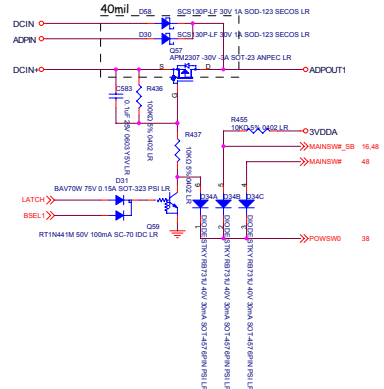
DCIN+ to DCIN



BATIN



ADPOUT1



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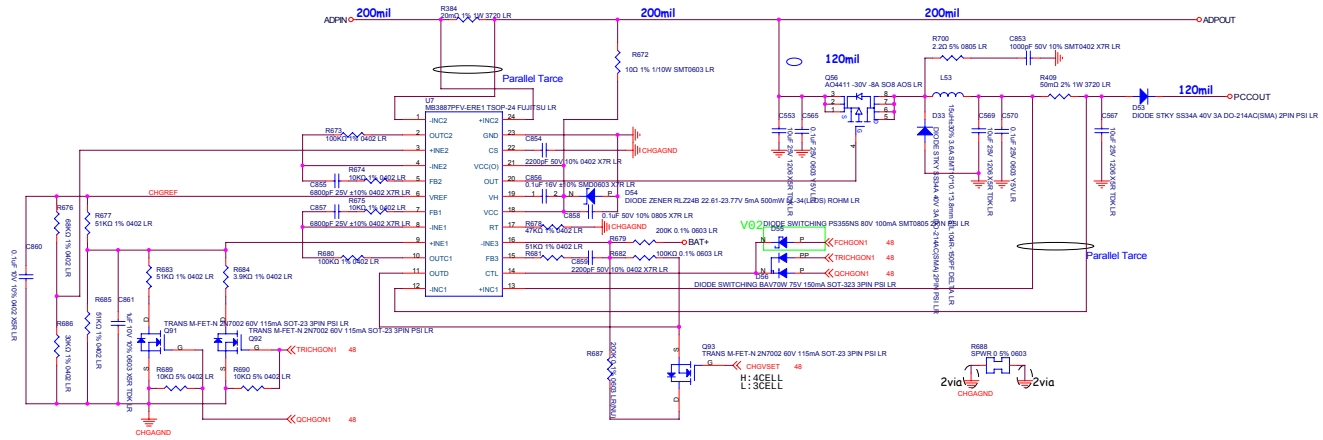
Title		
Size: C	Document Number: AC-IN / BATTERY-IN	Rev: 0.1
Date: Tuesday, July 03, 2007	Sheet 51 of 57	

PCHG PPMU

Charger



Total PWR =
85.52W(20V)

FCHG = 2.5A
QCHG = 1.67A
TCHG = 0.311A

51	ADPOUT	ADPOUT
51	ADPIN	ADPIN
51	PCCOUT	PCCOUT
48,51	BAT+	BAT+

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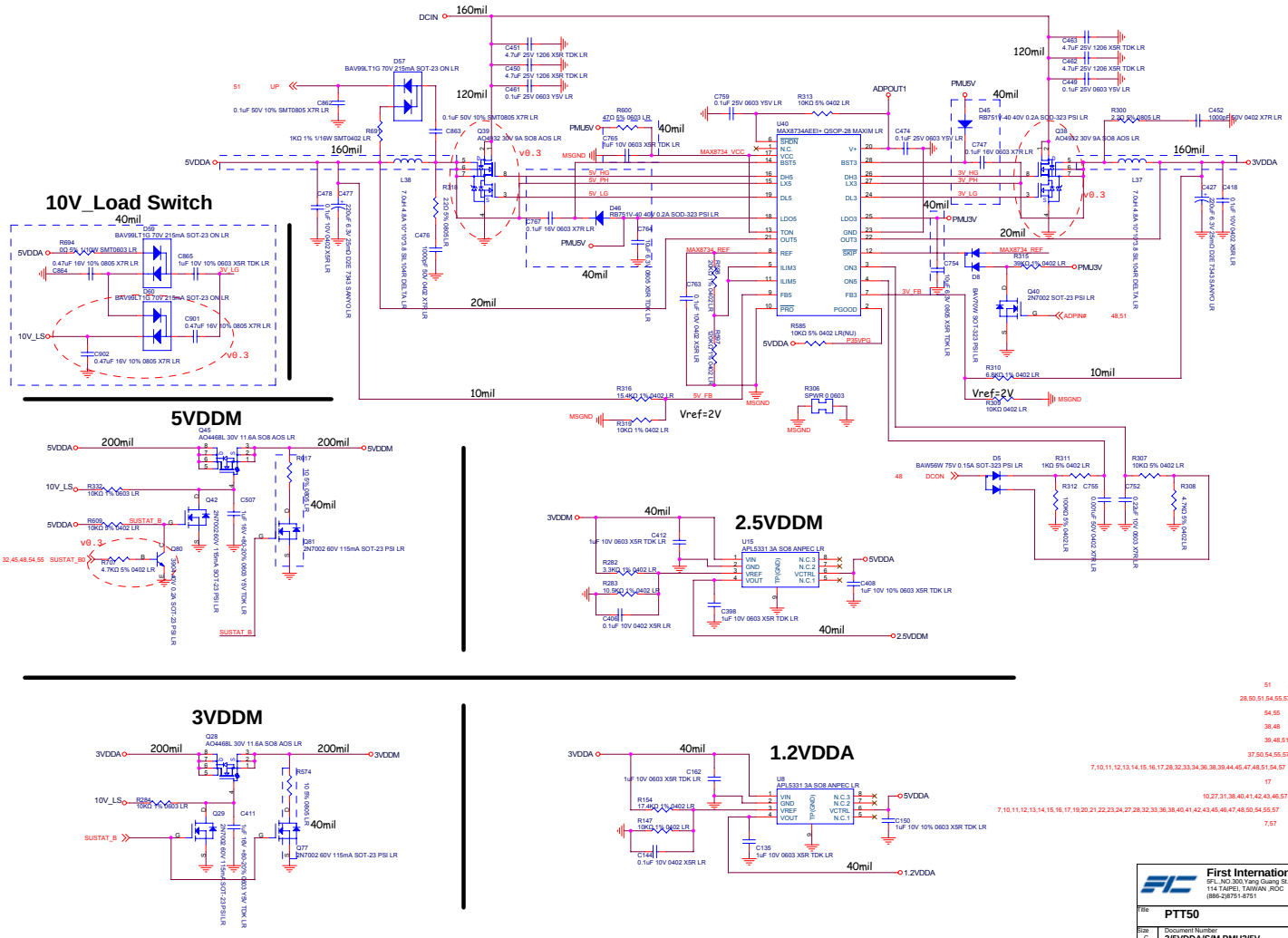
Title: Orion A/AM(PB) MTN70/PTB72(FIC)

Size: C | Document Number: Charger Circuit MB3887 | Rev: 0.2

Date: Tuesday, July 03, 2007 | Sheet 52 of 57

PCHG

PMU5V/3V, 5VDDA/S/M, 3VDDA/S/M, 1.2VDDA, 2.5VDDM



51 ADPOUT1
28,50,51,54,55,57 DCIN
54,55 10V_LS
38,48 PMU5V
39,48,51 PMU3V
37,50,54,55,57 5VDDA
7,10,11,12,13,14,15,16,17,28,32,33,34,36,38,39,44,45,47,48,51,54,57 3VDDA
17 1.2VDDA
10,27,31,38,40,41,42,43,46,57 5VDDM
7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,54,55,57 3VDDM
7,57 2.5VDDM

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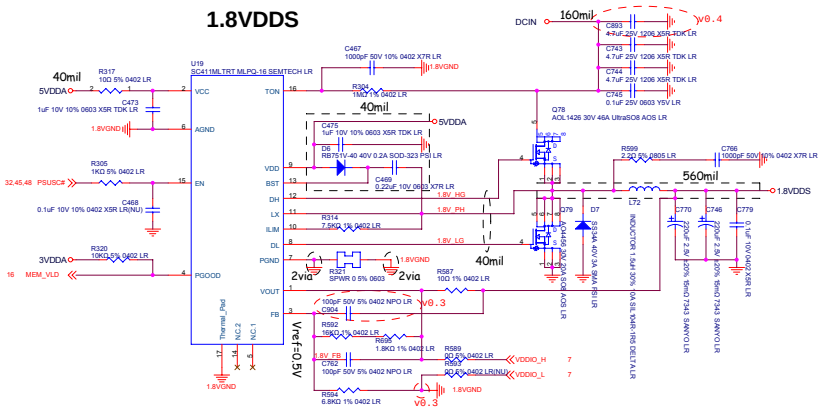
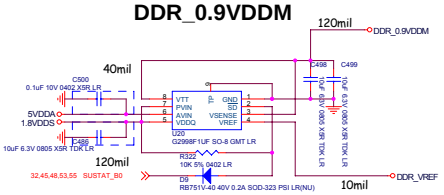
Title	PTT50	
Size: C	Document Number: 3/5VDDA/S/M,PMU3/5V	Rev: 0.3
Date: Tuesday, July 03, 2007	Sheet 53 of 57	

1.8VDDS/M, 0.9VDDM, 1.5VDDM

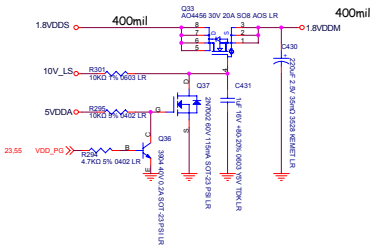
1.8VDDS



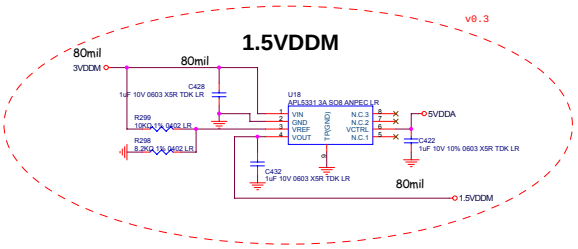
DDR_0.9VDDM



1.8VDDM



1.5VDDM



28,50,51,53,55,57 DCIN
53,55 10V_LS
37,50,53,55,57 5VDDA
7,10,11,12,13,14,15,16,17,28,32,33,34,36,38,39,44,45,47,48,51,53,57 3VDDA
7,8,9,19,20,50 1.8VDDS
8,19,20 DDR_0.9VDDM
20 DDR_VREF
13,23,24,25 1.8VDDM
VGADDR_0.9VDDM
VGADDR_VREF
7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,55,57 3VDDM
32,33 1.5VDDM

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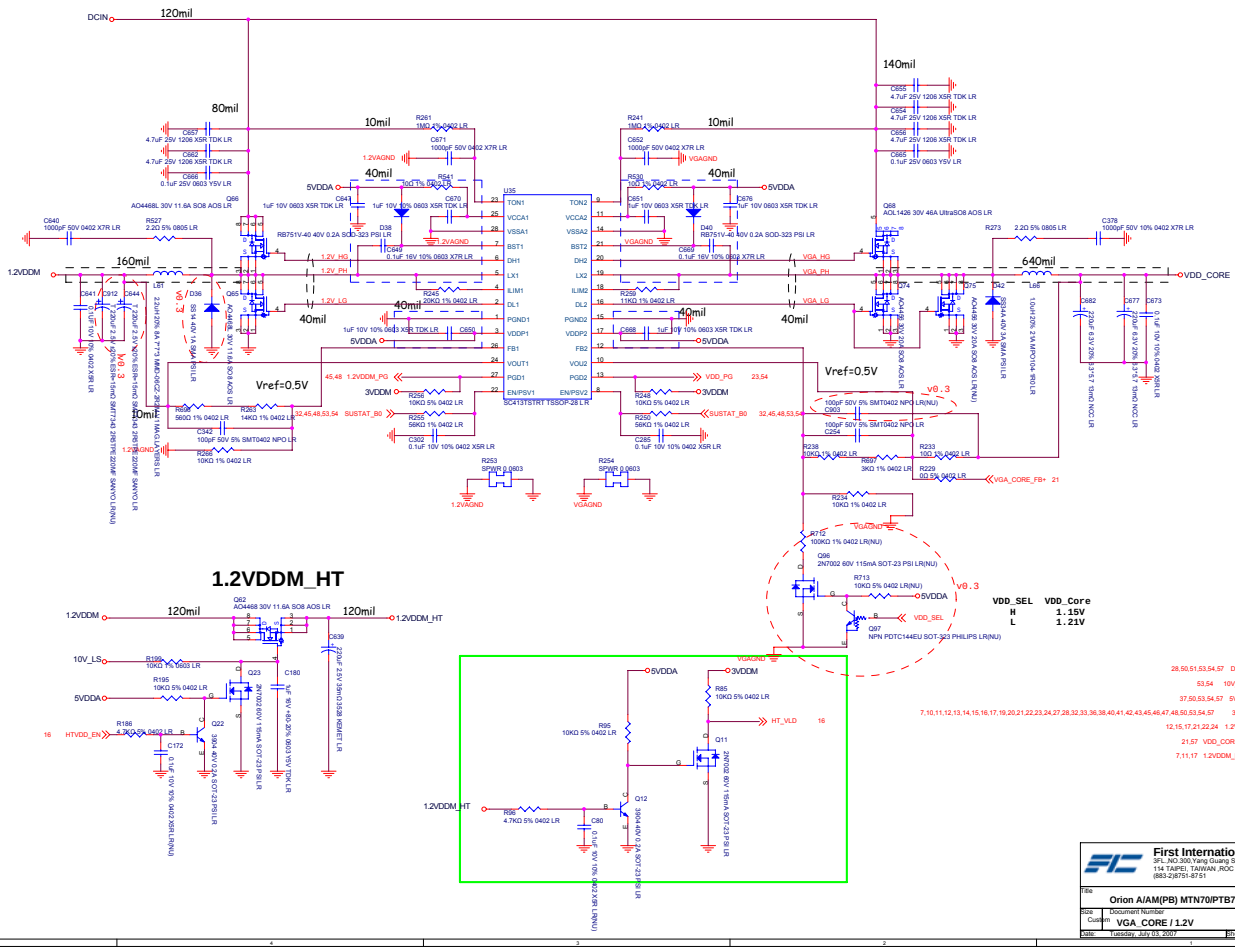
Date: Tuesday, July 03, 2007 | Sheet 54 of 57

MCP67D Core Power / 1.2VDDM / HyperTransport Power



1.2VDDM_HT

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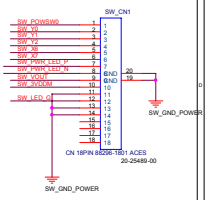
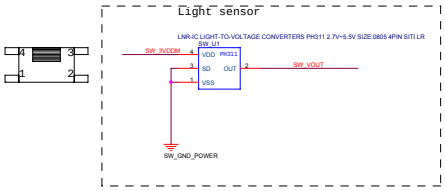
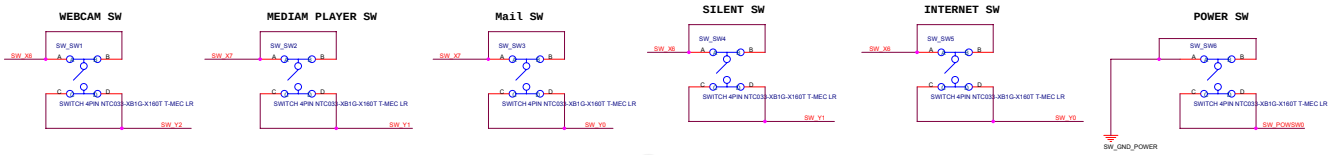
Switch Board



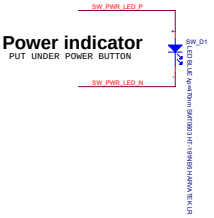


For MR040T w/ Hall sensor only



LEFT RIGHT

POSITION SEQUENCE	SW6	SW5	SW3	SW4	SW2	SW1



PCB : 50-71296-00/20/40
Name : PTT50 SW-B V0.1

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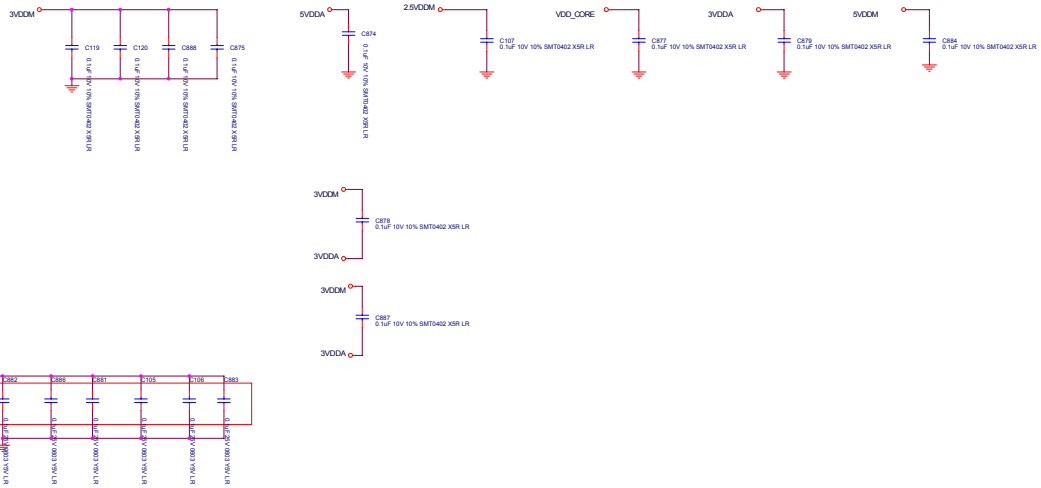
Size	Document Number	Rev
Custom	SW BOARD	0.1
Date: Tuesday, July 03, 2007	Sheet 56 of 57	



28,50,51,53,54,55 DCIN — DCIN

7,53 2.5VDDM — 2.5VDDM

7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55 3VDDM — 3VDDM

37,50,53,54,55 5VDDA — 5VDDA

21,55 VDD_CORE — VDD_CORE

7,10,11,12,13,14,15,16,17,28,32,33,34,36,38,39,44,45,47,48,51,53,54 3VDDA — 3VDDA

10,27,31,38,40,41,42,43,46,53 5VDDM — 5VDDM

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