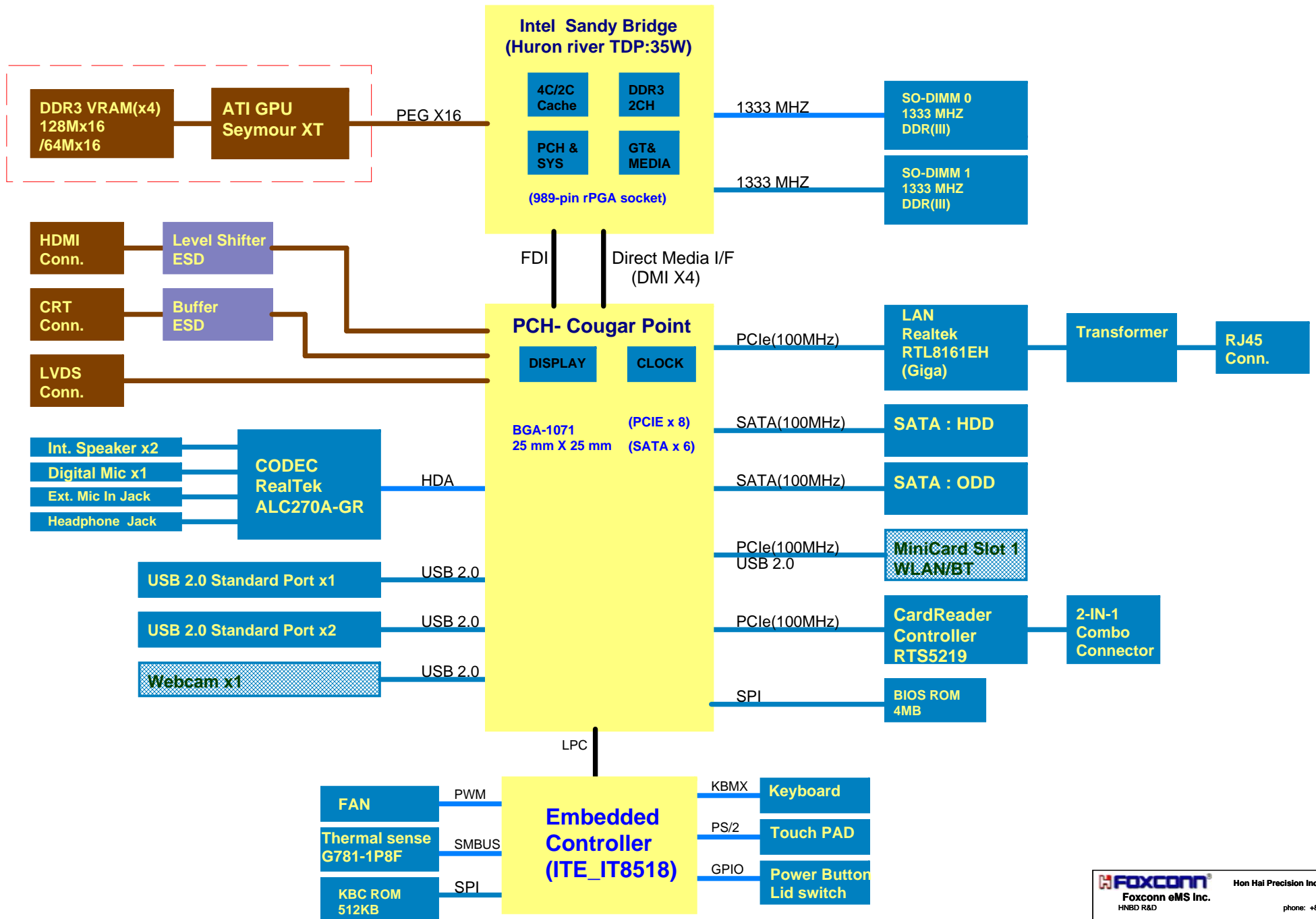


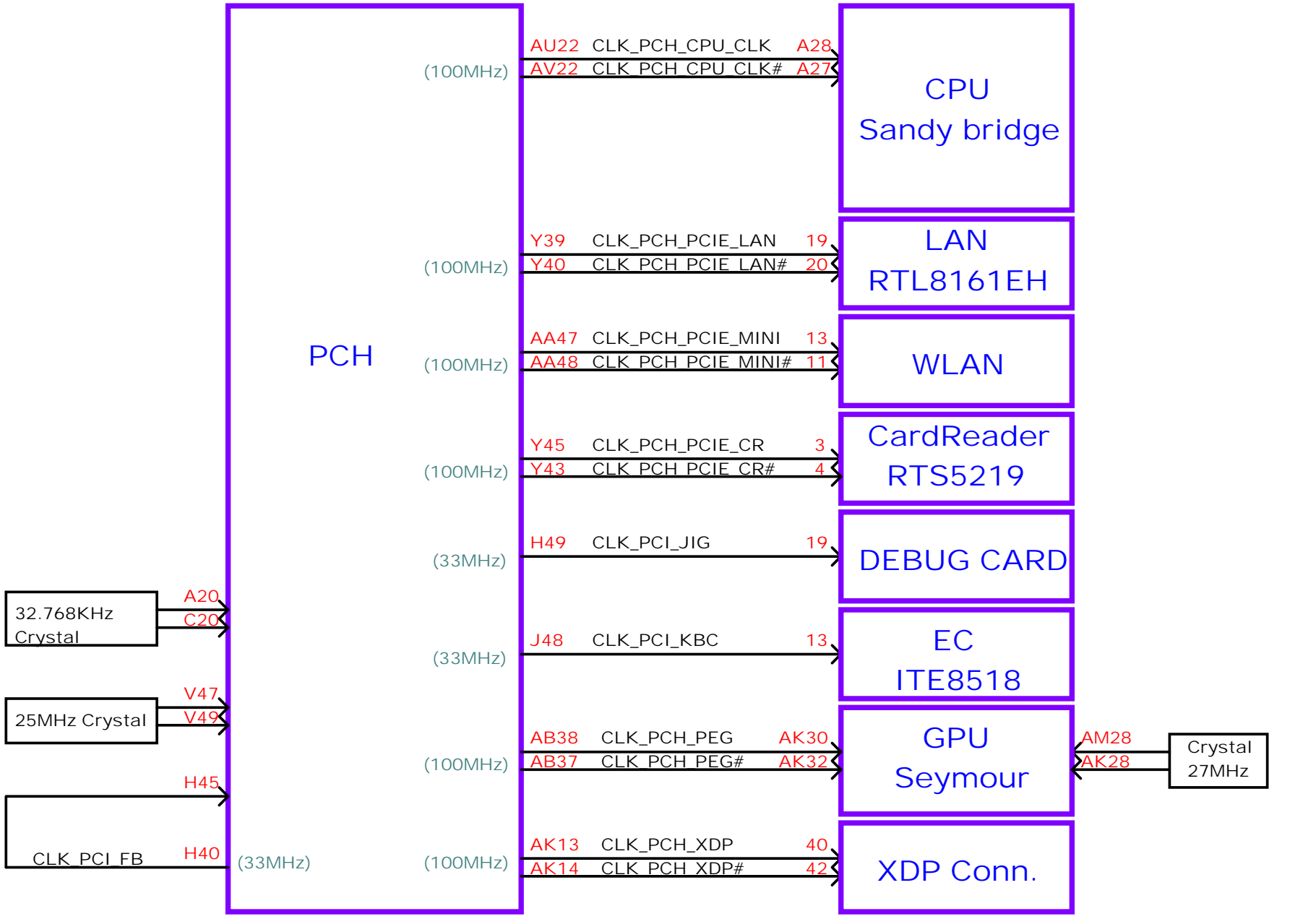
PROJECT : CHICAGO (For Intel Huron River Platform)

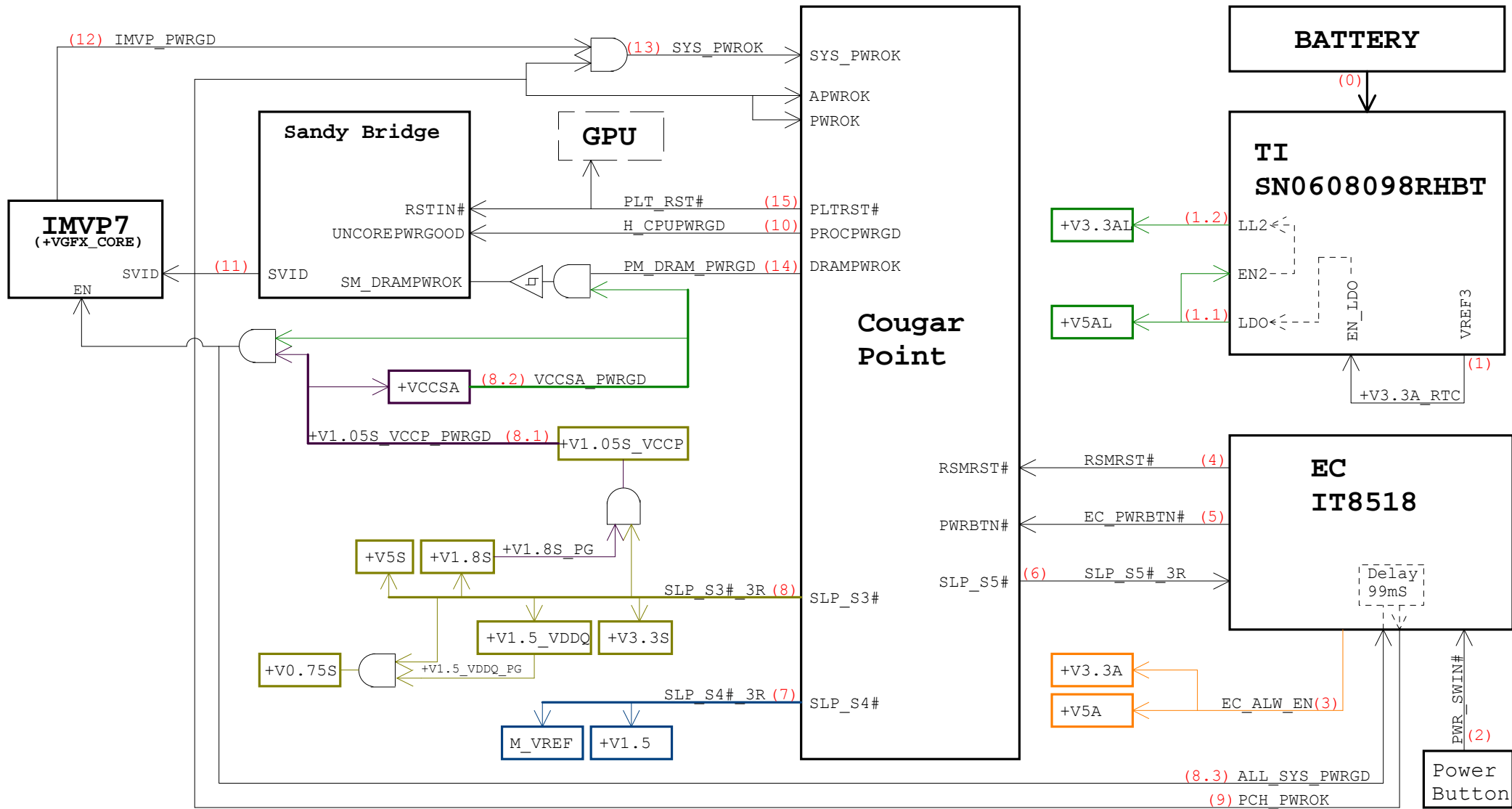
- 01 -- COVER SHEET
- 02 -- SYSTEM BLOCK DIAGRAM
- 03 -- CLOCK MAP
- 04 -- POWER SEQUENCY DIAGRAM
- 05 -- POWER MAP
- 06 -- SMBUS MAP
- 07 -- Blank
- 08 -- DCIN/BATT
- 09 -- PWR_CHARGE
- 10 -- PWR_5V/3.3V
- 11 -- PWR_VCCP
- 12 -- PWR_1.5V/0.75S
- 13 -- PWR_VCORE
- 14 -- PWR_OTHER
- 15 -- PWR_ATVDD
- 16 -- PWR_1.8VS
- 17 -- PWR_VCCSA
- 18 -- Sandy Bridge (DMI, PEG, FDI)
- 19 -- Sandy Bridge (CLK, JTAG..)
- 20 -- Sandy Bridge (DDR3)
- 21 -- Sandy Bridge (PWR/GND)
- 22 -- Sandy Bridge (GRAPHIC PWR)
- 23 -- CougarPoint (HDA, SATA..)
- 24 -- CougarPoint (PCI-E, CLK..)
- 25 -- CougarPoint (DMI, FDI..)
- 26 -- CougarPoint (USB, GPIO..)
- 27 -- CougarPoint (PWR/GND)
- 28 -- CougarPoint (PWR, GND)
- 29 -- DDR3 (SO-DIMM 0&1)
- 30 -- VGA (PCI-E/STRAP) 1/3
- 31 -- VGA_S3 (IO) 2/3
- 32 -- VGA_S3 (DDR3) 3/3
- 33 -- VRAM (DDR3)
- 34 -- EC+KBC (IT8518) & ROM
- 35 -- Audio (CODEC_ALC270A)
- 36 -- Audio (JACK+AMP+SPK+Mute)
- 37 -- LAN (RTL8161EH)
- 38 -- Mini PCIe & FAN
- 39 -- USBx2/USB DB/SATA CONN.
- 40 -- Card Reader (RTL5219-GR)
- 41 -- HDMI & CRT
- 42 -- LVDS & Webcam
- 43 -- Sequence circuit

P. Leader	Check by	Design by

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Index Page			
Size	Document Number	Rev	
Custom	CHICAGO	MV	
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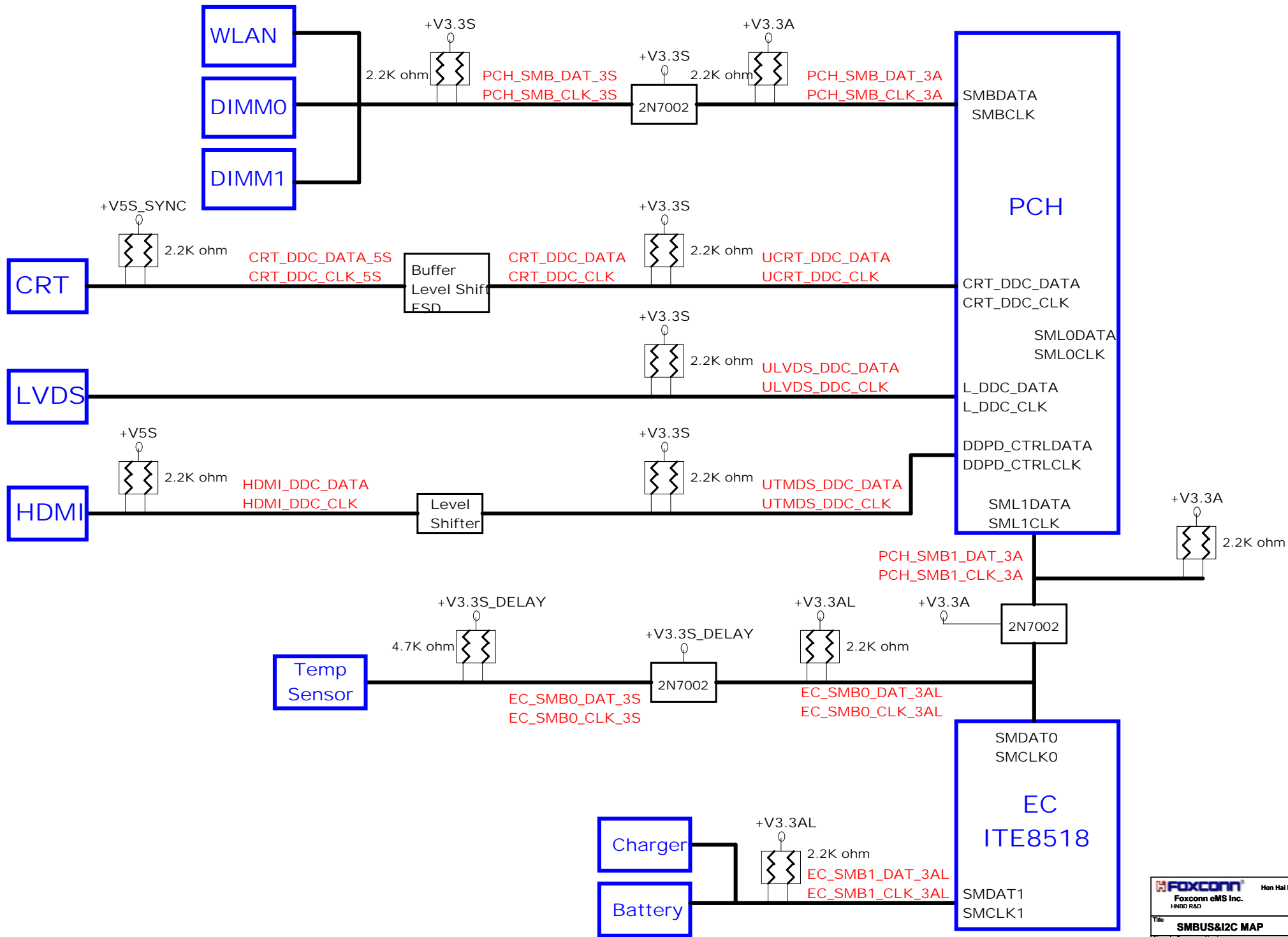






POWER MAP





5

4

3

2

1

D

D

C

C

B

B

A

A



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5

4

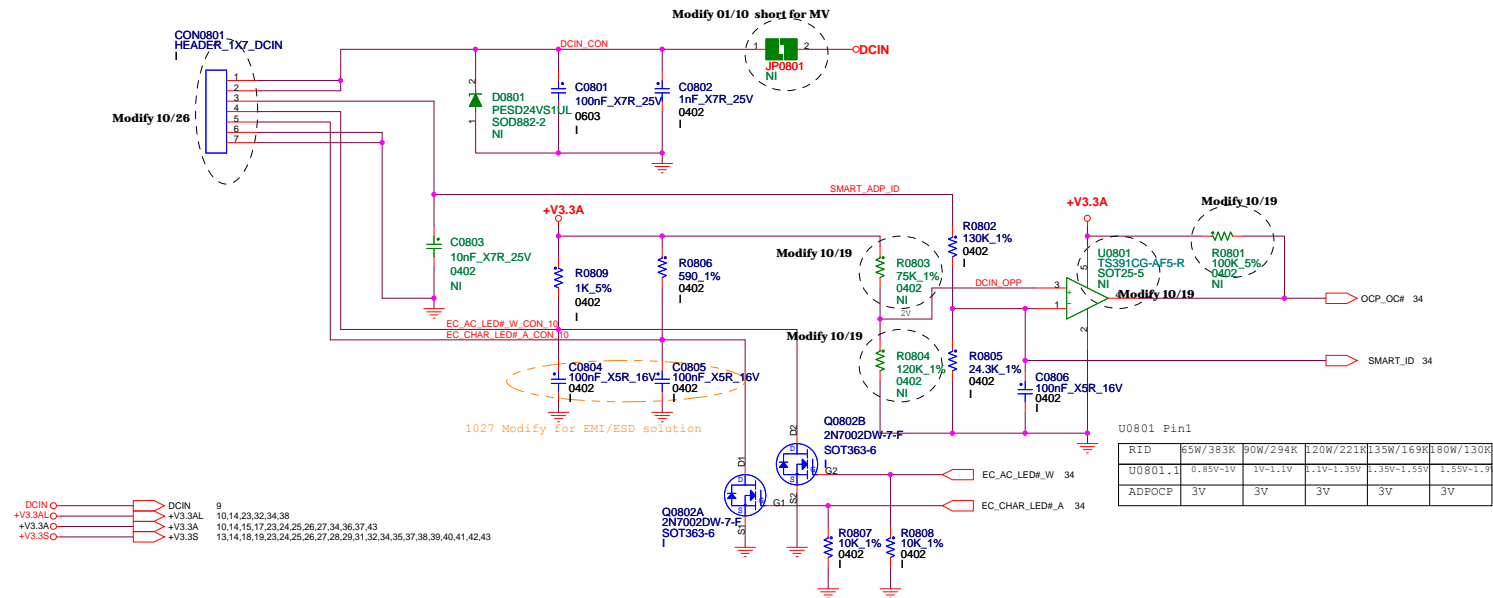
3

2

1

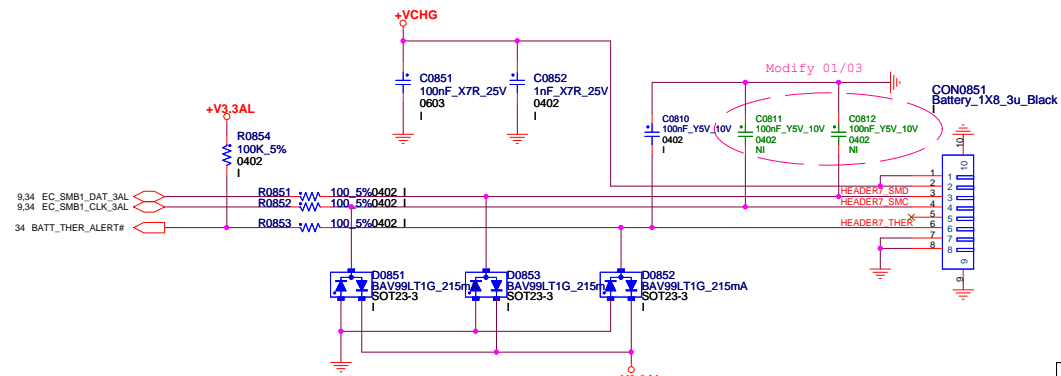
DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0

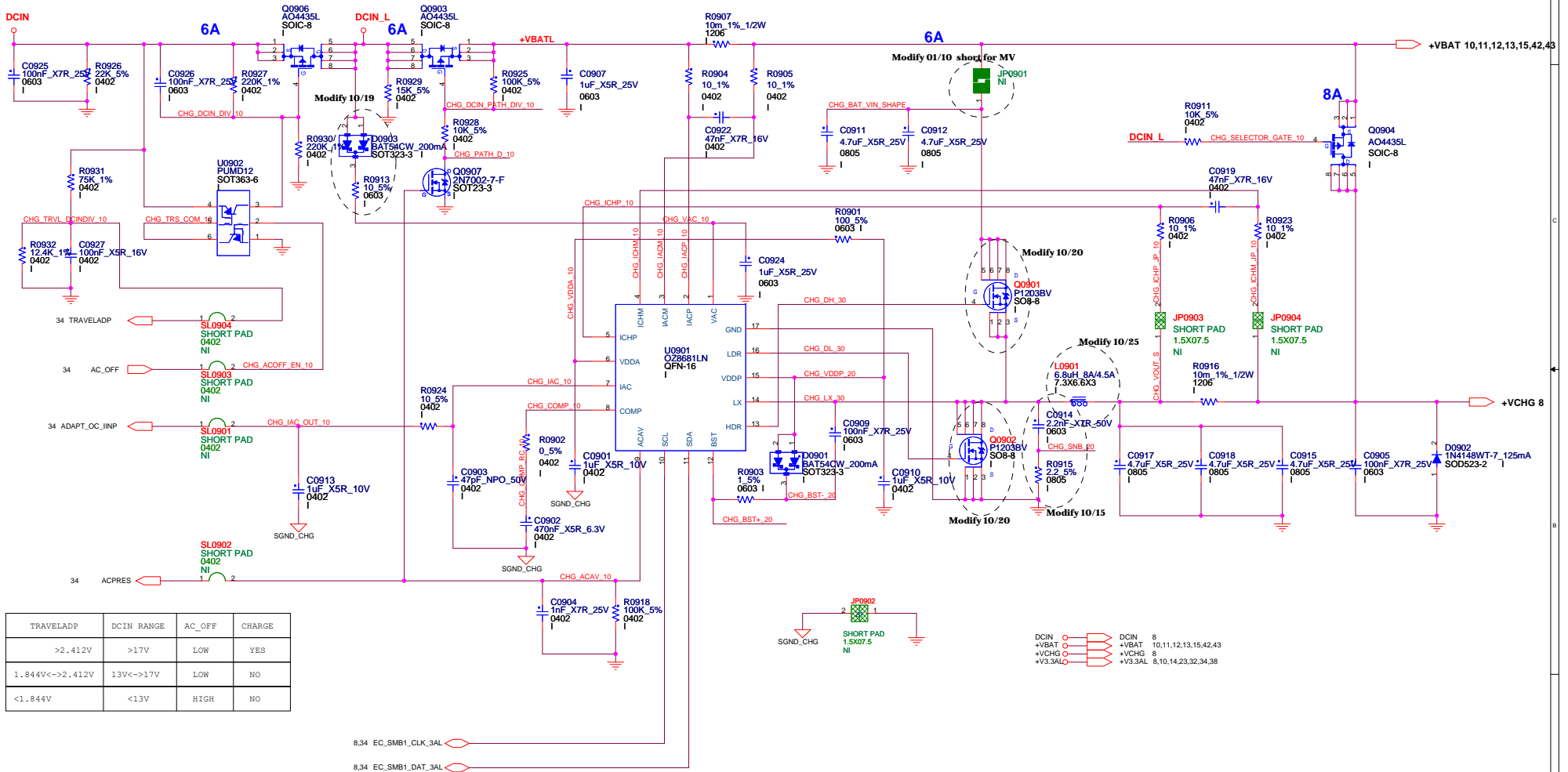


BATTERY CONNECTOR

2010.0914.0



BATTERY CHARGER



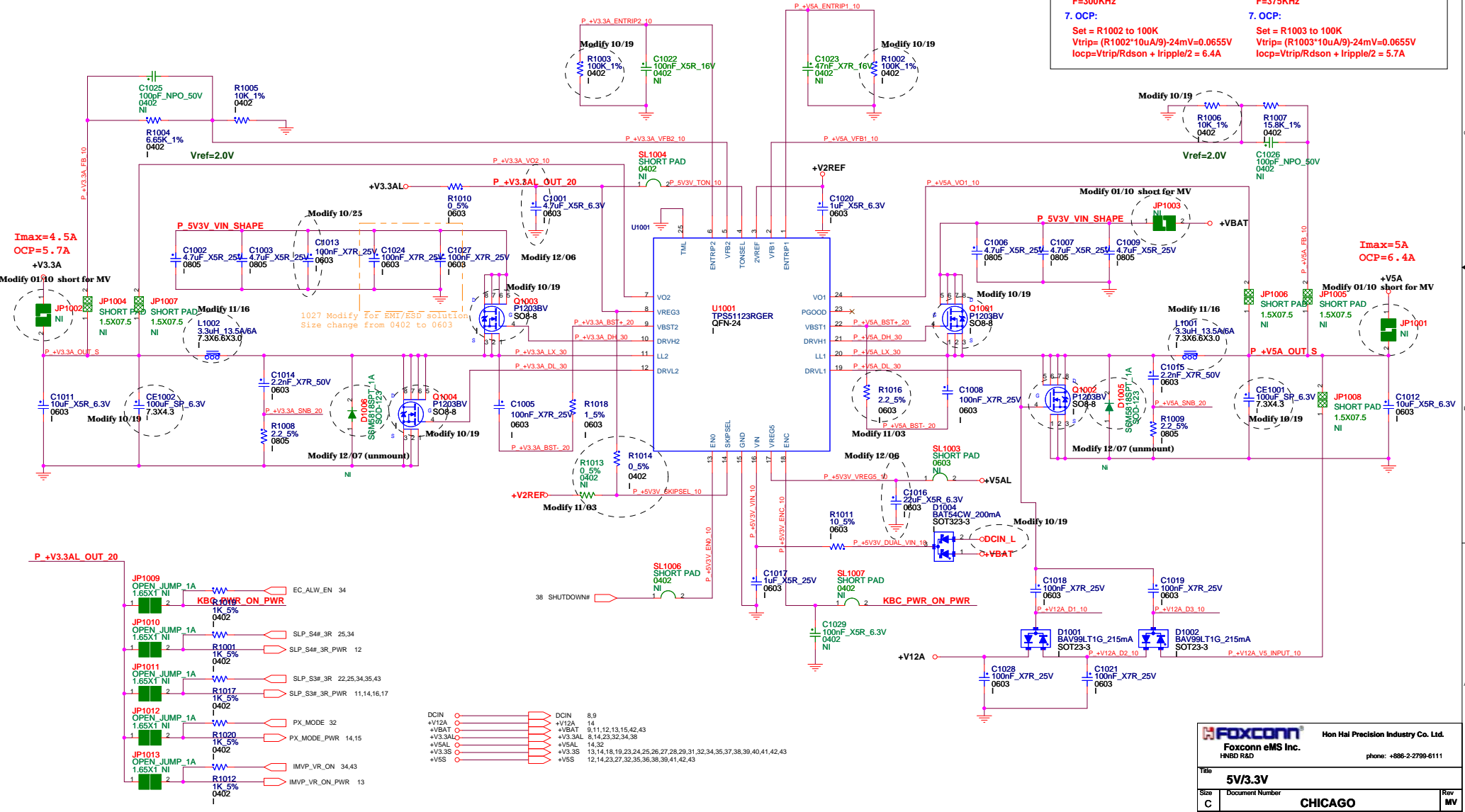
TRAVELADP	DCIN_RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

- DCIN 8
- +VBAT 10,11,12,13,15,42,43
- +VCHG 8
- +V3.AL0 8,10,14,23,32,34,38

+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current: lin=Vo*Io/(0.75*Vin)=3.7A	1. I/P Current: lin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current: Irip=3.72A	2. Ripple Current: Irip=2.21A
3. Ripple Voltage: ESR/1=15mohm Vrip=55.8mV	3. Ripple Voltage: ESR/1=15mohm Vrip=33.15mV
4. Inductor Spec: Isat=13.5A Idc=6A DCR=30mohm	4. Inductor Spec: Isat=13.5A Idc=6A DCR=30mohm
5. MOSFET Spec: H-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T=25 °C) I peak = 88A (Pause=10 us)	L-side MOSFET: IRF8707PBF Rds(ON)=17.5mohm (Vgs=4.5 V) I cont = 11A (T=25 °C) I peak = 88A (Pause=10 us)
6. Frequency: F=300KHz	6. Frequency: F=375KHz
7. OCP: Set = R1002 to 100K Vtrip= (R1002*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 6.4A	7. OCP: Set = R1003 to 100K Vtrip= (R1003*10uA/9)-24mV=0.0655V Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



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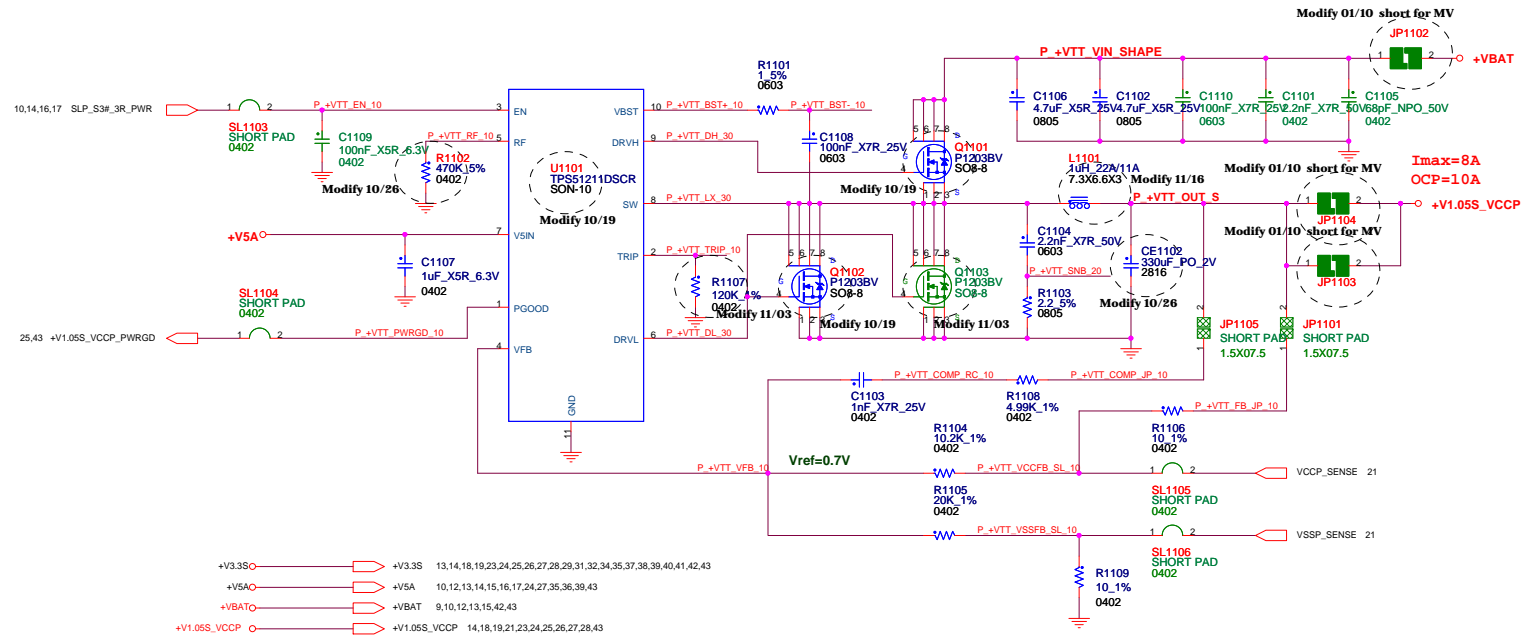
Title: **5V/3.3V**
 Size: Document Number
 C: **CHICAGO** Rev: MV
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+VTT POWER SUPPLY

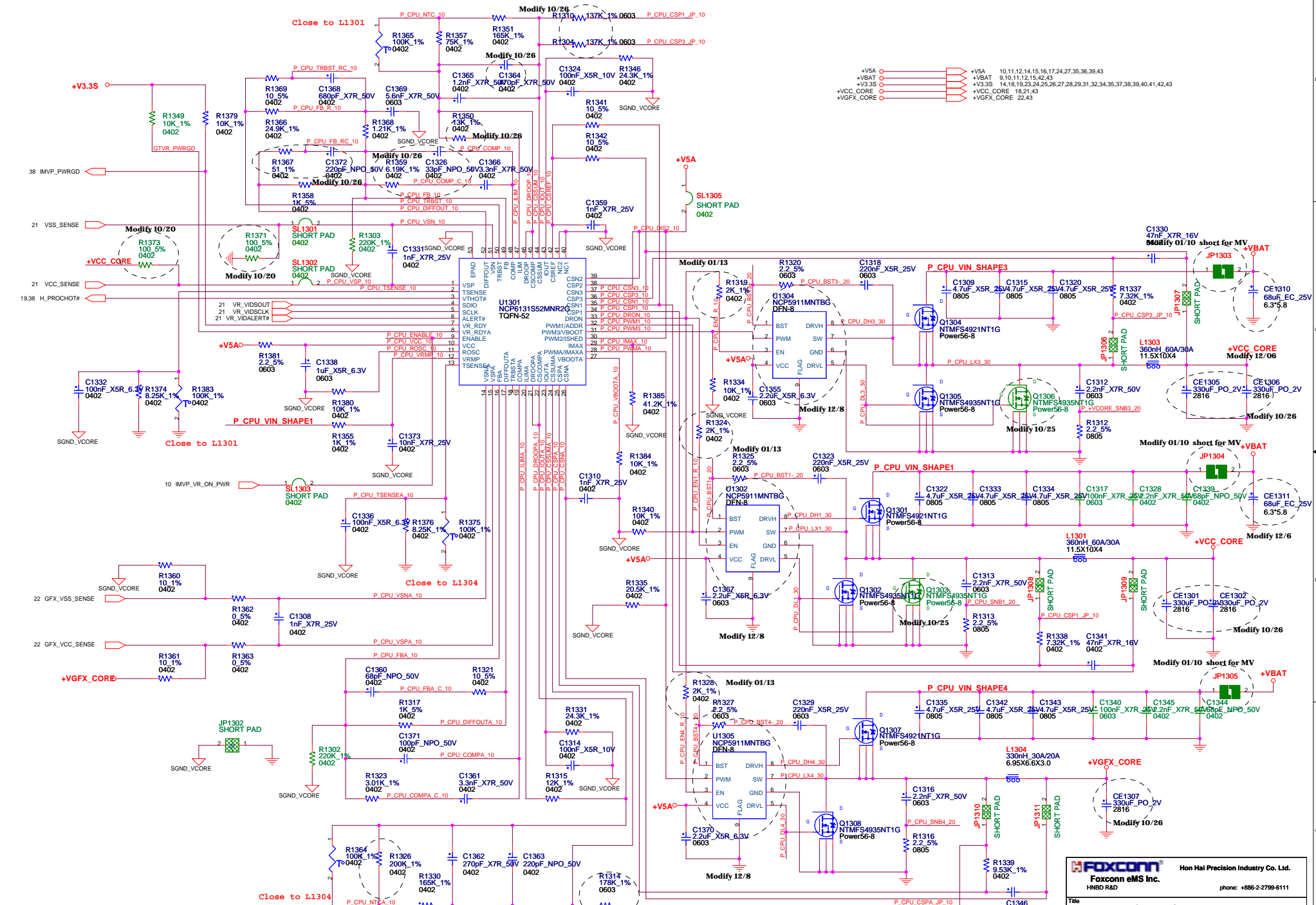
2010.1103.0

- +V1.05S_VCCP:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.24A$
 - Ripple Current:**
 $I_{rip} = 3.42A$
 - Ripple Voltage:**
 $ESR/1 = 9mohm$
 $V_{rip} = 30.78mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3mohm$
 - MOSFET Spec:**

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
$R_{ds}(ON) = 17.5mohm$ ($V_{gs} = 4.5V$)	$R_{ds}(ON) = 17.5mohm$ ($V_{gs} = 4.5V$)
$I_{cont} = 11A$ ($T = 25^\circ C$)	$I_{cont} = 11A$ ($T = 25^\circ C$)
$I_{peak} = 88A$ ($Pause = 10us$)	$I_{peak} = 88A$ ($Pause = 10us$)
 - Frequency:**
 $F = 290KHz$ ($R1102 = 0ohm$)
 - OCP:**
 $Set = R1107$ to 120K
 $V_{trip} = R1107 \cdot 10uA = 1.2V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{ds(on)}) + I_{ripple} / 2 = 10A$



2010.1026.0 IMVP7 CPU VCORE POWER SUPPLY

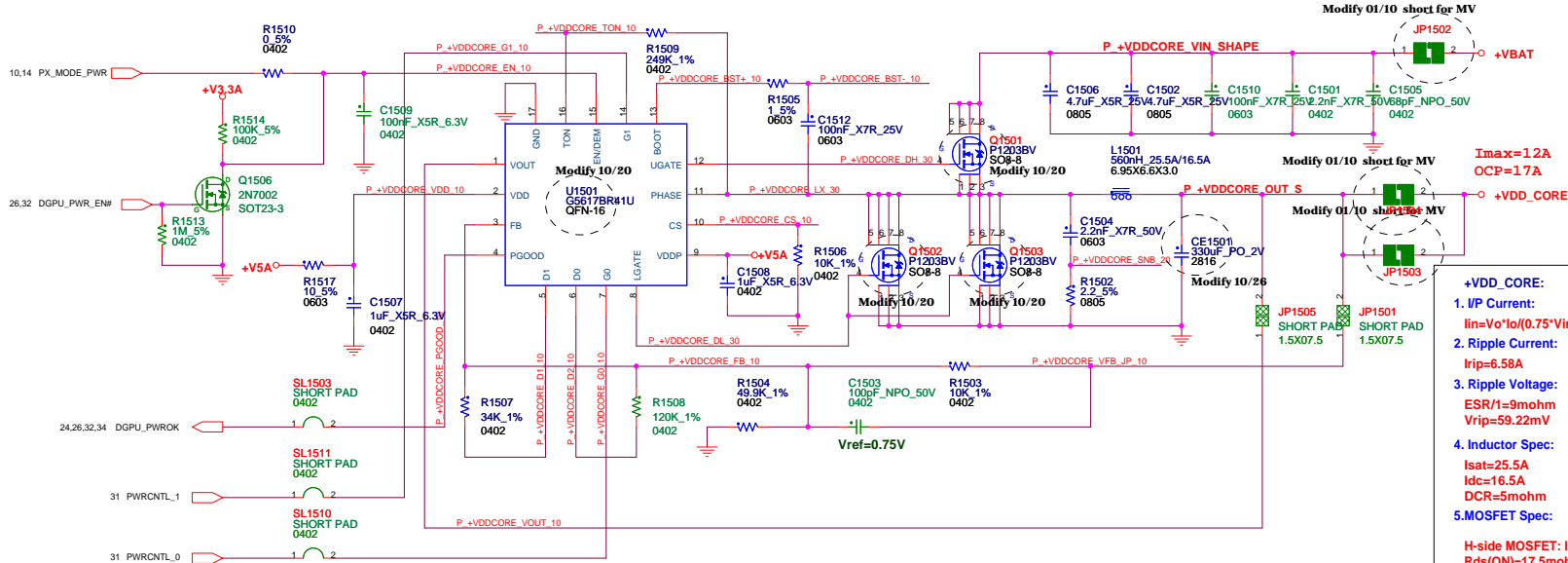


- +V5A 10,11,12,14,15,16,17,24,27,35,36,39,43
- +VBAT 9,10,11,12,15,42,43
- +V3.3S 14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
- +VCC_CORE 18,21,43
- +VFX_CORE 22,43

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Vcore NCP6131S			
Size	Document Number	Rev	
C	CHICAGO	MV	
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+VDD_CORE POWER SUPPLY

2010.1026.0

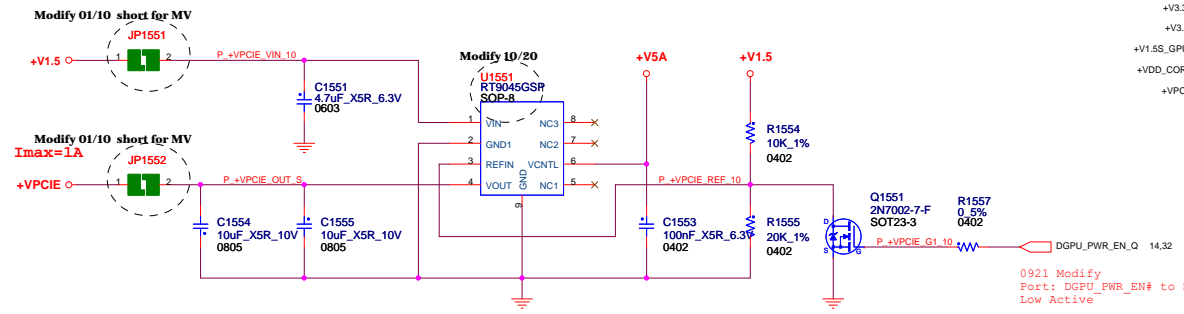


PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

- +VDD_CORE:**
- 1. I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.48A$
 - 2. Ripple Current:**
 $I_{rip} = 6.58A$
 - 3. Ripple Voltage:**
 $ESR / I = 9m\Omega$
 $V_{rip} = 59.22mV$
 - 4. Inductor Spec:**
 $I_{sat} = 25.5A$
 $I_{dc} = 16.5A$
 $DCR = 5m\Omega$
 - 5. MOSFET Spec:**

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
$R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)	$R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
$I_{cont} = 11A$ ($T = 25^\circ C$)	$I_{cont} = 11A$ ($T = 25^\circ C$)
$I_{peak} = 88A$ (Pause = 10 us)	$I_{peak} = 88A$ (Pause = 10 us)
 - 6. Frequency:**
 $TON = 9.6 \cdot P \cdot R1509 \cdot (VOUT + 0.1) / (VIN - 0.3) + 50ns = 206ns$
 $F = VOUT / (VIN \cdot TON) = 286KHz$
 - 7. OCP:**
 $Set = R1506 \text{ to } 10K$
 $V_{trip} = R1206 \cdot I_{O_uA} = 0.1V$
 $I_{ocp} = (V_{trip} / R_{ds(on)}) + I_{ripple} / 2 = 17A$

2010.1020.0 +VPCIE POWER SUPPLY



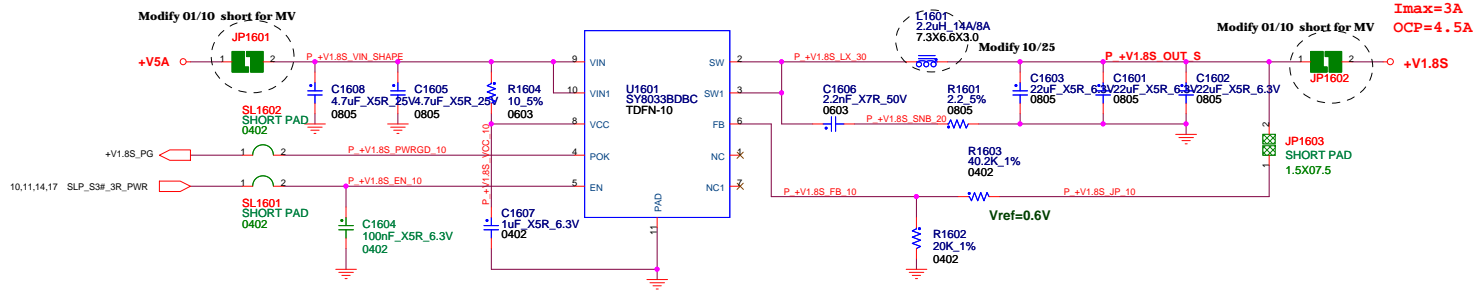
- +VBAT → +VBAT 9,10,11,12,13,42,43
- +V5A → +V5A 10,11,12,13,14,16,17,24,27,35,36,39,43
- +V3.3A → +V3.3A 8,10,14,17,23,24,25,26,27,34,36,37,43
- +V3.3S → +V3.3S 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
- +V1.5S_GPU → +V1.5S_GPU 14,30,32,33,43
- +VDD_CORE → +VDD_CORE 32,43
- +VPCIE → +VPCIE 30,31,32,43

0921 Modify
 Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
 Low Active

+V1.8S POWER SUPPLY

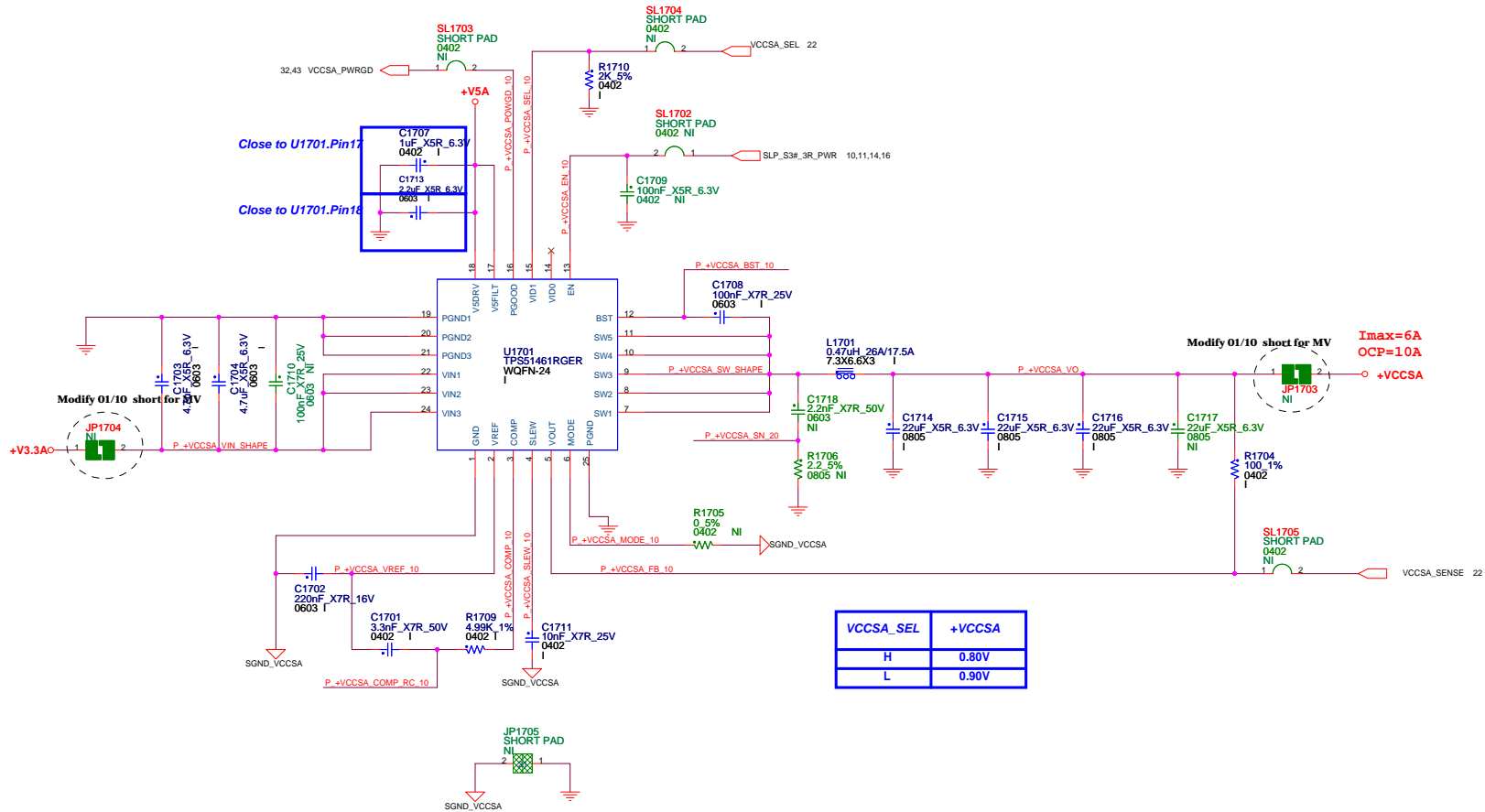
2010.1025.0

- +V1.8S:**
- 1. I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$
 - 2. Ripple Current:**
 $I_{rip} = 0.53A$
 - 3. Ripple Voltage:**
 $ESR/3 = 3.3m\Omega$
 $V_{rip} = 1.75mV$
 - 4. Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 20m\Omega$
 - 5. MOSFET Spec:**
H-side P-MOSFET: $R_{ds(ON)} = 110m\Omega$ ($V_{gs} = 4.5V$)
L-side N-MOSFET: $R_{ds(ON)} = 75m\Omega$ ($V_{gs} = 4.5V$)
 - 6. Frequency:**
 $F = 1MHz$ (min=800KHz, max=1.2MHz)
 - 7. OCP:**
 $I_{ocp} = 4A(\min) / 4.5A(\text{typ}) / 5A(\text{max})$



+VCCSA POWER SUPPLY

2010.1026.0

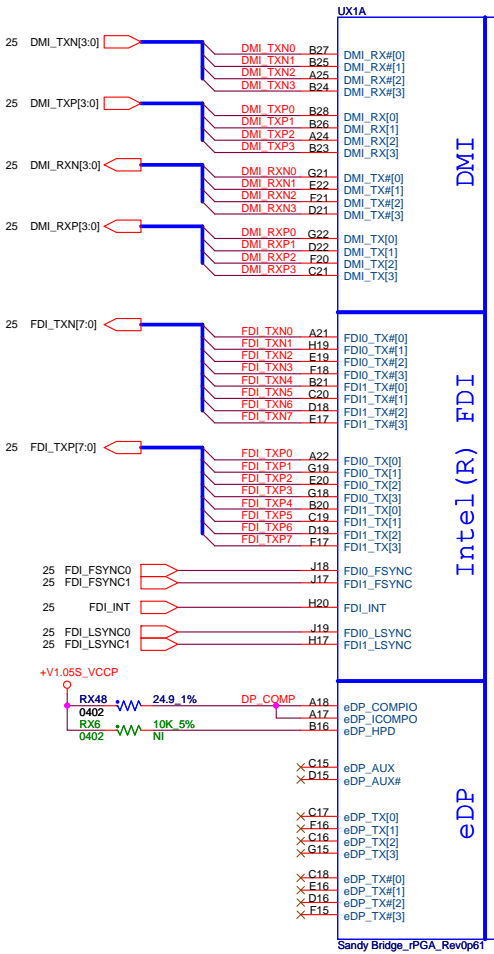


- +VCCSA:
- 1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.18A$
- 2. Ripple Current:
 $I_{rip} = 1.39A$
- 3. Ripple Voltage:
 $ESR/4 = 1\text{mohm}$
 $V_{rip} = 1.39\text{mV}$
- 4. Inductor Spec:
 $I_{sat} = 26A$
 $I_{dc} = 17.5A$
 $DCR = 4.2\text{mohm}$
- 5. MOSFET Spec:

- 6. Frequency:
 $F = 1\text{MHz}$ (R1705=Open)
- 7. OCP:
Min : 6A / Typ : 7.5A

VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

+V3.3S
 +V1.05S_VCCP → +V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43



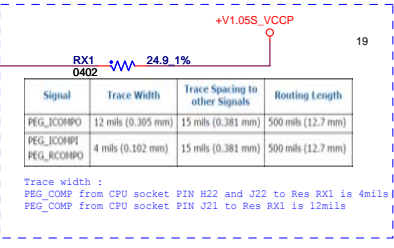
Intel(R) FDI
 PCI EXPRESS* - GRAPHICS

eDP

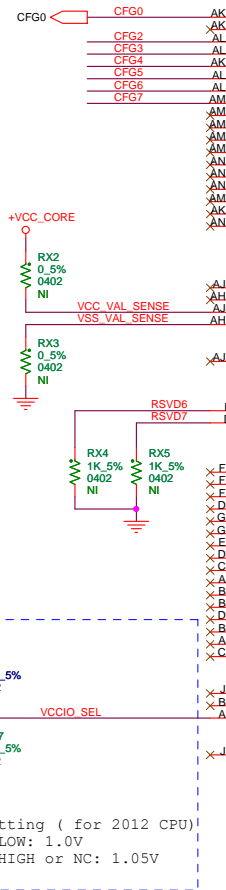
Signal	Trace Width	Trace Spacing to other Signals	Routing Length
PEG_ICOMPO	12 mils (0.305 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)
PEG_ICOMPI	4 mils (0.102 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)

Signal	Trace Width	Trace Spacing to other Signals	Routing Length
PEG_COMP	12 mils (0.305 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)
PEG_ICOMPI	4 mils (0.102 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)

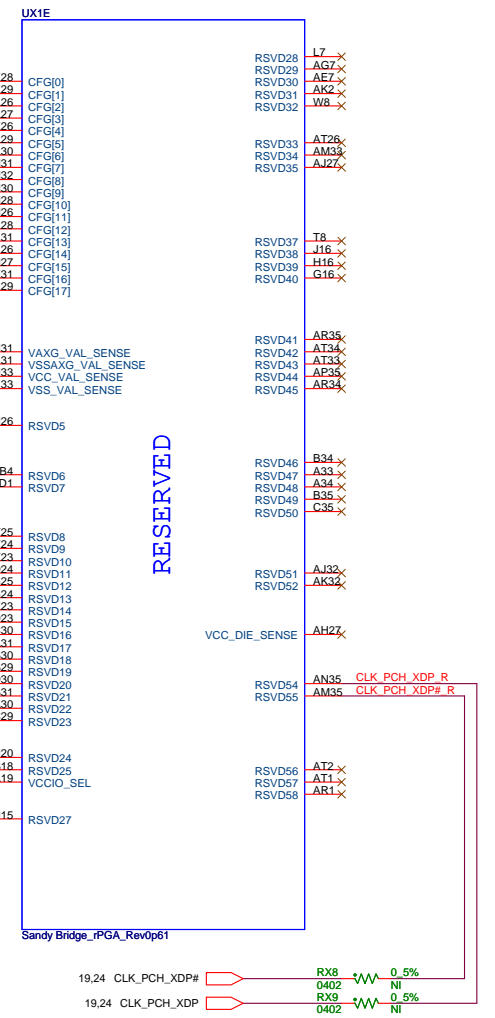
Signal	Trace Width	Trace Spacing to other Signals	Routing Length
PEG_COMP	12 mils (0.305 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)
PEG_ICOMPI	4 mils (0.102 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)



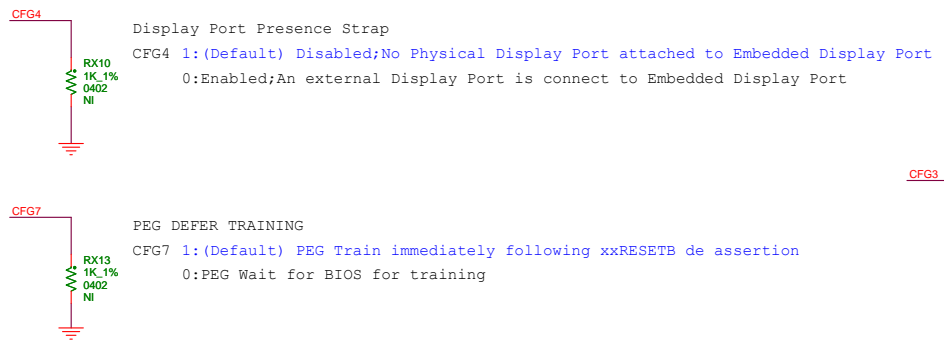
Trace width :
 PEG_COMP from CPU socket PIN H22 and J22 to Res RX1 is 4mils
 PEG_ICOMPO from CPU socket PIN J21 to Res RX1 is 12mils



Control 1.05V VR Setting (for 2012 CPU)
 H_SNB_IVB#_PWRCTRL LOW: 1.0V
 H_SNB_IVB#_PWRCTRL HIGH or NC: 1.05V

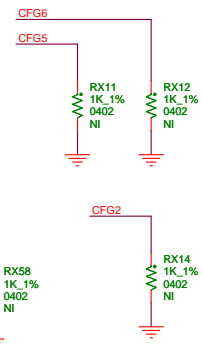


RESERVED



Display Port Presence Strap
 CFG4 1:(Default) Disabled/No Physical Display Port attached to Embedded Display Port
 0:Enabled;An external Display Port is connect to Embedded Display Port

PEG DEFER TRAINING
 CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion
 0:PEG Wait for BIOS for training



PCIE Port Bifurcation Straps
 CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
 10:x:8,x8 - Device 1 function 1 enabled ; function 2 disabled
 01:Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00:x:8,x4,x4 - (Device 1 functions 1 & 2 enabled)

PEG Static Lane Reversal - CFG2 is for the 16x
 CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition
 0:Lane Reversed

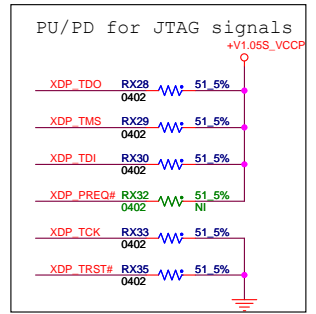
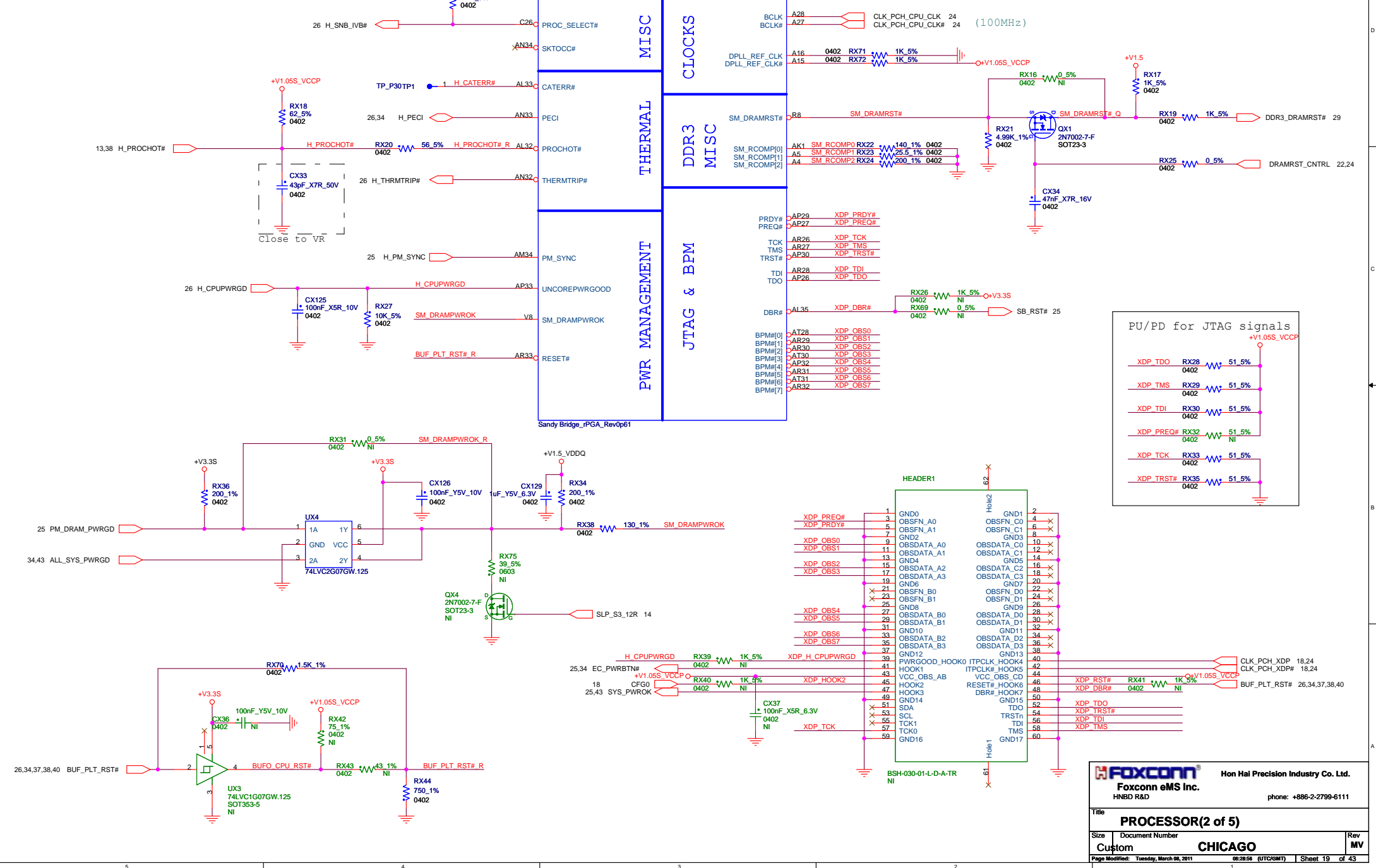
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Title: **PROCESSOR(1 of 5)**

Size: Document Number
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- +V3.3S → +V3.3S 13,14,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
- +V1.05S_VCCP → +V1.05S_VCCP 11,14,18,21,23,24,25,26,27,28,43
- +V1.5_VDDQ → +V1.5_VDDQ 12,14,22,27,38
- +V1.8S → +V1.8S 14,16,22,28,43
- +V1.5C → +V1.5 12,14,15,22,29,43

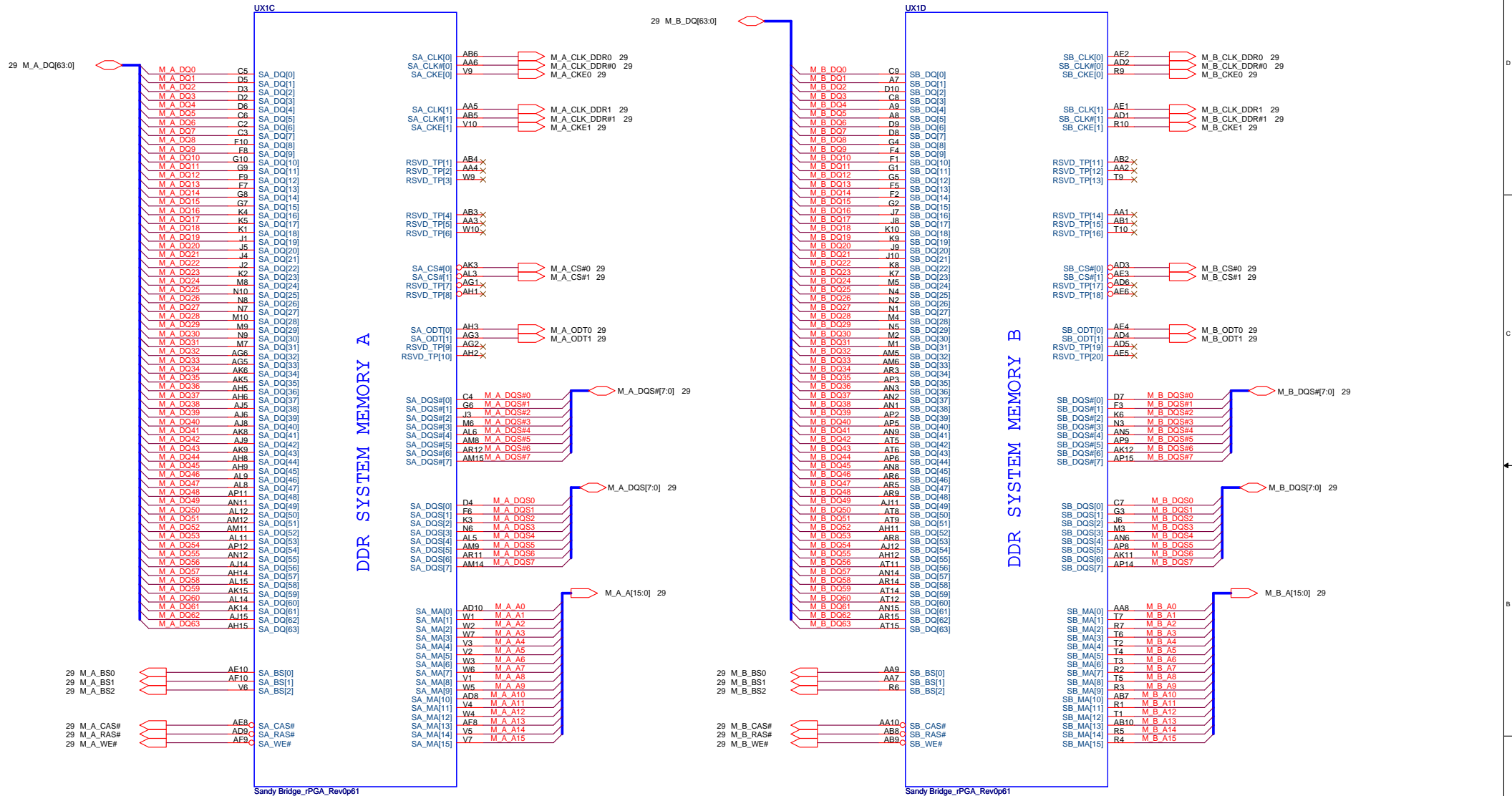


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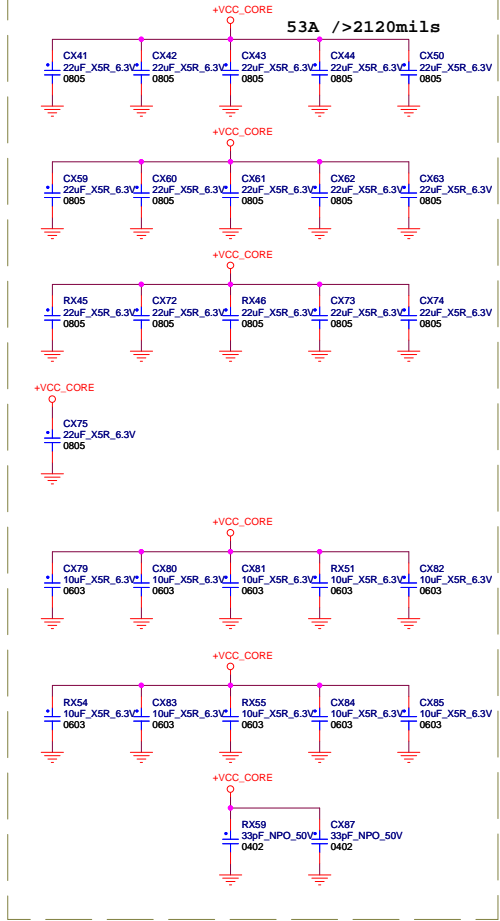
Sandy Bridge_rPGA_Rev0p61

Sandy Bridge_rPGA_Rev0p61

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Title			
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+V1.05S_VCCP \rightarrow +V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43
 +VCC_CORE \rightarrow +VCC_CORE 13,18,43

FOR VCC:
 4x 330 μ F Bottom Edge,
 10x 0603 10 μ F Bottom Cavity,
 8x 0805 22 μ F Top Cavity,
 8x 0805 22 μ F Top Edge,



- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AD36 VCC20
- AD34 VCC21
- AD33 VCC22
- AD32 VCC23
- AD31 VCC24
- VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC34 VCC31
- AC33 VCC32
- AC32 VCC33
- AC31 VCC34
- AC30 VCC35
- AC29 VCC36
- AC28 VCC37
- AC27 VCC38
- AC26 VCC39
- AA35 VCC40
- AA34 VCC41
- AA33 VCC42
- AA32 VCC43
- AA31 VCC44
- AA30 VCC45
- AA29 VCC46
- AA28 VCC47
- AA27 VCC48
- AA26 VCC49
- VCC50
- VCC51
- Y32 VCC52
- Y31 VCC53
- Y30 VCC54
- Y29 VCC55
- Y28 VCC56
- Y27 VCC57
- Y26 VCC58
- VCC59
- VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- V25 VCC70
- U34 VCC71
- U33 VCC72
- U32 VCC73
- U31 VCC74
- U30 VCC75
- U29 VCC76
- U28 VCC77
- U27 VCC78
- U26 VCC79
- VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- VCC99
- P26 VCC100

POWER

PEG AND DDR

CORE SUPPLY

SVID

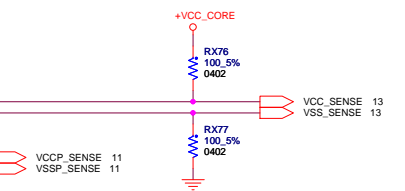
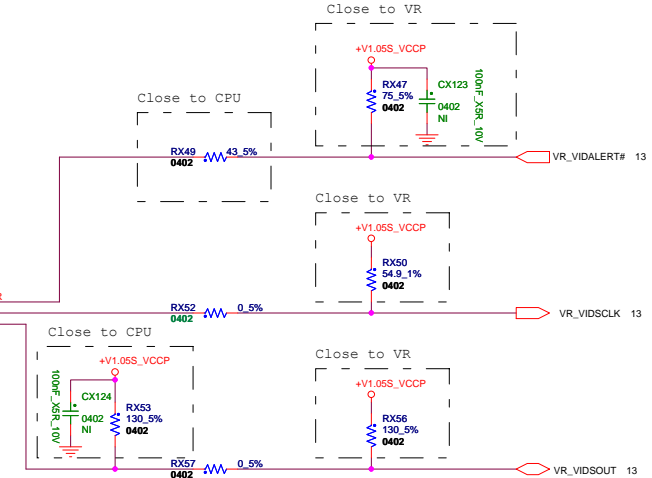
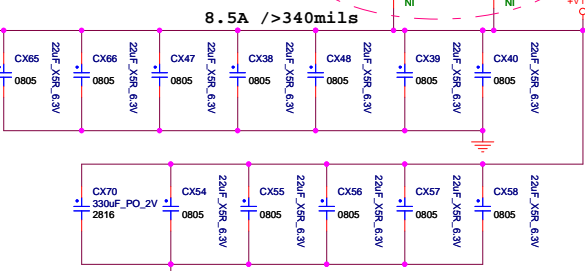
SENSE LINES

- AH13 VCCIO1
- AH10 VCCIO2
- AC10 VCCIO3
- Y10 VCCIO4
- L10 VCCIO5
- L10 VCCIO6
- F10 VCCIO7
- L10 VCCIO8
- J14 VCCIO9
- J13 VCCIO10
- J12 VCCIO11
- J11 VCCIO12
- H14 VCCIO13
- H12 VCCIO14
- H11 VCCIO15
- G14 VCCIO16
- G13 VCCIO17
- G12 VCCIO18
- E14 VCCIO19
- E13 VCCIO20
- E12 VCCIO21
- E11 VCCIO22
- E14 VCCIO23
- E12 VCCIO24
- E11 VCCIO25
- D14 VCCIO26
- D13 VCCIO27
- D12 VCCIO28
- D11 VCCIO29
- C14 VCCIO30
- C13 VCCIO31
- C12 VCCIO32
- C11 VCCIO33
- B14 VCCIO34
- B12 VCCIO35
- A14 VCCIO36
- A13 VCCIO37
- A12 VCCIO38
- A11 VCCIO39
- J23 VCCIO40

- AJ29 VR_SVID_ALERT# R
- AJ30 VR_SVID_CLK R
- AJ28 VR_SVID_DATA R

- AJ35 VCC_SENSE
- AJ34 VSS_SENSE
- B10 VCCIO_SENSE
- A10 VSSIO_SENSE

FOR VCCIO:
 2x 330 μ F,
 5x 0805 22 μ F Bottom Cavity,
 7x 0805 22 μ F Top Cavity,

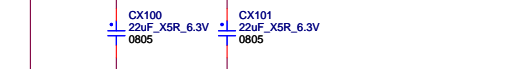
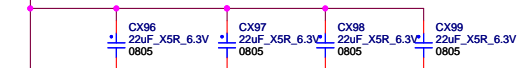
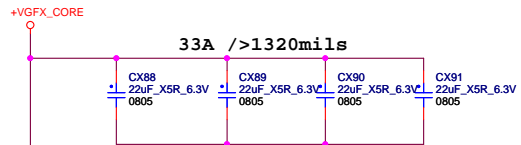


- AT36 VSS1
- AT32 VSS2
- AT29 VSS3
- AT27 VSS4
- AT25 VSS5
- AT19 VSS6
- AT16 VSS7
- AT11 VSS8
- AT7 VSS9
- AT3 VSS10
- AR25 VSS11
- AR14 VSS12
- AR13 VSS13
- AR12 VSS14
- AR11 VSS15
- AR10 VSS16
- AR7 VSS17
- AR4 VSS18
- AR2 VSS19
- AP24 VSS20
- AP23 VSS21
- AP22 VSS22
- AP21 VSS23
- AP19 VSS24
- AP18 VSS25
- AP13 VSS26
- AP10 VSS27
- AP7 VSS28
- AP4 VSS29
- AN30 VSS30
- AN27 VSS31
- AN25 VSS32
- AN22 VSS33
- AN19 VSS34
- AN18 VSS35
- AN16 VSS36
- AN13 VSS37
- AN10 VSS38
- AN7 VSS39
- AN4 VSS40
- AM29 VSS41
- AM25 VSS42
- AM22 VSS43
- AM19 VSS44
- AM16 VSS45
- AM15 VSS46
- AM10 VSS47
- AM7 VSS48
- AM4 VSS49
- AM2 VSS50
- AL34 VSS51
- AL31 VSS52
- AL28 VSS53
- AL25 VSS54
- AL22 VSS55
- AL19 VSS56
- AL16 VSS57
- AL13 VSS58
- AL10 VSS59
- AL7 VSS60
- AL4 VSS61
- AL2 VSS62
- AK33 VSS63
- AK30 VSS64
- AK27 VSS65
- AK22 VSS66
- AK19 VSS67
- AK16 VSS68
- AK13 VSS69
- AK10 VSS70
- AK7 VSS71
- AK4 VSS72
- AL25 VSS73
- VSS81
- AJ22
- AH19
- VSS82
- AH16
- VSS83
- AJ13
- VSS84
- AJ10
- VSS85
- AJ7
- VSS86
- AH4
- VSS87
- AJ3
- VSS88
- AH35
- VSS89
- AJ1
- VSS90
- AH35
- VSS91
- AH34
- VSS92
- AH32
- VSS93
- AH30
- VSS94
- AH29
- VSS95
- AH28
- VSS96
- AH27
- VSS97
- AH25
- VSS98
- AH22
- VSS99
- AH19
- VSS100
- AH17
- VSS101
- AH16
- VSS102
- AH14
- VSS103
- AG9
- VSS104
- AG8
- VSS105
- AG8
- VSS106
- AF6
- VSS107
- AF5
- VSS108
- AF3
- VSS109
- AE2
- VSS110
- AE25
- VSS111
- AE35
- VSS112
- AE34
- VSS113
- AE32
- VSS114
- AE31
- VSS115
- AE29
- VSS116
- AE28
- VSS117
- AE27
- VSS118
- AE26
- VSS119
- AE22
- VSS120
- AE9
- VSS121
- AD7
- VSS122
- AC9
- VSS123
- AC8
- VSS124
- AC6
- VSS125
- AC5
- VSS126
- AC3
- VSS127
- AC2
- VSS128
- AB35
- VSS129
- AB34
- VSS130
- AB33
- VSS131
- AB32
- VSS132
- AB31
- VSS133
- AB30
- VSS134
- AB29
- VSS135
- AB28
- VSS136
- AB27
- VSS137
- AB26
- VSS138
- Y9
- VSS139
- Y6
- VSS140
- Y3
- VSS141
- Y2
- VSS142
- W35
- VSS143
- W34
- VSS144
- W32
- VSS145
- W31
- VSS146
- W30
- VSS147
- W29
- VSS148
- W28
- VSS149
- W27
- VSS150
- W26
- VSS151
- U9
- VSS152
- U7
- VSS153
- U6
- VSS154
- U5
- VSS155
- U4
- VSS156
- U3
- VSS157
- U2
- VSS158
- U1
- VSS159
- U2
- VSS160

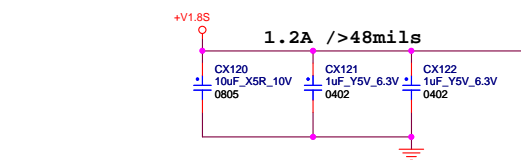
Sandy Bridge_rPGA_Rev0p61

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Title: **PROCESSOR(4 of 5)**
 Size: Document Number
 Custom: **CHICAGO** Rev: MV
 Page Modified: Tuesday, March 06, 2011 08:28:06 (UTC/GMT) Sheet 21 of 43

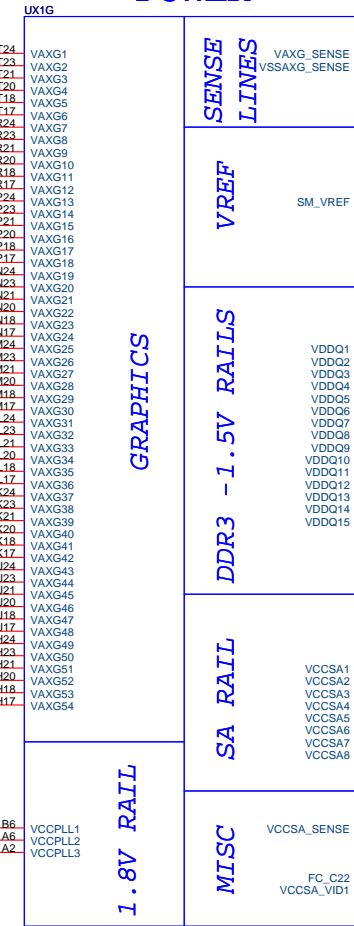


FOR VAXG:
 2x 330 μ F Bottom Edge,
 4x 0805 22 μ F Top & Bottom Cavity,
 8x 0805 22 μ F Top & Bottom Edge,

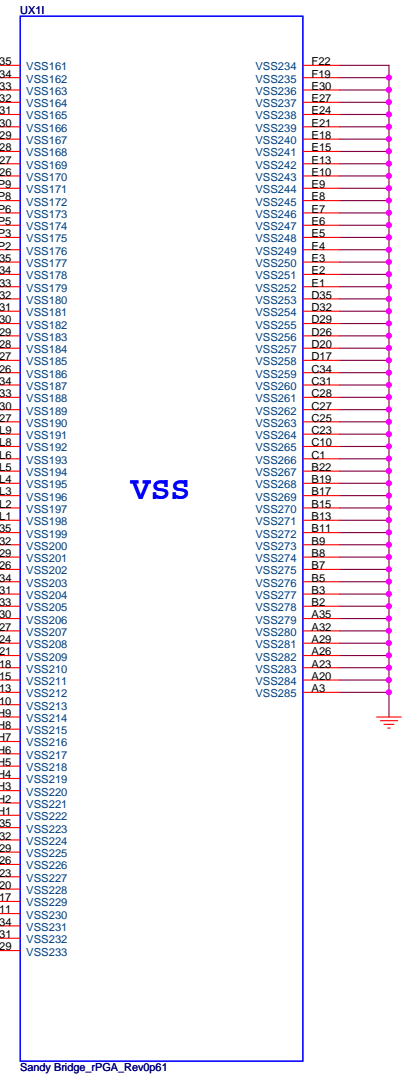
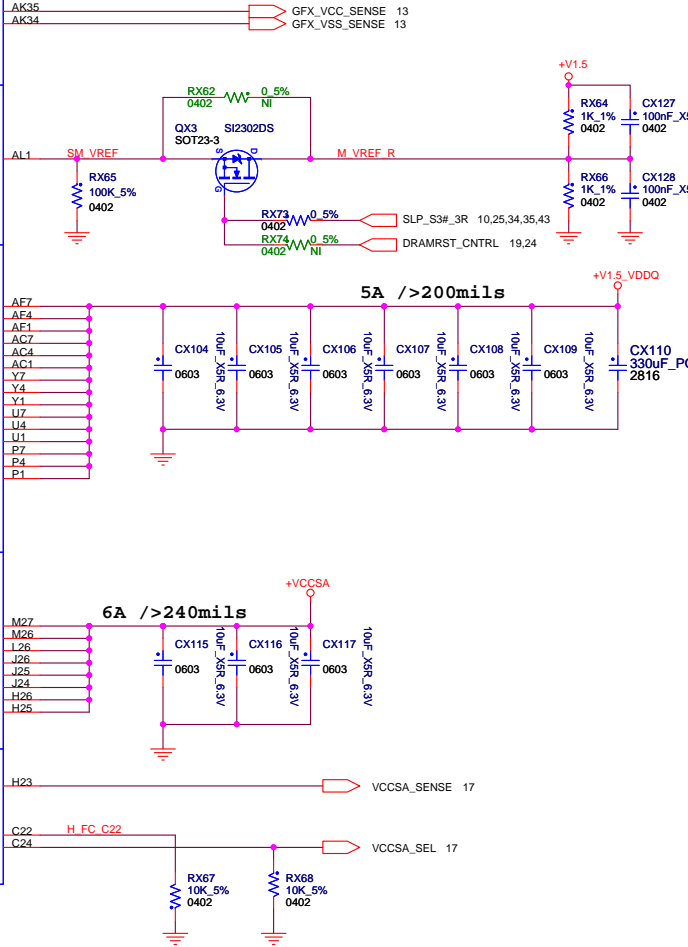
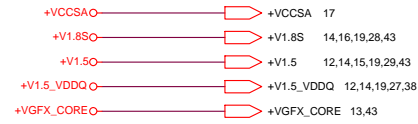


FOR VCCPLL:
 1x 330 μ F Bottom Edge,
 2x 0402 1 μ F Bottom Edge,
 1x 0805 10 μ F Bottom Edge,

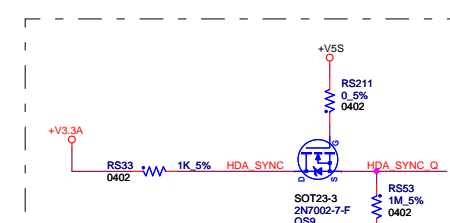
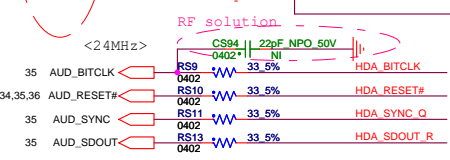
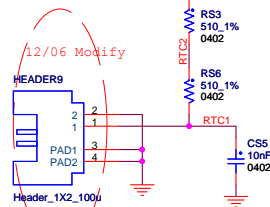
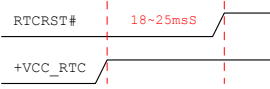
POWER



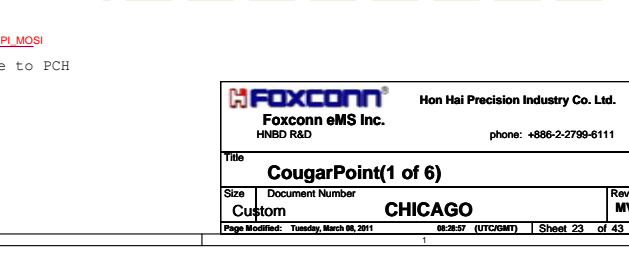
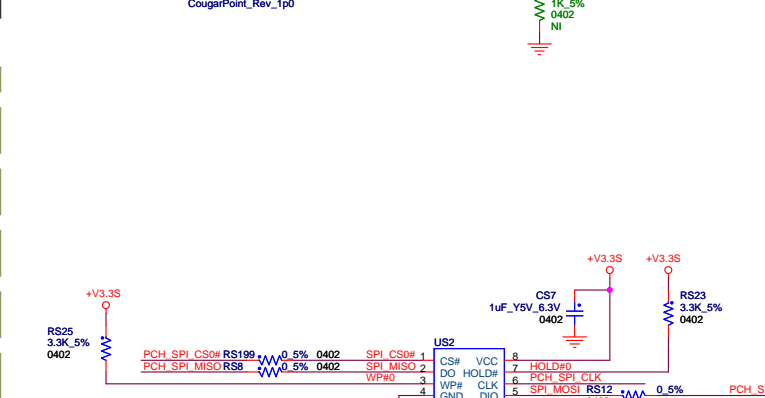
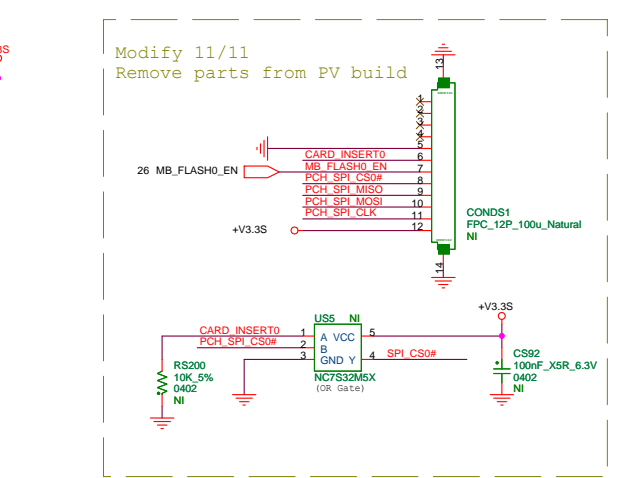
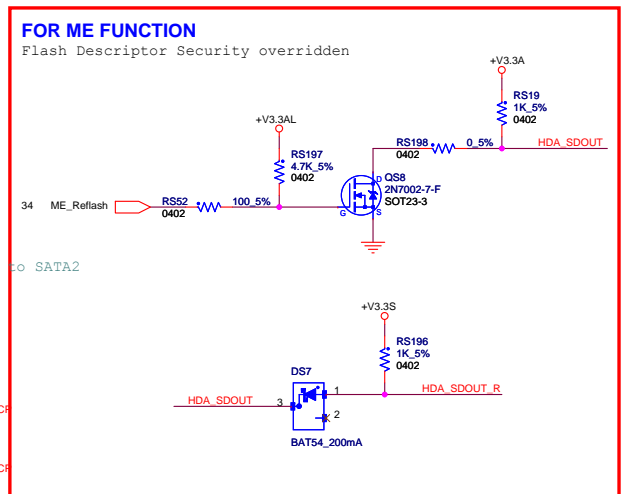
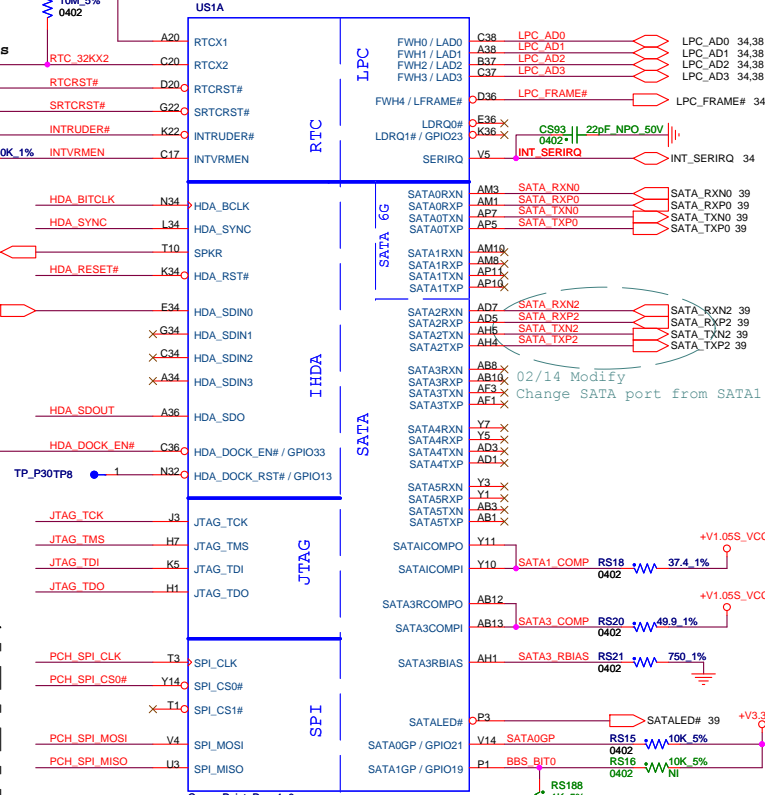
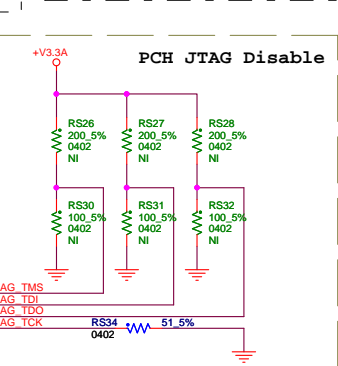
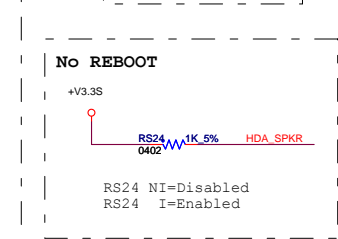
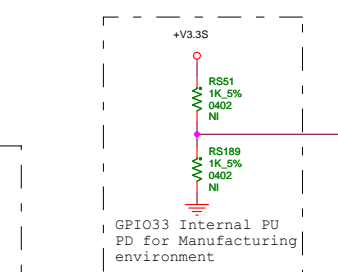
Sandy Bridge_PGA_Rev0p61

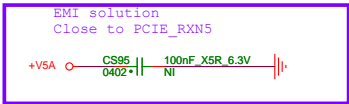
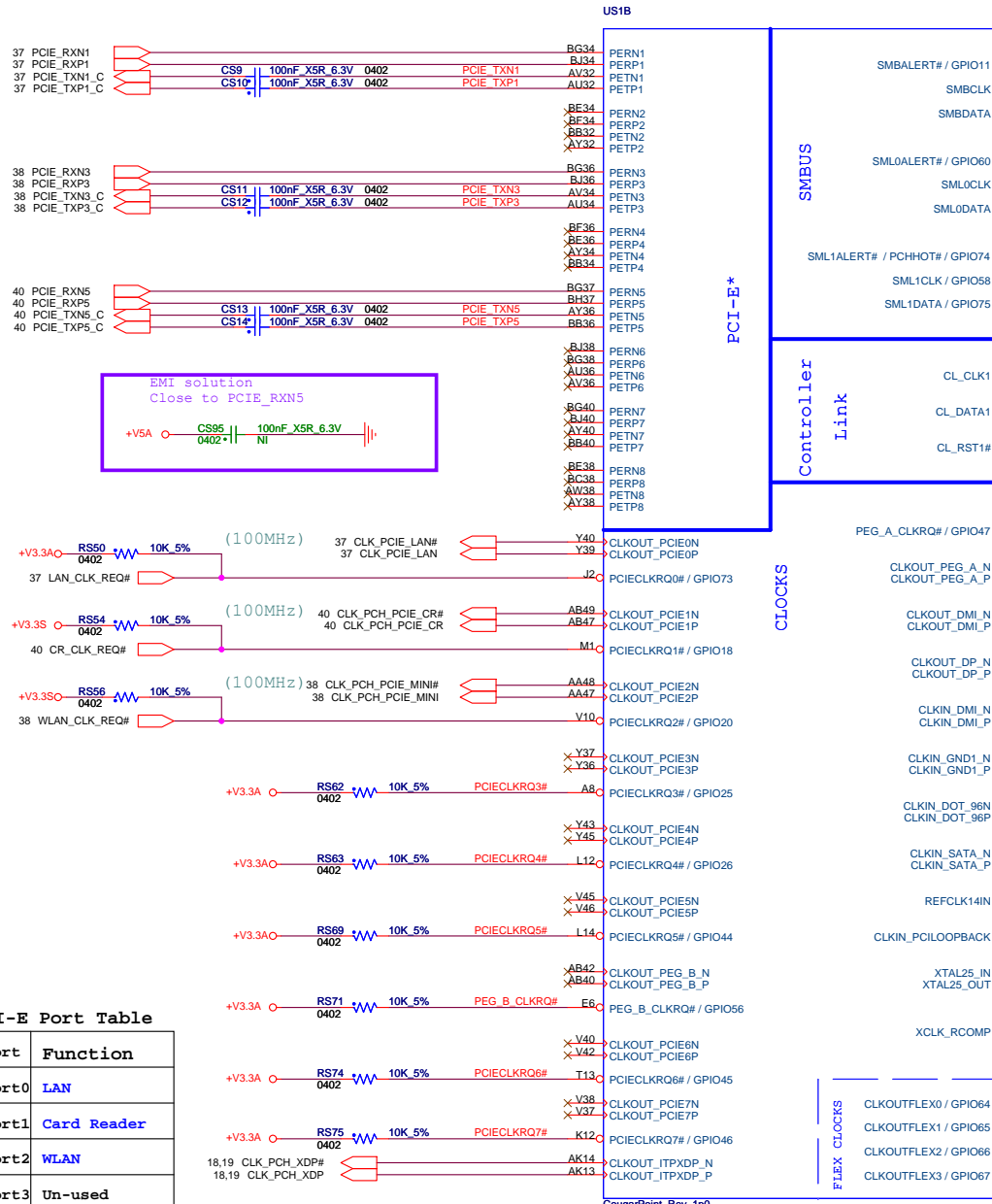


Sandy Bridge_PGA_Rev0p61



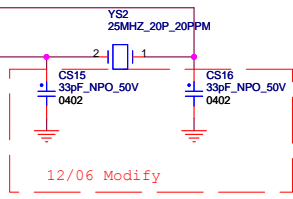
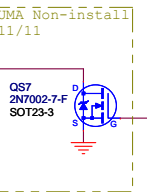
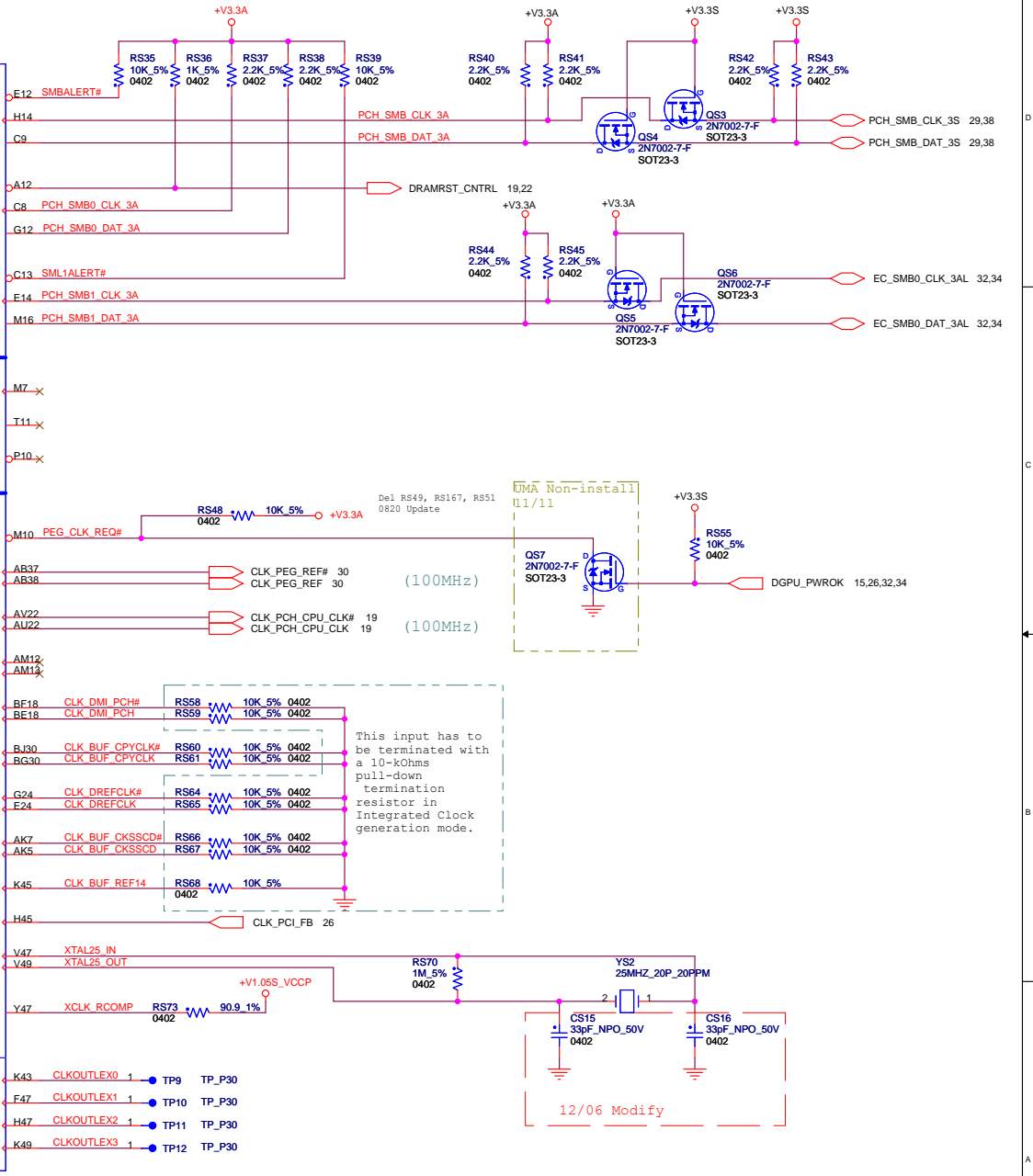
On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. (Default:1.5V for Mobile)

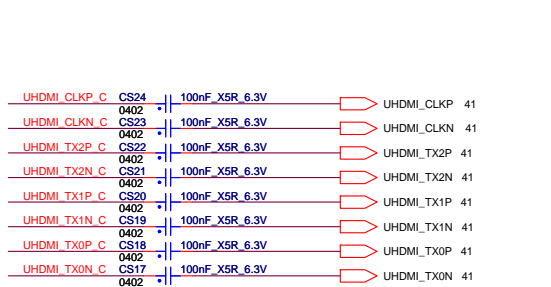
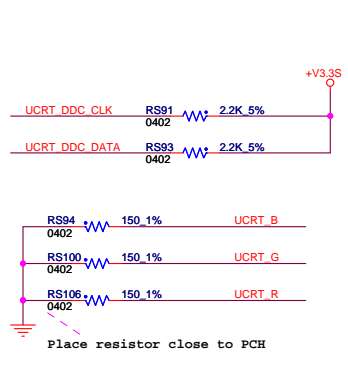
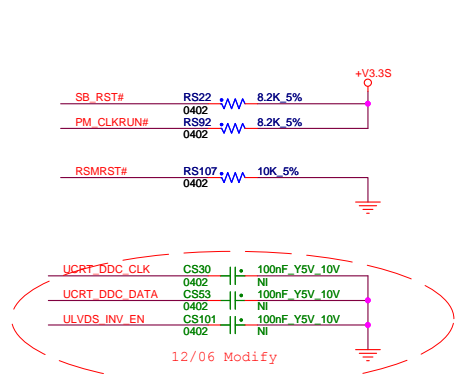
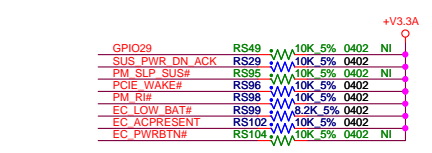
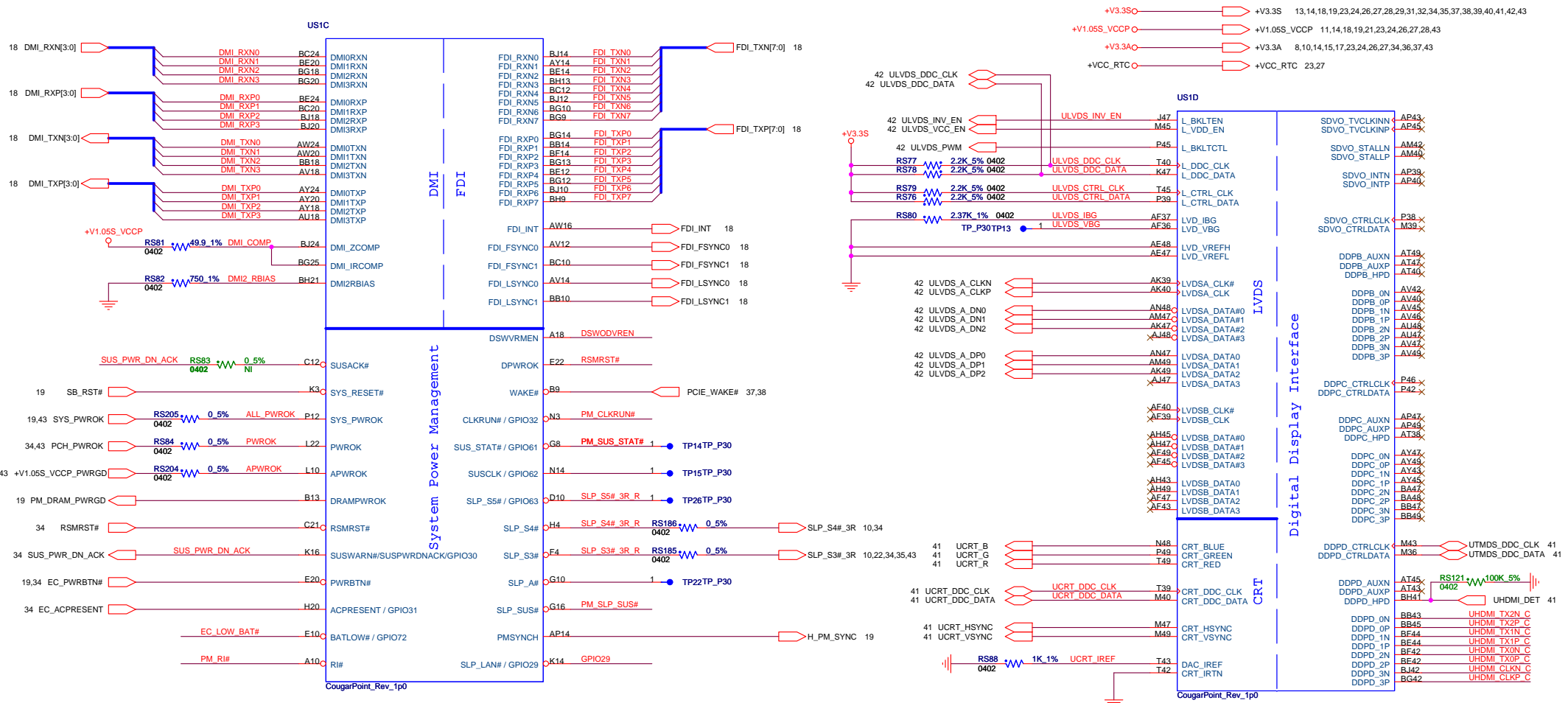




PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used





DSWODVREN - on Die DSW VR Enable

RS97	RS103	
I	NI	Enabled
NI	I	Disabled

12/06 Modify
Modify CS30/CS53/CS101 to non-stuff on 01/11

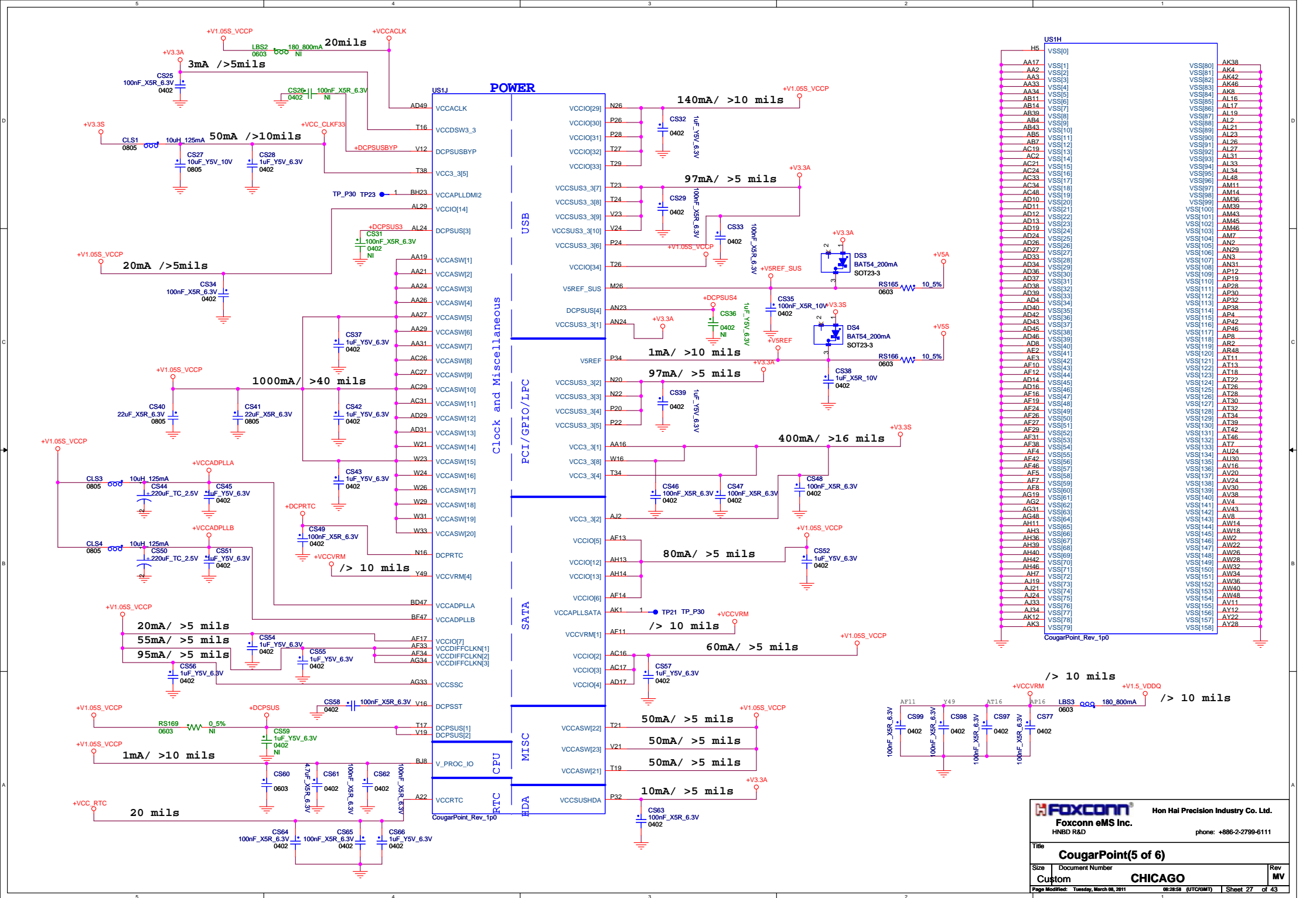
Place resistor close to PCH

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Title: **CougarPoint(3 of 6)**

Size: Document Number
 Custom **CHICAGO** Rev **MV**

Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT) Sheet 25 of 43



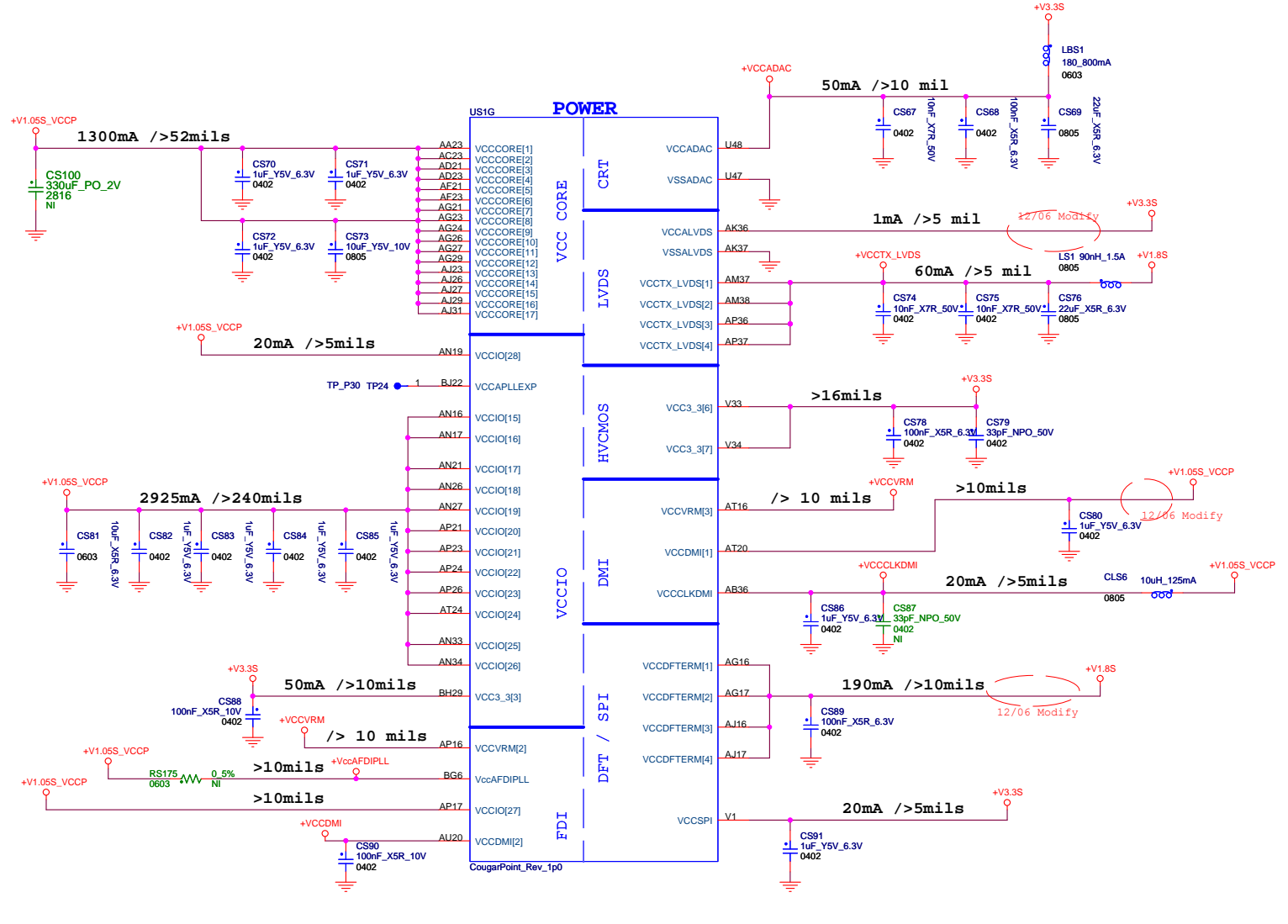
FOXCONN Hon Hai Precision Industry Co. Ltd.
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 HNBD R&D phone: +886-2-2799-6111

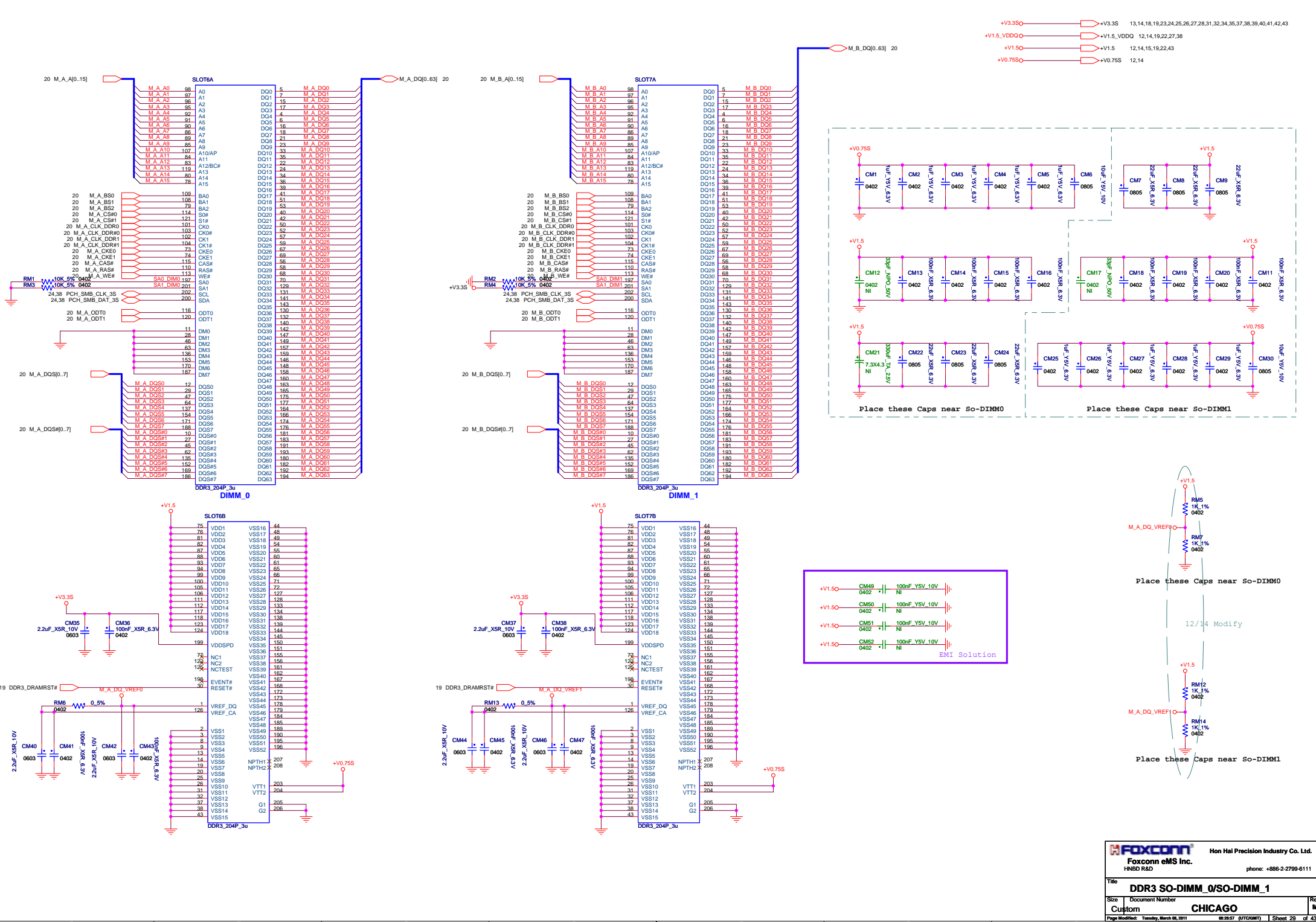
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Size: Document Number
 Custom **CHICAGO** Rev **MV**

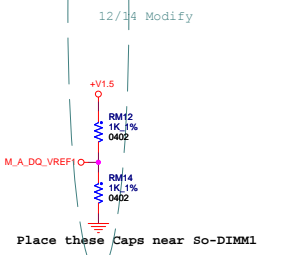
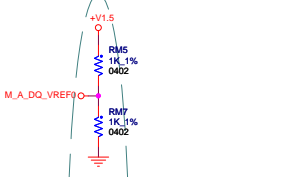
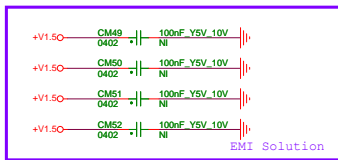
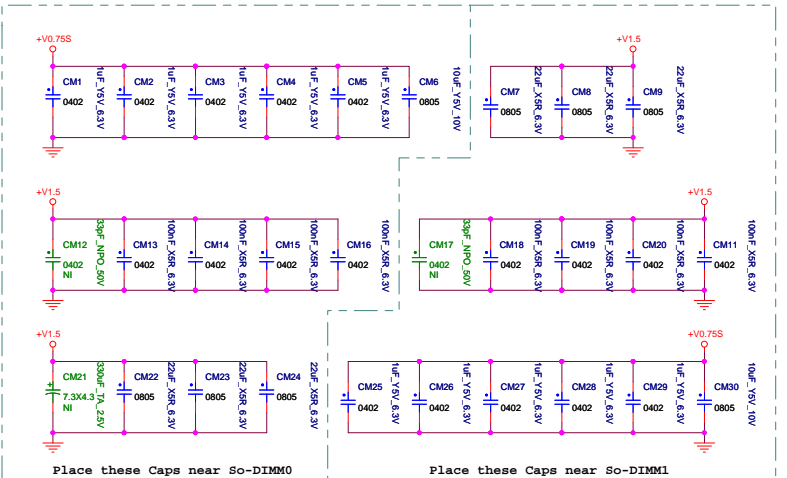
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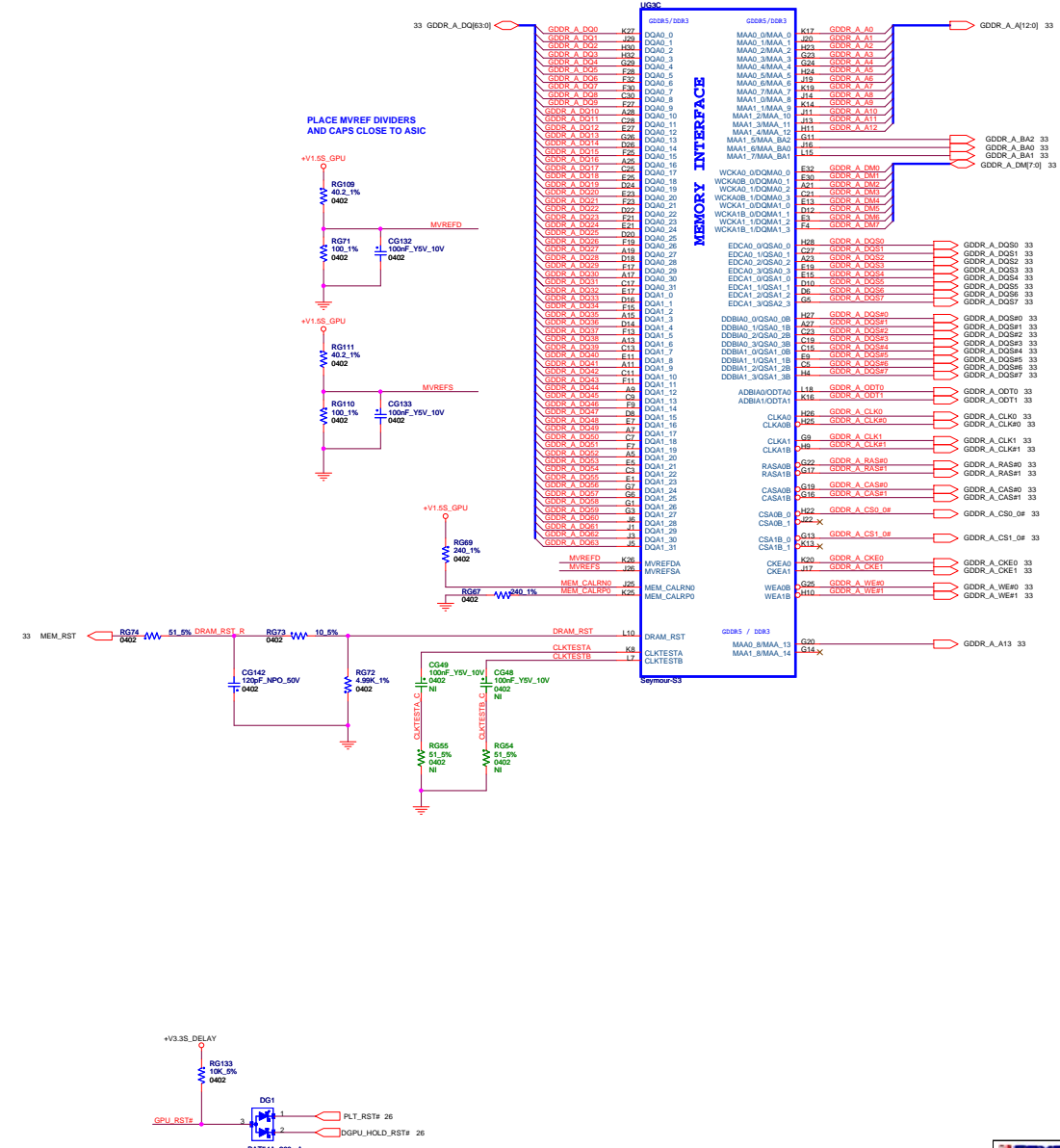
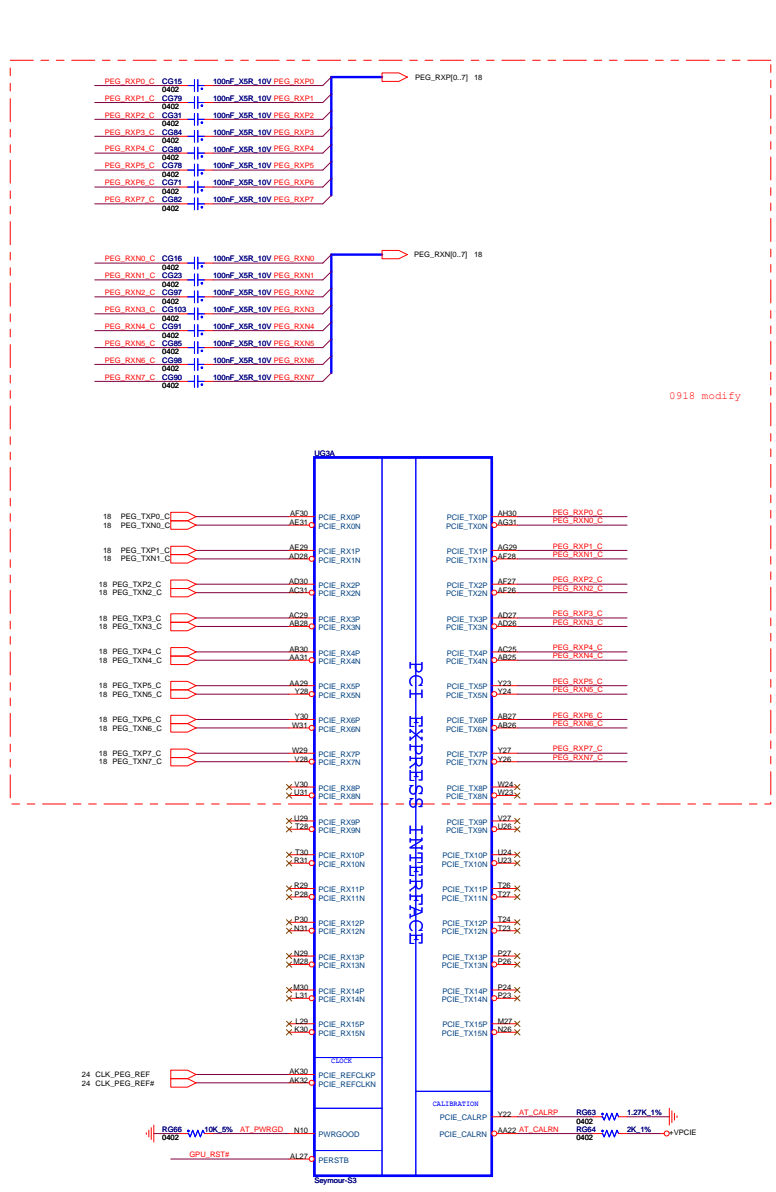
US11		
AY4	VSS[159]	VSS[259]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B15	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
BC14	VSS[183]	VSS[283]
BC18	VSS[184]	VSS[284]
BC2	VSS[185]	VSS[285]
BC22	VSS[186]	VSS[286]
BC26	VSS[187]	VSS[287]
BC32	VSS[188]	VSS[288]
BC34	VSS[189]	VSS[289]
BC36	VSS[190]	VSS[290]
BC40	VSS[191]	VSS[291]
BC42	VSS[192]	VSS[292]
BC48	VSS[193]	VSS[293]
BD46	VSS[194]	VSS[294]
BD8	VSS[195]	VSS[295]
BE22	VSS[196]	VSS[296]
BE26	VSS[197]	VSS[297]
BE40	VSS[198]	VSS[298]
BE10	VSS[199]	VSS[299]
BE12	VSS[200]	VSS[300]
BE16	VSS[201]	VSS[301]
BE20	VSS[202]	VSS[302]
BE24	VSS[203]	VSS[303]
BE26	VSS[204]	VSS[304]
BE28	VSS[205]	VSS[305]
BD3	VSS[207]	VSS[307]
BF30	VSS[208]	VSS[308]
BF38	VSS[209]	VSS[309]
BF40	VSS[210]	VSS[310]
BF8	VSS[211]	VSS[311]
BG17	VSS[212]	VSS[312]
BG21	VSS[213]	VSS[313]
BG33	VSS[214]	VSS[314]
BG44	VSS[215]	VSS[315]
BG8	VSS[216]	VSS[316]
BH11	VSS[217]	VSS[317]
BH15	VSS[218]	VSS[318]
BH17	VSS[219]	VSS[319]
BH19	VSS[220]	VSS[320]
H10	VSS[221]	VSS[321]
BH27	VSS[222]	VSS[322]
BH31	VSS[223]	VSS[323]
BH33	VSS[224]	VSS[324]
BH35	VSS[225]	VSS[325]
BH39	VSS[226]	VSS[326]
BH43	VSS[227]	VSS[327]
BH7	VSS[228]	VSS[328]
D3	VSS[229]	VSS[329]
D12	VSS[230]	VSS[330]
D16	VSS[231]	VSS[331]
D18	VSS[232]	VSS[332]
D22	VSS[233]	VSS[333]
D24	VSS[234]	VSS[334]
D26	VSS[235]	VSS[335]
D30	VSS[236]	VSS[336]
D32	VSS[237]	VSS[337]
D34	VSS[238]	VSS[338]
D38	VSS[239]	VSS[339]
D42	VSS[240]	VSS[340]
D8	VSS[241]	VSS[341]
E18	VSS[242]	VSS[342]
E26	VSS[243]	VSS[343]
G18	VSS[244]	VSS[344]
G20	VSS[245]	VSS[345]
G26	VSS[246]	VSS[346]
G28	VSS[247]	VSS[347]
G38	VSS[248]	VSS[348]
G48	VSS[249]	VSS[349]
H12	VSS[250]	VSS[350]
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

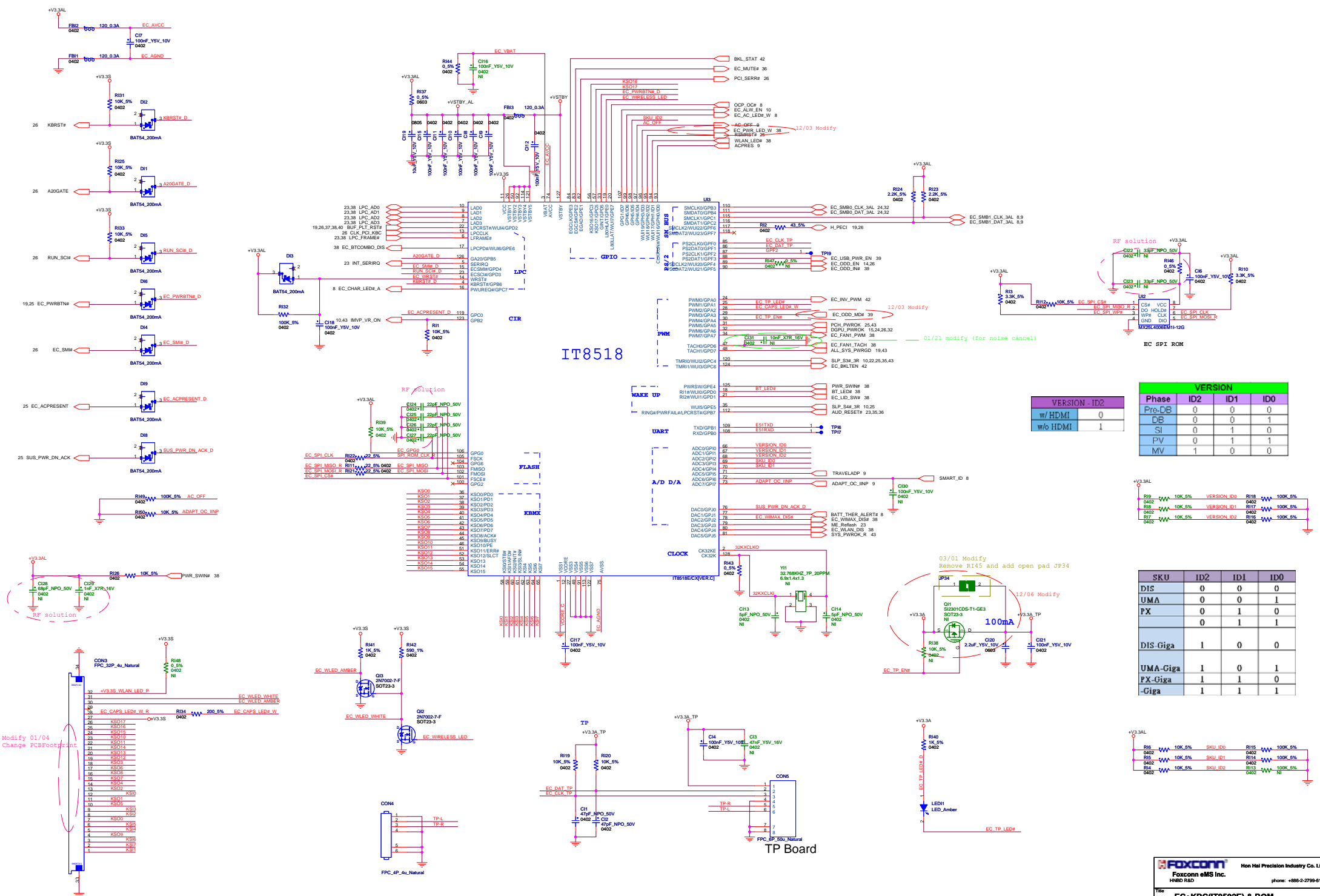




+V3.3S 13,14,18,19,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41,42,43
 +V1.5_VDDQ 12,14,19,22,27,38
 +V1.5 12,14,15,19,22,43
 +V0.75S 12,14







IT5151

VERSION ID2	
w/ HDMI	0
w/o HDMI	1

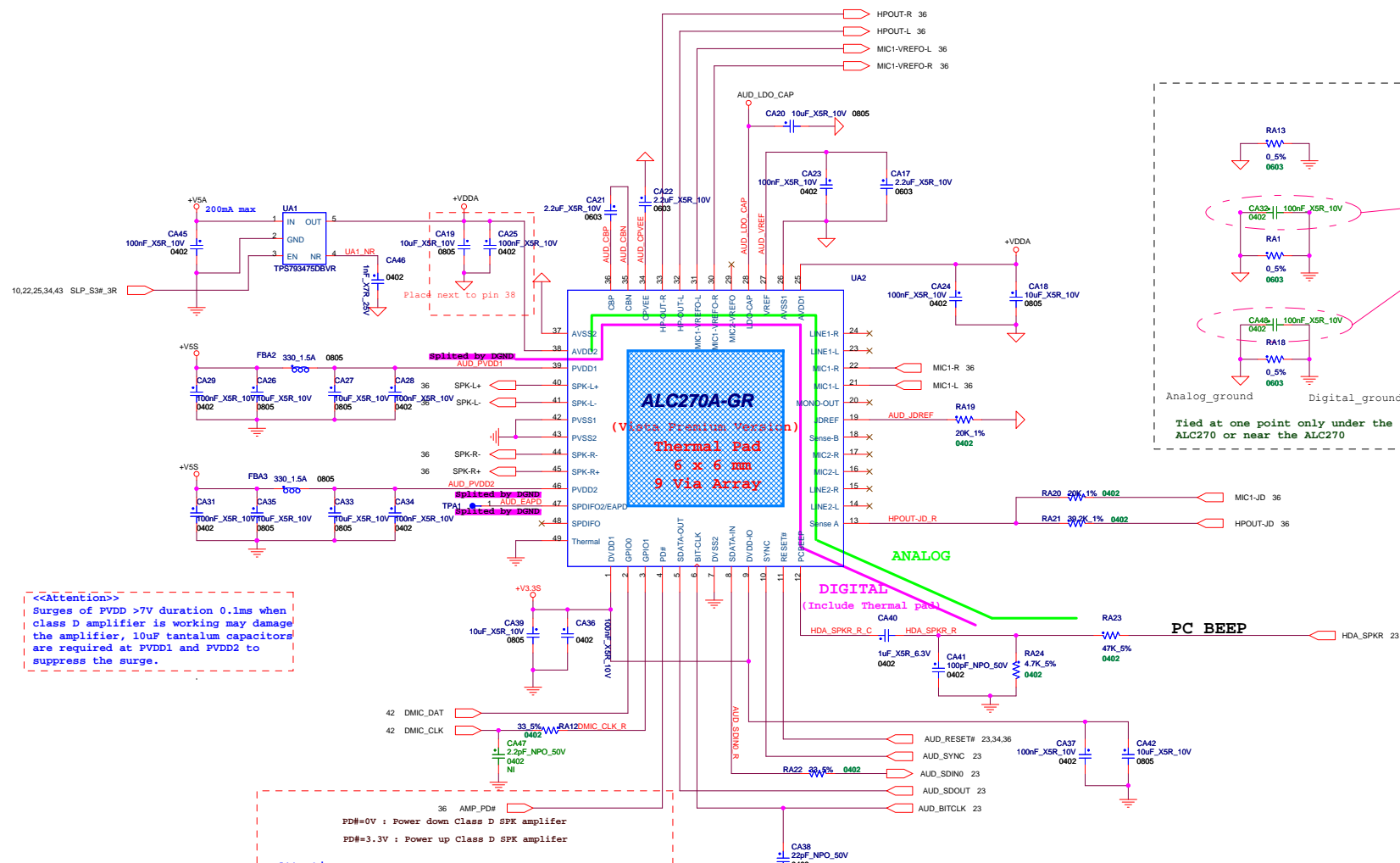
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Pre-DB	0	0	0
DB	0	0	1
SI	0	1	0
PV	0	1	1
MV	1	0	0

SKU			
ID2	ID1	ID0	
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
	0	1	1
DIS Giga	1	0	0
UMA-Giga	1	0	1
PX-Giga	1	1	0
-Giga	1	1	1

Modify 01/04
Change PCB footprint

03/01 Modify
Remove R145 and add open pad JP34

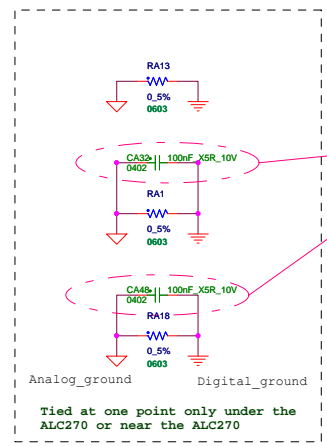
12/06 Modify



<<Attention>>
 Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

36 AMP_PD#
 PD#=0V : Power down Class D SPK amplifier
 PD#=3.3V : Power up Class D SPK amplifier

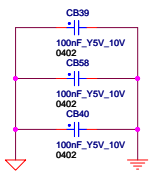
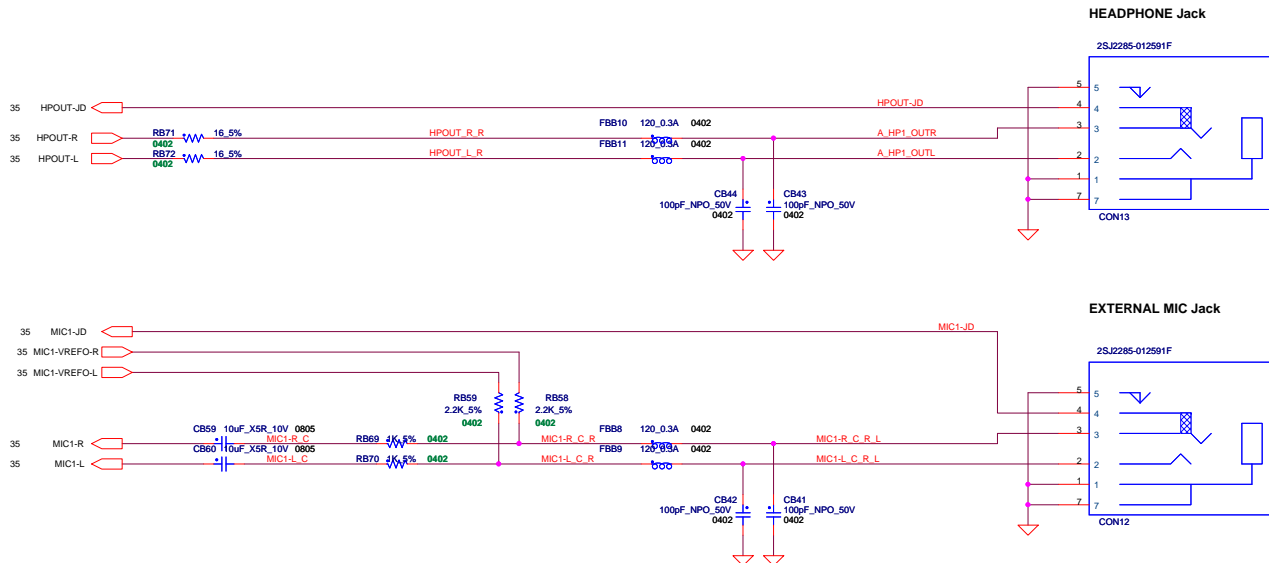
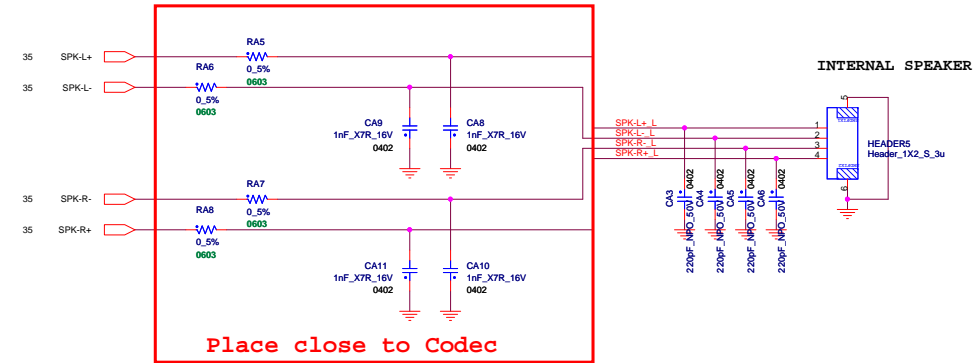
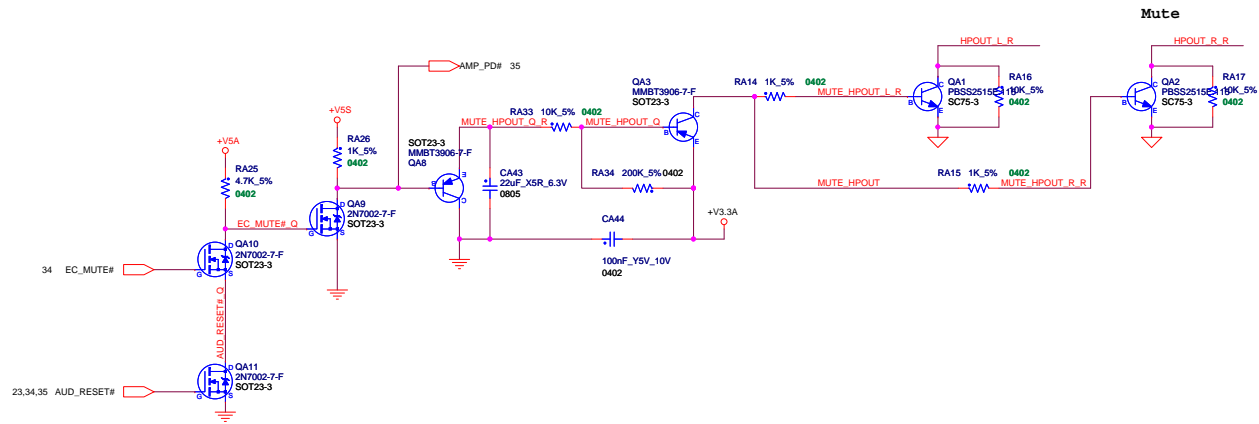
<<Attention>>
 For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
 1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
 2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)

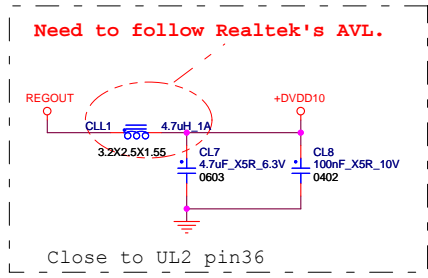
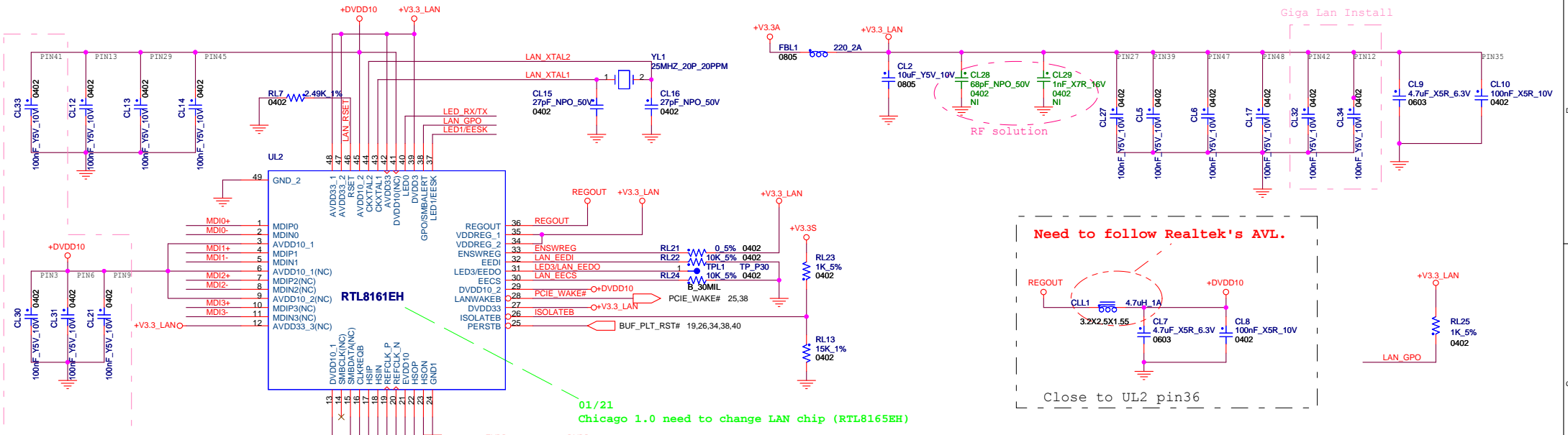


ANALOG
 DIGITAL
 (Include Thermal pad)

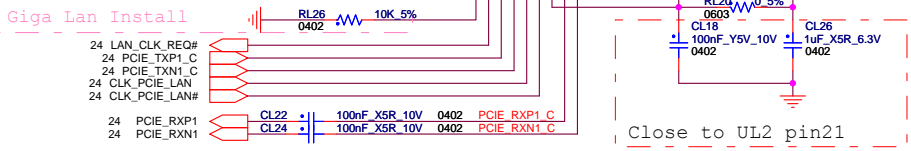
EMI solution

Analog_ground
 Digital_ground
 Tied at one point only under the ALC270 or near the ALC270

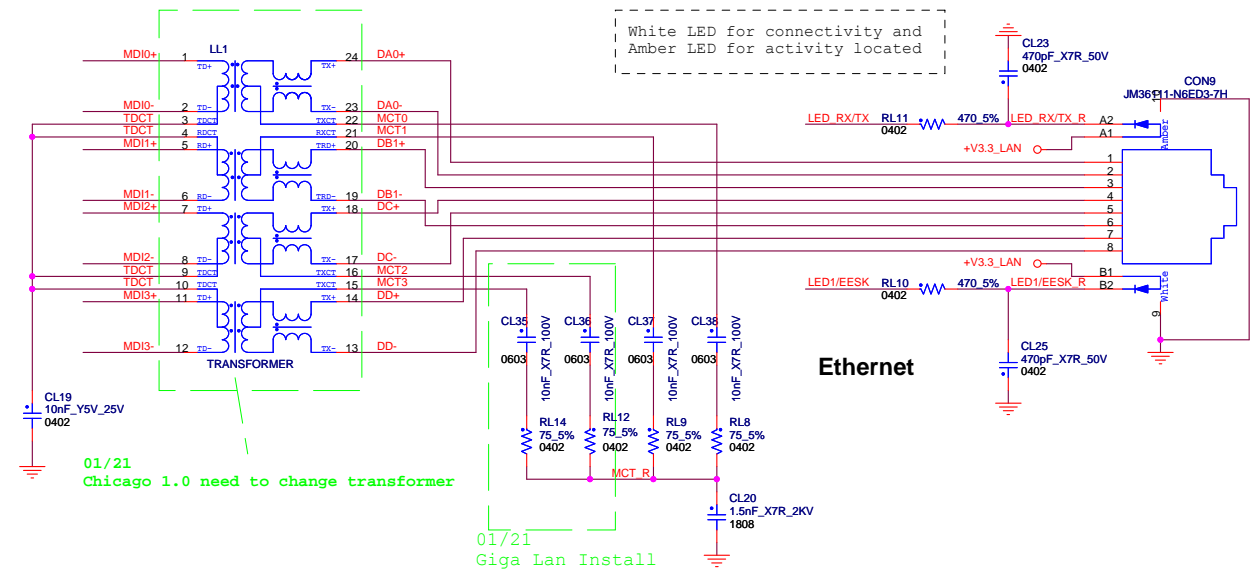




01/21
Chicago 1.0 need to change LAN chip (RTL8165EH)



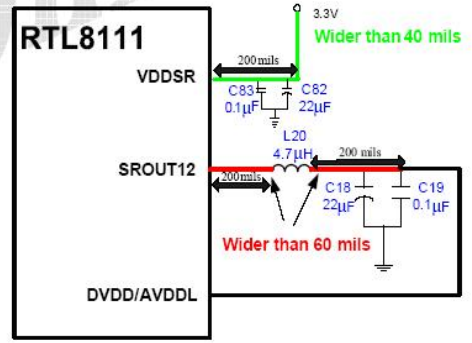
White LED for connectivity and Amber LED for activity located



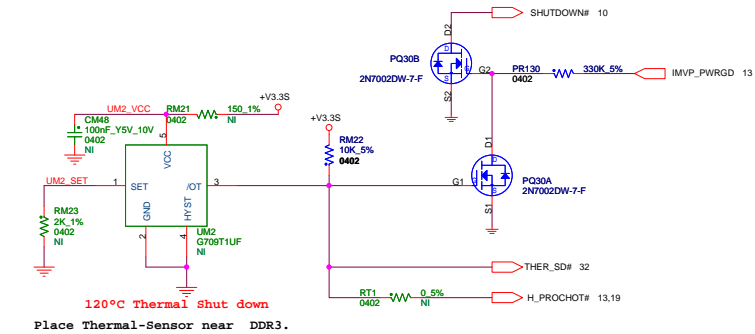
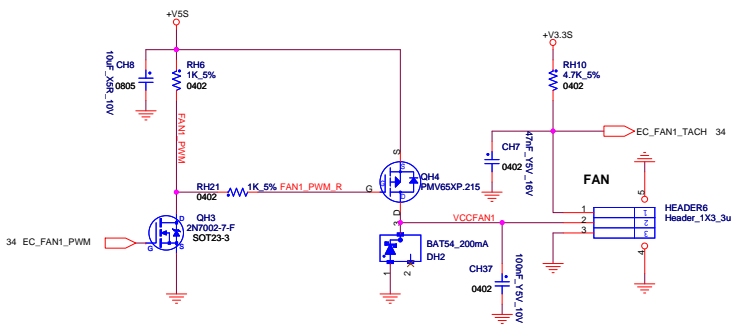
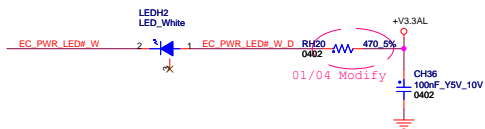
7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

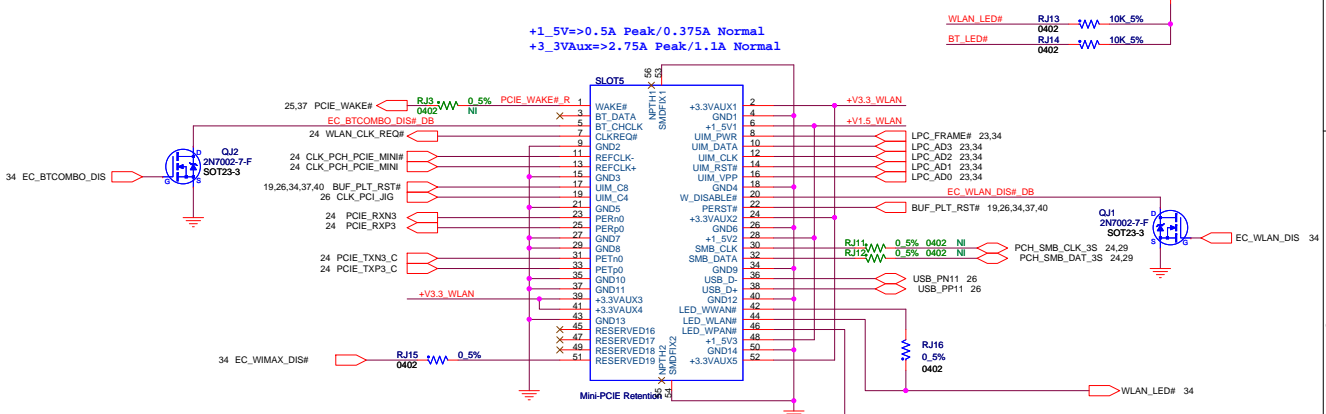
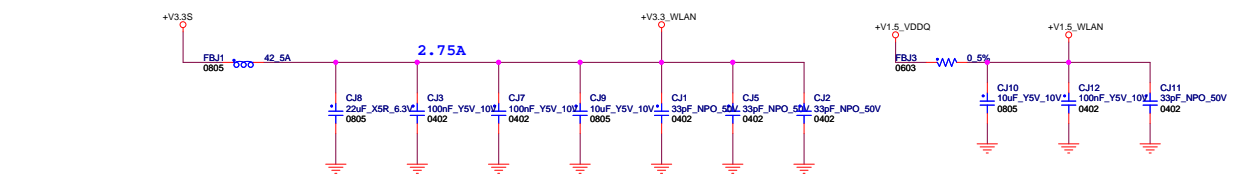
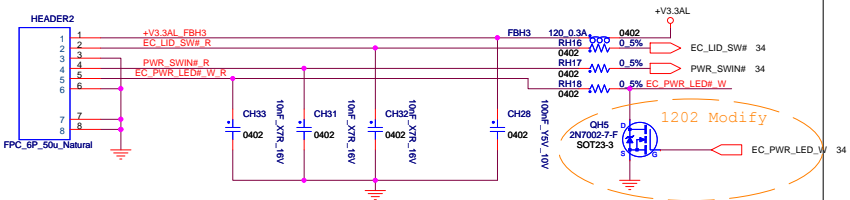
Note: Violation of the above rules will damage the IC.



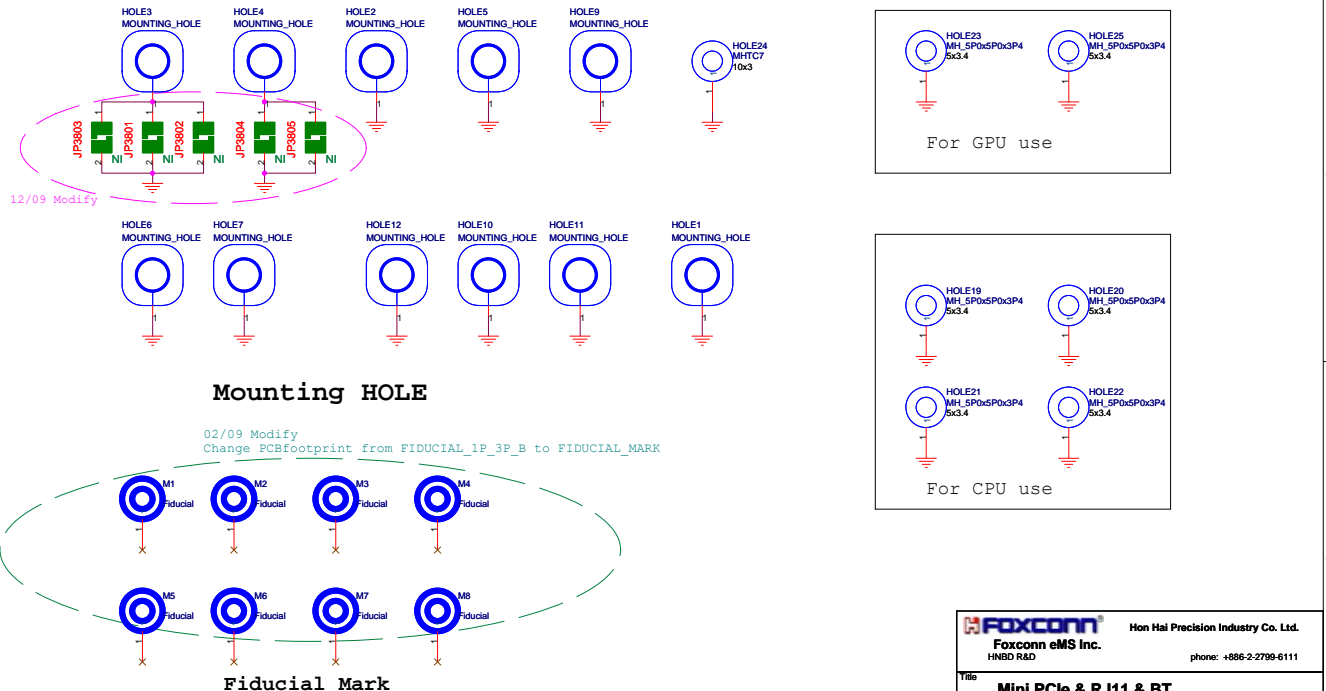
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBDR R&D	
		phone: +886-2-2799-6111	
Title LAN (RTL8165EH)			
Size Custom		Document Number Rev	
Page Modified: Tuesday, March 05, 2011		08:28:59 (UTC+GMT) Sheet 37 of 43	

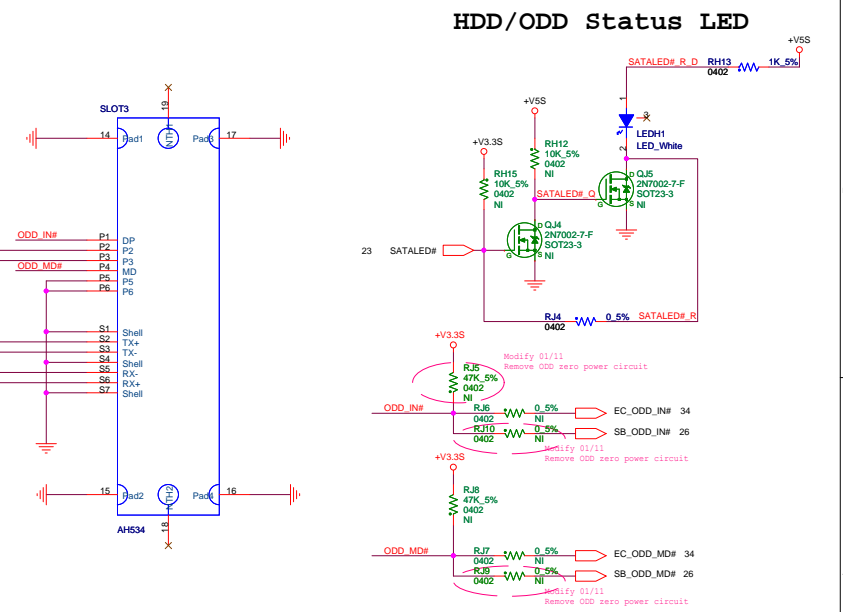
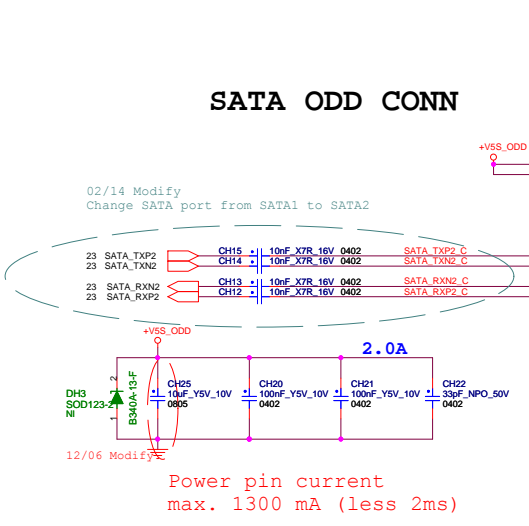
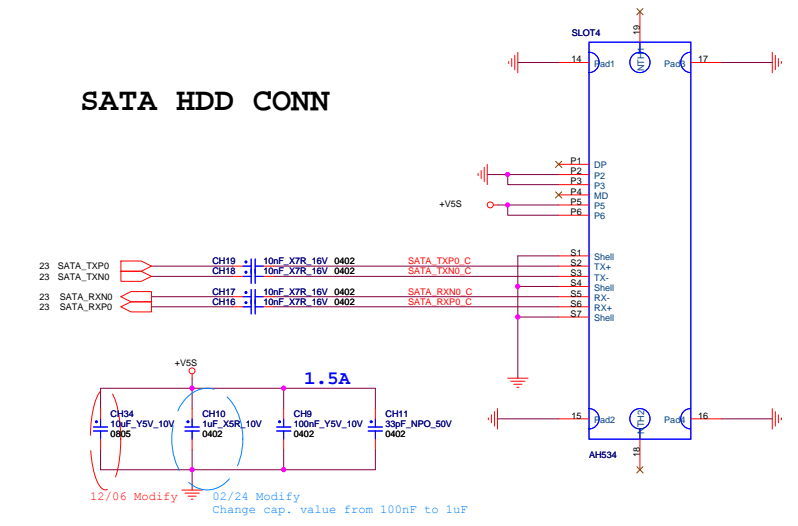
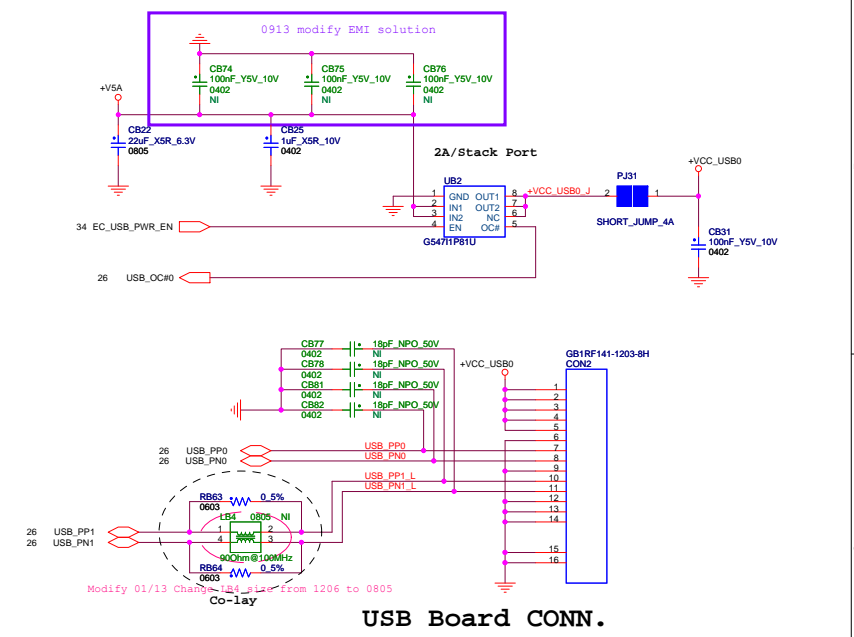
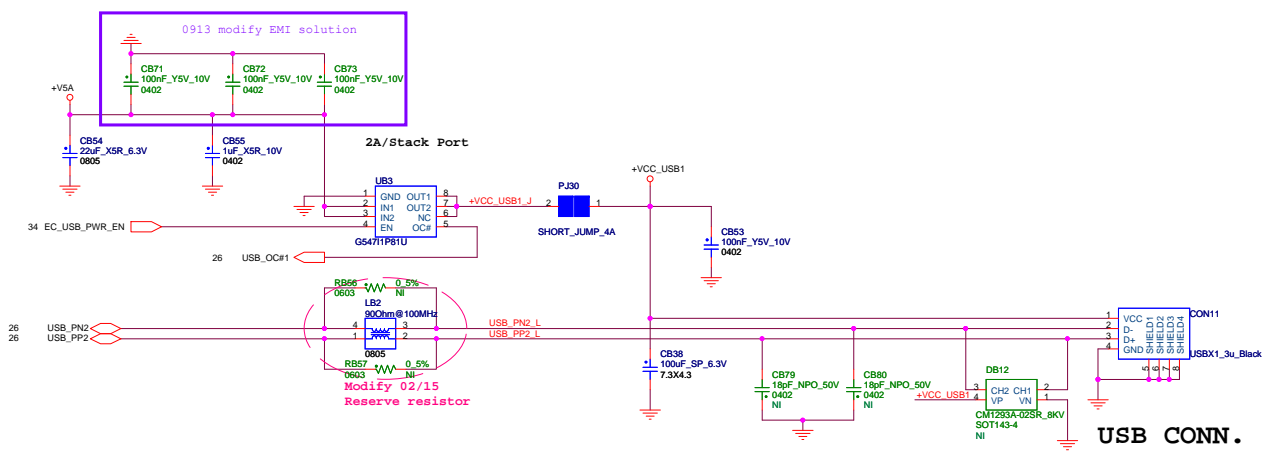


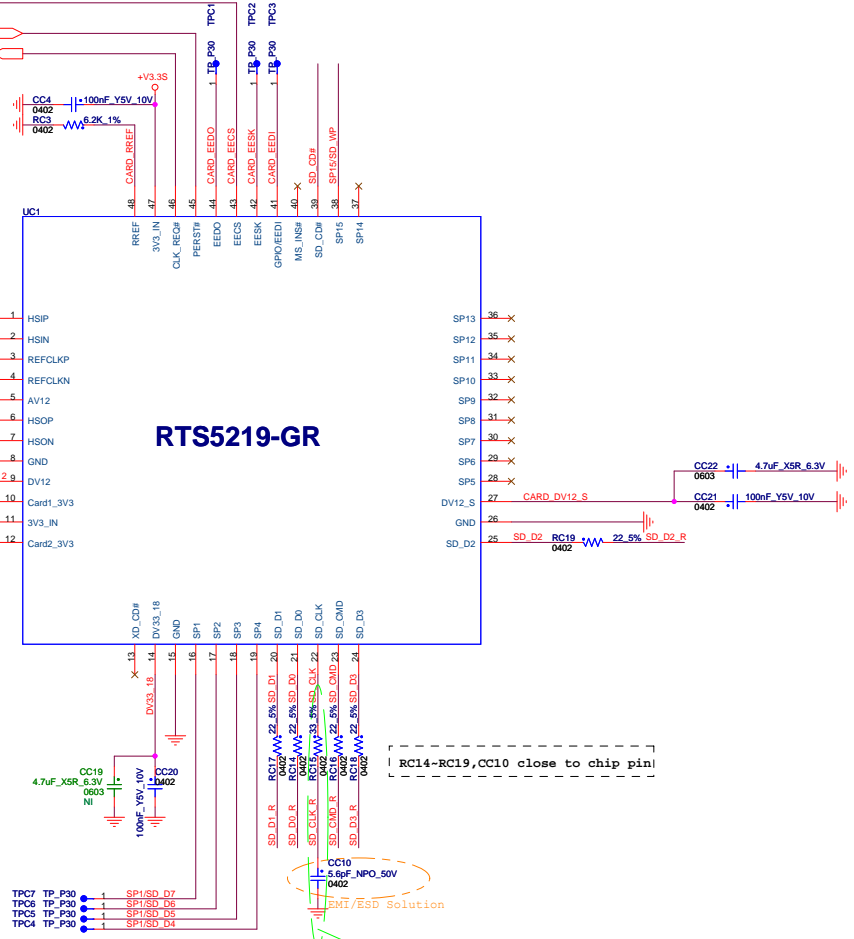
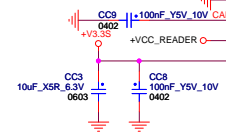
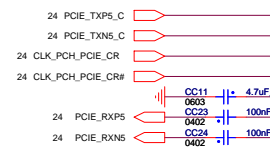
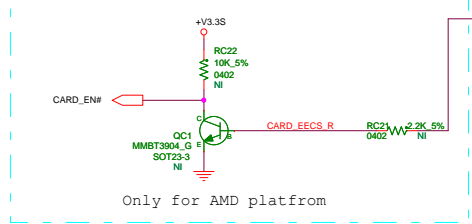
PWR Board CONN.



Half Mini Card for WLAN



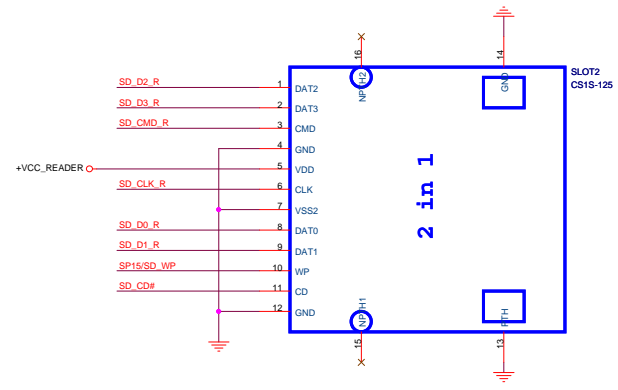
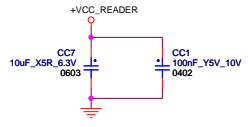


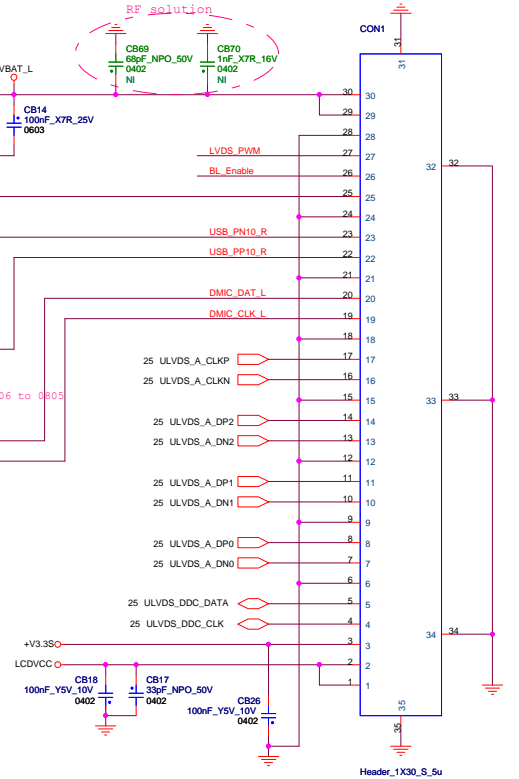
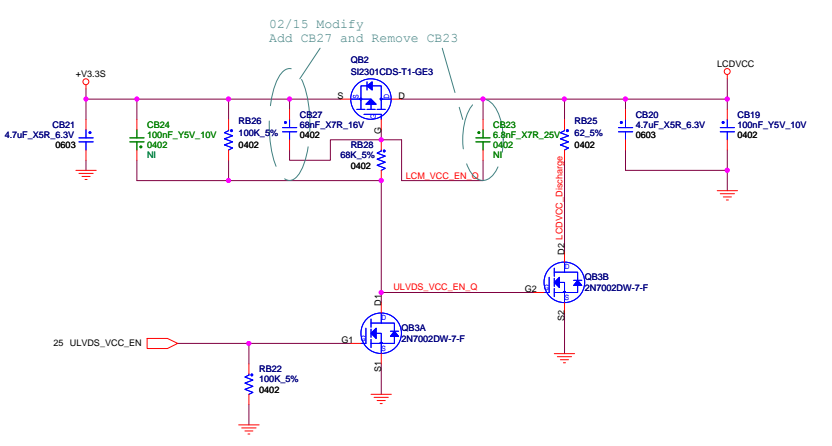
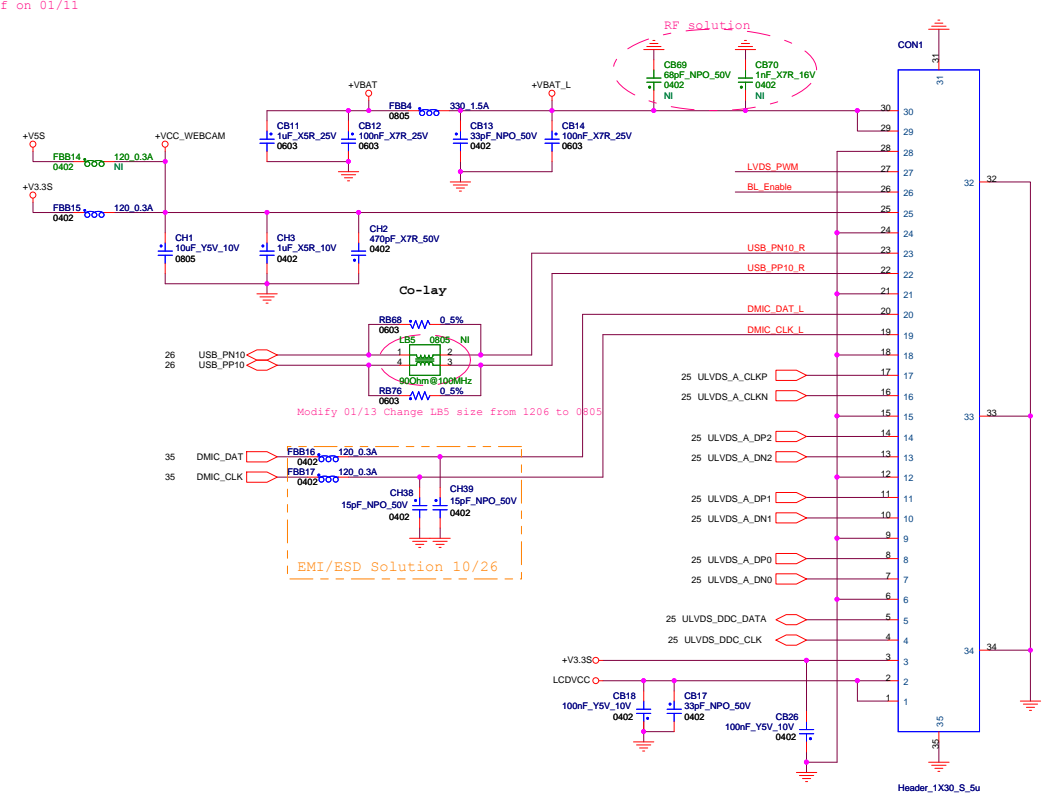
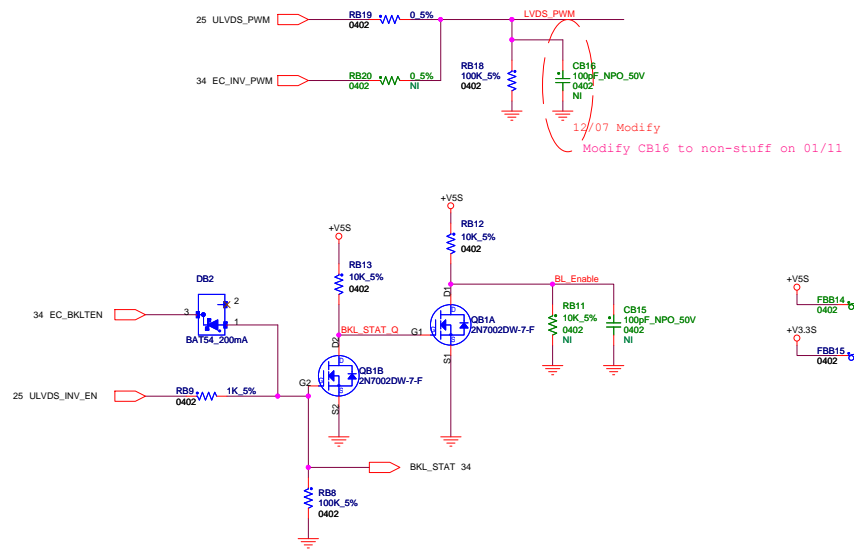


RC14-RC19, CC10 close to chip pin!

EMI/Esd Solution

1/24 Modify Check with EMI/ESDMax





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