

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page
01	Schematics Page Index
02	Block Diagram
03	Penryn(HOST BUS) 1/3
04	Penryn(HOST BUS) 2/3
05	Penryn (Power/Gnd) 3/3
06	CLOCK GEN
07	Cantiga (HOST) 1/7
08	Cantiga (DMI) 2/7
09	Cantiga (GRAPHIC) 3/7
10	Cantiga (DDR2) 4/7
11	Cantiga (POWER,VCC) 5/7
12	Cantiga (VCC CORE) 6/7
13	Cantiga (VSS) 7/7
14	DDR2(SO-DIMM_0) 1/3
15	DDR2(SO-DIMM_1) 2/3
16	DDR2(Termination) 3/3
17	VGA (PCI-E) 1/5
18	VGA (STRAP) 2/5
19	VGA (IO) 3/5
20	VGA (GDDR) 4/5
21	VGA (POWER) 5/5
22	VRAM (GDDR3) 1/2
23	VRAM (BYPASS) 2/2
24	CRT
25	LVDS
26	HDMI
27	ICH9-M(PCI/USB) 1/5
28	ICH9-M(LPC,IDE,SATA)2/5
29	ICH9-M(GPIO) 3/5
30	ICH9-M(POWER) 4/5
31	ICH9-M(GND) 5/5
32	SATA HDD/ODD
33	EC+KBC(WPCE775L)
34	Flash ROM/SPI
35	EXPRESS CARD
36	Bluetooth&CAM&LID SW
37	DB connector & Docking

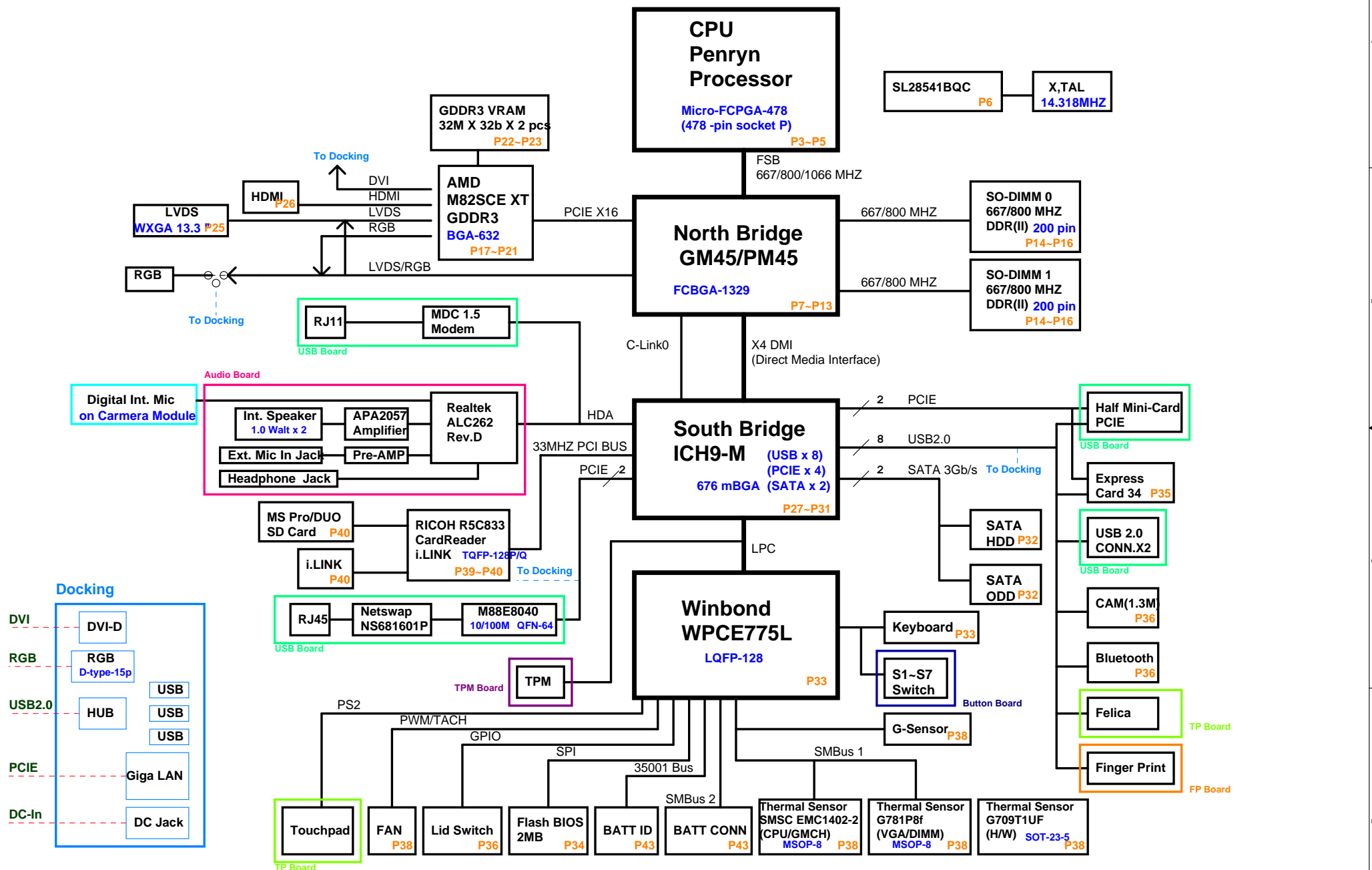
Page	Title of Schematics Page
38	FAN/Thermal & G-Sensor
39	PCI (PCI BUS)
40	PCI (ILINK&MS&SD)
41	LED & WLAN Switch
42	Power Design Diagram
43	DCIN&Charger
44	SYS Power (+3_3V/+5V)
45	SYS Power(+1_5V/+1_05V)
46	DDR2 Power(+1_8V/+0_9V)
47	CPU_Vcore---ISL6262A
48	Others power plane
49	OVP protection
50	VGA Power(ATI_M82 XT-S)
51	LED Backlight Power
52	HOLE
53	CHANGELIST

BOM Control Table						
Value Prefix	CA_	AT_	DS_	ND_	LND_	HD_
UMA (W/ Dock)	v		v			
UMA (W/O Dock)	v			v	v	
M82 (W/ Dock)		v	v			
M82 (W/O Dock HDMI)		v		v		
M82 (w/dock W/ HDMI)		v	v			v

Project Code & Schematics Subject: M750 Main Board PCB P/N:

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Index Page			
Size	Document Number	Rev	
Custom	M750-1-01	1.0	
Date:	Monday, June 23, 2008	Sheet	1 of 54

M750 (Montevina + M82SCE XT)



7 H_AA#[3..35]

7 H_ADSTB#0

7 H_REQ#[4..0]

7 H_ADSTB#1

28 H_A20M#

28 H_FERR#

28 H_IGNNE#

28 H_STPCLK#

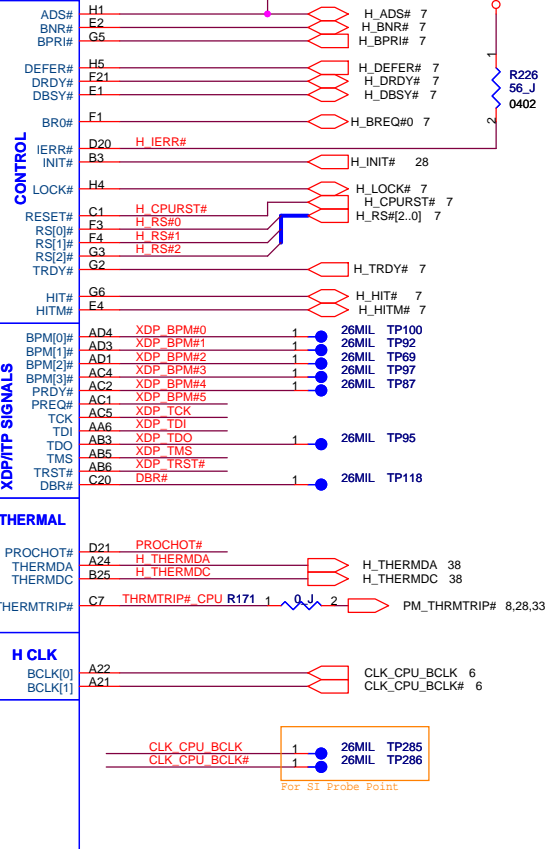
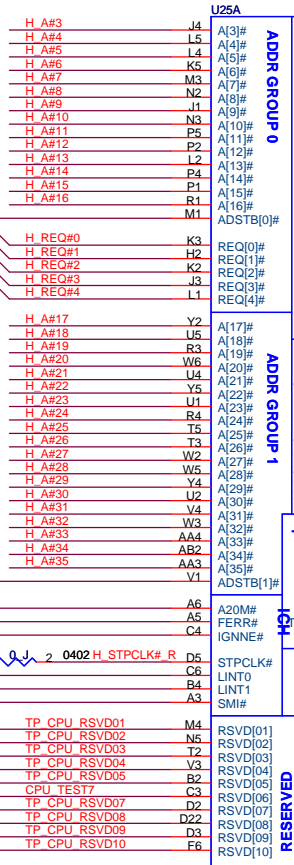
28 H_INTR

28 H_NMI

28 H_SMI#

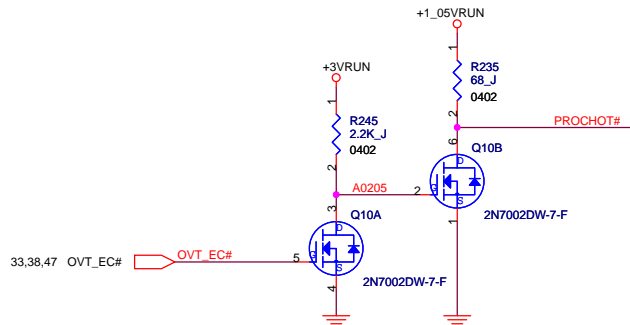
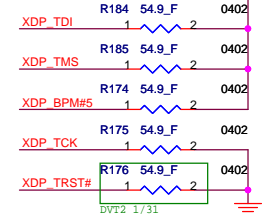
- TP98 26MIL 1 TP CPU RSVD01 M4
- TP102 26MIL 1 TP CPU RSVD02 N5
- TP86 26MIL 1 TP CPU RSVD03 T2
- TP99 26MIL 1 TP CPU RSVD04 V3
- TP78 26MIL 1 TP CPU RSVD05 B2
- TP91 26MIL 1 CPU TEST7 C3
- TP94 26MIL 1 TP CPU RSVD07 D2
- TP121 26MIL 1 TP CPU RSVD08 D22
- TP93 26MIL 1 TP CPU RSVD09 D3
- TP105 26MIL 1 TP CPU RSVD10 F6

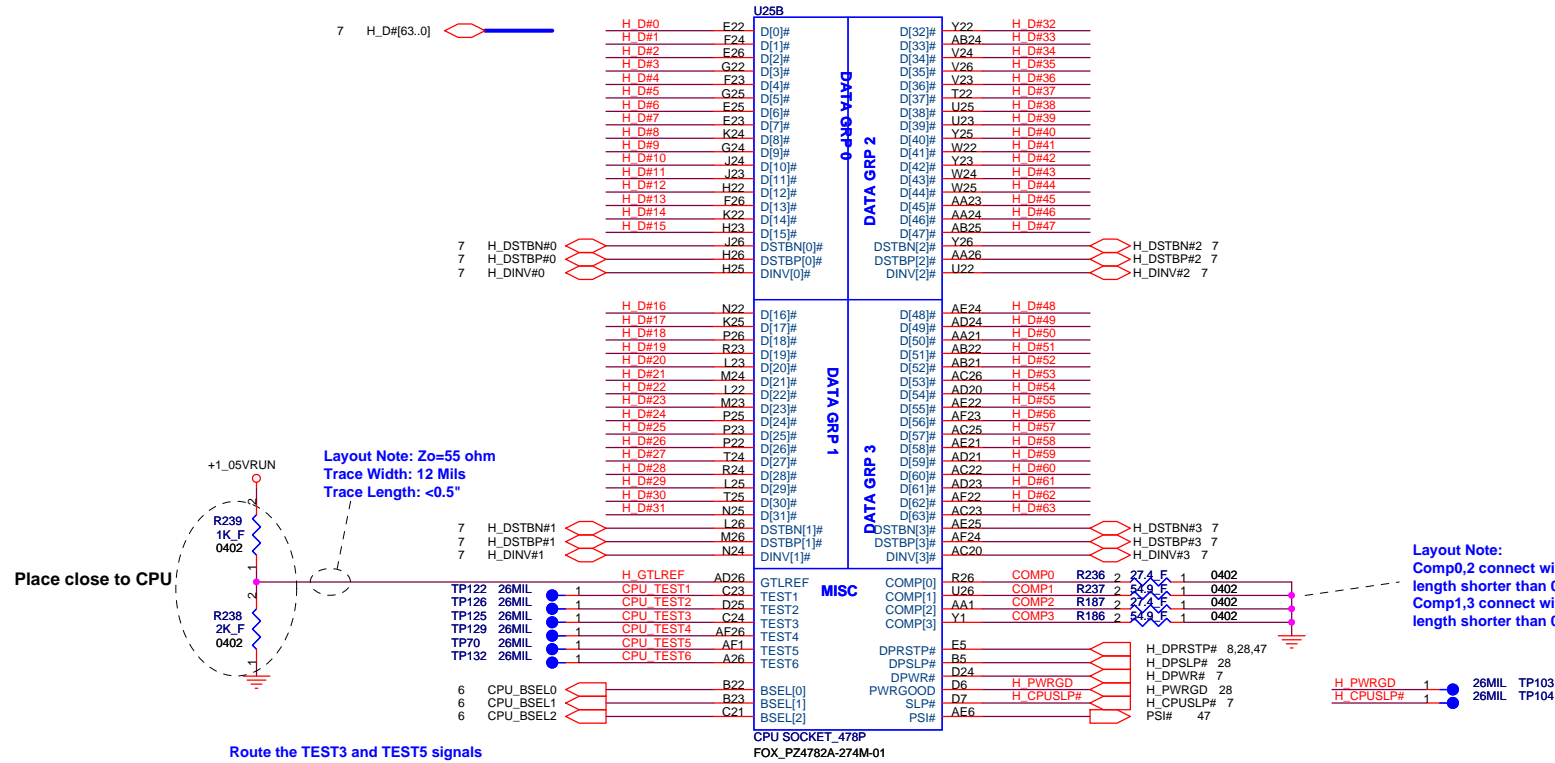
CPU SOCKET_478P
FOX_P24782A-274M-01



H_CPURST# 1 26MIL TP85

+1_05VRUN

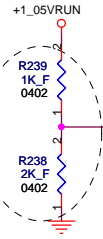




7 H_D#[63..0]

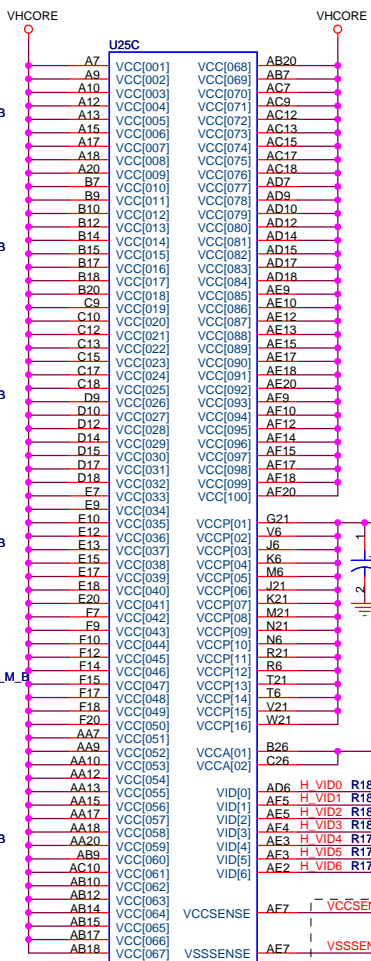
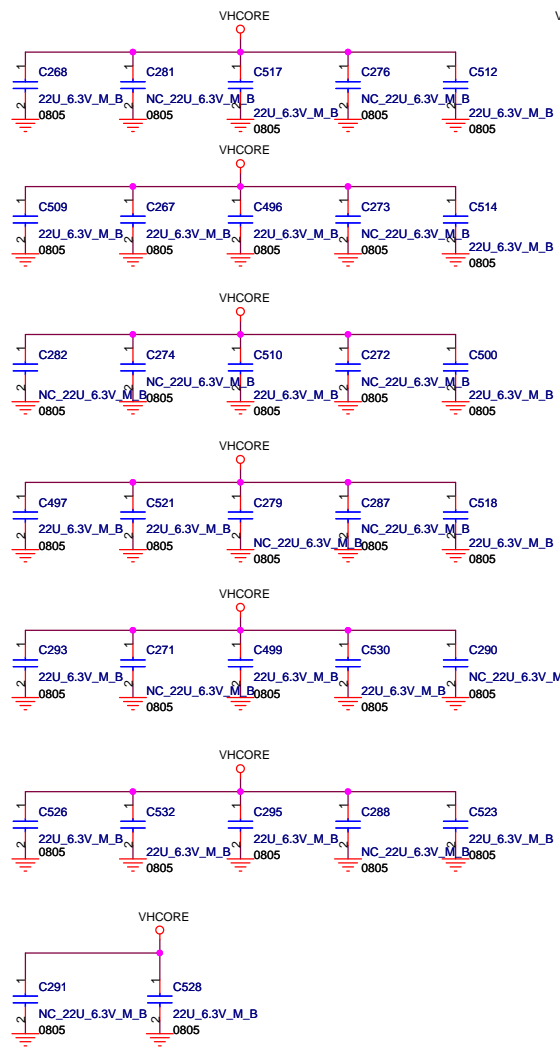
Layout Note: Zo=55 ohm
Trace Width: 12 Mils
Trace Length: <0.5"

Place close to CPU

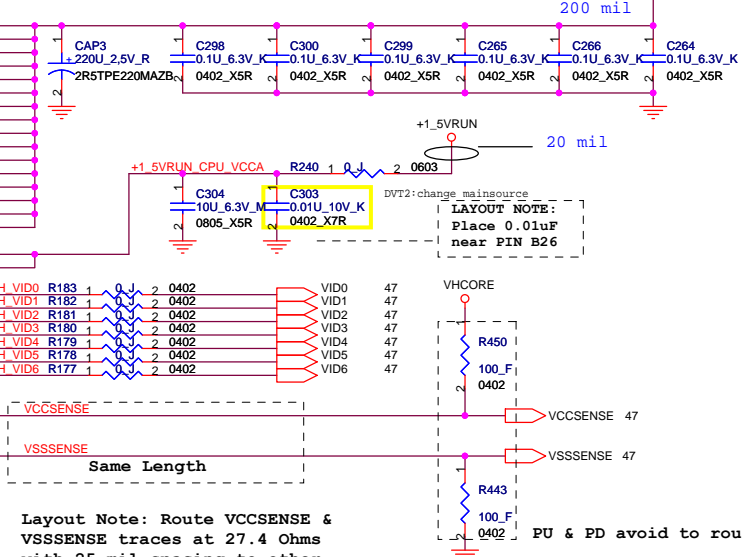


Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Width=13mil (MS)
Comp1,3 connect with Zo=55 ohm, make trace length shorter than 0.5". Width=4mil

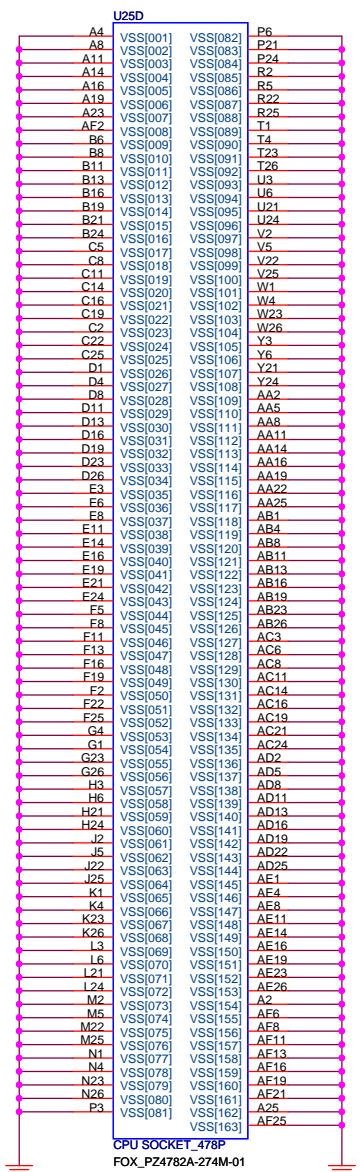


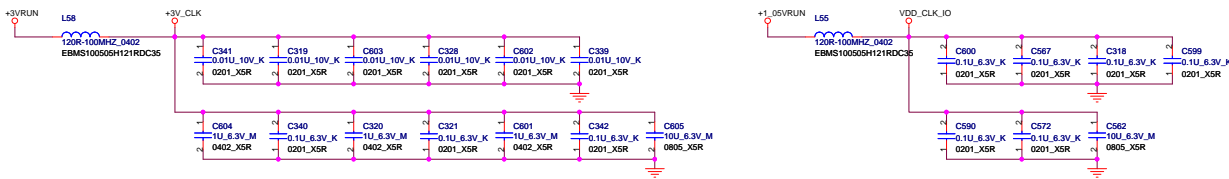
CPU_VCCA---->0.13A
 CPU_VCCP---->2.5A
 CPU_VCC---->47A



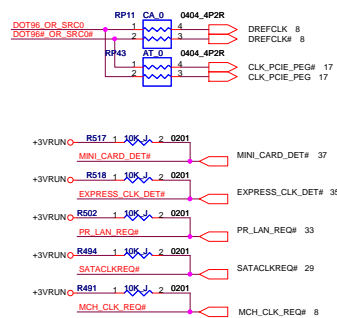
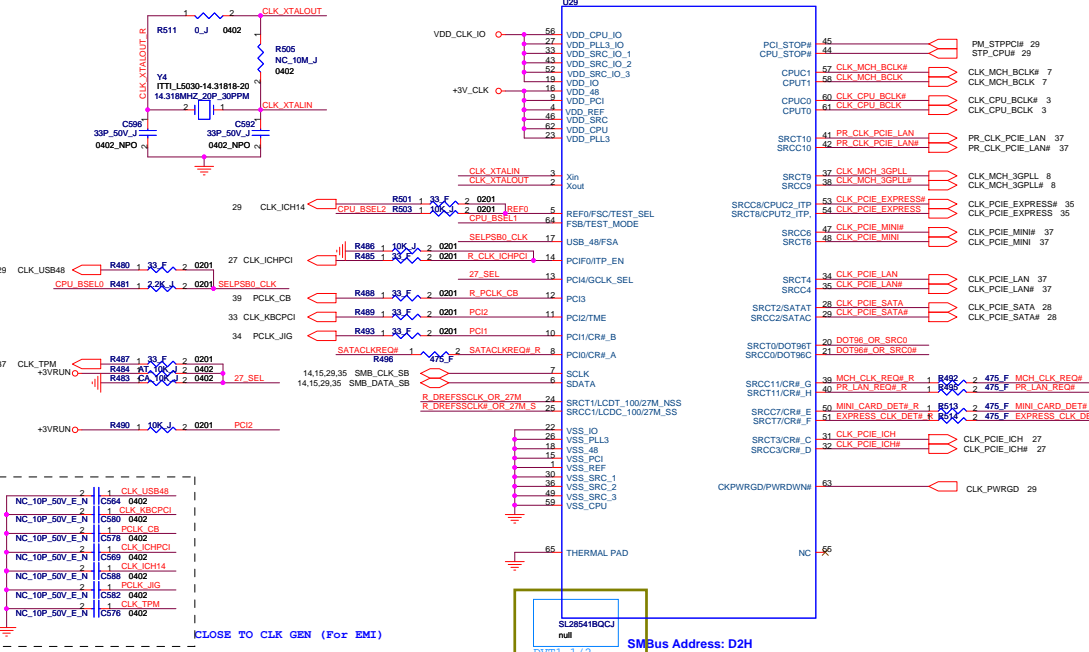
Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.
 Outer width=13 mil spacing=7 mil
 Inner width=13 mil spacing=7 mil
 Length match < 25 mil

PU & PD avoid to route with stub



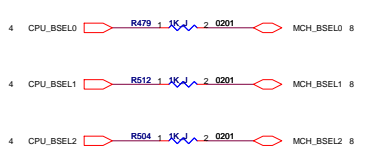


Clock Request	Clock Request Function
CR#A	SRC0, 2
CR#B	SRC1, 4
CR#C	SRC0, 2
CR#D	SRC1, 4
CR#E	SRC6
CR#F	SRC8
CR#G	SRC9
CR#H	SRC10



FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

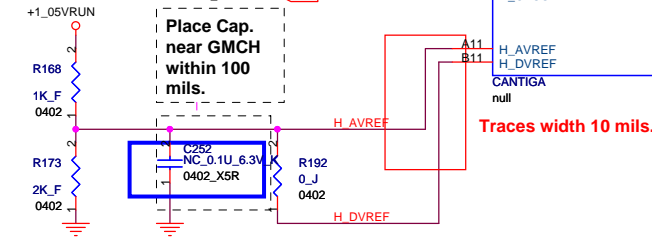
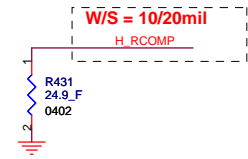
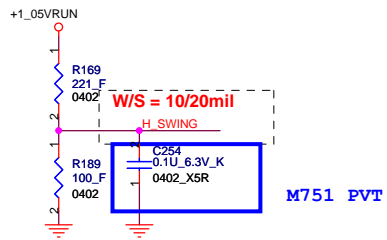
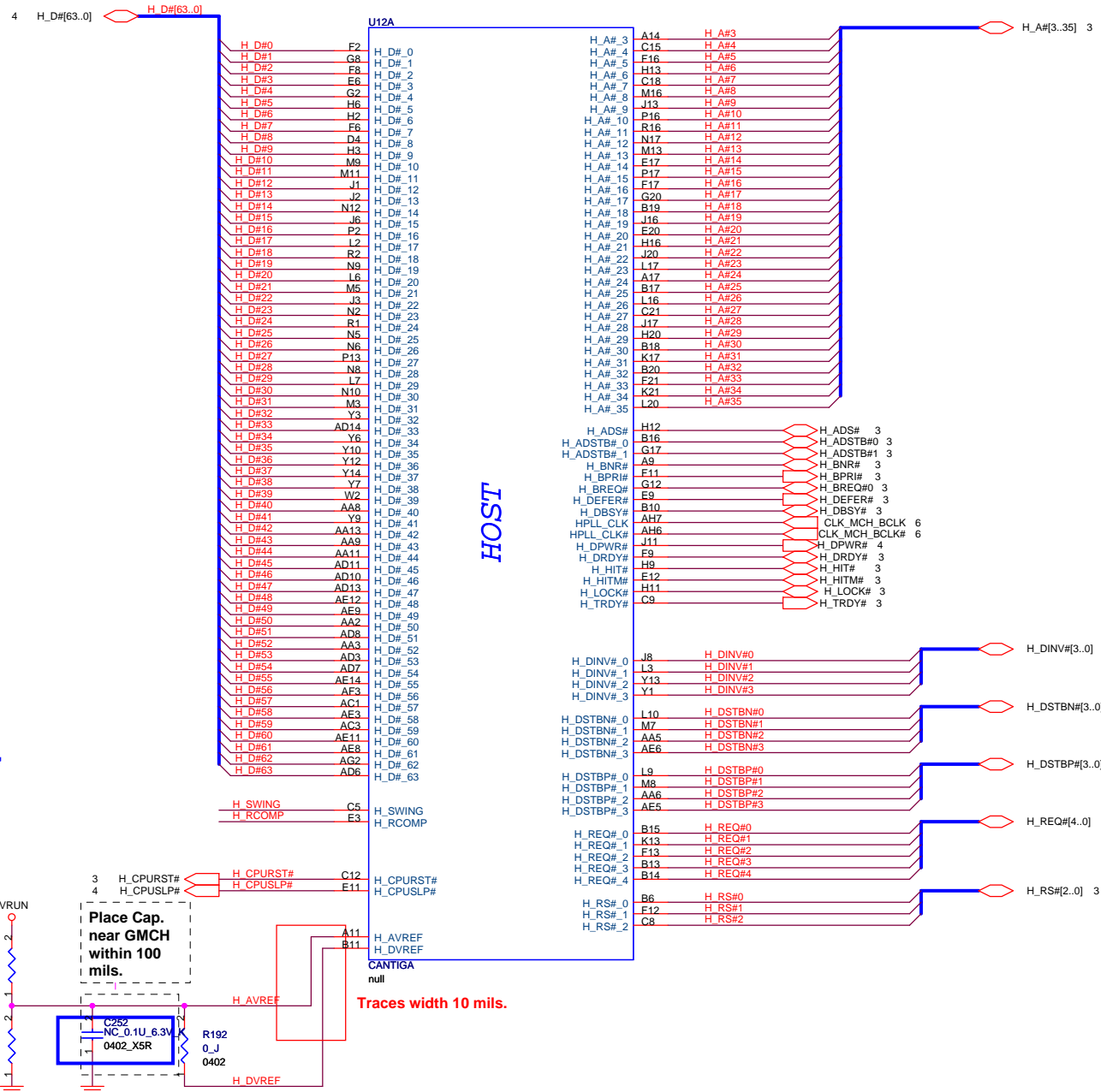


SMbus Address: D2H
DVT Update footprint for Japan/Mitsui package

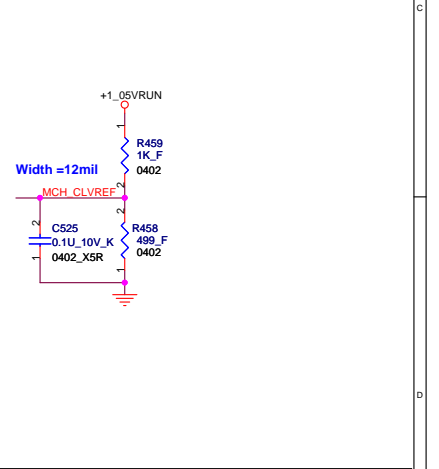
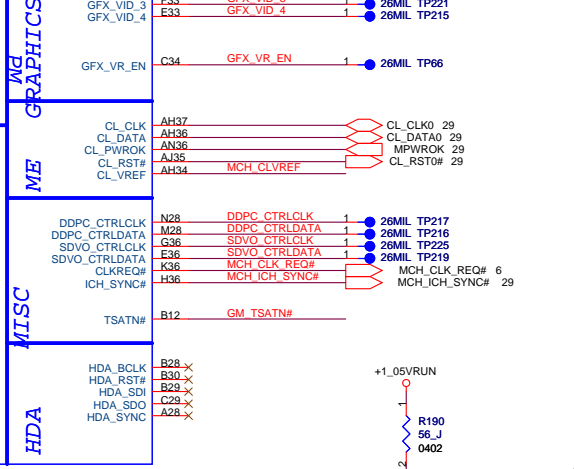
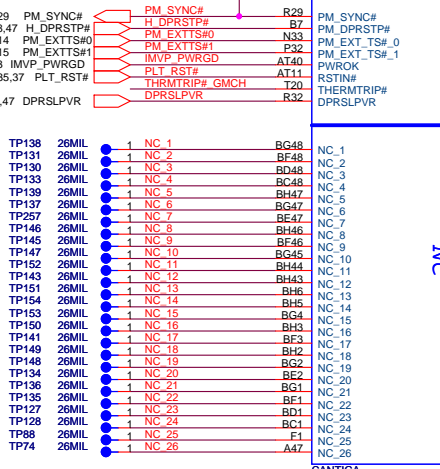
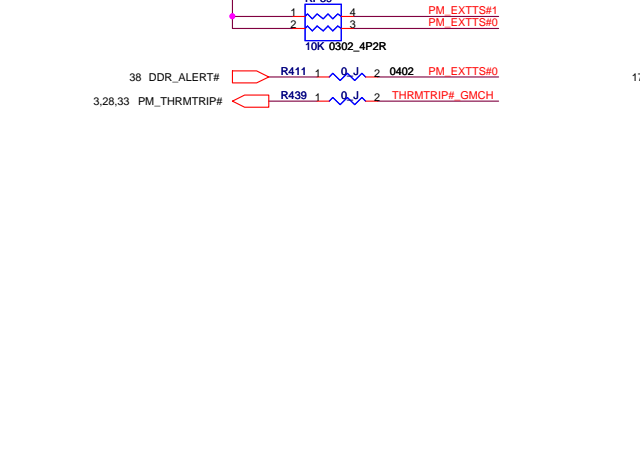
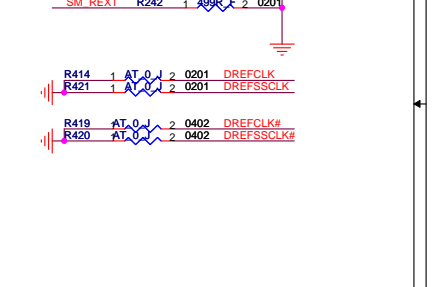
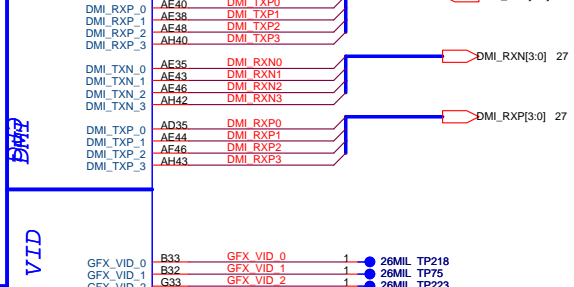
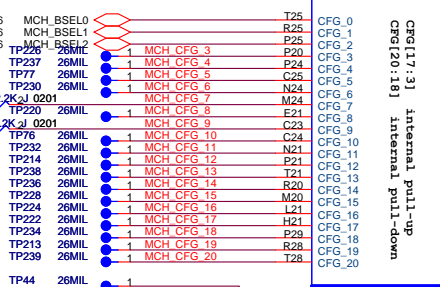
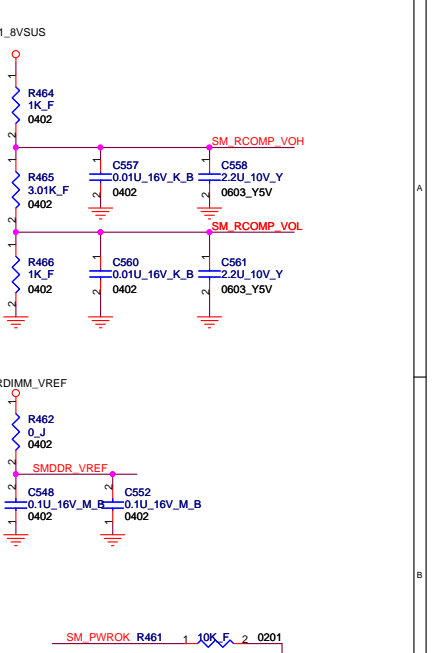
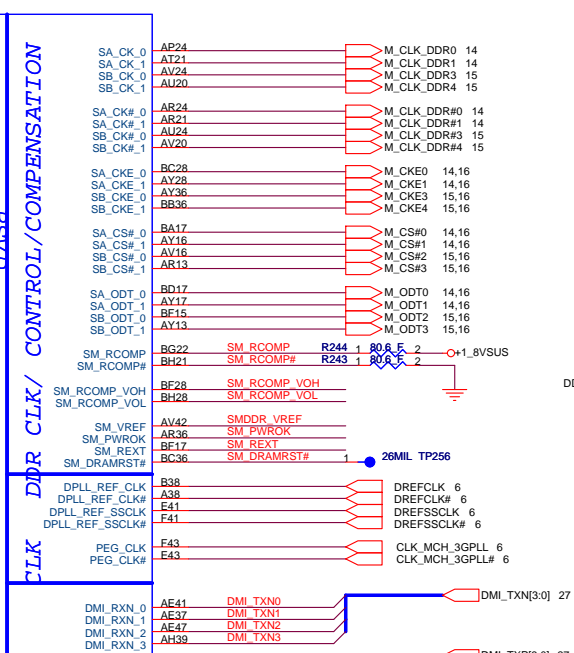
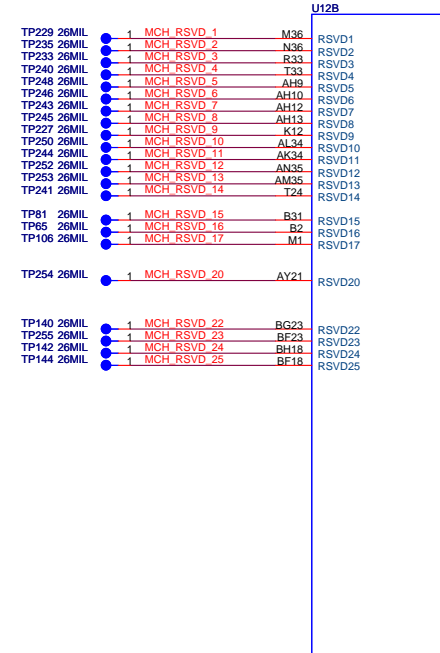
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

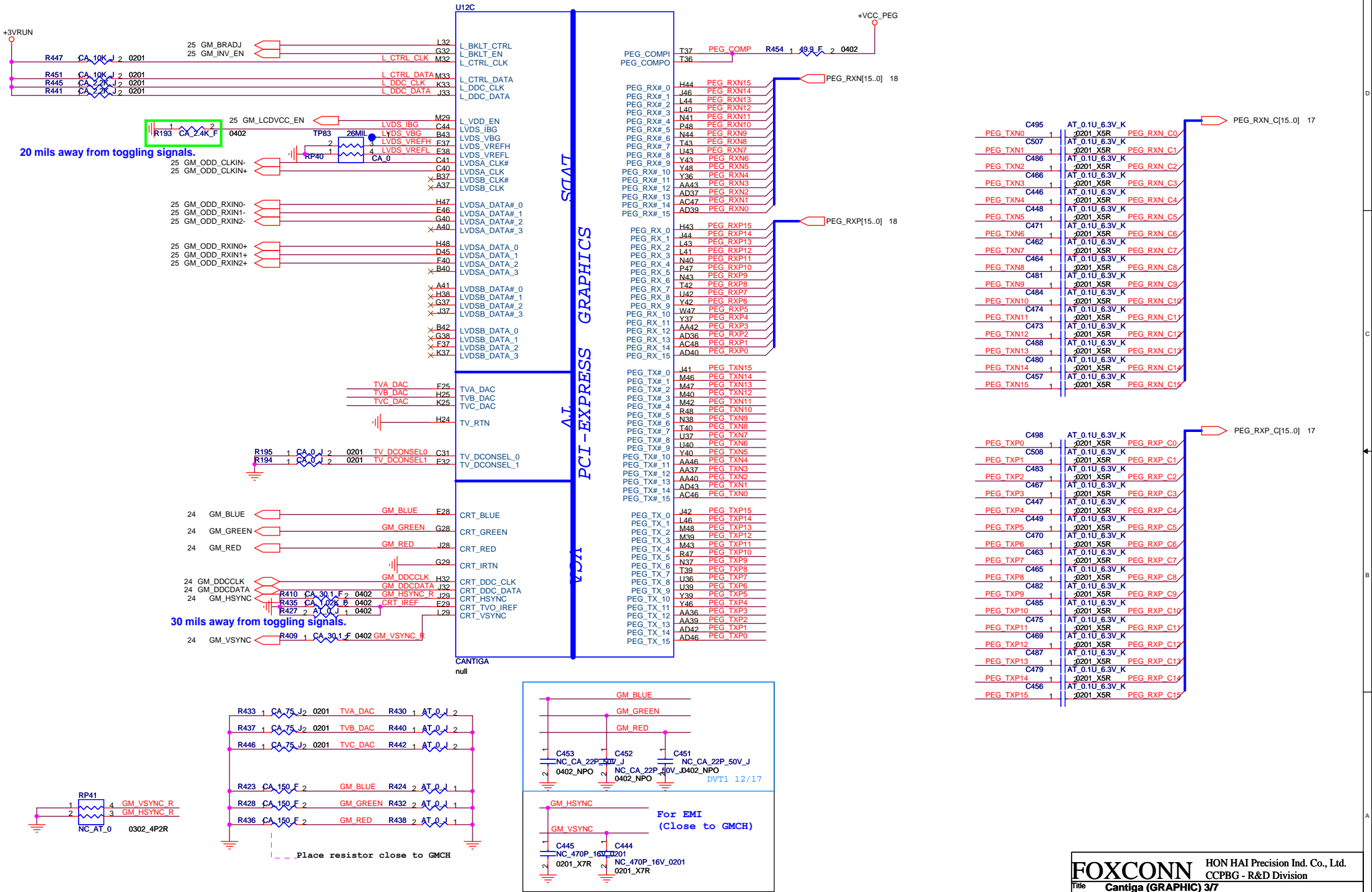
CLOCK GEN

File	Document Number	Rev
A2	M750-1-01	1.0
Date:	Monday, June 23, 2008	Sheet 6 of 54



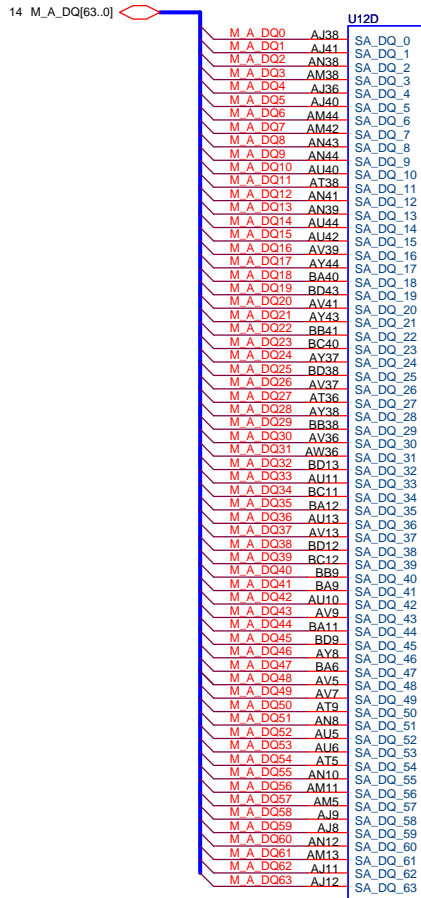
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800 ; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Lane Reversed High = Normal operation
MCH_CFG_10 PCIe Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default). High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



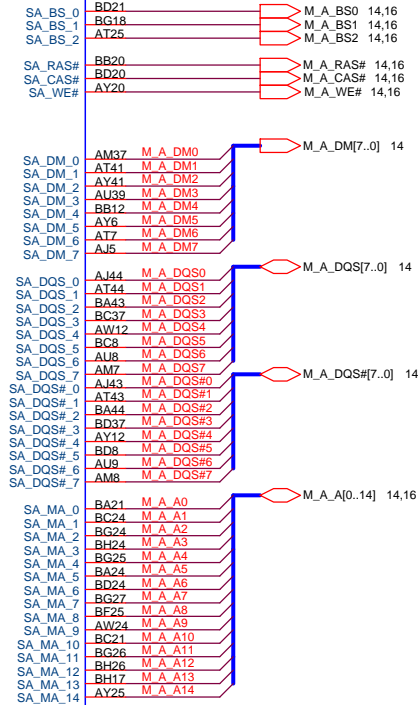


PEG_TXN0	C495	AT_0.1U_6.3V_K	PEG_RXN_C0	PEG_RXN_C[15..0]	17
PEG_TXN1	C507	AT_0.1U_6.3V_K	PEG_RXN_C1		
PEG_TXN2	C486	AT_0.1U_6.3V_K	PEG_RXN_C2		
PEG_TXN3	C466	AT_0.1U_6.3V_K	PEG_RXN_C3		
PEG_TXN4	C446	AT_0.1U_6.3V_K	PEG_RXN_C4		
PEG_TXN5	C448	AT_0.1U_6.3V_K	PEG_RXN_C5		
PEG_TXN6	C471	AT_0.1U_6.3V_K	PEG_RXN_C6		
PEG_TXN7	C462	AT_0.1U_6.3V_K	PEG_RXN_C7		
PEG_TXN8	C464	AT_0.1U_6.3V_K	PEG_RXN_C8		
PEG_TXN9	C481	AT_0.1U_6.3V_K	PEG_RXN_C9		
PEG_TXN10	C484	AT_0.1U_6.3V_K	PEG_RXN_C10		
PEG_TXN11	C474	AT_0.1U_6.3V_K	PEG_RXN_C11		
PEG_TXN12	C473	AT_0.1U_6.3V_K	PEG_RXN_C12		
PEG_TXN13	C488	AT_0.1U_6.3V_K	PEG_RXN_C13		
PEG_TXN14	C480	AT_0.1U_6.3V_K	PEG_RXN_C14		
PEG_TXN15	C457	AT_0.1U_6.3V_K	PEG_RXN_C15		

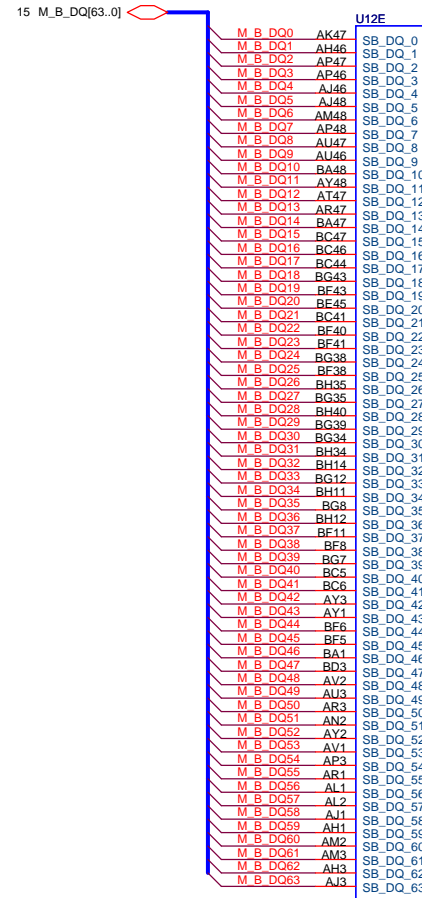
PEG_RXP0	C498	AT_0.1U_6.3V_K	PEG_RXP_C0	PEG_RXP_C[15..0]	17
PEG_RXP1	C508	AT_0.1U_6.3V_K	PEG_RXP_C1		
PEG_RXP2	C483	AT_0.1U_6.3V_K	PEG_RXP_C2		
PEG_RXP3	C467	AT_0.1U_6.3V_K	PEG_RXP_C3		
PEG_RXP4	C447	AT_0.1U_6.3V_K	PEG_RXP_C4		
PEG_RXP5	C449	AT_0.1U_6.3V_K	PEG_RXP_C5		
PEG_RXP6	C470	AT_0.1U_6.3V_K	PEG_RXP_C6		
PEG_RXP7	C463	AT_0.1U_6.3V_K	PEG_RXP_C7		
PEG_RXP8	C465	AT_0.1U_6.3V_K	PEG_RXP_C8		
PEG_RXP9	C482	AT_0.1U_6.3V_K	PEG_RXP_C9		
PEG_RXP10	C485	AT_0.1U_6.3V_K	PEG_RXP_C10		
PEG_RXP11	C475	AT_0.1U_6.3V_K	PEG_RXP_C11		
PEG_RXP12	C469	AT_0.1U_6.3V_K	PEG_RXP_C12		
PEG_RXP13	C487	AT_0.1U_6.3V_K	PEG_RXP_C13		
PEG_RXP14	C479	AT_0.1U_6.3V_K	PEG_RXP_C14		
PEG_RXP15	C456	AT_0.1U_6.3V_K	PEG_RXP_C15		



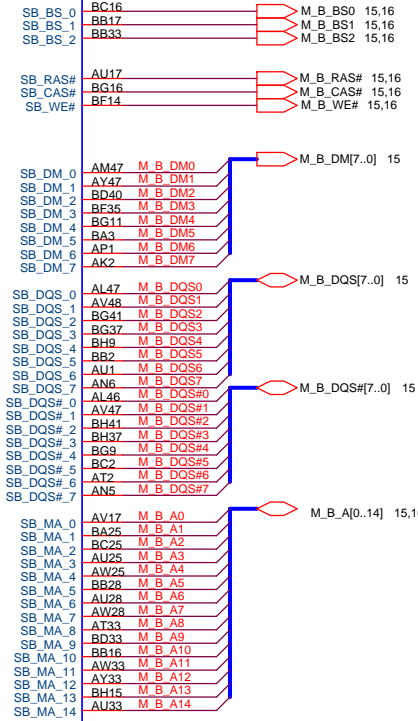
DDR SYSTEM MEMORY A



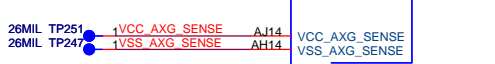
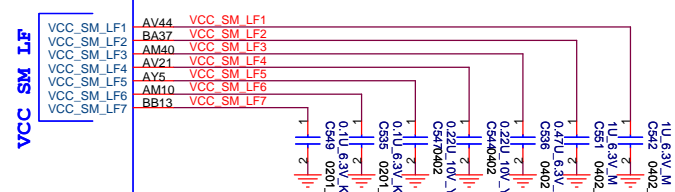
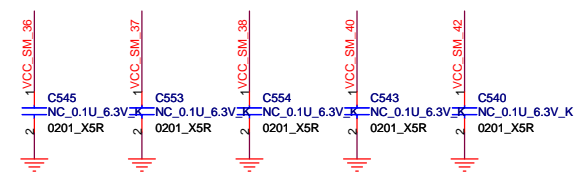
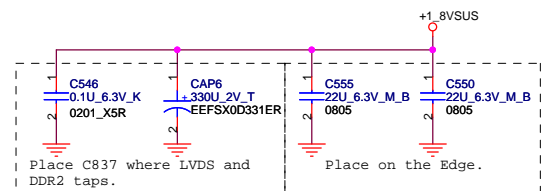
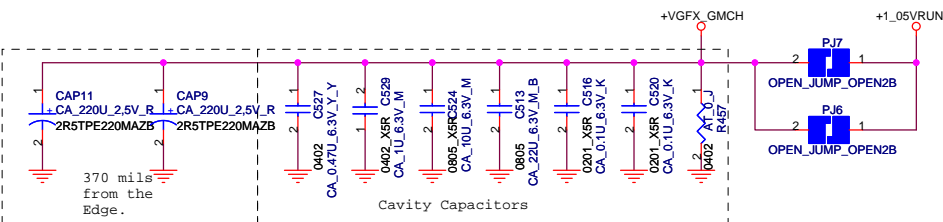
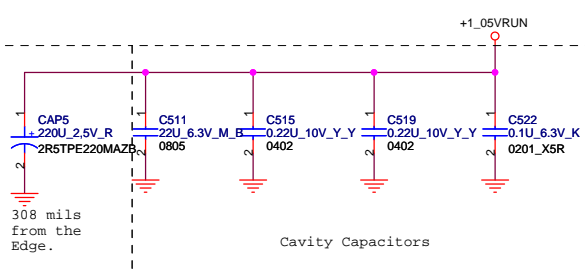
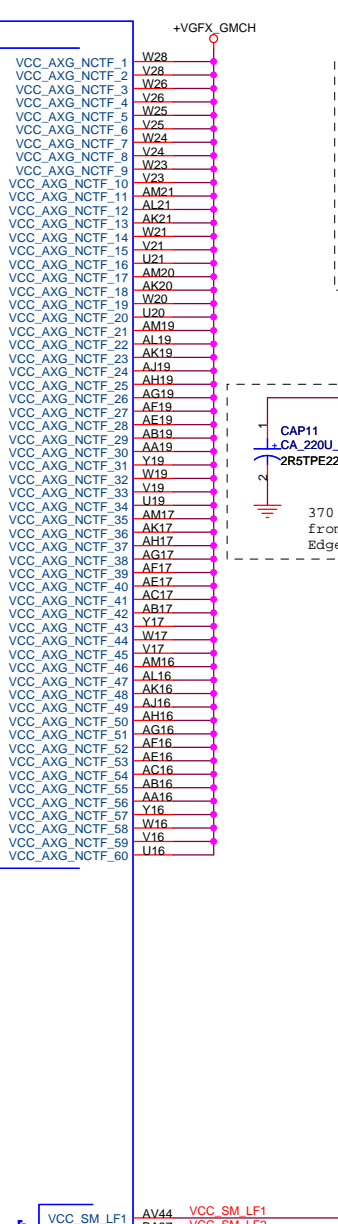
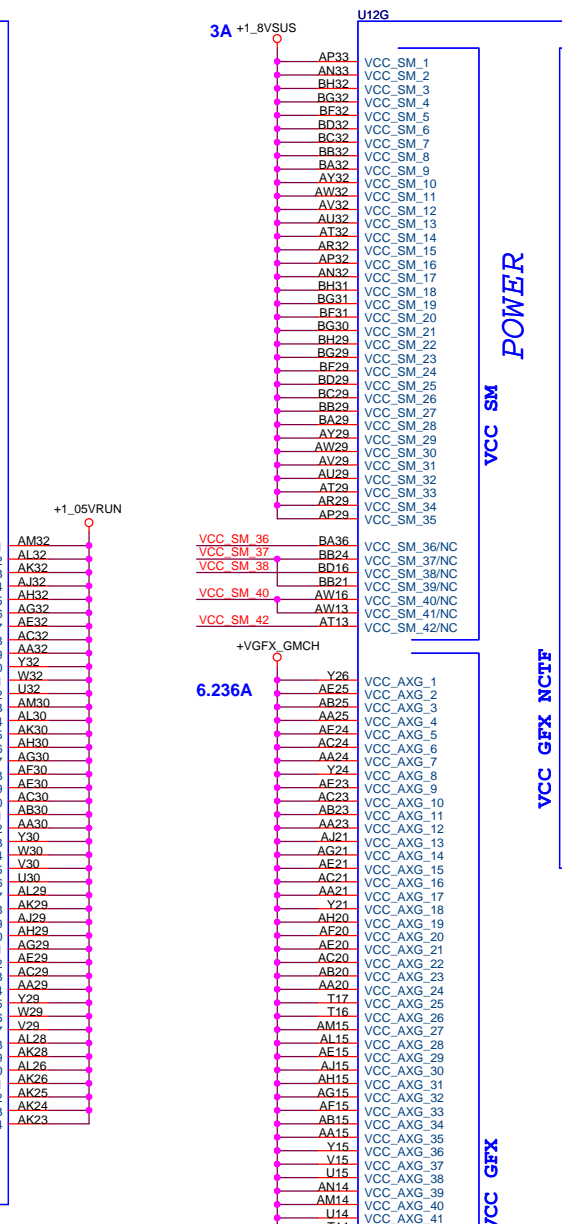
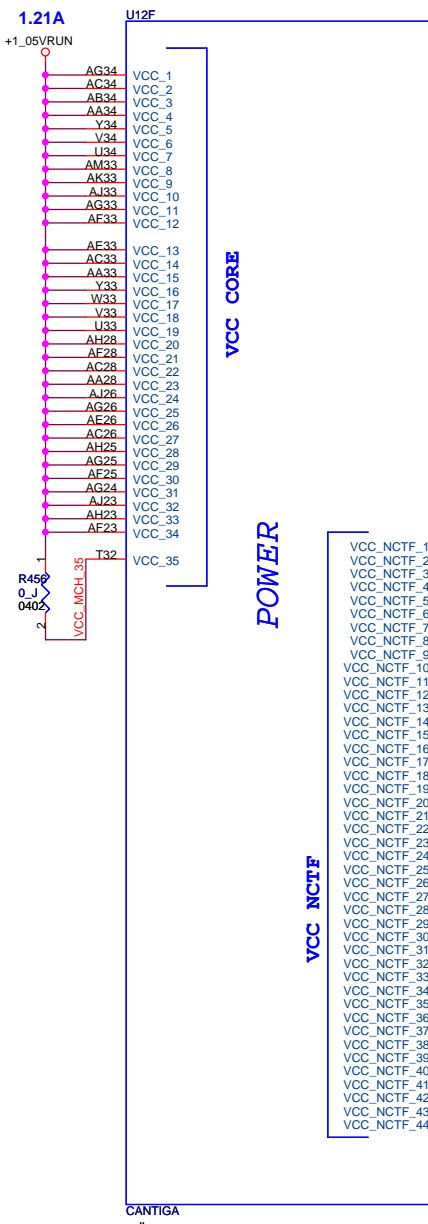
CANTIGA
null



DDR SYSTEM MEMORY B



CANTIGA
null



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **Cantiga (VCC CORE) 6/7**

Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 12	of 54

U121		VSS	
ALJ48	VSS_1	VSS_100	AM36
AR48	VSS_2	VSS_101	AE36
AL48	VSS_3	VSS_102	P36
BB47	VSS_4	VSS_103	L36
AW47	VSS_5	VSS_104	J36
AM47	VSS_6	VSS_105	E36
AF47	VSS_7	VSS_106	AF21
AD47	VSS_8	VSS_107	AH35
AB47	VSS_9	VSS_108	AA35
Y47	VSS_10	VSS_109	Y35
T47	VSS_11	VSS_110	J21
N47	VSS_12	VSS_111	T35
L47	VSS_13	VSS_112	BF34
G47	VSS_14	VSS_113	AM34
BD46	VSS_15	VSS_114	AJ34
BA46	VSS_16	VSS_115	AF34
AY46	VSS_17	VSS_116	AE34
AV46	VSS_18	VSS_117	W34
AR46	VSS_19	VSS_118	Y20
AM46	VSS_20	VSS_119	B34
V46	VSS_21	VSS_120	A34
R46	VSS_22	VSS_121	BG33
P46	VSS_23	VSS_122	BC33
H46	VSS_24	VSS_123	BA33
F46	VSS_25	VSS_124	AV33
BF44	VSS_26	VSS_125	AR33
AH44	VSS_27	VSS_126	AL33
AD44	VSS_28	VSS_127	AH33
AA44	VSS_29	VSS_128	AB33
Y44	VSS_30	VSS_129	P33
U44	VSS_31	VSS_130	L33
T44	VSS_32	VSS_131	H33
M44	VSS_33	VSS_132	N32
F44	VSS_34	VSS_133	M17
BC43	VSS_35	VSS_134	K32
AV43	VSS_36	VSS_135	F32
AU43	VSS_37	VSS_136	C32
AM43	VSS_38	VSS_137	A31
J43	VSS_39	VSS_138	AN29
C43	VSS_40	VSS_139	T29
BG42	VSS_41	VSS_140	N29
AY42	VSS_42	VSS_141	K29
AT42	VSS_43	VSS_142	H29
AN42	VSS_44	VSS_143	F29
AJ42	VSS_45	VSS_144	G16
AE42	VSS_46	VSS_145	E16
N42	VSS_47	VSS_146	BG28
L42	VSS_48	VSS_147	BD28
BD41	VSS_49	VSS_148	BA28
AU41	VSS_50	VSS_149	AV28
AM41	VSS_51	VSS_150	AT28
AH41	VSS_52	VSS_151	AR28
AD41	VSS_53	VSS_152	AJ28
AA41	VSS_54	VSS_153	AG28
Y41	VSS_55	VSS_154	AE28
U41	VSS_56	VSS_155	AB28
T41	VSS_57	VSS_156	Y28
M41	VSS_58	VSS_157	P28
G41	VSS_59	VSS_158	K28
B41	VSS_60	VSS_159	H28
BG40	VSS_61	VSS_160	F28
BB40	VSS_62	VSS_161	C28
AV40	VSS_63	VSS_162	N13
AM40	VSS_64	VSS_163	L13
H40	VSS_65	VSS_164	G13
E40	VSS_66	VSS_165	E13
AT39	VSS_67	VSS_166	BF26
AM39	VSS_68	VSS_167	AH26
AJ39	VSS_69	VSS_168	AF26
AE39	VSS_70	VSS_169	AB26
N39	VSS_71	VSS_170	AA26
L39	VSS_72	VSS_171	C26
B39	VSS_73	VSS_172	B26
BH38	VSS_74	VSS_173	BH25
BC38	VSS_75	VSS_174	BD25
BA38	VSS_76	VSS_175	BB25
AU38	VSS_77	VSS_176	AV25
AH38	VSS_78	VSS_177	AR25
AD38	VSS_79	VSS_178	AJ25
AA38	VSS_80	VSS_179	AG25
Y38	VSS_81	VSS_180	AE25
U38	VSS_82	VSS_181	AB25
T38	VSS_83	VSS_182	Y25
J38	VSS_84	VSS_183	N25
F38	VSS_85	VSS_184	L25
C38	VSS_86	VSS_185	J25
BF37	VSS_87	VSS_186	G25
BB37	VSS_88	VSS_187	E25
AW37	VSS_89	VSS_188	BF24
AT37	VSS_90	VSS_189	AD12
AN37	VSS_91	VSS_190	AY24
AJ37	VSS_92	VSS_191	AT24
H37	VSS_93	VSS_192	AJ24
G37	VSS_94	VSS_193	AE10
CG36	VSS_95	VSS_194	AA10
BD36	VSS_96	VSS_195	M10
AK15	VSS_97	VSS_196	BF9
AU36	VSS_98	VSS_197	BC9
	VSS_99	VSS_198	AN9
		VSS_199	AM9
			J24
			G24
			B9
			BH8
			BB8
			AV8
			AT8
			AJ6

CANTIGA null

U12J		VSS	
BG21	VSS_199	VSS_297	AH8
L12	VSS_200	VSS_298	Y8
AW21	VSS_201	VSS_299	L8
AU21	VSS_202	VSS_300	E8
AP21	VSS_203	VSS_301	B8
AN21	VSS_204	VSS_302	AY7
AH21	VSS_205	VSS_303	AU7
AE21	VSS_206	VSS_304	AN7
AB21	VSS_207	VSS_305	AJ7
R21	VSS_208	VSS_306	AE7
M21	VSS_209	VSS_307	AA7
J21	VSS_210	VSS_308	N7
G21	VSS_211	VSS_309	J7
BC20	VSS_212	VSS_310	BG6
BA20	VSS_213	VSS_311	BD6
AW20	VSS_214	VSS_312	AV6
AT20	VSS_215	VSS_313	AT6
AJ20	VSS_216	VSS_314	AM6
AG20	VSS_217	VSS_315	M6
W34	VSS_218	VSS_316	CG6
Y20	VSS_219	VSS_317	BA5
N20	VSS_220	VSS_318	AH5
K20	VSS_221	VSS_319	AD5
F20	VSS_222	VSS_320	Y5
C20	VSS_223	VSS_321	L5
A20	VSS_224	VSS_322	J5
BG19	VSS_225	VSS_323	H5
AL19	VSS_226	VSS_324	F5
BG17	VSS_227	VSS_325	BE4
BC17	VSS_228		
AW17	VSS_229	VSS_327	BC3
AT17	VSS_230	VSS_328	AV3
R17	VSS_231	VSS_329	AL3
M17	VSS_232	VSS_330	R3
K17	VSS_233	VSS_331	P3
C17		VSS_332	F3
		VSS_333	BA2
BA16	VSS_235	VSS_334	AW2
		VSS_335	AU2
ALJ16	VSS_237	VSS_336	AB2
AN16	VSS_238	VSS_337	AP2
N16	VSS_239	VSS_338	AJ2
K16	VSS_240	VSS_339	AH2
G16	VSS_241	VSS_340	AE2
E16	VSS_242	VSS_341	AE2
BG15	VSS_243	VSS_342	AD2
AC15	VSS_244	VSS_343	AC2
BA15	VSS_245	VSS_344	Y2
A15	VSS_246	VSS_345	M2
BG14	VSS_247	VSS_346	K2
AA14	VSS_248	VSS_347	AM1
C14	VSS_249	VSS_348	AA1
BG13	VSS_250	VSS_349	P1
BC13	VSS_251	VSS_350	H1
BA13	VSS_252		
		VSS_351	U24
AN13	VSS_255	VSS_352	U28
AJ13	VSS_256	VSS_353	U25
AE13	VSS_257	VSS_354	U29
C13	VSS_258		
N13	VSS_259		
L13	VSS_260		
G13	VSS_261		
E13	VSS_262		
BF12	VSS_263		
AV12	VSS_264		
C26	VSS_265		
AM12	VSS_266		
AA12	VSS_267		
J12	VSS_268		
A12	VSS_269		
BD11	VSS_270		
BB11	VSS_271		
AY11	VSS_272		
AN11	VSS_273		
AH11	VSS_274		
Y11	VSS_275		
N11	VSS_276		
G11	VSS_277		
E11	VSS_278		
BF10	VSS_279		
AV10	VSS_280		
AT10	VSS_281		
AJ10	VSS_282		
AE10	VSS_283		
AA10	VSS_284		
M10	VSS_285		
BF9	VSS_286		
BC9	VSS_287		
AN9	VSS_288		
AM9	VSS_289		
J24	VSS_290		
G24	VSS_291		
B9	VSS_292		
BH8	VSS_293		
BB8	VSS_294		
AV8	VSS_295		
AT8	VSS_296		

CANTIGA null

VSS

VSS NCTF

VSS SCB

NC

VSS_NCTF_1	AF32
VSS_NCTF_2	AB32
VSS_NCTF_3	V32
VSS_NCTF_4	AJ30
VSS_NCTF_5	AM29
VSS_NCTF_6	AB29
VSS_NCTF_7	U26
VSS_NCTF_8	U23
VSS_NCTF_9	AL20
VSS_NCTF_10	V20
VSS_NCTF_11	AC19
VSS_NCTF_12	AL17
VSS_NCTF_13	AJ17
VSS_NCTF_14	P1
VSS_NCTF_15	AA17
VSS_NCTF_16	U17

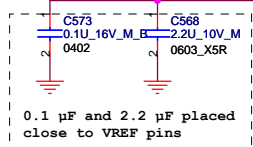
VSS_SCB_1	BH48
VSS_SCB_2	BH1
VSS_SCB_3	A48
VSS_SCB_4	C1
VSS_SCB_5	A3

E1	26MIL	TP89
D2	26MIL	TP63
C3	26MIL	TP64
B4	26MIL	TP62
A5	26MIL	TP61
A6	26MIL	TP60
A43	26MIL	TP73
A44	26MIL	TP71
B45	26MIL	TP84
C46	26MIL	TP82
D47	26MIL	TP90
B47	26MIL	TP79
A46	26MIL	TP88
F48	26MIL	TP101
E48	26MIL	TP96
C48	26MIL	TP67
B48	26MIL	TP80

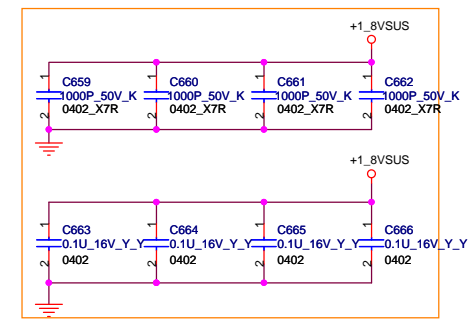
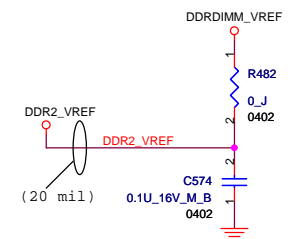
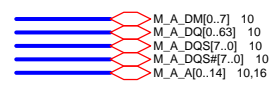
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **Cantiga (VSS) 777**

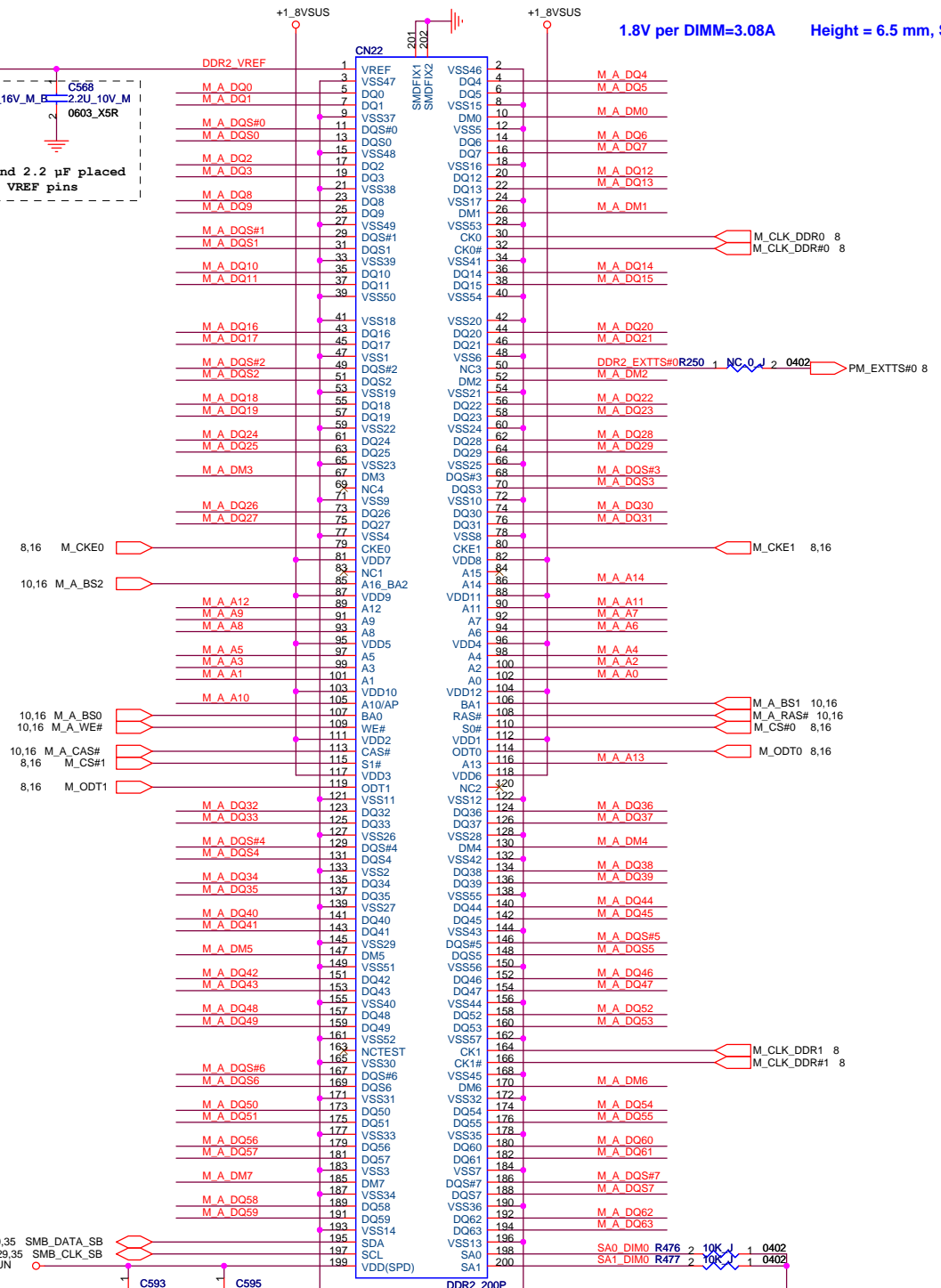
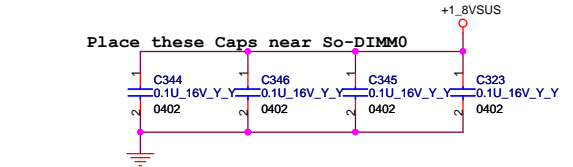
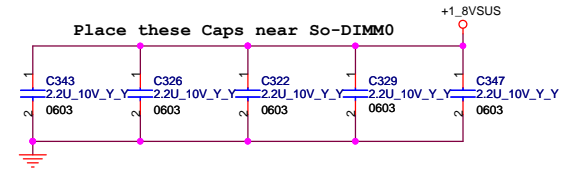
Size: A3	Document Number: M750-1-01	Rev: 1.0
Date: Monday, June 23, 2008	Sheet: 13	of 54



1.8V per DIMM=3.08A Height = 6.5 mm, Standard Type

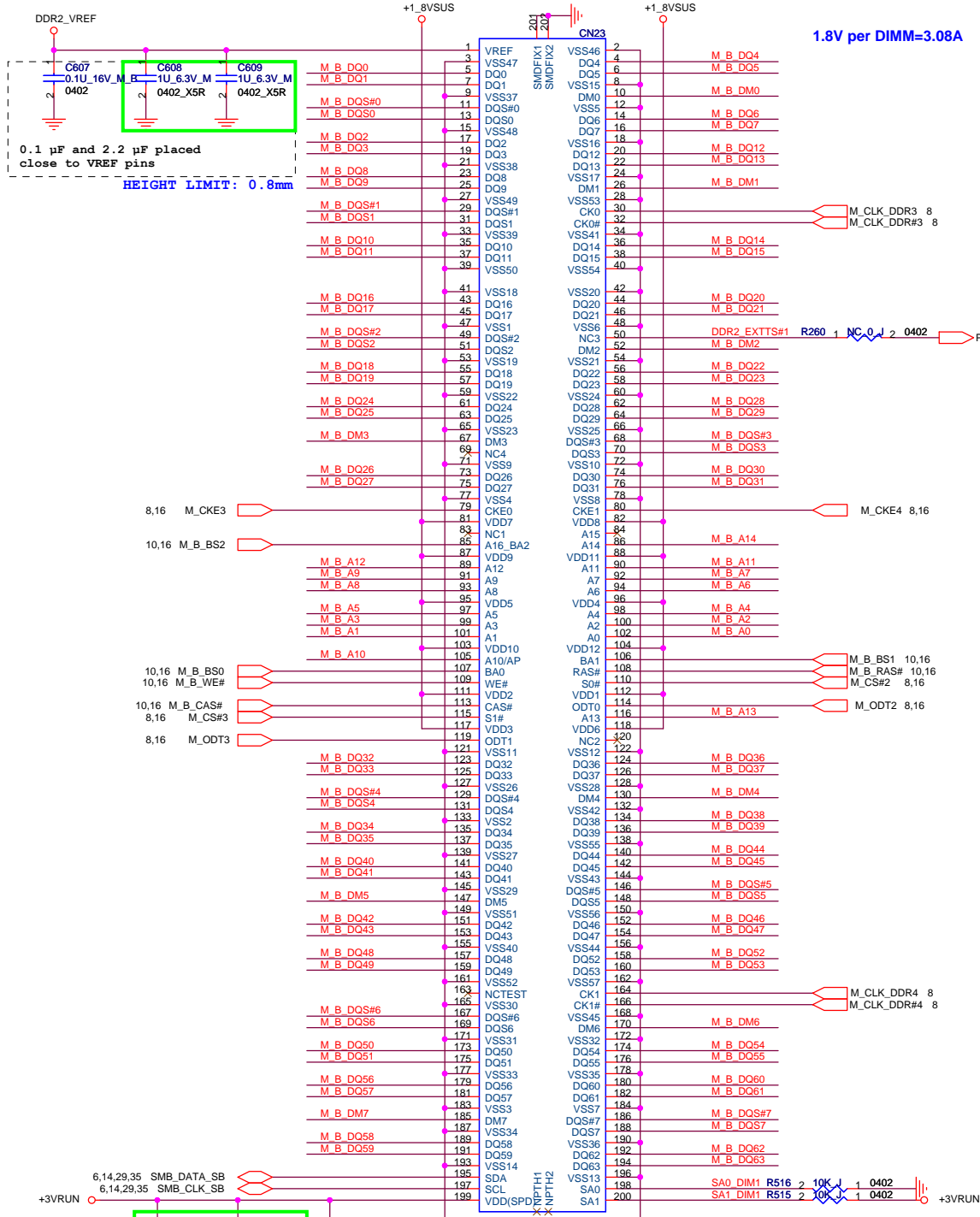


EVT2 11/09 Reserved For EMI. Place around +1.8VSUS plane.

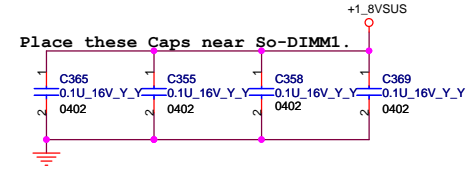
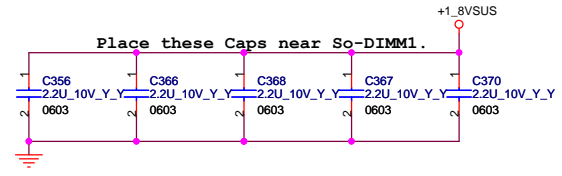
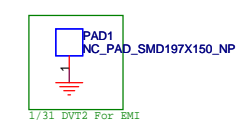
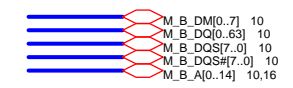


SMBus Address: A0H(W)/A1H(R)
Place DIMM_0 near GMCH

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title DDR(H)SO-DIMM_0		CCPBG - R&D Division	
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 14	of 54	

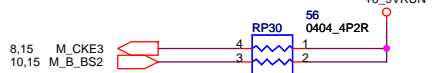
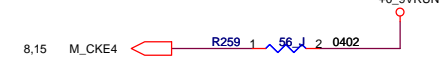
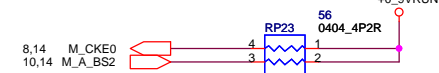
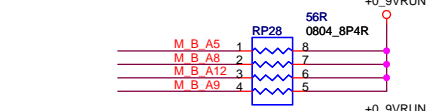
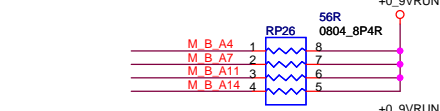
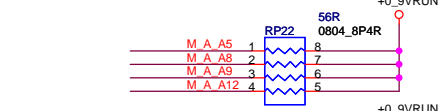
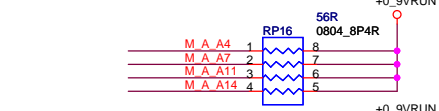
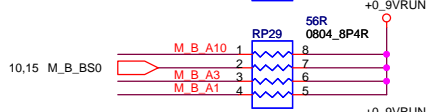
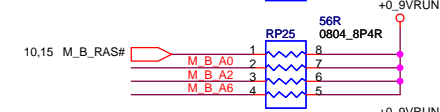
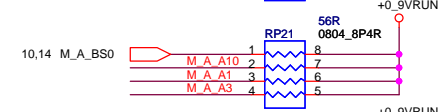
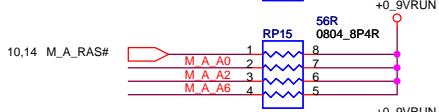
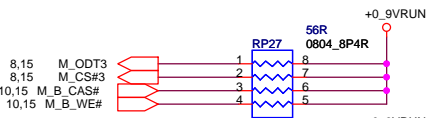
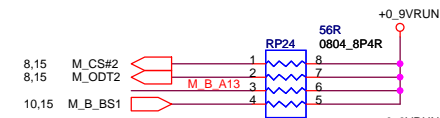
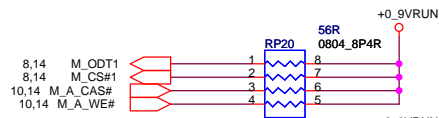
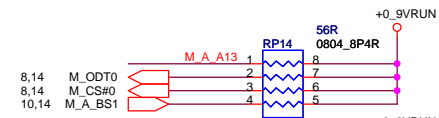
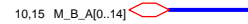
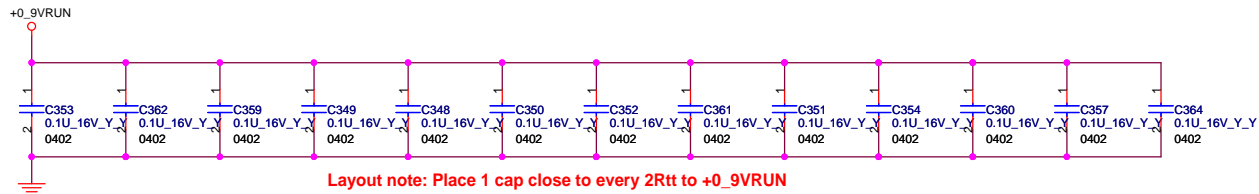
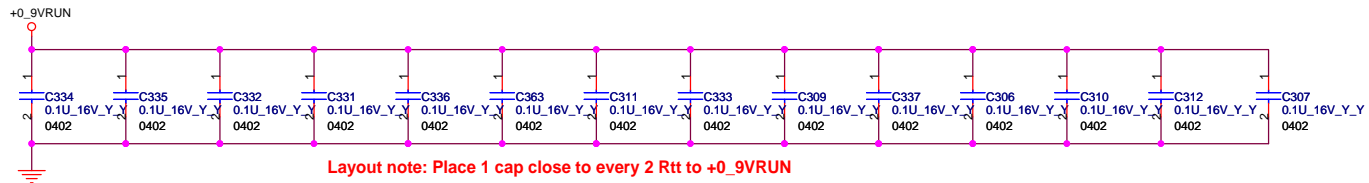


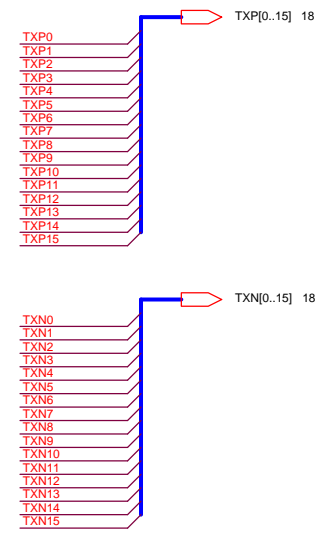
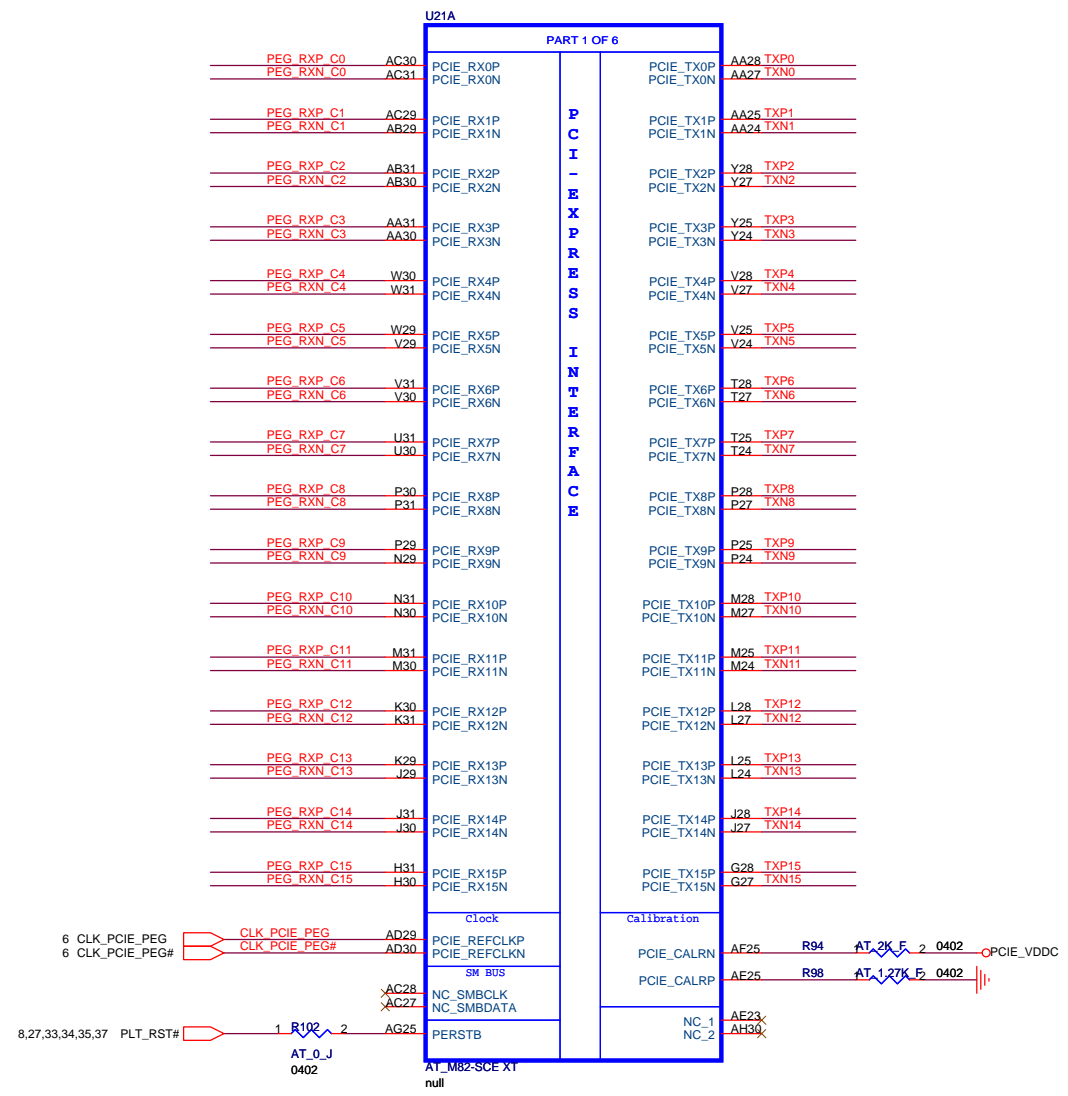
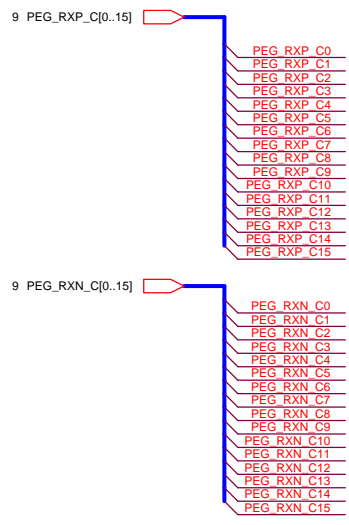
1.8V per DIMM=3.08A Height = 5.2mm, Reversed Type

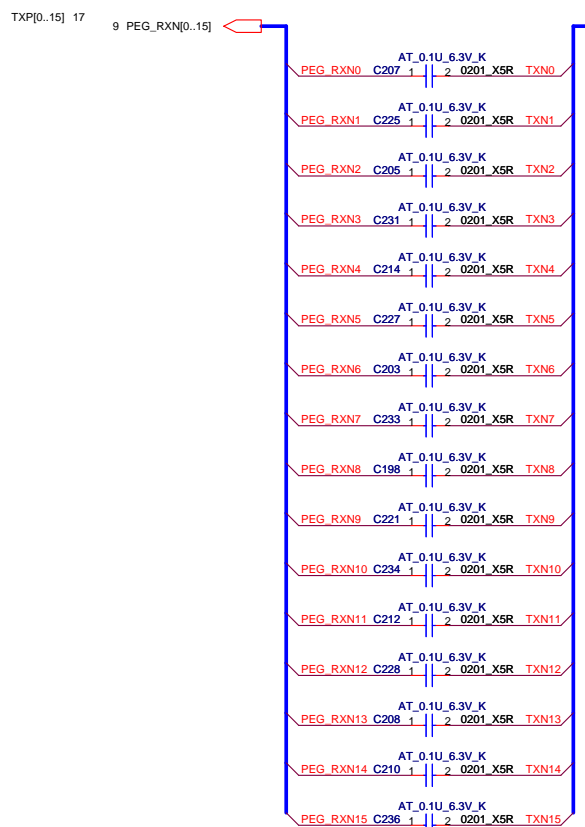
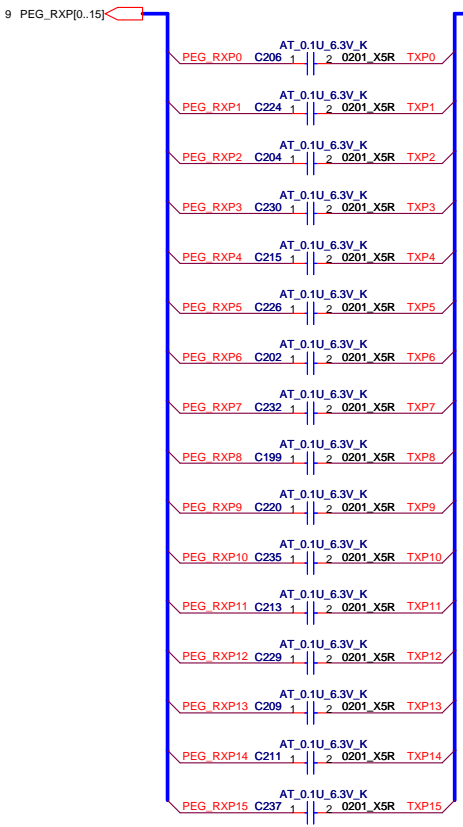


DDR2 SO-DIMM_2x100P
FOX_AS0A426_N2RN_7F
SMBus Address: A4(W)/A5(R)
DIMM_1 is placed farther from the GMCH than DIMM_0

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title DDR(I)SO-DIMM_1		CCPBG - R&D Division	
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 15	of 54	





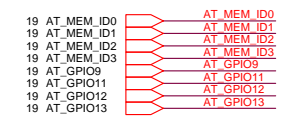
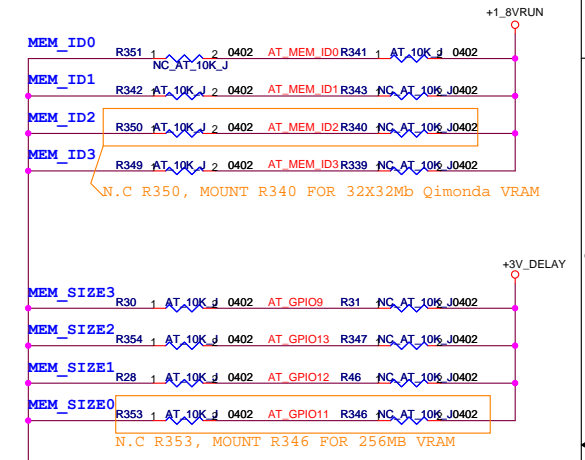


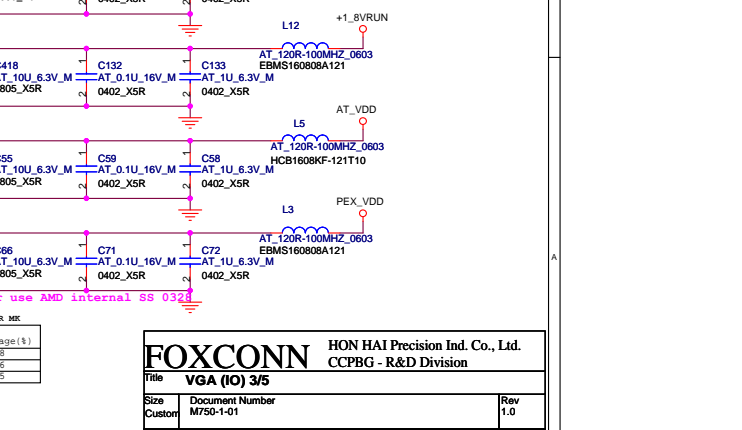
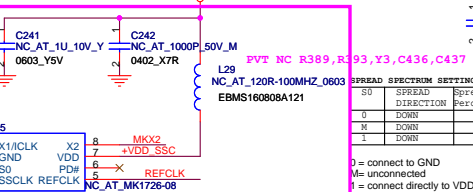
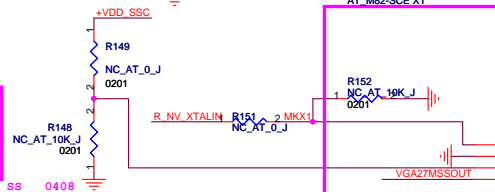
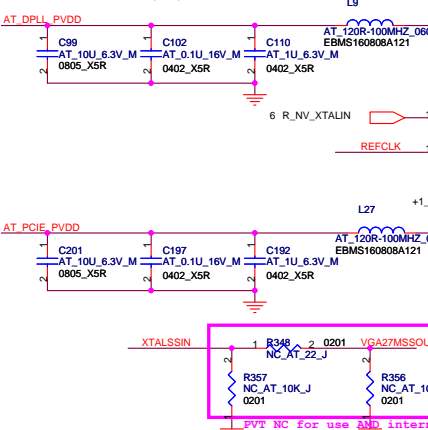
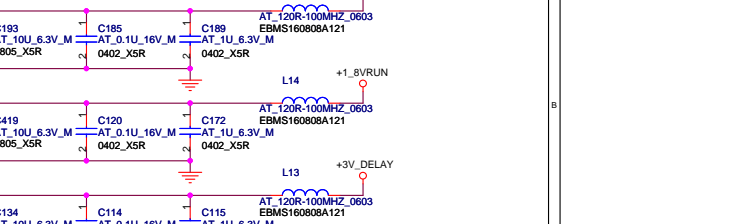
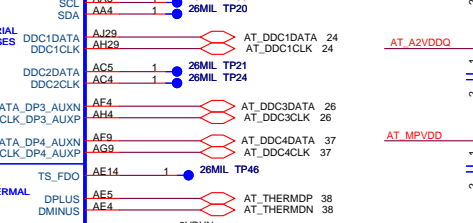
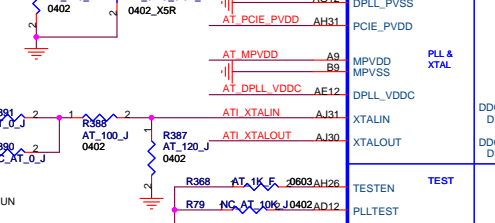
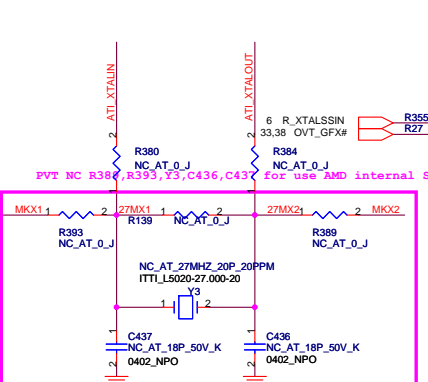
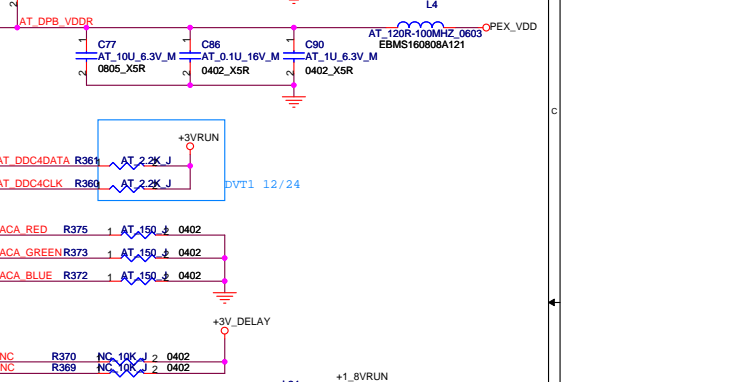
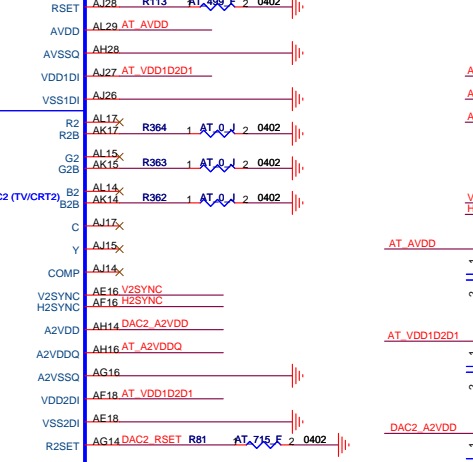
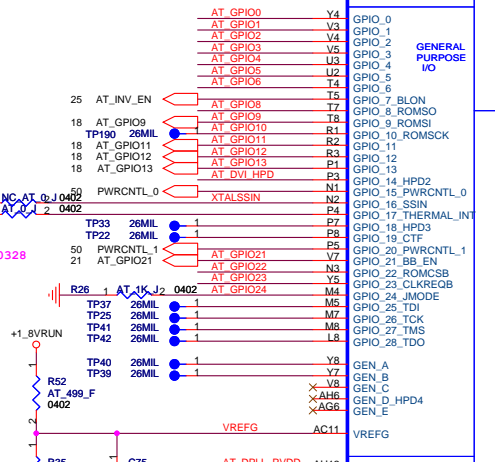
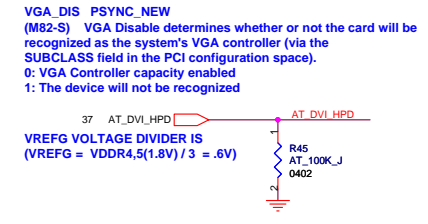
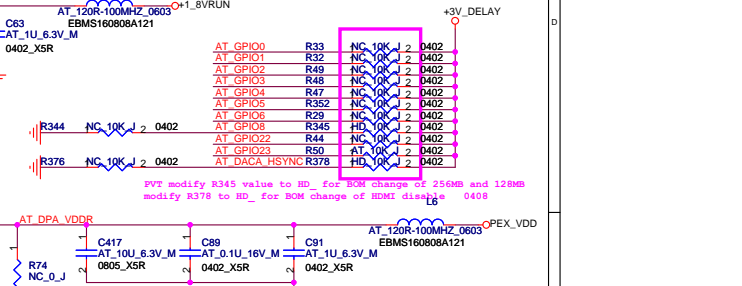
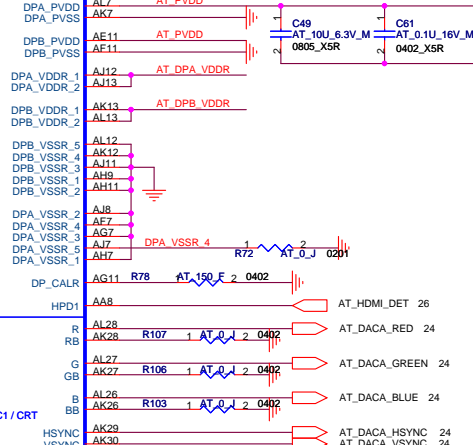
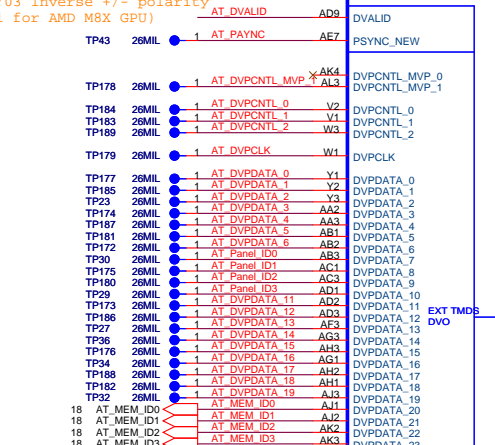
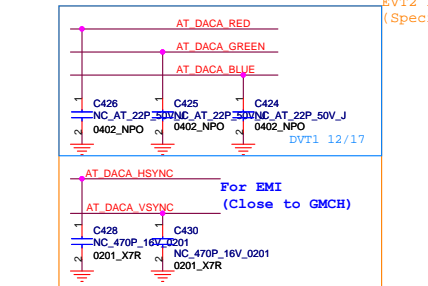
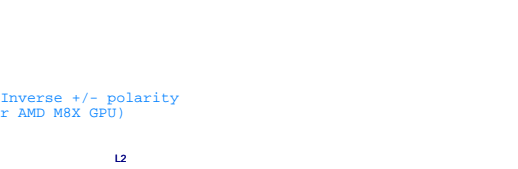
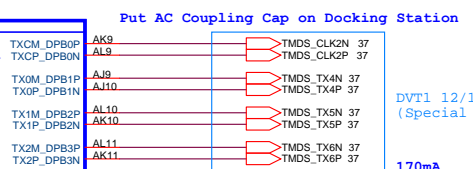
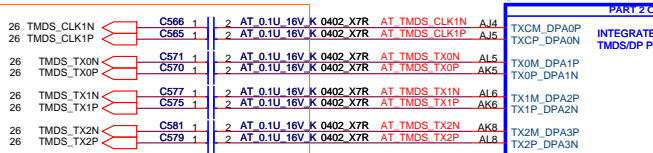
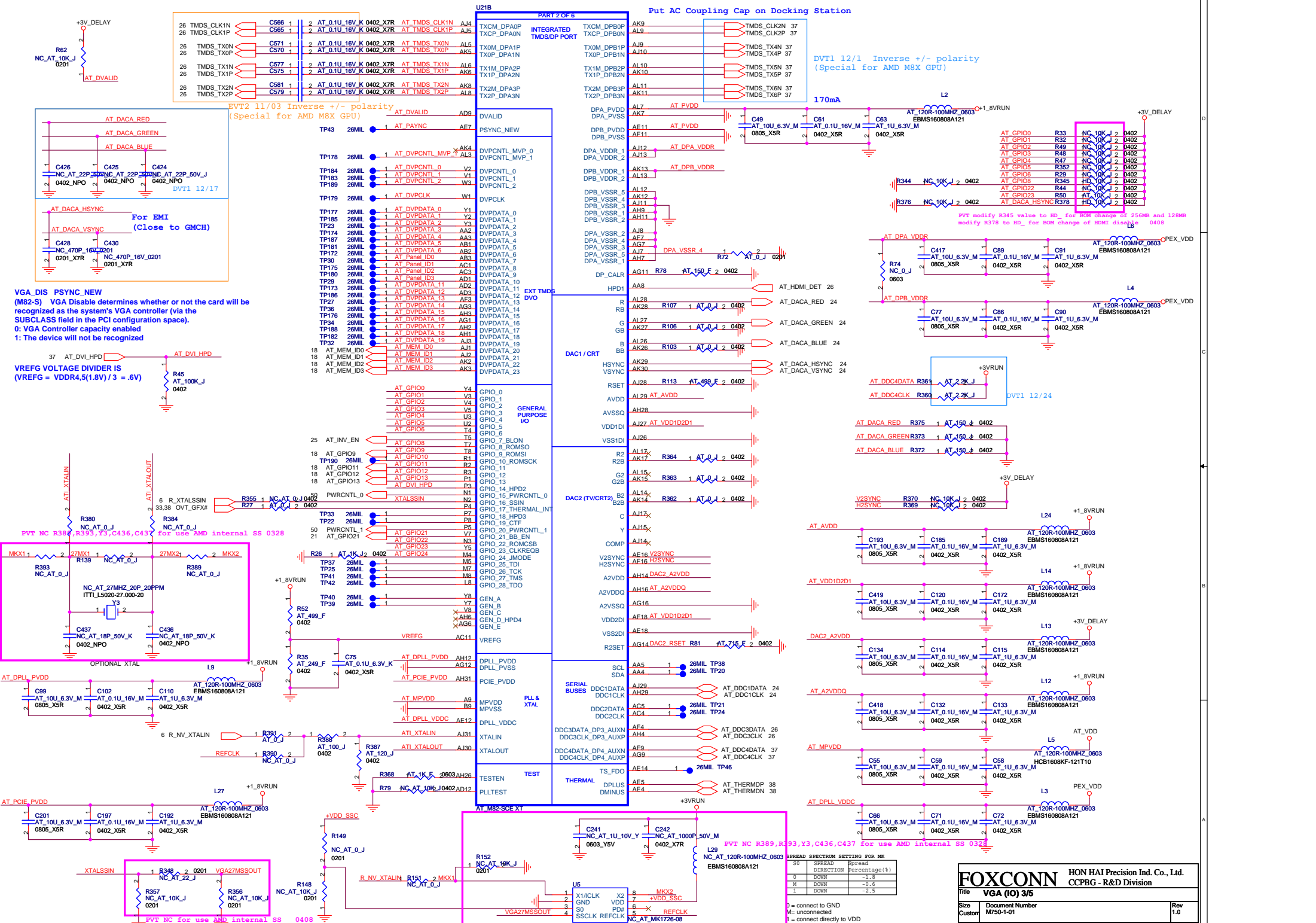
Strap for GDDR3-136ball
 ATL_DVPDATA[23 : 20]

0001 16Mx32 Qimonda
 0010 16Mx32 Hynix
 0011 16Mx32 Samsung
 0101 32Mx32 Qimonda
 0110 32Mx32 Hynix
 0111 32Mx32 Samsung

If no ROM attached, GPIO[9:13:12:11]
 CONFIG(3:0)
 controls the memory aperture size.

128MB	X000
256MB	X001
64MB	X010
32MB	X011
512MB	X100
1GB	X101
2GB	X110
4GB	X111





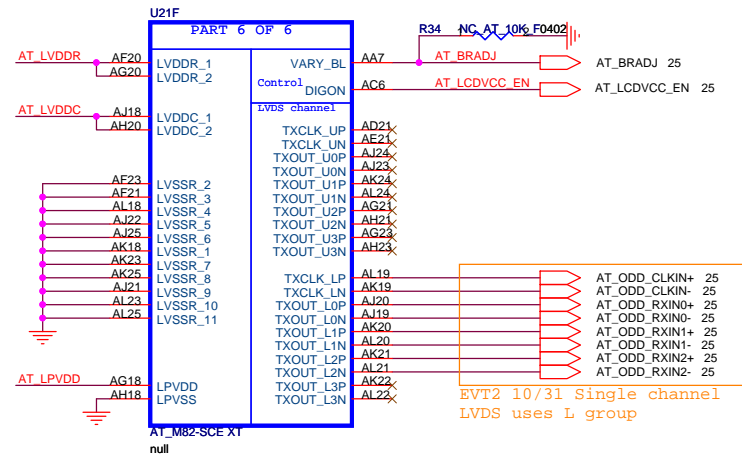
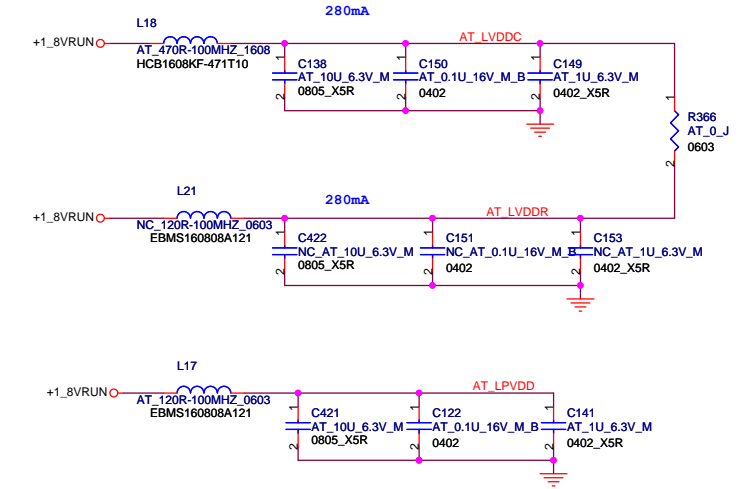
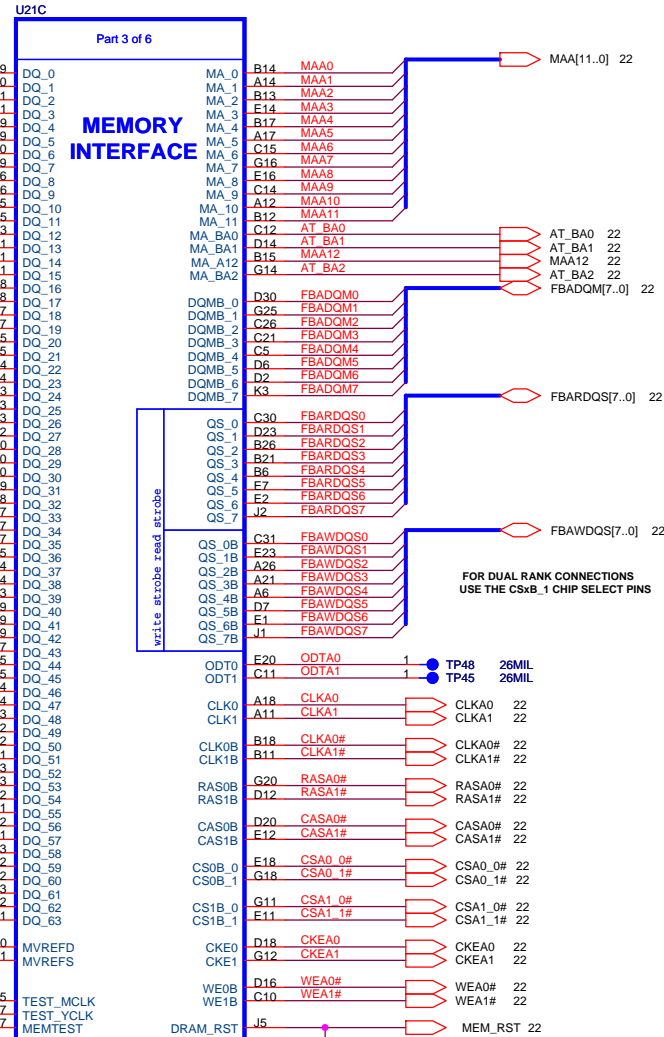
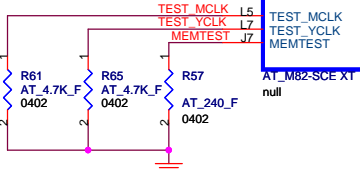
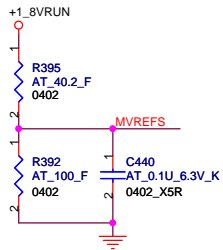
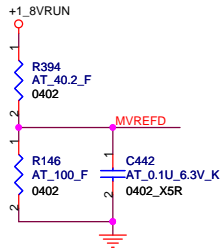
SPREAD SPECTRUM SETTING FOR MK

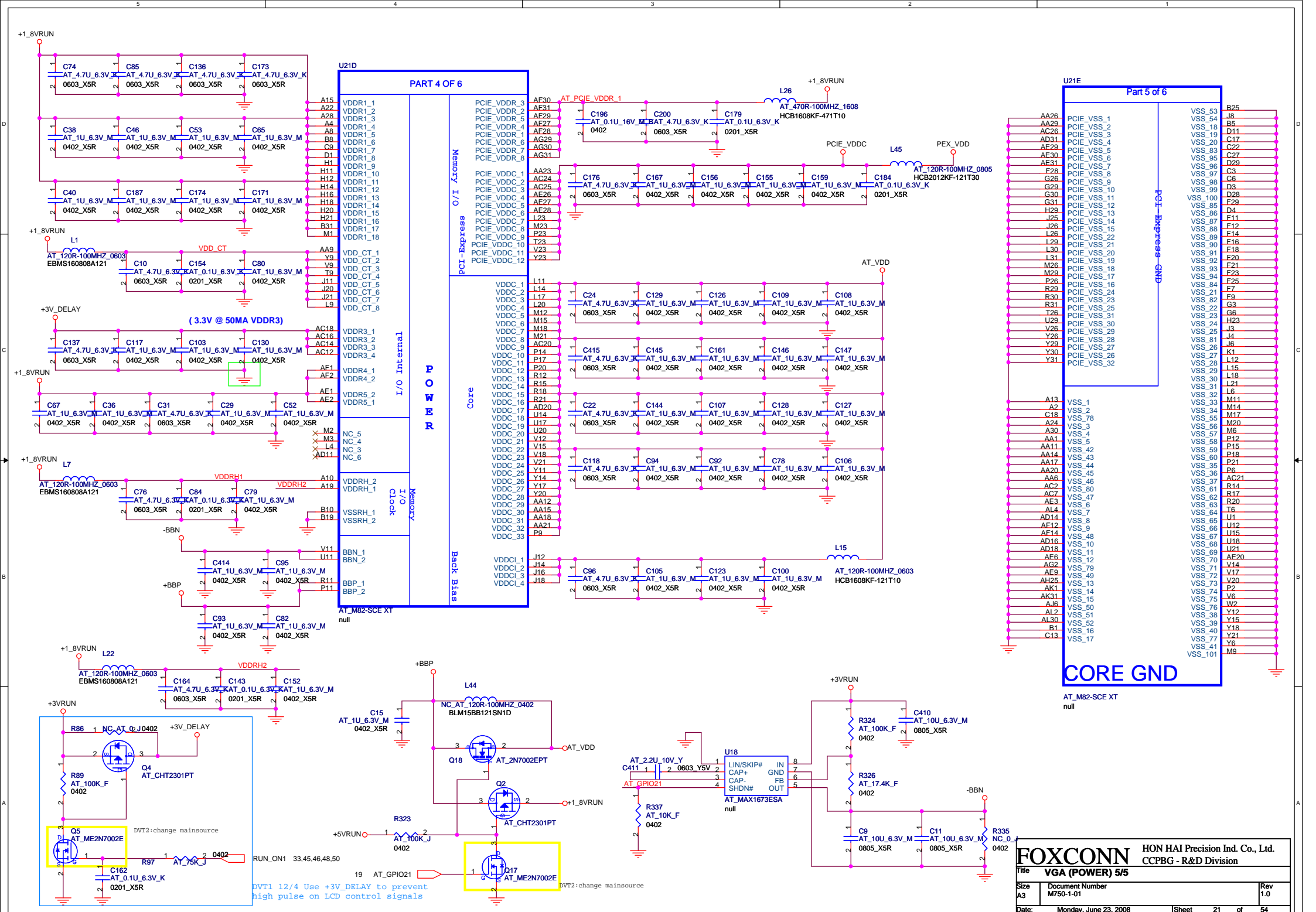
S0	SPREAD DIRECTION	Spread Percentage (%)
0	DOWN	-1.8
1	DOWN	-0.6
1	DOWN	-2.5

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

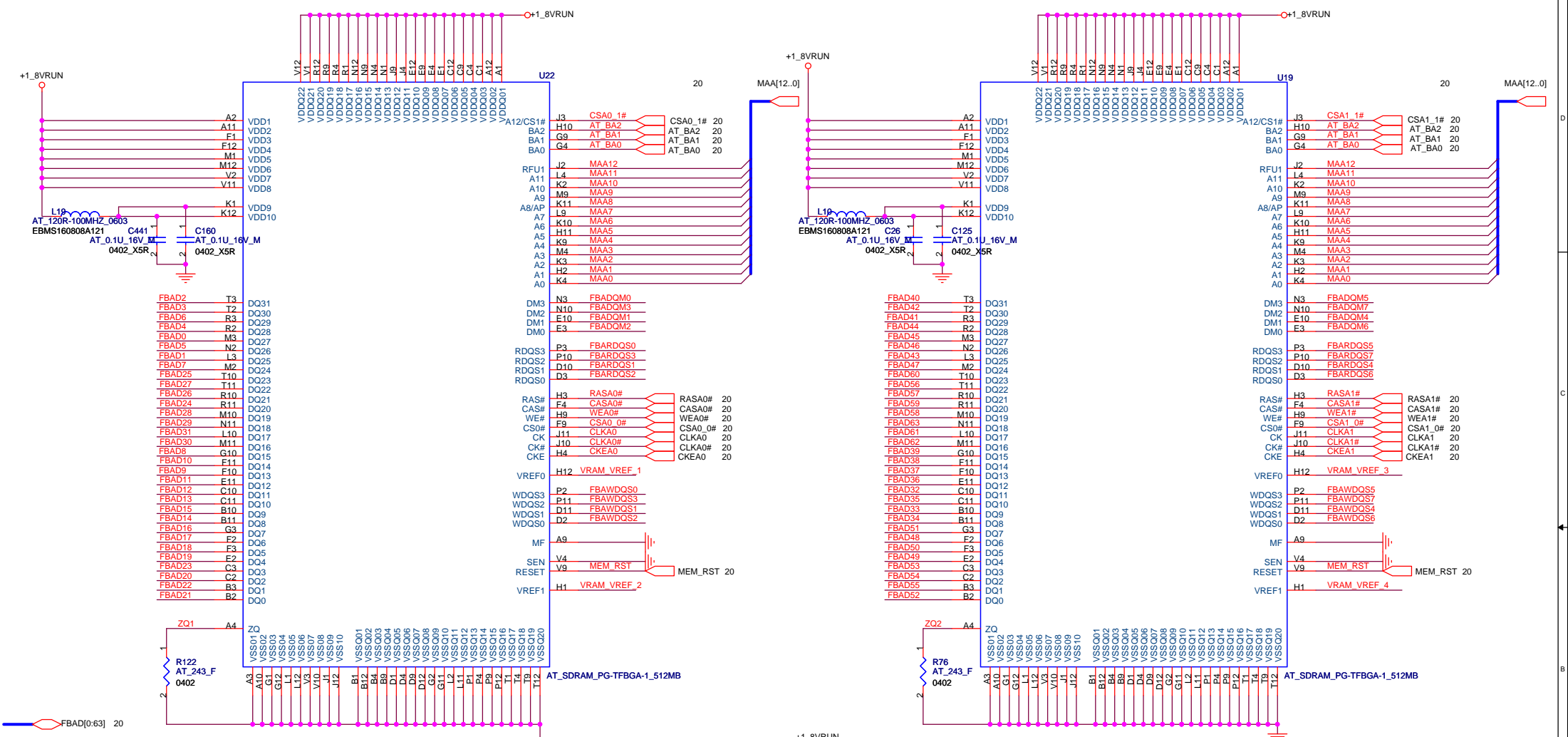
Title VGA (IO) 3/5
Size Custom
Document Number M750-1-01
Rev 1.0
Date Monday, June 23, 2008
Sheet 19 of 54

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

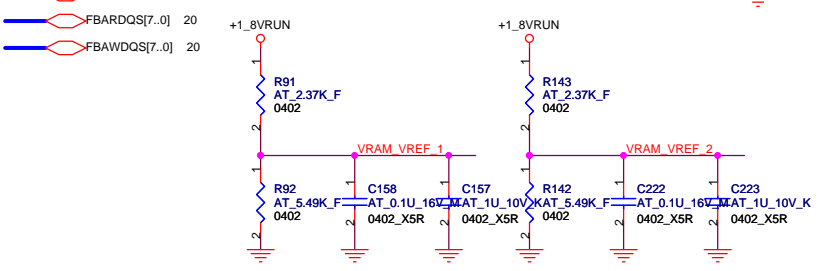




FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title VGA (POWER) 5/5		
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 21	of 54

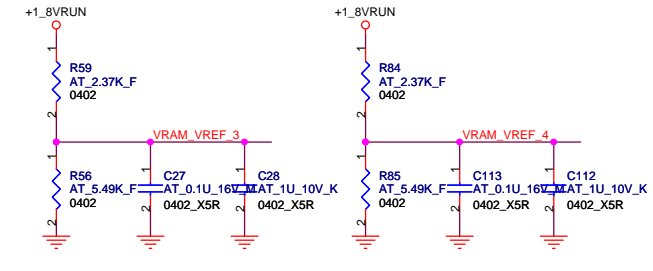


- FBAD[0:63] 20
- FBADQM[7:0] 20
- FBARDQS[7:0] 20
- FBAWDQS[7:0] 20

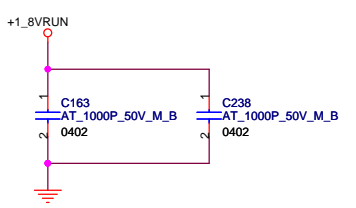
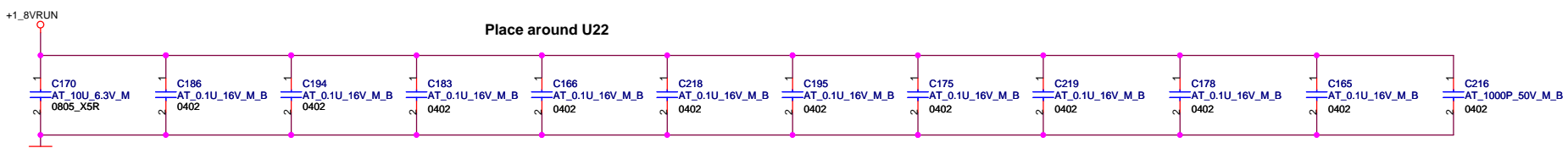
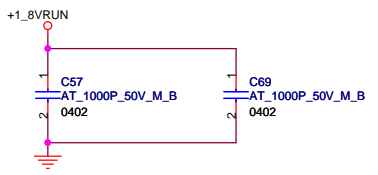
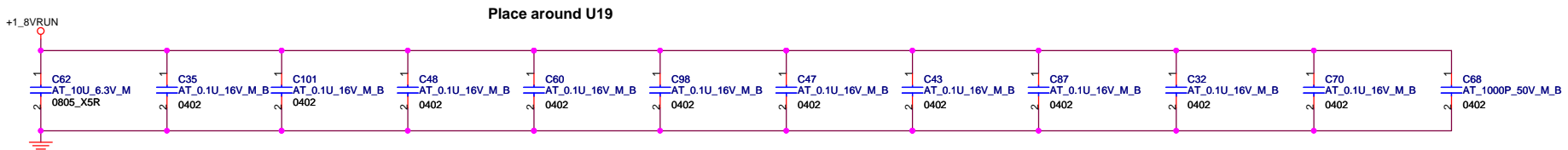


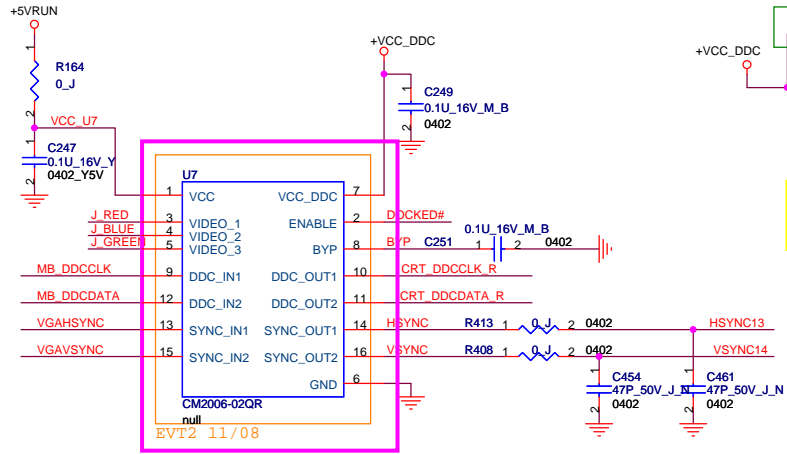
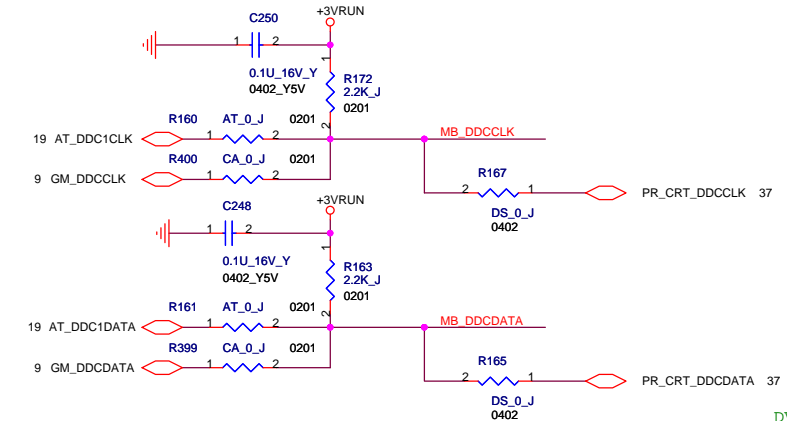
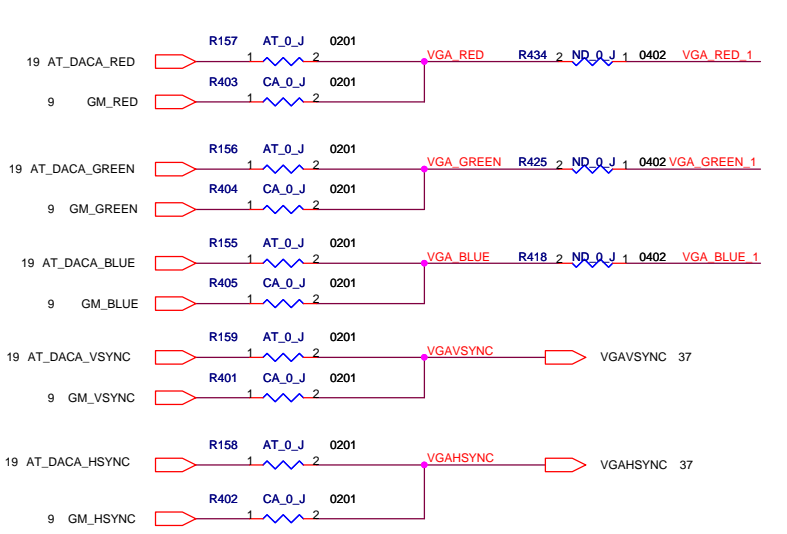
VRAM_VREF is 70%VDDQ for GDDR3

- RASA0# R130 AT_120 2 0402
- RASA1# R83 AT_20 2 0402
- CASA0# R120 AT_20 2 0402
- CASA1# R75 AT_20 2 0402
- WEA0# R117 AT_20 2 0402
- WEA1# R63 AT_20 2 0402
- CSA0_0#R118 AT_20 2 0402
- CSA1_0#R70 AT_20 2 0402
- CKEA0 R119 AT_20 2 0402
- CKEA1 R73 AT_20 2 0402
- CLKA0 R99 AT_20 2 0402
- CLKA0# R105 AT_20 2 0402
- CLKA1# R63 AT_20 2 0402
- CLKA1# R67 AT_20 2 0402
- CSA0_1#R133 AT_20 2 0402
- CSA1_1#R68 AT_20 2 0402

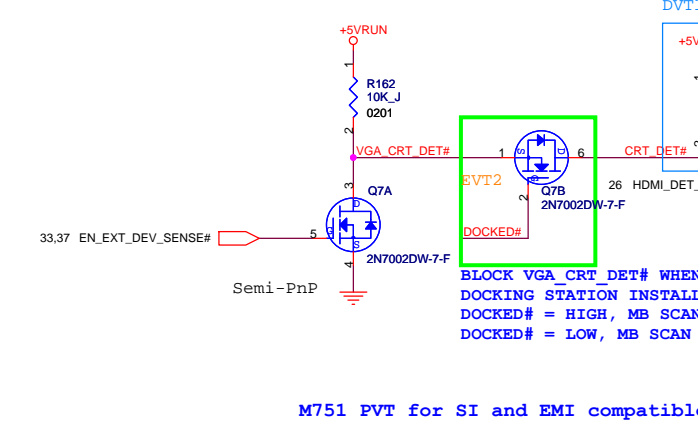
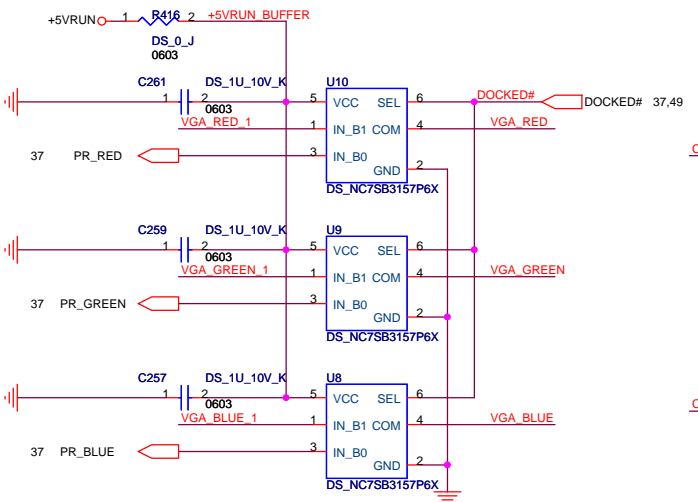


VRAM_VREF is 70%VDDQ for GDDR3



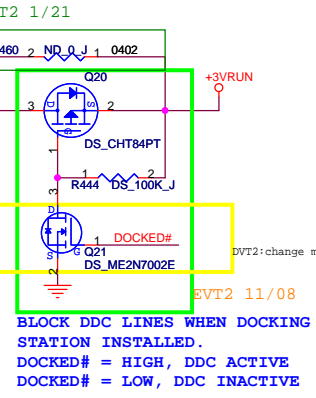


PVT update symbol to CM2006-02QR

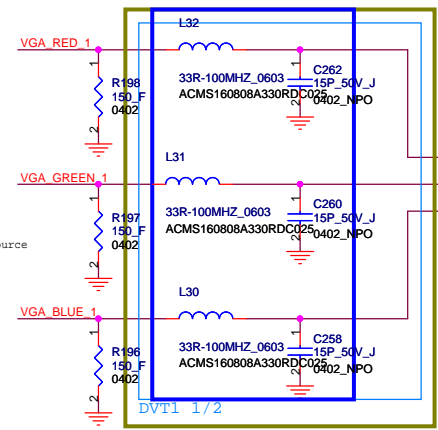


DOCKED#
BLOCK VGA CRT_DET# WHEN DOCKING STATION INSTALLED.
DOCKED# = HIGH, MB SCAN ON
DOCKED# = LOW, MB SCAN OFF

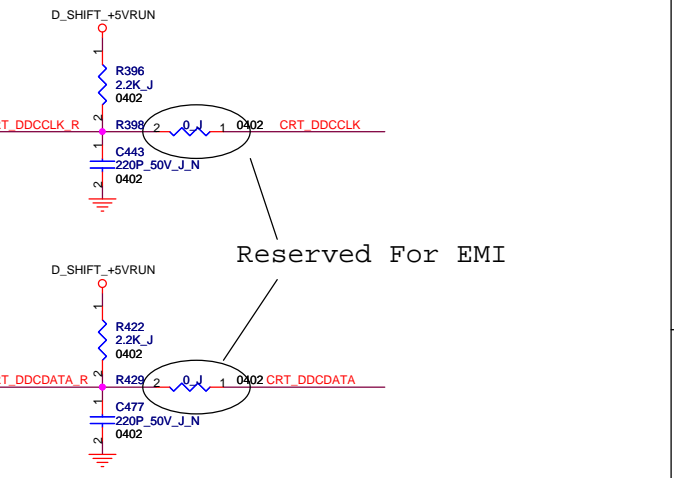
M751 PVT for SI and EMI compatible



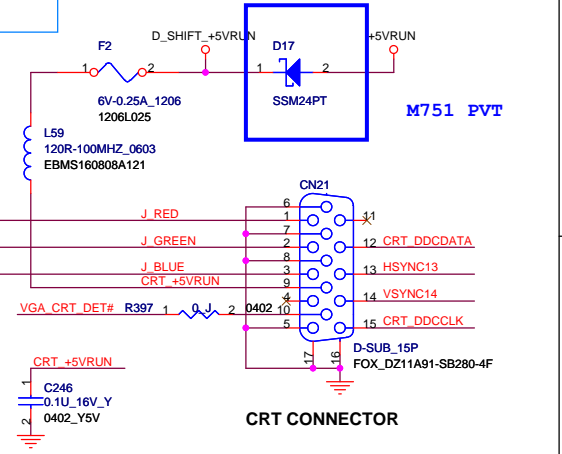
DOCKED#
BLOCK DDC LINES WHEN DOCKING STATION INSTALLED.
DOCKED# = HIGH, DDC ACTIVE
DOCKED# = LOW, DDC INACTIVE



M751 DVT changed for EMI



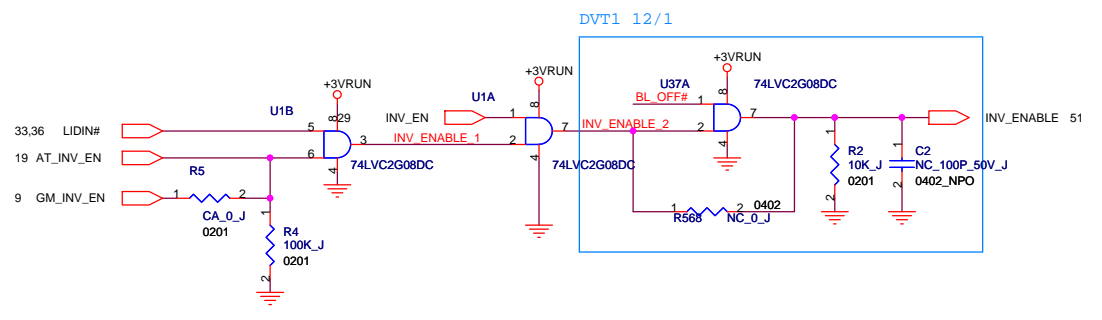
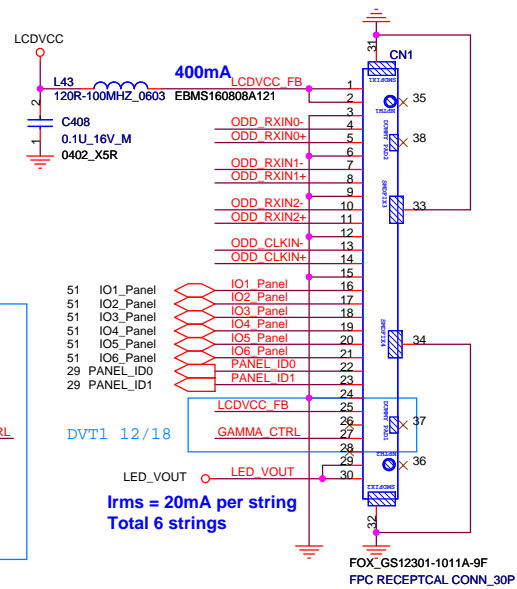
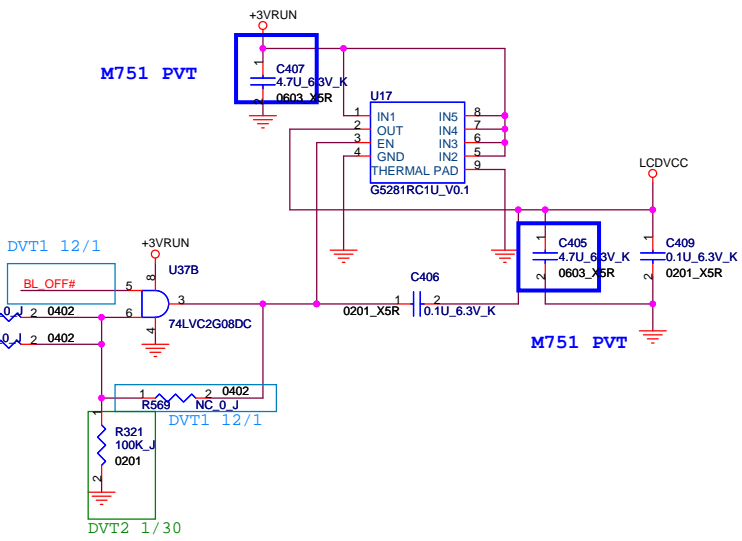
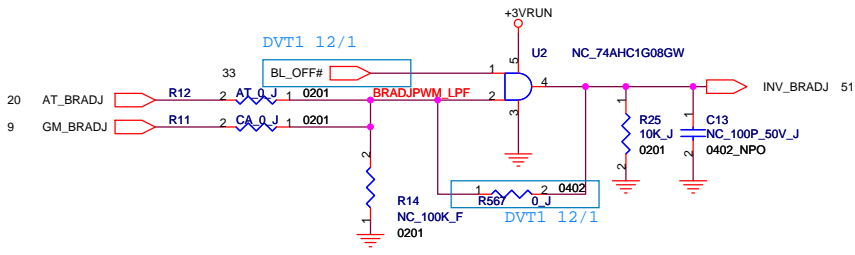
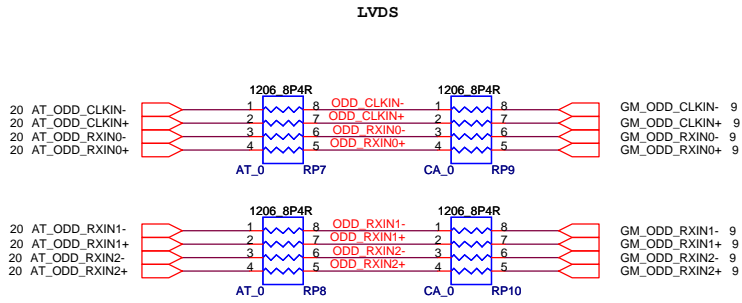
Reserved For EMI

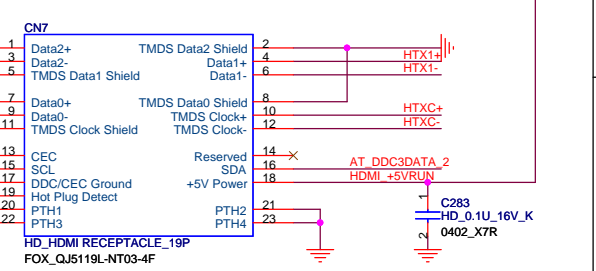
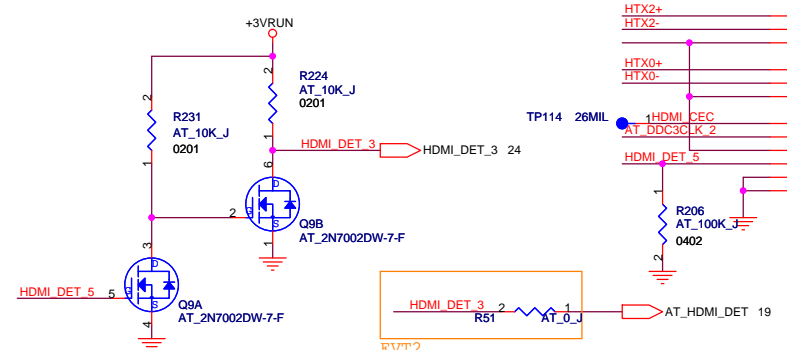
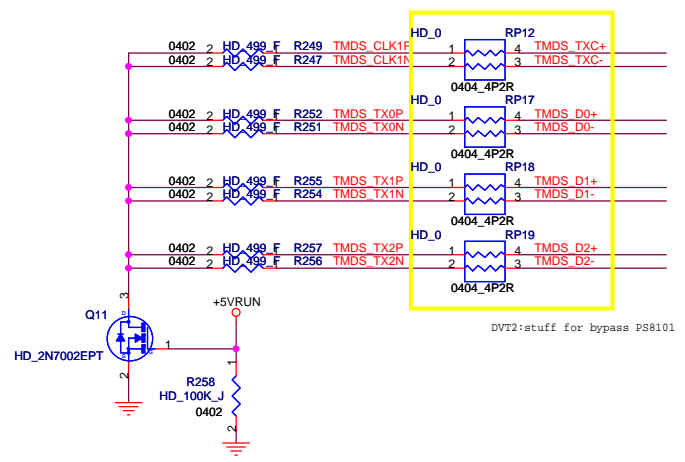
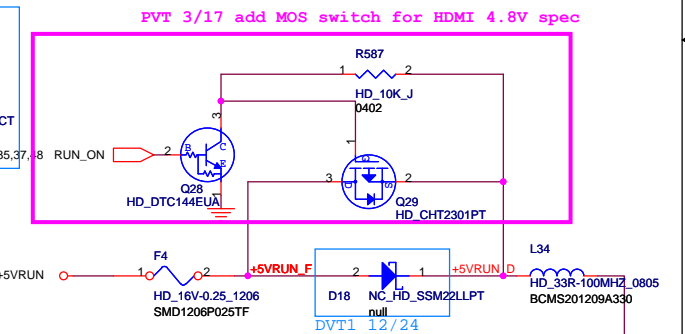
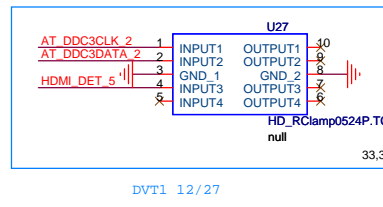
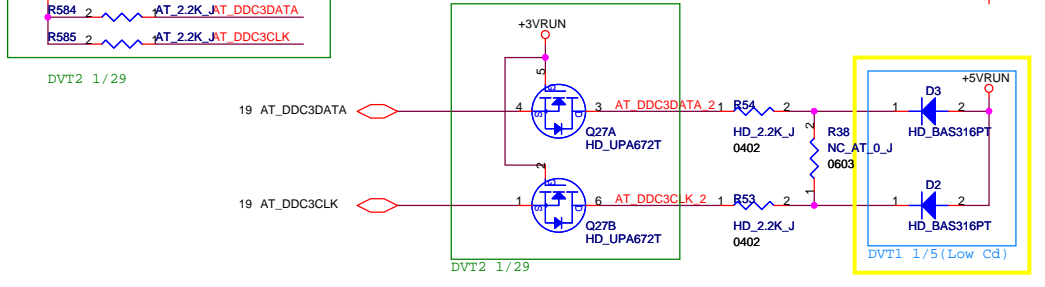
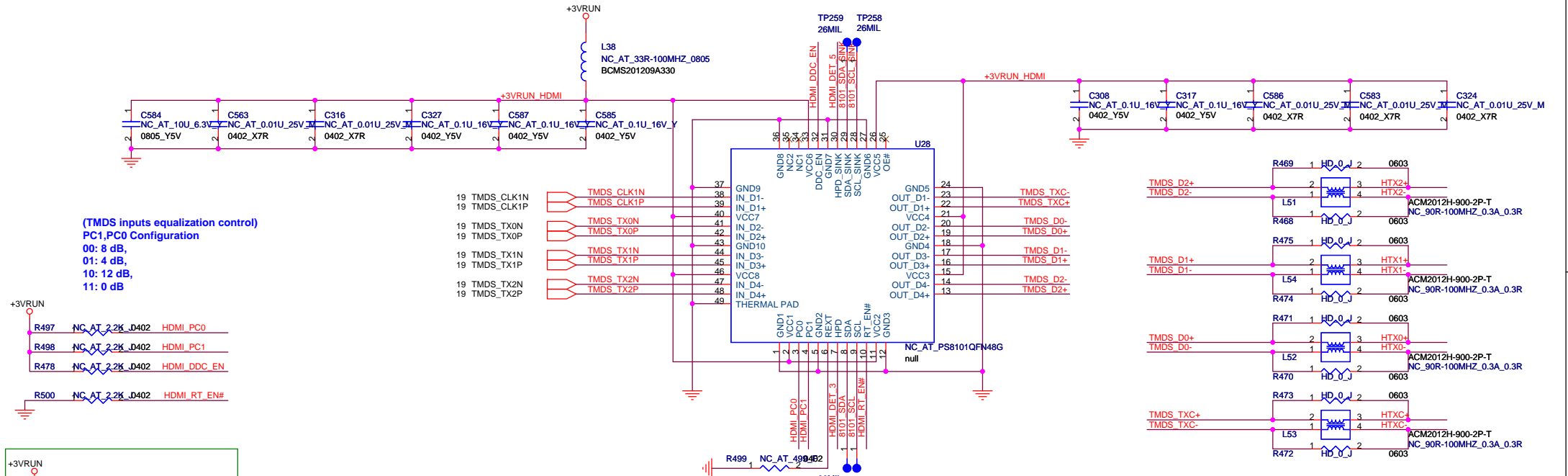


M751 PVT

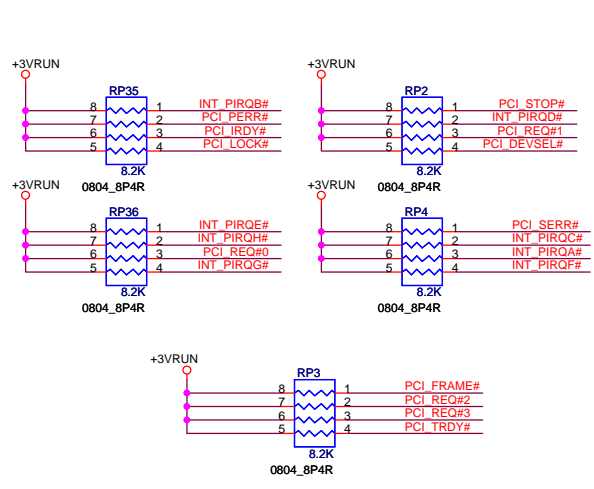
CRT CONNECTOR

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
File	CRT	
Size	Document Number	Rev
A3	M750-1-01	1.0
Date:	Thursday, June 26, 2008	Sheet 24 of 54

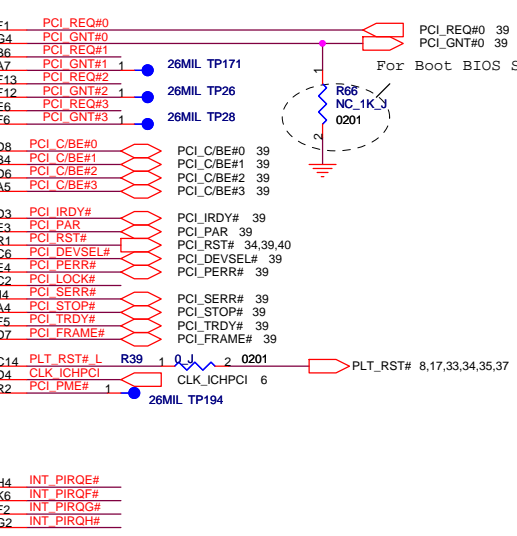
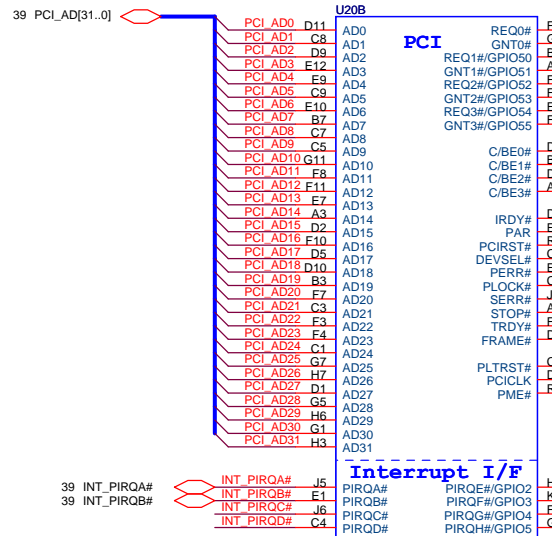




FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	HDMI	
Size	Document Number	Rev
A3	M750-1-01	1.0
Date	Monday, June 23, 2008	Sheet 26 of 54

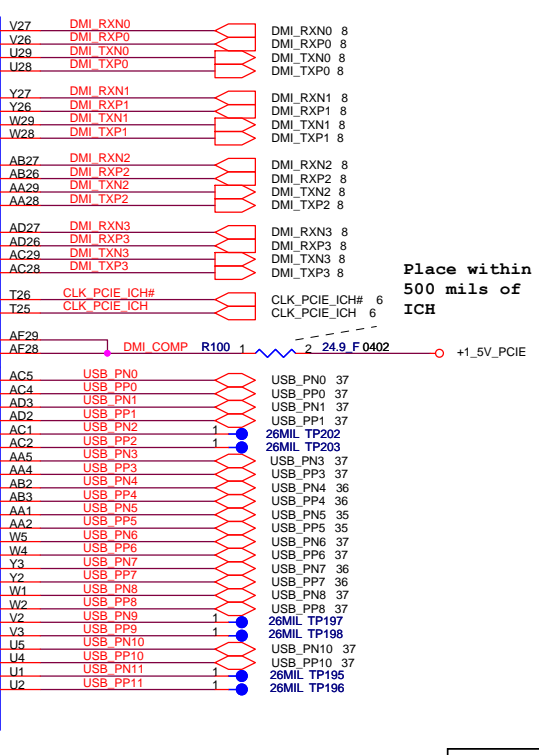
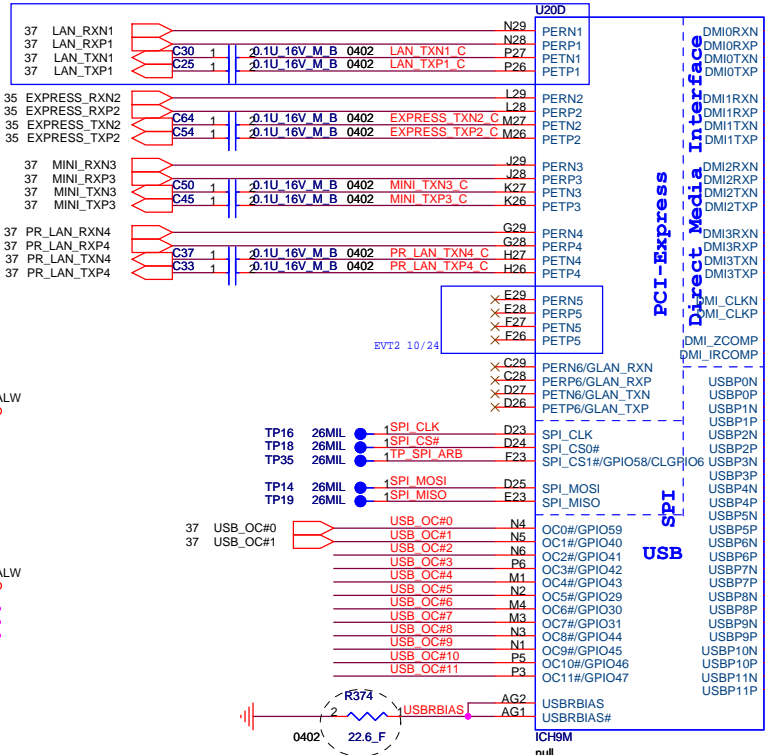


PCI Pullups

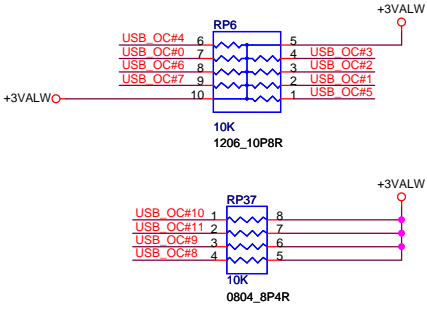


Strap for Boot-BIOS

	GNT#	SPI_CS#
IPI(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI



USB PORT	Function
PORT-0	SIDE-1
PORT-1	SIDE-2
PORT-2	x
PORT-3	Docking Hub
PORT-4	Bluetooth
PORT-5	ExpressCard
PORT-6	FingerPrint
PORT-7	Camera
PORT-8	Felica
PORT-9	x
PORT-10	Wimax
PORT-11	x



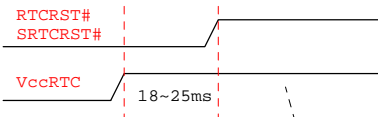
Place within 500 mils of ICH and don't route next to high speed signals

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **ICH9-M(PCI/DMI/USB/PCIE) 1/5**

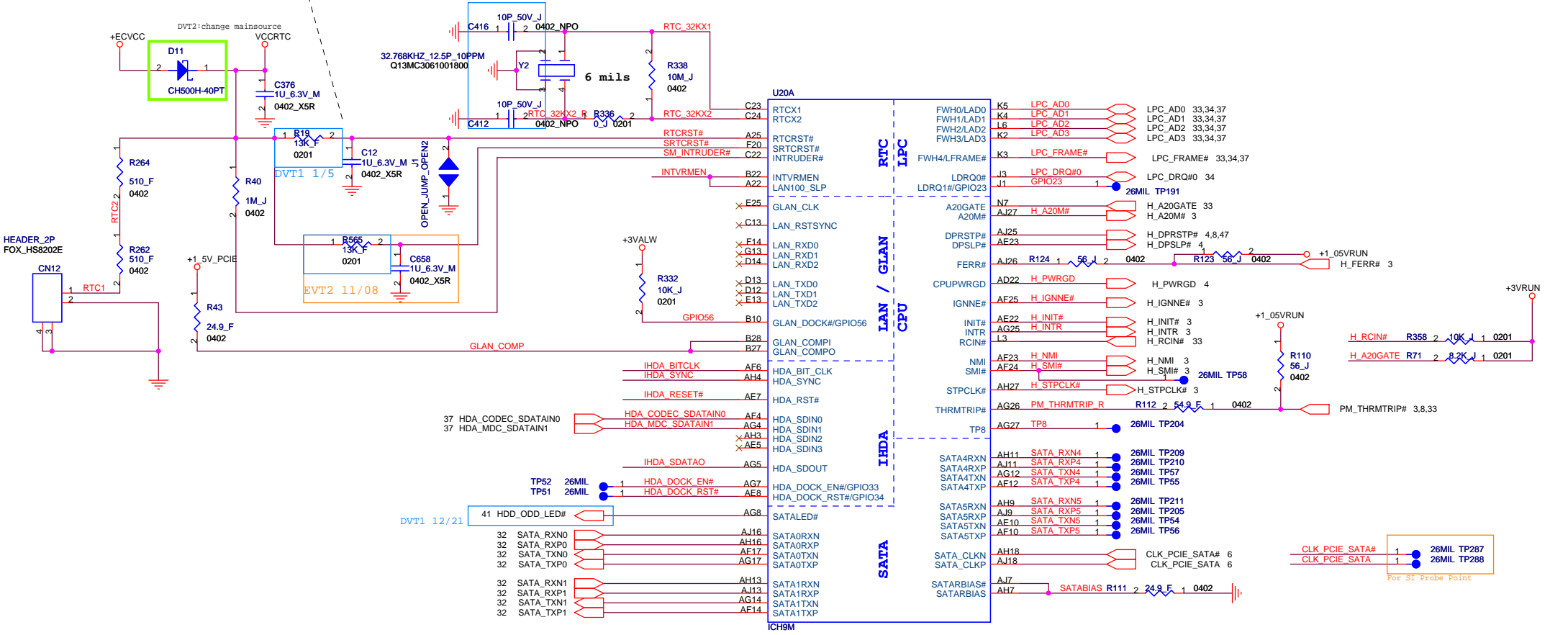
Size A3 Document Number M750-1-01 Rev 1.0

Date: Monday, June 23, 2008 Sheet 27 of 54

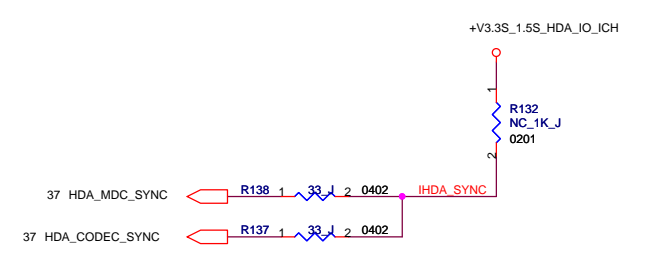
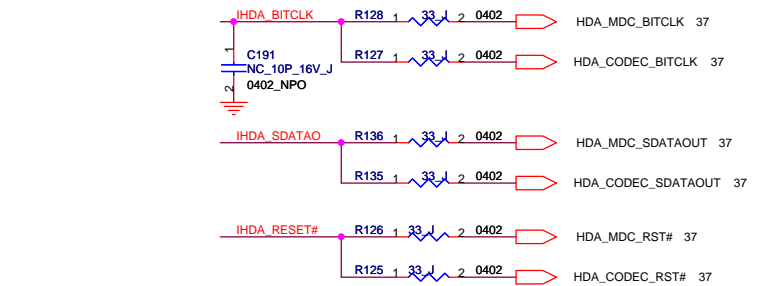


Internal VRM enabled for VccSus1_05, VccSus1_5, VccC1_5, VccLAN1_05 and VccC1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)

The traces inside this block should be wider.
DVT1 12/23



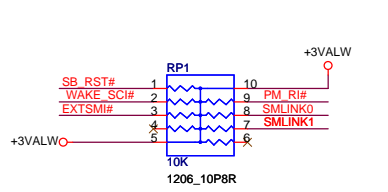
HEADER_2P
FOX_HS8202E



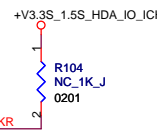
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **ICH9-M (LPC,IDE,SATA) 2/5**

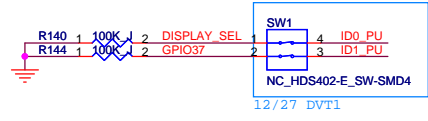
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 28	of 54



Stuff for No-reboot
 Low=Default
 High=No-reboot



SYSTEM ID0-3

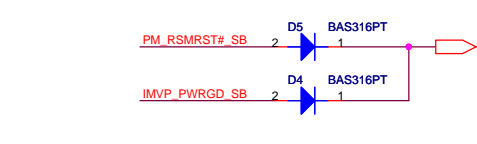
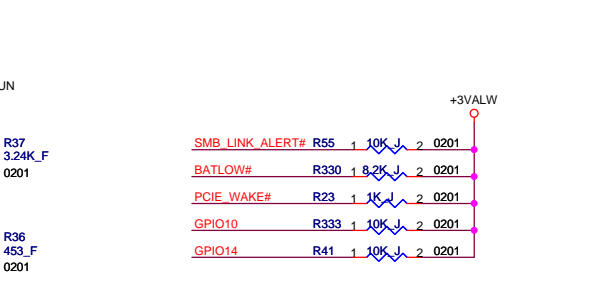
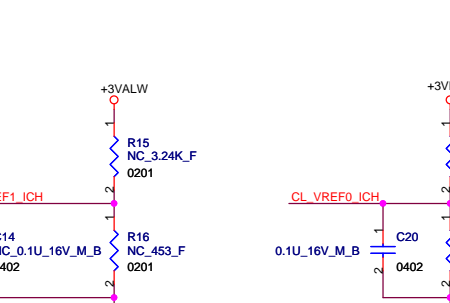
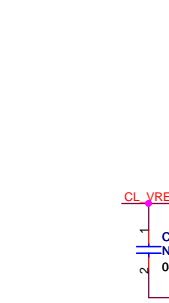
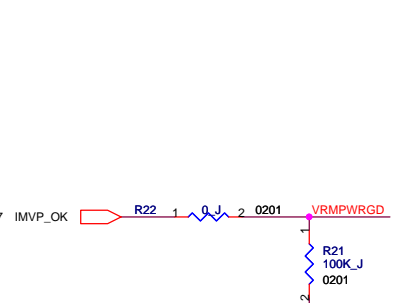
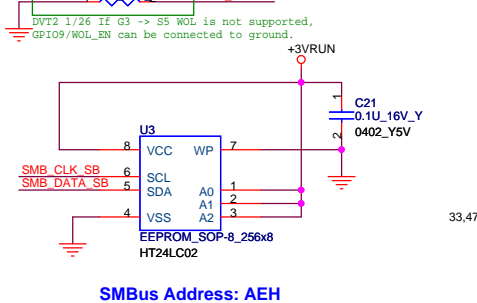
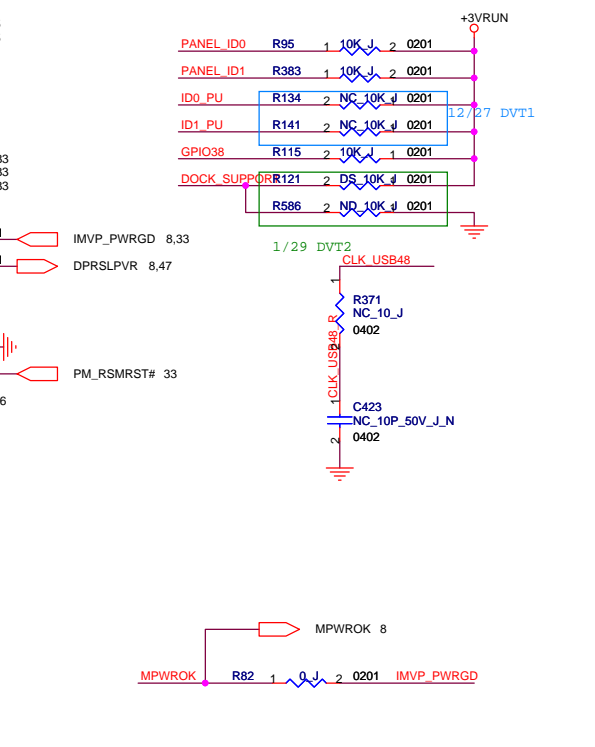
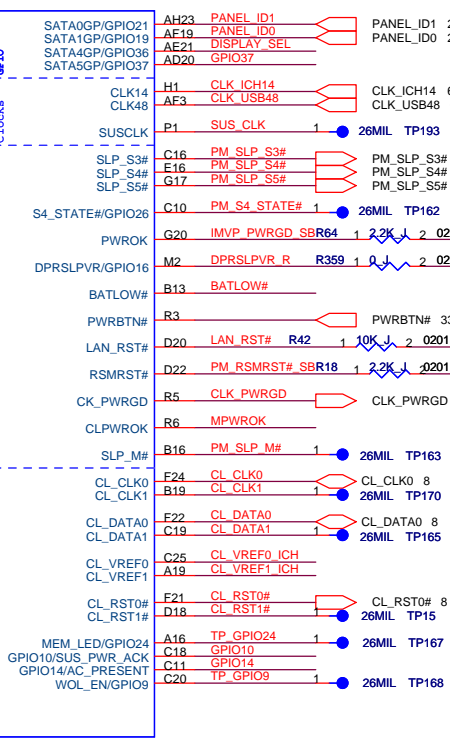
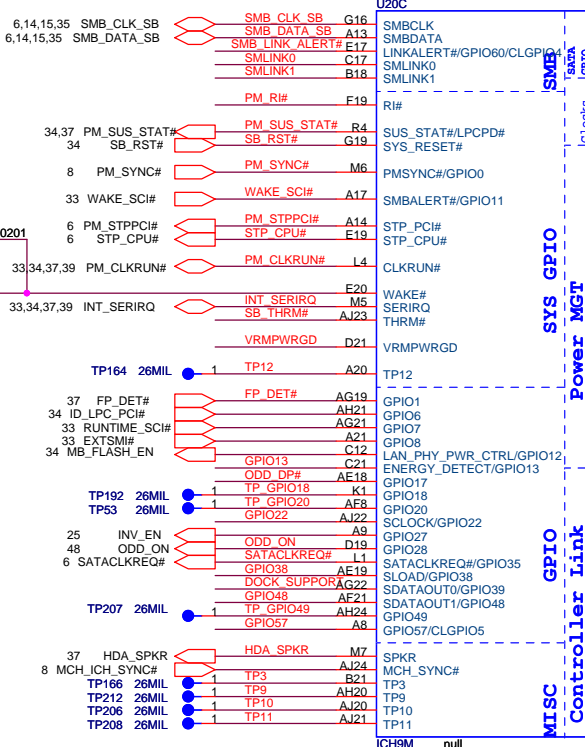
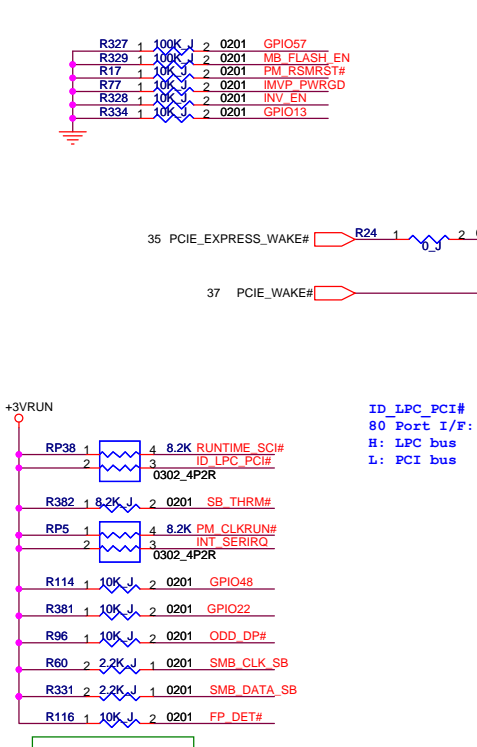
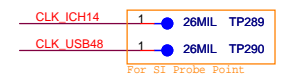


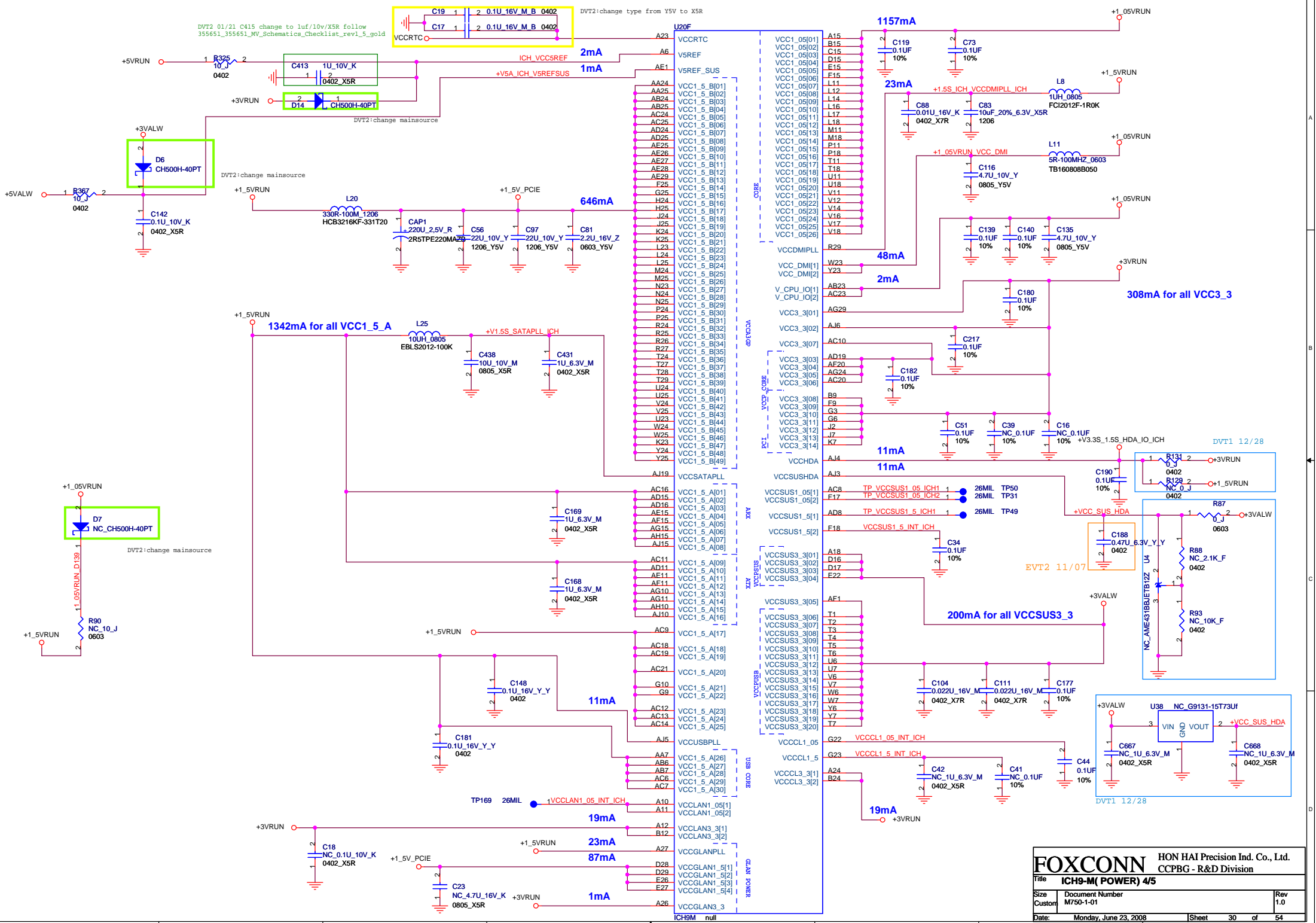
SW1: DISPLAY OUTOUT SELECTION
 (FOR DEBUG ONLY)

DISPLAY_SEL	
0	CRT
1	LVDS

Dock Support Selection

	Dock Support
0	Not Support
1	Support

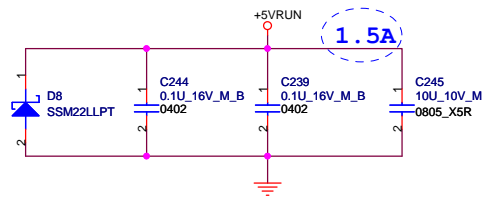




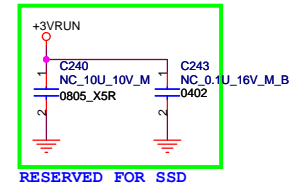
U20E		
AA26	VSS[001]	VSS[107]
AA27	VSS[002]	VSS[108]
AA3	VSS[003]	VSS[109]
AA6	VSS[004]	VSS[110]
AB1	VSS[005]	VSS[111]
AA23	VSS[006]	VSS[112]
AB28	VSS[007]	VSS[113]
AB29	VSS[008]	VSS[114]
AB4	VSS[009]	VSS[115]
AB5	VSS[010]	VSS[116]
AC17	VSS[011]	VSS[117]
AC26	VSS[012]	VSS[118]
AC27	VSS[013]	VSS[119]
AC3	VSS[014]	VSS[120]
AD1	VSS[015]	VSS[121]
AD10	VSS[016]	VSS[122]
AD12	VSS[017]	VSS[123]
AD13	VSS[018]	VSS[124]
AD14	VSS[019]	VSS[125]
AD17	VSS[020]	VSS[126]
AD18	VSS[021]	VSS[127]
AD21	VSS[022]	VSS[128]
AD28	VSS[023]	VSS[129]
AD29	VSS[024]	VSS[130]
AD4	VSS[025]	VSS[131]
AD5	VSS[026]	VSS[132]
AD6	VSS[027]	VSS[133]
AD7	VSS[028]	VSS[134]
AD9	VSS[029]	VSS[135]
AE12	VSS[030]	VSS[136]
AE13	VSS[031]	VSS[137]
AE14	VSS[032]	VSS[138]
AE16	VSS[033]	VSS[139]
AE17	VSS[034]	VSS[140]
AE2	VSS[035]	VSS[141]
AE20	VSS[036]	VSS[142]
AE24	VSS[037]	VSS[143]
AE3	VSS[038]	VSS[144]
AE4	VSS[039]	VSS[145]
AE6	VSS[040]	VSS[146]
AE9	VSS[041]	VSS[147]
AF13	VSS[042]	VSS[148]
AF16	VSS[043]	VSS[149]
AF18	VSS[044]	VSS[150]
AF22	VSS[045]	VSS[151]
AH26	VSS[046]	VSS[152]
AF26	VSS[047]	VSS[153]
AF27	VSS[048]	VSS[154]
AF5	VSS[049]	VSS[155]
AF7	VSS[050]	VSS[156]
AF9	VSS[051]	VSS[157]
AG13	VSS[052]	VSS[158]
AG18	VSS[053]	VSS[159]
AG18	VSS[054]	VSS[160]
AG20	VSS[055]	VSS[161]
AG23	VSS[056]	VSS[162]
AG3	VSS[057]	VSS[163]
AG6	VSS[058]	VSS[164]
AG9	VSS[059]	VSS[165]
AH12	VSS[060]	VSS[166]
AH14	VSS[061]	VSS[167]
AH17	VSS[062]	VSS[168]
AH19	VSS[063]	VSS[169]
AH2	VSS[064]	VSS[170]
AH22	VSS[065]	VSS[171]
AH25	VSS[066]	VSS[172]
AH28	VSS[067]	VSS[173]
AH5	VSS[068]	VSS[174]
AH8	VSS[069]	VSS[175]
AJ12	VSS[070]	VSS[176]
AJ14	VSS[071]	VSS[177]
AJ17	VSS[072]	VSS[178]
AJ8	VSS[073]	VSS[179]
B11	VSS[074]	VSS[180]
B14	VSS[075]	VSS[181]
B17	VSS[076]	VSS[182]
B2	VSS[077]	VSS[183]
B20	VSS[078]	VSS[184]
B23	VSS[079]	VSS[185]
B5	VSS[080]	VSS[186]
B8	VSS[081]	VSS[187]
C26	VSS[082]	VSS[188]
C27	VSS[083]	VSS[189]
E11	VSS[084]	VSS[190]
E14	VSS[085]	VSS[191]
E18	VSS[086]	VSS[192]
E2	VSS[087]	VSS[193]
E21	VSS[088]	VSS[194]
E24	VSS[089]	VSS[195]
E5	VSS[090]	VSS[196]
E8	VSS[091]	VSS[197]
F16	VSS[092]	VSS[198]
F28	VSS[093]	VSS[199]
F29	VSS[094]	VSS[200]
G12	VSS[095]	VSS[201]
G14	VSS[096]	VSS[202]
G18	VSS[097]	VSS[203]
G21	VSS[098]	VSS[204]
G24	VSS[099]	VSS[205]
G26	VSS[100]	VSS[206]
G27	VSS[101]	VSS[207]
G8	VSS[102]	VSS[208]
H2	VSS[103]	VSS[209]
H23	VSS[104]	VSS[210]
H28	VSS[105]	VSS[211]
H29	VSS[106]	VSS[212]

ICH9M null

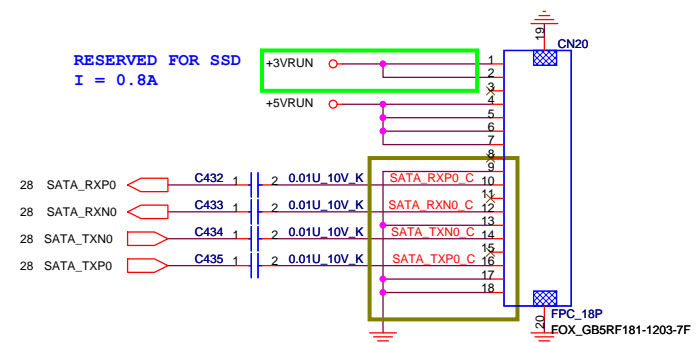
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ICH9-M (GND) 5/5		
Size	Document Number	Rev	
A3	M750-1-01	1.0	
Date:	Monday, June 23, 2008	Sheet	31 of 54



1.5A



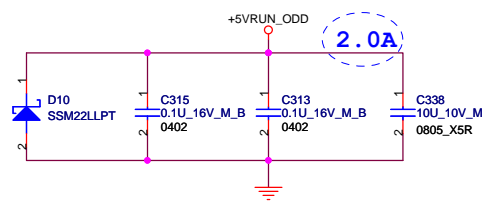
RESERVED FOR SSD



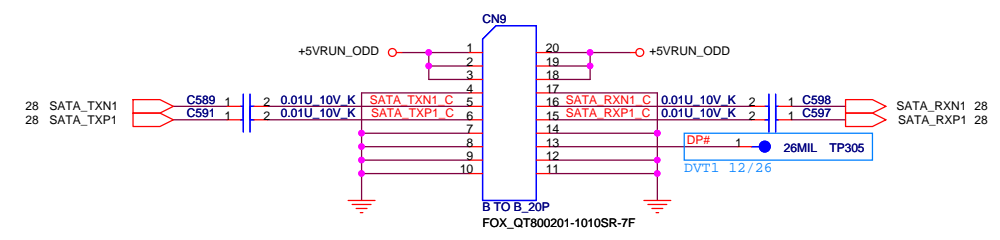
RESERVED FOR SSD
I = 0.8A

M751 DVT to increase the impedance for sata SI fail

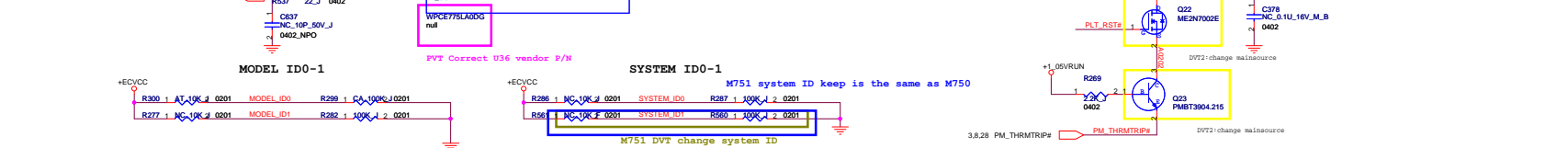
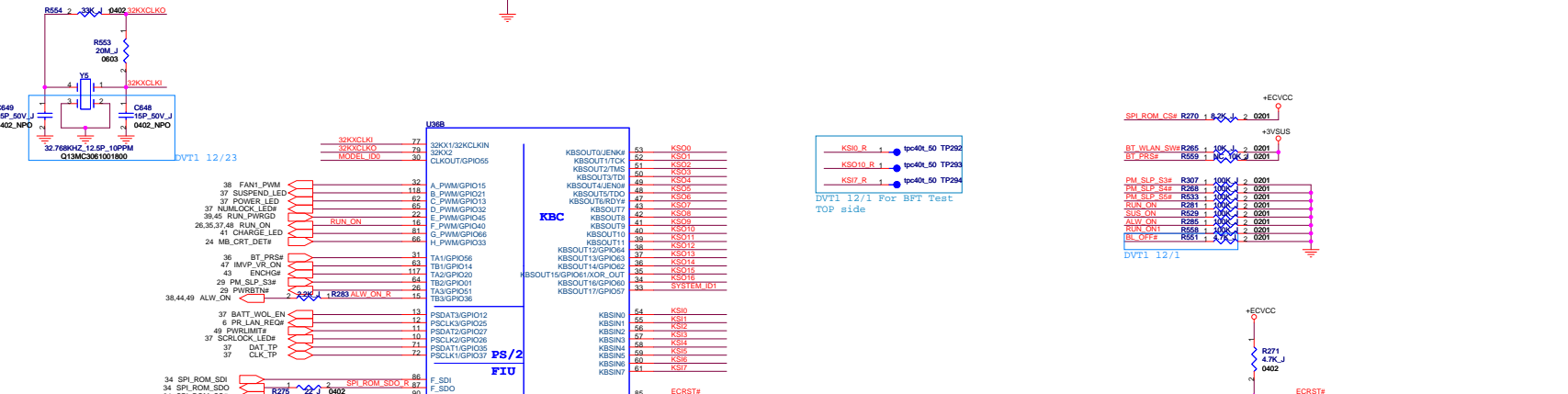
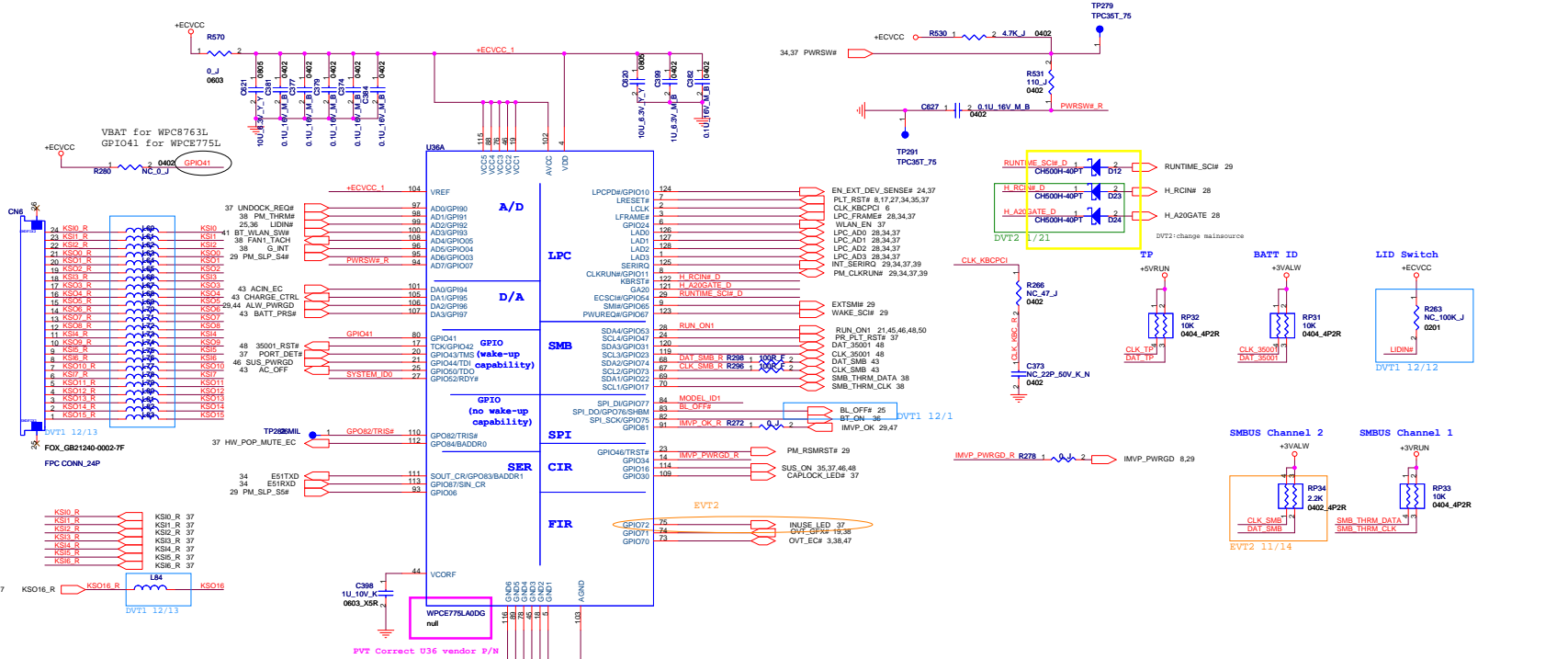
SATA HDD CONN



2.0A



SATA ODD CONN

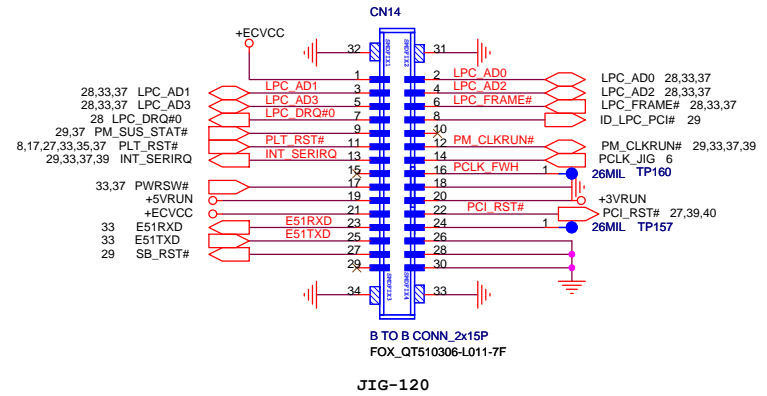
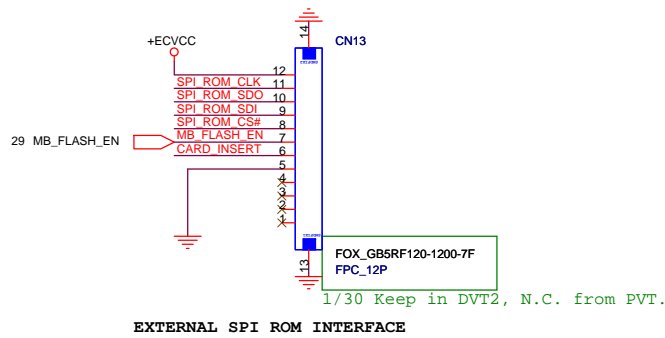
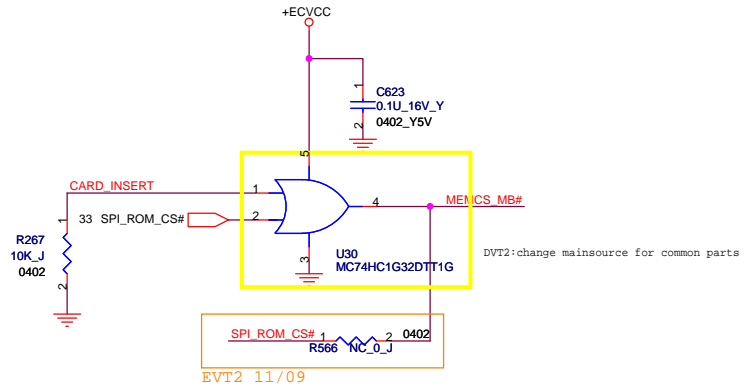
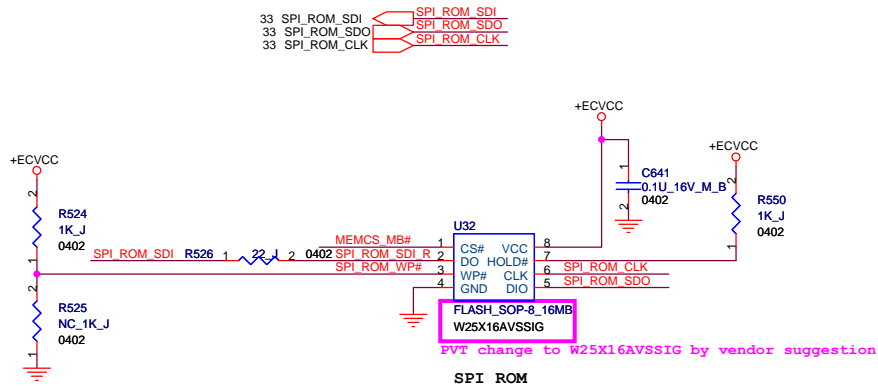


MODEL ID0-1

ID1	ID0	Sku
0	0	UMA
0	1	DISCRETE
		M750

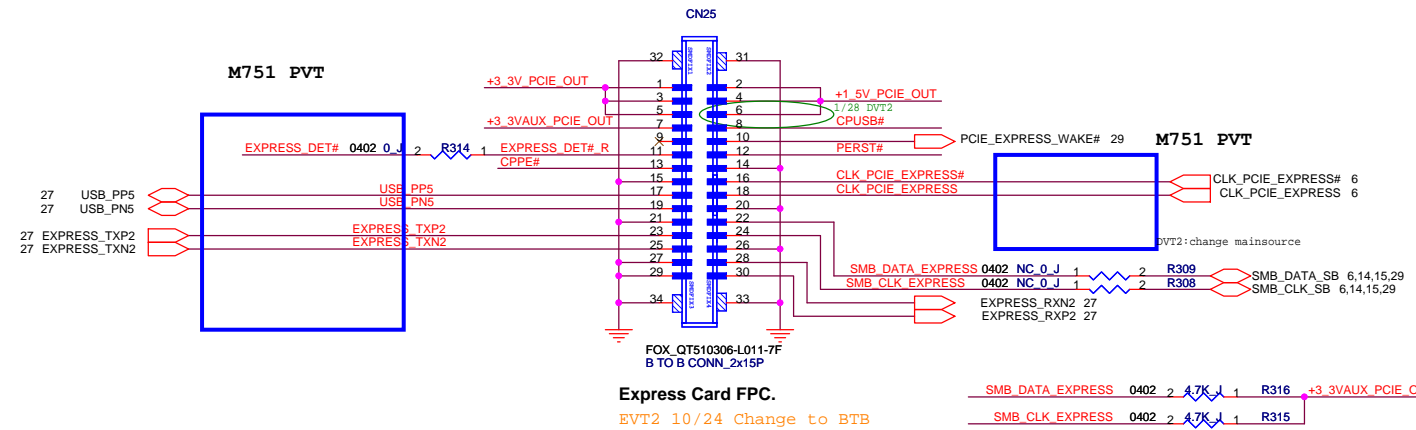
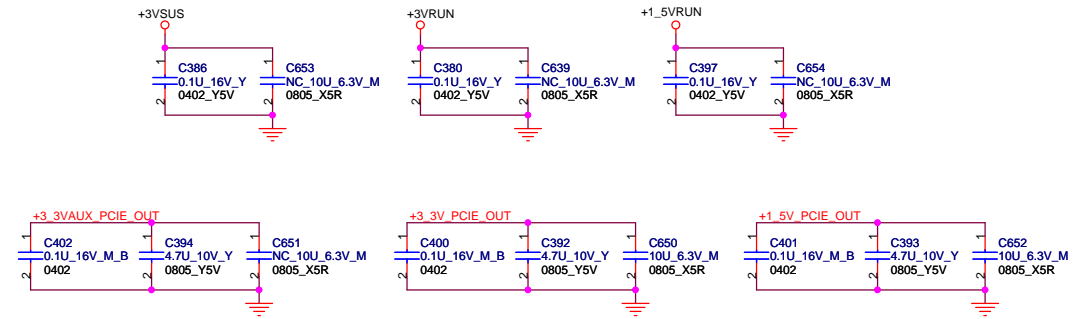
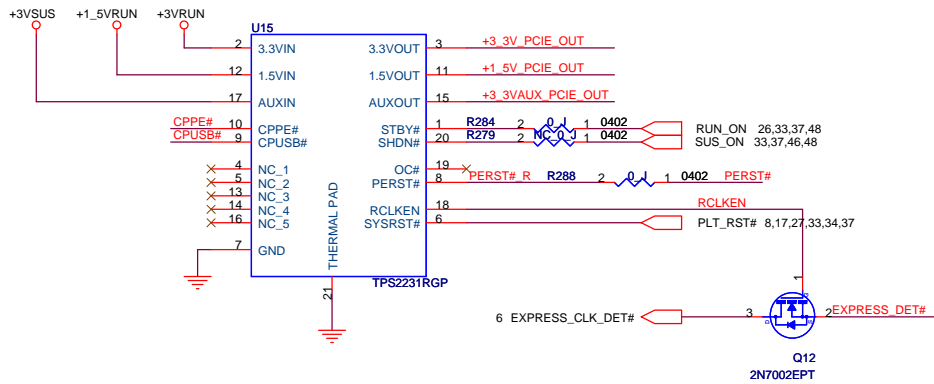
SYSTEM ID0-1

ID1	ID0	MODEL
0	0	M750
0	1	M751
1	0	M752

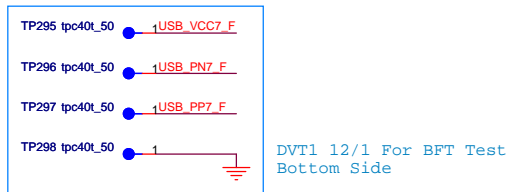
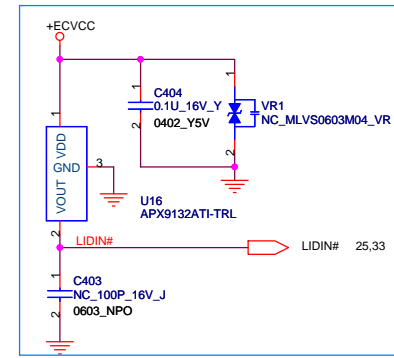
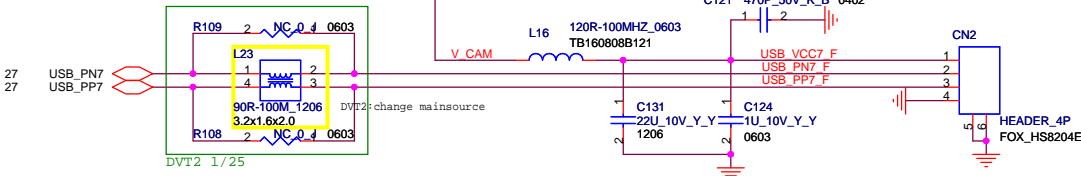
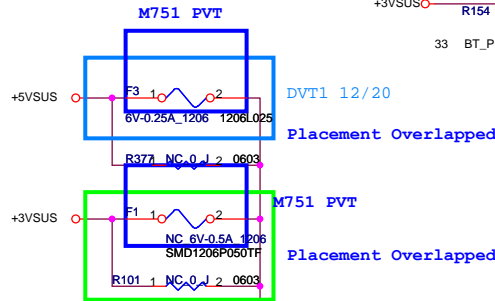
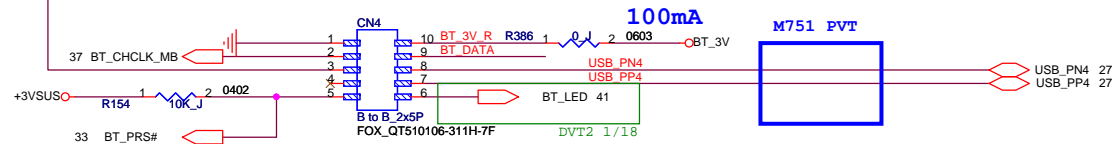
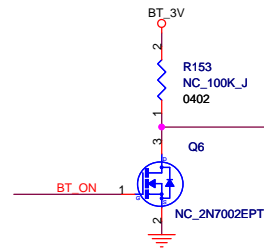
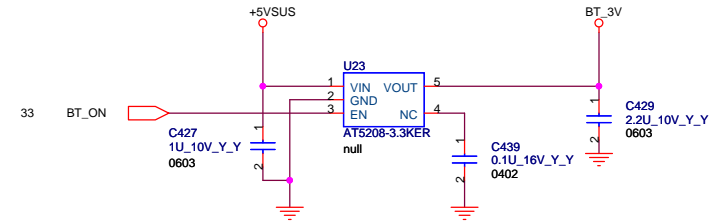
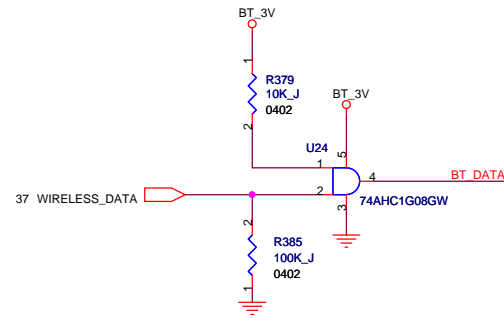


+1_5V=>0.65A
 +3_3VAux=>0.275A
 +3_3V=>1.3A

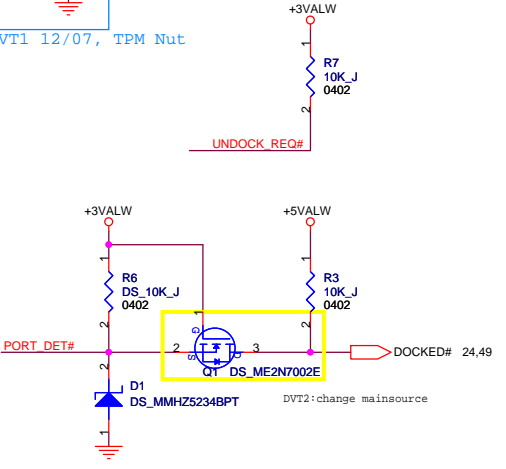
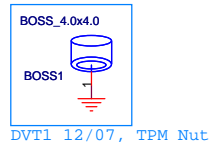
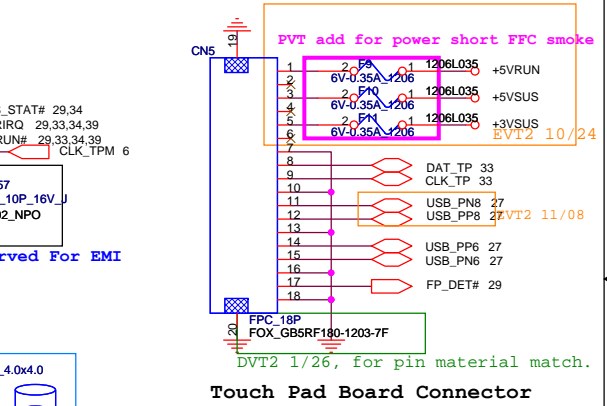
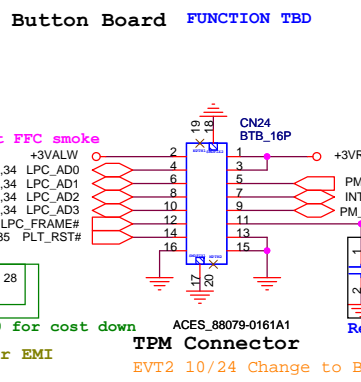
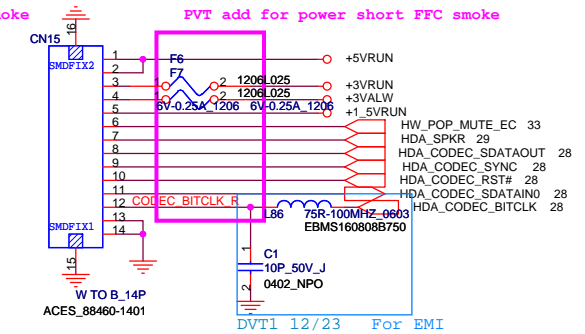
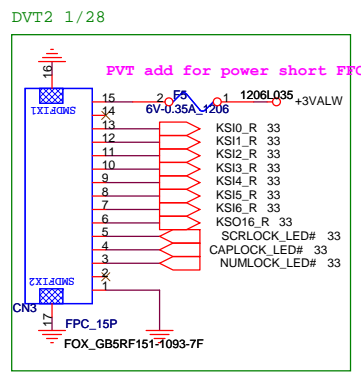
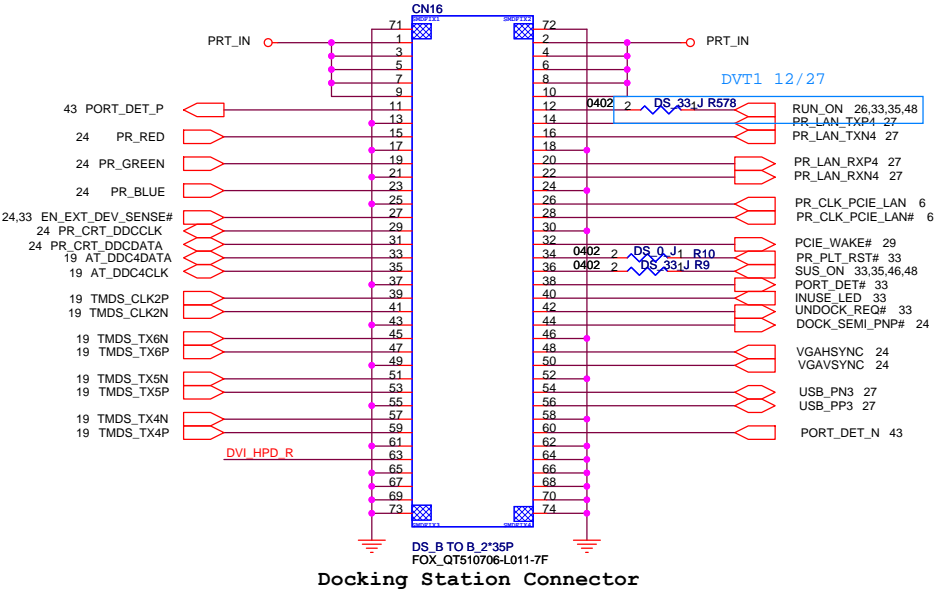
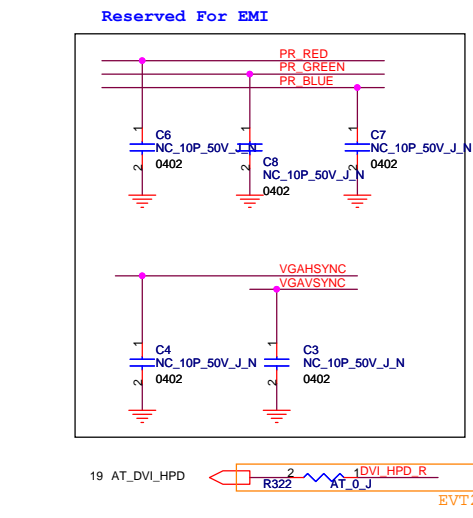
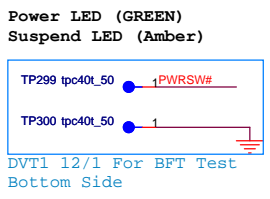
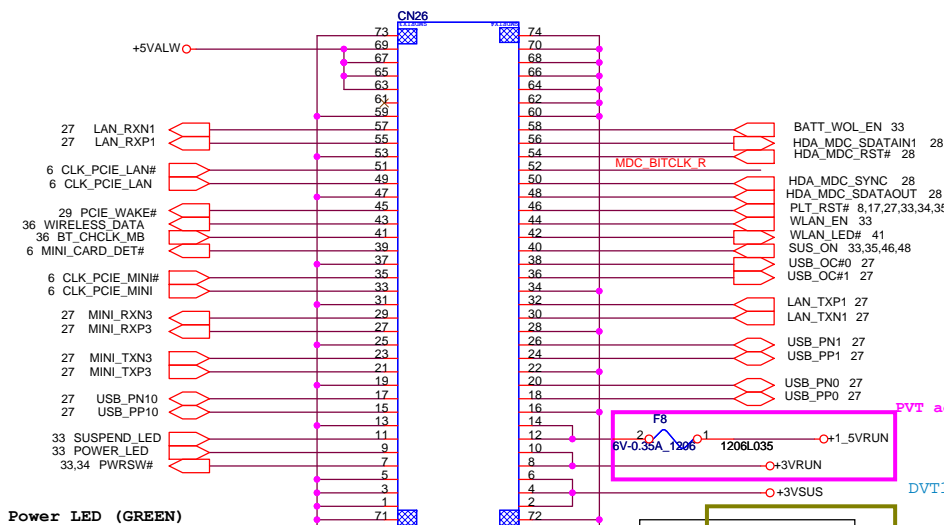
Express Card Power Switch



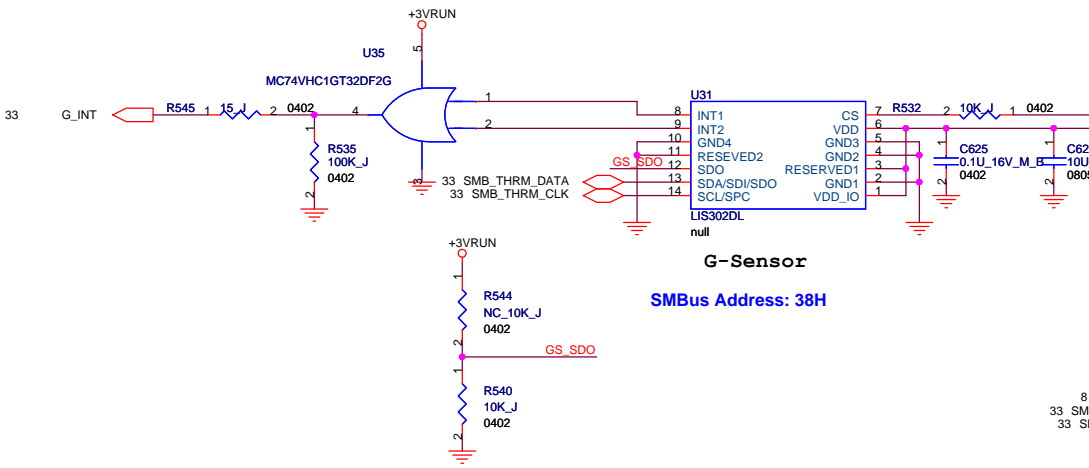
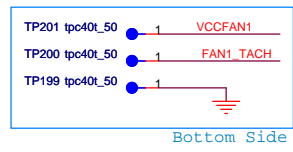
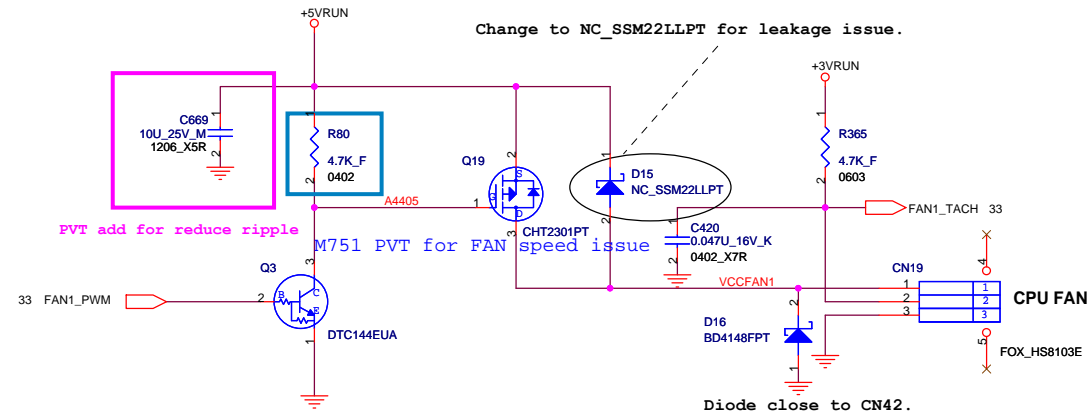
Express Card FPC.
 EVT2 10/24 Change to BTB



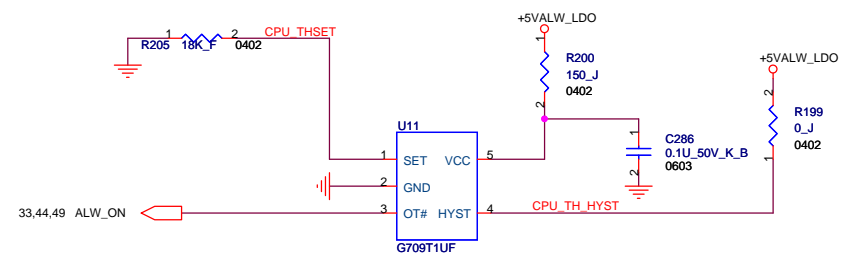
LID Switch



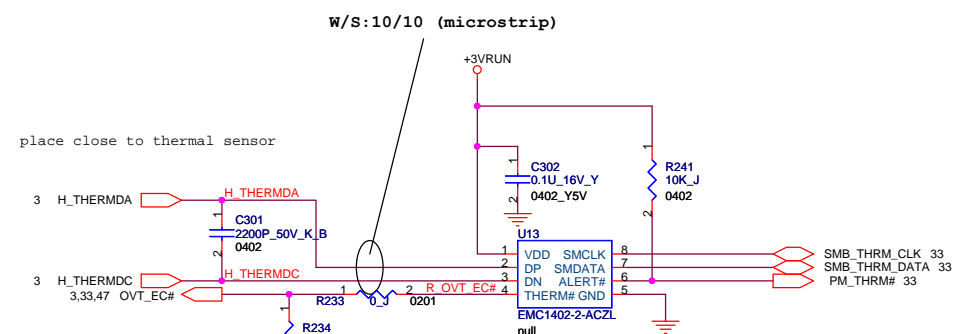
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DB connector & Docking			
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 37	of 54	



HW THERMAL PROTECTION



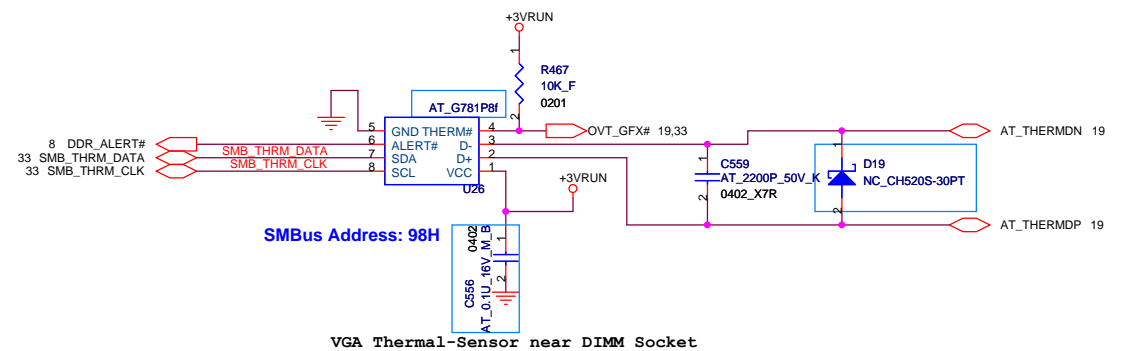
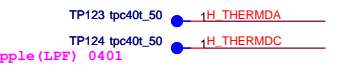
HW thermal shut down temperature setting 95 degree . Put Near CPU .

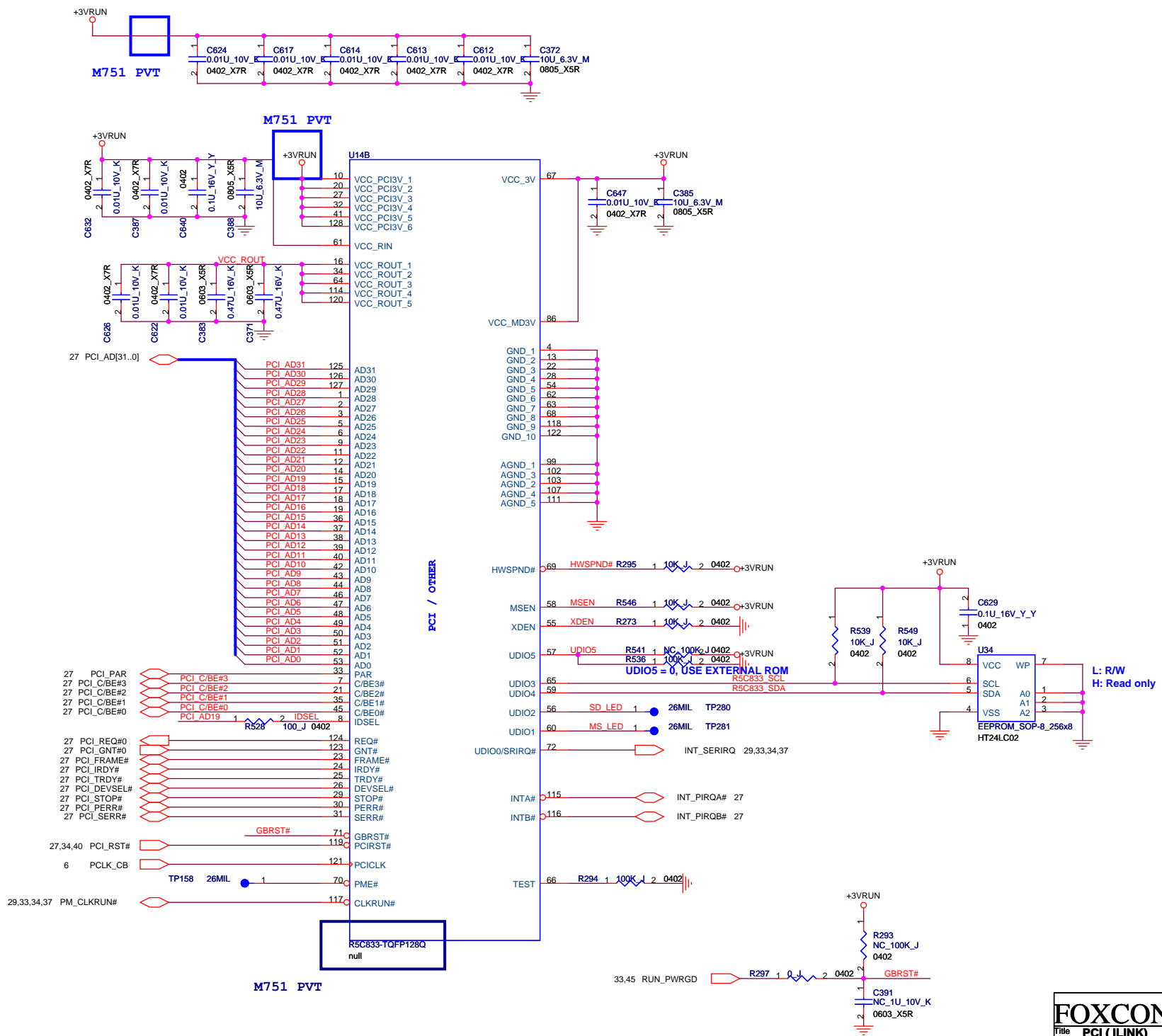


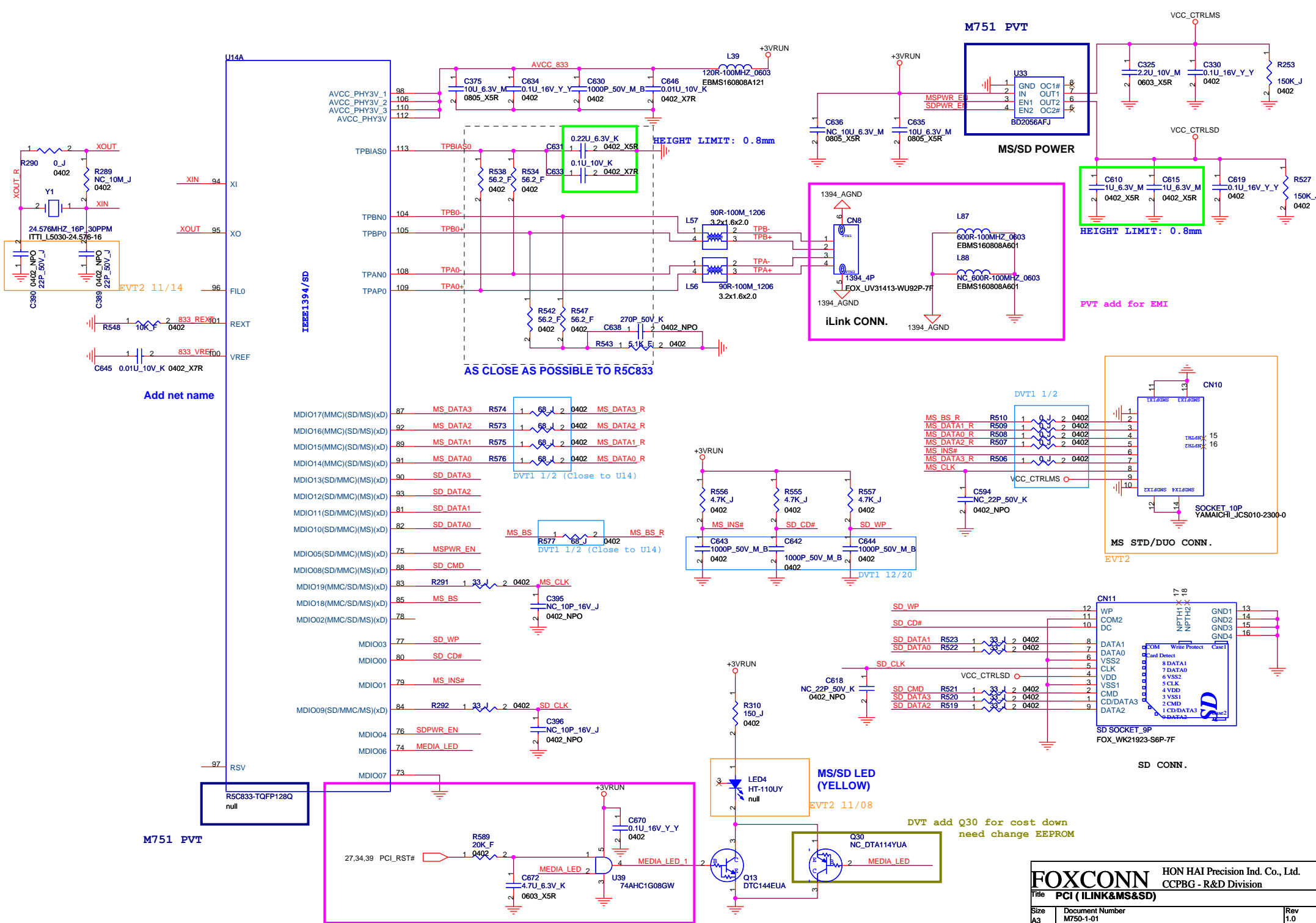
SMBus Address: 9AH

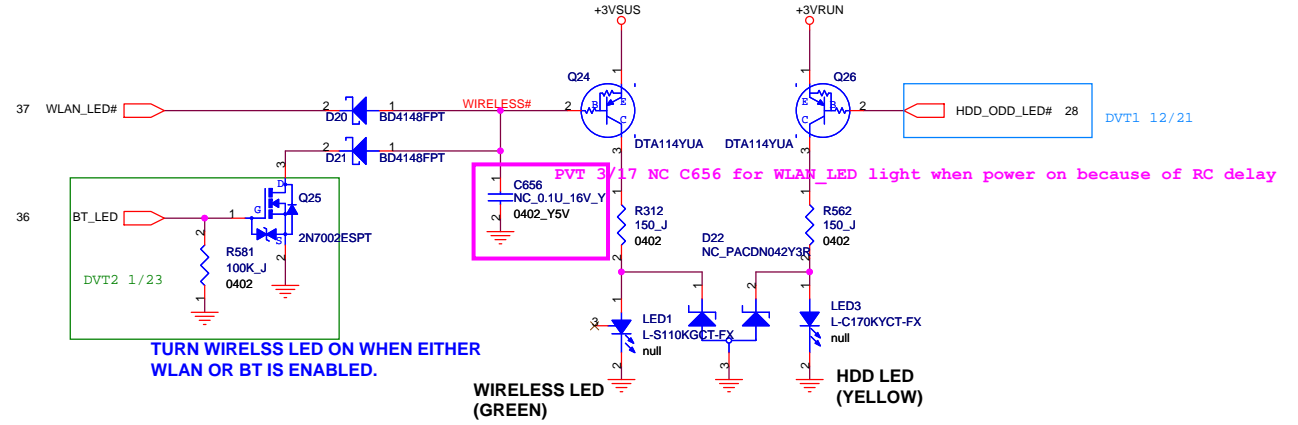
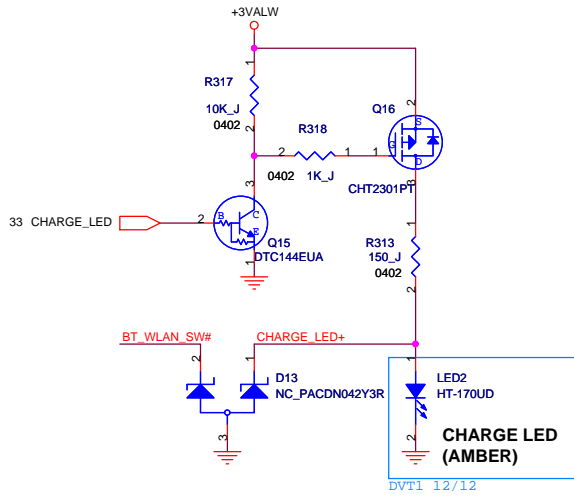
CPU Thermal-Sensor

Place Thermal-Sensor near GMCH.

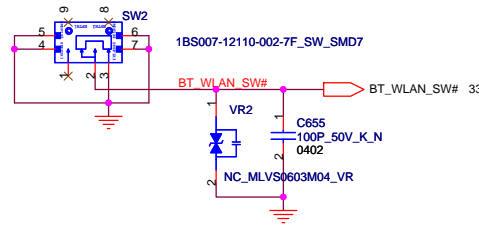


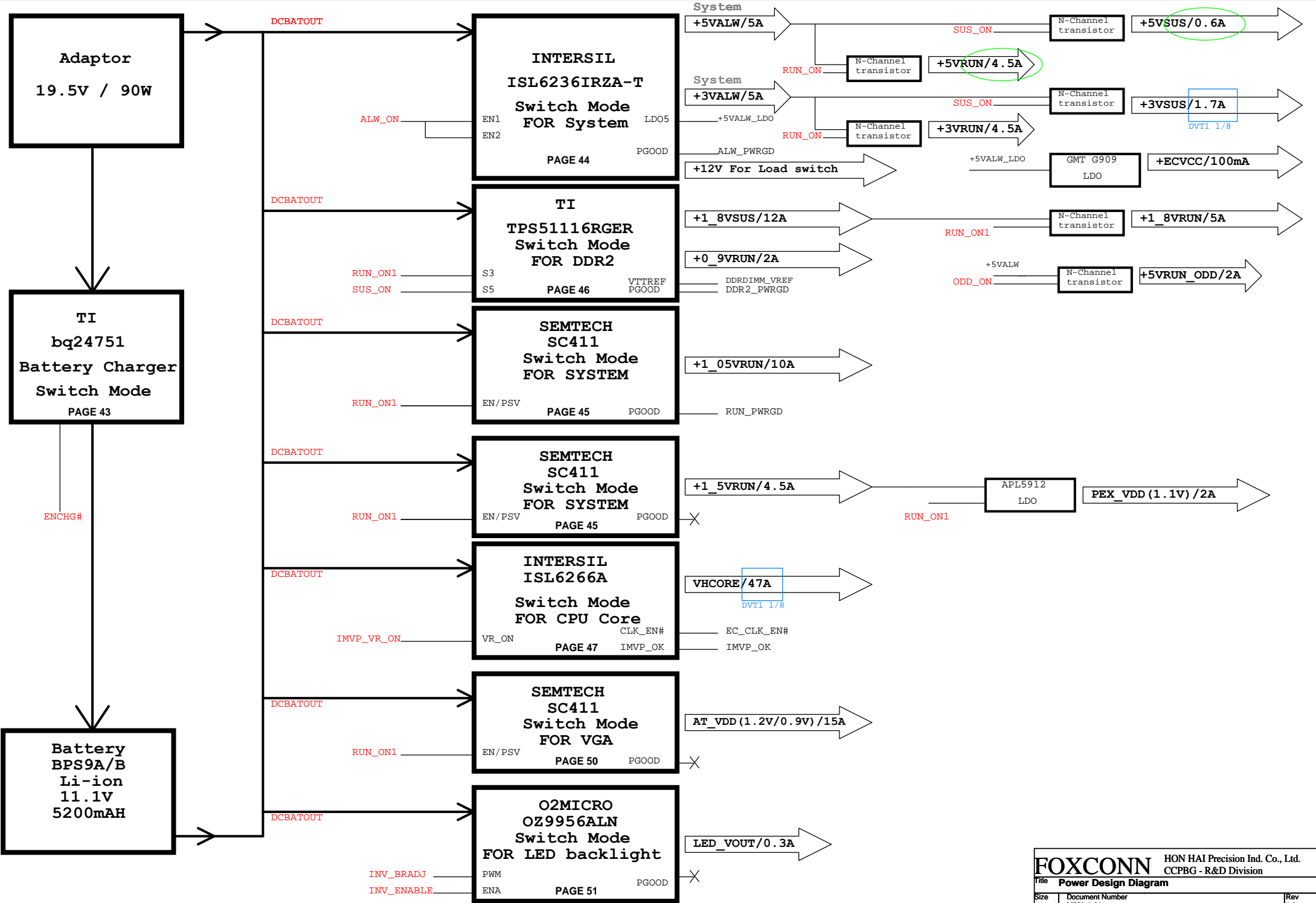


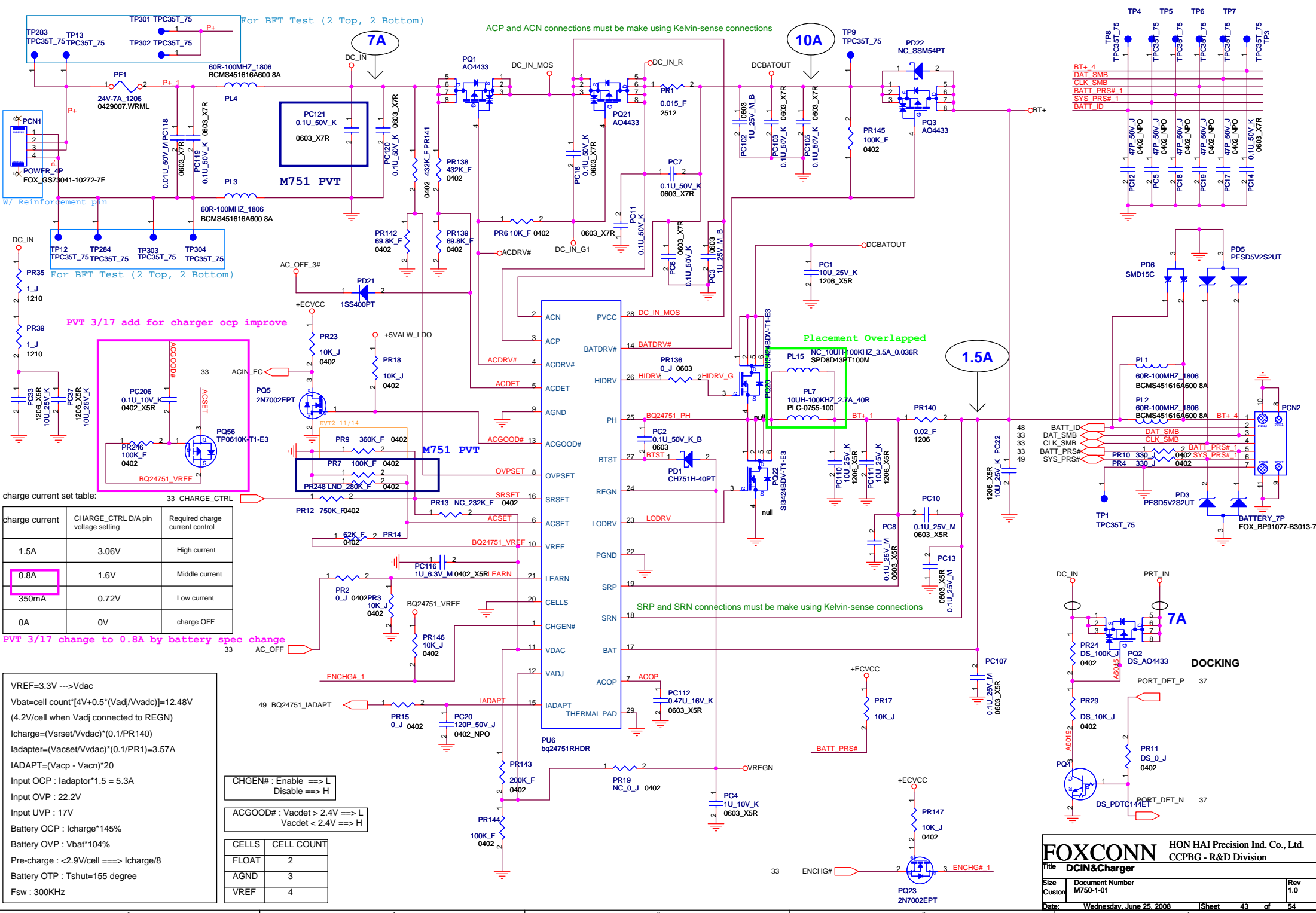




WLAN/BT ON/OFF SWITCH







For BFT Test (2 Top, 2 Bottom)

ACP and ACN connections must be made using Kelvin-sense connections

W/ Reinforcement pin

For BFT Test (2 Top, 2 Bottom)

PVT 3/17 add for charger ocp improve

Placement Overlapped

charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

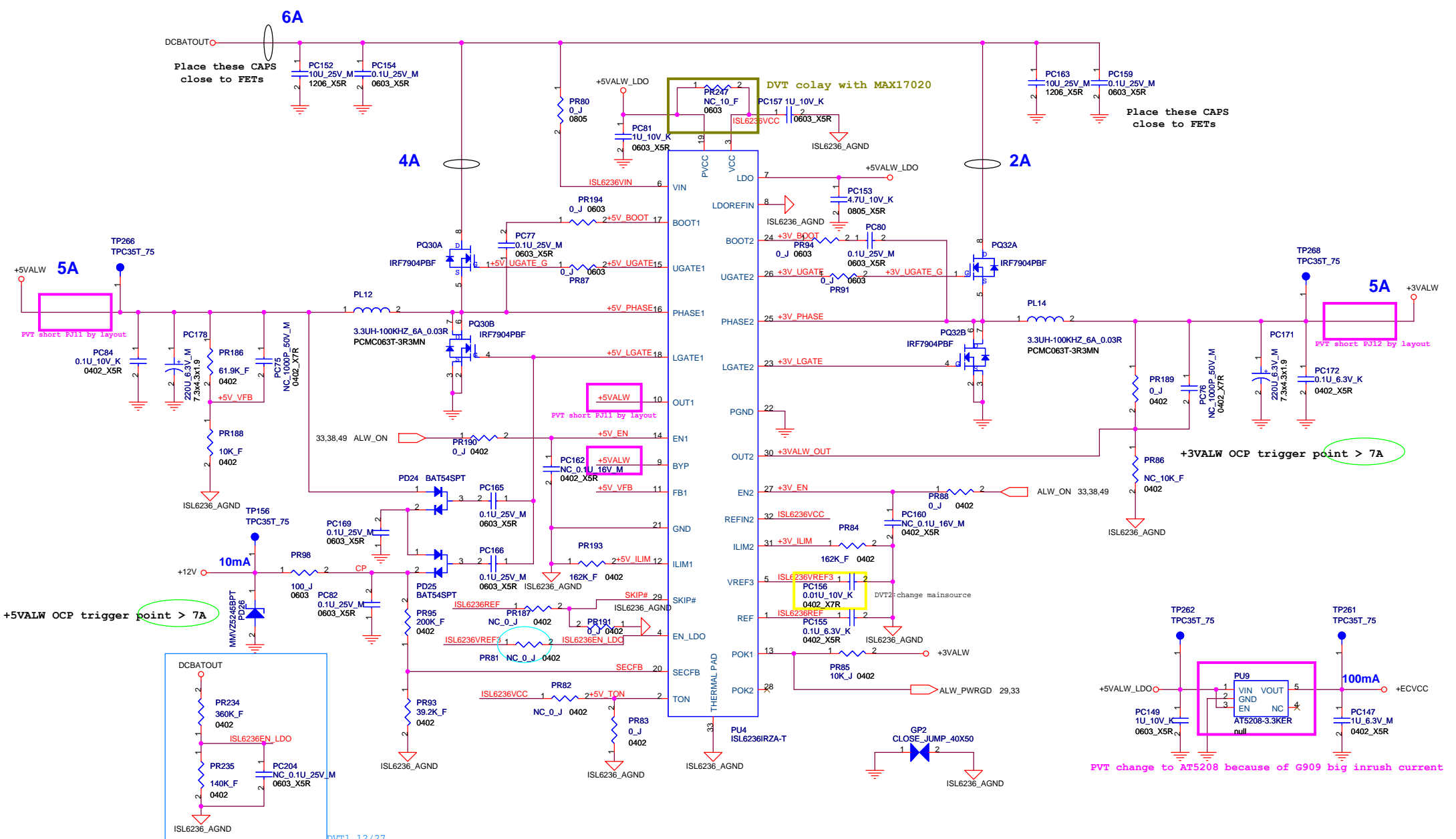
PVT 3/17 change to 0.8A by battery spec change

VREF=3.3V ---> Vdac
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vadc})] = 12.48V$
 (4.2V/cell when Vadj connected to REGN)
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR140)$
 $I_{adaptor} = (V_{acset} / V_{vdac}) * (0.1 / PR1) = 3.57A$
 $IADAPT = (V_{acp} - V_{vacn}) * 20$
 Input OCP : $I_{adaptor} * 1.5 = 5.3A$
 Input OVP : 22.2V
 Input UVP : 17V
 Battery OCP : $I_{charge} * 145\%$
 Battery OVP : $2.9V * 104\%$
 Pre-charge : $< 2.9V / \text{cell} \implies I_{charge} / 8$
 Battery OTP : $T_{shut} = 155 \text{ degree}$
 $F_{sw} = 300KHz$

CHGEN# : Enable ==> L
 Disable ==> H

ACGOOD# : $V_{acdet} > 2.4V \implies L$
 $V_{acdet} < 2.4V \implies H$

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4



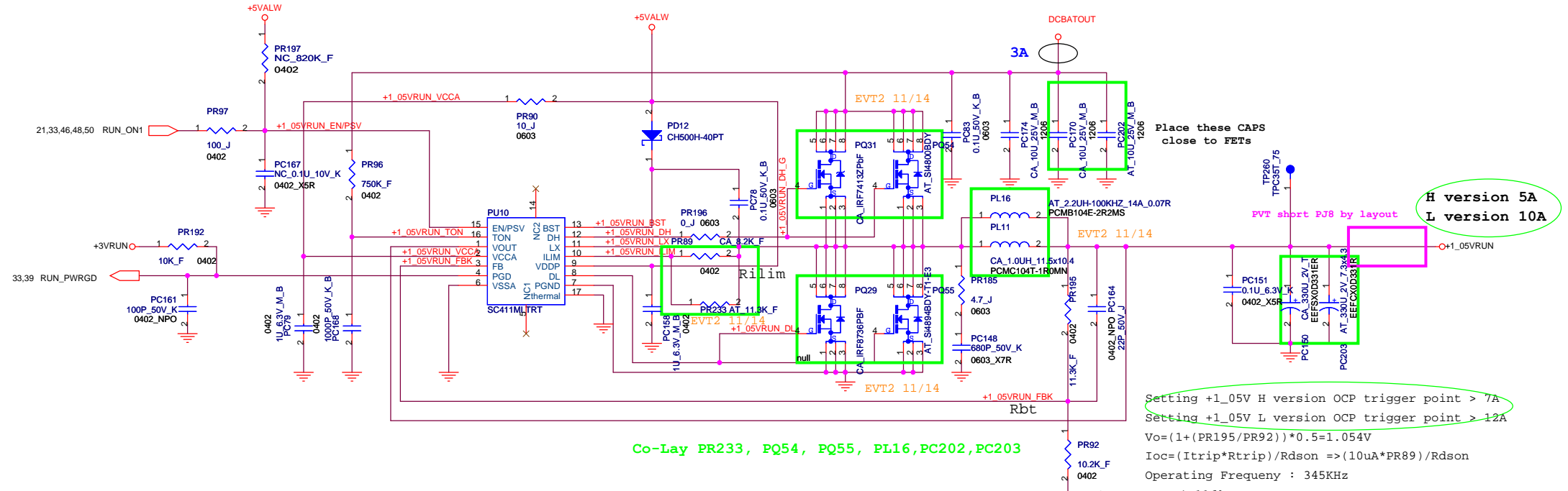
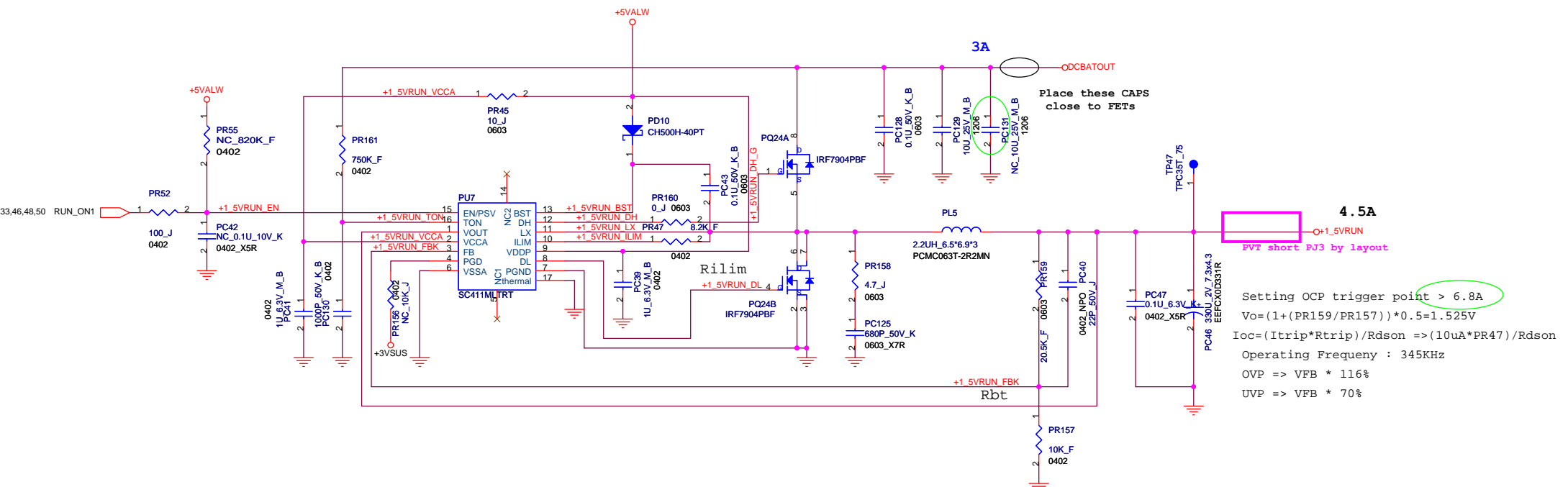
TON	Operating Freqence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

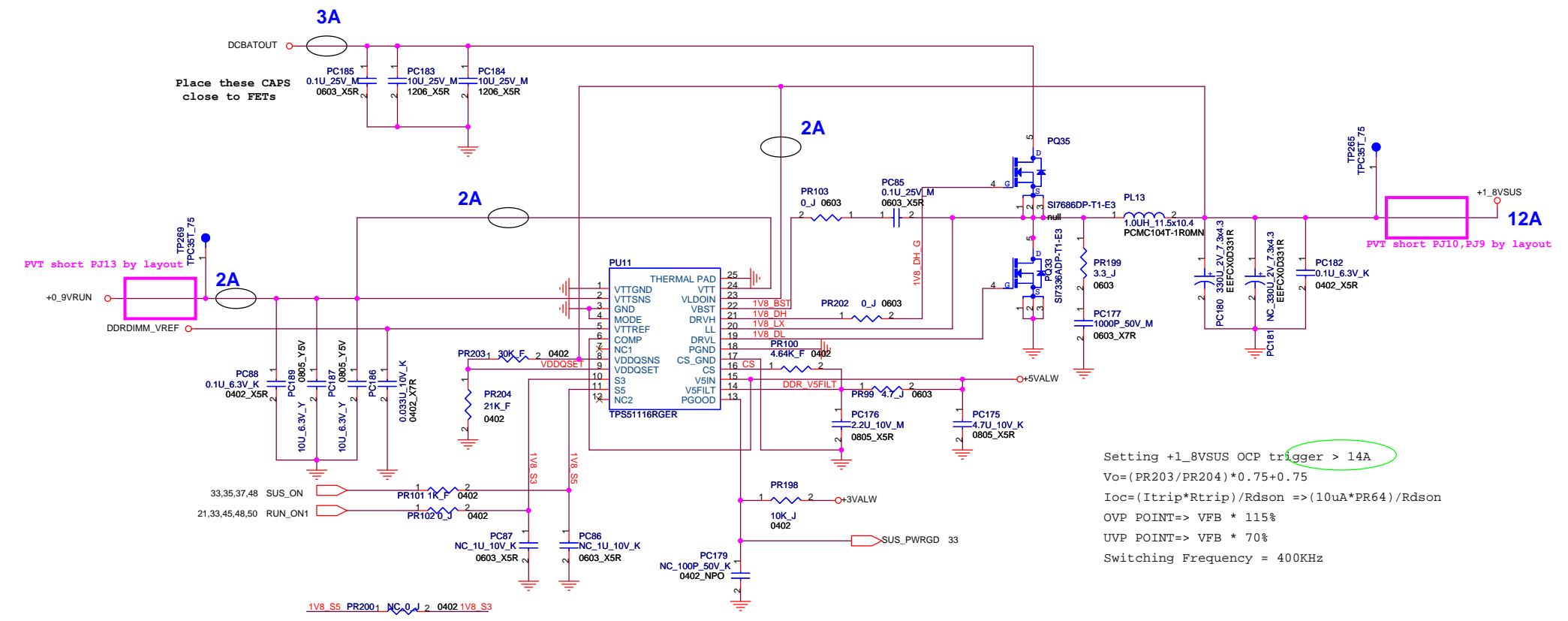
SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / (VIN * F * LIR * ILOAD(MAX))$$

$$Rocp = (Iocp - Iripple/2) * (10 * Rds(on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) * VFB1$$





Setting +1_8VSUS OCP trigger > 14A

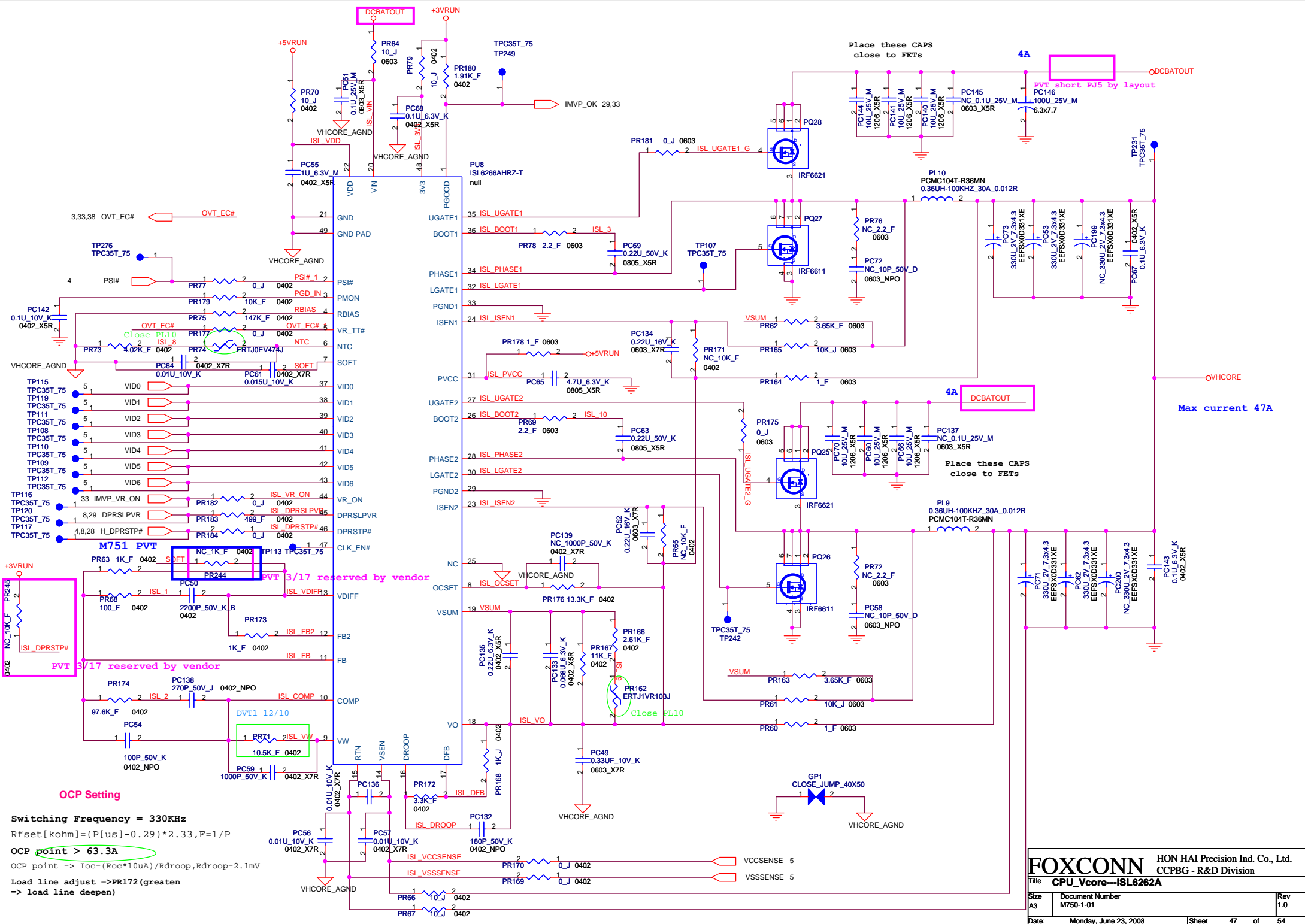
$$V_o = (PR203/PR204) * 0.75 + 0.75$$

$$I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR64) / R_{dson}$$

OVP POINT => VFB * 115%

UVP POINT => VFB * 70%

Switching Frequency = 400KHz



3.33,38 OVT_EC#

TP276 TPC35T_75

TP115 TPC35T_75

TP119 TPC35T_75

TP111 TPC35T_75

TP108 TPC35T_75

TP110 TPC35T_75

TP109 TPC35T_75

TP112 TPC35T_75

TP116 TPC35T_75

TP120 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

TP117 TPC35T_75

OCP Setting

Switching Frequency = 330KHz

$$R_{fset}[kohm] = (P_{us} - 0.29) * 2.33, F = 1/P$$

OCP point > 63.3A

OCP point => $I_{oc} = (R_{oc} * 10uA) / R_{droop}$, $R_{droop} = 2.1mV$

Load line adjust => PR172 (greaten => load line deepen)

Place these CAPS close to FETs

4A

PVT short PJ5 by layout
PC146 NC 0.1U_25V_M
100U_25V_M
6.3x7.7

OVCBATOUT

Max current 47A

4A

4A

4A

4A

4A

4A

4A

4A

4A

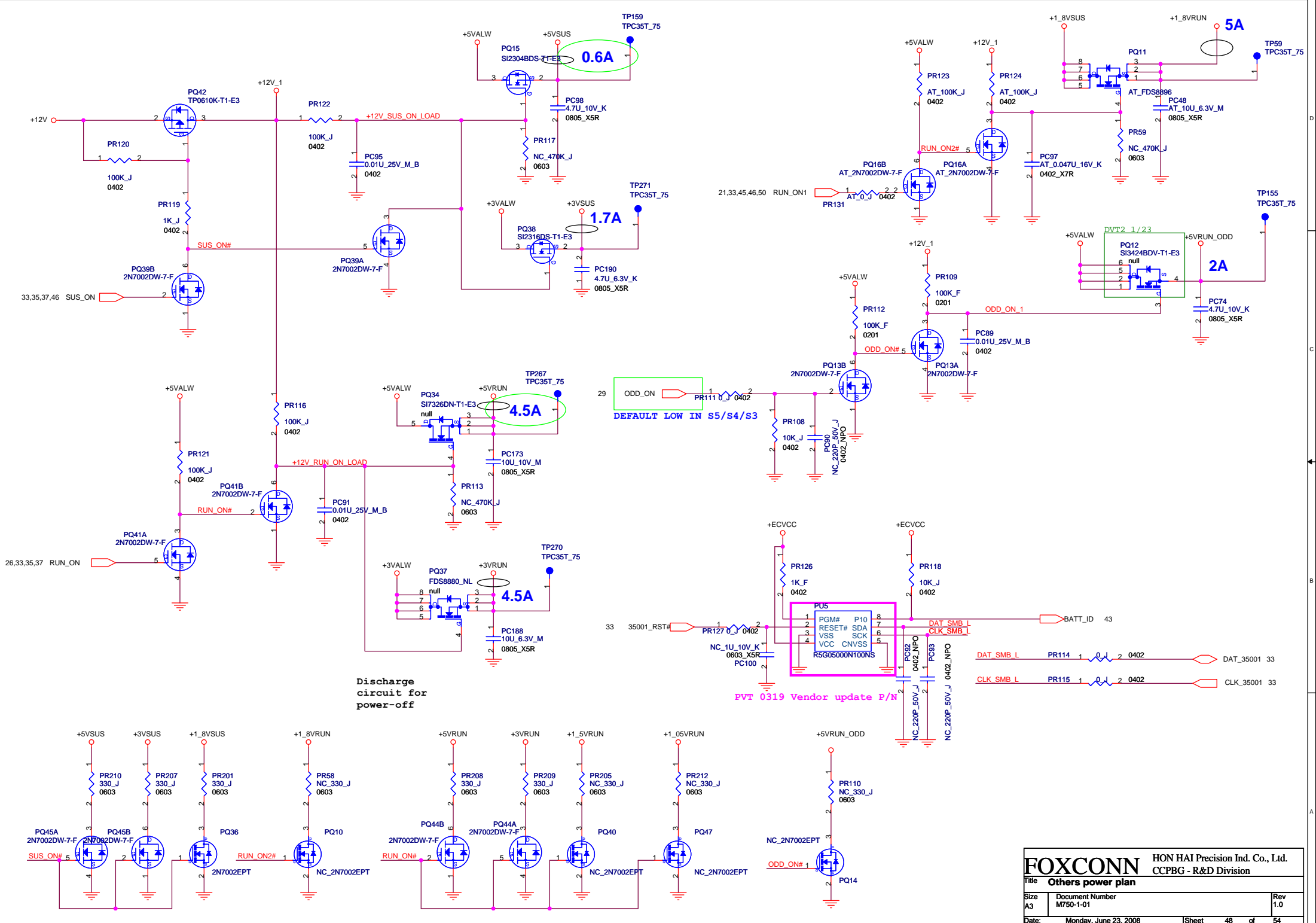
4A

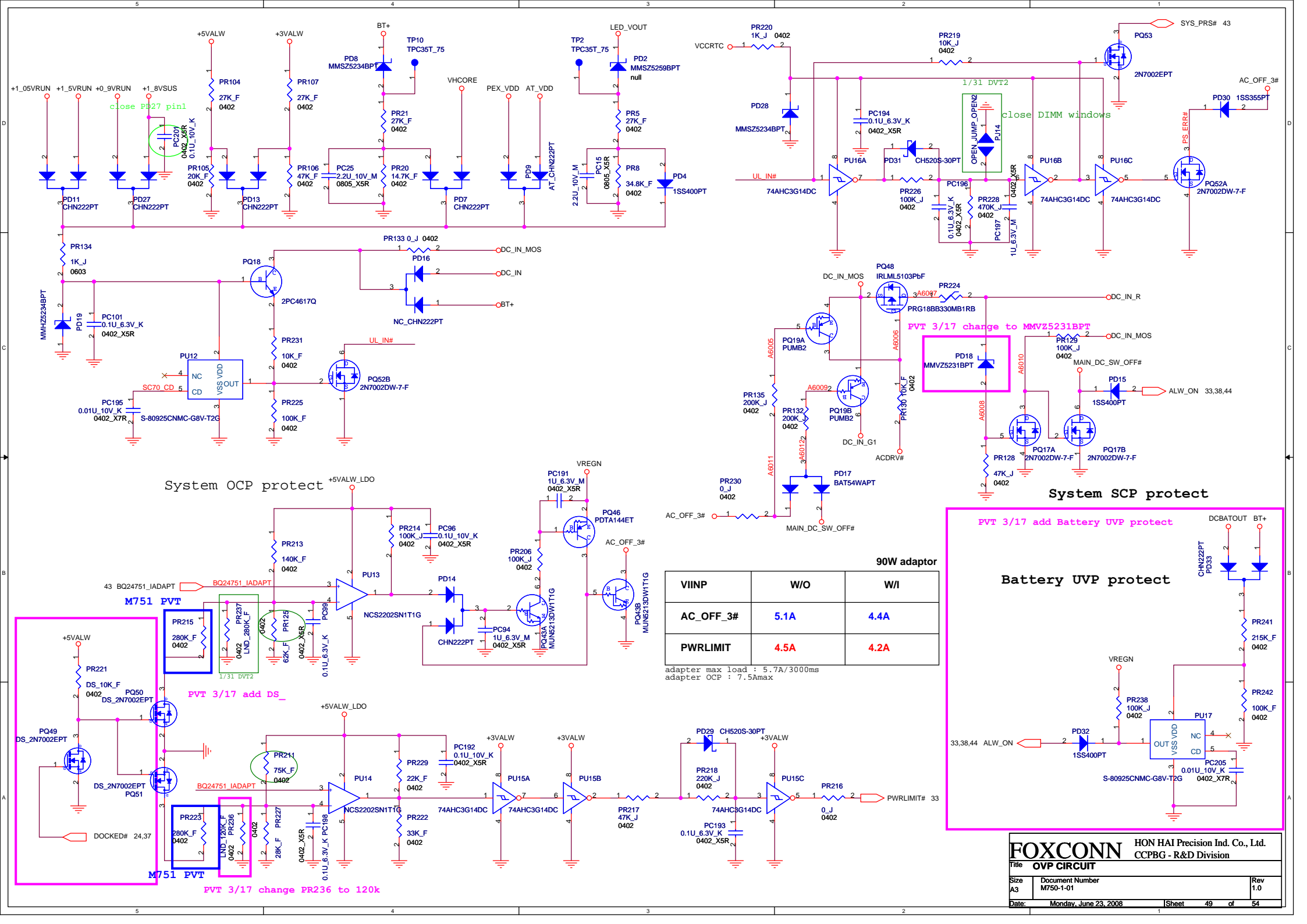
4A

4A

4A

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title CPU_Vcore-ISL6262A			
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 47	of 54	





System OCP protect

System SCP protect

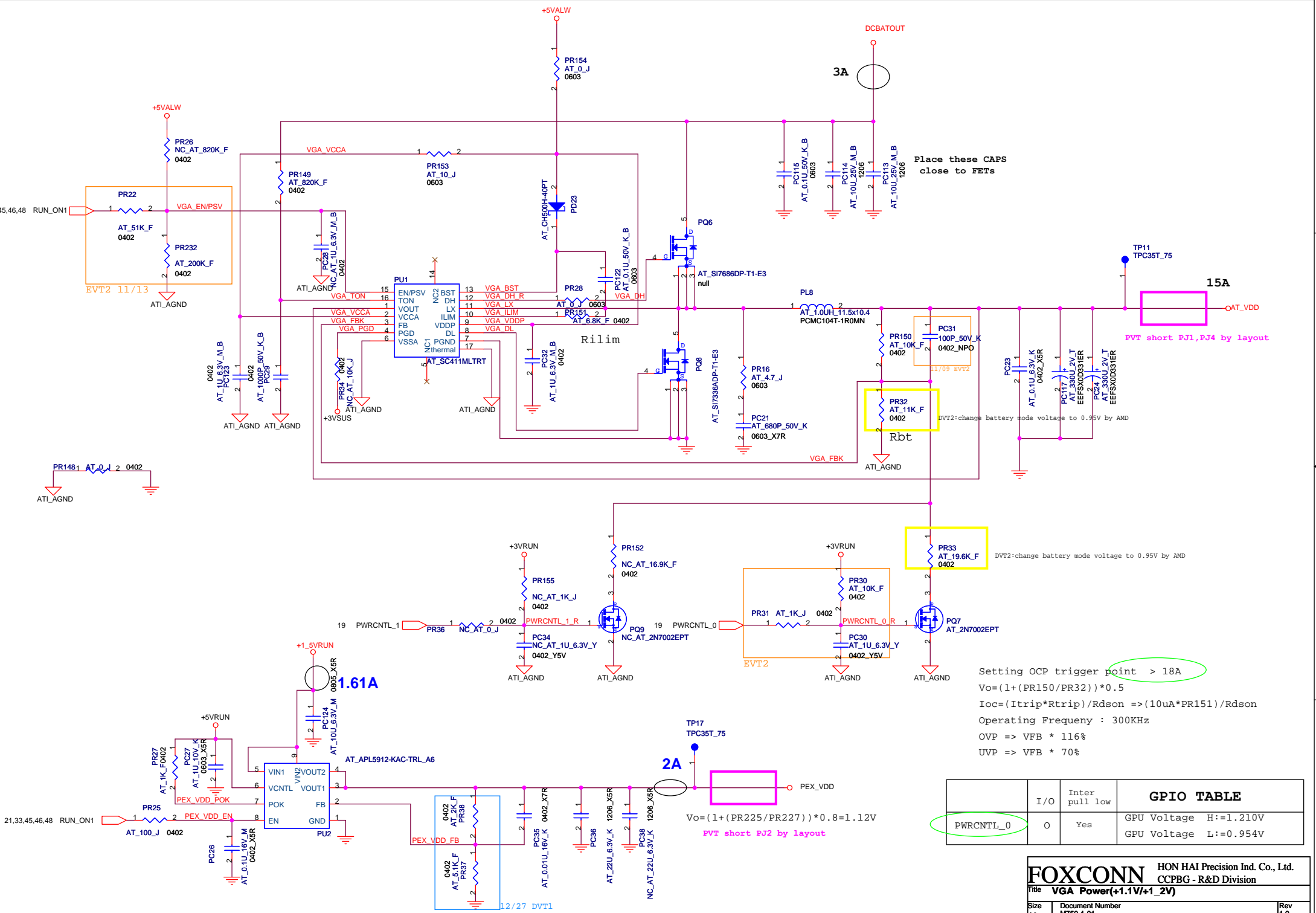
PVT 3/17 add Battery UVP protect

90W adaptor

VIINP	W/O	W/I
AC_OFF_3#	5.1A	4.4A
PWRLIMIT	4.5A	4.2A

adapter max load : 5.7A/3000ms
 adapter OCP : 7.5Amax

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division



Place these CAPS close to FETs

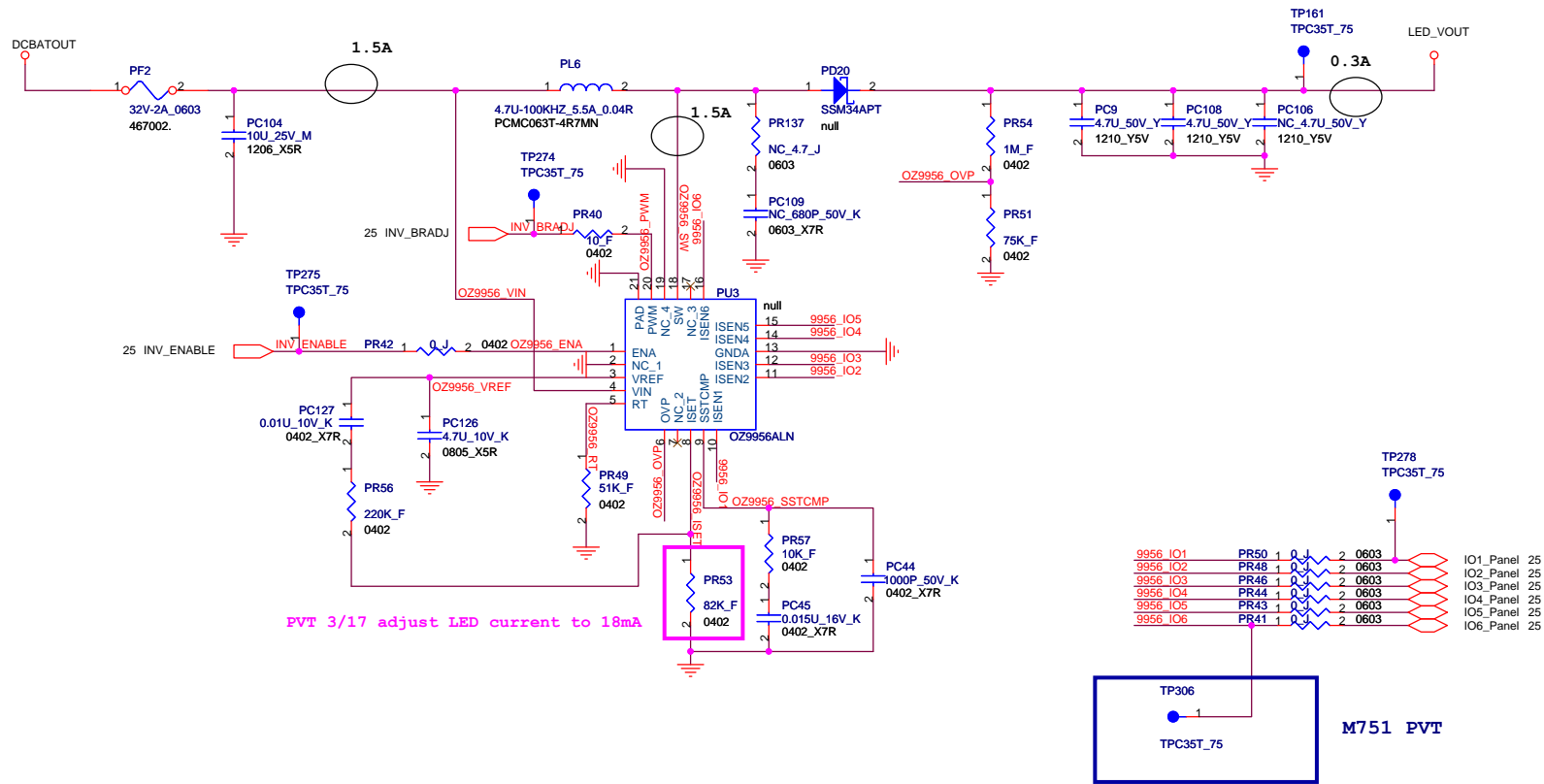
PVT short PJ1, PJ4 by layout

DVT2: change battery mode voltage to 0.95V by AMD

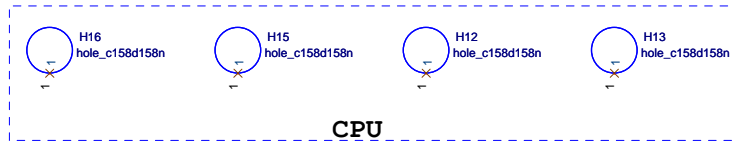
Setting OCP trigger point > 18A

$V_o = (1 + (PR150/PR32)) * 0.5$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR151) / R_{dson}$
 Operating Frequency : 300KHz
 OVP $\Rightarrow V_{FB} * 116\%$
 UVP $\Rightarrow V_{FB} * 70\%$

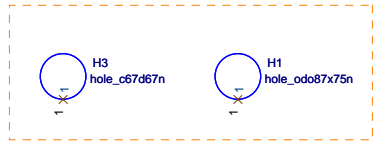
GPIO TABLE		
I/O	Inter pull low	GPU Voltage H: =1.210V GPU Voltage L: =0.954V
PWRCNTL_0	0	Yes



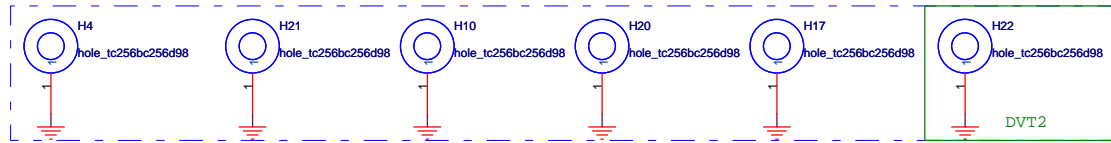
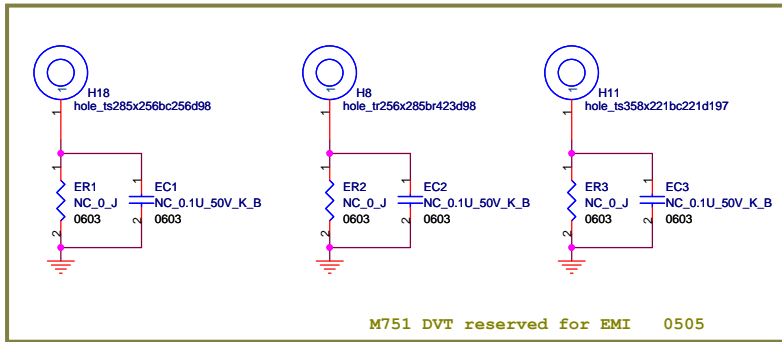
9956_IO1	PR50	1	0	2	0603	IO1_Panel	25
9956_IO2	PR48	1	0	2	0603	IO2_Panel	25
9956_IO3	PR46	1	0	2	0603	IO3_Panel	25
9956_IO4	PR44	1	0	2	0603	IO4_Panel	25
9956_IO5	PR43	1	0	2	0603	IO5_Panel	25
9956_IO6	PR41	1	0	2	0603	IO6_Panel	25



CPU

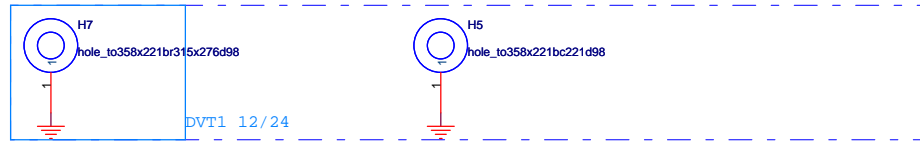


EVT2 11/10 Guide Pin Hole



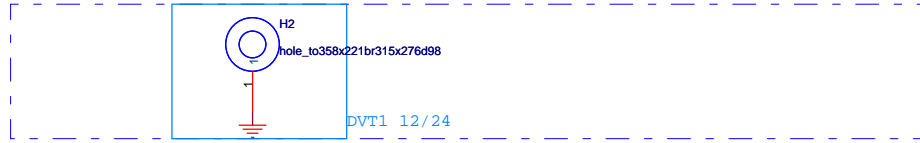
DVT2

TYPE A



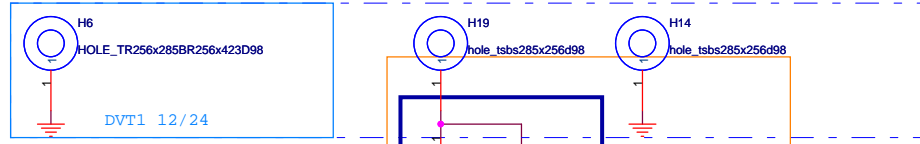
DVT1 12/24

TYPE C



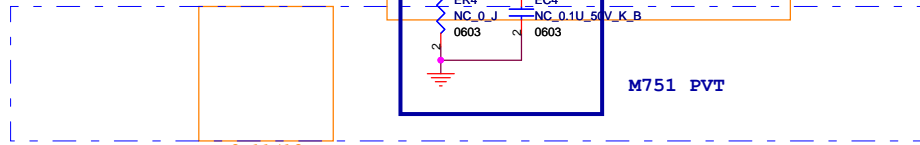
DVT1 12/24

TYPE G



DVT1 12/24

TYPE J



M751 PVT

TYPE O

EVT2 11/12

Mainboard

10/12
Change color of MS/SD/HDD LED.
Mount R419, R414, R420, R421.
10/13
SYSTEM_ID, MODEL_ID definition update.
10/20
CPU 22uF CAP N.C. parts location change.
N.C. R101 For EVT2 (Use +5V type camera module)
10/24
Move PCI Express pair of LAN from port5 to port1.
10/29
Change PR9 to 422K.
Add PL15 and PL7 co-lay.
Modify charge current setting table.
Mount PR83.
PL11 change to 1uH.
Add TP276 test point.
Add PC201 0.1uF and close to PD27 pin1.
Change PL6 to 4.7uH and add TP274,TP275 test points.
10/30
Refer to PUR suggestoin to change component source.
Add NC_PR232
Change PR30 to 10K and PR31 to 1K.
Mount PC30
Add TP278 test point.
10/31
Refer to PUR suggestoin to change component source.
Swap LVDS group of ATI M82.
11/02
Change "*" to net "EN_EXT_DEV_SENSE" for low active.
Modify MB Semi-PNP circuit.
11/03
Inverse HDMI pairs polarity(DVI pairs inversed on docking side).
11/04
Change USB board connector.
Combine MS/SD LED to one(MEDIA_LED).
11/05
N.C. R377, Mount F3.
Change INUSE_LED to GPIO72.
Change MS slot to YAMAICHI JCS010-2300-0.
11/06
Change part of CN16/CN26.(Height Change)
Change netname of "SD_WP#" to "SD_WP".
Change PR143 to 200kohm.
Update charge current setting table.
Reserve BATT_WOL_EN for LAN wake up enable/disable in battery mode.
11/07
C453, C452, C451,C426, C425, C424 change size to 0402.
Mount PR158, PC125 and PR185, PC148 and PR199, PC177 and PR16, PC21.
N.C. PR36.
Change C188 from 0.1uF to 0.47uF.
11/08
Swap USB_PP8/PN8 for ease of routing.
Change button board connector to WBF31326-F04TR.
Change MS/SD LED to side view, yellow color.
Change U7 from CM2009 to CM2006.
Update VCC_DDC power isolation circuit.
Add R565,C658 for SRTCST#.
11/09
Change PC31 from 22p to 100p.
Reserve R566 for removal of Ext. SPI Conn on DVT.
Reverse Button Brd CN pin assignment.
Add EMI Cap C659-C666 on +1_8VSUS.
11/10
Delete guide pin hole H9, H22.
N.C. F3, mount P1. (Use +3VSUS for camera power on EVT2).
11/11
Change pin assignment of Express CN.

11/12
Change PTH hole size. (H11)
Add TP283,TP284.
Change net name "ISL_VSSSENSE_" to "ISL_VSSSENSE".
11/13
Add TP285-290 for SI probe point.
Change type of H14,H19.
Change PR22=51K, PR232=200k.
11/14
Tune crystal accuracy, change C390/C389/C416/C412 to 22PF,C648/C649 to 18PF.
Change PR6=360K.(Charge Current Control)
Co-Lay PR233, PQ54, PQ55, PL16.
Change RP34 to 2.2K for SI.
N.C. R415, mount L47 on H model.
11/19
N.C. R559 (Double pull up on BT_PRS#)
11/23
Change camera power to +5VSUS.
DVT1 12/01
Swap DVI bus polarity.
Route RUN_ON to docking station CN.
Add logic gate(U37) to prevent panel flash when boot up.
Add R567, bypass brightness control signal.
Use +3V_DELAY(Q4) to prevent M82 high pulse on LCD control signals.
12/07
Change DC-IN CN(PCN1, With Reinforcement Pin).
Swap TPM Nut (BOSS1).
Add R570 for power consumption measurement.
12/12
Change U6 from Quad to Dual XOR gate.
Change EMI Caps C424-C426, C451-453 to 10pF.
Change color of LED2(Charge LED) to Amber.
Change U16 from MR-sensor to Hall-sensor. (N.C. R263)
12/13
Change damping resistors of keyboard matrix to 120ohm Ferrite bead.(For EMI)
12/17
Change C451,C452,C453,C424,C425,C451 to 22pF. (For EMI)
Add one more +3VSUS (CN26) for WLAN module to cover 1500mA(peak)/1100mA(normal) requirement.
12/18
Add one more LCDVCC pin (CN1) for panel to improve voltage drop.
Add optional resistors(R571,R572) for gamma control.
Reduce LED_VOUT from 6 pins to 2 pins.
12/20
Change net "BL_OFF" to "BL_OFF#".
Add R573-577 to improve MS signal overshoot/undershoot.
Mount C642-644.
Change F3 to 0.25A.
12/21
Change Net "HDD_LED#" to "HDD_ODD_LED#"
12/23
Change C412/C416 from 22pF to 10pF.
Change C648,C649 from 18pF to 15pF.
Mount U26(VGA Thermal Sensor) on H model only.
Add 75 ohm bead, 10pF capacitor on HDA_MDC_BITCLK/HDA_CODECD_BITCLK for EMI.
12/24
Update H2/H6/H7/H8 footprint.
Delete R563, R564 (CPL_GND).
Change D17, D18 to SSM22 to reduce voltage drop.
Change pull up voltage of R360/R361 to +3VRUN. (Only Strap/GPIO pin connected to +3V_DELAY)
N.C. C403 (Not necessary for ESD)
12/26
Delete ODD_DP# connection to ICH9M.

12/27
Add PC204 for noise filtering.
Add R578 for protection.
Change U27 from RClamp0514 to RClamp0524.
N.C. SW1, R134,R141
Change PR38 to 2K, PR37 to 5.1K.
12/28
N.C. U4 shunt regulator to reduce S4 consumption.
Mount R131, N.C. R129.
Reserve LDO (U38) for 1.5V type VCCSUSHDA.
Add R579,R580 to avoid floating on input pin.
1/2
N.C. C451-453, C424-426.
N.C. PC204.
Add prefix AT_ on R322, R51.
Change damping resistor value of MS card.
(R573-577 from 33 to 68 ohm)
(R506-510 from 33 to 0 ohm)
Change L30-32 to 27mH inductor.
Change C258,260,262 to 2.2pF.
Change revision of clock generator(U29) to Rev.B
1/5
Change D2/D3 to low capacitance type.
Fine tune delay timing. Change R19/R565 to 13K.
1/8
Update power design spec.
VCore: 47A, +3VSUS: 1.7A.
DVT2
1/15
Update power budget of VCCHDA,VCCSUSHDA,VCCDMI,VCC1_5_A
Add GND pin on C130.2
1/21
Add BT_LED on CM4.6
Update WIRELESS LED circuit. Page41.
1/21
Add screw hole H22.
Add D23, D24 for leakage issue when EC initialization.
Add R460 for Non-Dock Sku.
1/23
PQ12 change to SI3424BDV-T1-E3.
PR125 change to 62Kohm
PR215 change to 205Kohm
PR211 change to 75Kohm
PR223 change to 154Kohm
Add PR237 ND_280Kohm , PR236 ND_154Kohm for Non-Dock sku.
Add pull down resistor (R581) on BT_LED.
1/25
Mount L23, N.C. R108, R109 for EMI.
Change L86 from 75R to 10R for SI.
For Docking sku, add prefix DS_ on value of C257,C259,C261,CN16 D1, PQ2, PQ4, PR11, PR24, PR29, Q1, Q20, Q21, R6, R9, R10, R165, R167, R416 R444, R578, U8, U9, U10.
1/26
Change R176 from 54.9 to 649 Ohm.
Del L48, Add R582, R583 (N.C.)
Change C413 from 0.1uF to 1uF.
Change CN5 from Gold plated to TIN plated.
1/28
Mount R555, R556, R557.
Add +1.5V_PCIE_OUT on CN25.6 to reduce voltage drop.
Change CN3 from WBF31526-F04TR to GBSRF151-1093-7F.
(Vendor naming rule change, same part.
layout footprint pin reversed)
1/29
Add R584, R585, Q27 to solve DDC capacitance issue.
Add R586 for identification of Dock support.
1/30
Change L86 back to 75R, change L85 from 75R to 10R.
Mount CN13 for software debug on DVT2.
N.C. R572.
Move R321 to U37B.6
1/31
Move PJ14 to PR226.2
Change R176 back to 54.9 ohm.
Add prefix LND on PR36, PR37 for Non-Dock skue for LOW model.
Add PAD1 for EMI Grounding.

0218
M750
change U30 from NC7832M5X(14-NC7832M-5X00) to MC74HC1G32DTT1G(14-MC74HC1-G300)
change D2,D3 from BAS316(16-BAS3160-0000) to BAS316PT(16-BAS316P-T000) for common parts
change D6,D7,D9,D11,D12,D14,D23,D24 from 16-SC5500V-4000 to CH5500H-40PT(16-CH5500H-40P00) for common parts
change Q1,Q5,Q17,Q21,Q22 from 17-2N7002P-T000 to ME2N7002E(17-ME2N700-2E00) for common parts
change Q23 from 17-MMBT390-4001 to PMBT3904.215(17-PMBT390-4200) for common parts
change C303,PC156 from 0.01U_6.3V_K(1C-2B20103-R100) to 0.01U_10V_K(1C-2B20103-K200) for common parts
change L23,L28,L40,L41,L42 from 90R-100MHZ_0R35(1L-FDLW315-N900) to 90R-100M_1206(1L-FWCM321-6F00) for common parts
change C19,C17 from Y5V to X5R tolerance
change PR32 to 11K, PR33 to 19.6k to set the battery mode voltage to 0.95V by AMD for battery mode dual display

0318 PVT
NC C656 for WLAN_LED light when power on because of RC delay
update battery identify (CPU5) P/N to R500500DN10NS by vendor
update U7 symbol to CM2006-02QR
modify R345 value to HD_ for BOM change of disable HDAudio in L28MB SKU
remove PU11,PU12,PU3,PU8,PU10,PU9,PU13,PU5 and short by layout
correct U36 vendor P/N to WPCB775LAADG
change U32 to W25X16AVSSIG by vendor suggestion
add PQ56,PC206,PR246 for charger ocp improve by M760 battery OCP issue
modify P43 charge current table ,middle current change from 1A to 0.8A
add PR244 and PR245(dummy directly) for intersil ISL6266A found C4 hang at the other company
add UVP circuit (PU17,PR238,PD32,PC205,PR242,PR241,PD33)
change PR236 to 120Kohm for power limit point improved
change PQ50,PQ51,PQ49,PR221 value title to DS.
change PR53 to 82Kohm for LED backlight current modify
add R587,Q28,Q29 for improve HDMI voltage drop
0326
Short R31,R32,P34 by layout
add C669 for reduce fan power source ripple
add L87,L88 for EMI
add U39,C670 for MS/SD abnormal behavior
0327
change PU9 to AT5208 because of G909 big inrush current
0328
NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS
add R589,C672 for MS/SD led abnormal when power on
NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS
add R589,C672 for MS/SD led abnormal when power on
reserve R588 for reduce G-sensor power ripple
0402
add F5-F11 for power short
0403
change PR241 from 232K to 215K for UVP circuit improve
0408
NC R348,R356,R357 for using AMD internal SS
change R378 value to HD_ for HDMI disable

M751 DVT
 0505
 Reserve EC1,EC2,EC3, ER1,ER2,ER3 for Hynix 1GB EMI
 change HDD sata CN20 pin define to increase the impedance for SATA SI
 0506
 reserve PR247 for colay with MAX17020
 Update U29 footprint for Japan/Mitsui package
 change L85 to 60ohm for EMI
 NC C5 for EMI
 0508
 add Q30 for MS/SD LED cost down
 M751 PVT

0618
 Page 24:Change L30,L31,L32 to 33ohm and change C258,C260,C262 to 15PF for SI issue
 Page 25:chang C405 C407 to 1C-2B30475-K100 for PUR request
 Page 33:NC R561,Mount R560 ,keep system ID the same as M750
 Page 36:NC F1 ,mount F3,for 5v Camera moudle
 Page 38:Change R80 to 4.7k from 10k , for FAN speed issue
 Page 40 :NC Q30 ,Mount U39 Q13 C672 C670 R589 for mor Request
 Page 47:NC PR244 ,Vendor suggestion and it is related with DC4
 Page 43,49:1.FR14 change to 62Kohm , co-lay PR248 LND 56.6Kohm with PR7.
 2.PR215 205Kohm change to 280Kohm
 3.PR223 154Kohm change to 280Kohm
 Page 24: change D17 to 16-SSM24AP-T000' for leakage issue
 Page 7:Change C254,C252 rating to 6.3v for cost down
 Page 35:del R301,R302,R303,R304,R305,R306,L40,L41,L42 for cost down
 Page36:del R147 H150 L28 for cost down
 Page 39:del R261 for cost down,change U14 version
 Page 33:Change CN6 to 1N-0024000-F1T0 for pur request
 Page 52:add ER4 EC4 for EMI Issue

0625
 Page 43:.PC121 change from 0.1uF/25V to 0.1uF/50V(1C-2B30104-K000)
 Page 52 : change ER4 EC4 to 0603 for EMI request
 Page 40:modify the U33 F/N to 15-BD2056A-FJ00 for CE update component library
 Page 35:resume CN6 main source 1N-0024000-M1T0, for 2nd source layout issue
 Page 24:change D17 to 16-SSM24PT-0000 For design change
 Page 51:add one test point in PR41 pin1.

www.s-manuals.com