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P. Leader	Check by	Design by

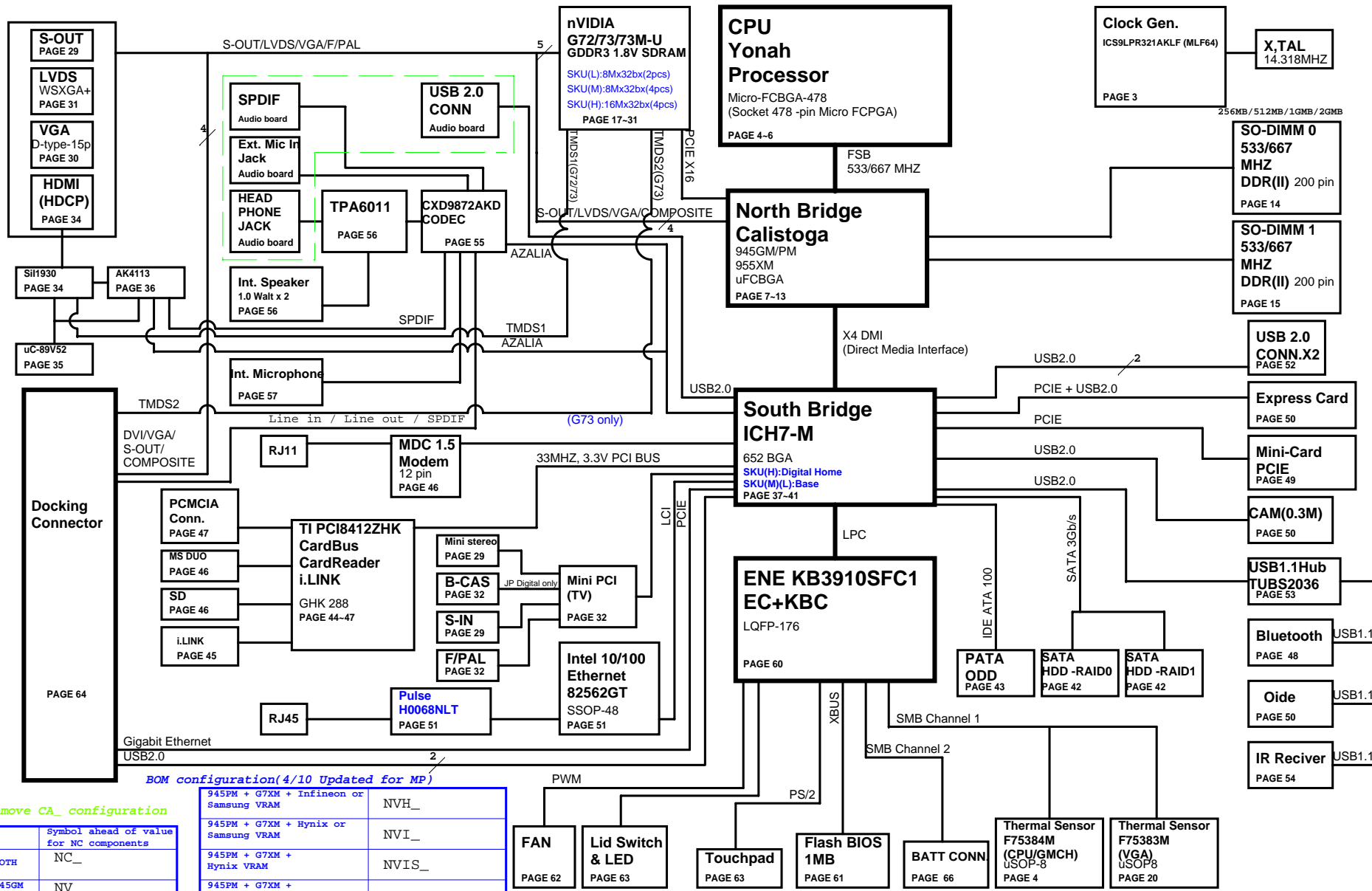
Project Code & Schematics Subject: MS21 MP Main Board
(TYPE 2)

PCB P/N: 1P-0068100-8011 (FUBAI)
 1P-0068500-8011 (Hannstar)

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
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MS21(CALISTOGA PM+Gfx Block Diagram)

Red texts:
New modified



Remove CA_configuration

Symbol	Value	NC components
BOTH	NC_	
945GM	NV_	
945PM + G72M	NV73_	
945PM + G73M	NV72_	
945PM + G72M or G73M-U	NV73Only_	

Configuration	Value
945PM + G7XM + Infineon or Samsung VRAM	NVH_
945PM + G7XM + Hynix or Samsung VRAM	NVI_
945PM + G7XM + Hynix VRAM	NVIS_
945PM + G7XM + Infineon VRAM	NVHS_
945PM + G72M or G73M	NV16M_, NV73U_
945PM + G73M-U	NV8M_, NV7273_
*JP Digital TV Tuner SKU & No Tuner SKU not stick	JDTVNC_

BOM configuration(4/10 Updated for MP)

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	CLK_JIG

close to terminal side (For EMI)

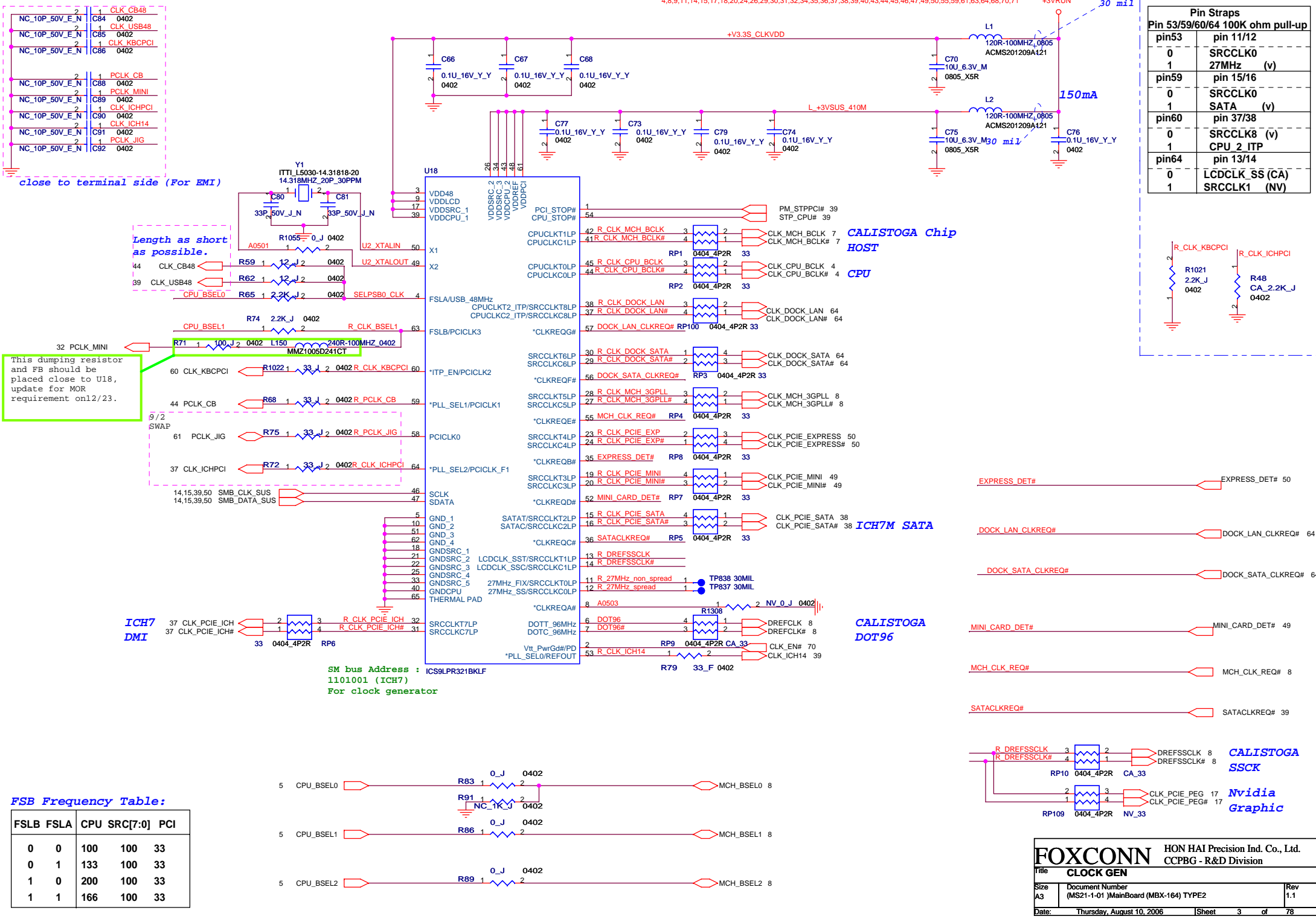
Length as short as possible.

This dumping resistor and FB should be placed close to U18, update for MOR requirement on12/23.

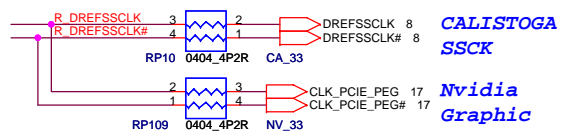
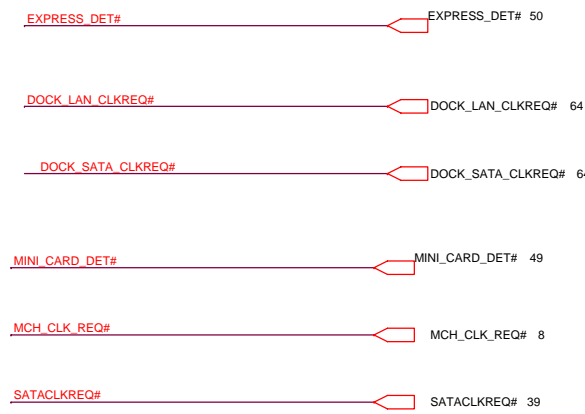
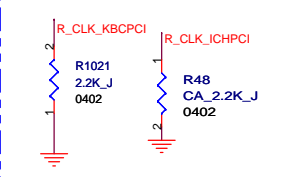
ICH7 DMI

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100
0	1	133	100
1	0	200	100
1	1	166	100



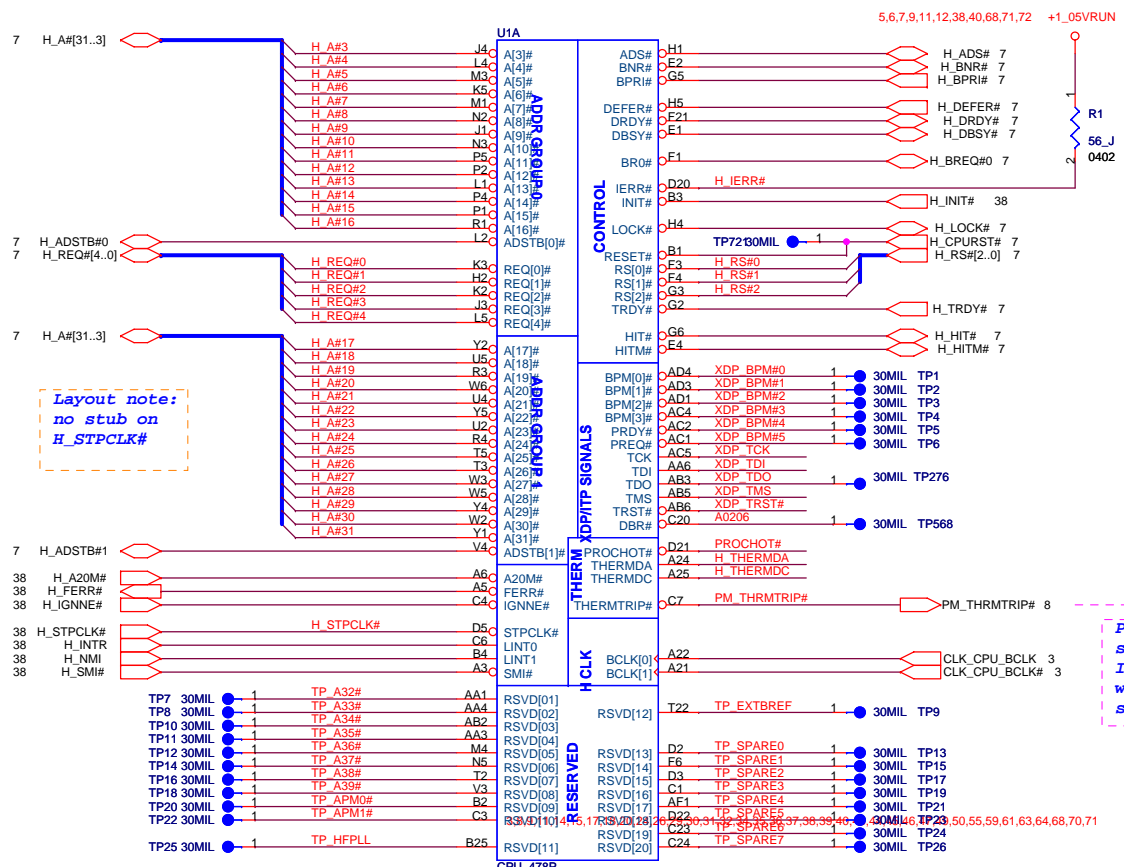
Pin Straps	
pin53/59/60/64 100K ohm pull-up	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCCLK1 (NV)



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File: **CLOCK_GEN**

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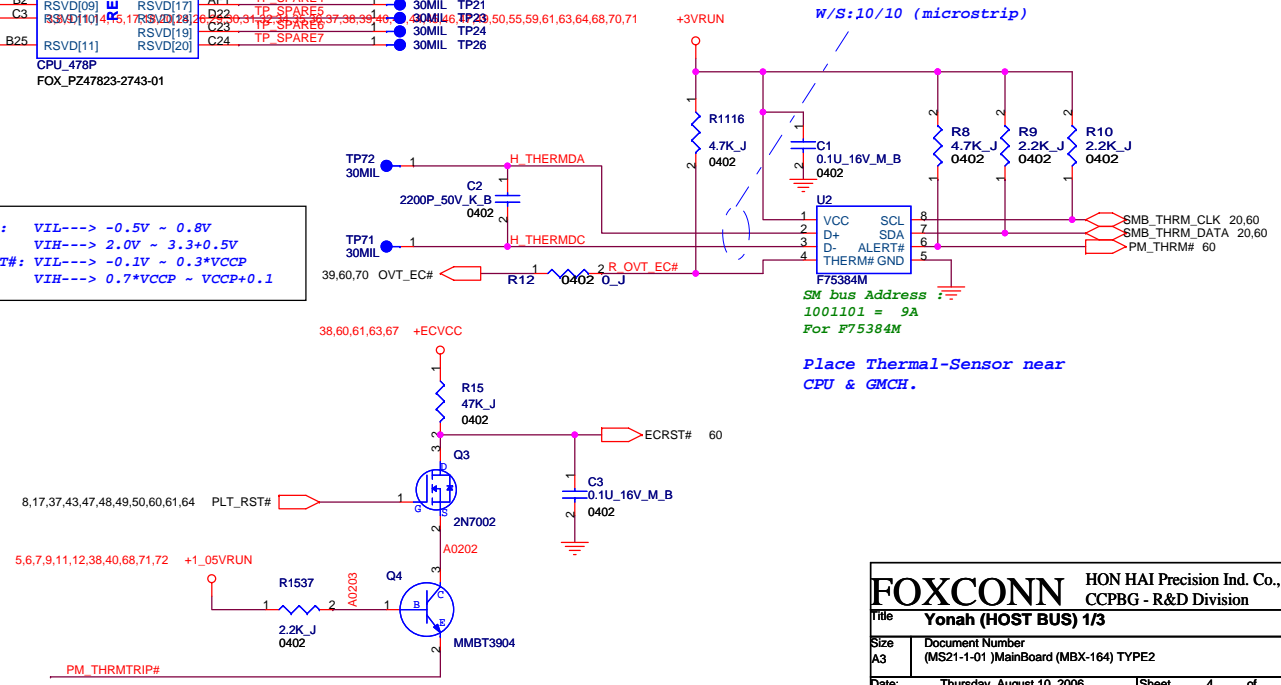
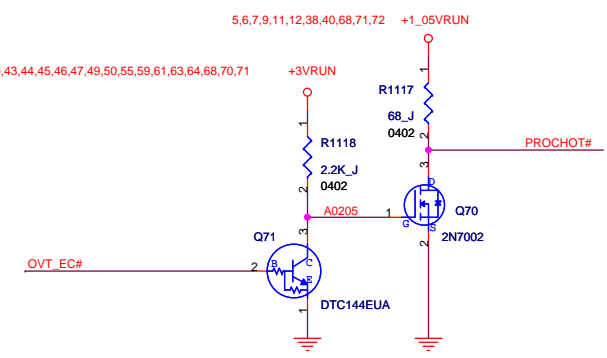
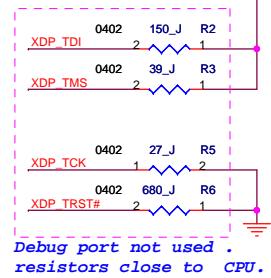


Layout note:
no stub on
H_STPCLK#

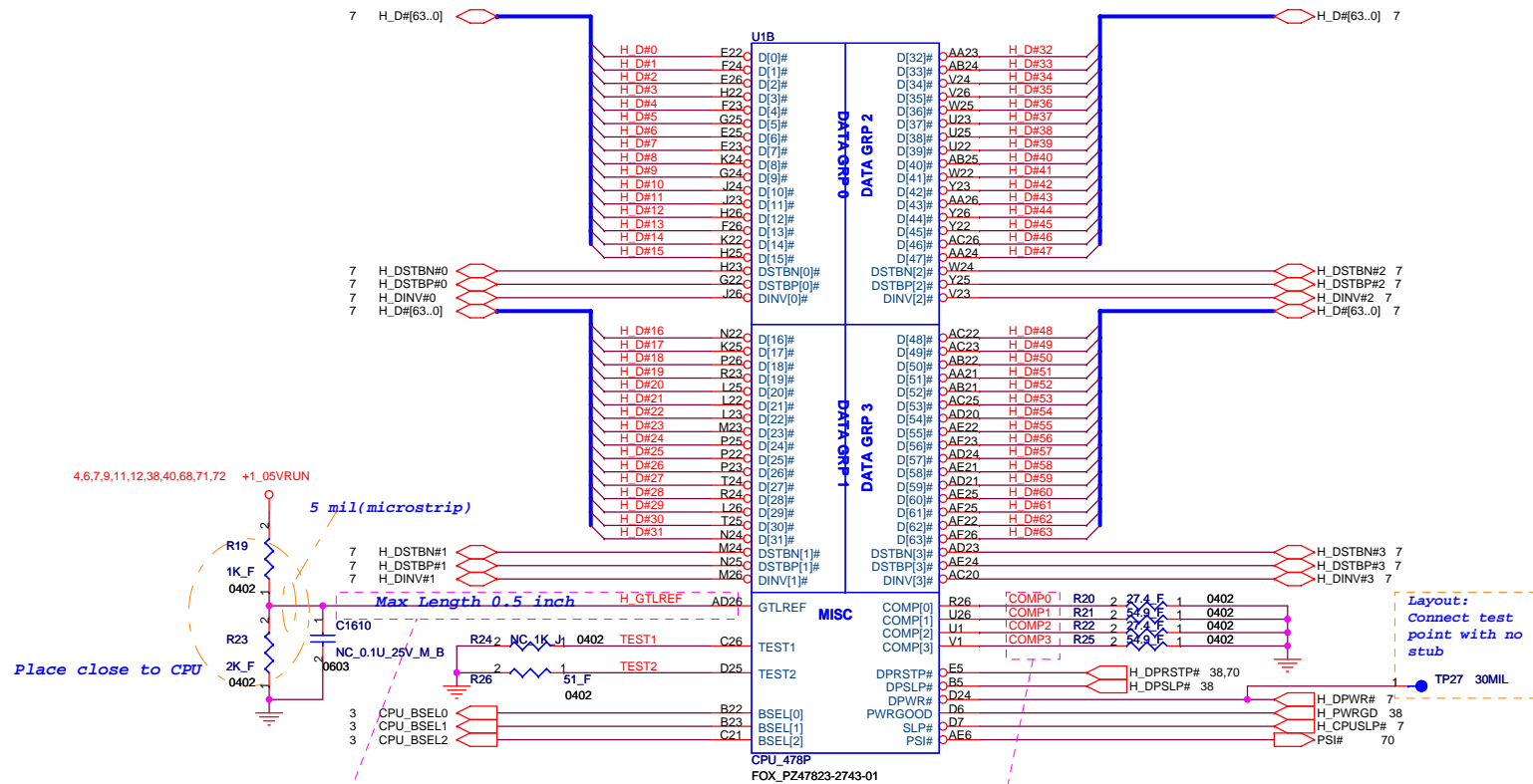
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL----> -0.5V - 0.8V
VIH----> 2.0V - 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V - 0.3*VCCP
VIH----> 0.7*VCCP - VCCP+0.1

PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)



Place Thermal-Sensor near
CPU & GMCH.



4,6,7,9,11,12,38,40,68,71,72 +1_05VVRUN

5 mil(microstrip)

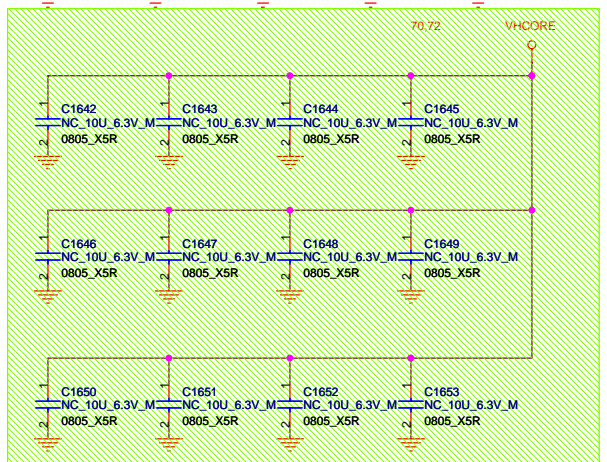
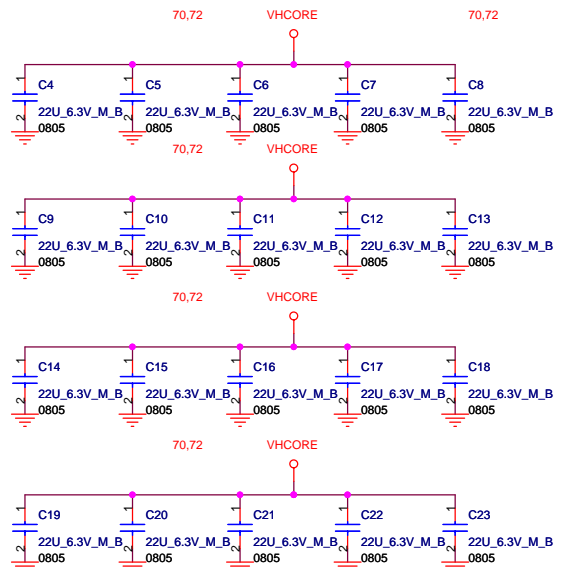
Max Length 0.5 inch

Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".

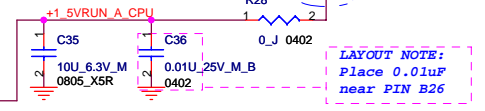
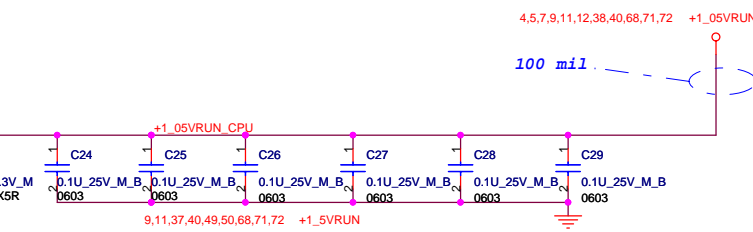
Layout:
Connect test
point with no
stub



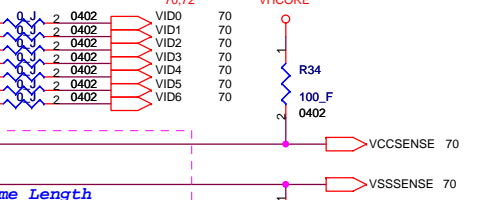
Backup 10uF capacitors for 22uF shortage.

U1C		U1D	
A7	VCC[001]	A4	VSS[001]
A9	VCC[002]	A8	VSS[002]
A10	VCC[003]	A11	VSS[003]
A12	VCC[004]	A14	VSS[004]
A13	VCC[005]	A16	VSS[005]
A15	VCC[006]	A19	VSS[006]
A17	VCC[007]	A23	VSS[007]
A18	VCC[008]	A26	VSS[008]
A20	VCC[009]	B6	VSS[009]
B7	VCC[010]	B9	VSS[010]
B9	VCC[011]	B11	VSS[011]
B10	VCC[012]	B13	VSS[012]
B12	VCC[013]	B16	VSS[013]
B14	VCC[014]	B19	VSS[014]
B15	VCC[015]	B21	VSS[015]
B17	VCC[016]	B24	VSS[016]
B18	VCC[017]	C5	VSS[017]
B20	VCC[018]	C8	VSS[018]
C9	VCC[019]	C11	VSS[019]
C10	VCC[020]	C14	VSS[020]
C12	VCC[021]	C16	VSS[021]
C13	VCC[022]	C19	VSS[022]
C15	VCC[023]	C22	VSS[023]
C17	VCC[024]	C25	VSS[024]
C18	VCC[025]	C27	VSS[025]
D9	VCC[026]	C28	VSS[026]
D10	VCC[027]	C29	VSS[027]
D12	VCC[028]	D1	VSS[028]
D14	VCC[029]	D4	VSS[029]
D15	VCC[030]	D8	VSS[030]
D17	VCC[031]	D11	VSS[031]
D18	VCC[032]	D13	VSS[032]
E7	VCC[033]	D19	VSS[033]
E9	VCC[034]	D23	VSS[034]
E10	VCC[035]	D26	VSS[035]
E13	VCC[036]	E3	VSS[036]
E15	VCC[037]	E6	VSS[037]
E17	VCC[038]	E8	VSS[038]
E18	VCC[039]	E11	VSS[039]
E20	VCC[040]	E14	VSS[040]
F7	VCC[041]	E16	VSS[041]
F9	VCC[042]	E19	VSS[042]
F10	VCC[043]	E21	VSS[043]
F12	VCC[044]	E24	VSS[044]
F14	VCC[045]	F8	VSS[045]
F15	VCC[046]	F11	VSS[046]
F17	VCC[047]	F13	VSS[047]
F18	VCC[048]	F16	VSS[048]
F20	VCC[049]	F19	VSS[049]
AA7	VCC[050]	F2	VSS[050]
AA9	VCC[051]	F22	VSS[051]
AA10	VCC[052]	F25	VSS[052]
AA12	VCC[053]	G4	VSS[053]
AA13	VCC[054]	G1	VSS[054]
AA15	VCC[055]	G23	VSS[055]
AA17	VCC[056]	G26	VSS[056]
AA18	VCC[057]	H3	VSS[057]
AA20	VCC[058]	H6	VSS[058]
AB9	VCC[059]	H21	VSS[059]
AC10	VCC[060]	H24	VSS[060]
AB10	VCC[061]	J2	VSS[061]
AB12	VCC[062]	N5	VSS[062]
AB14	VCC[063]	J25	VSS[063]
AB15	VCC[064]	K1	VSS[064]
AB17	VCC[065]	K4	VSS[065]
AB18	VCC[066]	K23	VSS[066]
	VCC[067]	K26	VSS[067]
		L3	VSS[068]
		L6	VSS[069]
		L21	VSS[070]
		L24	VSS[071]
		M2	VSS[072]
		M5	VSS[073]
		M22	VSS[074]
		N1	VSS[075]
		N4	VSS[076]
		N23	VSS[077]
		N26	VSS[078]
		P3	VSS[079]
			VSS[080]
			VSS[081]
			VSS[082]
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			VSS[162]

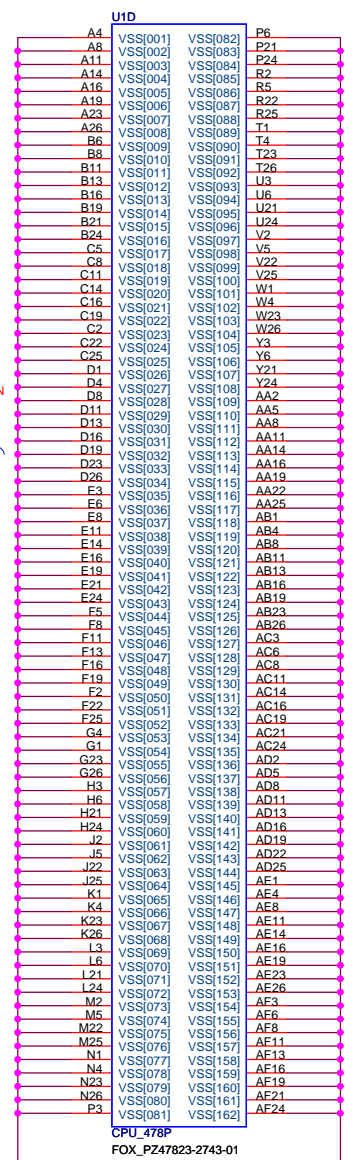
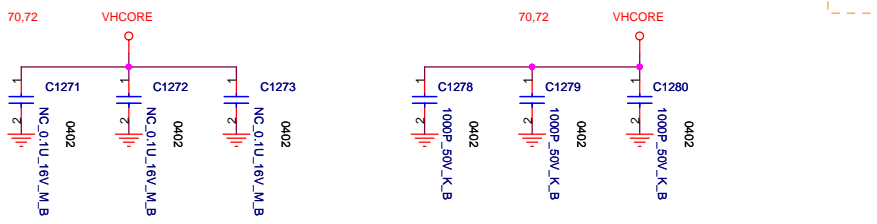
CPU_VCCA----->120mA
 CPU_VCCP----->2.5A
 CPU_VCC----->44A

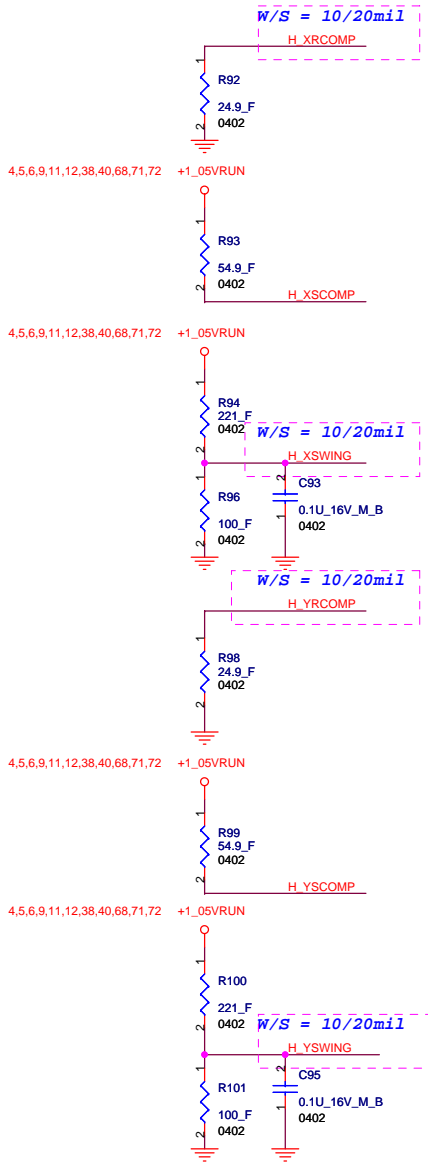


LAYOUT NOTE:
 Place 0.01uF near PIN B26



Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
 width=18 mil spacing=7 mil

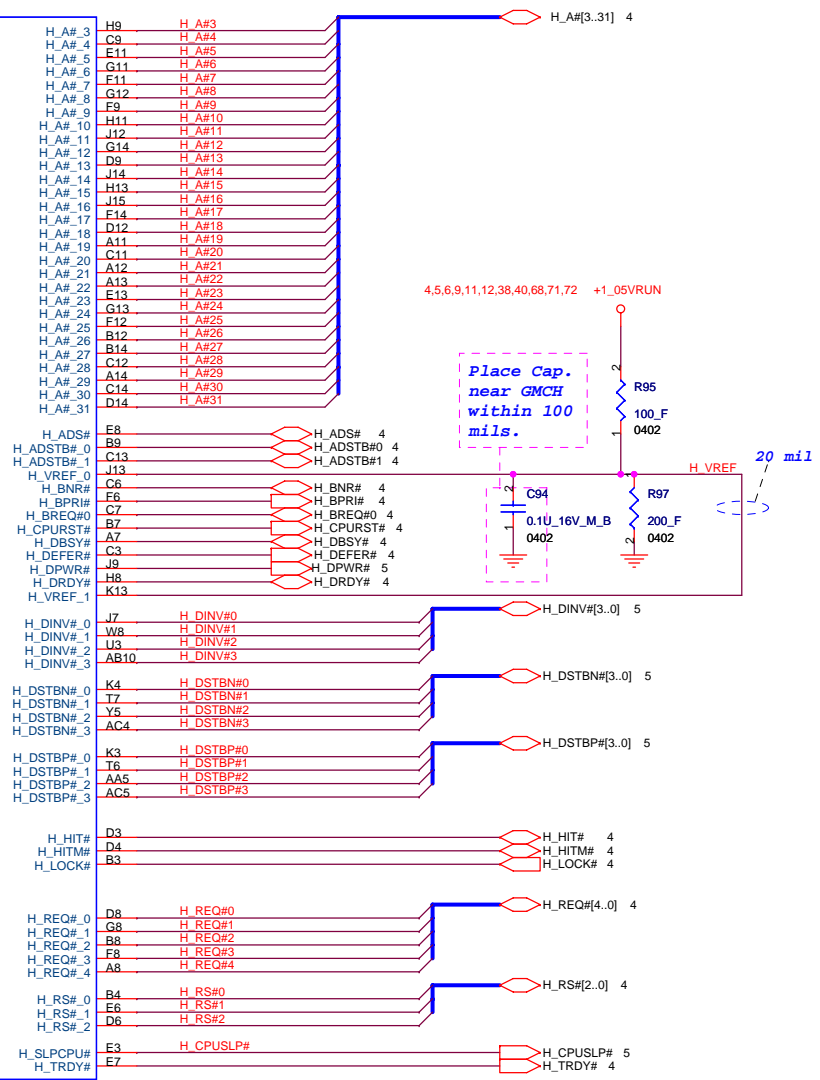




5 H_D#[63..0] H_D#[63..0]

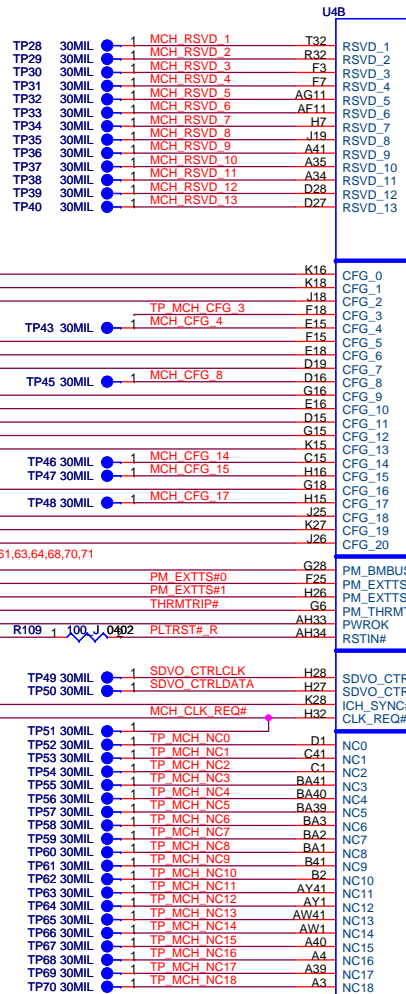
U4A	
H_D#0	F1
H_D#1	J1
H_D#2	H1
H_D#3	J6
H_D#4	H3
H_D#5	K2
H_D#6	G1
H_D#7	G2
H_D#8	K9
H_D#9	K1
H_D#10	K7
H_D#11	J8
H_D#12	H4
H_D#13	J3
H_D#14	K11
H_D#15	G4
H_D#16	T10
H_D#17	W11
H_D#18	T3
H_D#19	U9
H_D#20	U7
H_D#21	U11
H_D#22	T11
H_D#23	W9
H_D#24	T1
H_D#25	T4
H_D#26	T4
H_D#27	W7
H_D#28	U5
H_D#29	T9
H_D#30	W6
H_D#31	T5
H_D#32	AB7
H_D#33	AA9
H_D#34	W4
H_D#35	W3
H_D#36	Y3
H_D#37	Y7
H_D#38	W5
H_D#39	Y10
H_D#40	AB8
H_D#41	W2
H_D#42	AA4
H_D#43	AA7
H_D#44	AA2
H_D#45	AA6
H_D#46	AA10
H_D#47	Y8
H_D#48	AA1
H_D#49	AB4
H_D#50	AC9
H_D#51	AB11
H_D#52	AC11
H_D#53	AB3
H_D#54	AC2
H_D#55	AD1
H_D#56	AD9
H_D#57	AC1
H_D#58	AD7
H_D#59	AC6
H_D#60	AB5
H_D#61	AD10
H_D#62	AD4
H_D#63	AC8
H_XRCOMP	E1
H_XSCOMP	E2
H_XSWING	E4
H_YRCOMP	Y1
H_YSCOMP	U1
H_YSWING	W1
H_CLKIN	AG2
H_CLKIN#	AG1

HOST

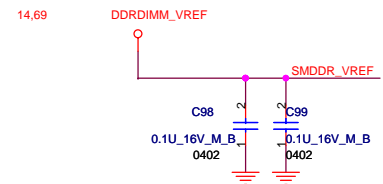
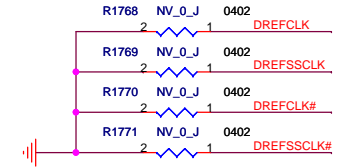


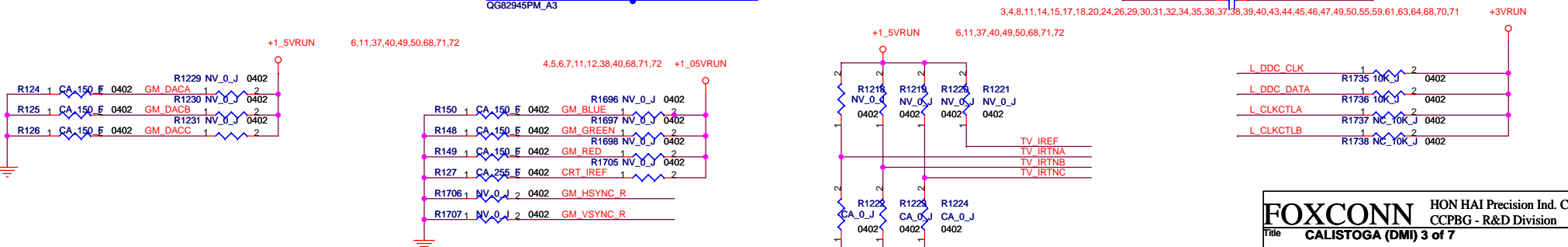
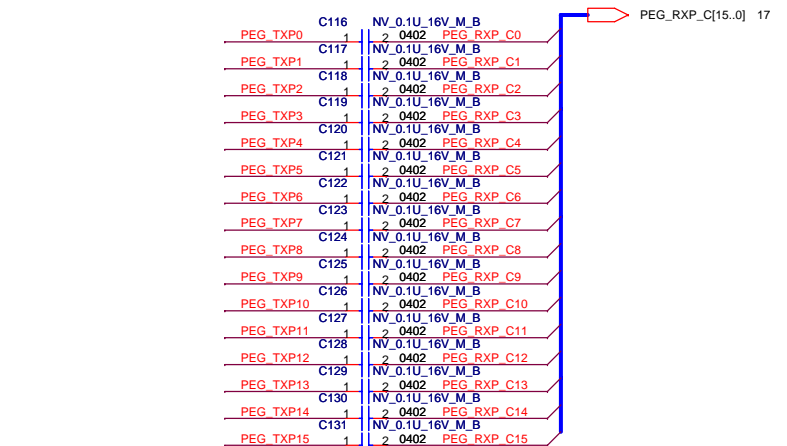
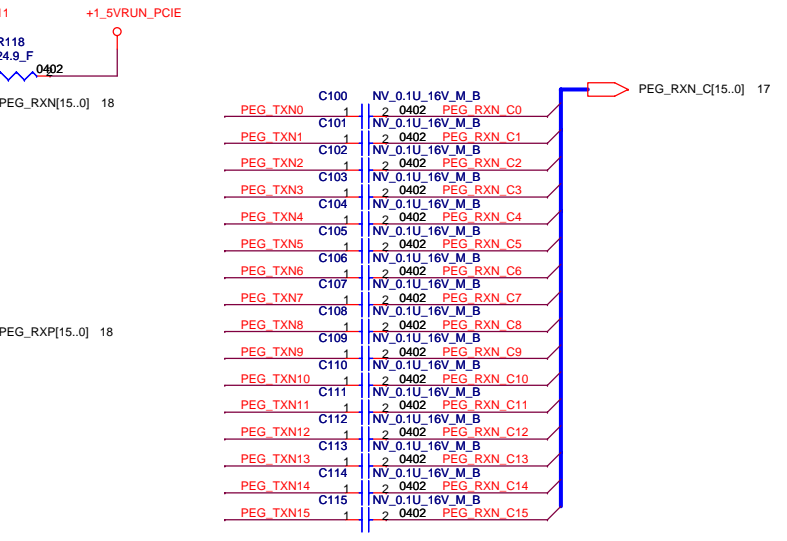
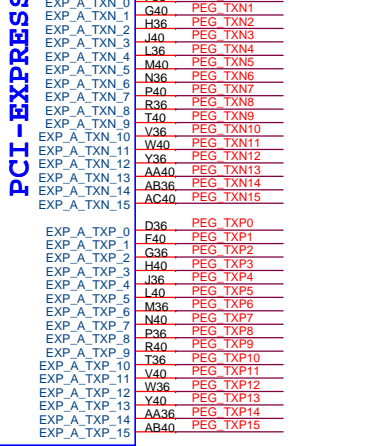
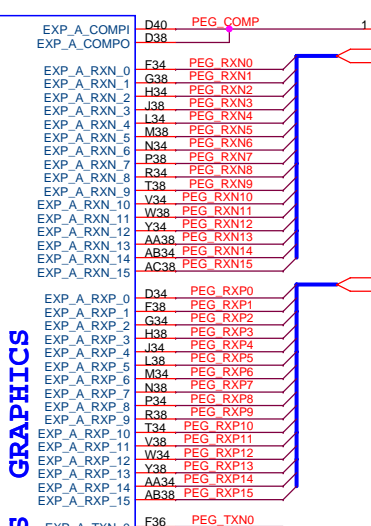
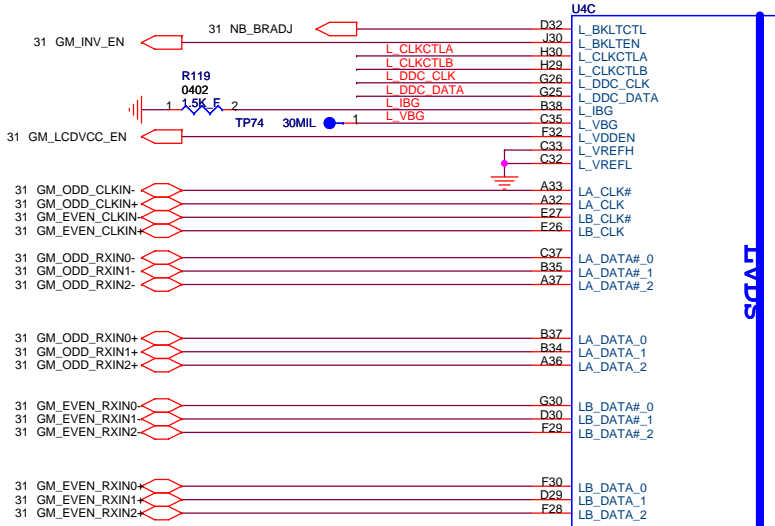
3 CLK_MCH_BCLK
3 CLK_MCH_BCLK#

QG82945PM_A3



5/5 Remove R110 for PM_EXTTTS#1 back up pull up res.
 ICH7 (DPRSLPVR) already have internal pull up

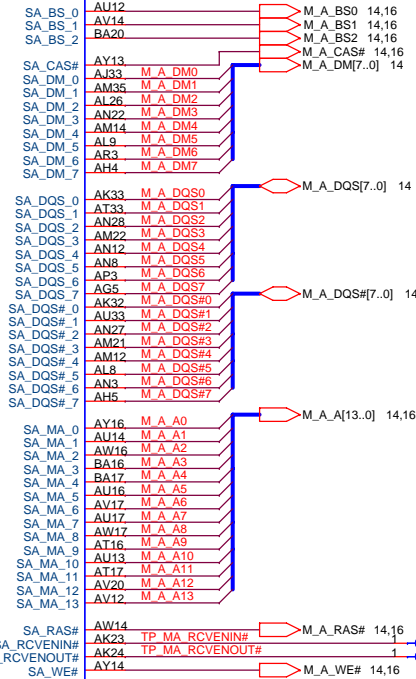




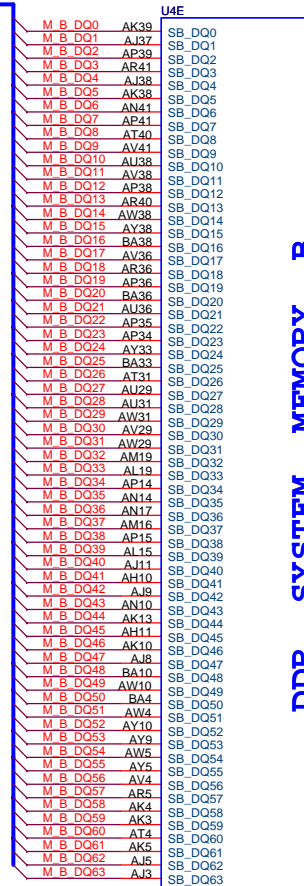
14 M_A_DQ[63.0]



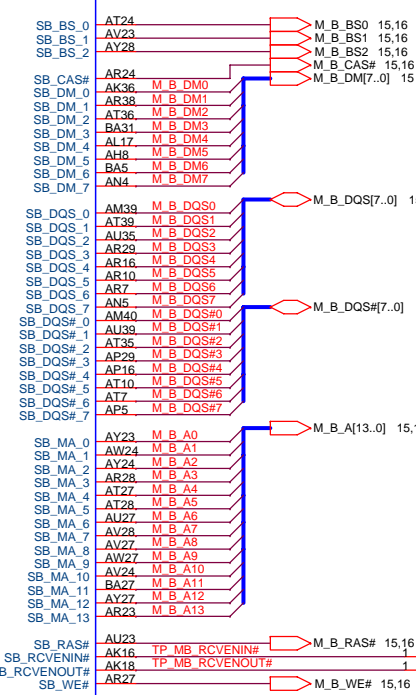
QG82945PM_A3

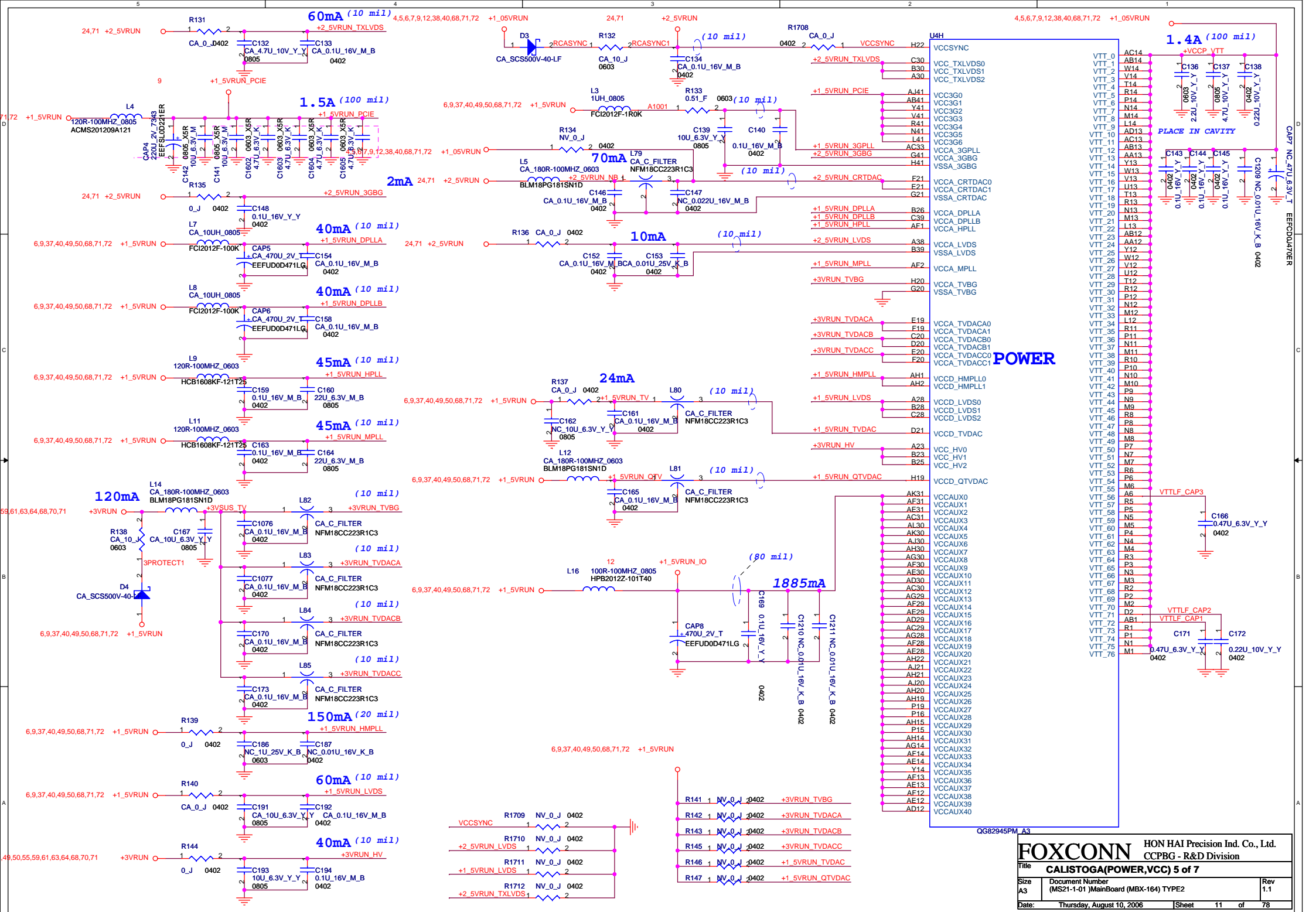


15 M_B_DQ[63.0]

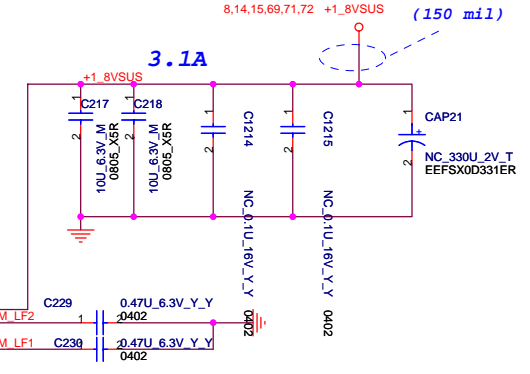
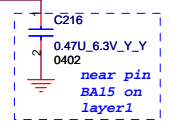
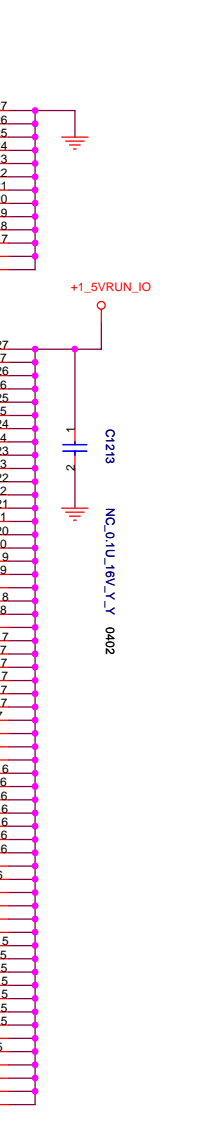
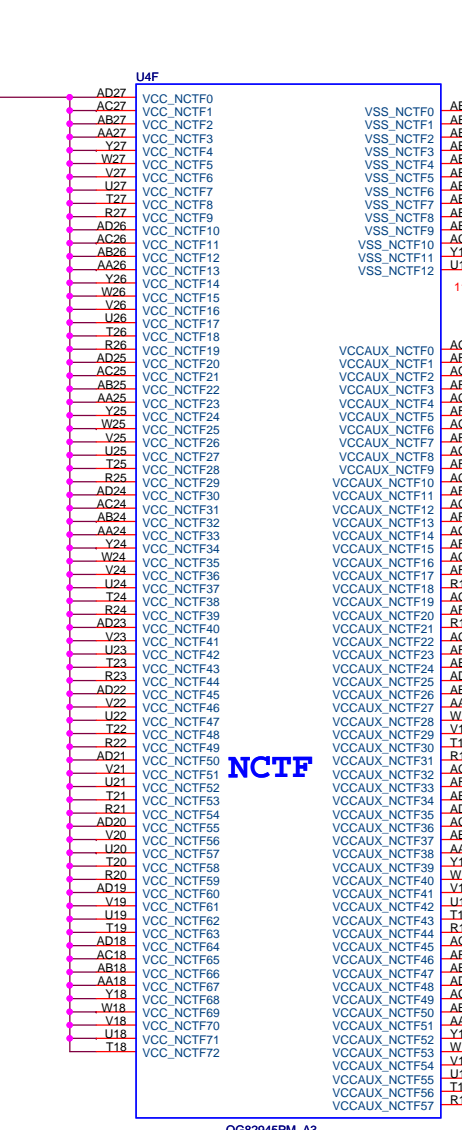
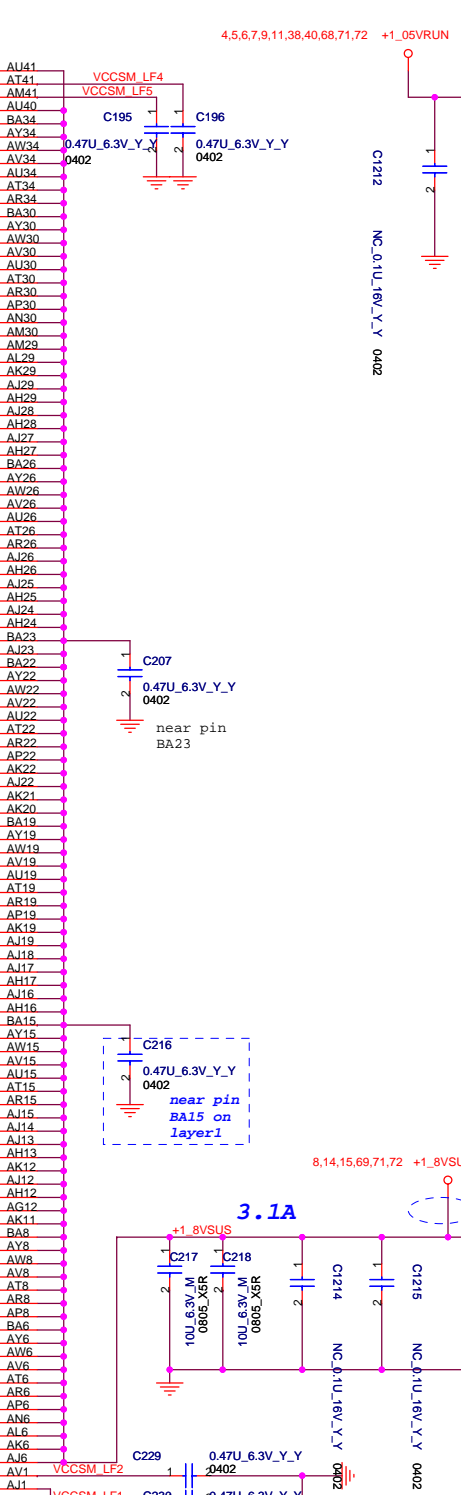
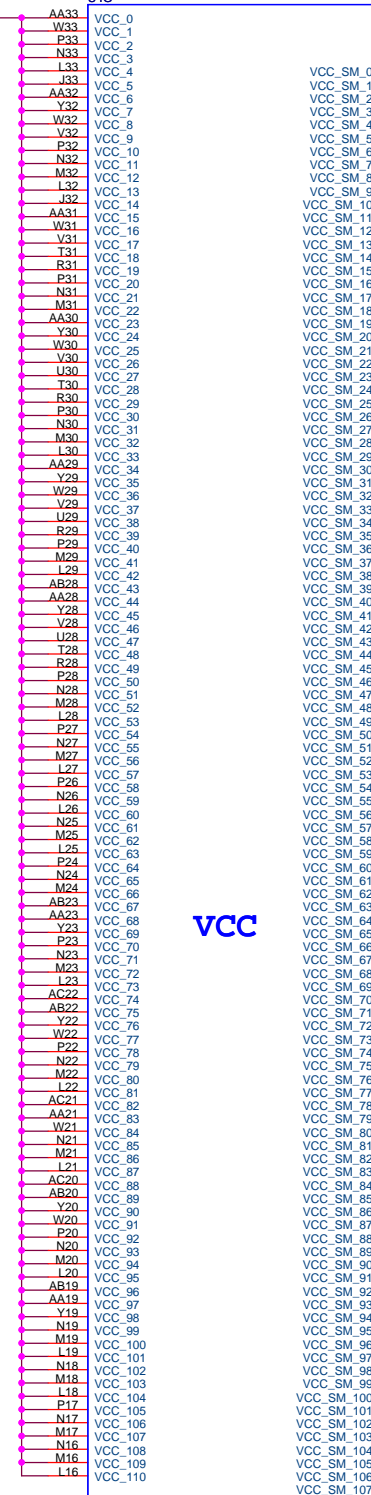
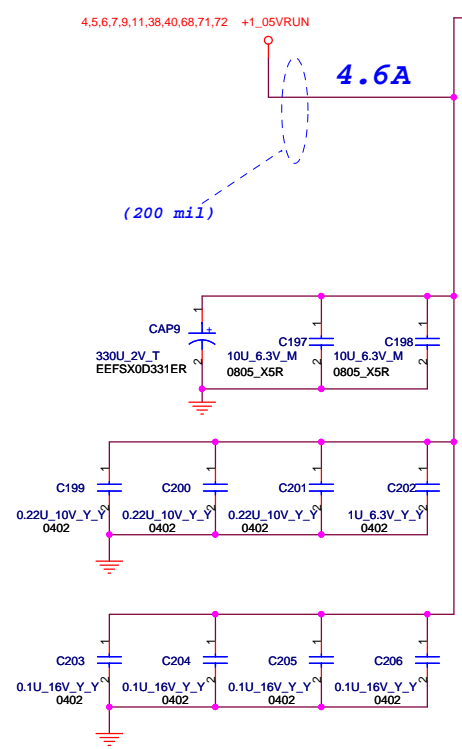


QG82945PM_A3





FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title CALISTOGA(POWER,VCC) 5 of 7		
Size A3	Document Number (MS21-01>MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 11	of 78



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CALISTOGA(VCC CORE) 6 of 7	
Size	Document Number	Rev	
Custom	(MS21-1-01) MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	12 of 78

8 MCH_CFG_5 ← 1 ● 30MIL TP554

MCH_CFG_5
Low = DMIX2
High = DMIX4

8 MCH_CFG_6 ← 1 ● 30MIL TP556

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

8 TP_MCH_CFG_7 ← TP_MCH_CFG_7

MCH_CFG_7 (CPU Strap)
Low = RSVD
High = Mobile Yonah processor

8 MCH_CFG_9 ← 1 ● 30MIL TP559

MCH_CFG_9 (PCIe Graphics Lane)
Low = Reverse Lane
High = Normal operation
For layout convenience

8 MCH_CFG_10 ← 1 ● 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

8 MCH_CFG_11 ← 1 ● 30MIL TP562

MCH_CFG_11 (PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved

8 MCH_CFG_12 ← 1 ● 30MIL TP562

8 MCH_CFG_13 ← 1 ● 30MIL TP563

MCH_CFG_[13:12]
(XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

8 MCH_CFG_16 ← 1 ● 30MIL TP564

MCH_CFG_16 (FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

8 MCH_CFG_18 ← 1 ● 30MIL TP555

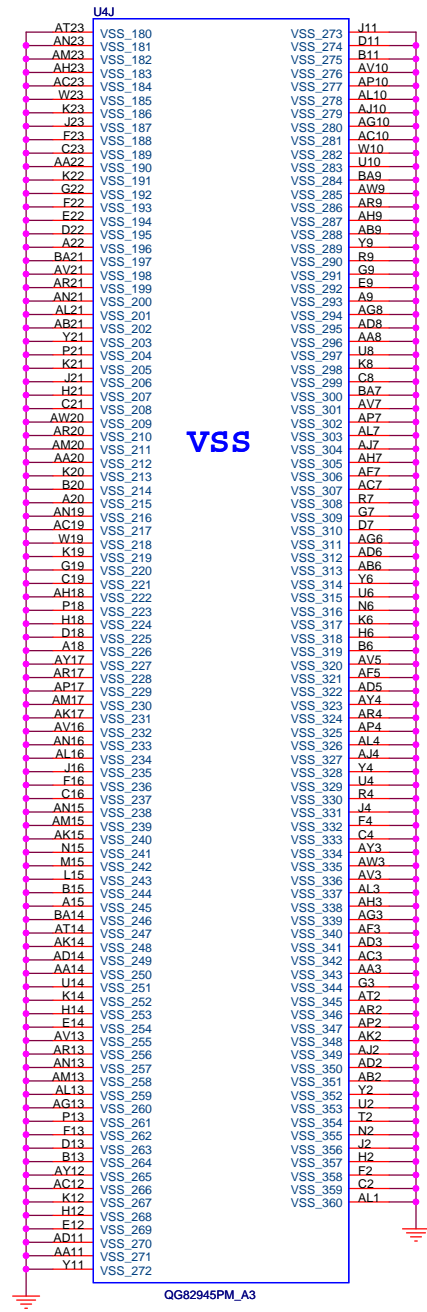
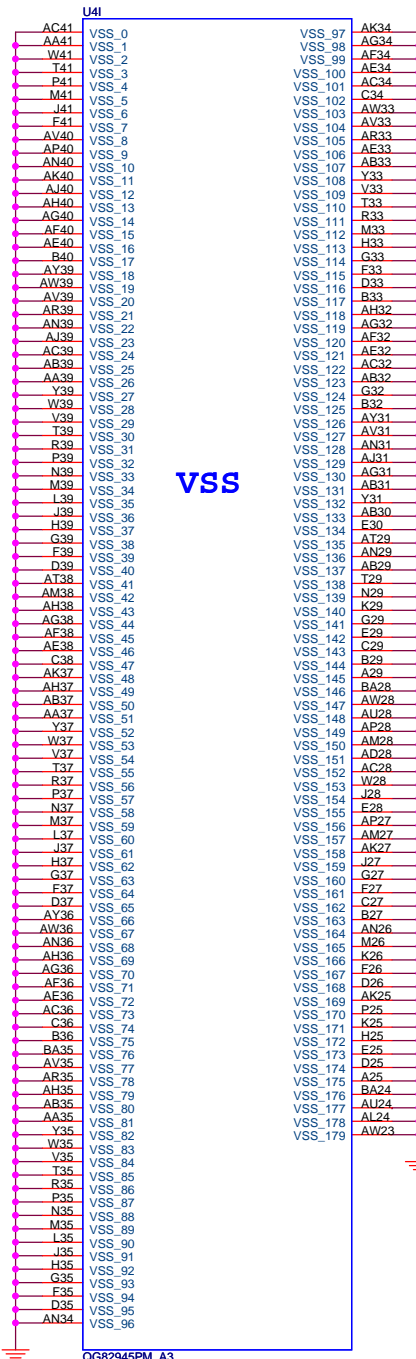
MCH_CFG_19 (DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

8 MCH_CFG_19 ← 1 ● 30MIL TP558

MCH_CFG_20
Low = Only SDVO or PCIE x1 is operational (defaults)
High = SDVO and PCIE x1 are operating simultaneously via the PEG port

8 MCH_CFG_20 ← 1 ● 30MIL TP561

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

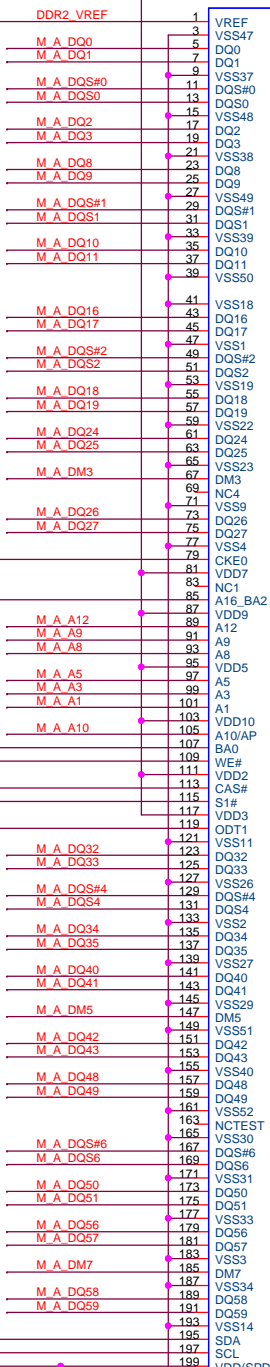
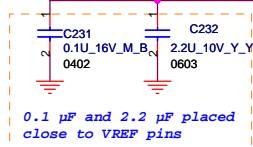


FOXCONN HON HAI Precision Ind. Co., Ltd.
Title CALISTOGA(VSS) 7 of 7
Size A3 Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2 Rev 1.1
Date: Thursday, August 10, 2006 Sheet 13 of 78

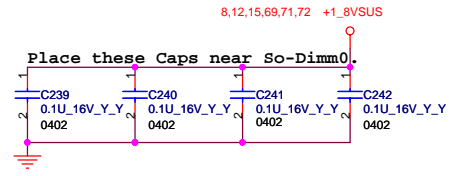
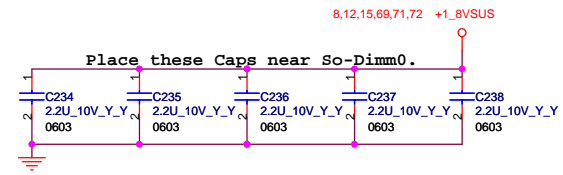
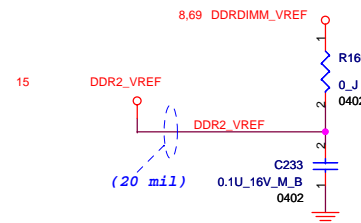
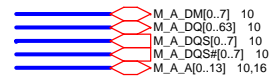
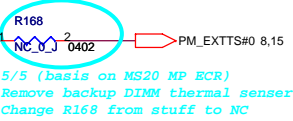
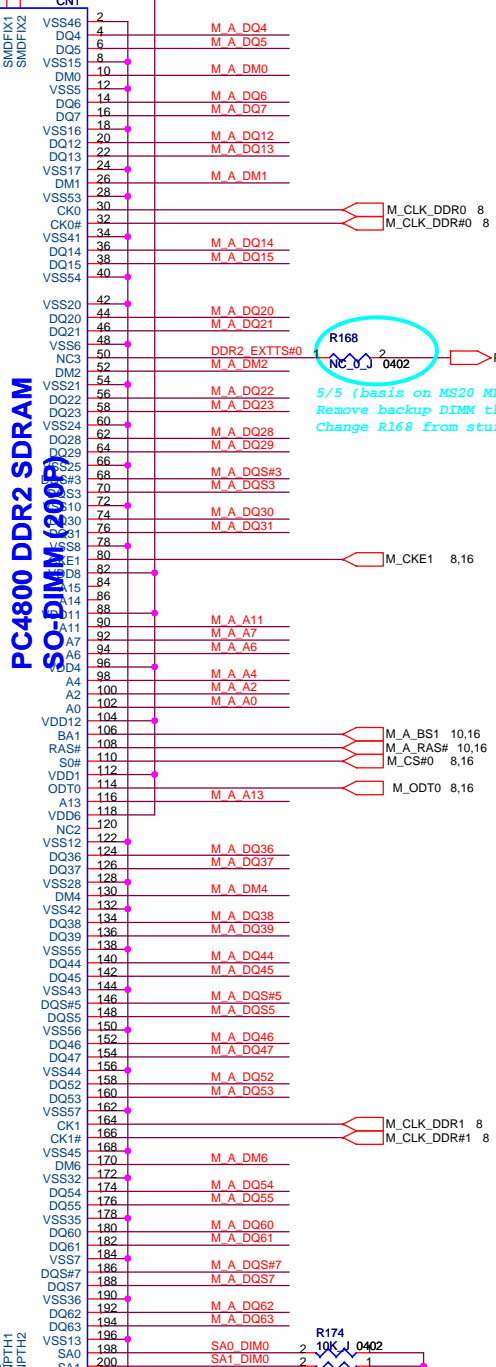
8,12,15,69,71,72 +1_8VSUS

+1_8VSUS 8,12,15,69,71,72

1.8V per DIMM=3.08A



PC4800 DDR2 SDRAM SO-DIMM (200P)



3,15,39,50 SMB_DATA_SUS
3,15,39,50 SMB_CLK_SUS
+3VRUN



DIMM_0

DDR2 SO-DIMM_200P
FOX_AS0A426_N4RC_4F
SMBus Address: A0(W)/A1(R)

Place DIMM_0 near GMCH

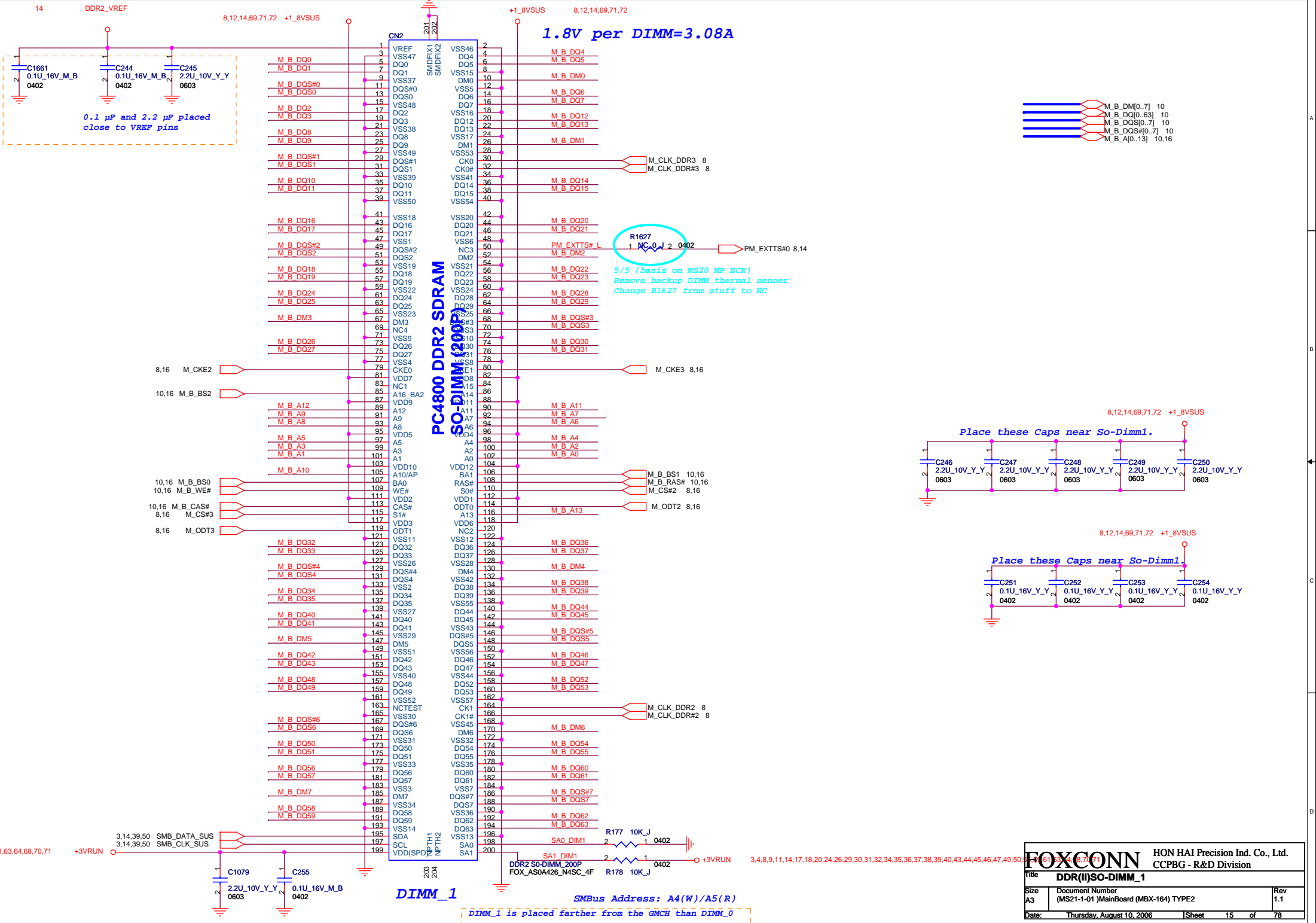


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CCPBG - R&D Division

Title: **DDR(II)SO-DIMM_0**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
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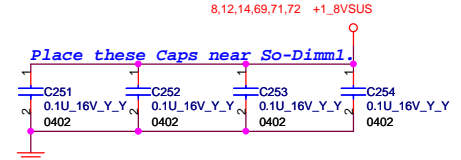
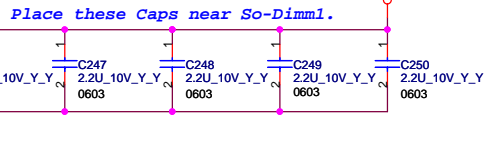


1.8V per DIMM=3.08A

- M_B_DM[0..7] 10
- M_B_DQ[0..63] 10
- M_B_DQS[0..7] 10
- M_B_DQS#[0..7] 10
- M_B_A[0..13] 10,16

R1627
1 NC_0 2 0402 → PM_EXTT#0 8,14

5/5 (basis on MS20 MP ECR)
Remove backup DIMM thermal sensor
Change R1627 from stuff to NC



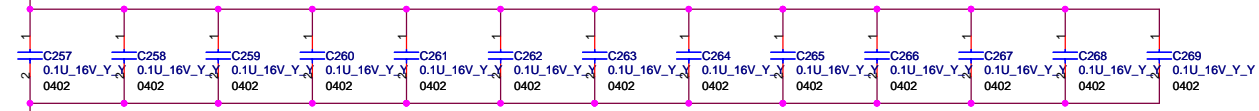
PC4800 DDR2 SDRAM
SO-DIMM (200P)

DIMM_1
SMBus Address: A4(W)/A5(R)
DIMM_1 is placed farther from the GMCH than DIMM_0

FOXCONN			HON HAI Precision Ind. Co., Ltd.
			CCPBG - R&D Division
Title DDR(H)SO-DIMM_1			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 15	of 78	

69,72

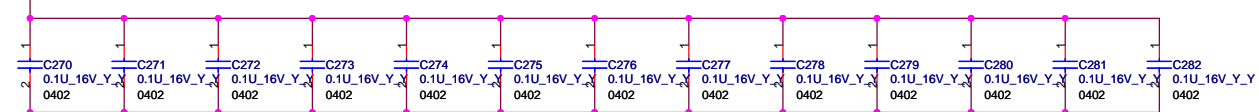
+0_9VSUS



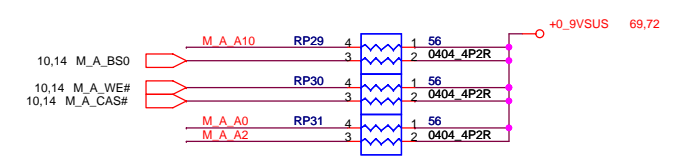
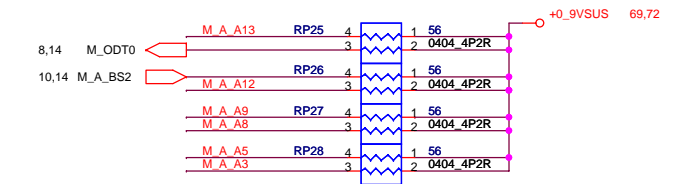
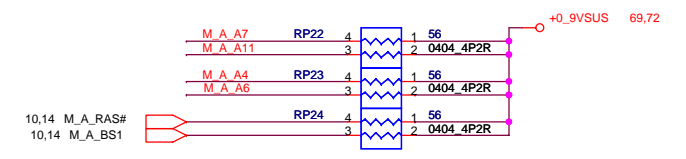
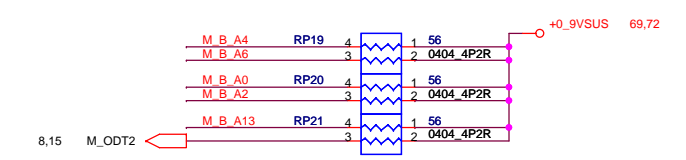
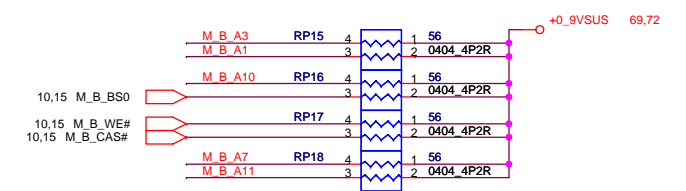
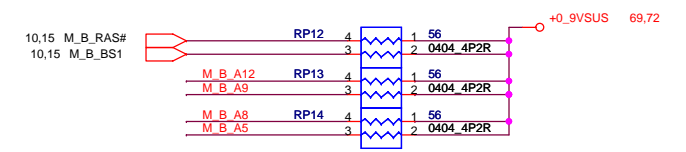
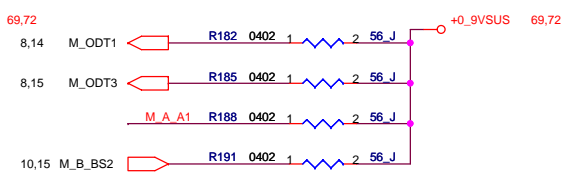
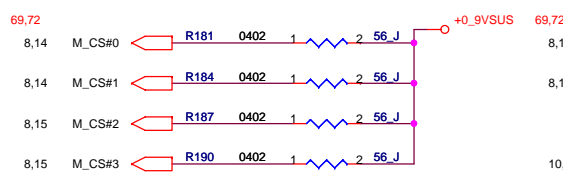
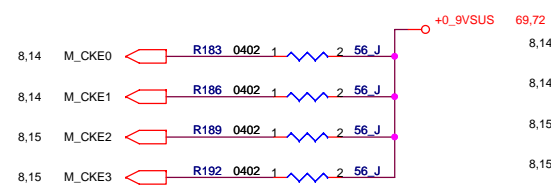
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

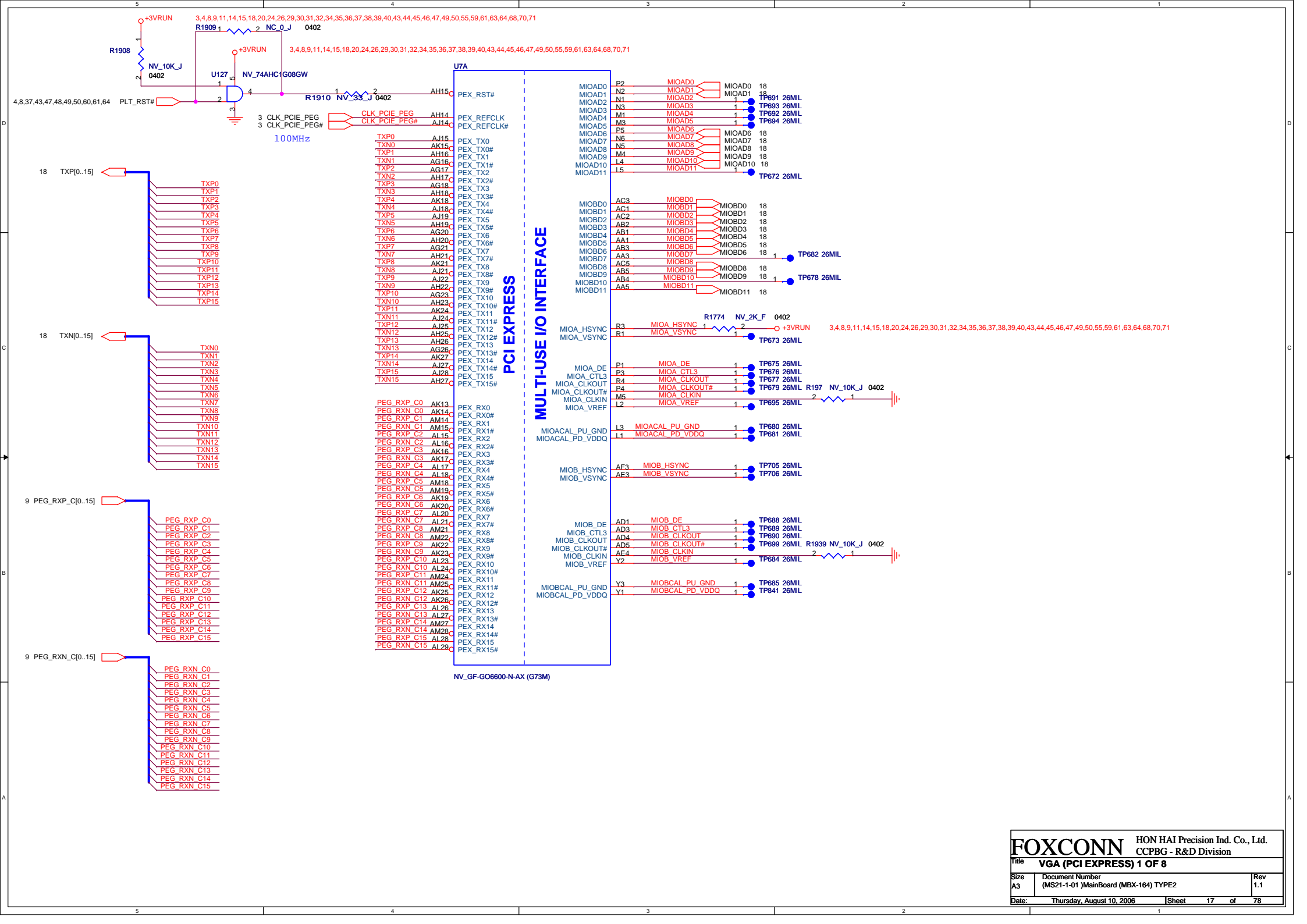
69,72

+0_9VSUS

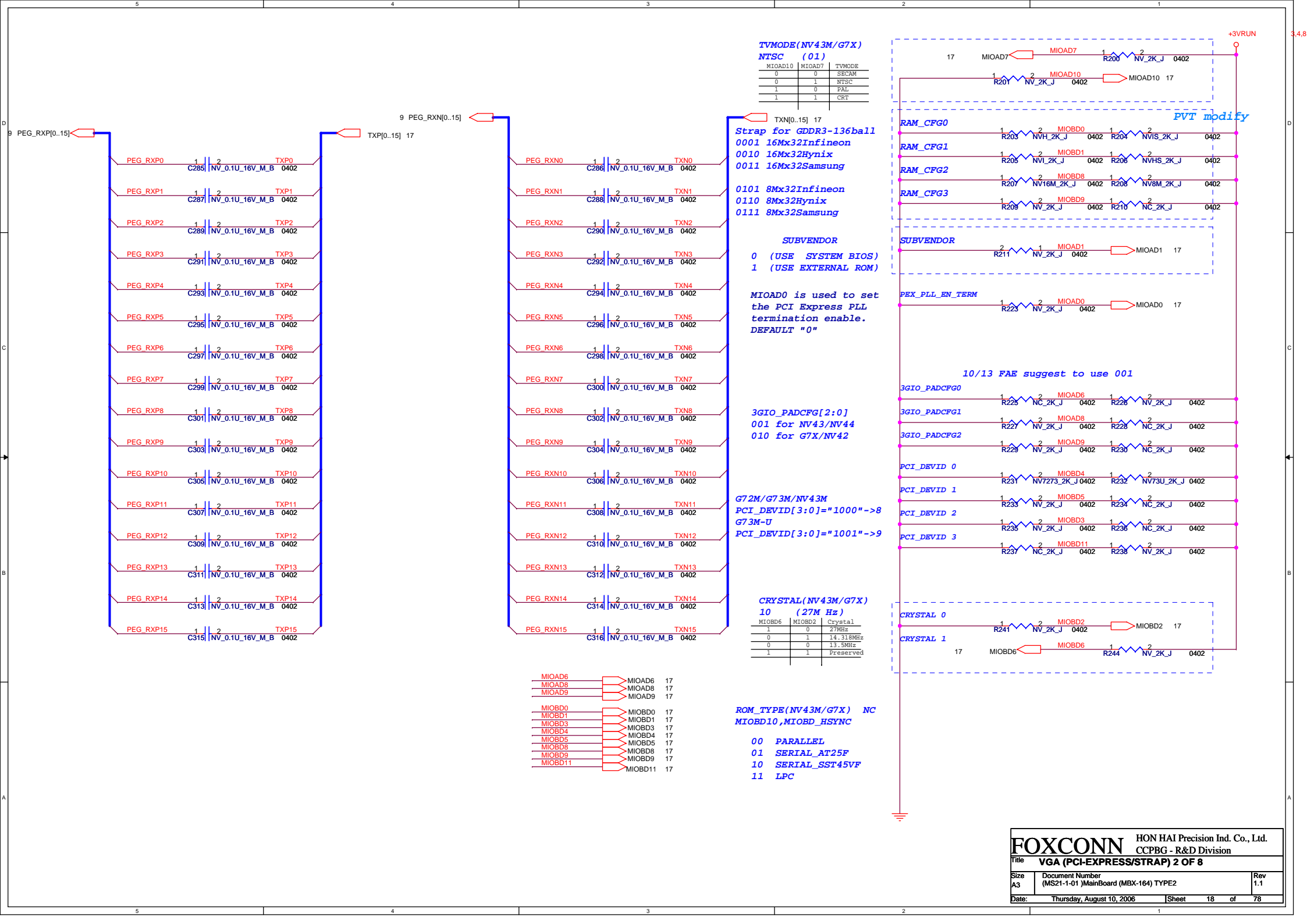


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS





- U7A
- 3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG#
- 100MHz
- TXP0 AH15 PEX_TX0
TXP1 AK15C PEX_TX0#
TXP2 AH16 PEX_TX1#
TXN1 AG16C PEX_TX1#
TXP2 AG17 PEX_TX2
TXN2 AH17C PEX_TX2#
TXP3 AG18 PEX_TX3
TXN3 AH18C PEX_TX3#
TXP4 AK18 PEX_TX4
TXN4 AJ18C PEX_TX4#
TXP5 AJ19 PEX_TX5
TXN5 AH19C PEX_TX5#
TXP6 AG20 PEX_TX6
TXN6 AH20C PEX_TX6#
TXP7 AG21 PEX_TX7
TXN7 AH21C PEX_TX7#
TXP8 AK21 PEX_TX8
TXN8 AJ21C PEX_TX8#
TXP9 AJ22 PEX_TX9
TXN9 AH22C PEX_TX9#
TXP10 AG23 PEX_TX10
TXN10 AH23C PEX_TX10#
TXP11 AK24 PEX_TX11
TXN11 AJ24C PEX_TX11#
TXP12 AJ25 PEX_TX12
TXN12 AH25C PEX_TX12#
TXP13 AG26 PEX_TX13
TXN13 AH26C PEX_TX13#
TXP14 AJ27C PEX_TX14
TXN14 AJ27C PEX_TX14#
TXP15 AJ28 PEX_TX15
TXN15 AH27C PEX_TX15#
- PEG_RXP_C0 AK13 PEX_RX0
PEG_RXN_C0 AK14C PEX_RX0#
PEG_RXP_C1 AM14 PEX_RX1
PEG_RXN_C1 AM15C PEX_RX1#
PEG_RXP_C2 AL15 PEX_RX2
PEG_RXN_C2 AL16C PEX_RX2#
PEG_RXP_C3 AK16 PEX_RX3
PEG_RXN_C3 AK17C PEX_RX3#
PEG_RXP_C4 AL17 PEX_RX4
PEG_RXN_C4 AL18C PEX_RX4#
PEG_RXP_C5 AM18 PEX_RX5
PEG_RXN_C5 AM19C PEX_RX5#
PEG_RXP_C6 AK19 PEX_RX6
PEG_RXN_C6 AK20C PEX_RX6#
PEG_RXP_C7 AL20 PEX_RX7
PEG_RXN_C7 AL21C PEX_RX7#
PEG_RXP_C8 AM21 PEX_RX8
PEG_RXN_C8 AM22C PEX_RX8#
PEG_RXP_C9 AK22 PEX_RX9
PEG_RXN_C9 AK23C PEX_RX9#
PEG_RXP_C10 AL23 PEX_RX10
PEG_RXN_C10 AL24C PEX_RX10#
PEG_RXP_C11 AM24 PEX_RX11
PEG_RXN_C11 AM25C PEX_RX11#
PEG_RXP_C12 AK25 PEX_RX12
PEG_RXN_C12 AK26C PEX_RX12#
PEG_RXP_C13 AL26 PEX_RX13
PEG_RXN_C13 AL27C PEX_RX13#
PEG_RXP_C14 AM27 PEX_RX14
PEG_RXN_C14 AM28C PEX_RX14#
PEG_RXP_C15 AL28 PEX_RX15
PEG_RXN_C15 AL29C PEX_RX15#
- NV_GF-GO6600-N-AX (G73M)



**TVMODE(NV43M/G7X)
NTSC (01)**

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball
 0001 16Mx32Infineon
 0010 16Mx32Hynix
 0011 16Mx32Samsung

0101 8Mx32Infineon
 0110 8Mx32Hynix
 0111 8Mx32Samsung

SUBVENDOR

0 (USE SYSTEM BIOS)
 1 (USE EXTERNAL ROM)

MIOAD0 is used to set
 the PCI Express PLL
 termination enable.
 DEFAULT "0"

3GIO_PADCFG[2:0]
 001 for NV43/NV44
 010 for G7X/NV42

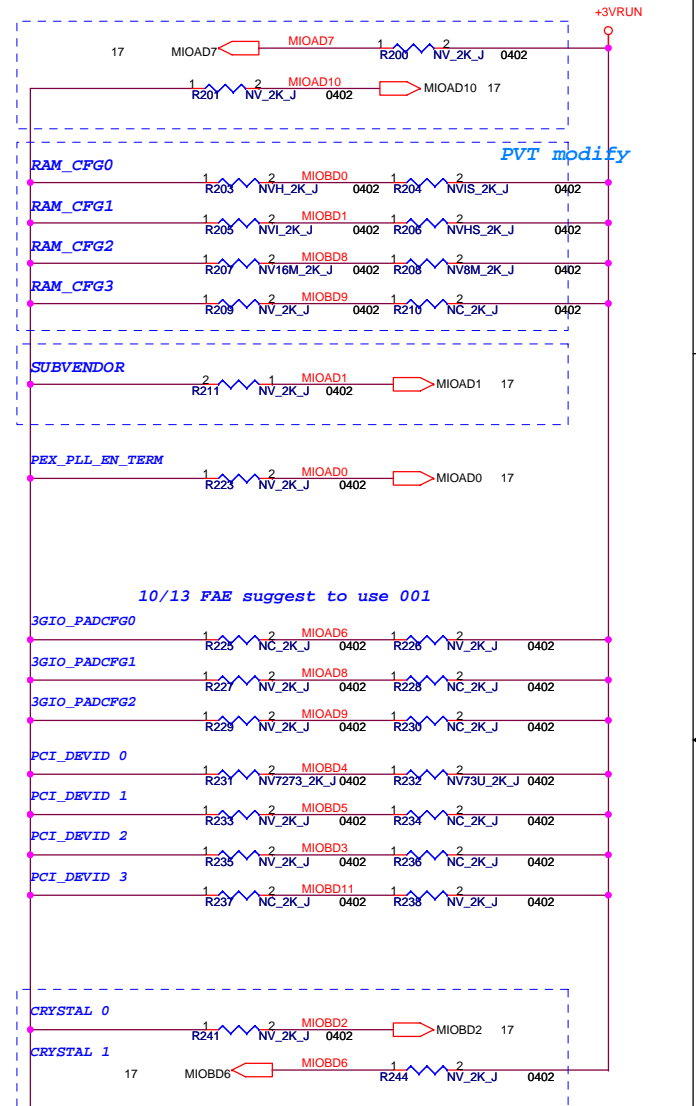
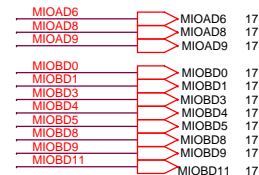
G72M/G73M/NV43M
 PCI_DEVID[3:0]="1000"-->8
 G73M-U
 PCI_DEVID[3:0]="1001"-->9

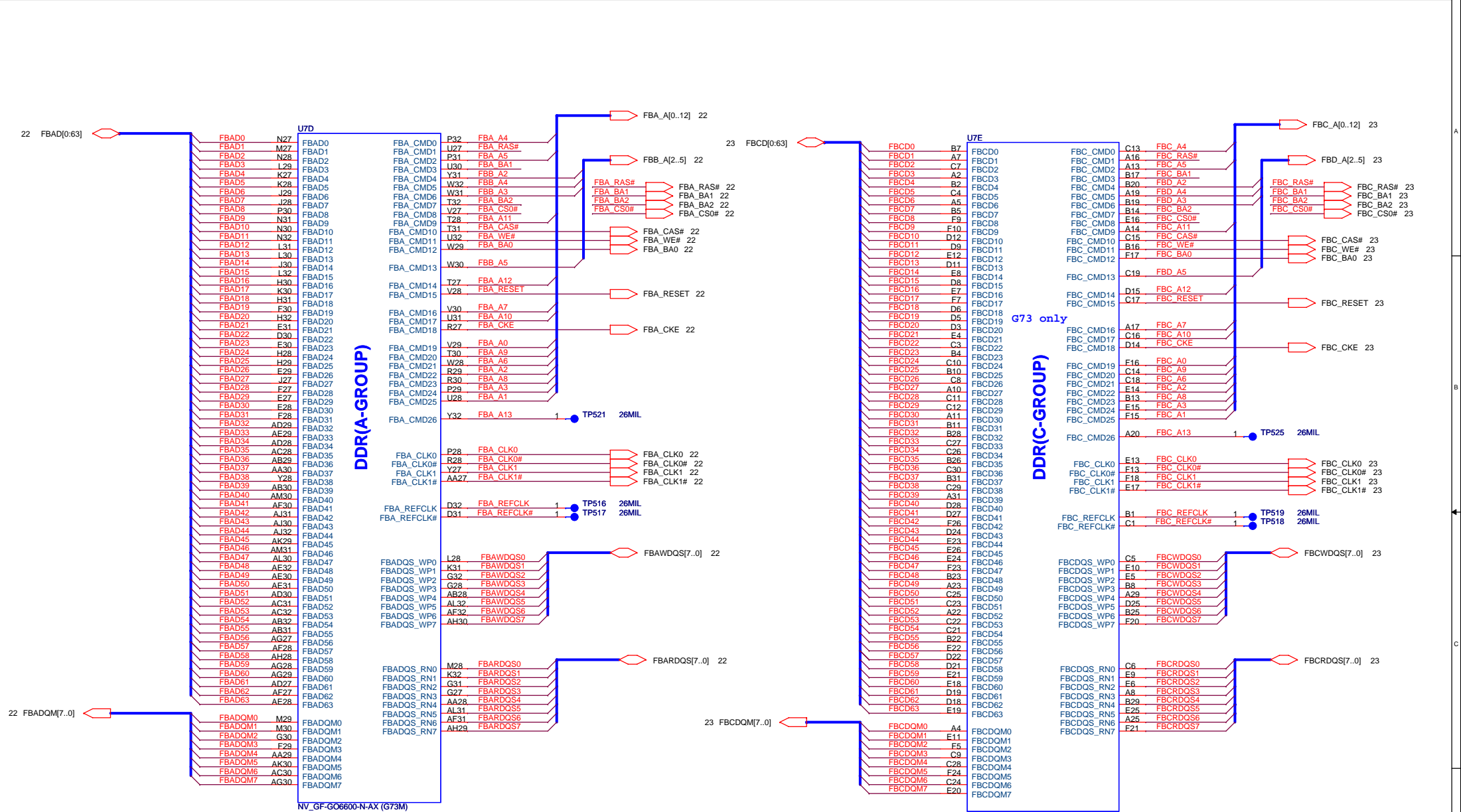
**CRYSTAL(NV43M/G7X)
10 (27M Hz)**

MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

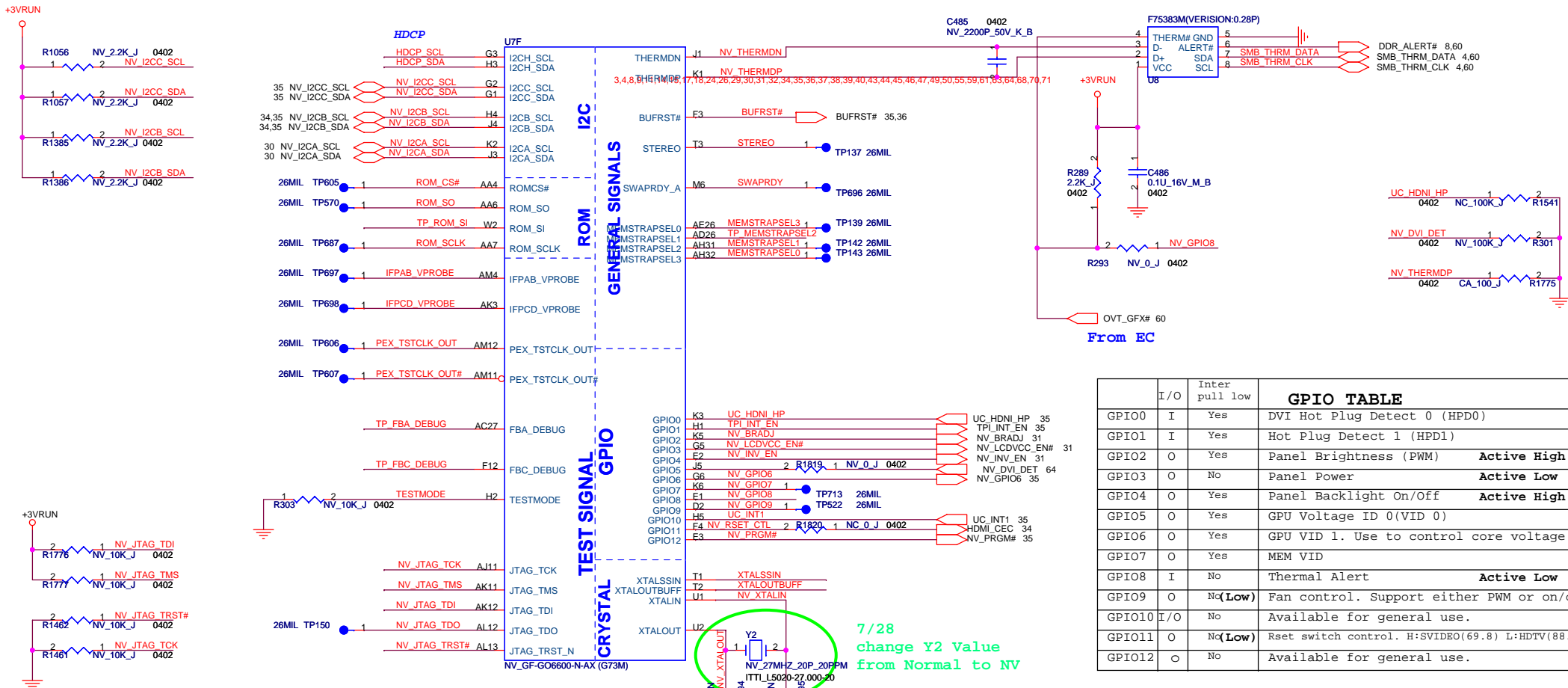
ROM_TYPE(NV43M/G7X) NC
 MIOBD10, MIOBD_HSYNC

00 PARALLEL
 01 SERIAL_AT25F
 10 SERIAL_SST45VF
 11 LPC





SM bus Address :
1001100(BC)
For F75383M



	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	GPU Voltage ID 0(VID 0)
GPIO6	O	Yes	GPU VID 1. Use to control core voltage
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

7/28
change Y2 Value
from Normal to NV

SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

0 = connect to GND
M = unconnected
1 = connect directly to VDD

nVidia support Down -1.25%

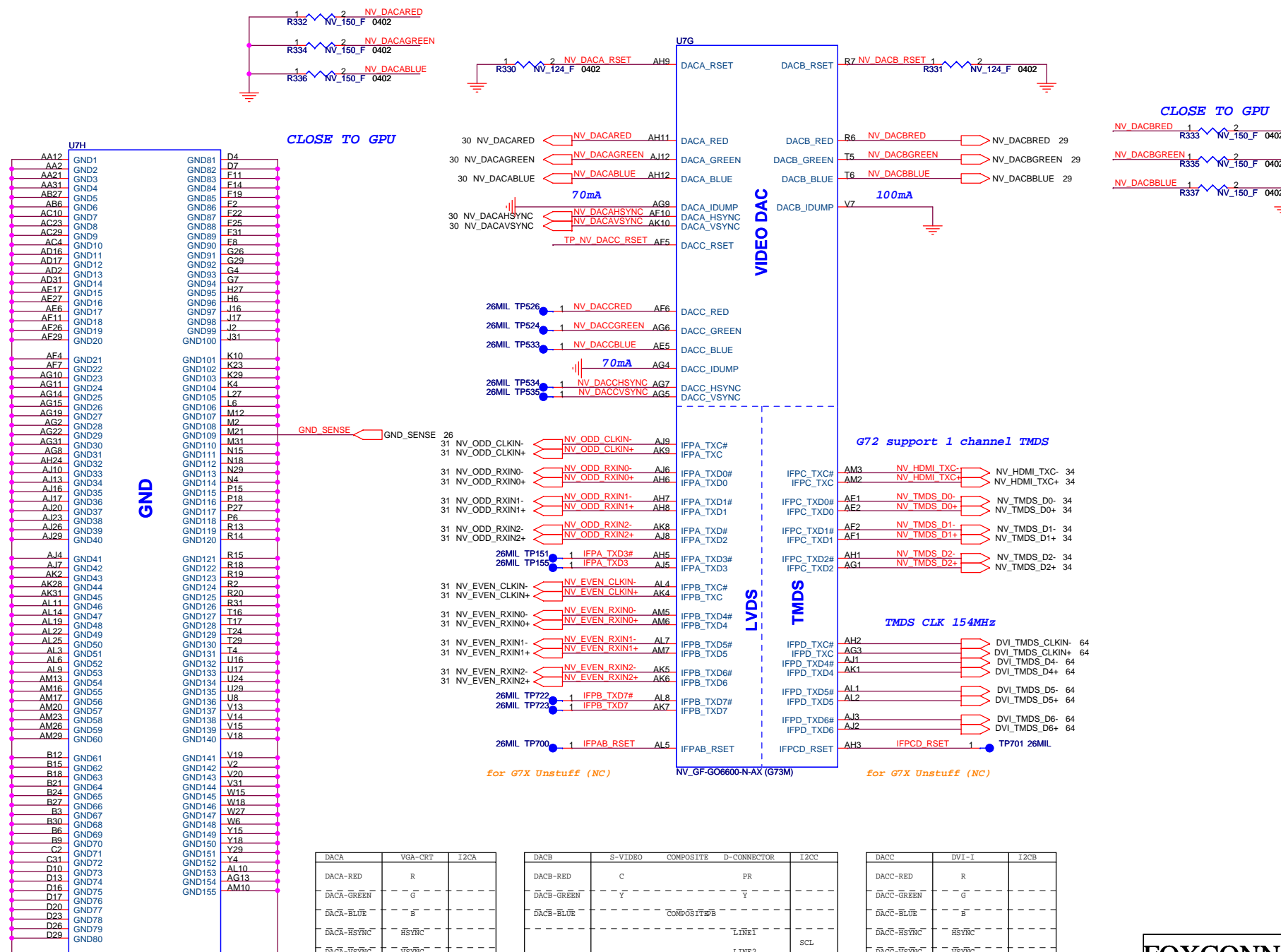
Tis chip can use MK1726 or P1819B

R316 place near GPU
R317 place near spectrum chip

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CCPBG - R&D Division

Title: **VGA (POWER) 7 OF 8**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 20	of 78



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
VGA-DDCCLK	SCL	
VGA-DDCDATA	SDA	

DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		FR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	

DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
DVI-DDCCLK	SCL	
DVI-DDCDATA	SDA	

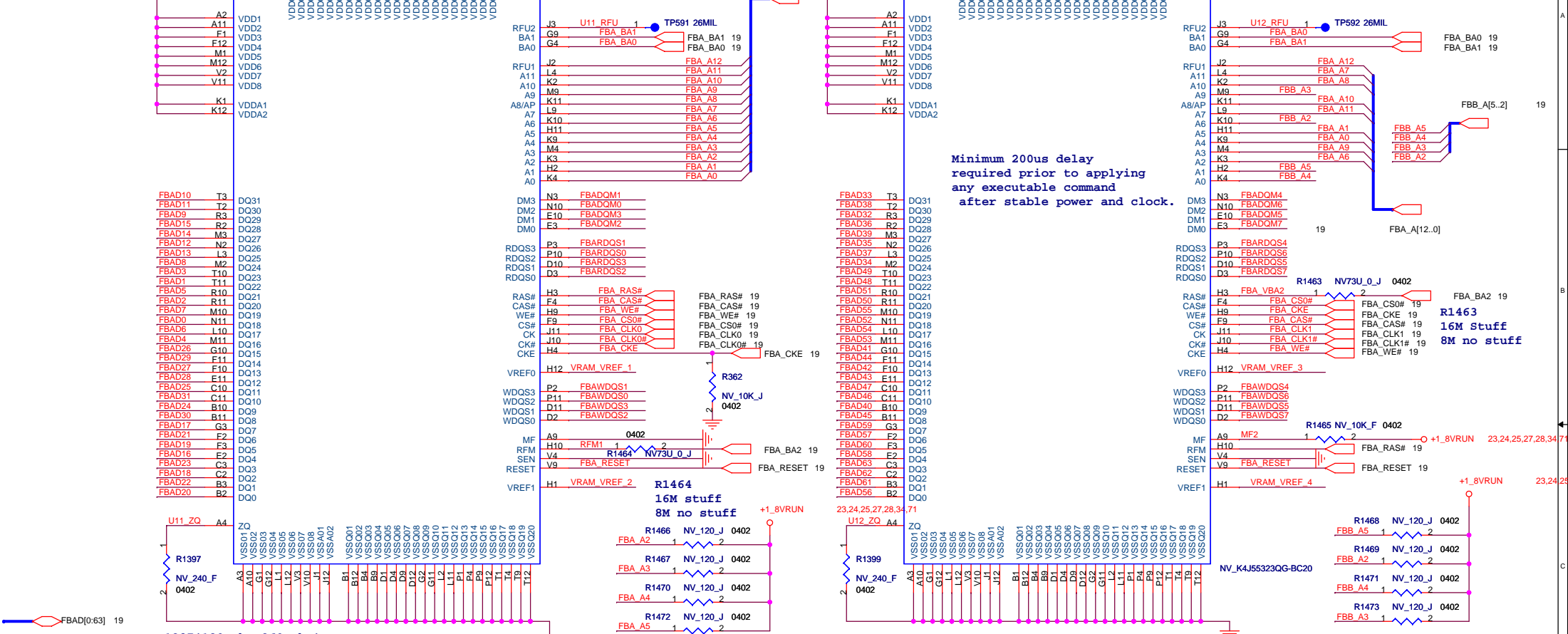
FOXCONN HON HAI Precision Ind. Co., Ltd.
 MS21-1-01 MainBoard (MBX-164) TYPE2
VGA (POWER) 8 of 8
 Size A3 Document Number MS21-1-01 MainBoard (MBX-164) TYPE2 Rev 1.1
 Date: Thursday, August 10, 2006 Sheet 21 of 78

23,24,25,27,28,34,71 +1_8VRUN

23,24,25,27,28,34,71 +1_8VRUN

+1_8VRUN 23,24,25,27,28,34,71

U12 Mirror function on



Minimum 200us delay required prior to applying any executable command after stable power and clock.

R1463 16M Stuff 8M no stuff

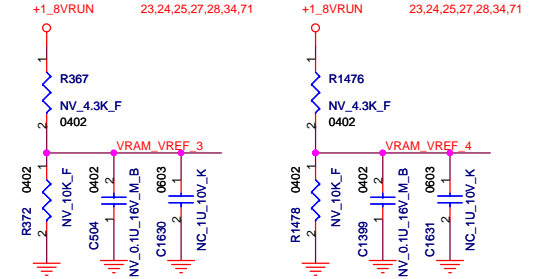
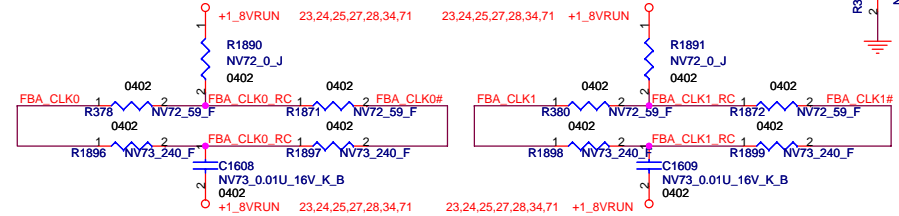
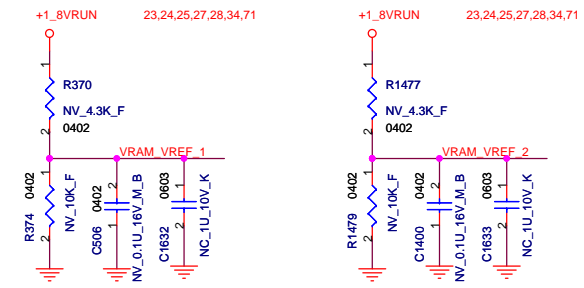
R1397(120 ohm-360 ohm) 240 ohm --> Output impedance 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

R1475 8M Stuff 16M no stuff

FAE suggestion on 10/26 Close to VRAM

	DDR3 (G72M)	DDR3 (G73M) (G73M-U)
R378,R380	60 ohm	240 ohm
R,C 1890	0 ohm	0.01uF



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

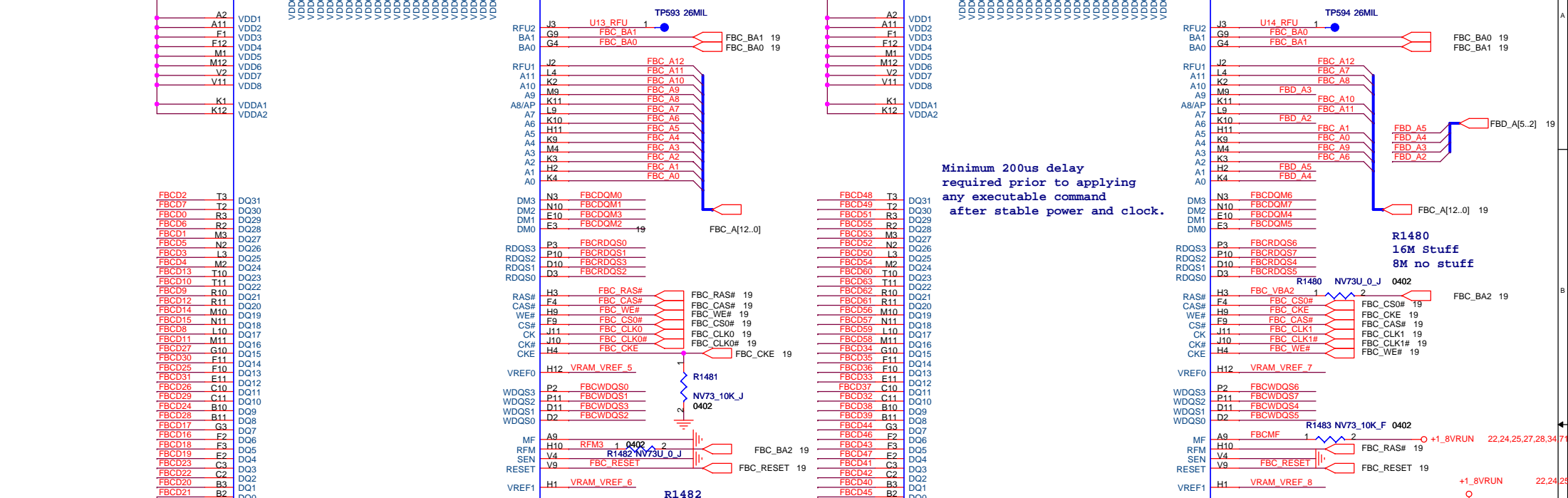
Title VRAM (GDDR) 1 OF 4		
Size A3	Document Number (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 22	of 78

22.24.25.27.28.34.71 +1_8VRUN

22.24.25.27.28.34.71 +1_8VRUN

+1_8VRUN 22.24.25.27.28.34.71

U14
Mirror function on



Minimum 200us delay
required prior to applying
any executable command
after stable power and clock.

R1480
16M Stuff
8M no stuff

R1482
16M stuff
8M no stuff

R1483 NV73_10K_F 0402

R1485 NV73_120_J 0402

R1487 NV73_120_J 0402

R1489 NV73_120_J 0402

R1491 NV73_120_J 0402

11/3 nVidia update

	DDR3 (G72M)	DDR3 (G73M) (G73M-U)
R1502, R1873	40 ohm	240 ohm
R1503, R1874		
C1582, C1583	0 ohm	0.01uF

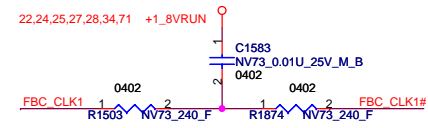
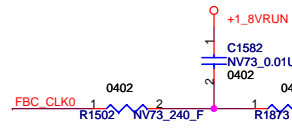
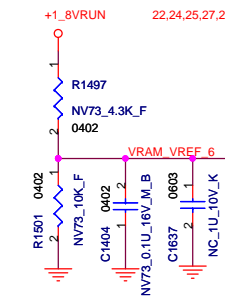
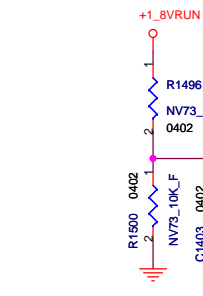
R1493
8M Stuff
16M no stuff

040506
R1493 change part name (G73Only_ -> NV73Only_)
to meet BOM configuration
*PVT already modify (special noties V0.6)

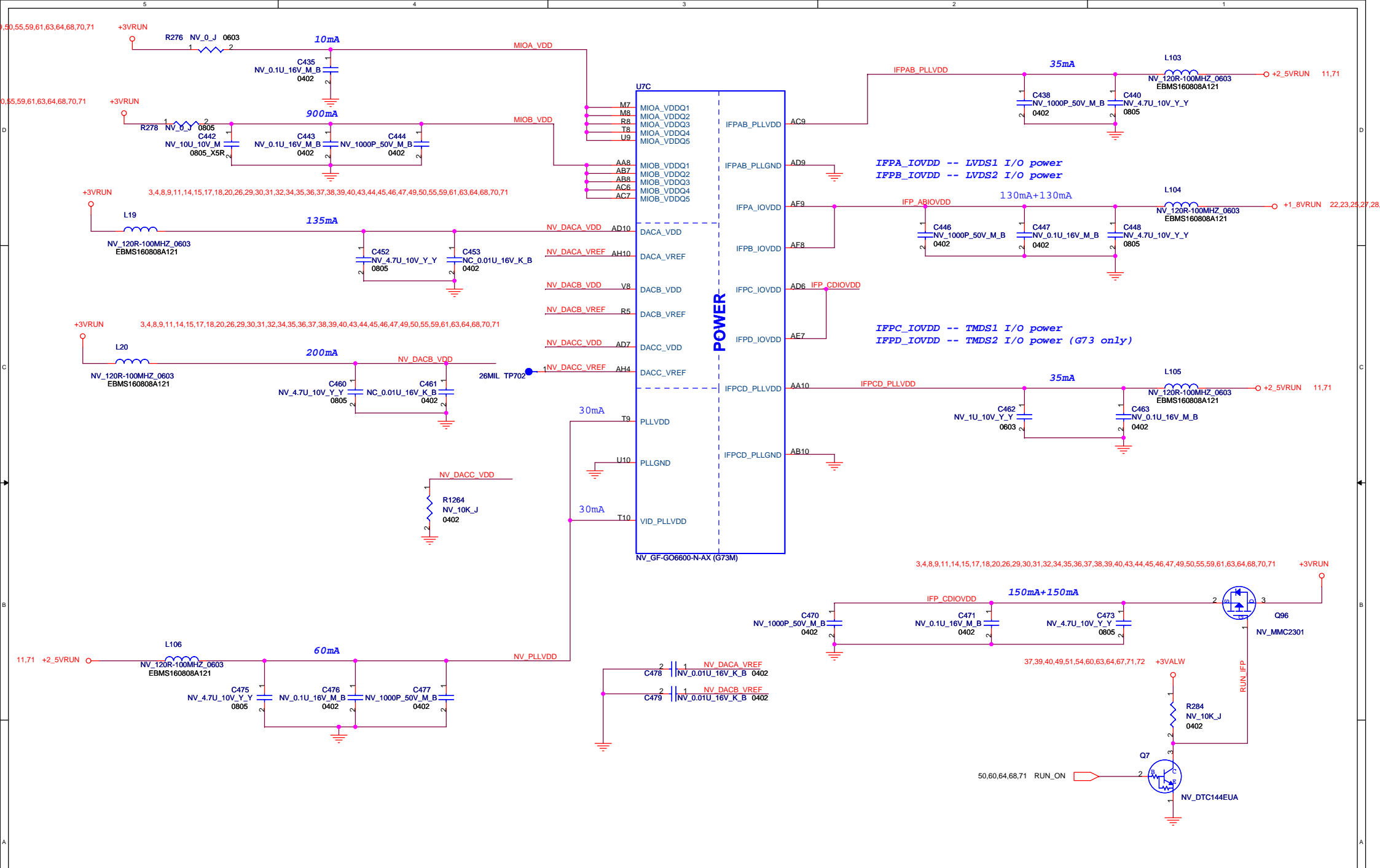
VRAM_VREF is 70%FBVDDQ for GDDR 1.26V

- FBCD[0:63] 19
- FBCDQM[7..0] 19
- FBCRDQS[7..0] 19
- FBCWDQS[7..0] 19

R1414 (120 ohm-360 ohm)
240 ohm --> Output impedance 40 ohm

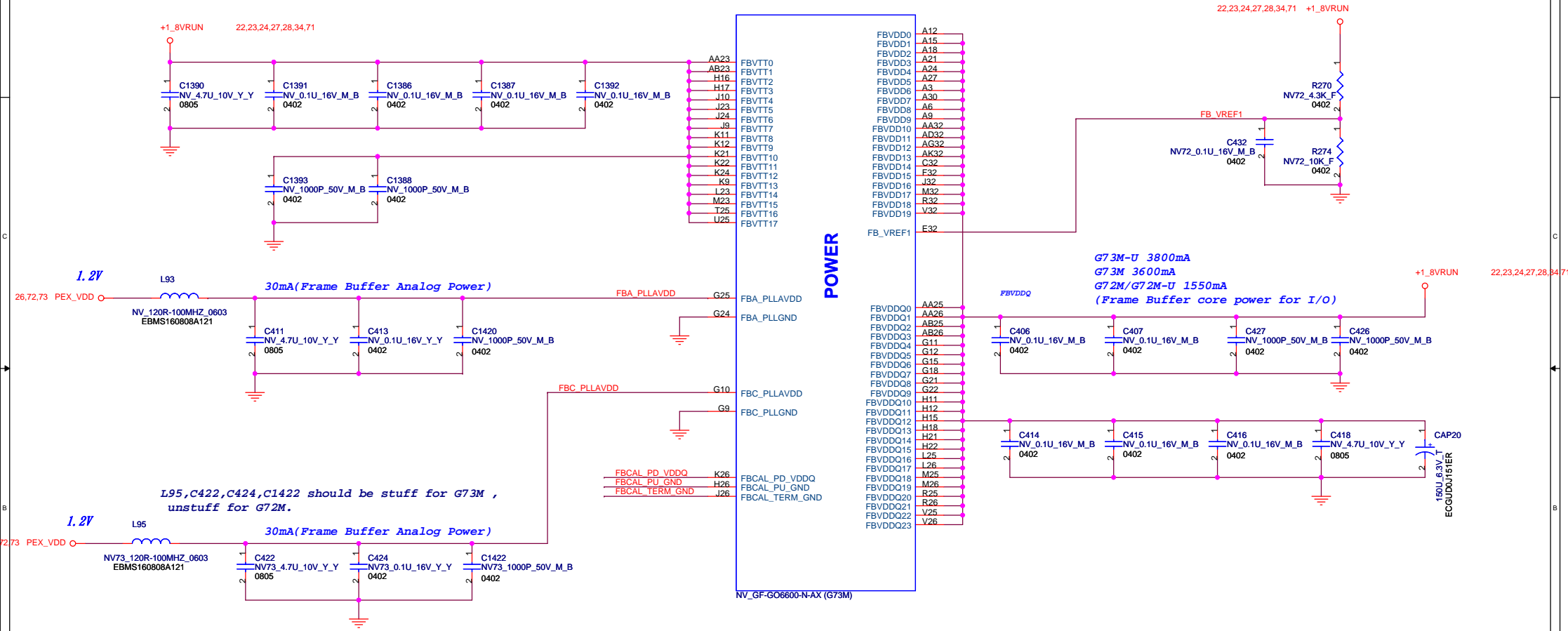


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division



For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.

U71

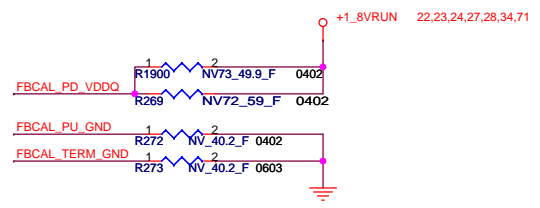


POWER

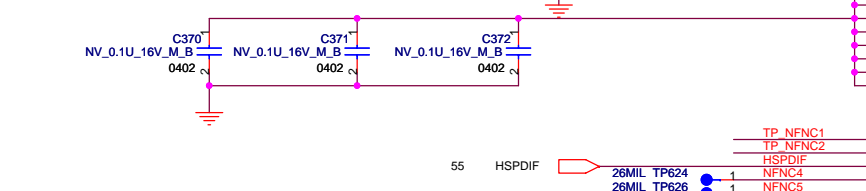
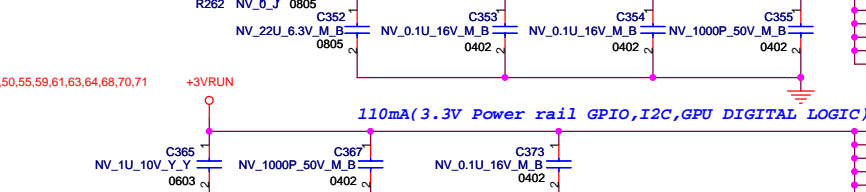
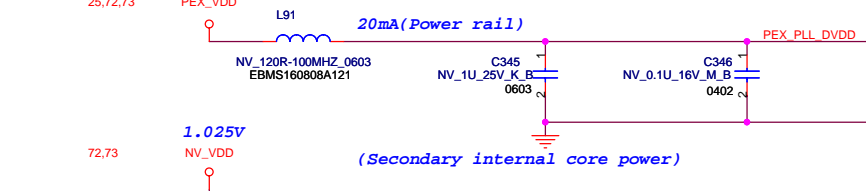
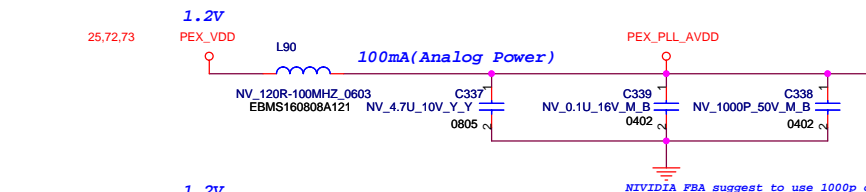
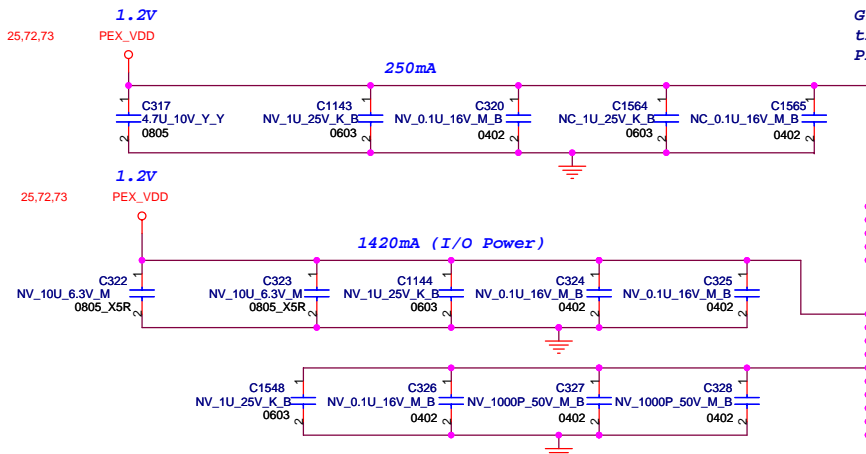
G73M-U 3800mA
 G73M 3600mA
 G72M/G72M-U 1550mA
 (Frame Buffer core power for I/O)

11/3 nVidia update

	DDR1	DDR3(G72M)	DDR3(G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm



G3 design guide require that PEX_IOVDD/Q directly connect to PEX_VDD on page 16.



- U7B
- AD23 PEX_IOVDD0
- AF24 PEX_IOVDD1
- AE23 PEX_IOVDD2
- AF25 PEX_IOVDD4
- AG24 PEX_IOVDD3
- AG25 PEX_IOVDD5
- AC16 PEX_IOVDD00
- AC17 PEX_IOVDD01
- AC21 PEX_IOVDD02
- AC22 PEX_IOVDD03
- AE18 PEX_IOVDD04
- AE21 PEX_IOVDD05
- AE22 PEX_IOVDD06
- AE12 PEX_IOVDD07
- AF18 PEX_IOVDD08
- AF21 PEX_IOVDD09
- AF22 PEX_IOVDD10

- AF15 PEX_PLLAVDD
- AE15 PEX_PLLDVDD
- AE16 PEX_PLLGND

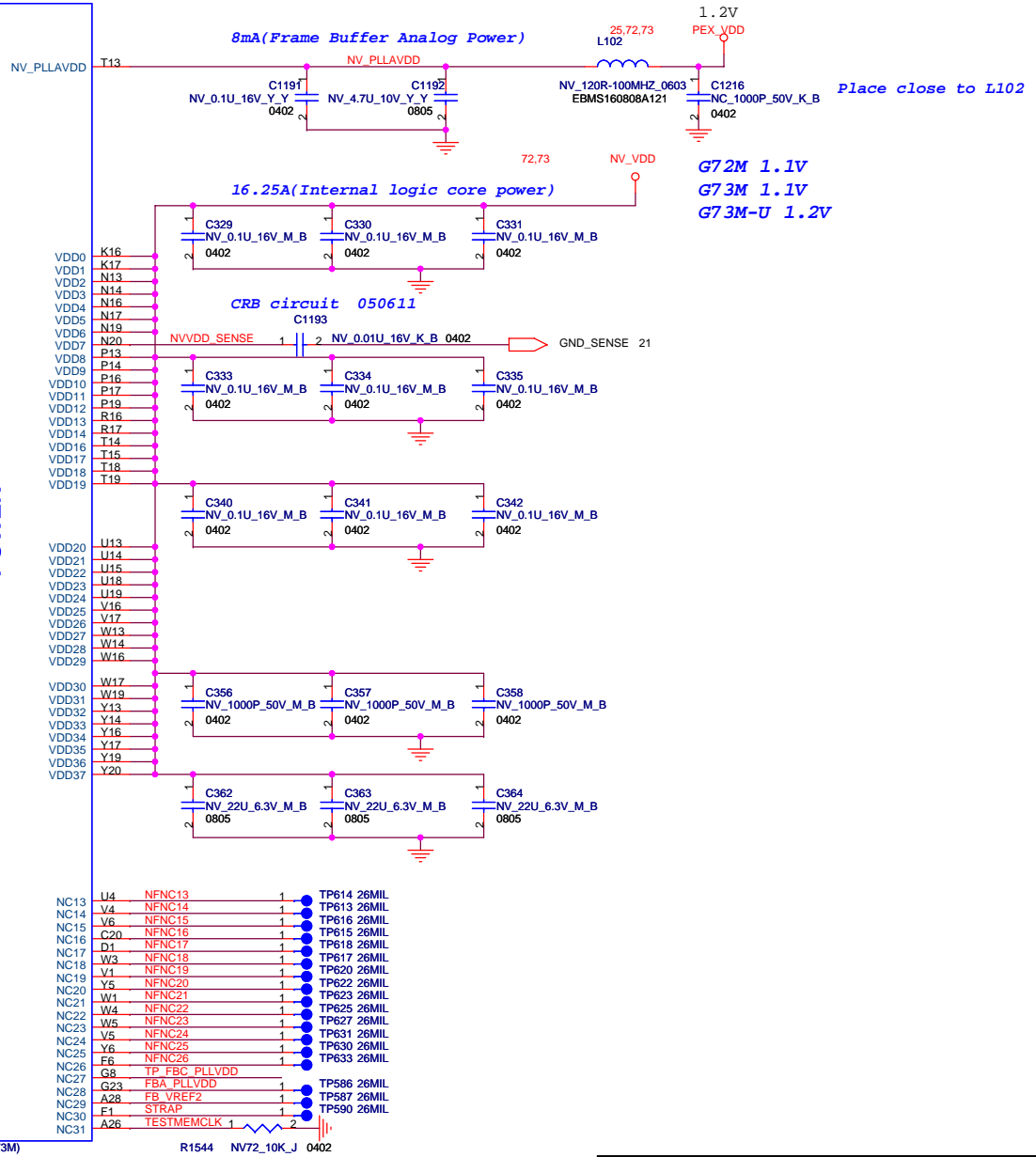
- VDD_LP1
- VDD_LP2
- VDD_LP3
- VDD_LP4
- VDD_LP5
- VDD_LP6

- VDD33_0
- VDD33_1
- VDD33_2
- VDD33_3
- VDD33_4
- VDD33_5
- VDD33_6
- VDD33_7
- VDD33_8
- VDD33_9
- VDD33_10
- VDD33_11
- VDD33_12

- NC1
- NC2
- NC3
- NC4
- NC5
- NC6
- NC7
- NC8
- NC9
- NC10
- NC11
- NC12

NV_GF-G06600-N-AX (G73M)

POWER



- NC13 U4 NFNC13
- NC14 V4 NFNC14
- NC15 V6 NFNC15
- NC16 C20 NFNC16
- NC16 D1 NFNC17
- NC17 W3 NFNC18
- NC18 V1 NFNC19
- NC20 Y6 NFNC20
- NC21 W1 NFNC21
- NC22 W4 NFNC22
- NC23 W5 NFNC23
- NC24 Y6 NFNC25
- NC25 E6 NFNC26
- NC27 G8 TP_FBC_PLLVDD
- NC28 G23 FBA_PLLVDD
- NC29 A28 FB_VREF2
- NC30 F1 STRAP
- NC30 A26 TESTMEMCLK
- NC31 TP614 26MIL
- NC31 TP613 26MIL
- NC31 TP616 26MIL
- NC31 TP615 26MIL
- NC31 TP618 26MIL
- NC31 TP617 26MIL
- NC31 TP620 26MIL
- NC31 TP622 26MIL
- NC31 TP623 26MIL
- NC31 TP625 26MIL
- NC31 TP627 26MIL
- NC31 TP631 26MIL
- NC31 TP630 26MIL
- NC31 TP633 26MIL
- NC31 TP586 26MIL
- NC31 TP587 26MIL
- NC31 TP590 26MIL

R1544 NV72_10K_J 0402
G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K

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 CCPBG - R&D Division

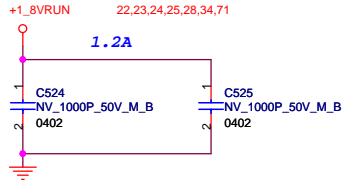
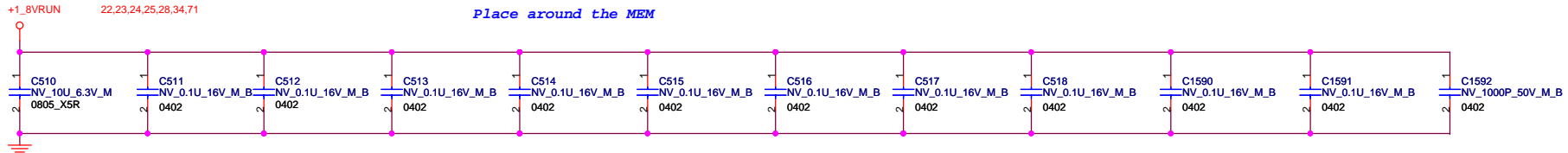
Title **VGA (GDDR/12C/ROM) 4 OF 8**

Size Document Number Rev 1.1
 A3 (MS21-1-01)MainBoard (MBX-164) TYPE2

Date: Thursday, August 10, 2006 Sheet 26 of 78

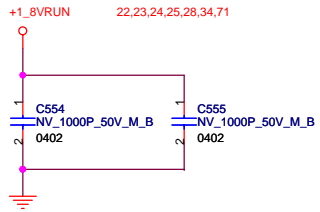
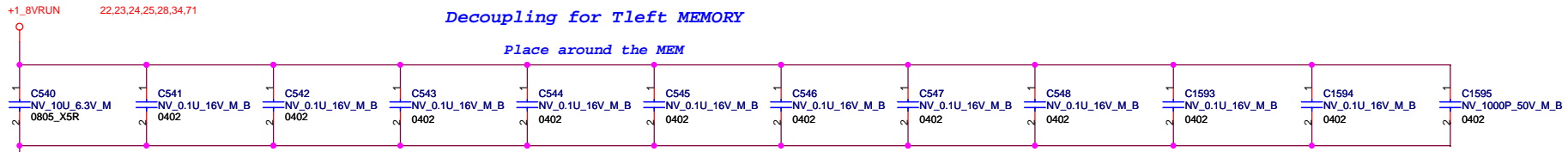
Decoupling for Tright MEMORY

Place around the MEM



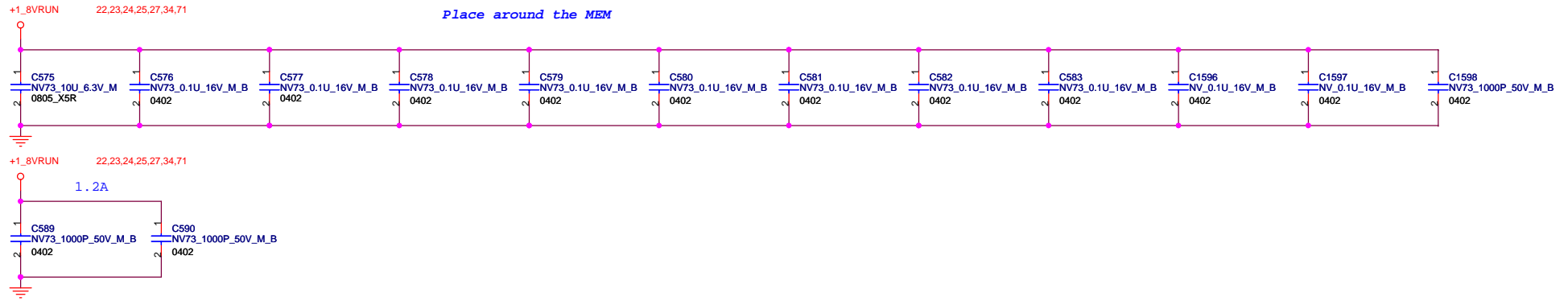
Decoupling for Tleft MEMORY

Place around the MEM



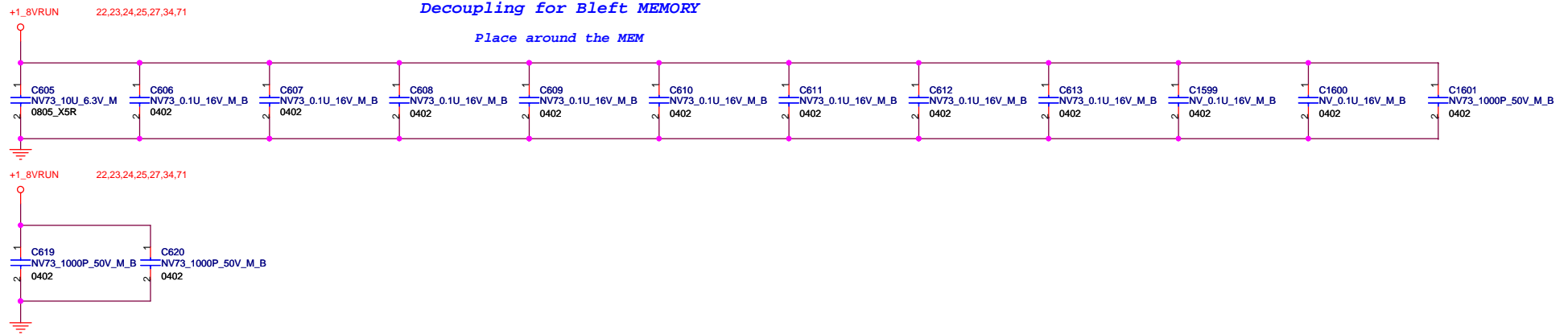
Decoupling for Bright MEMORY

Place around the MEM



Decoupling for Bleft MEMORY

Place around the MEM

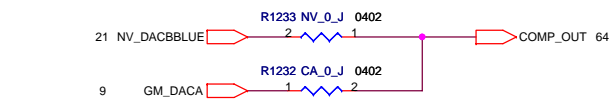
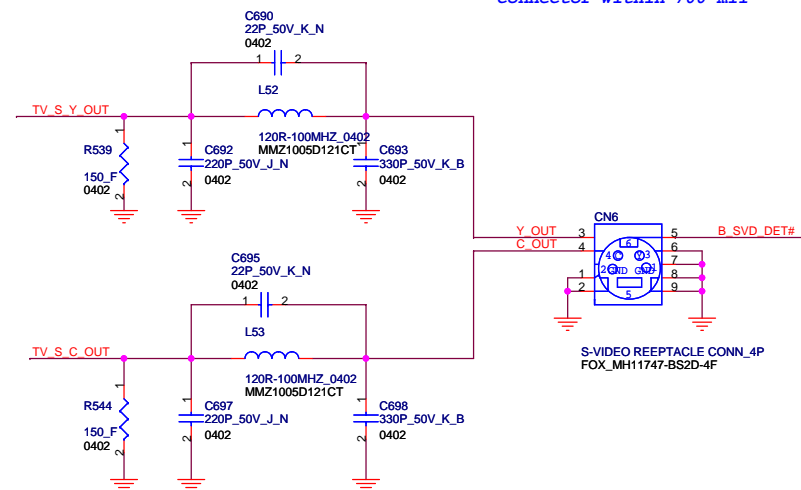
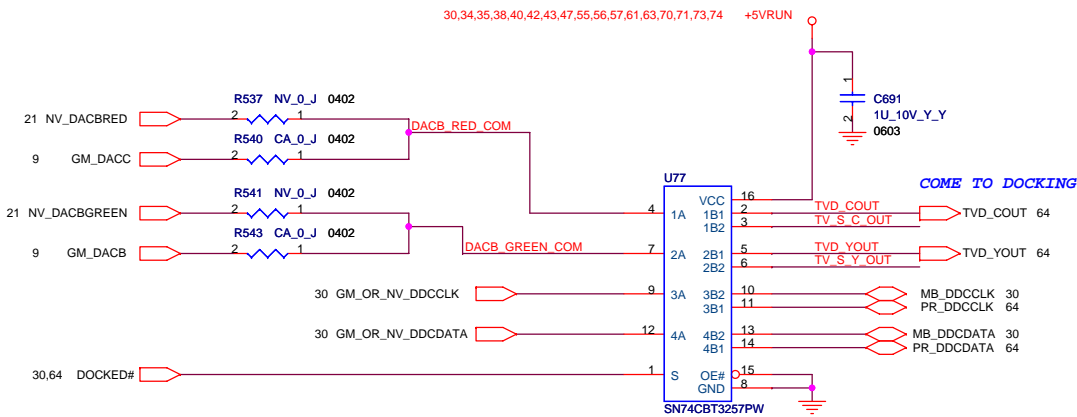


S-VIDEO ANALOG SWITCH

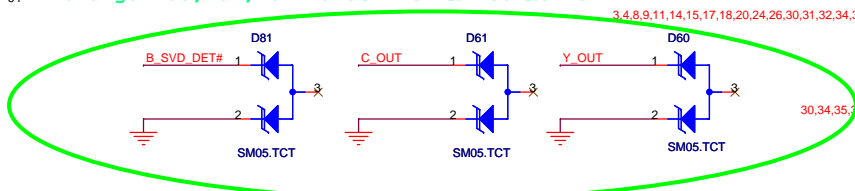
H : S-VIDEO&CVBS
L : PORT REPLICATOR

S-VIDEO

These component close to S-Video connector within 700 mil

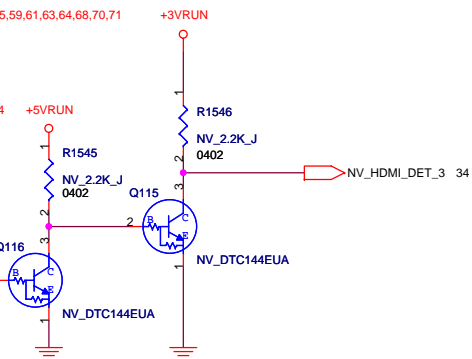
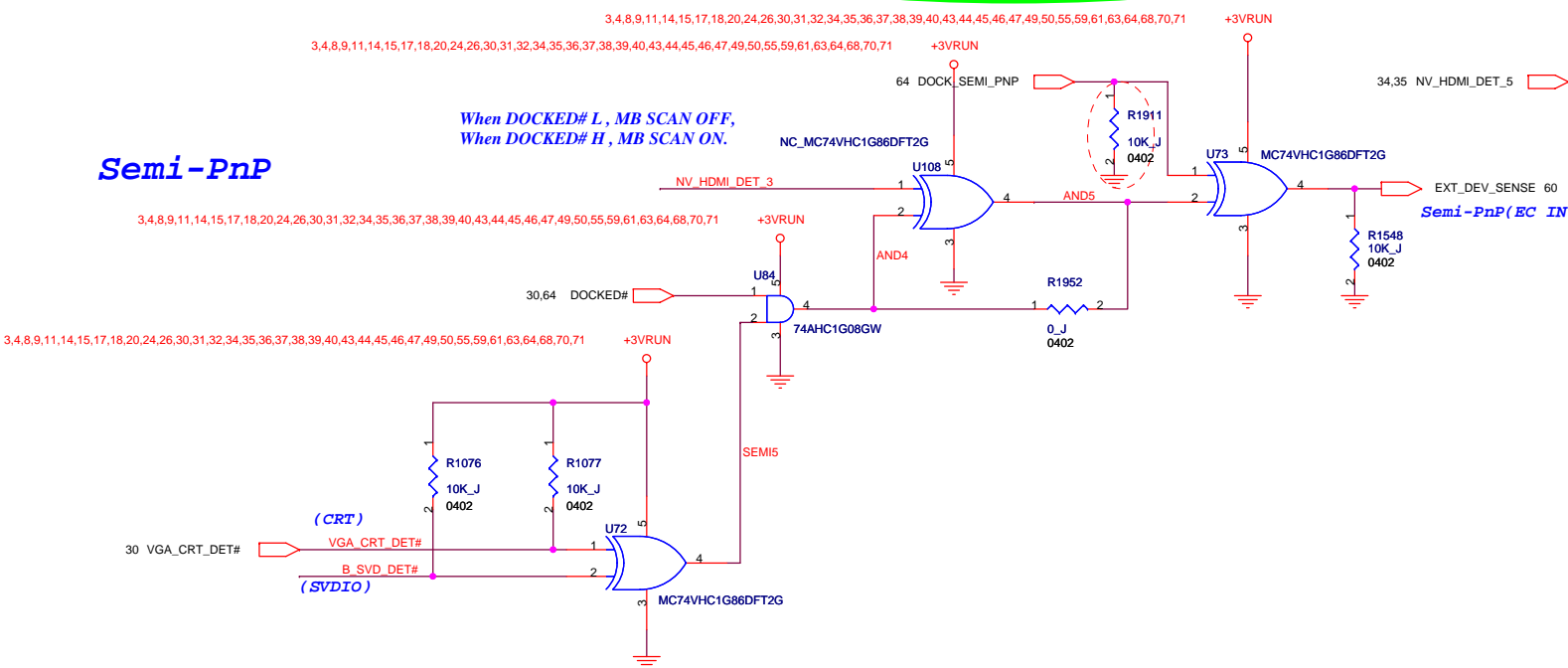


2006/8/7
change D60,D61,D81 Value from NV to Normal

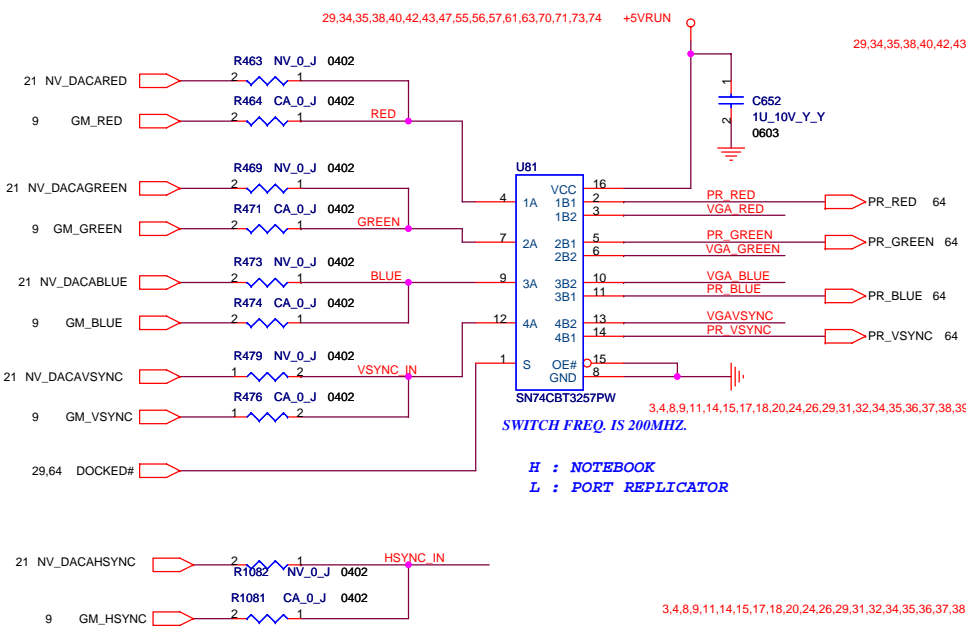


Semi-PnP

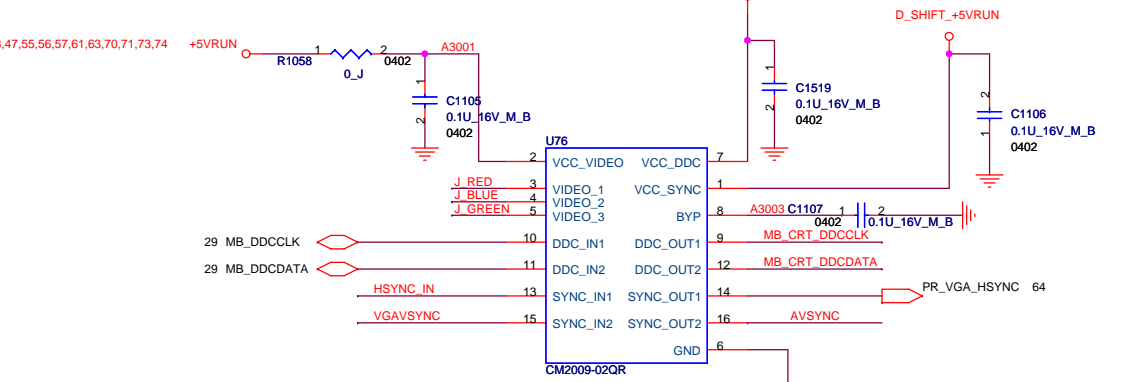
When DOCKED# L, MB SCAN OFF,
When DOCKED# H, MB SCAN ON.



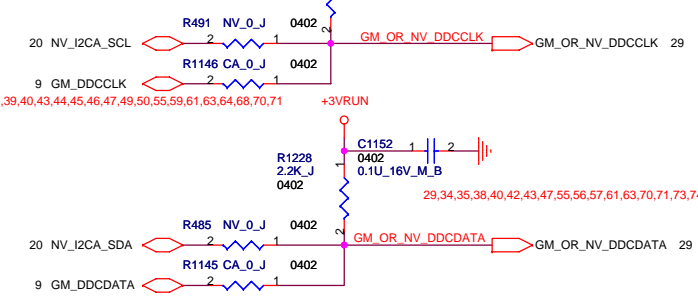
CRT ANALOG SWITCH



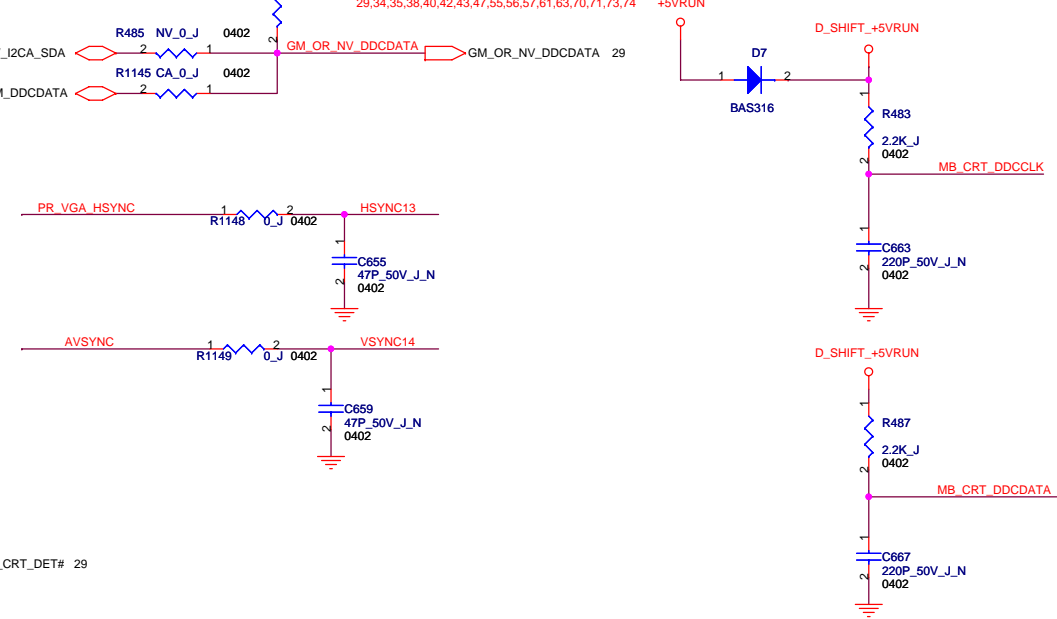
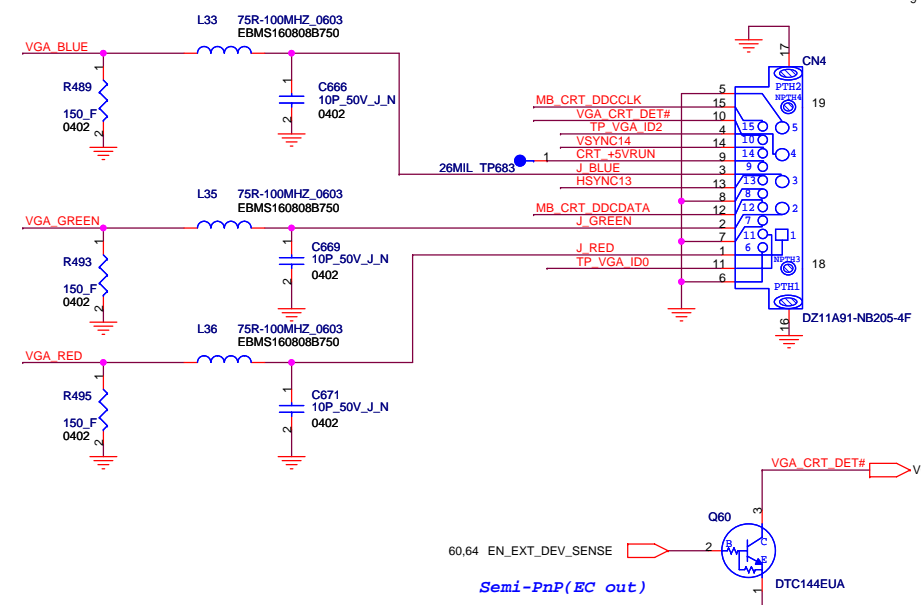
3,4,8,9,11,14,15,17,18,20,24,26,29,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71



5/12
Follow Intel FAE suggest GM_DDCCLK and GM_DDCDATA are 3.3V tolerance signals from Callstoga



CRT CONNECTOR

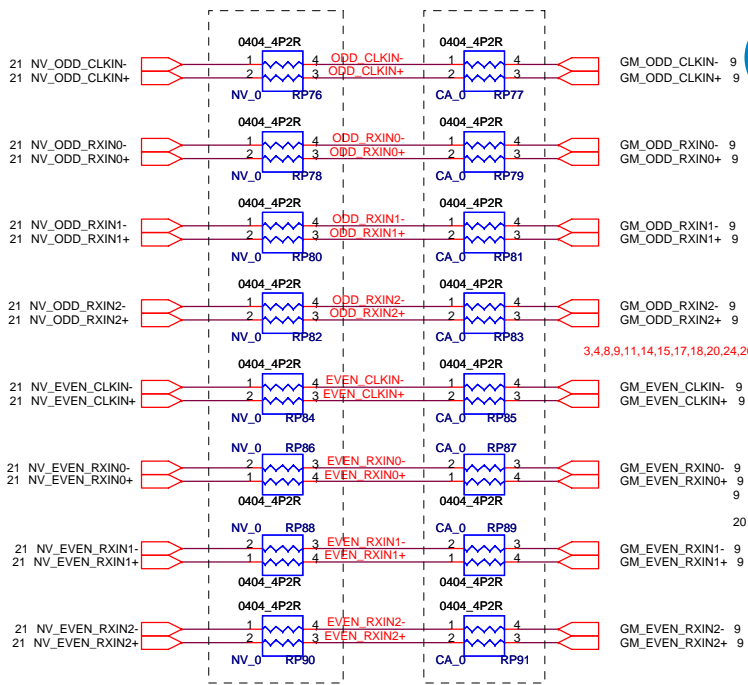


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CRT	
Size	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date:	Thursday, August 10, 2006	Sheet 30 of 78

LVDS

Group1

Group2

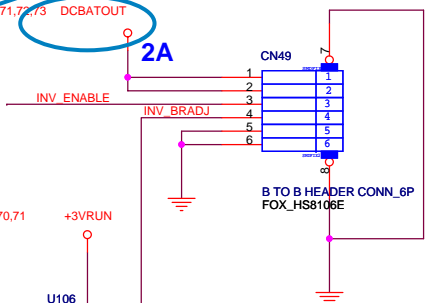
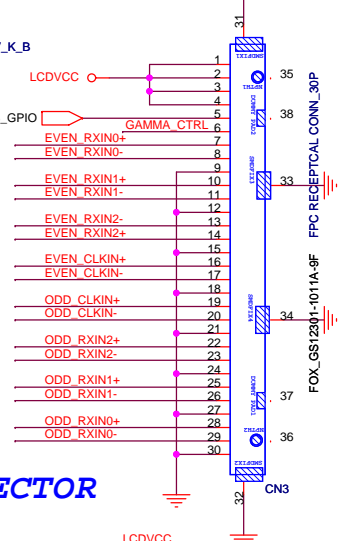


2006/6/26
 (Del inverter boost circuit, after change, the inverter circuit is the same with MS20 MP)
 Detail change list
 Delete PR426&PR427 and change C604-1, C1557-1, C1558-1, CN49pin1, pin2 net name INVERTER_VCC to net DCBATOUT.

Place C640 and C1558 close to CN49.

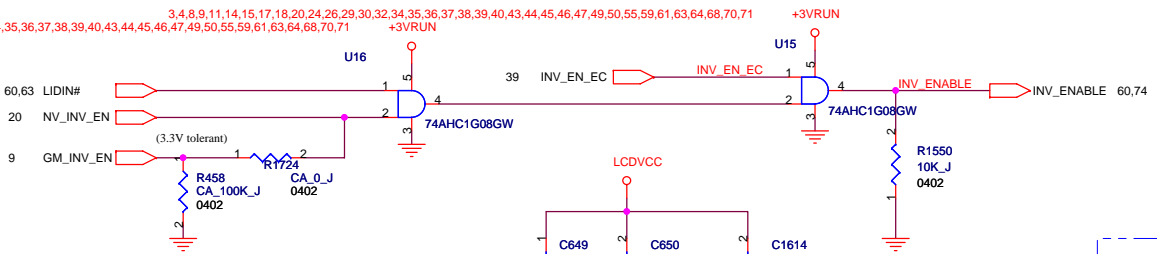
66,67,68,69,70,71,72,73 DCBATOUT

LVDS CONNECTOR

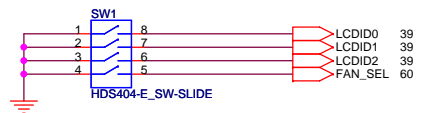


INVERTER CONNECTOR

U106, U15, U16 can use ON (MC74VHC1G08DFT2G)
 H.H. PN: 14-MC74VHC-1G04



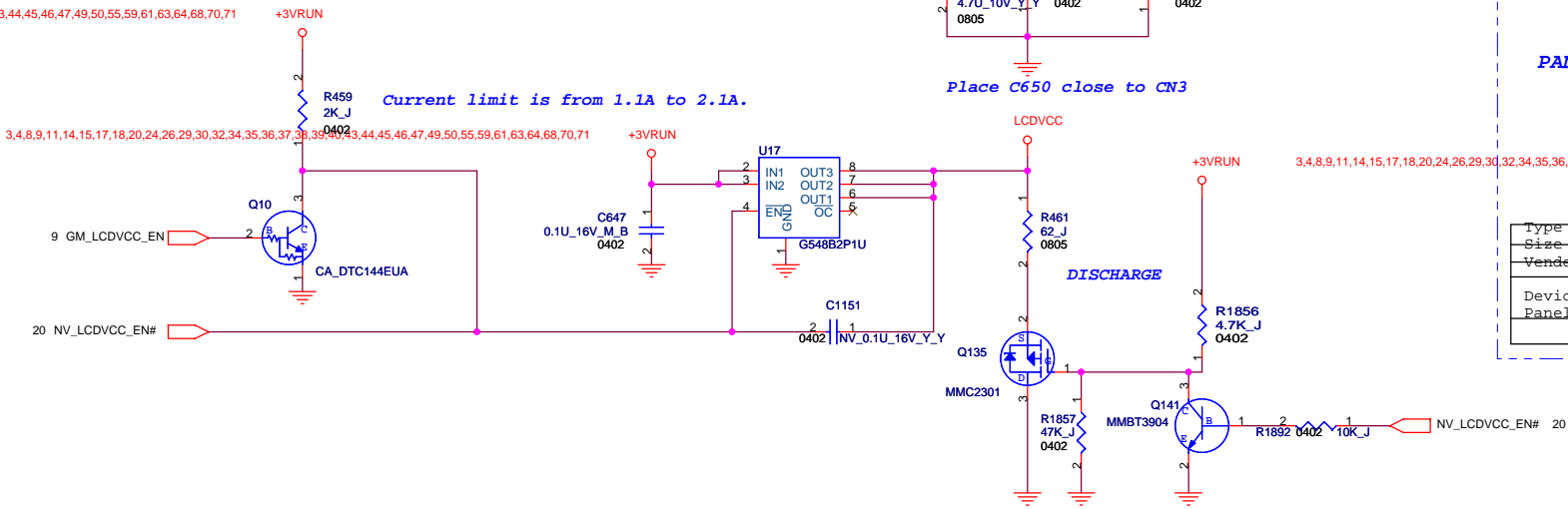
PANEL ID



FAN_SEL:
 H: Foxconn FAN
 L: MOR cooling unit

Current limit is from 1.1A to 2.1A.

Place C650 close to CN3



Type	WXGA+	WXGA+	WUXGA
Size	17" wide	17" wide	17" wide
Vender	LG-PHILIPS	LG-PHILIPS	SHARE
Device Name	LP171WP7-1LA1	LP171WX2-A4K3	LQ170M1LA04
Panel ID Check[3..0]	0001	0010	0100

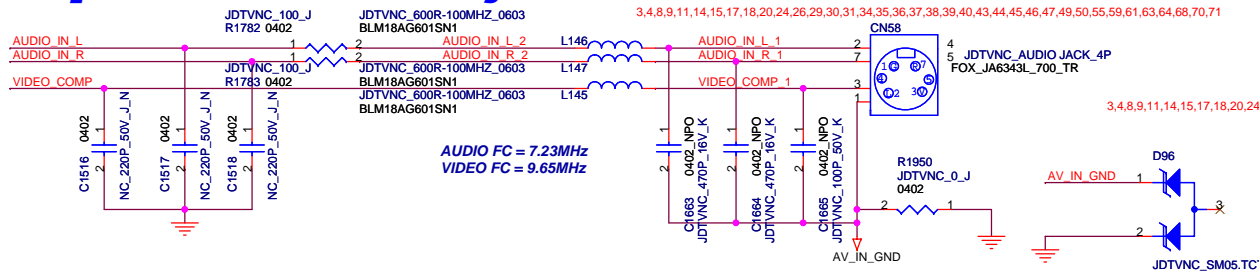
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **LVDS**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
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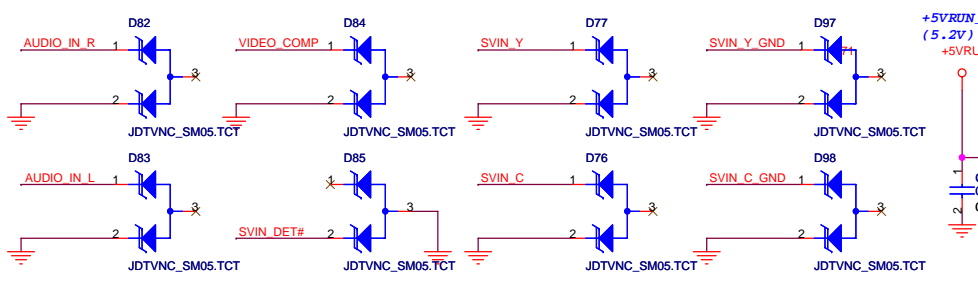
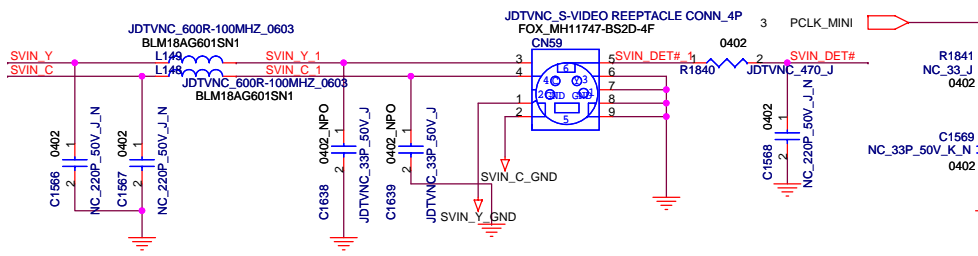
Date: Thursday, August 10, 2006 Sheet 31 of 78

Special mini stereo jack



040406 Modify BOM roul
 (1)Mini PCI socket circuit group change part neam from TV_ to normal.
 (2)Special mini stereo jack and S-VIDEO in group change part name from TV_ to JDTVNC_
 (JP digital tuner sku & No tuner SKU NOT stuff)

S-VIDEO IN

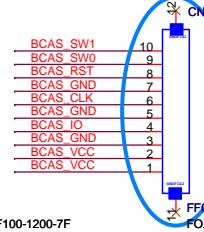
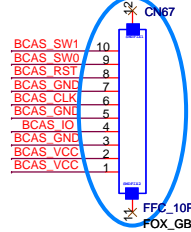


B-CAS connentor

(Close to TV Tuner)

FFC CONNECT TO TV TUNER BOARD

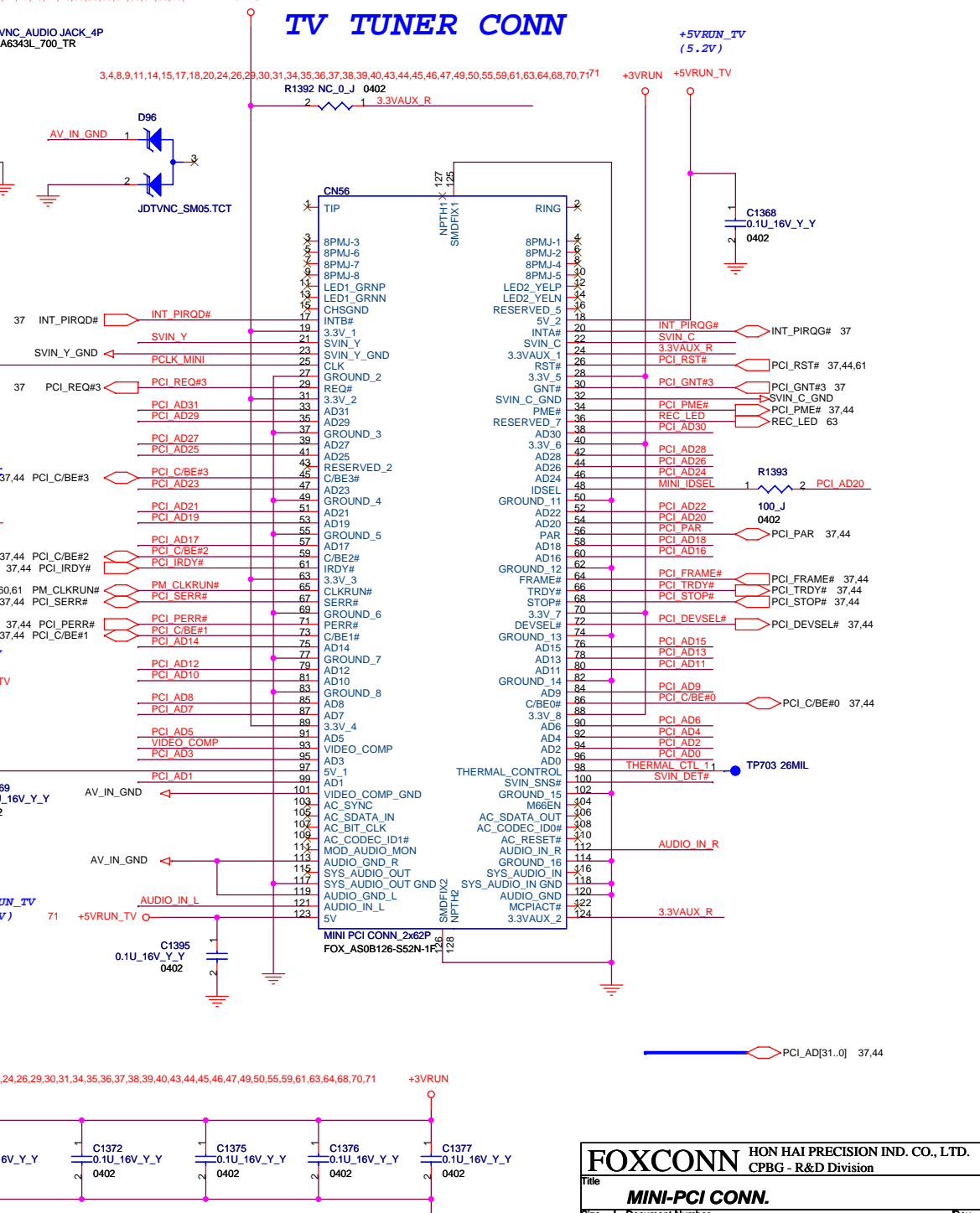
(FOR JP DIAGITAL)



BFT Test Pad

BCAS SW1	TP725	tpc32l_100
BCAS SW0	TP727	tpc32l_100
BCAS RST	TP726	tpc32l_100
BCAS CLK	TP728	tpc32l_100
BCAS IO	TP729	tpc32l_100
BCAS GND	TP731	tpc32l_100
BCAS VCC	TP730	tpc32l_100

TV TUNER CONN

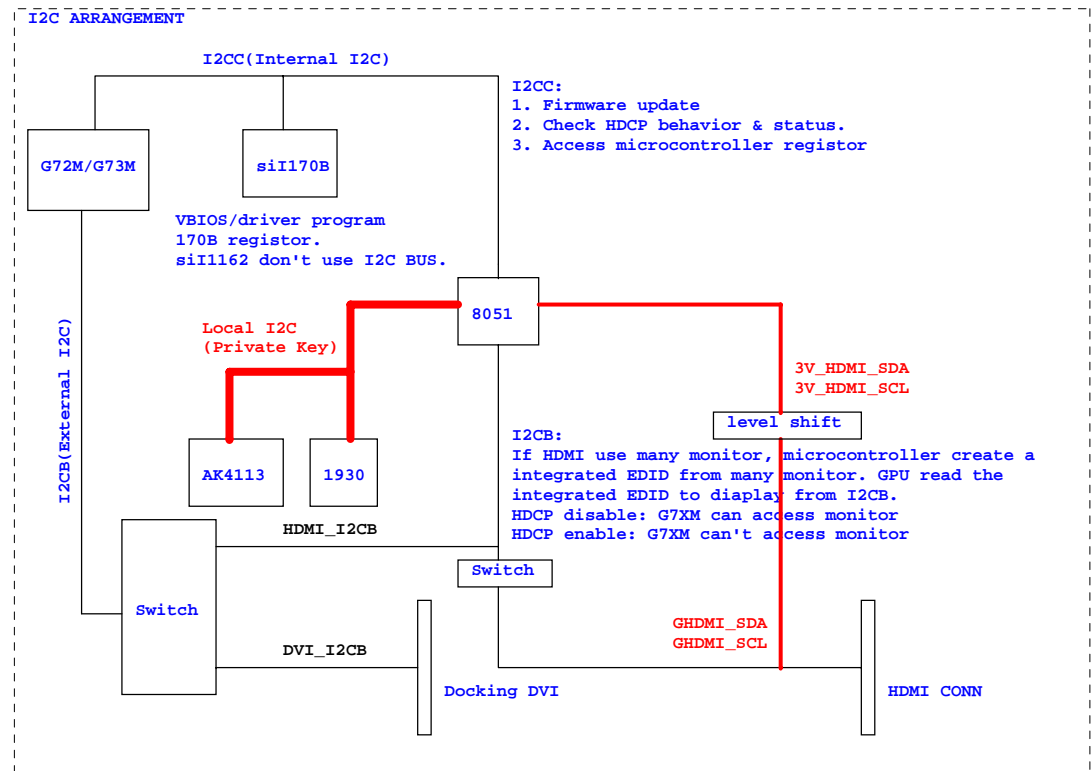
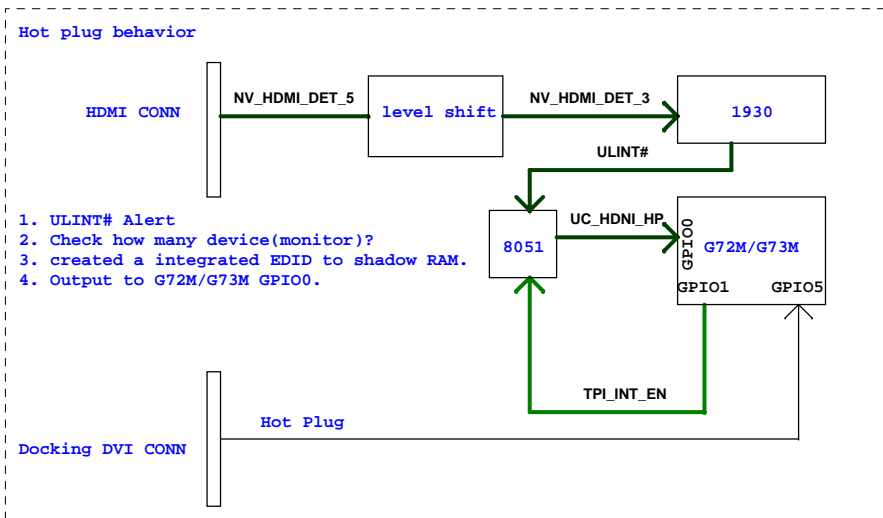


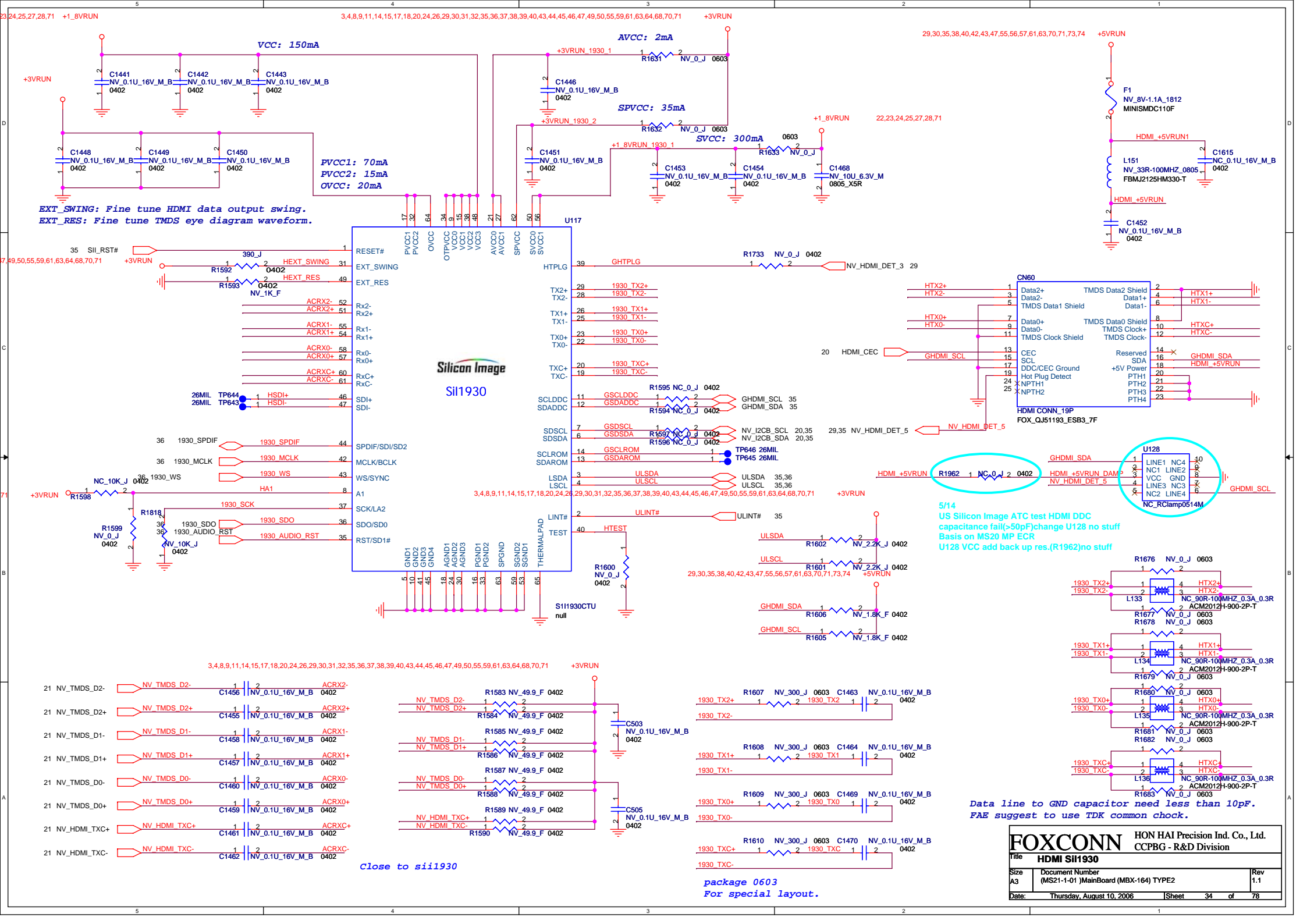
TV-TUNER not support CLKRUN

CN62, CN67 Change from MOLEX to FOXCONN

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	MINI-PCI CONN.
Size	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2
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Rev	1.1

Hot plug behavior & I2C ARRANGEMENT block diagram





EXT_SWING: Fine tune HDMI data output swing.
 EXT_RES: Fine tune TMDS eye diagram waveform.

PVCC1: 70mA
 PVCC2: 15mA
 OVCC: 20mA

AVCC: 2mA
 SPVCC: 35mA
 SVCC: 300mA



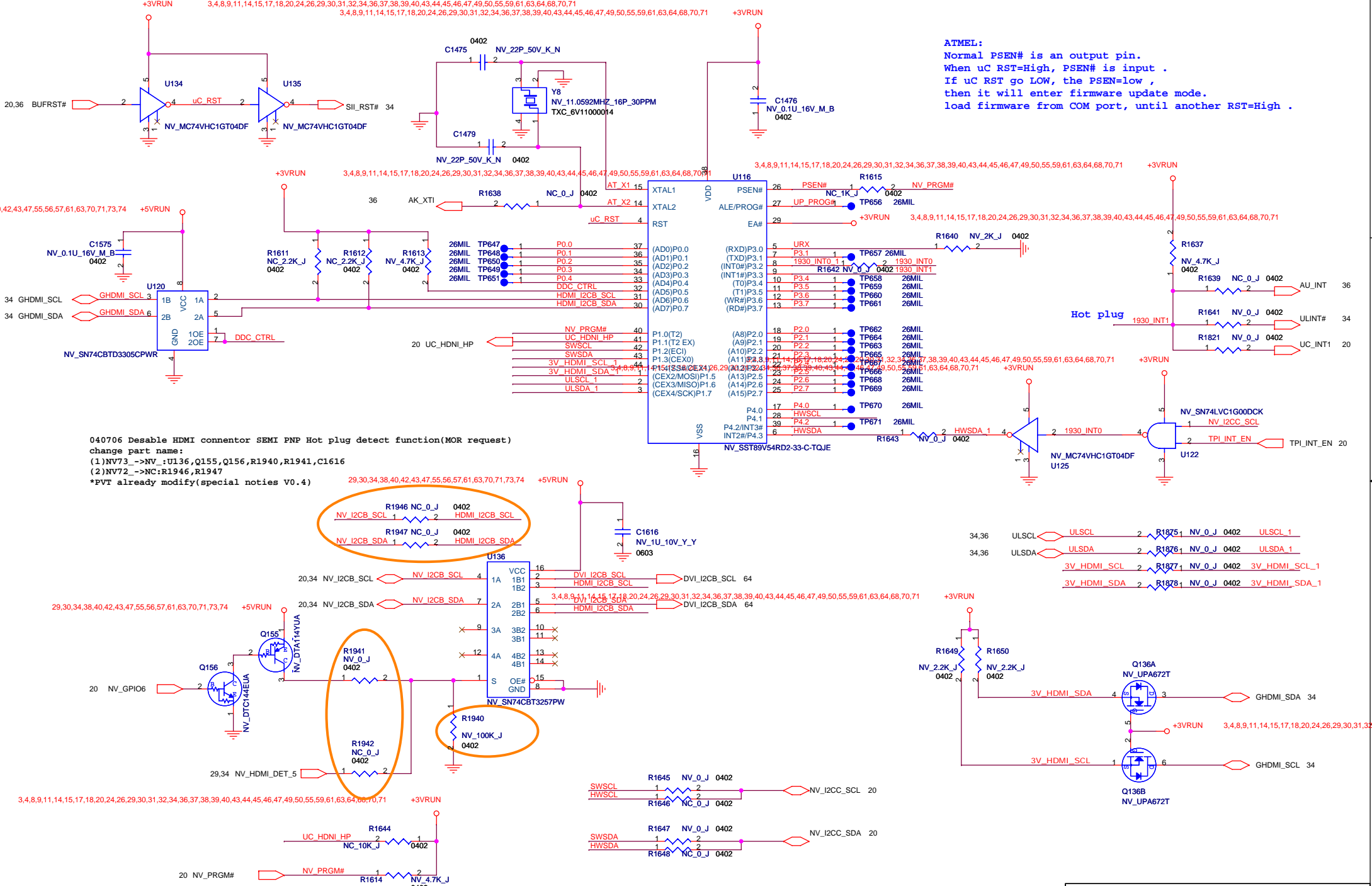
5/14
 US Silicon Image ATC test HDMI DDC
 capacitance fail(>50pF)change U128 no stuff
 Basis on MS20 MP ECR
 U128 VCC add back up res.(R1962)no stuff

Data line to GND capacitor need less than 10pF.
 FAE suggest to use TDK common chock.

Close to sii1930

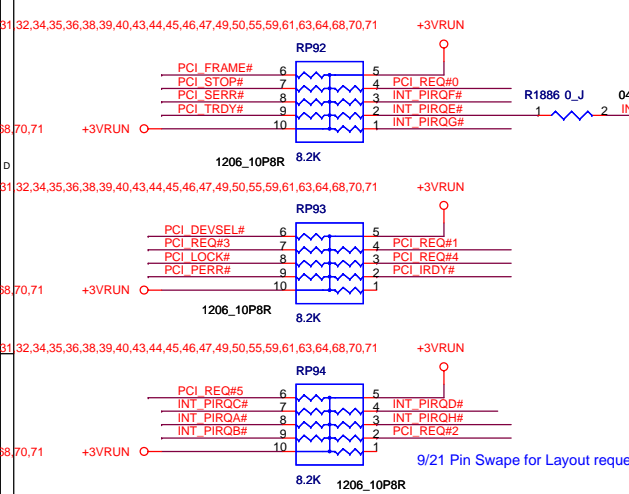
package 0603
 For special layout.

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
File	HDMI SiI1930	
Size	Document Number	Rev
A3	(MS21-1-01)MainBoard (MBX-164) TYPE2	1.1
Date:	Thursday, August 10, 2006	Sheet 34 of 78

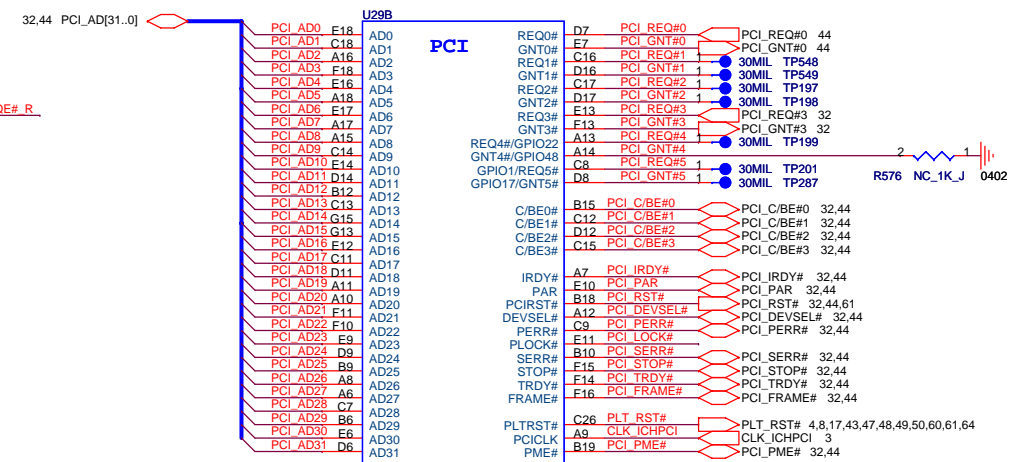


ATMEL:
 Normal PSEN# is an output pin.
 When uC RST=High, PSEN# is input .
 If uC RST go LOW, the PSEN=low ,
 then it will enter firmware update mode.
 load firmware from COM port, until another RST=High .

040706 Desable HDMI connentor SEMI PNP Hot plug detect function(MOR request)
 change part name:
 (1)NV73_ ->NV :U136,Q155,Q156,R1940,R1941,C1616
 (2)NV72_ ->NC:R1946,R1947
 *PVT already modify(special noties V0.4)

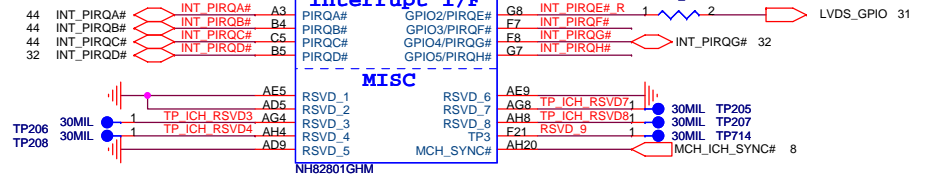


PCI Pullups



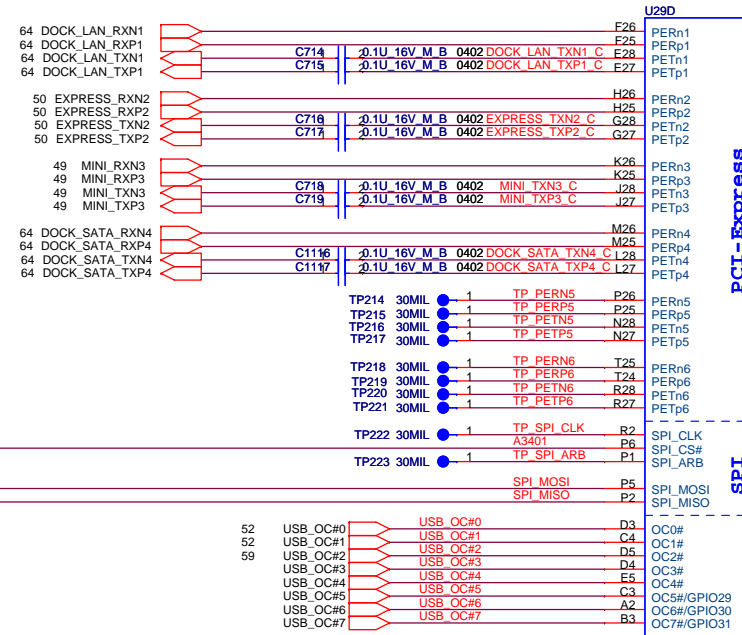
Interrupt I/F

MISC



Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	HI	HI
PCI	HI	LOW



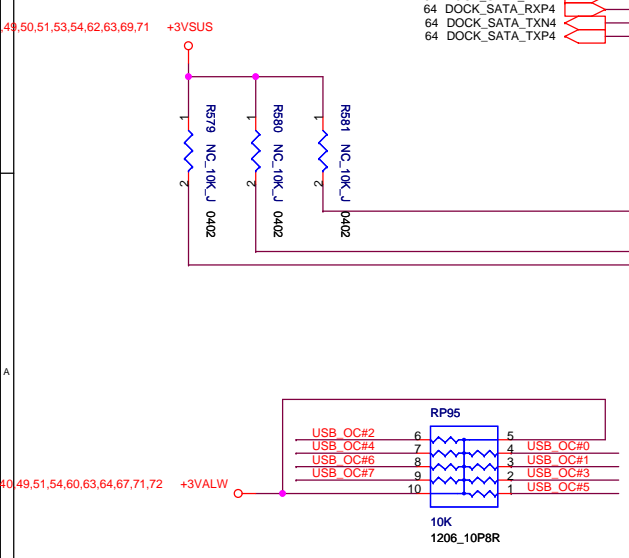
Direct Media Interface

SPI

USB

Place within 500 mils of ICH

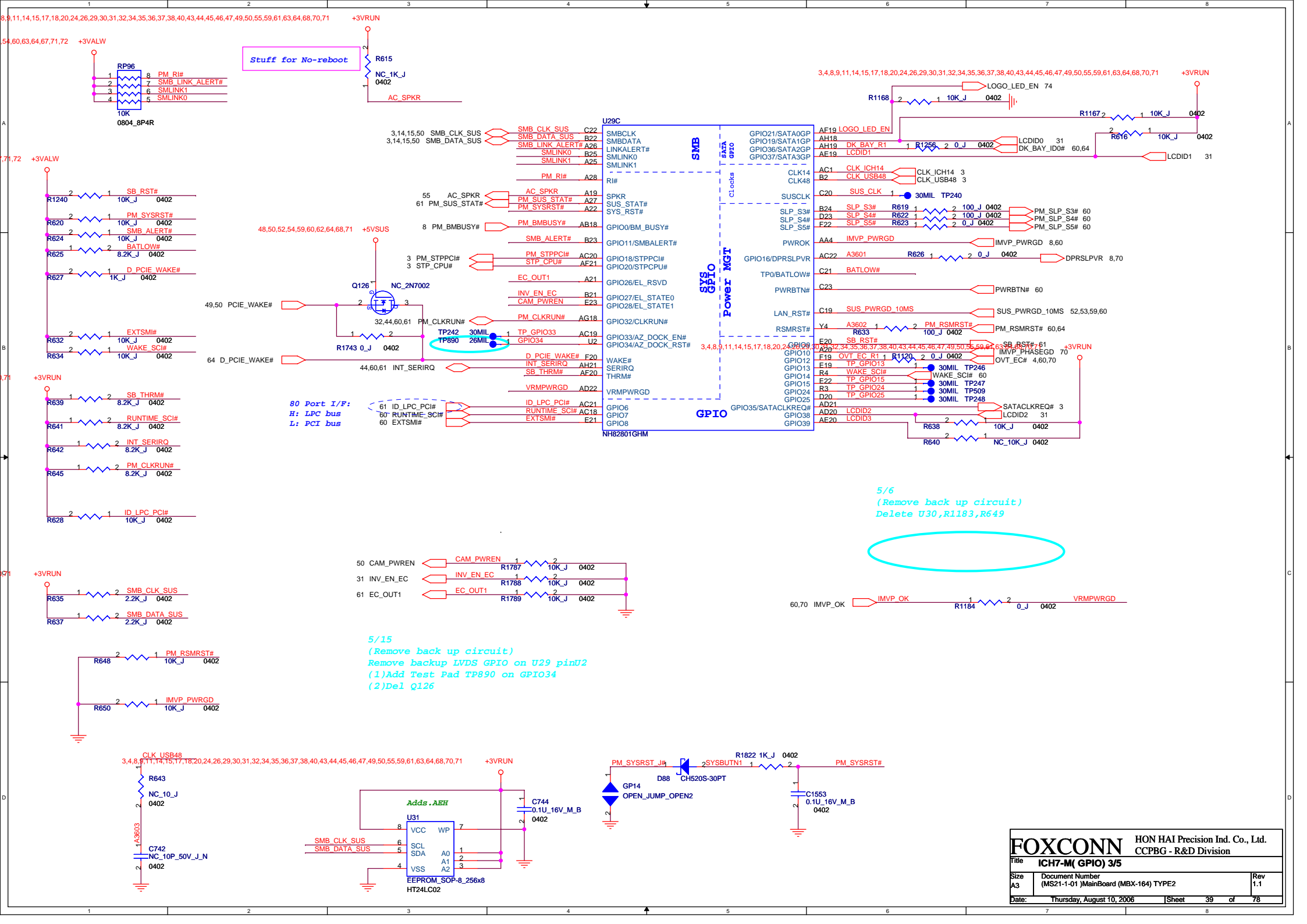
Place within 500 mils of ICH and don't routing next to high speed signals

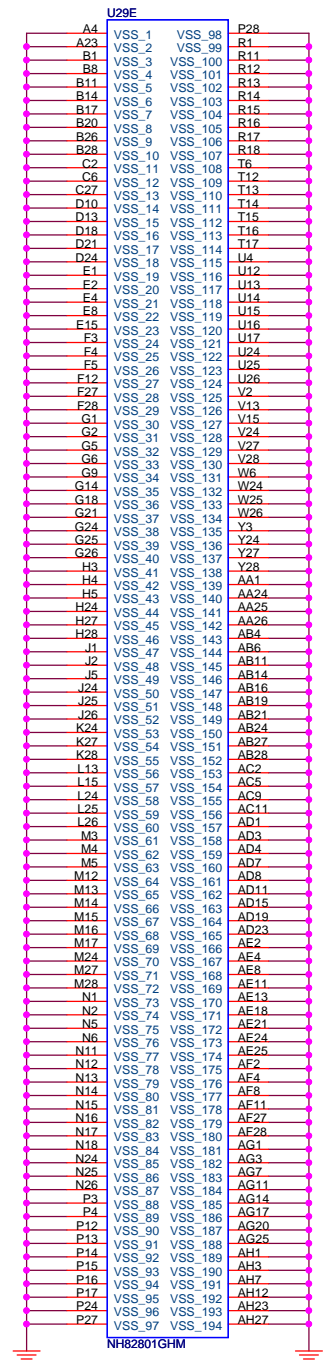


FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **ICH7-M(PC/DMI/USB/PCIE) 1/5**

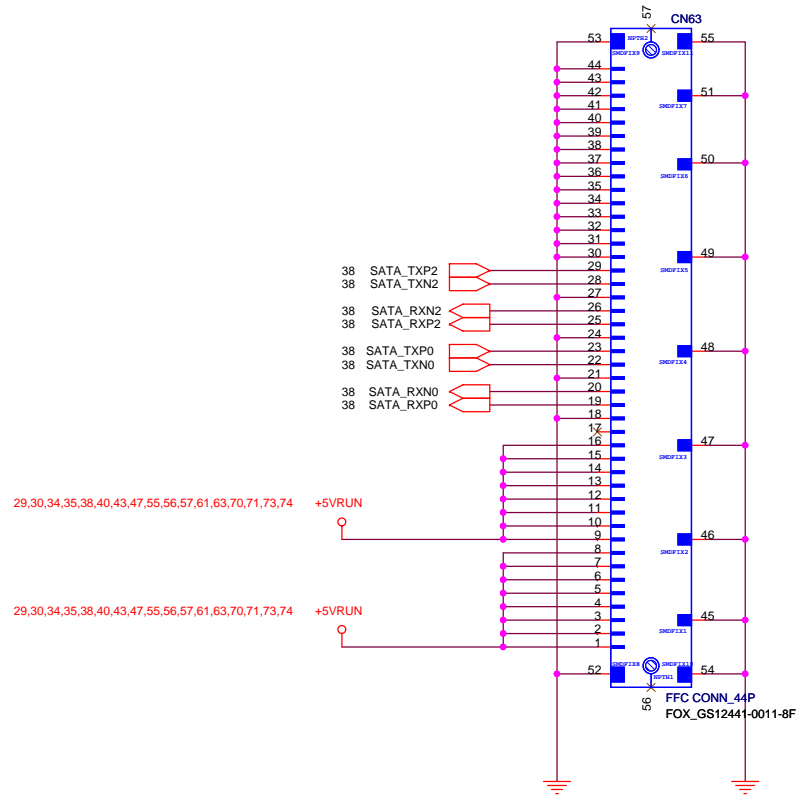
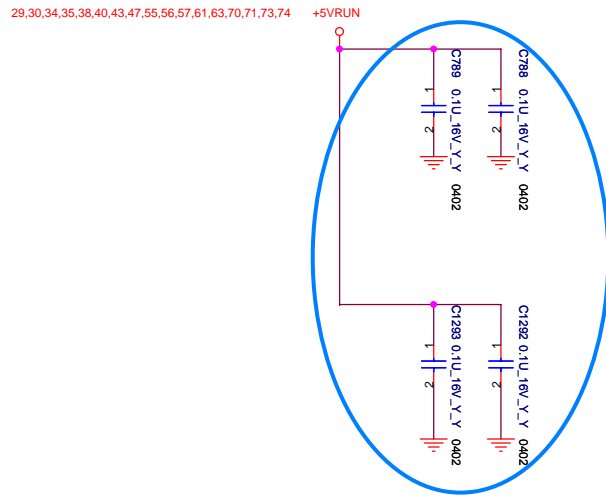
Size A3	Document Number (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 37	of 78





FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title ICH7-M(GND) 5/5			
Size	Document Number	Rev	
A3	(MS21-1-01)MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	41 of 78

5/6
 For power droup cause 0.16V voltage loss Issue
 (1)F7,F8,F19,F20 no stuff
 (2)Co-layout normal open gap GP17-GP18 with fuse
 5/27 Delete SATA HDD Fuse backup circuit
 (1)Remove F7,F8,F19,F20 Pad
 (2)Remove GP17-GP18 open gap



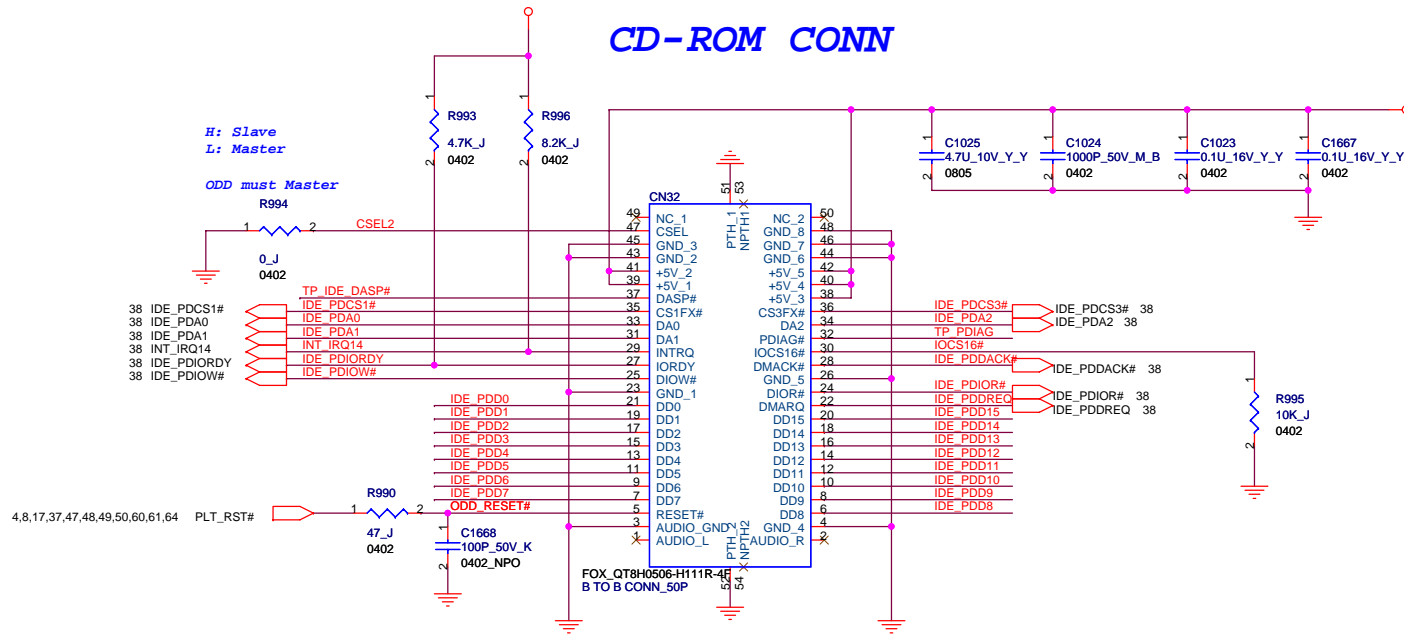
3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,44,45,46,47,49,50,55,59,61,63,64,68,70,71

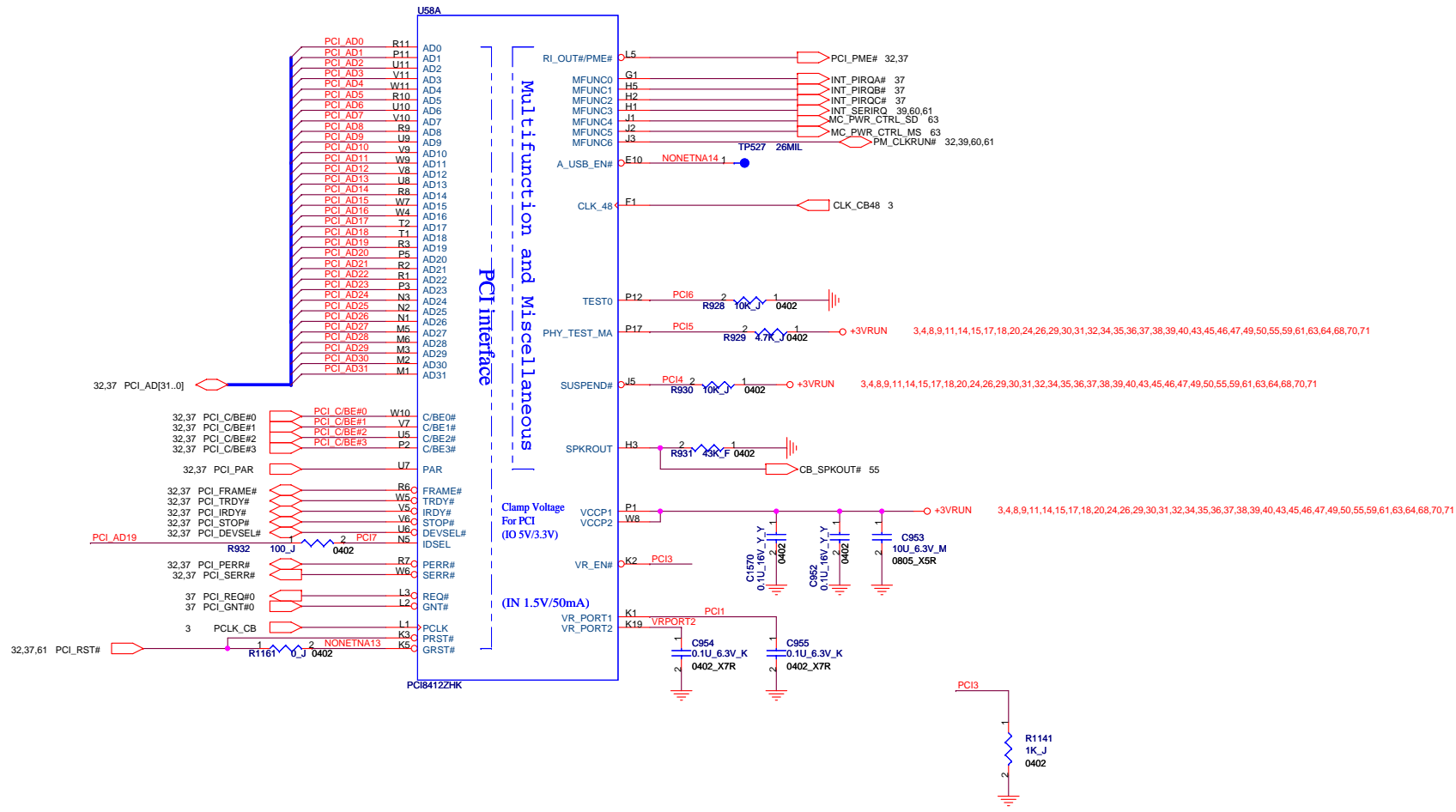
38 IDE_PDD[0..15] IDE_PDD[0..15]

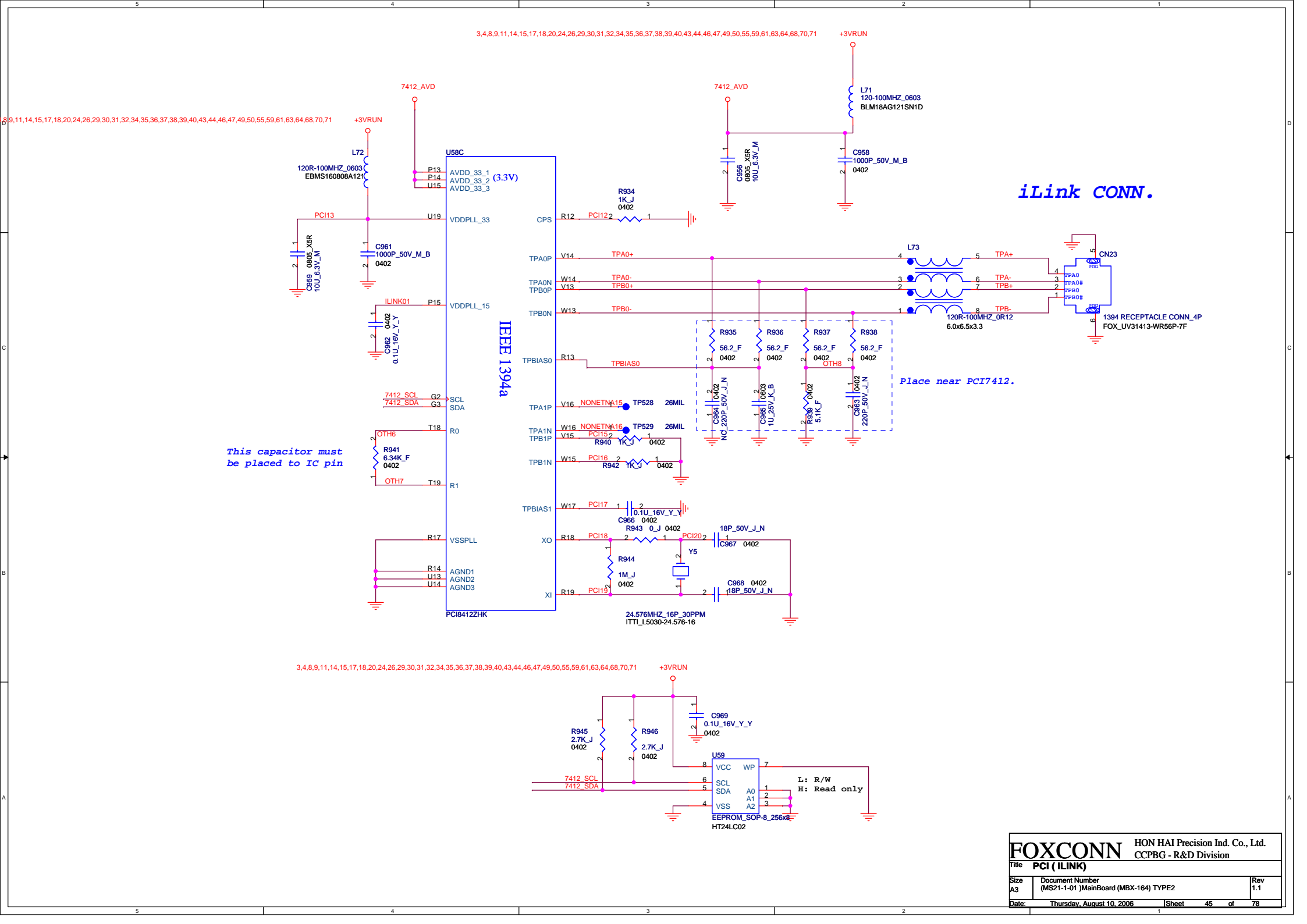
+3VRUN

CD-ROM CONN

+5VRUN 29,30,34,35,38,40,42,47,55,56,57,61,63,70,71,73,74







3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,46,47,49,50,55,59,61,63,64,68,70,71

8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,46,47,49,50,55,59,61,63,64,68,70,71

+3VRUN

+3VRUN

iLink CONN.

IBE81394a

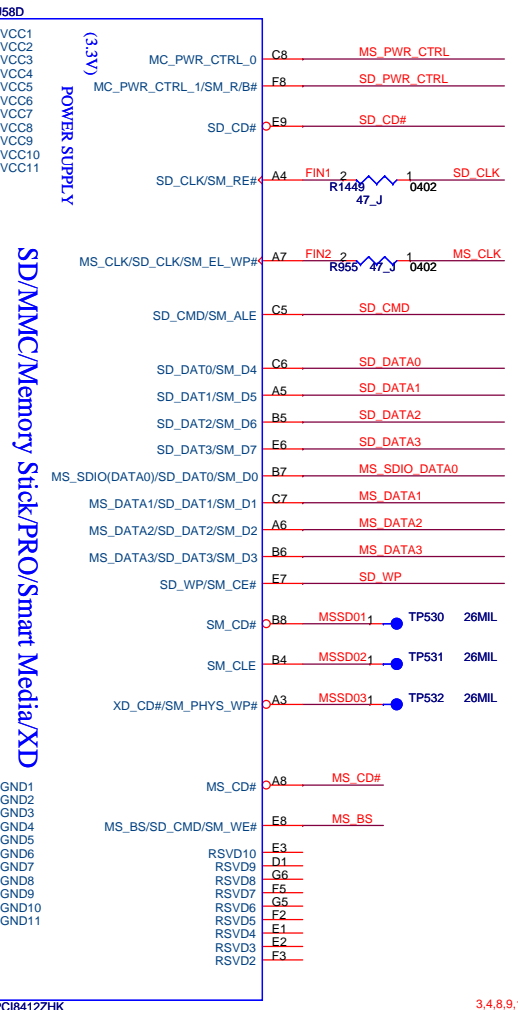
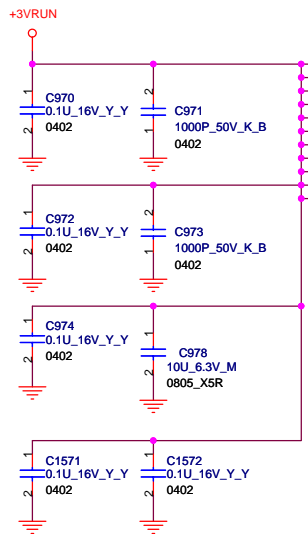
Place near PCI7412.

This capacitor must be placed to IC pin

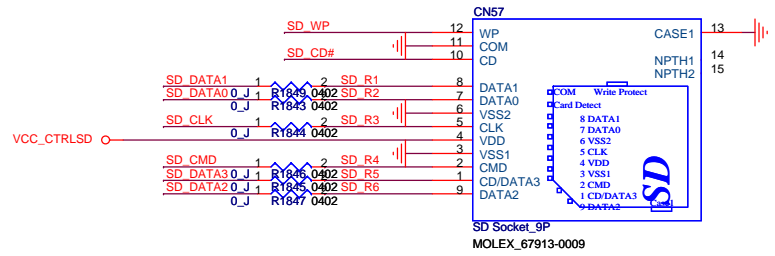
3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,46,47,49,50,55,59,61,63,64,68,70,71

+3VRUN

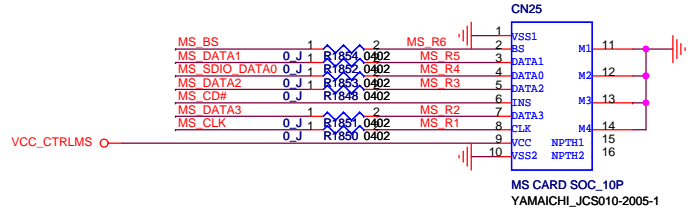
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title PCI (iLINK)			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 45	of 78	



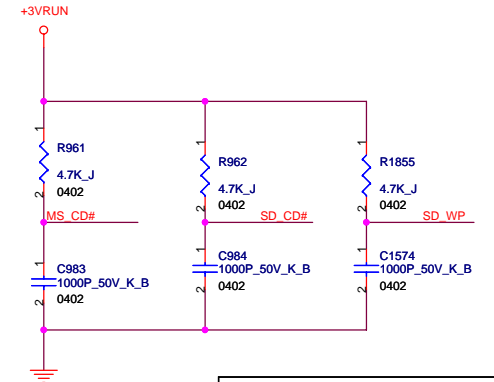
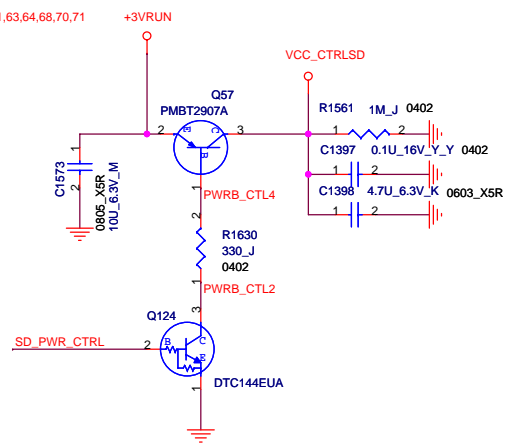
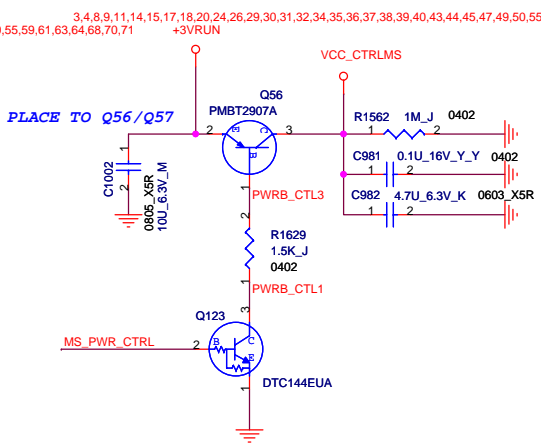
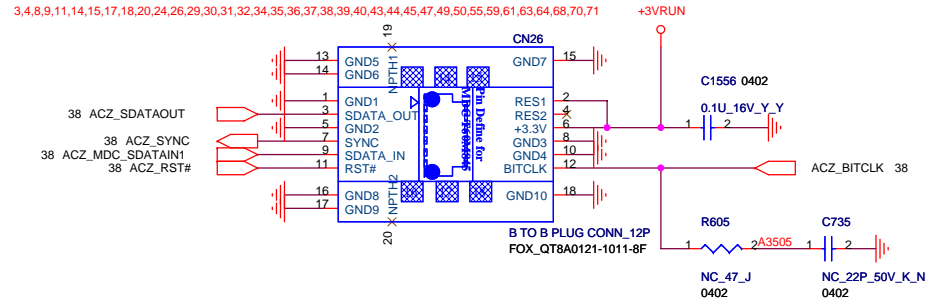
SD CONN.

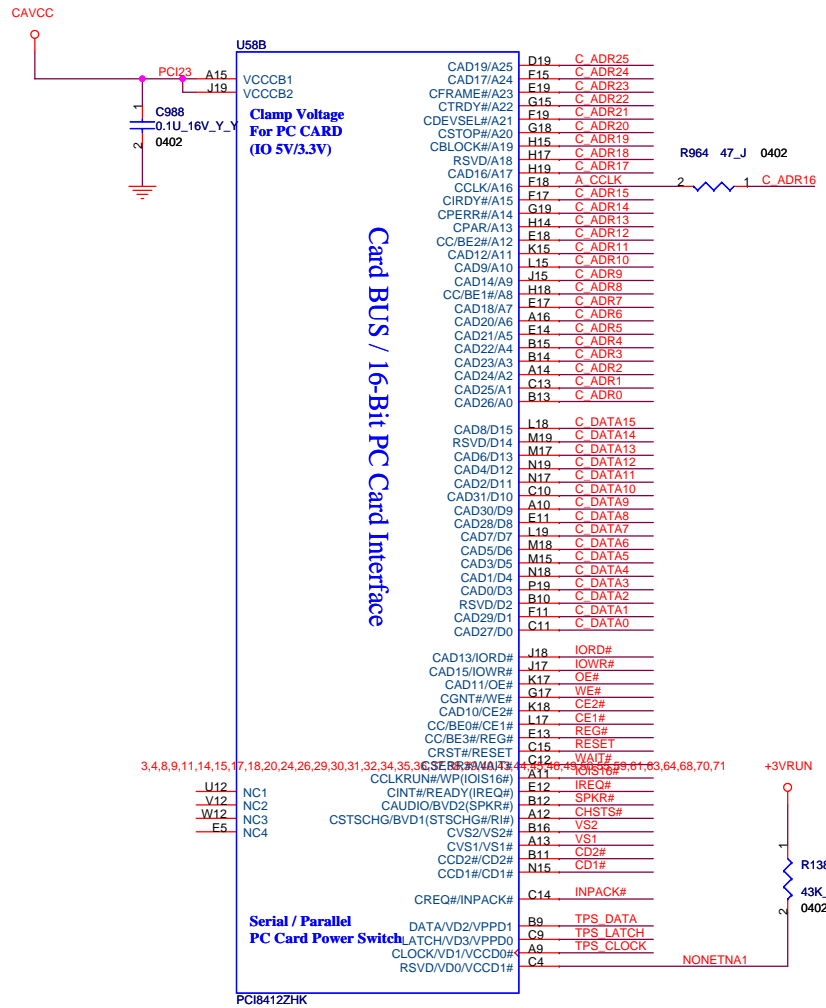


MS STD/DUO CONN.

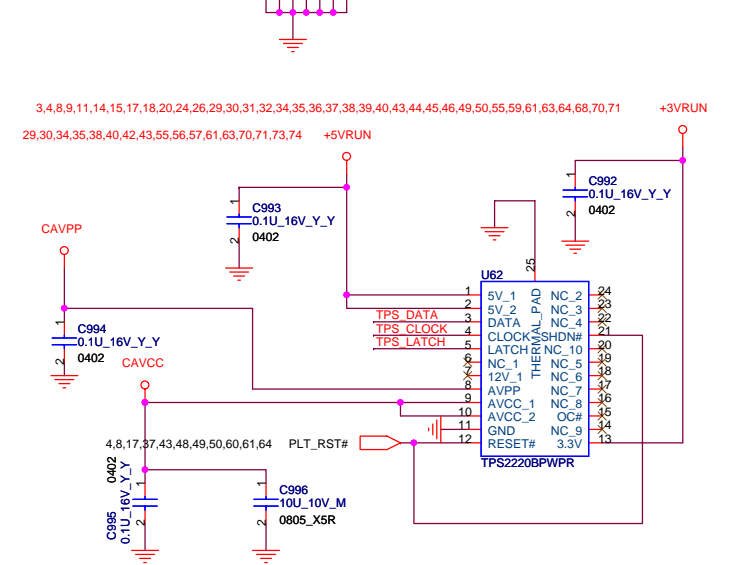
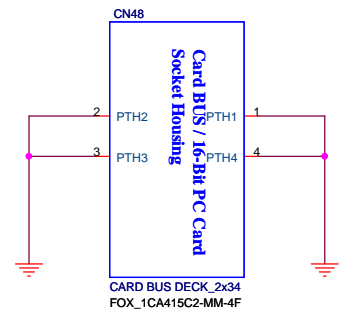
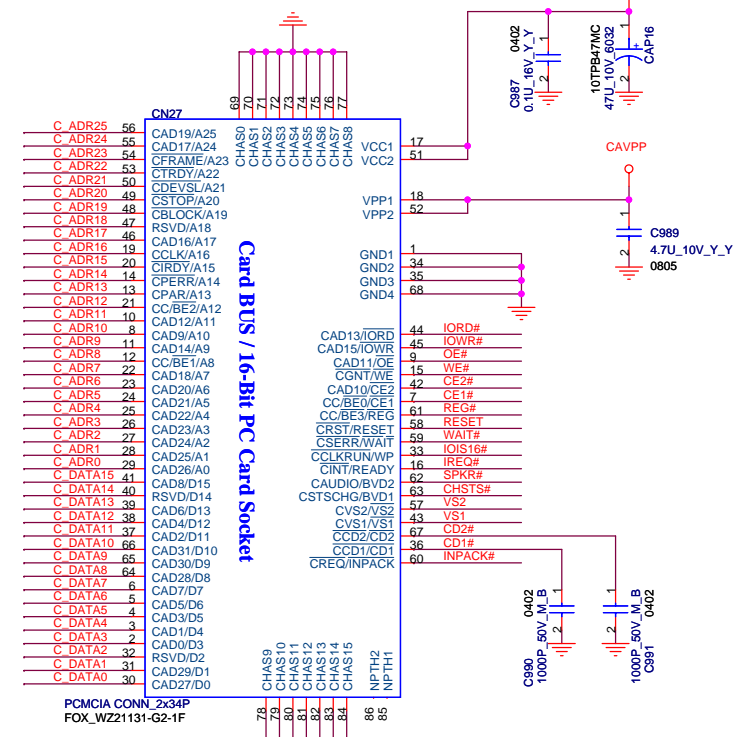


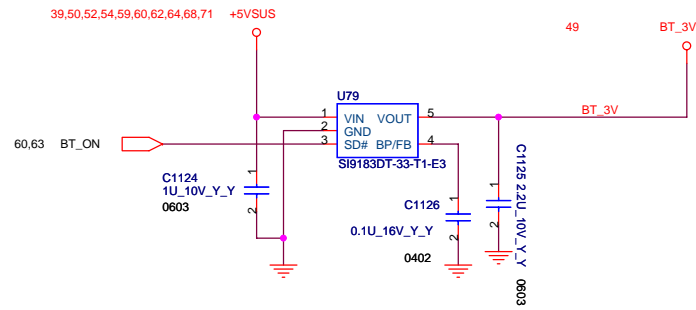
MDC CONN.



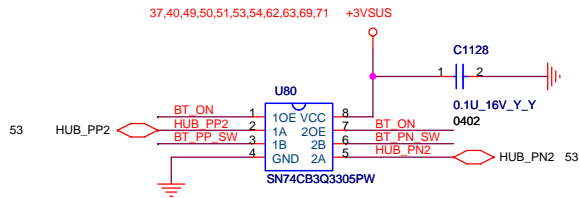
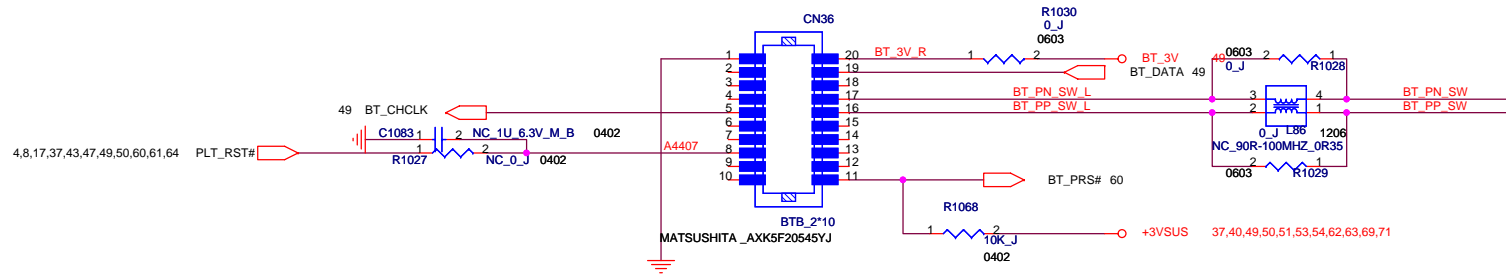


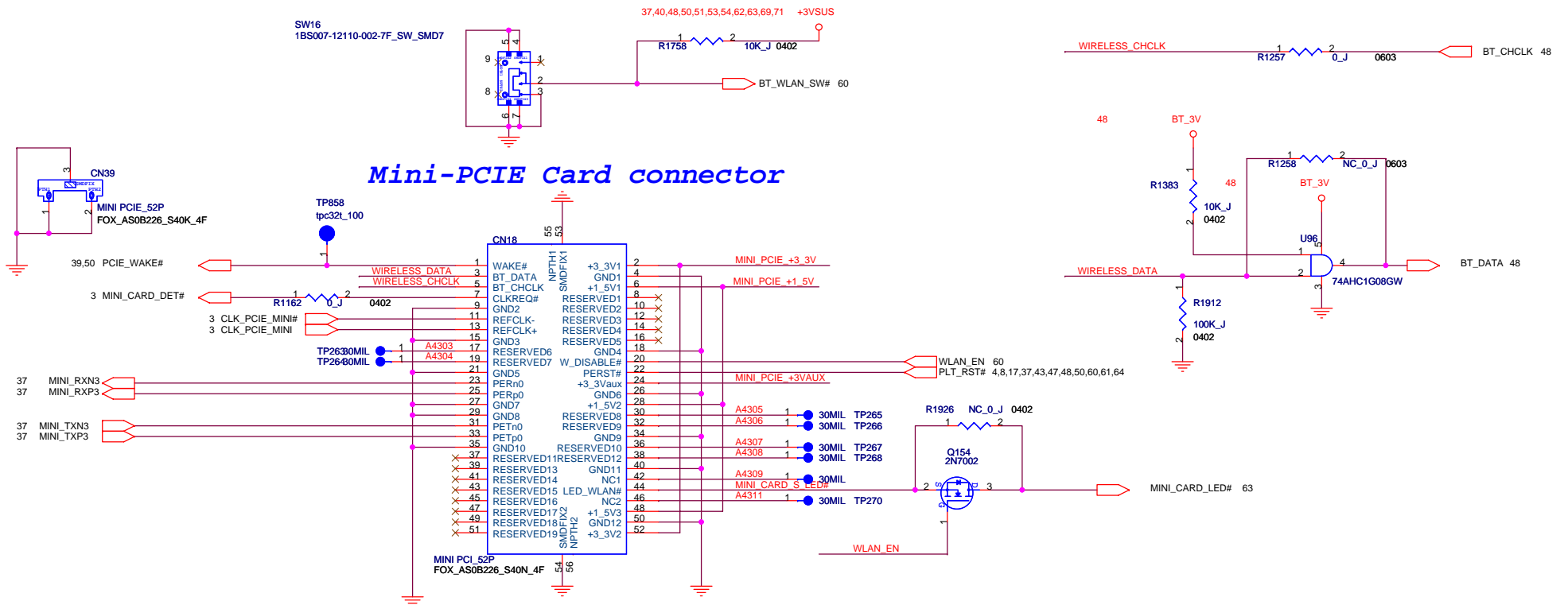
PCMCIA CONN.



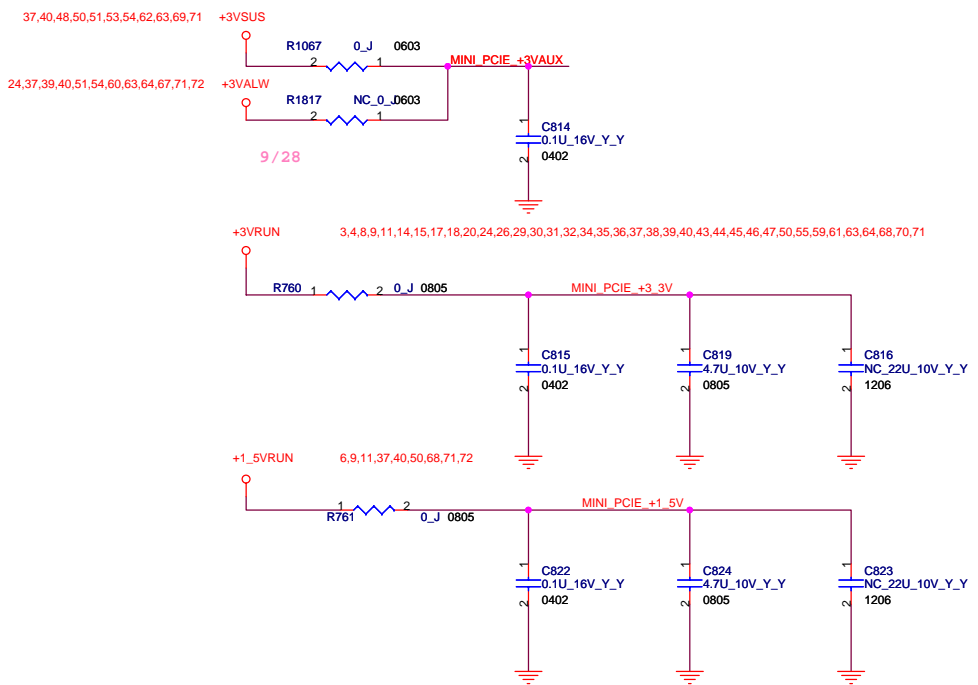


Bluetooth connector





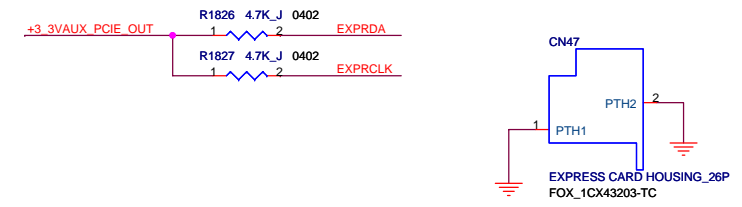
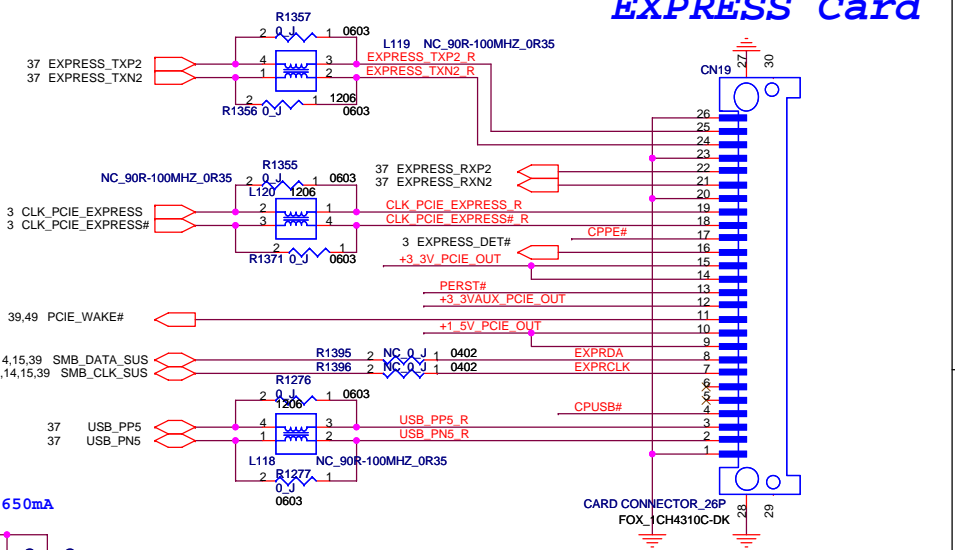
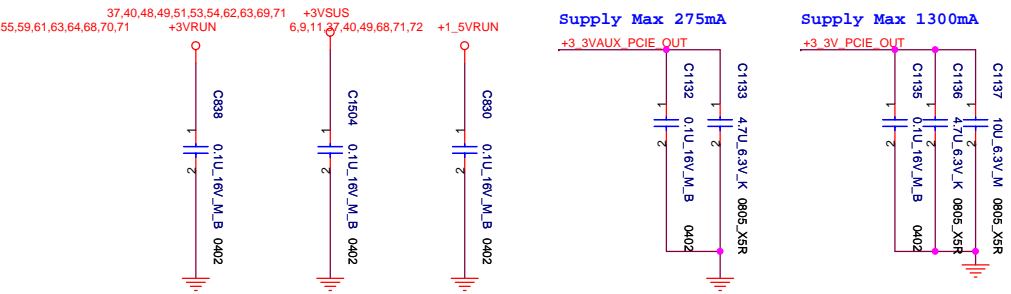
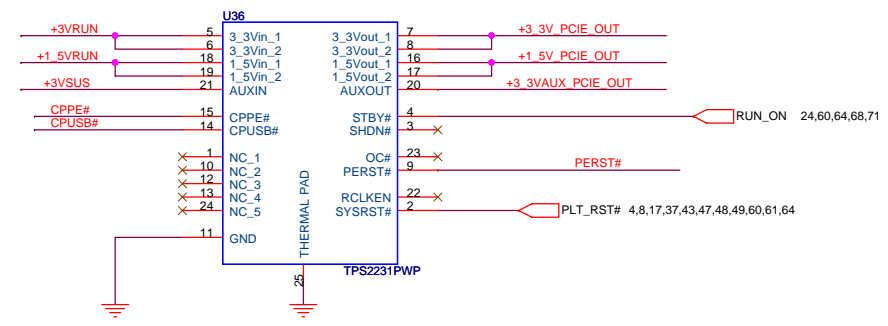
Mini-PCIE Card connector



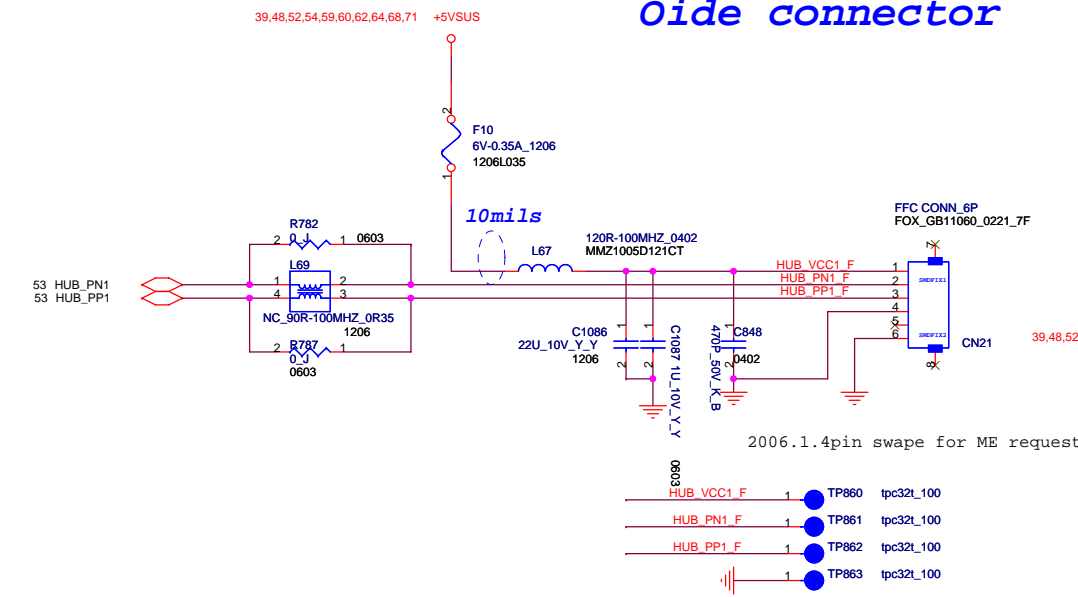
FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title Mini-PCIE Card	
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2
Date: Thursday, August 10, 2006	Rev 1.1
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EXPRESS Card

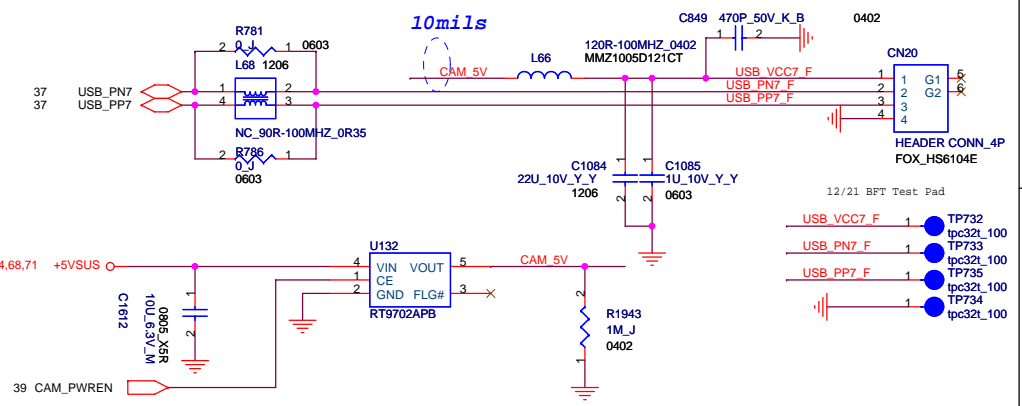
VOLTAGE INPUTS ⁽¹⁾					LOGIC INPUTS					VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT					
Off	x	x	x	x	x	Off	Off	Off				OFF	
On	x	x	0	x	x	GND	GND	GND				Shutdown	
On	x	x	1	x	1	GND	GND	GND				No Card	
On	On	On	1	0	0	On	Off	Off				Standby	
On	On	On	1	1	0	On	On	On				Card Inserted	



Oide connector



CAMERA connector

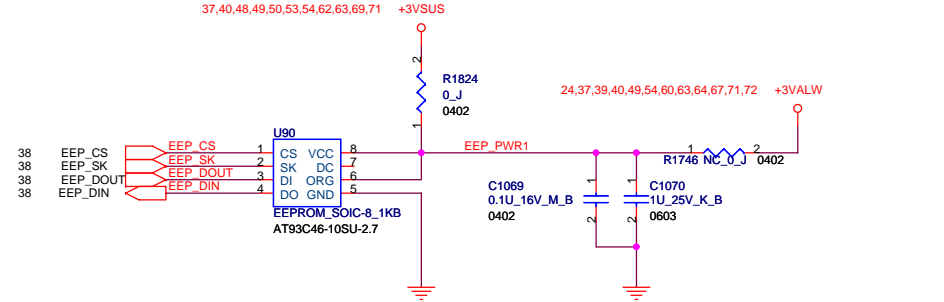
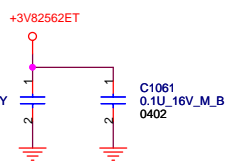
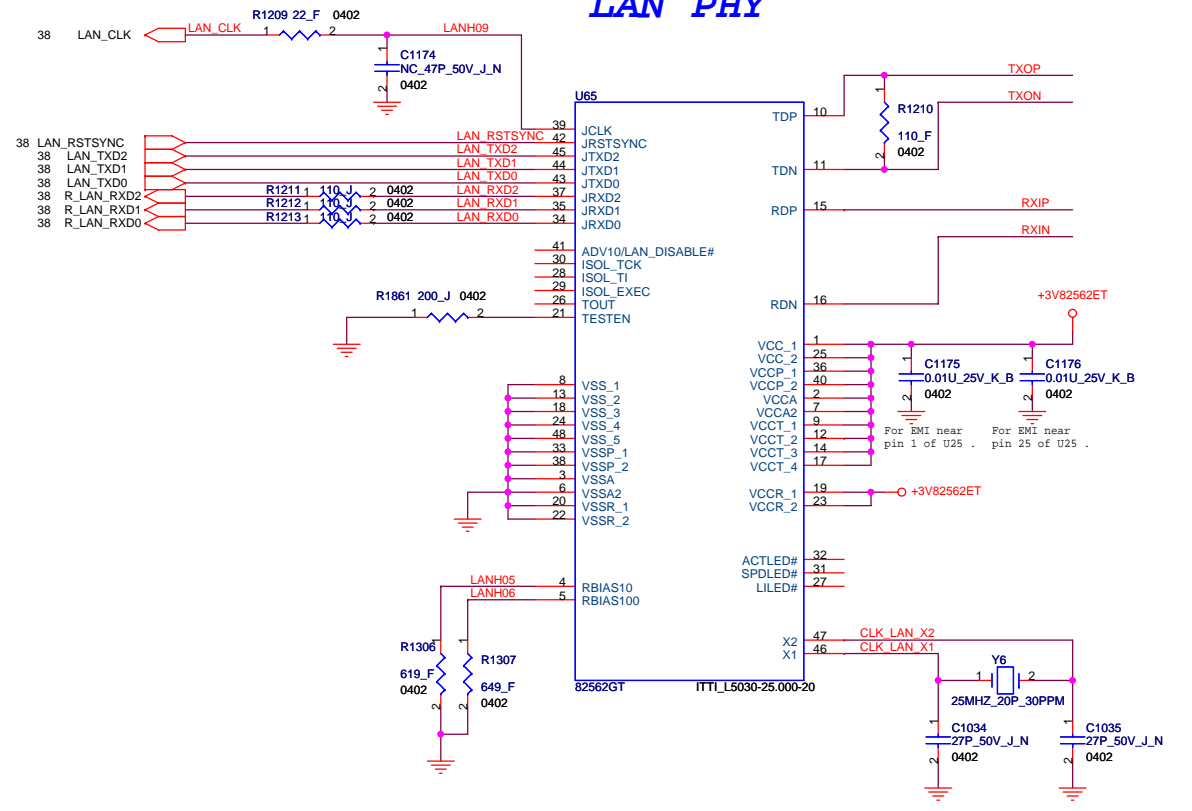
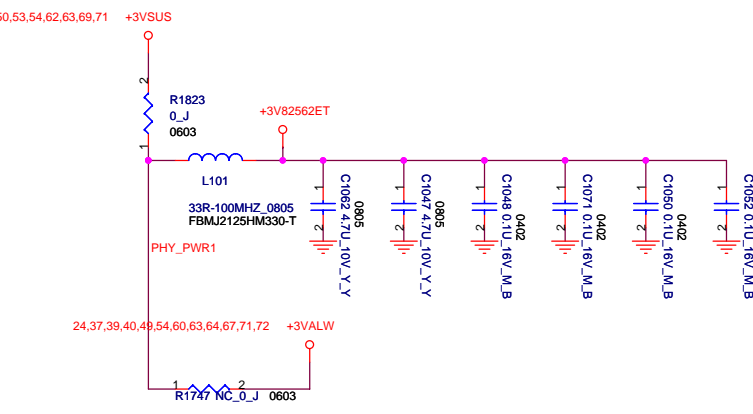
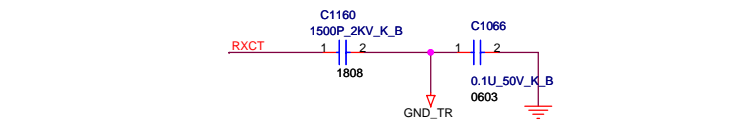
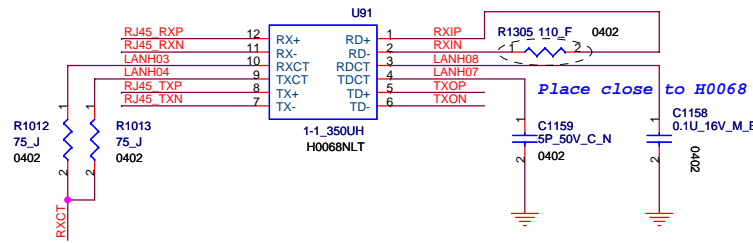
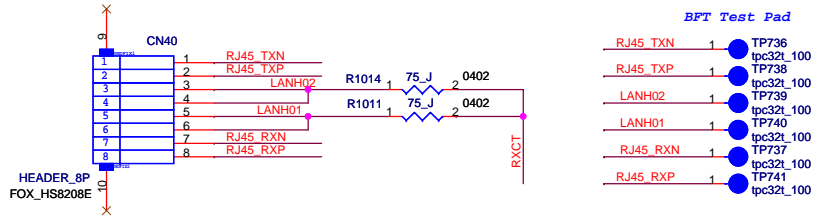


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **EXPRESS/CAM/OIDE**

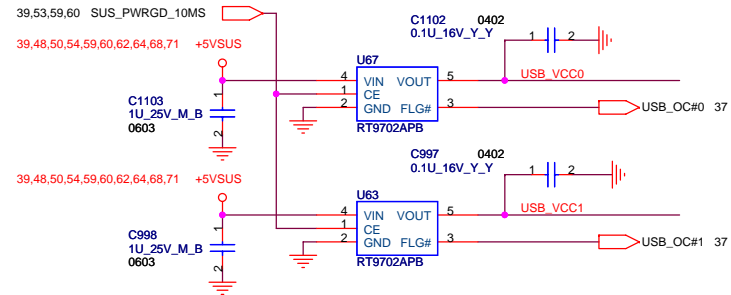
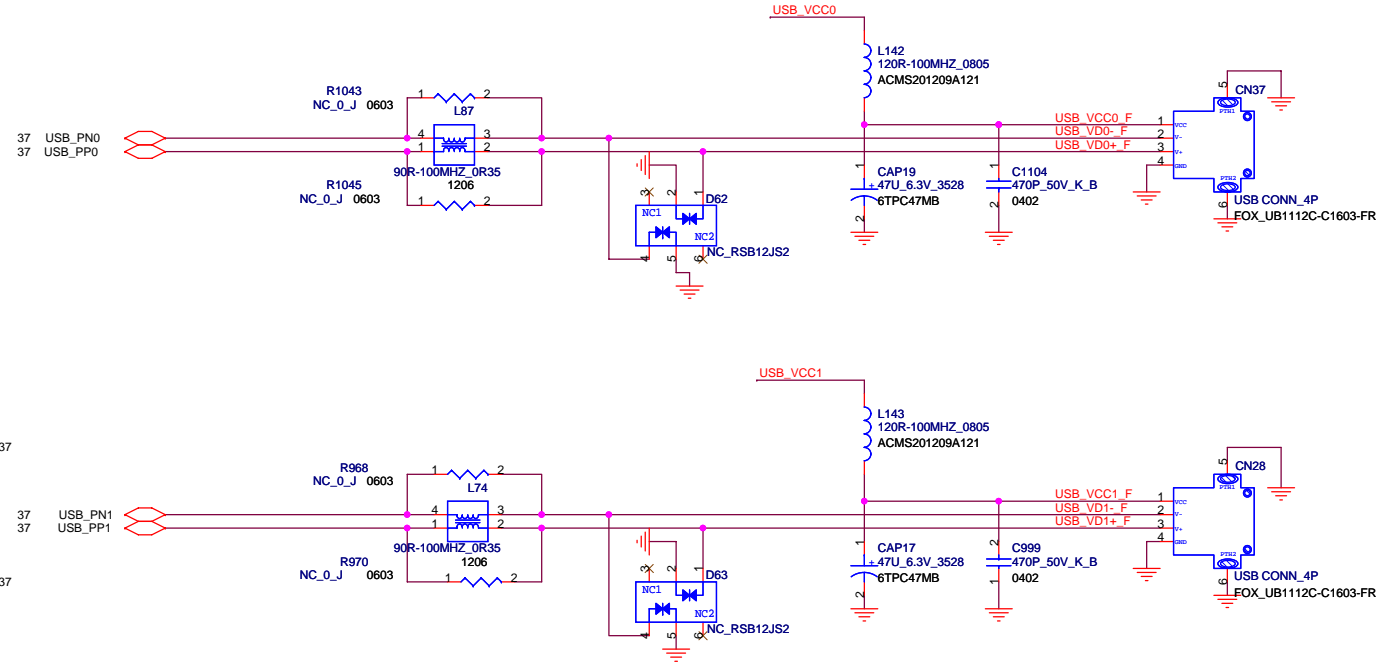
Size: A3	Document Number: (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev: 1.1
Date: Thursday, August 10, 2006	Sheet: 50	of: 78

LAN connector



Default for S3 waking up event ,
backup for S4 waking up event

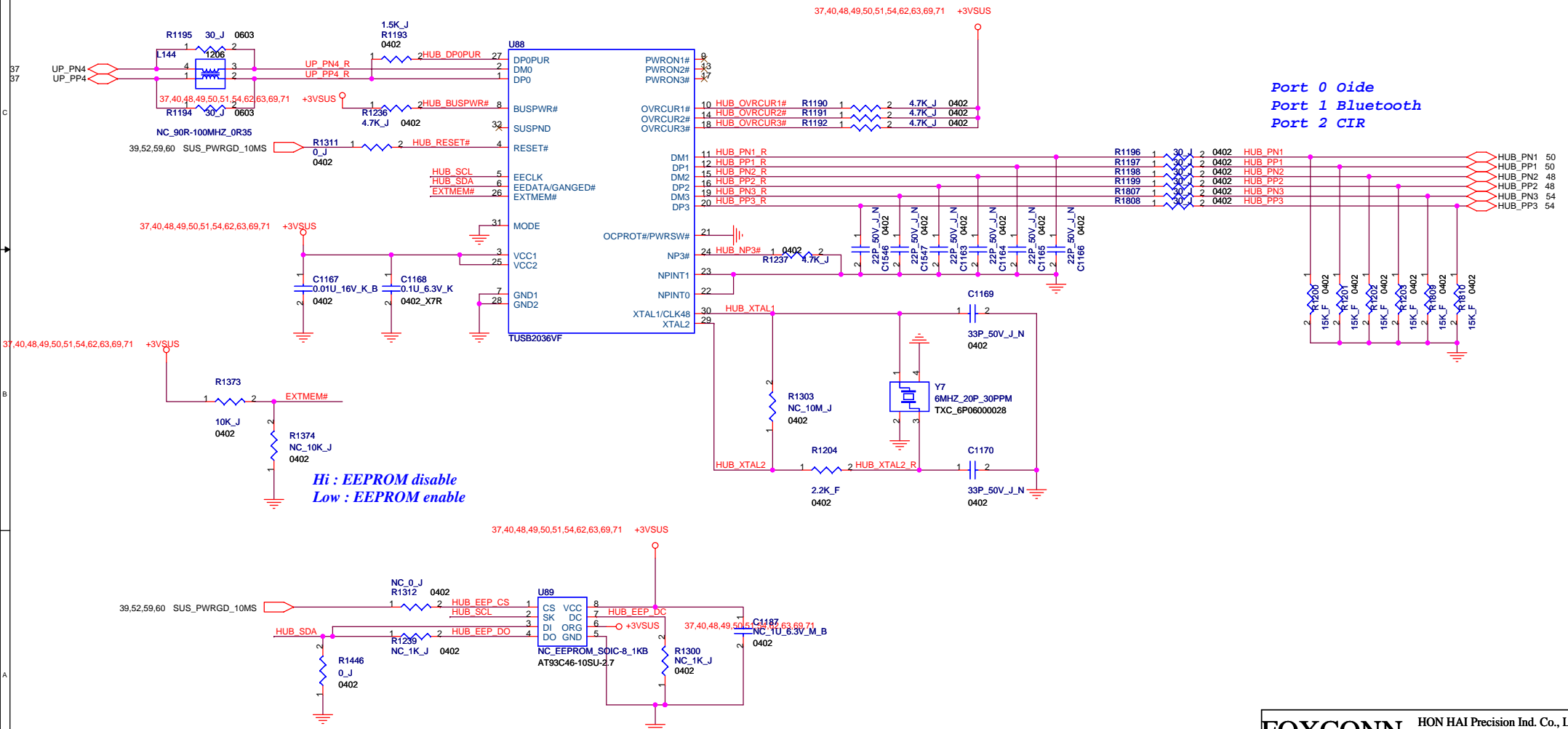
USB connector #2



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title USB2.0/DOCKING CONN.		
Size A3	Document Number (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 52	of 78

Application design in datasheet 27 ohm;
but 30ohm is also in range of USB Spec.

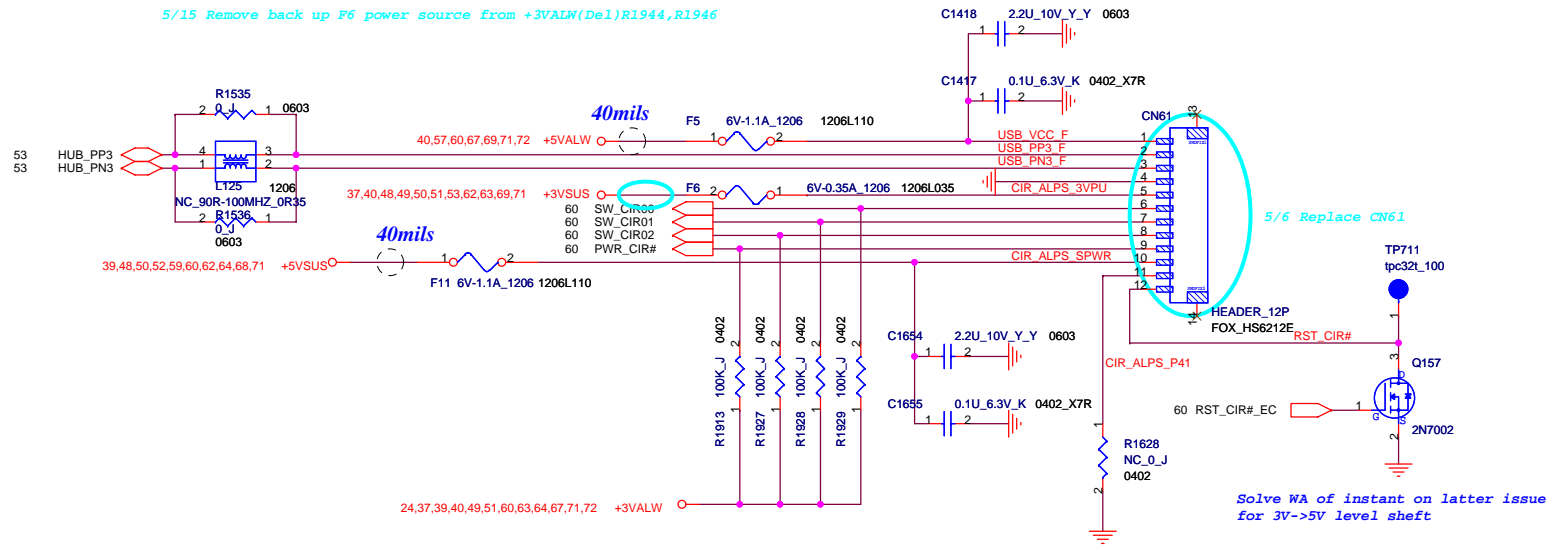
USB 1.1 HUB



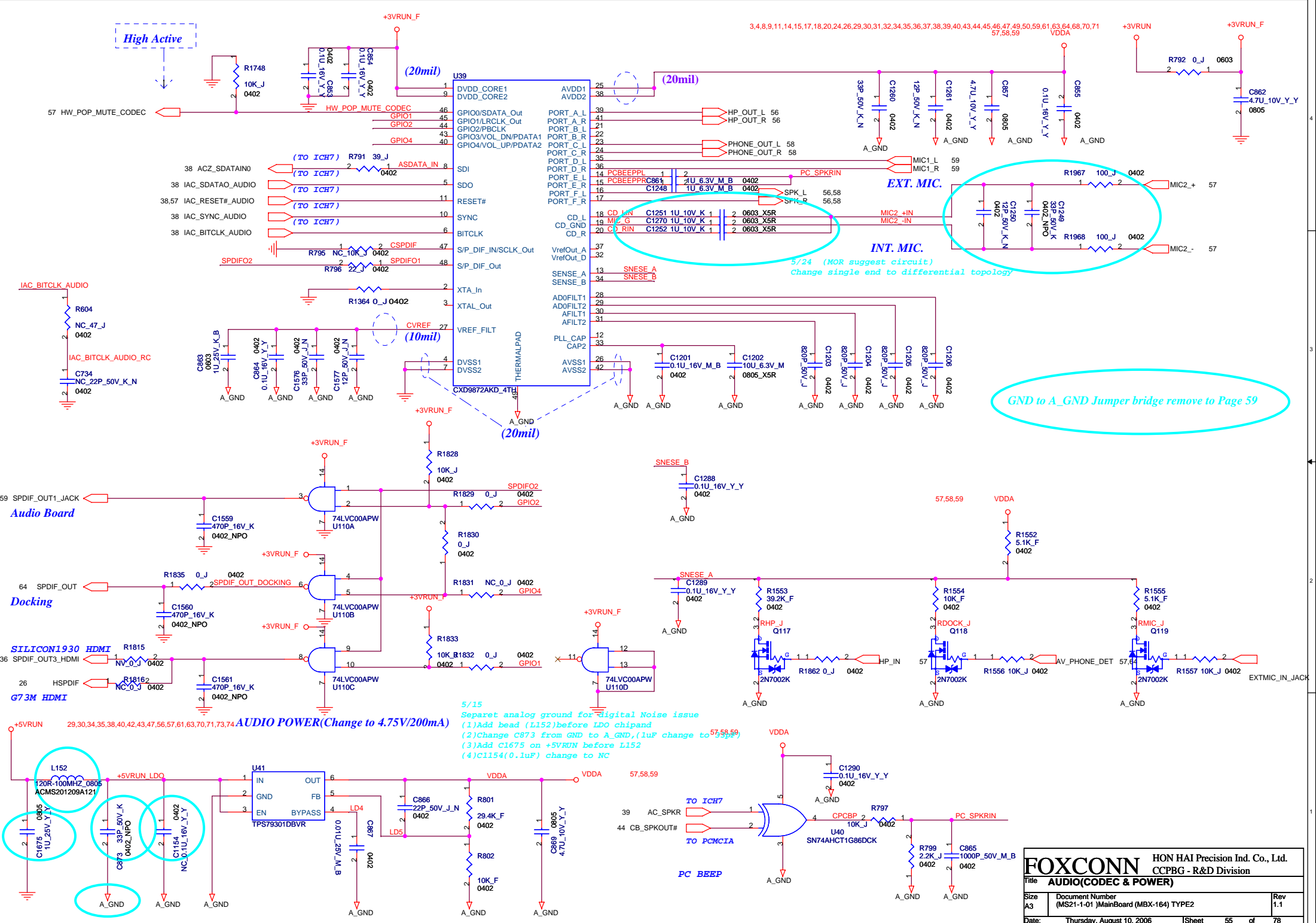
Port 0 Oide
Port 1 Bluetooth
Port 2 CIR

Hi : EEPROM disable
Low : EEPROM enable

IR Receiver connector



USB_VCC_F	1	TP847
USB_PP3_F	1	tpc32t_100
USB_PP3_F	1	TP848
USB_PP3_F	1	tpc32t_100
USB_PN3_F	1	TP849
USB_PN3_F	1	tpc32t_100
USB_PN3_F	1	TP850
USB_PN3_F	1	tpc32t_100
CIR_ALPS_3VPU	1	TP851
CIR_ALPS_3VPU	1	tpc32t_100
SW_CIR00	1	TP852
SW_CIR00	1	tpc32t_100
SW_CIR01	1	TP853
SW_CIR01	1	tpc32t_100
SW_CIR02	1	TP854
SW_CIR02	1	tpc32t_100
PWR_CIR#	1	TP855
PWR_CIR#	1	tpc32t_100
CIR_ALPS_SPWR	1	TP856
CIR_ALPS_SPWR	1	tpc32t_100



High Active

(20mil)

(20mil)

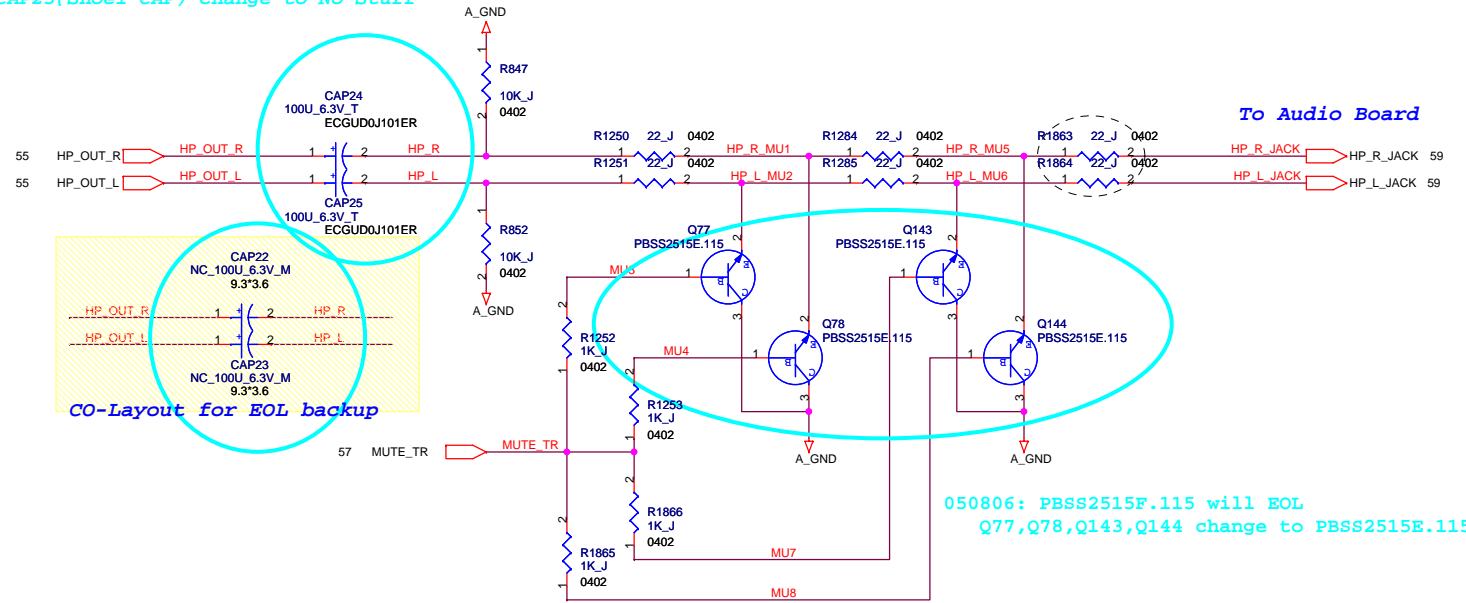
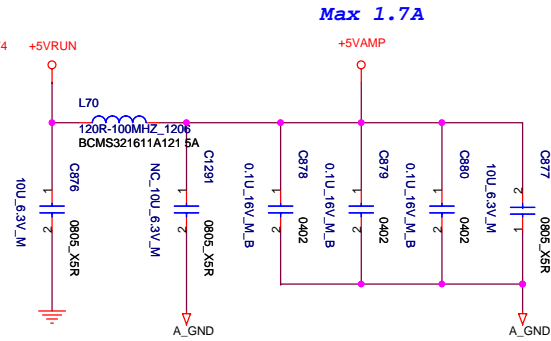
GND to A_GND Jumper bridge remove to Page 59

5/15
 Separate analog ground for digital noise issue
 (1) Add bead (L152) before LDO chip and
 (2) Change C873 from GND to A_GND, (1uF change to 57.58.59)
 (3) Add C1675 on +5VRUN before L152
 (4) C1154 (0.1uF) change to NC

PC BEEP

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size	Document Number	Rev	
A3	(MS21-1-01) MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	55 of 78

050806: Shoei CAP will EOL
 CAP24,CAP25(SP CAP) change to Stuff
 CAP22,CAP23(Shoei CAP) change to No Stuff



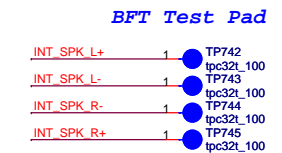
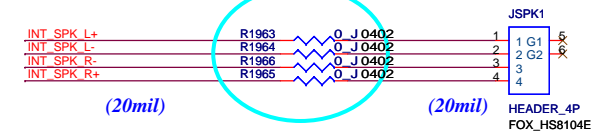
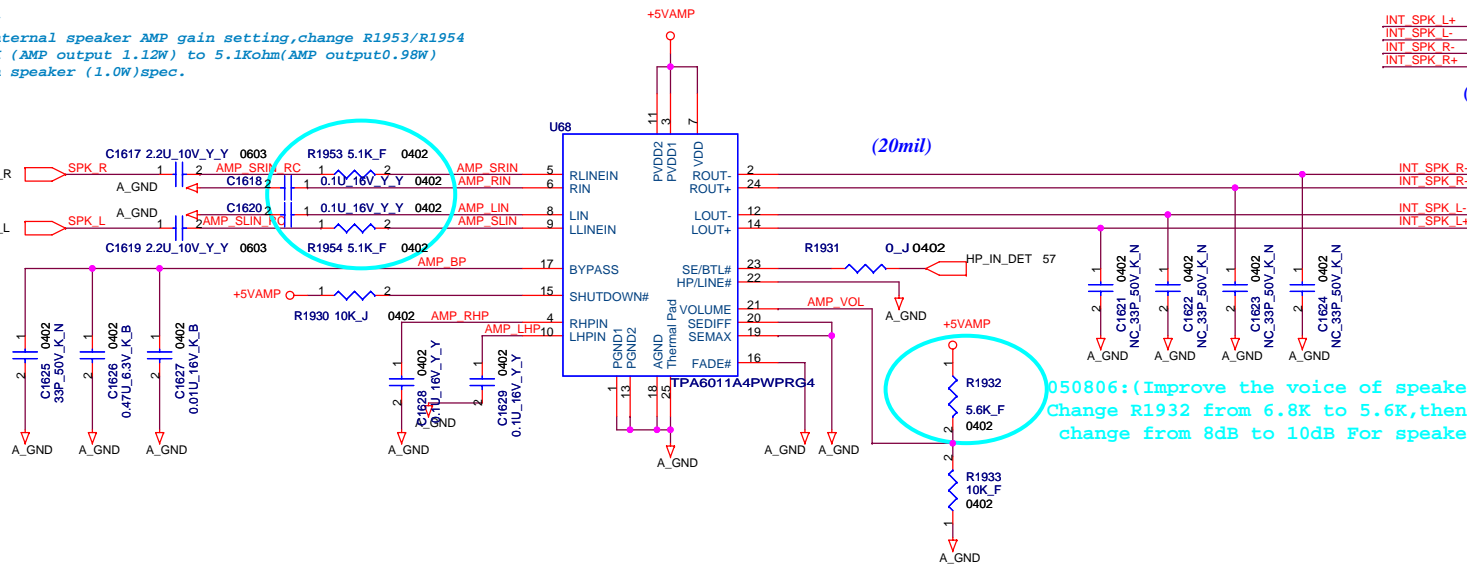
050806: PBSS2515F.115 will EOL
 Q77,Q78,Q143,Q144 change to PBSS2515E.115

INTERNAL SPEAKER

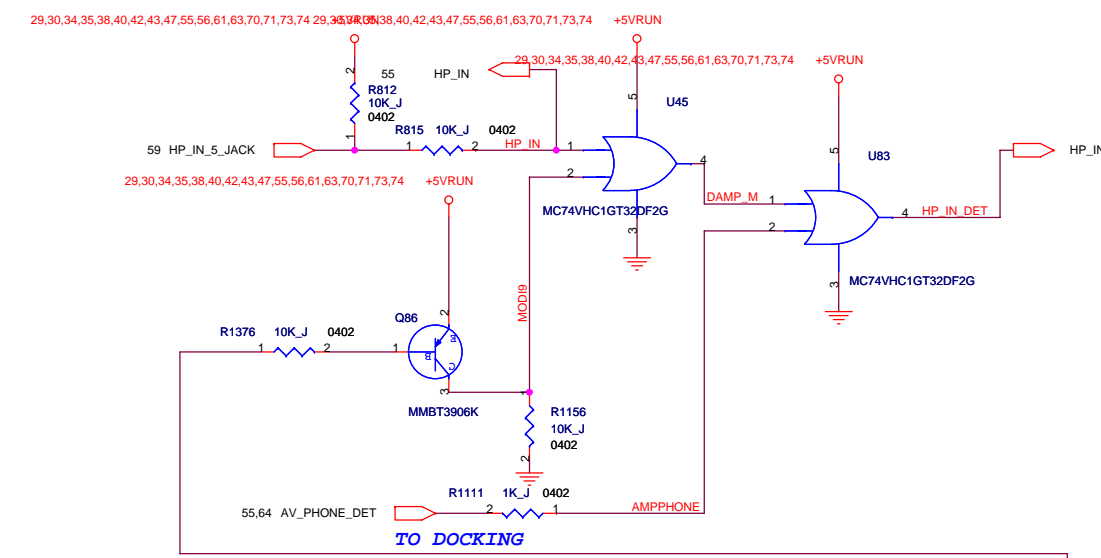
050806:(Improve the voice of speaker up to 0.94W).
 Add damping Resistors R1953 on AMP_SRIN,R1954 on AMP_SLIN
 then speaker amp output won't be distorted.
 For speaker loudness issue.

050806:(Improve the voice of speaker up to 0.94W).
 EMI team confirm whether
 it is ok to use 0ohm resistor replacing bead

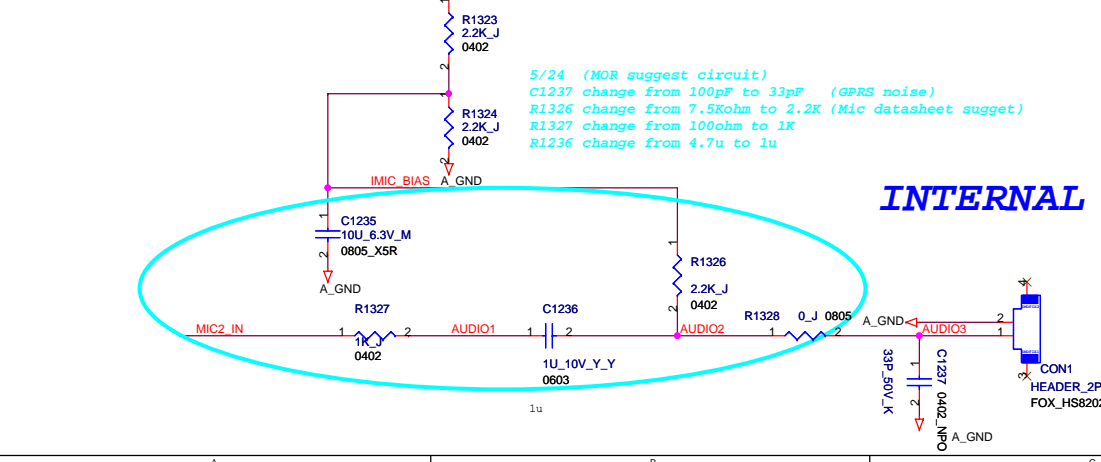
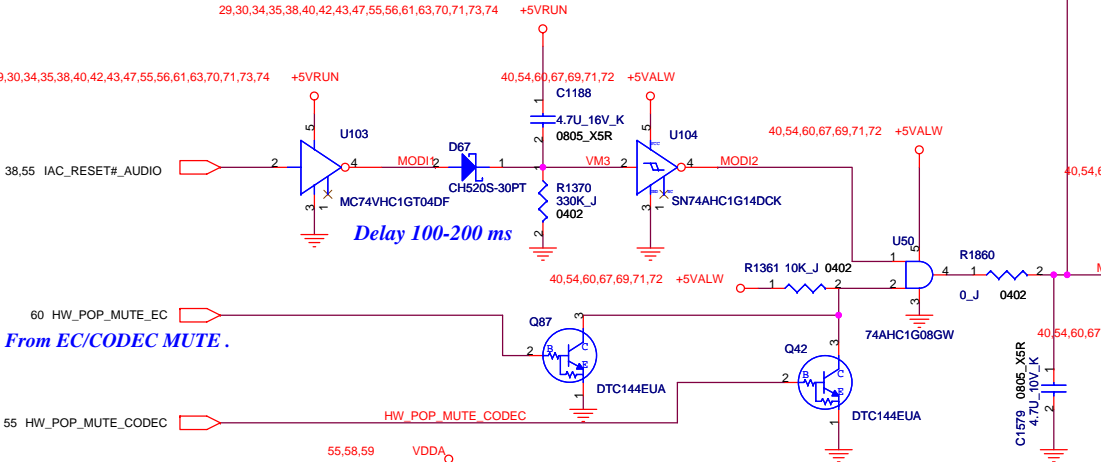
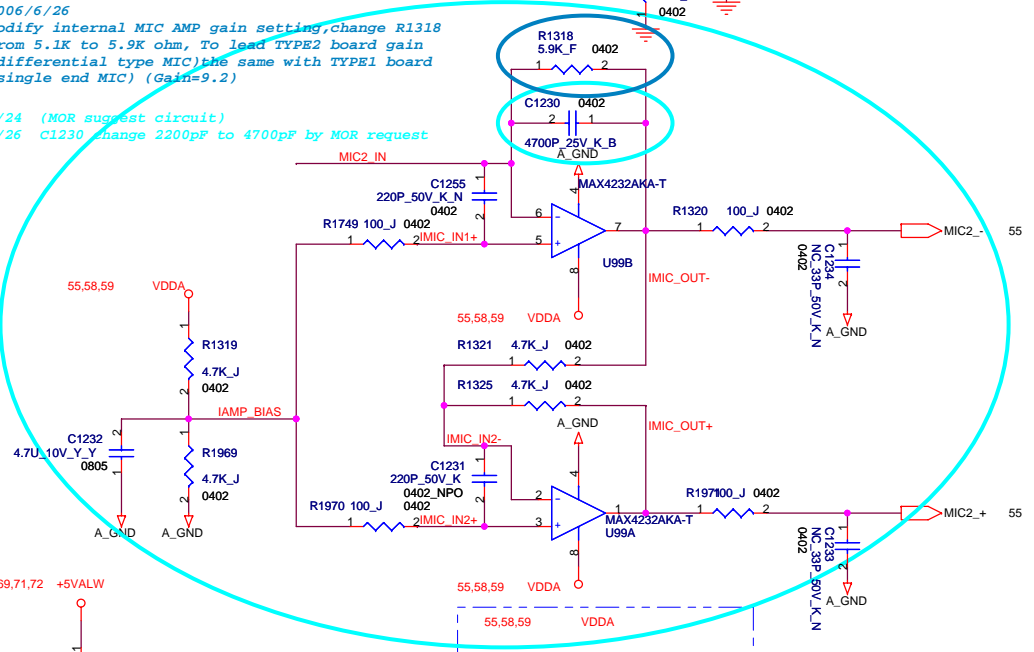
2006/6/26
 Modify internal speaker AMP gain setting,change R1953/R1954
 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W)
 to fit in speaker (1.0W)spec.



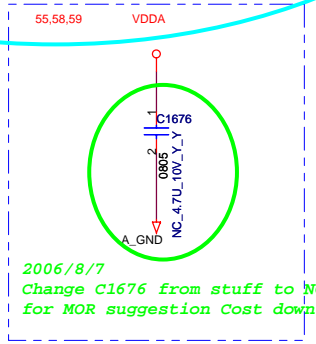
050806:(Improve the voice of speaker up to 0.94W).
 Change R1932 from 6.8K to 5.6K,then amp gain
 change from 8dB to 10dB For speaker loudness issue



2006/6/26
 Modify internal MIC AMP gain setting, change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC) the same with TYPE1 board (single end MIC) (Gain=9.2)
 5/24 (MOR suggest circuit)
 5/26 C1230 change 2200pF to 4700pF by MOR request

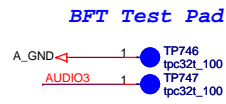


5/24 (MOR suggest circuit)
 C1237 change from 100pF to 33pF (GPRS noise)
 R1326 change from 7.5Kohm to 2.2K (Mic datasheet suggest)
 R1327 change from 100ohm to 1K
 R1236 change from 4.7u to 1u



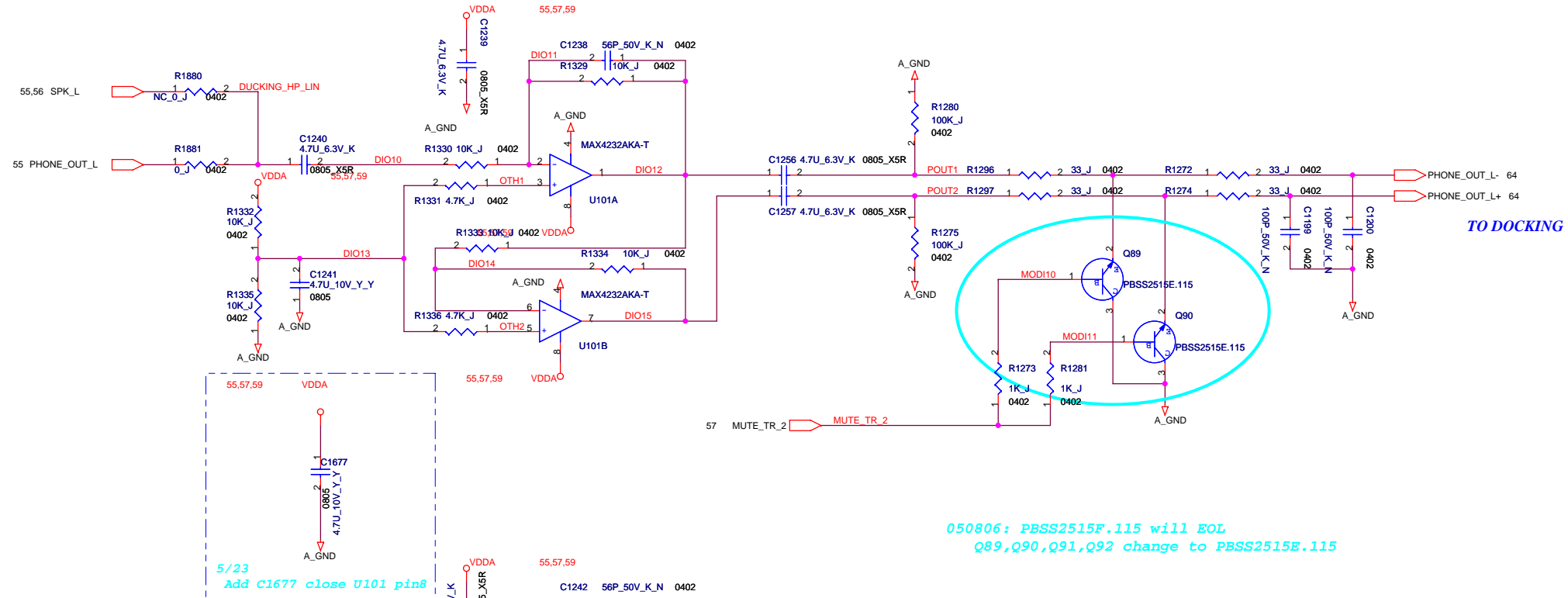
2006/8/7
 Change C1676 from stuff to NC for MOR suggestion Cost down request.

INTERNAL MIC(Non)

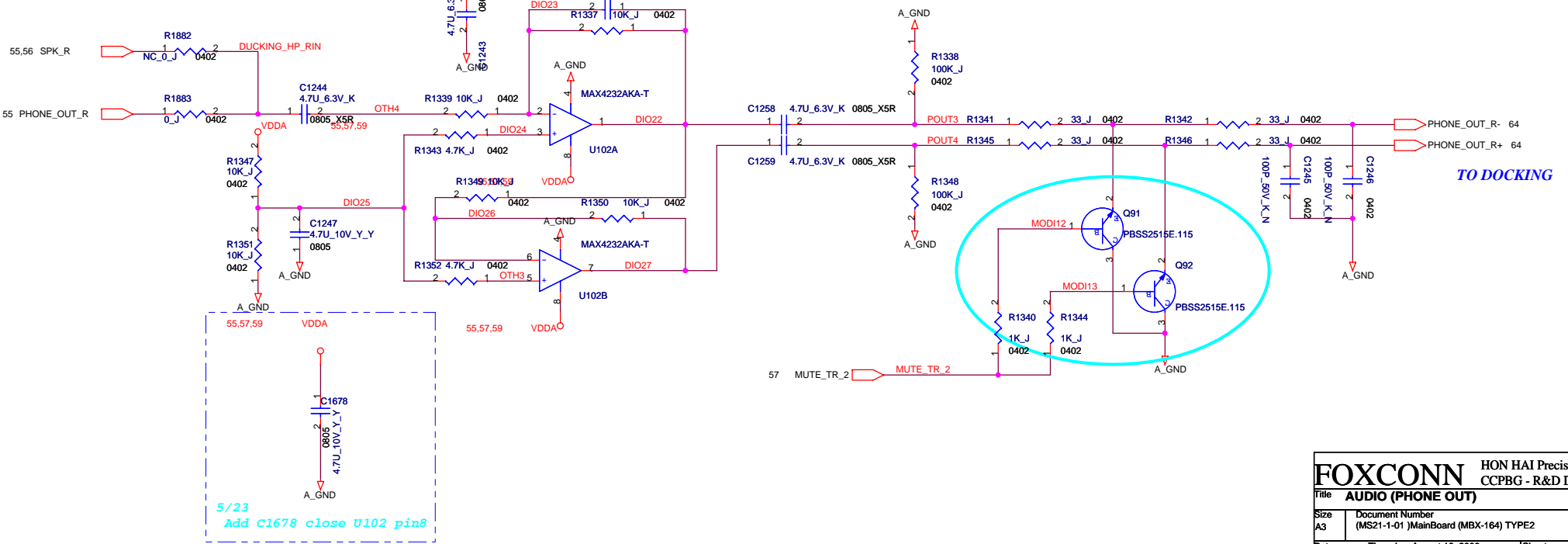


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title AUDIO (MUTE & INTMIC)		
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 57	of 78

PHONE OUT



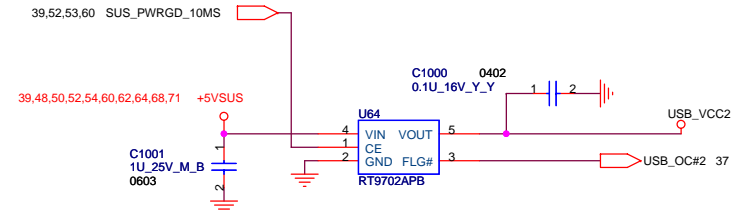
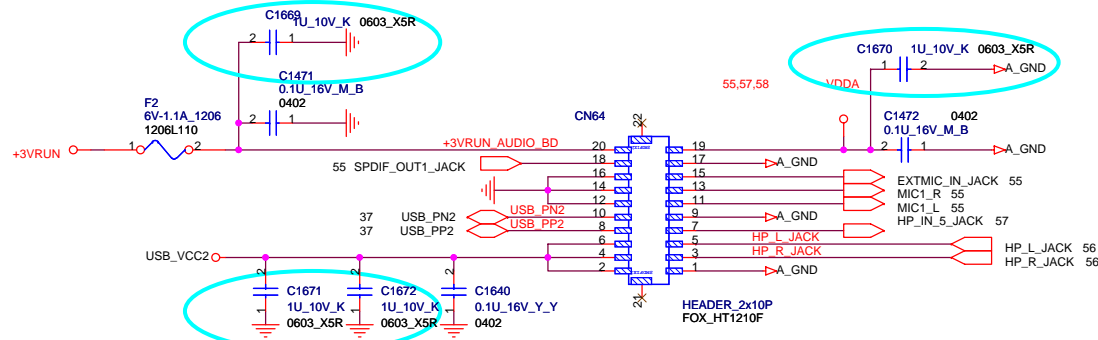
050806: PBSS2515F.115 will EOL
 Q89,Q90,Q91,Q92 change to PBSS2515E.115



Audio Board connector

050806: (To improve SNR issue)

Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2, C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .



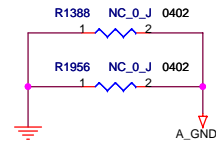
5/6

Separate analog ground for digital Noise issue:

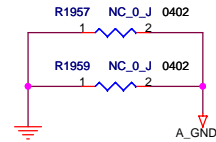
- (1) Remove GP3 (Close Jumper) not bridge between GND and A_GND
- (2) Backup two jumper resistors for bridge between GND and A_GND (C1388, C1966 on Screw hole H3, C1957, C1959 on screw hole H5)
- (3) Isolate screw hole H4, add 100pF capacitors C1673, C1674 for EMI, Zener diode D100 for ESD
- (4) Add jumper resistor for Return patch R1955 close L70 (+5VAMP) & R1958 close U41 (+5VRUN) & R1960 close codec.

Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

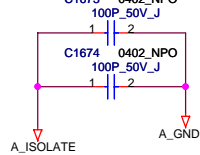


Close screw hole H5

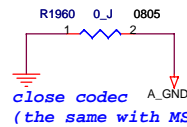
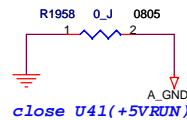


Isolate screw hole H4, and add EMI/ESD solution

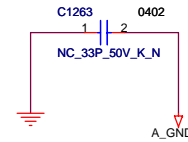
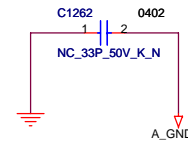
EMI



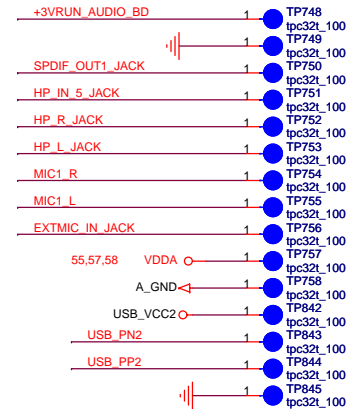
Add jumper resistor for Return patch

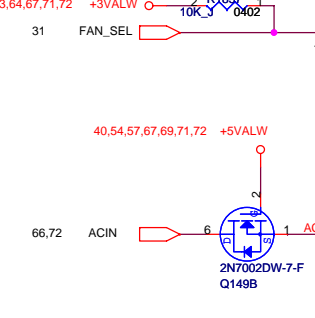
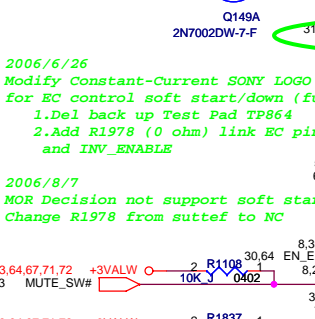
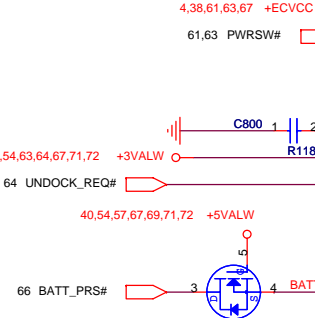
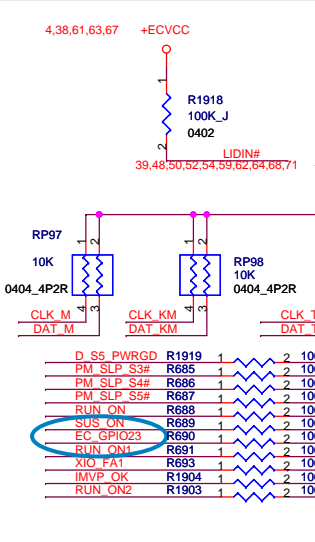
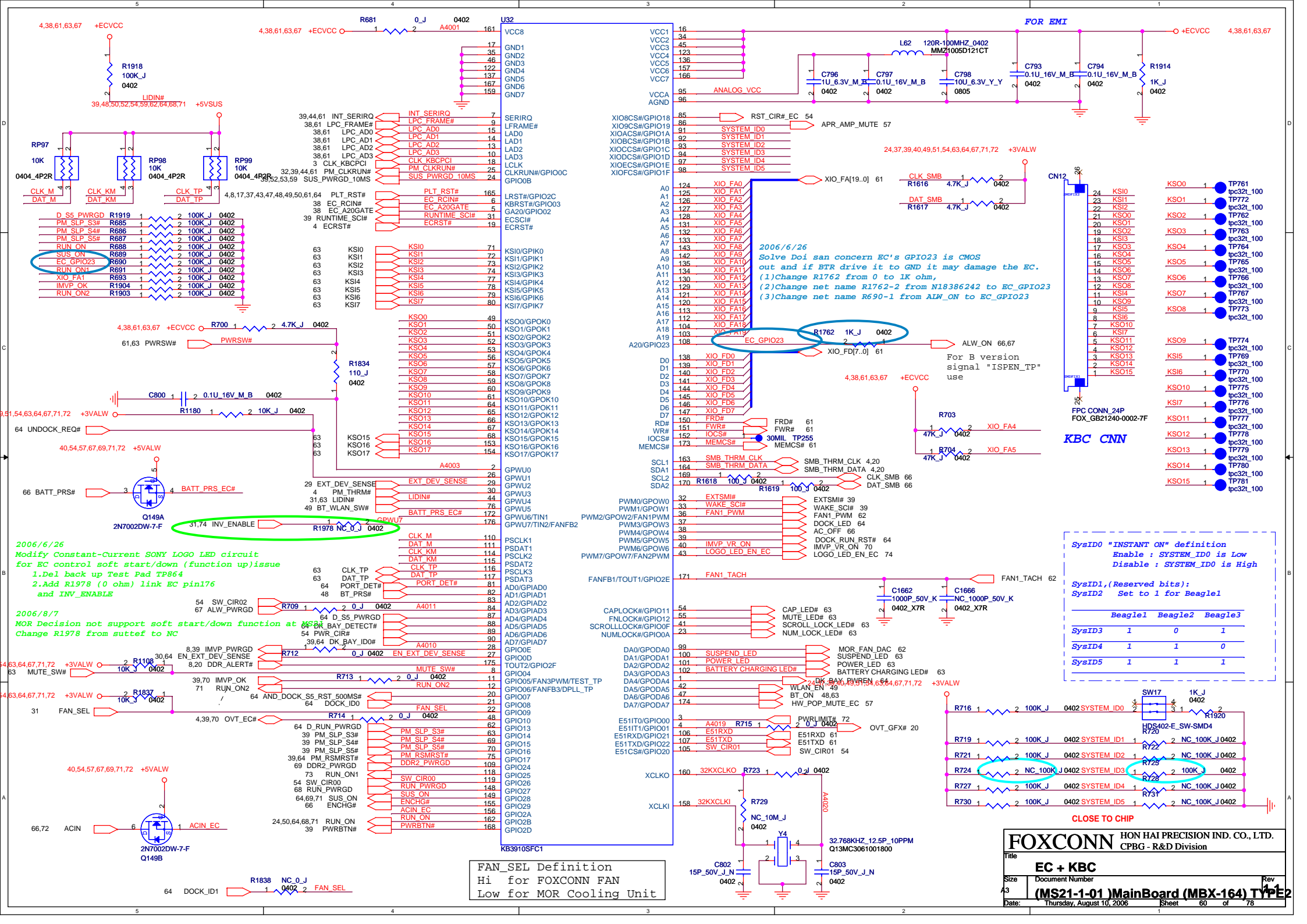


Original EMI back up solution to continue with MS20 (bridge between GND and A_GND)



BFT Test Pad





2006/6/26
 Modify Constant-Current SONY LOGO LED circuit
 for EC control soft start/down (function up/issue)
 1. Del back up Test Pad TP864
 2. Add R1978 (0 ohm) link EC pin176
 and INV_ENABLE

2006/8/7
 MOR Decision not support soft start/down function at BAY DETECT#
 Change R1978 from suttef to NC

FAN_SEL Definition
 Hi for FOXCONN FAN
 Low for MOR Cooling Unit

2006/6/26
 Solve Doi sun concern EC's GPIO23 is CMOS
 out and if BTR drive it to GND it may damage the EC.
 (1) Change R1762 from 0 to 10 ohm
 (2) Change net name R1762-2 from N18386242 to EC_GPIO23
 (3) Change net name R690-1 from ALW_ON to EC_GPIO23

SysID0 "INSTANT ON" definition
 Enable : SYSTEM_ID0 is Low
 Disable : SYSTEM_ID0 is High

SysID1,(Reserved bits):
 SysID2 Set to 1 for Beagle1

	Beagle1	Beagle2	Beagle3
SysID3	1	0	1
SysID4	1	1	0
SysID5	1	1	1

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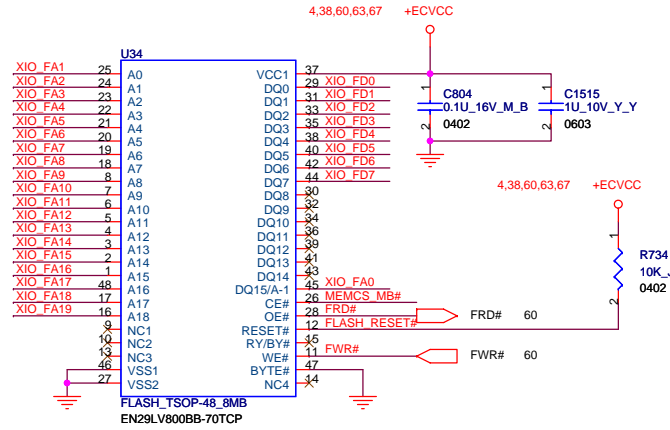
Title: **EC + KBC**

Size: 43 Document Number: **(MS21-1-01) MainBoard (MBX-164) TYPE2**

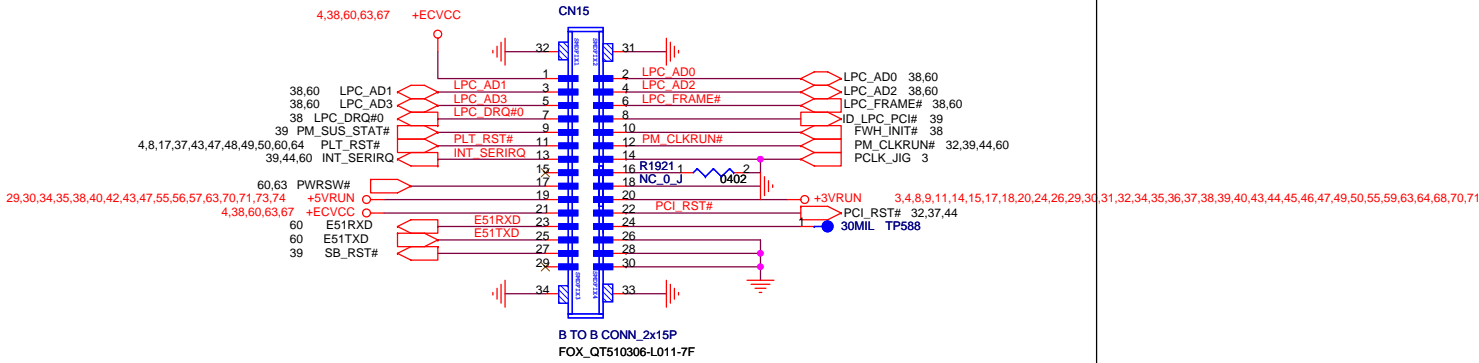
Date: Thursday, August 10, 2006 Sheet 60 of 78

FLASH BIOS

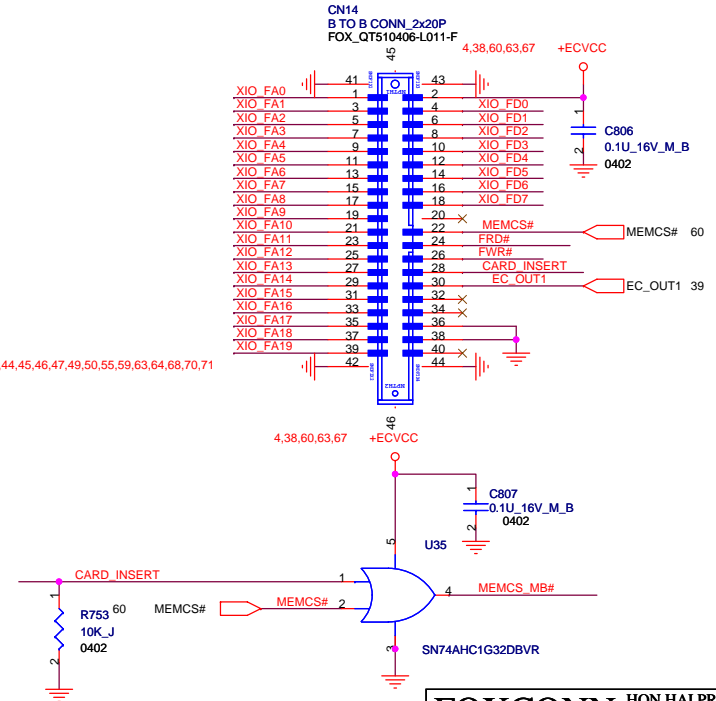
60 XIO_FA[19..0]
60 XIO_FD[7..0]



JIG-120



X-BUS



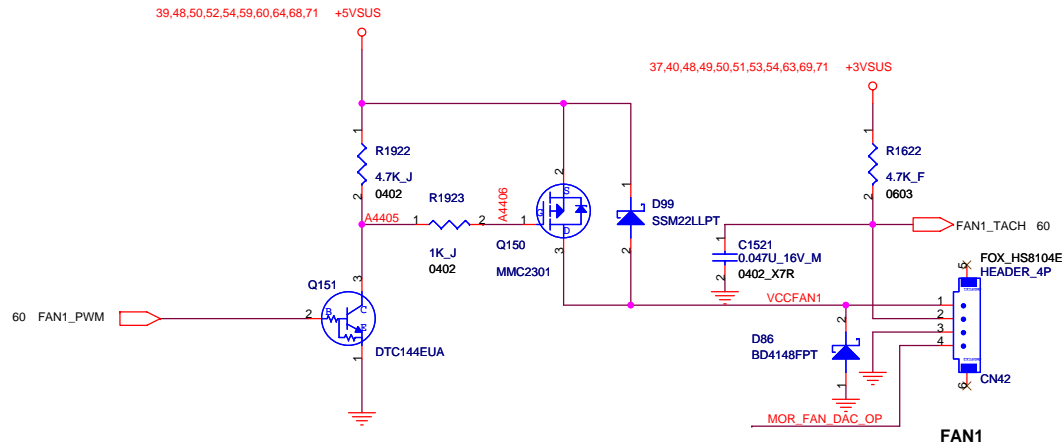
FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: **Flash ROM + Jig-120 + XBUS**

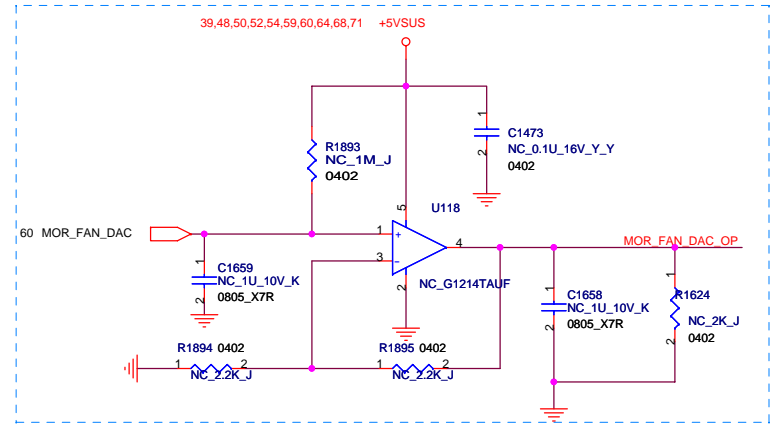
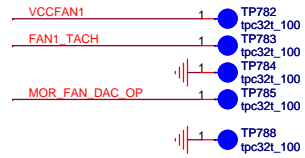
Size: 43 Document Number: (MS21-1-01) MainBoard (MBX-164) TYPE 2

Date: Thursday, August 10, 2006 Sheet 61 of 78

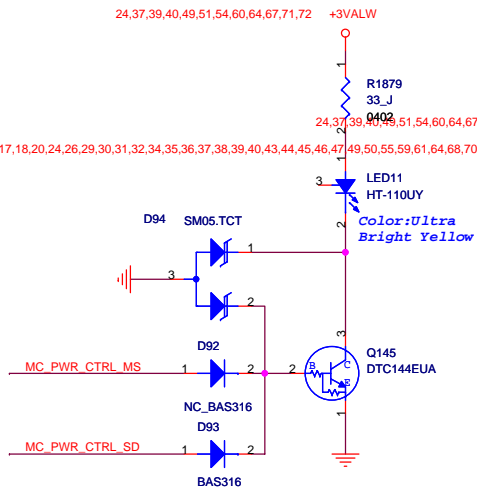
FAN(FAN1+MOR FAN)



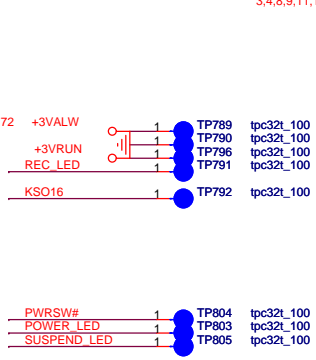
FAN1



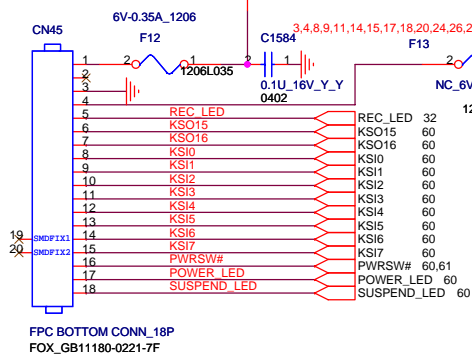
6/28 MOR fan circuit modify to backup
 (NC)U118
 (NC)R1893
 (NC)R1894
 (NC)R1895
 (NC)R1624
 (NC)C1473



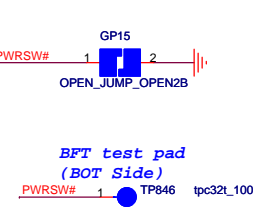
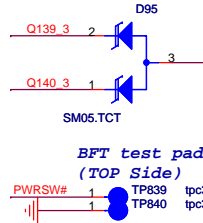
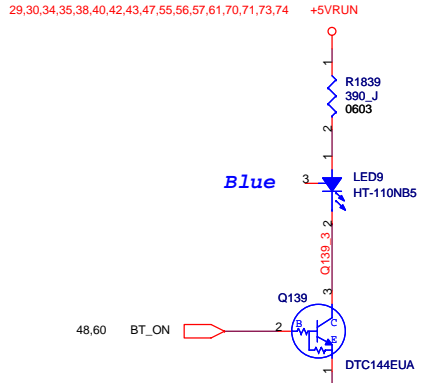
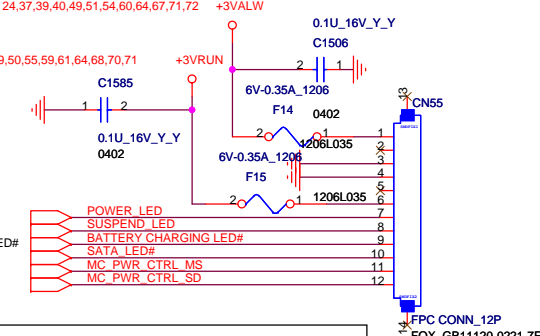
**SD LED
BLUETOOTH LED**



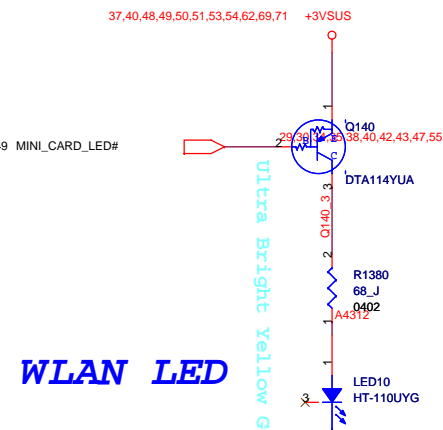
To Power Button Board Connector



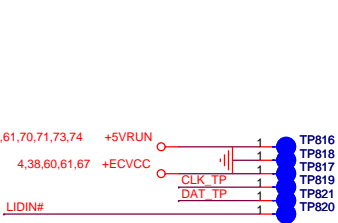
To LED Board Connector



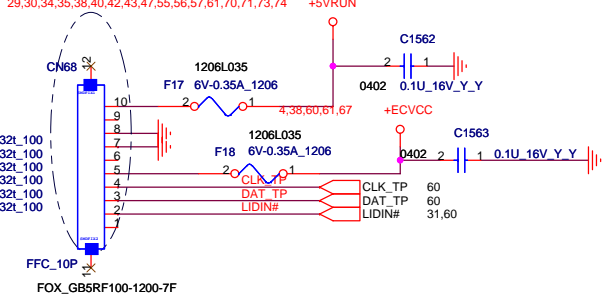
CN68 Change from MOLEX to FOXCONN By kain 0517



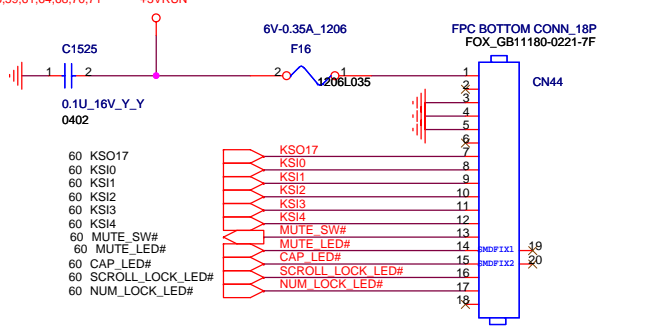
LED IF SPEC:
20mA(TYP), 30mA(MAX)



To Touch Pad Board Connector



To AV Function Board Connector



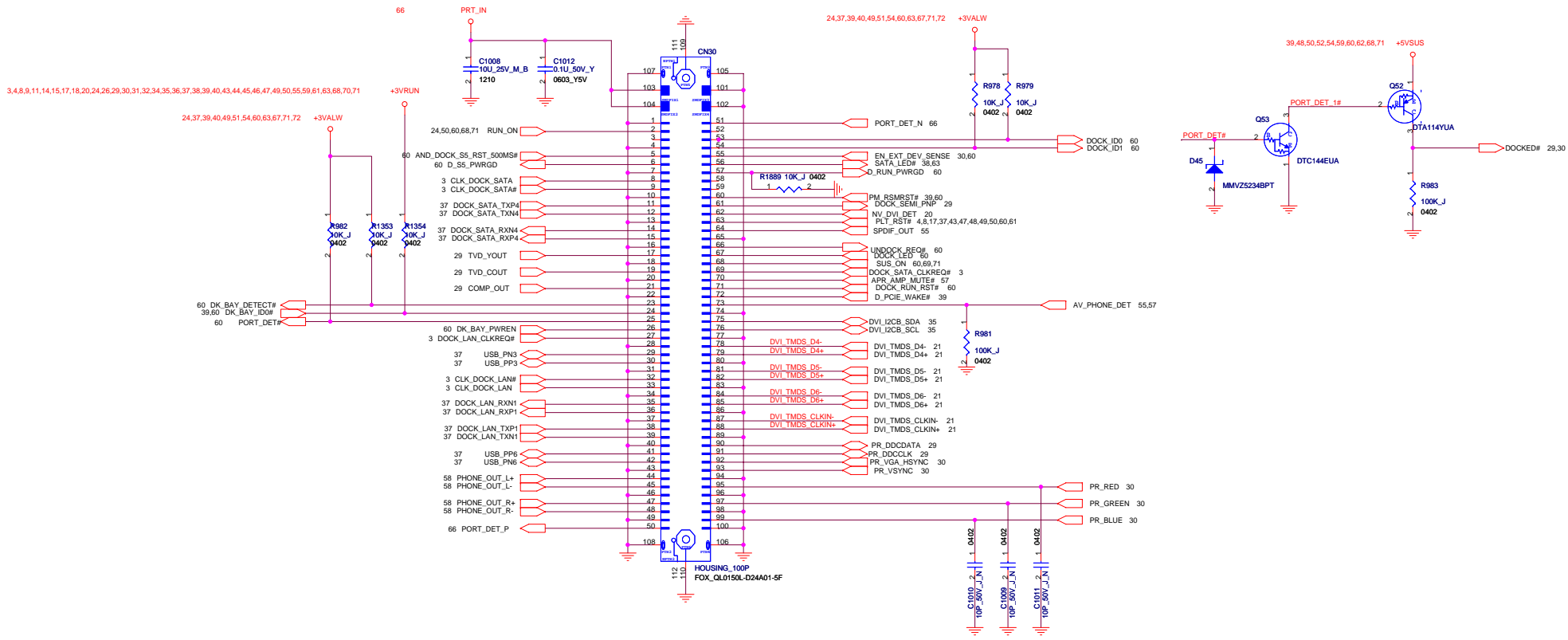
062606: Move Logo Led Circuit module to page 74.

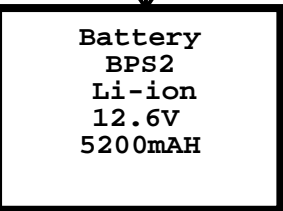
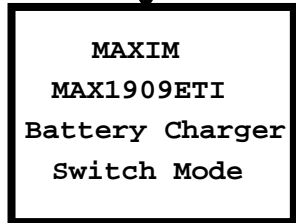
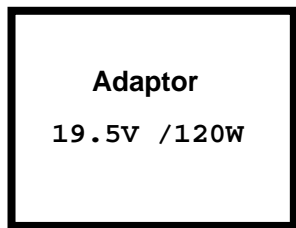
FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: **POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED**

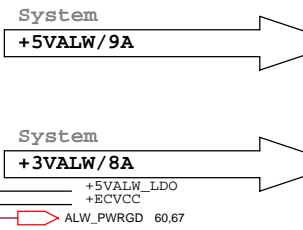
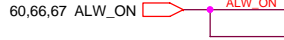
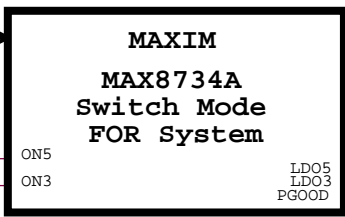
Size: Document Number
43 **(MS21-1-01) MainBoard (MBX-164) TYPE 2** Rev

Date: Thursday, August 10, 2006 Sheet 63 of 78

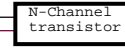




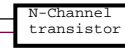
DCBATOUT



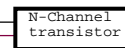
60,64,69,71 SUS_ON



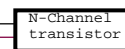
+5VSUS/3.1A



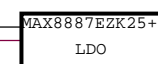
+5VRUN/4.5A



+3VSUS/1.5A

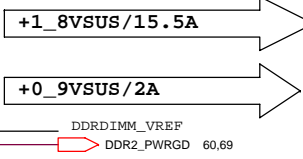
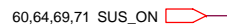
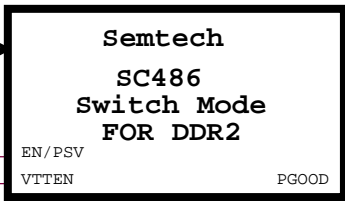


+3VRUN/7A

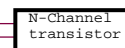


+2_5VRUN/300mA

DCBATOUT

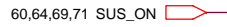
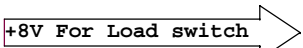
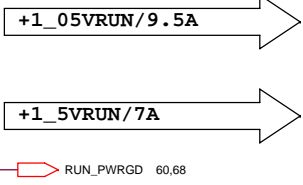
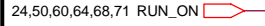
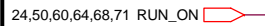
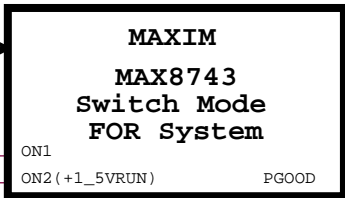


60,71 RUN_ON2

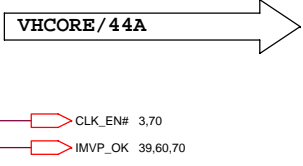
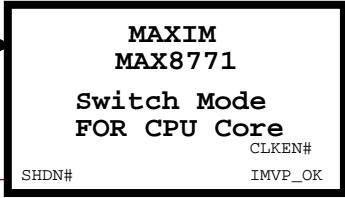


+1_8VRUN/6A

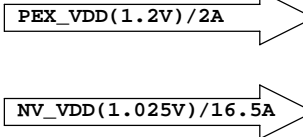
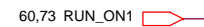
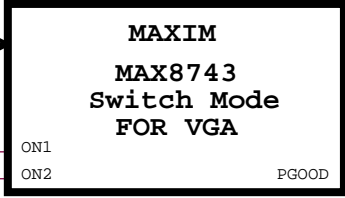
DCBATOUT



DCBATOUT



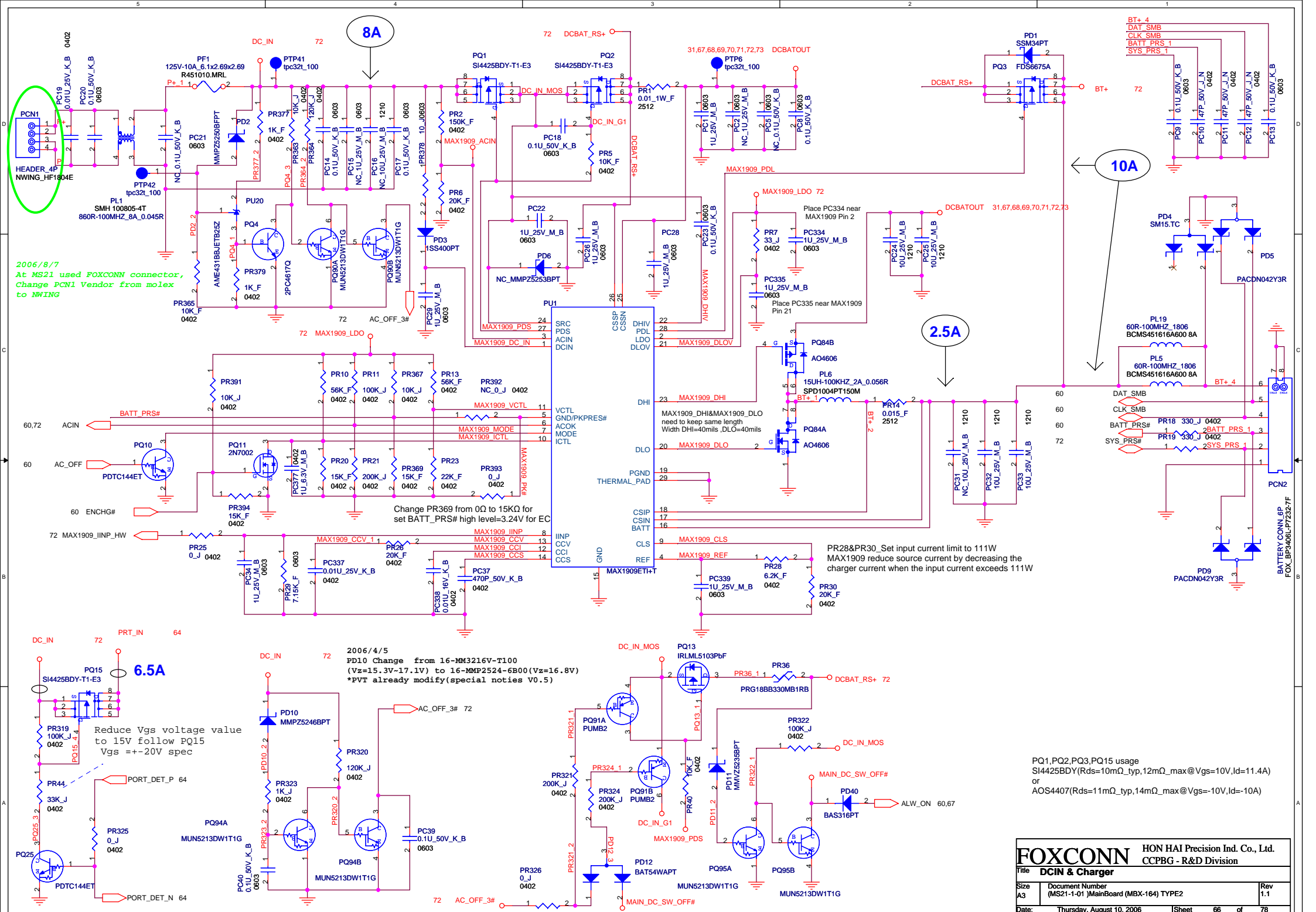
DCBATOUT



DCBATOUT

ENCHG#

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Power Design Diagram-ZG			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 65	of 78	



2006/8/7
 At MS21 used FOXCONN connector,
 Change PCN1 Vendor from molex
 to Nwings

2006/4/5
 PD10 Change from 16-MM3216V-T100
 (Vz=15.3V-17.1V) to 16-MMP2524-6B00 (Vz=16.8V)
 *PVT already modify (special notice V0.5)

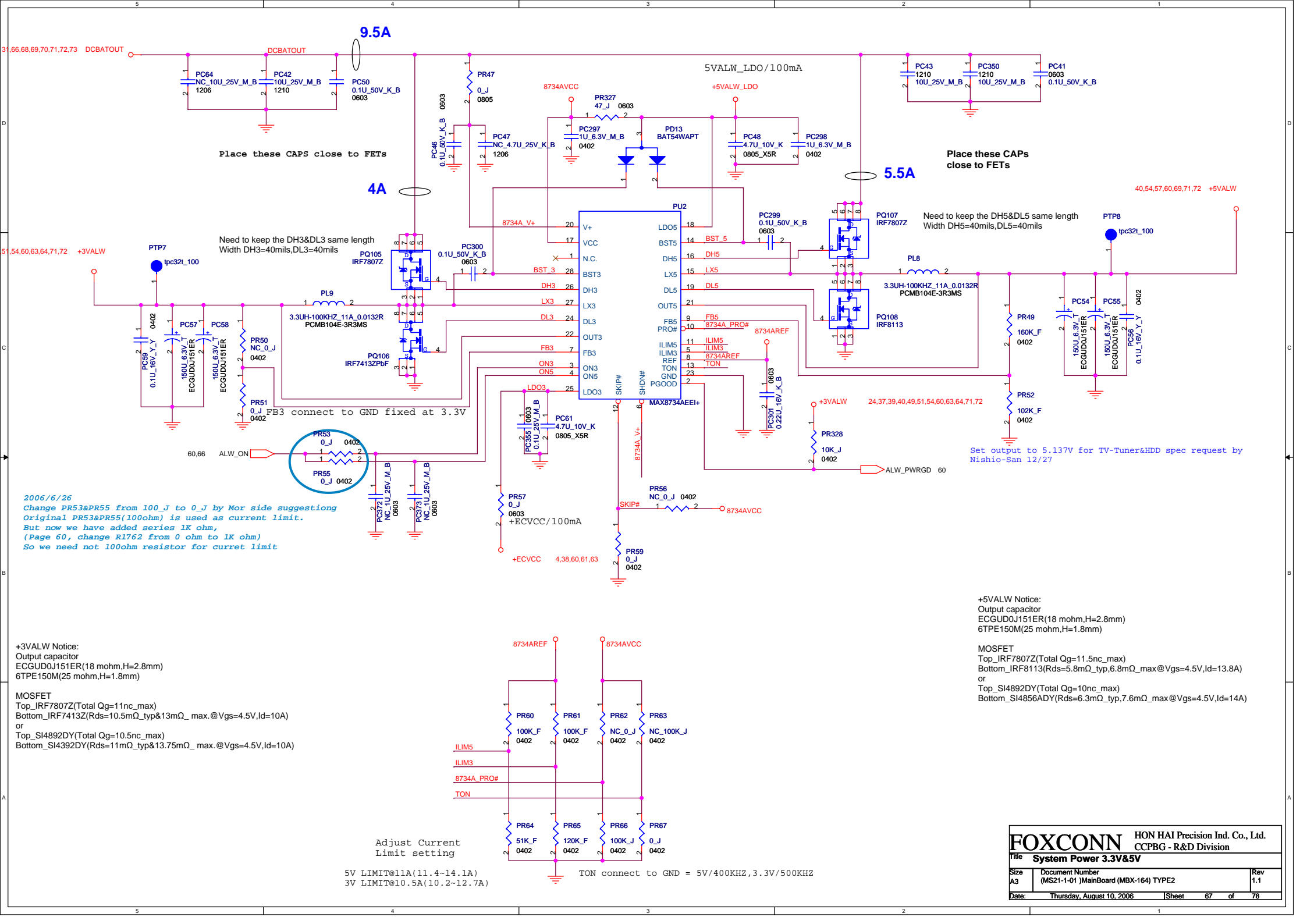
Reduce Vgs voltage value
 to 15V follow PQ15
 Vgs = +-20V spec

PR28&PR30_Set input current limit to 11W
 MAX1909 reduce source current by decreasing the
 charger current when the input current exceeds 11W

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title **DCIN & Charger**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 66	of 78



Place these CAPS close to FETs

Place these CAPS close to FETs

Need to keep the DH3&DL3 same length
Width DH3=40mils, DL3=40mils

Need to keep the DH5&DL5 same length
Width DH5=40mils, DL5=40mils

2006/6/26
Change PR53&PR55 from 100_J to 0_J by Mor side suggesting
Original PR53&PR55(100ohm) is used as current limit.
But now we have added series 1K ohm,
(Page 60, change R1762 from 0 ohm to 1K ohm)
So we need not 100ohm resistor for curret limit

+3VALW Notice:
Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
6TPE150M(25 mohm,H=1.8mm)

MOSFET
Top_IRF7807Z(Total Qg=11nc_max)
Bottom_IRF7413Z(Rds=10.5mΩ_typ&13mΩ_max.@Vgs=4.5V,Id=10A)
or
Top_SI4892DY(Total Qg=10.5nc_max)
Bottom_SI4392DY(Rds=11mΩ_typ&13.75mΩ_max.@Vgs=4.5V,Id=10A)

+5VALW Notice:
Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
6TPE150M(25 mohm,H=1.8mm)

MOSFET
Top_IRF7807Z(Total Qg=11.5nc_max)
Bottom_IRF8113(Rds=5.8mΩ_typ,6.8mΩ_max@Vgs=4.5V,Id=13.8A)
or
Top_SI4892DY(Total Qg=10nc_max)
Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

Adjust Current
Limit setting

5V LIMIT@11A(11.4~14.1A)
3V LIMIT@10.5A(10.2~12.7A)

TON connect to GND = 5V/400KHZ, 3.3V/500KHZ

Set output to 5.137V for TV-Tuner&HDD spec request by
Nishio-San 12/27

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title System Power 3.3V&5V			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 67	of 78	

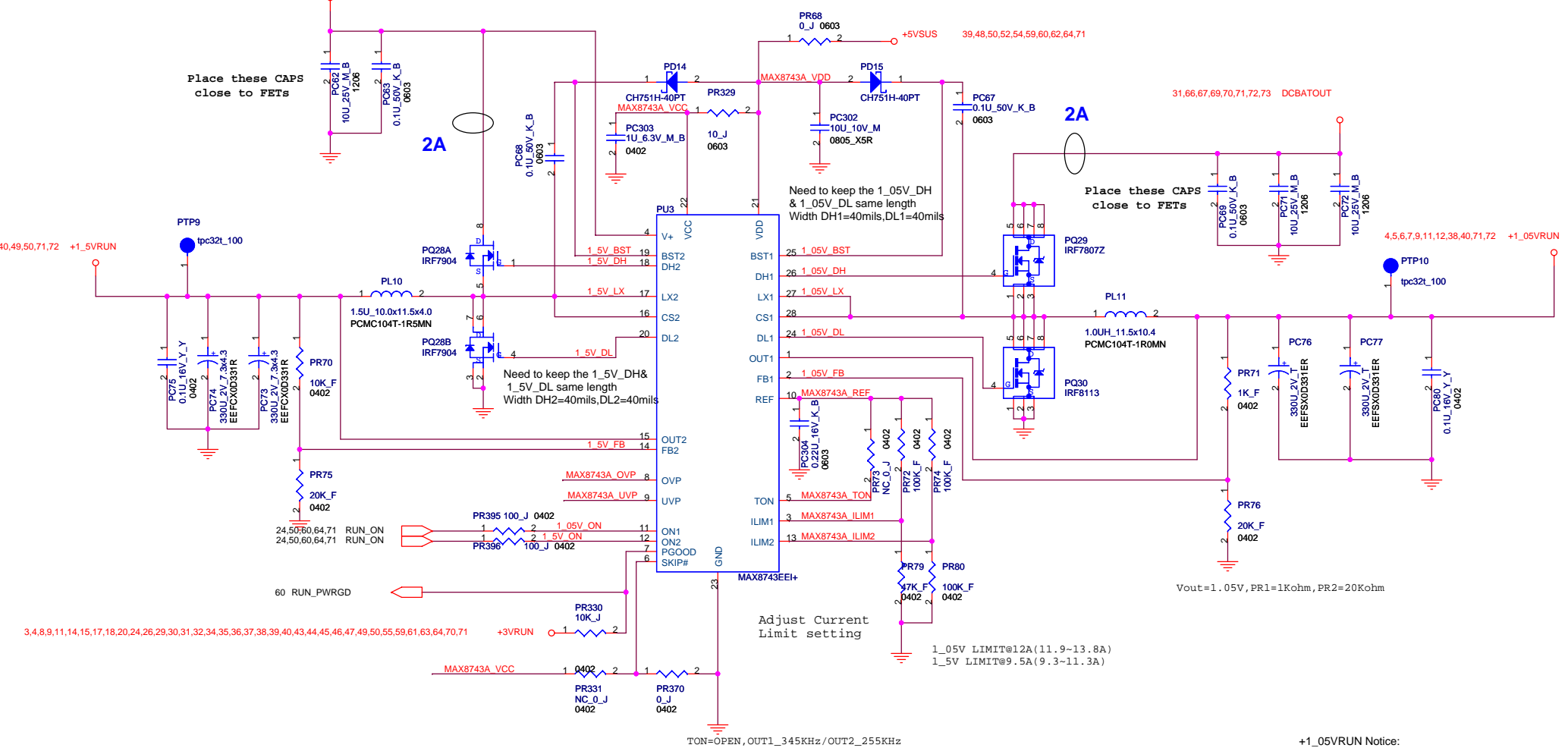
Use +5VSUS for PU3 pin21 to ensure
PU3 will ready before PU3 pin11,12 trun high

31,66,67,69,70,71,72,73 DCBATOUT

Place these CAPS
close to FETs

31,66,67,69,70,71,72,73 DCBATOUT

Place these CAPS
close to FETs

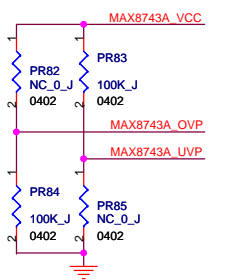


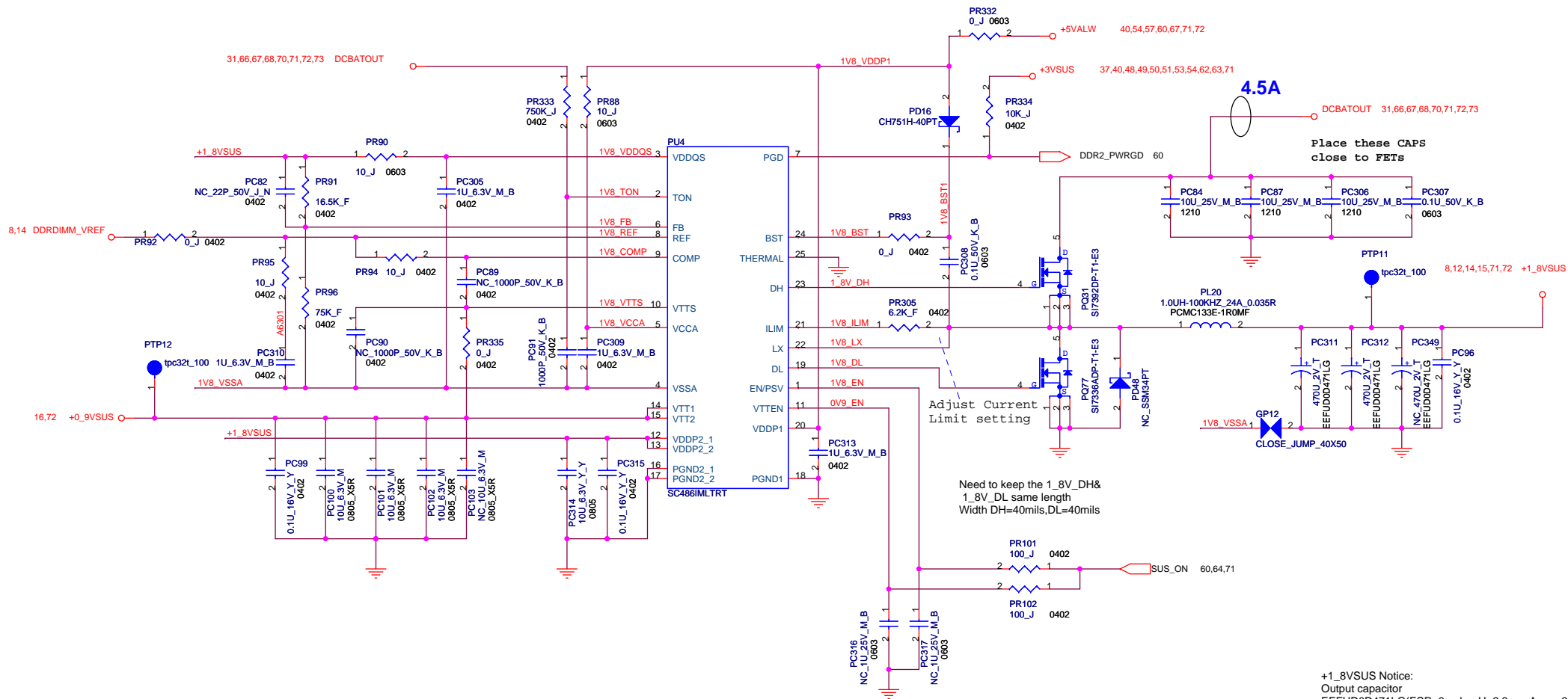
+1_5VVRUN Notice:
Output capacitor
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1A)

MOSFET(Top+Bottom)
IRF7904(Low side Rds=10.5mΩ_typ,13mΩ_max@Vgs=4.5V,Id=8.9A)

+1_05VVRUN Notice:
Output capacitor usage
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_IRF7807Z(Total Qg=11.5nc_max)
Bottom_IRF8113(Rds=5.8mΩ_typ,6.8mΩ_max@Vgs=4.5V,Id=13.8A)
or
Top_SI4892DY(Total Qg=10nc_max)
Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)





Place these CAPS close to FETs

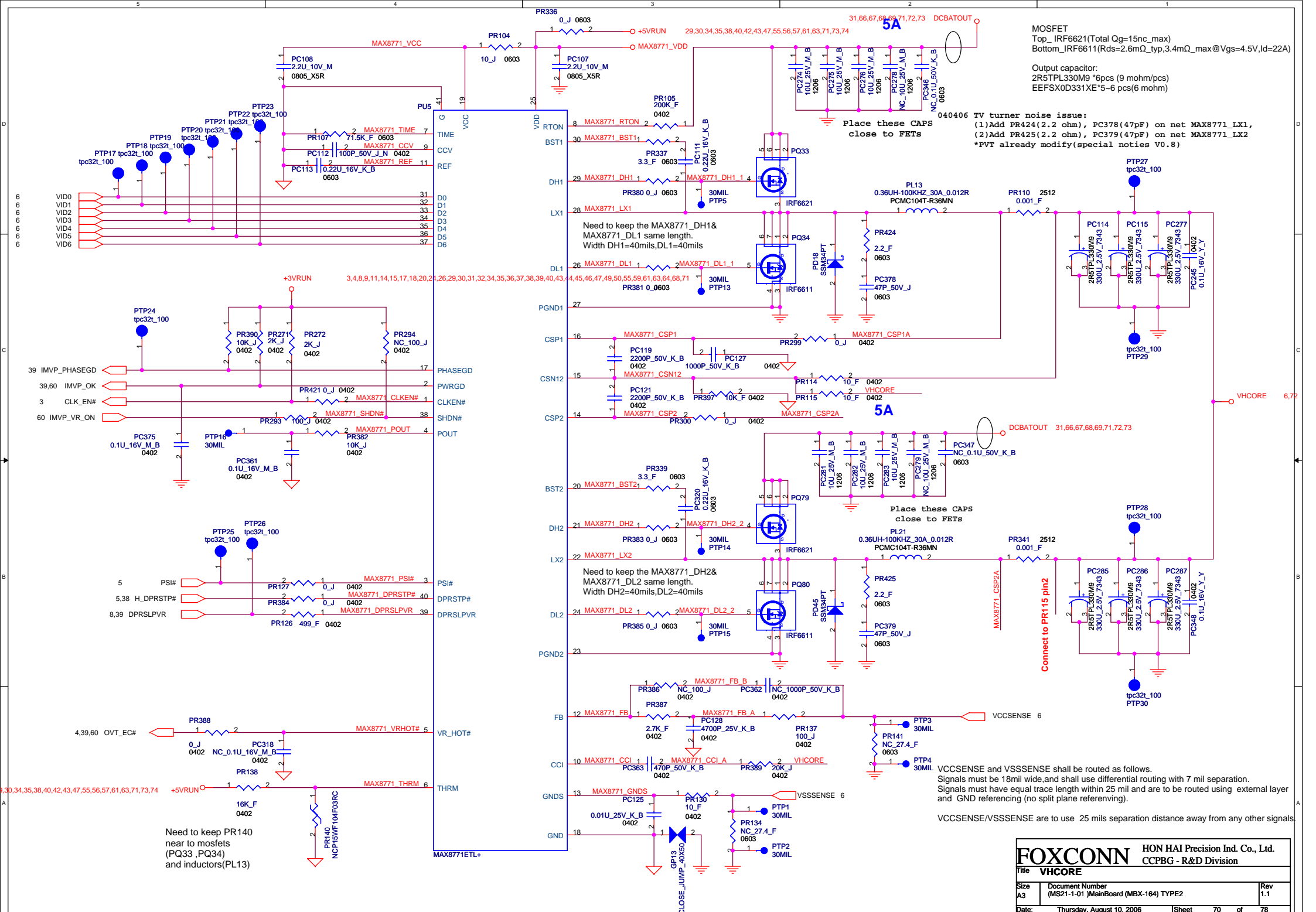
Adjust Current Limit setting

Need to keep the 1.8V_DH & 1.8V_DL same length
Width DH=40mils, DL=40mils

+1.8VSUS Notice:
Output capacitor
EEFUD0471LG(ESR=9mohm,H=2.8mm,Arms=3.4A)
2R5TPE470M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_Si7392DP(Total Qg=15nc_max)
Bottom_Si7336ADP(Rds=3.1mΩ_typ,4.0mΩ_max@19A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8mΩ_max@25A)

1.8V LIMIT@20A(19.2-24A)



MOSFET
 Top_ IRF6621 (Total Qg=15nc_max)
 Bottom_IRF6611 (Rds=2.6mΩ typ, 3.4mΩ_max @ Vgs=4.5V, Id=22A)

Output capacitor:
 2R5TPL330M9 *6pcs (9 mohm/pcs)
 EEFSX0D331XE*5-pcs(6 mohm)

TV turner noise issue:
 (1) Add PR424 (2.2 ohm), PC378 (47pF) on net MAX8771_LX1,
 (2) Add PR425 (2.2 ohm), PC379 (47pF) on net MAX8771_LX2
 *PVT already modify (special notes V0.8)

Need to keep the MAX8771_DH1 &
 MAX8771_DL1 same length.
 Width DH1=40mils, DL1=40mils

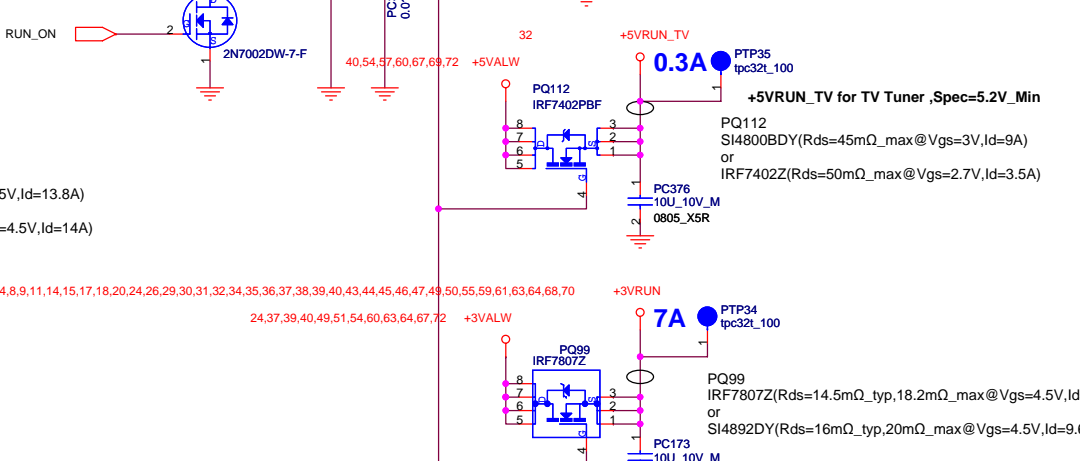
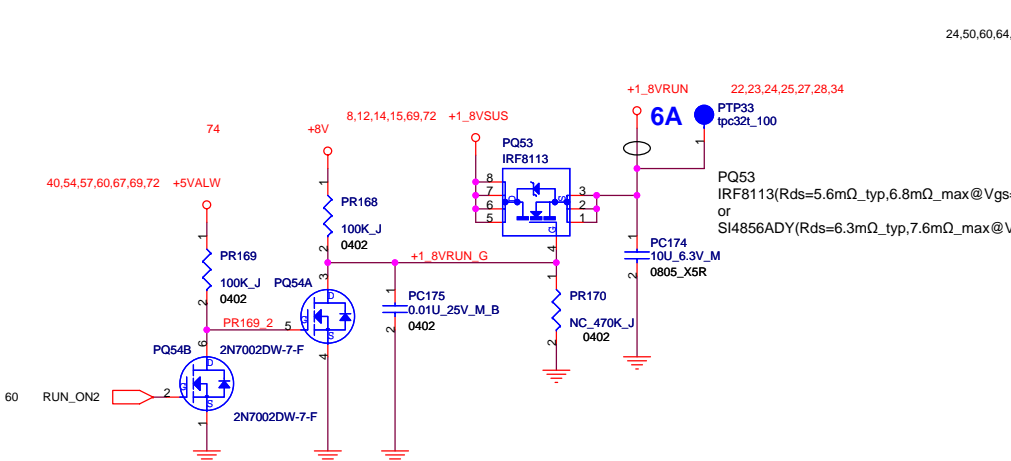
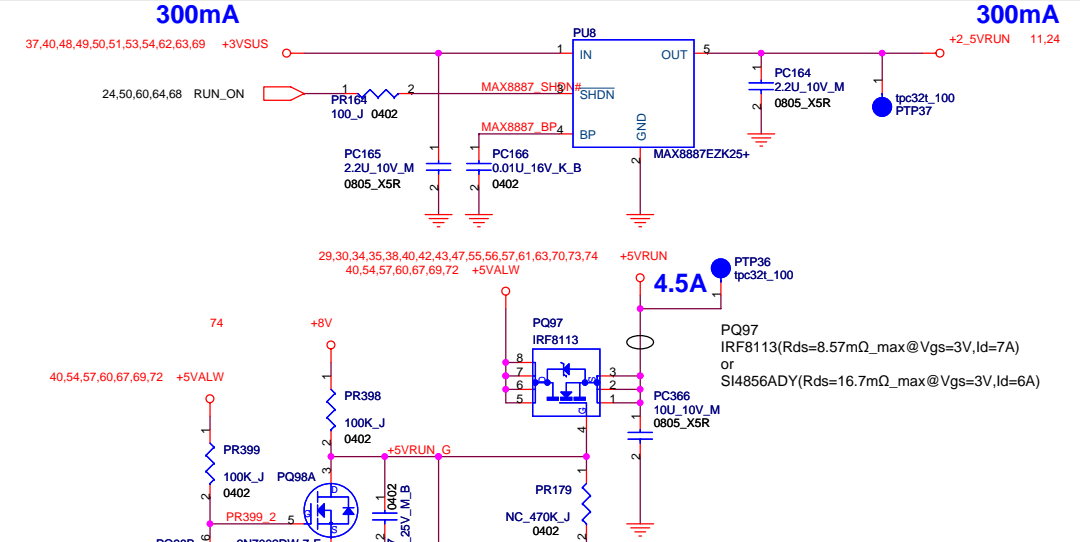
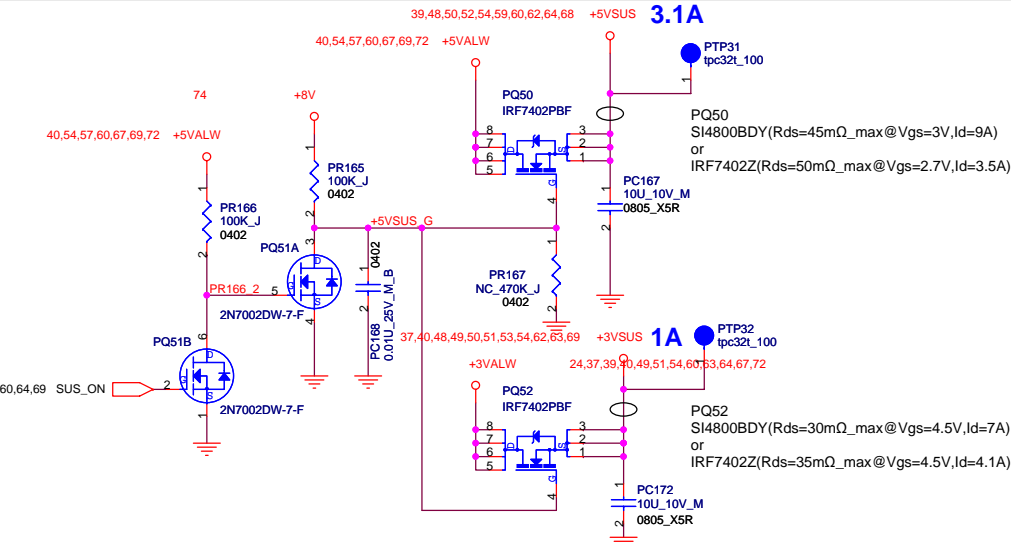
Need to keep the MAX8771_DH2 &
 MAX8771_DL2 same length.
 Width DH2=40mils, DL2=40mils

Need to keep PR140
 near to mosfets
 (PQ33, PQ34)
 and inductors (PL13)

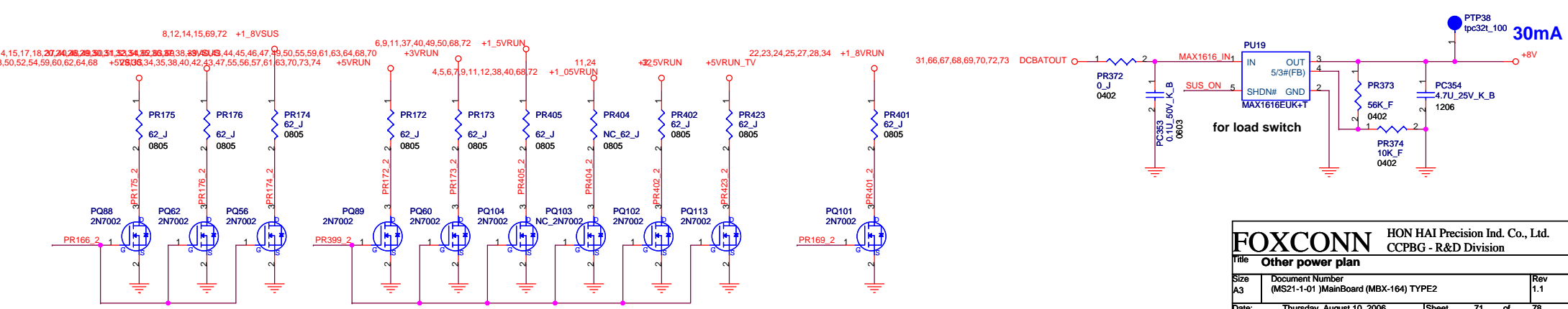
VCCSENSE and VSSSENSE shall be routed as follows.
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
 Signals must have equal trace length within 25 mil and are to be routed using external layer
 and GND referencing (no split plane referencing).

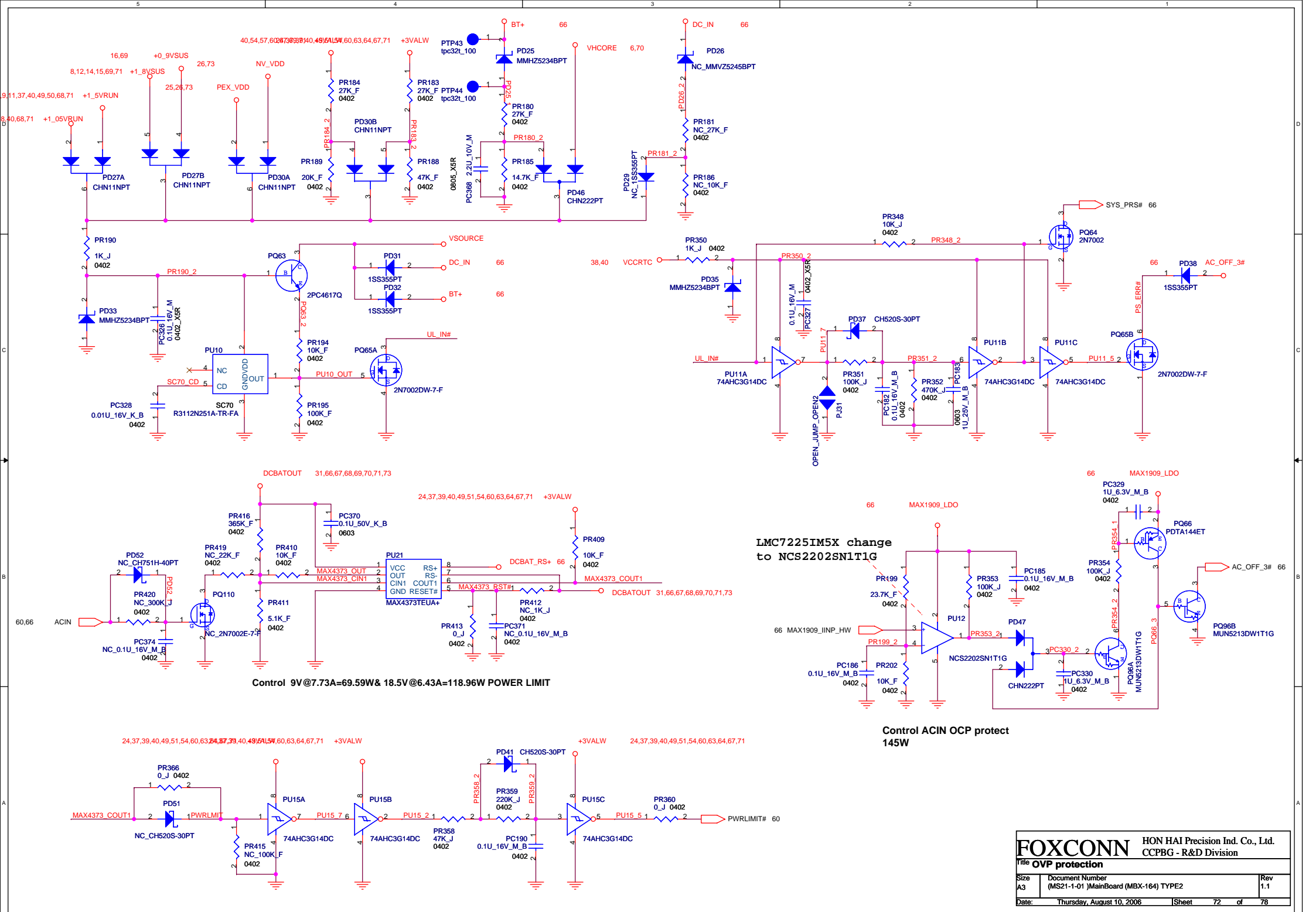
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

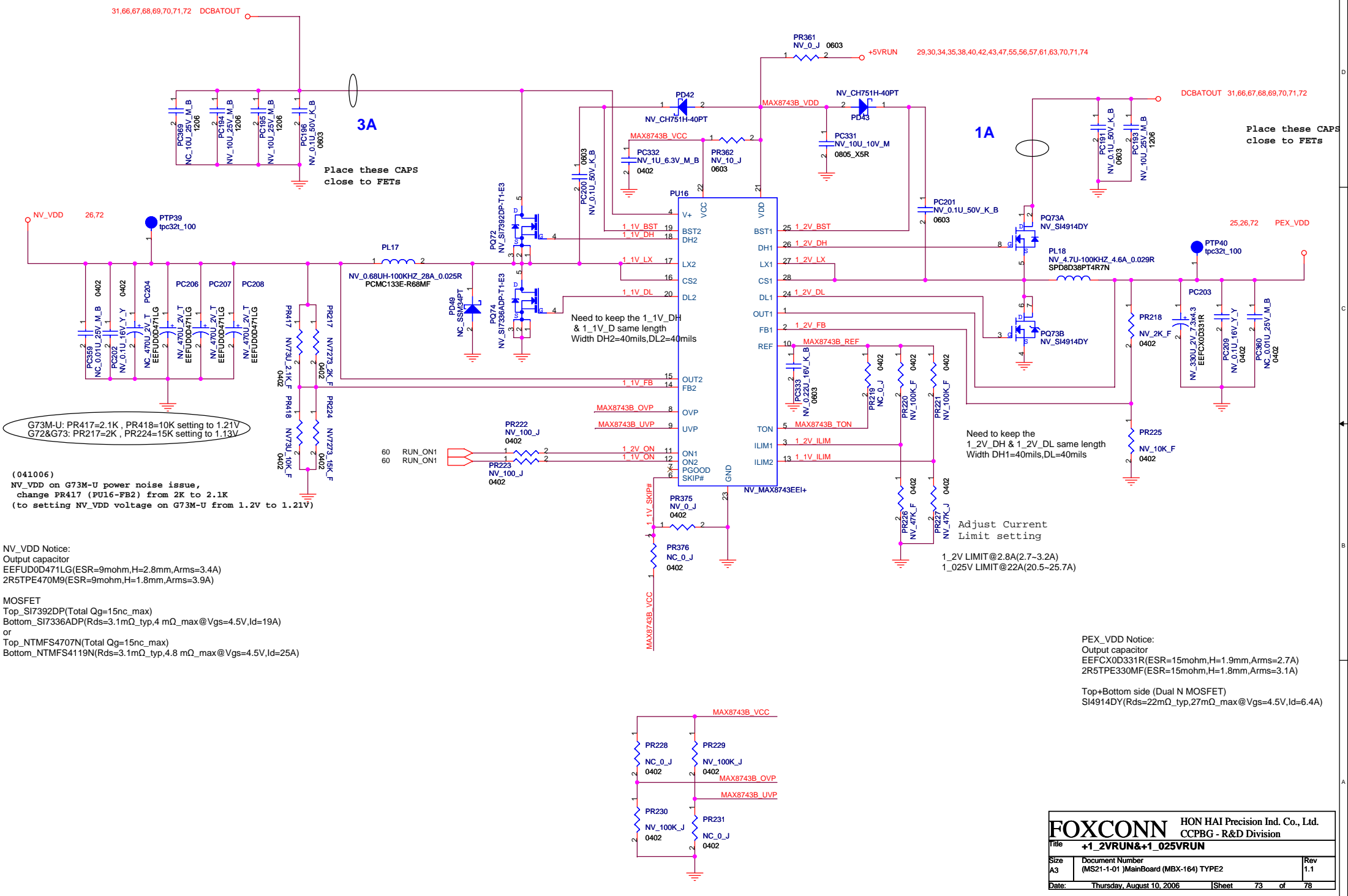
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title VHCORE		CCPBG - R&D Division	
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 70	of 78	



Discharge circuit for power-off







NV_VDD 26.72

PTP39 tpc32t_100

PC359 NC_0.01U_25V_M_B 0402
 PC360 NV_0.1U_16V_X_Y 0402
 PC204 NV_470U_2V_T EEFUD00471G
 PC206 NV_470U_2V_T EEFUD00471G
 PC207 NV_470U_2V_T EEFUD00471G
 PC208 NV_470U_2V_T EEFUD00471G

G73M-U: PR417=2.1K, PR418=10K setting to 1.21V
 G72&G73: PR217=2K, PR224=15K setting to 1.13V

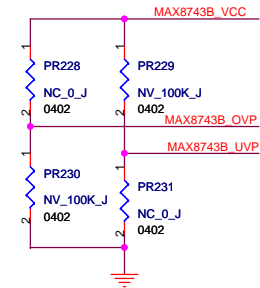
(041006)
 NV_VDD on G73M-U power noise issue,
 change PR417 (PU16-FB2) from 2K to 2.1K
 (to setting NV_VDD voltage on G73M-U from 1.2V to 1.21V)

NV_VDD Notice:
 Output capacitor
 EEFUD0D471LG (ESR=9mohm,H=2.8mm,Arms=3.4A)
 2R5TPE470M9 (ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
 Top_S17392DP (Total Qg=15nc_max)
 Bottom_S17336ADP (Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
 or
 Top_NTMFS4707N (Total Qg=15nc_max)
 Bottom_NTMFS4119N (Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

PEX_VDD Notice:
 Output capacitor
 EEFCX0D331R (ESR=15mohm,H=1.9mm,Arms=2.7A)
 2R5TPE330MF (ESR=15mohm,H=1.8mm,Arms=3.1A)

Top+Bottom side (Dual N MOSFET)
 SI4914DY (Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)



Modify Constant-Current SONY LOGO LED circuit

for U138 cost issue

- 1.Back up:U138(MAX1916EZT),R1936 (91K ohm,0402),R1982(OR,NC),R1983(OR,NC)
- 2.Remove back up solution U139(GMT,G5920TB1UE),C1660(0.1u)
- 3.Add new Constant-Current circuit (OP + MOS)
 - 51K ohm: R1972 ,
 - 1.2K ohm: R1973 ,
 - 1k ohm:R1974 ,
 - 10 ohm: R1975
 - (NC)0 ohm: R1976(for back up U138 MAX1916)
 - 0.1uF,16V: C1679
 - (NC)22uF,6.3V: C1680
 - OP LM358 ADR : U139
 - N-MOS 2N7002: Q158
 - N-MOS DTA114YUA:Q159
 - P-MOS DTC144EUA:Q160

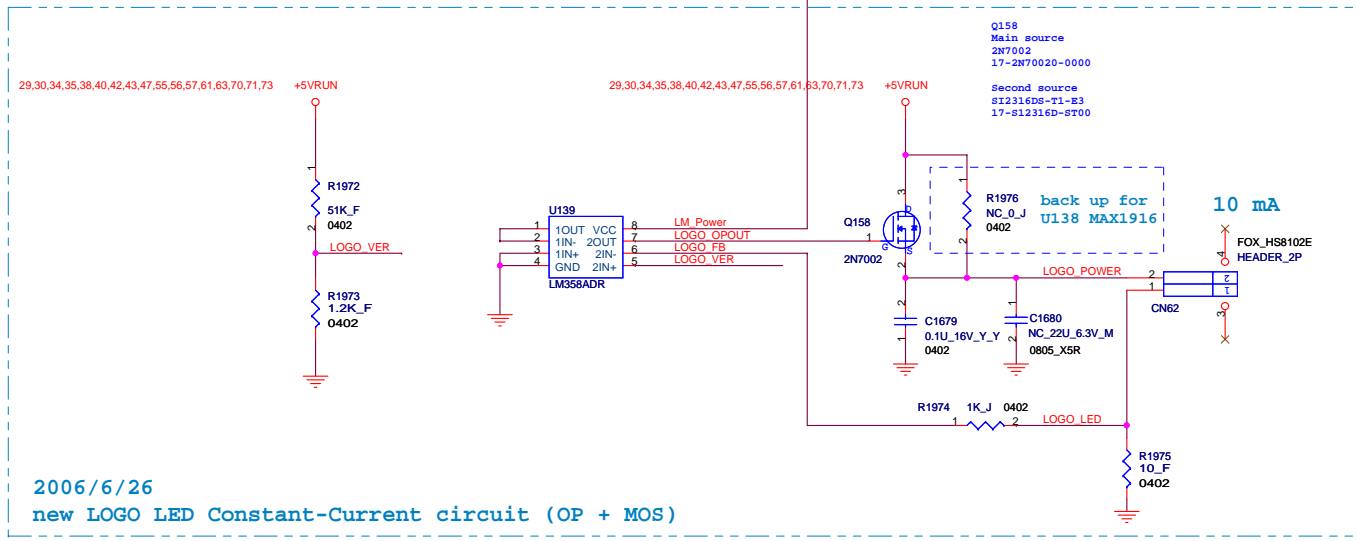
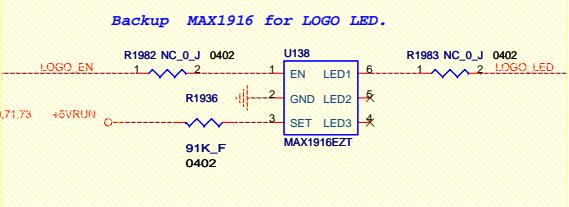
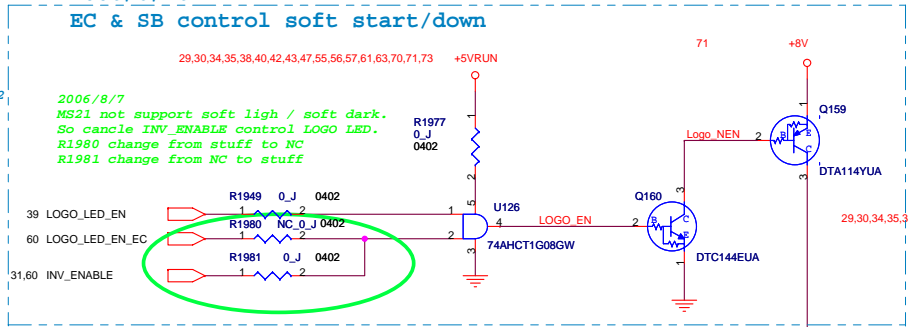
Constant-Current SONY LOGO LED

for EC control soft start/down (function up)issue

- 1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
- 2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
- 3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
- 4.Add R1977 between +5VRUN to U126 pin5(VCC)
- 5.Add R1980 between Logo_led_en_ec to U126 pin2

2006/6/26

EC & SB control soft start/down



2006/6/26

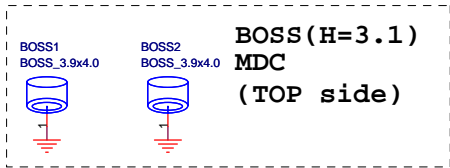
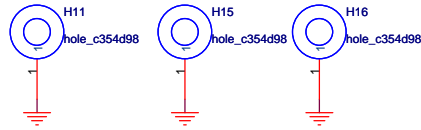
new LOGO LED Constant-Current circuit (OP + MOS)

2006/6/26
 (1)remove TP835(GND Test Pad)
 (2)add TP857(LOGO_POWER)

2006/6/26
 (Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP)
 Detail location
 10U_25V_M*9pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390) ,
 0.01U_25V_K*1pcs(PC387) ,1U_25V_M*1pcs(PC388) ,0.22U_16V_M*1pcs(PC391) ,
 220P_50V_K*1pcs(PC392) ,SKS30-04AT-G*1pcs(PD53) ,8UH-100KHZ_2.5A_0.07R*1pcs(PL22) ,
 2N7002*2pcs(PQ9114,PQ116) ,FDS6680A*1pcs(PQ117) ,120K_F*1pcs(PR432) ,
 0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435) ,10K_F*1pcs(PR436) ,MAX668EUB+T*1pcs(PU22) ,

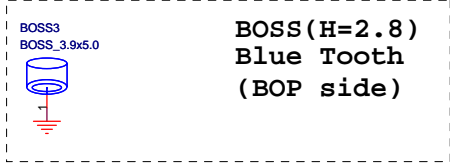
HOLE

Type 1



Type 2

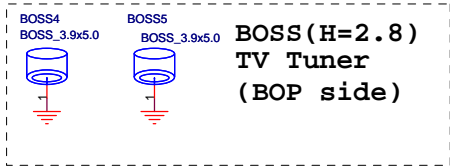
2005/10/24
Remove Screw Hole H2 P/N 1X-HOLE000-0108
because the Hole overlay with CN32 and layout will
modify component screw shipe



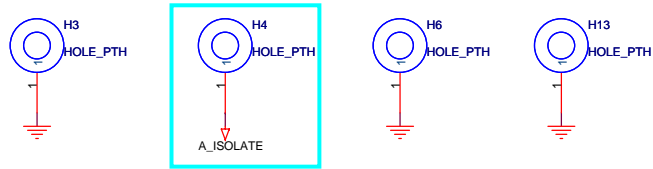
Type 3

2005/10/24
Remove Screw Hole H1 P/N 1X-HOLE000-0110
because the Hole overlay with CN32 and layout will
modify component screw shipe

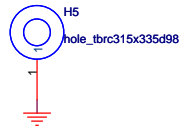
2006/5/6
Separat analog ground for digital Noise issue:
Isolate screw hole H4 Change H4 net name from
A_GND to A_ISOLATE



Type 4



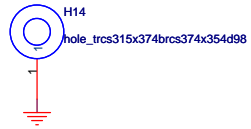
Type 5



Type NPTH Guide (spherical)HOLD



Type 6



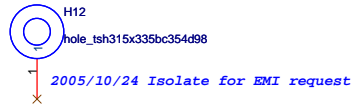
Type NPTH Guide (oval-shaped)HOLD



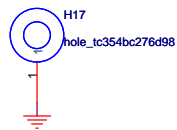
Type 7



Type 8



Type 9



Type CPU



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		HOLE & BOSS	
Size	Document Number	Rev	
A3	(MS21-1-01)MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	75 of 78

MS20 MP to MS21 DVT Change History

(2006/5/23)

- (川) 01.(Page08) Remove R110 for PM_EXTTSH1 back up pull up res.ICH7 (DPRSLPVR)already have internal pull up
- (川) 02.(Page14) Remove backup DIMM thermal sensor Change R168 from stuff to NC(basis on MS20 MP ECR)
- (川) 03.(Page15) Remove backup DIMM thermal sensor Change R1627 from stuff to NC(basis on MS20 MP ECR)
- (蘭) 04.(Page34) US Silicon Image ATC test HDMI DDC capacitance fail(>50pF)change U128 no stuff Basis on MS20 MP ECR add back up res.(R1962)no stuff for U128 VCC
- (才) 05.(Page39) Delete U30,R1183,R649 (backup circuit)
- (業) 06.(Page42) For power droop cause 0.16V voltage loss issue(1)F7,F8,F19,F20 no stuff(2)Co-layout GP17-GP20 with fuse
- (業) 07.(Page55) Separate analog ground for digital Noise issue
(1)Add bead (L152)before LDO chipand
(2)Change C873 from GND to A_GND
(3)Add C1675 on +5VRUN before L152
- (業) 08.(Page56) Shoei CAP will EOL. CAP24,CAP25(SF CAP) change to Stuff: CAP22,CAP23(Shoei CAP) change to No Stuff
- (業) 09.(Page56) PBSS2515F.115 will EOL ,Q77,Q78,Q143,Q144 change to PBSS2515E.115
- (業) 10.(Page56) Improve the voice of speaker up to 0.94W
(1)Add damping Resistors R1953 on SRIN,R1954 on AMP_SLIN then speaker amp output won't be distorted.
(2)Change R1932 from 6.8K to 5.6K, then amp gain change from 8dB to 10dB.
- (業) 11.(Page57) PBSS2515F.115 will EOL Q89,Q90,Q91,Q92 change to PBSS2515E.115
- (業) 12.(Page59) Improve SMR issue,Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .
- (業) 13.(Page59) Separate analog ground for digital Noise issue:
(1)Remove GP3 (Close Jumper)not bridge between GND and A_GND
(2)Backup two jumper resistors for bridge between GND and A_GND (C1388,C1966 on Screw hole H3,C1957,C1959 on screw hole H5)
(3)Isolate screw hole H4,add 100pF capacitors C1673,C1674 for EM, Zener diode D100 for ESD
(4)Add jumper resistor for Return patch R1955 close L70(+5VAMP), & R1960 close codec
- (才) 14.(Page39) Remove back up circuit LVDS GPIO on U29 pinU2(1)Add Test Pad TP890 on GPIO34(2)Del Q126
- (業) 15.(Page54) Remove back up F6 power source from +3VALW (Del)R1944,R1946
- (業) 16.(Page67) Reserve PC64(10U_25V_M_B 1206) for 1210 size shortage. Change PR57 from 0805 size to 0603 size for 0603 size rated current is also enough.
- (業) 17.(Page70) Add PC375 (0.1uF) to avoid IMVP_OK signal 700mV pulse when power on. Change PC107/PC108 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (業) 18.(Page71) Change PC164/PC165 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (業) 19.(Page71) Change PC368 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage. Change PU12 from LMC7225IM5X to NCS2202SN1T1G for LMC7225IM5X shortage.
- (才) 20.(Page60) Modify system ID setting. R725 from stuff change to NC,R726 from NC change to stuff
- (蘭) 21.(Page32) CN66,CN67 Change from MOLEX(IN-0010000-MWGO) to FOXCONN(IN-0010000-F0T0)
- (業) 22.(Page63) CN68 Change from MOLEX(IN-0010000-MWGO) to FOXCONN(IN-0010000-F0T0)
- (業) 23.(Page57) Add C1676 (4.7 uF/bypass cap) close A_U99 pin8
- (業) 24.(Page58) Add C1677,C1678 (4.7 uF/bypass cap) close A_U101,U102 pin8
- (業) 25.(Page74) Add Inverter Boost Circuit

(2006/5/24)

- (業) 1.(Page55) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1251 change from 33pF 0402 to 1uF 0603
(2) C1252 change from 12pF 0402 to 1uF 0603
(3) C1270 change from 0.1F 0402 to 1uF 0603
(4) Add R1967, R1968 100 ohm 0402
- 2.(Page57) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1231 change from 4.7uF 0805 to 220pF 0402
(2) C1232 change from 1uF 0805 to 4.7uF 0805
(3) C1233 change from 4.7uF 0805 to NC_33pF 0402
(4) C1234 change from 100pF 0402 to NC_33pF 0402
(5) C1237 change from 100pF 0402 to 33pF 0402
(6) R1318 change from 10Kohm 0402 to 5.1Kohm 0402
(7) R1319 change from 1Kohm 0402 to 4.7Kohm 0402
(8) R1320 change from 33ohm 0402 to 100ohm 0402
(9) R1321 change from NC_0ohm 0402 to 4.7Kohm 0402
(10) R1325 change from 47Kohm 0402 to 4.7Kohm 0402
(11) R1326 change from 7.5Kohm 0402 to 2.2Kohm 0402
(12) R1327 change from 100ohm 0402 to 1Kohm 0402
(13) Add R1970, R1971 100 ohm 0402
(14) Add R1969 4.7 Kohm 0402
(15) R1236 change from 4.7u to 1u

(2006/5/26)

- (業) (1) C1230 change from 2200pF to 4700 pF by MOR request

MS21 DVT to MS21 PVT Change History

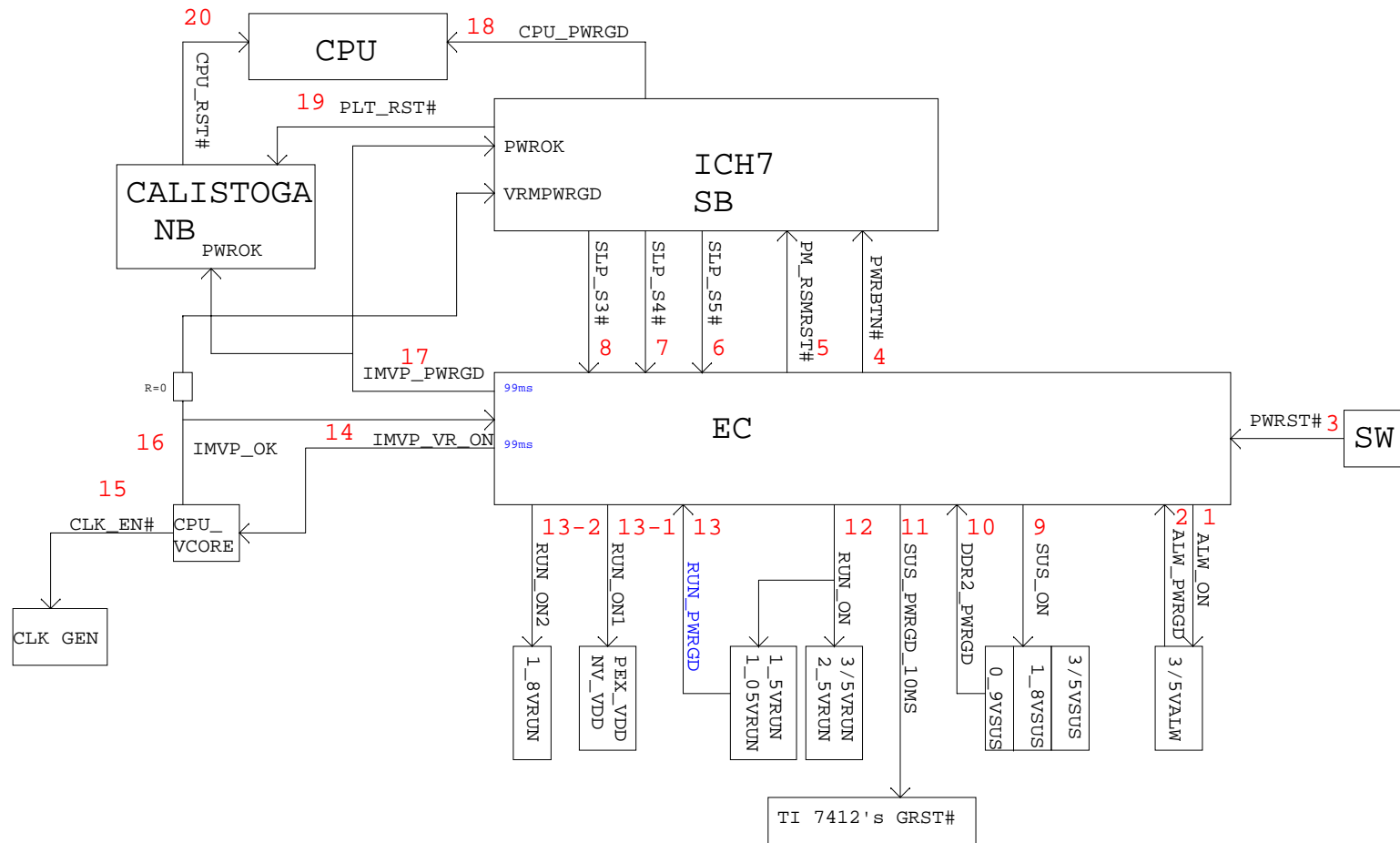
(2006/6/26)

- (才) 01.(Page60) Solve Doi san concern EC's GPIO23 is CMOS out and if BTR drive it to GND it may damage the EC.
(1)Change R1762 from 0 to 1K ohm,
(2)Change net name R1762-2 from N18386242 to EC_GPIO23
(3)Change net name R690-1 from ALW_ON to EC_GPIO23
- (蘭) 02.(Page31) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
(1)Delete PR426&PR427
(2)change C604-1,C1557-1,C1558-1,CN49 pin1, pin2 net name INVERTER_VCC to net DCBATOUT.
- (業) 03.(Page74) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
Delete 10U_25V_M*9pcs(PC380, PC381, PC382, PC383, PC384, PC385, PC386, PC389, PC390),
0.01U_25V_K*1pcs (PC387), 1U_25V_M*1pcs(PC388), 0.22U_16V_M*1pcs(PC391),
220P_50V_K*1pcs(PC392), SKS30-04AT-G*1pcs(PD53), 8UH-100KHZ_2.5A_0.07R*1pcs(PL22),
2N7002*2pcs(PQ114, PQ116), FDS86680A*1pcs(PQ117), 120K_F*1pcs(PR432),
0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435), 10K_F*1pcs(PR436), MAX668EUB+T*1pcs(PU22),
100K_u*1pcs (PR428) 100K_u*1pcs (PR429)
- (業) 04.(Page67)Change PR53&PR55 from 100_J to 0_J by Mor side suggestions
Original PR53&PR55(100ohm) is used as current limit. But now we have added series 1K ohm,
(Page 60, change R1762 from 0 ohm to 1K ohm) So we need not 100ohm resistor for curret limit
- (業) 05.(Page56) Modify internal speaker AMP gain setting, change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W) to fit in speaker (1.0W)spec.
- (業) 06.(Page57) Modify internal MIC AMP gain setting, change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC)the same with TYPE1 board single end MIC) (Gain=9.2)
- (才) 07.(Page60) Modify Constant-Current SONY LOGO LED circuit for EC control soft start/down (function up)issue
(1).Del back up Test Pad TP864
(2).Add R1978 (0 ohm) link EC pin176 and INV_ENABLE
- (業) 08.(Page74) Modify Constant-Current SONY LOGO LED circuit
A. for U138 cost issue
1.Back up:U138(MAX1916E2T),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
2.Remove back up solution U139(GMT,G5920TB1UF),C1660(0.1u)
3.Add new Constant-Current circuit (OP + MOS)
51K ohm: R1972 ,
1.2K ohm: R1973 ,
1k ohm:R1974
10 ohm: R1975
(NC)0 ohm: R1976(for back up U138 MAX1916)
0.1uF,16V: C1679
(NC)22uF,6.3V: C1680
OP LM558 AMP : U139
N-MOS 2N7002: Q158
N-MOS DTA114YUA:Q159
P-MOS DTC144EUA:Q160
B. for EC control soft start/down (function up)issue
1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
4.Add R1977 between +5VRUN to U126 pin5(VCC)
5.Add R1980 between Logo_led_en_ec to U126 pin2
- (業) 09.(Page 42) Delete SATA HDD Fuse backup circuit
(1)Remove F7,F8,F19,F20 Pad
(2)Remove GP17-GP18 open gap
- (才) 10. (Page 62) MOR fan circuit modify to backup
(NC)U118 (NC)R1893
(NC)R1624 (NC)C1473
(NC)R1894 (NC)R1895

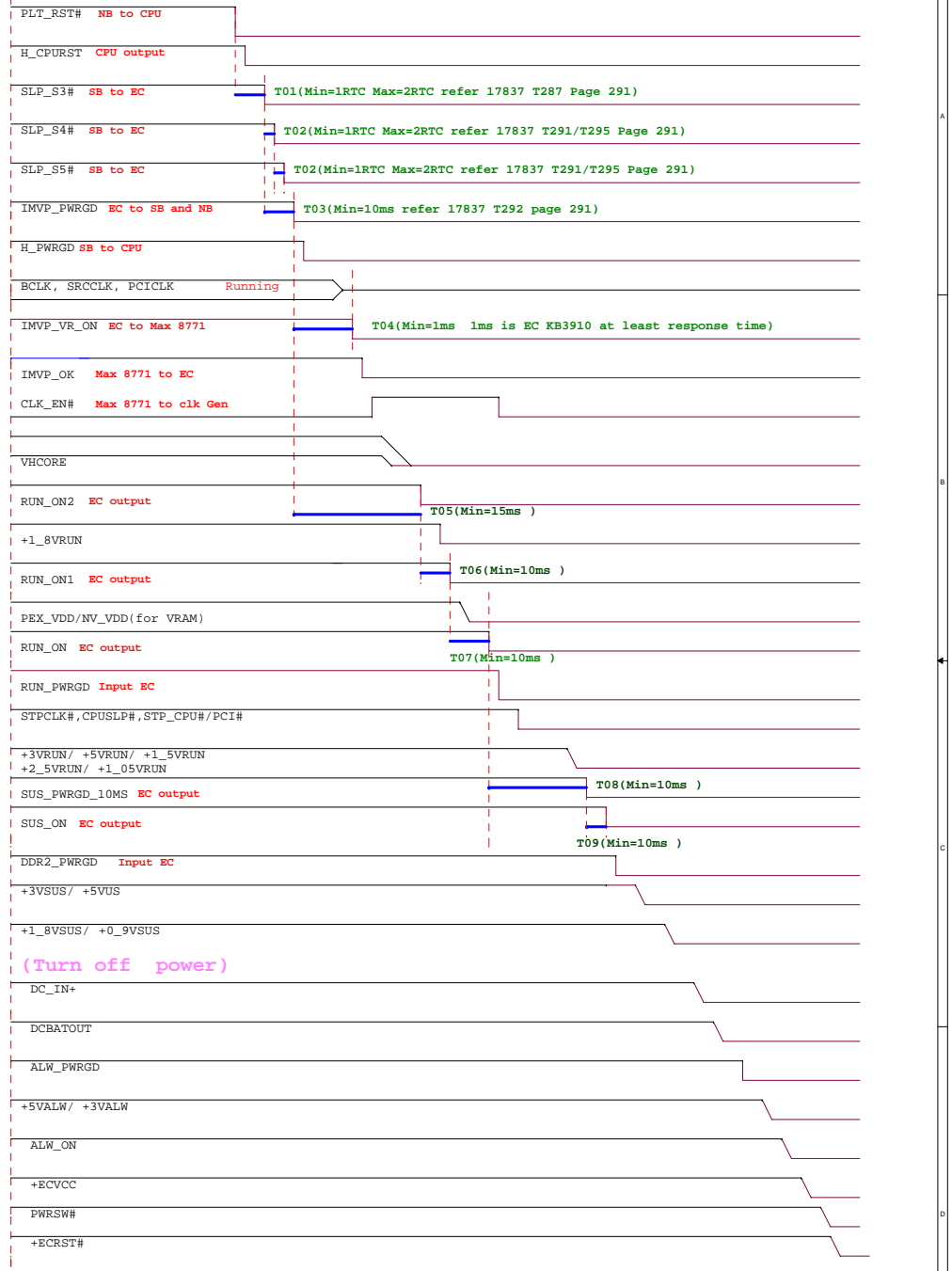
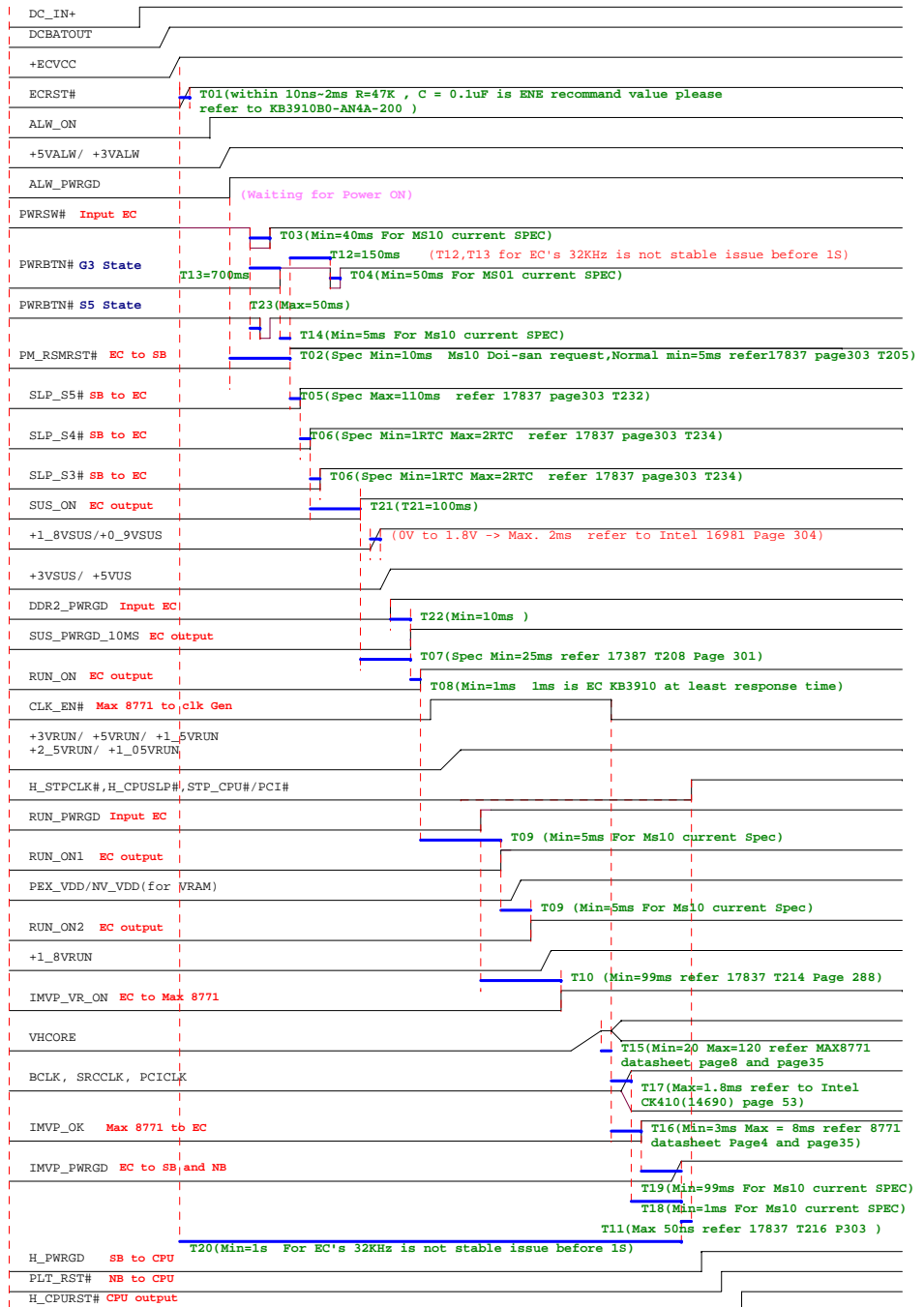
MS21 PVT to MS21 MP Change History

- (業) 01.(Page74) MS21 not support soft light / soft dark. So cancel INV_ENABLE control LOGO LED.
R1980 change from stuff to NC
R1981 change from NC to stuff
- (才) 02.(Page60) MS21 not support soft light / soft dark. So cancel INV_ENABLE control LOGO LED.
R1978 Change from stuff to NC
- (業) 03.(Page57) Change C1676 from stuff to NC for MOR suggestion Cost down request.
- (業) 04.(Page66) At MS21 PCN1 used FOXCONN connector, Change PCN1 Vendor from molex to NWING
- (業) 05.(Page29) Change D60,D61,D81 Value from NV to Normal
- (業) 06.(Page20) Change Y2 Value from Normal to NV

MS21 Power On Sequence Block Diagram



Power On/Off Sequerence Specification



T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	
within 10ns-2ms	Min. 10ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCCLK	Min. 25ms	Min. 1ms	Min. 10ms	Min. 99ms	Max. 50ms	
T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23
Min. 150ms	Min. 700ms	Min. 5ms	Min. : 20us Max : 120us	Min : 3ms Max : 8ms	Max 1.8ms	Min. 1ms	Min. 99ms	Min. 1s	100ms	Min. 10ms	Max 50ms

T01	T02	T03	T04	T05	T06	T07	T08	T09
1 - 2 RTCCCLK	1 RTCCLK	Min. 10ms	Min. 1ms	Min. 15ms	Min. 10ms	Min. 10ms	Min. 10ms	Min. 10ms

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

File MS21 Power On Sequence Timing specification

Doc No MS21-1-01 MainBoard (MBX-164) TYPE2 Rev 1.1

Date: Thursday, August 10, 2006 78 of 78

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