

2010.04.07 MV Schematic

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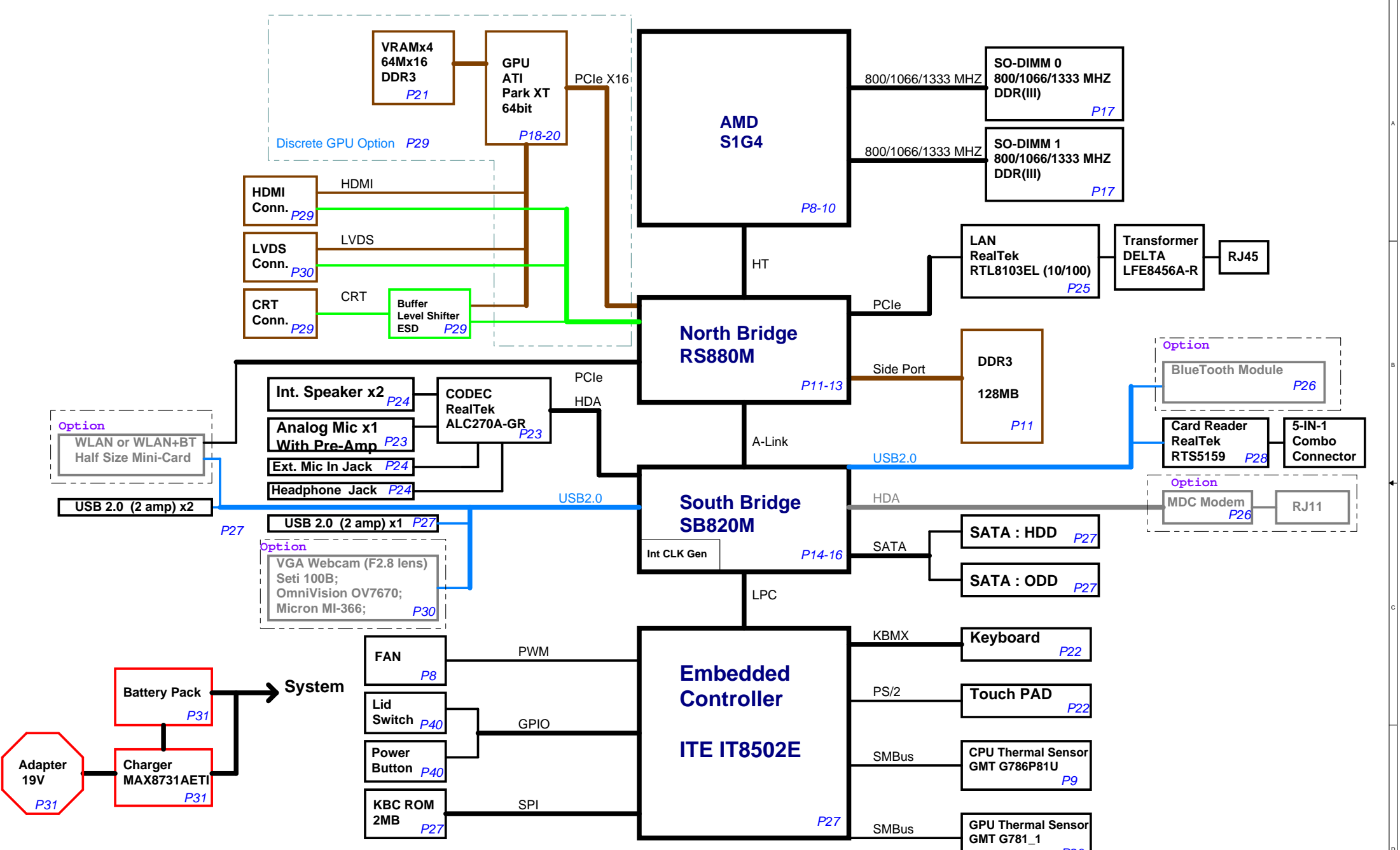
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 P34 : +V1.1S TPS51117 & VDDR
 P35 : +V1.8S RT8253ALGS & VDDA
 P36 : PWR_Others power plane
 P37 : +VCCNB & 1.5VDDR3 +0_75V
 P38 : ATVDD TPS51217 & +VPCIE
 P39 : Stitch CAP

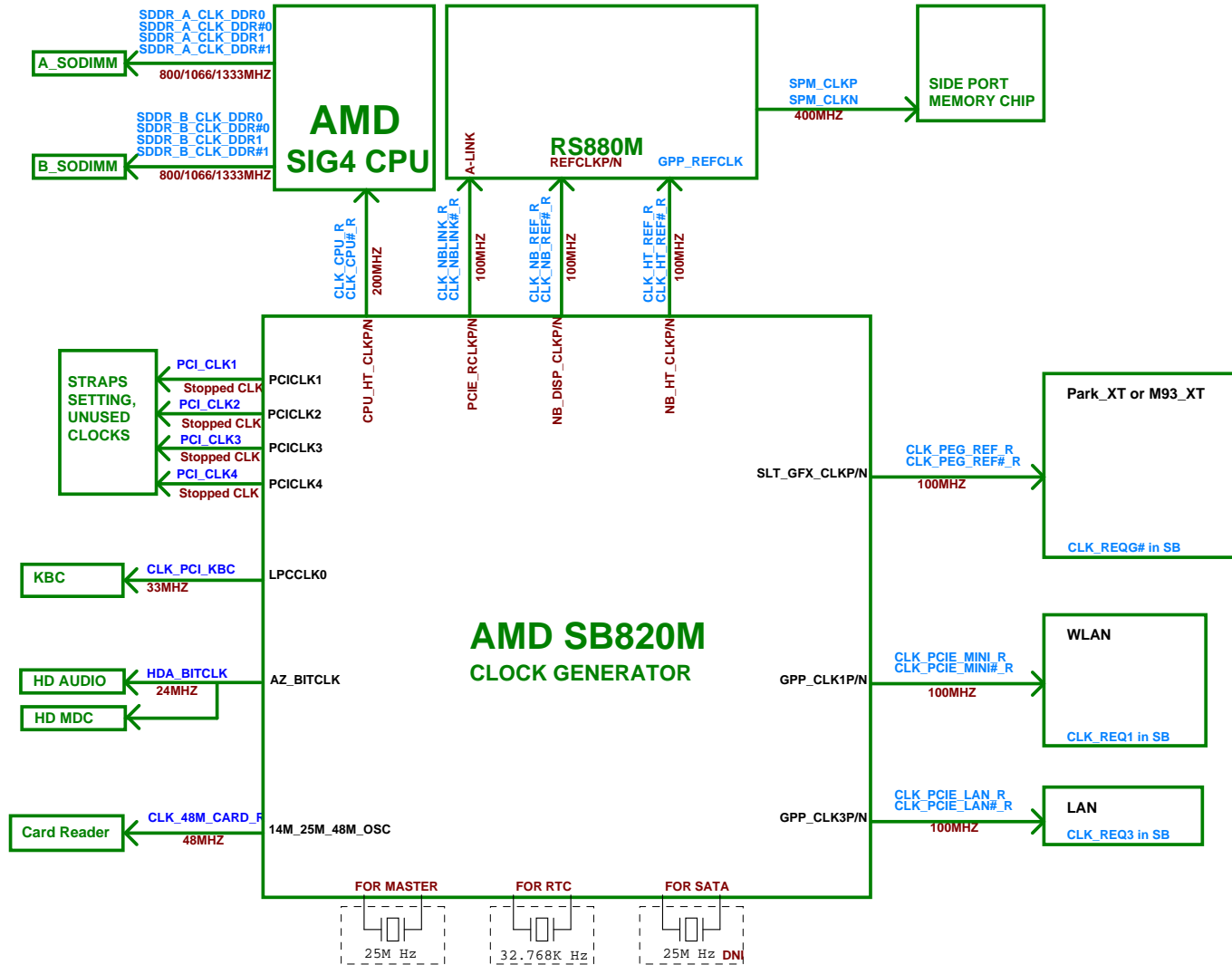
Daughter Board

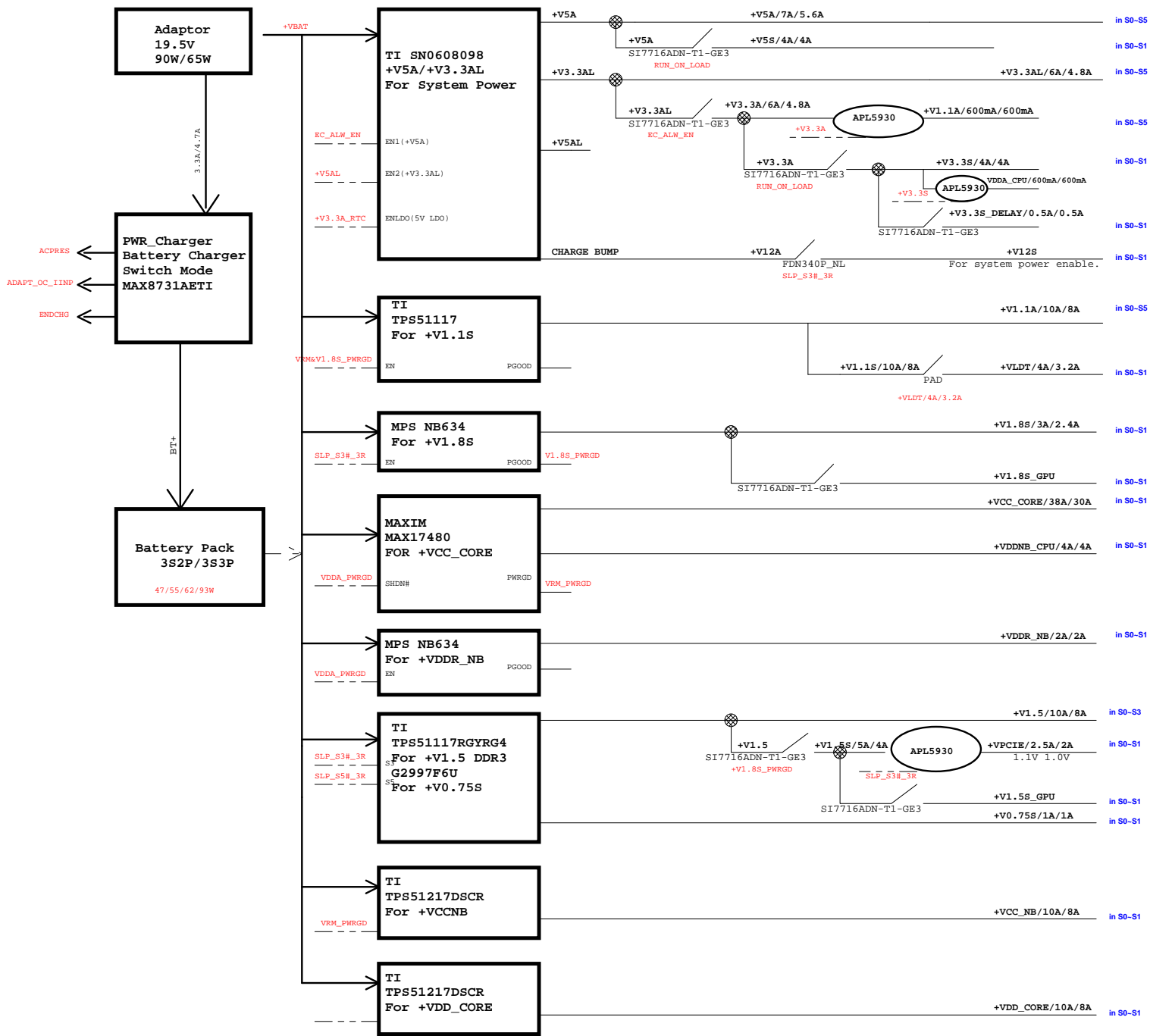
P40 -- Power Board / USB Board / SW Board

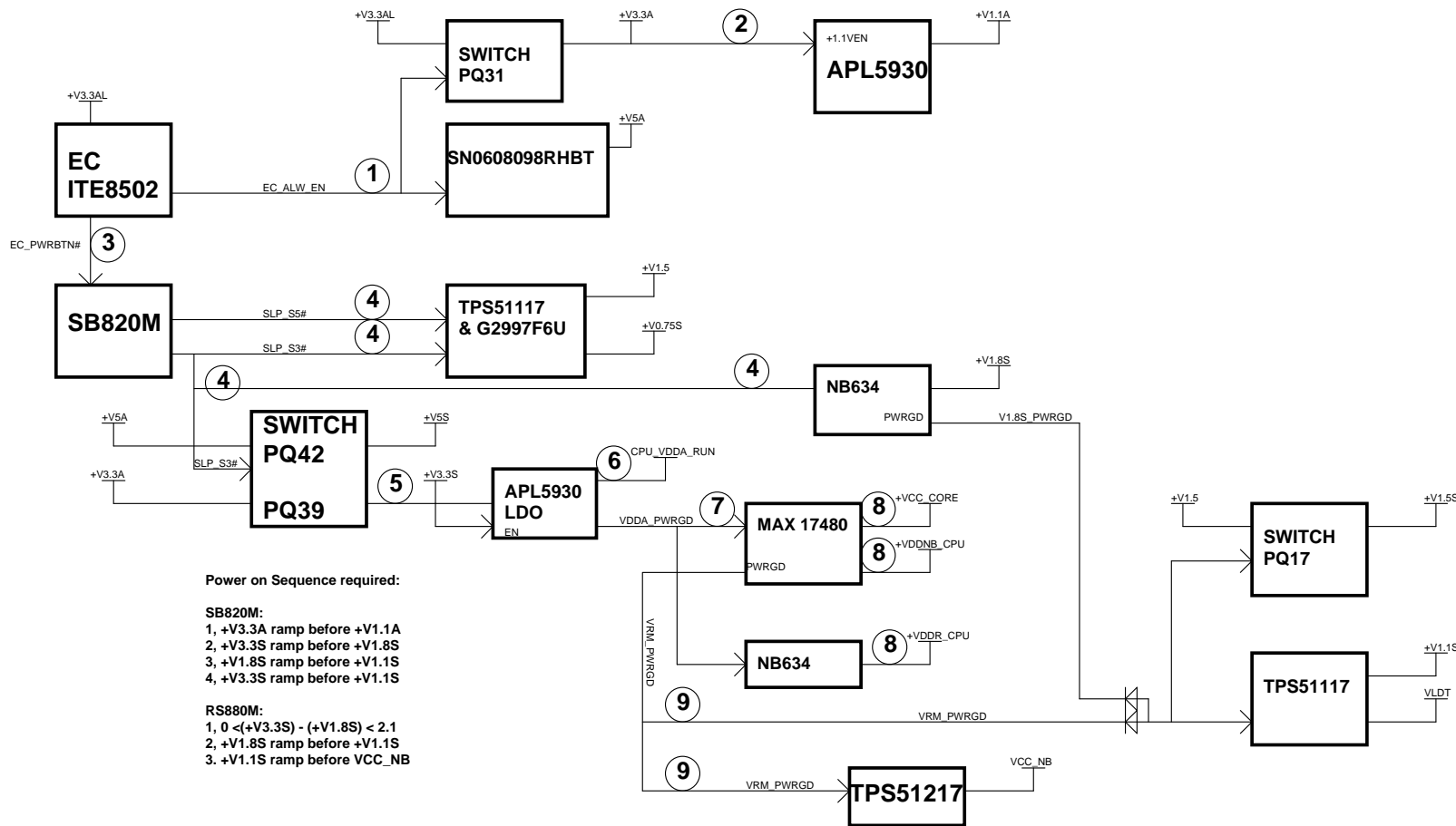
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 Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D phone: +886-2-2799-6111		
Title		
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Size	Document Number	Rev
Custom	Safina	MV
Page Modified: Wednesday, April 07, 2010 12:11:12 (UTC+8) Sheet 1 of 39		



INTERNAL CLOCK MODE







Power on Sequence required:

SB820M:

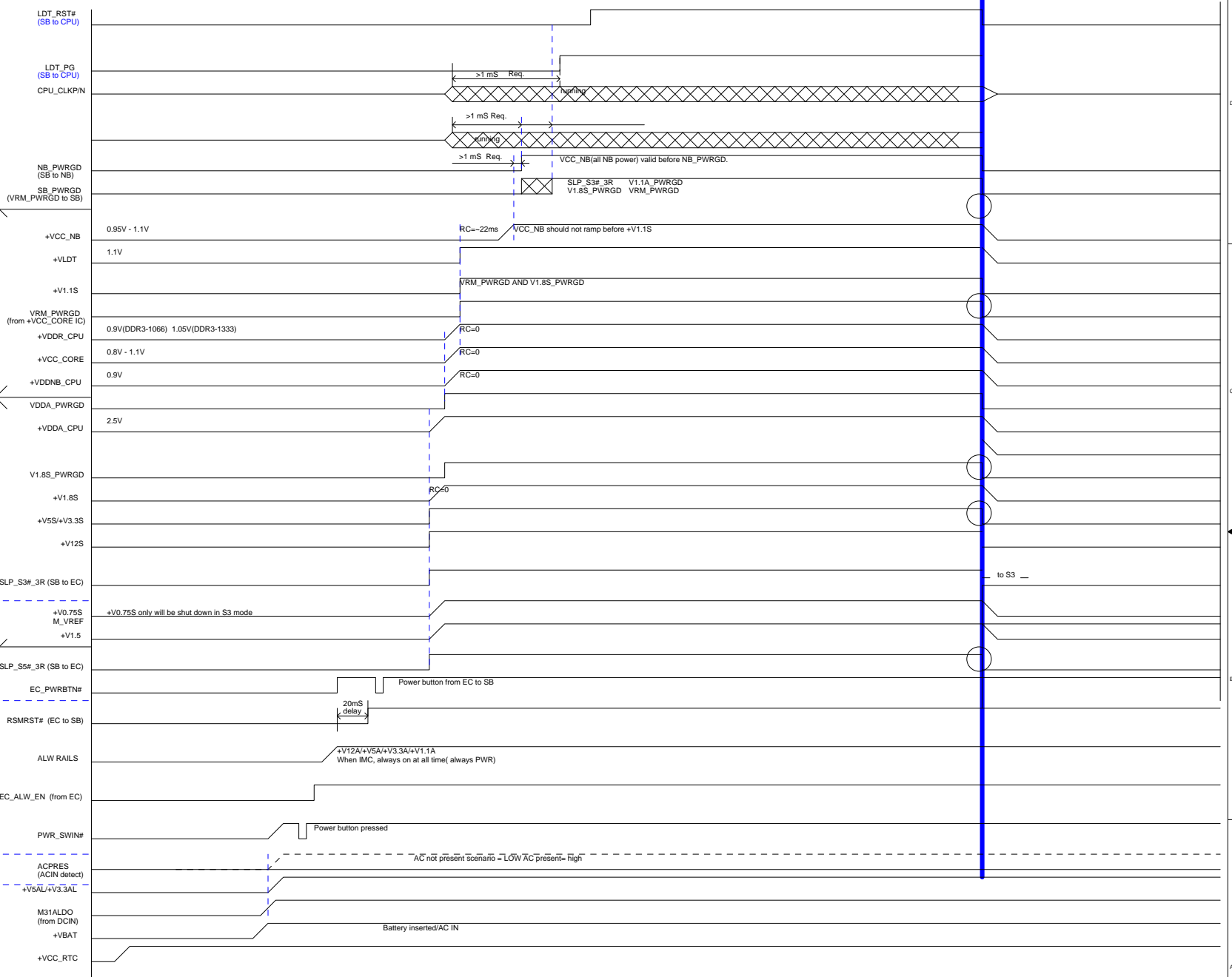
- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 4, +V3.3S ramp before +V1.1S

RS880M:

- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before VCC_NB

GROUP B

GROUP A



CPU MEM CTL & DDR3 SODIMM PWRS

CPU_THM/SB/SB_SCL1/2 SB_KB/SPI/LPC ROM PWRS

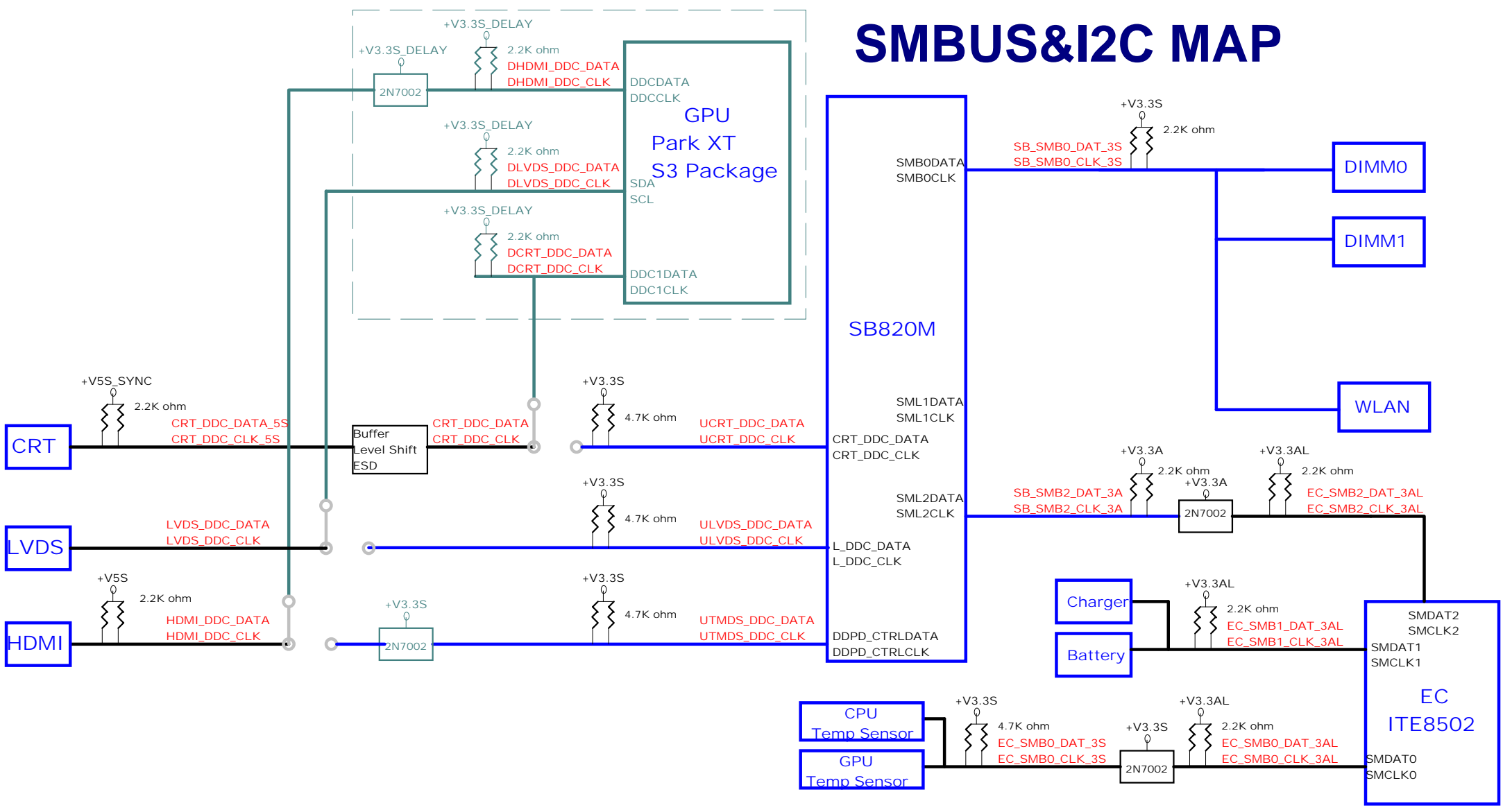
KBC is ready

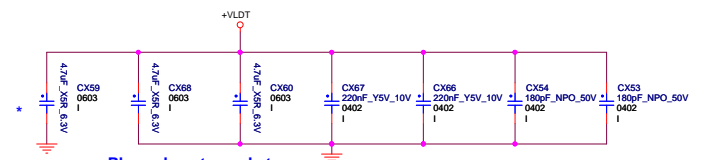
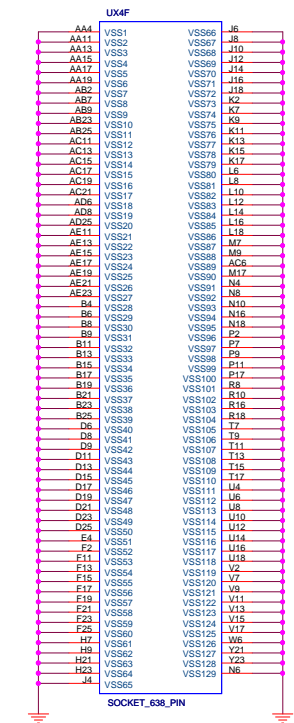
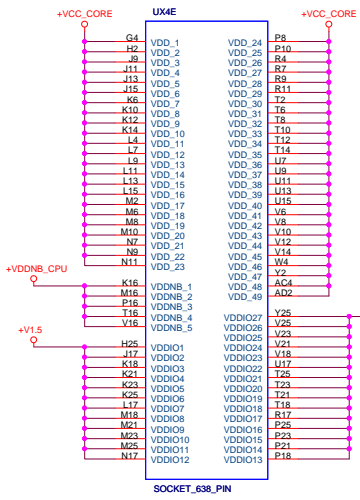
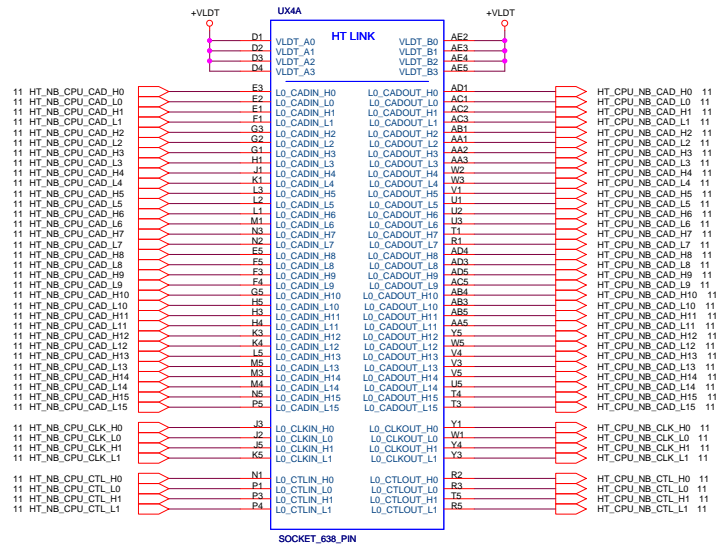
KBC is powered by +V3.3AL

- Power on Sequence required:**
- SB820:
 1. +V3.3A ramp before +V1.1A
 2. +V3.3S ramp before +V1.8S
 3. +V1.8S ramp before +V1.1S
 5. +V3.3A ramping down time > 300us
 6. 50uS <= All power rails except +V3.3A <= 40mS
 7. 100uS <= +V3.3A <= 40mS
 - RS880M:
 1. 0 <(+V3.3S) - (+V1.8S) < 2.1
 2. +V1.8S ramp before +V1.1S
 3. +V1.1S ramp before +VCC_NB

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Title: POWER SEQUENCY TIMING			
Size: Custom	Document Number: Safina	Rev: MV	
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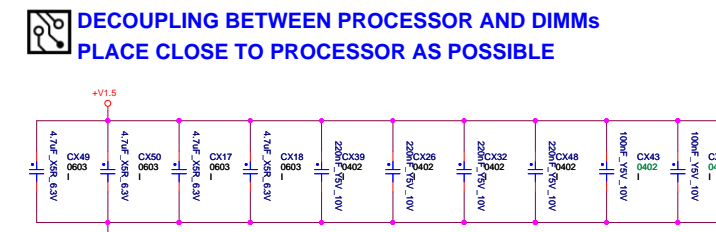
SMBUS&I2C MAP



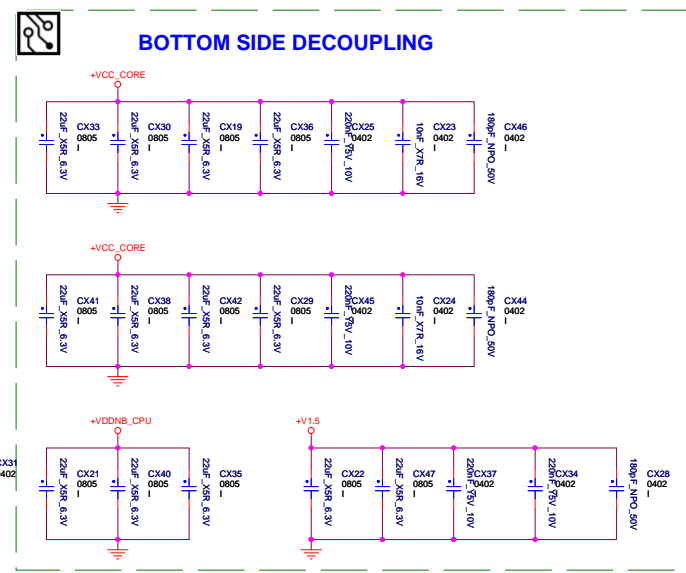


Place close to socket

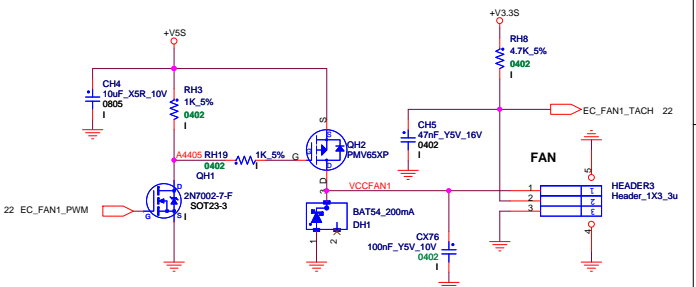
* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE



BOTTOM SIDE DECOUPLING

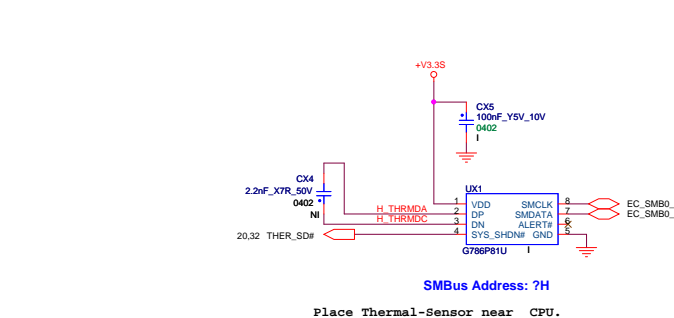
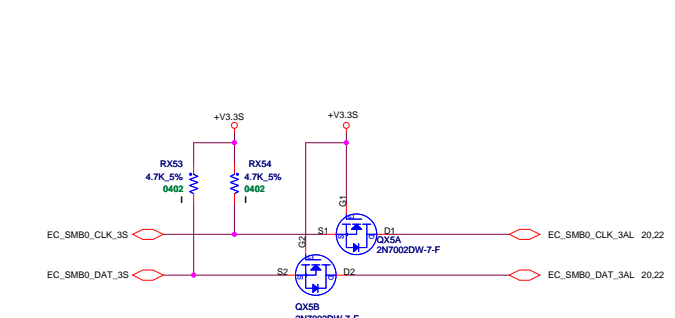
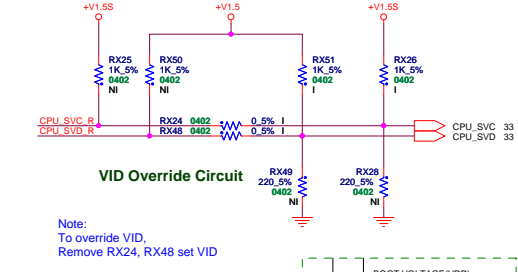
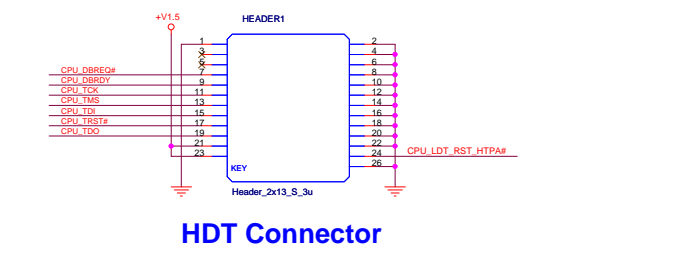
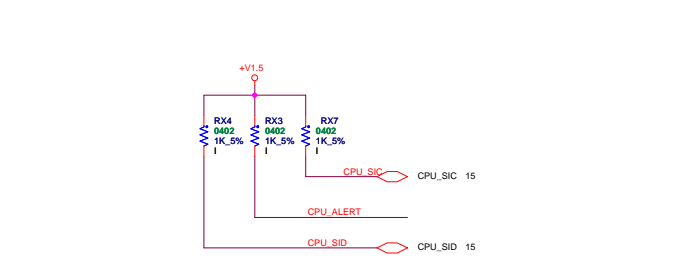
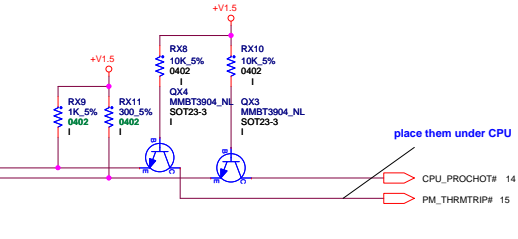
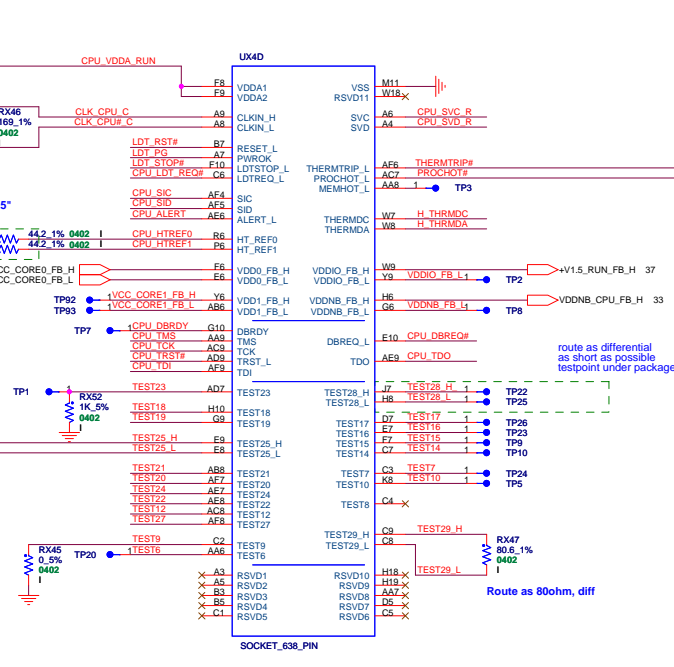
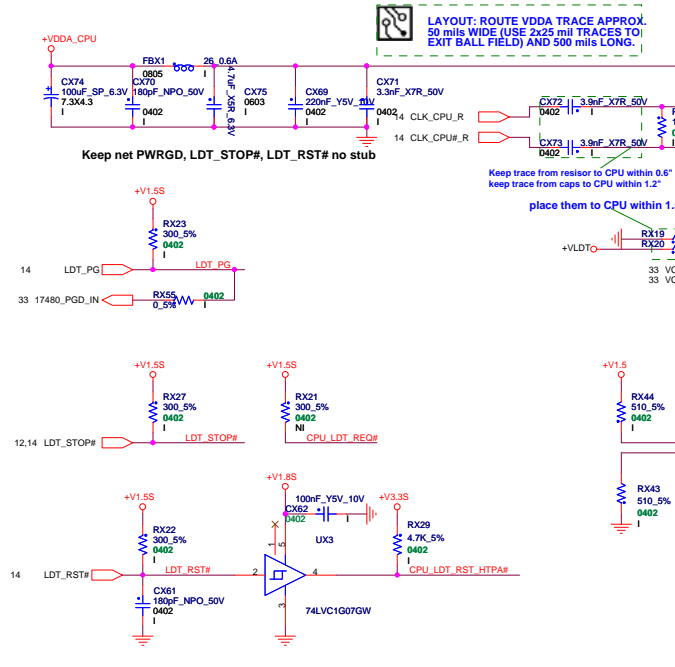


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Title: **S1G4 HT I/F & PWR**

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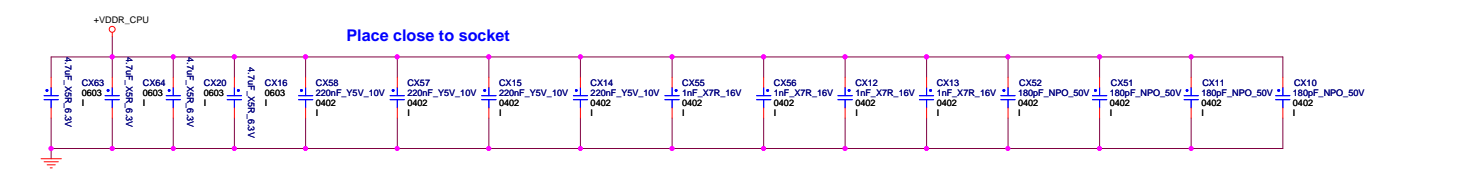
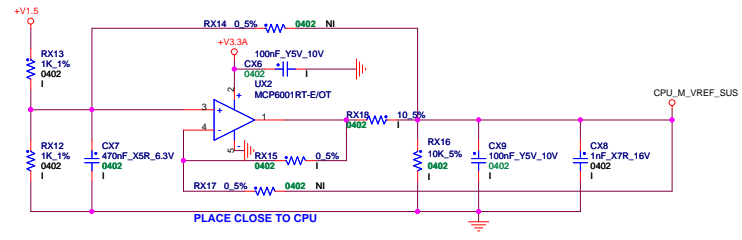
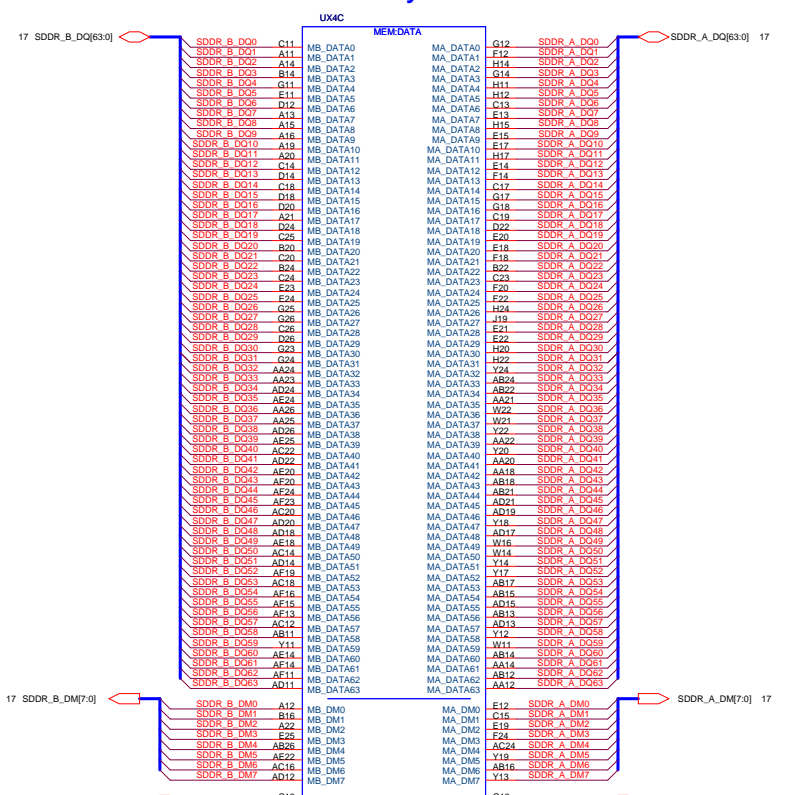
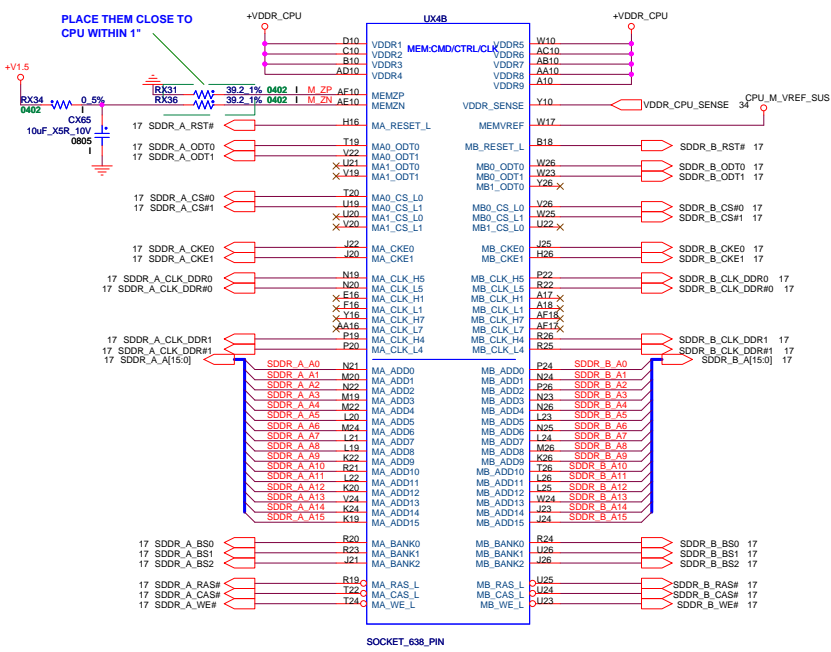


Note:
To override VID,
Remove RX24, RX48 set VID

SVC	SVD	BOOT VOLTAGE(VDD)	
		(CPU/VRM PROG +VCC/GND)	(CPU/VRM PROG +CPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

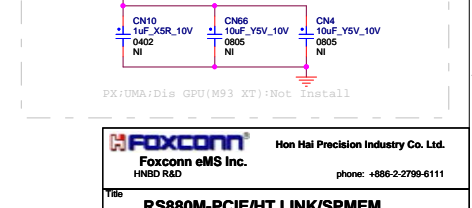
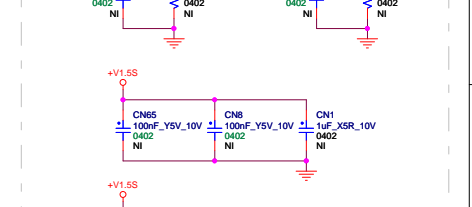
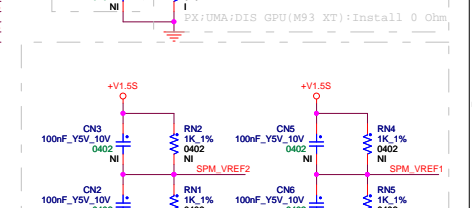
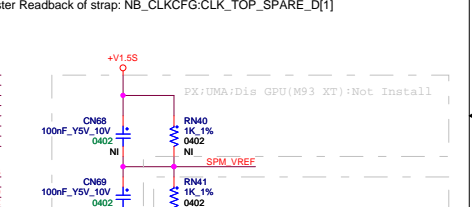
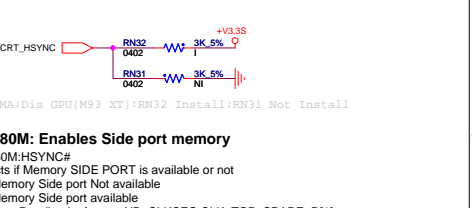
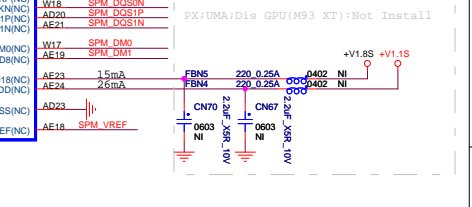
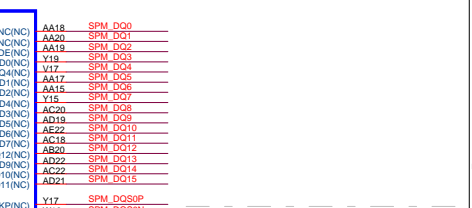
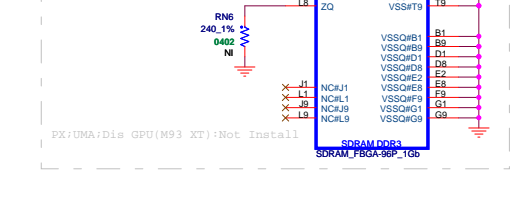
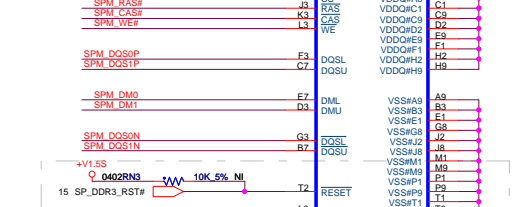
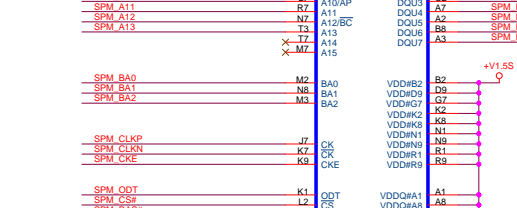
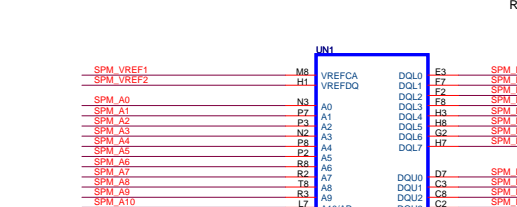
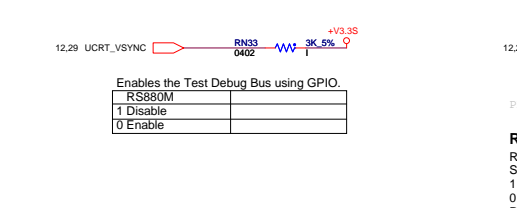
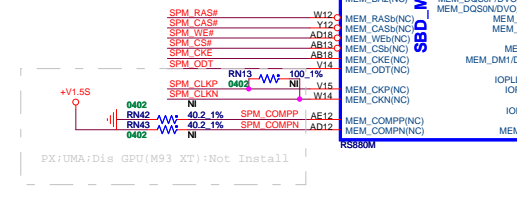
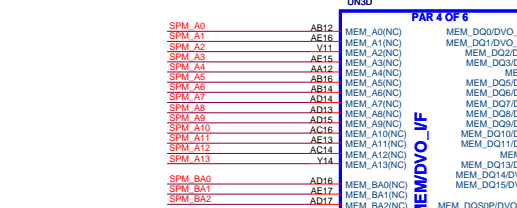
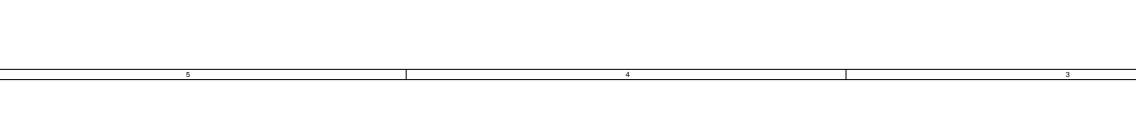
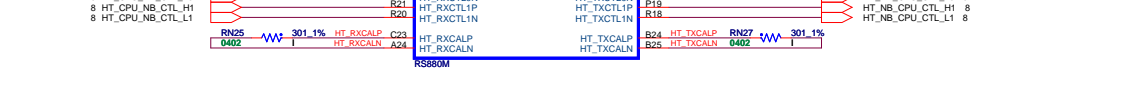
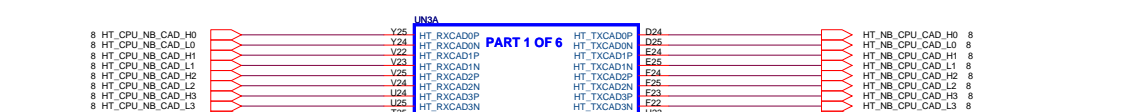
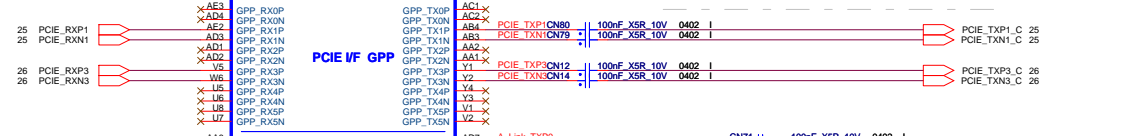
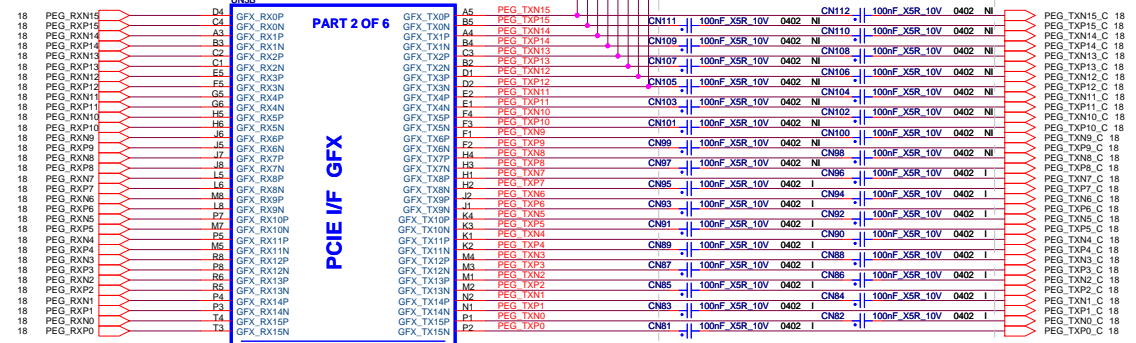
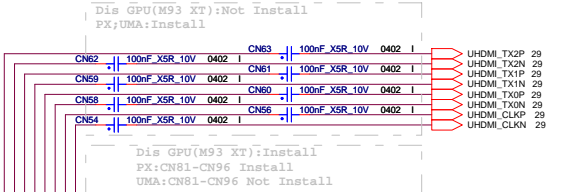
VID OVERRIDE TABLE (VDD)

Processor Memory Interface



Keep the impedance of PCIe lane to 85ohm +/-15% including the A-link

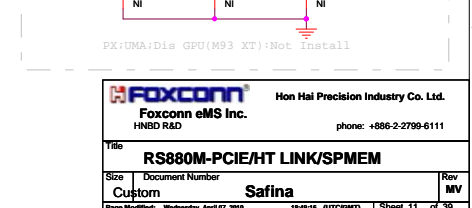
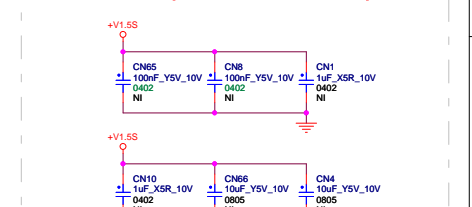
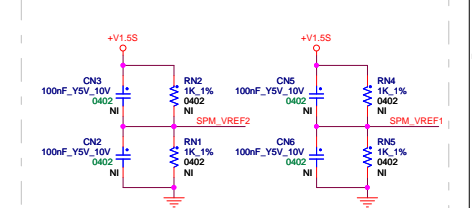
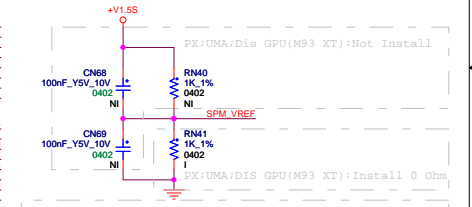
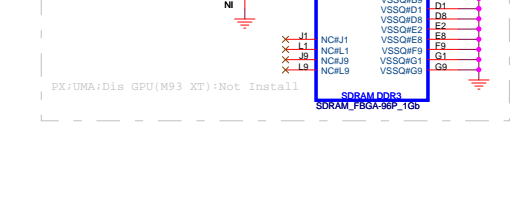
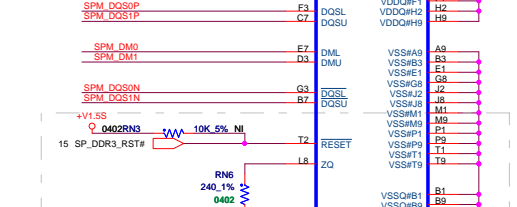
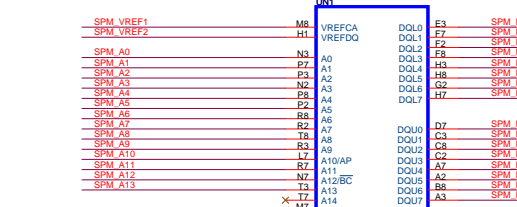
All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices



Enables the Test Debug Bus using GPIO.

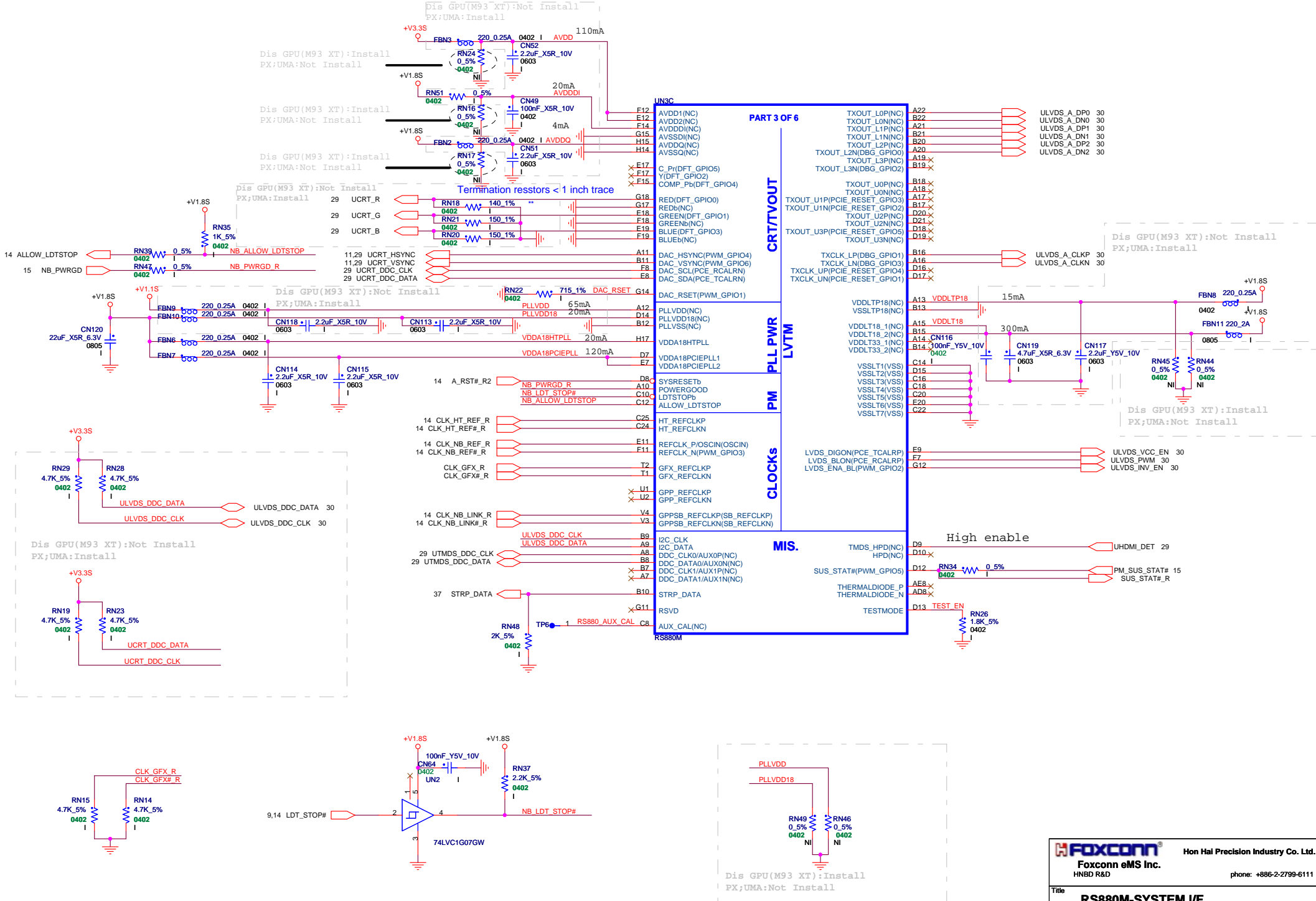
RS880M	
1	Disable
0	Enable

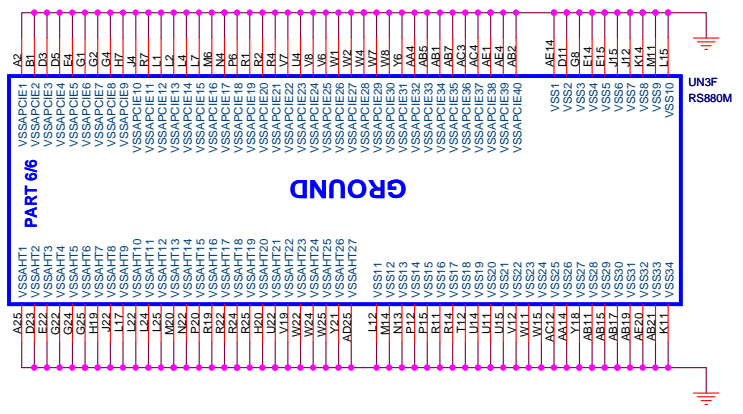
RS880M: Enables Side port memory
 RS880M:HSYNC#
 Selects if Memory Side PORT is available or not
 1 = Memory Side port Not available
 0 = Memory Side port available
 Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



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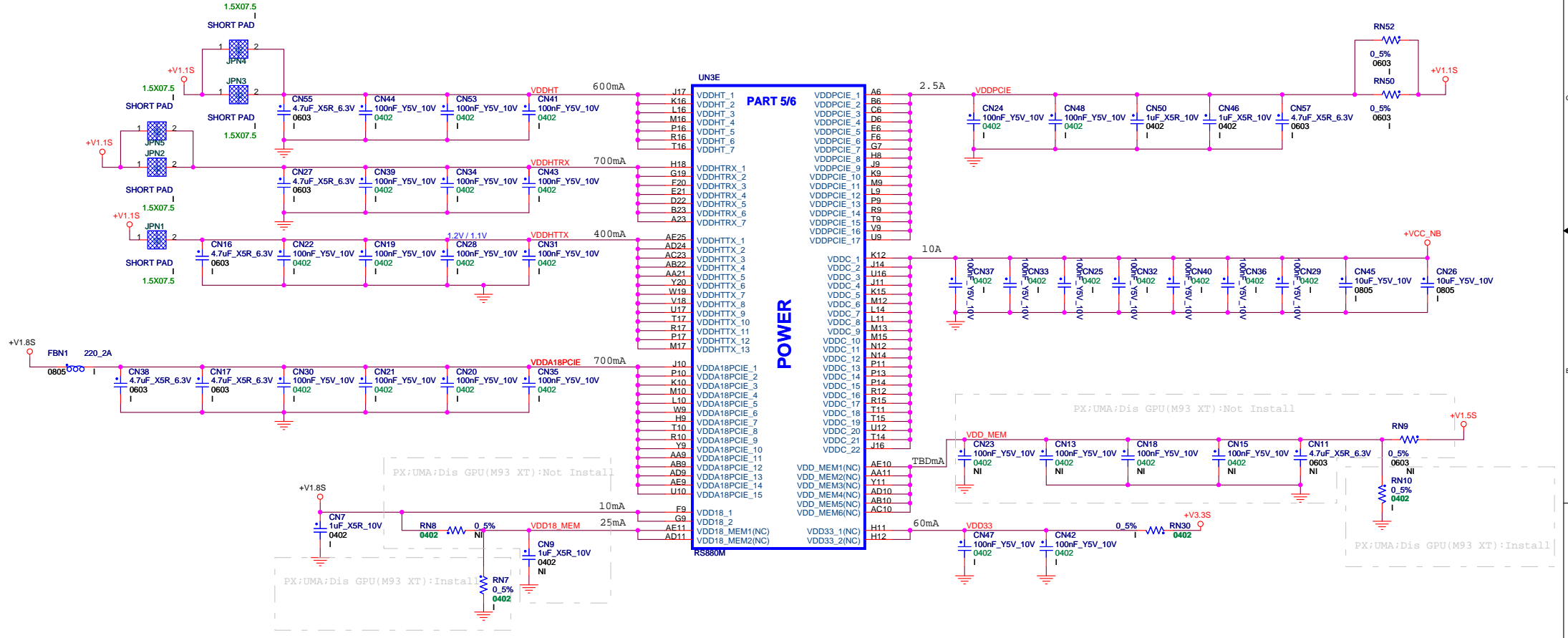
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RS880M-PCIE/HT LINK/SPMEM			
Size	Document Number	Rev	
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RS880M POWER TABLE

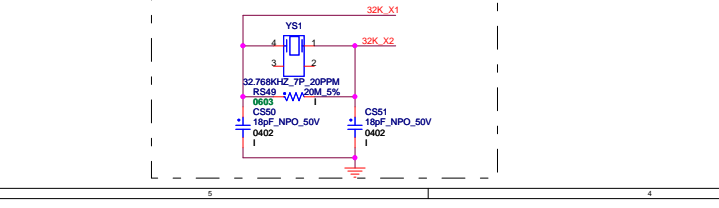
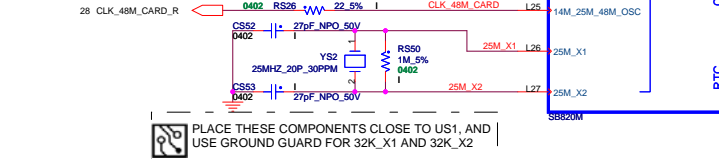
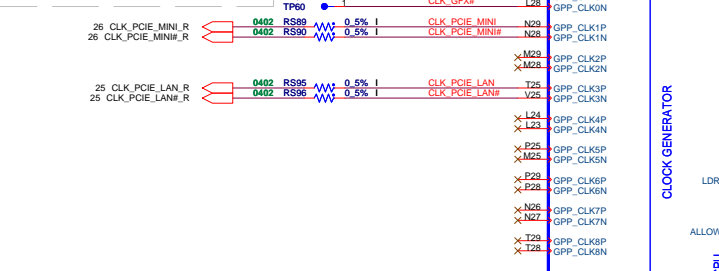
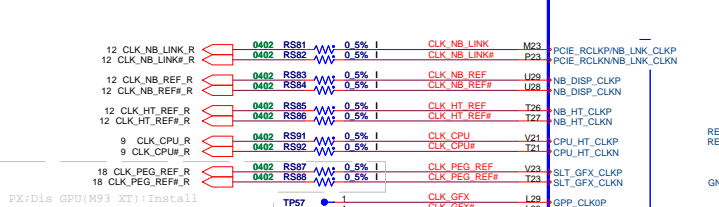
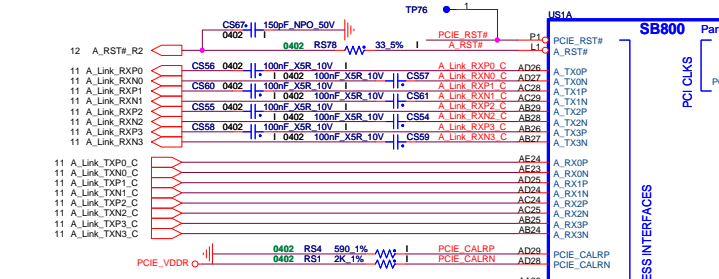
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



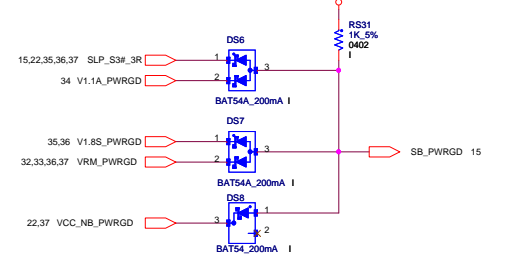
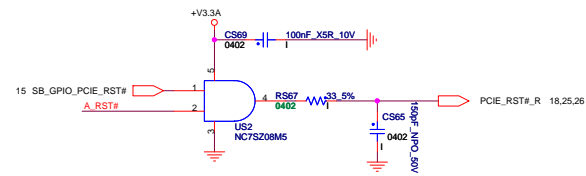
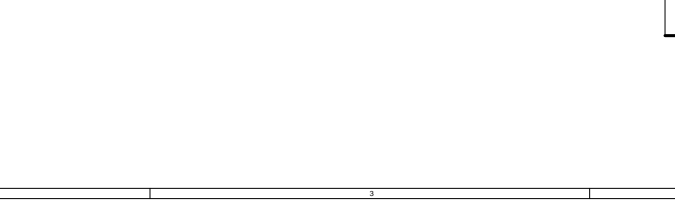
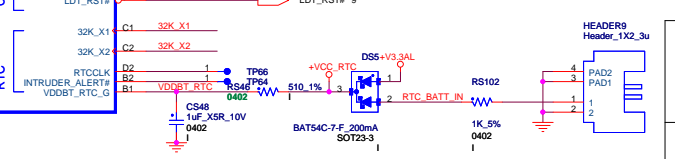
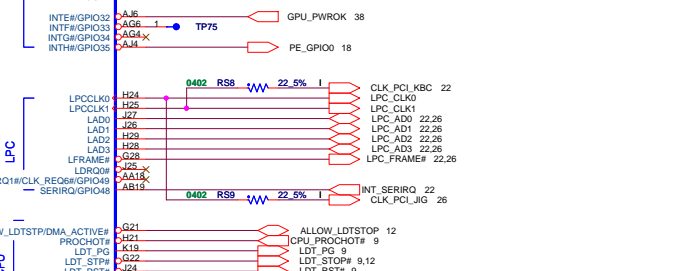
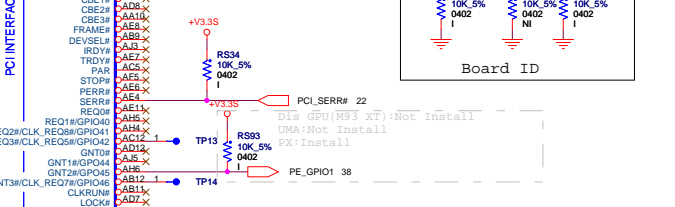
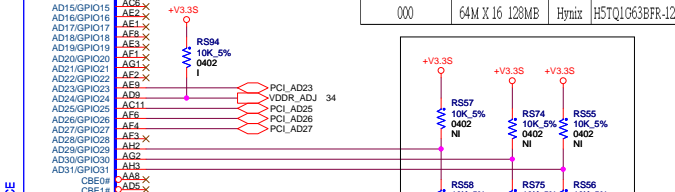
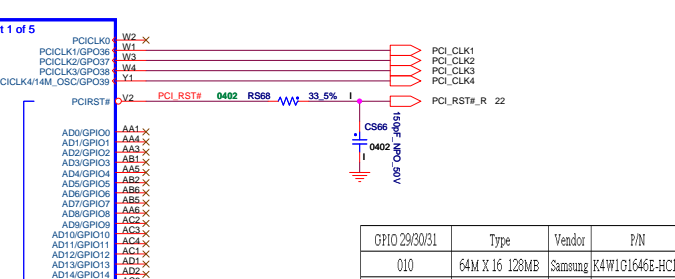

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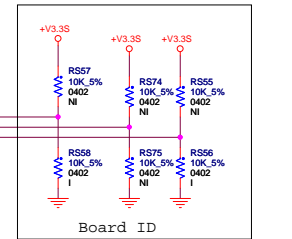
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO US1



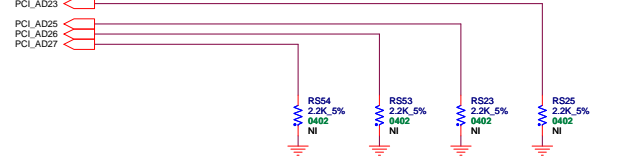
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO US1



GPIO 29/30/31	Type	Vendor	P/N
010	64M X 16 128MB	Samsung	K4W1G1646E-HC12
000	64M X 16 128MB	Hynix	H5TQ1G63BFR-12C

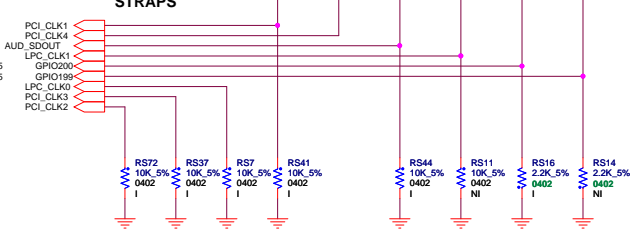


DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE PCI MEM BOOT

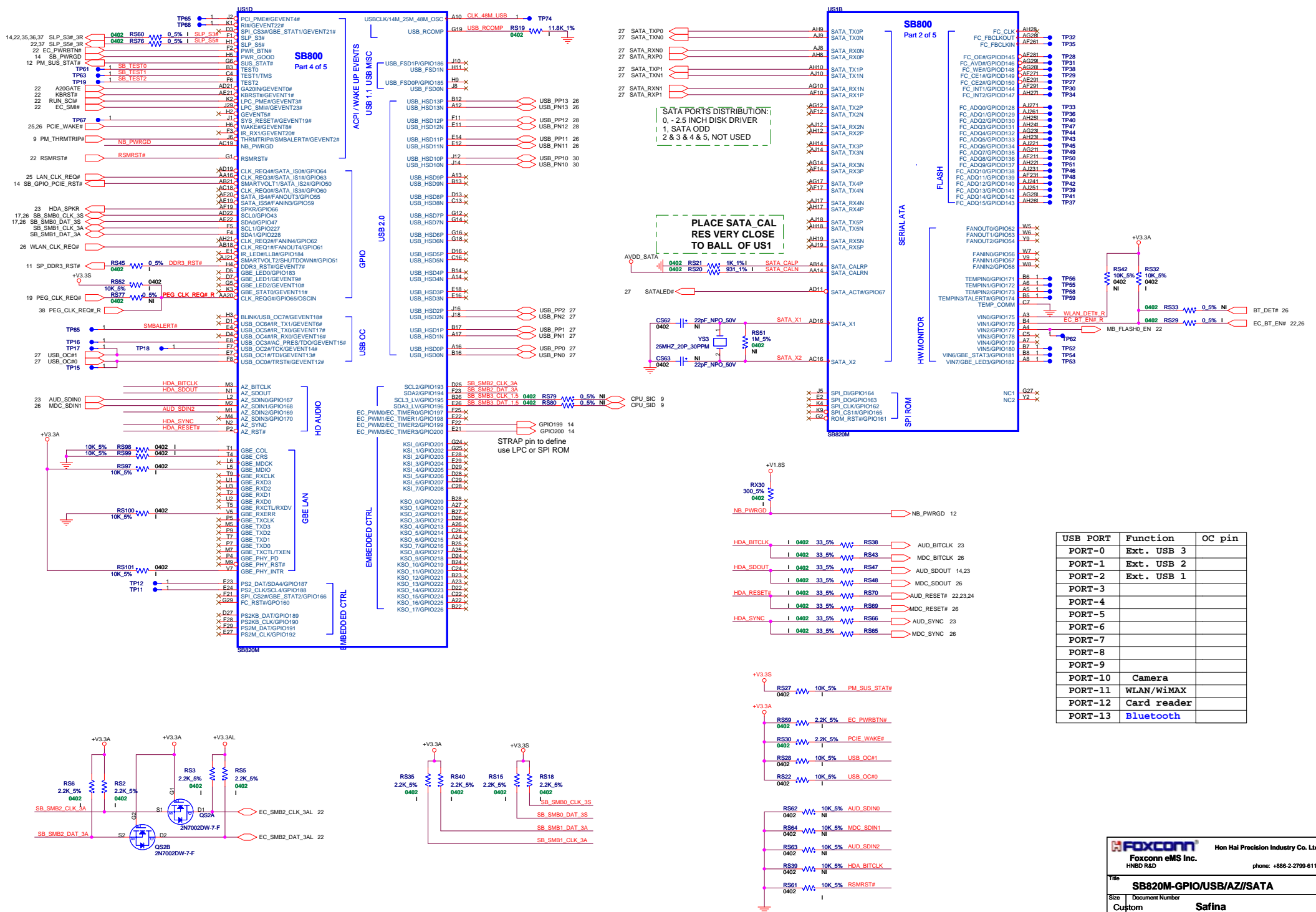
REQUIRED STRAPS



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		
PULL LOW	PERFORMANCE MODE	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

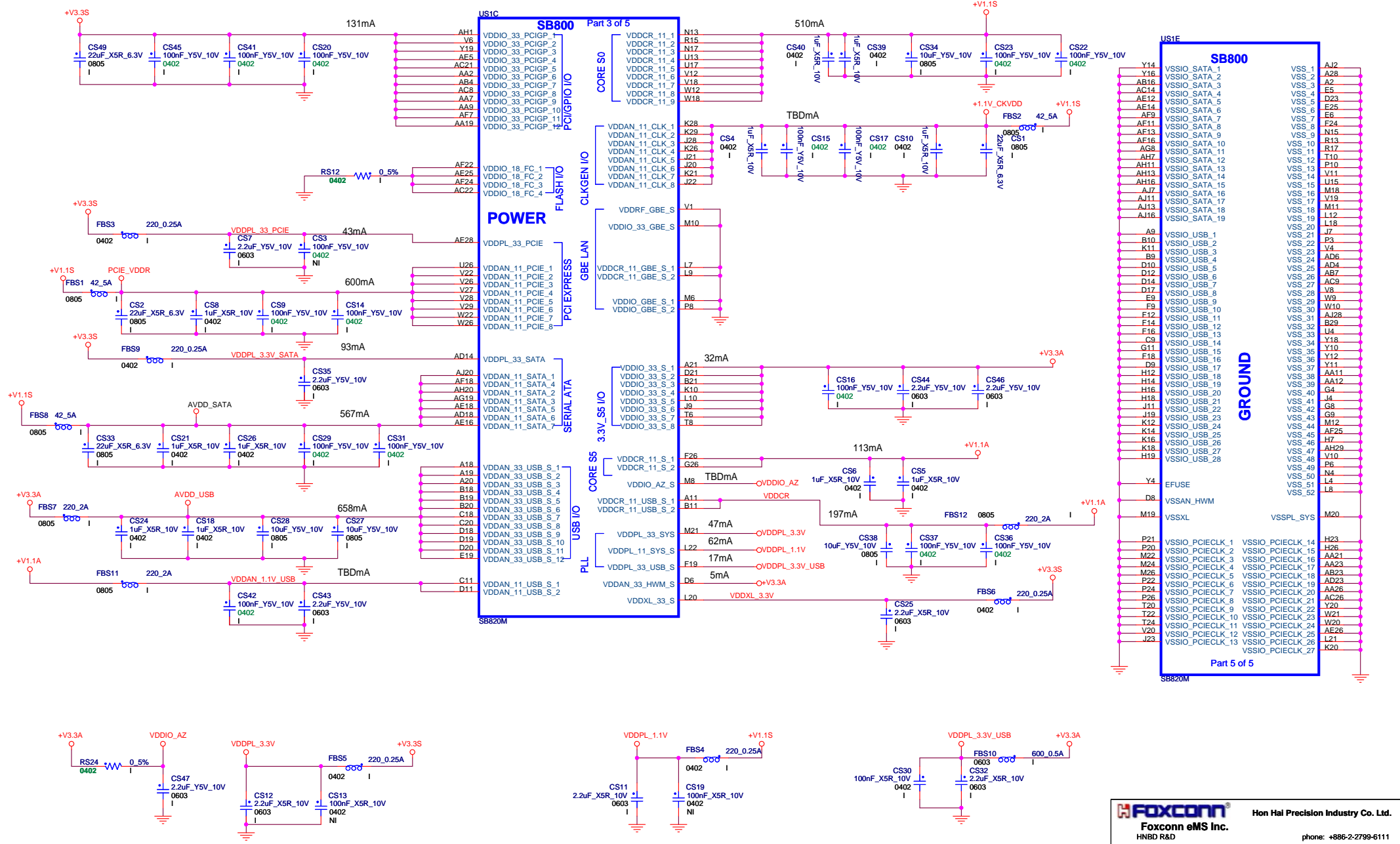
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Title		SB820M-PCIE/CPU/LPC/STRAP	
Size	Document Number	Rev	Rev
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Page Modified: Wednesday, April 27, 2011		184818 (UTC/GMT) Sheet 14 of 39	





PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

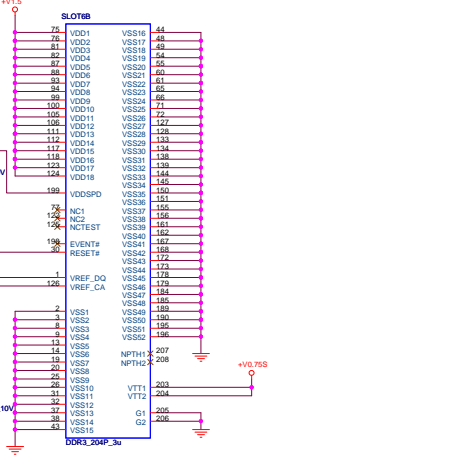
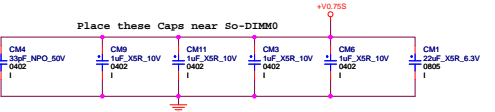
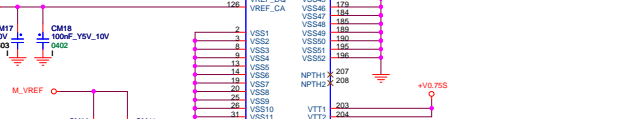
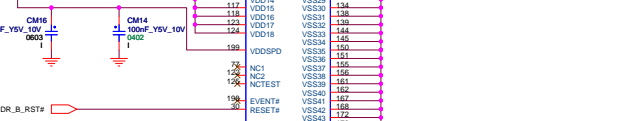
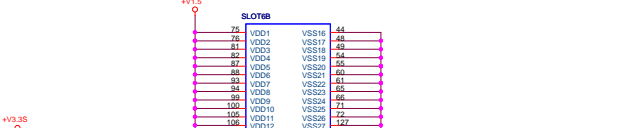
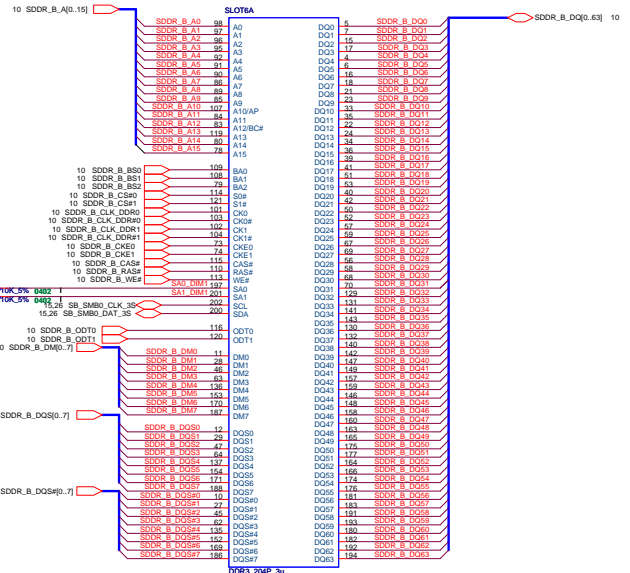
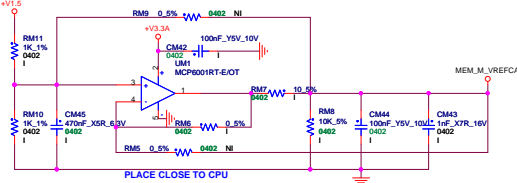
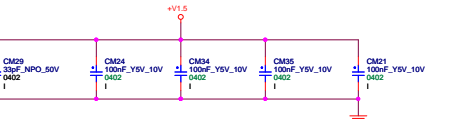
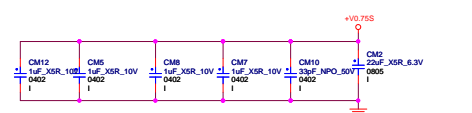
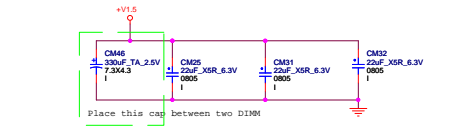


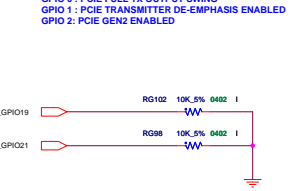
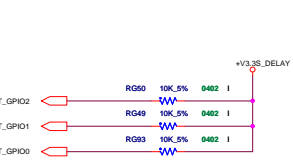
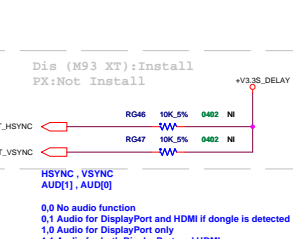
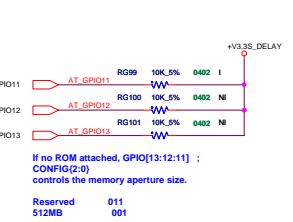
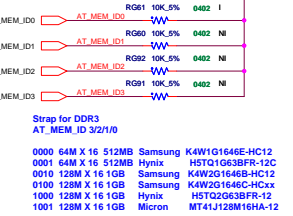
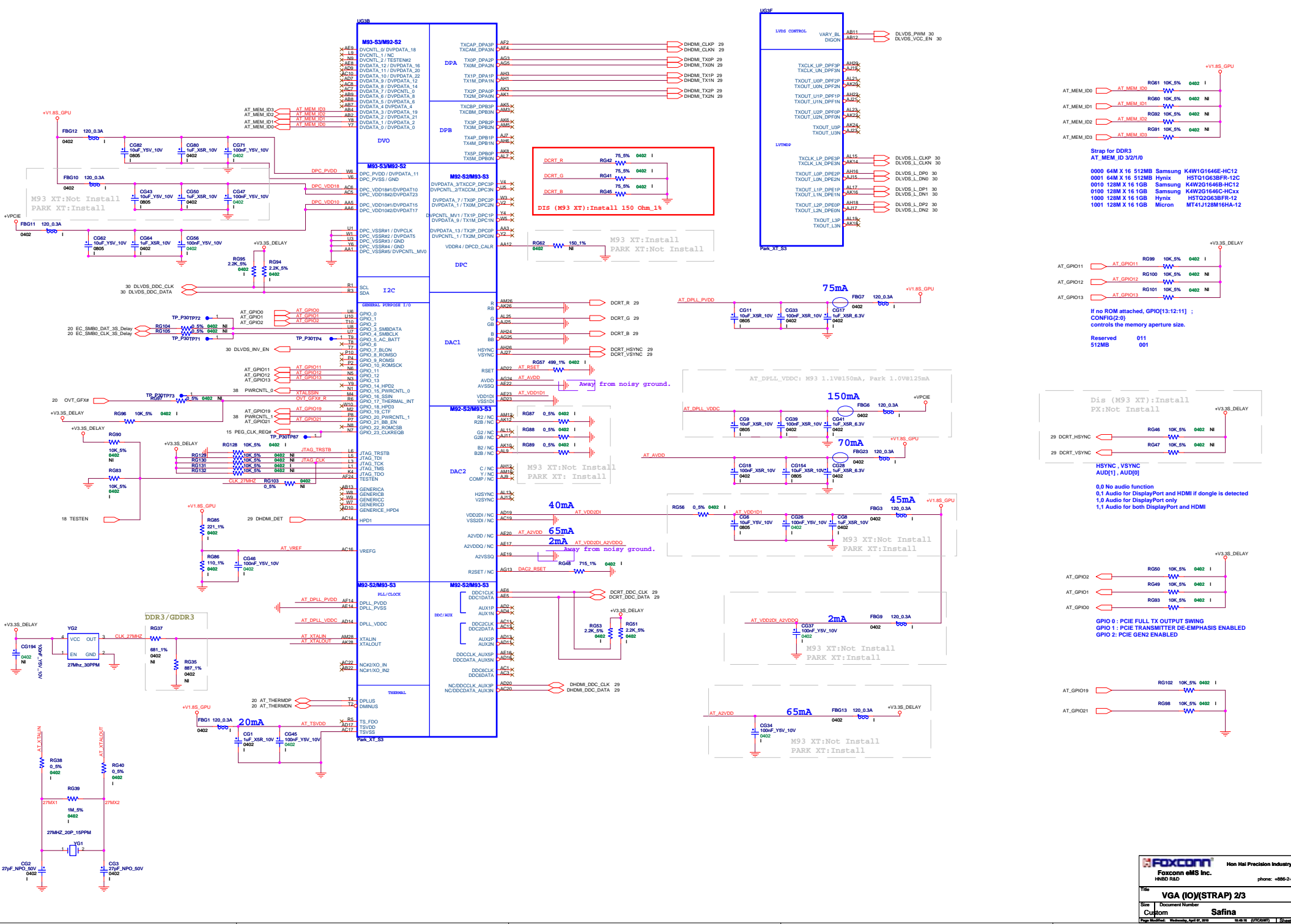
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 Foxconn eMS Inc. HNBDR R&D phone: +886-2-2799-6111

Title SB820-POWER & DECOUPLING		
Size	Document Number	Rev
Custom	Safina	MV
Page Modified: Wednesday, April 07, 2010 18:49:17 (UTC+0800)		Sheet 16 of 39

SMBus Address: A0H(WJA1H(R))

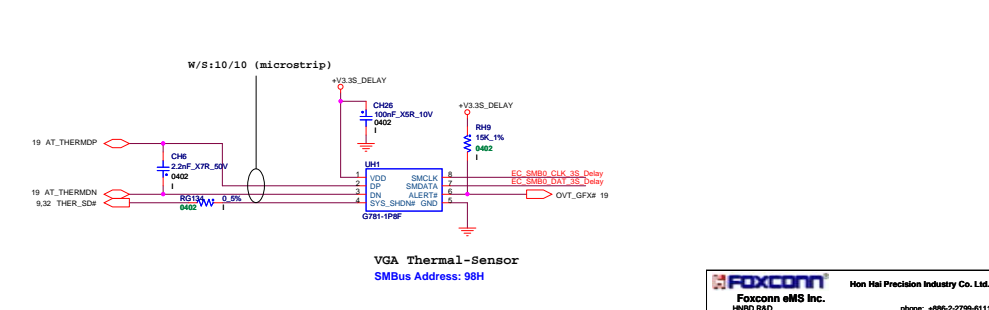
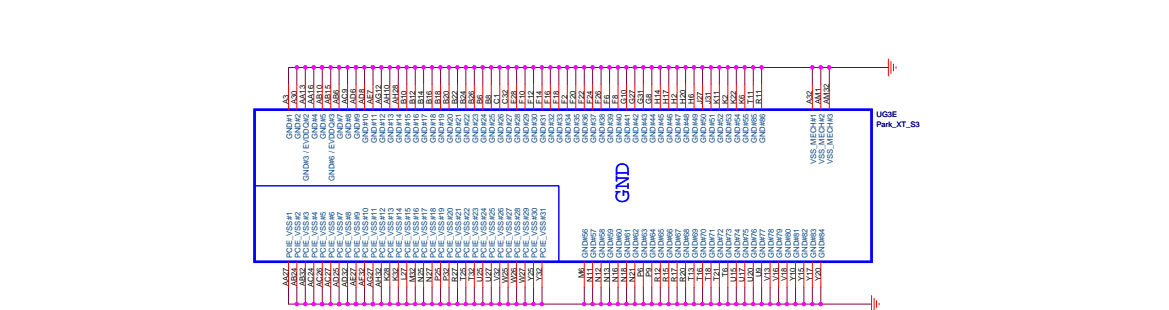
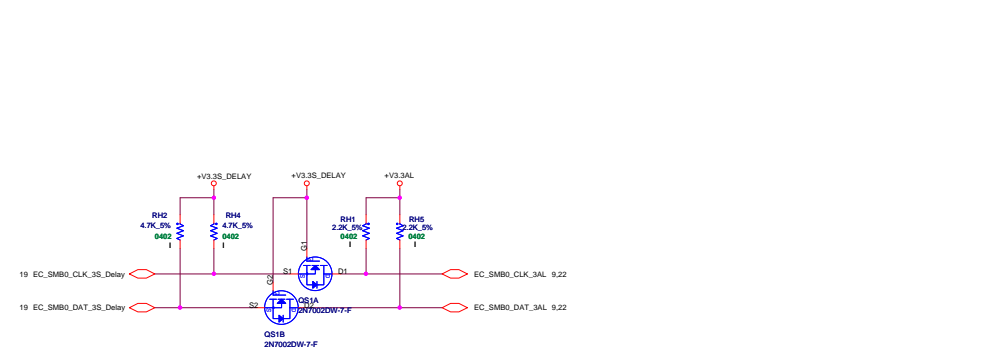
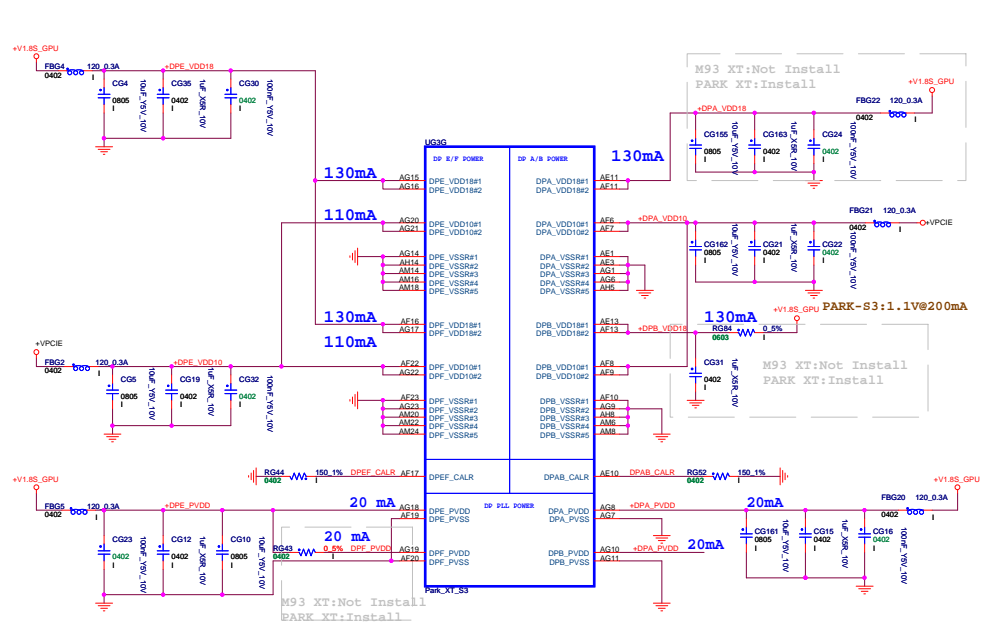
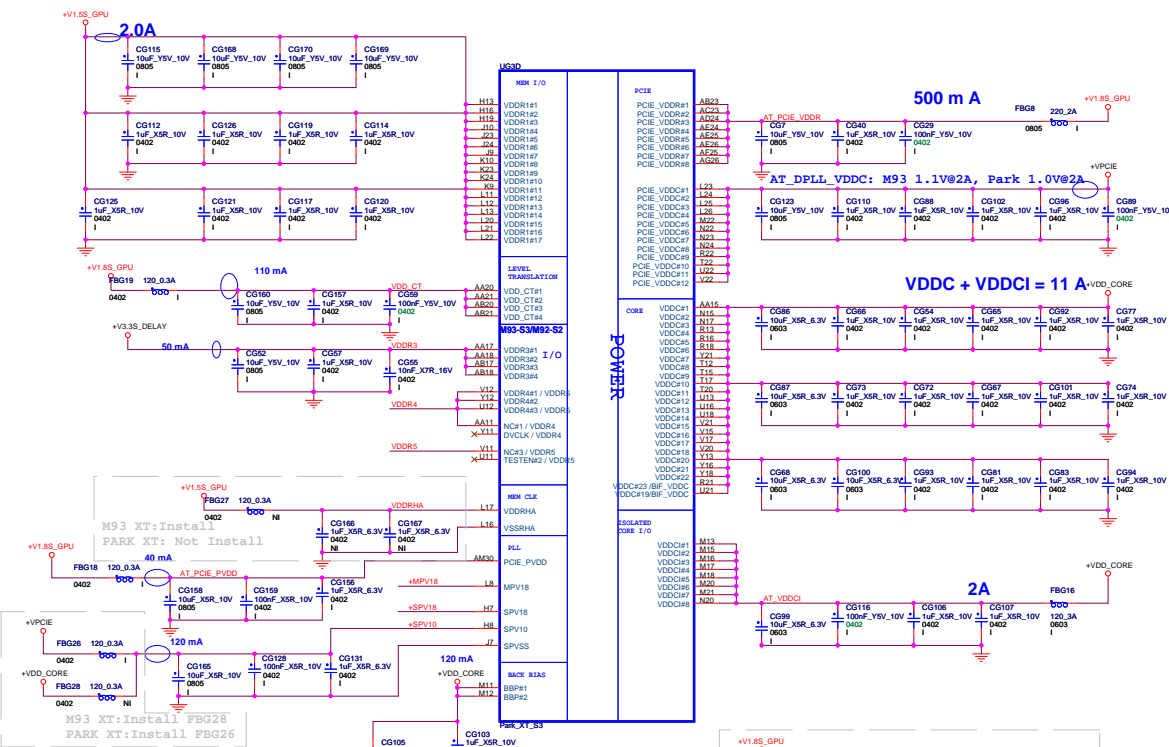
RM1 10K 5% 0402
RM1 10K 5% 0402
RM2 10K 5% 0402
RM2 10K 5% 0402
RM3 10K 5% 0402
RM3 10K 5% 0402





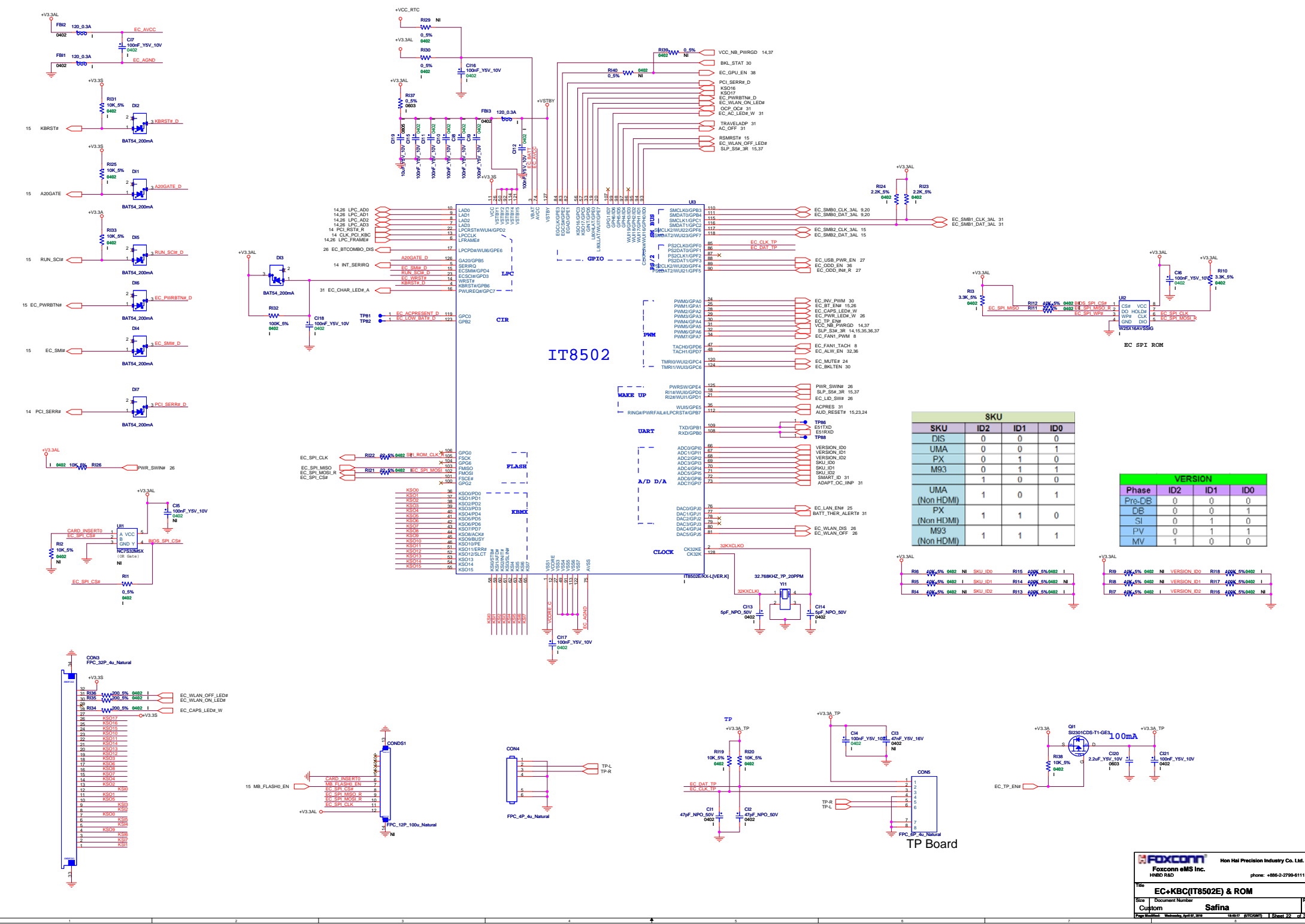
If no ROM attached, GPIO[13:12:11] ;
 CONFIG[0] controls the memory aperture size.
 Reserved 011
 512MB 001

0000 64M X 16 512MB Samsung K4W1G1646E-HC12
 0001 64M X 16 512MB Hynix H5TQ1G638FR-12C
 0010 128M X 16 1GB Samsung K4W2G1646E-HC12
 0100 128M X 16 1GB Samsung K4W2G1646C-HCxx
 1000 128M X 16 1GB Hynix H5TQ2G638FR-12
 1001 128M X 16 1GB Micron MT41J128M16HA-12

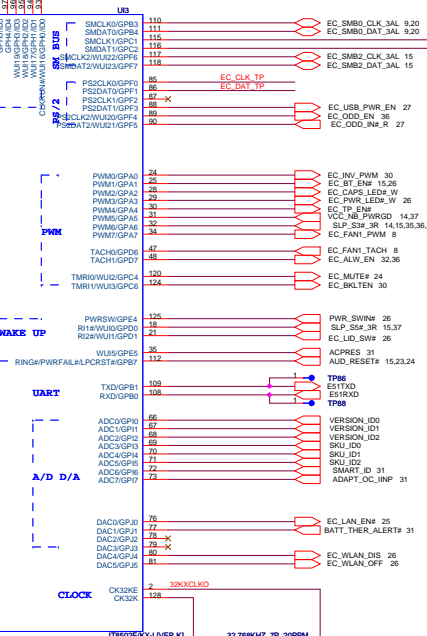


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H9BD R&D

Title: **VGA_S3 (POWER) 3/3**
Doc: Document Number
Rev: MW
Date: 2011.04.08
Page: 20 of 29

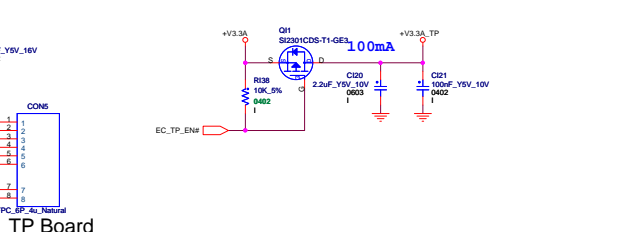
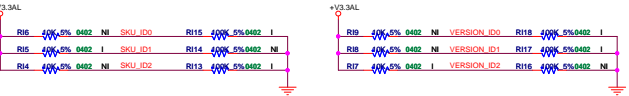


IT8502

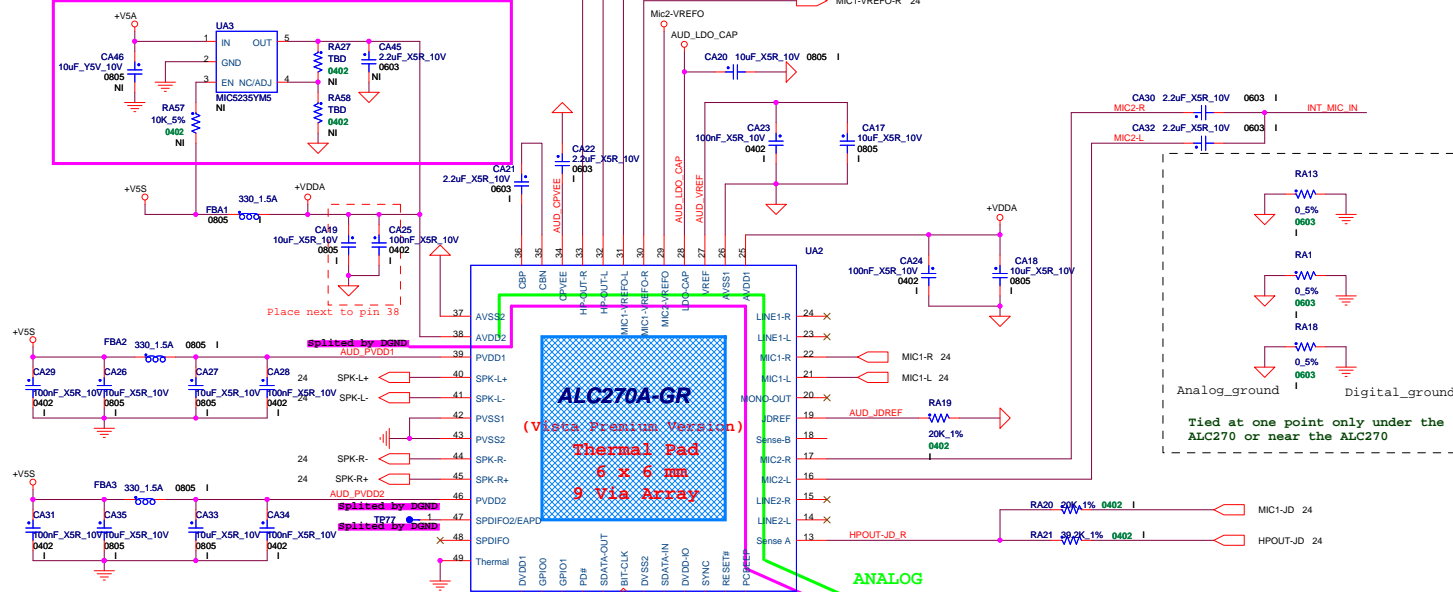


SKU			
SKU	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
M93	0	1	1
UMA (Non HDMI)	1	0	1
PX (Non HDMI)	1	1	0
M93 (Non HDMI)	1	1	1

VERSION			
Phase	ID2	ID1	ID0
Pre-DB	0	0	0
DB	0	0	1
SI	0	1	0
PV	0	1	1
MV	1	0	0



Reserved LDO circuitry for +VDDA power source



Place next to pin 38

Splited by GND

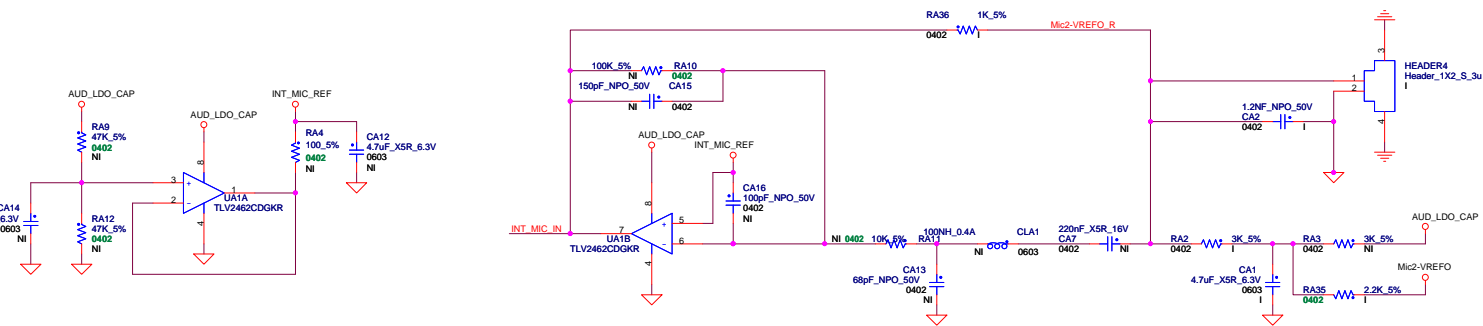
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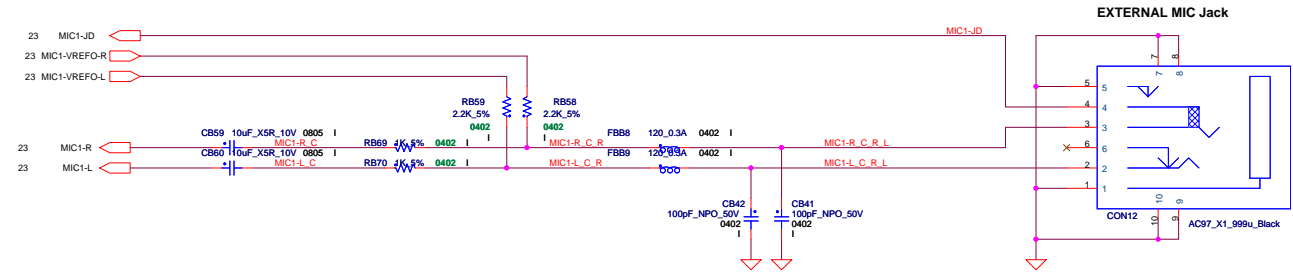
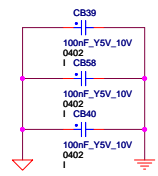
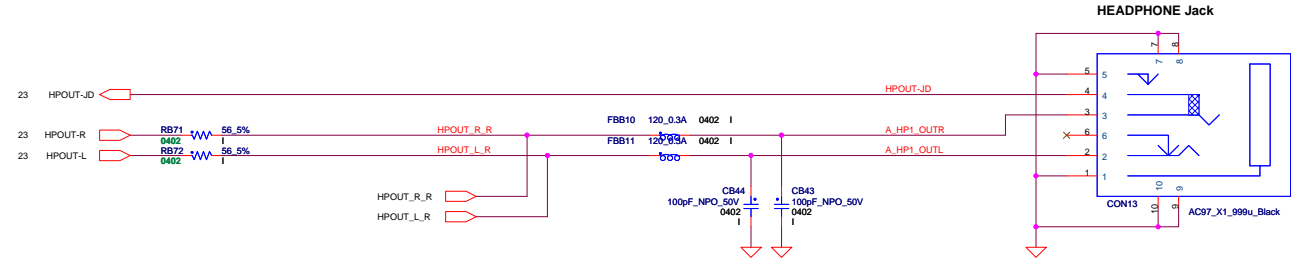
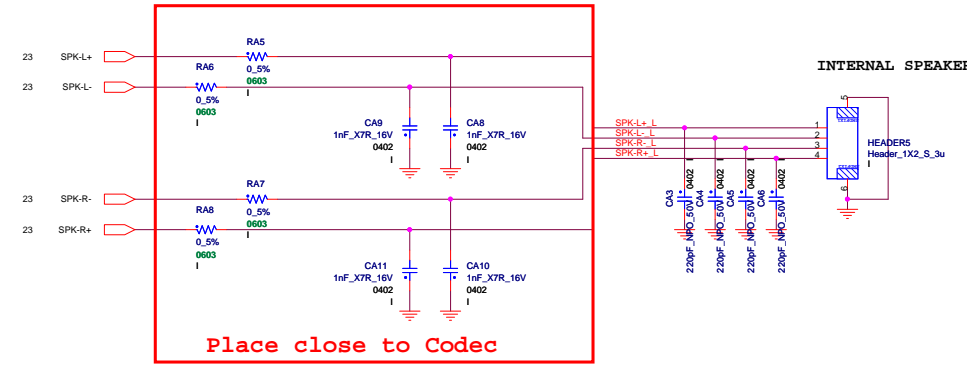
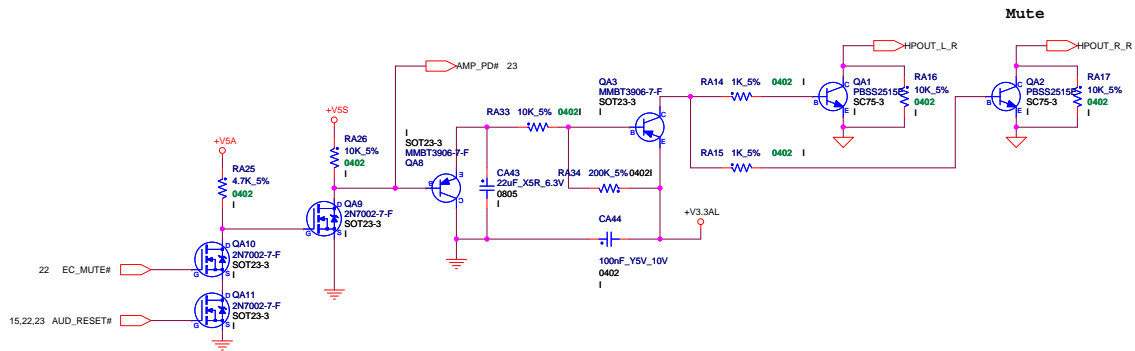
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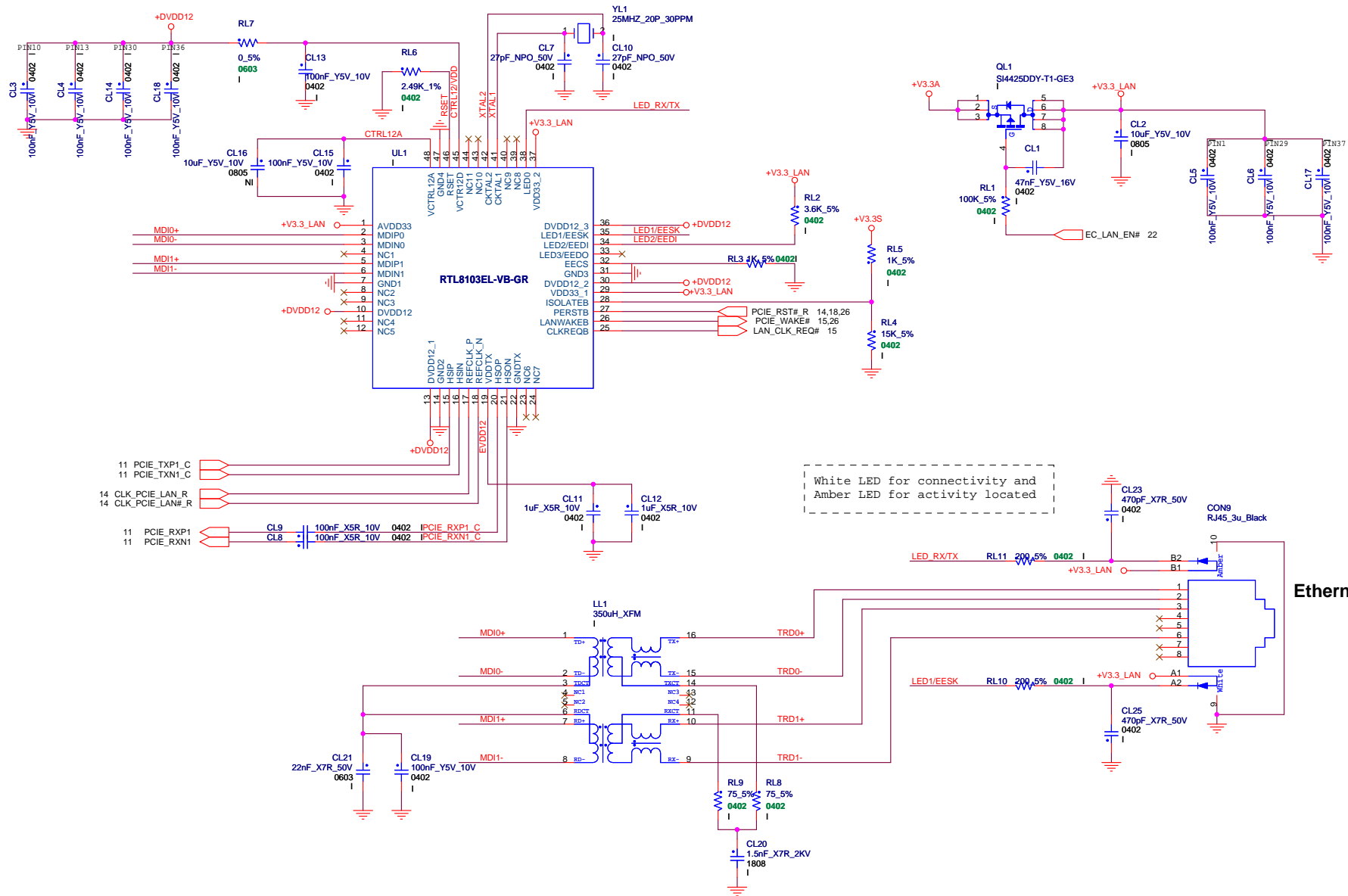
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

PD# = 0V : Power down Class D SPK amplifier
PD# = 3.3V : Power up Class D SPK amplifier

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)



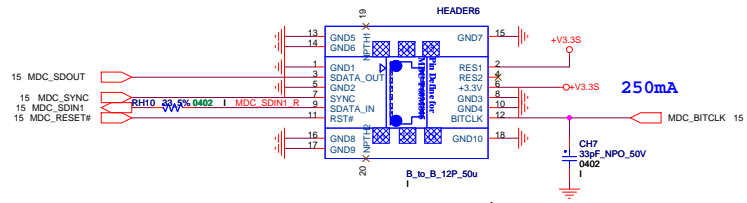




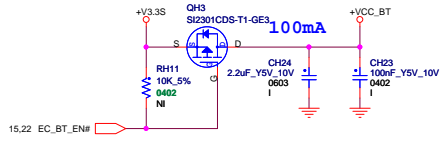
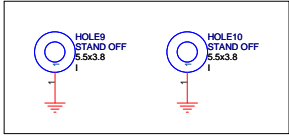
White LED for connectivity and Amber LED for activity located

Ethernet

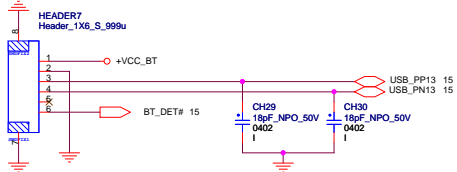
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNB D R&D	
		phone: +886-2-2799-6111	
Title LAN (RTL8103EL)			
Size	Document Number	Rev	
Custom	Safina	MV	
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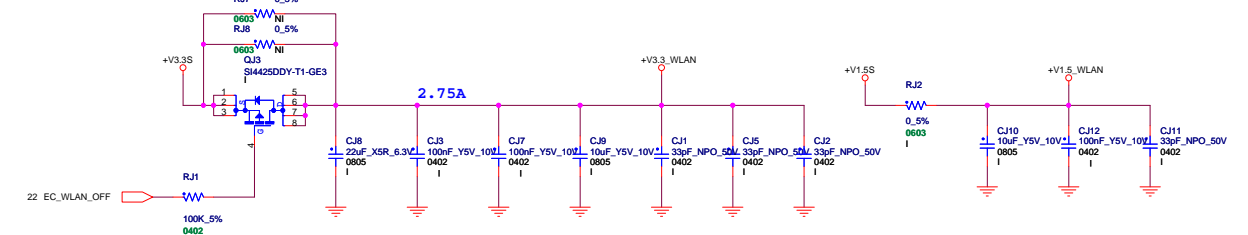
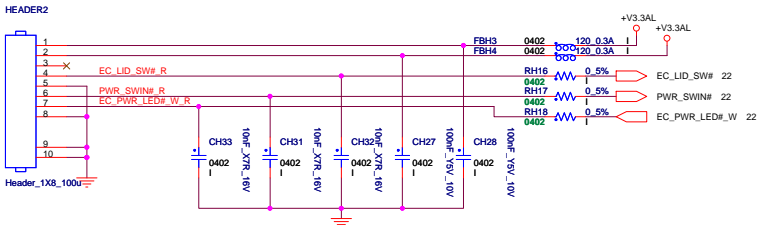
MDC CONN. Option



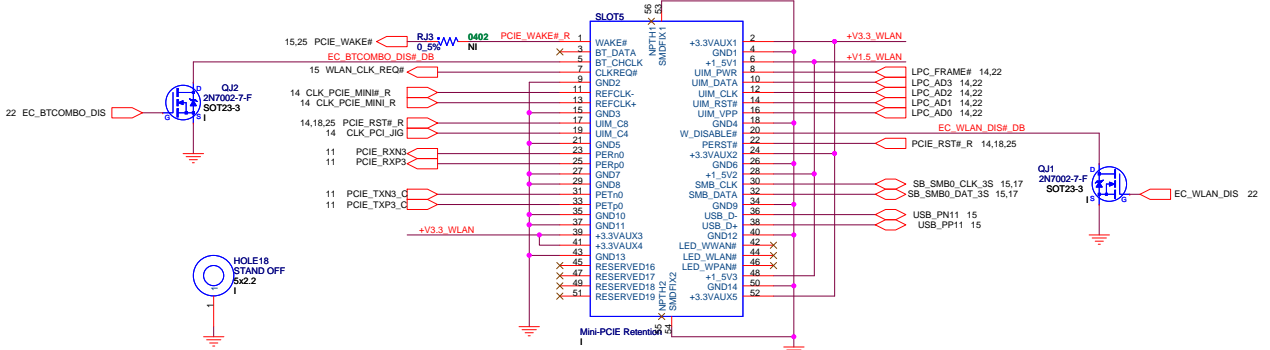
Bluetooth CONN.



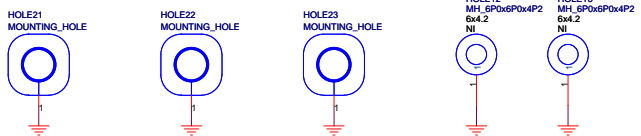
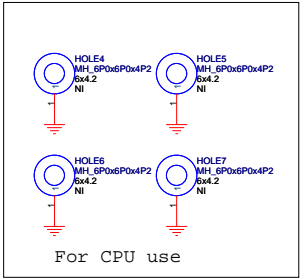
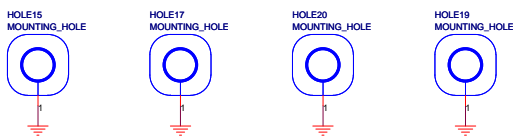
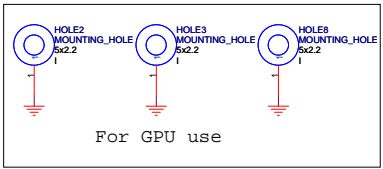
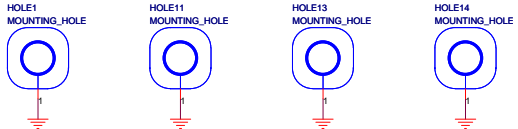
PWR Board CONN.



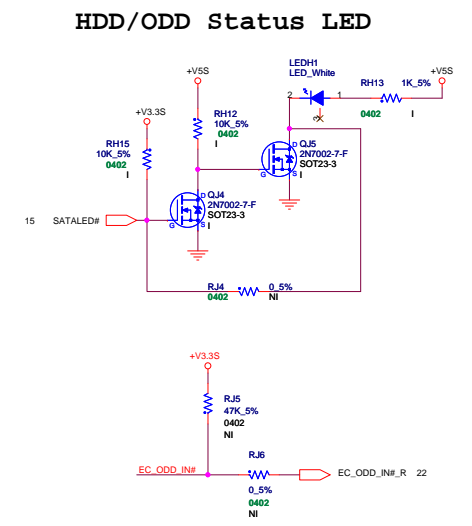
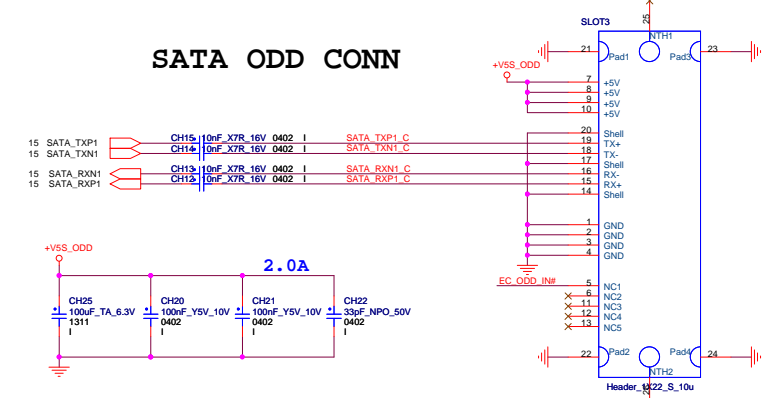
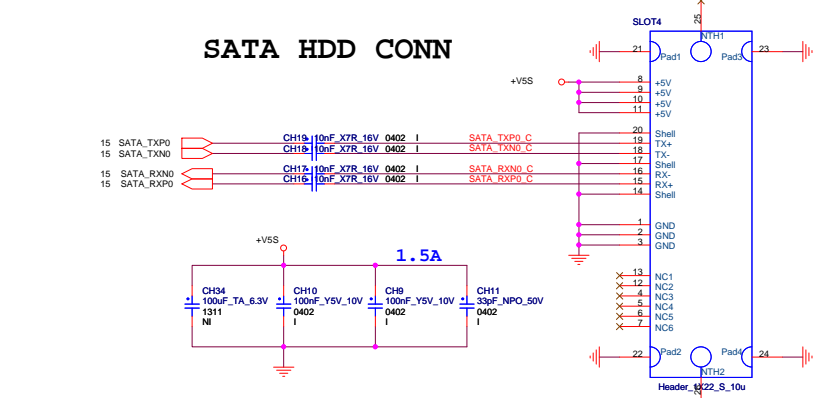
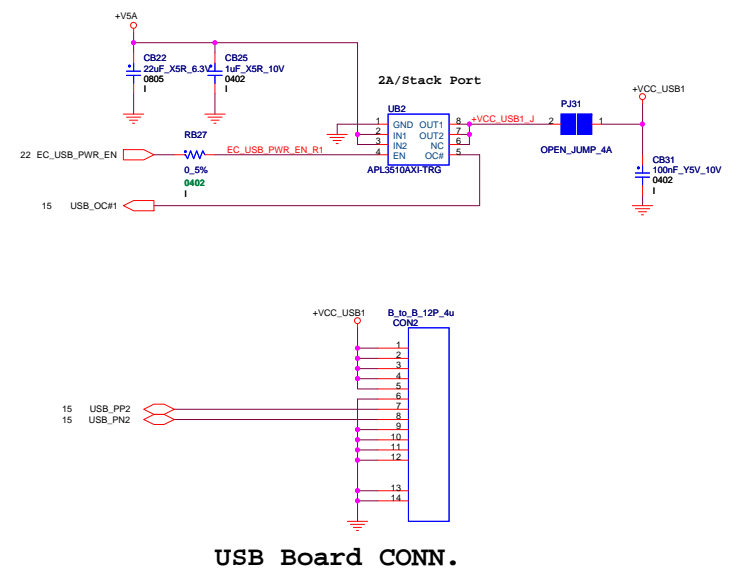
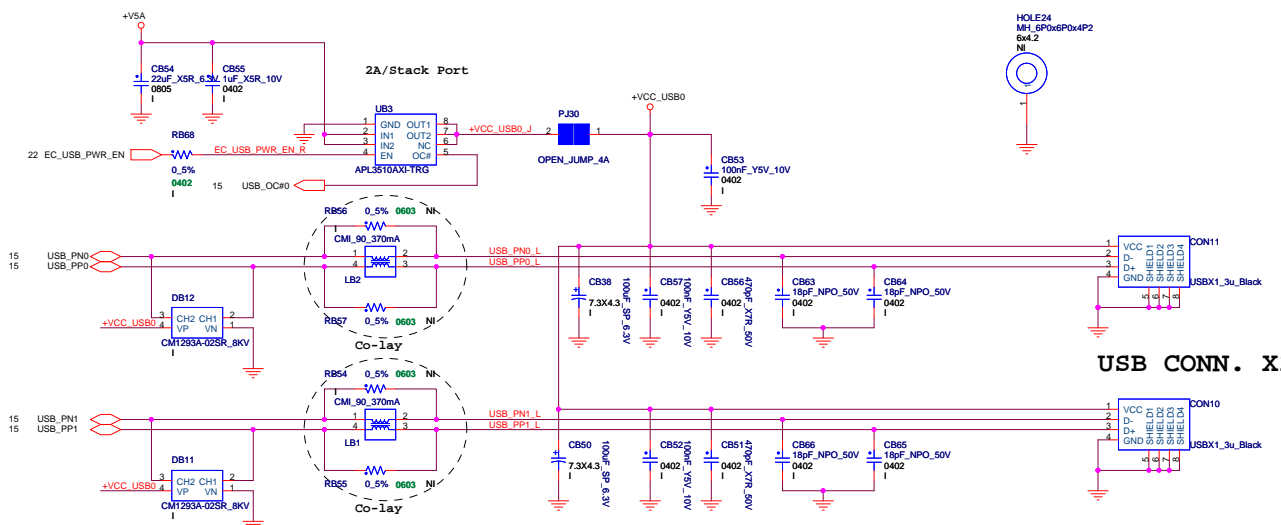
+1.5V=>0.5A Peak/0.375A Normal
+3.3Vaux=>2.75A Peak/1.1A Normal



Half Mini Card for WLAN

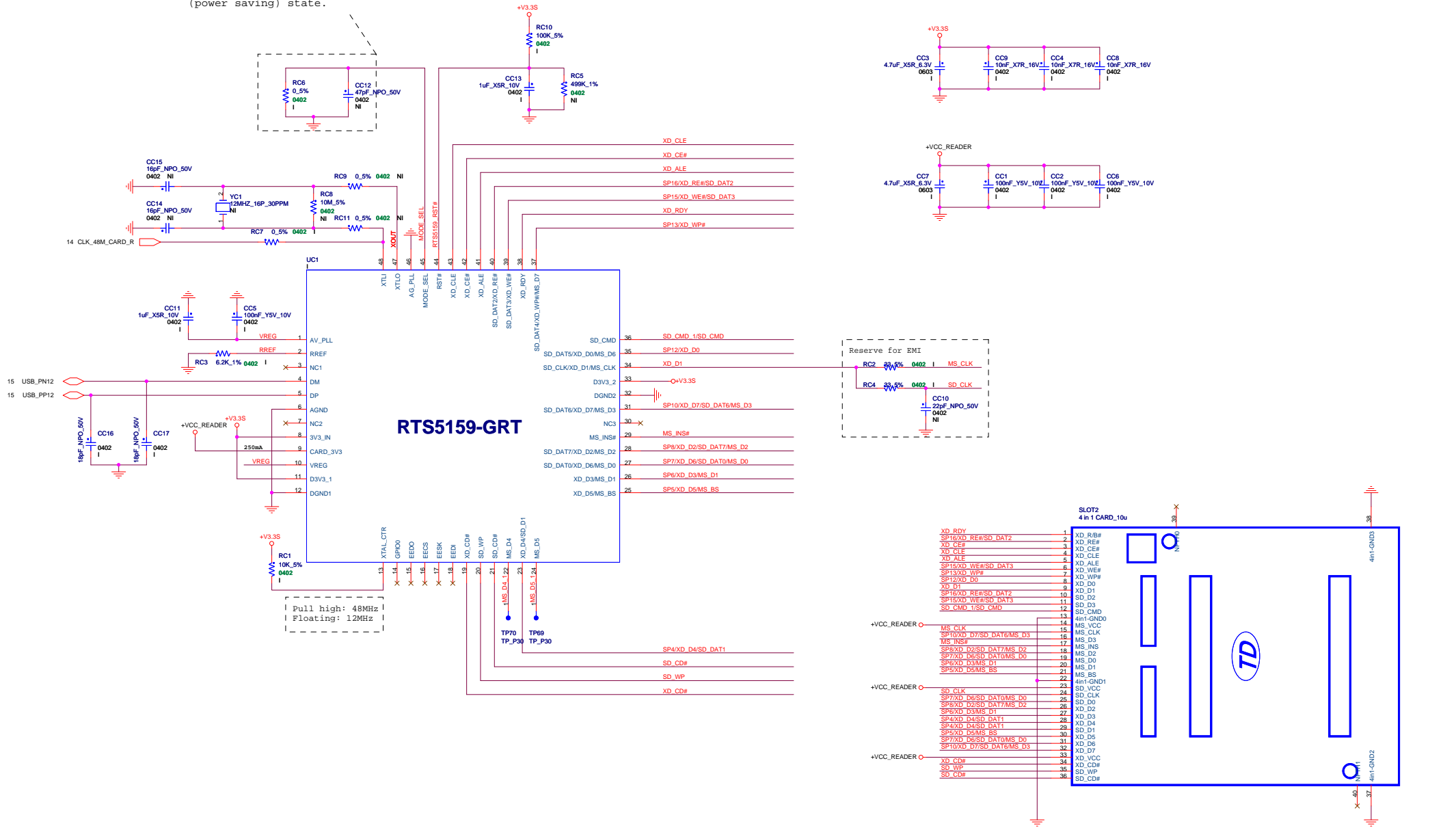


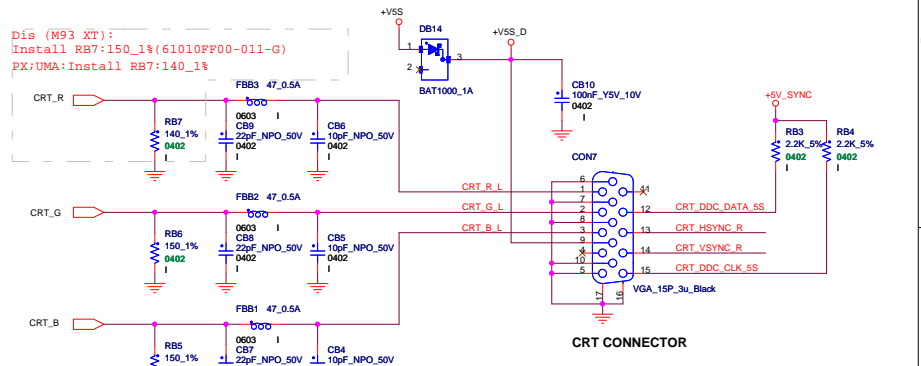
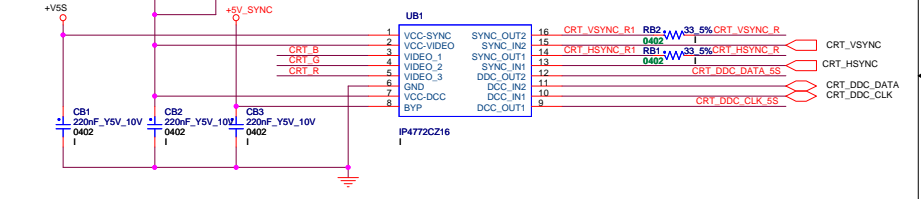
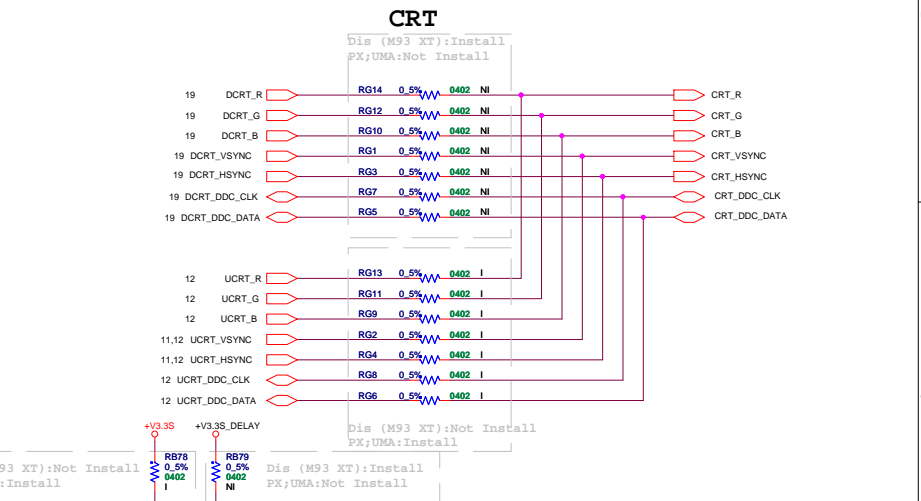
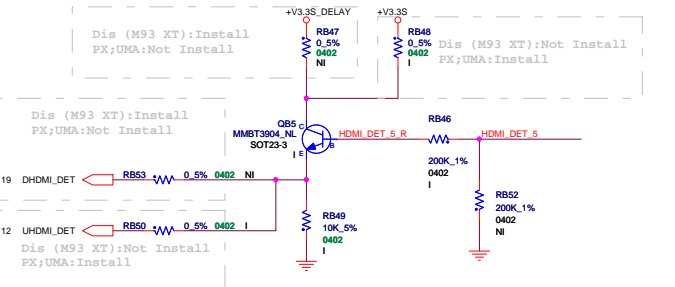
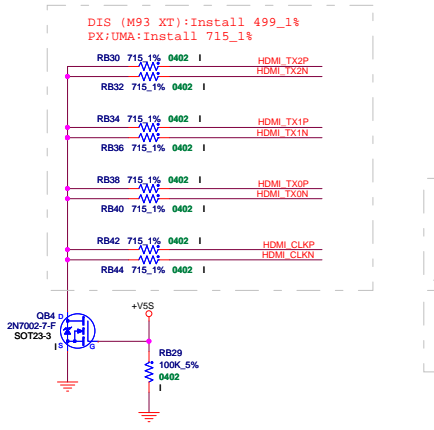
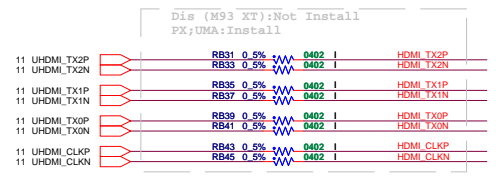
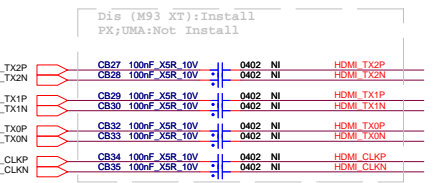
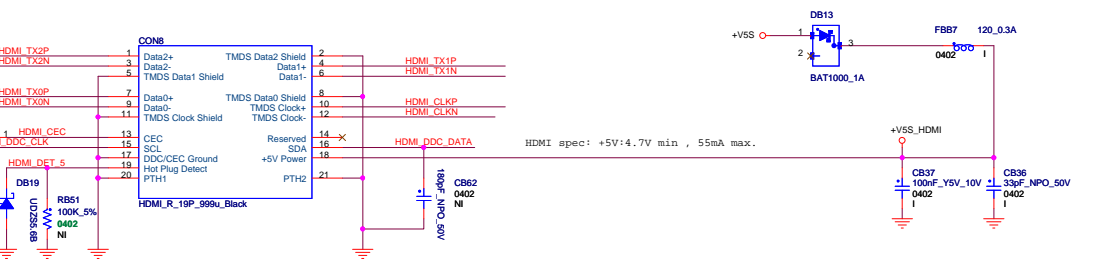
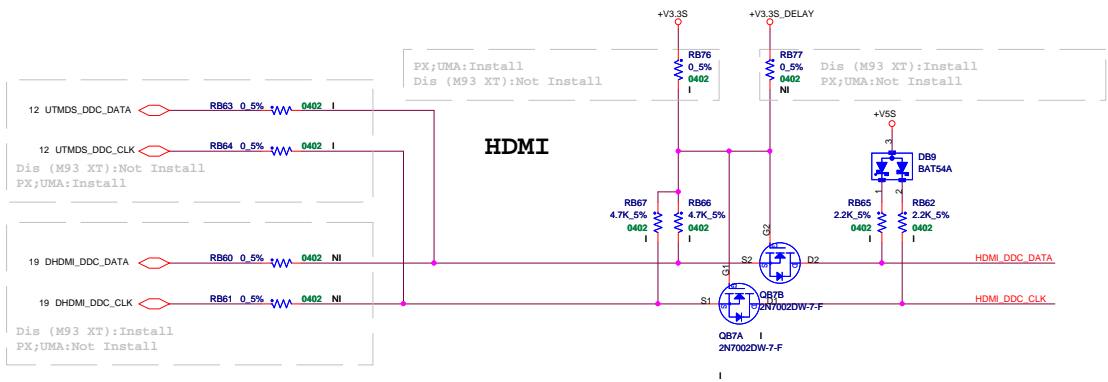
Mounting HOLE

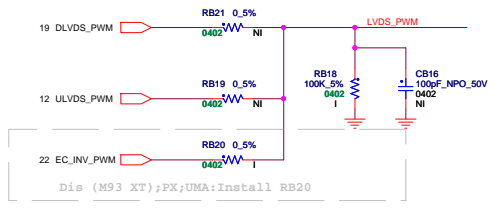


Power pin current
max. 1300 mA (less 2ms)

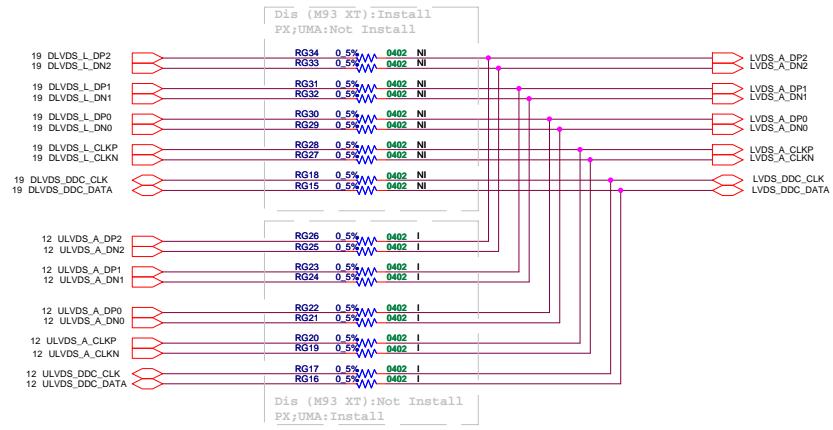
D3 mode: (R:0 ohm ; C:NC)
 If user remove memory card from
 socket, RTS5159 will terminate
 USB bus connection and enter D3
 (power saving) state.



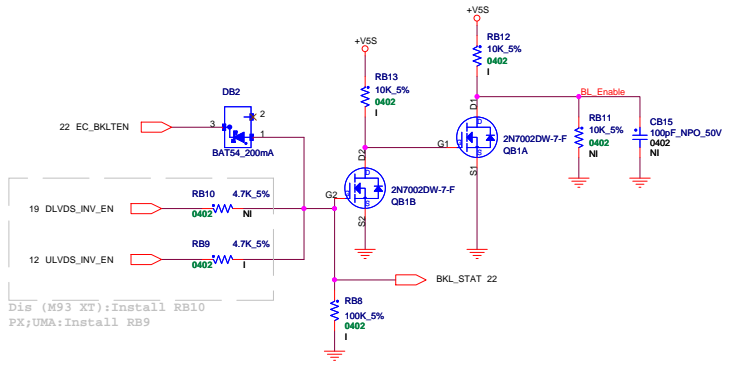




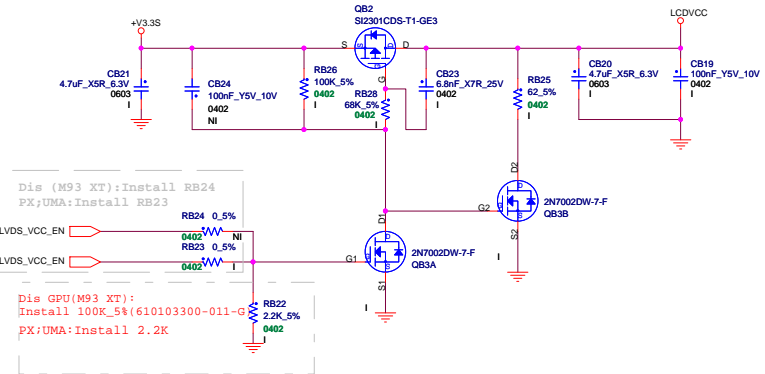
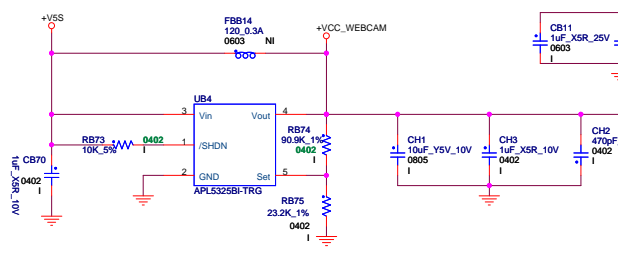
Dis (M93 XT):PX;UMA:Install RB20



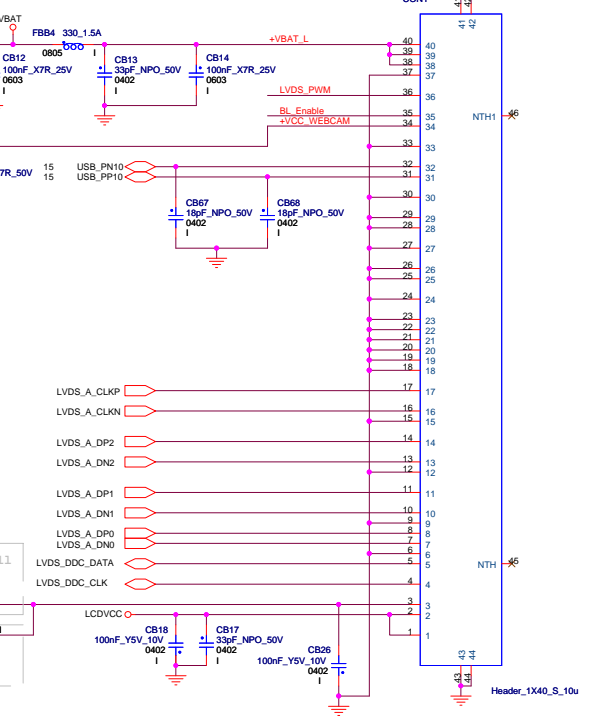
Dis (M93 XT):Not Install
PX;UMA:Install



Dis (M93 XT):Install RB10
PX;UMA:Install RB9

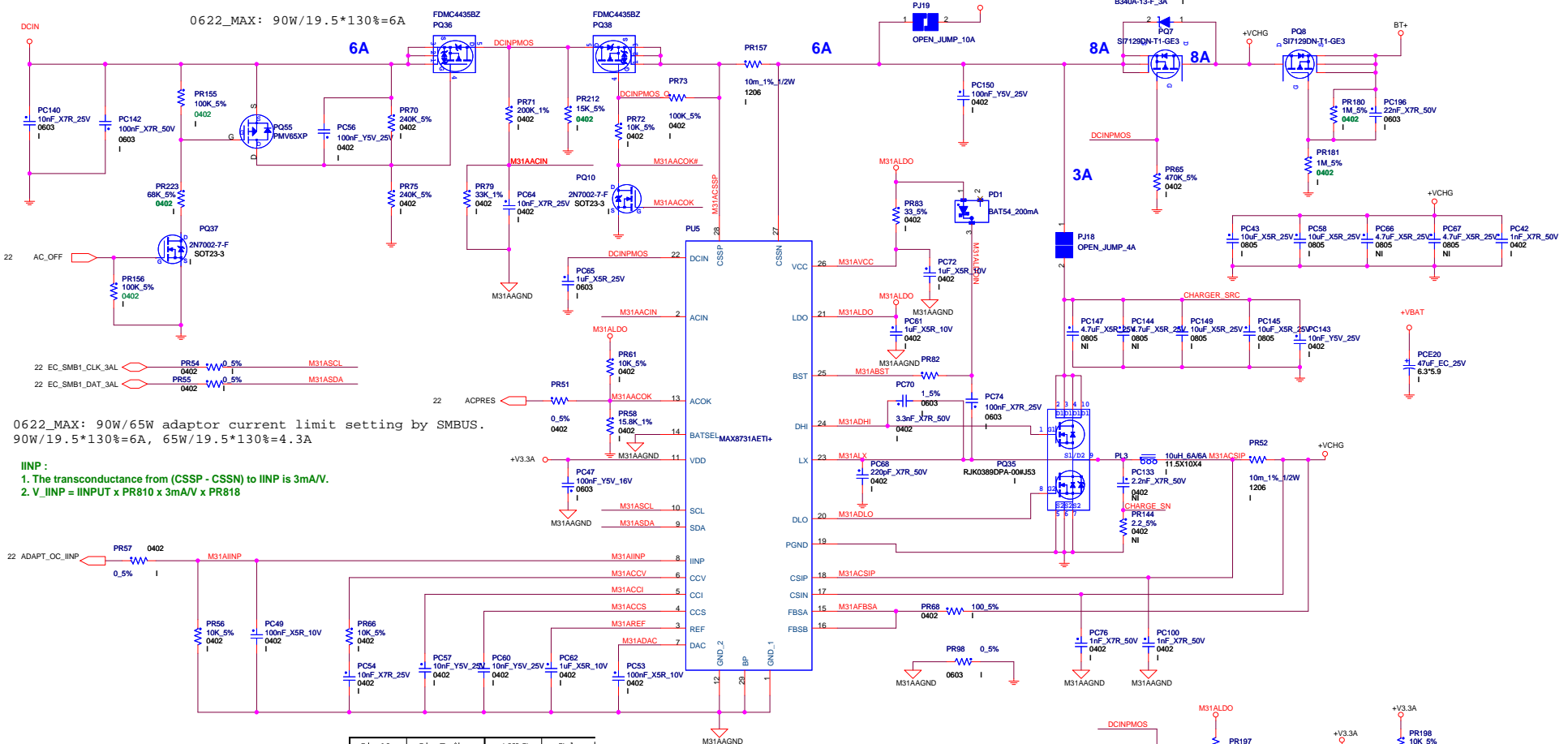


Dis GPU(M93 XT):
Install 100k_5%(610103300-011-G)
PX;UMA:Install 2.2K



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Title		LVDS&Webcam	
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Custom	Safina		
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0622_MAX: 90W/65W adaptor current limit setting by SMBUS.
 $90W/19.5 \times 130\% = 6A$, $65W/19.5 \times 130\% = 4.3A$

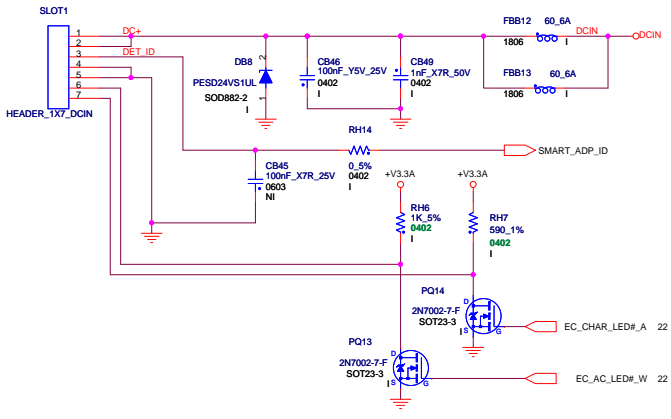
IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_IINP = IINP \times PR810 \times 3mA/V \times PR818$

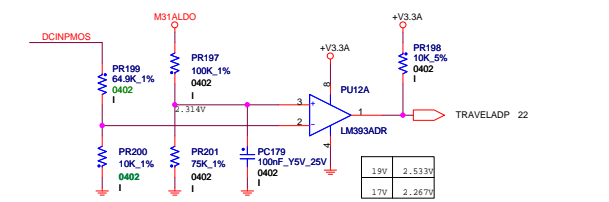
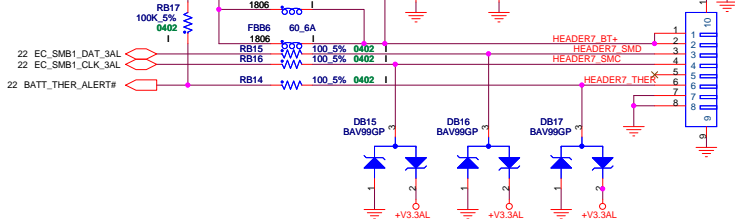
Pin No	Pin Define	AWG	Color
1	DC+	22	Red
2	DC+	22	Red
3	Detect (ID)	28	White
4	DC-	22	Black
5	DC-	22	Black
6	LED-	28	Black
7	LED+	28	yellow

Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal.
2	BATT+	Batt+, Battery Positive Terminal.
3	SMD	SMBus data interface I/O pin..
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

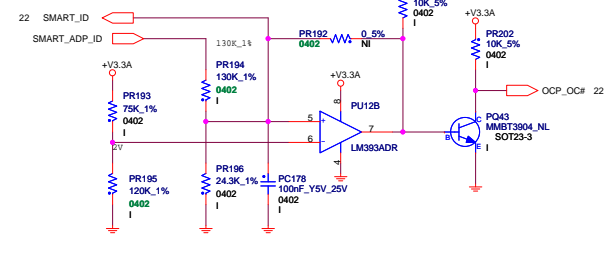
ADAPTOR In CON.



BATTERY CON.



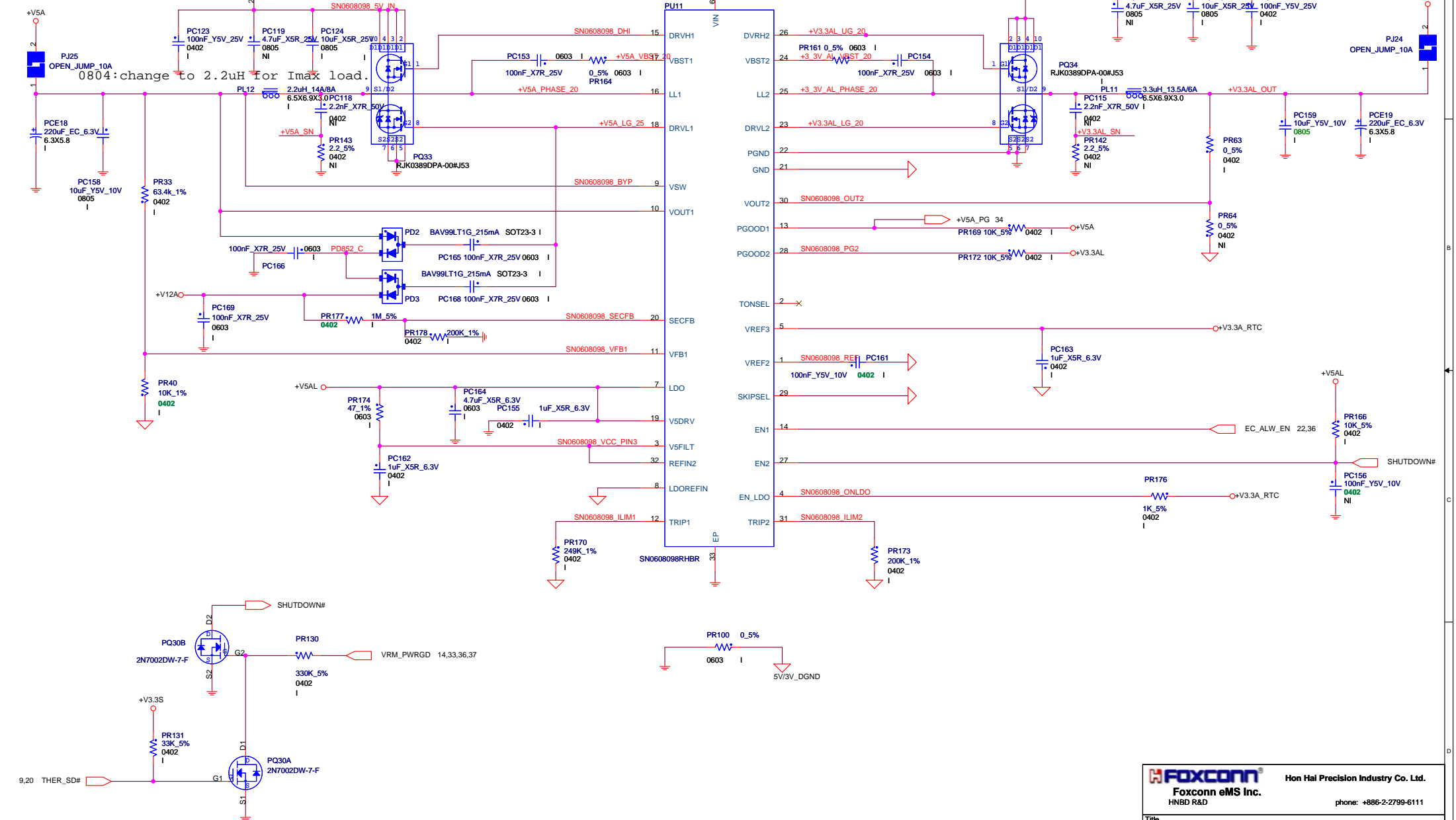
U1A Pin	8SD	GSW	281K	90W	294K	120W	221K	135V	169V	180W	130K
Non	0.495V	0.62V	0.773V	0.938V	1.115V						
ADPDC	3V	3V	3V	3V	3V						



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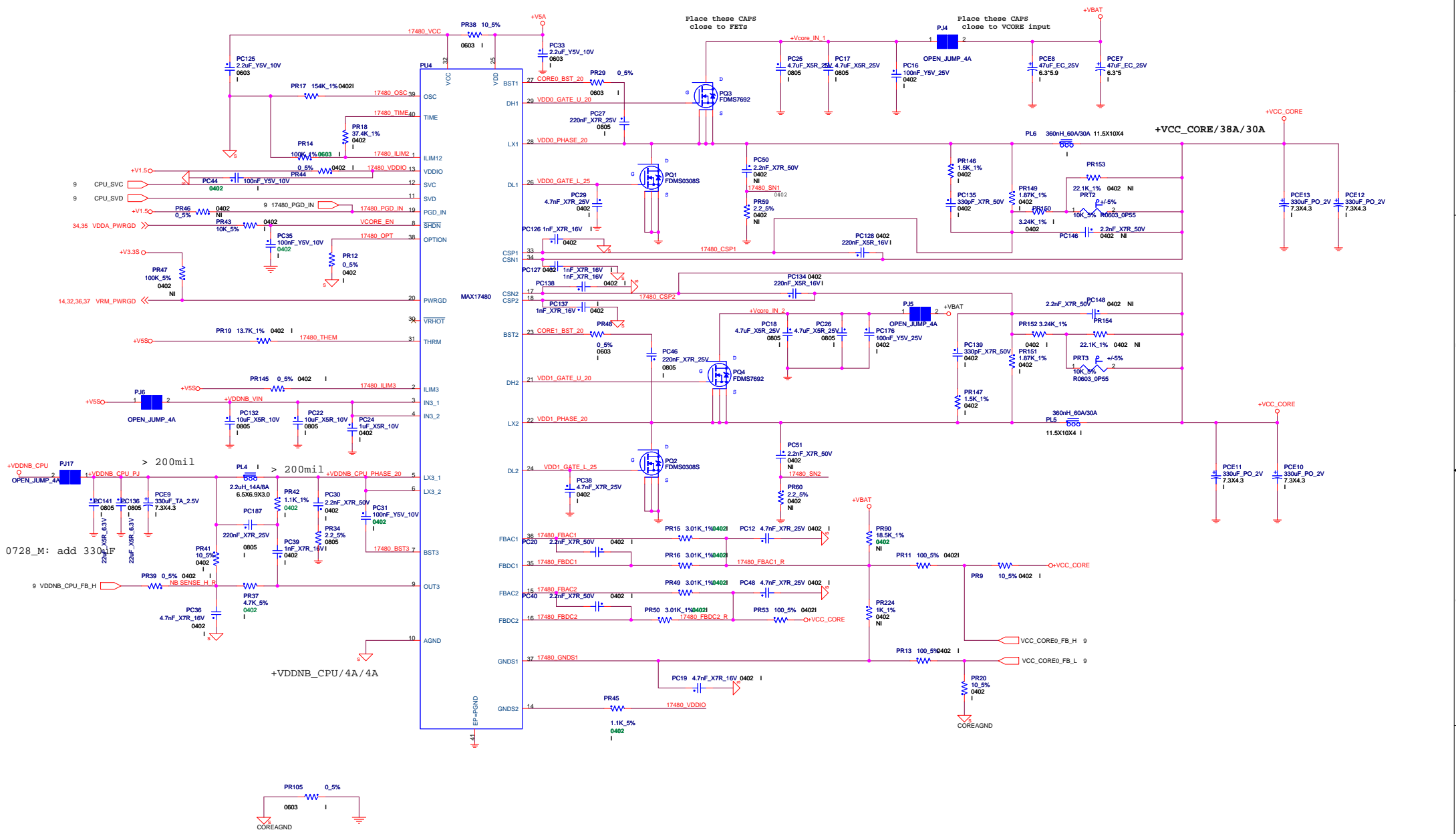
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 Custom: Safina Rvw: MV
 Page Modified: Wednesday, April 07, 2010 16:16:16 (UTC/GMT) Sheet 31 of 39

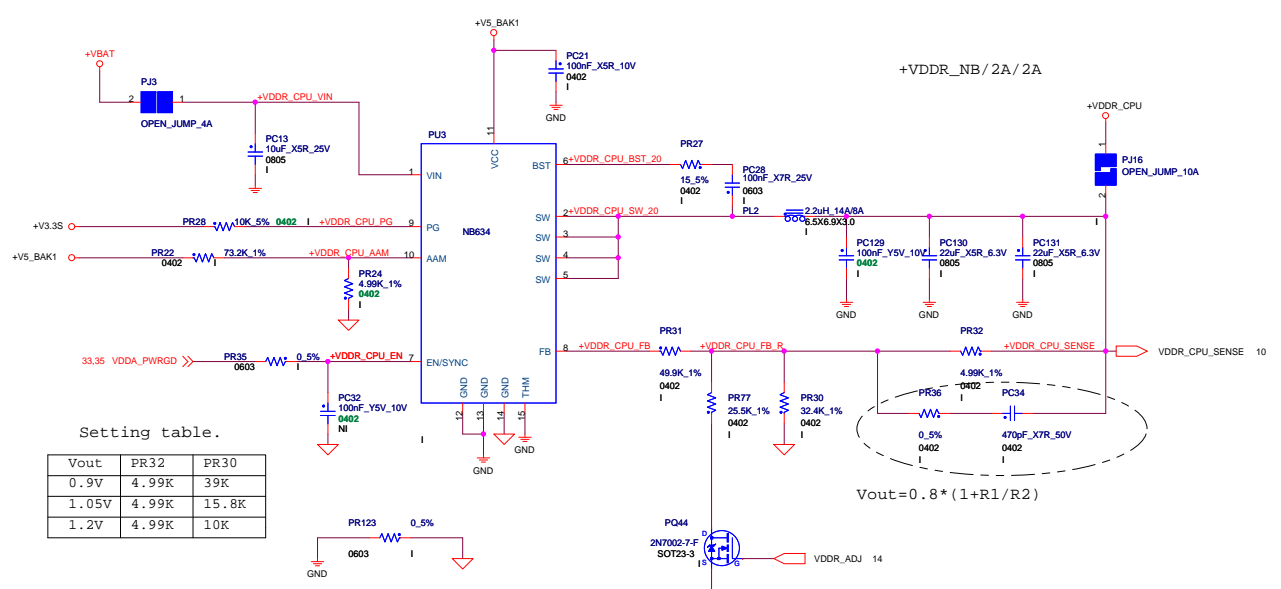
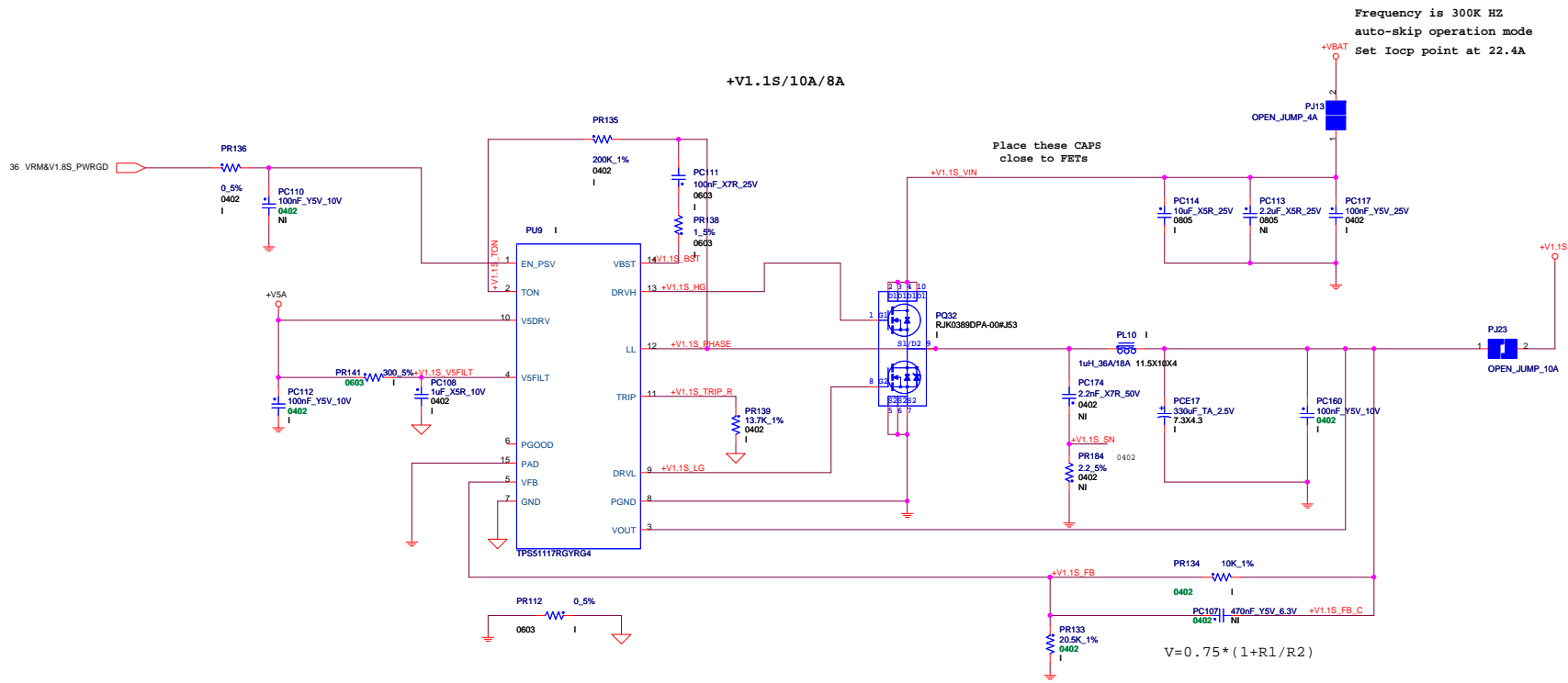
+V5A/7A/5.6A

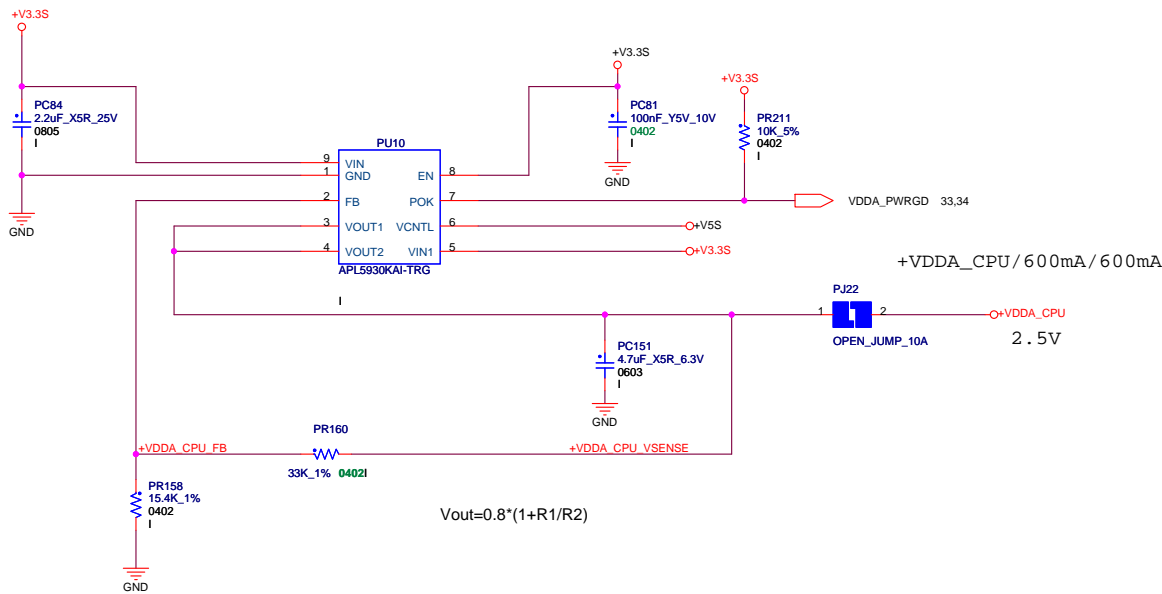
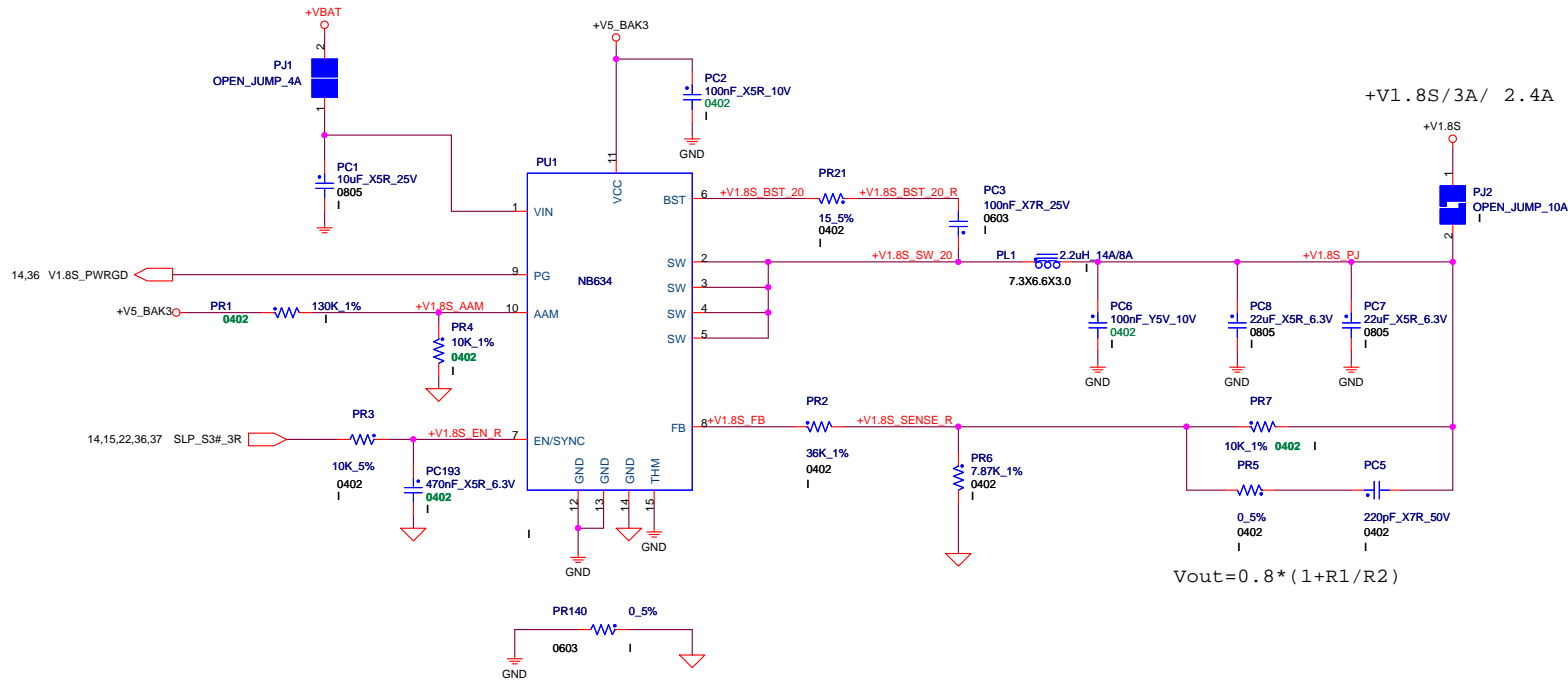


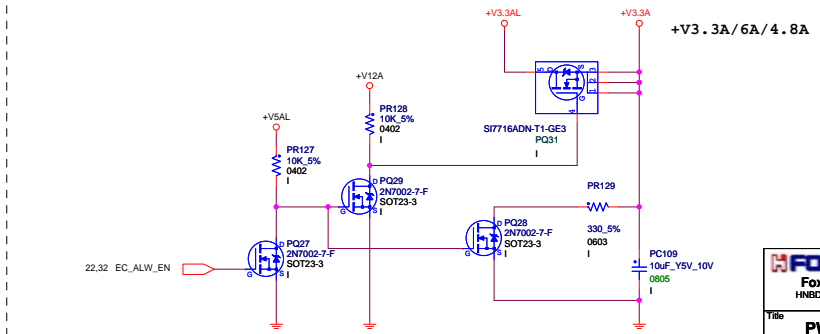
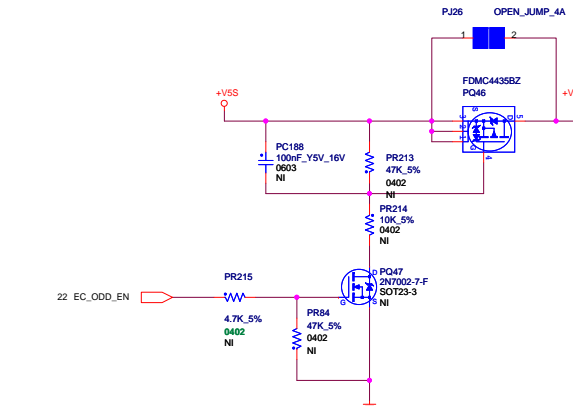
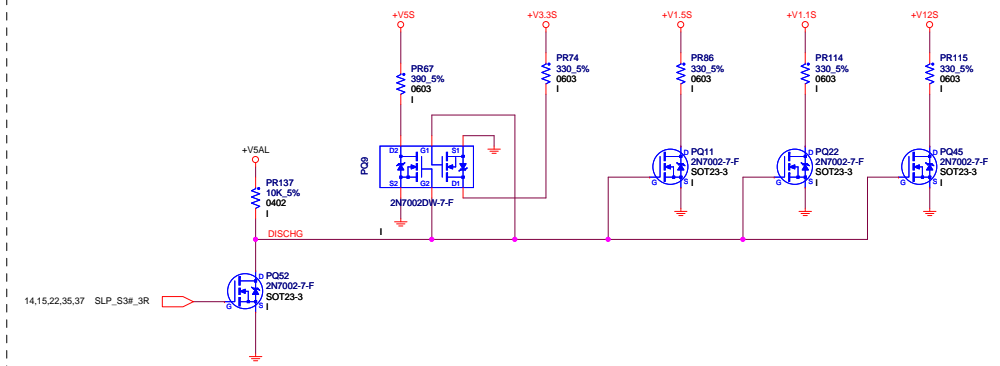
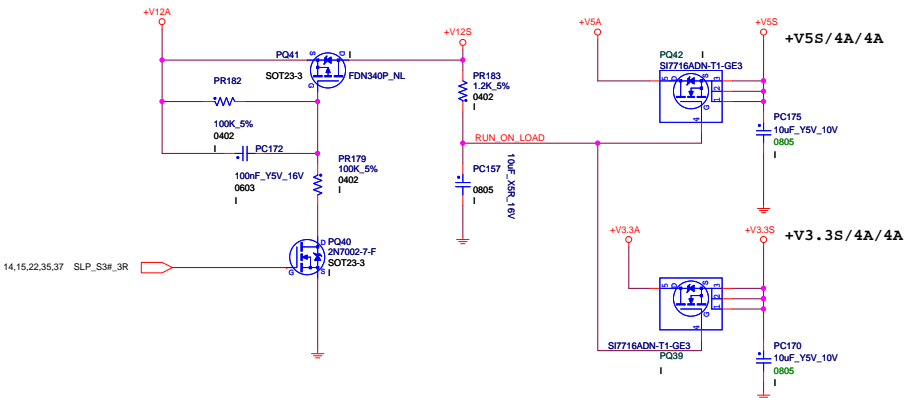
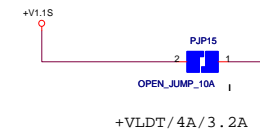
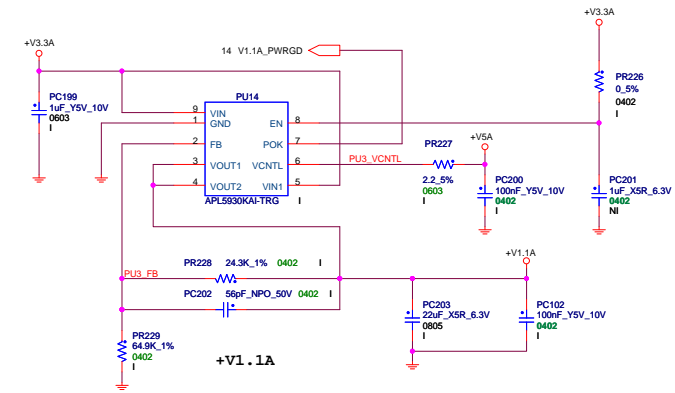
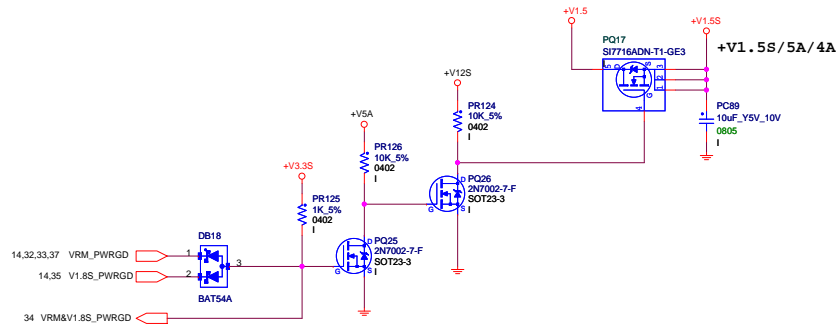
0804:change to 2.2uH for I_{max} load.

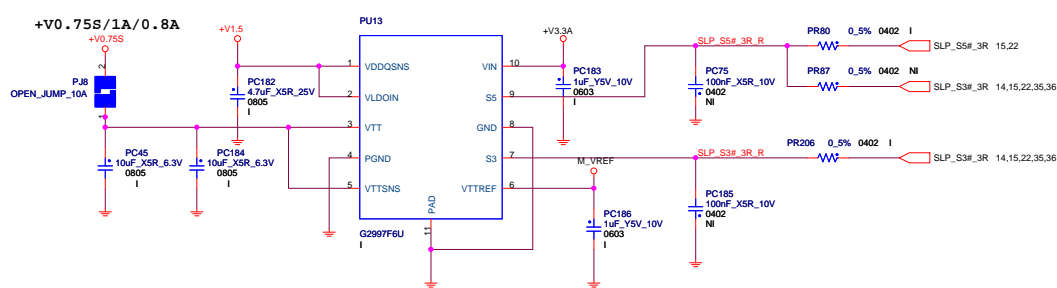
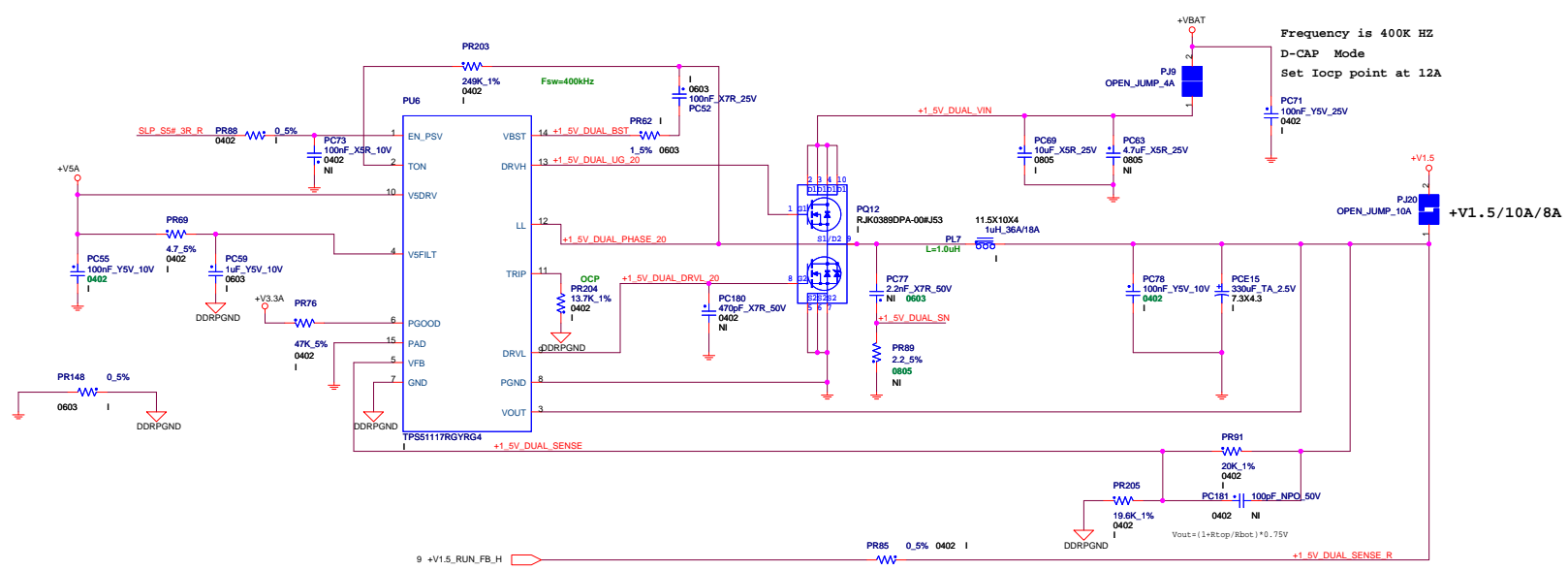
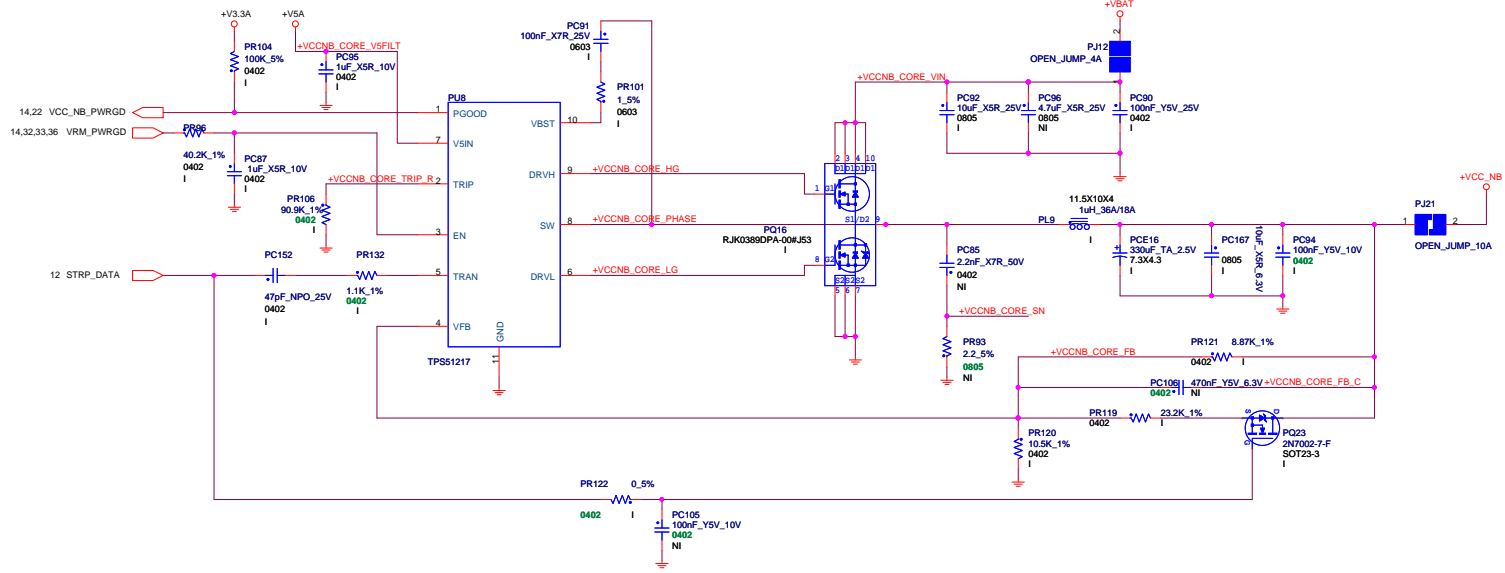
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Title 5V/3.3V SN0608098RHBT			
Size Custom	Document Number Safina	Rev MV	
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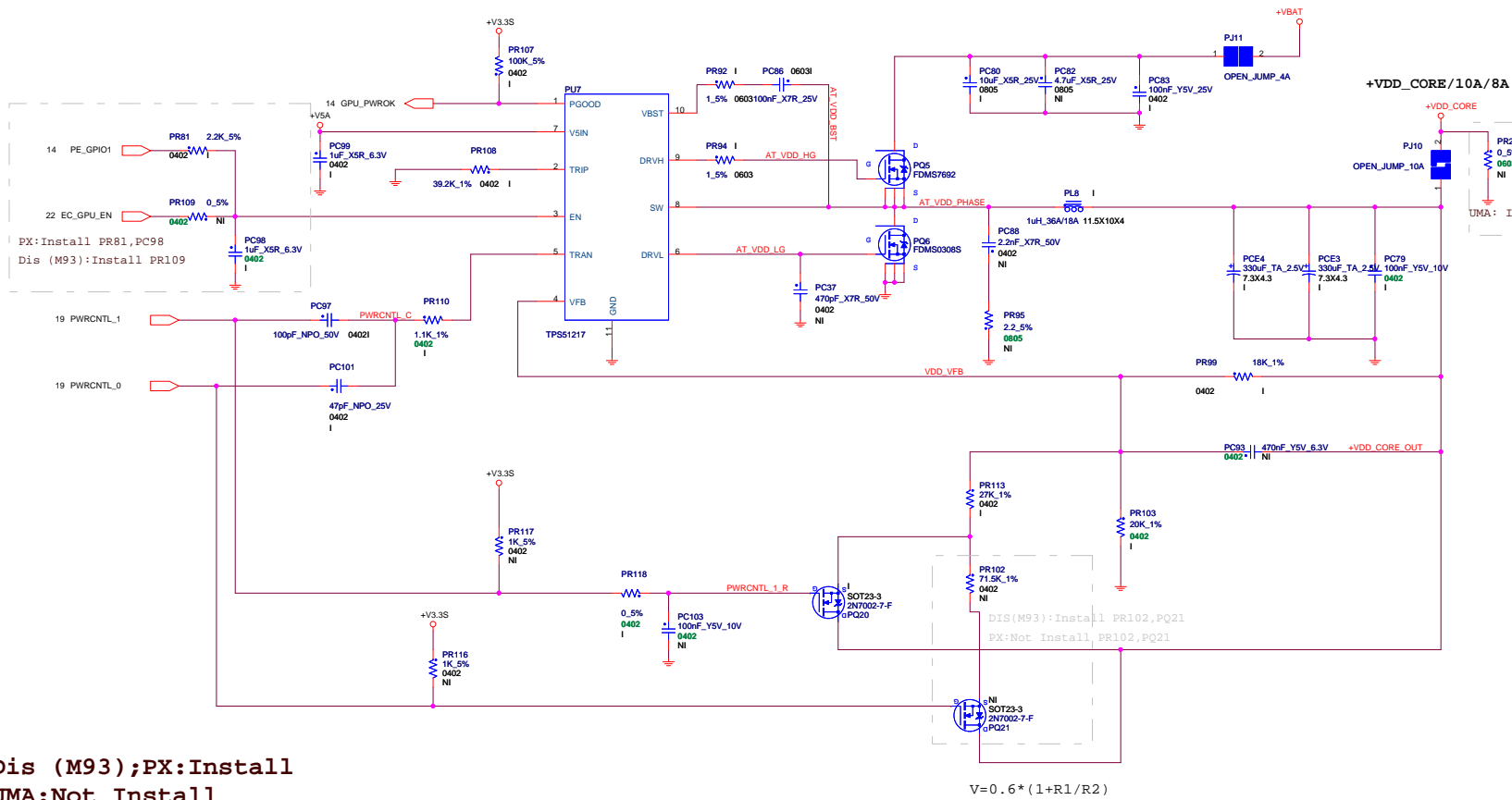












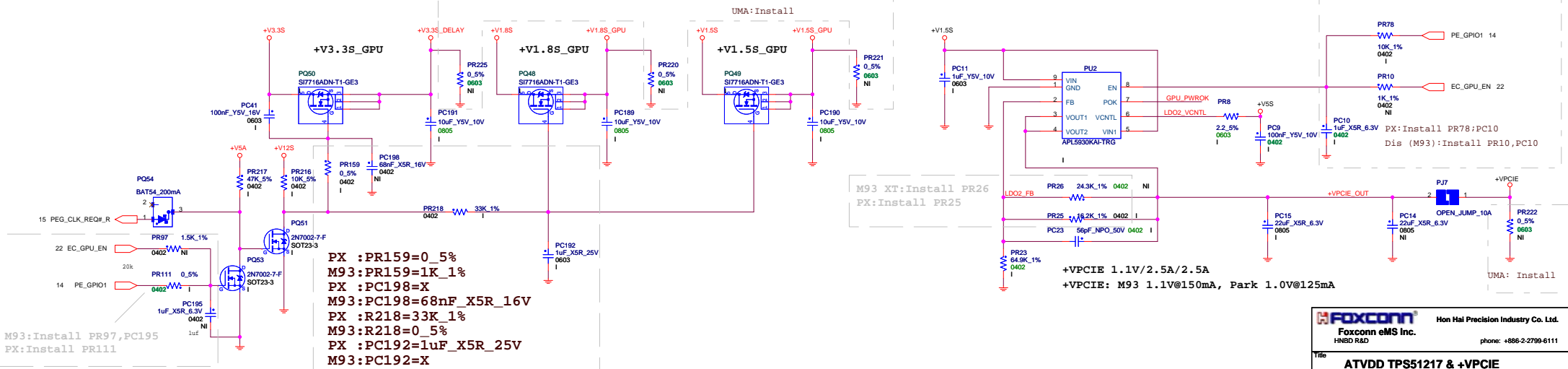
VID table	M93_XT_S3	Park_XT_S3
PR99	20.5K_1% (610113W00-012-G)	18K_1% (610115W00-012-G)
PR103	20K_1% (610114H00-011-G)	20K_1% (610114H00-011-G)
PR113	28.7K_1% (61011B400-012-G)	27K_1% (610117200-012-G)
PR102	71.5K_1% (611008700-011-G)	N/A

PWRCNTL_1	PWRCNTL_0	M93_XT_S3
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V

PWRCNTL_1	Park_XT_S3
0	1.12V
1	0.9V

Dis (M93);PX:Install
UMA:Not Install

$$V = 0.6 * (1 + R1/R2)$$

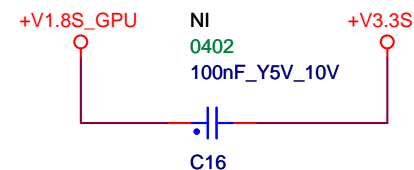
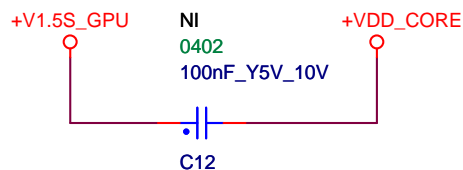
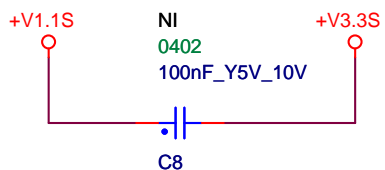
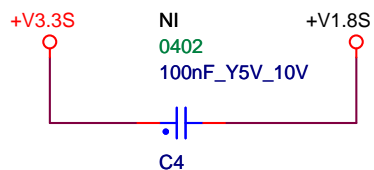
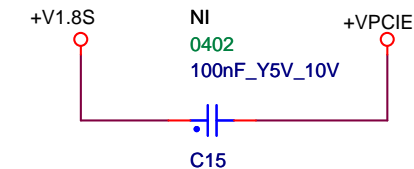
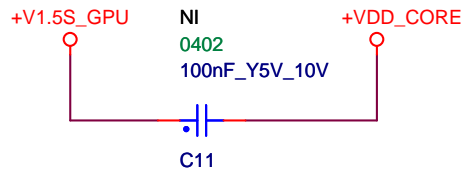
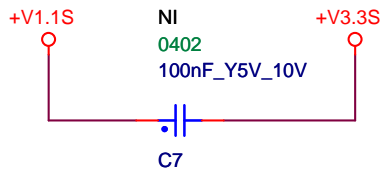
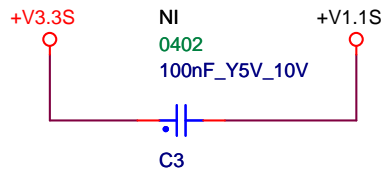
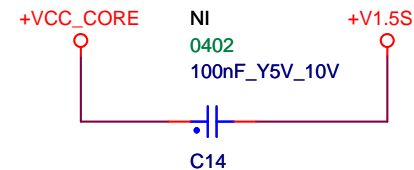
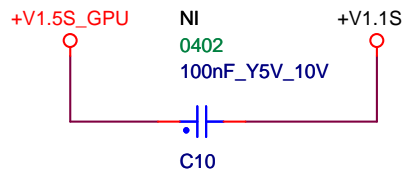
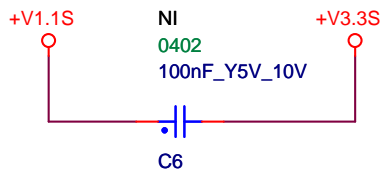
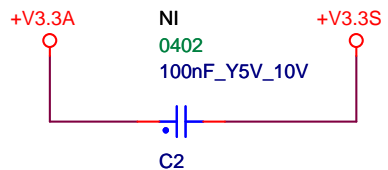
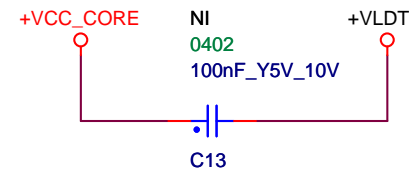
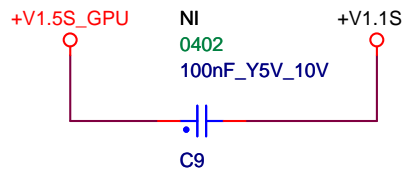
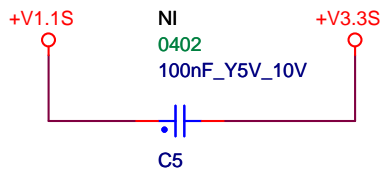
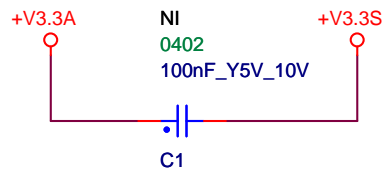


PX : PR159=0.5%
M93: PR159=1K_1%
PX : PC198=X
M93: PC198=68nF_X5R_16V
PX : R218=33K_1%
M93: R218=0.5%
PX : PC192=1uF_X5R_25V
M93: PC192=X

M93 XT: Install PR26
PX: Install PR25

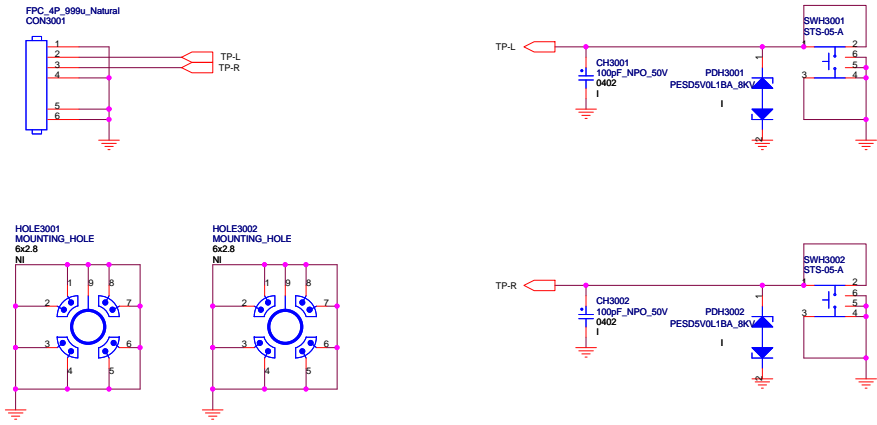
+VPCIE 1.1V/2.5A/2.5A
+VPCIE: M93 1.1V@150mA, Park 1.0V@125mA

M93: Install PR97, PC195
PX: Install PR111

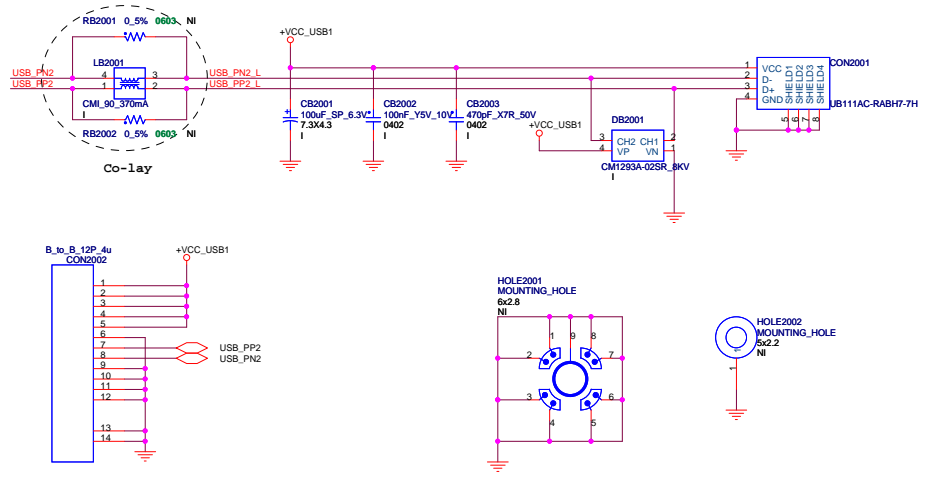


Only for 6 layer M/B use

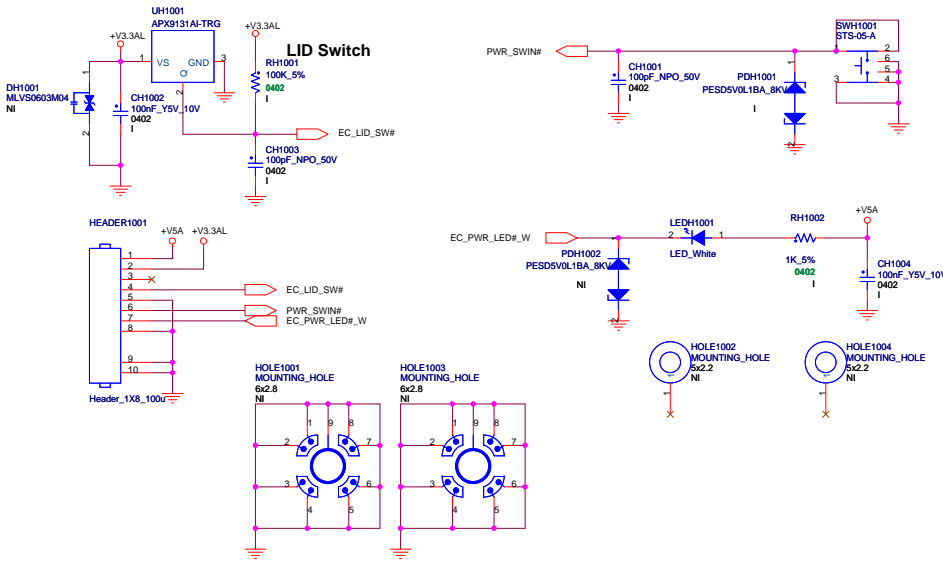
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Title SYSTEM BLOCK DIAGRAM			
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SW Board



USB Board



Power Board

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