

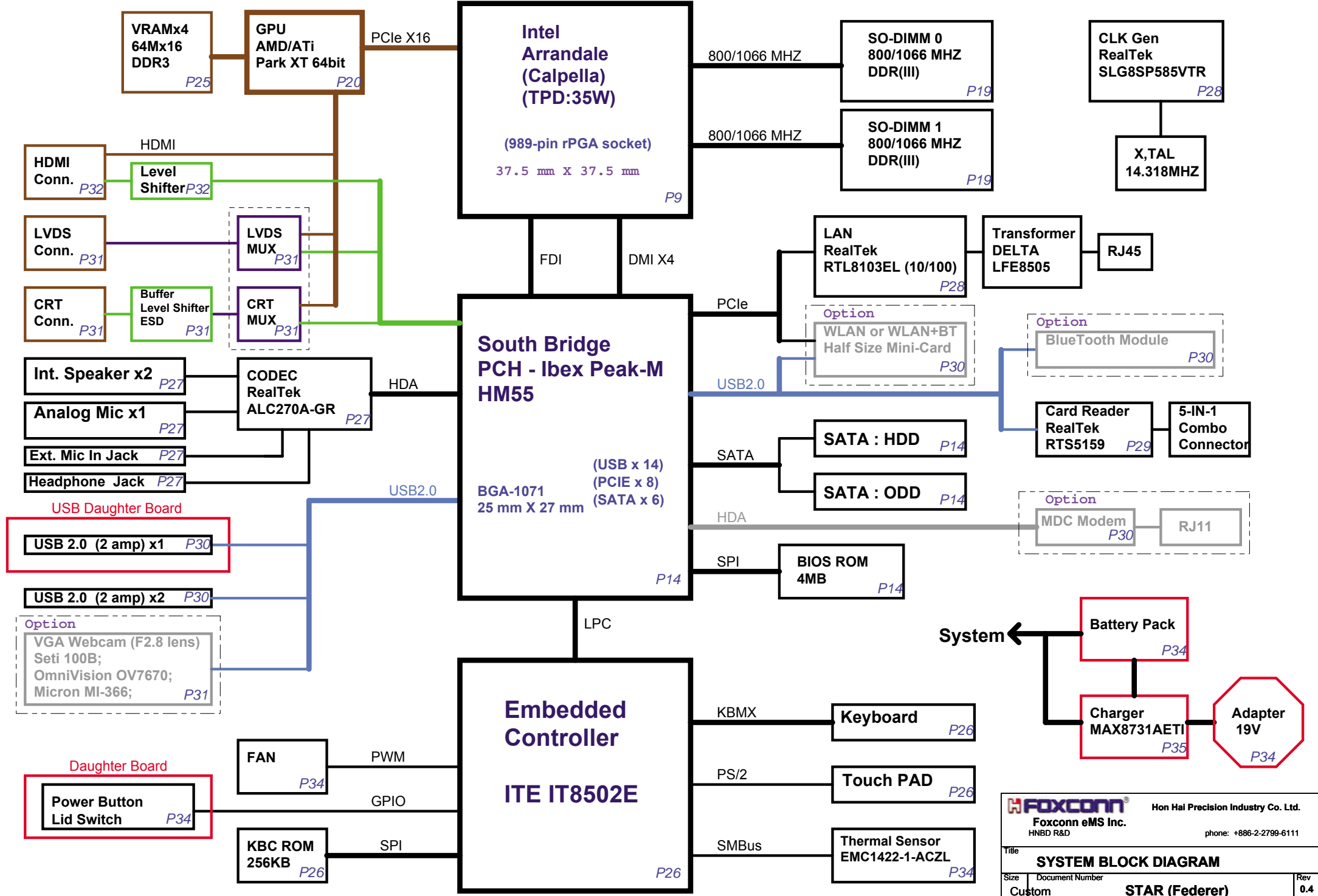
01 -- COVER SHEET	21 -- VGA_S3 (IO) 2/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DDR3) 3/5
03 -- CLOCK MAP	23 -- VGA_S3 (DP) 4/5
04 -- POWER MAP	24 -- VGA_S3 (POWER) 5/5
05 -- POWER SEQUENCY DIAGRAM	25 -- VRAM (DDR3)
06 -- POWER SEQUENCY TIMING	26 -- EC+KBC (IT8502E)
07 -- SMBUS MAP	27 -- CODEC/JACK/SPEAKER/MIC
08 -- RESET SIGNAL MAP	28 -- LAN (RTL8103EL)/CLOCK GEN
09 -- Calpella (DMI,PEG,FDI)	29 -- Card Reader
10 -- Calpella (CLK,MISC,JTAG)	30 -- WLAN/BT/MDC/USB/MOUNTING
11 -- Calpella (DDR3)	31 -- LVDS/CRT/Webcam
12 -- Calpella (POWER/GND)	32 -- HDMI
13 -- Calpella (GRAPHIC POWER)	33 -- DCIN/Battery/OCP/FAN
14 -- PCH (HDA,JTAG,SATA)	34 -- PWR_Charger MAX8731AETI
15 -- PCH (PCI-E,SMBUS,CLK)	35 -- 5V/3.3V SN0608098RHBT
16 -- PCH (DMI,FDI,GPIO,LVDS)	36 -- Vcore MAX17030
17 -- PCH (PCI,USB,NVRAM,GPIO)	37 -- 1.1V VTT/+V1.05RUN
18 -- PCH (POWER)	38 -- 1.5VDDR3+0.75V+V1.8RUN
19 -- DDR3(SO-DIMM_0&1)	39 -- PWR_Others power plane
20 -- VGA (PCI-E/STRAP) 1/5	40 -- CPU VREG & Decoupling
	41 -- ATVDD/+VPCIE

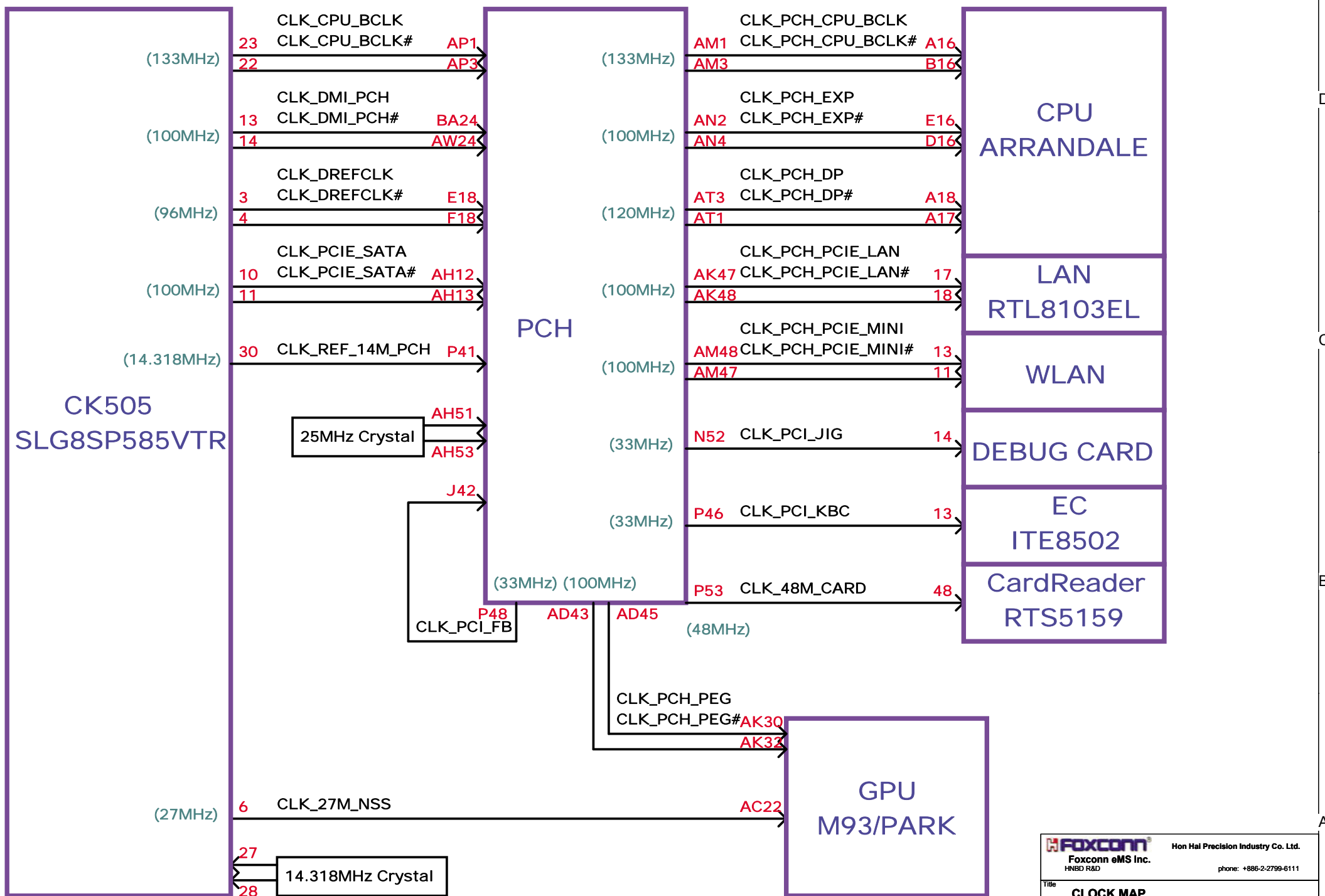
P. Leader	Check by	Design by

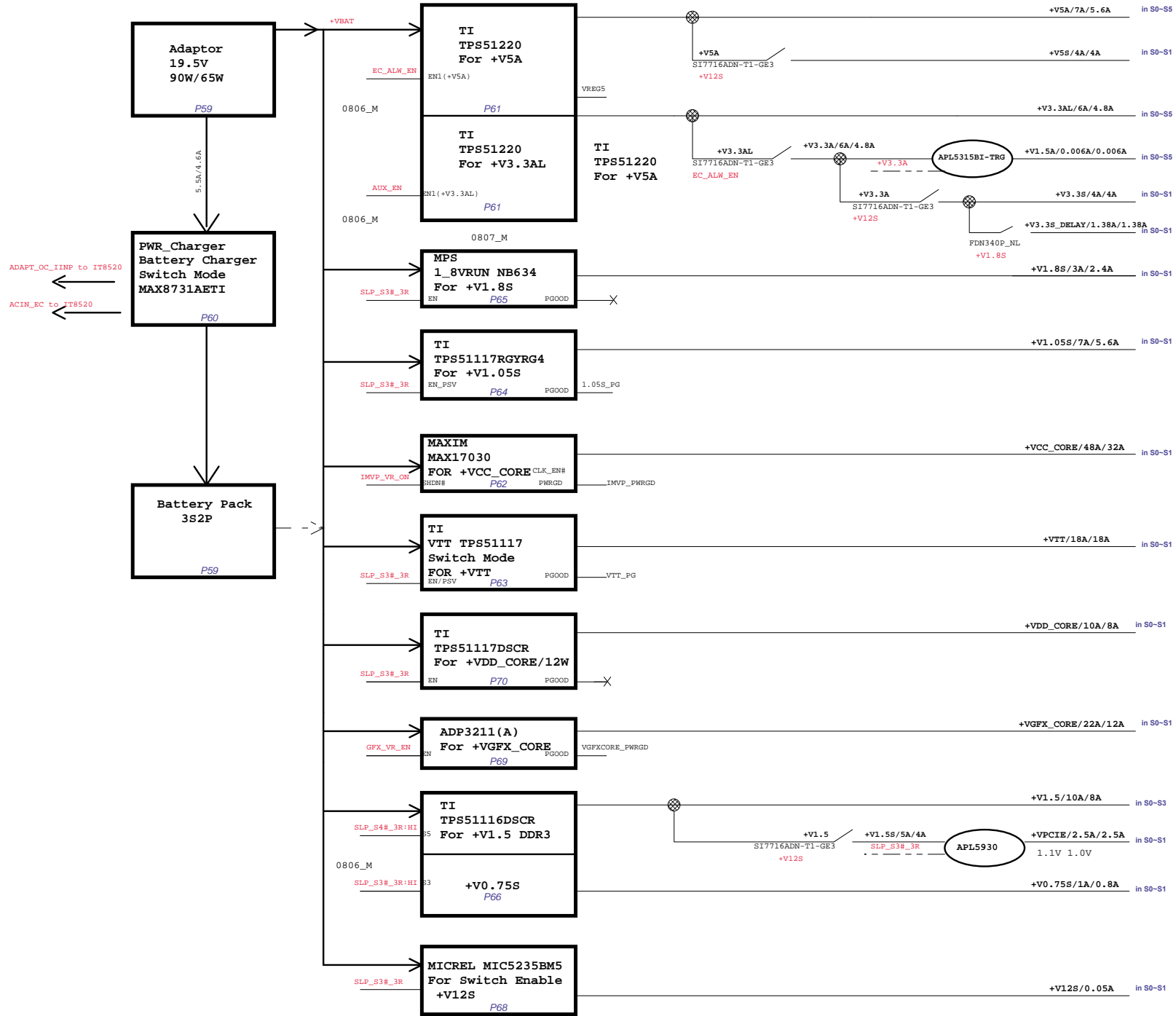
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
**Foxconn eMS Inc.**  
 HNBD R&D phone: +886-2-2799-6111

Title **Index Page**

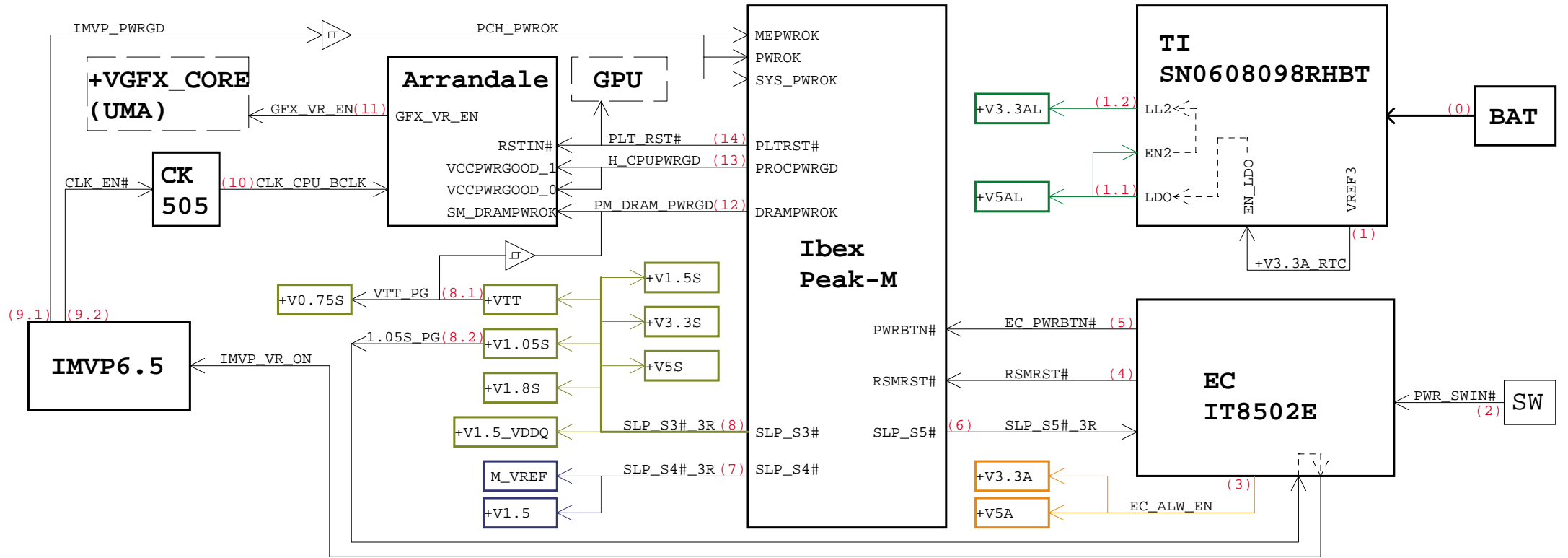
Size	Document Number	Rev
Custom	<b>STAR (Federer)</b>	<b>0.4</b>







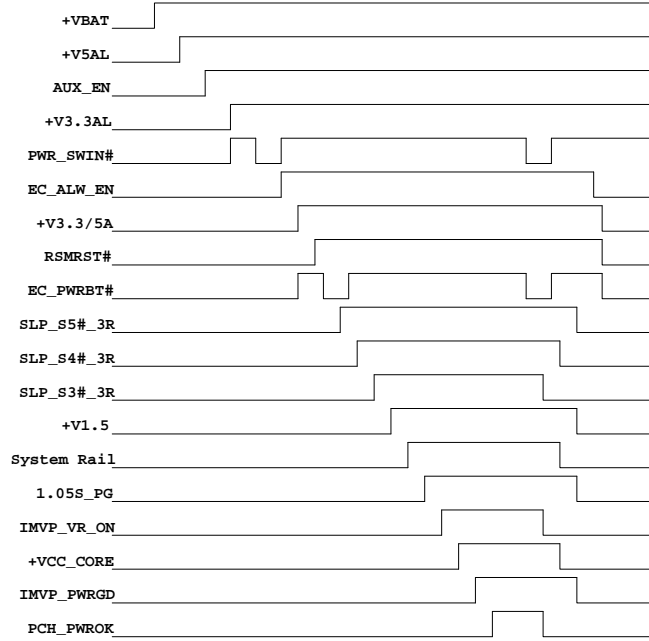
# POWER SEQUENCY DIAGRAM



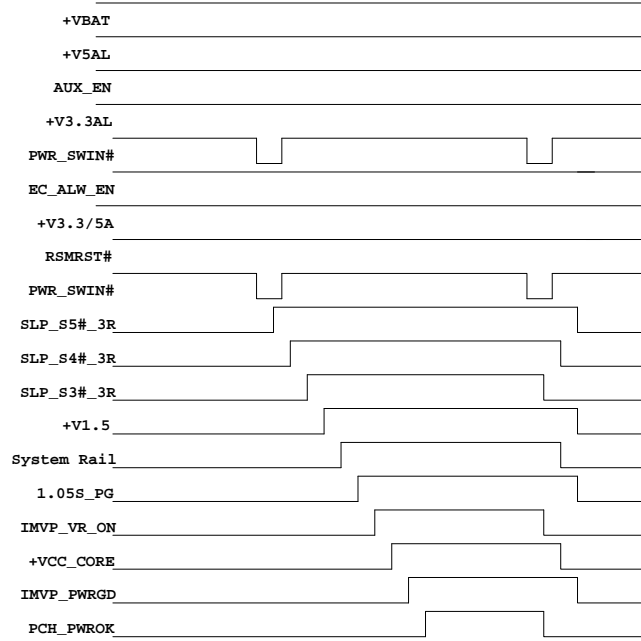
Source Rail	EN	PG	Power Status				Remark
			S0	S3	AC S4/S5	DC S4/S5	
+VBAT			V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC	V	V	V	V	
+V3.3AL	+VBAT	+V5AL	V	V	V	V	
+V5A	+VBAT	EC_ALW_EN	V	V	V	V	
+V3.3A	+V3.3AL	EC_ALW_EN	V	V	V	V	
+V1.5	+VBAT	SLP_S4#_3R	V	V			
+V0.75S	+V1.5	VTT_PG	V				
+V1.5S	+V1.5	RUN_ON_LOAD	V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD	V				
+VCC_CORE	+VBAT	IMVP_VR_ON	V				
+VTT	+VBAT	SLP_S3#_3R	V				
+VGFX_CORE	+VBAT	GFX_VR_EN	V				
+V1.8S	+VBAT	SLP_S3#_3R	V				
+V1.05S	+VBAT	SLP_S3#_3R	V	1.05S_PG			
+V5S	+V5A	RUN_ON_LOAD	V				
+V3.3S	+V3.3A	RUN_ON_LOAD	V				
+VDD_CORE	+VBAT	SLP_S3#_3R	V				
+V3.3S_Delay	+V3.3S	+V1.8S	V				
+VPCIE	+V1.5S	SLP_S3#_3R	V				

# POWER SEQUENCE TIMING

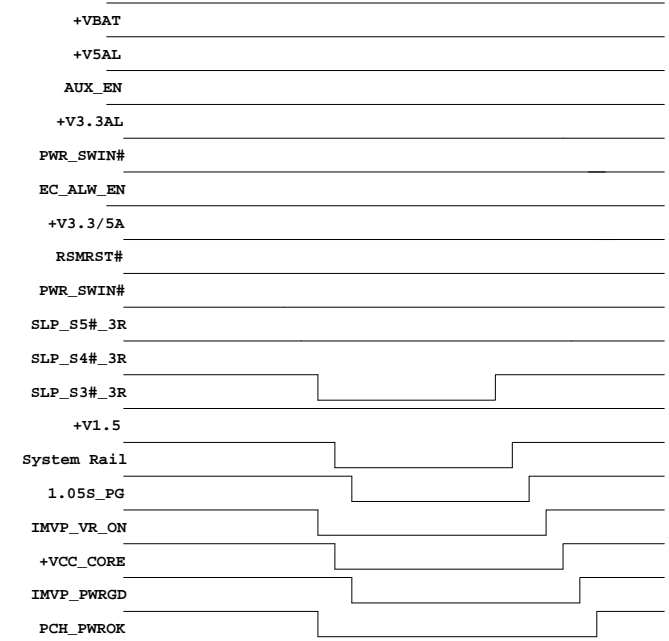
## G3(OFF)->S0->S5



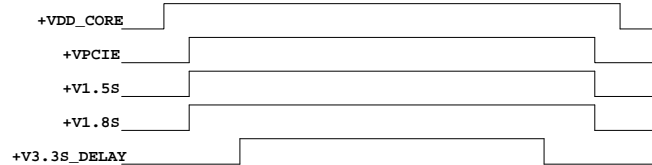
## S5->S0->S5



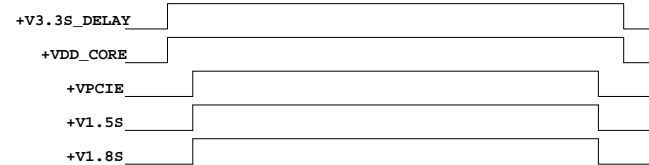
## S0->S3->S0



## M93 Sequence

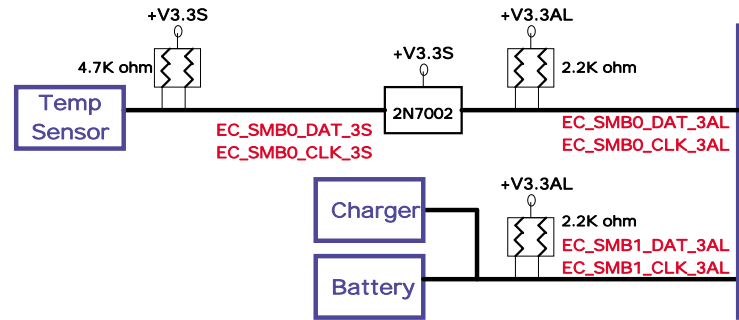
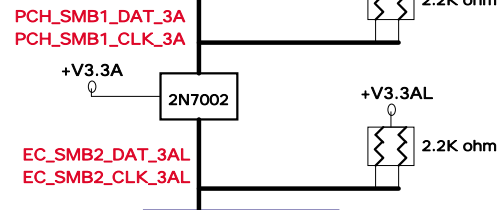
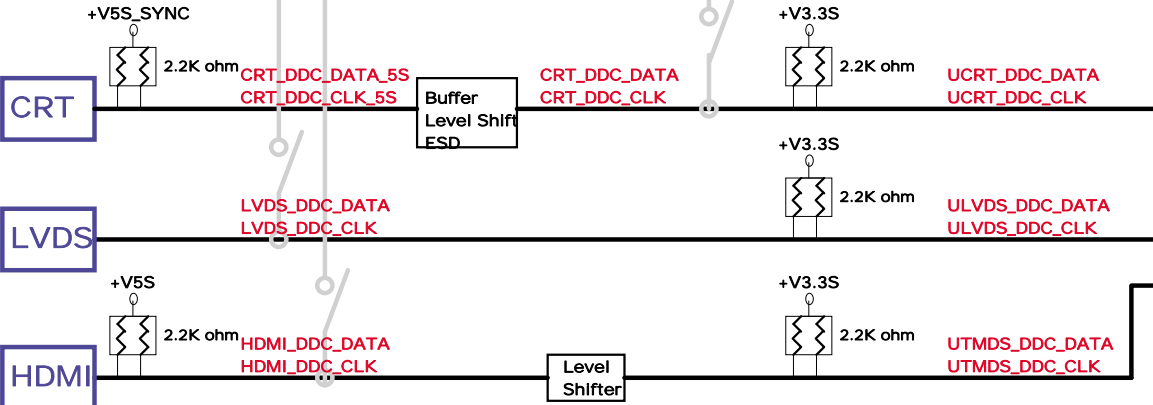
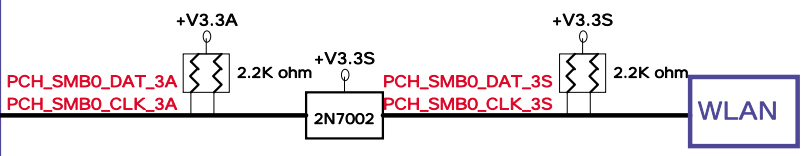
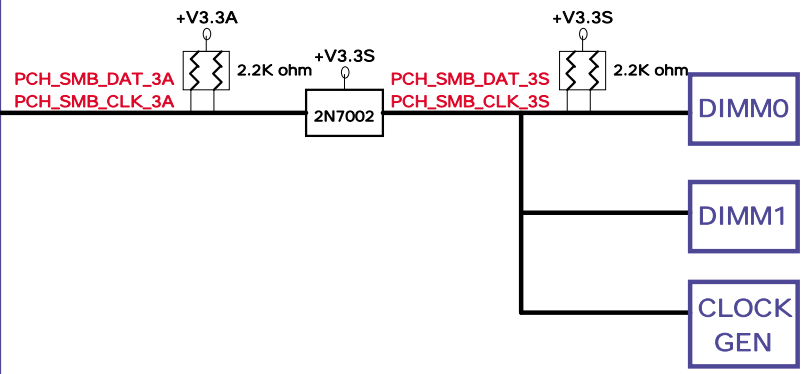
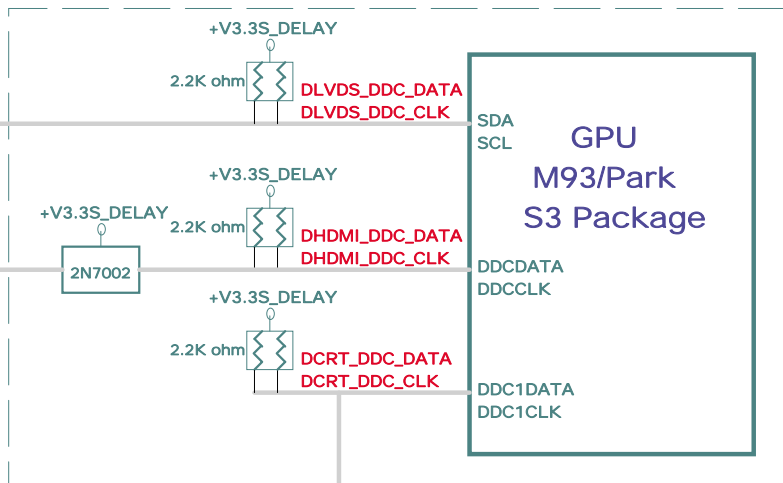


## Park Sequence




# SMBUS&I2C MAP

Discrete GPU



# RESET SIGNAL MAP

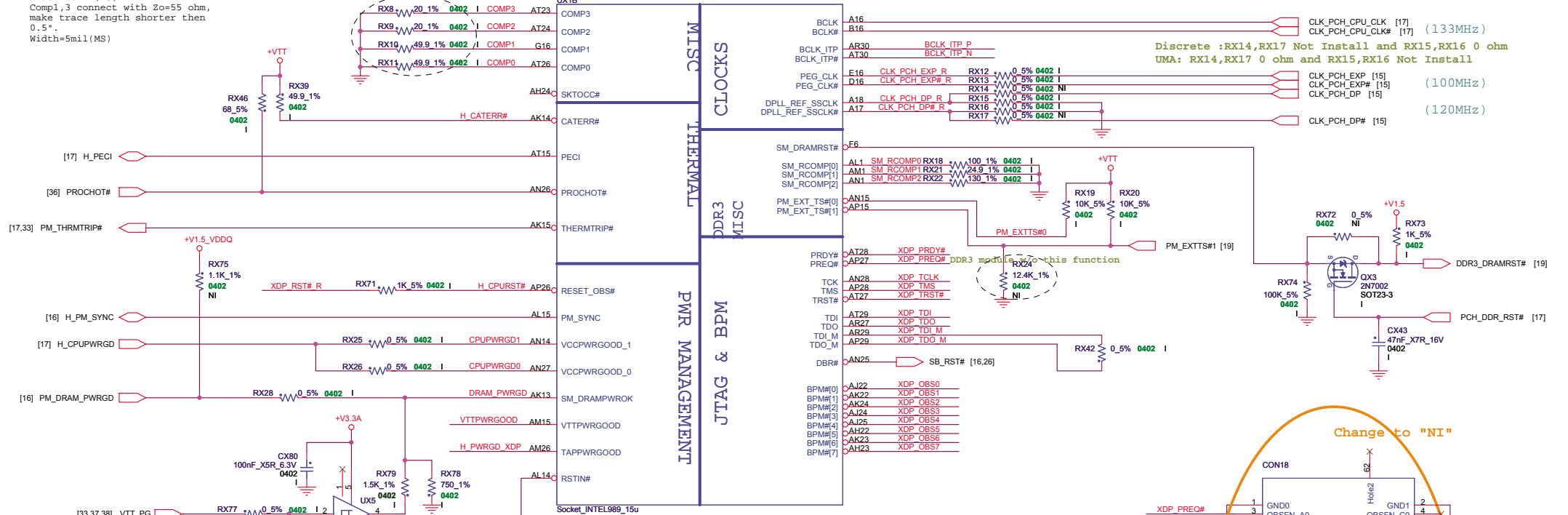
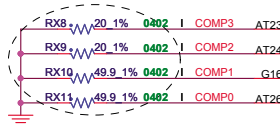
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title			
<b>RESET SIGNAL MAP</b>			
Size	Document Number		Rev
Custom	<b>STAR (Federer)</b>		<b>0.4</b>
Page Modified: Tuesday, December 29, 2009 12:59:41 (UTC/GMT) Sheet 8 of 41			



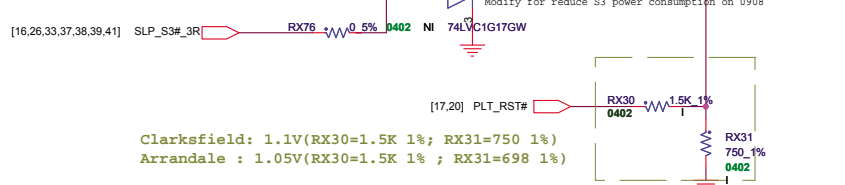
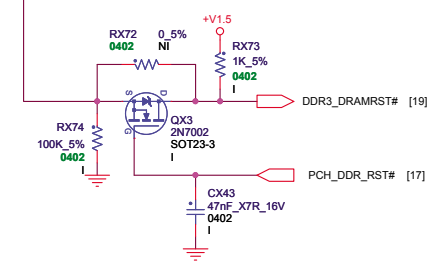
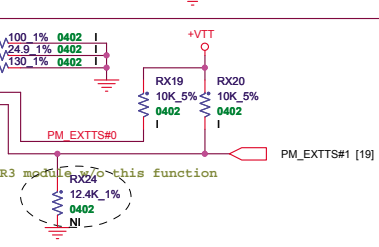


Layout Note:  
 Comp0,2 connect with Zo=27.4 ohm,  
 make trace length shorter then  
 0.5".  
 Width=20mil(MS)  
 Comp1,3 connect with Zo=55 ohm,  
 make trace length shorter then  
 0.5".  
 Width=5mil(MS)

Place close to chip

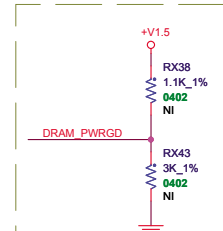
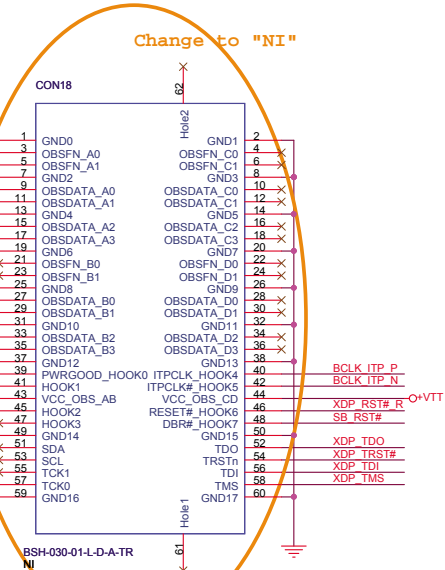
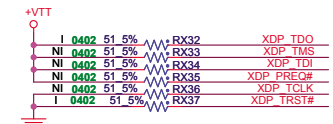


Discrete :RX14,RX17 Not Install and RX15,RX16 0 ohm  
 UMA :RX14,RX17 0 ohm and RX15,RX16 Not Install

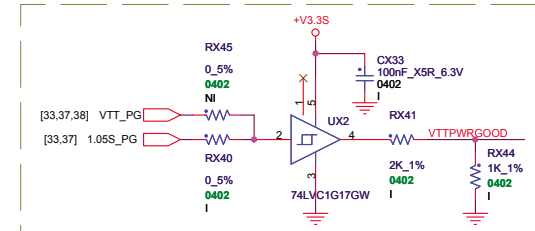


Clarksfield: 1.1V(RX30=1.5K 1%; RX31=750 1%)  
 Arrandale : 1.05V(RX30=1.5K 1% ; RX31=698 1%)

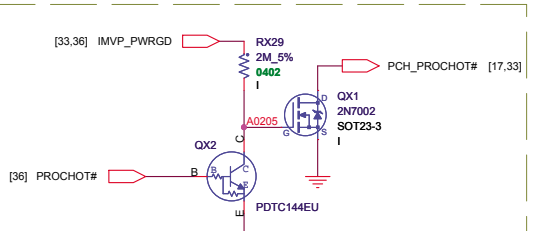
TCK 50 PD  
 TMS 2k~5k PU  
 TRST 2k~5k PU  
 TDI 50 PU  
 TDO unconnect  
 TDI\_M 50 PU  
 TDO\_M unconnect



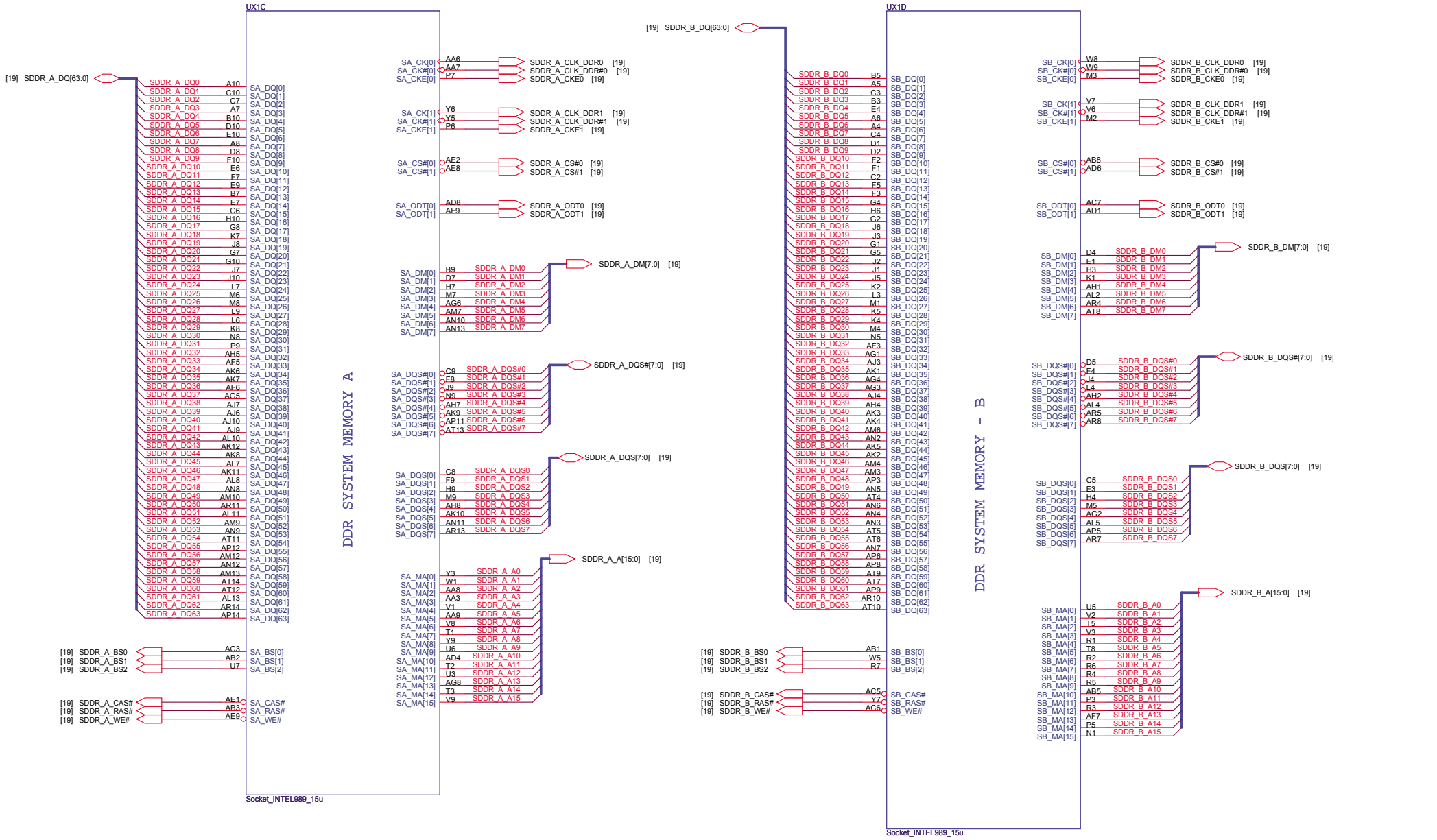
Clarksfield: 1.1V(RX38=1.1K 1%; RX43=3.01K 1%)  
 Arrandale : 1.05V(RX38=1.1K 1% ; R43=2.61K 1%)



Clarksfield: 1.1V(RX41=2K 1%; RX44=1K 1%)  
 Arrandale : 1.05V(RX41=2K 1% ; R44=931ohm 1%)



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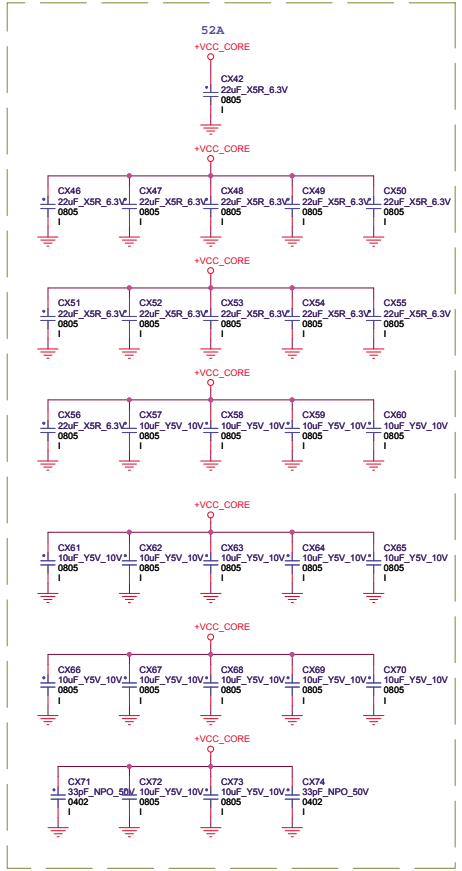


Socket\_INTEL989\_15u

Socket\_INTEL989\_15u

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<b>Foxconn eMS Inc.</b>		phone: +886-2-2799-6111	
HNBD R&D			
<b>Title</b>			
<b>Calpella (DDR3)</b>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	
Custom	<b>STAR (Federer)</b>	<b>0.4</b>	
Page Modified: Tuesday, December 29, 2009 12:02:38 (UTC/GMT) Sheet 11 of 41			

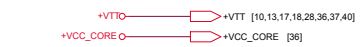
FOR VCC:  
 12x 0805 22 µF inside cavity,  
 7x 0805 10 µF under cavity and 9 x 0805 10 µF  
 between inductor and socket on top layer



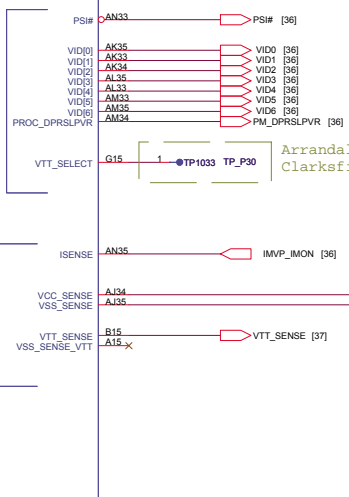
UX1F

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AD35	VCC20
AD34	VCC21
AD33	VCC22
AD32	VCC23
AD31	VCC24
AD30	VCC25
AD29	VCC26
AD28	VCC27
AD27	VCC28
AD26	VCC29
AD25	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U34	VCC71
U33	VCC72
U32	VCC73
U31	VCC74
U30	VCC75
U29	VCC76
U28	VCC77
U27	VCC78
U26	VCC79
U25	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

Socket\_INTEL989\_15u



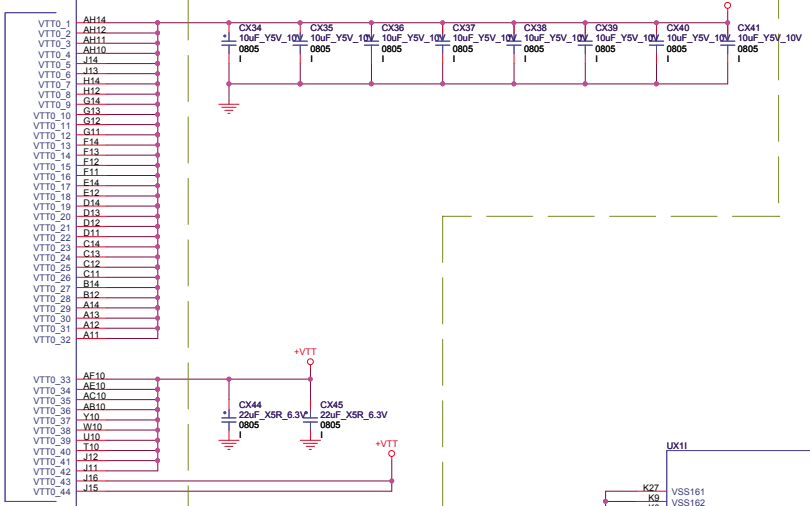
1. 1V RAIL POWER  
 CPU VIDS  
 SENSE LINES



Arrandale drives this pin High  
 Clarkfield drives this pin Low.

Place close to CPU

FOR VTT:  
 7x 0805 22 µF under  
 cavity  
 8x 0805 10 µF edge caps



UX11

K27	VSS161
K6	VSS162
K9	VSS163
K3	VSS164
I32	VSS165
J30	VSS166
J19	VSS167
H36	VSS169
H28	VSS170
H32	VSS171
H26	VSS172
H24	VSS173
H22	VSS174
H18	VSS175
H15	VSS176
H13	VSS177
H11	VSS178
H8	VSS179
H5	VSS180
G34	VSS181
G31	VSS183
G20	VSS184
G9	VSS185
G3	VSS186
F27	VSS187
F30	VSS188
F25	VSS189
F22	VSS190
E22	VSS191
E10	VSS192
E16	VSS193
E32	VSS194
E31	VSS195
E29	VSS196
E21	VSS197
E18	VSS199
E13	VSS200
E11	VSS201
E8	VSS202
E4	VSS203
E2	VSS204
D33	VSS205
D30	VSS206
D26	VSS207
D9	VSS208
D6	VSS209
D3	VSS210
C34	VSS211
C32	VSS212
C28	VSS213
C22	VSS214
C24	VSS215
C22	VSS216
C20	VSS217
C19	VSS218
C16	VSS219
B31	VSS220
B25	VSS221
B21	VSS222
B17	VSS223
B13	VSS224
B11	VSS225
B8	VSS226
B6	VSS227
B4	VSS228
B2	VSS229
A20	VSS230
A27	VSS231
A33	VSS232
A9	VSS233

VSS

VSS

VSS

VSS

VSS

VSS

VSS

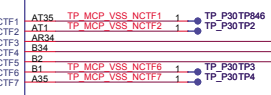
VSS

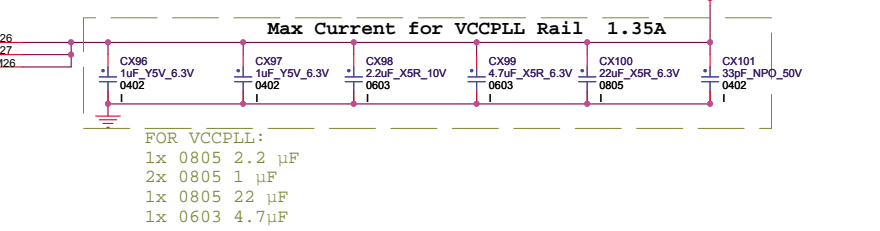
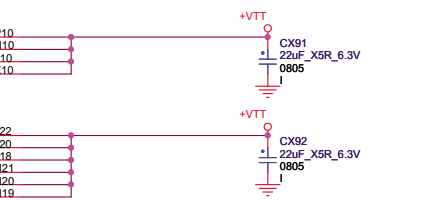
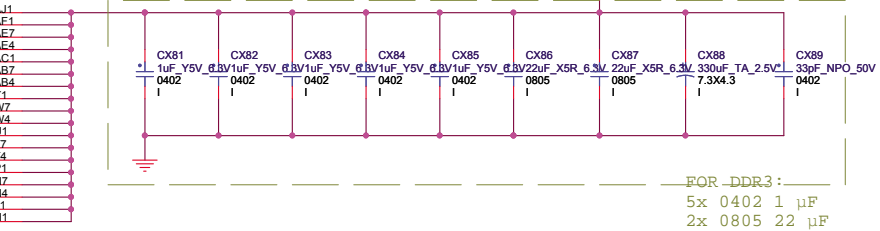
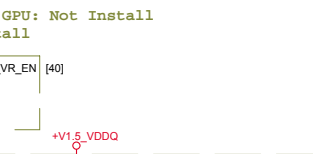
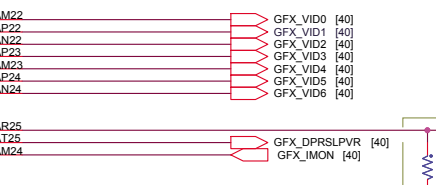
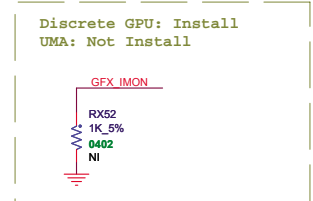
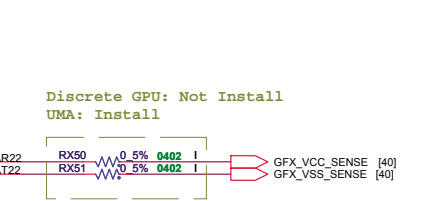
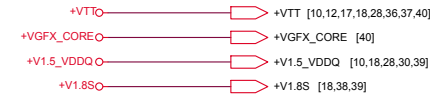
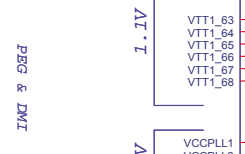
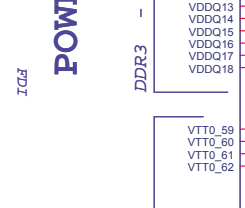
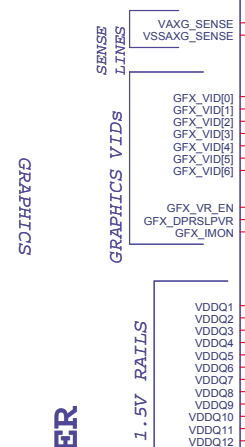
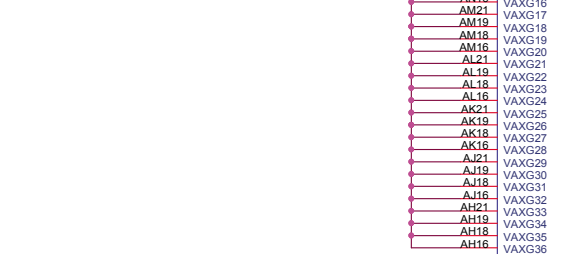
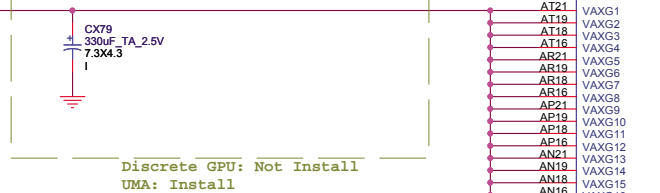
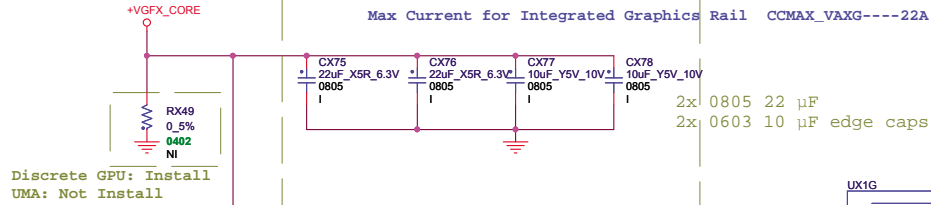
UX1H

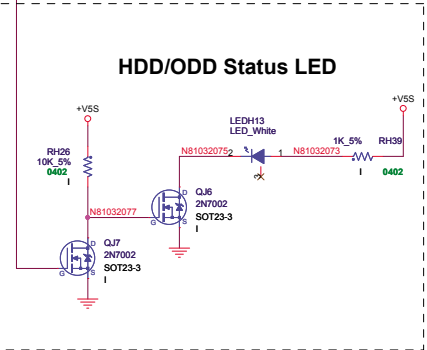
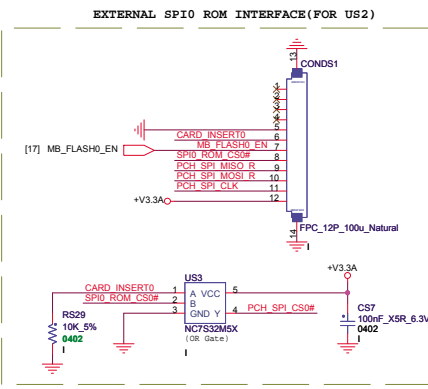
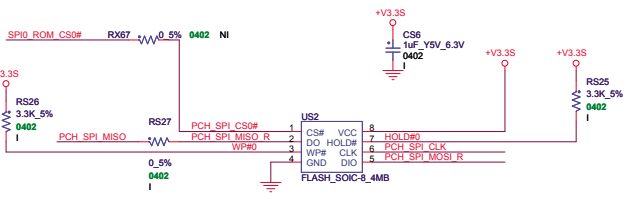
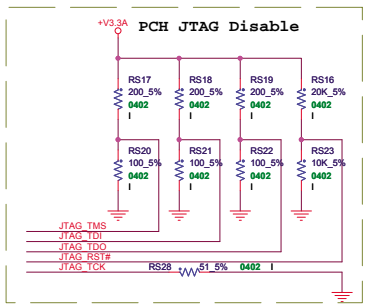
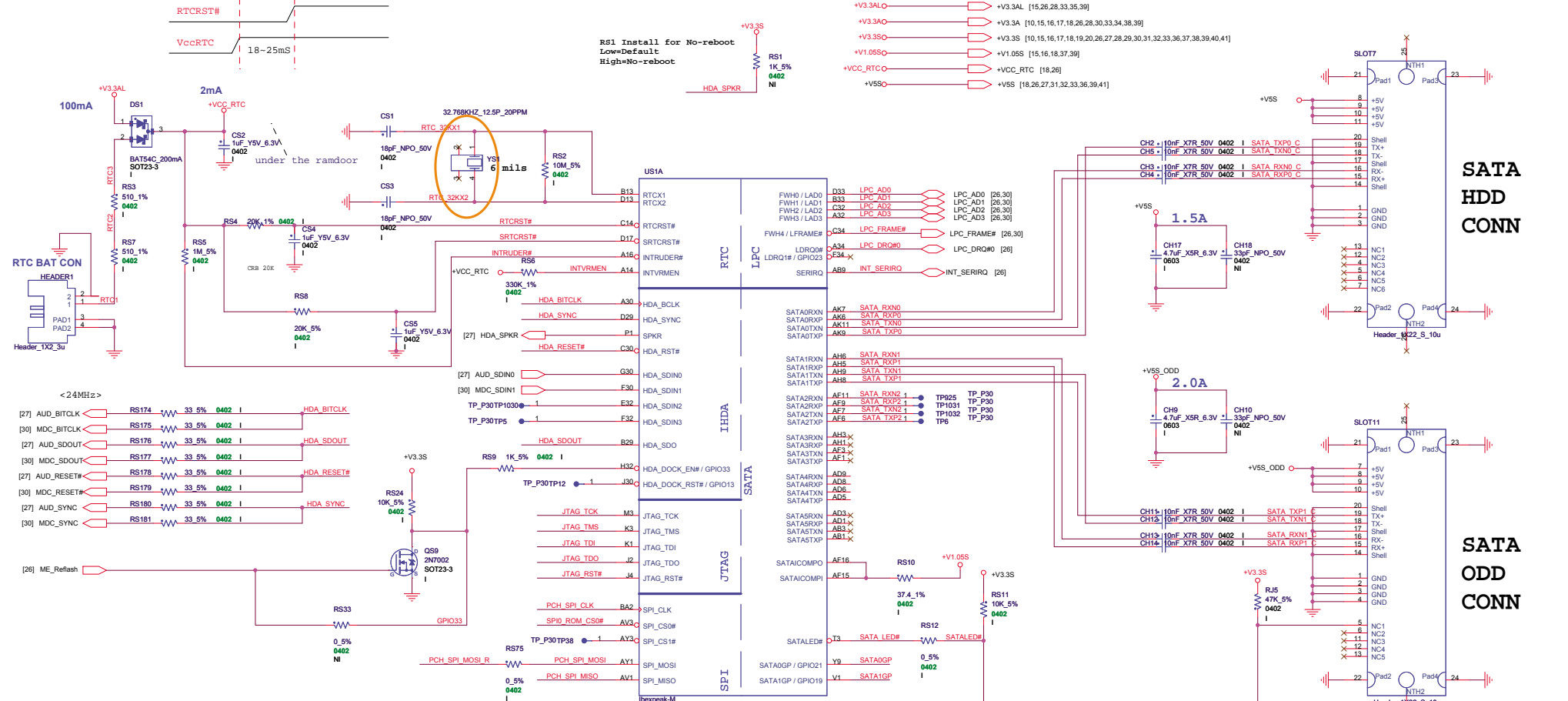
AT20	VSS1	VSS81	AE34
AT17	VSS2	VSS82	AE33
AR01	VSS3	VSS83	AE32
AR28	VSS4	VSS84	AE31
AR04	VSS5	VSS85	AE30
AR23	VSS6	VSS86	AE28
AR17	VSS7	VSS87	AE29
AR20	VSS8	VSS88	AE27
AR12	VSS9	VSS89	AE26
AR15	VSS10	VSS90	AE8
AR09	VSS11	VSS91	AD10
AR6	VSS12	VSS92	AC8
AR3	VSS13	VSS93	AC4
AP20	VSS14	VSS94	AC2
AP17	VSS15	VSS95	AB35
AP13	VSS16	VSS96	AB34
AP10	VSS17	VSS97	AB33
AP7	VSS18	VSS98	AB32
AP4	VSS19	VSS99	AB30
AP2	VSS20	VSS100	AB29
AN34	VSS21	VSS101	AB6
AN31	VSS22	VSS102	AB27
AN24	VSS23	VSS103	AB26
AN20	VSS24	VSS104	AB6
AN17	VSS25	VSS105	AA10
AM29	VSS27	VSS107	X4
AM27	VSS28	VSS108	Y4
AM25	VSS29	VSS109	Y2
AM17	VSS30	VSS110	W35
AM14	VSS31	VSS111	W34
AM11	VSS32	VSS112	W33
AM8	VSS33	VSS113	W32
AM5	VSS35	VSS115	W20
AM2	VSS36	VSS116	W29
AL31	VSS38	VSS118	W26
AL23	VSS39	VSS119	W6
AL20	VSS40	VSS120	W8
AL17	VSS41	VSS121	W10
AL12	VSS42	VSS122	L8
AL9	VSS43	VSS123	L2
AL6	VSS44	VSS124	L2
AL3	VSS46	VSS126	L35
AK26	VSS47	VSS127	L33
AK27	VSS48	VSS128	L34
AK25	VSS49	VSS129	L32
AK20	VSS50	VSS130	L31
AK17	VSS51	VSS131	L30
AJ31	VSS52	VSS132	L29
AJ23	VSS53	VSS133	L27
AJ20	VSS54	VSS134	L26
AJ17	VSS55	VSS135	L6
AJ14	VSS56	VSS136	R10
AJ11	VSS57	VSS137	P4
AJ8	VSS58	VSS138	P2
AJ2	VSS59	VSS139	N5
AH35	VSS60	VSS140	N4
AH34	VSS61	VSS141	N32
AH32	VSS62	VSS142	N33
AH31	VSS63	VSS143	N31
AH30	VSS64	VSS144	N30
AH29	VSS65	VSS145	N29
AH28	VSS66	VSS146	N28
AH27	VSS67	VSS147	N27
AH26	VSS68	VSS148	N26
AH25	VSS69	VSS149	N6
AH20	VSS70	VSS150	M10
AH17	VSS71	VSS151	L35
AH13	VSS72	VSS152	L33
AH8	VSS73	VSS153	L32
AH6	VSS74	VSS154	L29
AH3	VSS75	VSS155	L8
AG10	VSS76	VSS156	L2
AF8	VSS77	VSS157	K34
AF2	VSS78	VSS158	K33
AE8	VSS79	VSS159	K30
AE6	VSS80	VSS160	

VSS

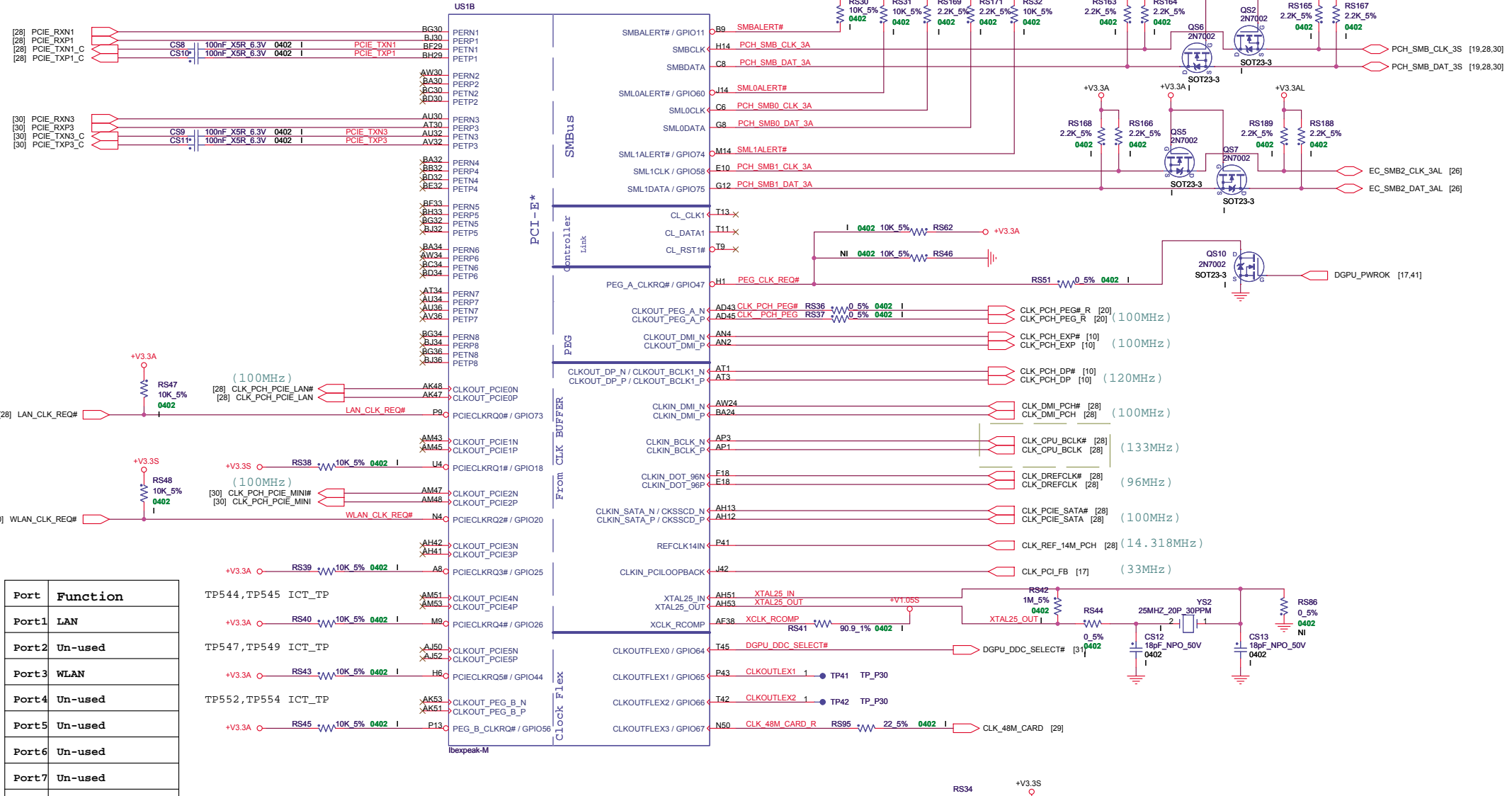
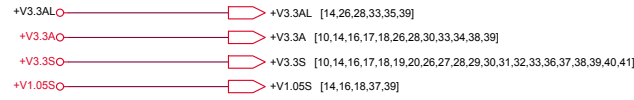
Socket\_INTEL989\_15u







Power pin current max. 1300 mA (less 2ms)

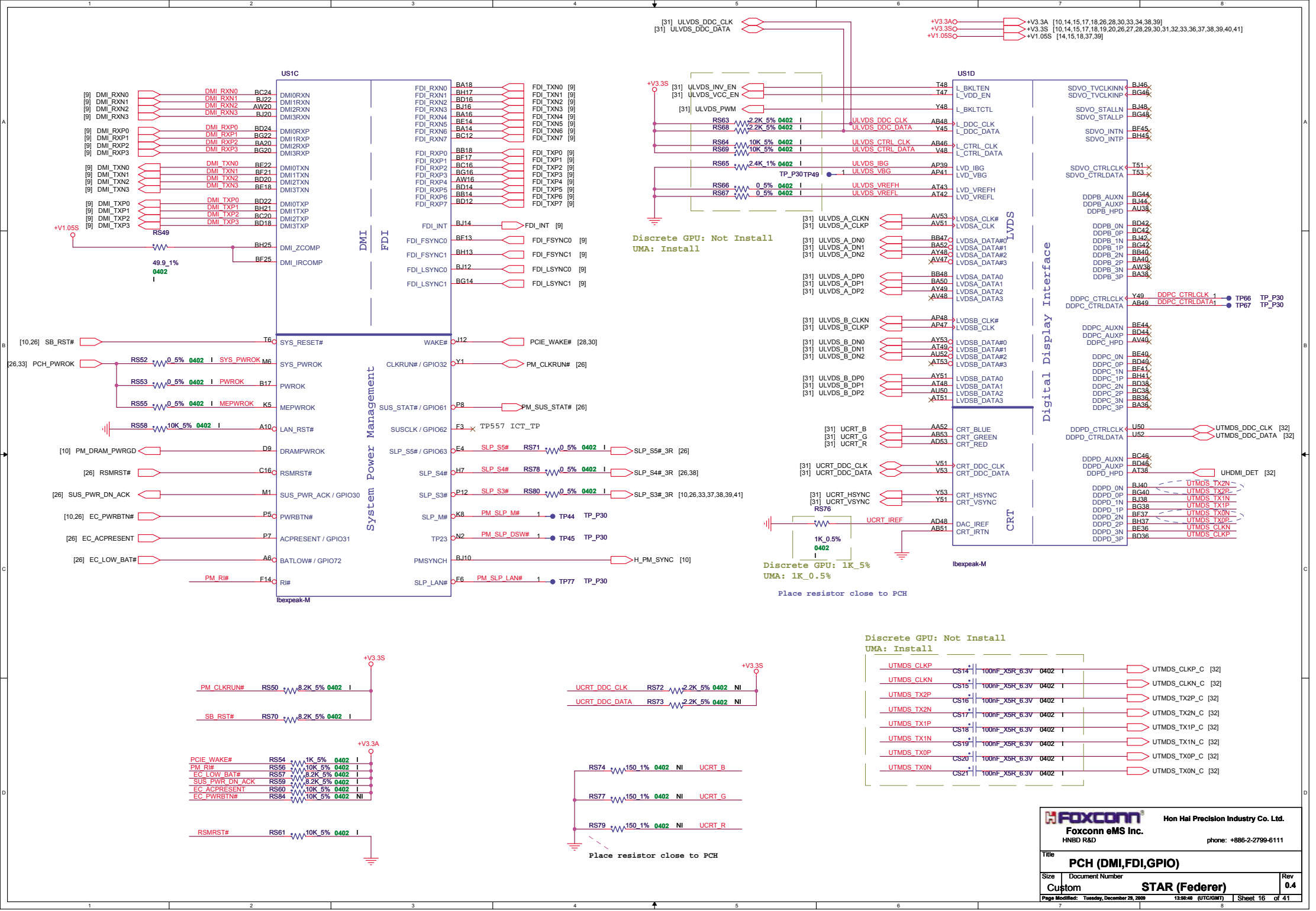


Port	Function
Port1	LAN
Port2	Un-used
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

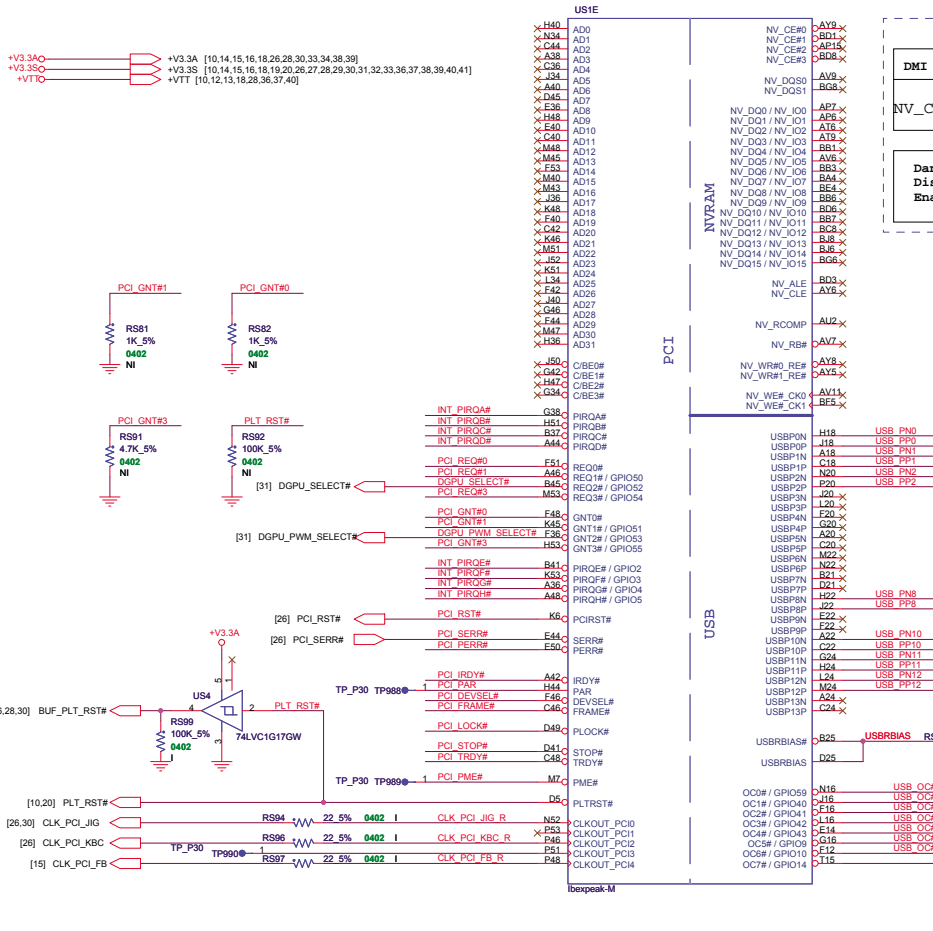
PCI-E Port Table

**FOXCONN**  
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 Hon Hai Precision Industry Co. Ltd.  
 phone: +886-2-2799-6111

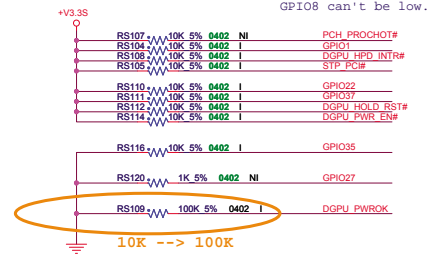
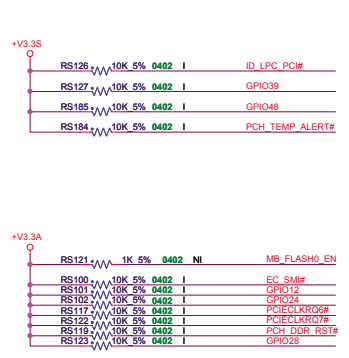
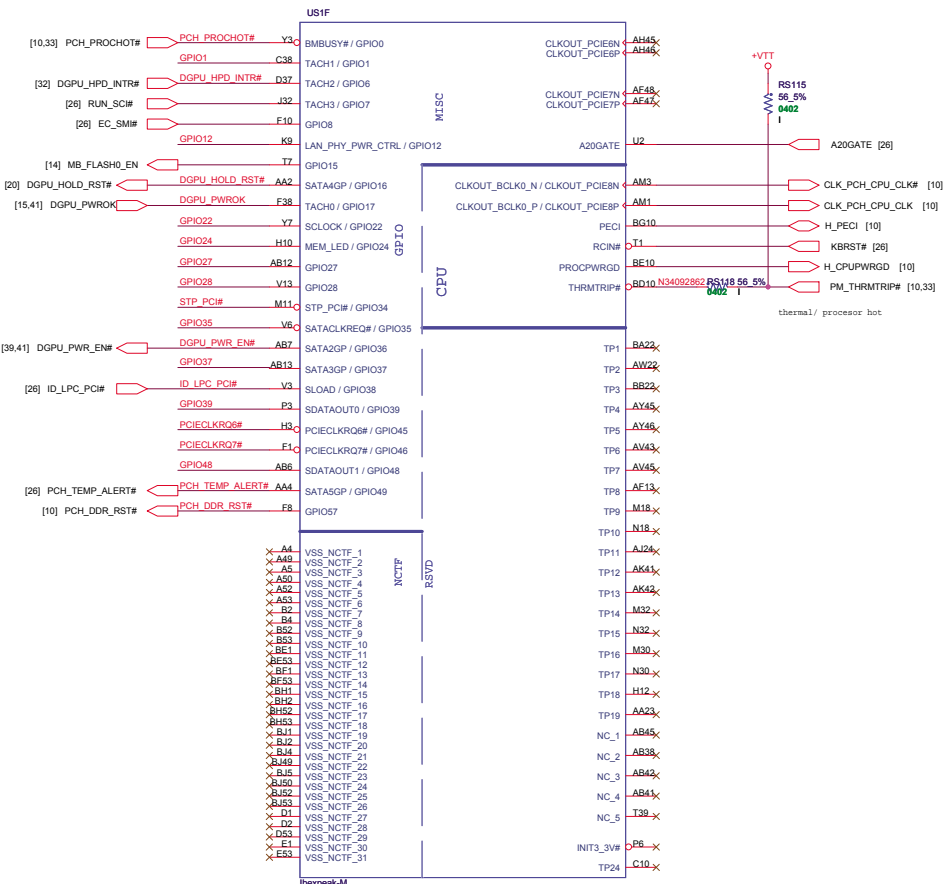
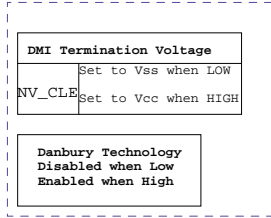
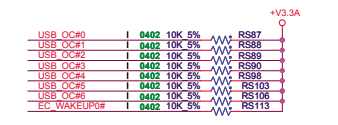
Title: **PCH (PCI-E,SMBUS,CLK)**  
 Size: Document Number  
 Custom: **STAR (Federer)**  
 Rev: **0.4**  
 Page Modified: Tuesday, December 29, 2009 12:59:40 (UTC/GMT) Sheet 15 of 41







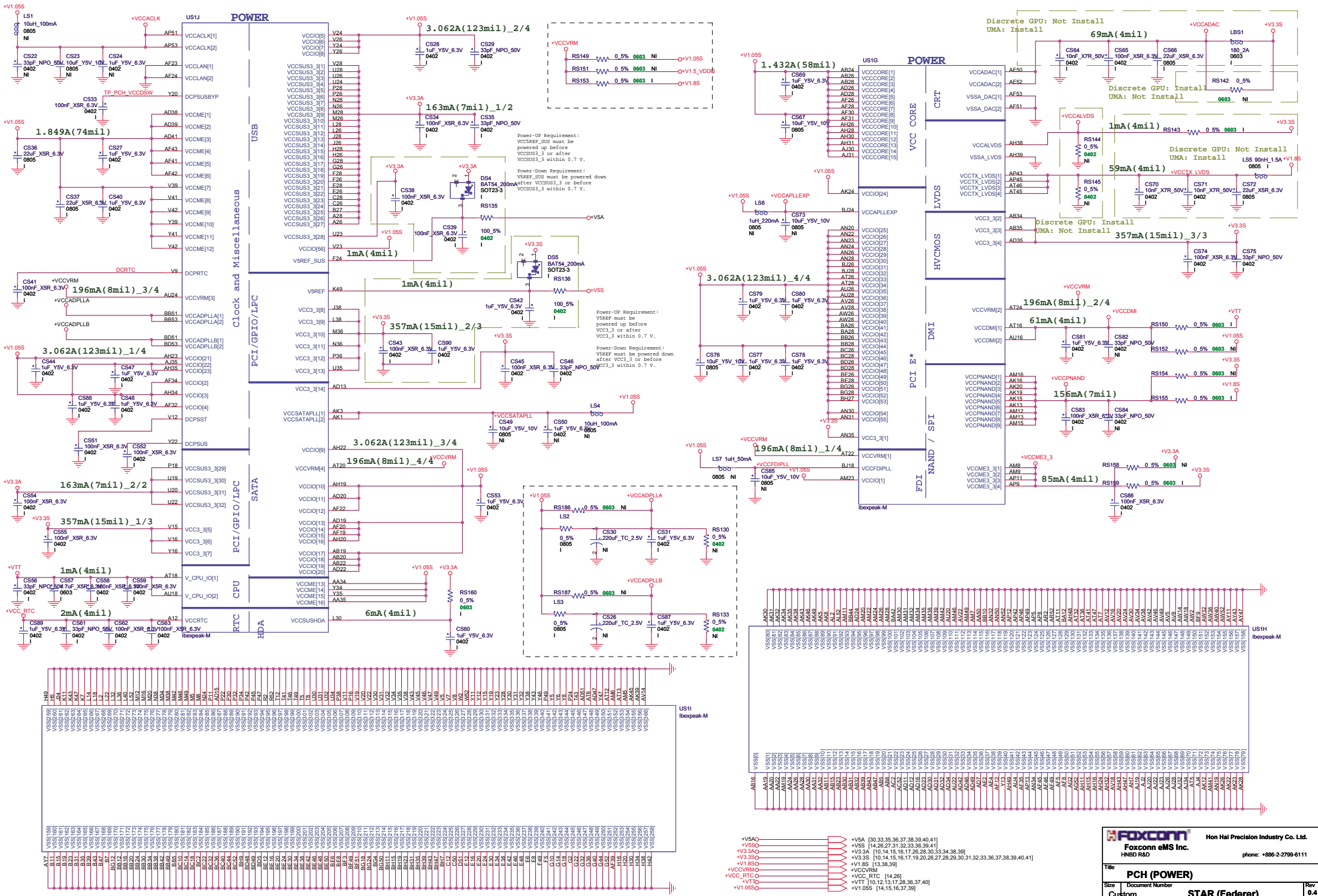
USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8	Bluetooth	
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12	Card reader	
PORT-13		



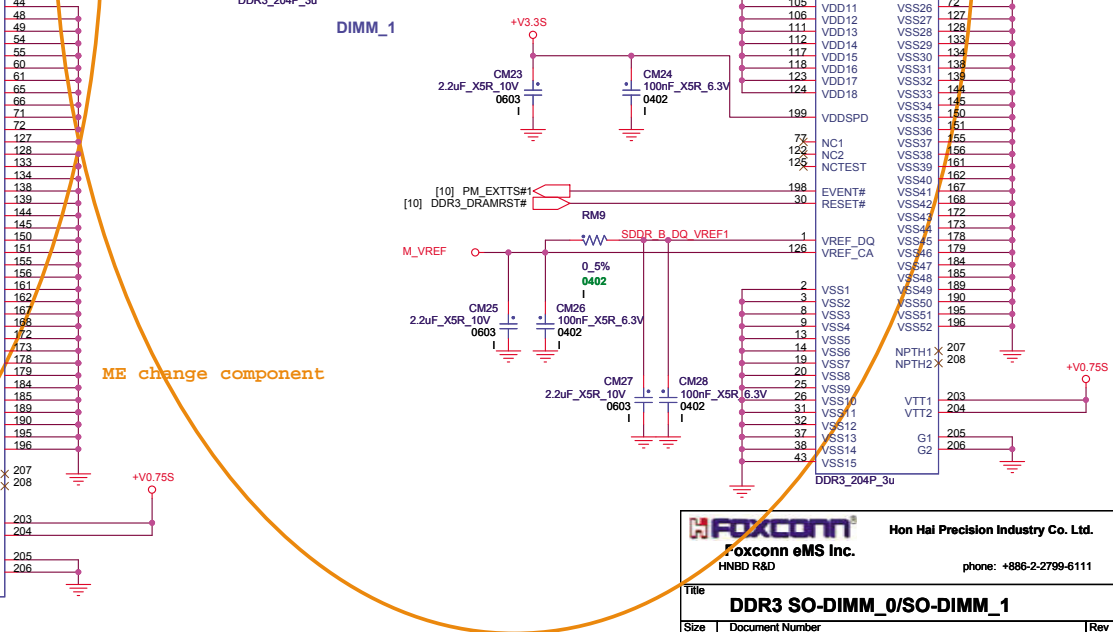
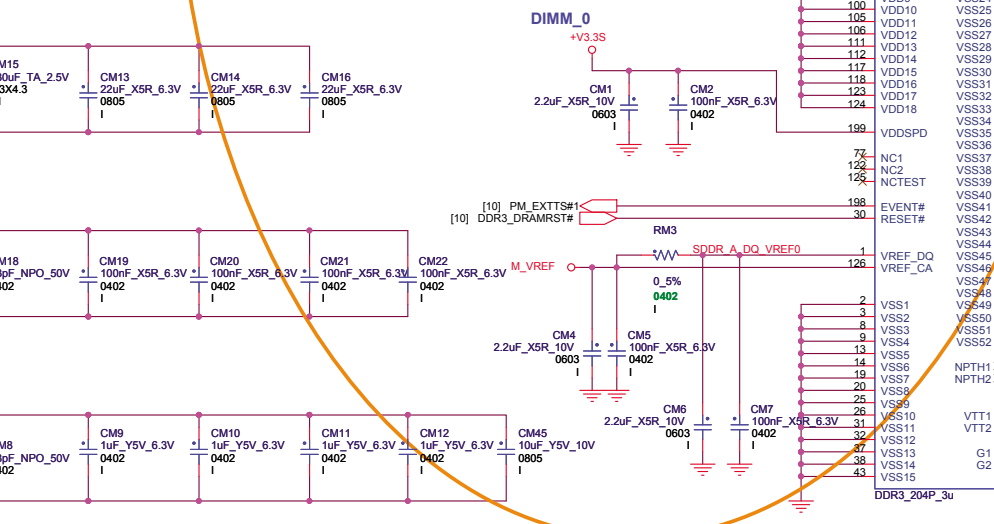
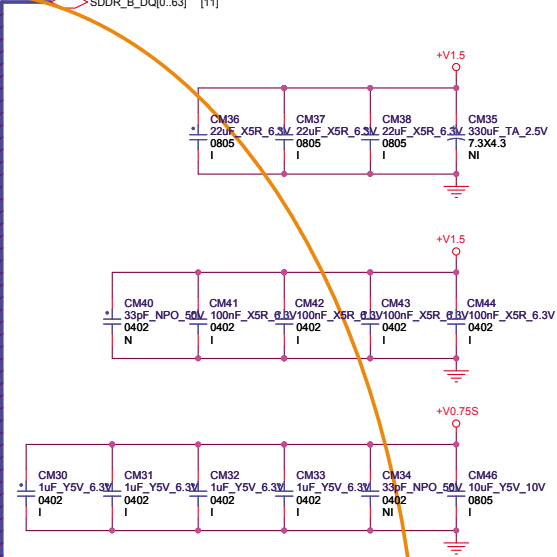
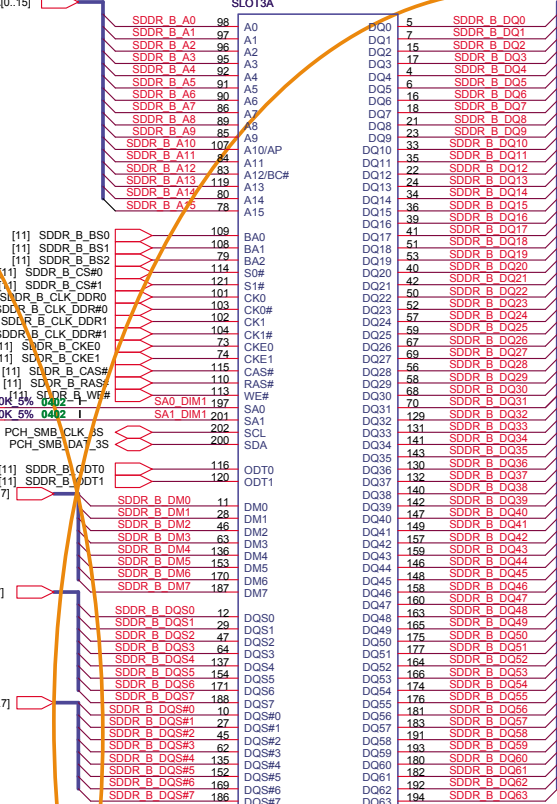
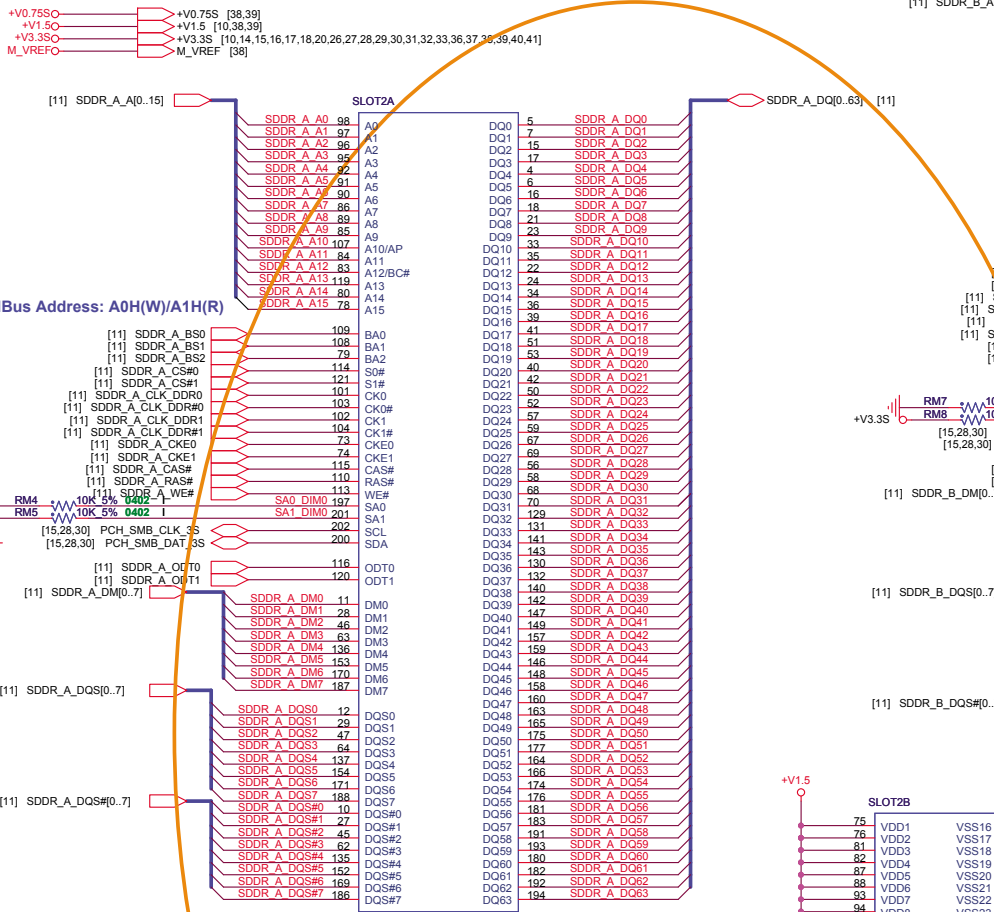
DVT Ask EC if we need to change GPIO pin.  
GPIO8 can't be low.

**10K --> 100K**

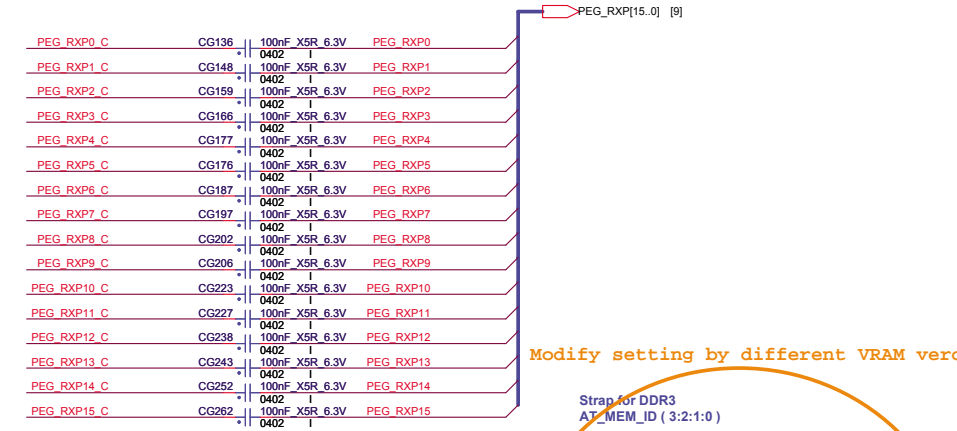
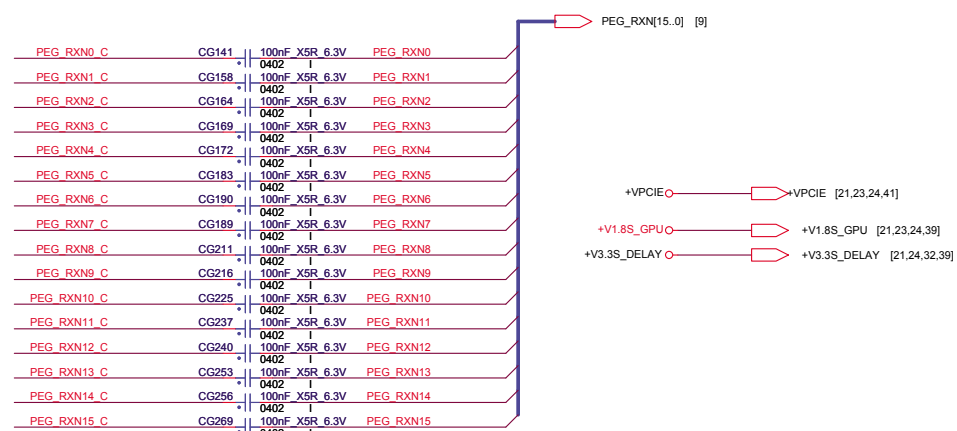
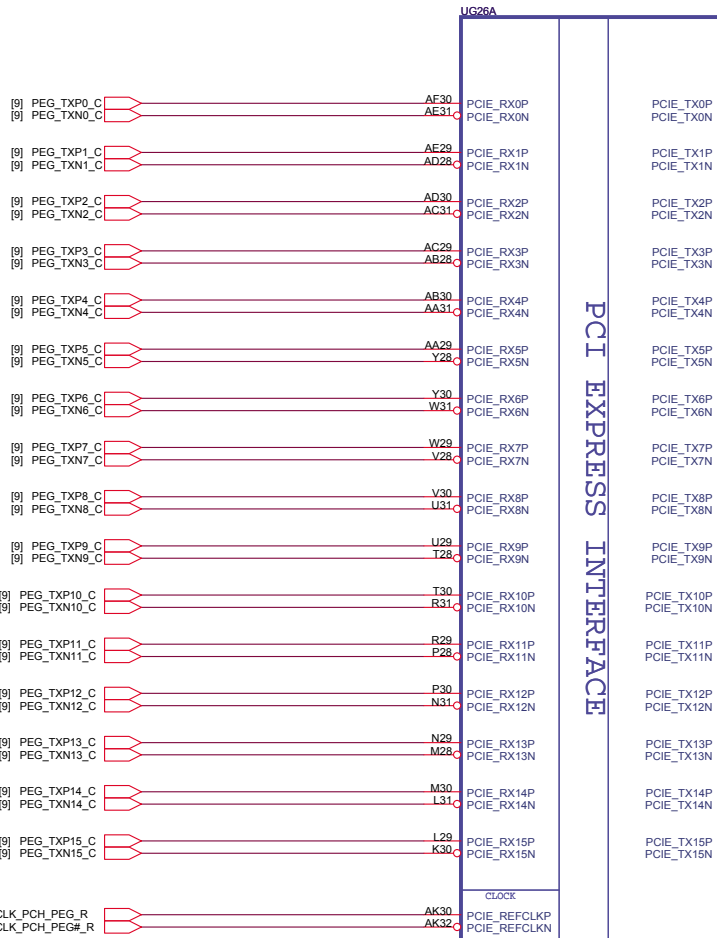
<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		phone: +886-2-2799-6111	
HNB0 R&D			
Title: <b>PCH (PCI,USB,NVRAM,GPIO)</b>			
Size	Document Number	Rev	0.4
Custom		STAR (Federor)	
Page Modified: Tuesday, December 23, 2009 11:26:41 AM (UTC+08:00)   Sheet 17 of 41			



- +V5A0 [90,33,35,36,37,38,39,40,41]
- +V5S [14,27,27,31,32,33,38,39,41]
- +V3.3A0 [10,14,15,16,17,26,28,30,33,34,38,39]
- +V3.3S [10,14,15,16,17,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40,41]
- +V1.8S [13,38,39]
- +VCCVCRM [14,26]
- +VCC\_RTC [14,26]
- +VTT [10,12,13,17,28,36,37,40]
- +V1.05S [14,15,16,37,39]



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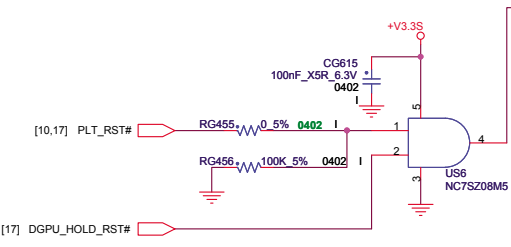


Modify setting by different VRAM vendor

Strap for DDR3  
AT\_MEM\_ID (3:2:1:0)

0000	64Mx16	Samsung (K4W1G1646E-HC12)	512MB
0001	64Mx16	Hynix (H5TQ1G63BFR-12C)	512MB
0010	128Mx16	Samsung (K4W2G1646B-HC12)	1GB
0100	128Mx16	Samsung (K4W2G1646C-HCxx)	1GB
1000	128Mx16	Hynix (H5TQ2G63BFR-12C)	1GB
1001	128Mx16	Micron (MT41J128M16HA-12)	1GB

M93-S3 Not Install  
PARK-S3 Install 10K ohm

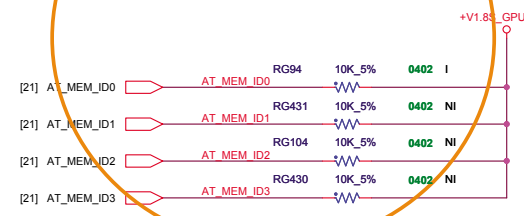
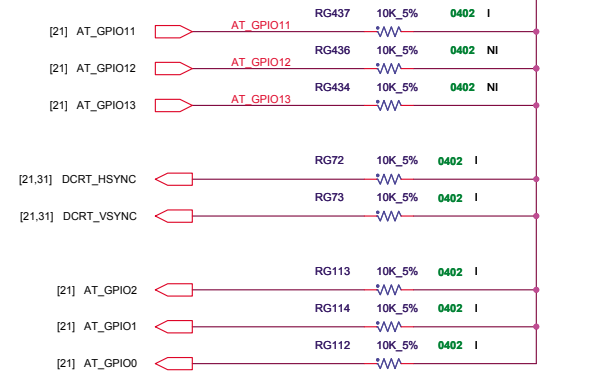


If no ROM attached, GPIO[13:12:11] ; CONFIG(2:0) controls the memory aperture size.

Reserved 011 512MB 001

HSYNC , VSYNC  
AUD[1] , AUD[0]  
0,0 No audio function  
0,1 Audio for DisplayPort and HDMI if dongle is detected  
1,0 Audio for DisplayPort only  
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING  
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED  
GPIO 2 : PCIE GEN2 ENABLED



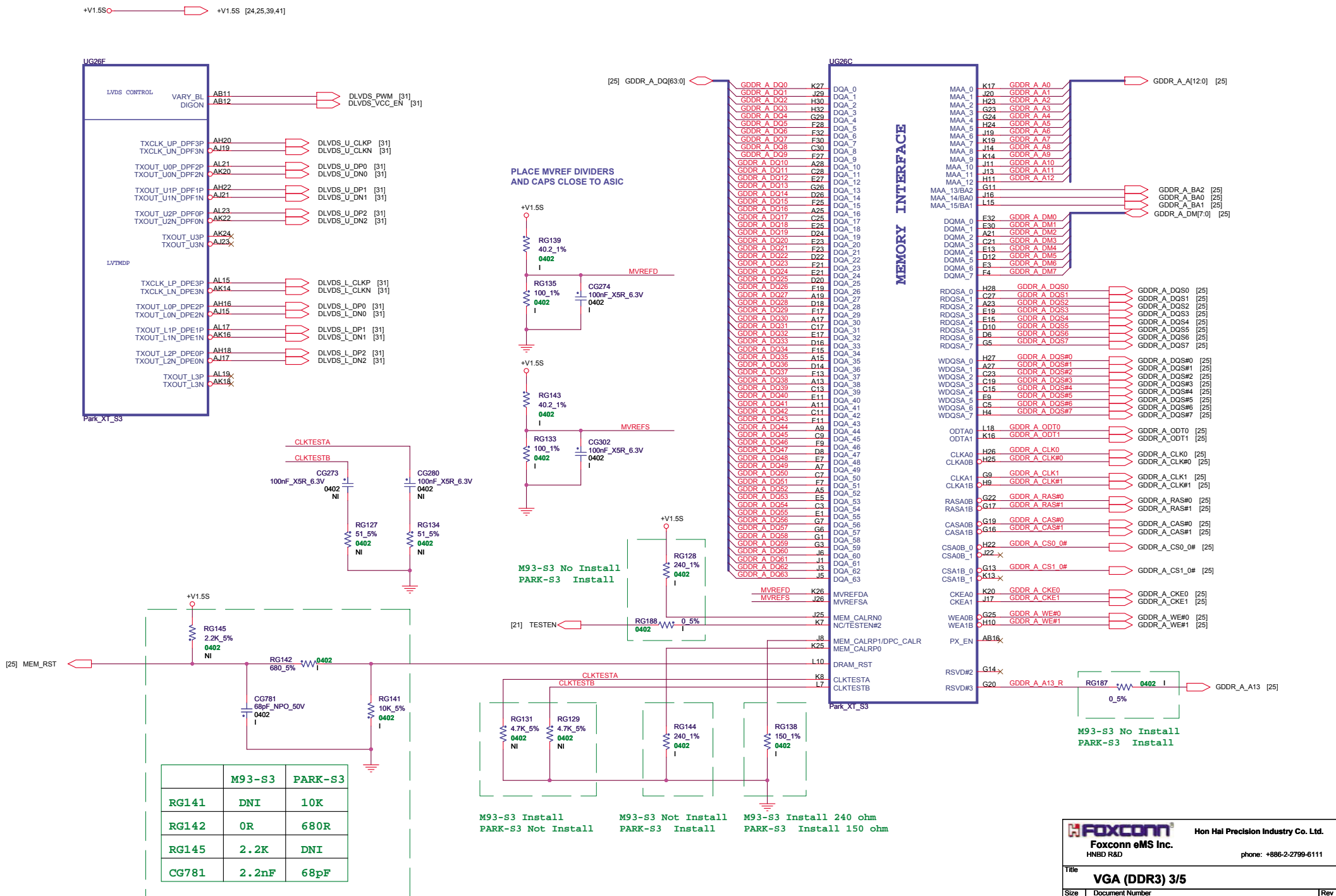
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Title: **VGA (PCI-E/STRAP) 1/5**

Size	Document Number	Rev
Custom	STAR (Federer)	0.4

Page Modified: Tuesday, December 29, 2009 12:59:40 (UTC/GMT) Sheet 20 of 41





	M93-S3	PARK-S3
RG141	DNI	10K
RG142	0R	680R
RG145	2.2K	DNI
CG781	2.2nF	68pF

M93-S3 Install  
PARK-S3 Not Install

M93-S3 Not Install  
PARK-S3 Install

M93-S3 Install 240 ohm  
PARK-S3 Install 150 ohm

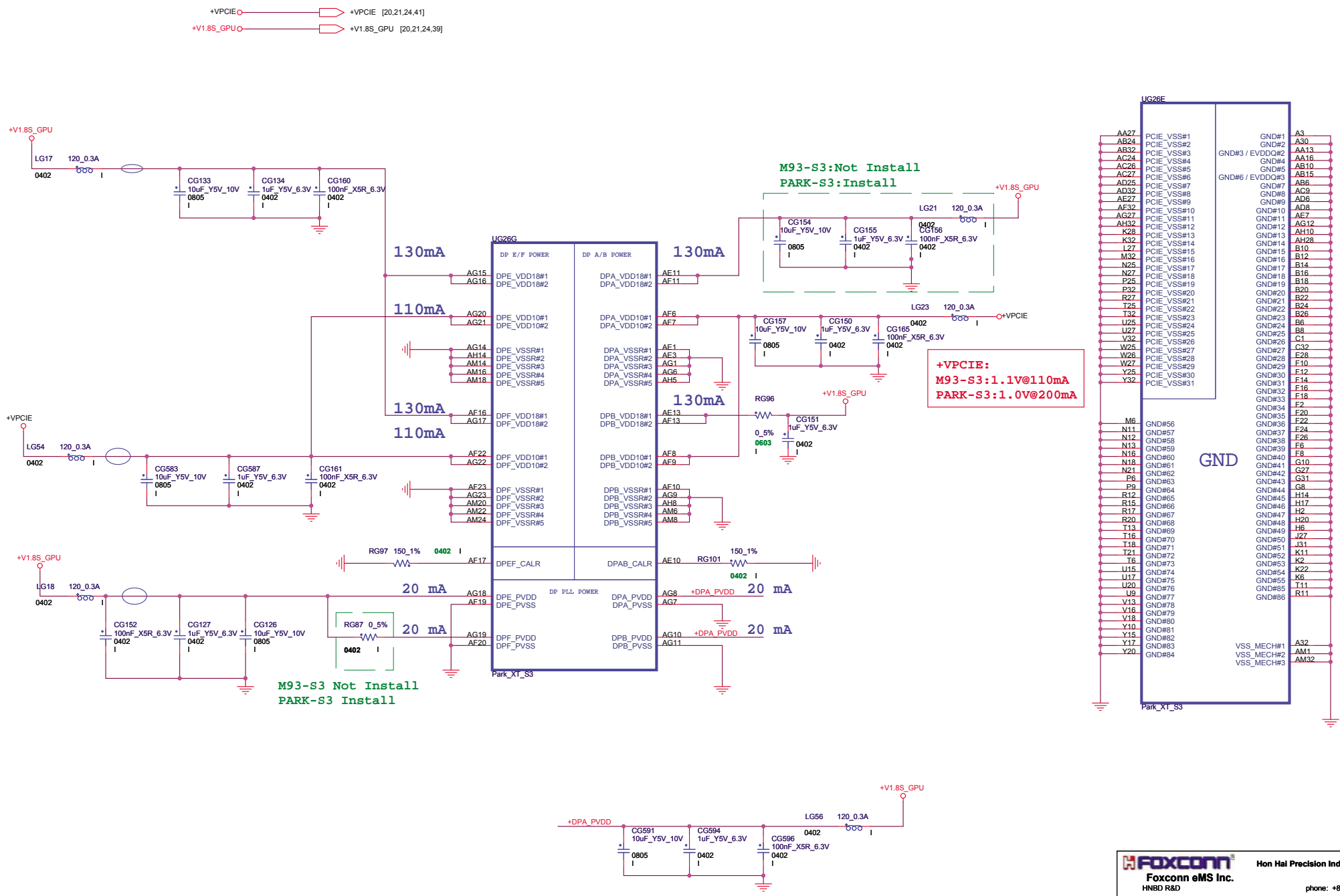
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Title: **VGA (DDR3) 3/5**

Size: Custom Document Number: STAR (Federer) Rev: 0.4

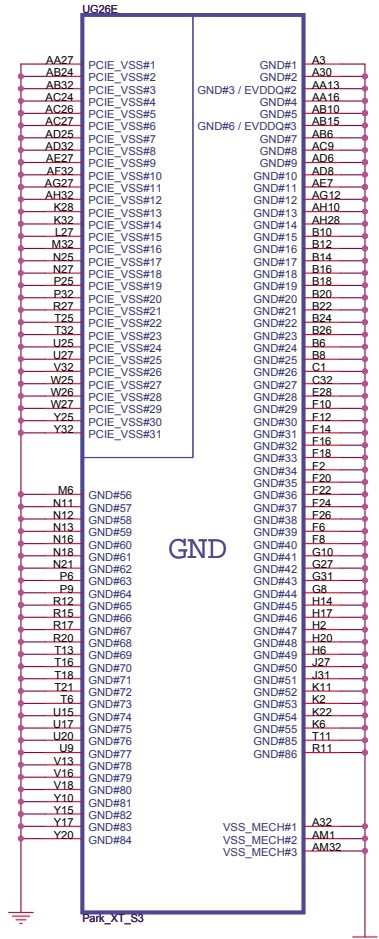
Page Modified: Tuesday, December 29, 2010 12:59:28 (UTC/GMT) | Sheet 22 of 41



**+VPCIE:**  
M93-S3: 1.1V@110mA  
PARK-S3: 1.0V@200mA

M93-S3 Not Install  
PARK-S3 Install

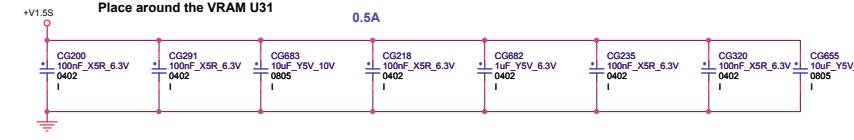
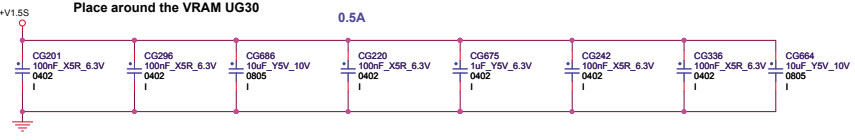
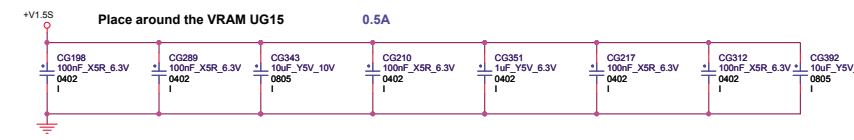
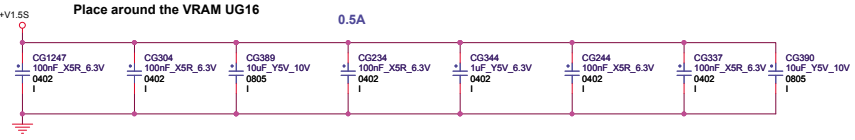
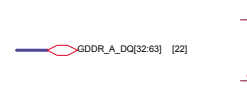
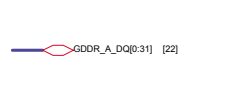
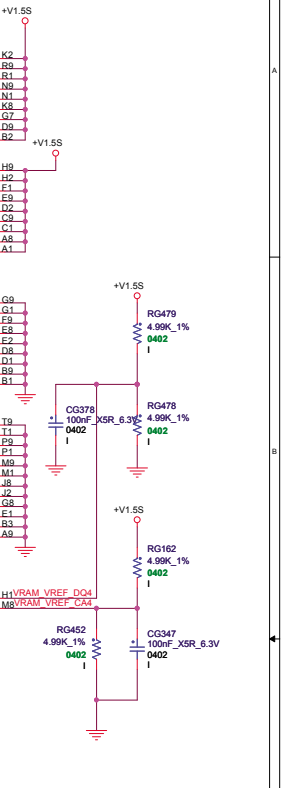
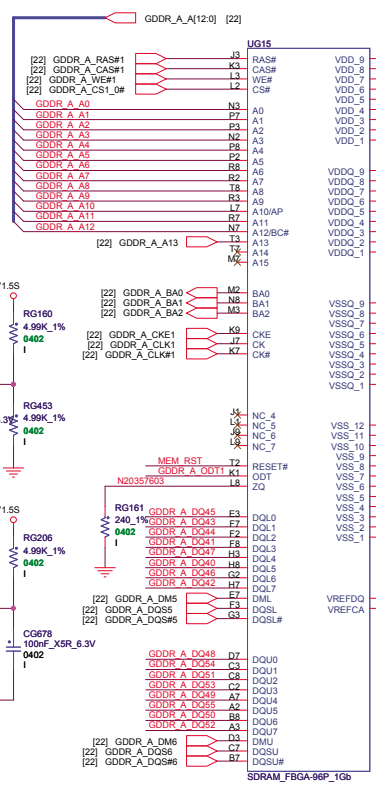
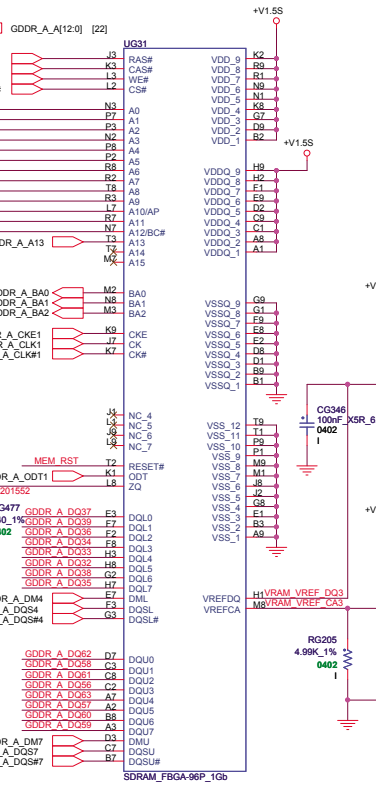
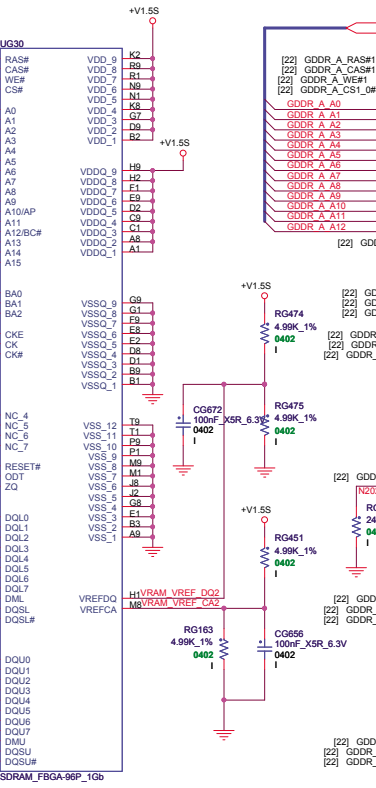
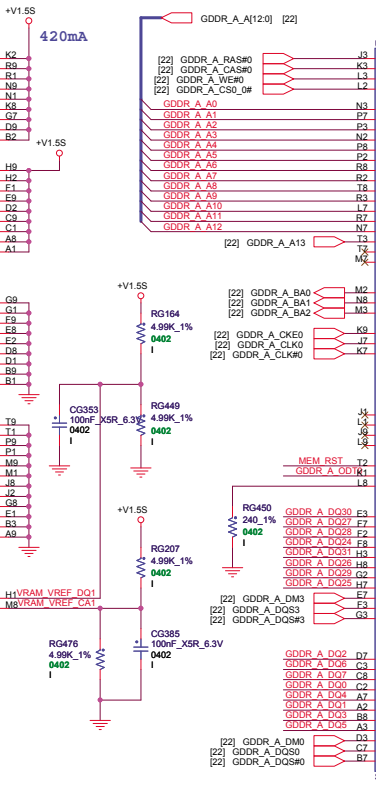
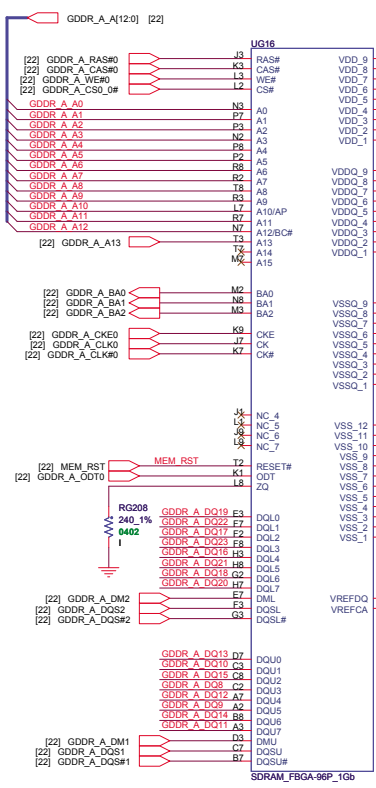
M93-S3: Not Install  
PARK-S3: Install

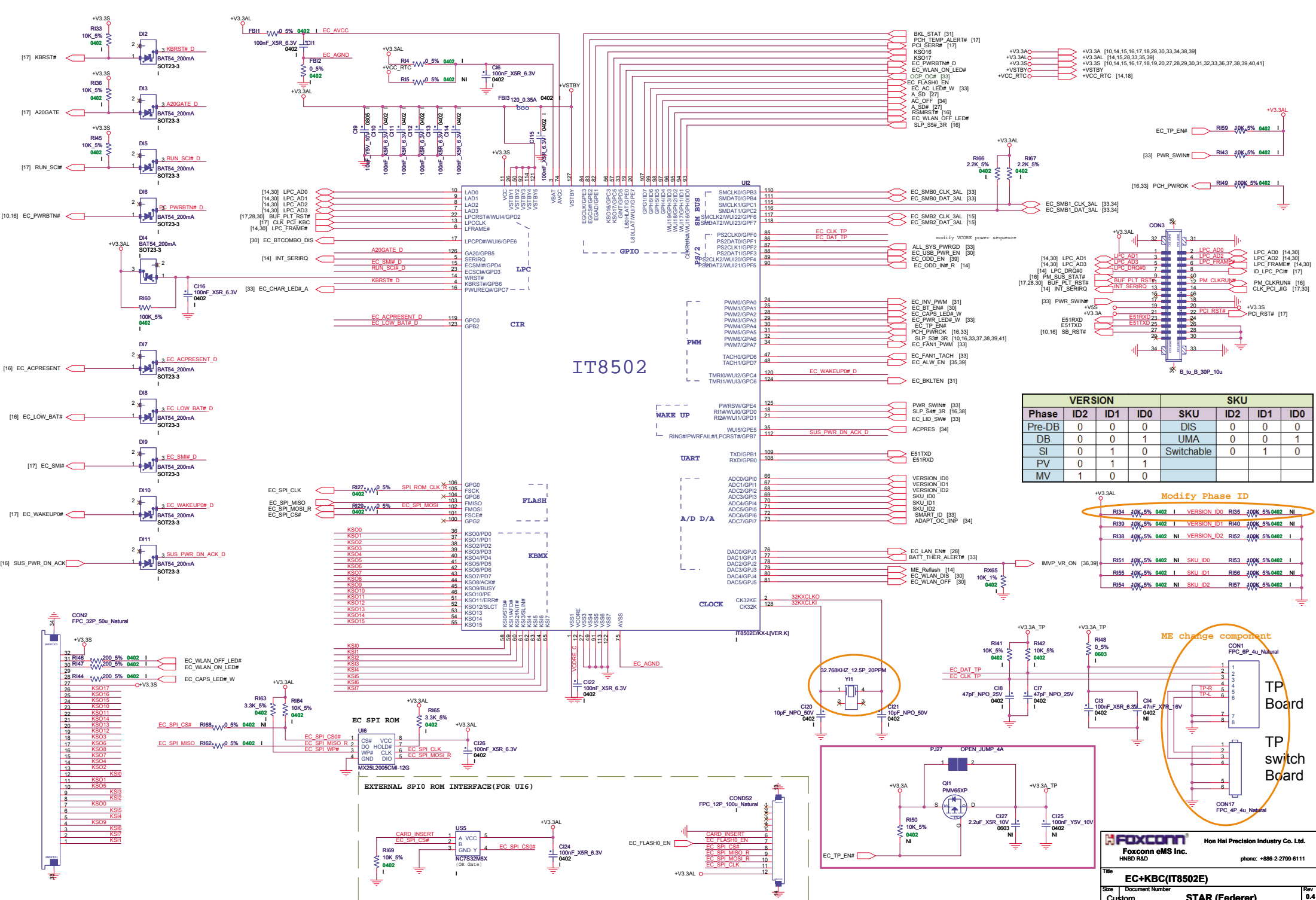




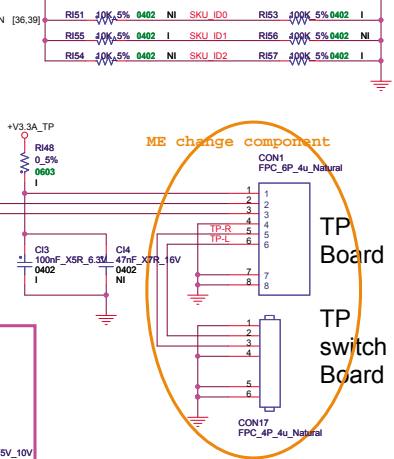
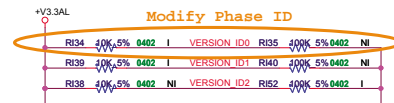


+V1.5S [22,24,39,41]



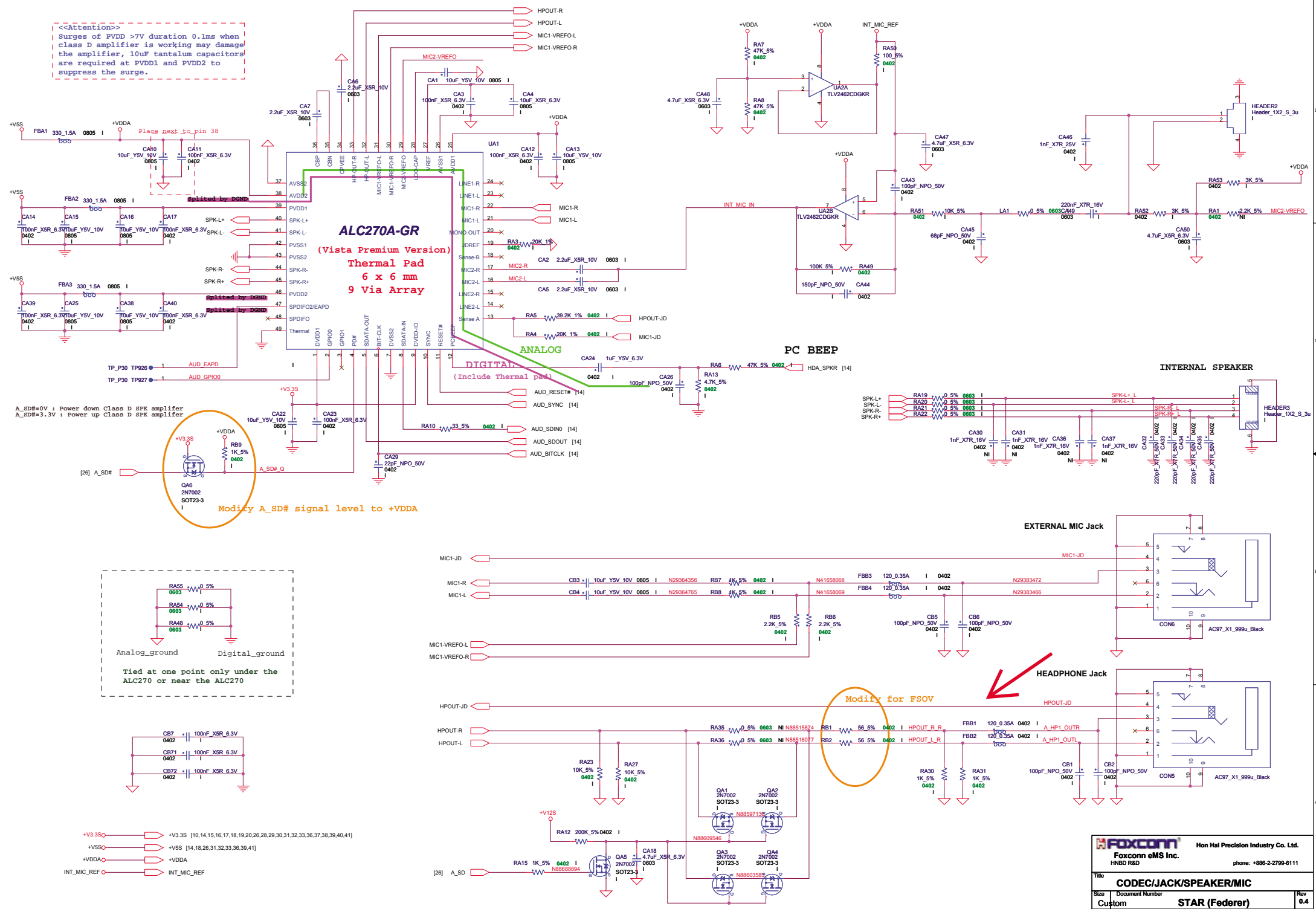


Phase	VERSION			SKU		
	ID2	ID1	ID0	SKU ID2	ID1	ID0
Pre-DB	0	0	0	DIS	0	0
DB	0	0	1	UMA	0	0
SI	0	1	0	Switchable	0	1
PV	0	1	1			
MV	1	0	0			

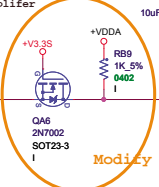


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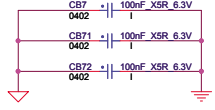
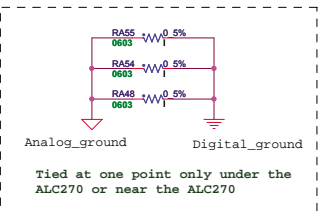
<<Attention>>  
Surges of FVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at FVDD1 and FVDD2 to suppress the surge.



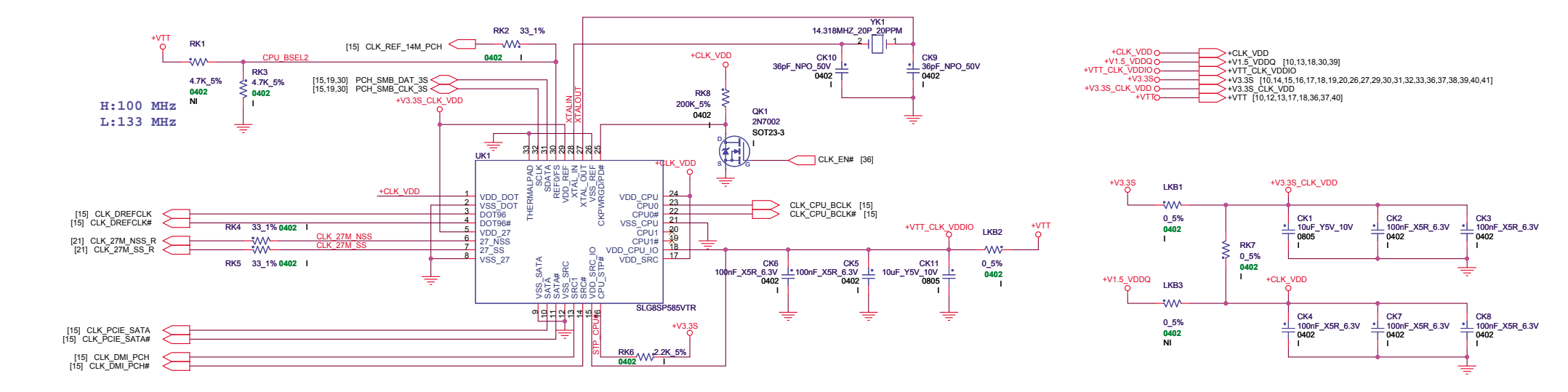
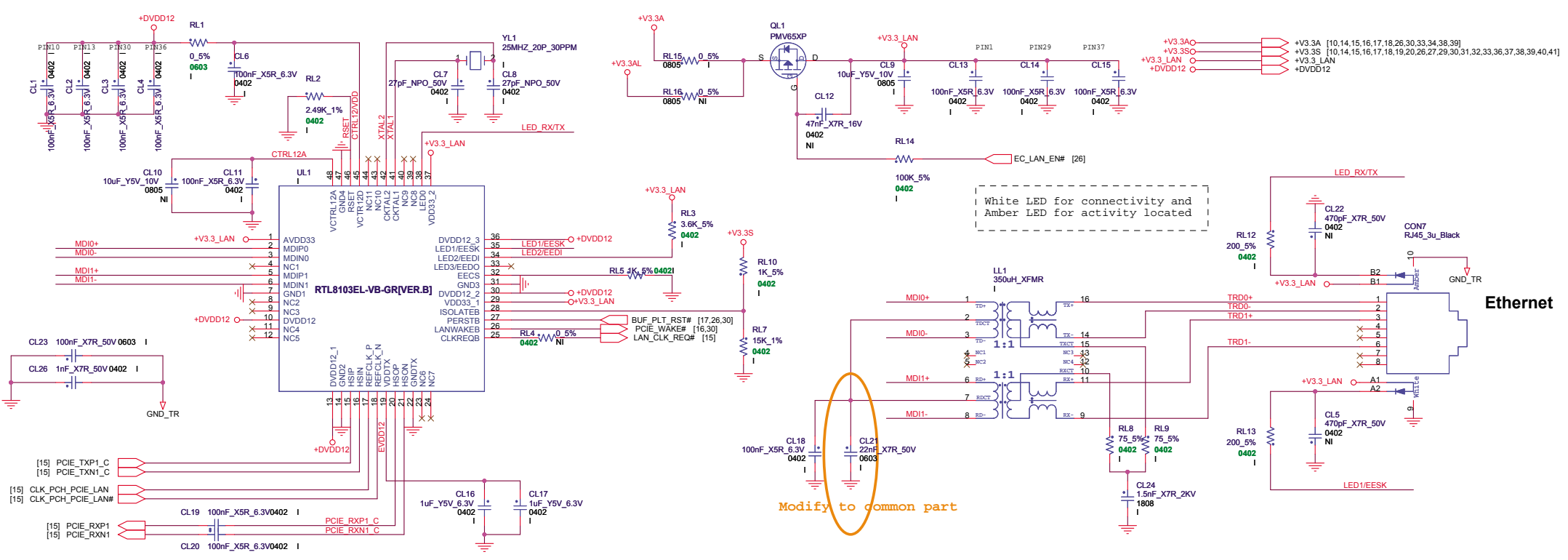
A\_SD# = 0V : Power down Class D SPK amplifier  
A\_SD# = 3.3V : Power up Class D SPK amplifier



Modify A\_SD# signal level to +VDDA



- +V3.3S [10,14,15,16,17,18,19,20,26,28,29,30,31,32,33,36,37,38,39,40,41]
- +VSS [14,18,26,31,32,33,36,39,41]
- +VDDA [14,18,26,31,32,33,36,39,41]
- INT\_MIC\_REF INT\_MIC\_REF



FSP Table

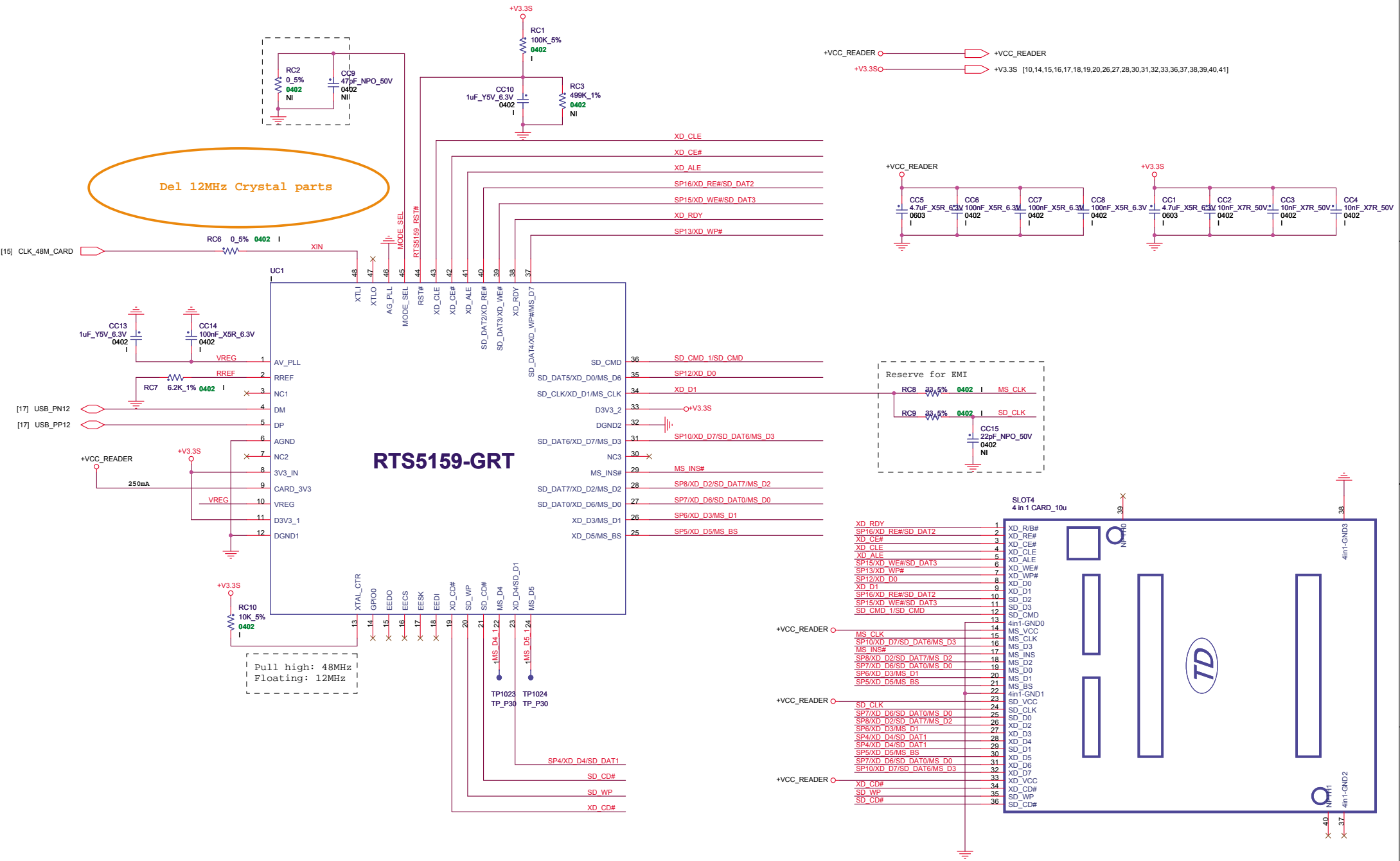
FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

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Title: **LAN (RTL8103EL)/CLOCK GEN**

Size: Custom Document Number  
 Custom **STAR (Federer)** Rev 0.4

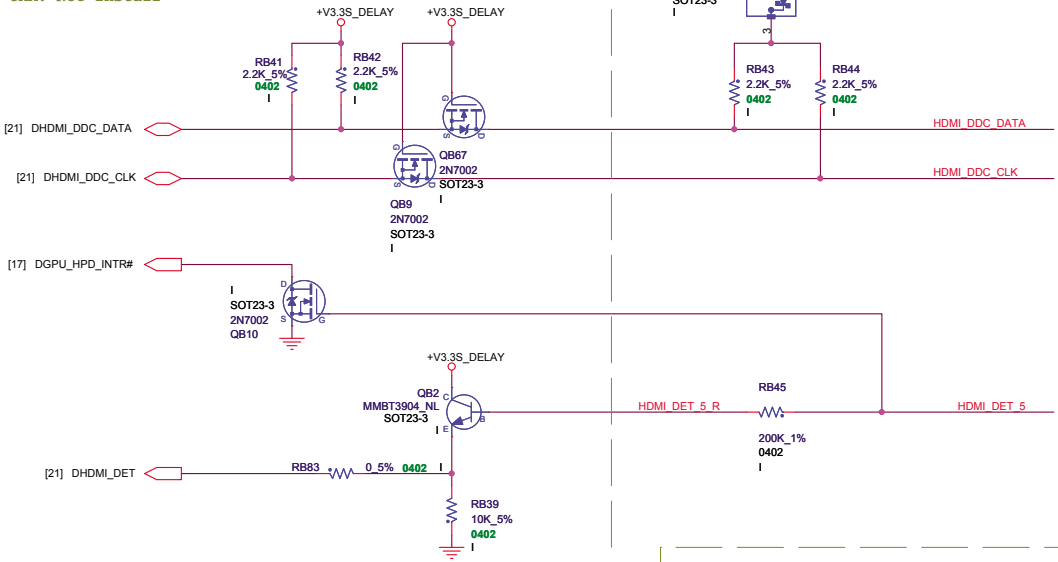
Page Modified: Tuesday, December 29, 2009 12:52:40 (UTC/GMT) | Sheet 28 of 41



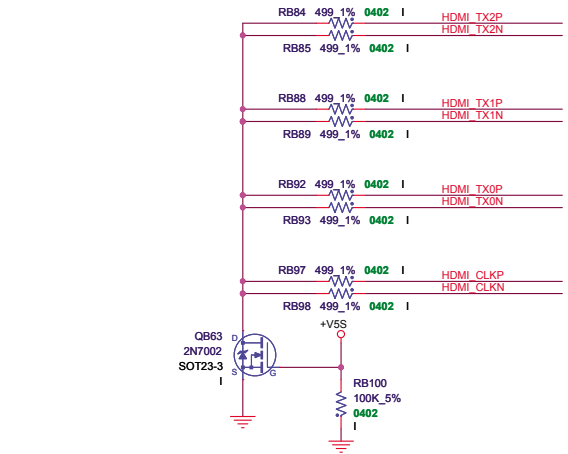




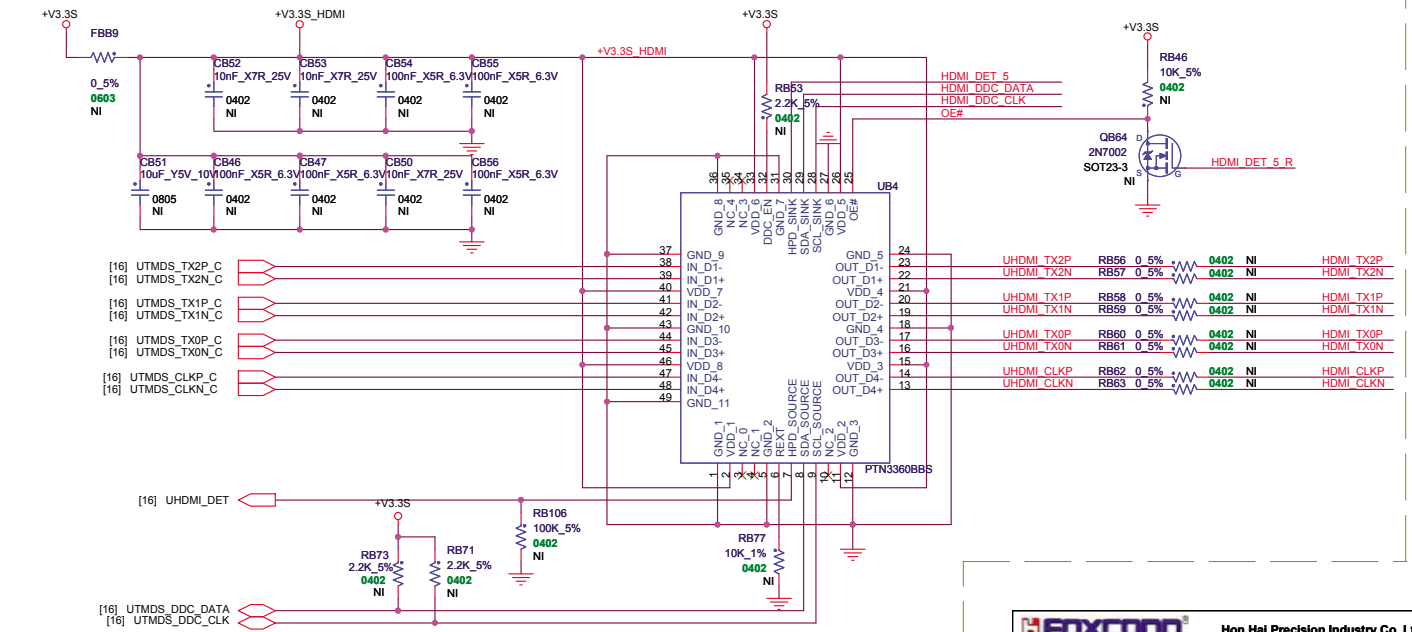
Discrete GPU: Install  
UMA: Not Install



[21] DHDMI_TX2P	CB63	0402	100nF_X5R_6.3V	I	HDMI_TX2P
[21] DHDMI_TX2N	CB64	0402	100nF_X5R_6.3V	I	HDMI_TX2N
[21] DHDMI_TX1P	CB65	0402	100nF_X5R_6.3V	I	HDMI_TX1P
[21] DHDMI_TX1N	CB66	0402	100nF_X5R_6.3V	I	HDMI_TX1N
[21] DHDMI_TX0P	CB67	0402	100nF_X5R_6.3V	I	HDMI_TX0P
[21] DHDMI_TX0N	CB68	0402	100nF_X5R_6.3V	I	HDMI_TX0N
[21] DHDMI_CLKP	CB69	0402	100nF_X5R_6.3V	I	HDMI_CLKP
[21] DHDMI_CLKN	CB70	0402	100nF_X5R_6.3V	I	HDMI_CLKN



Discrete GPU:Not Install  
UMA:Install



[16] UTMD5_TX2P_C	RB56	0.5%	0402	NI	HDMI_TX2P
[16] UTMD5_TX2N_C	RB57	0.5%	0402	NI	HDMI_TX2N
[16] UTMD5_TX1P_C	RB58	0.5%	0402	NI	HDMI_TX1P
[16] UTMD5_TX1N_C	RB59	0.5%	0402	NI	HDMI_TX1N
[16] UTMD5_TX0P_C	RB60	0.5%	0402	NI	HDMI_TX0P
[16] UTMD5_TX0N_C	RB61	0.5%	0402	NI	HDMI_TX0N
[16] UTMD5_CLKP_C	RB62	0.5%	0402	NI	HDMI_CLKP
[16] UTMD5_CLKN_C	RB63	0.5%	0402	NI	HDMI_CLKN

+V5S	+V5S [14,18,26,27,31,33,36,39,41]
+V3.3S	+V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,33,36,37,38,39,40,41]
+V3.3S_DELAY	+V3.3S_DELAY [20,21,24,39]
+V5S_HDMI	+V5S_HDMI
+V3.3S_HDMI	+V3.3S_HDMI

HDMI spec: +5V: 4.7V min , 55mA max.

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HNBD R&D

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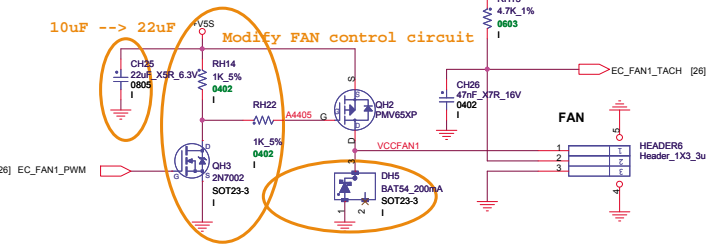
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Size: Custom Document Number: **STAR (Federer)** Rev: **0.4**

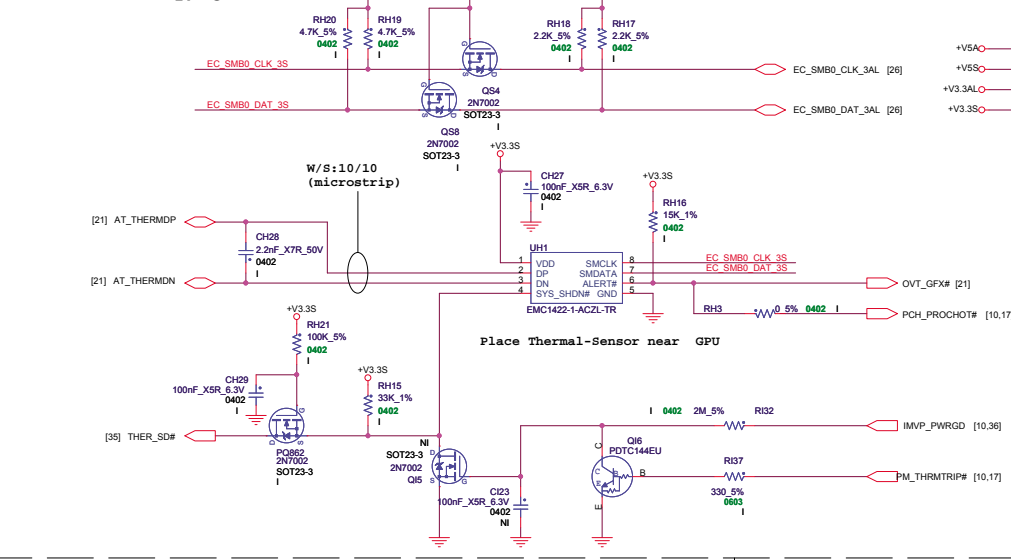
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### FAN CONNECTOR



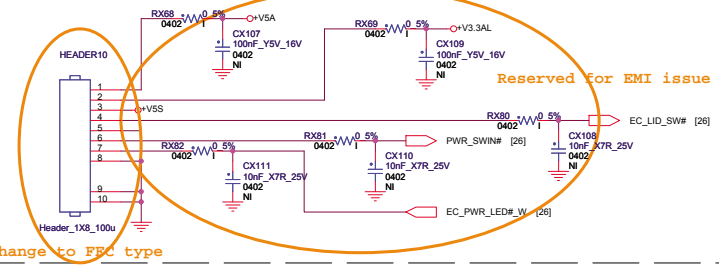
### THERMAL SENSOR



SYS\_SHDN Threshold Temperature

SYS_SHDN PULLUP	4.7K OHM 510%	6.8K OHM 510%	10K OHM 510%	15K OHM 510%	22K OHM 510%	33K OHM 510%
ALERT#	77°C	83°C	89°C	95°C	101°C	107°C
4.7K OHM 510%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM 510%	79°C	84°C	90°C	96°C	102°C	108°C
10K OHM 510%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM 510%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM 510%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM 510%	82°C	88°C	94°C	100°C	106°C	112°C

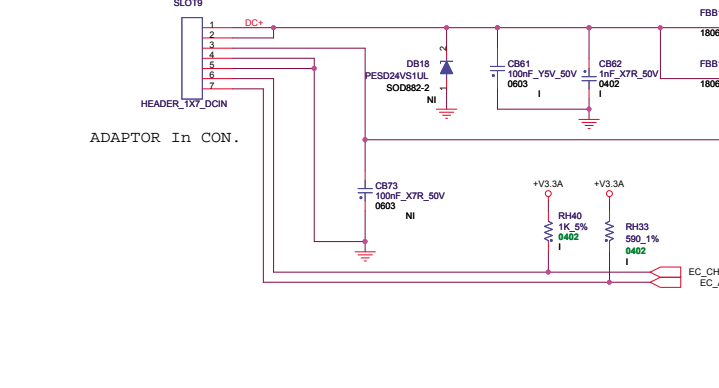
### POWER BUTTON BOARD CONNECTOR



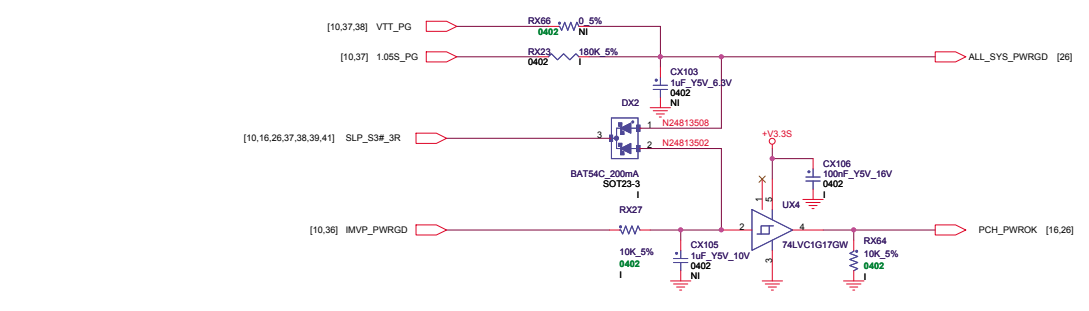
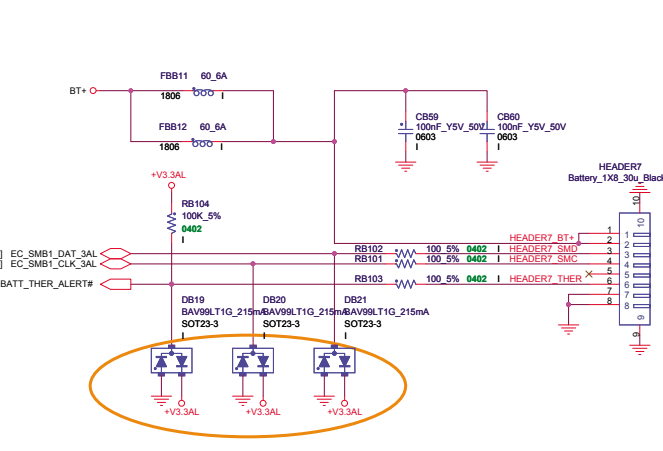
Change to FPC type

### DC JACK

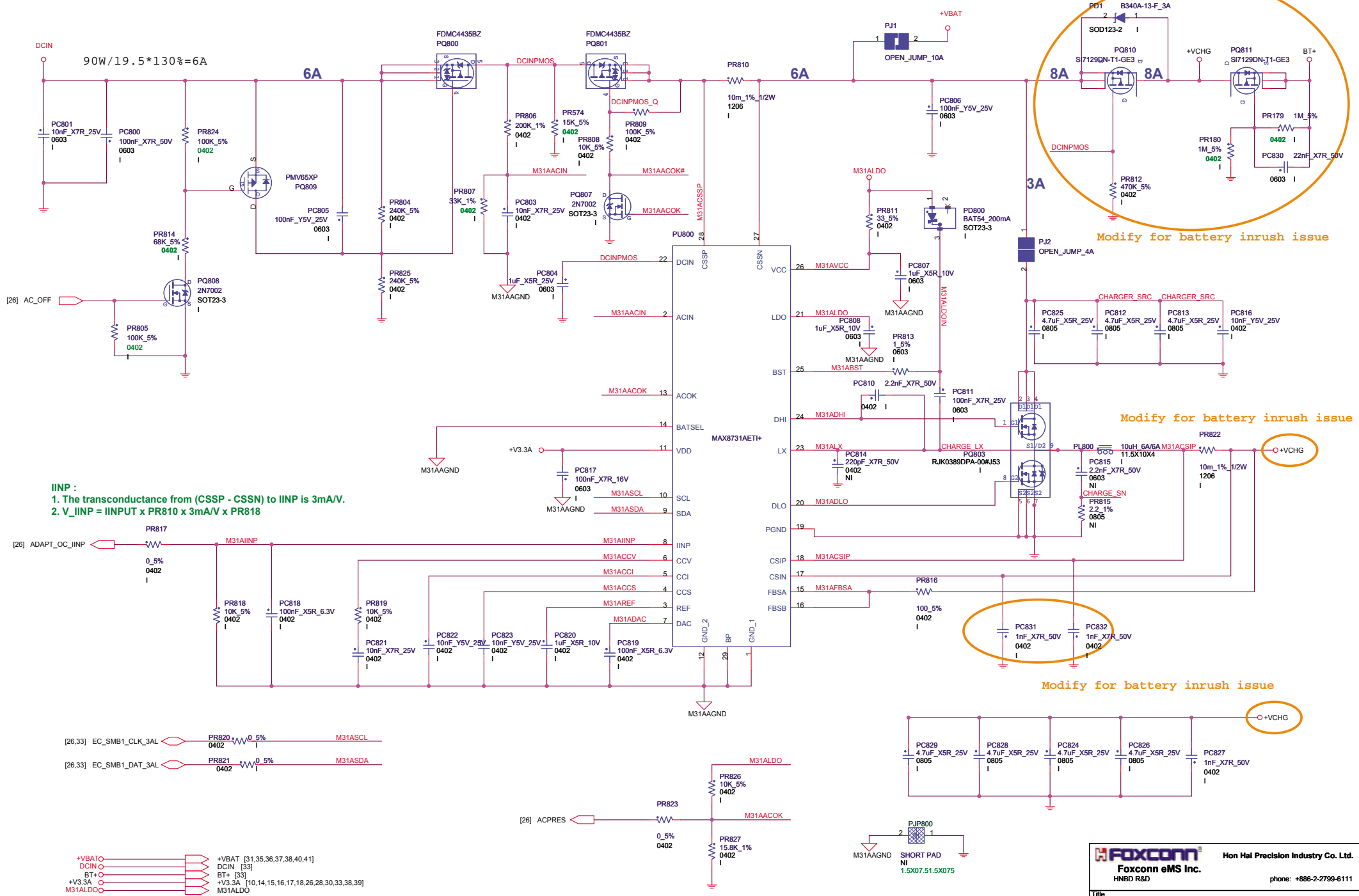
#### Wire to Board CONNECTOR



### BATTERY CONNECTOR



Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin.
4	SMC	SMBus clock interface I/O pin.
5	ID	Open
6	B/I	Connected to thermistor (103AT) equivalent
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



IINP :  
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.  
 2.  $V_{IINP} = IINPUT \times PR810 \times 3mA/V \times PR818$

Modify for battery inrush issue

Modify for battery inrush issue

Modify for battery inrush issue

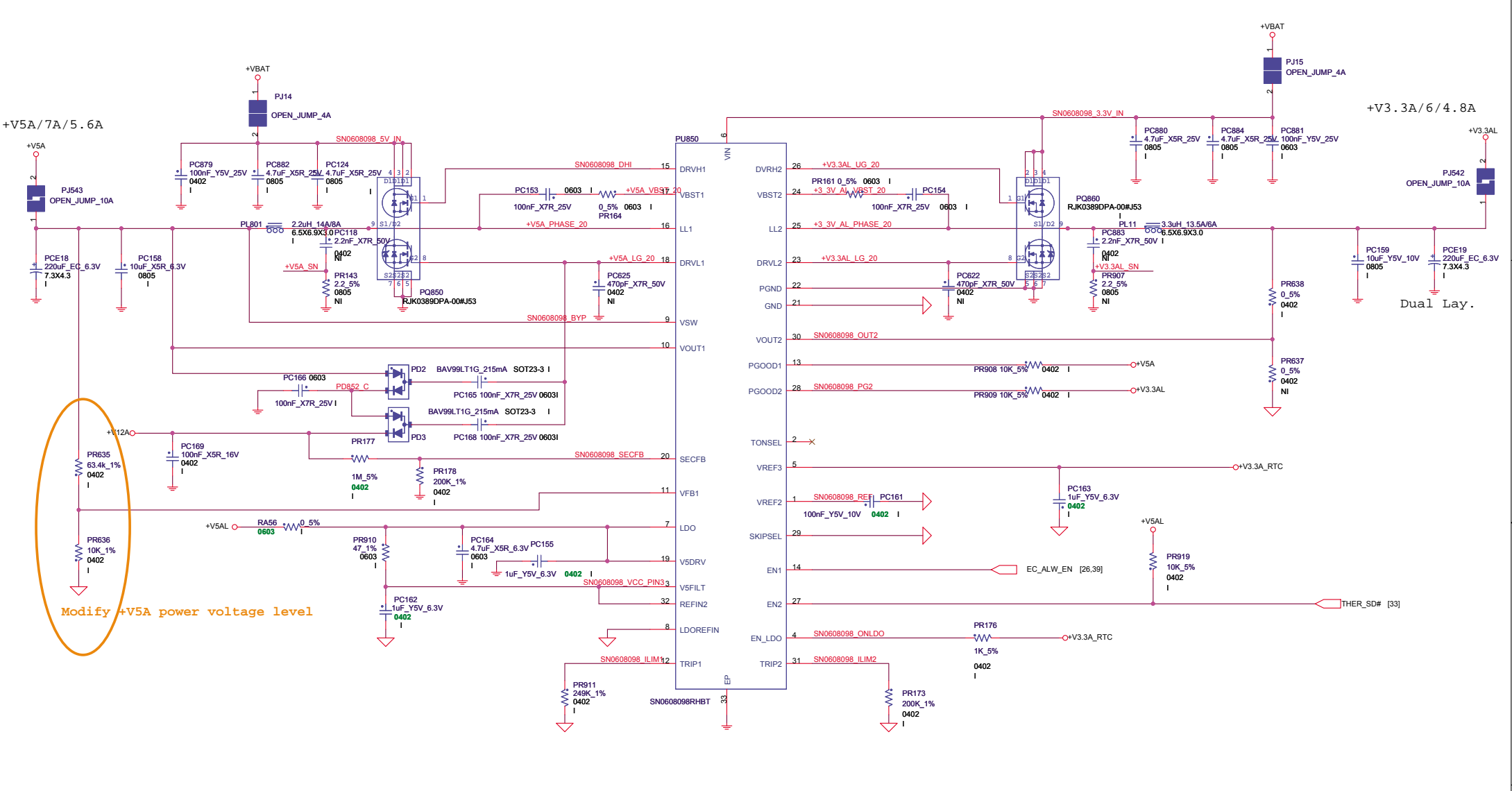
**FOXCONN**  
 Foxconn eMS Inc.  
 HNBD R&D  
 Hon Hai Precision Industry Co. Ltd.  
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Title		<b>PWR_Charger</b>	
Size	Document Number	Rev	0.4
Custom	STAR (Federer)		
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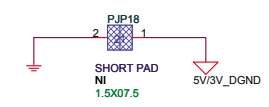
- +VBAT0 [31,35,36,37,38,40,41]
- DCIN [33]
- BT+ [33]
- +V3.3A [10,14,15,16,17,18,26,28,30,33,38,39]
- M31ALDO

- [26.33] EC\_SMB1\_CLK\_3AL PR820 0.5% M31ASCL
- [26.33] EC\_SMB1\_DAT\_3AL PR821 0.5% M31ASDA

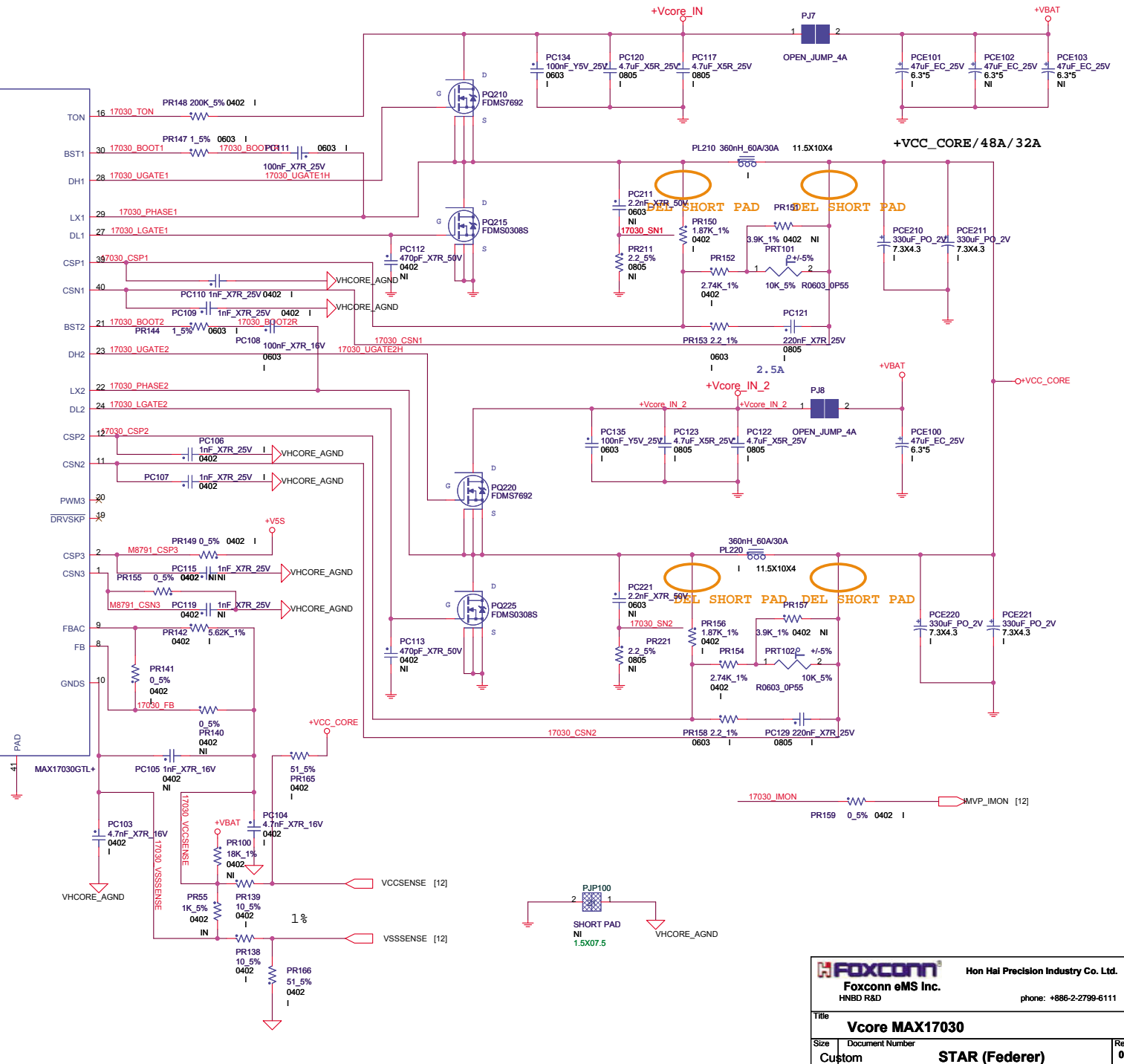
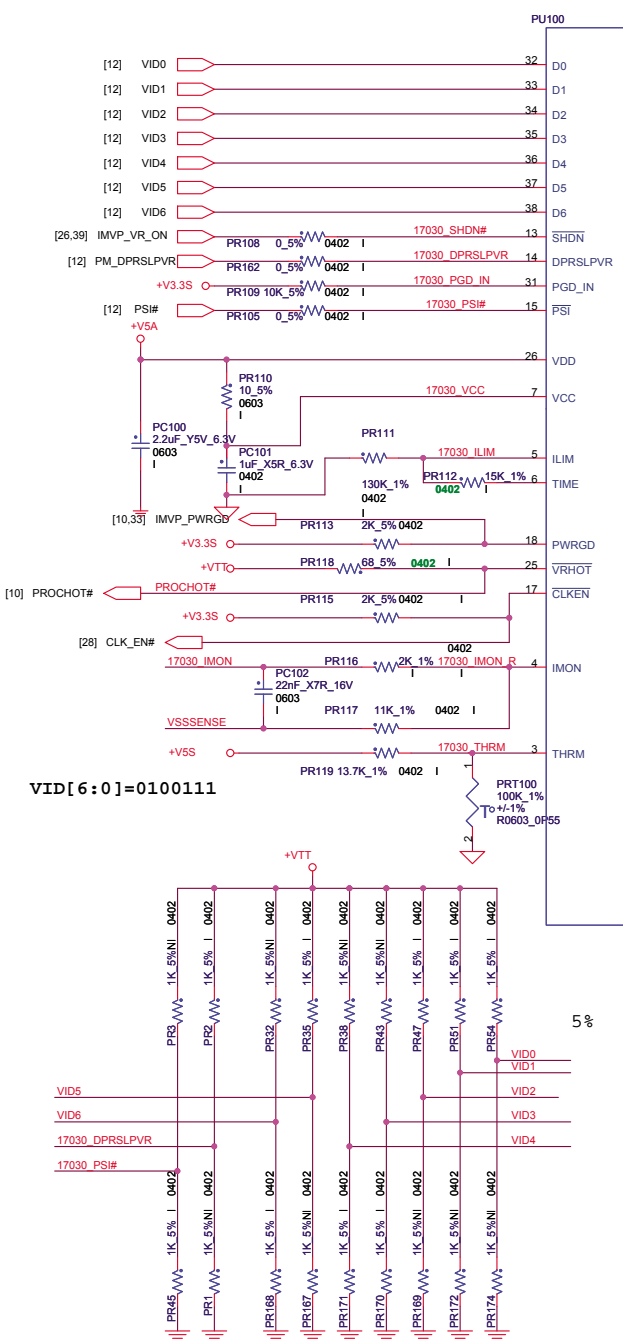
- [26] ACPRES PR823 0.5% M31AACOK



- +V3.3AL +V3.3AL [14,15,26,28,33,39]
- +V3.3AO +V3.3A [10,14,15,16,17,18,26,28,30,33,34,38,39]
- +V3.3S +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40,41]
- +VBATO +VBAT [31,34,36,37,38,40,41]
- +V12AO +V12A [39]
- +V5AO +V5A [18,30,33,36,37,38,39,40,41]
- +V5ALO +V5AL [39]

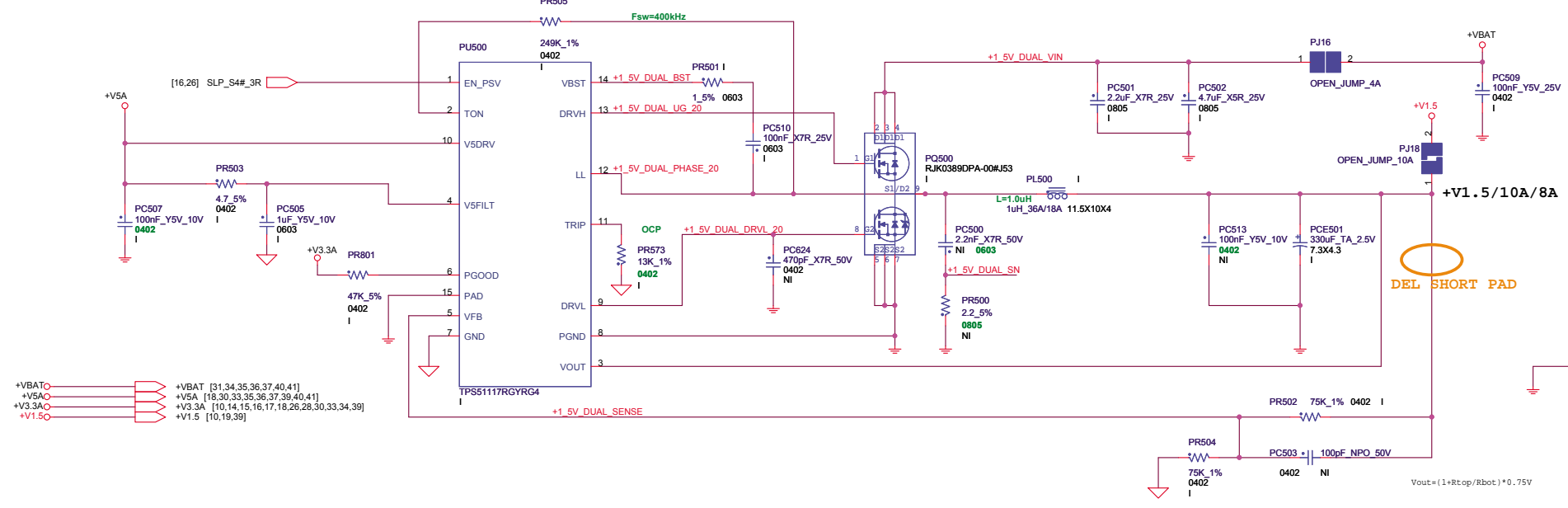


+V3.3S +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,37,38,39,40,41]  
 +V5S +V5S [14,18,26,27,31,32,33,39,41]  
 +VBAT +VBAT [31,34,35,37,38,40,41]  
 +VTT +VTT [10,12,13,17,18,28,37,40]  
 +VCC\_CORE +VCC\_CORE [12]

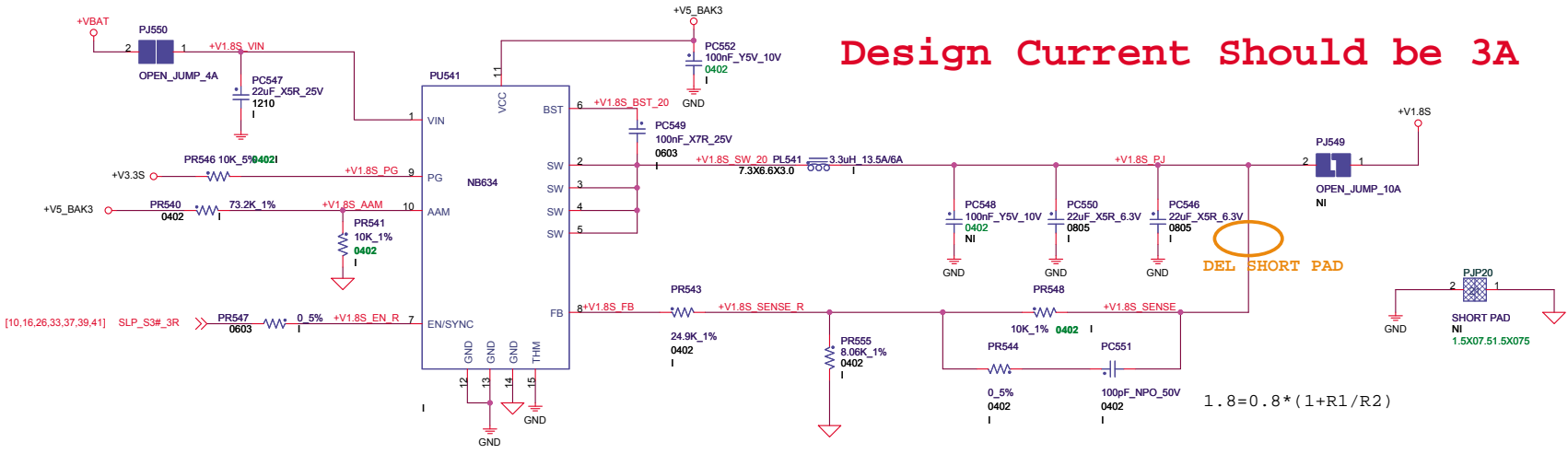




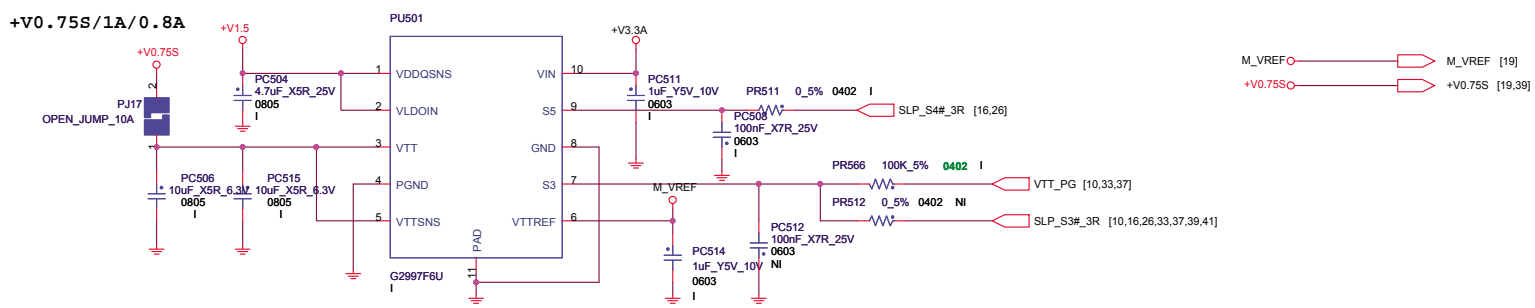
Frequency is 400K HZ  
 D-CAP Mode  
 Set Iocp point at 12A

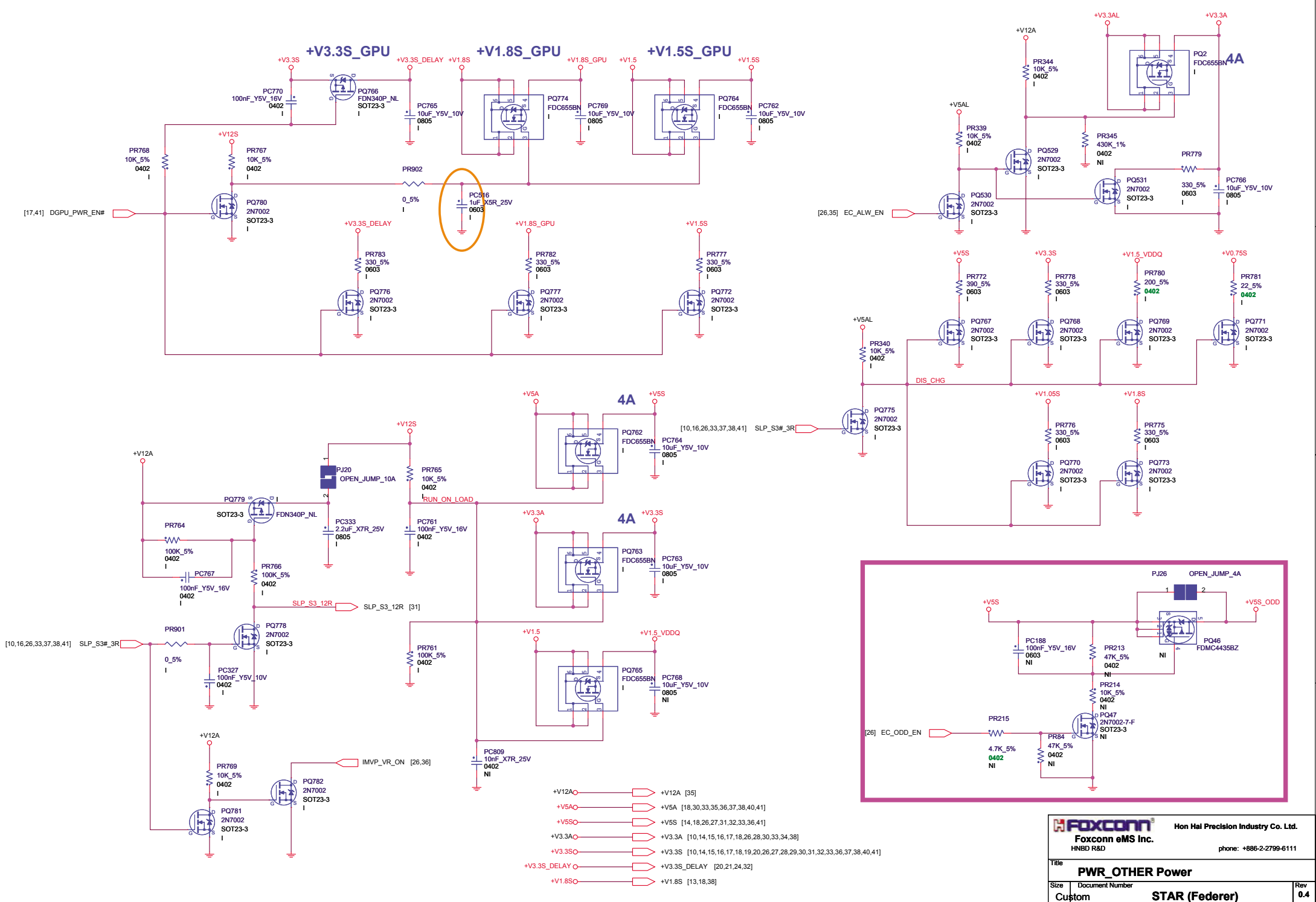


## Design Current Should be 3A



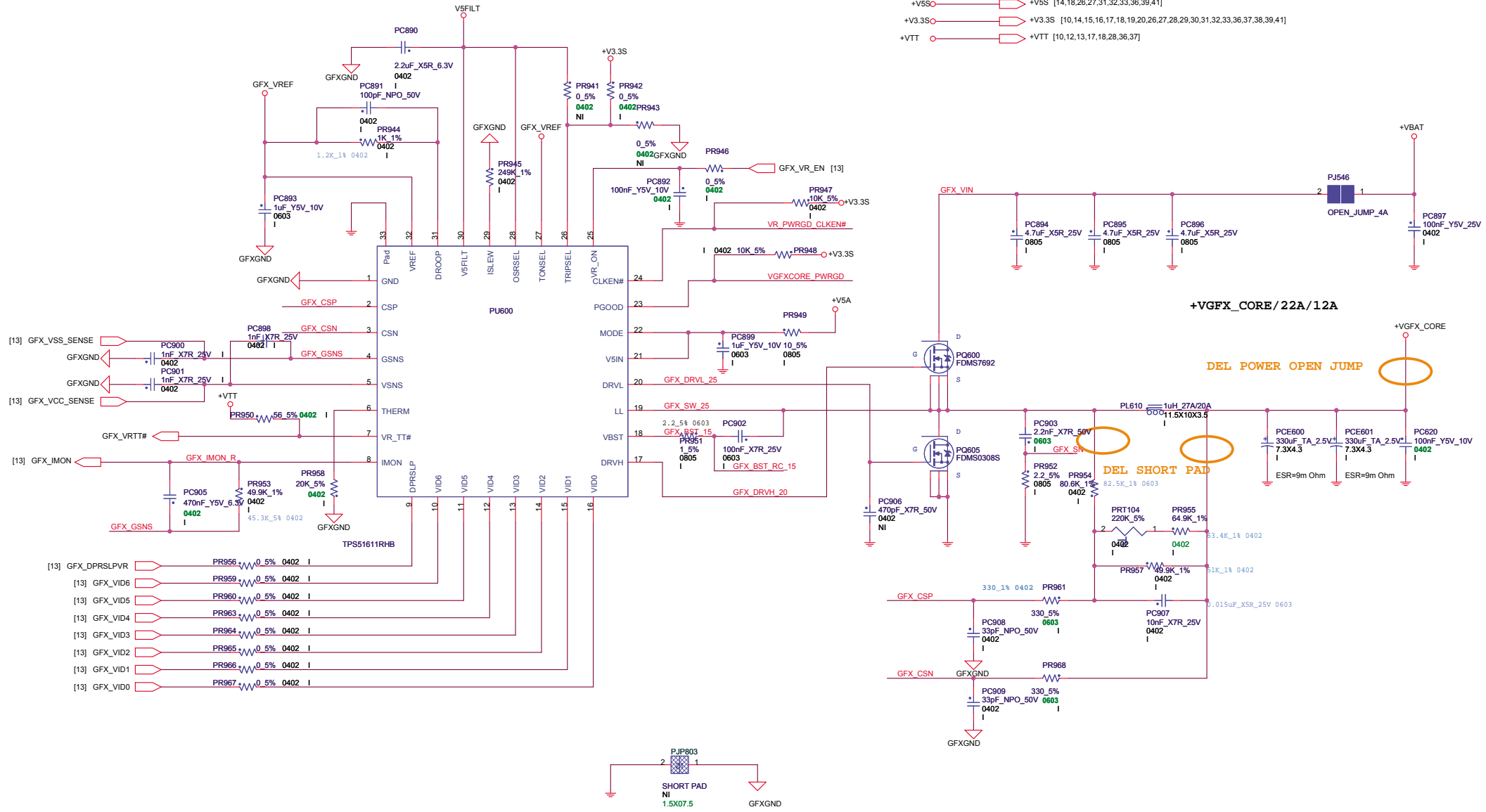
$$1.8 = 0.8 * (1 + R1/R2)$$





- +V12A O → +V12A [35]
- +V5A O → +V5A [18,30,33,35,36,37,38,40,41]
- +V5S O → +V5S [14,18,26,27,31,32,33,36,41]
- +V3.3A O → +V3.3A [10,14,15,16,17,18,26,28,30,33,34,38]
- +V3.3S O → +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,40,41]
- +V3.3S\_DELAY O → +V3.3S\_DELAY [20,21,24,32]
- +V1.8S O → +V1.8S [13,18,38]

**+VGFXCORE**



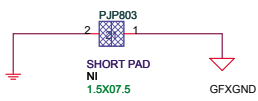
- +VBAT +VBAT [31,34,35,36,37,38,41]
- +VGFX\_CORE +VGFX\_CORE [13]
- +V5S +V5S [14,18,26,27,31,32,33,36,39,41]
- +V3.3S +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,41]
- +VTT +VTT [10,12,13,17,18,28,36,37]

- [13] GFX\_VSS\_SENSE
- [13] GFX\_VCC\_SENSE
- [13] GFX\_IMON
- [13] GFX\_DPRSPLPVR
- [13] GFX\_VID6
- [13] GFX\_VID5
- [13] GFX\_VID4
- [13] GFX\_VID3
- [13] GFX\_VID2
- [13] GFX\_VID1
- [13] GFX\_VID0

**+VGFX\_CORE/22A/12A**

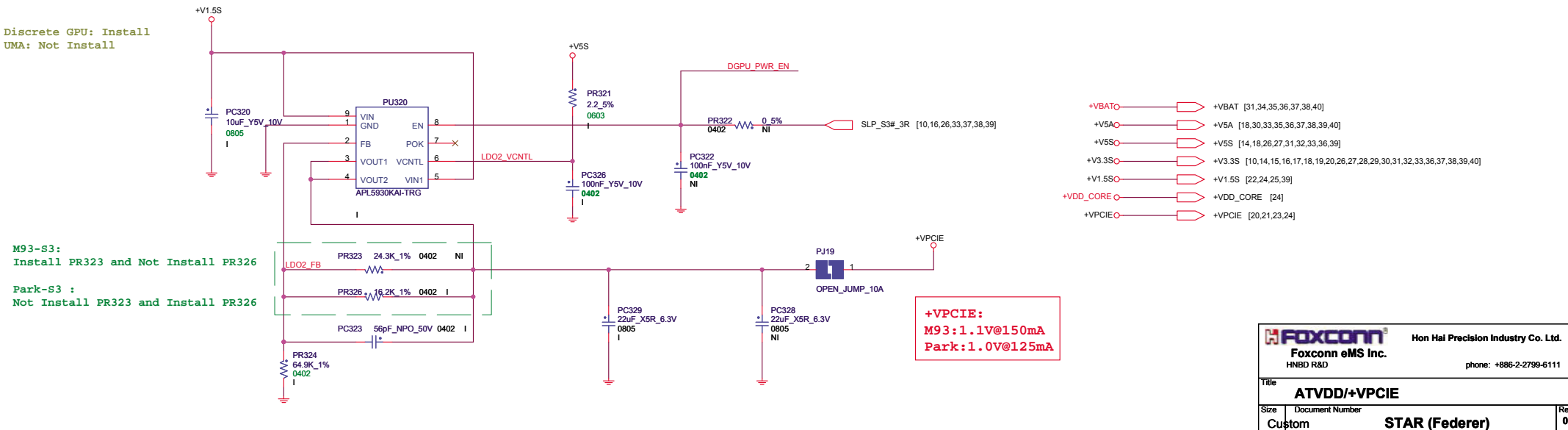
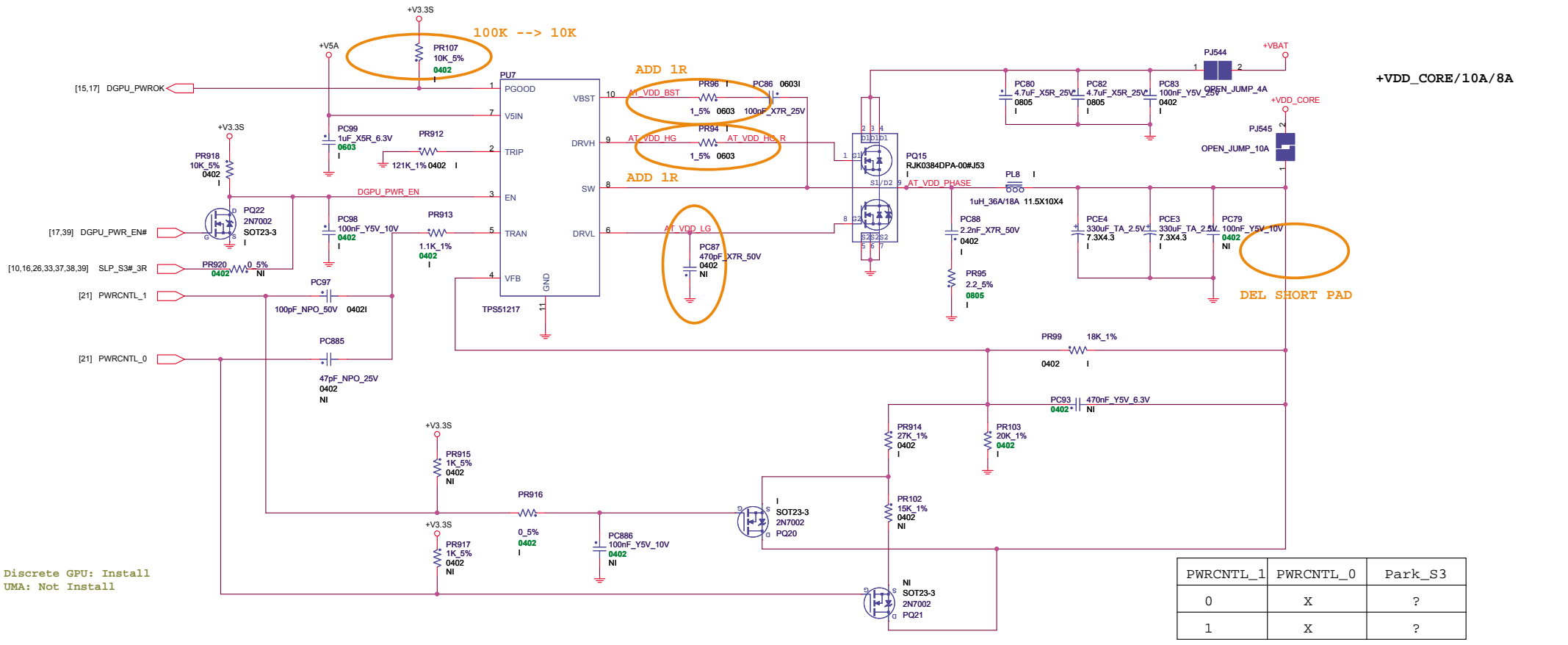
**DEL POWER OPEN JUMP**

**DEL SHORT PAD**



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<b>Title</b> CPU VREG & Decoupling				
<b>Size</b>	<b>Document Number</b>			<b>Rev</b>
Custom	STAR (Federer)			0.4
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