

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4_LGA775_A
06	P4_LGA775_B
07	P4_LGA775_C
08	P4_LGA775_D
09	GMCH-BROADWATER_HOST
10	GMCH-BROADWATER_DDRII
11	GMCH-BROADWATER_PCI E, DMI
12	GMCH-BROADWATER_INT VGA
13	GMCH-BROADWATER_GND
14	GMCH-BROADWATER_PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH8 PCI, USB, DMI, LAN
20	ICH8 GPIO, CTRL
21	ICH8 SATA, FAN PWM
22	ICH8 VCC, GND
23	CLOCK GEN ICS9LPRS587
24	PCI EXPRESS X4 PORT1 SLOT
25	PCI SLOT 1, 2, 3
26	PCIE_1,SW
27	ITE 8718 CX

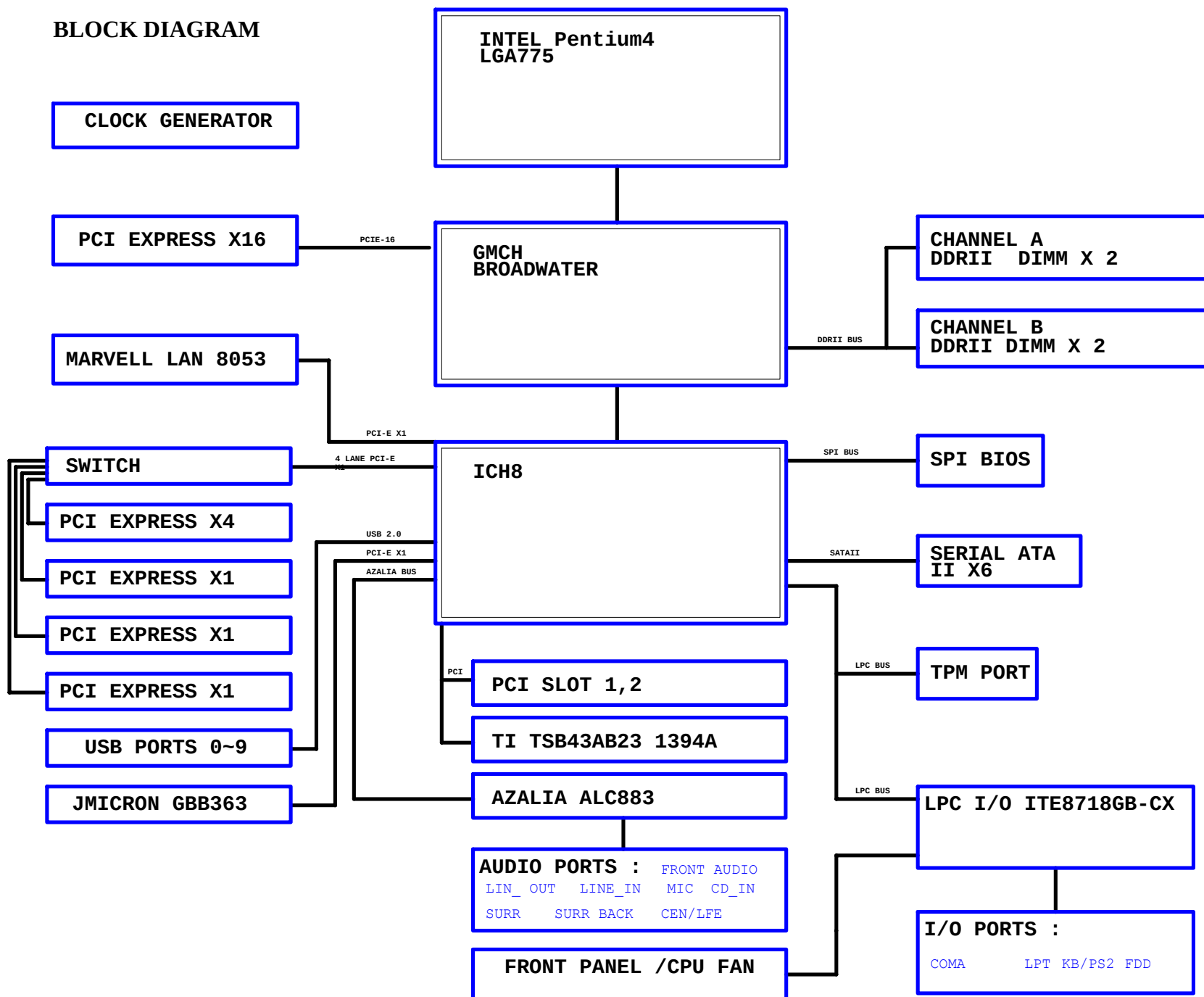
SHEET TITLE

28	COM_LPT, -PROHOT,DYNAMIC OC
29	DUAL BIOS
30	ALC883
31	REAR AUDIO JACK
32	VCORE PWM_ISL6307-1
33	VCORE PWM_ISL6307-2
34	VCORE PWM_ISL6307-3
35	DISCRETE POWER
36	ATX, OTHERS POWER
37	MARVELL 88E8053
38	TI TSB43AB23 1394
39	FP,FUSB,FDD
40	JMB363
41	CI,HWM,KB/MS, FAN CTRL
42	
43	
44	

Circuit or PCB layout change for next version

[illegible][illegible]

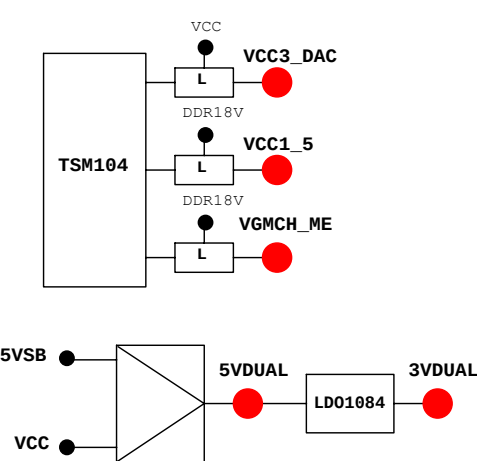
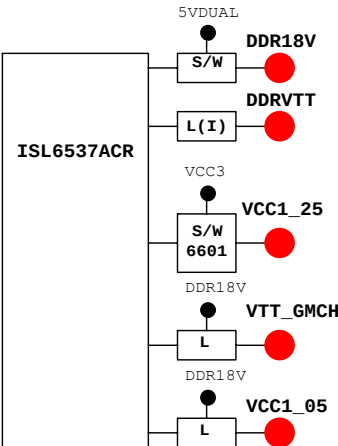
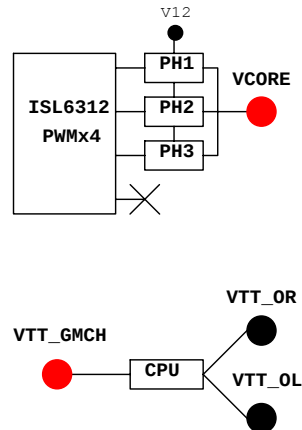
BLOCK DIAGRAM



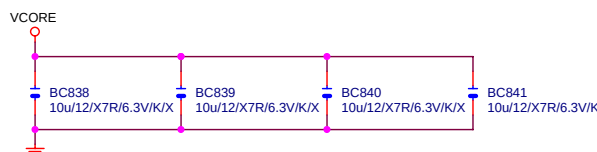
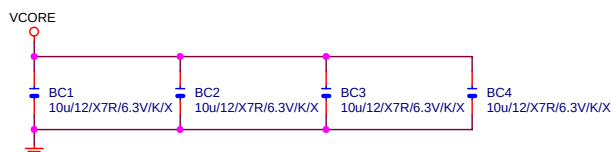
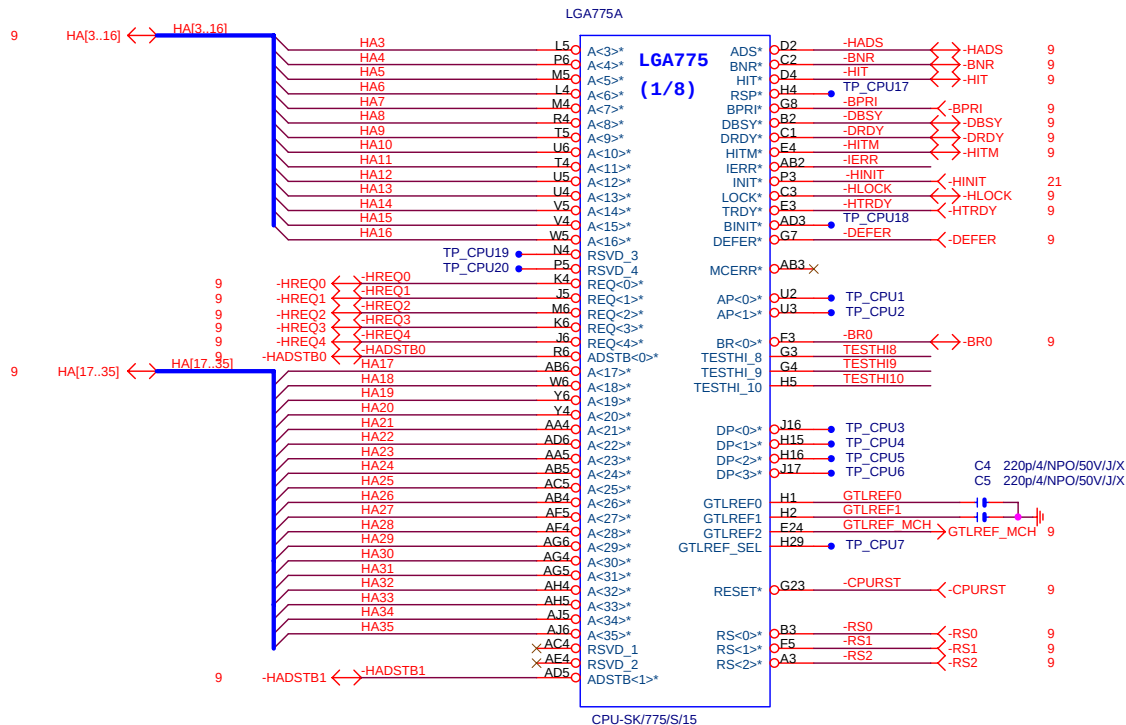
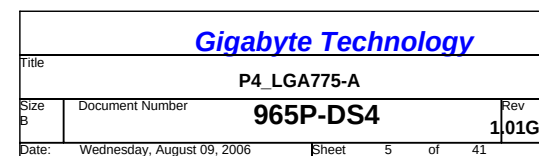
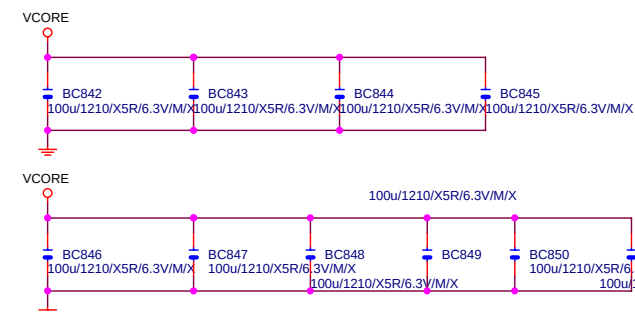
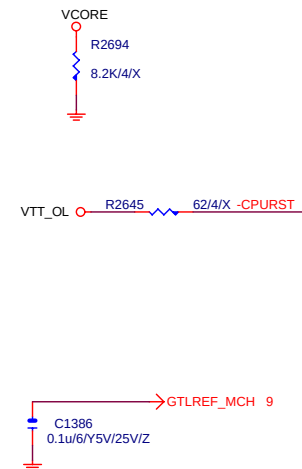
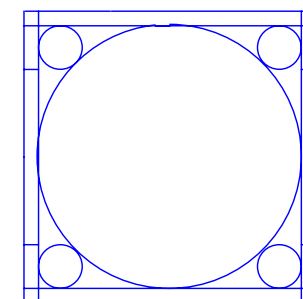
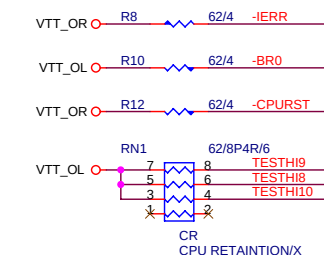
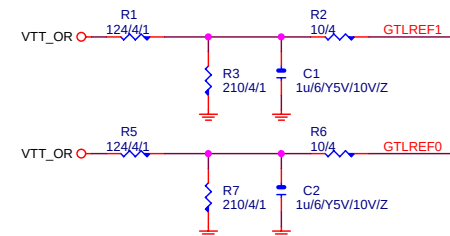
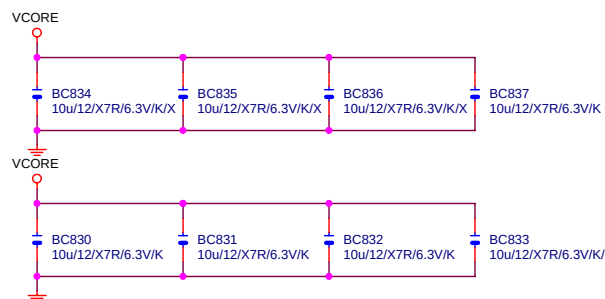
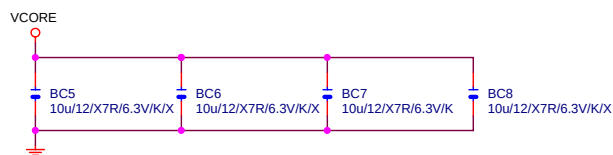
ICH8 GPIO LIST TABLE

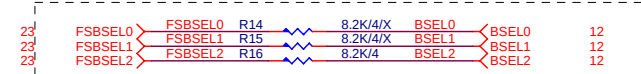
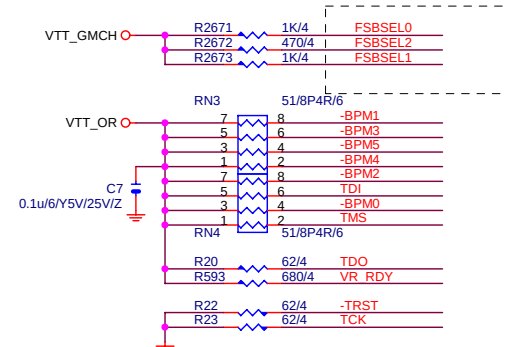
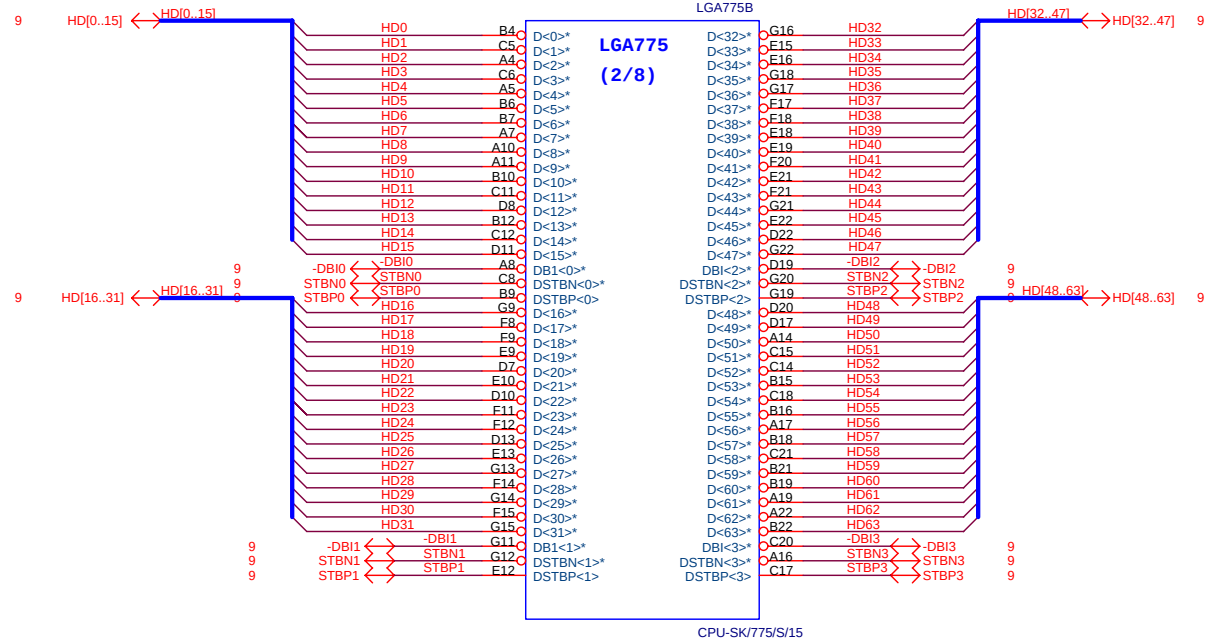
PIN	NAME	PWR WELL	AFTER/ ELTRST	USAGE	NOTE
GP0		MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1		MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#		MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#		MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQ6#		MAIN	IN	-PIRQ6	P/U 8.2K VCC3
GP5/PIRQH#		MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2		MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3		MAIN	IN	VTT_GMCH_OV3	P/U 8.2K VCC3
GP8		STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9		STBY	OUT	WOL_ONLY	P/D 100K GND
GP10		STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#		STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12		STBY	IN	DDR18V_OV5	P/U 8.2K 3VDUAL
GP13		STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14		STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15		STBY	OUT	RM	N/A
GP16		MAIN	OUT/LOW	RESET	N/A
GP17/TACH0		MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18		MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19		MAIN	IN	VCC15_OV1	P/U 8.2K VCC3
GP20		MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21		MAIN	IN	VCC15_OV3	P/U 8.2K VCC3
GP22		MAIN	IN	VCORE_OV3	P/U 8.2K VCC3
GP23		MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24		STBY	OUT	TLS	P/U 8.2K 3VDUAL
GP25		STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#		STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27		STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28		STBY	OUT/LOW	-SPI_WP0	N/A
GP29/OC5#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP30/OC6#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP31/OC7#		STBY	IN	-USB0C_R	P/U FUSEVCC
GP32		MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33		MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34		MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35		MAIN	OUT	VCC15_OV2	N/A
GP36		MAIN	IN	VCORE_OV4	P/U 8.2K VCC3
GP37		MAIN	IN	VCORE_OV5	P/U 8.2K VCC3
GP38		MAIN	IN	VCORE_OV2	P/U 8.2K VCC3
GP39		MAIN	IN	GPIO39	P/D 8.2K GND
GP48		MAIN	IN	VCORE_OV1	P/U 8.2K VCC3
GP49		MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:3 PHASE PWM--ISL6312

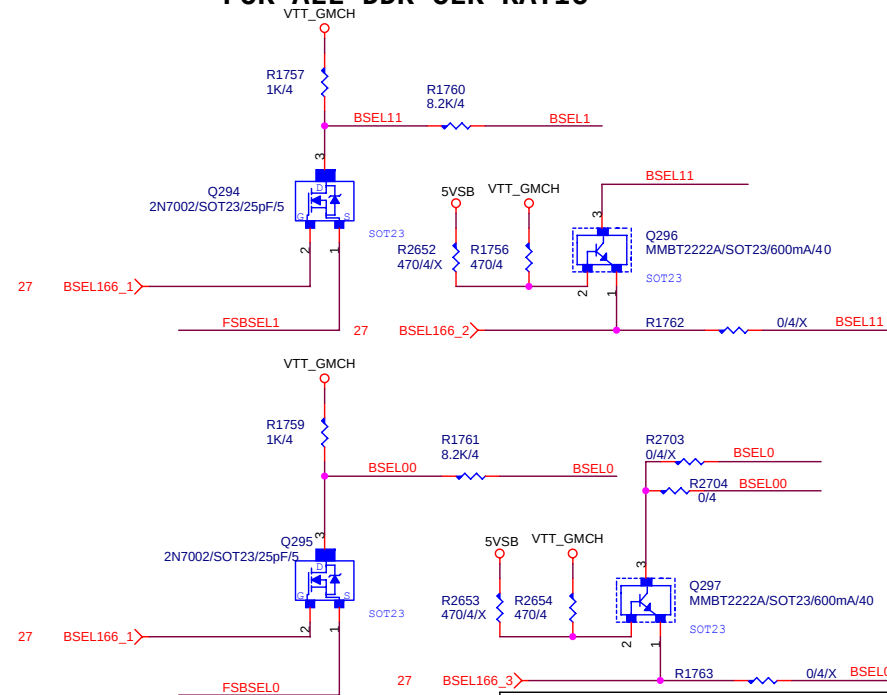


	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8718
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	ICH8
SYS FAN	FANPWM2	N/A	FANIO2	IT8718
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	ICH8
PWR FAN	N/A	N/A	FANIO3	IT8718
			ICH_FAN_TACH2	ICH8



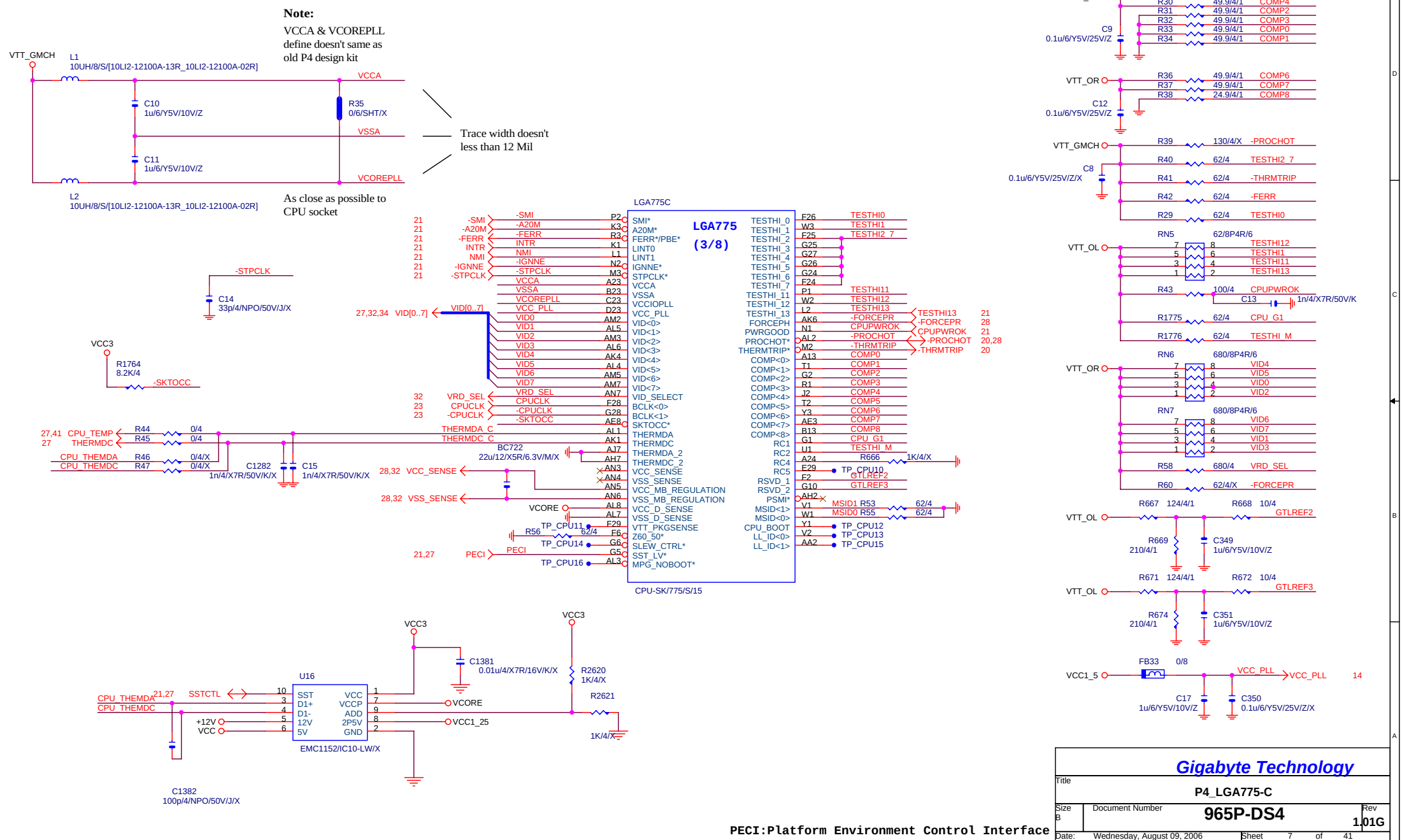


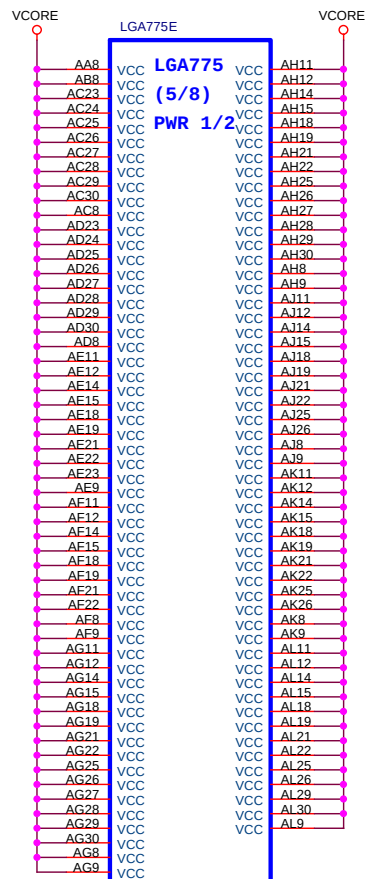
FOR ALL DDR CLK RATIO



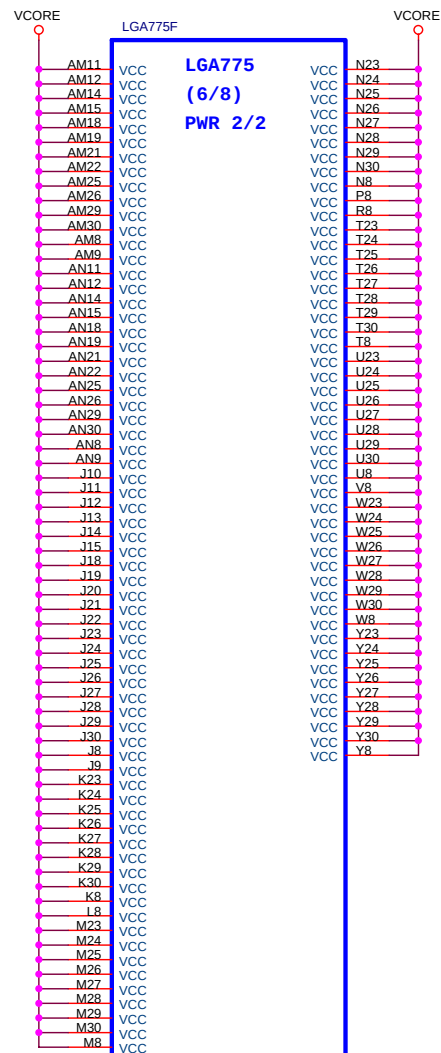
Gigabyte Technology

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Size	Document Number	965P-DS4		Rev
B				1,01G
Date:	Wednesday, August 09, 2006	Sheet	6	of 41

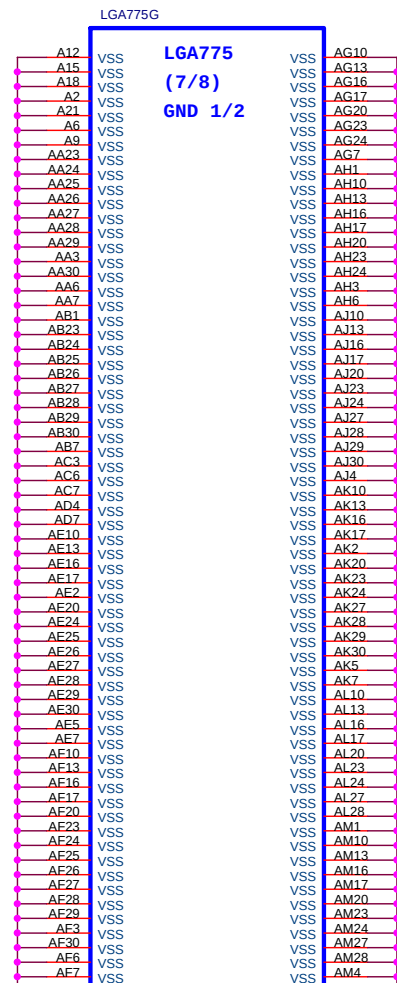




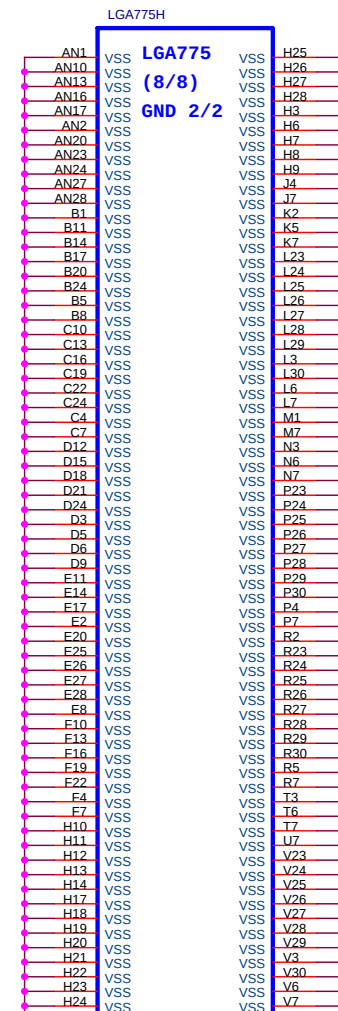
CPU-SK/775/S/15



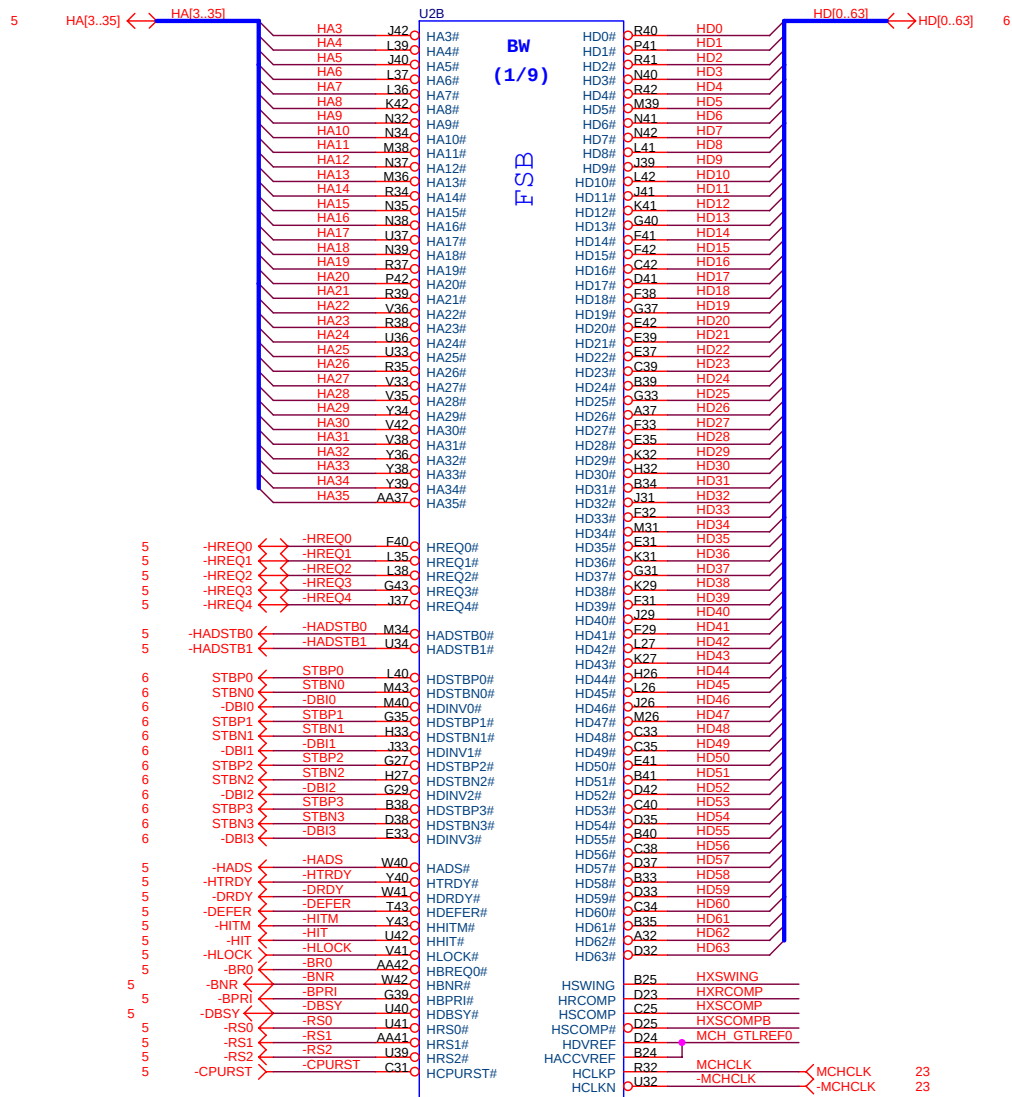
CPU-SK/775/S/15



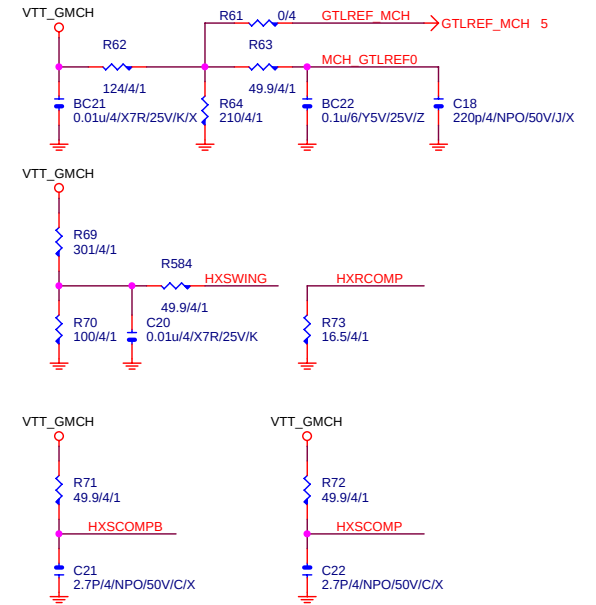
CPU-SK/775/S/15



CPU-SK/775/S/15



P965-C1/QM62[10HB1-030082-30R]
CPU INTERFACE



Gigabyte Technology			
Title			
GMCH-HOST			
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U2C

BW
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MAAA0	BA31	SMA_A0	SDQS_A0
MAAA1	BA25	SMA_A1	SDQS_A0#
MAAA2	BA26	SMA_A2	SDM_A0
MAAA3	BA25	SMA_A3	
MAAA4	AY25	SMA_A4	SDQ_A0
MAAA5	BA23	SMA_A5	SDQ_A1
MAAA6	AY24	SMA_A6	SDQ_A2
MAAA7	AY23	SMA_A7	SDQ_A3
MAAA8	BB23	SMA_A8	SDQ_A4
MAAA9	BA22	SMA_A9	SDQ_A5
MAAA10	AY33	SMA_A10	SDQ_A6
MAAA11	BB22	SMA_A11	SDQ_A7
MAAA12	AW21	SMA_A12	
MAAA13	AY38	SMA_A13	SDQS_A1
MAAA14	BA21	SMA_A14	SDQS_A1#
			SDM_A1
-SWEA	-SWEA	SWE_A#	
-SCASA	-SCASA	SCAS_A#	
-SRASA	-SRASA	SRAS_A#	
SBA00	SBA00	SBS_A0	
SBA01	SBA01	SBS_A1	
SBA02	SBA02	SBS_A2	
-CSA0	-CSA0	SCS_A0#	
-CSA1	-CSA1	SCS_A1#	
-CSA2	-CSA2	SCS_A2#	
-CSA3	-CSA3	SCS_A3#	
CKEA0	CKEA0	SCKE_A0	
CKEA1	CKEA1	SCKE_A1	
CKEA2	CKEA2	SCKE_A2	
CKEA3	CKEA3	SCKE_A3	
MODT_A0	AY37	SODT_A0	
MODT_A1	BA30	SODT_A1	
MODT_A2	BB35	SODT_A2	
MODT_A3	BA39	SODT_A3	
DCLKA0	DCLKA0	SCLK_A0	
DCLKA0	DCLKA0	SCLK_A0#	
DCLKA1	DCLKA1	SCLK_A1	
DCLKA1	DCLKA1	SCLK_A1#	
DCLKA2	DCLKA2	SCLK_A2	
DCLKA2	DCLKA2	SCLK_A2#	
DCLKA3	DCLKA3	SCLK_A3	
DCLKA3	DCLKA3	SCLK_A3#	
DCLKA4	DCLKA4	SCLK_A4	
DCLKA4	DCLKA4	SCLK_A4#	
DCLKA5	DCLKA5	SCLK_A5	
DCLKA5	DCLKA5	SCLK_A5#	

DDR_0

P965-C1/QM62[10HB1-030082-30R]

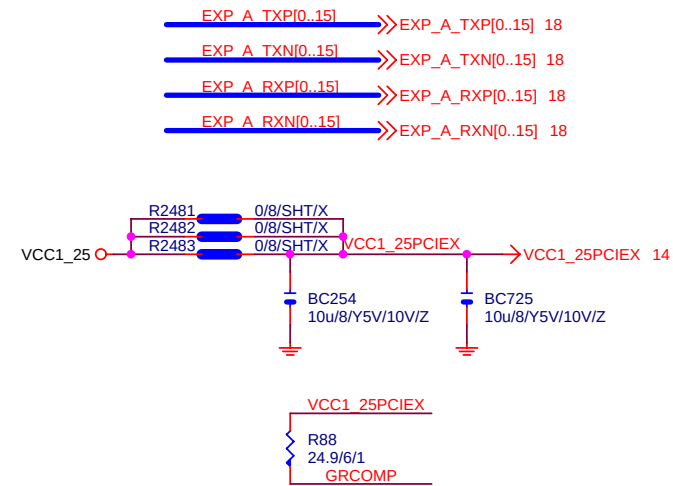
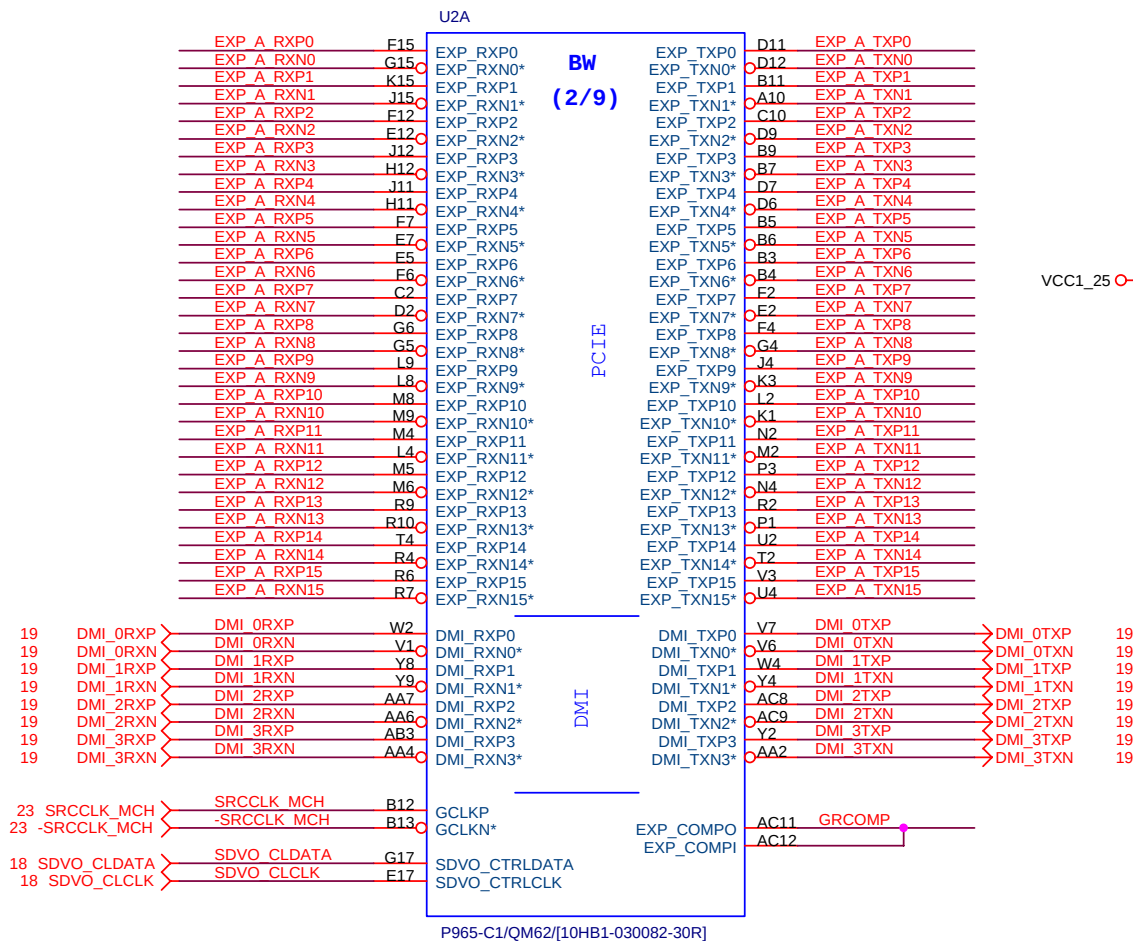
DDR INTERFACE

RESERVED

U2D

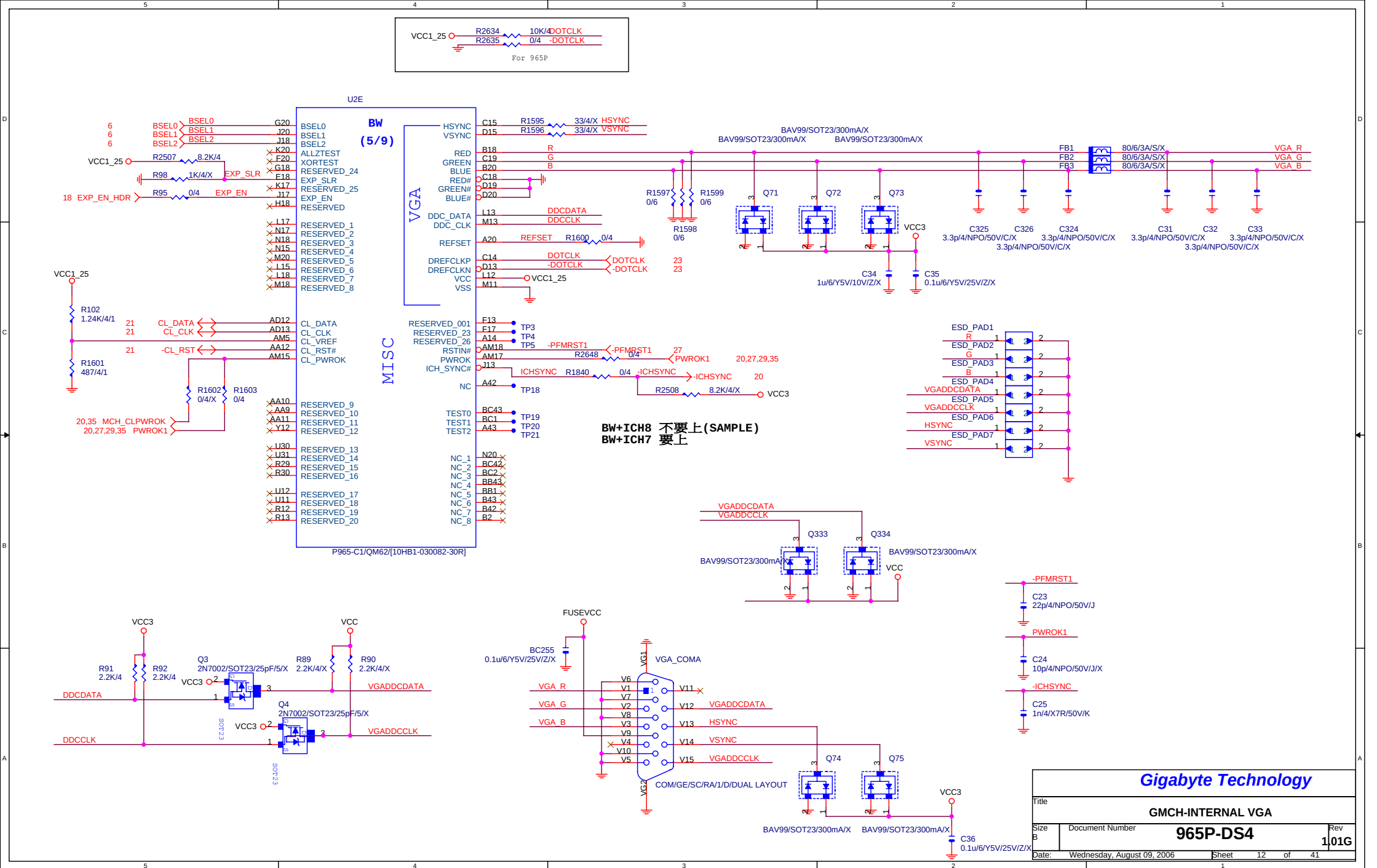
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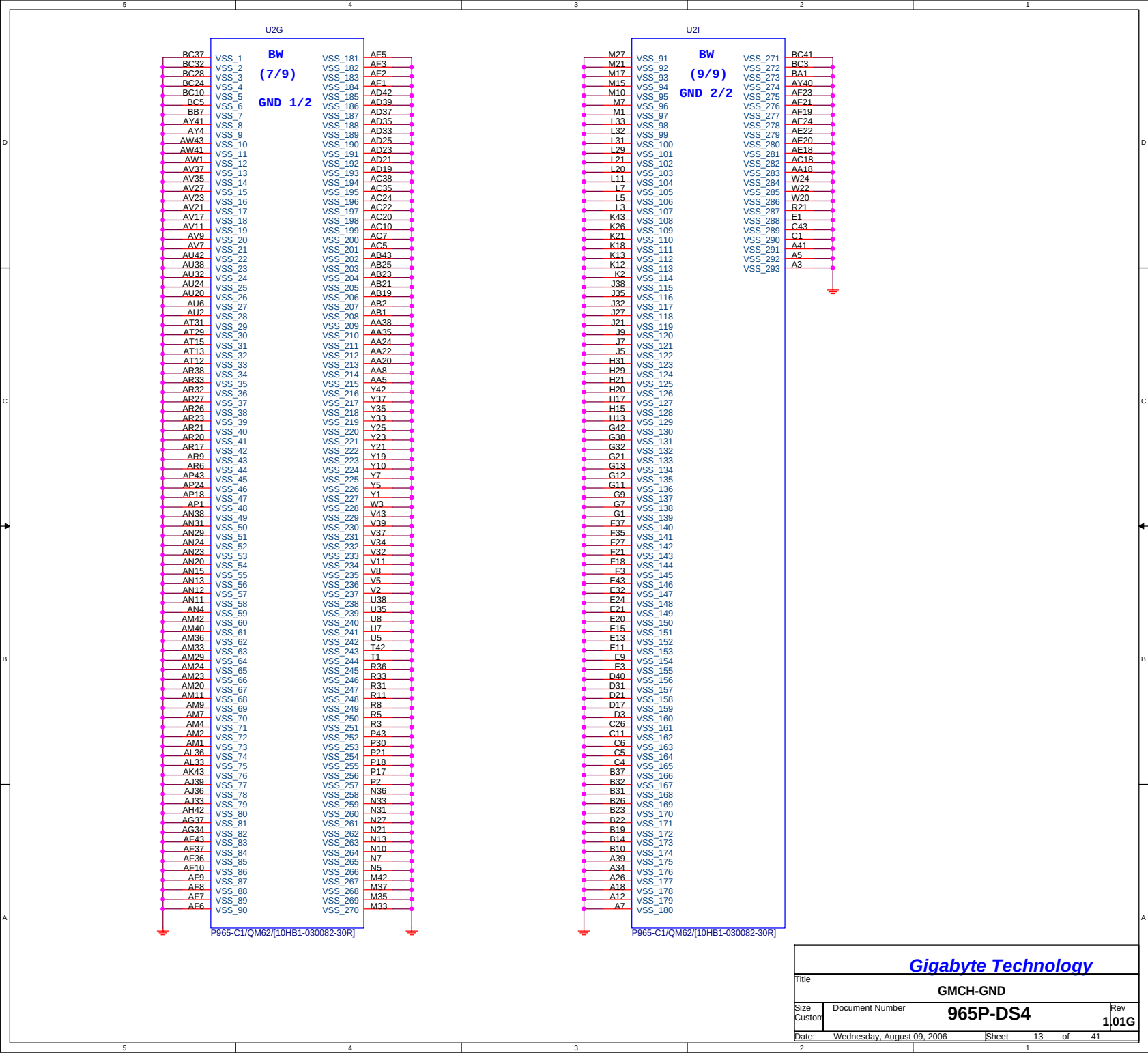
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		MAAB2	BA17	SMA_B2	SDM_B0	AB7	DMB0
		MAAB3	BC16	SMA_B3			
		MAAB4	AW15	SMA_B4	SDQ_B0	AN7	MDB0
		MAAB5	BA15	SMA_B5	SDQ_B1	AN8	MDB2
		MAAB6	BB15	SMA_B6	SDQ_B2	AW5	MDB2
		MAAB7	BA14	SMA_B7	SDQ_B3	AW7	MDB3
		MAAB8	AY15	SMA_B8	SDQ_B4	AN6	MDB4
		MAAB9	BB14	SMA_B9	SDQ_B5	AN8	MDB5
		MAAB10	AW18	SMA_B10	SDQ_B6	AN9	MDB7
		MAAB11	BB13	SMA_B11	SDQ_B7	AB7	MDB7
		MAAB12	BA13	SMA_B12			
		MAAB13	AY20	SMA_B13	SDQS_B1	AR12	DO5B1
		MAAB14	AY13	SMA_B14	SDQS_B1#	AP12	DO5B1
					SDM_B1	AW9	DMB1
16,17	-SWEB	-SWEB	BA27C	SWE_B#	SDQ_B8	AT11	MDB8
16,17	-SCASB	-SRASB	AW26C	SCAS_B#	SDQ_B8	AP11	MDB9
16	-SRASB			SRAS_B#	SDQ_B10	AR13	MDB11
16,17	SBAB0	SBAB0	AY19	SBS_B0	SDQ_B11	AR13	MDB11
16,17	SBAB1	SBAB1	BA18	SBS_B1	SDQ_B13	AU9	MDB13
16,17	SBAB2	SBAB2	BC12	SBS_B2	SDQ_B14	AV12	MDB14
					SDQ_B14	AT12	MDB15
16,17	-CSB0	-CSB0	BB27C	SCS_B0#	SDQ_B2	AP15	DO5B2
16,17	-CSB1	-CSB1	BB30C	SCS_B1#	SDQ_B2	AR15	DO5B2
16,17	-CSB2	-CSB2	AV27C	SCS_B2#	SDQ_B5	AW12	DMB2
16,17	-CSB3	-CSB3	AY34C	SCS_B3#			
16,17	CKEB0	CKEB0	AY12	SCKE_B0	SDQ_B8	AT15	MDB16
16,17	CKEB1	CKEB1	AW12	SCKE_B1	SDQ_B16	AU15	MDB16
16,17	CKEB2	CKEB2	BB11	SCKE_B2	SDQ_B17	AV13	MDB17
16,17	CKEB3	CKEB3	BA11	SCKE_B3	SDQ_B19	AT17	MDB19
	MODT_B0	BA20		SODT_B0	SDQ_B19	AT17	MDB19
	MODT_B1	BA30		SODT_B1	SDQ_B20	AM13	MDB21
	MODT_B2	BB20		SODT_B2	SDQ_B21	AW15	MDB22
	MODT_B3	BB31		SODT_B3	SDQ_B22	AV17	MDB22
					SDQ_B23		
16	DCLKB0	DCLKB0	AV31	SCLK_B0	SDQS_B3	AT24	DO5B3
16	DCLKB0	DCLKB0	AW31C	SCLK_B0#	SDQS_B3#	AT26	DO5B3
16	DCLKB1	DCLKB1	SCLK_B1	SCLK_B1	SDQ_B18	AP23	DMB3
16	DCLKB1	DCLKB1	AT17C	SCLK_B1#	SCLK_B2		
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16	DCLKB2	DCLKB2	AT32C	SCLK_B2#	SDQ_B24	AV23	MDB25
16	DCLKB3	DCLKB3	AT32C	SCLK_B3	SDQ_B26	AT26	MDB26
16	DCLKB3	DCLKB3	AR20C	SCLK_B3#	SDQ_B26	AT26	MDB26
16	DCLKB4	DCLKB4	AW27C	SCLK_B4	SDQ_B27	AT26	MDB27
16	DCLKB4	DCLKB4	AW27C	SCLK_B4#	SDQ_B28	AT23	MDB28
16	DCLKB5	DCLKB5	AN34C	SCLK_B5	SDQ_B29	AR24	MDB30
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					SDQ_B31		
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					SDM_B4	AU39	DO5B4
						AW7	DMB4
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					SDQ_B33	AN36	MDB34
					SDQ_B34	AN37	MDB35
					SDQ_B35	AN37	MDB35
					SDQ_B36	AR35	MDB37
					SDQ_B37	AR37	MDB39
					SDQ_B38	AN37	MDB39
					SDQ_B39		
					SDQS_B5	AL35	DO5B5
					SDQS_B5#	AL34	DO5B5
					SDM_B5	AM37	DMB5
					SDQ_B40	AM35	MDB40
					SDQ_B41	AM38	MDB41
					SDQ_B42	AL38	MDB43
					SDQ_B44	AR39	MDB44
					SDQ_B45	AM34	MDB45
					SDQ_B46	AL37	MDB46
					SDQ_B47	AL32	MDB47
					SDQS_B6	AG36	DO5B6
					SDQS_B6#	AG39	DMB6
					SDM_B6		
					SDQ_B48	AG38	MDB48
					SDQ_B49	AF35	MDB50
					SDQ_B50	AF35	MDB50
					SDQ_B51	AF34	MDB51
					SDQ_B52	AL37	MDB52
					SDQ_B53	AJ36	MDB54
					SDQ_B54	AF34	MDB55
					SDQ_B55		
					SDQS_B7	AC36	DO5B7
					SDQS_B7#	AC37	DO5B7
					SDM_B7	AC38	DMB7
					SDQ_B56	AC36	MDB56
					SDQ_B57	AC33	MDB57
					SDQ_B58	AC36	MDB59
					SDQ_B59	AD34	MDB60
					SDQ_B60	AD34	MDB60
					SDQ_B61	AC34	MDB62
					SDQ_B62	AC33	MDB63
					SDQ_B63		
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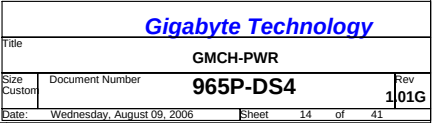
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Size	Document Number	Rev	
Custom	965P-DS4	1.01G	
Date:	Wednesday, August 09, 2006	Sheet	11 of 41

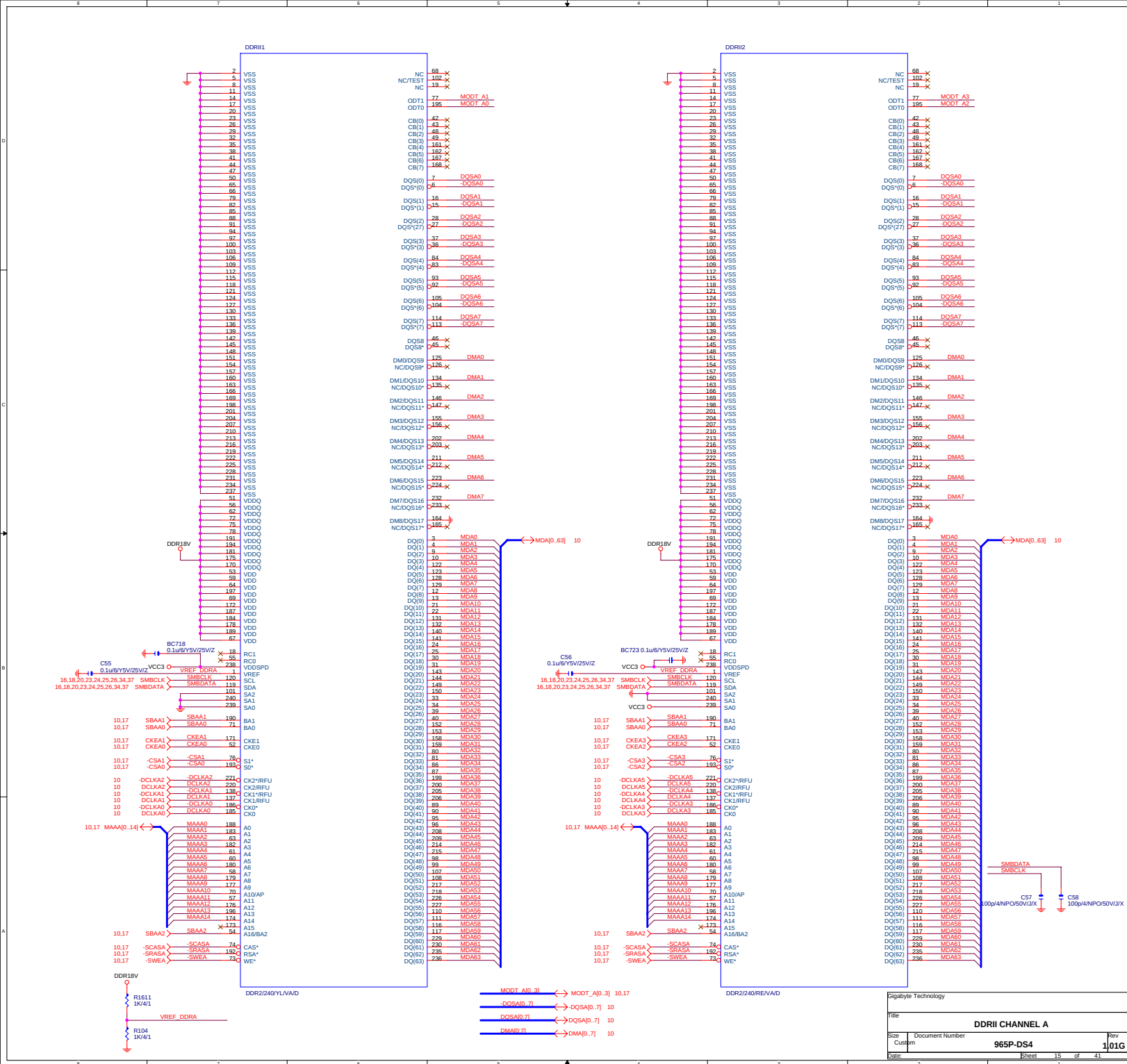


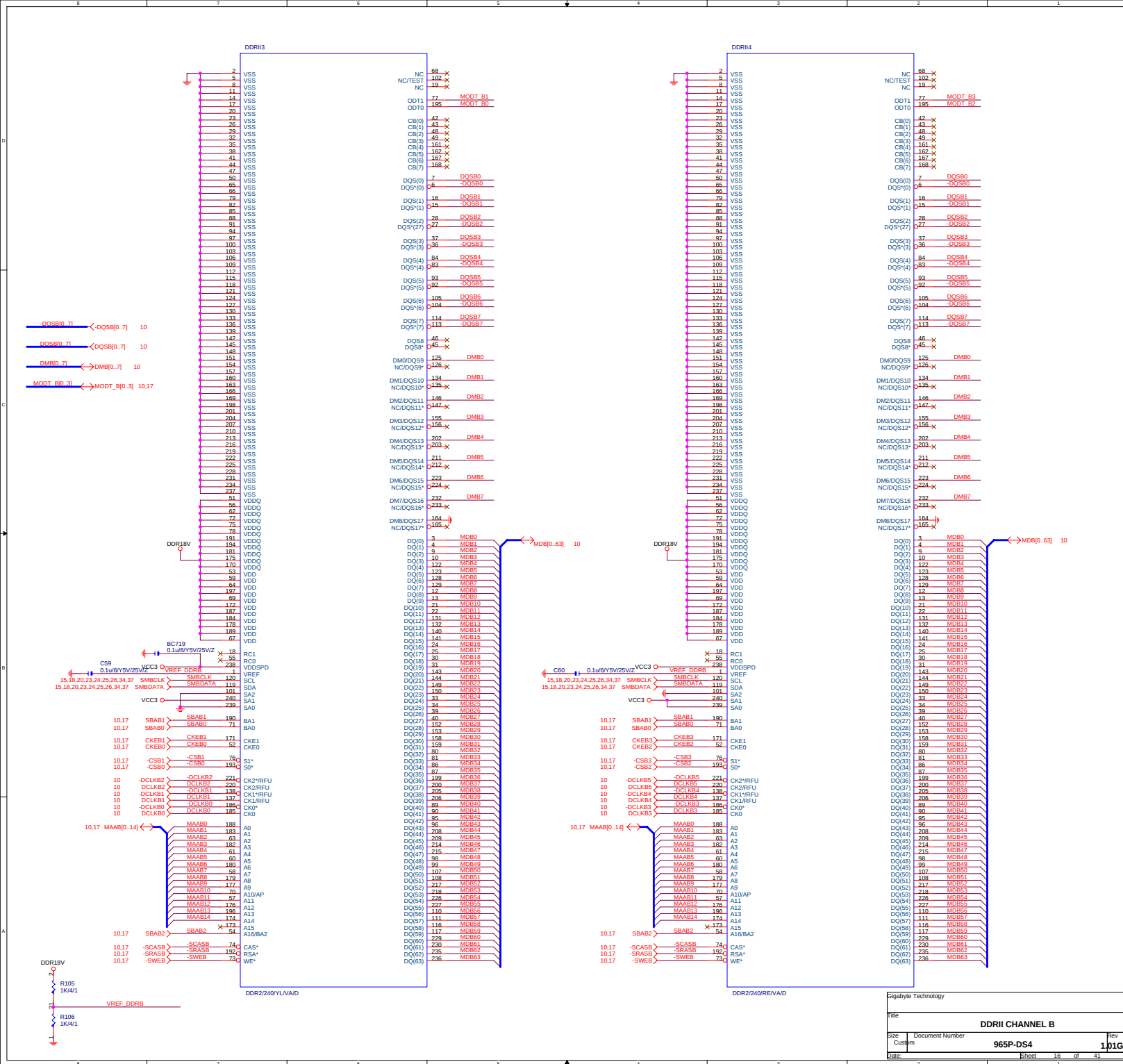


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Custom			1,01G
Date:	Wednesday, August 09, 2006	Sheet	13 of 41

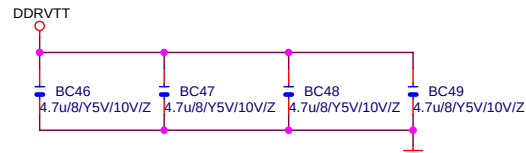
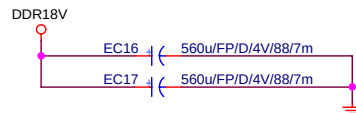
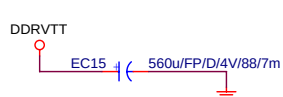






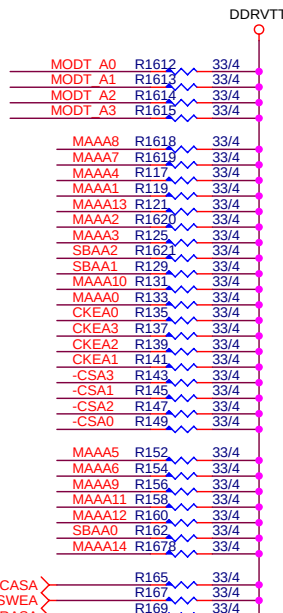
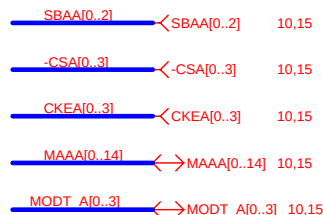
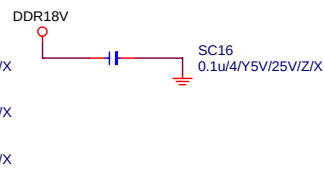
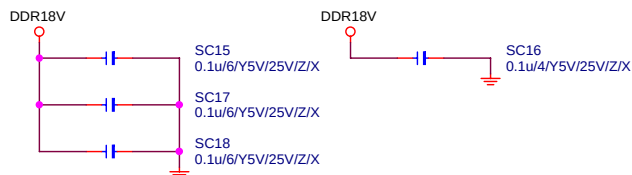
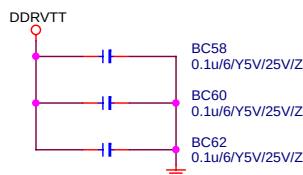
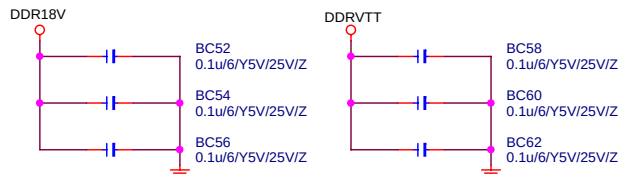
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

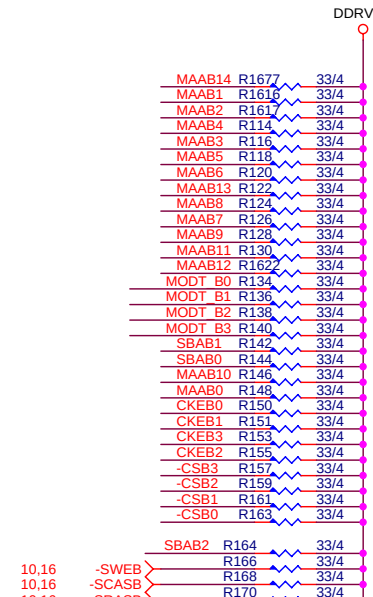
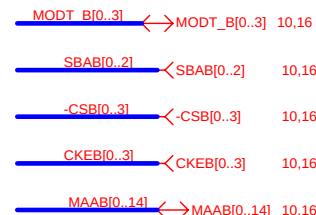
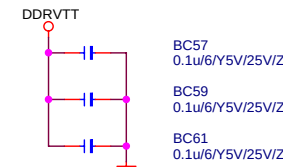
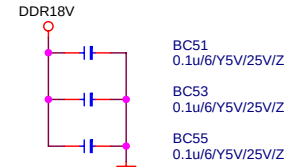
DDRVTT Decouple



DDR TERMINATION CHANNEL B

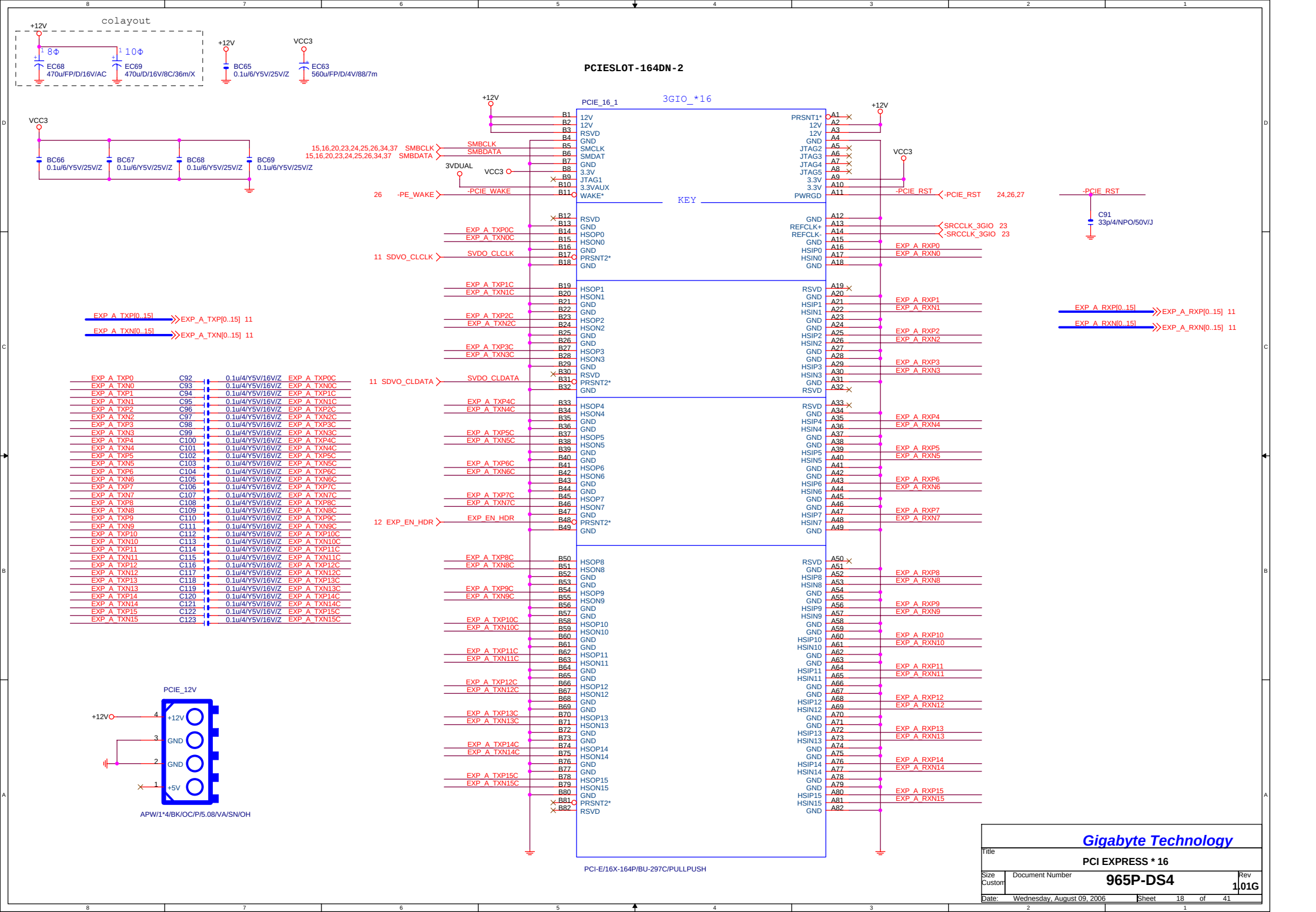
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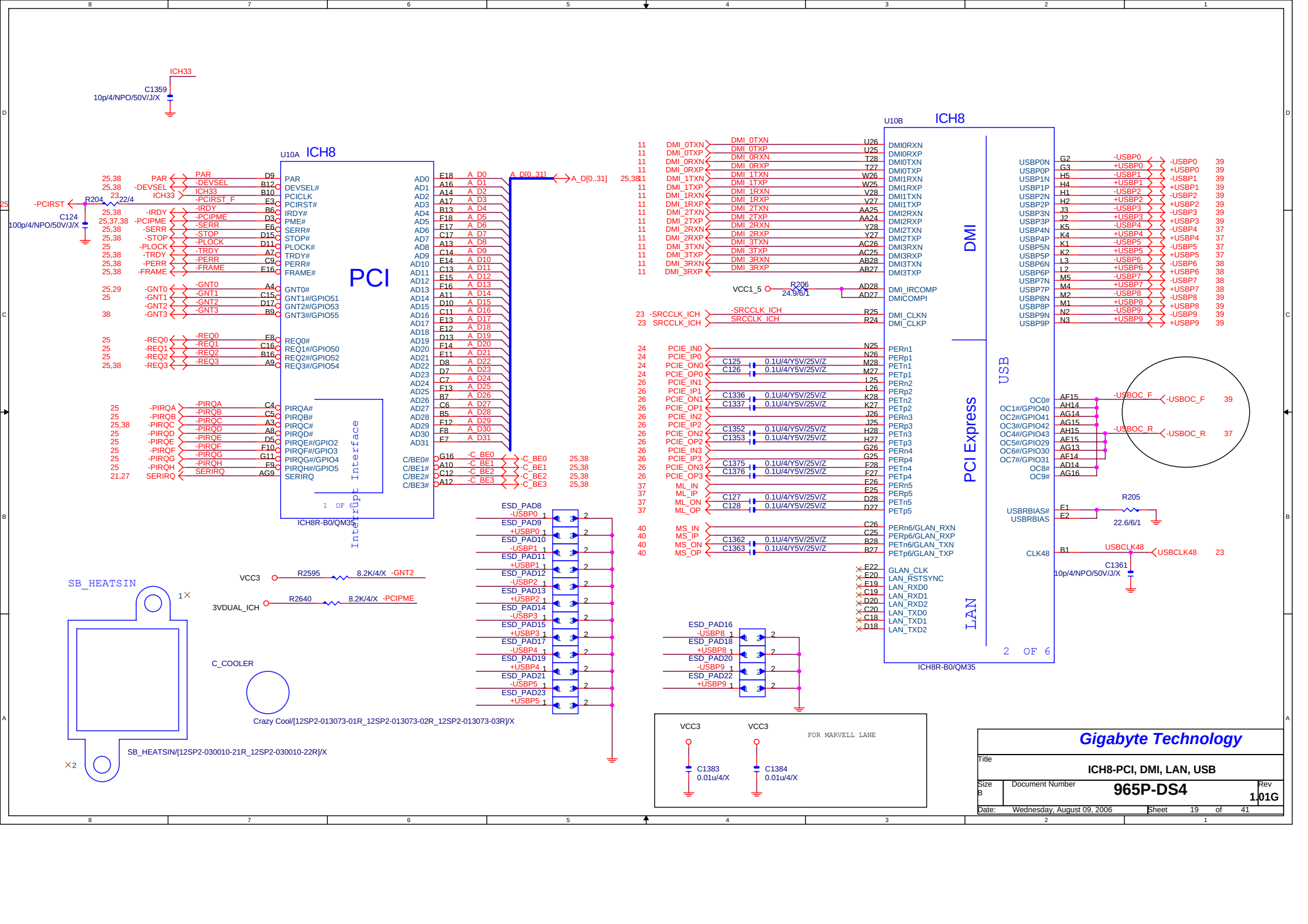
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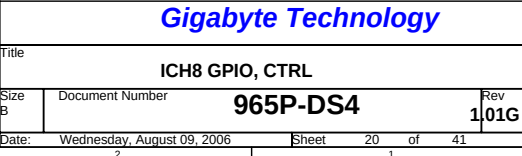


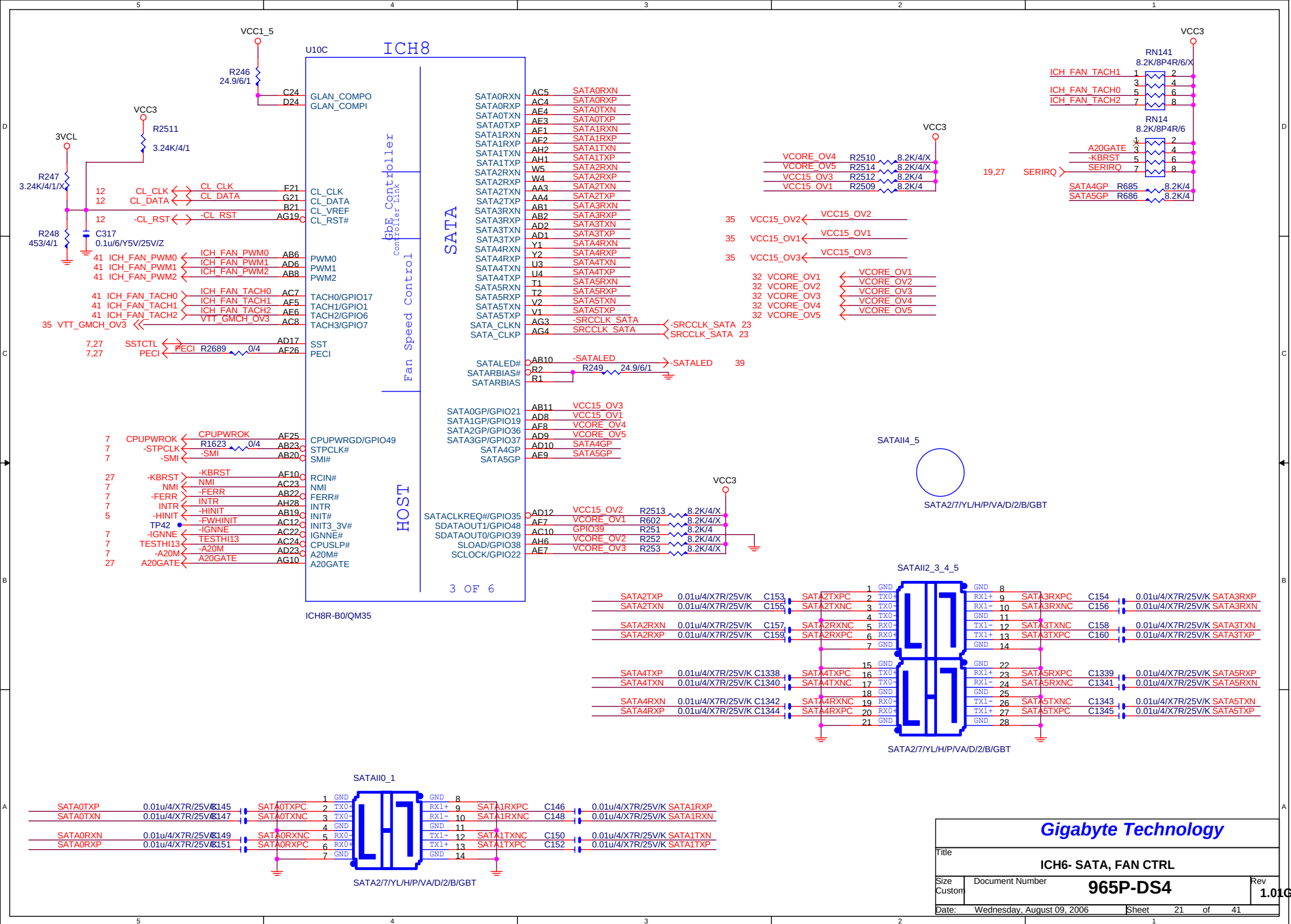
Gigabyte Technology

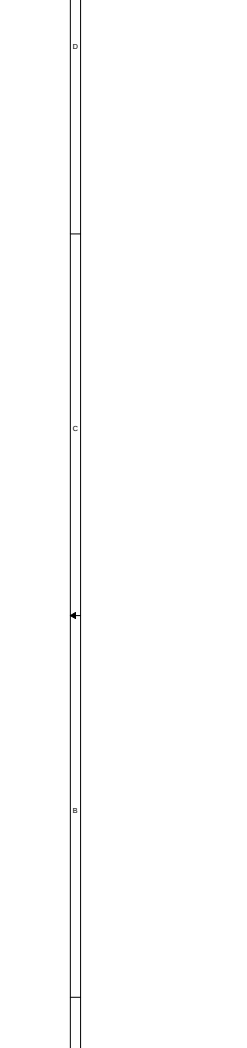
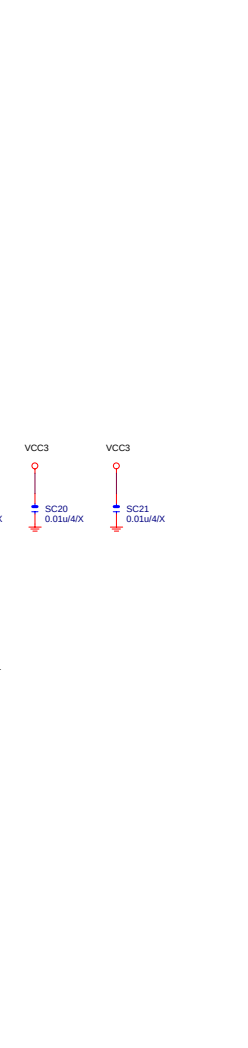
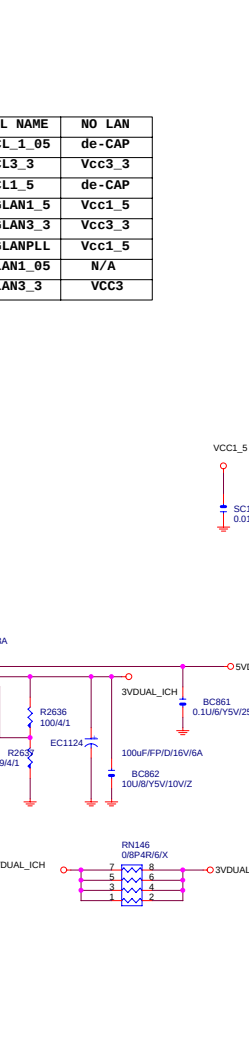
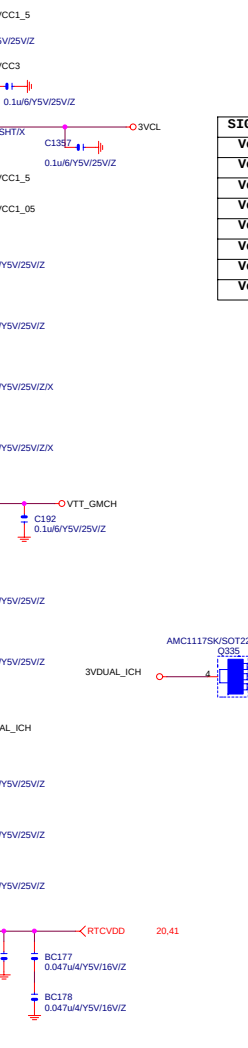
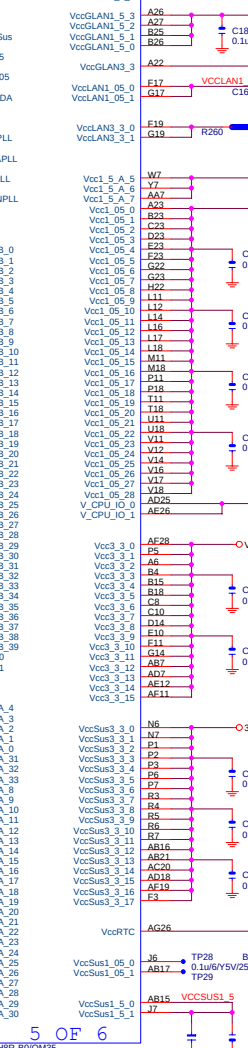
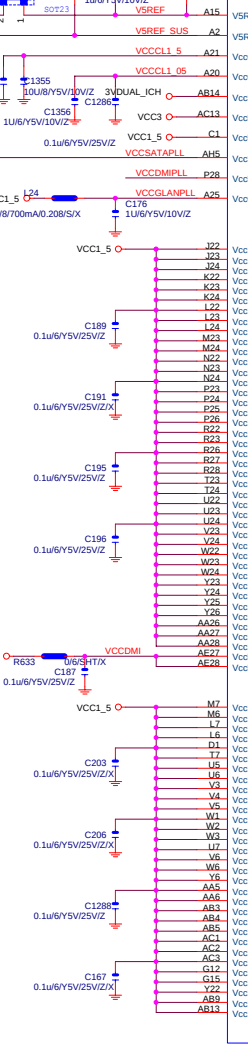
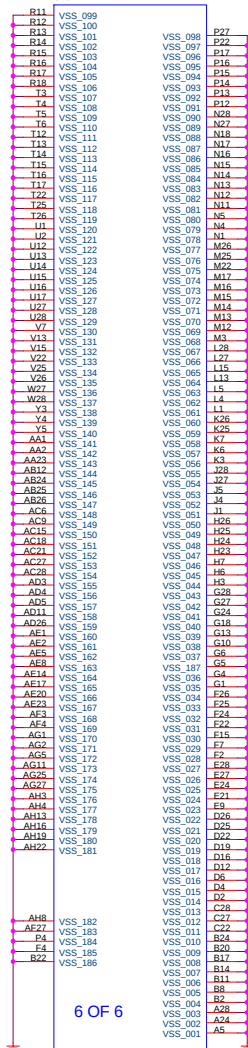
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Size	Document Number	965P-DS4	
Custom		Rev 101G	
Date:	Wednesday, August 09, 2006	Sheet	17 of 41



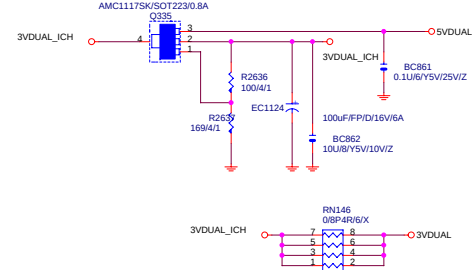




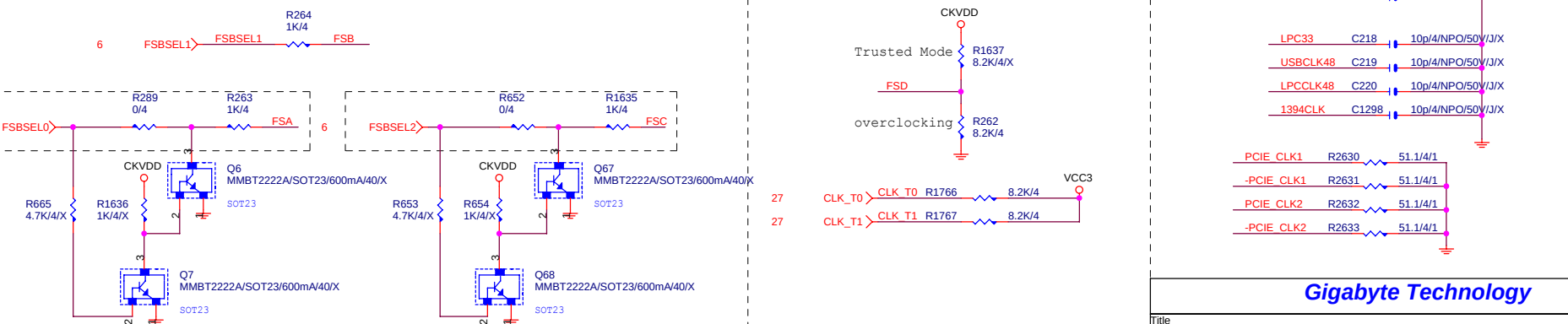
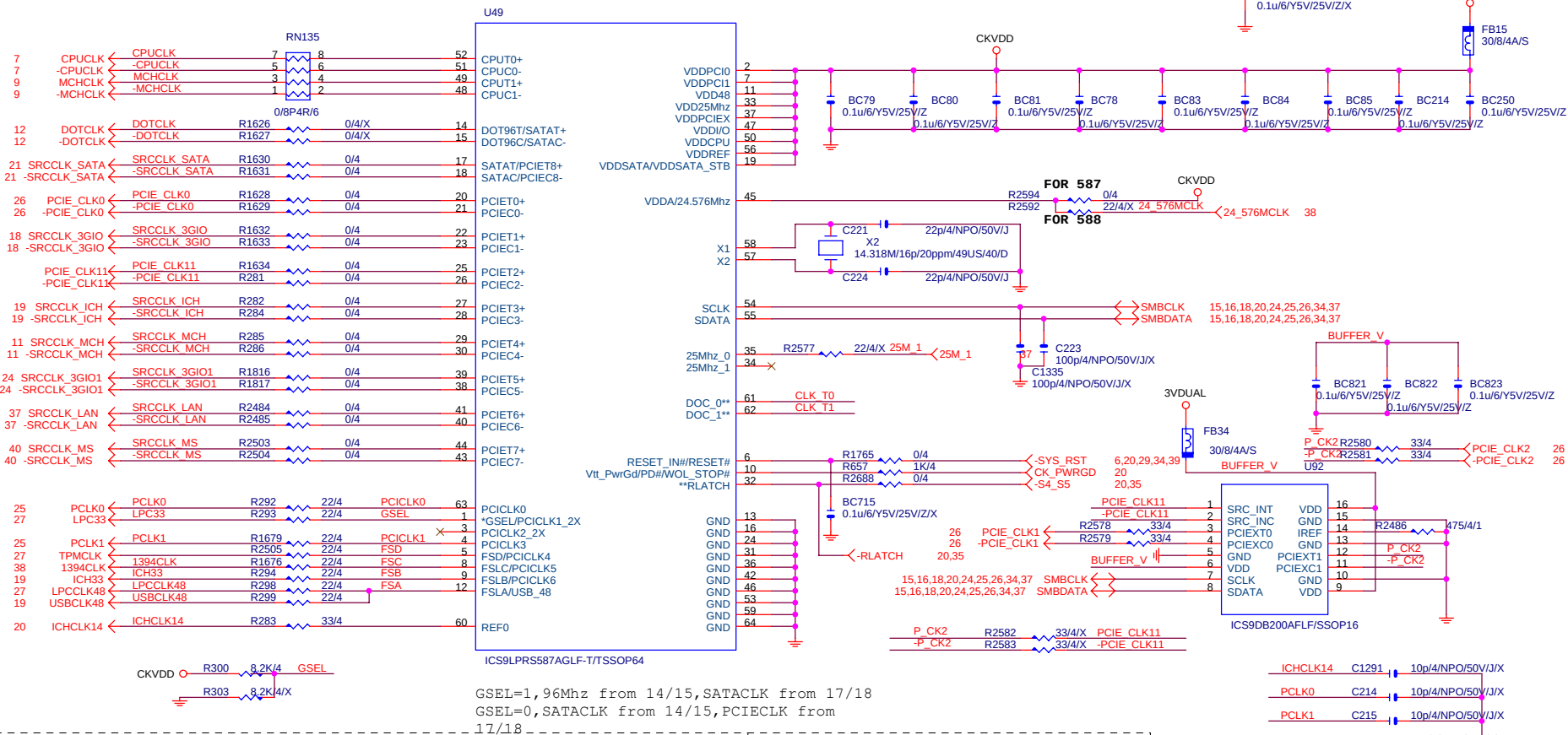




SIGNAL NAME	NO LAN
VccCL1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3

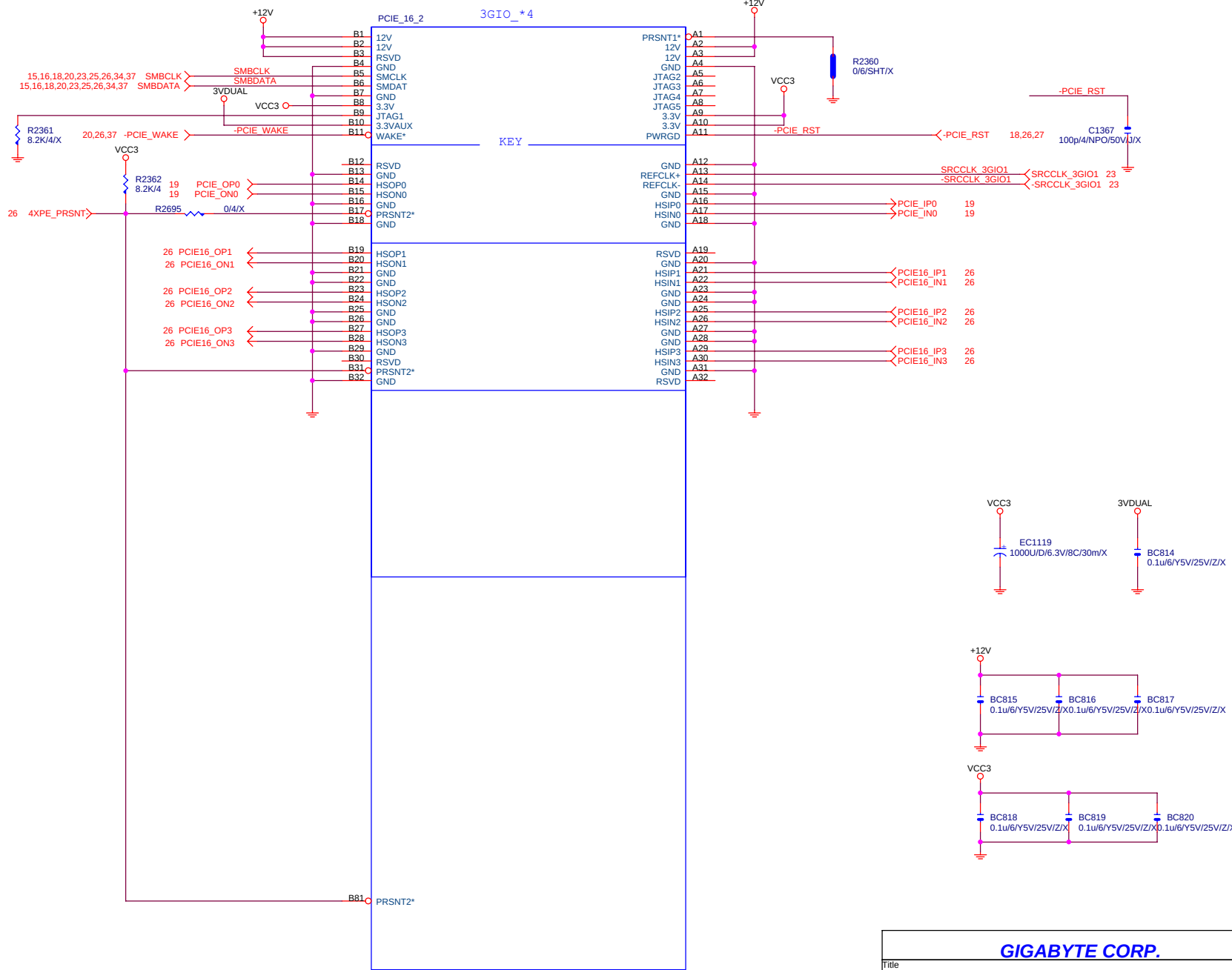
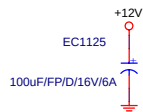


CLK GEN CK505



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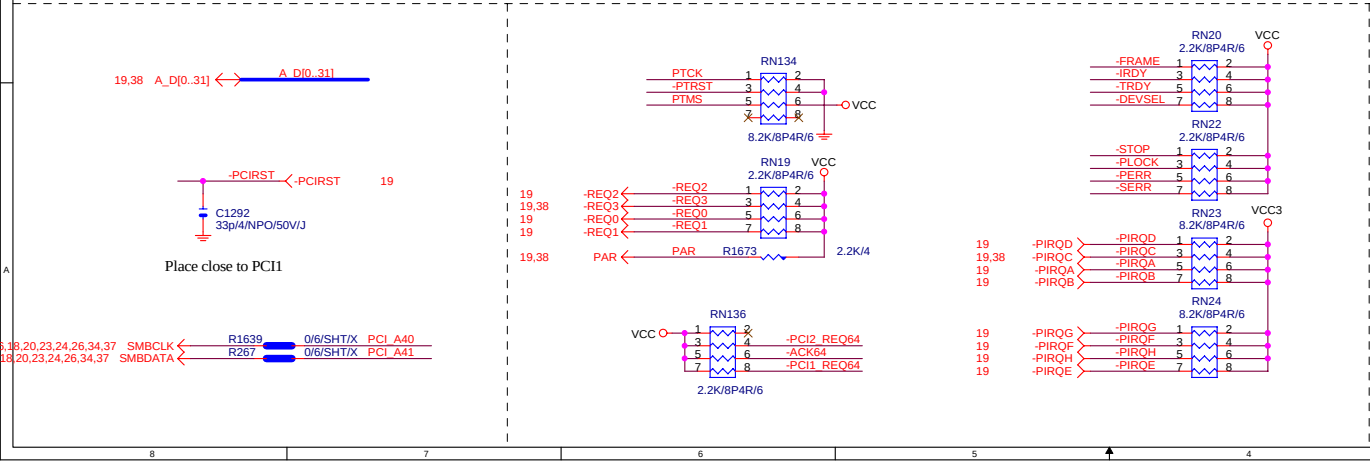
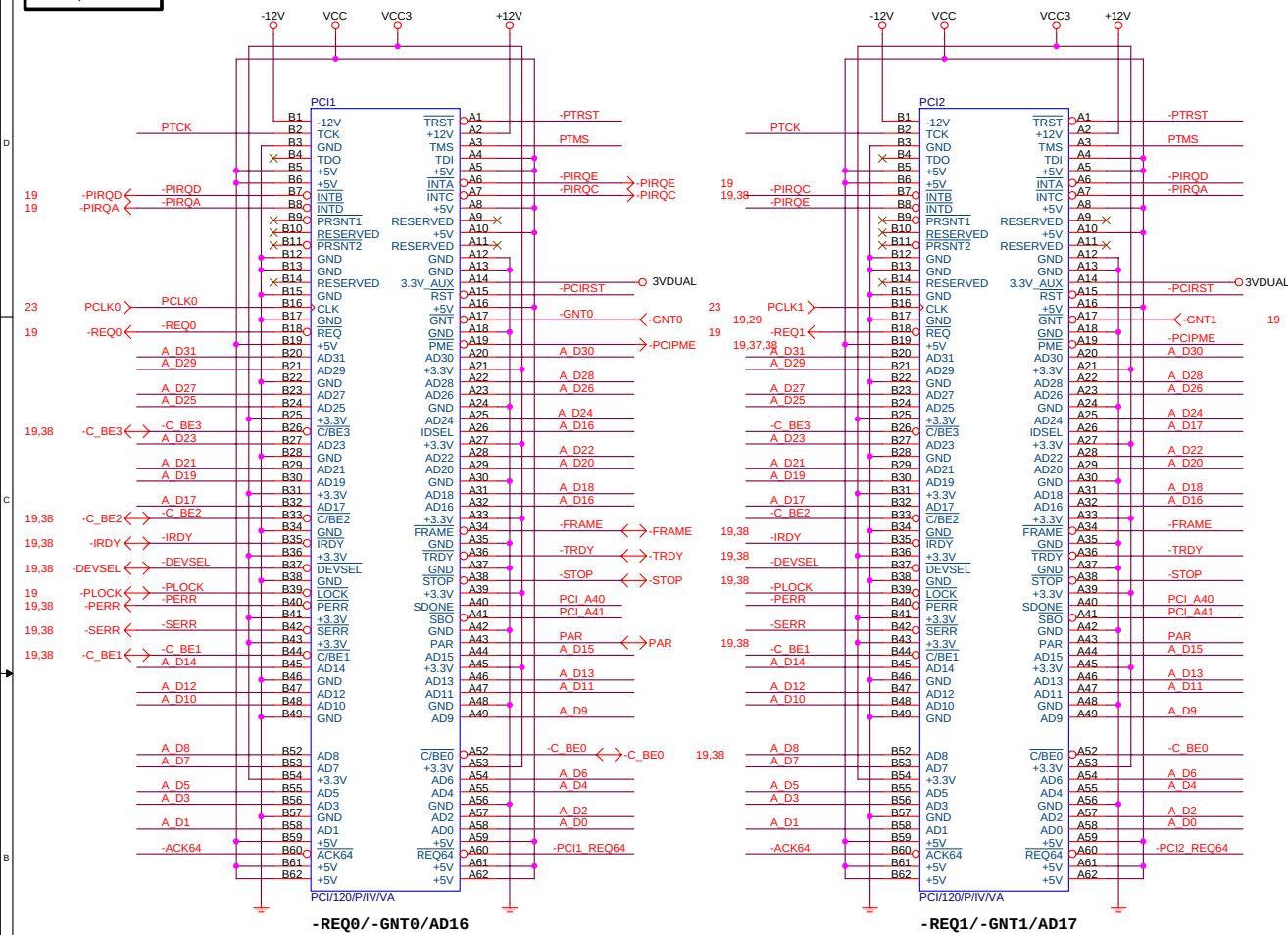
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Custom		Rev 1.01G	
Date:	Wednesday, August 09, 2006	Sheet	23 of 41



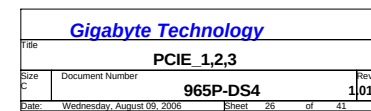
PCI-E/16X-65P/BU/RIGHT PUSH

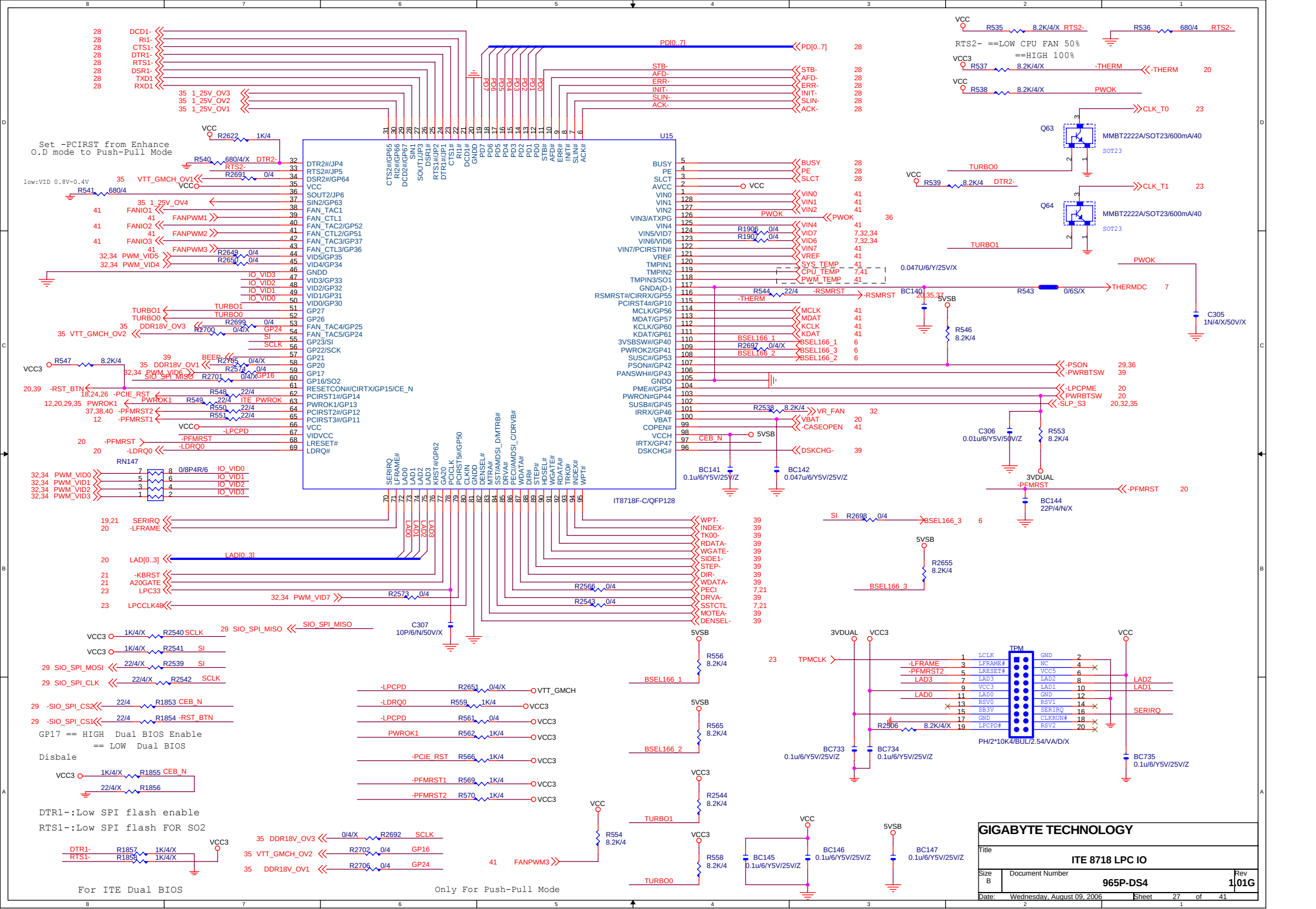
GIGABYTE CORP.			
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Size	Document Number	Rev	
Custom	965P-DS4	1.01G	
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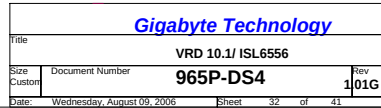
PCI1, 2 SLOT

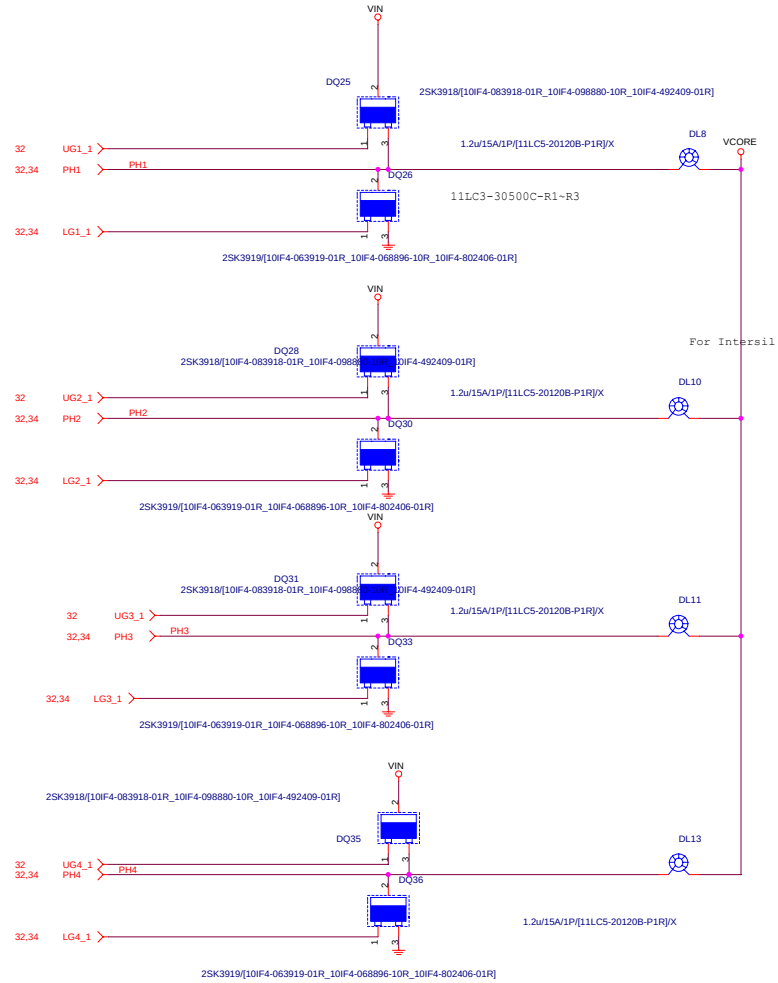
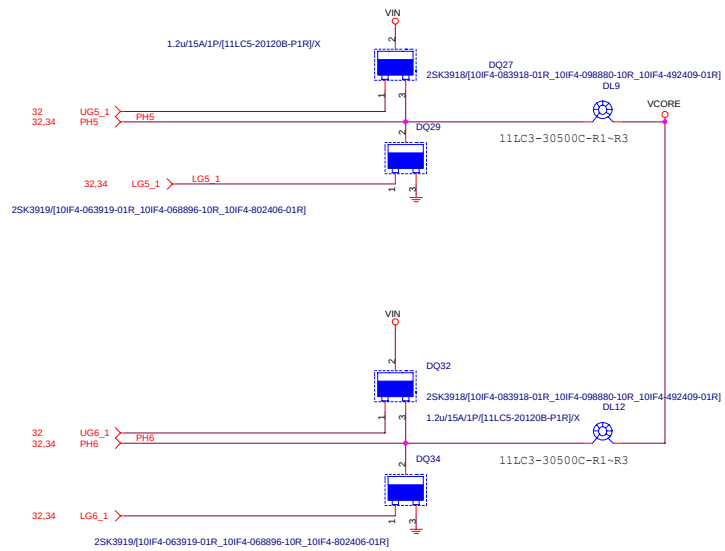
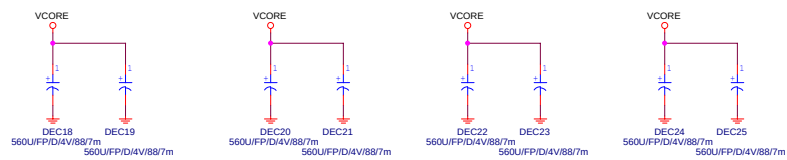


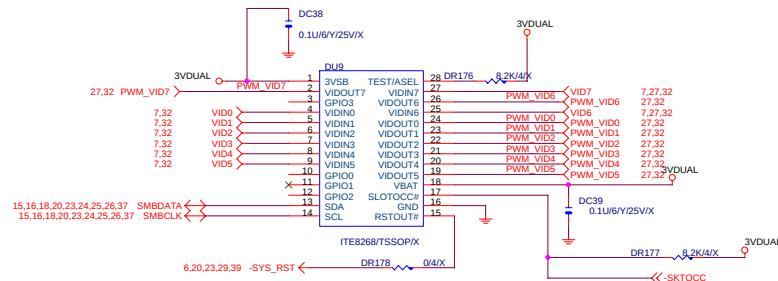
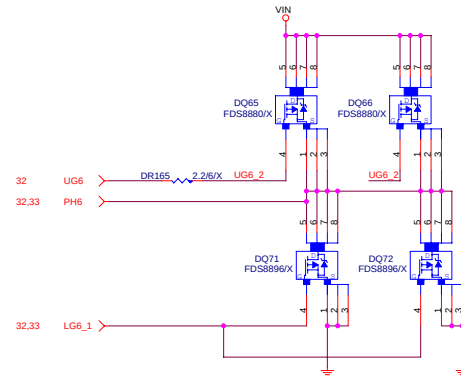
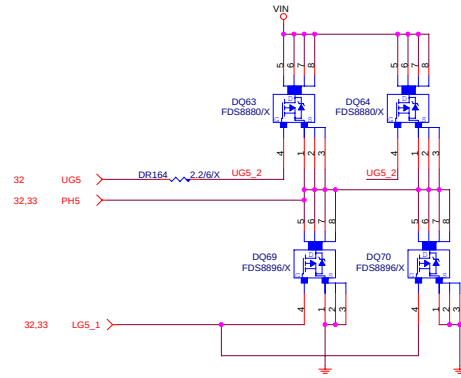
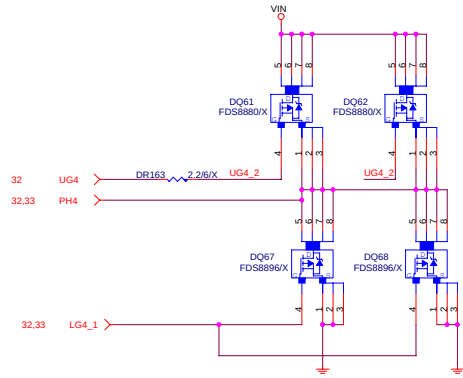
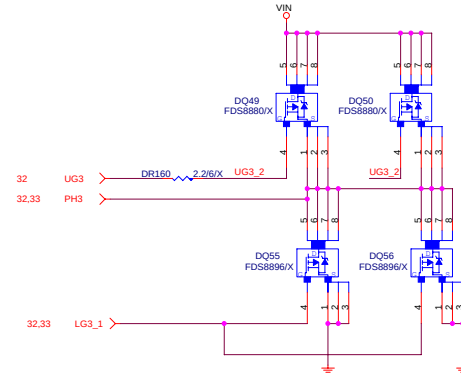
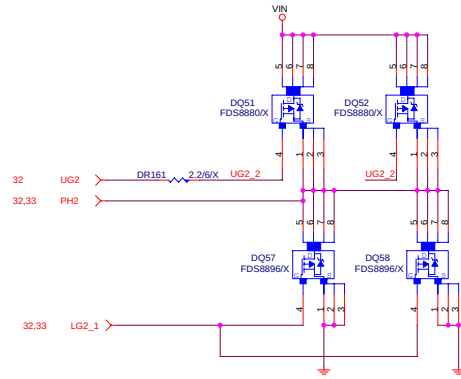
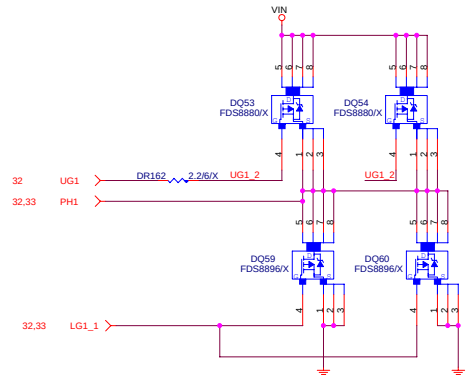
For Vih level consideration



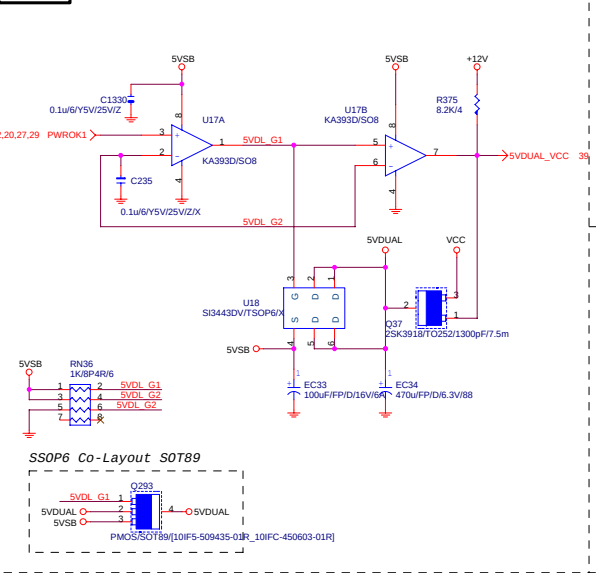




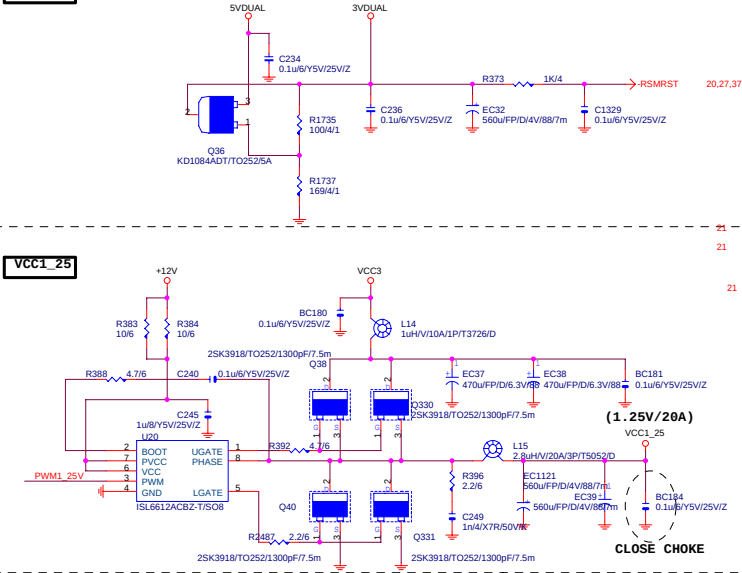




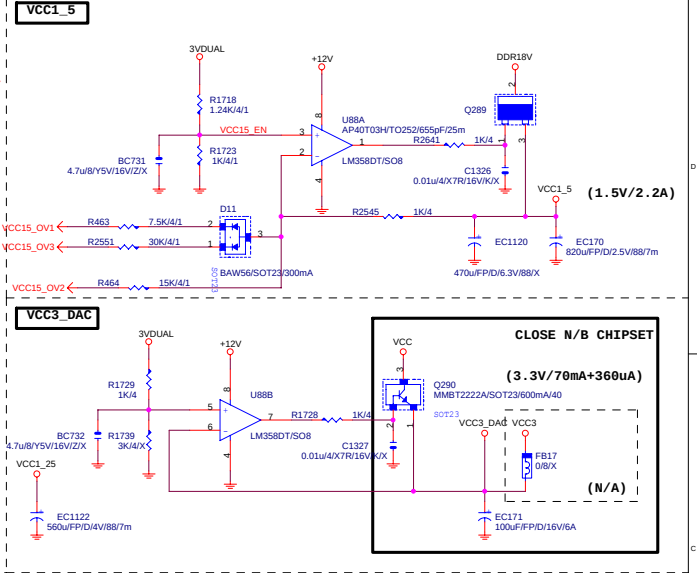
5VDUAL



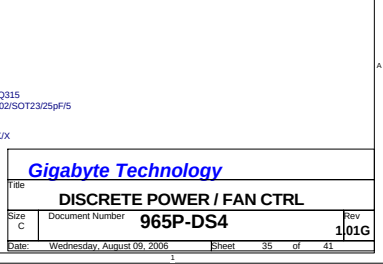
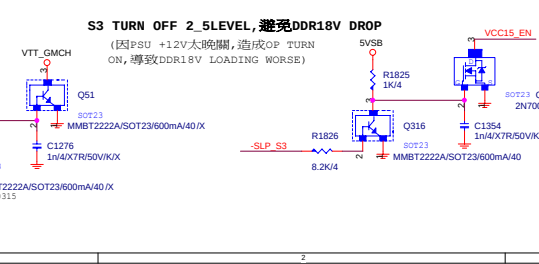
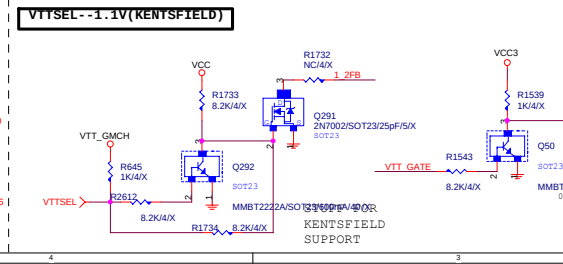
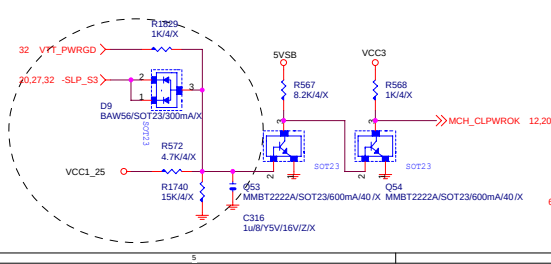
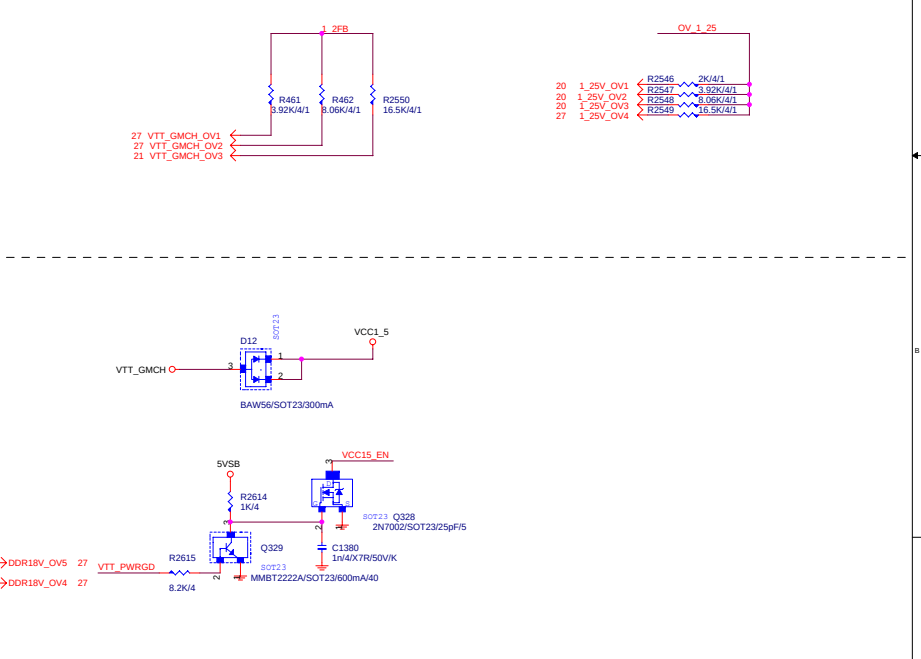
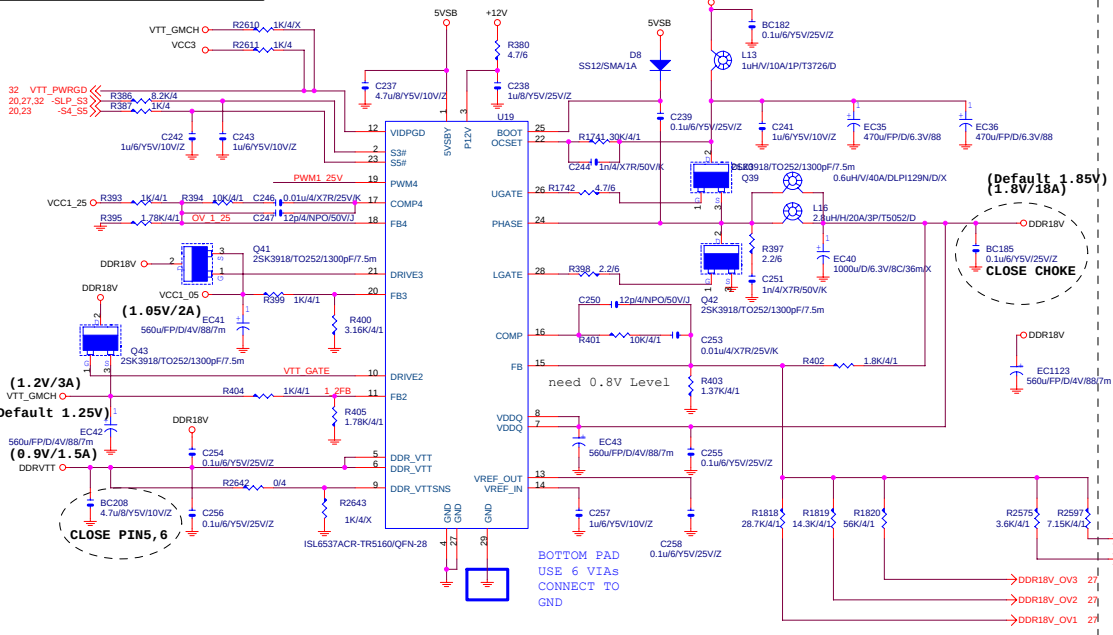
3VDUAL



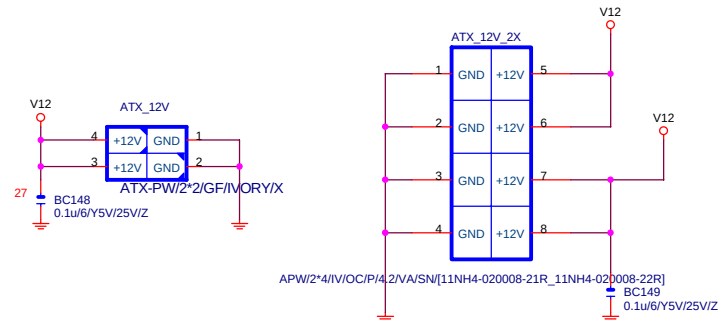
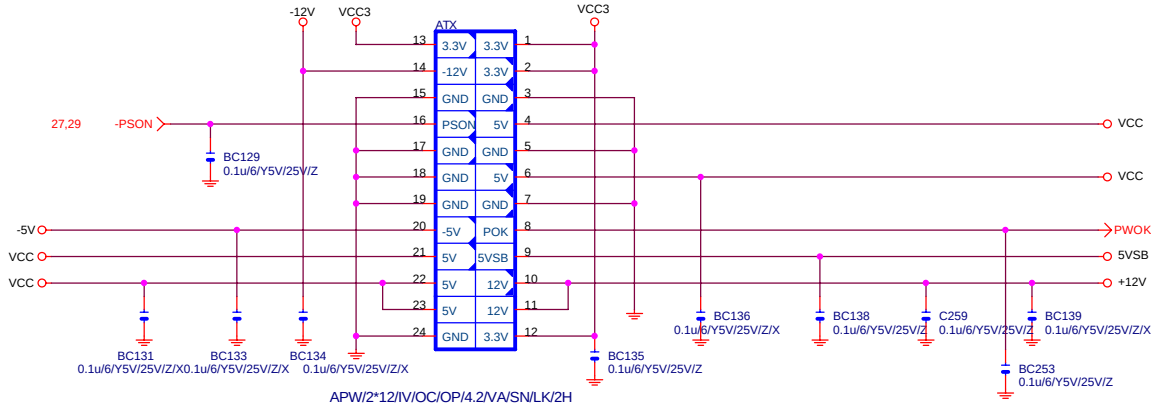
VCC1_5



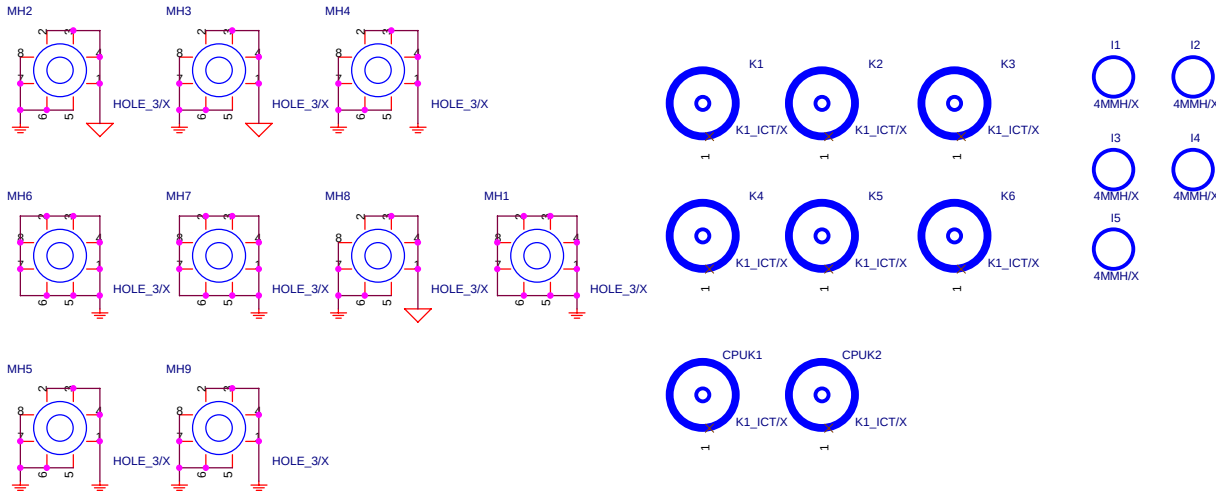
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ATX POWER CONNECTOR



HOLE_3-2--->有鉛



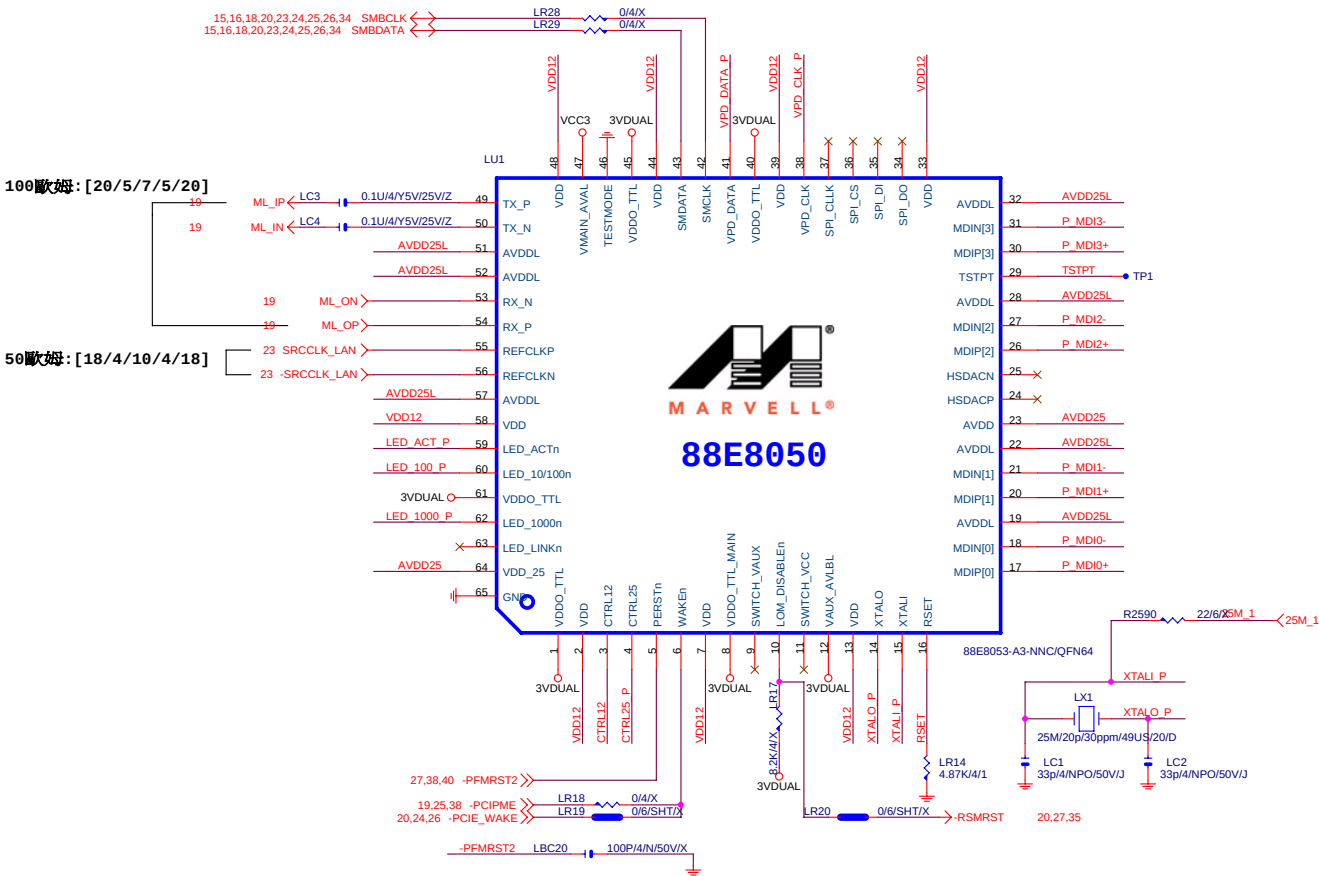
PCIE-16 LAN

Layout Check 注意事項

1. LU1 PIN65 需下內層GND,打12 VIA
2. 3VDUAL, VCC3, VDD15 L, AVDD25 L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8, 每對之間保持 40mil

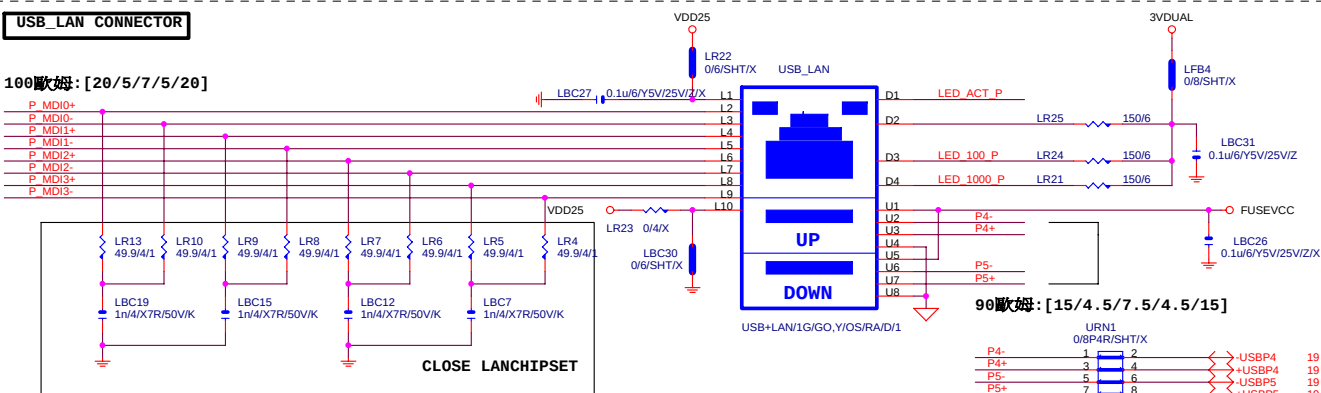
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50歐母:[18/4/10/4/18]

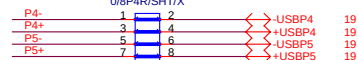


USB LAN CONNECTOR

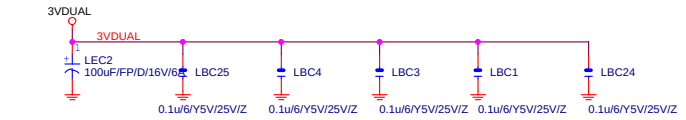
100歐母:[20/5/7/5/20]



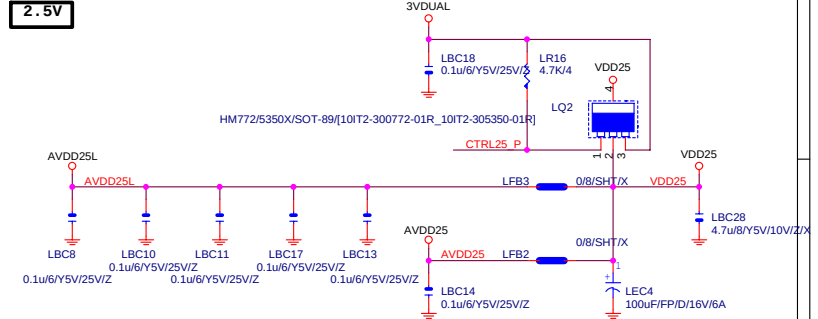
90歐母:[15/4.5/7.5/4.5/15]



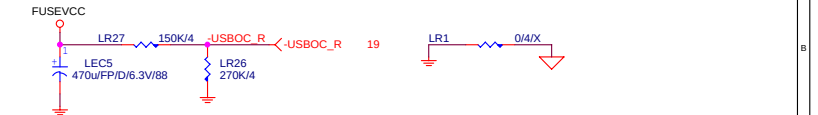
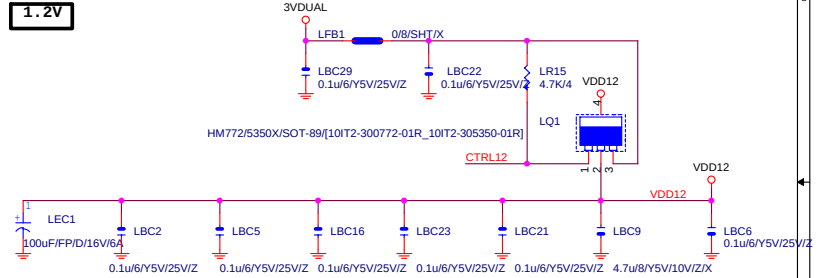
3VDUAL



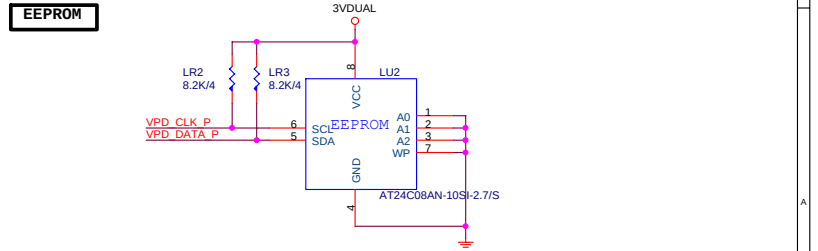
2.5V



1.2V

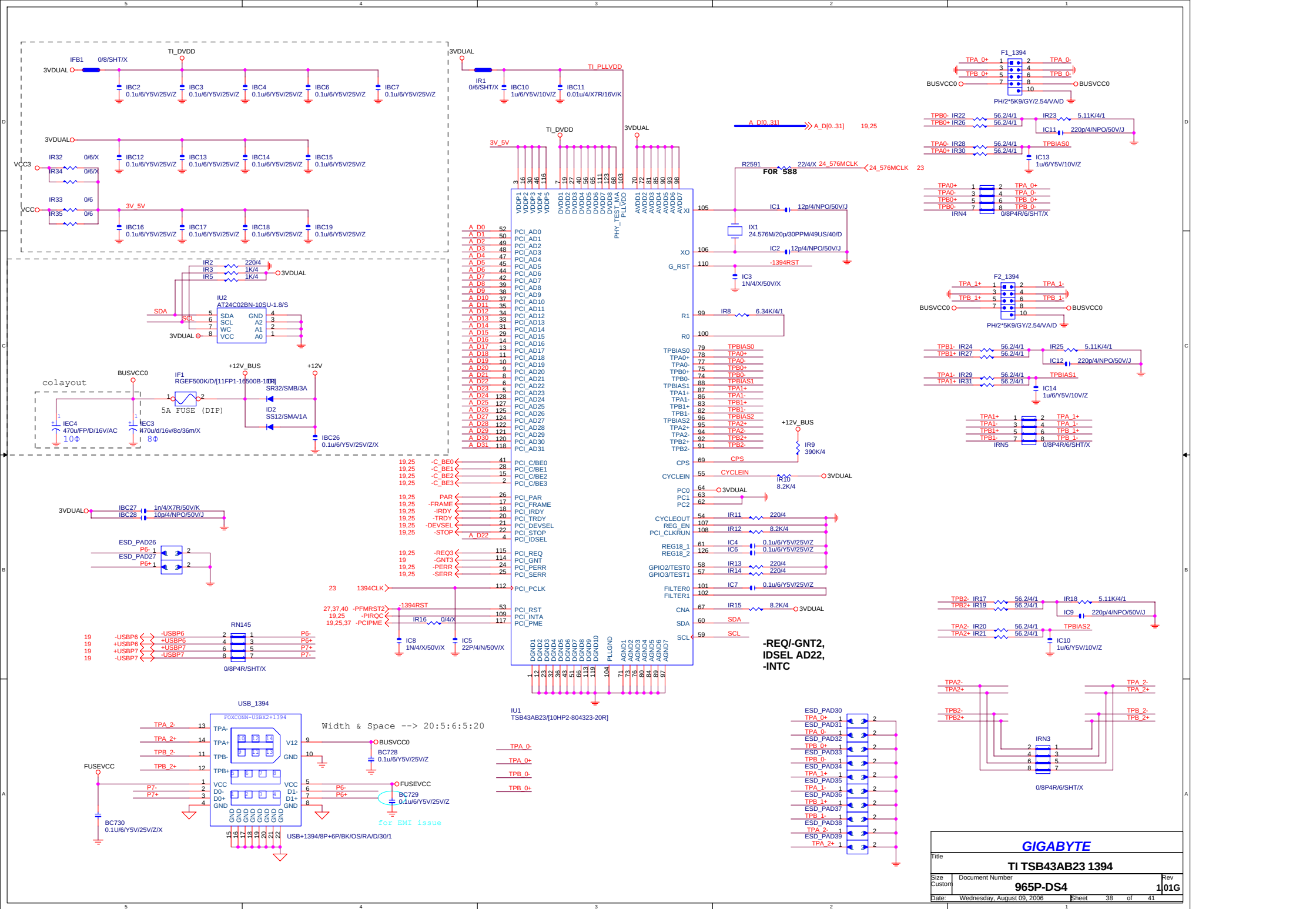


EEPROM

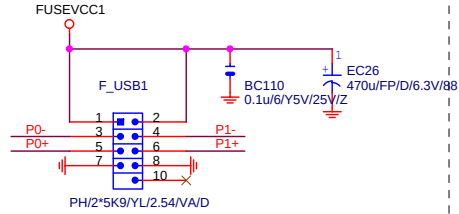
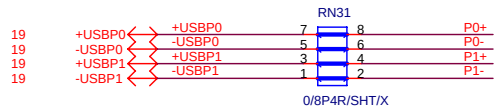


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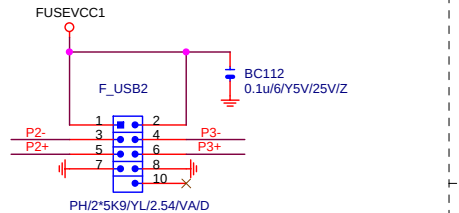
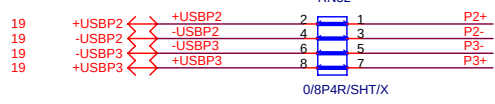
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Size	Document Number	965P-DS4	Rev 1.01G
Custom			
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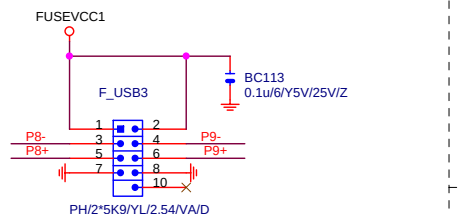
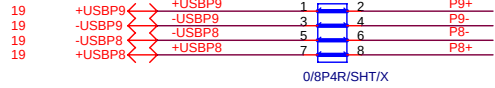
FRONT USB1



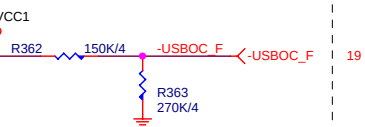
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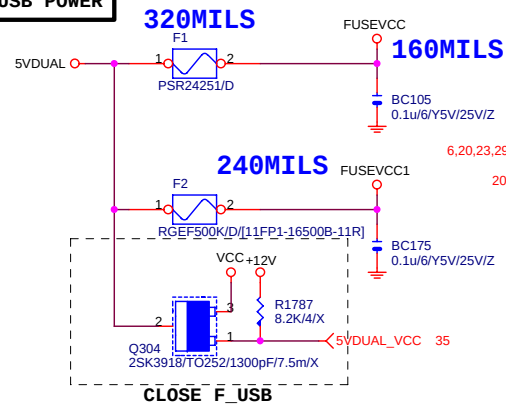
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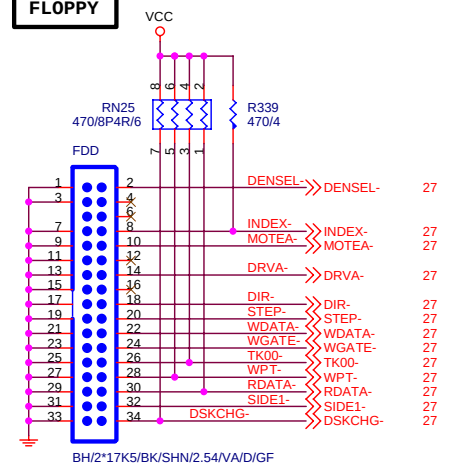
FRONT USB OC1



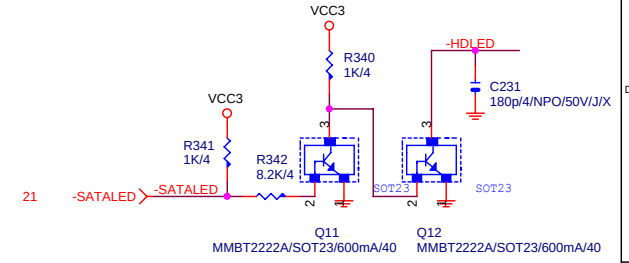
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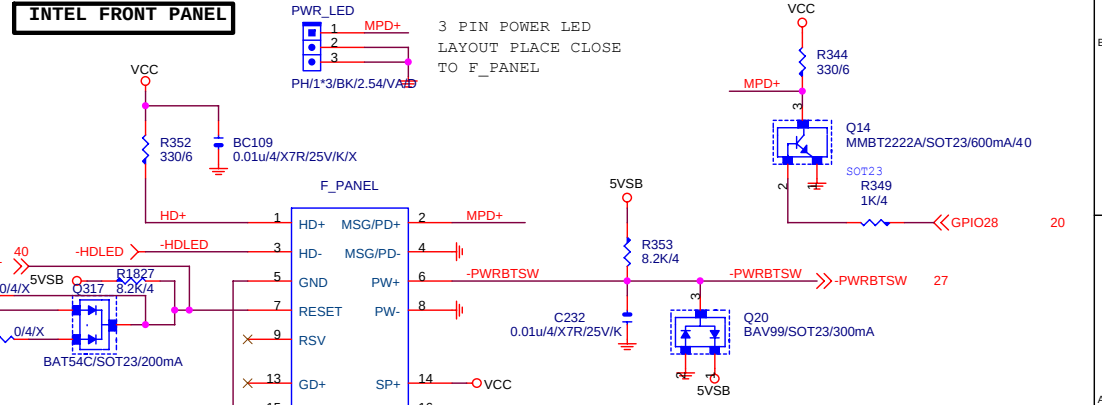
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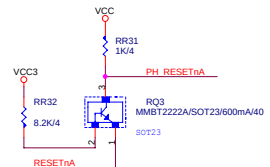
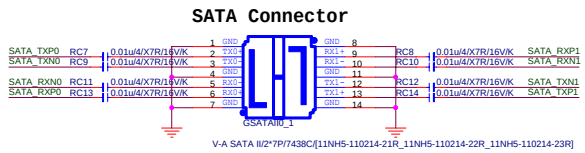
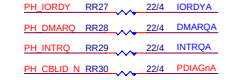
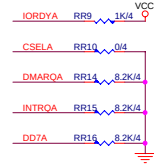
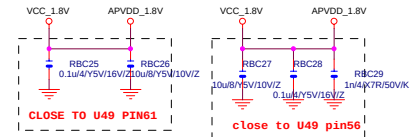
SATA LED



INTEL FRONT PANEL

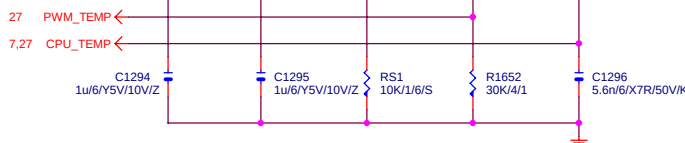


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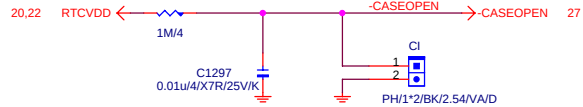


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TEMP H/W MONITOR

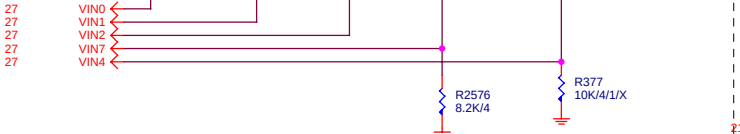


CASE OPEN

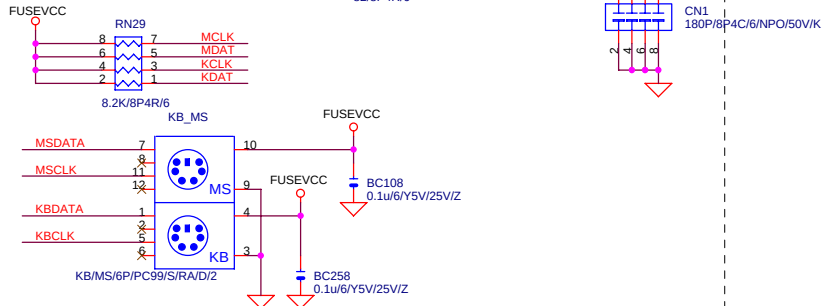


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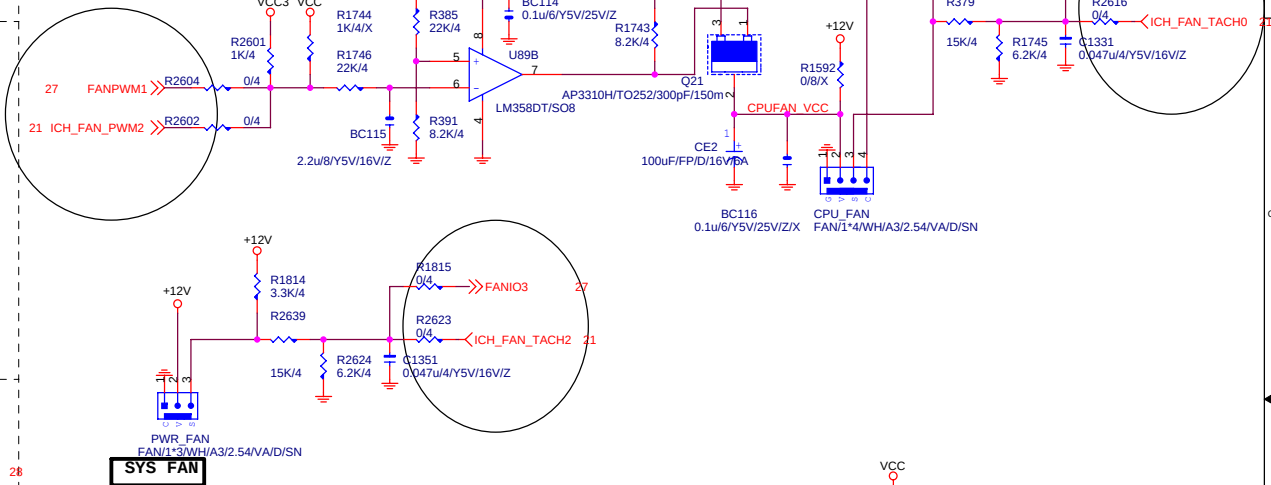
VOLTAGE-- H/W MONITOR



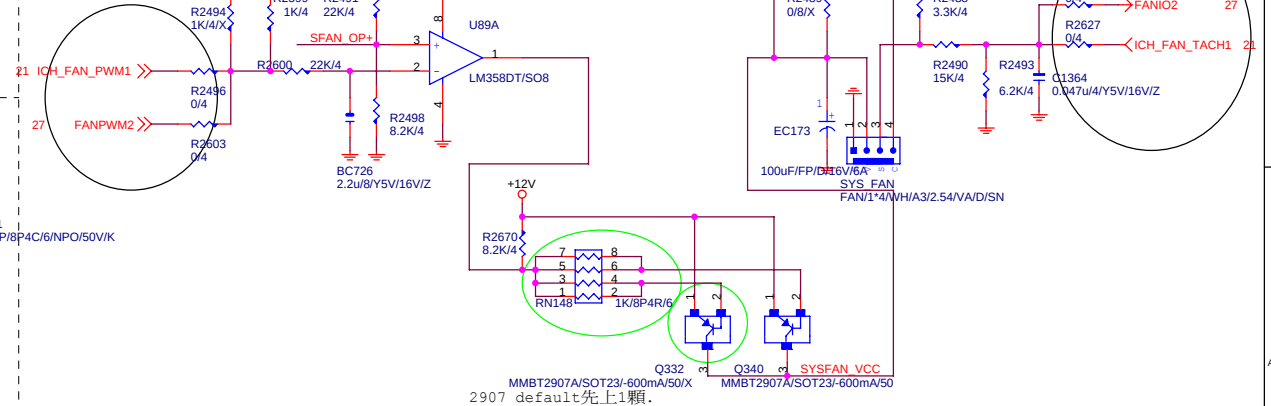
KB/MS



CPU SMART FAN



Linear SYS_FAN



Gigabyte Technology

Title

COM & LPT PORT

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Custom	

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