INDEX

A

Accumulating Fast Timer instruction, 5–42
Accumulating Timer (TMRA) instruction, 5–42
Accumulator, 5–69
Accumulator Instructions, 5–52
Aliases, 3–31
Analog IBoxes, 5–230
Approvals, 2–10
ASCII Conversion Table, G-2
ASCII In/Out and PRINT, 4–11
ASCII Instructions, 5–210
Auto tuning error, 8–48
Auto Tuning Procedure, 8–45
Automatic Trapezoidal Profile, E–47
Auxiliary Functions, 3–9, A–2
  CPU Configuration, A–5
  EEPROM Operations, A–8
  Handheld Programmer Configuration, A–8
  Password Operations, A–9
  RLL Operations, A–4
  via DirectSOFT32, A–3
  via the Handheld Programmer, A–3
  V-memory Operations, A–4

B

Basic EMC Installation Guidelines, J-4
Battery Backup, 3–8
BCD Numbering System, I–5
Binary Numbering System, I–2
Bit Override, 9–19
Boolean Instructions, 5–5, 5–10
Bumpless Transfer, 8–2, 8–3, 8–13, 8–26, 8–76, 8–77

C

C Data Type, 3–26
C-more, I-9
Cables
  programming, 1–8
Cascade Control, 8–65
  Tuning, 8–67
Changing Date and Time, 10–14
Clock / Calendar Instructions, 5–171
Combination Networks, 5–7
Comm Port 2, 3–4
Comm Ports, configuring, 4–7
Communication IBoxes, 5–231
Communications from a Ladder Program, K–13
  Read and Write Interlocks, K–13
Communications Problems, 9–7
Communications Protocols, K–3
Comparative Boolean Instructions, 5–26
Components, 1–6
Connecting DC I/O, 2–18
Connections
  power input, 1–8
  programming device, 1–8

toggle switches, 1–7
Contacts in Series, 5–6
Control Relay Bit Map, 3–36
Converge Jump instruction, 7–23
Converge Stage instruction, 7–23
Convergence Jump instruction, 7–20
Convergence Stages, 7–19
Counter Example Using Discrete Status Bits instruction, 5–46
Counter I/O IBoxes, 5–231
Counter Status Bit Map, 3–38
CPU Features, 3–2
CPU Operation, 3–12
CPU Setup, 3–5
CPU Specifications, 3–3
CT Data type, 3–27

D

Data Type Mismatch, I–7
Date and Time, 10–14
DC input wiring, 2–26
DC output wiring, 2–27
Diagnostics, 9–2
Dimensions, 2–7
DIN rail mounting, 2–9
DirectNET, 4–9, K–10
DirectNET Port Configuration, 4–10
Discrete Helper IBoxes, 5–230
Discrete Inputs with Filter, E–73
DL06 Error Codes, B–2
DL06 PLCMemory, F-2
DL06 Port Pinouts, K–5
DL06 Port Specifications, K–5
Drum Instruction, 6–12
chart representation, 6–3
counter assignments, 6–6
drum control techniques, 6–10
event drum (EDRUM), 6–14
handheld programmer mnemonics, 6–16
masked event drum (MDRMD), 6–19, 6–21
overview, 6–8
powerup state, 6–9
self-resetting, 6–11
step transitions, 6–11
Terminology, 6–2
Drum sequencer programming, 1–11
Duplicate Reference Check, 9–13

E

Edits, Run-time, 9–14
Electrical Noise, 9–10
END Instruction, 9–12
END Statement, 5–5
Error Code Locations, 9–3
Error Codes, 9–4, 9–5
Error Term Selection, 8–33
Errors, 9–2
European Union Directives, J-2

F

Feedforward Control, 8–70
Force I/O, 3–14
Forcing I/O Points, 9–16
Freeze Bias, 8–11, 8–34
Front Panel, 2–5
Fuse protection, 2–11

H

Hexadecimal Numbering System, I–3
High-Speed Counter, E–7
High-speed I/O wiring, 2–29
High-Speed Interrupts, E–64

HSIO Features, E–2
HSIO Operating Mode, E–4
Hysteresis, 8–3, 8–13, 8–36, 8–37, 8–38

I

I/O Configuration, 4–4
I/O type selection, 1–5
Indicators, 9–6
Inductive loads, 2–21
Initial Stage (ISG), 7–22
Instruction execution times, C–3
Instruction index, 5–2
Instructions
  drum, 6–12
  stage, 7–21
  stage programming, 7–2
Instructions, by category
  Accumulator / Stack Load, 5–52
  Bit Operation, 5–120
  Boolean, 5–10
  Clock / Calendar, 5–171
  Comparative, 5–26
  CPU Control, 5–173
  Immediate, 5–32
  Logical, 5–69
  Math, 5–86
  Number Conversion, 5–127
  Table, 5–141
  Timer, Counter and Shift Register, 5–39
  Transcendental, 5–118
Intelligent Box (IBox) Instruction Index, 5–230

K

K-Sequence, K–10

L

LCD Display Panel, 10–2
LCD Installation, 10–3
LCD instruction, 10–26
LCD Keypad, 10–2
LCD Menu Navigation, 10–5
Loop Mode, 8–27
Loop Table Word Definitions, 8–20

M

Maintenance, 9–2
Manual, documentation, 1–2
Marine Use, 2–10
Math IBoxes, 5–230
Memory
  EEPROM, 1–12
  FLASH, 1–12
Memory IBoxes, 5–230
Memory Map, 3–25, 3–32
Message Instructions, 5–186
Midline Outputs, 5–6
MODBUS, 4–9
MODBUS RTU Communications, K–14
MODBUS RTU Instructions, 5–204
Mode 10, E–7
Mode 20, E–24
Mode 30, E–38
Mode 40, E–64
Mode 50, E–69
Mode 60, E–73
Mode Switch, 3–6
Motion Control, E–2
Mounting Guidelines, 2–7
  Clearances, 2–8
MRX instruction, 4–22
MWX instruction, 4–22

N

Network Master, 4–18
Network Slave, 4–12
Network Specification, 4–8
Noise, 9–10
Non-volatile V-memory, F-3
Not Jump, 7–22
Numbering Systems, 3–23

O

Octal Numbering System, I–4

P

Parallel Branches in Series, 5–7
Parallel Elements, 5–7
Parallel Processing, 7–19
Password, 3–11, 10–17
PAUSE Instruction, 9–12
PID
  Analog Filter, 8–55
  DirectSOFT 5 Filter Intelligent Box Instruction, 8–57
  Error Flags, 8–18
  Example Program, 8–72
  Loop Modes, 8–3, 8–27, 8–53, 8–54, 8–66
  Parameters, 8–32
  Setup Alarms, 8–35
  Special Features, 8–53
PID Alarms, 8–35
  Calculation Overflow/Underflow Error, 8–38
  Hysteresis, 8–38
  Mode/Alarm Bit Description, 8–23
  Monitor Limit, 8–35
  Programming Error, 8–38
  PV Deviation, 8–36
  Rate-of-Change, 8–37
PID Loop
  Alarms, 8–13
  Auto Tuning, 8–40
  Configure, 8–25
  Features, 8–2
  Manual Tuning, 8–40, 8–41, 8–44, 8–47, 8–55
  Mode, 8–27
  Operating Modes, 8–14
  Operation, 8–9
  Program Setup, 8–72
  Reverse Acting, 8–12, 8–14, 8–26, 8–40
  Setup, 8–18
  Terminology, 8–77
  Troubleshooting Tips, 8–75
PID Mode 2 Word Description, 8–22
PID Mode Setting 1 Description, 8–21
Port Setup, K–6
Position Algorithm, 8–9, 8–15, 8–78
  Position Form, 8–9
Power Budgeting, 4–5
Power supply, 2–12
Product Weight table, H–2
Products and Data Types, I–9
Program Mode, 3–13
Programming Devices, 2–15
Pulse Catch Input, E–69
Pulse Output, E–38

Q

Quick Start, 1–6

R

Ramp/Soak Generator, 8–58
  Controls, 8–61
  DirectSOFT 5 Ramp/Soak Example, 8–63
  Profile Monitoring, 8–62

Ramp/Soak Flag Bit Description, 8–23
Ramp/Soak Table Location, 8–24
Relay Ladder, 8–63
Table, 8–59
Table Flags, 8–61
Test Profile with PID View, 8–64
Testing, 8–62
Rate-of-Change, 8–3, 8–13, 8–14, 8–37
Real Numbering System, I–5
Relay outputs, 2–20
Remote I/O Bit Map, 3–39
Reset Windup, 8–10, 8–34, 8–78
Response Time, 3–17
Retentive Memory Ranges, 3–10
RUN Indicator, 9–7
Run Mode, 3–13
Run Time Edits, 9–14

S

S Data type, 3–28
Safety, 2–2
Emergency Stops, 2–3
Orderly System Shutdown, 2–4
Scan Time, 3–20
Serial Communications, K–2
RS-232C, K–2
RS-422, K–2
RS-485, K–3
Series Branches in Parallel, 5–7
Signed vs. Unsigned Integers, I–8
Simple Rungs, 5–5
Sinking / sourcing concepts, 2–16
Slot Numbering, 4–3
SP Data Type, 3–28
Special Instructions, 9–12
Special Relays, D–2
Special Relays, Error Codes, 9–3
Specifications, 2–30
Specifications, environmental, 2–10
Square Root, 8–14
Stage Control / Status Bit Map, 3–34
Stage Counter instruction, 7–17
Stage instructions, 7–21
Stage Jump Instruction, 7–7
Stage Programming, 7–2, 7–15
convergence, 7–19
emergency stop, 7–14
four steps to stage programmig, 7–9
garage door opener example, 7–10
introduction, 7–2
jump instruction, 7–7
mutually exclusive transitions, 7–14
parallel processes, 7–12
parallel processing concepts, 7–19
power flow transition, 7–18
program organization, 7–15
questions and answers, 7–27
stage instruction characteristics, 7–6
stage view, 7–18
state transition diagrams, 7–3
supervisory process, 7–17
timer inside stage, 7–13
Startup, 9–11
State Diagram, 7–11
Status Indicators, 3–6
Step Transitions, 6–4
Step Trapezoidal Profile, E–46
STOP Instruction, 9–12
Syntax Check, 9–11
System Design, 1–10

T

T Data Type, 3–26
Technical Support, 1–2
Terminal Block Removal, 2–6
Time-Proportioning Control, 8–68
On/Off Control Program, 8–69
Timer (TMR) and Timer Fast (TMRF), 5–40
Timer Example Using Discrete Status Bits instruction, 5–41
Timer Status Bit Map, 3–38
Timer, Counter and Shift Register Instructions,5–39
Transfer Mode, 8–26
Troubleshooting, 9–8, 9–11

U

Up/Down Counter, E–24

V

V Data Type, 3–27
Velocity Algorithm, 8–9, 8–15, 8–78
Velocity Form, 8–12
V-memory, 3–29

W

Web site, 1–2
Wiring Diagrams, 2–30
D0–06AA I/O Wiring Diagram, 2–30
D0–06AR I/O Wiring Diagram, 2–32
D0–06DA I/O Wiring Diagram, 2–34
D0–06DD1 I/O Wiring Diagram, 2–36
D0–06DD1–D I/O Wiring Diagram, 2–42
D0–06DD2 I/O Wiring Diagram, 2–38
D0–06DD2–D I/O Wiring Diagram, 2–44
D0–06DR I/O Wiring Diagram, 2–40
D0–06DR–D I/O Wiring Diagram, 2–46
Wiring Guidelines, 2–11

X

X Data Type, 3–26
X Input / Y Output Bit Map, 3–33

Y

Y Data Type, 3–26