HSF Property : **Halogen-Free**

ROMEO 2.0

UMA & Dis Muxless Switching

MV BUILD

2011/3/31

DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE = 3 VER :

FILE NAME : XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE ***ROMEO20***

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

SHEET 1 OF 70

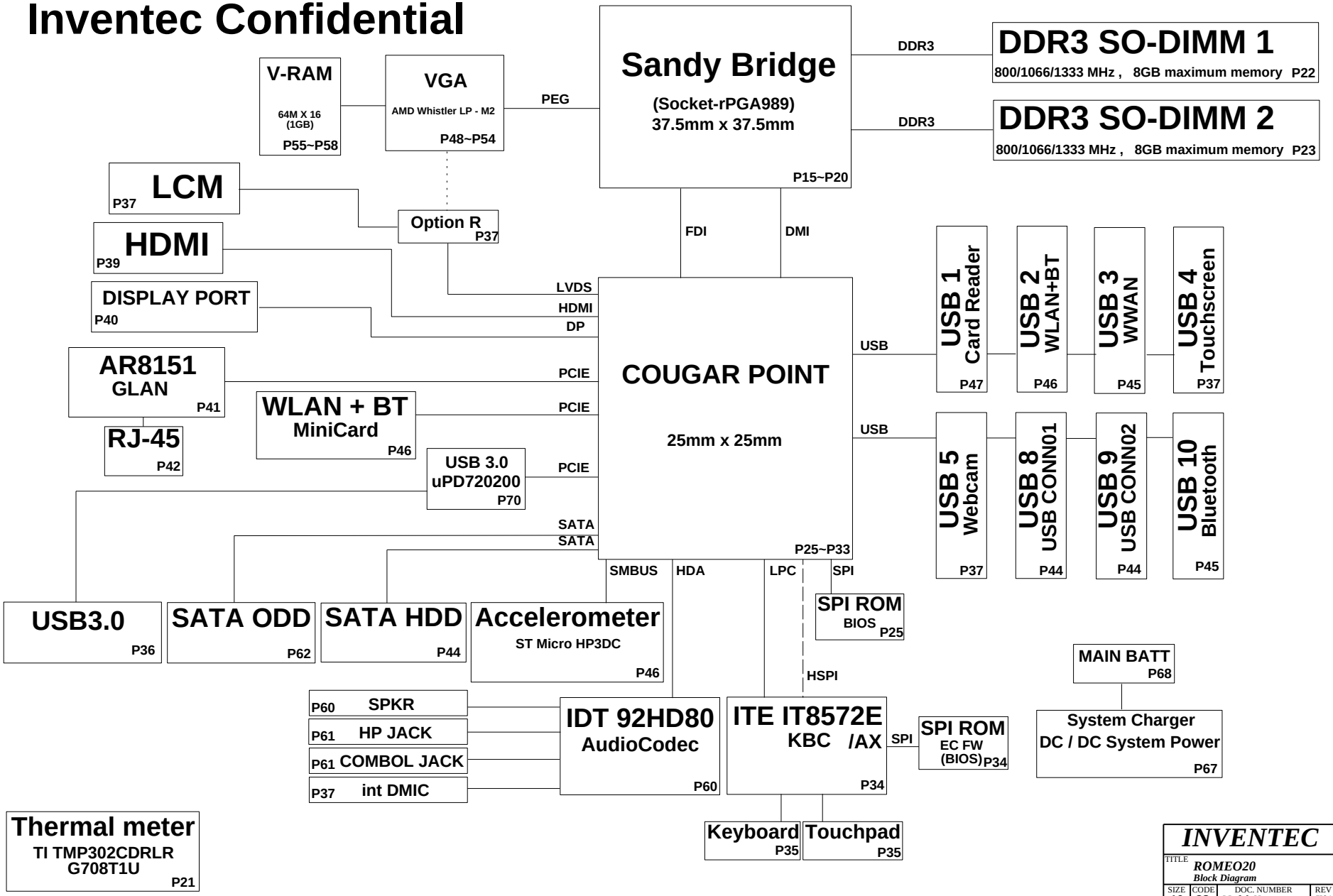
Index

CHANGE by	*Drawer_Name*	*28-Dec-2010*	

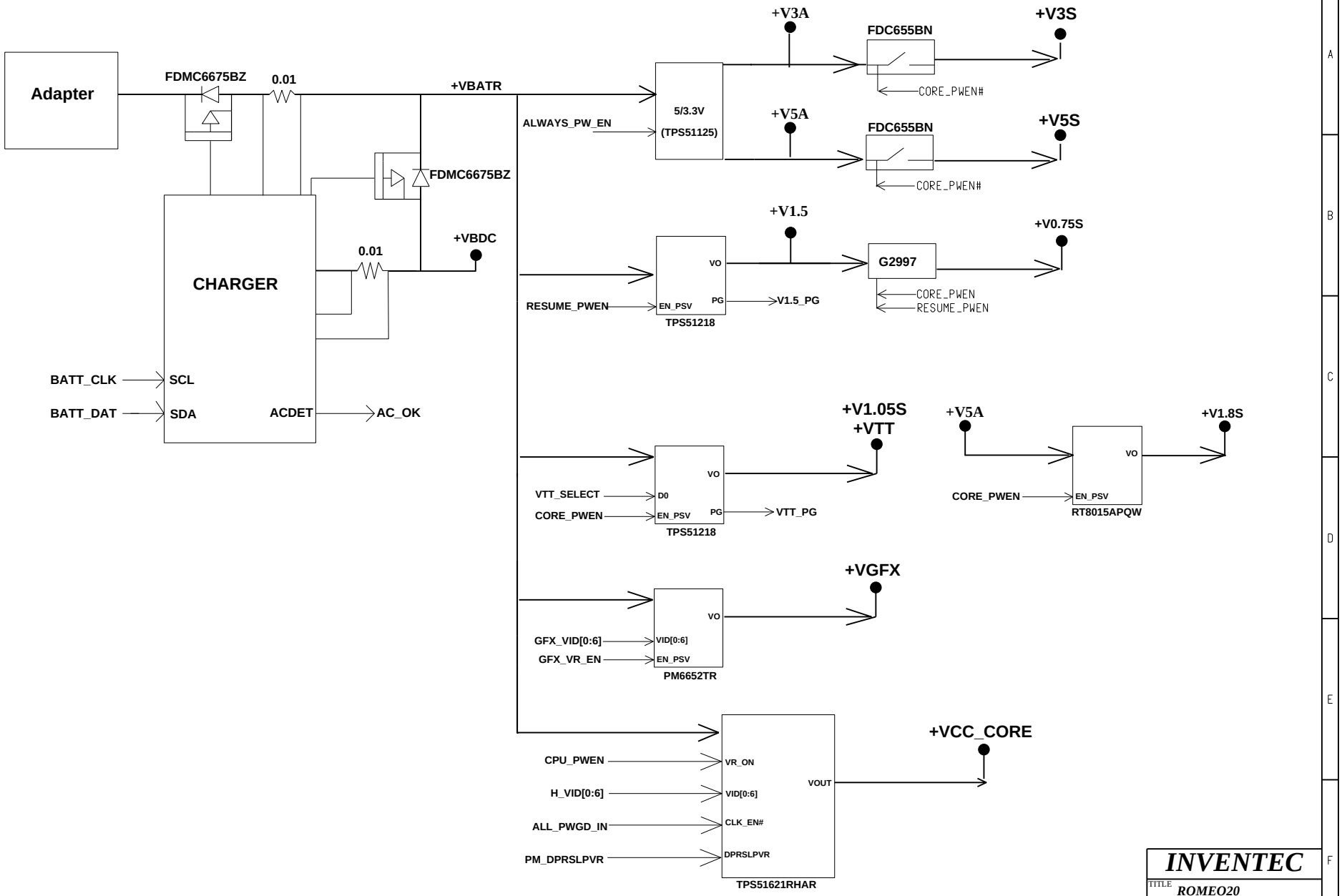
INVENTEC

TITLE	*ROMEO20* *Index*		
SIZE A3	CODE CS	DOC. NUMBER *Model_No*	REV *X01*
SHEET 2 OF 70			

Inventec Confidential



CHANGE by	*Drawer_Name*	*28-Dec-2010*	
INVENTEC			
TITLE	*ROMEO20* *Block Diagram*		
SIZE A3	CODE CS	DOC. NUMBER *Model_No*	REV *X01*
SHEET 3 OF 70			



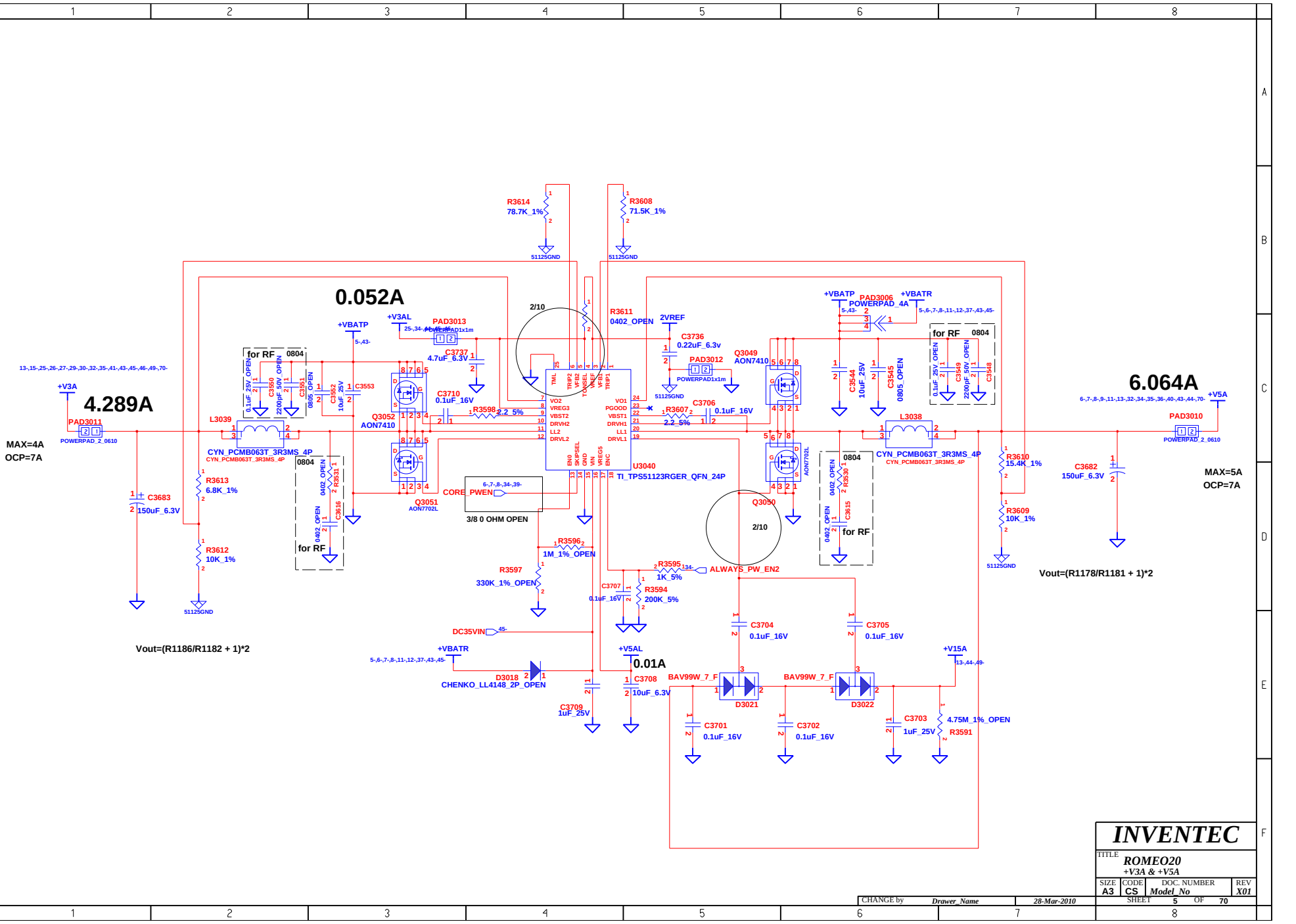
CHANGE by	Drawer_Name	20-Apr-2010	

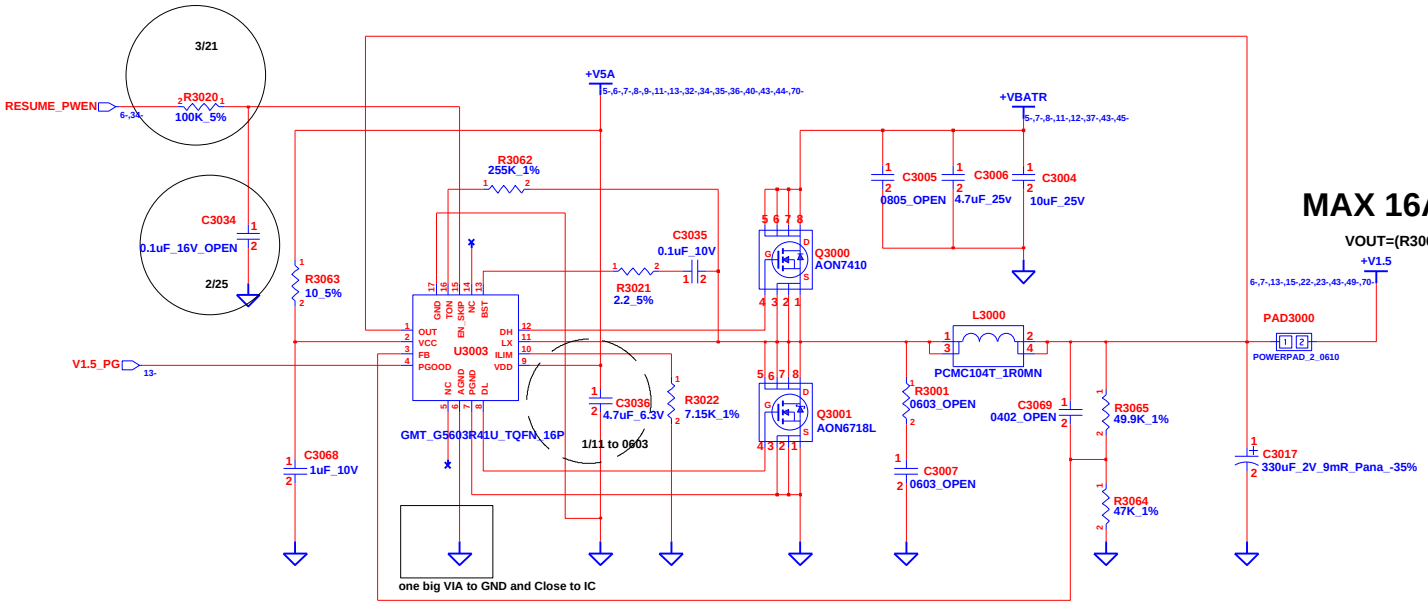
INVENTEC

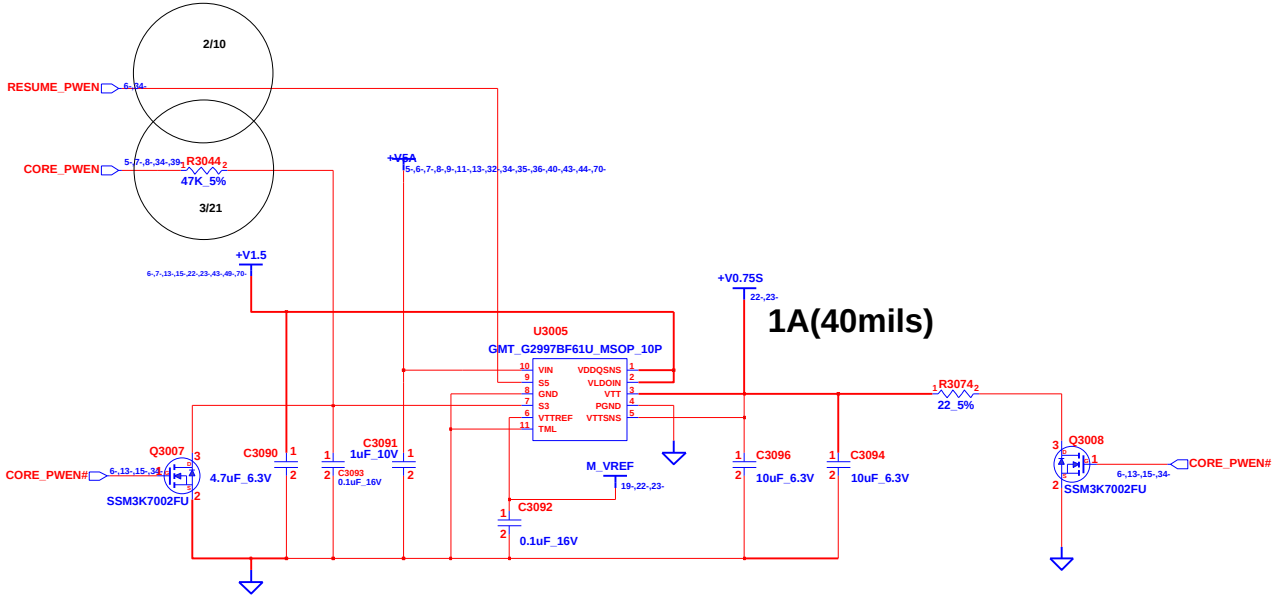
TITLE: *ROMEO20*
Power Procedure

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 4 OF 70


0.052A
4.289A
6.064A
0.01A
MAX=4A
OCP=7A
MAX=5A
OCP=7A
Vout=(R1186/R1182 + 1)*2
Vout=(R1178/R1181 + 1)*2
U3040
TI_TPS51123RGER_QFN_24P
CYN_PCMB063T_3R3MS_4P
Q3052
AON7410
Q3051
AON7702L
Q3049
AON7410
Q3050
AON7702L
D3018
CHENKO_LL4148_2P_OPEN
D3021
BAV99W_7_F
D3022
BAV99W_7_F
L3039
L3038
R3614
78.7K_1%
R3608
71.5K_1%
R3611
0402_OPEN
R3613
6.8K_1%
R3612
10K_1%
R3610
15.4K_1%
R3609
10K_1%
R3596
1M_1%_OPEN
R3597
330K_1%_OPEN
R3595
1K_5%
R3594
200K_5%
R3598
2.2_5%
R3607
2.2_5%
R3591
4.75M_1%_OPEN
C3683
150uF_6.3V
C3682
150uF_6.3V
C3736
0.22uF_6.3v
C3737
4.7uF_6.3V
C3710
0.1uF_16V
C3706
0.1uF_16V
C3704
0.1uF_16V
C3705
0.1uF_16V
C3701
0.1uF_16V
C3702
0.1uF_16V
C3703
1uF_25V
C3708
10uF_6.3V
C3709
1uF_25V
C3544
10uF_25V
C3545
0805_OPEN
C3549
2200pF_50V_OPEN
C3548
0.1uF_25V_OPEN
C3550
2200pF_50V_OPEN
C3551
0805_OPEN
C3552
10uF_25V
C3553
0.1uF_25V_OPEN
C3707
0.1uF_16V
C3615
0402_OPEN
C3616
0402_OPEN
R3530
0402_OPEN
R3531
0402_OPEN
PAD3011
POWERPAD_2_0610
PAD3010
POWERPAD_2_0610
PAD3013
POWERPAD1x1m
PAD3012
POWERPAD1x1m
PAD3006
POWERPAD_4A
+V3A
+V3AL
+VBATP
+VBATR
+V5A
+V5AL
+V15A
2VREF
DC35VIN
CORE_PWEN
ALWAYS_PW_EN2
51125GND
3/8 0 OHM OPEN
for RF
0804
2/10
INVENTEC
TITLE
ROMEO20
+V3A & +V5A
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
CHANGE by Drawer_Name
28-Mar-2010
SHEET 5 OF 70



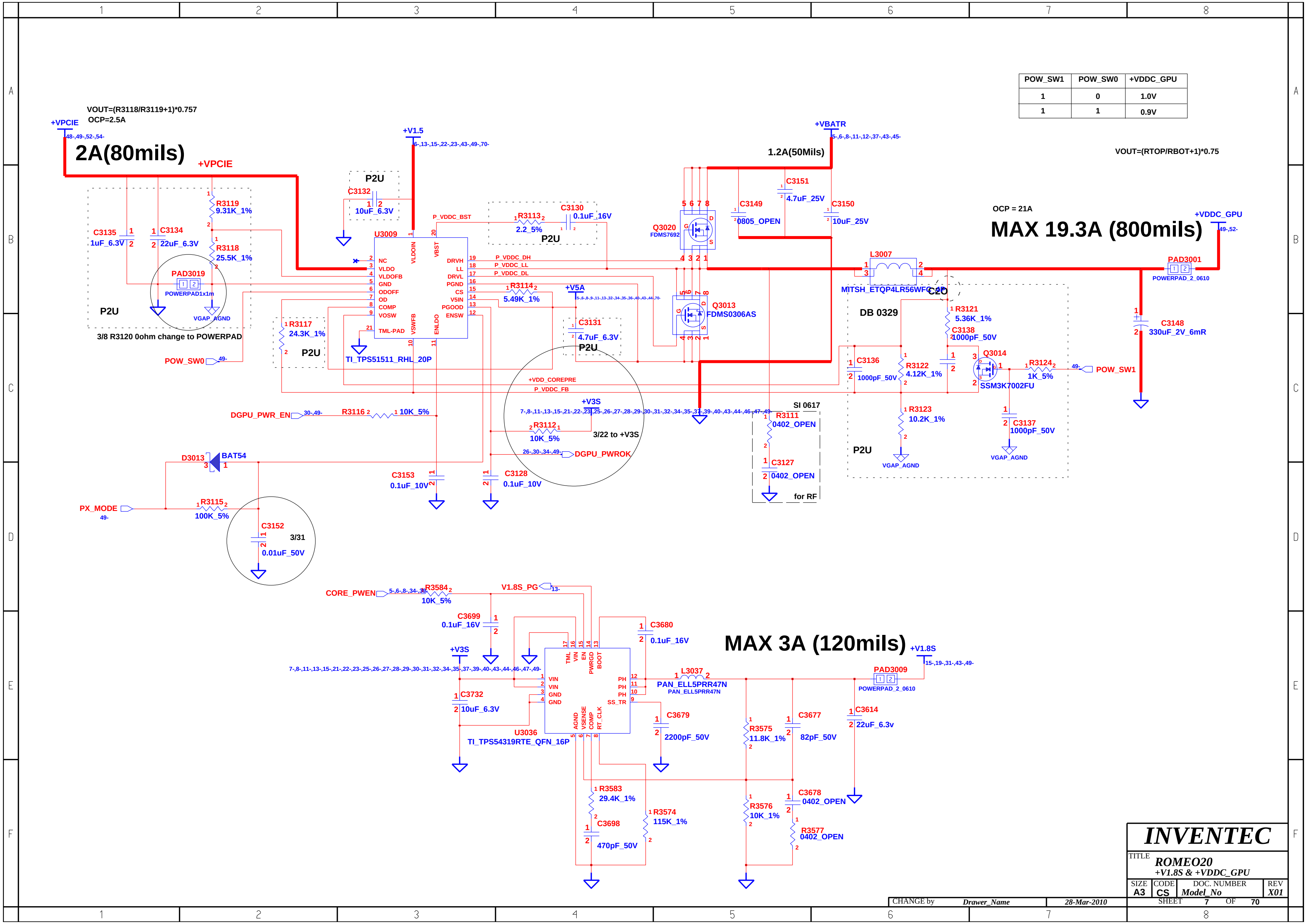


NOTE: DDR3 REGULATOR

CHANGE by	*Drawer_Name*	*13-Jan-2011*	

INVENTEC

TITLE	*ROMEO20* *+V1.5 & +V0.75*		
SIZE A3	CODE CS	DOC. NUMBER *Model_No*	REV *X01*
SHEET 6	OF 70		



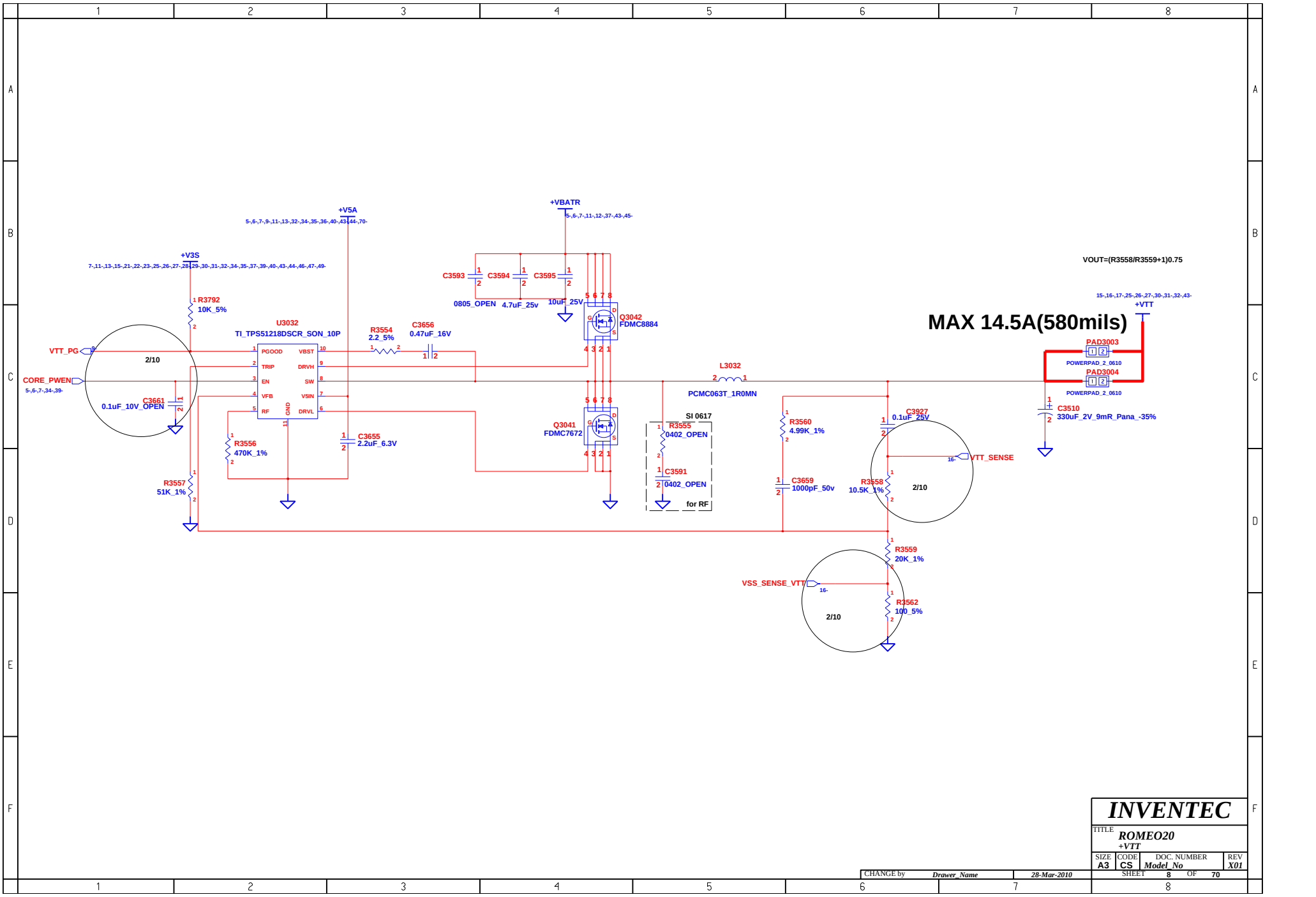
POW_SW1	POW_SW0	+VDDC_GPU
1	0	1.0V
1	1	0.9V

INVENTEC

TITLE ROMEO20 +V1.8S & +VDDC_GPU

SIZE A3 | CODE CS | DOC. NUMBER Model_No | REV X01

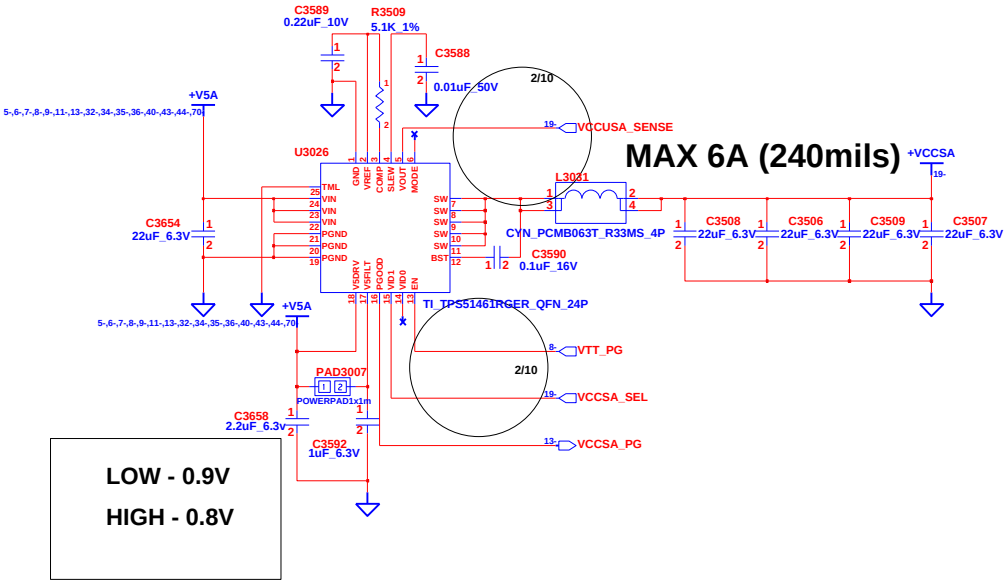
CHANGE by Drawer_Name 28-Mar-2010 SHEET 7 OF 70



CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

TITLE	ROMEO20 +VTT			
SIZE	CODE	DOC. NUMBER		REV
A3	CS	Model_No		X01
		SHEET 8	OF 70	



CHANGE by	*Drawer_Name*	*28-Mar-2010*		

INVENTEC

TITLE	*ROMEO20* *+VCCSA*		
SIZE **A3**	CODE **CS**	DOC. NUMBER *Model_No*	REV *X01*
SHEET **9**	OF **70**		

BLANK

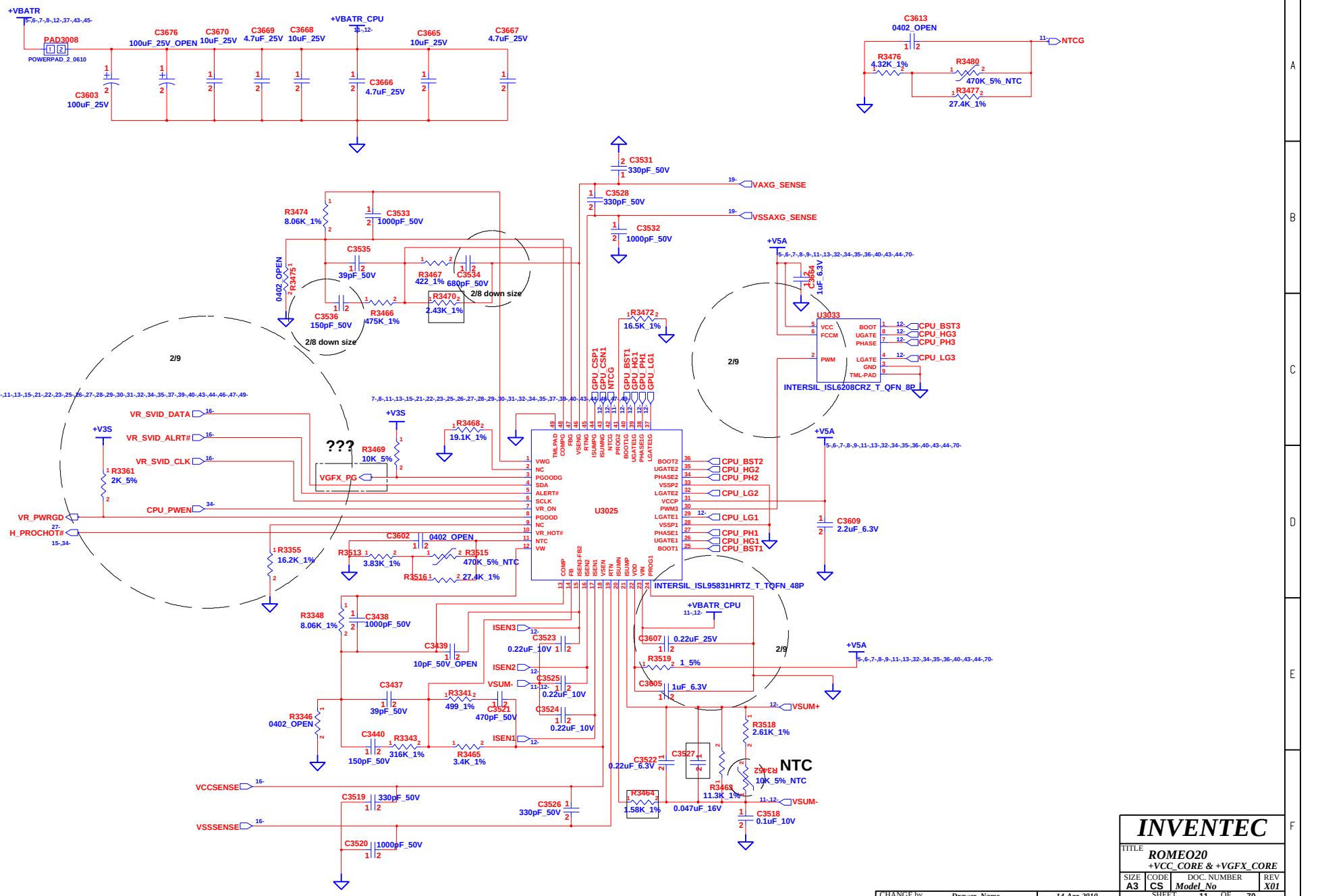
CHANGE by	*Drawer_Name*	*14-Apr-2010*	

INVENTEC

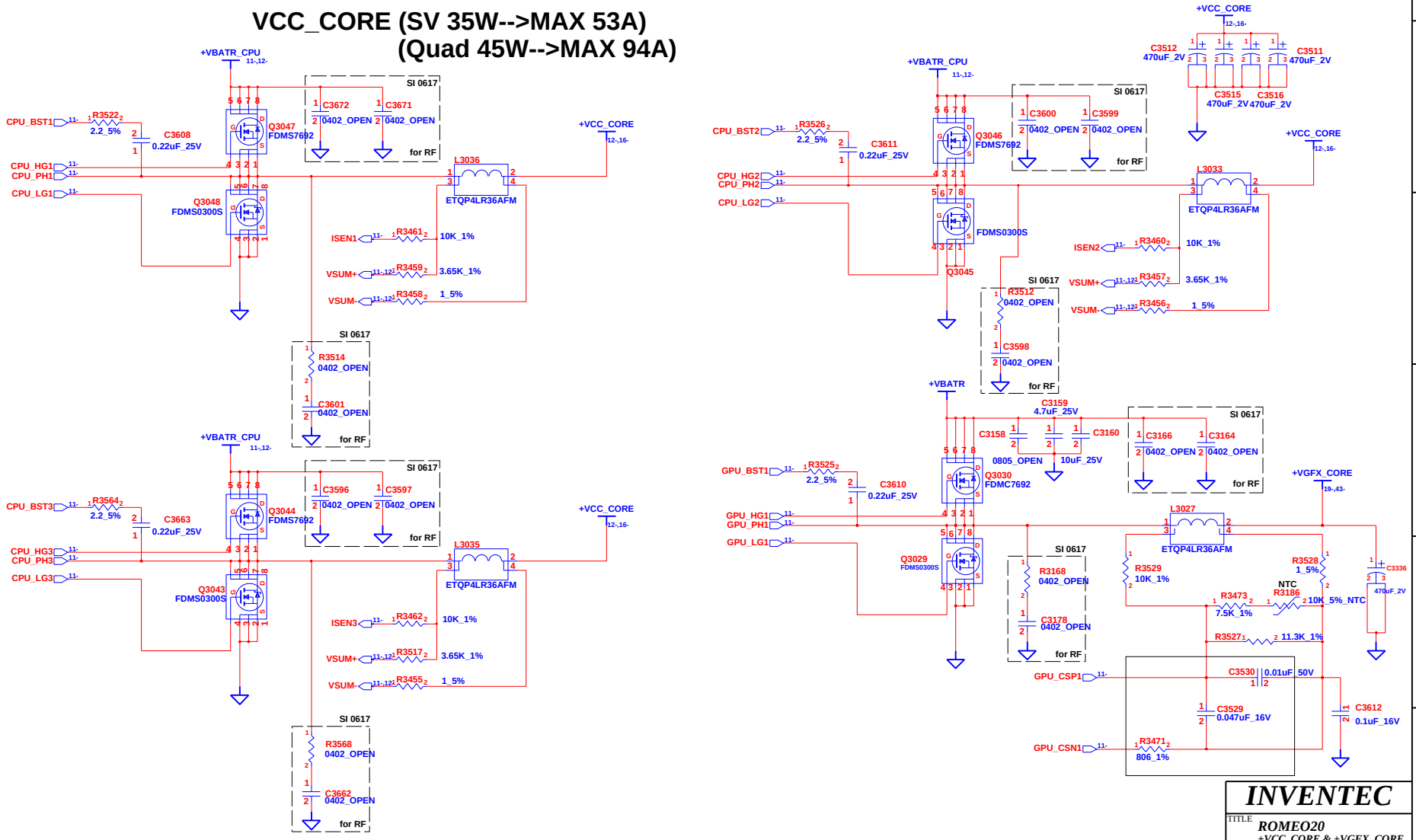
TITLE *ROMEO20*
BLANK

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

SHEET 10 OF 70


+VBATR
PAD3008
POWERPAD_2_0610
C3603 100uF_25V
C3676 100uF_25V_OPEN
C3670 10uF_25V
C3669 4.7uF_25V
C3668 10uF_25V
+VBATR_CPU
C3666 4.7uF_25V
C3665 10uF_25V
C3667 4.7uF_25V
C3613 0402_OPEN
R3476 4.32K_1%
R3480 470K_5%_NTC
R3477 27.4K_1%
NTCG
C3531 330pF_50V
C3528 330pF_50V
C3532 1000pF_50V
VAXG_SENSE
VSSAXG_SENSE
R3474 8.06K_1%
C3533 1000pF_50V
C3535 39pF_50V
R3467 422_1%
C3534 680pF_50V
R3470 2.43K_1%
C3536 150pF_50V
R3466 475K_1%
0402_OPEN
R3475
2/8 down size
2/8 down size
2/9
2/9
+V5A
C3604 1uF_6.3V
U3033
VCC
FCCM
PWM
BOOT
UGATE
PHASE
LGATE
GND
TML-PAD
CPU_BST3
CPU_HG3
CPU_PH3
CPU_LG3
INTERSIL_ISL6208CRZ_T_QFN_8P
R3472 16.5K_1%
GPU_CSP1
GPU_CSN1
GPU_NTCG
GPU_BST1
GPU_HG1
GPU_PH1
GPU_LG1
+V3S
R3468 19.1K_1%
R3469 10K_5%
???
VGFX_PG
VR_SVID_DATA
VR_SVID_ALRT#
VR_SVID_CLK
CPU_PWEN
VR_PWRGD
H_PROCHOT#
R3361 2K_5%
R3355 16.2K_1%
U3025
VWG
NC
PGOODG
SDA
ALERT#
SCLK
VR_ON
PGOOD
NC
VR_HOT#
NTC
VW
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
PWM3
LGATE1
VSSP1
PHASE1
UGATE1
BOOT1
CPU_BST2
CPU_HG2
CPU_PH2
CPU_LG2
CPU_LG1
CPU_PH1
CPU_HG1
CPU_BST1
INTERSIL_ISL95831HRTZ_T_TQFN_48P
+V5A
C3609 2.2uF_6.3V
C3602 0402_OPEN
R3513 3.83K_1%
R3515 470K_5%_NTC
R3516 27.4K_1%
R3348 8.06K_1%
C3438 1000pF_50V
C3439 10pF_50V_OPEN
C3437 39pF_50V
R3346 0402_OPEN
C3440 150pF_50V
R3343 316K_1%
R3465 3.4K_1%
R3341 499_1%
C3521 470pF_50V
ISEN3
ISEN2
ISEN1
VSUM-
C3523 0.22uF_10V
C3525 0.22uF_10V
C3524 0.22uF_10V
+VBATR_CPU
C3607 0.22uF_25V
R3519 1_5%
C3605 1uF_6.3V
VSUM+
R3518 2.61K_1%
C3522 0.22uF_6.3V
C3527
R3462 10K_5%_NTC
NTC
R3463 11.3K_1%
R3464 1.58K_1%
0.047uF_16V
VSUM-
C3518 0.1uF_10V
VCCSENSE
VSSSENSE
C3519 330pF_50V
C3526 330pF_50V
C3520 1000pF_50V
CHANGE by
Drawer_Name
14-Apr-2010
INVENTEC
TITLE
ROMEO20
+VCC_CORE & +VGFX_CORE
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 11 OF 70

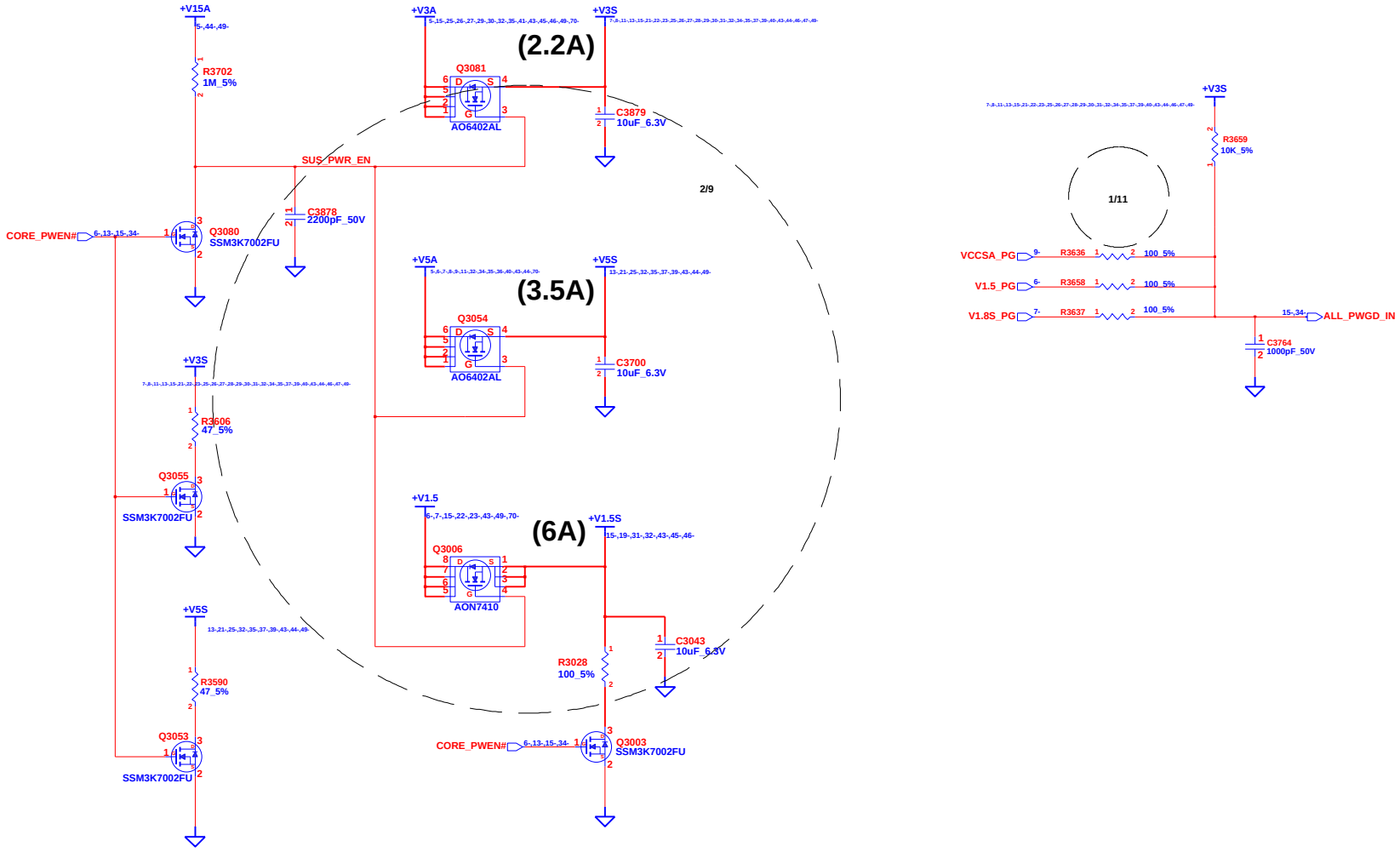
VCC_CORE (SV 35W-->MAX 53A)
(Quad 45W-->MAX 94A)



CHANGE by	Drawer_Name	28-Mar-2010

INVENTEC

TITLE	ROMEO20 +VCC_CORE & +VGFX_CORE		
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01
SHEET 12 OF 70			



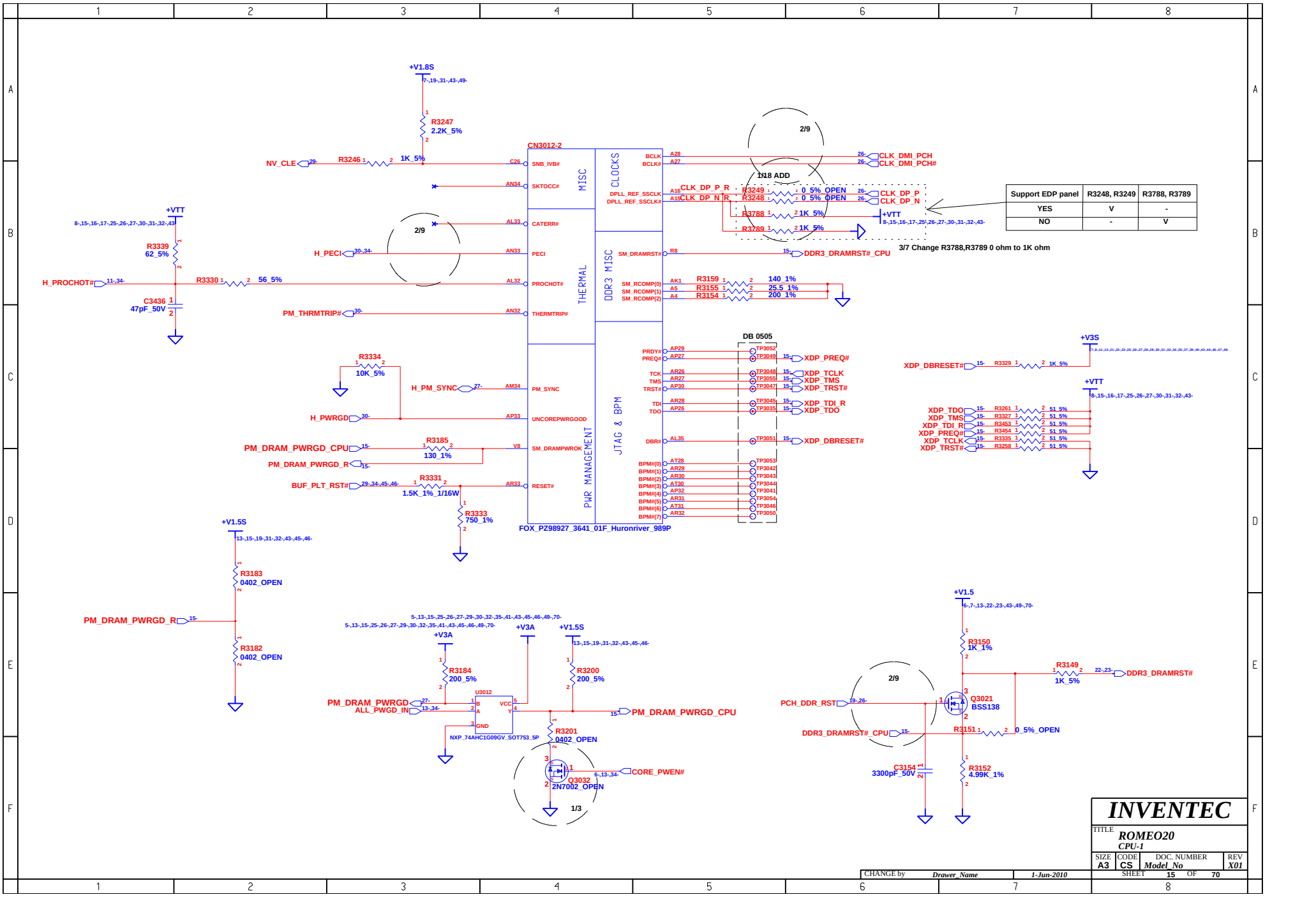
CHANGE by	*Drawer_Name*	*7-May-2010*	

INVENTEC

TITLE	*ROMEO20* *+V5S & +V3S*		
SIZE: A3	CODE: CS	DOC. NUMBER: *Model_No*	REV: *X01*
		SHEET 13 OF 70	

12/17 CLOCK GEN DELETED

INVENTEC			
TITLE	ROMEO20 CLK GEN		
SIZE: A3	CODE: CS	DOC. NUMBER: Model_No	REV: X01
CHANGE by: Drawer_Name	17-Dec-2010	SHEET 14 OF 70	



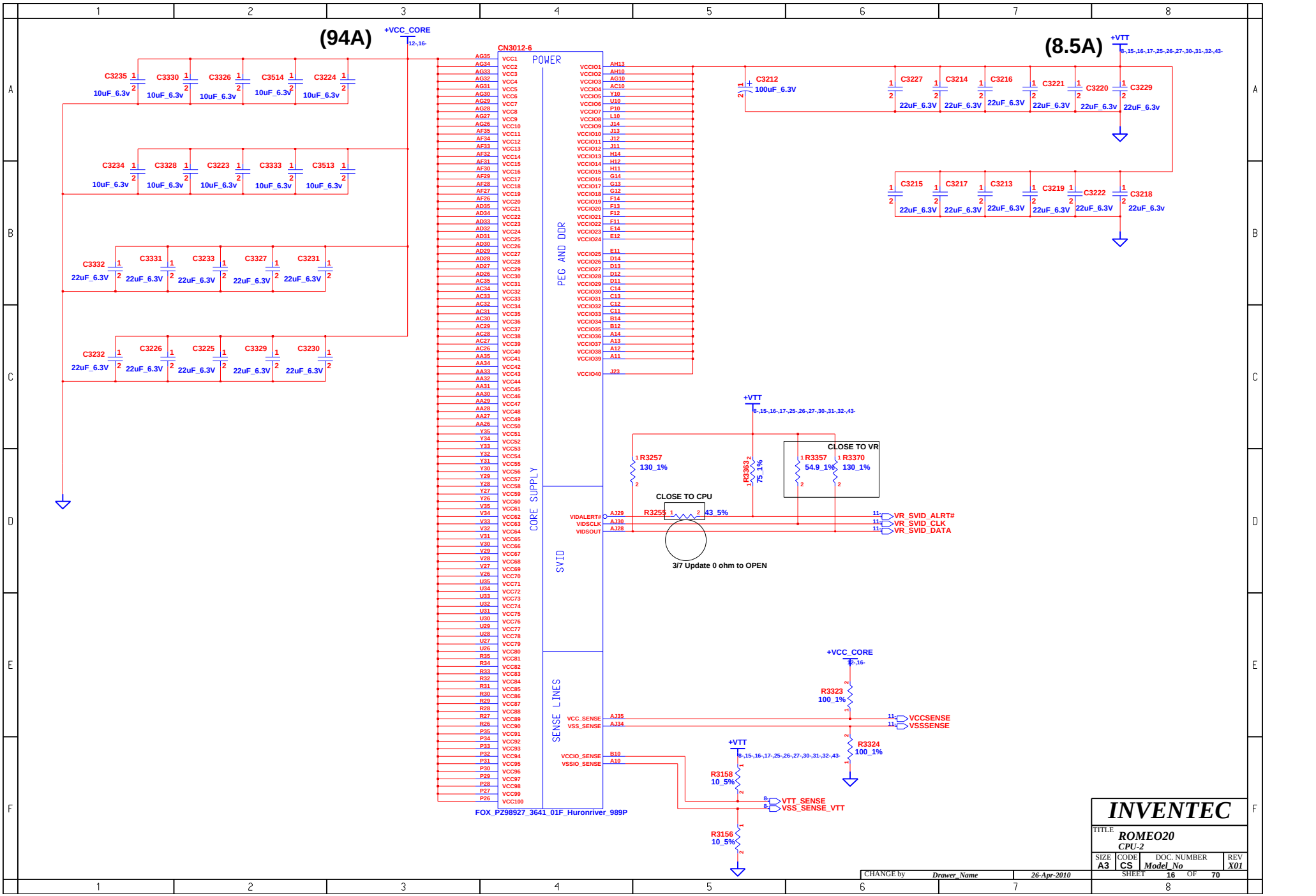
Support EDP panel	R3248, R3249	R3788, R3789
YES	V	-
NO	-	V

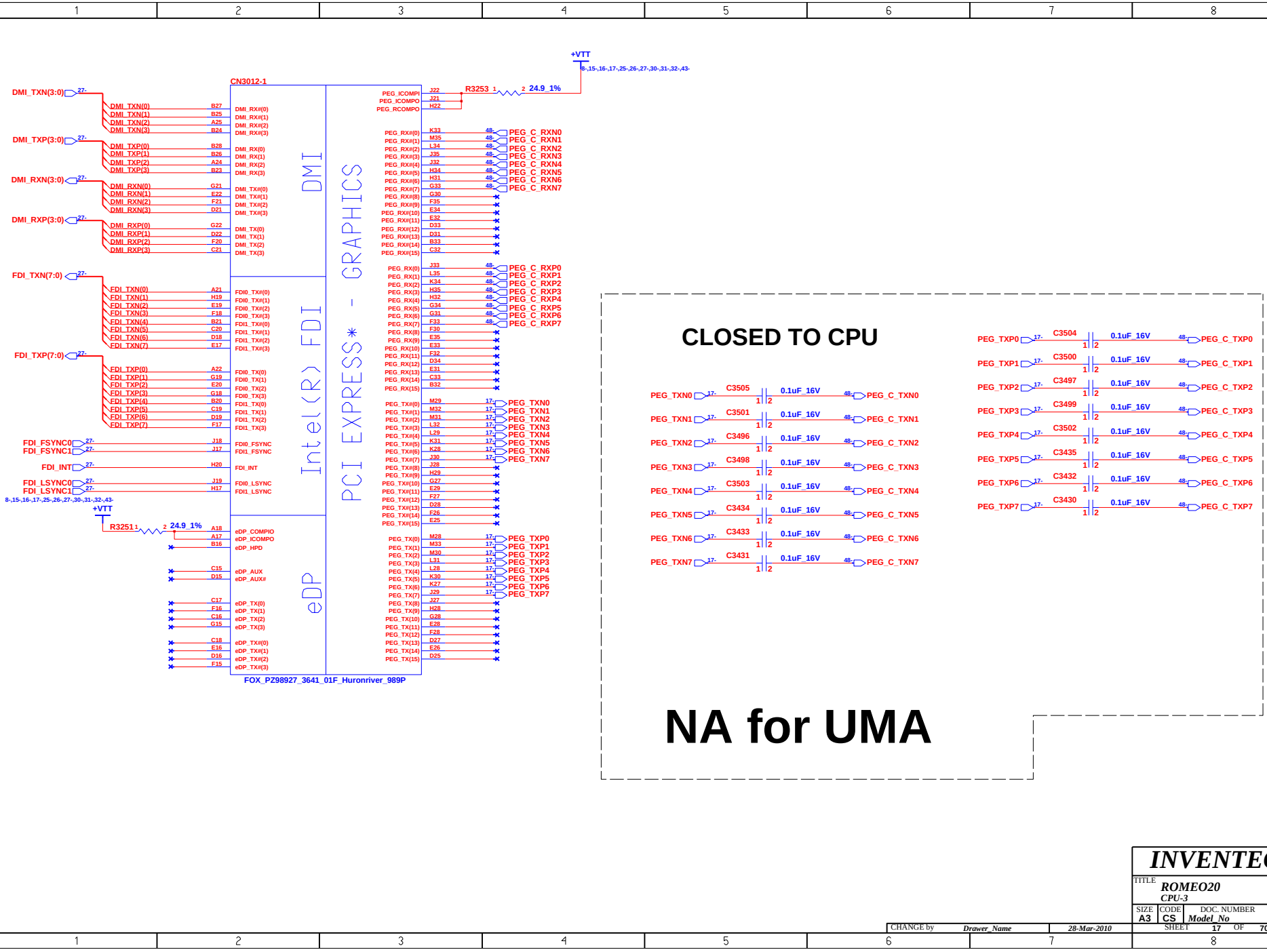
3/7 Change R3788,R3789 0 ohm to 1K ohm

CHANGE by	Drawer_Name	1-Jun-2010			

INVENTEC

TITLE				
ROMEO20 CPU-1				
SIZE	CODE	DOC. NUMBER		REV
A3	CS	Model_No		X01
		SHEET 15	OF 70	


(94A)
+VCC_CORE
12-,16-
CN3012-6
POWER
PEG AND DDR
CORE SUPPLY
SVID
SENSE LINES
C3235 C3330 C3326 C3514 C3224
10uF_6.3v
C3234 C3328 C3223 C3333 C3513
10uF_6.3v
C3332 C3331 C3233 C3327 C3231
22uF_6.3V
C3232 C3226 C3225 C3329 C3230
22uF_6.3V
(8.5A)
+VTT
8-,15-,16-,17-,25-,26-,27-,30-,31-,32-,43-
C3212
100uF_6.3V
C3227 C3214 C3216 C3221 C3220 C3229
22uF_6.3V
C3215 C3217 C3213 C3219 C3222 C3218
22uF_6.3V
R3257
130_1%
R3363
75_1%
CLOSE TO VR
R3357
54.9_1%
R3370
130_1%
CLOSE TO CPU
R3255
43_5%
VIDALERT#
VIDSCLK
VIDSOUT
VR_SVID_ALRT#
VR_SVID_CLK
VR_SVID_DATA
3/7 Update 0 ohm to OPEN
R3323
100_1%
R3324
100_1%
VCC_SENSE
VSS_SENSE
VCCSENSE
VSSSENSE
VCCIO_SENSE
VSSIO_SENSE
R3158
10_5%
R3156
10_5%
VTT_SENSE
VSS_SENSE_VTT
FOX_PZ98927_3641_01F_Huronriver_989P
INVENTEC
TITLE
ROMEO20
CPU-2
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 16 OF 70
CHANGE by Drawer_Name
26-Apr-2010



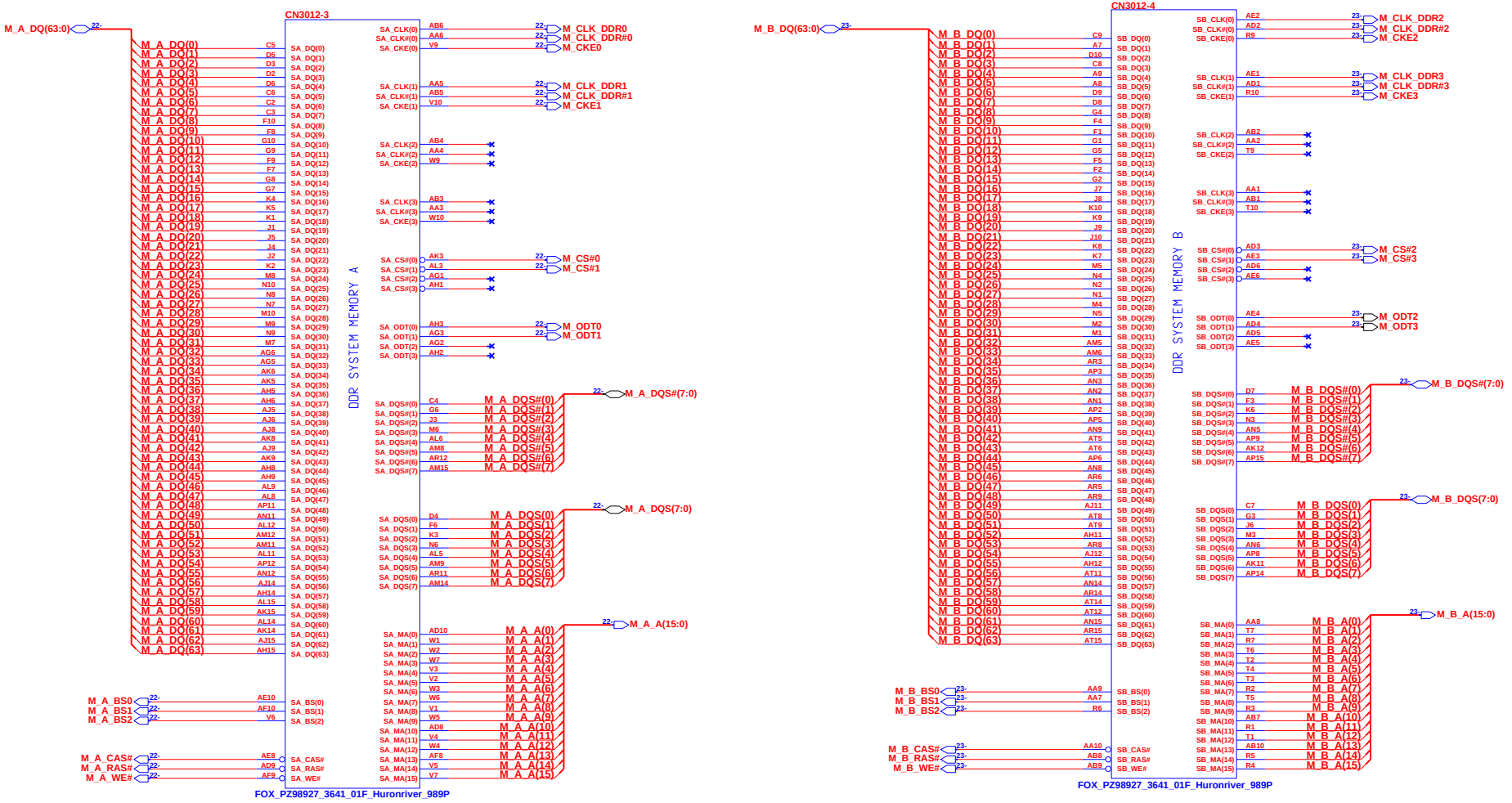
CHANGE by	Drawer_Name	28-Mar-2010		

INVENTEC

TITLE: ROMEO20
CPU-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

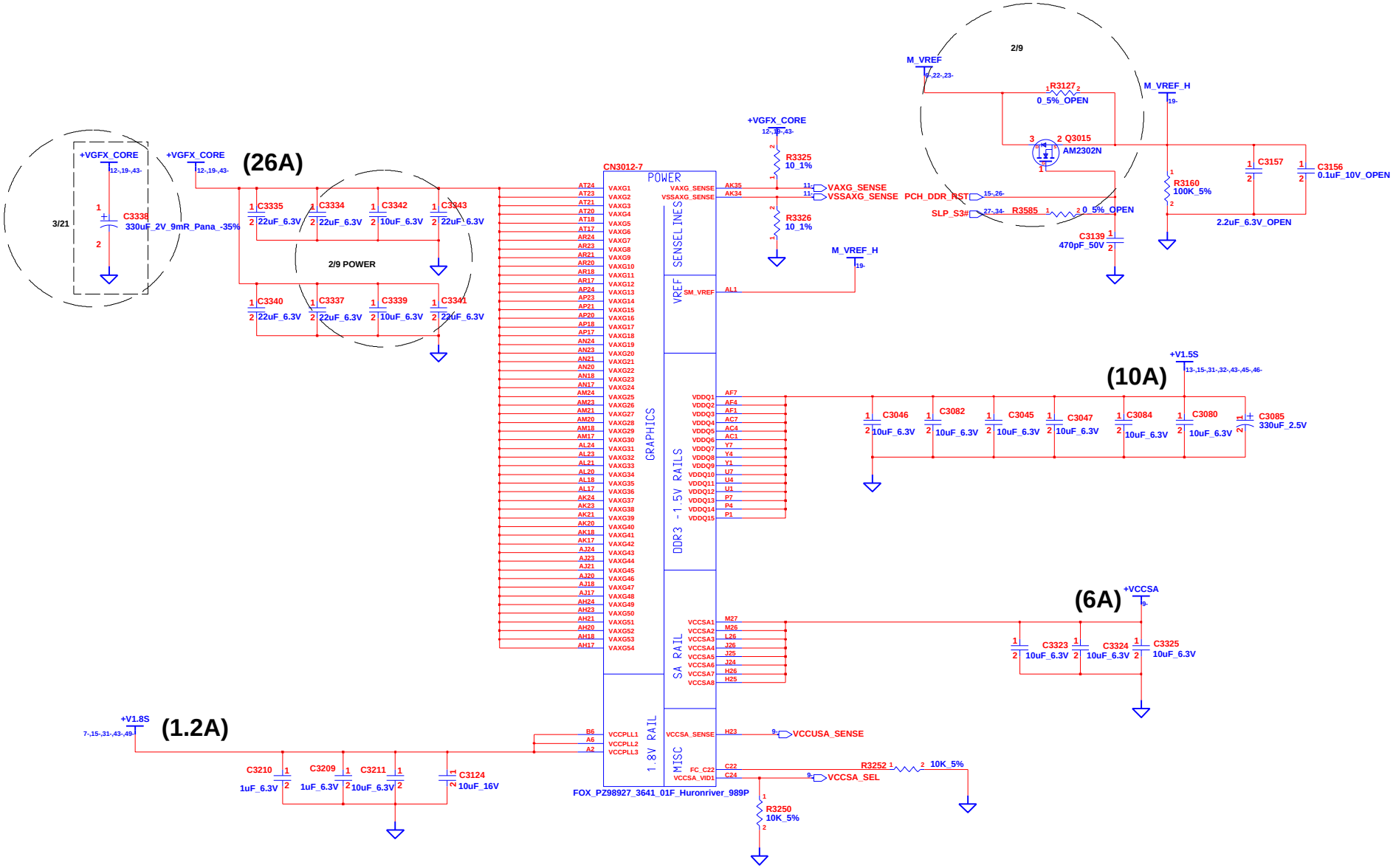
SHEET 17 OF 70



CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

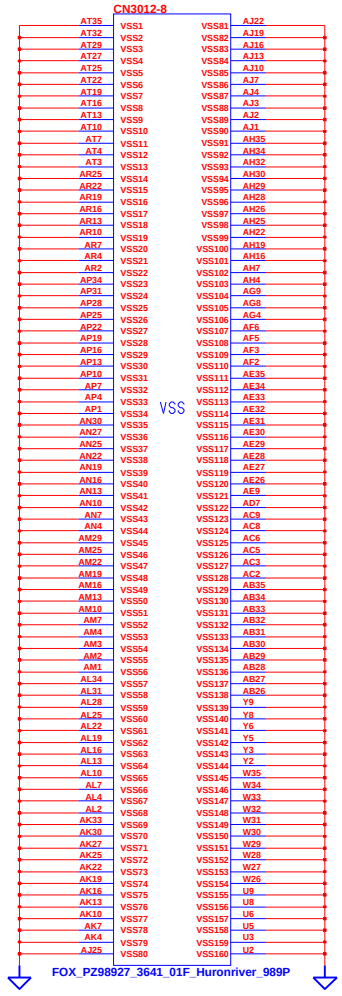
TITLE	ROMEO20 CPU-4		
SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
		SHEET 18 OF 70	

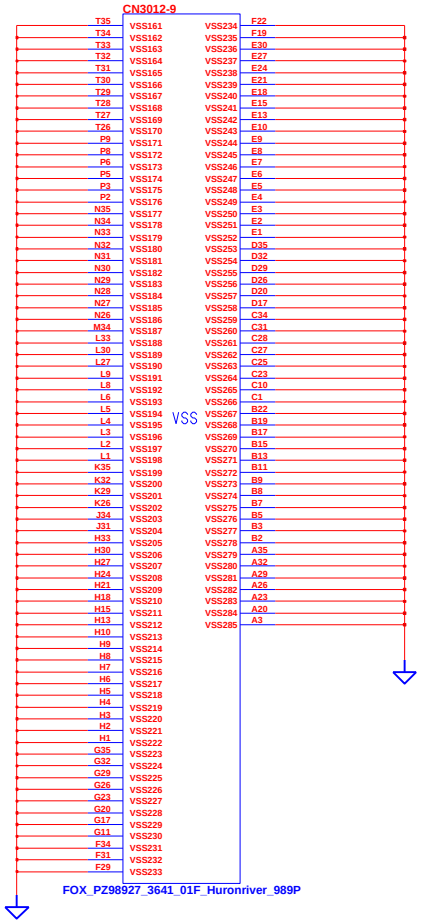


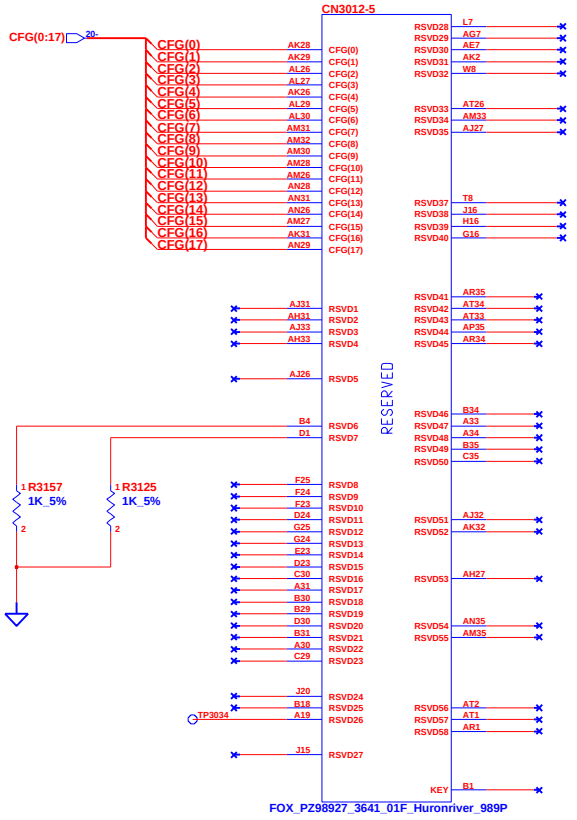
CHANGE by	Drawer_Name	28-Mar-2010		

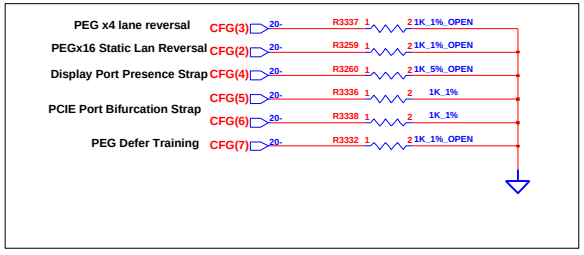
INVENTEC

TITLE	ROMEO20 CPU-5		
SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
		SHEET 19 OF 70	









STRAP PIN

CHANGE by	*Drawer_Name*	*14-Apr-2010*	

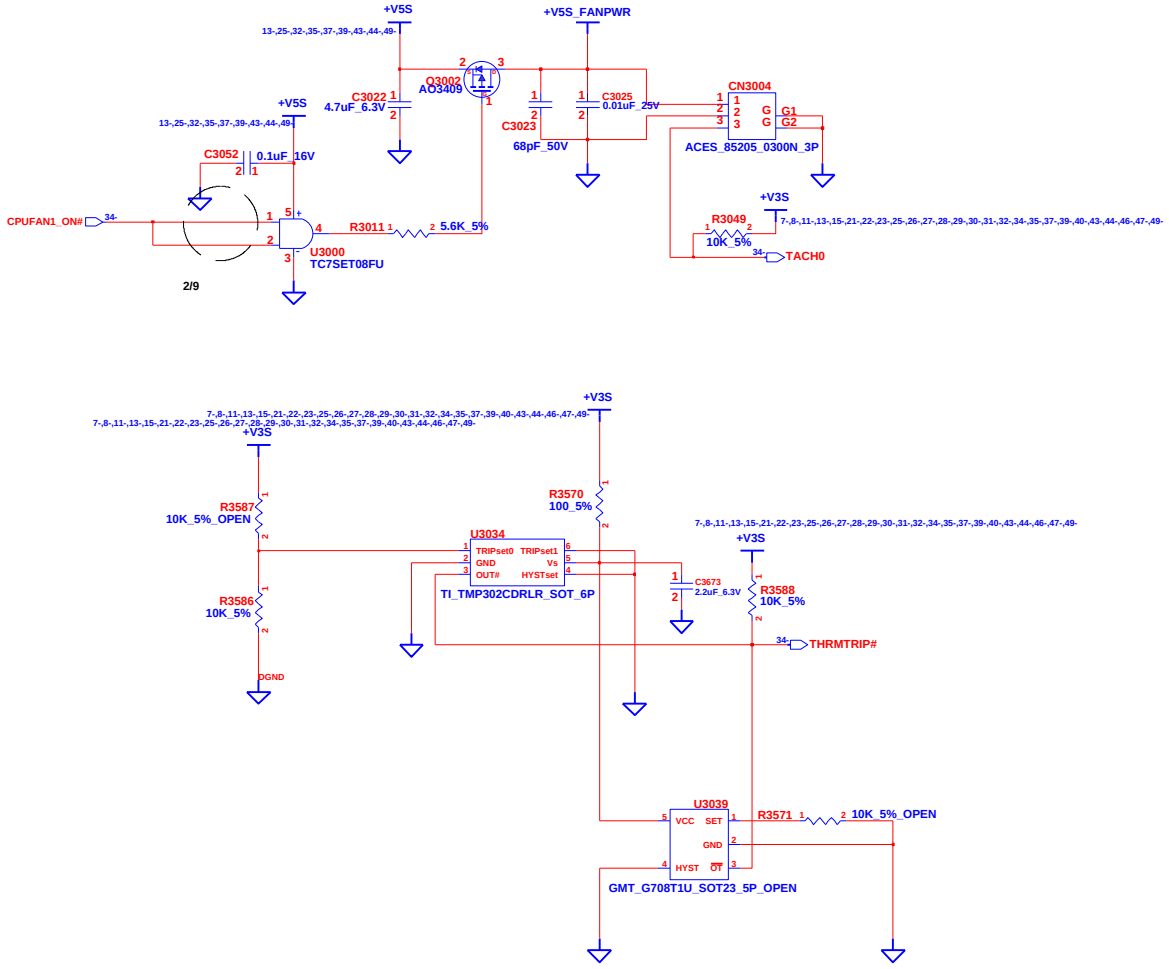
INVENTEC

TITLE: *ROMEO20*
CPU-6

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

SHEET 20 OF 70

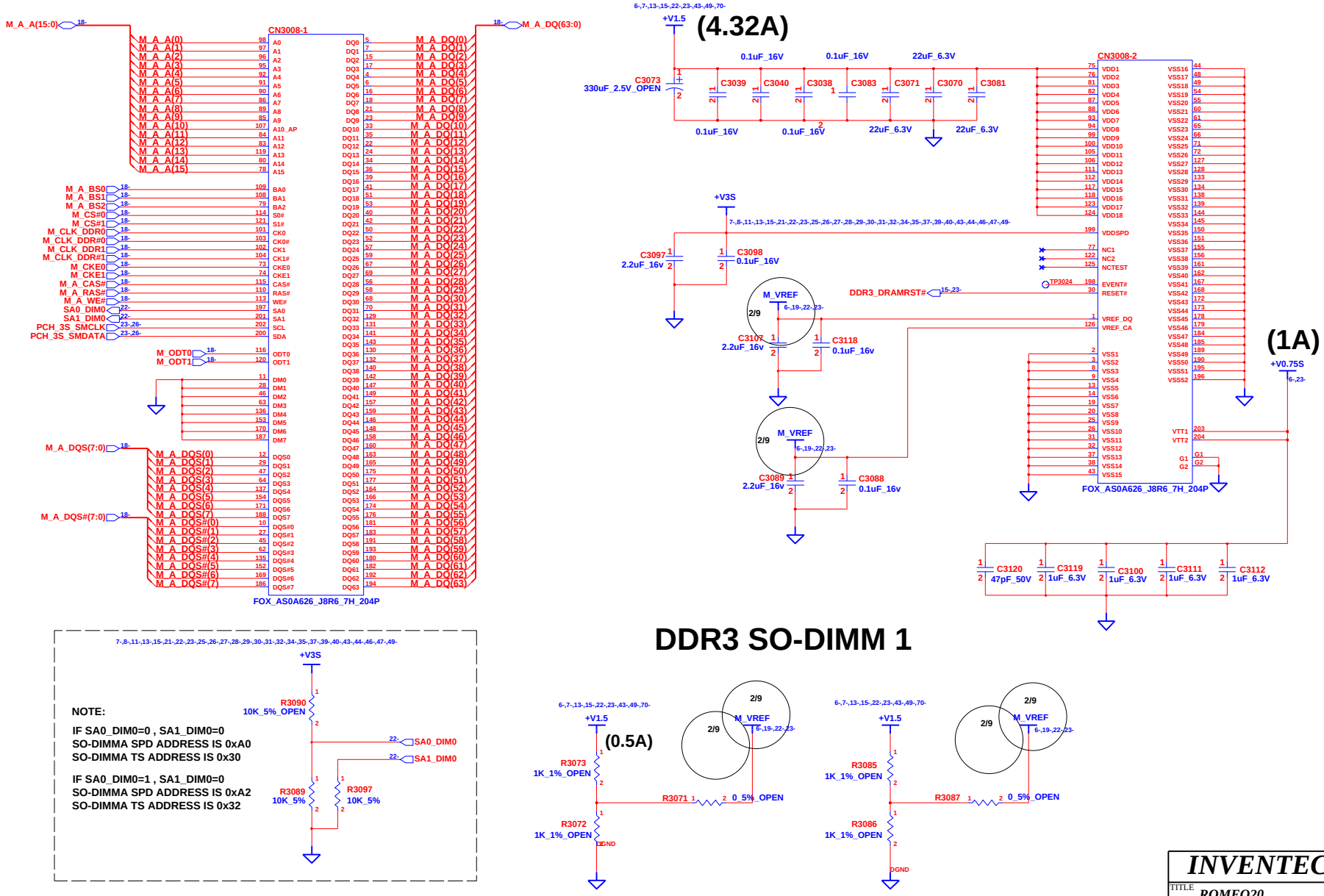
FAN CONN



CHANGE by	*Drawer_Name*	*28-Mar-2010*	

INVENTEC

TITLE	*ROMEO20* *FAN*		
SIZE A3	CODE CS	DOC. NUMBER *Model_No*	REV *X01*
		SHEET 21 OF 70	



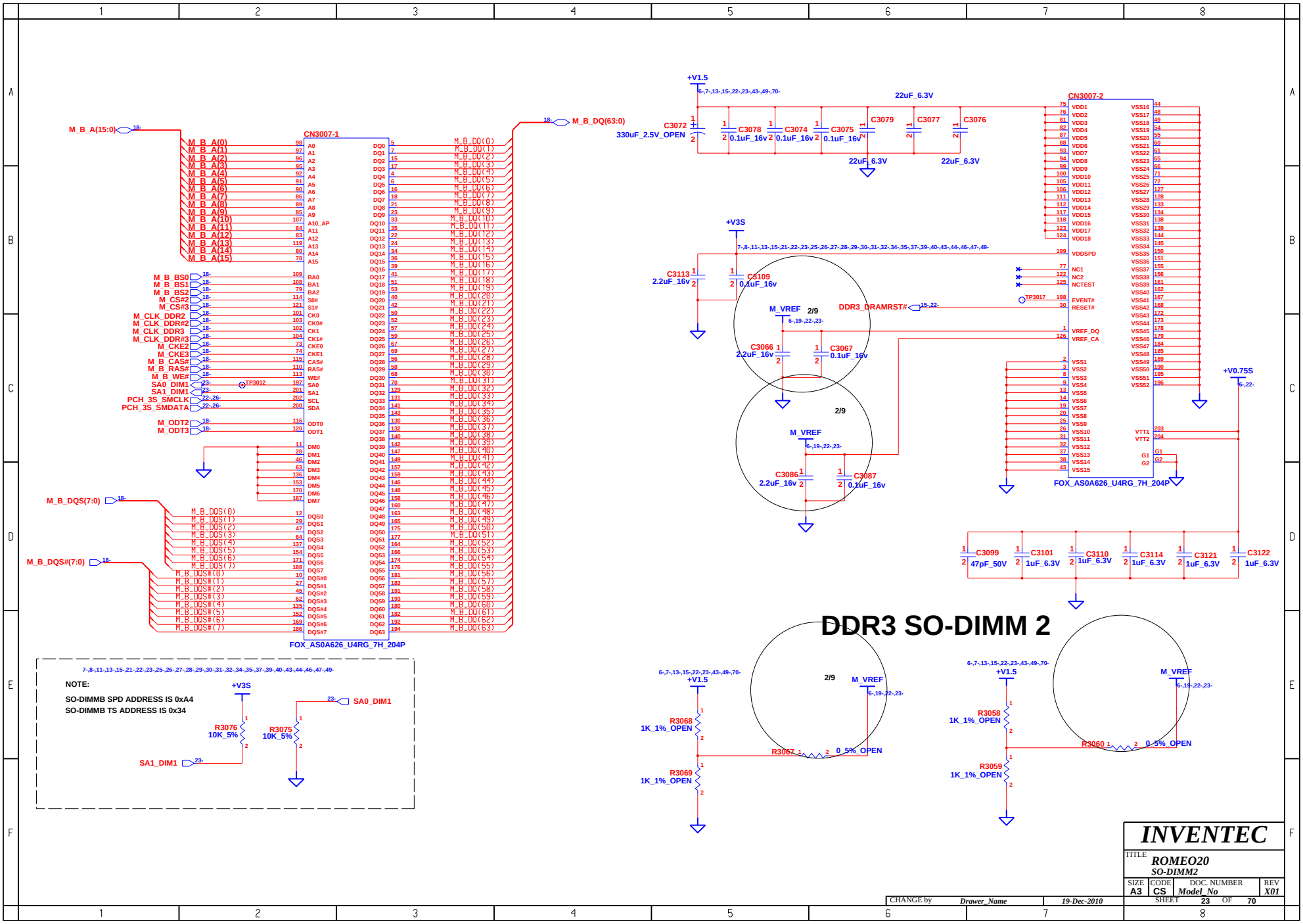
CHANGE by	Drawer_Name	14-Apr-2010		

INVENTEC

TITLE: ROMEO20
SO-DIMM1

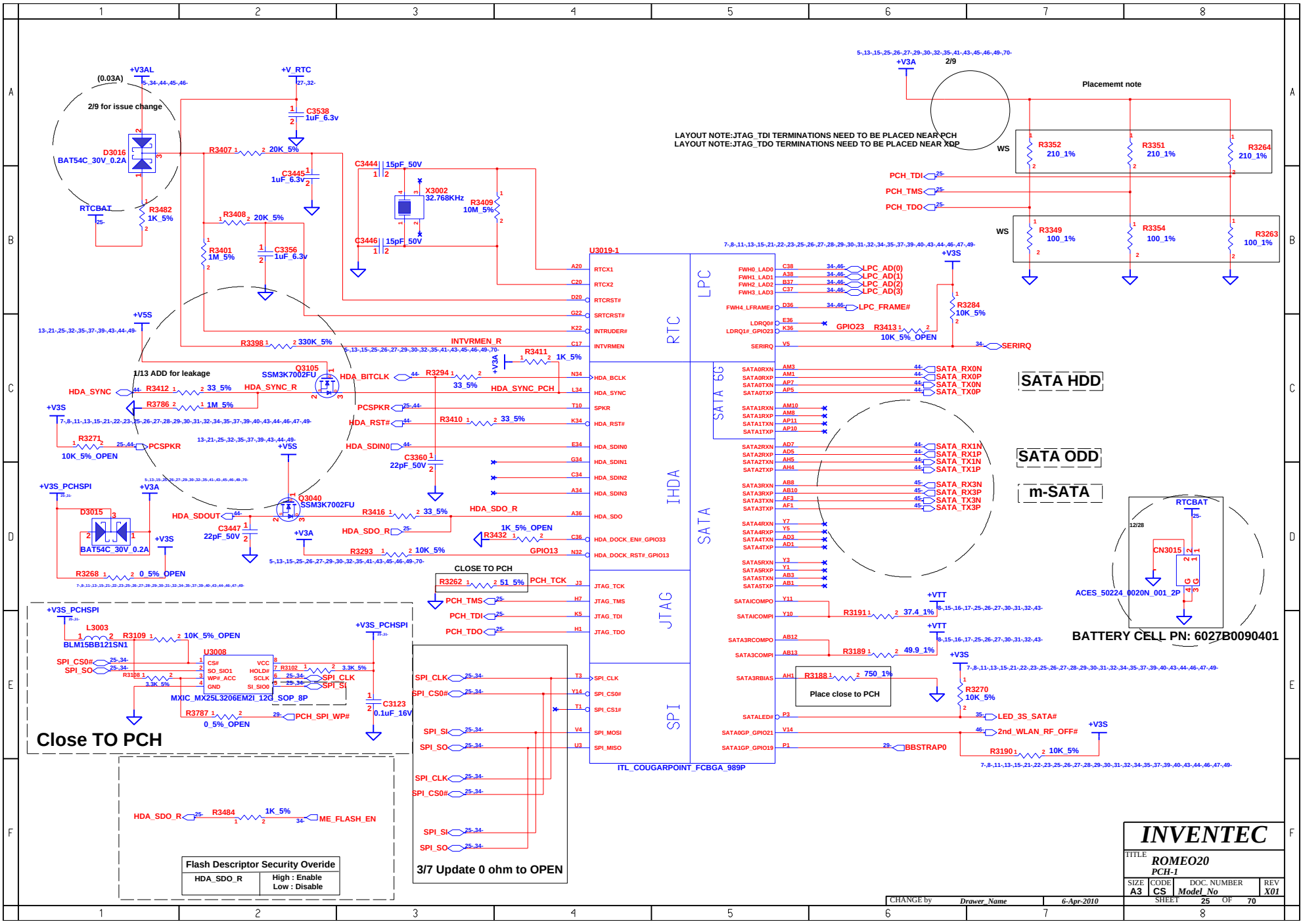
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

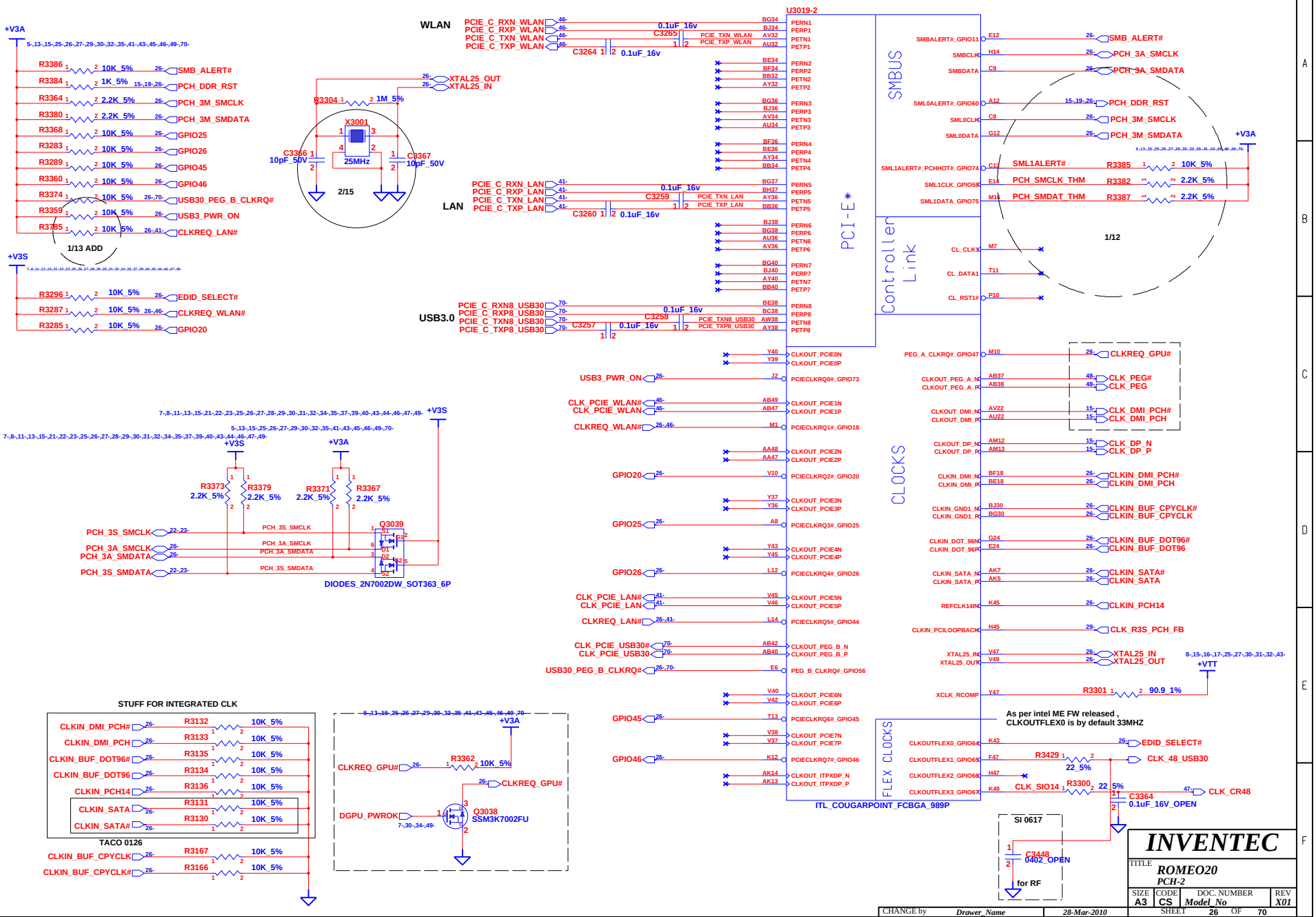
SHEET 22 OF 70


CN3007-1
FOX_AS0A626_U4RG_7H_204P
M_B_A(15:0)
M_B_DQ(63:0)
M_B_DQS(7:0)
M_B_DQS#(7:0)
M_B_BS0
M_B_BS1
M_B_BS2
M_CS#2
M_CS#3
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
M_CKE2
M_CKE3
M_B_CAS#
M_B_RAS#
M_B_WE#
SA0_DIM1
SA1_DIM1
PCH_3S_SMCLK
PCH_3S_SMDATA
M_ODT2
M_ODT3
TP3012
NOTE:
SO-DIMMB SPD ADDRESS IS 0xA4
SO-DIMMB TS ADDRESS IS 0x34
+V3S
R3076 10K_5%
R3075 10K_5%
SA0_DIM1
SA1_DIM1
+V1.5
C3072 330uF_2.5V_OPEN
22uF_6.3V
C3078 0.1uF_16v
C3074 0.1uF_16v
C3075 0.1uF_16v
C3079
C3077
C3076
CN3007-2
C3113 2.2uF_16v
C3109 0.1uF_16v
M_VREF
2/9
DDR3_DRAMRST#
TP3017
C3066 2.2uF_16v
C3067 0.1uF_16v
C3086 2.2uF_16v
C3087 0.1uF_16v
+V0.75S
C3099 47pF_50V
C3101 1uF_6.3V
C3110 1uF_6.3V
C3114 1uF_6.3V
C3121 1uF_6.3V
C3122 1uF_6.3V
R3068 1K_1%_OPEN
R3069 1K_1%_OPEN
R3067 0_5%_OPEN
R3058 1K_1%_OPEN
R3059 1K_1%_OPEN
R3060 0_5%_OPEN
DDR3 SO-DIMM 2
INVENTEC
ROMEO20
SO-DIMM2
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 23 OF 70
CHANGE by Drawer_Name
19-Dec-2010

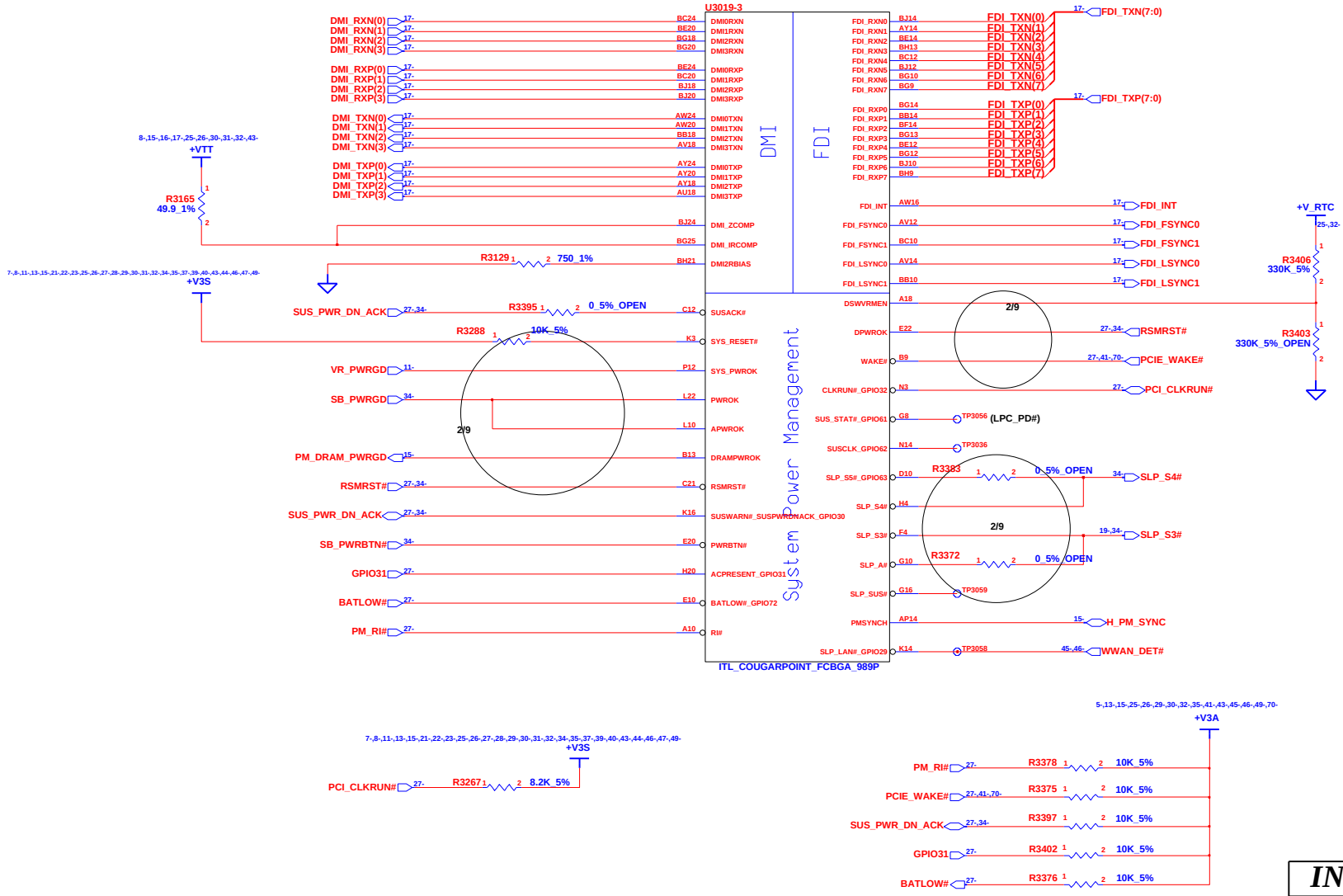
BLANK

INVENTEC			
TITLE: ROMEO20 BLANK			
SIZE: A3	CODE: CS	DOC. NUMBER: Model_No	REV: X01
CHANGE by: Drawer_Name	14-Apr-2010	SHEET 24 OF 70	


+V3AL
(0.03A)
2/9 for issue change
D3016
BAT54C_30V_0.2A
RTCBAT
R3482
1K_5%
+V_RTC
C3538
1uF_6.3v
R3407
20K_5%
C3445
1uF_6.3v
R3408
20K_5%
R3401
1M_5%
C3356
1uF_6.3v
C3444
15pF_50V
X3002
32.768KHz
R3409
10M_5%
C3446
15pF_50V
+V5S
R3398
330K_5%
INTVRMEN_R
1/13 ADD for leakage
Q3105
SSM3K7002FU
HDA_BITCLK
R3294
33_5%
HDA_SYNC
R3412
33_5%
HDA_SYNC_R
HDA_SYNC_PCH
R3786
1M_5%
PCSPKR
R3271
10K_5%_OPEN
HDA_RST#
R3410
33_5%
HDA_SDIN0
C3360
22pF_50V
+V3S_PCHSPI
D3015
BAT54C_30V_0.2A
+V3A
+V3S
HDA_SDOUT
C3447
22pF_50V
Q3040
SSM3K7002FU
R3416
33_5%
HDA_SDO_R
R3432
1K_5%_OPEN
R3293
10K_5%
GPIO13
R3268
0_5%_OPEN
R3411
1K_5%
CLOSE TO PCH
R3262
51_5%
PCH_TCK
PCH_TMS
PCH_TDI
PCH_TDO
L3003
BLM15BB121SN1
R3109
10K_5%_OPEN
U3008
SPI_CS0#
SPI_SO
SPI_CLK
SPI_SI
R3108
3.3K_5%
R3102
3.3K_5%
MXIC_MX25L3206EM2I_12G_SOP_8P
R3787
0_5%_OPEN
PCH_SPI_WP#
C3123
0.1uF_16V
Close TO PCH
HDA_SDO_R
R3484
1K_5%
ME_FLASH_EN
Flash Descriptor Security Overide
HDA_SDO_R
High : Enable
Low : Disable
SPI_CLK
SPI_CS0#
SPI_SI
SPI_SO
3/7 Update 0 ohm to OPEN
U3019-1
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN#_GPIO33
HDA_DOCK_RST#_GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
RTC
IHDA
JTAG
SPI
LPC
SATA 6G
SATA
ITL_COUGARPOINT_FCBGA_989P
LAYOUT NOTE:JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
LAYOUT NOTE:JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
Placememt note
WS
R3352
210_1%
R3351
210_1%
R3264
210_1%
PCH_TDI
PCH_TMS
PCH_TDO
R3349
100_1%
R3354
100_1%
R3263
100_1%
FWH0_LAD0
FWH1_LAD1
FWH2_LAD2
FWH3_LAD3
FWH4_LFRAME#
LDRQ0#
LDRQ1#_GPIO23
SERIRQ
LPC_AD(0)
LPC_AD(1)
LPC_AD(2)
LPC_AD(3)
LPC_FRAME#
GPIO23
R3413
10K_5%_OPEN
R3284
10K_5%
SERIRQ
SATA HDD
SATA ODD
m-SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_RX0N
SATA_RX0P
SATA_TX0N
SATA_TX0P
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_RX1N
SATA_RX1P
SATA_TX1N
SATA_TX1P
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA_RX3N
SATA_RX3P
SATA_TX3N
SATA_TX3P
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
R3191
37.4_1%
R3189
49.9_1%
R3188
750_1%
Place close to PCH
+VTT
+V3S
R3270
10K_5%
SATALED#
SATA0GP_GPIO21
SATA1GP_GPIO19
LED_3S_SATA#
2nd_WLAN_RF_OFF#
BBSTRAP0
R3190
10K_5%
RTCBAT
12/28
CN3015
ACES_50224_0020N_001_2P
BATTERY CELL PN: 6027B0090401
INVENTEC
TITLE
ROMEO20
PCH-1
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 25 OF 70
CHANGE by Drawer_Name
6-Apr-2010


WLAN
LAN
USB3.0
U3019-2
PCI-E*
Controller Link
SMBUS
CLOCKS
FLEX CLOCKS
ITL_COUGARPOINT_FCBGA_989P
DIODES_2N7002DW_SOT363_6P
STUFF FOR INTEGRATED CLK
TACO 0126
1/13 ADD
1/12
2/15
25MHz
SI 0617
for RF
As per intel ME FW released , CLKOUTFLEX0 is by default 33MHZ
INVENTEC
ROMEO20
PCH-2
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 26 OF 70
CHANGE by Drawer_Name 28-Mar-2010

Note: 1.SLP_SUS and SUSACK# are NC if DSW is not supported
2.DPWROK should connect to RSMRST# if DSW not supported
3.PCH_DPWROK pull up to +V3S enables DSW wupport. No install R5261 to disable DSW



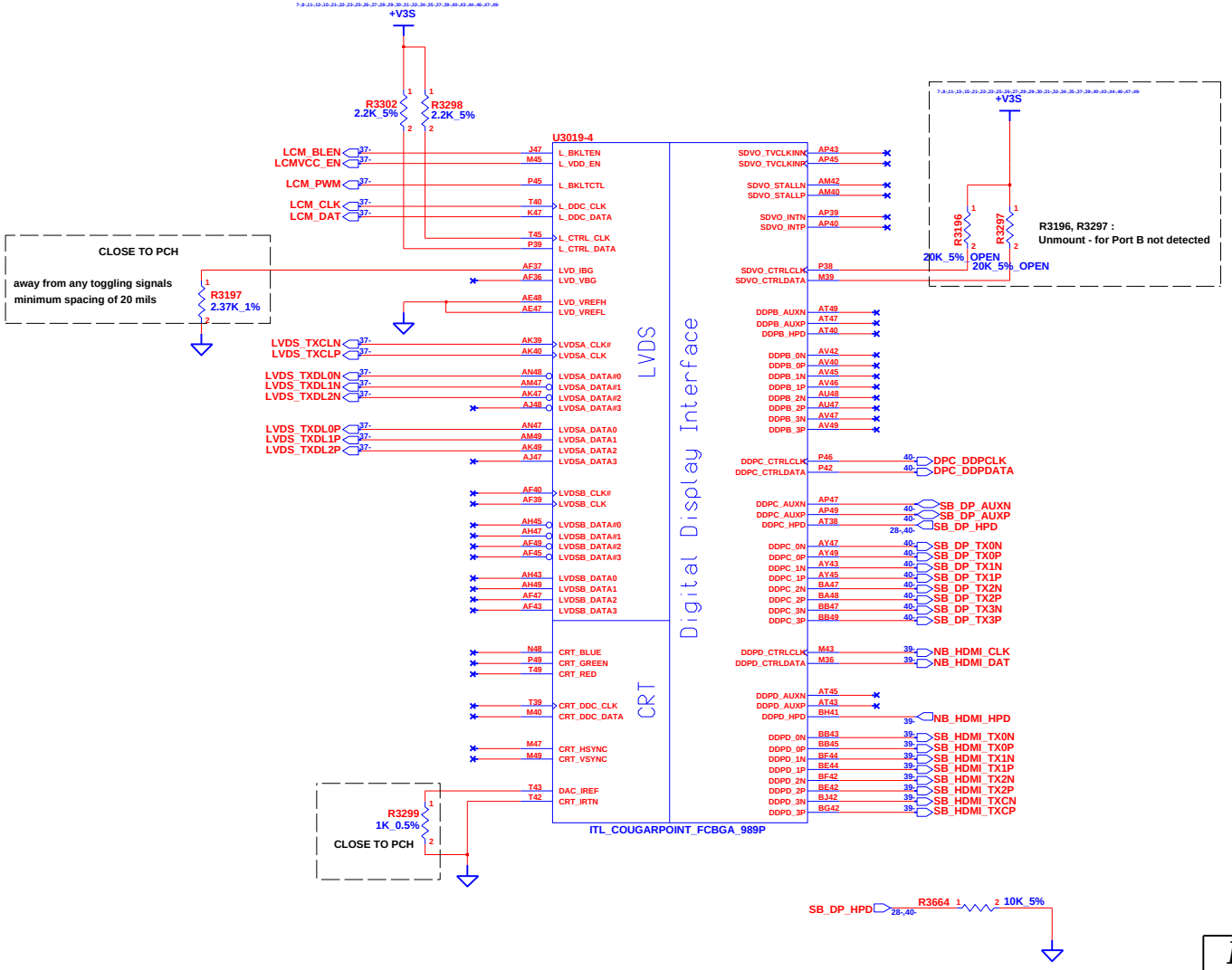
CHANGE by	Drawer_Name	24-Apr-2010	SIZE A3	CODE CS	DOC. NUMBER Model_No

REV X01

SHEET 27 OF 70

INVENTEC

TITLE ROMEO20
PCH-3



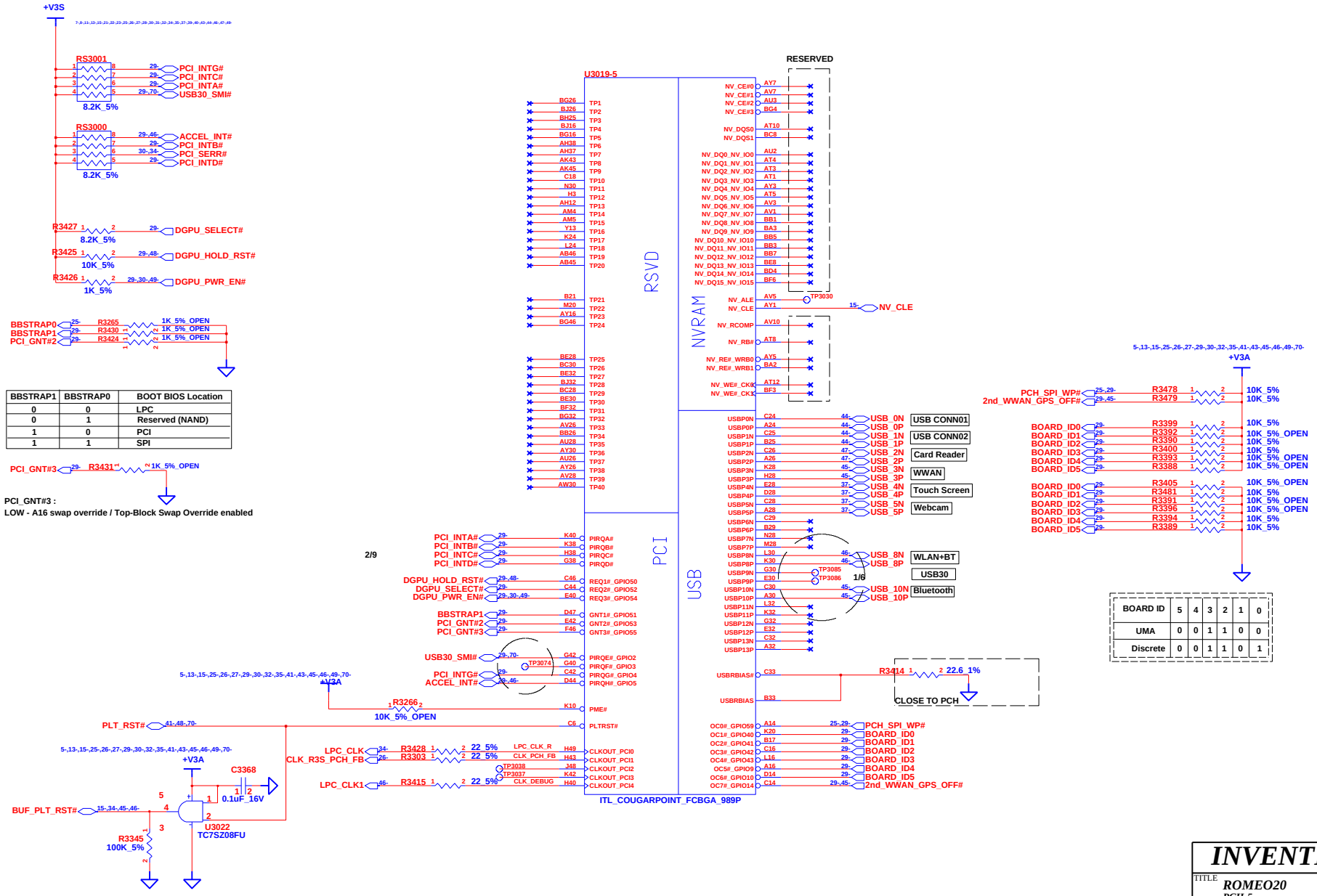
CHANGE by	*Drawer_Name*	*28-Mar-2010*	

INVENTEC

TITLE: ***ROMEO20***
PCH-4

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

SHEET 28 OF 70



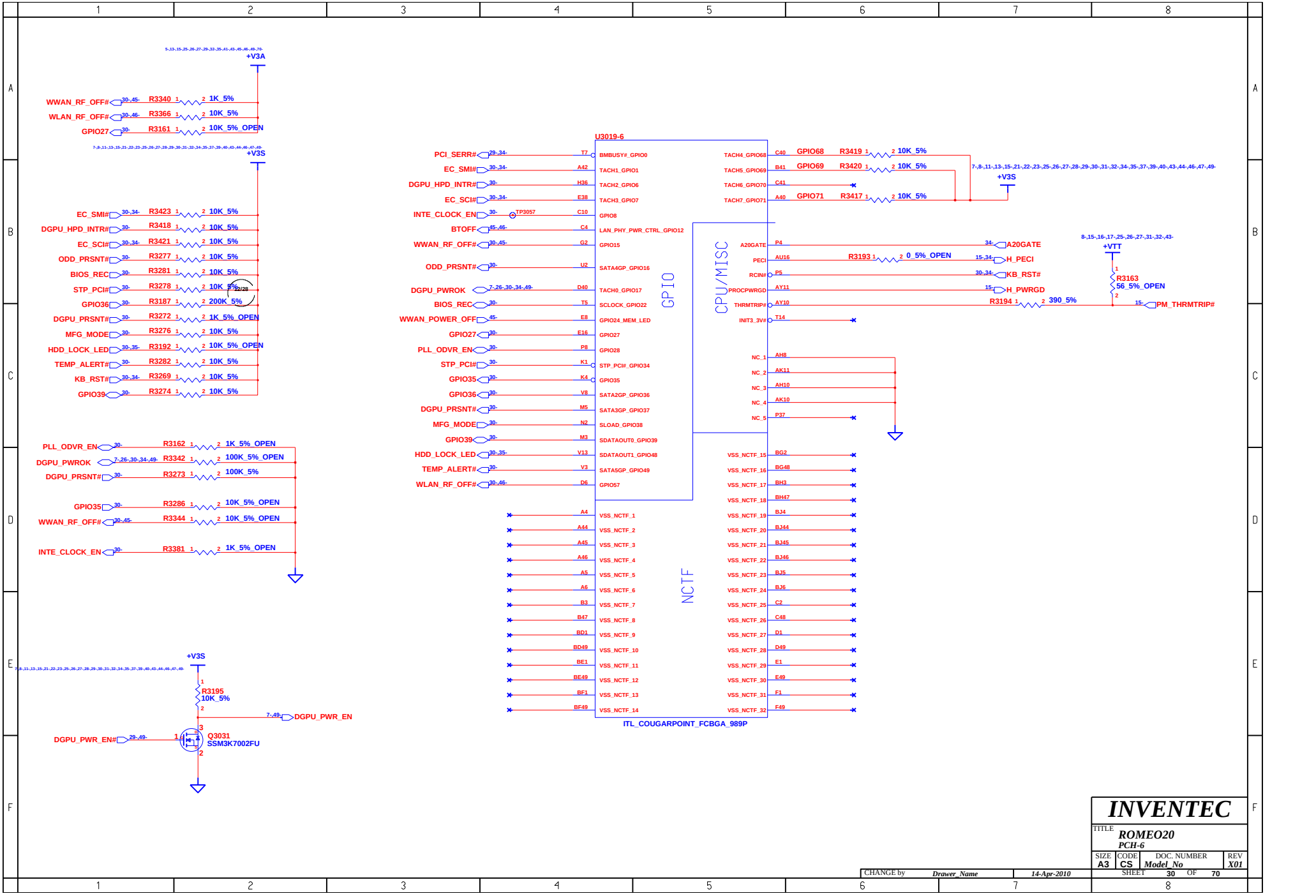
CHANGE by	Drawer_Name	28-Mar-2010				

INVENTEC

TITLE: ROMEO20
PCH-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

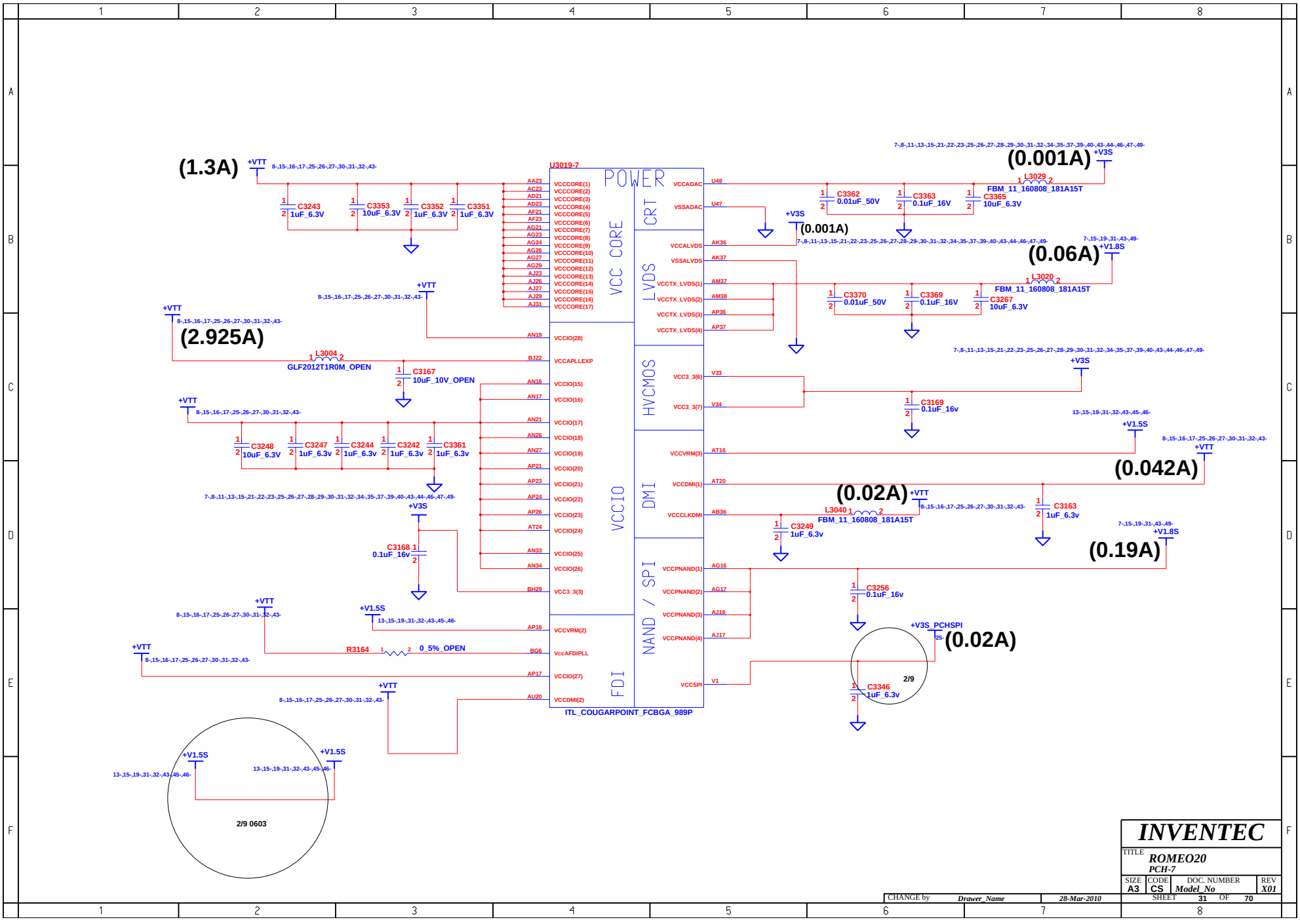
SHEET 29 OF 70

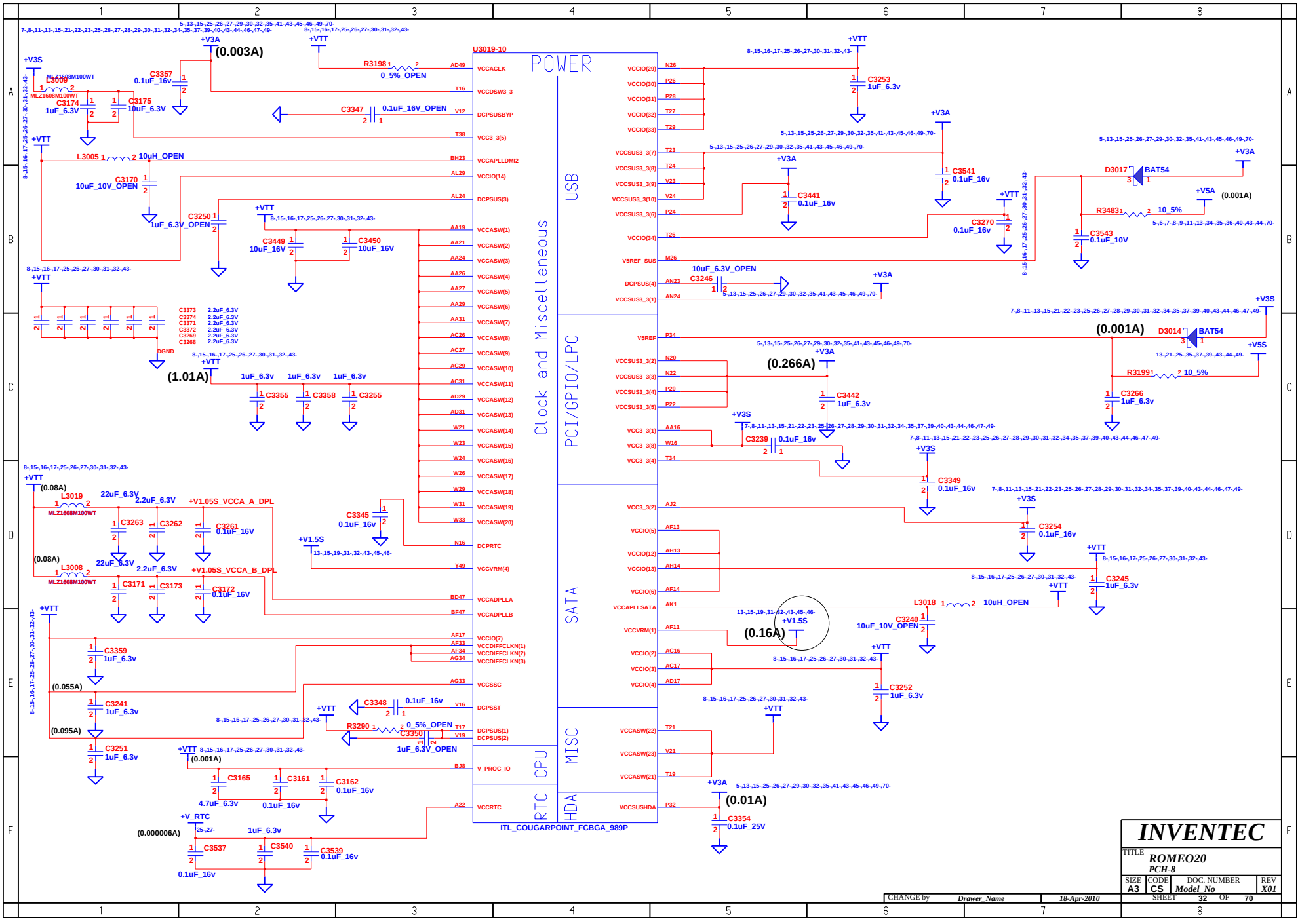


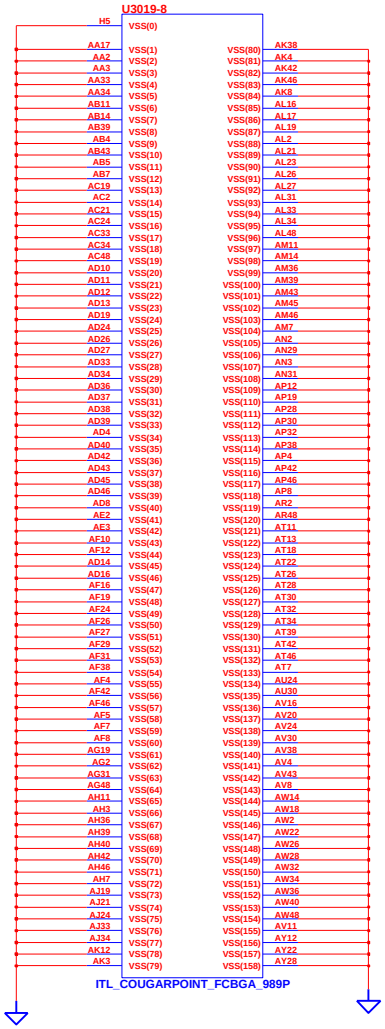
CHANGE by	Drawer_Name	14-Apr-2010	SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
					SHEET 30 OF 70	

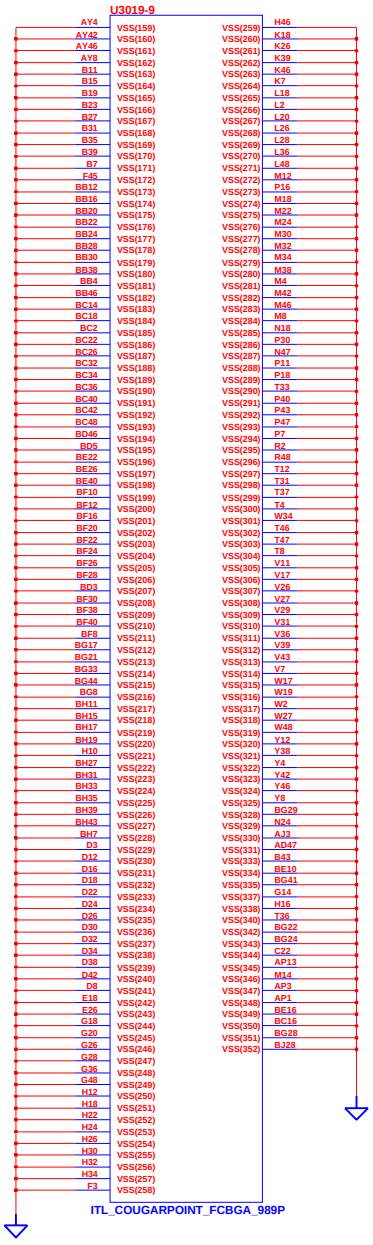
INVENTEC

TITLE: ROMEO20
PCH-6


(1.3A)
(0.001A)
(0.06A)
(2.925A)
(0.042A)
(0.02A)
(0.19A)
(0.02A)
U3019-7
POWER
VCC CORE
CRT
LVDS
HVCMOS
VCCIO
DMI
NAND / SPI
FDI
ITL_COUGARPOINT_FCBGA_989P
+VTT
+V3S
+V1.8S
+V1.5S
+V3S_PCHSPI
C3243 1uF_6.3V
C3353 10uF_6.3V
C3352 1uF_6.3V
C3351 1uF_6.3V
C3362 0.01uF_50V
C3363 0.1uF_16V
C3365 10uF_6.3V
L3029 FBM_11_160808_181A15T
C3370 0.01uF_50V
C3369 0.1uF_16V
C3267 10uF_6.3V
L3020 FBM_11_160808_181A15T
L3004 GLF2012T1R0M_OPEN
C3167 10uF_10V_OPEN
C3248 10uF_6.3V
C3247 1uF_6.3v
C3244 1uF_6.3v
C3242 1uF_6.3v
C3361 1uF_6.3v
C3168 0.1uF_16v
C3169 0.1uF_16v
C3163 1uF_6.3v
L3040 FBM_11_160808_181A15T
C3249 1uF_6.3v
C3256 0.1uF_16v
C3346 1uF_6.3v
R3164 0_5%_OPEN
2/9
2/9 0603
INVENTEC
TITLE
ROMEO20
PCH-7
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 31 OF 70
CHANGE by Drawer_Name 28-Mar-2010


U3019-10
ITL_COUGARPOINT_FCBGA_989P
POWER
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
HDA
RTC
CPU
+V3A
(0.003A)
+VTT
+V3S
+V5A
+V5S
+V_RTC
+V1.5S
+V1.05S_VCCA_A_DPL
+V1.05S_VCCA_B_DPL
(1.01A)
(0.266A)
(0.16A)
(0.001A)
(0.08A)
(0.055A)
(0.095A)
(0.000006A)
R3198 0_5%_OPEN
R3290 0_5%_OPEN
R3483 10_5%
R3199 10_5%
C3347 0.1uF_16V_OPEN
C3350 1uF_6.3V_OPEN
C3246 10uF_6.3V_OPEN
C3170 10uF_10V_OPEN
C3250 1uF_6.3V_OPEN
C3240 10uF_10V_OPEN
L3009 MLZ1608M100WT
L3005 10uH_OPEN
L3018 10uH_OPEN
D3017 BAT54
D3014 BAT54
INVENTEC
TITLE
ROMEO20
PCH-8
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 32 OF 70
CHANGE by Drawer_Name
18-Apr-2010





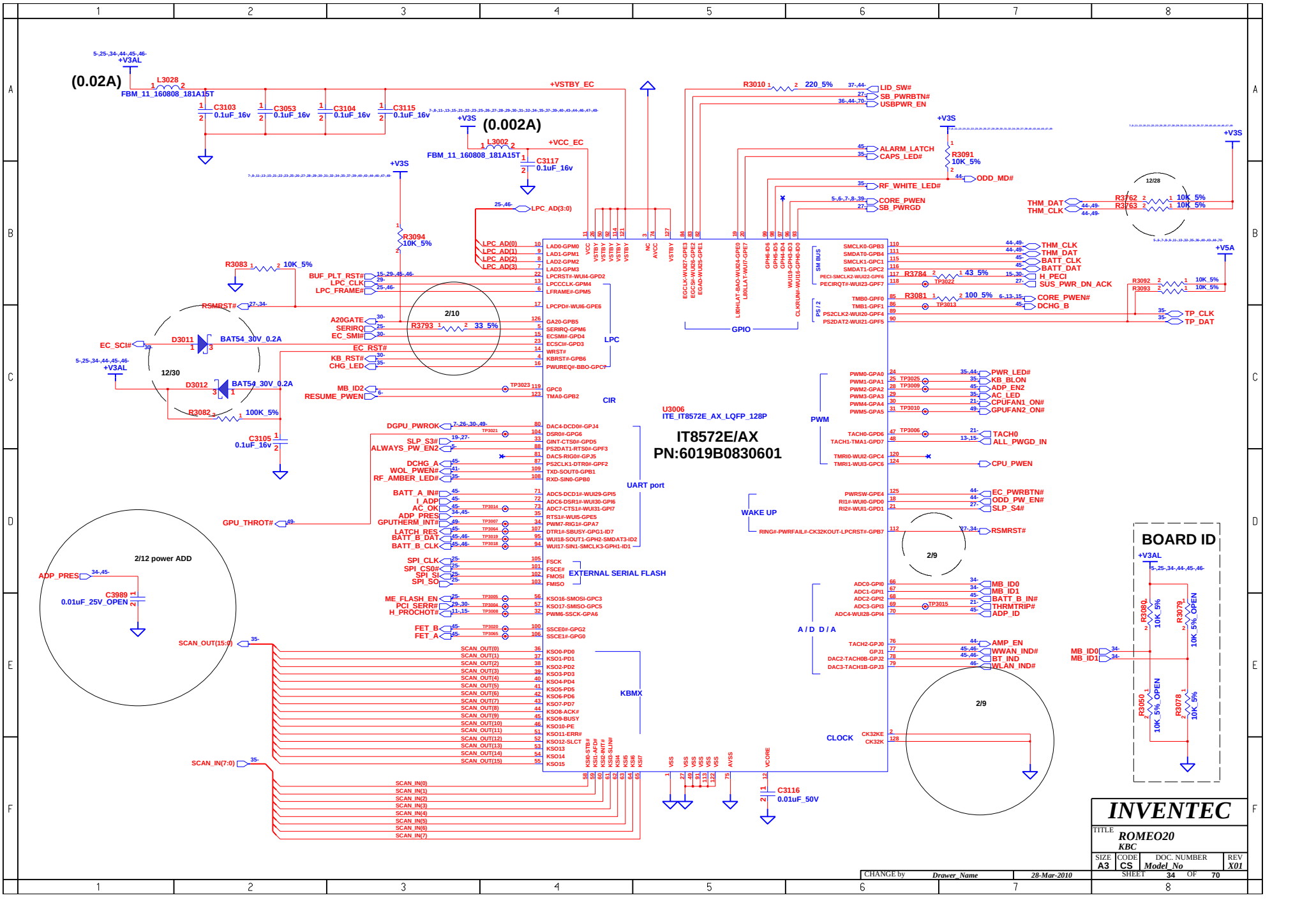
CHANGE by	*Drawer_Name*	*28-Mar-2010*	

INVENTEC

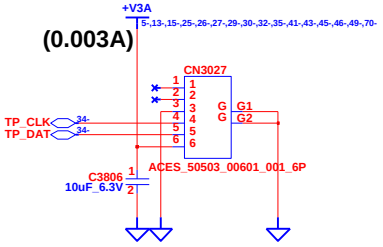
TITLE: ***ROMEO20***
PCH-9

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

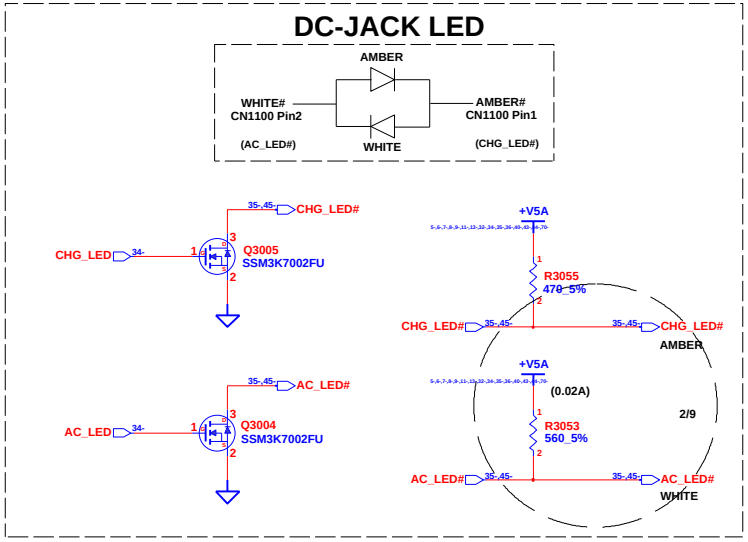
SHEET 33 OF 70


+V3AL
(0.02A)
L3028
FBM_11_160808_181A15T
C3103 0.1uF_16v
C3053 0.1uF_16v
C3104 0.1uF_16v
C3115 0.1uF_16v
+V3S
(0.002A)
L3002
FBM_11_160808_181A15T
C3117 0.1uF_16v
+VSTBY_EC
+VCC_EC
R3094 10K_5%
R3083 10K_5%
RSMRST#
BUF_PLT_RST#
LPC_CLK
LPC_FRAME#
LPC_AD(3:0)
LPC_AD(0)
LPC_AD(1)
LPC_AD(2)
LPC_AD(3)
A20GATE
SERIRQ
EC_SMI#
EC_RST#
KB_RST#
CHG_LED
R3793 33_5%
2/10
EC_SCI#
D3011 BAT54_30V_0.2A
D3012 BAT54_30V_0.2A
12/30
R3082 100K_5%
C3105 0.1uF_16v
MB_ID2
RESUME_PWEN
TP3023
DGPU_PWROK
SLP_S3#
ALWAYS_PW_EN2
DCHG_A
WOL_PWEN#
RF_AMBER_LED#
BATT_A_IN#
I_ADP
AC_OK
ADP_PRES
GPUTHERM_INT#
LATCH_RES
BATT_B_DAT
BATT_B_CLK
GPU_THROT#
SPI_CLK
SPI_CS0#
SPI_SI
SPI_SO
ME_FLASH_EN
PCI_SERR#
H_PROCHOT#
FET_B
FET_A
SCAN_OUT(15:0)
SCAN_IN(7:0)
SCAN_OUT(0)
SCAN_OUT(1)
SCAN_OUT(2)
SCAN_OUT(3)
SCAN_OUT(4)
SCAN_OUT(5)
SCAN_OUT(6)
SCAN_OUT(7)
SCAN_OUT(8)
SCAN_OUT(9)
SCAN_OUT(10)
SCAN_OUT(11)
SCAN_OUT(12)
SCAN_OUT(13)
SCAN_OUT(14)
SCAN_OUT(15)
SCAN_IN(0)
SCAN_IN(1)
SCAN_IN(2)
SCAN_IN(3)
SCAN_IN(4)
SCAN_IN(5)
SCAN_IN(6)
SCAN_IN(7)
2/12 power ADD
C3989 0.01uF_25V_OPEN
U3006
ITE_IT8572E_AX_LQFP_128P
IT8572E/AX
PN:6019B0830601
LPC
CIR
UART port
EXTERNAL SERIAL FLASH
KBMX
GPIO
PWM
WAKE UP
A / D D / A
CLOCK
LAD0-GPM0
LAD1-GPM1
LAD2-GPM2
LAD3-GPM3
LPCRST#-WUI4-GPD2
LPCCCLK-GPM4
LFRAME#-GPM5
LPCPD#-WUI6-GPE6
GA20-GPB5
SERIRQ-GPM6
ECSMI#-GPD4
ECSCI#-GPD3
WRST#
KBRST#-GPB6
PWUREQ#-BBO-GPC7
GPC0
TMA0-GPB2
DAC4-DCD0#-GPJ4
DSR0#-GPG6
GINT-CTS0#-GPD5
PS2DAT1-RTS0#-GPF3
DAC5-RIG0#-GPJ5
PS2CLK1-DTR0#-GPF2
TXD-SOUT0-GPB1
RXD-SIN0-GPB0
ADC5-DCD1#-WUI29-GPI5
ADC6-DSR1#-WUI30-GPI6
ADC7-CTS1#-WUI31-GPI7
RTS1#-WUI5-GPE5
PWM7-RIG1#-GPA7
DTR1#-SBUSY-GPG1-ID7
WUI18-SOUT1-GPH2-SMDAT3-ID2
WUI17-SIN1-SMCLK3-GPH1-ID1
FSCK
FSCE#
FMOSI
FMISO
KSO16-SMOSI-GPC3
KSO17-SMISO-GPC5
PWM6-SSCK-GPA6
SSCE0#-GPG2
SSCE1#-GPG0
KSO0-PD0
KSO1-PD1
KSO2-PD2
KSO3-PD3
KSO4-PD4
KSO5-PD5
KSO6-PD6
KSO7-PD7
KSO8-ACK#
KSO9-BUSY
KSO10-PE
KSO11-ERR#
KSO12-SLCT
KSO13
KSO14
KSO15
KSI0-STB#
KSI1-AFD#
KSI2-INIT#
KSI3-SLIN#
KSI4
KSI5
KSI6
KSI7
R3010 220_5%
LID_SW#
SB_PWRBTN#
USBPWR_EN
ALARM_LATCH
CAPS_LED#
R3091 10K_5%
ODD_MD#
RF_WHITE_LED#
CORE_PWEN
SB_PWRGD
SMCLK0-GPB3
SMDAT0-GPB4
SMCLK1-GPC1
SMDAT1-GPC2
PECI-SMCLK2-WUI22-GPF6
PECIRQT#-WUI23-GPF7
R3784 43_5%
TP3022
TMB0-GPF0
TMB1-GPF1
R3081 100_5%
TP3013
PS2CLK2-WUI20-GPF4
PS2DAT2-WUI21-GPF5
THM_CLK
THM_DAT
BATT_CLK
BATT_DAT
H_PECI
SUS_PWR_DN_ACK
CORE_PWEN#
DCHG_B
TP_CLK
TP_DAT
R3762 10K_5%
R3763 10K_5%
12/28
THM_DAT
THM_CLK
R3092 10K_5%
R3093 10K_5%
+V5A
PWM0-GPA0
PWM1-GPA1
PWM2-GPA2
PWM3-GPA3
PWM4-GPA4
PWM5-GPA5
PWR_LED#
KB_BLON
ADP_EN2
AC_LED
CPUFAN1_ON#
GPUFAN2_ON#
TACH0-GPD6
TACH1-TMA1-GPD7
TACH0
ALL_PWGD_IN
TMRI0-WUI2-GPC4
TMRI1-WUI3-GPC6
CPU_PWEN
PWRSW-GPE4
RI1#-WUI0-GPD0
RI2#-WUI1-GPD1
EC_PWRBTN#
ODD_PW_EN#
SLP_S4#
RING#-PWRFAIL#-CK32KOUT-LPCRST#-GPB7
RSMRST#
2/9
ADC0-GPI0
ADC1-GPI1
ADC2-GPI2
ADC3-GPI3
ADC4-WUI28-GPI4
TP3015
MB_ID0
MB_ID1
BATT_B_IN#
THRMTRIP#
ADP_ID
TACH2-GPJ0
GPJ1
DAC2-TACH0B-GPJ2
DAC3-TACH1B-GPJ3
AMP_EN
WWAN_IND#
BT_IND
WLAN_IND#
2/9
CK32KE
CK32K
C3116 0.01uF_50V
BOARD ID
R3080 10K_5%
R3079 10K_5%_OPEN
R3050 10K_5%_OPEN
R3078 10K_5%
MB_ID0
MB_ID1
INVENTEC
TITLE
ROMEO20
KBC
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
CHANGE by Drawer_Name
28-Mar-2010
SHEET 34 OF 70

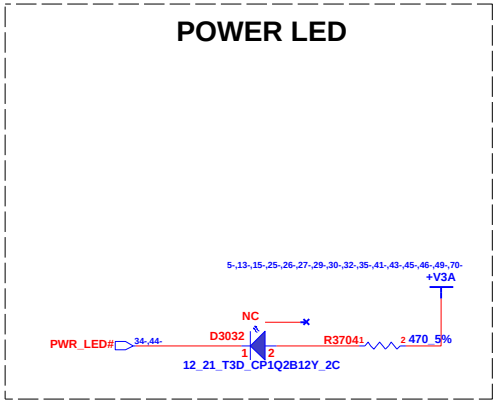
TouchPad Module CONN



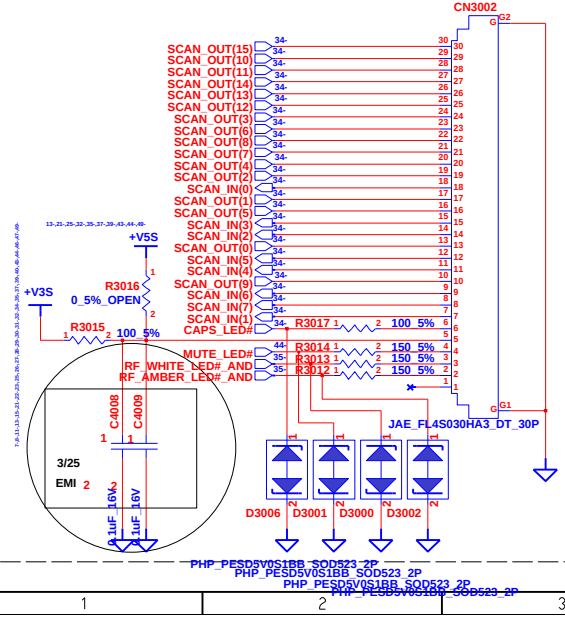
DC-JACK LED



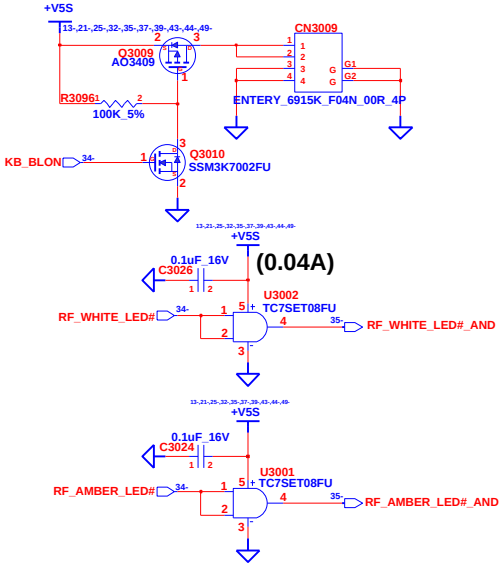
POWER LED



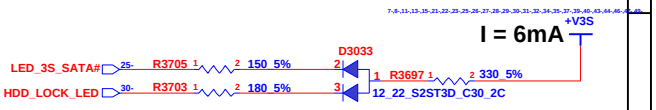
KeyBoard CONN (30 pin)



Backlight connector



SATA LED & HDD-HALTED LED



CHANGE by	Drawer_Name	28-Mar-2010

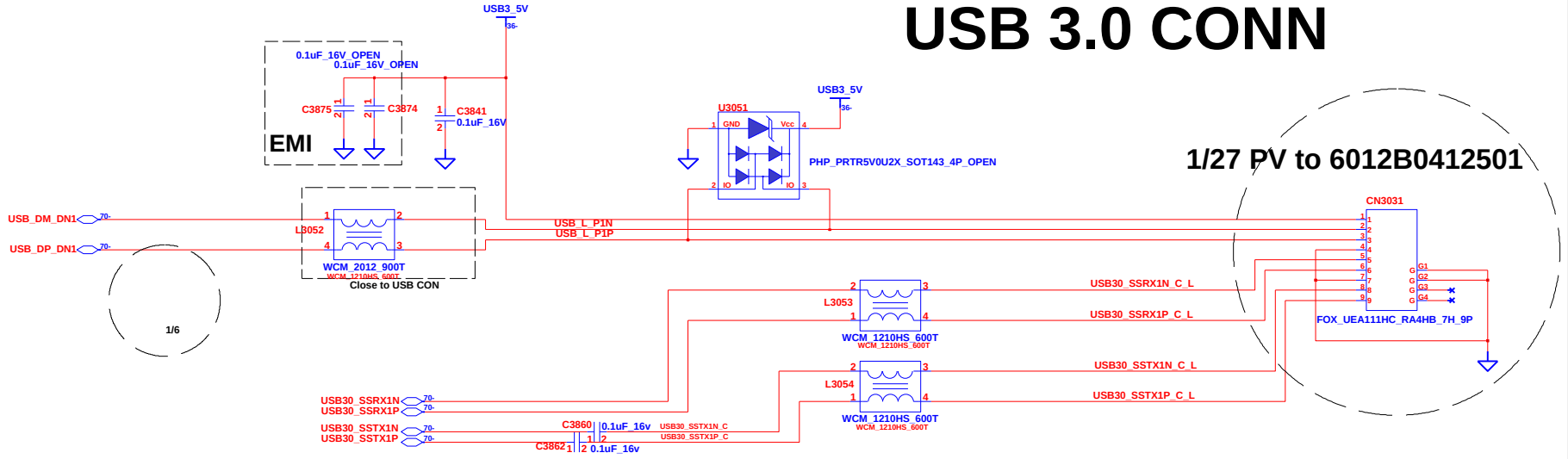
INVENTEC

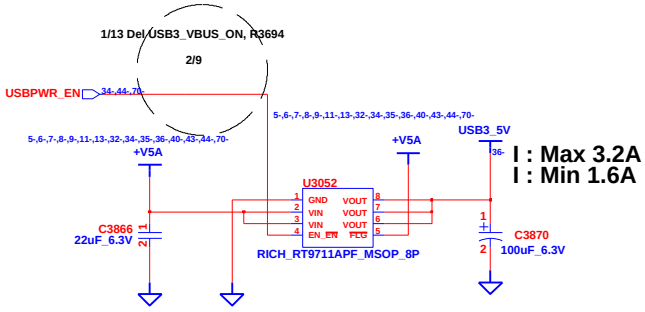
TITLE: ROMEO20
Keyboard & Touchpad

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 35 OF 70

USB 3.0 CONN





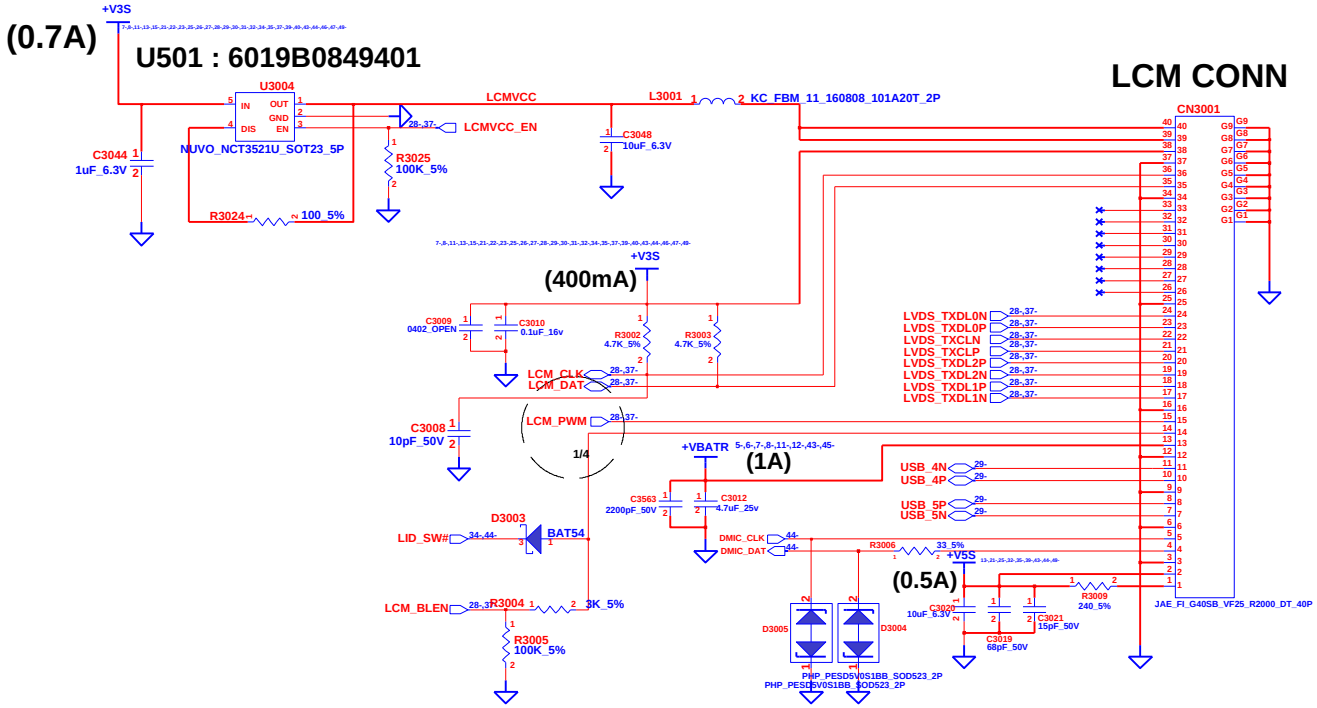
CHANGE by	Drawer_Name	19-Apr-2010	

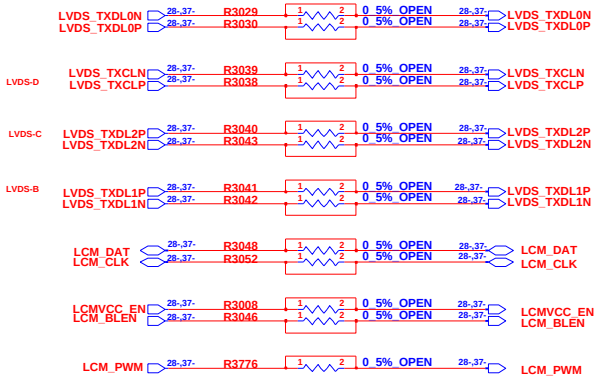
INVENTEC

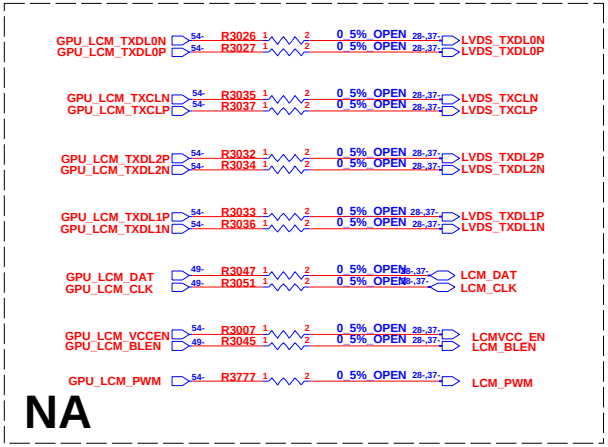
TITLE: ROMEO20
USB 3.0

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 36 OF 70







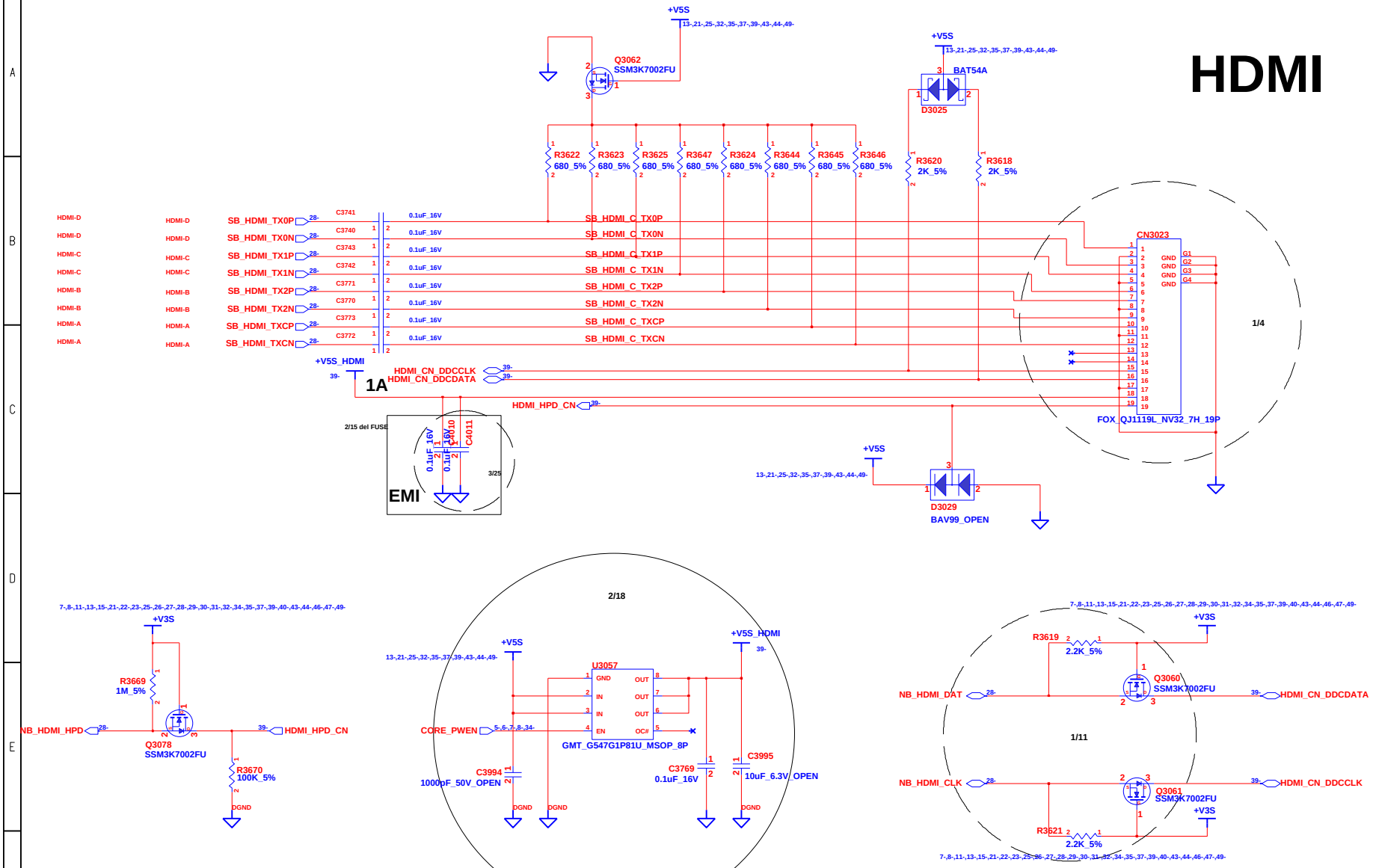
INVENTEC

TITLE	ROMEO20 LCM			
SIZE A3	CODE CS	DOC. NUMBER Model_No		REV X01
CHANGE by Drawer_Name	28-Mar-2010	SHEET 37 OF 70		

BLANK

INVENTEC			
TITLE *ROMEO20*			
SIZE A3	CODE CS	DOC. NUMBER *Model_No*	REV *X01*
CHANGE by *Drawer_Name*	*6-May-2010*	SHEET 38 OF 70	

HDMI



CHANGE by	Drawer_Name	28-Mar-2010			

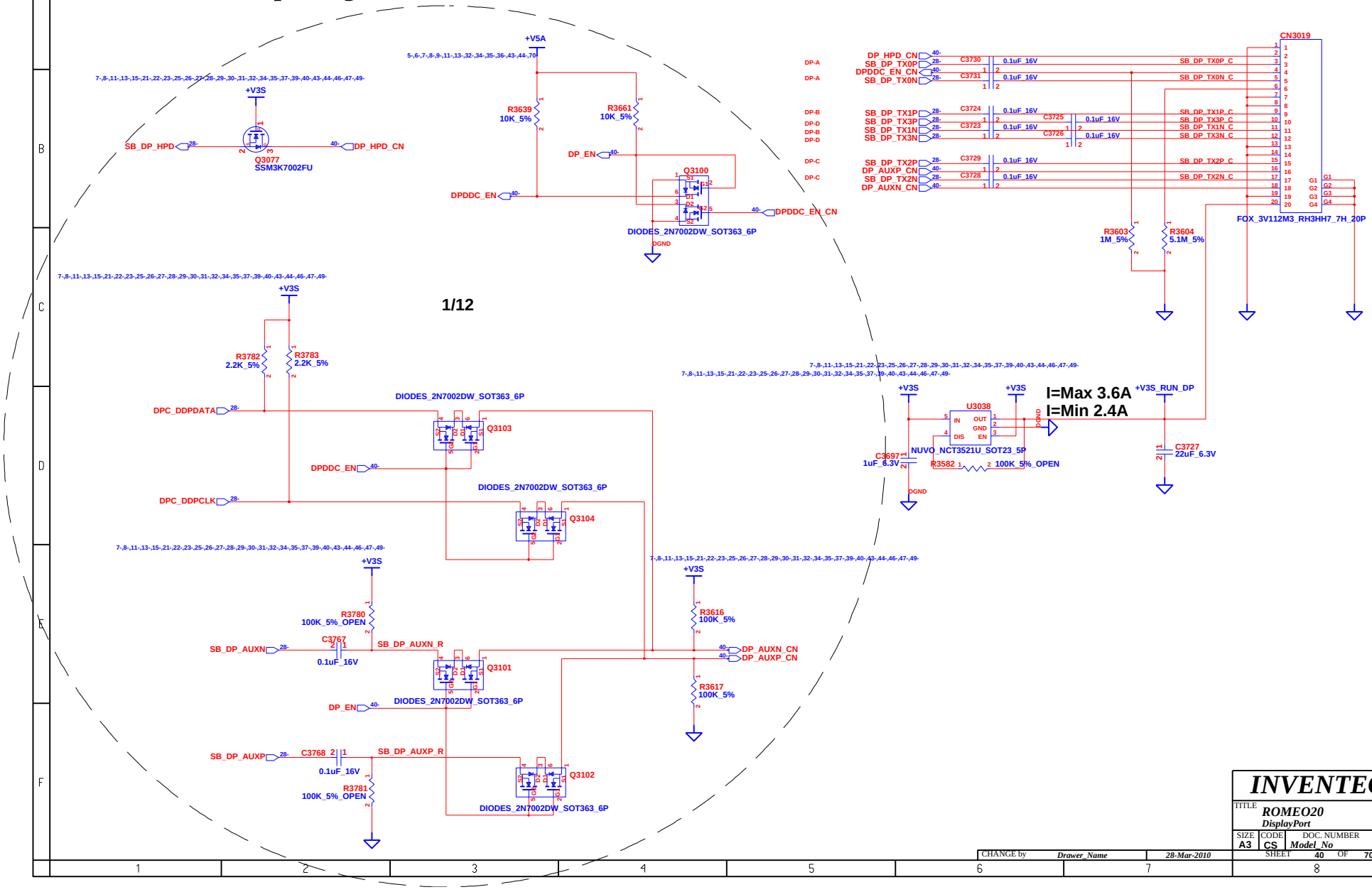
INVENTEC

TITLE: ROMEO20 HDMI

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 39 OF 70

Mini Display Port



CHANGE by	Drawer_Name	28-Mar-2010	

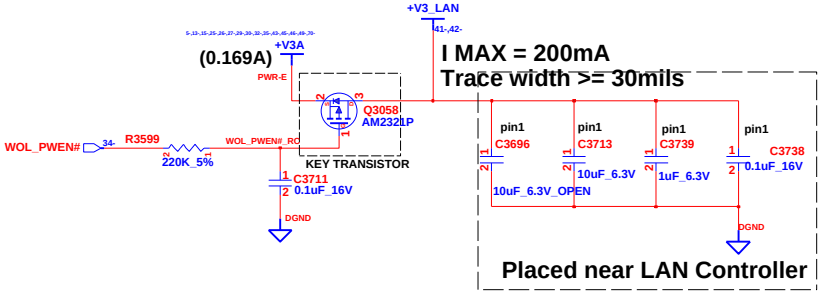
INVENTEC

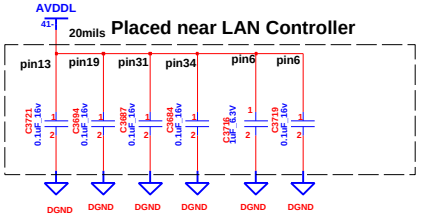
TITLE: *ROMEO20*
DisplayPort

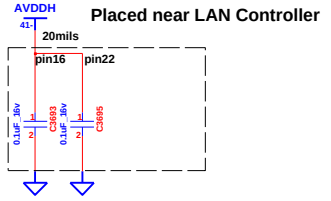
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

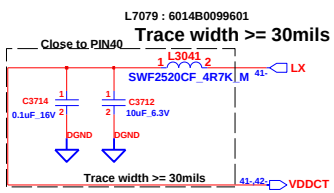
SHEET 40 OF 70

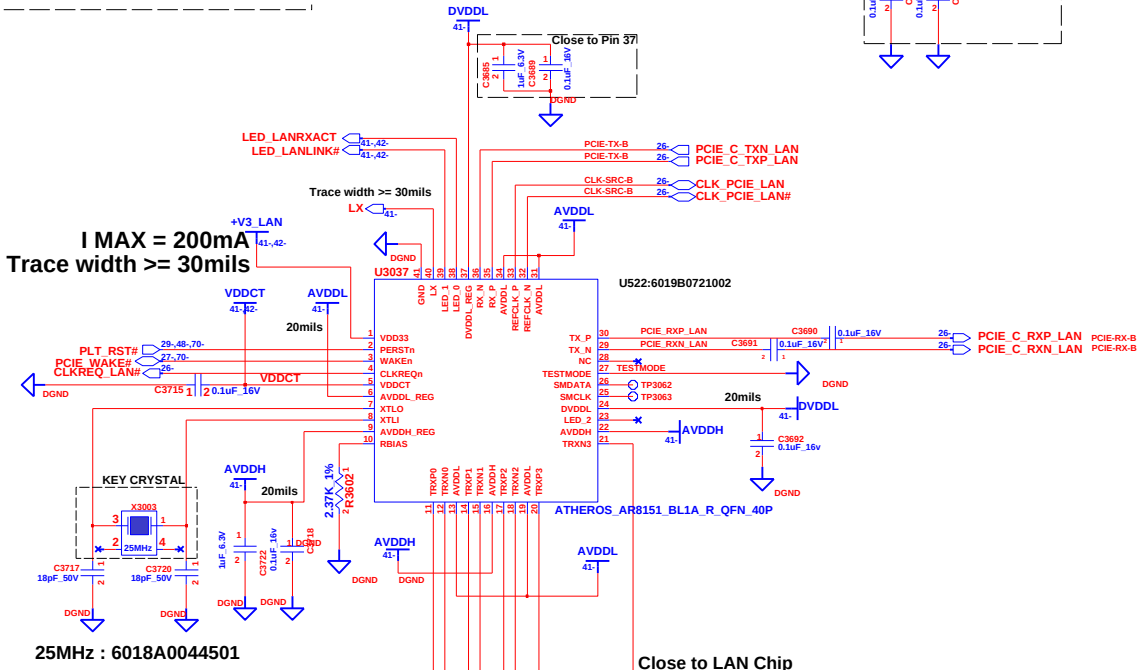
LAN

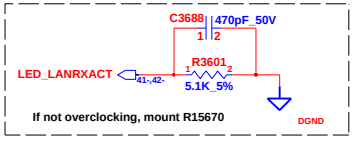


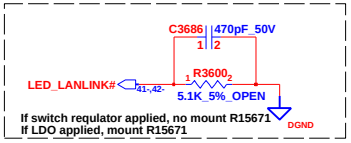


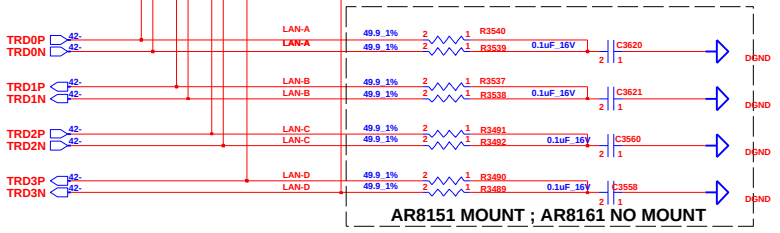








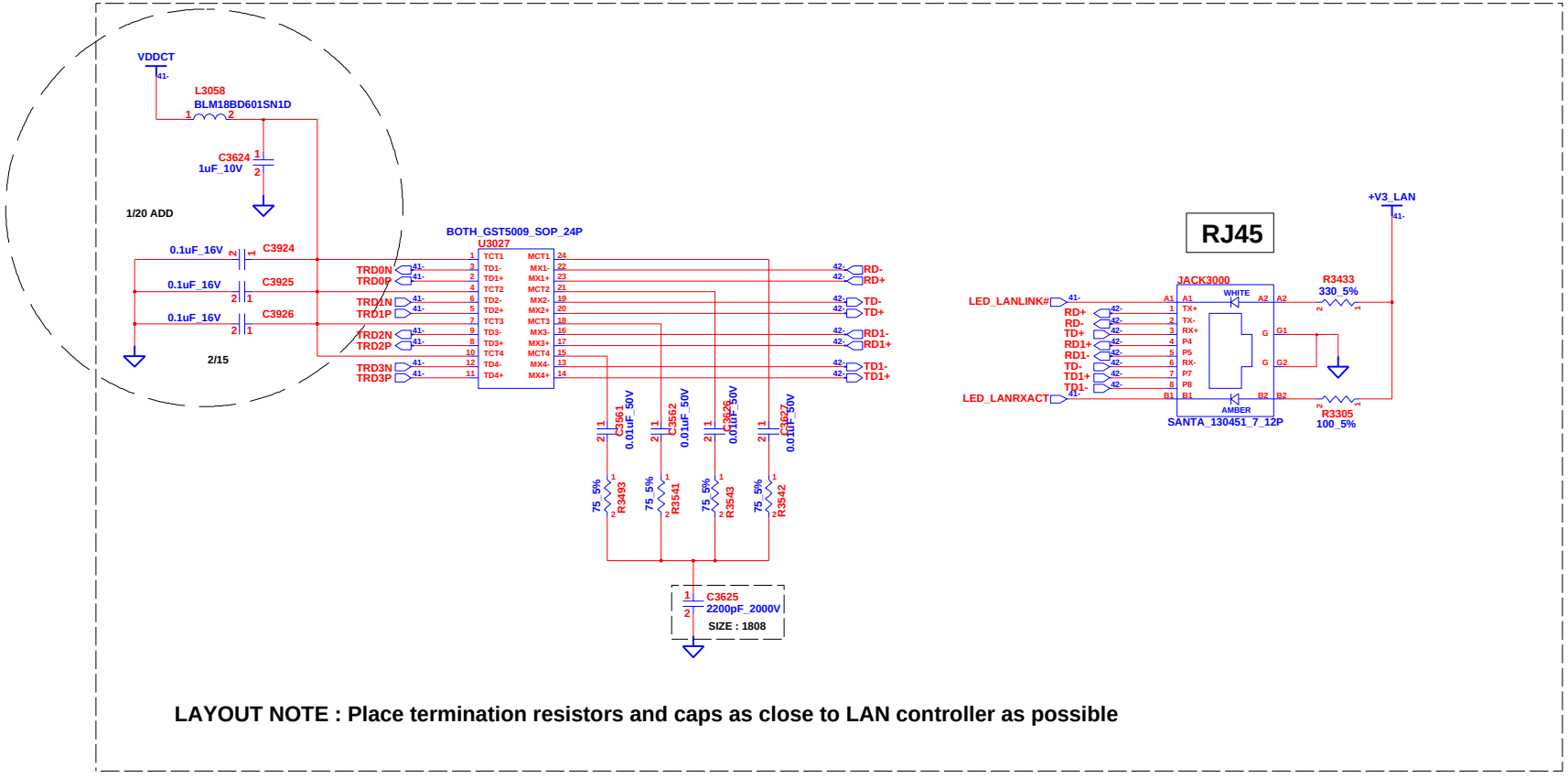




CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

TITLE	ROMEO20 LAN		
SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
SHEET 41 OF 70			



LAYOUT NOTE : Place termination resistors and caps as close to LAN controller as possible

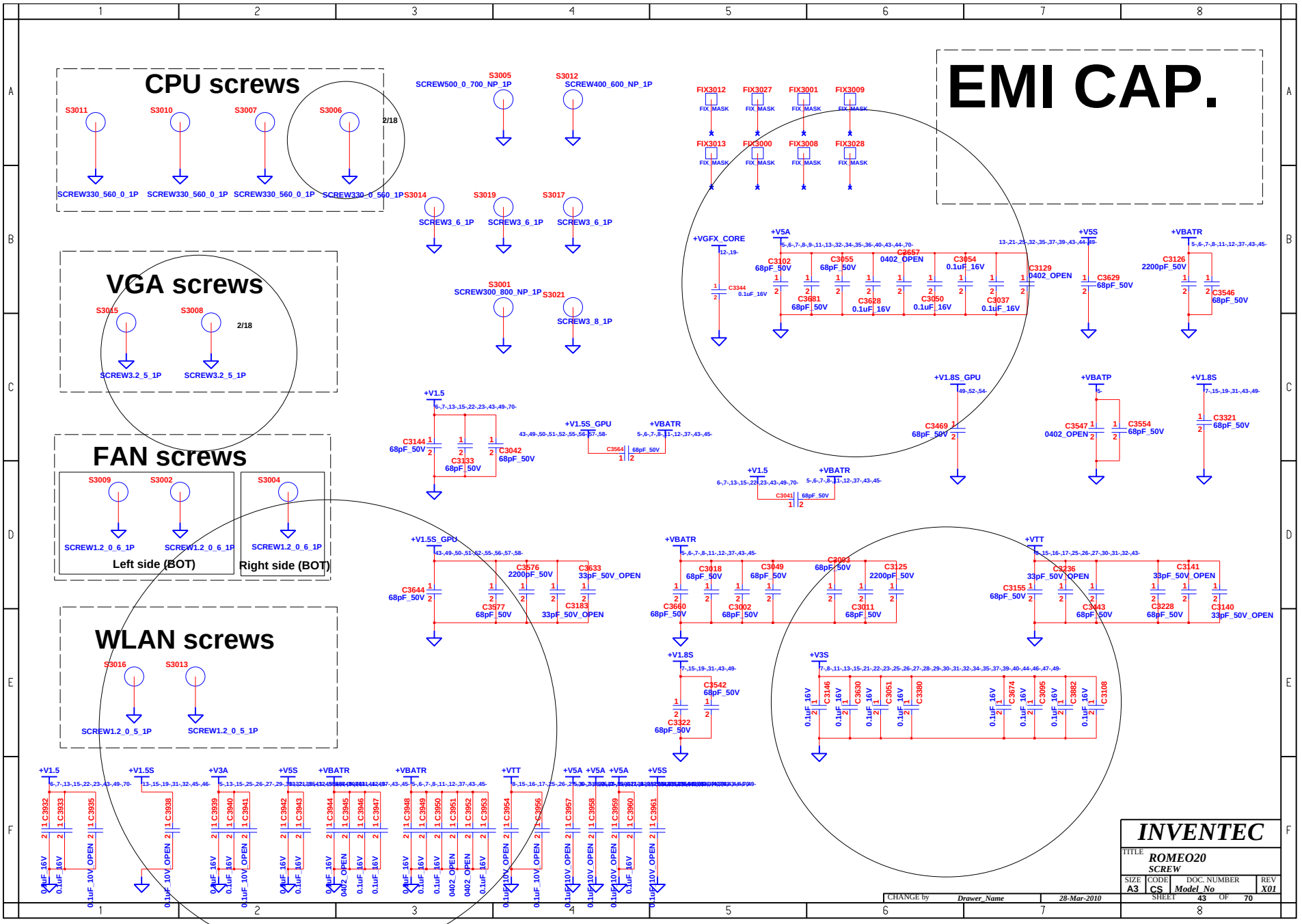
CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

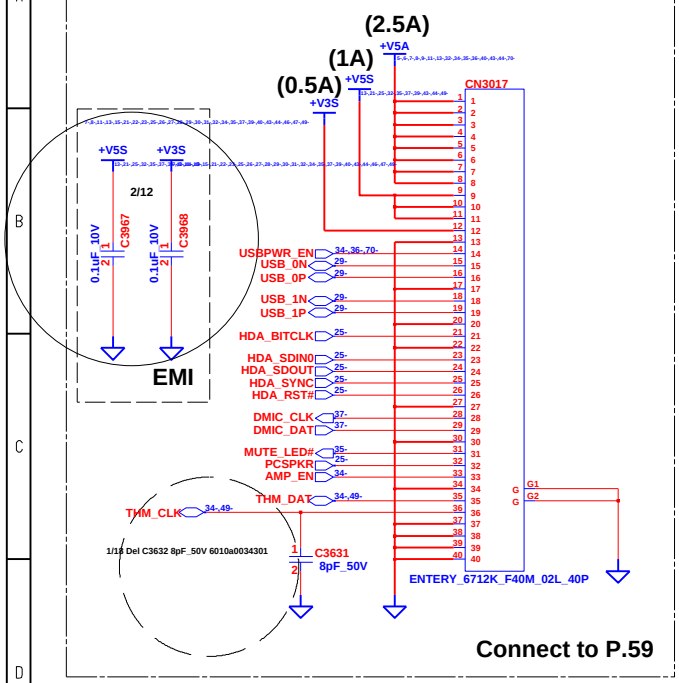
TITLE: *ROMEO20*
RJ-45

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

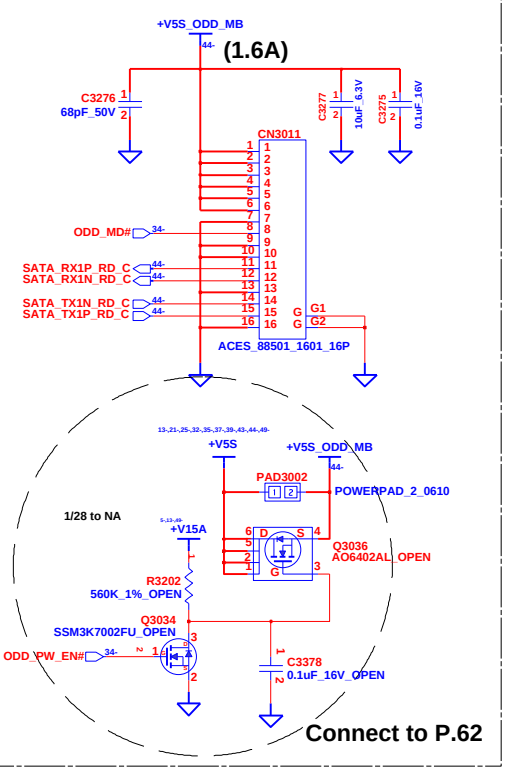
SHEET 42 OF 70


EMI CAP.
CPU screws
S3011
S3010
S3007
S3006
2/18
SCREW330_560_0_1P
SCREW330_560_0_1P
SCREW330_560_0_1P
SCREW330_560_0_1P
S3005
SCREW500_0_700_NP_1P
S3012
SCREW400_600_NP_1P
S3014
SCREW3_6_1P
S3019
SCREW3_6_1P
S3017
SCREW3_6_1P
S3001
SCREW300_800_NP_1P
S3021
SCREW3_8_1P
VGA screws
S3015
S3008
2/18
SCREW3.2_5_1P
SCREW3.2_5_1P
FAN screws
S3009
S3002
S3004
SCREW1.2_0_6_1P
SCREW1.2_0_6_1P
SCREW1.2_0_6_1P
Left side (BOT)
Right side (BOT)
WLAN screws
S3016
S3013
SCREW1.2_0_5_1P
SCREW1.2_0_5_1P
FIX3012
FIX3027
FIX3001
FIX3009
FIX3013
FIX3000
FIX3008
FIX3028
FIX_MASK
+VGFX_CORE
+V5A
+V5S
+VBATR
C3102 68pF_50V
C3055 68pF_50V
C2657 0402_OPEN
C3054 0.1uF_16V
C3129 0402_OPEN
C3629 68pF_50V
C3126 2200pF_50V
C3546 68pF_50V
C3344 0.1uF_16V
C3681 68pF_50V
C3628 0.1uF_16V
C3050 0.1uF_16V
C3037 0.1uF_16V
+V1.5
+V1.5S_GPU
+VBATR
C3144 68pF_50V
C3133 68pF_50V
C3042 68pF_50V
C3564 68pF_50V
+V1.8S_GPU
+VBATP
+V1.8S
C3469 68pF_50V
C3547 0402_OPEN
C3554 68pF_50V
C3321 68pF_50V
+V1.5
+VBATR
C3041 68pF_50V
+V1.5S_GPU
+VBATR
+VTT
C3644 68pF_50V
C3576 2200pF_50V
C3633 33pF_50V_OPEN
C3577 68pF_50V
C3183 33pF_50V_OPEN
C3018 68pF_50V
C3049 68pF_50V
C2003 68pF_50V
C3125 2200pF_50V
C3660 68pF_50V
C3002 68pF_50V
C3011 68pF_50V
C3236 33pF_50V_OPEN
C3155 68pF_50V
C3443 68pF_50V
C3141 33pF_50V_OPEN
C3228 68pF_50V
C3140 33pF_50V_OPEN
+V1.8S
C3542 68pF_50V
C3322 68pF_50V
+V3S
C3146
C3630
C3051
C3380
C3674
C3095
C3882
C3108
0.1uF_16V
+V1.5
+V1.5S
+V3A
+V5S
+VBATR
+VBATR
+VTT
+V5A
+V5A
+V5A
+V5S
C3932
C3933
C3935
C3938
C3939
C3940
C3941
C3942
C3943
C3944
C3945
C3946
C3947
C3948
C3949
C3950
C3951
C3952
C3953
C3954
C3956
C3957
C3958
C3959
C3960
C3961
0.1uF_16V
0.1uF_10V_OPEN
0402_OPEN
INVENTEC
TITLE ROMEO20 SCREW
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 43 OF 70
CHANGE by Drawer_Name
28-Mar-2010

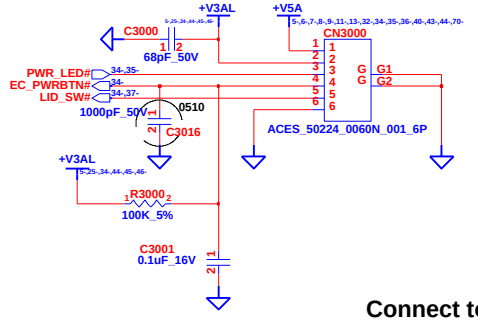
USB Board CN on MB



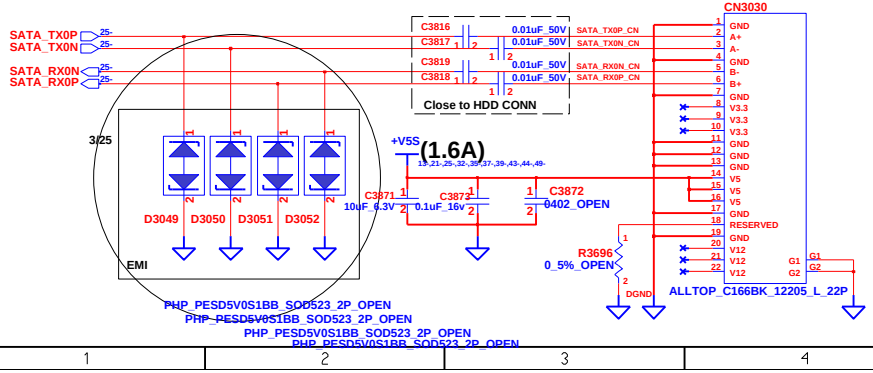
SATA ODD FFC CONN on MB

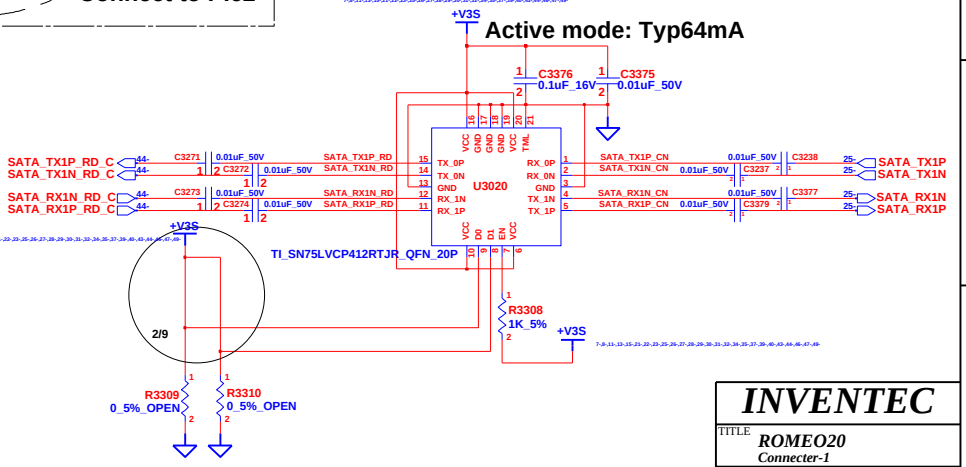


Power Switch BOARD CN on MB



SATA HDD CONN



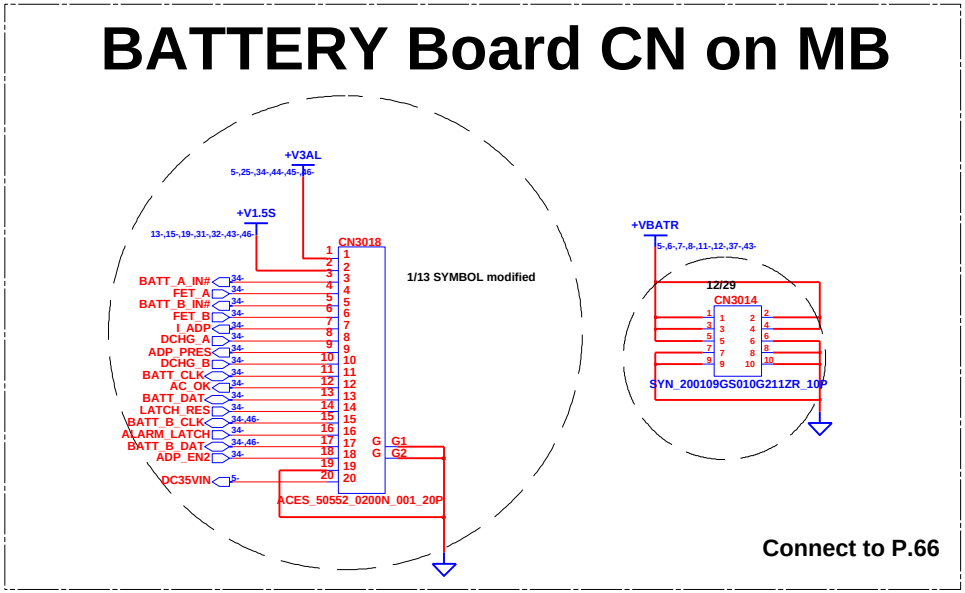


CHANGE by	Drawer_Name	17-Dec-2010	

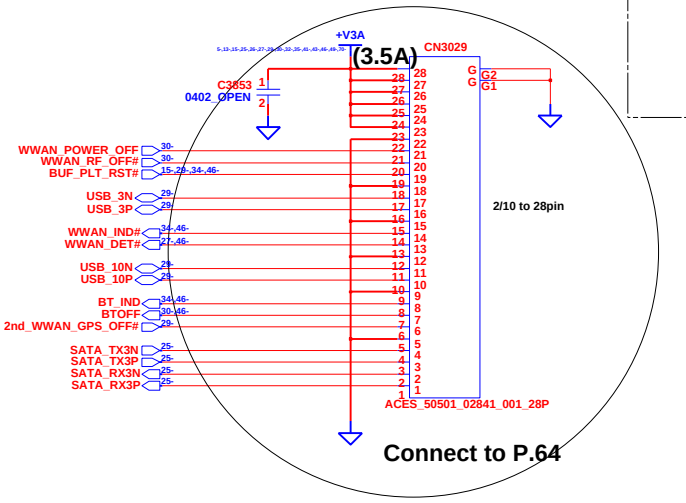
INVENTEC

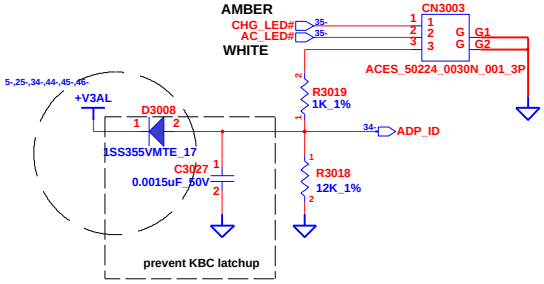
TITLE	ROMEO20 Connecter-1		
SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
SHEET 44	OF 70		

BATTERY Board CN on MB



WWAN & mSATA & BT CONN on MB





CHANGE by	Drawer_Name	28-Mar-2010		

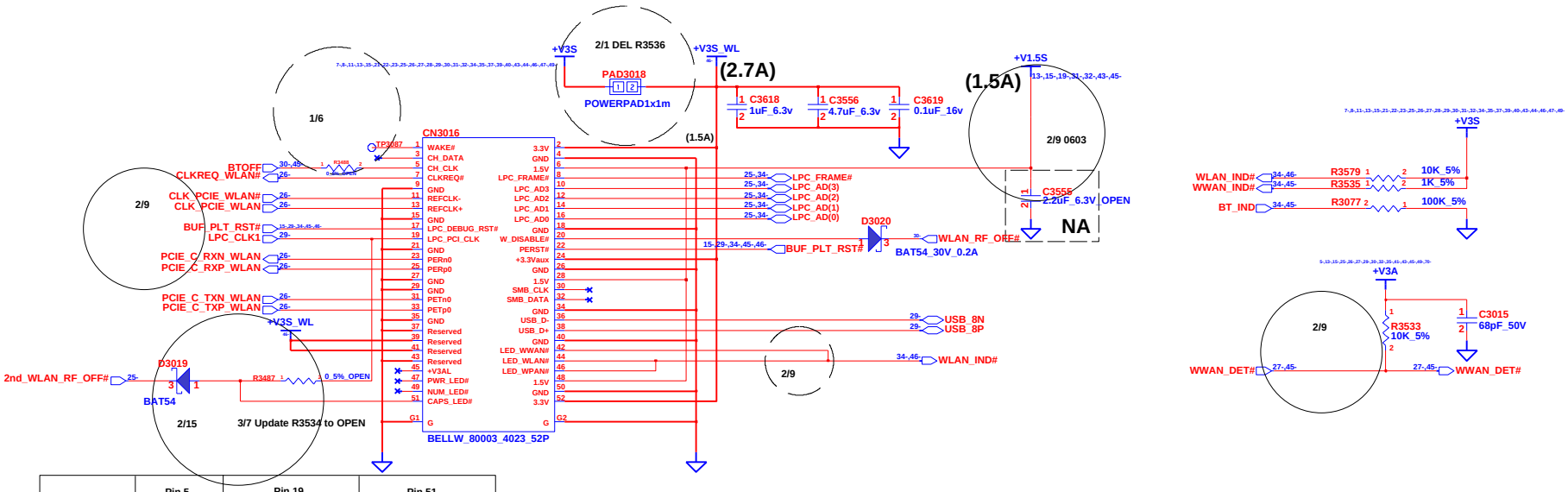
INVENTEC

TITLE: ROMEO20
Connecter-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

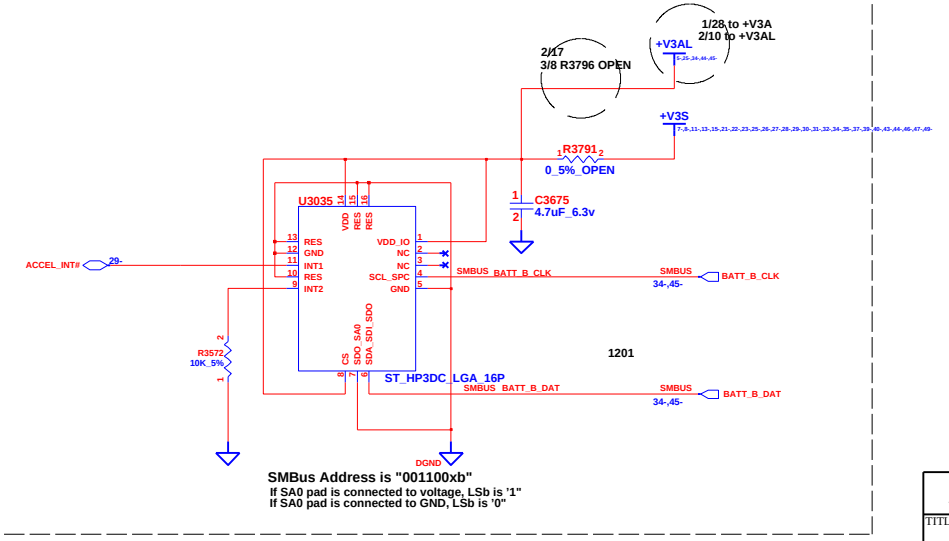
SHEET 45 OF 70

WLAN CONN (MINICARD)



	Pin 5	Pin 19	Pin 51
Atheros			V (Reserved)
Broadcom	V (Reserved)		
Ralink	V (Reserved)		
Realtek	V (Reserved)		
Intel (Rainbow peak)		V (ES2 sample / WW27)	V (QS sample/WW42)

HARDDRIVE PROTECTION



INVENTEC

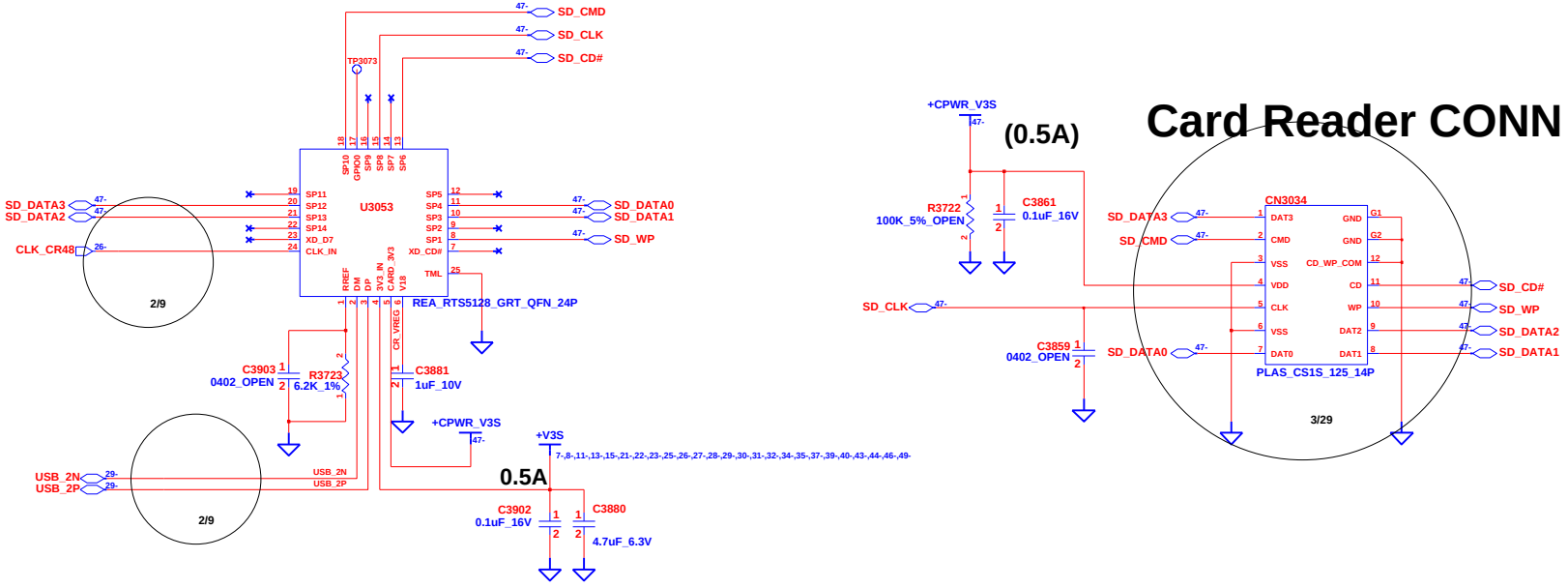
TITLE: ROMEO20
WLAN & HDD_Lock

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

CHANGE by: Drawer_Name | 28-Mar-2010

SHEET 46 OF 70

Card Reader



Card Reader CONN

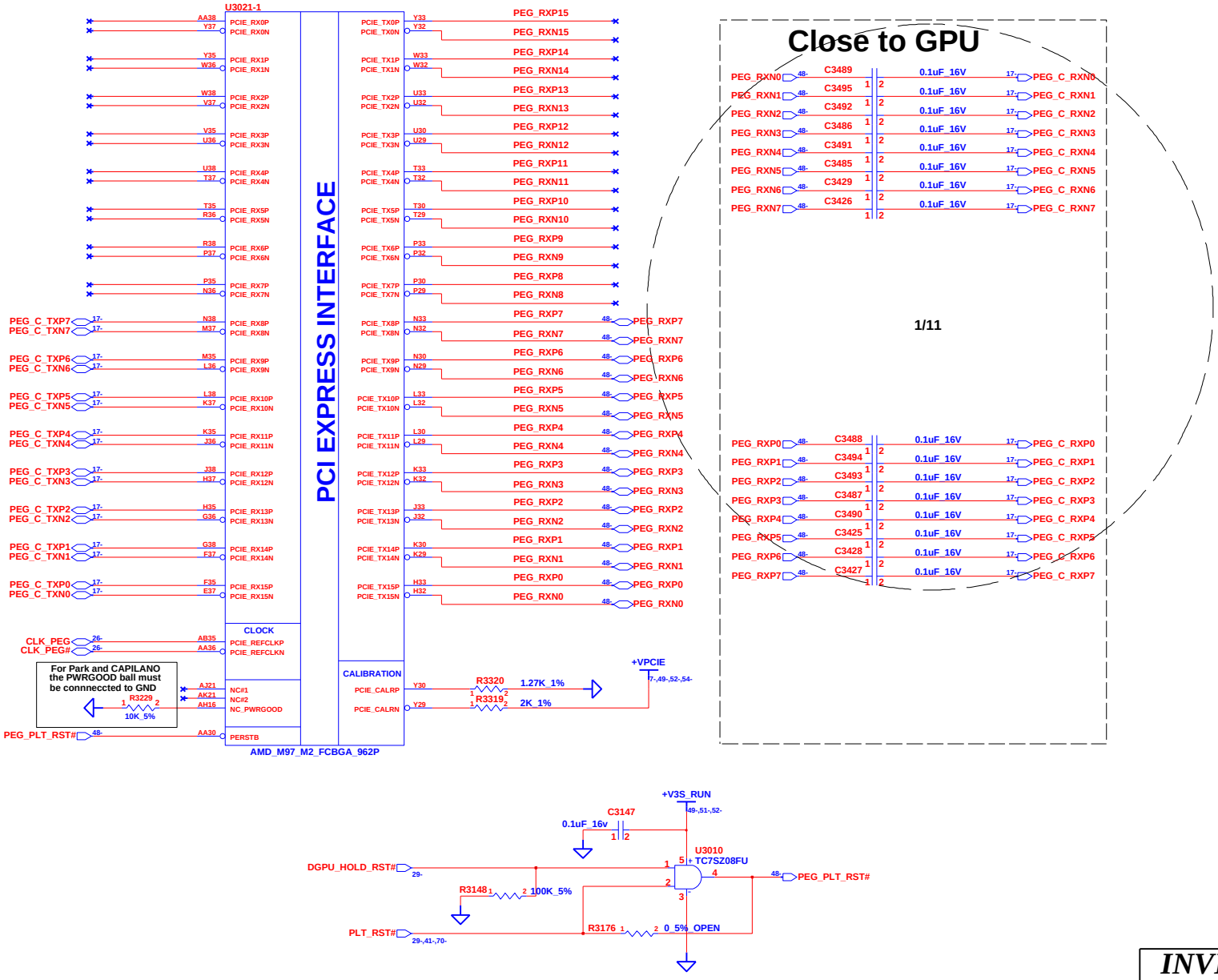
CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

TITLE: *ROMEO20*
CARD READER

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 47 OF 70



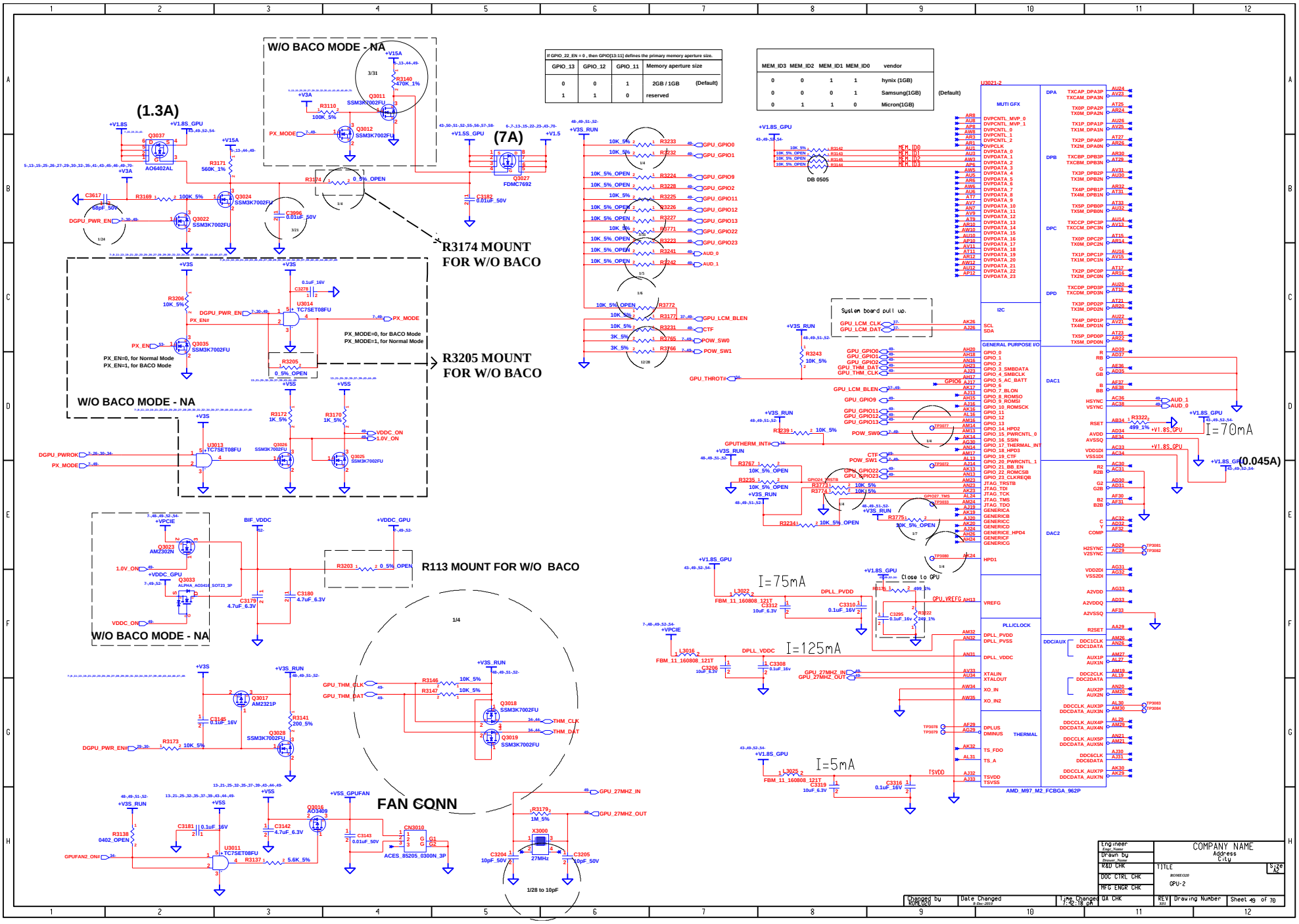
CHANGE by	Drawer_Name	17-May-2010	

INVENTEC

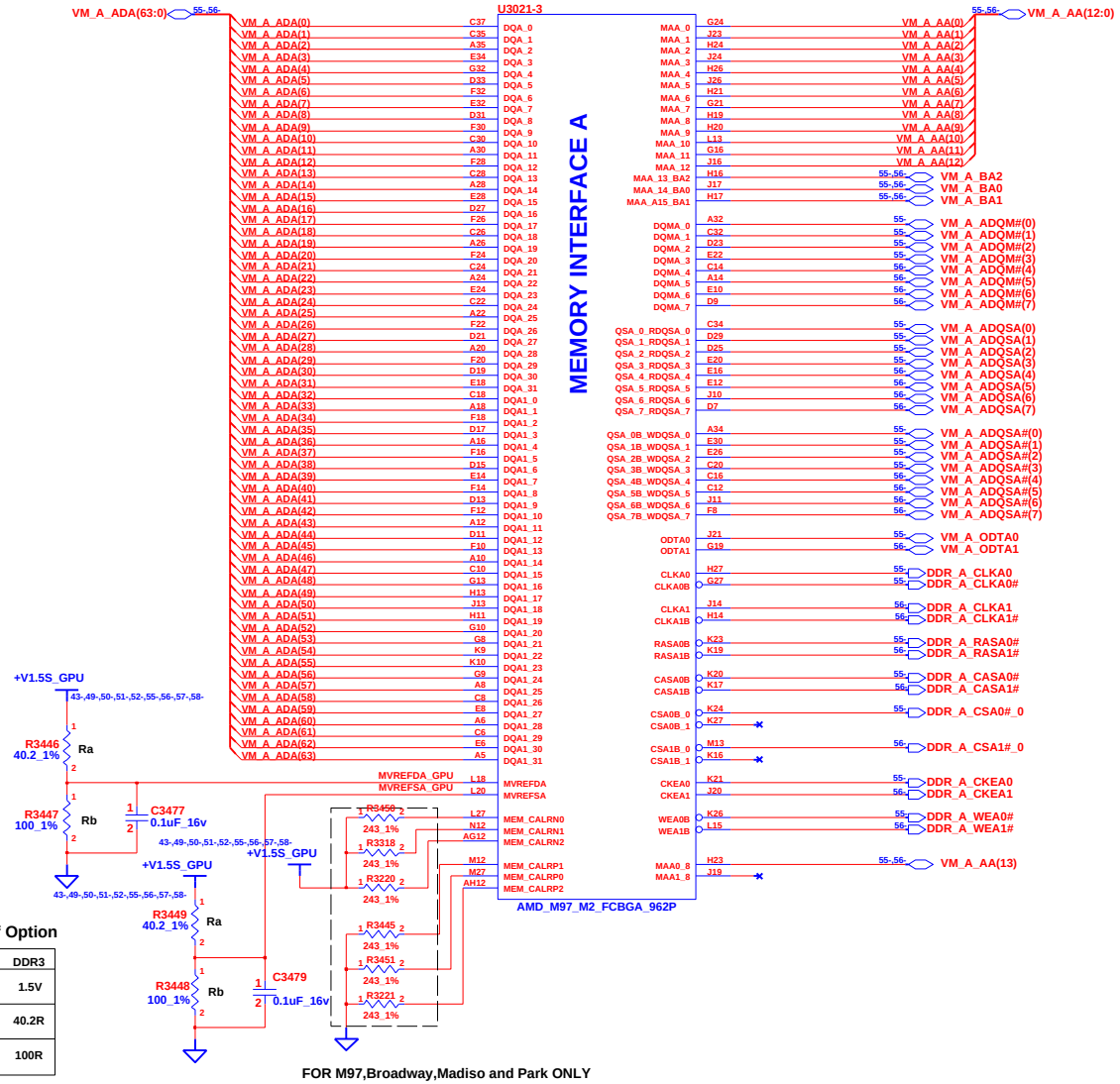
TITLE: ROMEO20
GPU-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 48 OF 70


W/O BACO MODE - NA
(1.3A)
(7A)
R3174 MOUNT FOR W/O BACO
R3205 MOUNT FOR W/O BACO
W/O BACO MODE - NA
R113 MOUNT FOR W/O BACO
W/O BACO MODE - NA
FAN CONN
If GPIO_22_EN = 0 , then GPIO[13:11] defines the primary memory aperture size.
GPIO_13 GPIO_12 GPIO_11 Memory aperture size
0 0 1 2GB / 1GB (Default)
1 1 0 reserved
MEM_ID3 MEM_ID2 MEM_ID1 MEM_ID0 vendor
0 0 1 1 hynix (1GB)
0 0 0 1 Samsung(1GB) (Default)
0 1 1 0 Micron(1GB)
System board pull up.
I=75mA
I=125mA
I=5mA
I=70mA
(0.045A)
Close to GPU
1/28 to 10pF
COMPANY NAME
Address
City
TITLE
GPU-2
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
Changed by
Date Changed
Time Changed
QA CHK
REV
Drawing Number
Sheet 43 of 70

Channel A



DDR3/GDDR3Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

FOR M97,Broadway,Madiso and Park ONLY

CHANGE by	Drawer_Name	28-Mar-2010

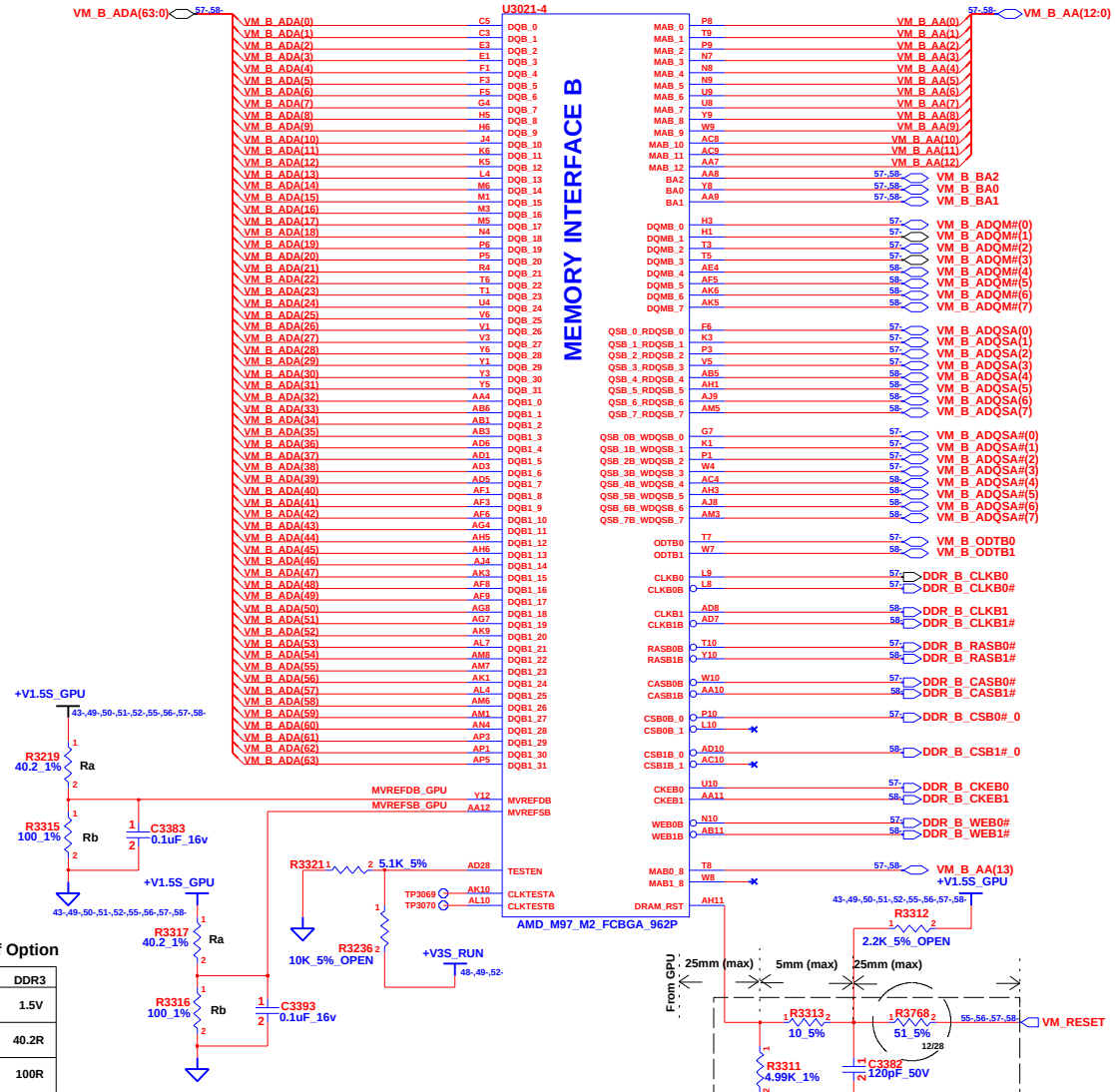
INVENTEC

TITLE: ROMEO20
GPU-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 50 OF 70

Channel B



DDR3/GDDR3Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Place all these components vry close to GPU (Within 25mm)
and keep all component close to each other (within 5mm) except Rser2
** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5
These Capacitors and Resistor values are an example only.
The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory , DRAM Load and board to pass Reset Signal Spec.

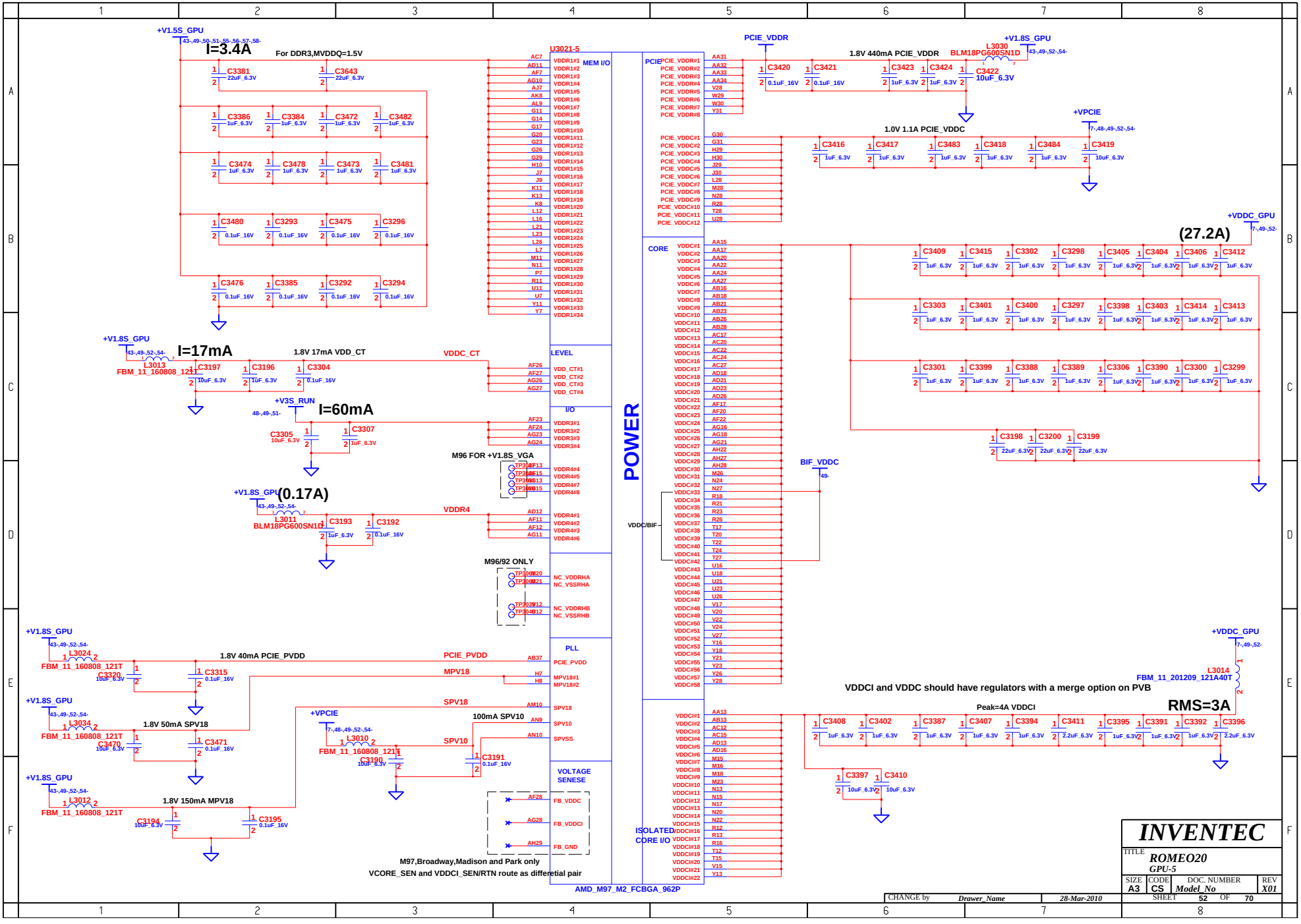
INVENTEC

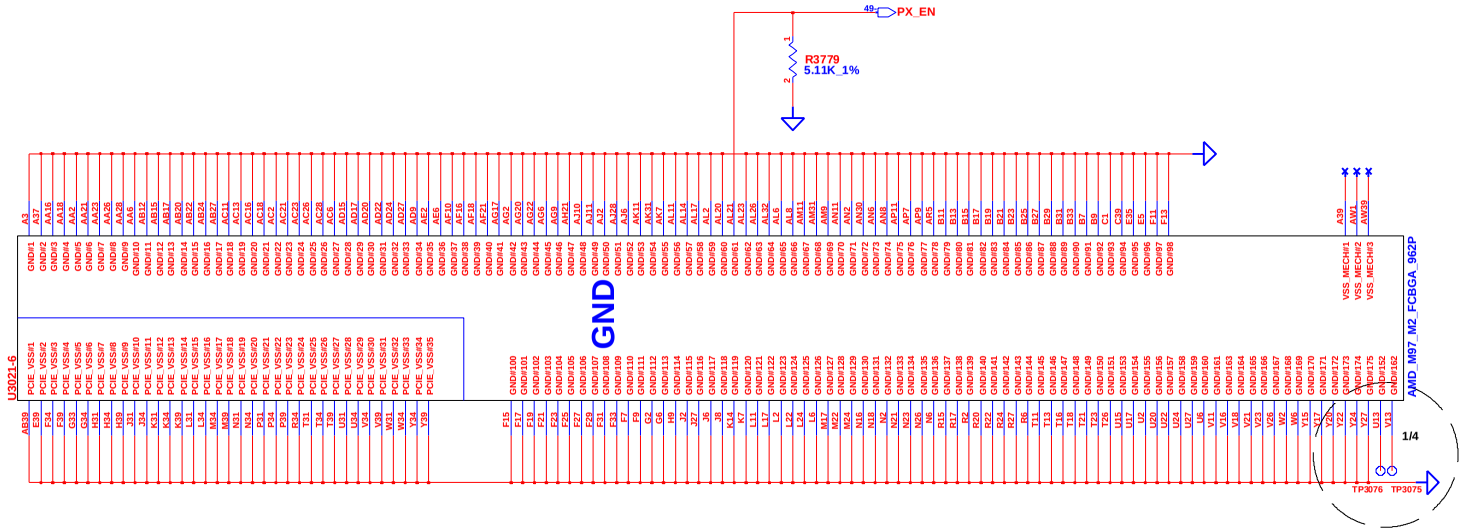
TITLE: ROMEO20
GPU-4

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

CHANGE by: Drawer_Name | 28-Mar-2010

SHEET 51 OF 70


+V1.5S_GPU
I=3.4A
For DDR3,MVDDQ=1.5V
U3021-5
MEM I/O
POWER
PCIE
CORE
LEVEL
I/O
VOLTAGE SENESE
PLL
VDDC/BIF
ISOLATED CORE I/O
AMD_M97_M2_FCBGA_962P
PCIE_VDDR
1.8V 440mA PCIE_VDDR
+V1.8S_GPU
+VPCIE
1.0V 1.1A PCIE_VDDC
+VDDC_GPU
(27.2A)
+V1.8S_GPU
I=17mA
1.8V 17mA VDD_CT
VDDC_CT
+V3S_RUN
I=60mA
M96 FOR +V1.8S_VGA
+V1.8S_GPU
(0.17A)
VDDR4
M96/92 ONLY
BIF_VDDC
+V1.8S_GPU
1.8V 40mA PCIE_PVDD
PCIE_PVDD
MPV18
+V1.8S_GPU
1.8V 50mA SPV18
SPV18
+VPCIE
100mA SPV10
SPV10
SPVSS
+V1.8S_GPU
1.8V 150mA MPV18
M97,Broadway,Madison and Park only
VCORE_SEN and VDDCI_SEN/RTN route as differetial pair
+VDDC_GPU
VDDCI and VDDC should have regulators with a merge option on PVB
Peak=4A VDDCI
RMS=3A
INVENTEC
ROMEO20
GPU-5
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
CHANGE by Drawer_Name
28-Mar-2010
SHEET 52 OF 70



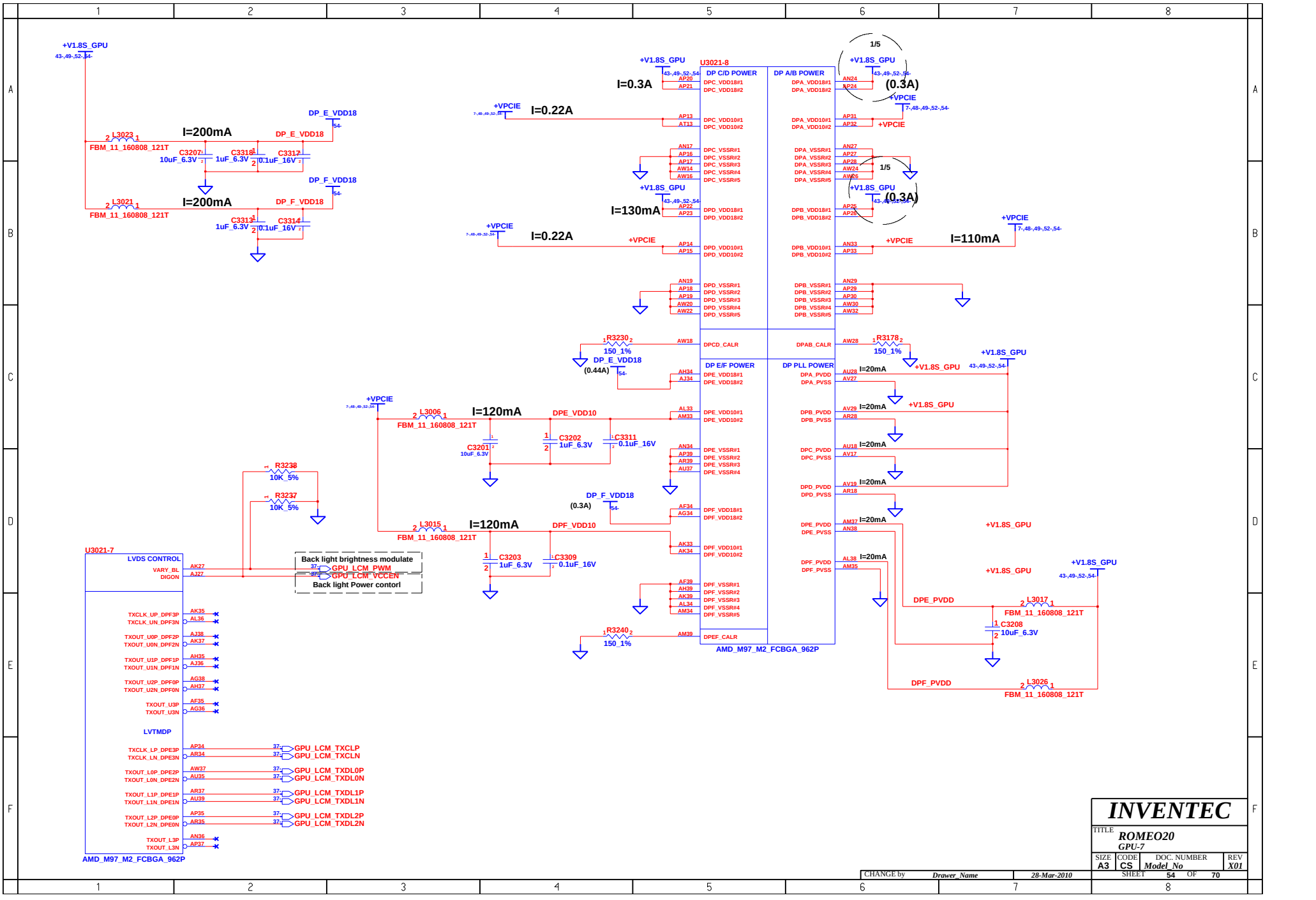
CHANGE by	Drawer_Name	28-Mar-2010	

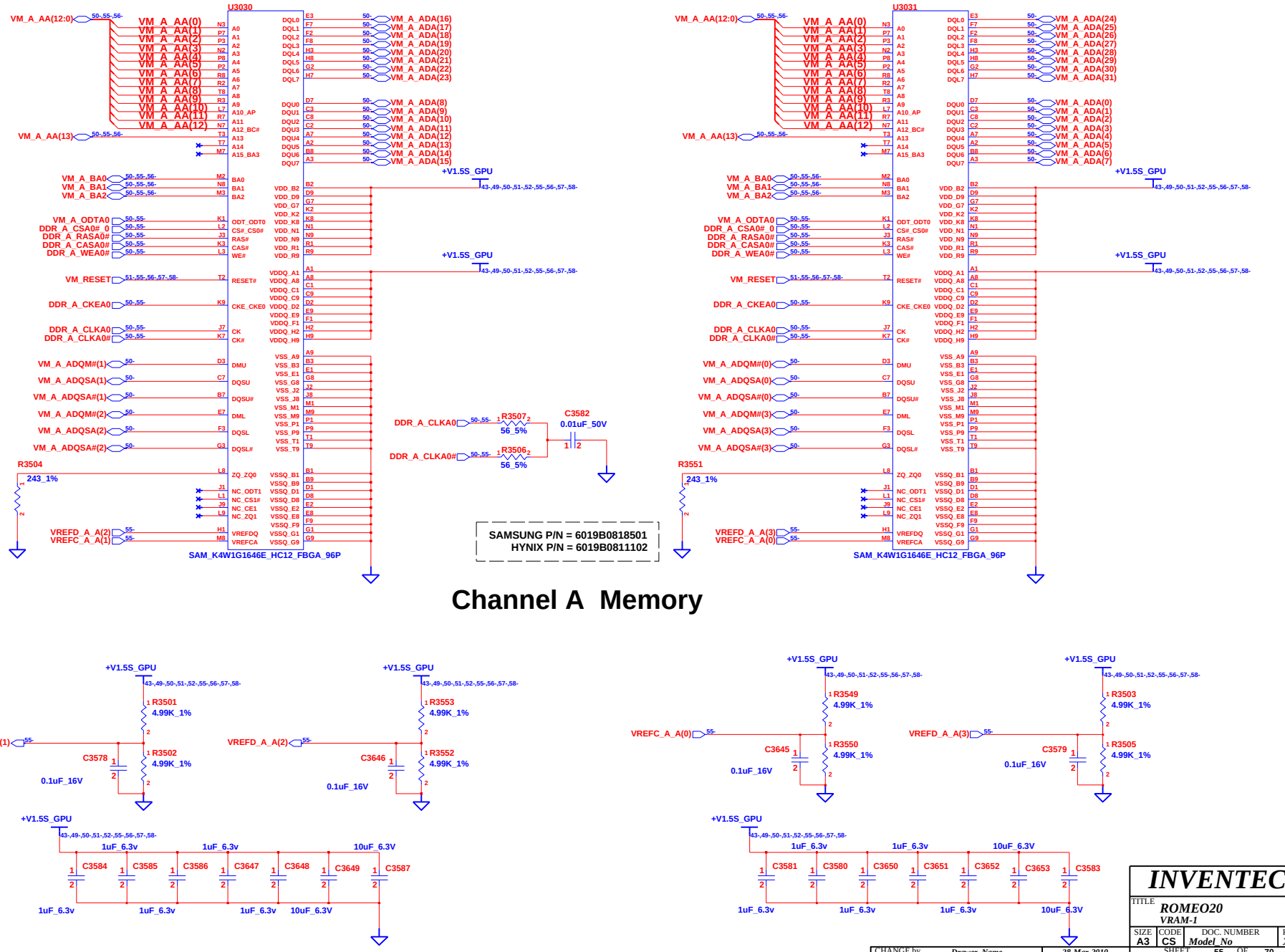
INVENTEC

TITLE: *ROMEO20*
GPU-6

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

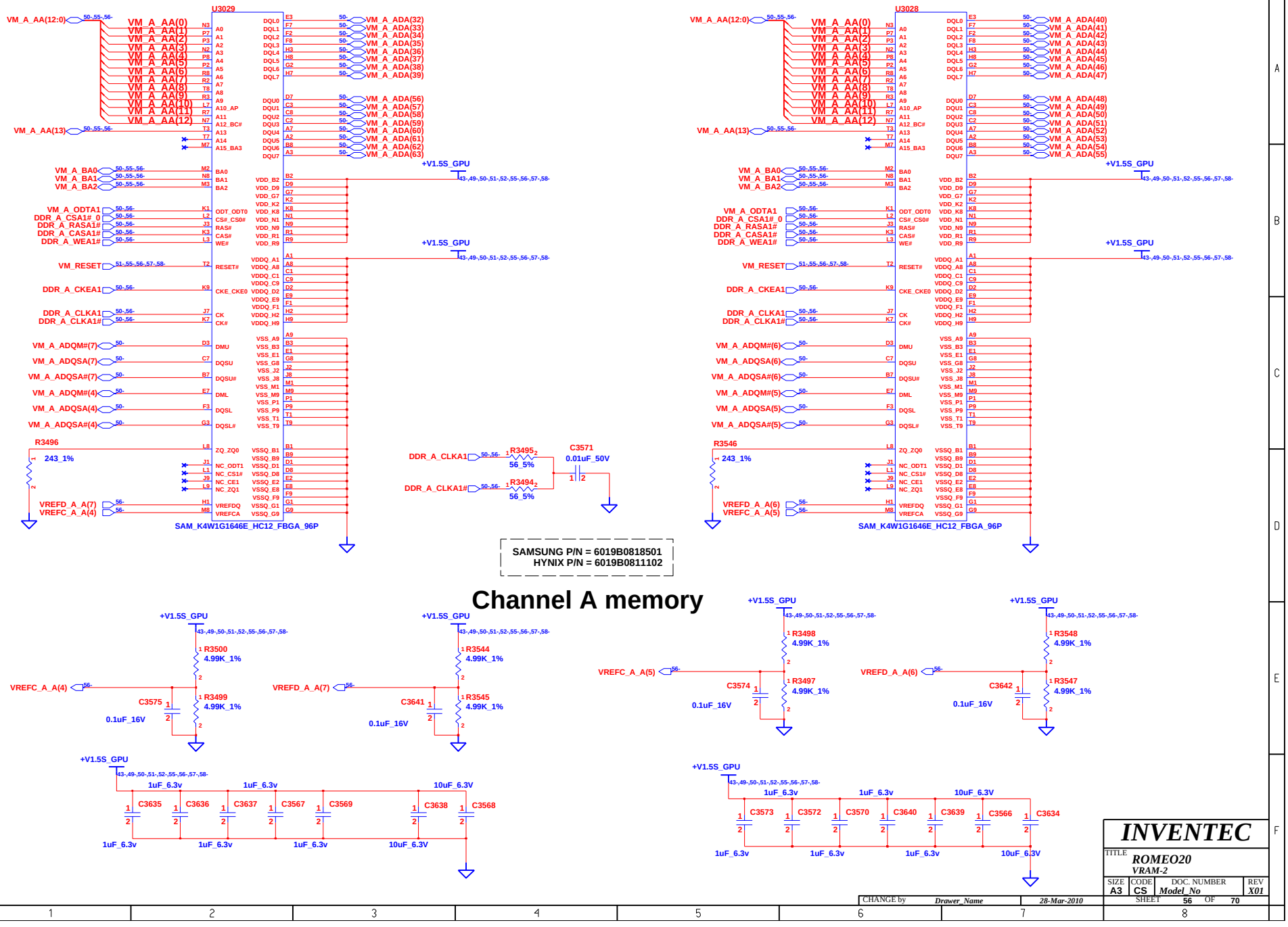
SHEET 53 OF 70

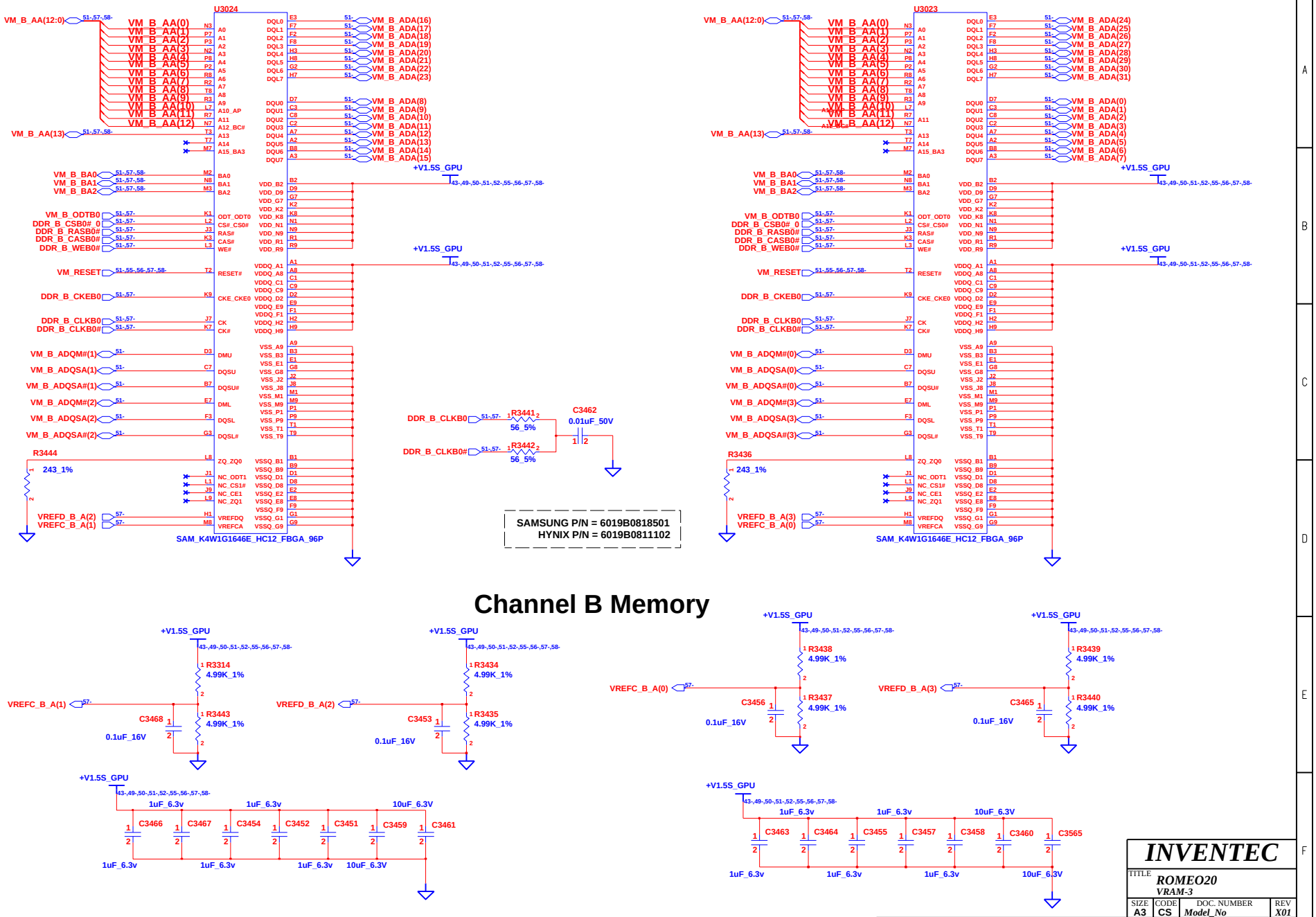

+V1.8S_GPU
43-,49-,52-,54-
DP_E_VDD18
54-
I=200mA
L3023
FBM_11_160808_121T
C3207
10uF_6.3V
C3316
1uF_6.3V
C3317
0.1uF_16V
DP_F_VDD18
L3021
C3313
C3314
U3021-8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
I=0.3A
I=0.22A
I=130mA
I=110mA
+VPCIE
7-,48-,49-,52-,54-
1/5
(0.3A)
DPC_VDD18#1
DPC_VDD18#2
DPC_VDD10#1
DPC_VDD10#2
DPC_VSSR#1
DPC_VSSR#2
DPC_VSSR#3
DPC_VSSR#4
DPC_VSSR#5
DPD_VDD18#1
DPD_VDD18#2
DPD_VDD10#1
DPD_VDD10#2
DPD_VSSR#1
DPD_VSSR#2
DPD_VSSR#3
DPD_VSSR#4
DPD_VSSR#5
DPA_VDD18#1
DPA_VDD18#2
DPA_VDD10#1
DPA_VDD10#2
DPA_VSSR#1
DPA_VSSR#2
DPA_VSSR#3
DPA_VSSR#4
DPA_VSSR#5
DPB_VDD18#1
DPB_VDD18#2
DPB_VDD10#1
DPB_VDD10#2
DPB_VSSR#1
DPB_VSSR#2
DPB_VSSR#3
DPB_VSSR#4
DPB_VSSR#5
DPCD_CALR
DPAB_CALR
DPEF_CALR
R3230
150_1%
R3178
DP_E_VDD18
(0.44A)
DPE_VDD18#1
DPE_VDD18#2
DPE_VDD10#1
DPE_VDD10#2
DPE_VSSR#1
DPE_VSSR#2
DPE_VSSR#3
DPE_VSSR#4
DPF_VDD18#1
DPF_VDD18#2
DPF_VDD10#1
DPF_VDD10#2
DPF_VSSR#1
DPF_VSSR#2
DPF_VSSR#3
DPF_VSSR#4
DPF_VSSR#5
DPA_PVDD
DPA_PVSS
DPB_PVDD
DPB_PVSS
DPC_PVDD
DPC_PVSS
DPD_PVDD
DPD_PVSS
DPE_PVDD
DPE_PVSS
DPF_PVDD
DPF_PVSS
I=20mA
DPE_VDD10
DPF_VDD10
L3006
L3015
FBM_11_160808_121T
C3201
C3202
C3311
C3203
C3309
R3238
10K_5%
R3237
U3021-7
LVDS CONTROL
VARY_BL
DIGON
Back light brightness modulate
GPU_LCM_PWM
GPU_LCM_VCCEN
Back light Power contorl
LVTMDP
TXCLK_UP_DPF3P
TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P
TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P
TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P
TXOUT_U2N_DPF0N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP_DPE3P
TXCLK_LN_DPE3N
TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N
TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N
TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N
TXOUT_L3P
TXOUT_L3N
GPU_LCM_TXCLP
GPU_LCM_TXCLN
GPU_LCM_TXDL0P
GPU_LCM_TXDL0N
GPU_LCM_TXDL1P
GPU_LCM_TXDL1N
GPU_LCM_TXDL2P
GPU_LCM_TXDL2N
AMD_M97_M2_FCBGA_962P
DPE_PVDD
DPF_PVDD
L3017
L3026
C3208
10uF_6.3V
INVENTEC
TITLE
ROMEO20
GPU-7
SIZE
A3
CODE
CS
DOC. NUMBER
Model_No
REV
X01
CHANGE by
Drawer_Name
28-Mar-2010
SHEET
54
OF
70

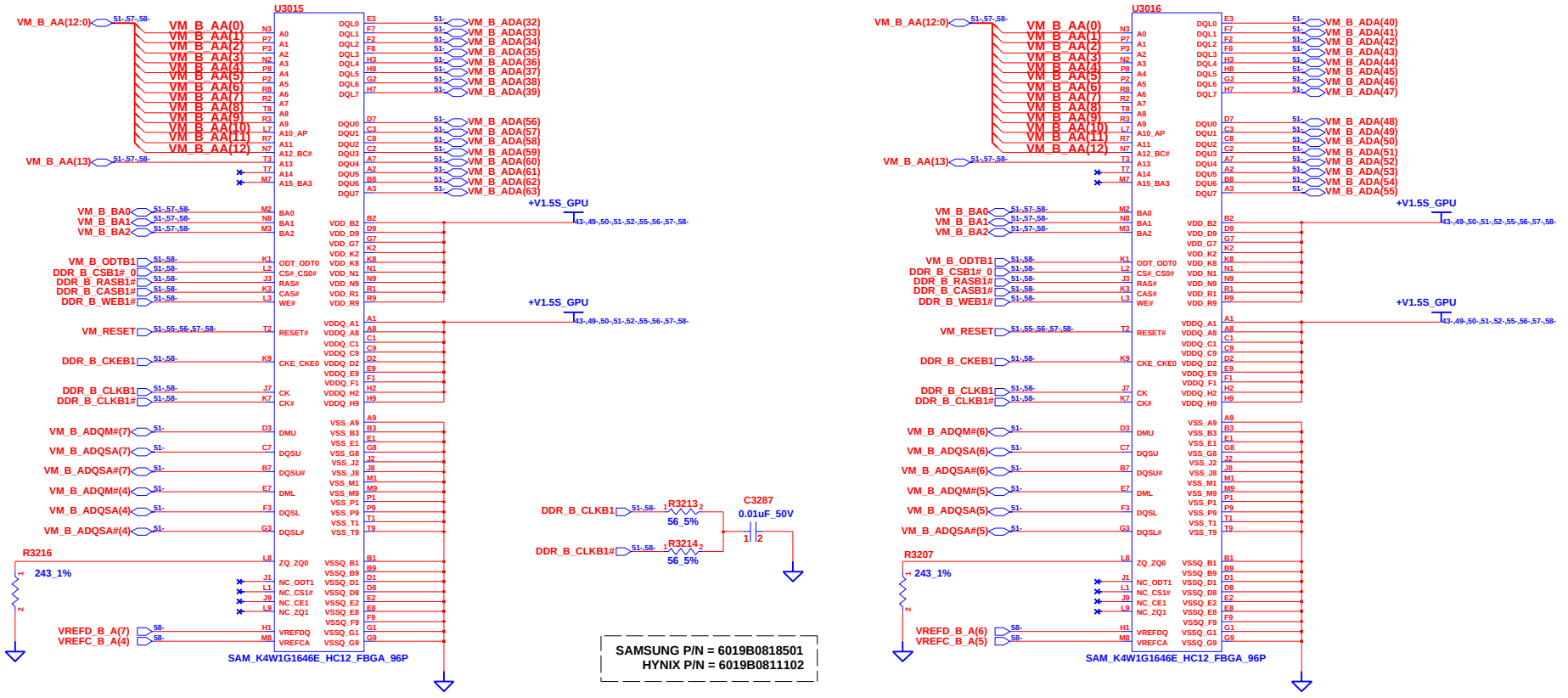


Channel A Memory

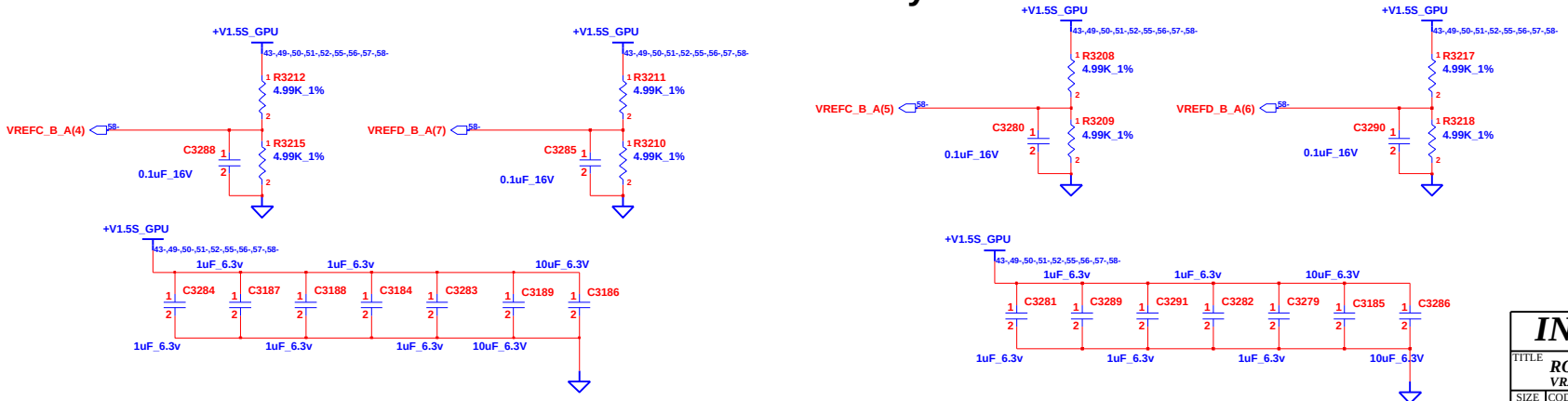
INVENTEC			
TITLE: ROMEO20 VRAM-1			
SIZE: A3	CODE: CS	DOC. NUMBER: Model_No	REV: X01
CHANGE by: Drawer_Name	28-Mar-2010	SHEET 55 OF 70	


U3029
U3028
VM_A_AA(12:0)
VM_A_AA(13)
VM_A_BA0
VM_A_BA1
VM_A_BA2
VM_A_ODTA1
DDR_A_CSA1#_0
DDR_A_RASA1#
DDR_A_CASA1#
DDR_A_WEA1#
VM_RESET
DDR_A_CKEA1
DDR_A_CLKA1
DDR_A_CLKA1#
VM_A_ADQM#(7)
VM_A_ADQSA(7)
VM_A_ADQSA#(7)
VM_A_ADQM#(4)
VM_A_ADQSA(4)
VM_A_ADQSA#(4)
VM_A_ADQM#(6)
VM_A_ADQSA(6)
VM_A_ADQSA#(6)
VM_A_ADQM#(5)
VM_A_ADQSA(5)
VM_A_ADQSA#(5)
R3496
243_1%
R3546
VREFD_A_A(7)
VREFC_A_A(4)
VREFD_A_A(6)
VREFC_A_A(5)
R3495
56_5%
R3494
56_5%
C3571
0.01uF_50V
+V1.5S_GPU
SAM_K4W1G1646E_HC12_FBGA_96P
SAMSUNG P/N = 6019B0818501
HYNIX P/N = 6019B0811102
Channel A memory
R3500
4.99K_1%
R3499
4.99K_1%
R3544
4.99K_1%
R3545
4.99K_1%
R3498
4.99K_1%
R3497
4.99K_1%
R3548
4.99K_1%
R3547
4.99K_1%
C3575
C3574
C3641
C3642
0.1uF_16V
1uF_6.3v
10uF_6.3V
C3635
C3636
C3637
C3567
C3569
C3638
C3568
C3573
C3572
C3570
C3640
C3639
C3566
C3634
INVENTEC
TITLE
ROMEO20
VRAM-2
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
CHANGE by Drawer_Name
28-Mar-2010
SHEET 56 OF 70


U3024
U3023
SAM_K4W1G1646E_HC12_FBGA_96P
SAMSUNG P/N = 6019B0818501
HYNIX P/N = 6019B0811102
Channel B Memory
INVENTEC
ROMEO20
VRAM-3
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 57 OF 70
CHANGE by Drawer_Name
28-Mar-2010



Channel B Memory



CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

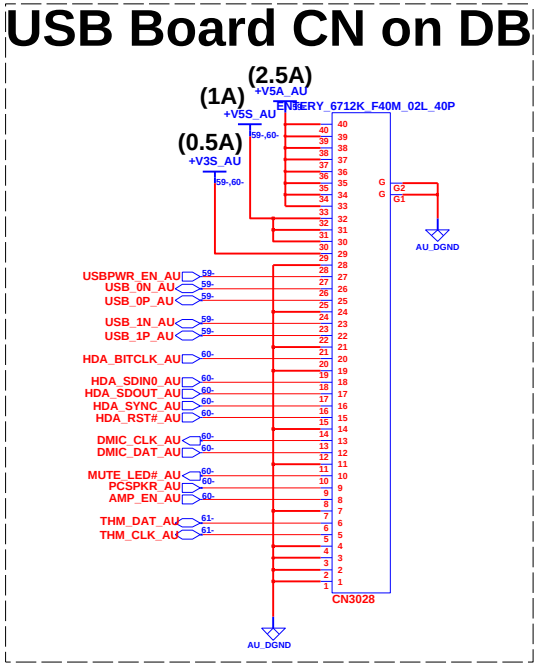
TITLE: *ROMEO20*
VRAM-4

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

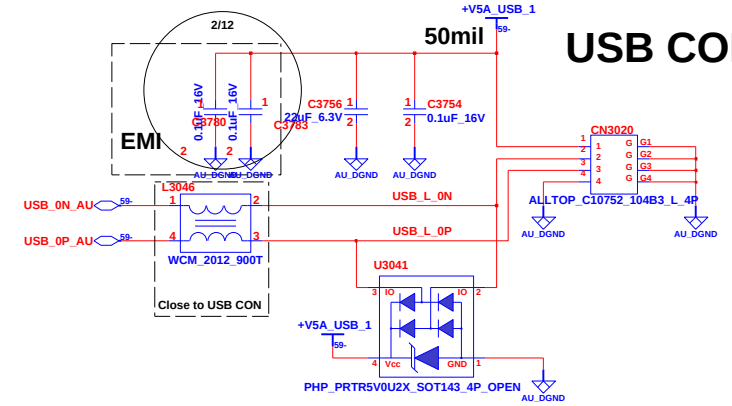
SHEET 58 OF 70

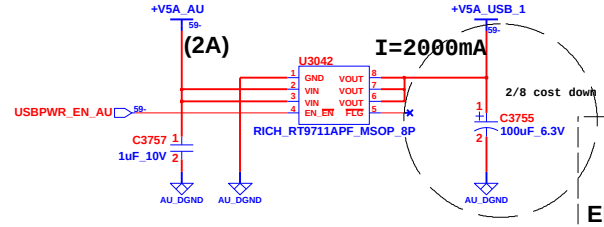
USB Board-1

USB Board CN on DB

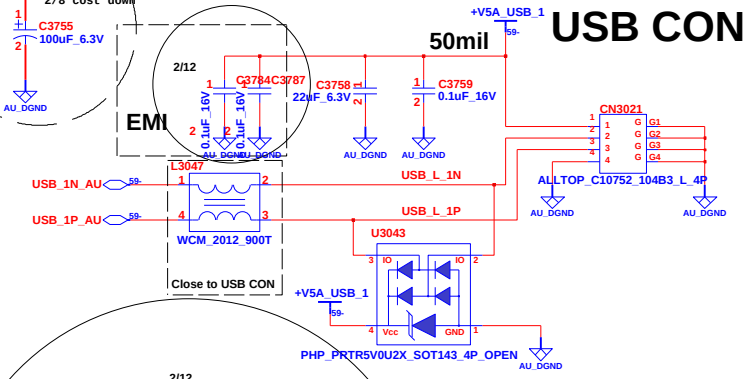


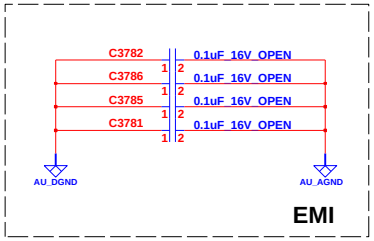
USB CONN01

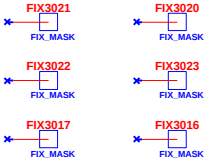


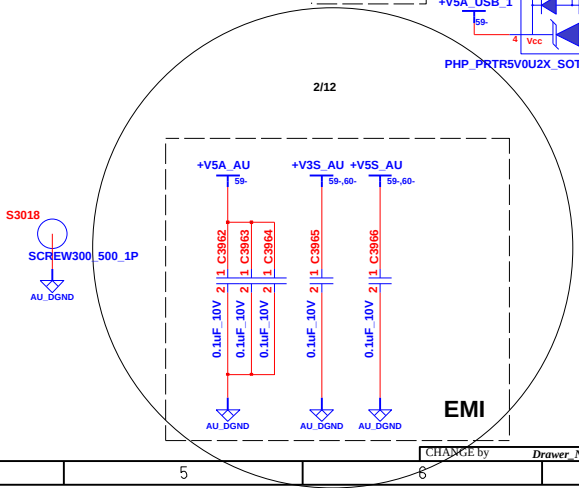


USB CONN02









CHANGE by	Drawer_Name	13-Apr-2010		

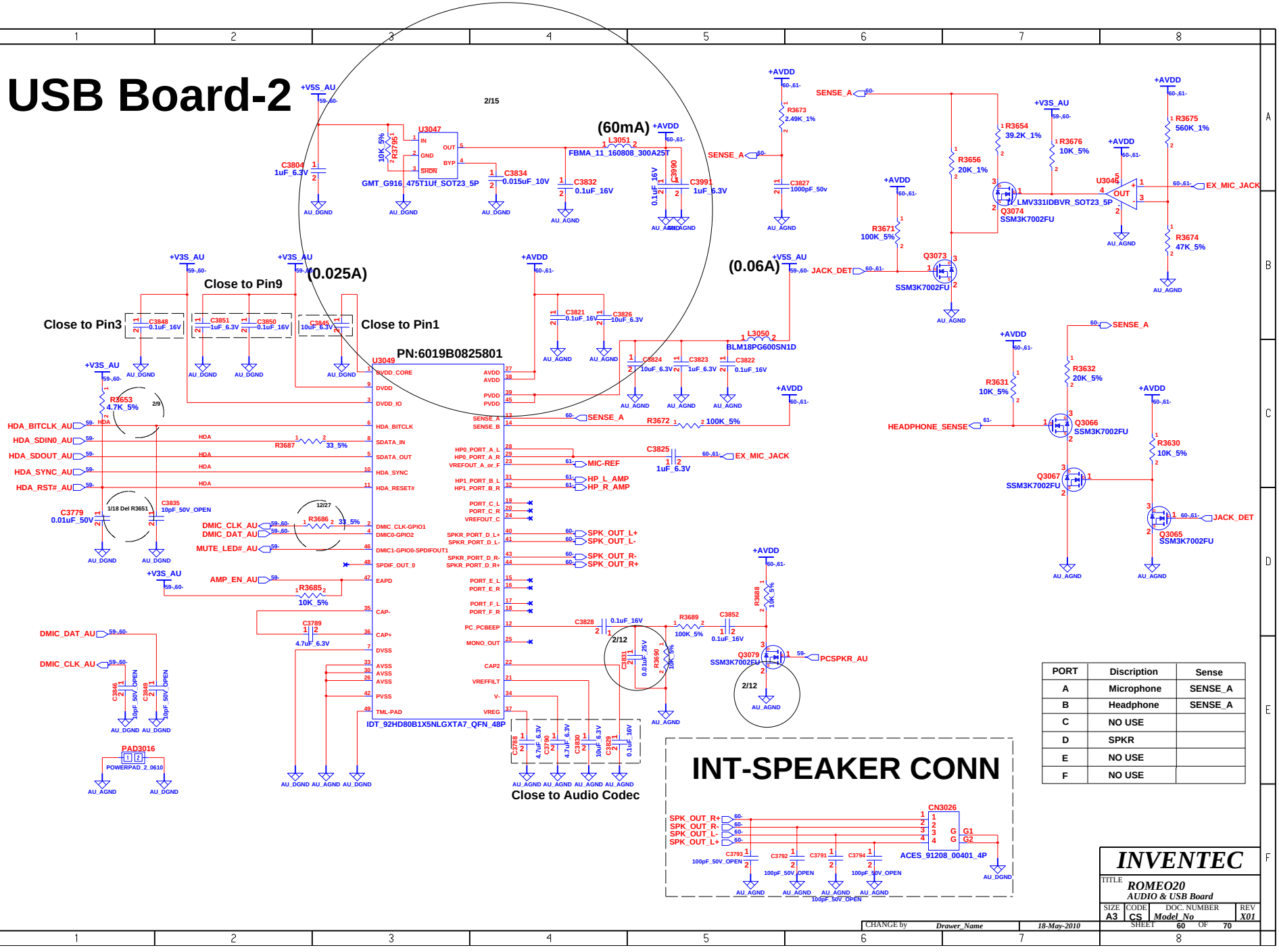
INVENTEC

TITLE: *ROMEO20*
AUDIO & USB Board

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 59 OF 70

USB Board-2



PORT	Discription	Sense
A	Microphone	SENSE_A
B	Headphone	SENSE_A
C	NO USE	
D	SPKR	
E	NO USE	
F	NO USE	

INVENTEC

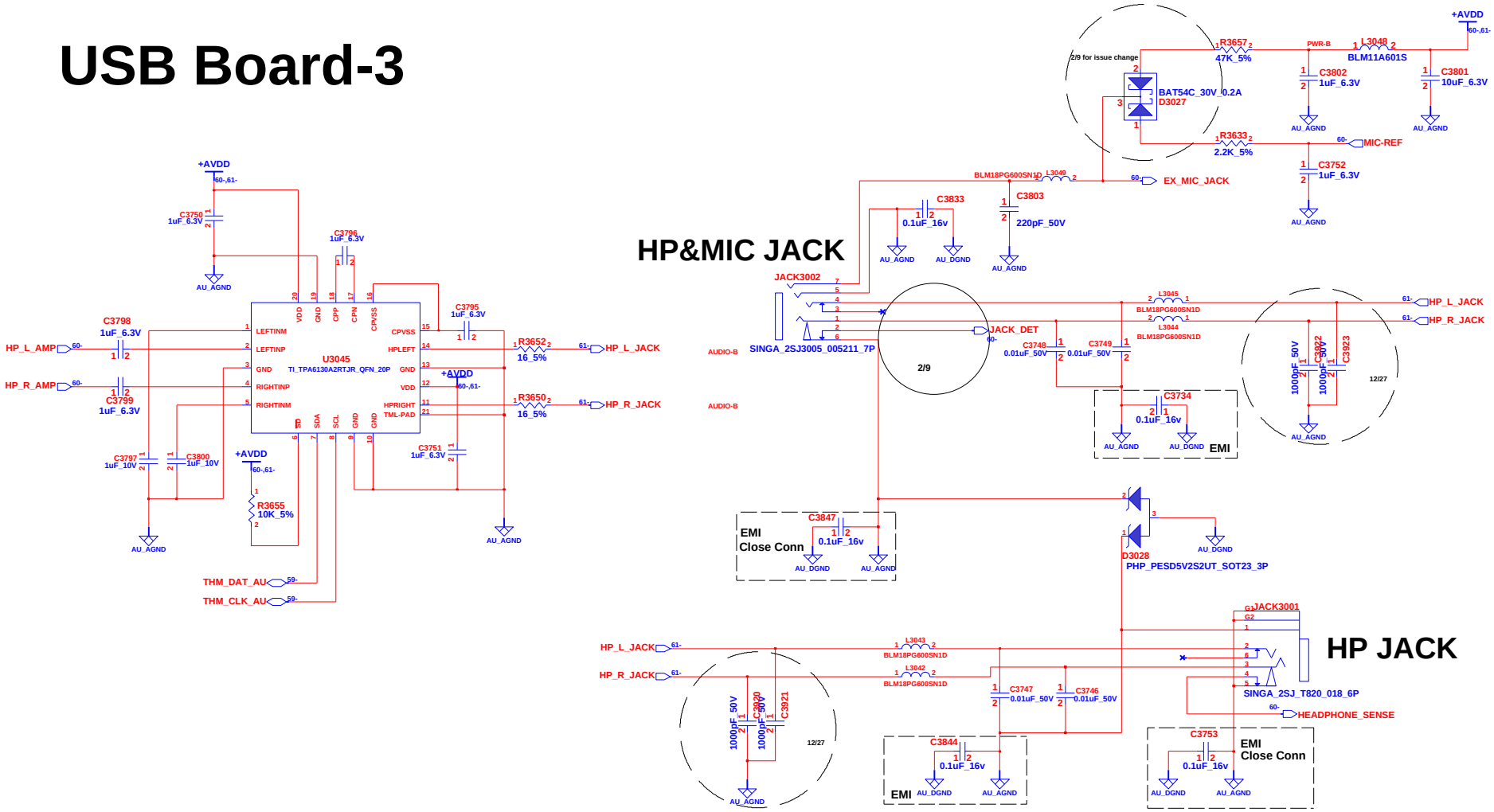
TITLE: *ROMEO20*
AUDIO & USB Board

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

CHANGE by *Drawer_Name* *18-May-2010*

SHEET 60 OF 70

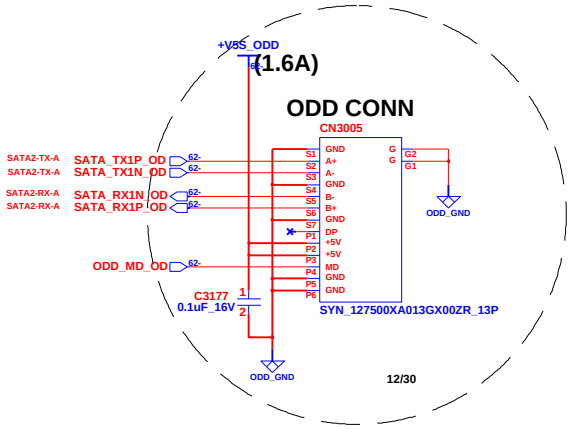
USB Board-3

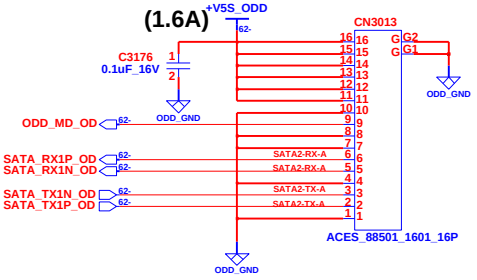


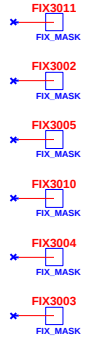
INVENTEC		
TITLE	ROMEO20 AUDIO & USB Board	
SIZE A3	CODE CS	DOC. NUMBER Model_No
REV X01		
CHANGE by Drawer_Name	28-Mar-2010	SHEET 61 OF 70

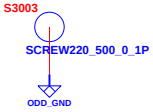
ODD Board

SATA ODD









CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

TITLE: *ROMEO20*
ODD EXT BOARD

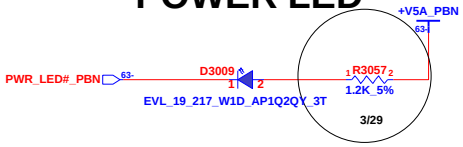
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

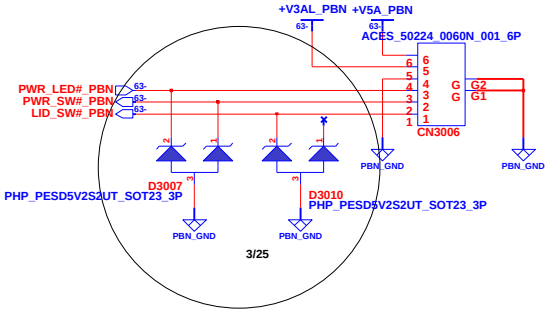
SHEET 62 OF 70

SWITCH BOARD

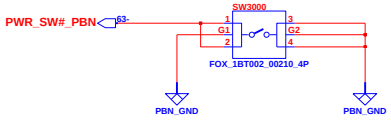
Power Button

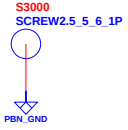
POWER LED



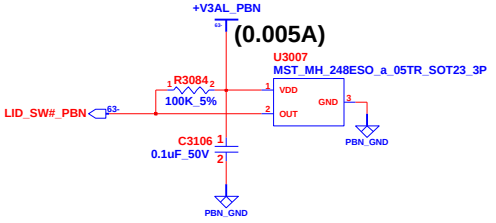


POWER BUTTON





LID SWITCH

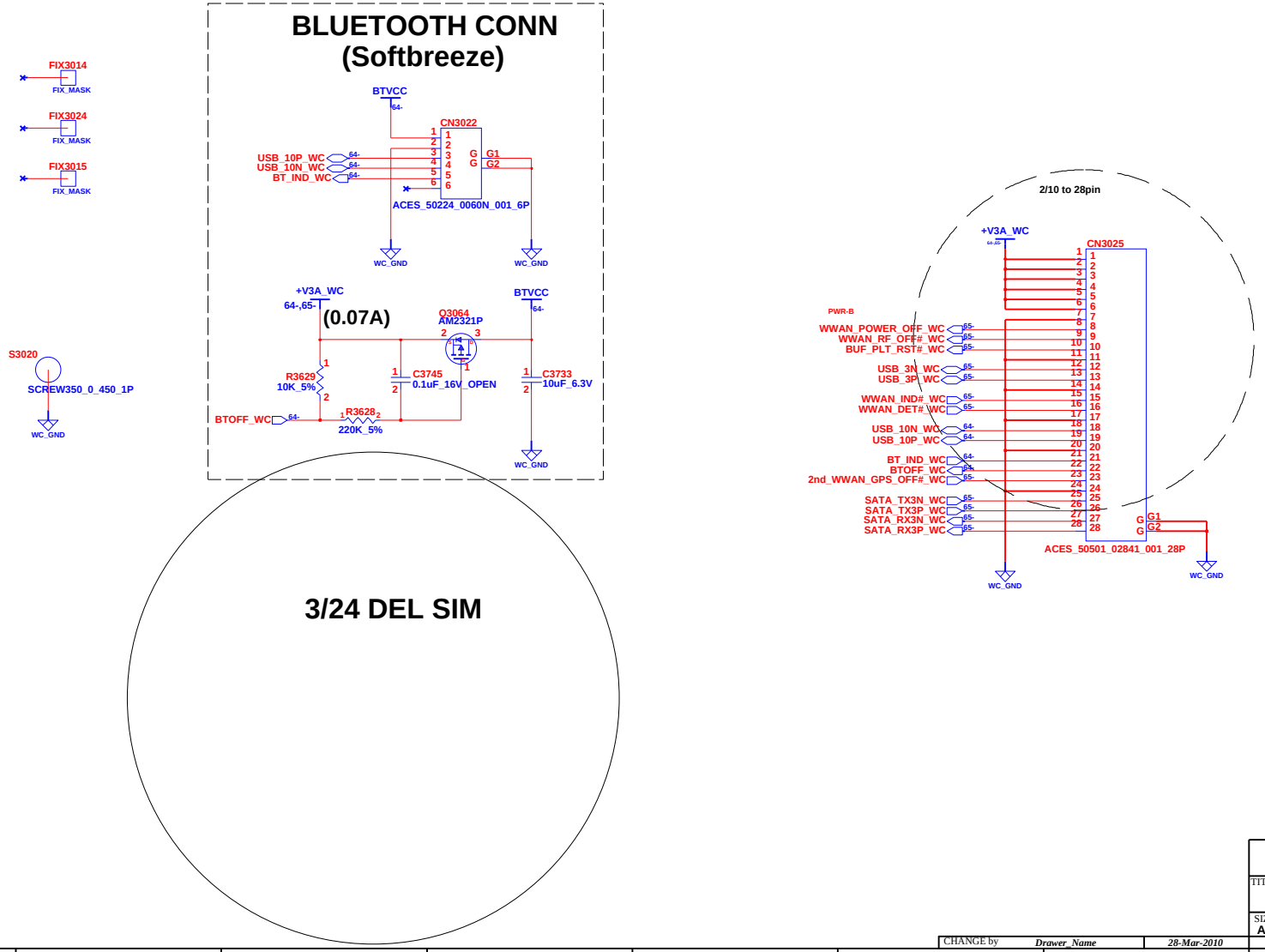


CHANGE by	*Drawer_Name*	*28-Mar-2010*	

INVENTEC

TITLE	*ROMEO20* *Power SW Board*		
SIZE A3	CODE CS	DOC. NUMBER *Model_No*	REV *X01*
		SHEET 63 OF 70	

SIM Board-1



CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

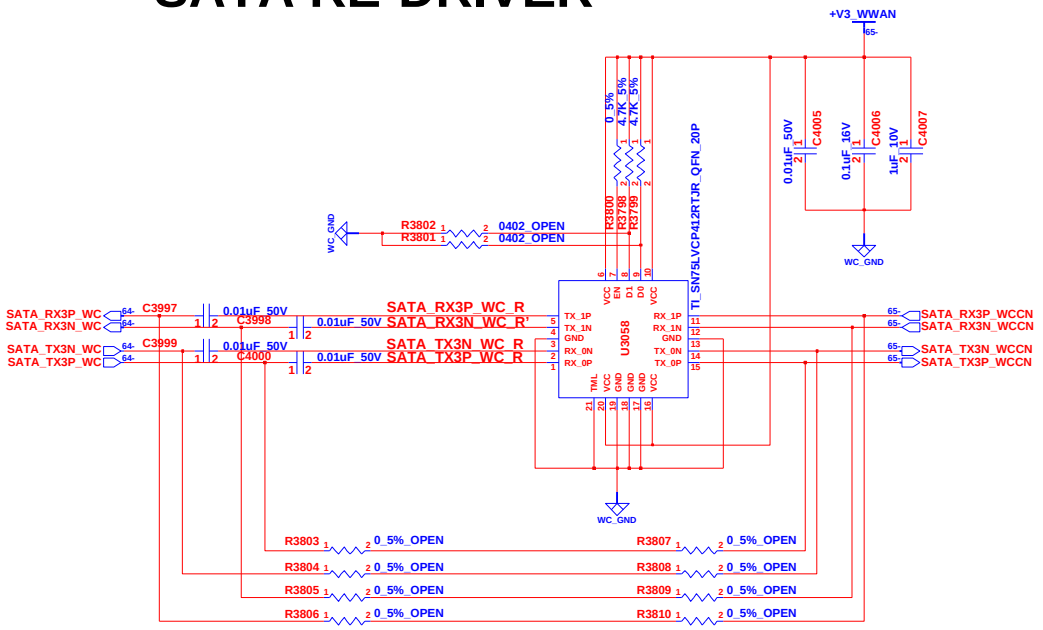
TITLE: *ROMEO20*
WIRELESS Board

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*

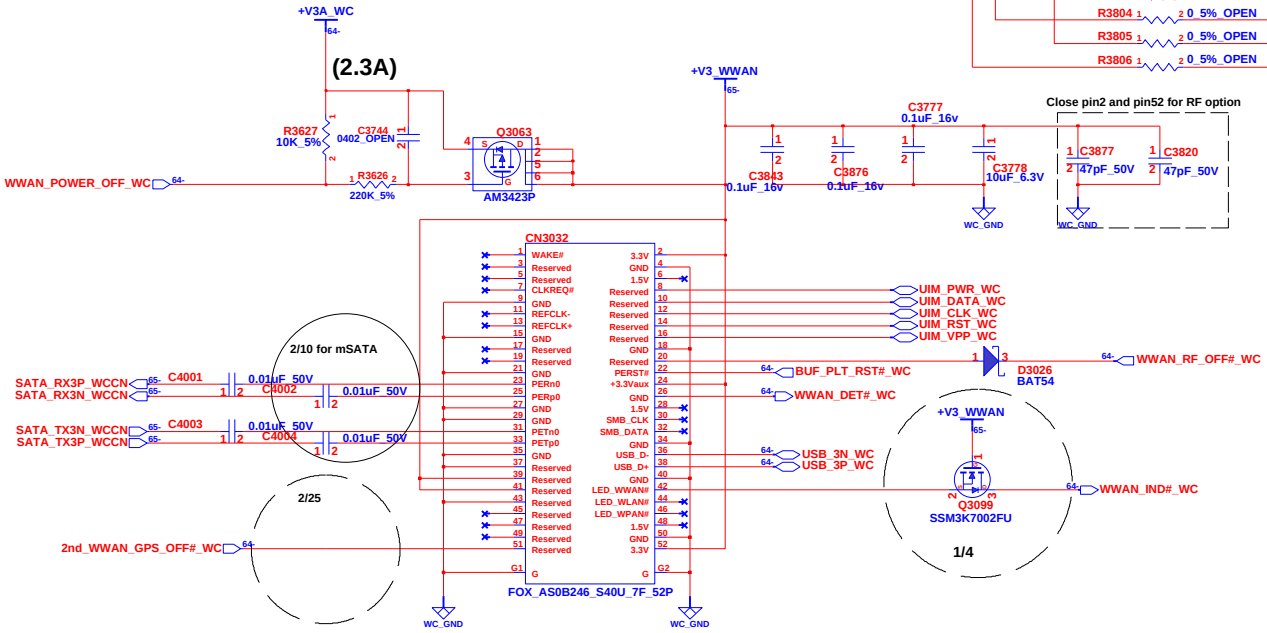
SHEET 64 OF 70

SIM Board-2

SATA RE-DRIVER



WWAN / mSATA



CHANGE by	Drawer_Name	28-Mar-2010	

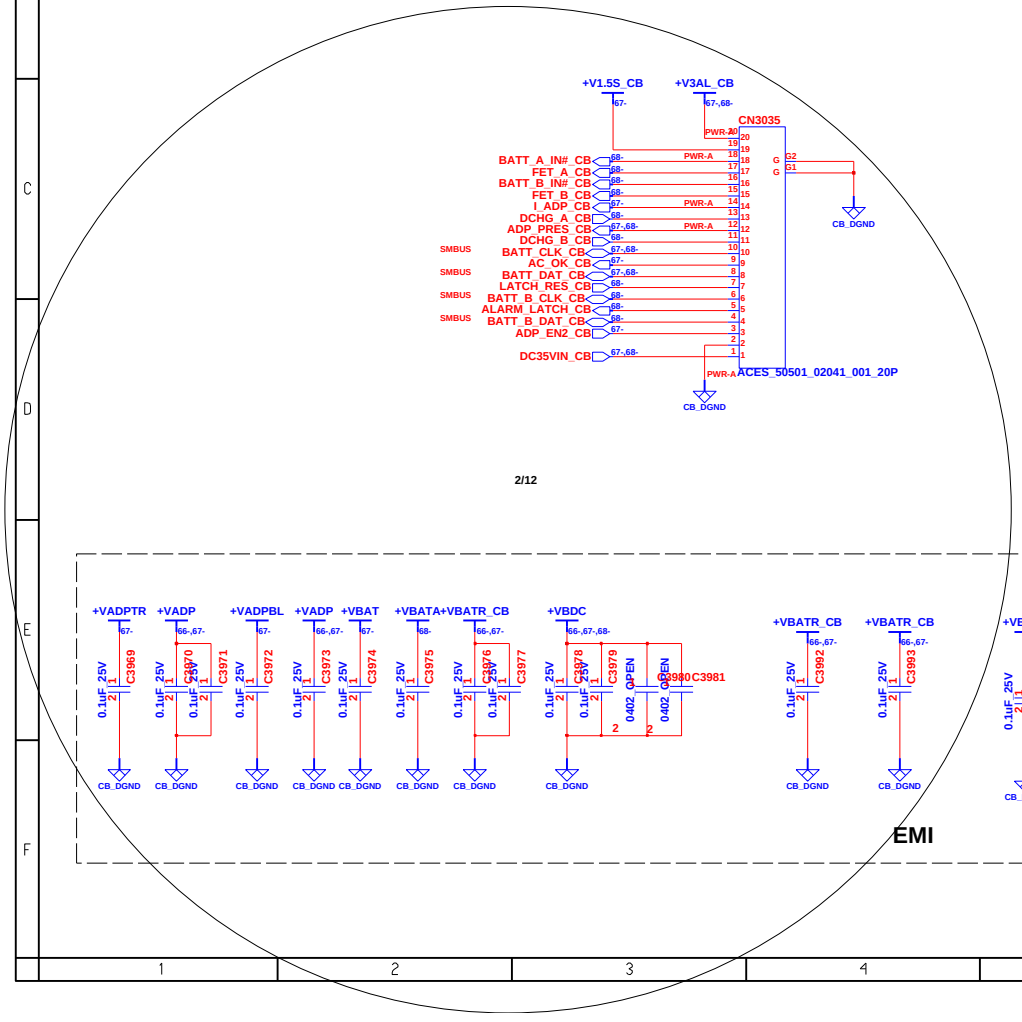
INVENTEC

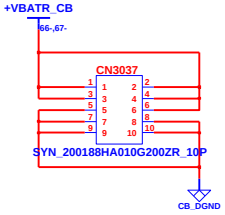
TITLE: *ROMEO20*
WIRELESS Board

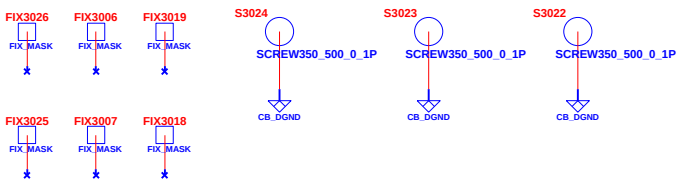
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 65 OF 70

BATTERY Board-1





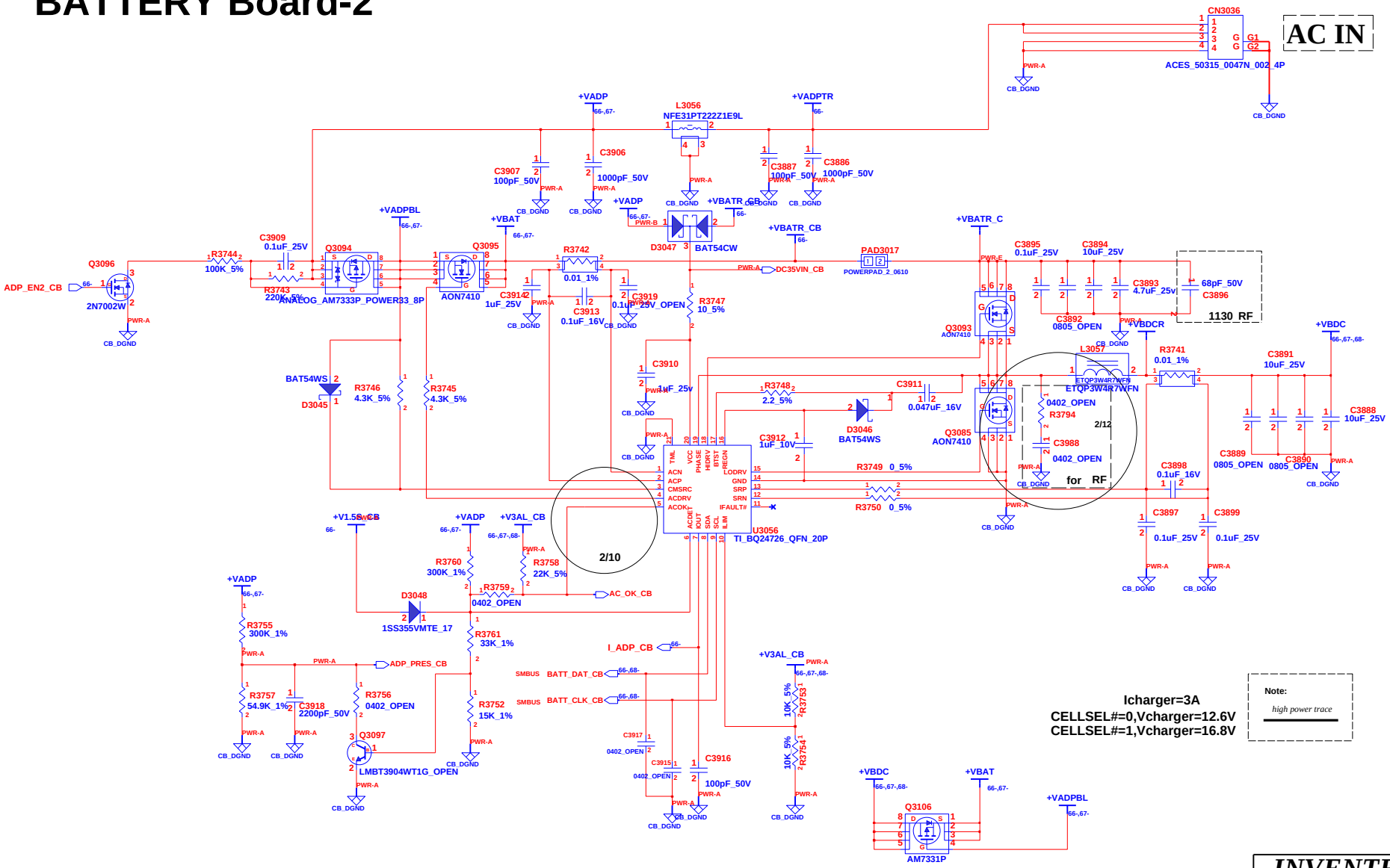


CHANGE by	Drawer_Name	28-Mar-2010	

INVENTEC

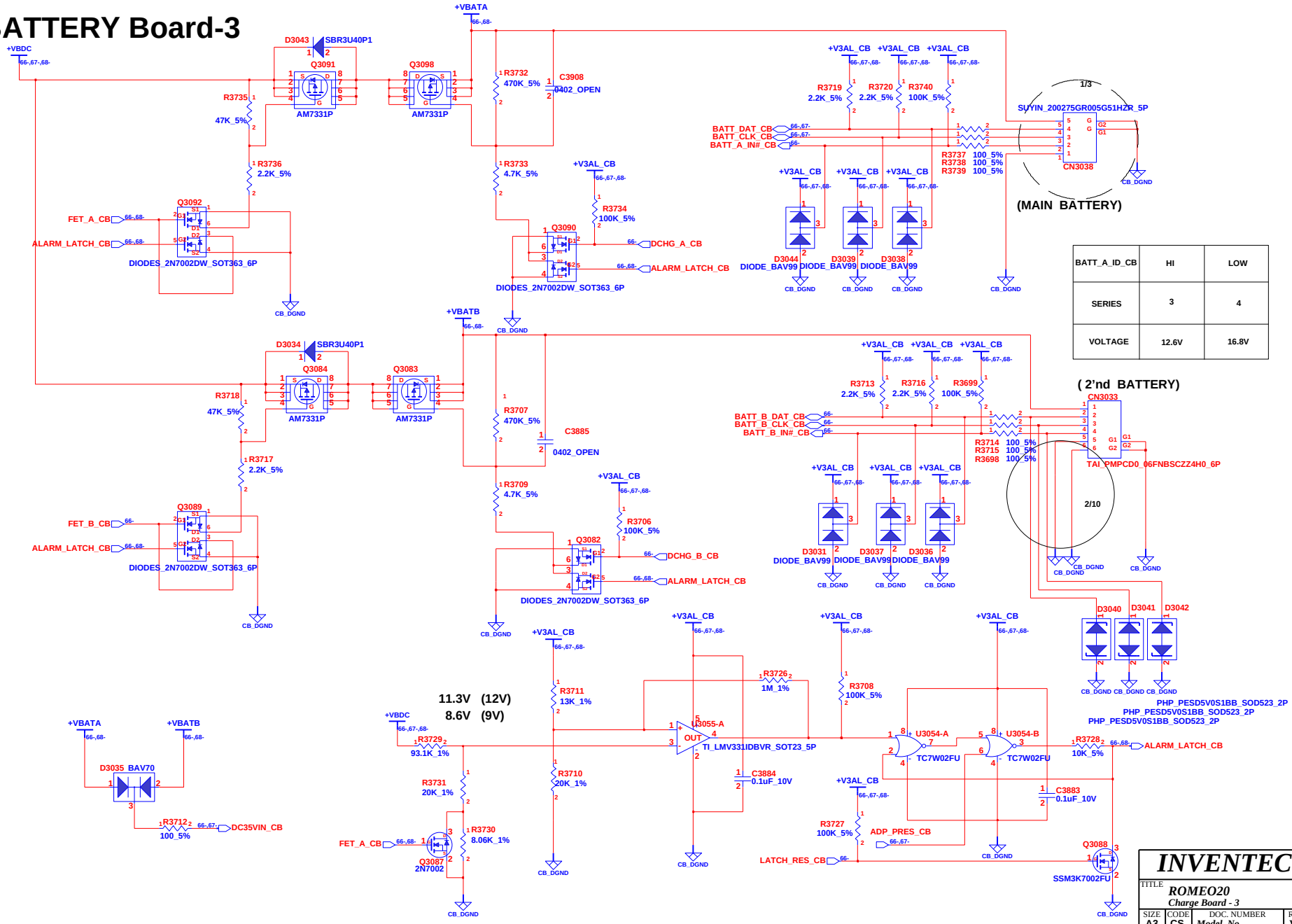
TITLE	ROMEO20 Charge Board - 1		
SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
		SHEET 66 OF 70	

BATTERY Board-2



INVENTEC			
TITLE	ROMEO20 Charge Board - 2		
SIZE A3	CODE CS	DOC. NUMBER Model_No	REV X01
CHANGE by Drawer_Name	28-Mar-2010	SHEET 67 OF 70	

BATTERY Board-3



BATT_A_ID_CB	HI	LOW
SERIES	3	4
VOLTAGE	12.6V	16.8V

CHANGE by	Drawer_Name	28-Mar-2010

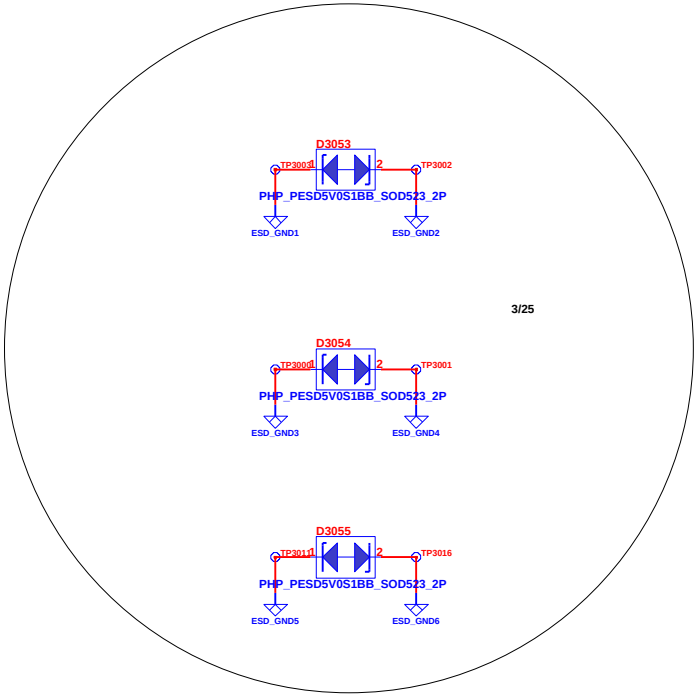
INVENTEC

TITLE: ROMEO20
Charge Board - 3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model_No	X01

SHEET 68 OF 70

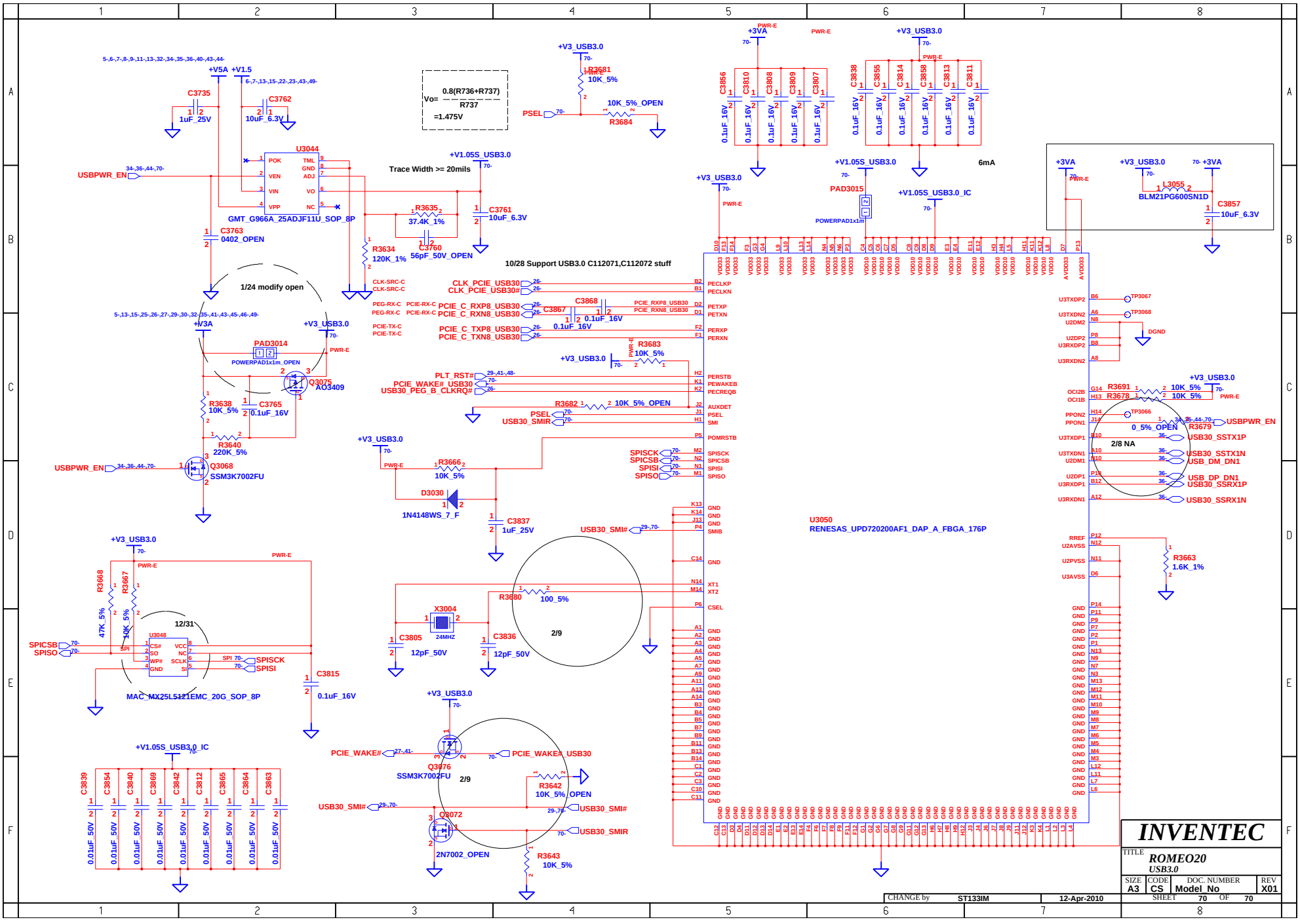
EMC Board



CHANGE by	*Drawer_Name*	*28-Mar-2010*	

INVENTEC

TITLE	*ROMEO20* *EMC*		
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*Model_No*	*X01*
SHEET	69	OF	70


+V5A
+V1.5
C3735
1uF_25V
C3762
10uF_6.3V
U3044
GMT_G966A_25ADJF11U_SOP_8P
USBPWR_EN
C3763
0402_OPEN
R3634
120K_1%
R3635
37.4K_1%
C3761
10uF_6.3V
C3760
56pF_50V_OPEN
Trace Width >= 20mils
Vo= 0.8(R736+R737) / R737 =1.475V
+V1.05S_USB3.0
+V3_USB3.0
R3681
10K_5%
R3684
10K_5%_OPEN
PSEL
1/24 modify open
+V3A
PAD3014
POWERPAD1x1m_OPEN
Q3075
AO3409
R3638
10K_5%
C3765
0.1uF_16V
R3640
220K_5%
Q3068
SSM3K7002FU
10/28 Support USB3.0 C112071,C112072 stuff
CLK_PCIE_USB30
CLK_PCIE_USB30#
PCIE_C_RXP8_USB30
PCIE_C_RXN8_USB30
C3868
C3867
0.1uF_16V
PCIE_C_TXP8_USB30
PCIE_C_TXN8_USB30
R3683
10K_5%
PLT_RST#
PCIE_WAKE#_USB30
USB30_PEG_B_CLKRQ#
R3682
10K_5%_OPEN
USB30_SMIR
R3666
10K_5%
D3030
1N4148WS_7_F
C3837
1uF_25V
USB30_SMI#
SPISCK
SPICSB
SPISI
SPISO
U3050
RENESAS_UPD720200AF1_DAP_A_FBGA_176P
R3680
100_5%
X3004
24MHZ
C3805
12pF_50V
C3836
12pF_50V
2/9
12/31
U3048
MAC_MX25L5121EMC_20G_SOP_8P
R3668
47K_5%
R3667
10K_5%
C3815
0.1uF_16V
+V1.05S_USB3.0_IC
C3839
C3854
C3840
C3869
C3842
C3812
C3865
C3864
C3863
0.01uF_50V
PCIE_WAKE#
PCIE_WAKE#_USB30
Q3076
SSM3K7002FU
R3642
10K_5%_OPEN
Q3072
2N7002_OPEN
R3643
10K_5%
C3856
C3810
C3808
C3809
C3807
C3838
C3855
C3814
C3858
C3813
C3811
0.1uF_16V
6mA
PAD3015
POWERPAD1x1m
L3055
BLM21PG600SN1D
C3857
10uF_6.3V
TP3067
TP3068
DGND
R3691
10K_5%
R3678
10K_5%
TP3066
0_5%_OPEN
R3679
2/8 NA
USBPWR_EN
USB30_SSTX1P
USB30_SSTX1N
USB_DM_DN1
USB_DP_DN1
USB30_SSRX1P
USB30_SSRX1N
R3663
1.6K_1%
INVENTEC
TITLE
ROMEO20
USB3.0
SIZE A3
CODE CS
DOC. NUMBER Model_No
REV X01
SHEET 70 OF 70
CHANGE by ST133IM
12-Apr-2010