630CF REV:3.0
Layout all Bead 0805-->0603

PPGA 370

VID3	VID2	VID1	VID0	VCC_CORE
1	1	1	1	1.30
1	1	1	0	1.35
1	1	0	1	1.40
1	1	0	0	1.45
1	0	1	1	1.50
1	0	1	0	1.55
1	0	0	1	1.60
1	0	0	0	1.65
0	1	1	1	1.70
0	1	1	0	1.75
0	1	0	1	1.80
0	1	0	0	1.85
0	0	1	1	1.90
0	0	1	0	1.95
0	0	0	1	2.00
0	0	0	0	2.05

For Cu-256 PU_cmos=150 Ohm

For Future Compatibility Upgrade

@ FOR FSB=133MHZ Lmax=4.5 inches

MENDOCINO PPGA

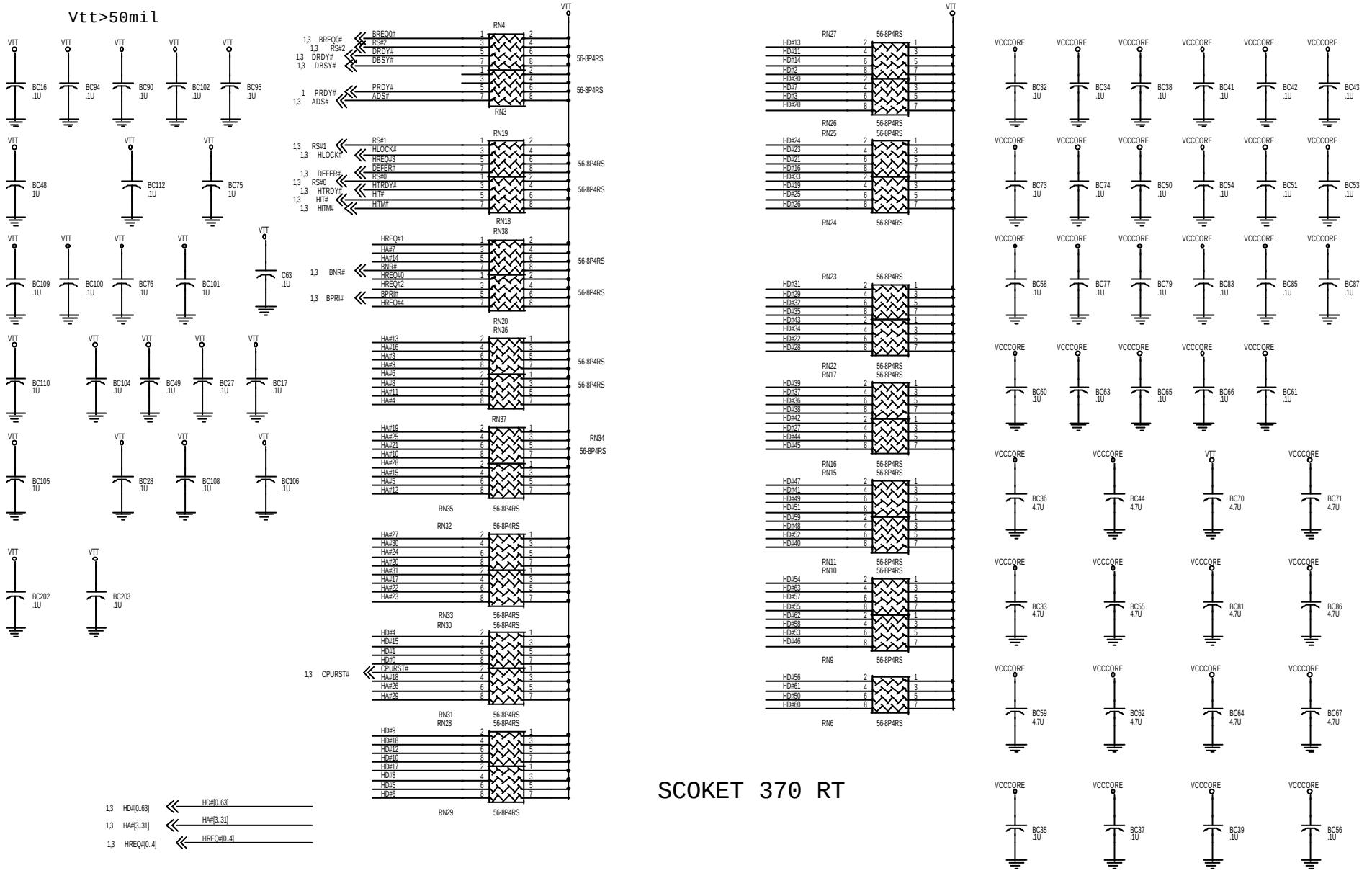
LINK
2.SCH
3.SCH
4.SCH
5.SCH
6.SCH
7.SCH
8.SCH
9.SCH
10.SCH
11.SCH
12.SCH
13.SCH
14.SCH
15.SCH
16.SCH
17.SCH
18.SCH
19.SCH
20.SCH
21.SCH
22.SCH
23.SCH
24.SCH
25.SCH
26.SCH

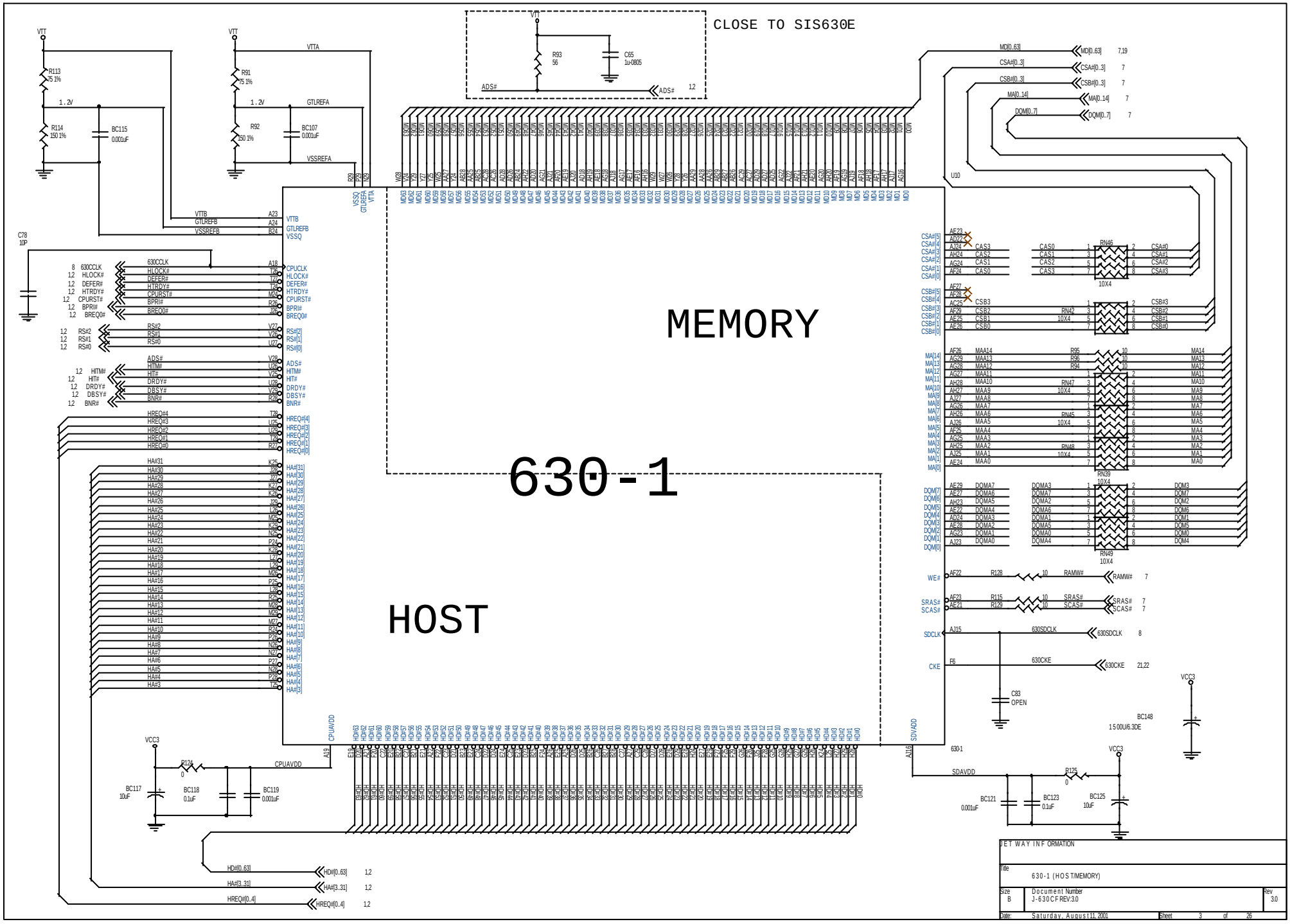
DET WAY INF ORMATION

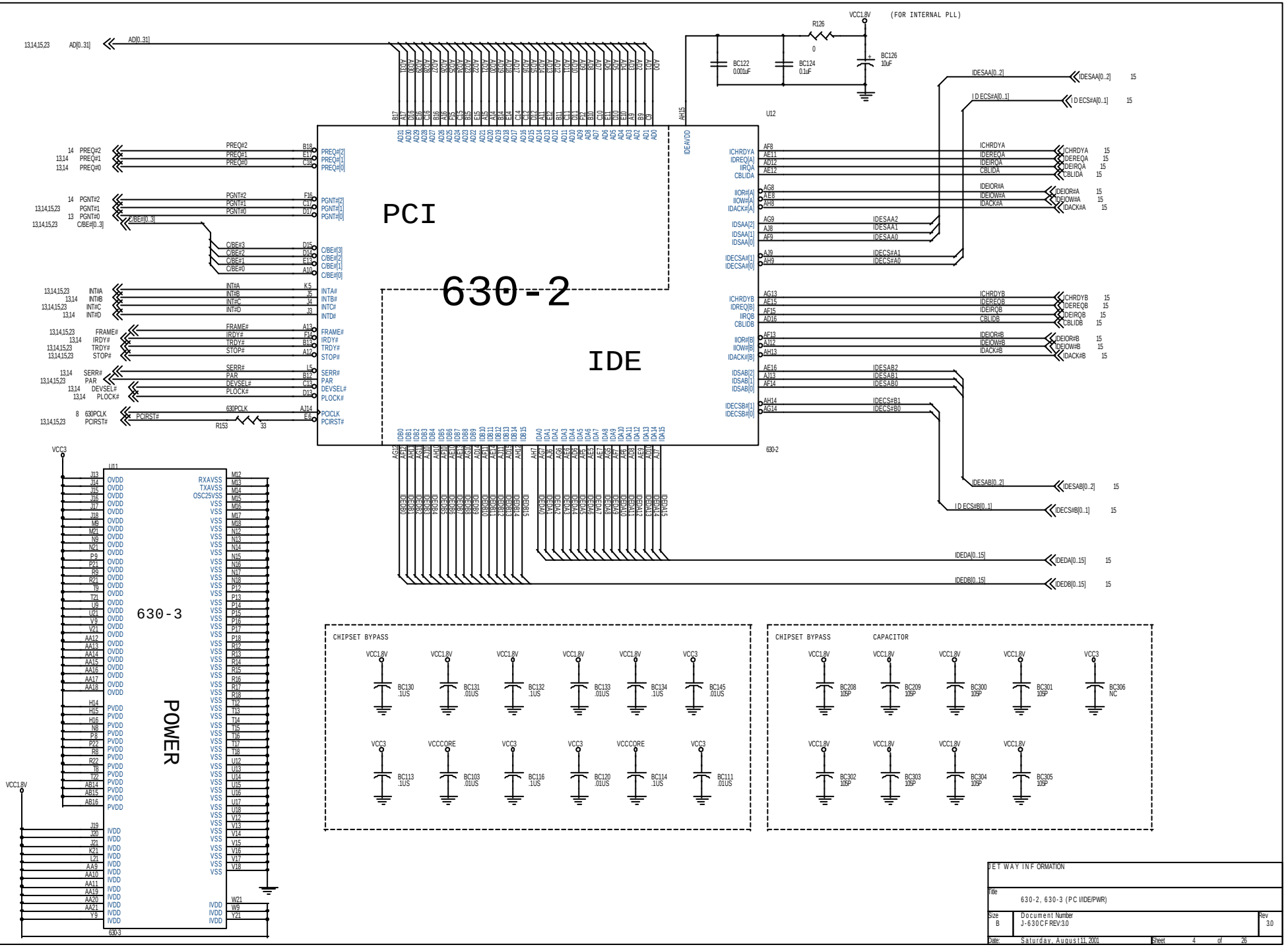
Title: MENDOCINO PPGA CPU

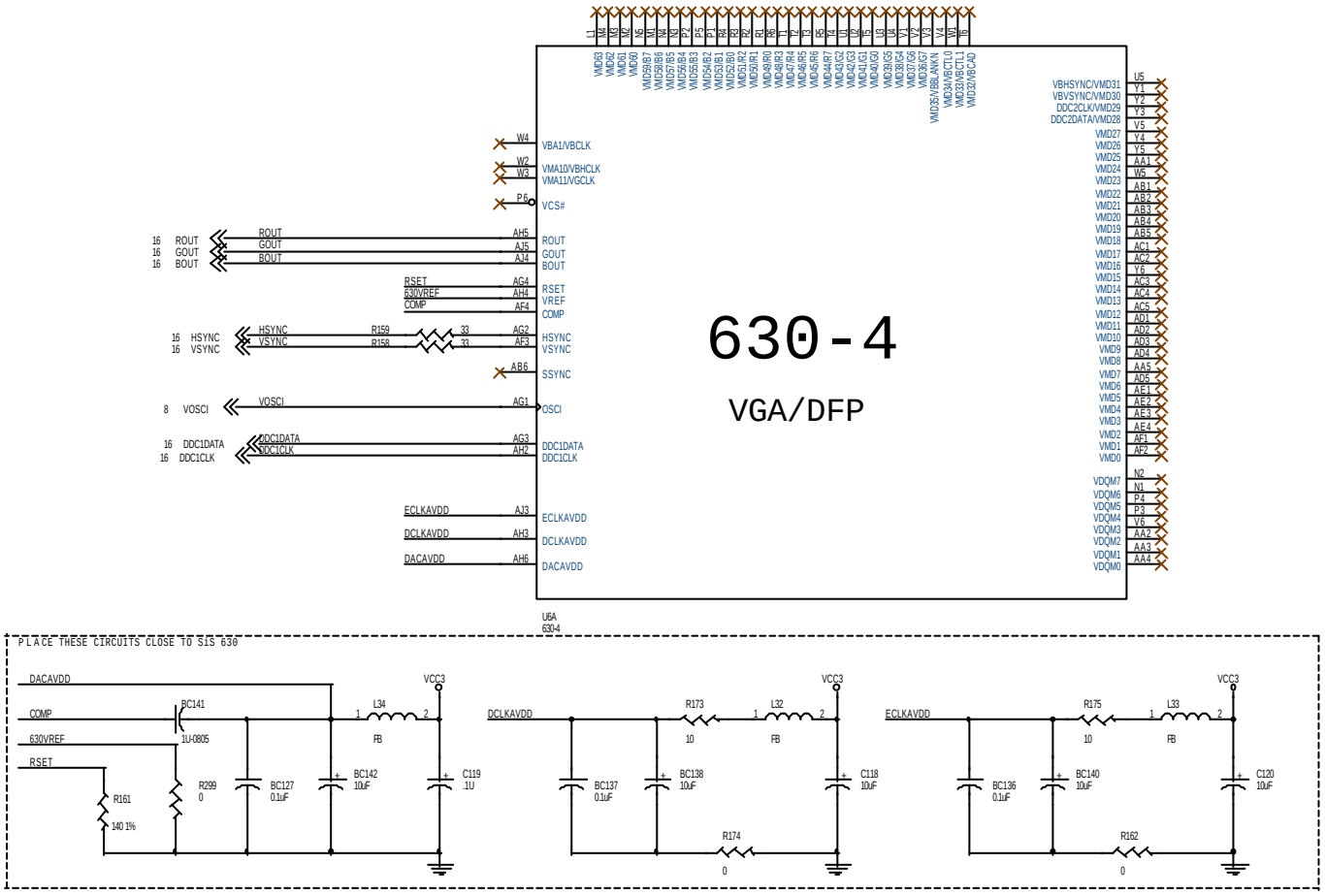
Size: B | Document Number: J-630CF REV:3.0 | Rev: 3.0

Date: Saturday, August 11, 2001 | Sheet 1 of 26

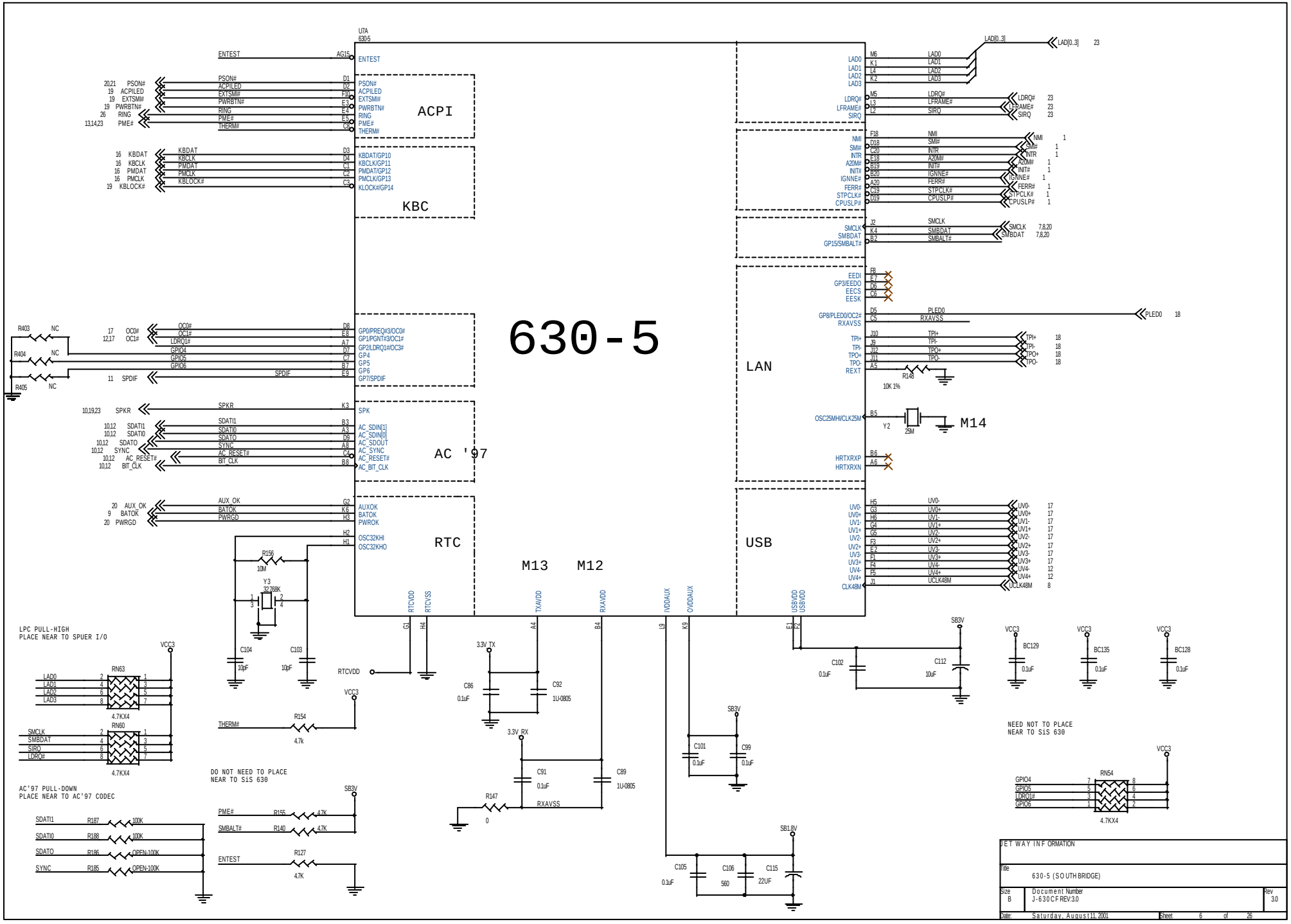

Vtt>50mil
SCOKET 370 RT
NOTE: GTL+ TERMINATION RESISTORS ONLY FOR MENDOCINO PPGA PROCESSOR.
GTL+ TERMINATION RESISTORS
Saturday, August 11, 2001
Sheet 2 of 26

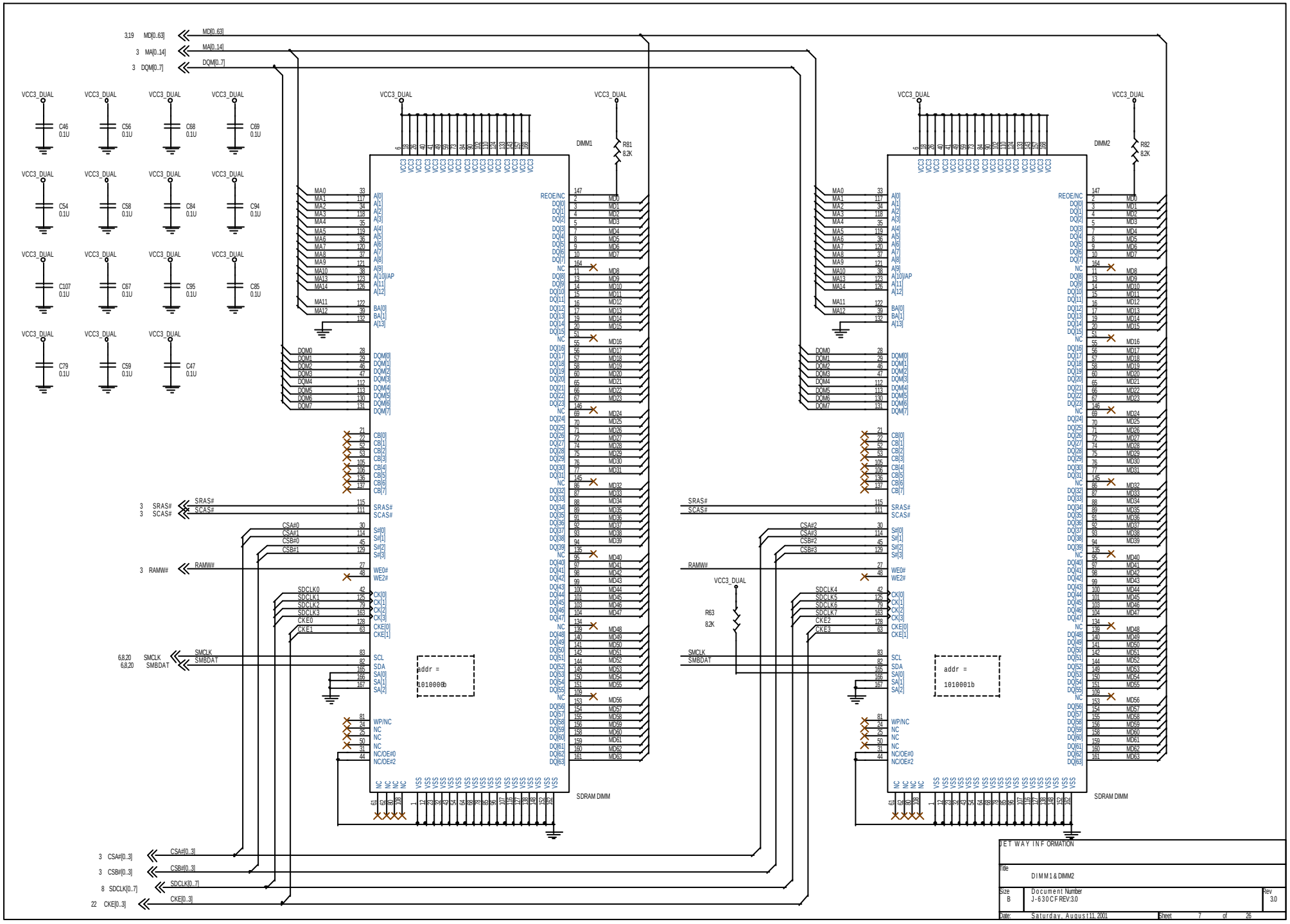

CLOSE TO SIS630E
MEMORY
630-1
HOST
R93
56
C65
1u-0805
ADS#
ADS# 1,2
R113
75 1%
R114
150 1%
1.2V
BC115
0.001uF
VTT
VTTA
R91
75 1%
R92
150 1%
GTLREFA
BC107
0.001uF
VSSREFA
C78
10P
VTTB
GTLREFB
VSSQ
VSSREFB
630CCLK
HLOCK#
DEFER#
HTRDY#
CPURST#
BPRI#
BREQ0#
RS#2
RS#1
RS#0
ADS#
HITM#
HIT#
DRDY#
DBSY#
BNR#
HREQ#4
HREQ#3
HREQ#2
HREQ#1
HREQ#0
HA#31
HA#30
HA#29
HA#28
HA#27
HA#26
HA#25
HA#24
HA#23
HA#22
HA#21
HA#20
HA#19
HA#18
HA#17
HA#16
HA#15
HA#14
HA#13
HA#12
HA#11
HA#10
HA#9
HA#8
HA#7
HA#6
HA#5
HA#4
HA#3
HD#[0..63]
HA#[3..31]
HREQ#[0..4]
HD#[0..63] 1,2
HA#[3..31] 1,2
HREQ#[0..4] 1,2
MD[0..63]
CSA#[0..3]
CSB#[0..3]
MA[0..14]
DQM[0..7]
MD[0..63] 7,19
CSA#[0..3] 7
CSB#[0..3] 7
MA[0..14] 7
DQM[0..7] 7
U10
RN46
10X4
RN42
10X4
RN47
10X4
RN45
10X4
RN48
10X4
RN39
10X4
RN49
10X4
R95
R96
R94
WE#
SRAS#
SCAS#
SDCLK
CKE
R128
R115
R129
RAMW#
SRAS#
SCAS#
630SDCLK
630CKE
C83
OPEN
BC148
1500UI6.3DE
VCC3
CPUAVDD
SDAVDD
R124
0
BC117
10uF
BC118
0.1uF
BC119
0.001uF
R125
0
BC121
0.001uF
BC123
0.1uF
BC125
10uF
DET WAY INF ORMATION
Title
630-1 (HOST/MEMORY)
Size
B
Document Number
J-630CF REV:3.0
Rev
3.0
Date:
Saturday, August 11, 2001
Sheet
3
of
26

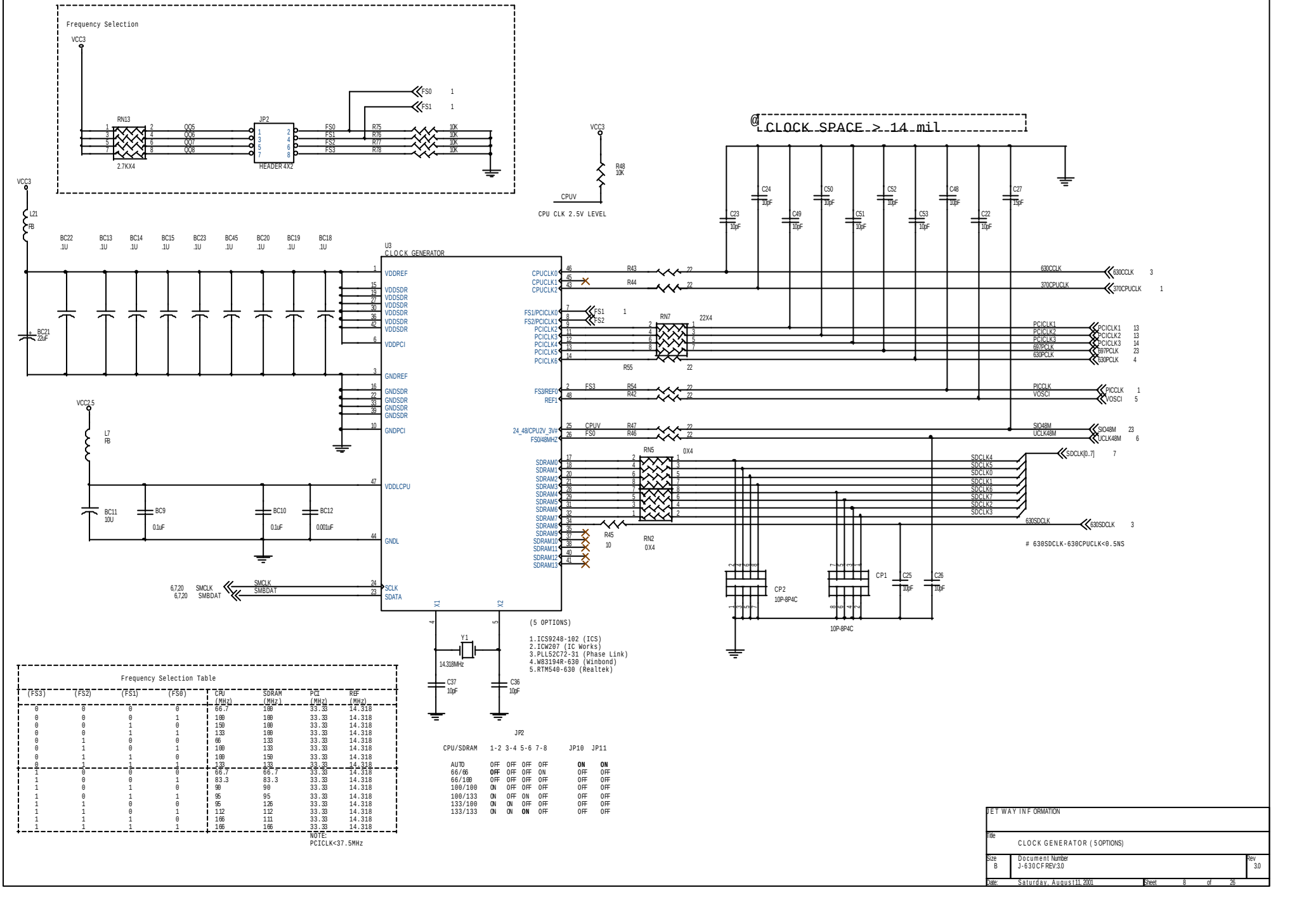

PCI
630-2
IDE
630-3
POWER
VCC1.8V (FOR INTERNAL PLL)
R126
0
BC122 0.001uF
BC124 0.1uF
BC126 10uF
U12
U11
AD[0..31]
IDESAA[0..2]
IDECS#A[0..1]
IDESAB[0..2]
IDECS#B[0..1]
IDEDA[0..15]
IDEDB[0..15]
CHIPSET BYPASS
CHIPSET BYPASS CAPACITOR
BC130 .1US
BC131 .01US
BC132 .1US
BC133 .01US
BC134 .1US
BC145 .01US
BC113 .1US
BC103 .01US
BC116 .1US
BC120 .01US
BC114 .1US
BC111 .01US
BC208 105P
BC209 105P
BC300 105P
BC301 105P
BC306 NC
BC302 105P
BC303 105P
BC304 105P
BC305 105P
DET WAY INF ORMATION
630-2, 630-3 (PC I/IDE/PWR)
Document Number J-630CF REV:3.0
Rev 3.0
Size B
Date: Saturday, August 11, 2001
Sheet 4 of 26



DET WAY INF ORMATION		
Title: 630-4 (VGA/DFP)		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 5 of 26	


630-5
ACPI
KBC
AC '97
RTC
LAN
USB
M13 M12
M14
U7A
630-5
ENTEST
PSON#
ACPILED
EXTSMI#
PWRBTN#
RING
PME#
THERM#
KBDAT
KBCLK
PMDAT
PMCLK
KBLOCK#
KBDAT/GP10
KBCLK/GP11
PMDAT/GP12
PMCLK/GP13
KLOCK#/GP14
OC0#
OC1#
LDRQ1#
GPIO4
GPIO5
GPIO6
SPDIF
GP0/PREQ#3/OC0#
GP1/PGNT#3/OC1#
GP2/LDRQ1#/OC3#
GP4
GP5
GP6
GP7/SPDIF
SPKR
SDATI1
SDATI0
SDATO
SYNC
AC_RESET#
BIT_CLK
SPK
AC_SDIN[1]
AC_SDIN[0]
AC_SDOUT
AC_SYNC
AC_RESET#
AC_BIT_CLK
AUX_OK
BATOK
PWRGD
AUXOK
BATOK
PWROK
OSC32KHI
OSC32KHO
LAD0
LAD1
LAD2
LAD3
LDRQ#
LFRAME#
SIRQ
NMI
SMI#
INTR
A20M#
INIT#
IGNNE#
FERR#
STPCLK#
CPUSLP#
SMCLK
SMBDAT
GP15/SMBALT#
EEDI
GP3/EEDO
EECS
EESK
GP8/PLED0/OC2#
RXAVSS
PLED0
TPI+
TPI-
TPO+
TPO-
REXT
10K 1%
OSC25MHI/CLK25M
Y2
25M
HRTXRXP
HRTXRXN
UV0-
UV0+
UV1-
UV1+
UV2-
UV2+
UV3-
UV3+
UV4-
UV4+
UCLK48M
RTCVDD
RXAVSS
TXAVDD
RXAVDD
IVDDAUX
OVDDAUX
USBVDD
SB3V
VCC3
SB1.8V
3.3V_TX
3.3V_RX
R156
10M
Y3
32.768K
C104
10pF
C103
10pF
R154
4.7k
THERM#
C86
0.1uF
C92
1U-0805
C91
0.1uF
C89
1U-0805
R147
0
C101
0.1uF
C99
0.1uF
C102
0.1uF
C112
10uF
BC129
BC135
BC128
0.1uF
C105
0.1uF
C106
560
C115
22UF
LPC PULL-HIGH
PLACE NEAR TO SPUER I/O
RN63
RN60
4.7KX4
AC'97 PULL-DOWN
PLACE NEAR TO AC'97 CODEC
SDATI1
SDATI0
SDATO
SYNC
R187
R188
R186
R185
100K
OPEN-100K
DO NOT NEED TO PLACE
NEAR TO SiS 630
PME#
SMBALT#
ENTEST
R155
R140
R127
4.7K
NEED NOT TO PLACE
NEAR TO SiS 630
RN54
R403
R404
R405
NC
R148
JET WAY INFORMATION
Title
630-5 (SOUTH BRIDGE)
Size
B
Document Number
J-630CF REV:3.0
Rev
3.0
Date: Saturday, August 11, 2001
Sheet 6 of 26


MD[0..63]
MA[0..14]
DQM[0..7]
VCC3_DUAL
C46 0.1U
C56 0.1U
C68 0.1U
C69 0.1U
C54 0.1U
C58 0.1U
C84 0.1U
C94 0.1U
C107 0.1U
C67 0.1U
C95 0.1U
C85 0.1U
C79 0.1U
C59 0.1U
C47 0.1U
DIMM1
DIMM2
R81 8.2K
R82 8.2K
R63 8.2K
SDRAM DIMM
addr = 1010000b
addr = 1010001b
SRAS#
SCAS#
RAMW#
SMCLK
SMBDAT
CSA#[0..3]
CSB#[0..3]
SDCLK[0..7]
CKE[0..3]
DET WAY INFORMATION
Title
DIMM1&DIMM2
Size B
Document Number J-630CF REV:3.0
Rev 3.0
Date: Saturday, August 11, 2001
Sheet 7 of 26



Frequency Selection Table

(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz)
0	0	0	0	66.7	100	33.33	14.318
0	0	0	1	100	100	33.33	14.318
0	0	1	0	150	100	33.33	14.318
0	0	1	1	133	100	33.33	14.318
0	1	0	0	66	133	33.33	14.318
0	1	0	1	100	133	33.33	14.318
0	1	1	0	100	150	33.33	14.318
0	1	1	1	133	133	33.33	14.318
1	0	0	0	66.7	66.7	33.33	14.318
1	0	0	1	83.3	83.3	33.33	14.318
1	0	1	0	99	90	33.33	14.318
1	0	1	1	95	95	33.33	14.318
1	1	0	0	95	126	33.33	14.318
1	1	0	1	112	112	33.33	14.318
1	1	1	0	166	111	33.33	14.318
1	1	1	1	166	166	33.33	14.318

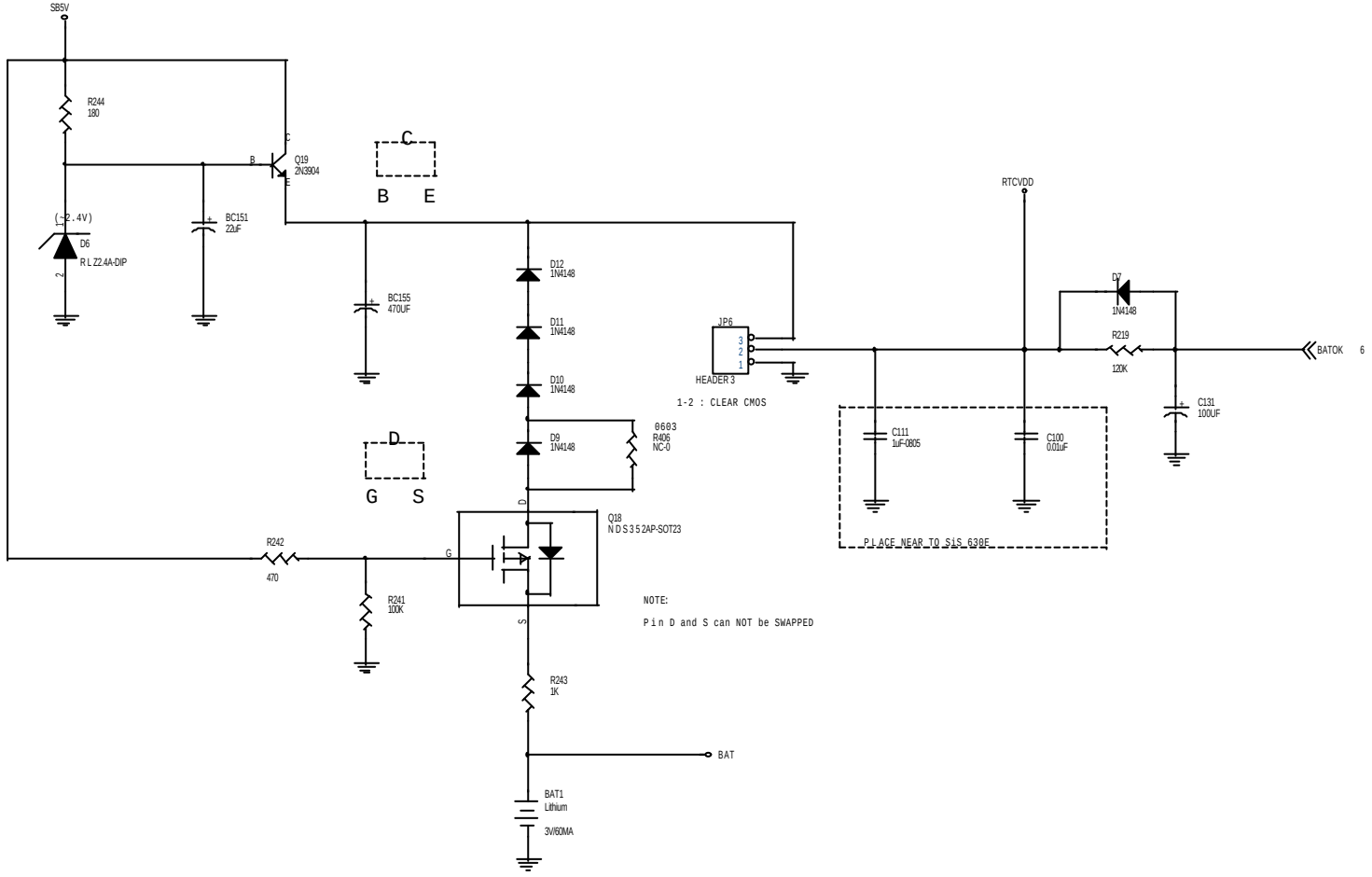
NOTE:
PCICLK<37.5MHz

JP2

CPU/SDRAM	1-2	3-4	5-6	7-8	JP10	JP11
AUTO	OFF	OFF	OFF	OFF	**ON**	**ON**
66/66	**OFF**	OFF	OFF	ON	OFF	OFF
66/100	OFF	OFF	OFF	OFF	OFF	OFF
100/100	ON	OFF	OFF	OFF	OFF	OFF
100/133	ON	OFF	ON	OFF	OFF	OFF
133/100	ON	ON	OFF	OFF	OFF	OFF
133/133	ON	ON	**ON**	OFF	OFF	OFF

DET WAY INF ORMATION	
Title	CLOCK GENERATOR (5 OPTIONS)
Size: B	Document Number: J-630CF REV:3.0
Rev: 3.0	
Date: Saturday, August 11, 2001	Sheet 8 of 26

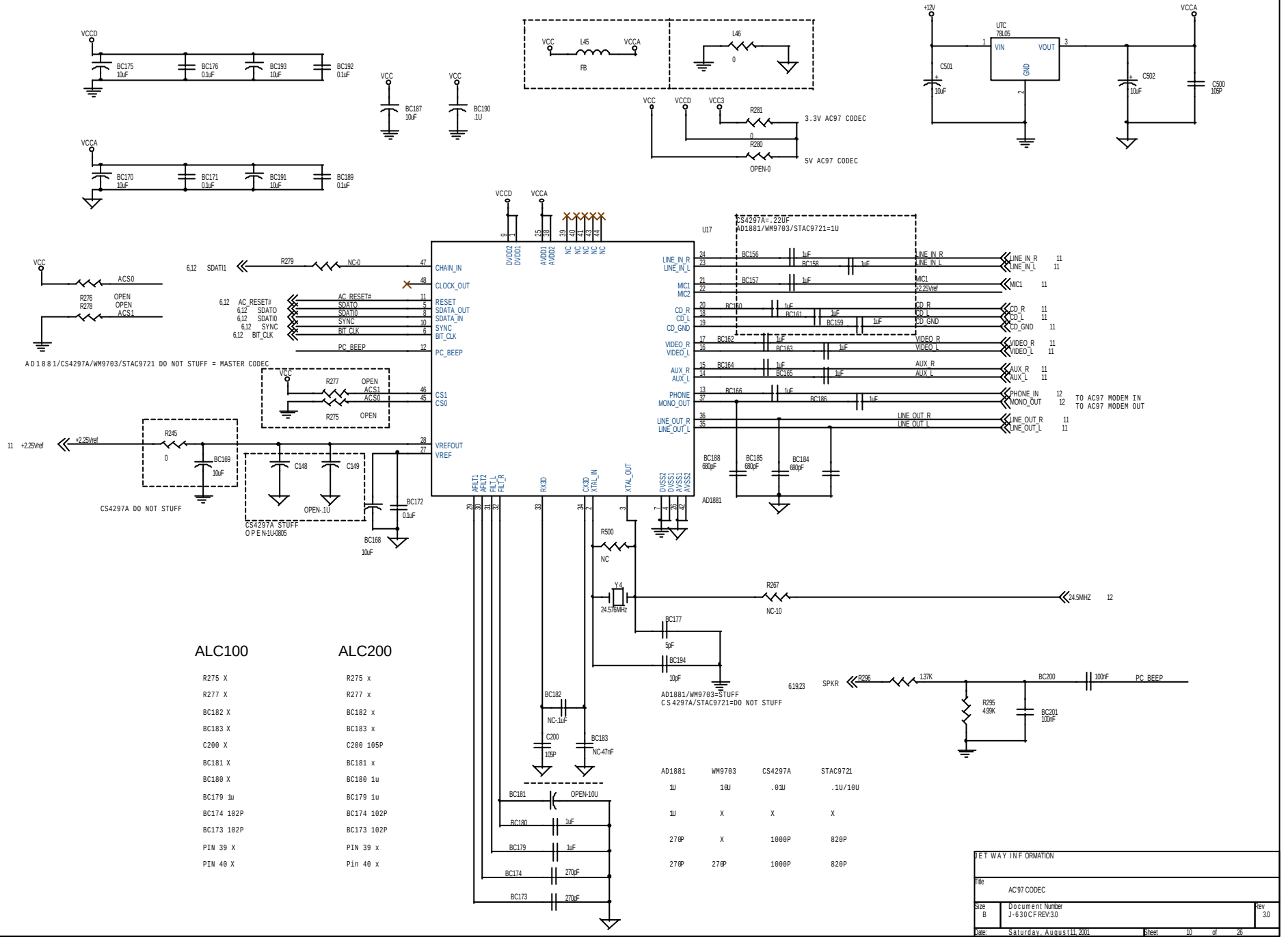
INT. RTC
MUST CLOSE TO CHIP RTCVDD PIN



NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

JETWAY INFORMATION		
Title: RTC		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 9 of 26	

ALC100/ALC200/AD1881/WM9703/CS4297A/STAC9721



ALC100

R275 X
R277 X
BC182 X
BC183 X
C200 X
BC181 X
BC180 X
BC179 1u
BC174 102P
BC173 102P
PIN 39 X
PIN 40 X

ALC200

R275 x
R277 x
BC182 x
BC183 x
C200 105P
BC181 x
BC180 1u
BC179 1u
BC174 102P
BC173 102P
PIN 39 x
Pin 40 x

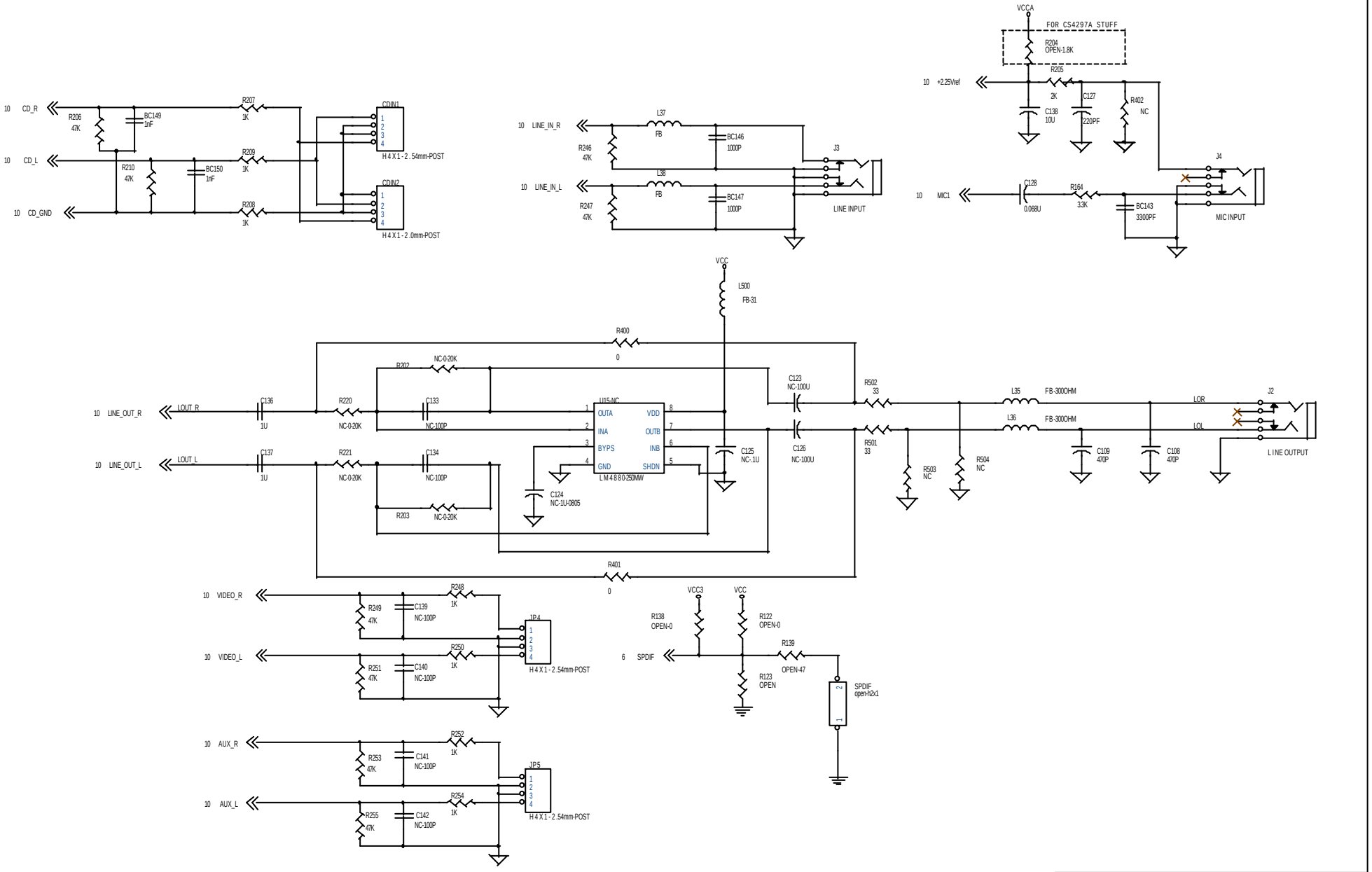
AD1881	WM9703	CS4297A	STAC9721
1U	10U	.01U	.1U/10U
1U	X	X	X
270P	X	1000P	820P
270P	270P	1000P	820P

DET WAY INFORMATION

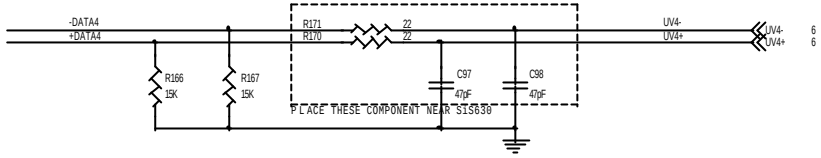
Title: AC'97 CODEC

Size: B | Document Number: J-630CF REV:3.0 | Rev: 3.0

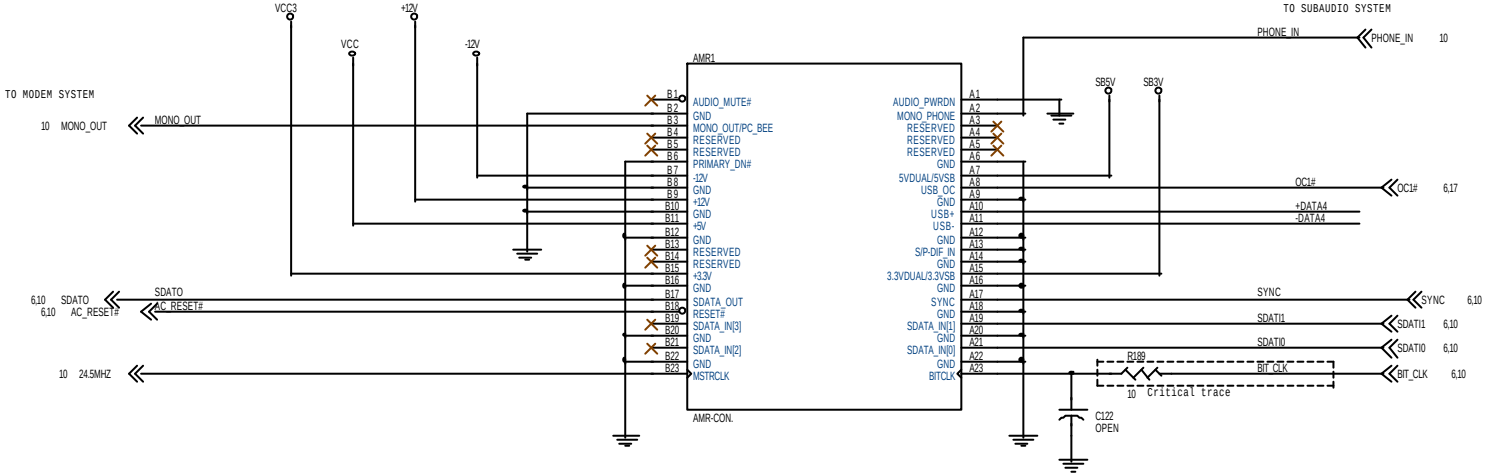
Date: Saturday, August 11, 2001 | Sheet 10 of 26



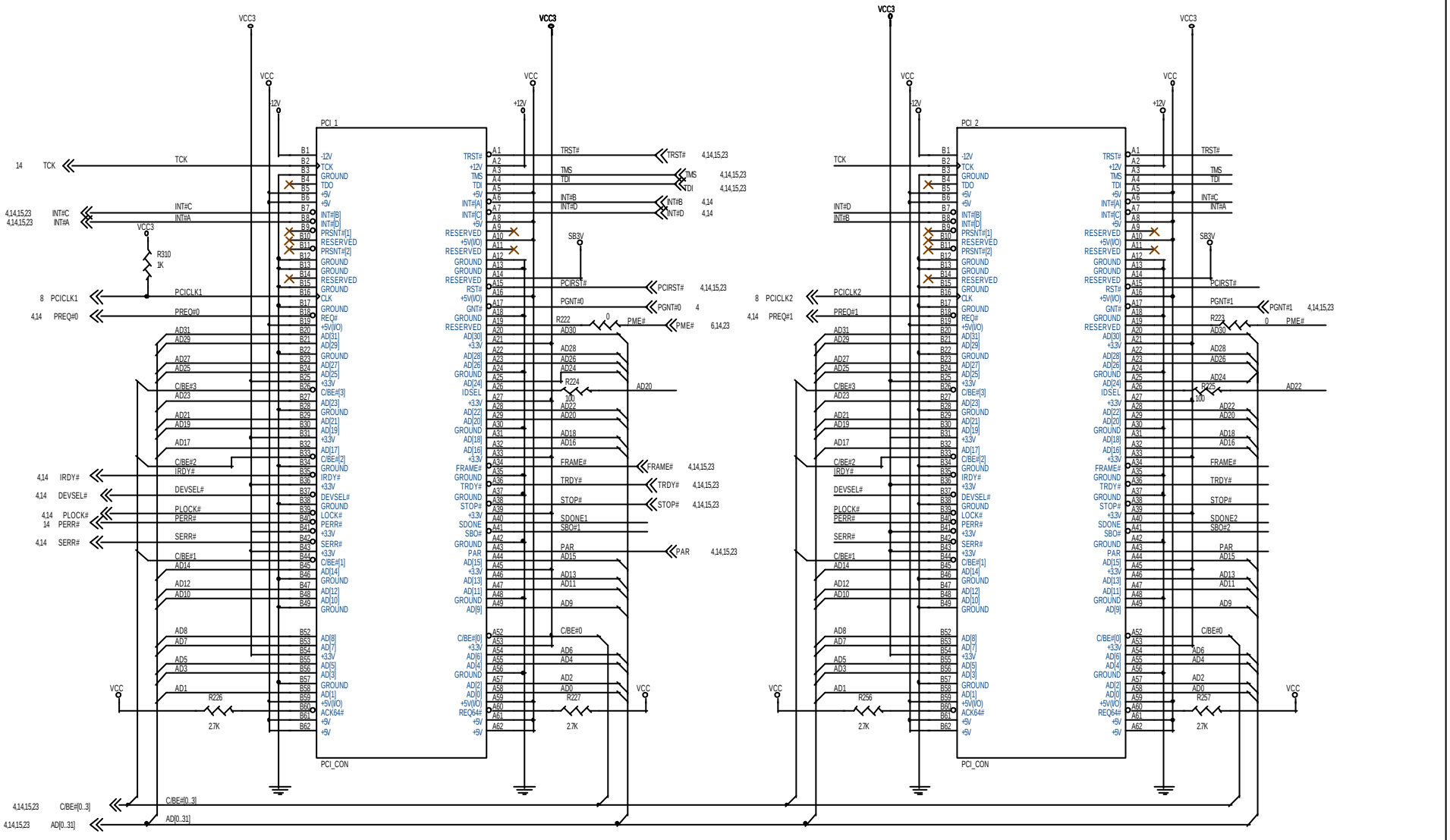
DET WAY INF ORMATION		
Title	AUDIO ANALOG UE IN/OUT	
Size B	Document Number J-630CF REV:3.0	Rev 3.0
Date: Saturday, August 11, 2001	Sheet 11 of 26	



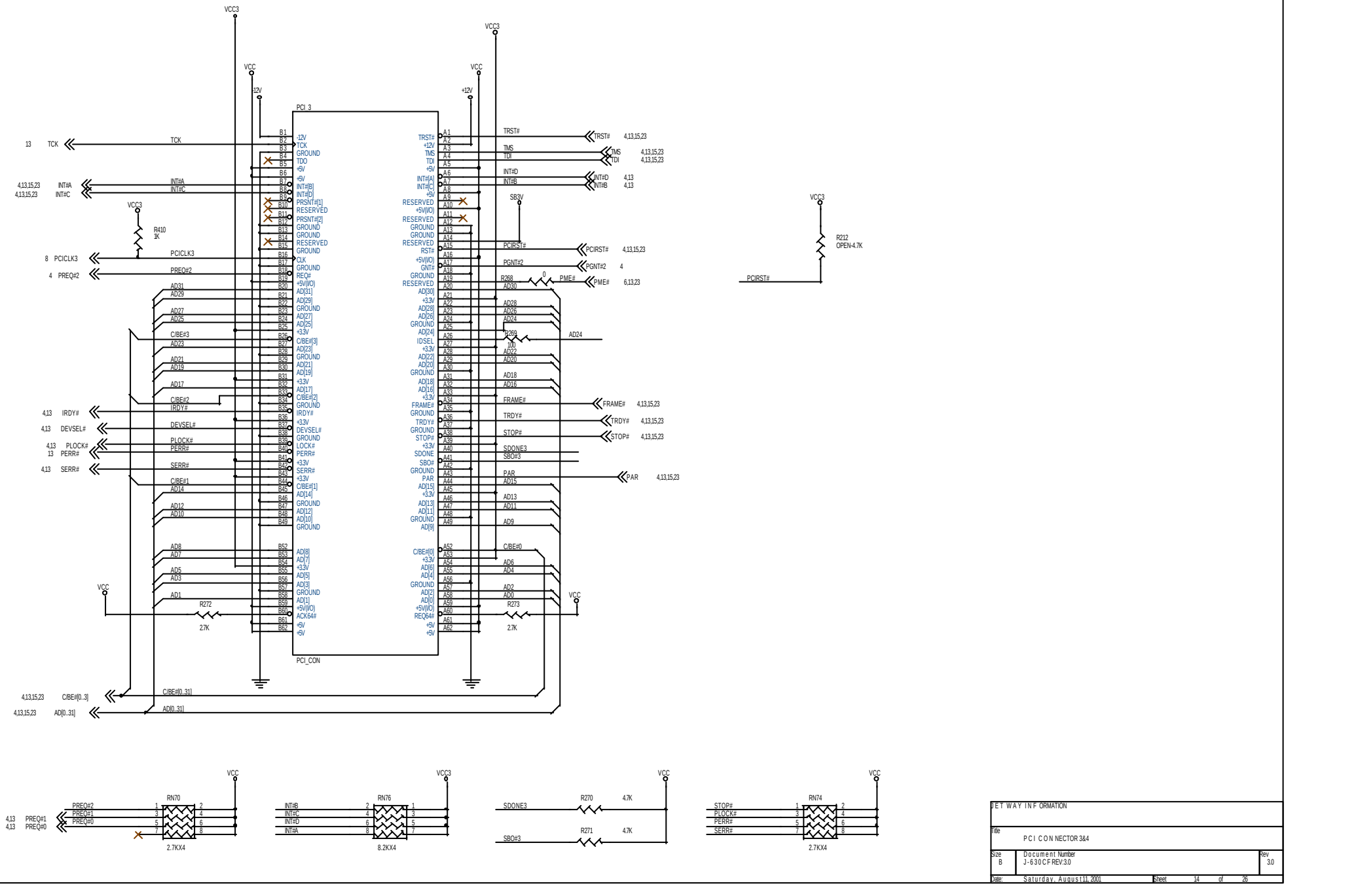
AMR



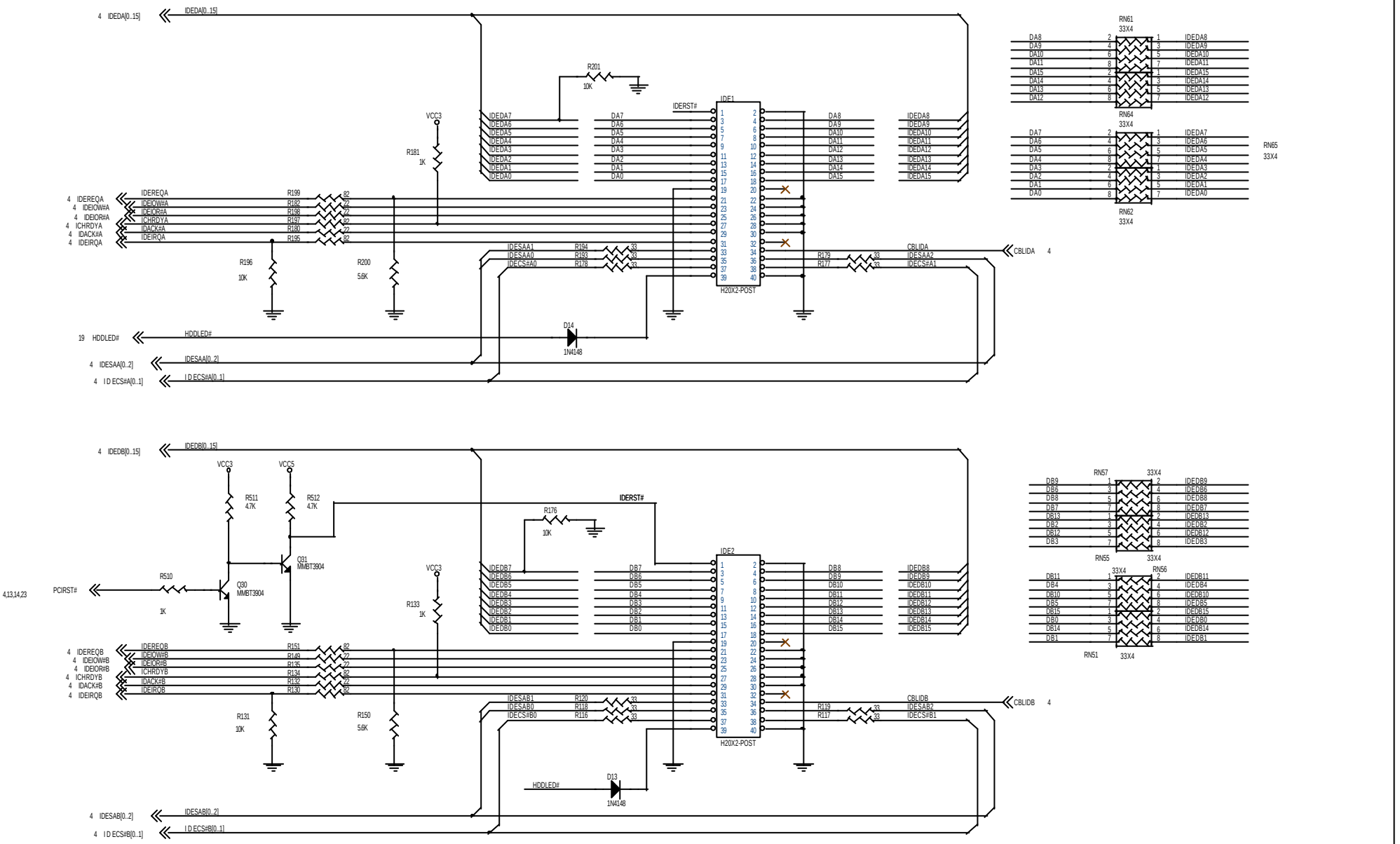
DET WAY INFORMATION		
Title: AUDIO/MODEM RISER		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 12 of 26	

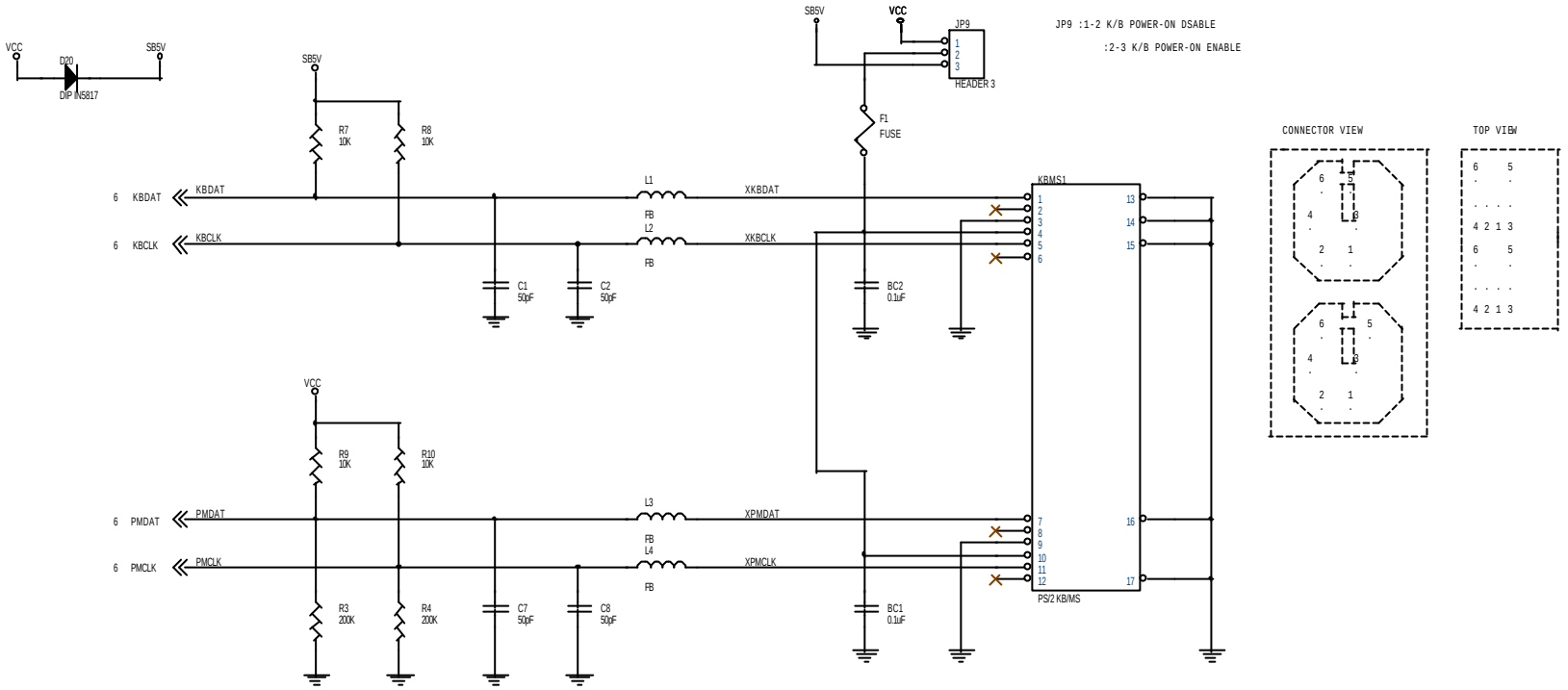


DET WAY INFORMATION		
Title: PCI CONNECTOR 1&2		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 13 of 26	

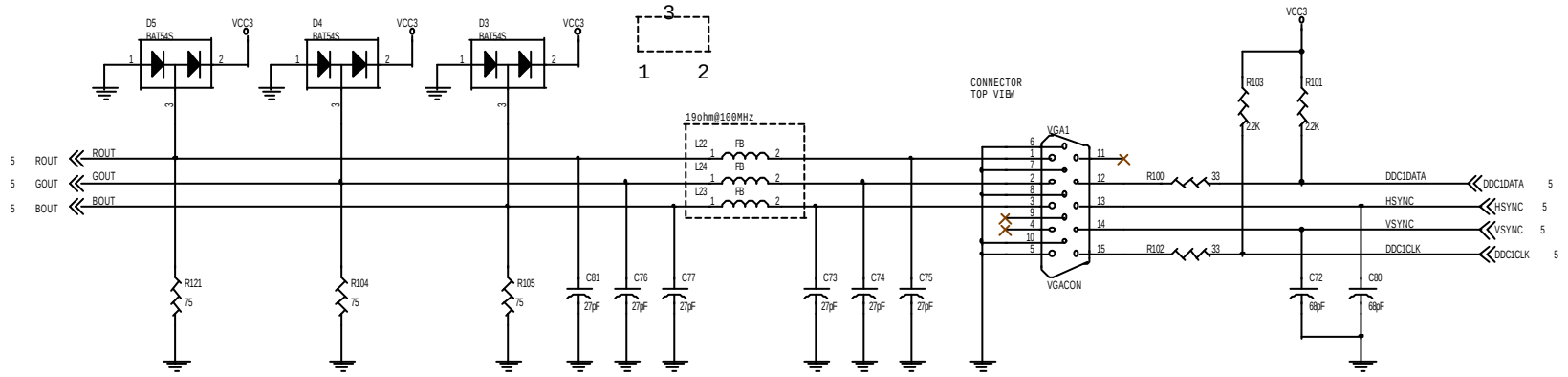


DET WAY INF ORMATION		
Title	PCI CONNECTOR 3&4	
Size B	Document Number J-630CF REV:3.0	Rev 3.0
Date: Saturday, August 11, 2001	Sheet 14 of 26	


4 IDEDA[0..15]
IDEDA[0..15]
R201
10K
VCC3
R181
1K
IDERST#
IDE1
IDEDA7
IDEDA6
IDEDA5
IDEDA4
IDEDA3
IDEDA2
IDEDA1
IDEDA0
DA7
DA6
DA5
DA4
DA3
DA2
DA1
DA0
DA8
DA9
DA10
DA11
DA12
DA13
DA14
DA15
IDEDA8
IDEDA9
IDEDA10
IDEDA11
IDEDA12
IDEDA13
IDEDA14
IDEDA15
RN61
33X4
RN64
33X4
RN62
33X4
RN65
33X4
4 IDEREQA
4 IDEIOW#A
4 IDEIOR#A
4 ICHRDYA
4 IDACK#A
4 IDEIRQA
IDEREQA
IDEIOW#A
IDEIOR#A
ICHRDYA
IDACK#A
IDEIRQA
R199
R182
R198
R197
R180
R195
82
22
22
82
22
82
R196
10K
R200
5.6K
IDESAA1
IDESAA0
IDECS#A0
R194
R193
R178
33
33
33
R179
R177
CBLIDA
IDESAA2
IDECS#A1
CBLIDA 4
H20X2-POST
D14
1N4148
19 HDDLED#
HDDLED#
4 IDESAA[0..2]
IDESAA[0..2]
4 IDECS#A[0..1]
IDECS#A[0..1]
4 IDEDB[0..15]
IDEDB[0..15]
VCC3
VCC5
R511
4.7K
R512
4.7K
IDERST#
R176
10K
Q31
MMBT3904
Q30
MMBT3904
R510
1K
PCIRST#
4,13,14,23
VCC3
R133
1K
IDE2
IDEDB7
IDEDB6
IDEDB5
IDEDB4
IDEDB3
IDEDB2
IDEDB1
IDEDB0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
IDEDB8
IDEDB9
IDEDB10
IDEDB11
IDEDB12
IDEDB13
IDEDB14
IDEDB15
RN57
33X4
RN55
33X4
RN56
RN51
33X4
4 IDEREQB
4 IDEIOW#B
4 IDEIOR#B
4 ICHRDYB
4 IDACK#B
4 IDEIRQB
IDEREQB
IDEIOW#B
IDEIOR#B
ICHRDYB
IDACK#B
IDEIRQB
R151
R149
R135
R134
R132
R130
82
22
22
82
22
82
R131
10K
R150
5.6K
IDESAB1
IDESAB0
IDECS#B0
R120
R118
R116
33
33
33
R119
R117
CBLIDB
IDESAB2
IDECS#B1
CBLIDB 4
H20X2-POST
D13
1N4148
HDDLED#
4 IDESAB[0..2]
IDESAB[0..2]
4 IDECS#B[0..1]
IDECS#B[0..1]
NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.
DET WAY INF ORMATION
Title
IDE CONNECTORS
Size
B
Document Number
J-630CF REV:3.0
Rev
3.0
Date:
Saturday, August 11, 2001
Sheet
15
of
26

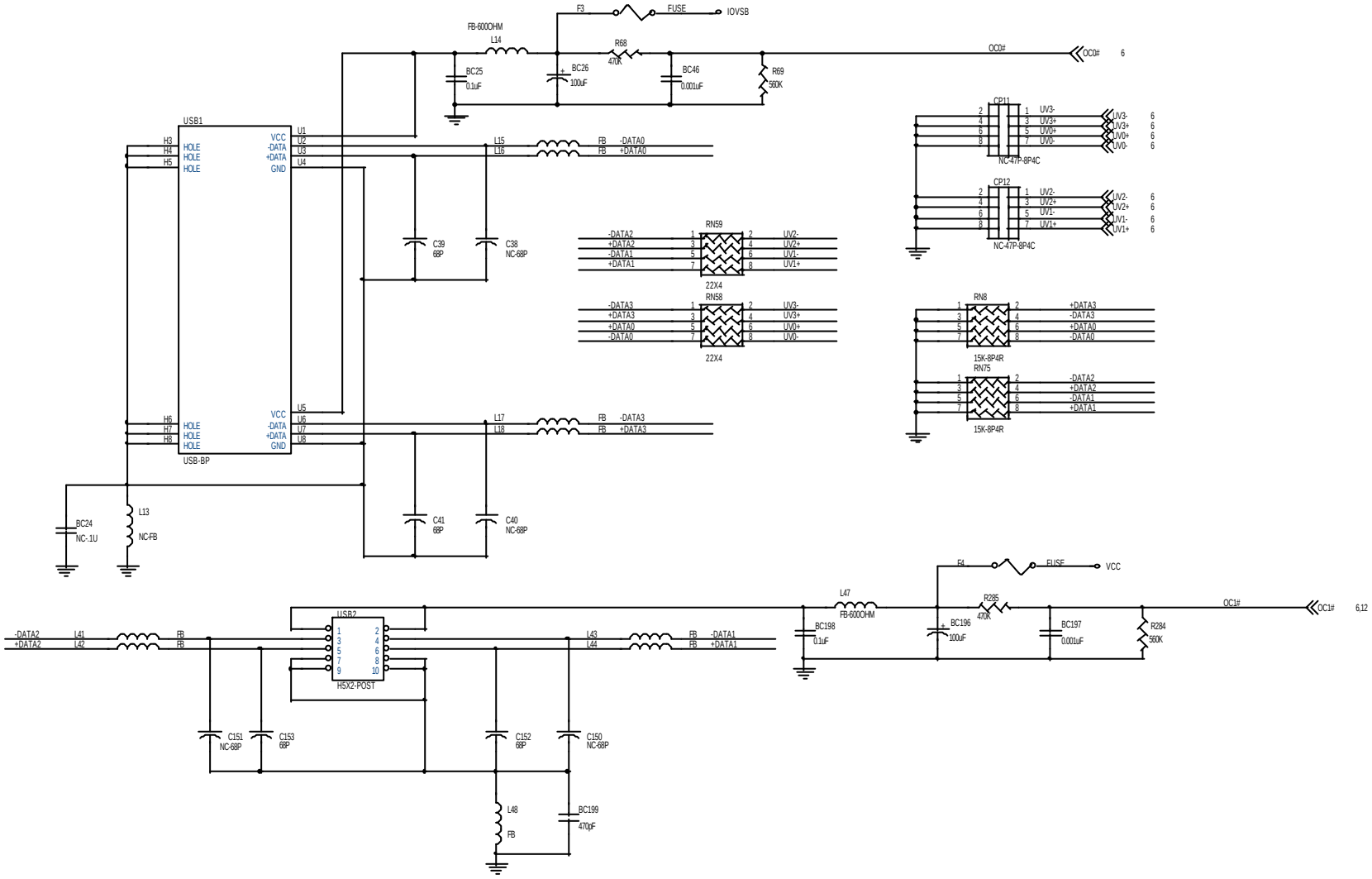


VGA CONNECTOR 1

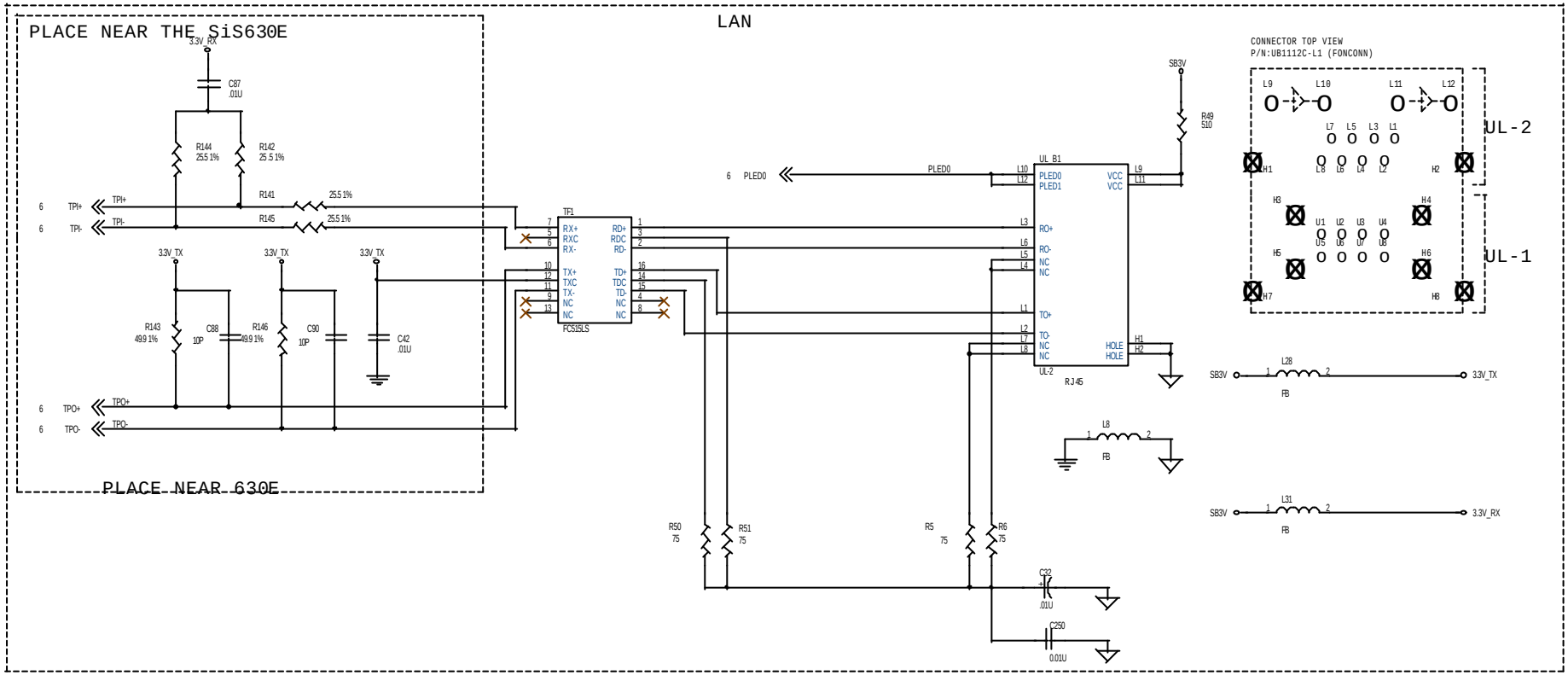


NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

JET WAY INFORMATION		
Title: KEYBOARD & MOUSE CONNECTORS		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 16 of 26	

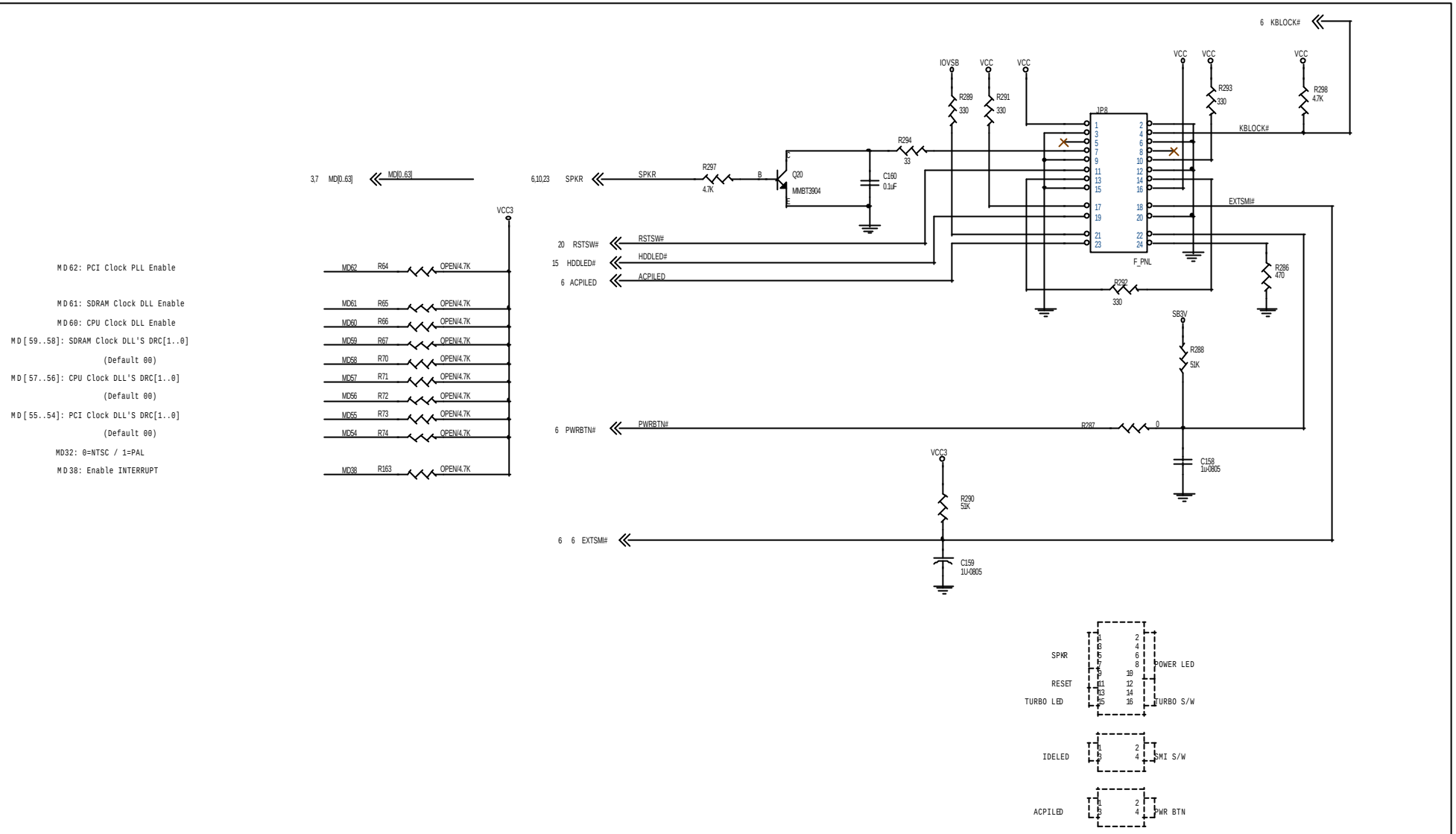


DET WAY INFORMATION		
Title: USB CONNECTORS		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 17 of 26	



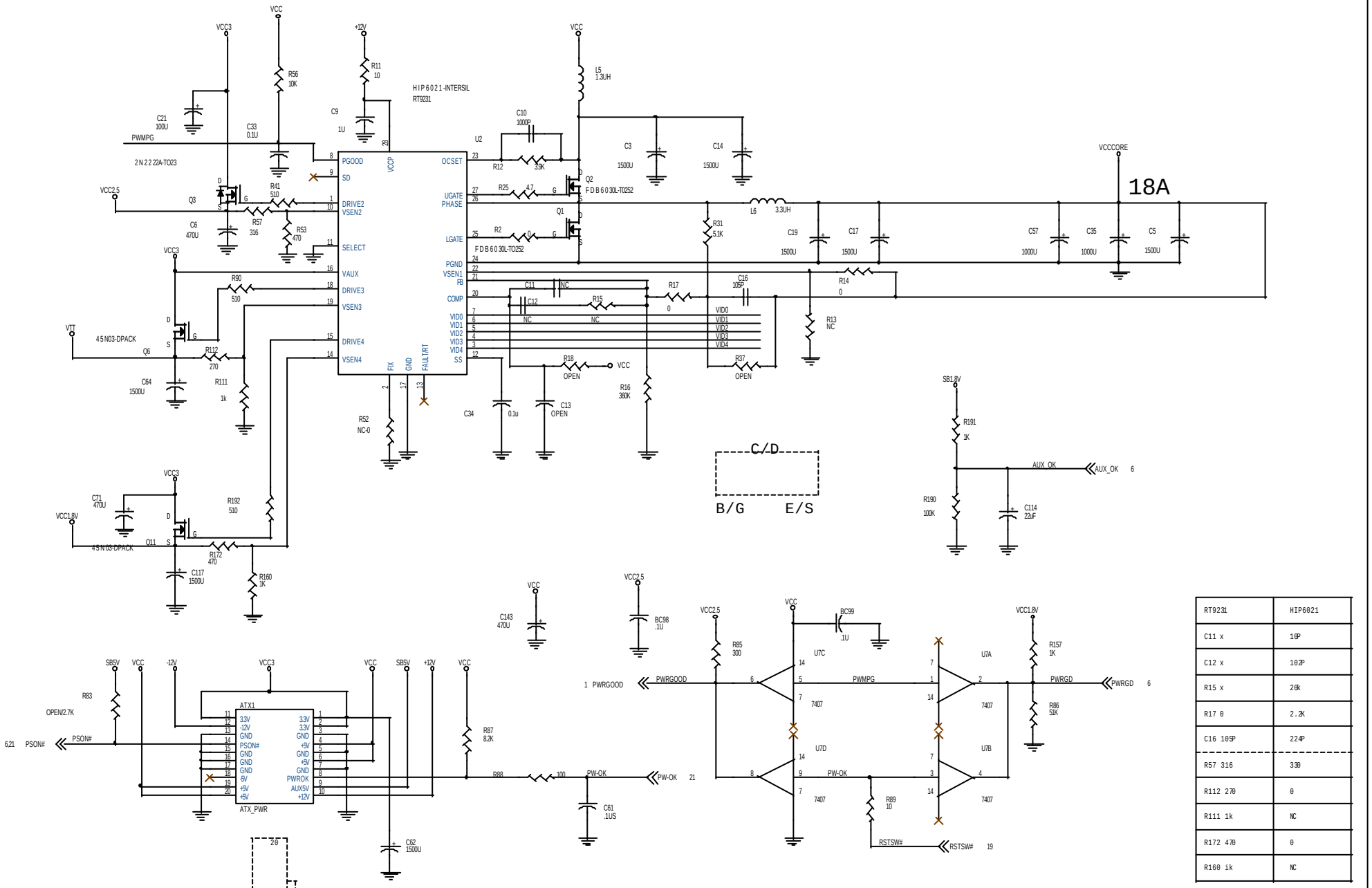
NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

JET WAY INFORMATION			
Title: NETWORK OPTION1			
Size: B	Document Number: J-630CF REV:3.0		Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 18 of 26		



NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

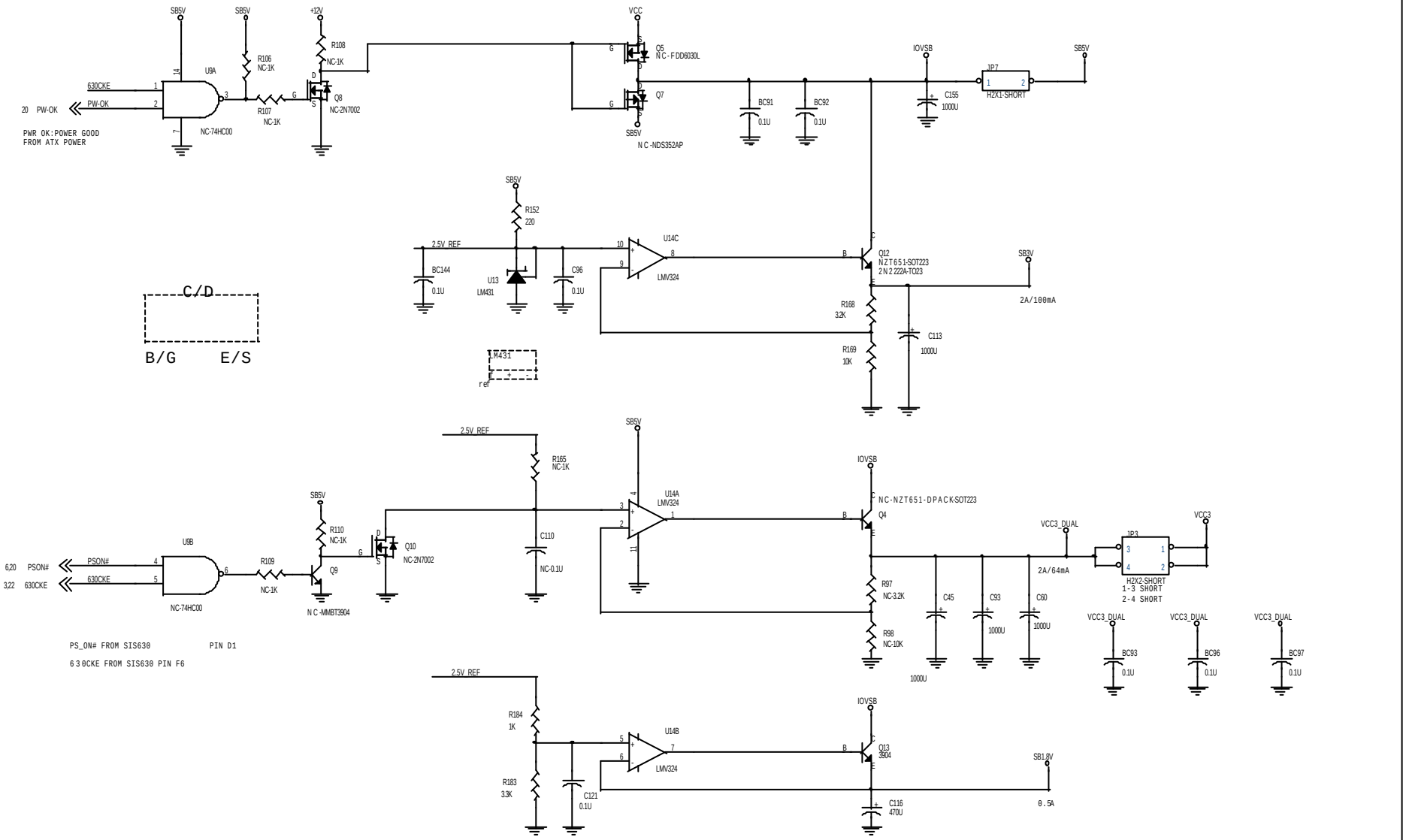
JETWAY INFORMATION		
Title: DATA ACQUISITION & JUMPERS		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 19 of 26	



RT9231	HIP6021
C11 x	10P
C12 x	102P
R15 x	20K
R17 0	2.2K
C16 105P	224P
R57 316	330
R112 270	0
R111 1k	NC
R172 470	0
R160 ik	NC

DET WAY INF ORMATION			
Title	HIP6021		
Size B	Document Number J-630CF REV:3.0		Rev 3.0
Date: Saturday, August 11, 2001		Sheet 20 of 26	

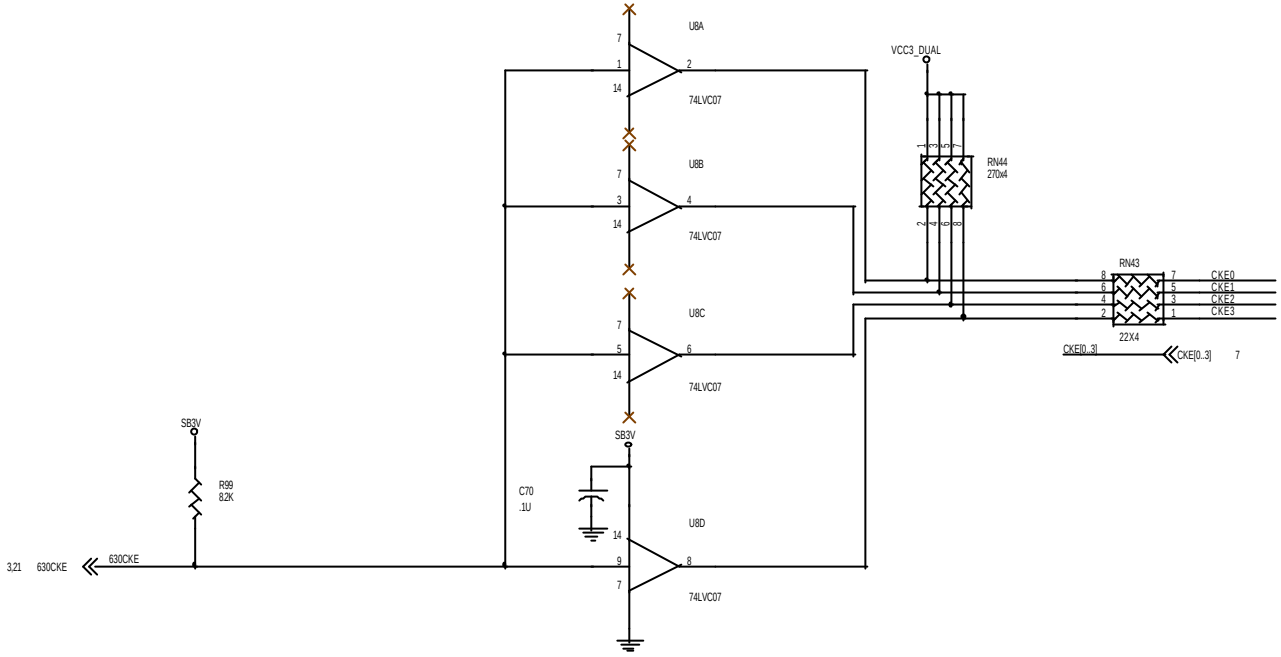
RC5058+Discrete ACPI FOR SIS630 - PAGE 2



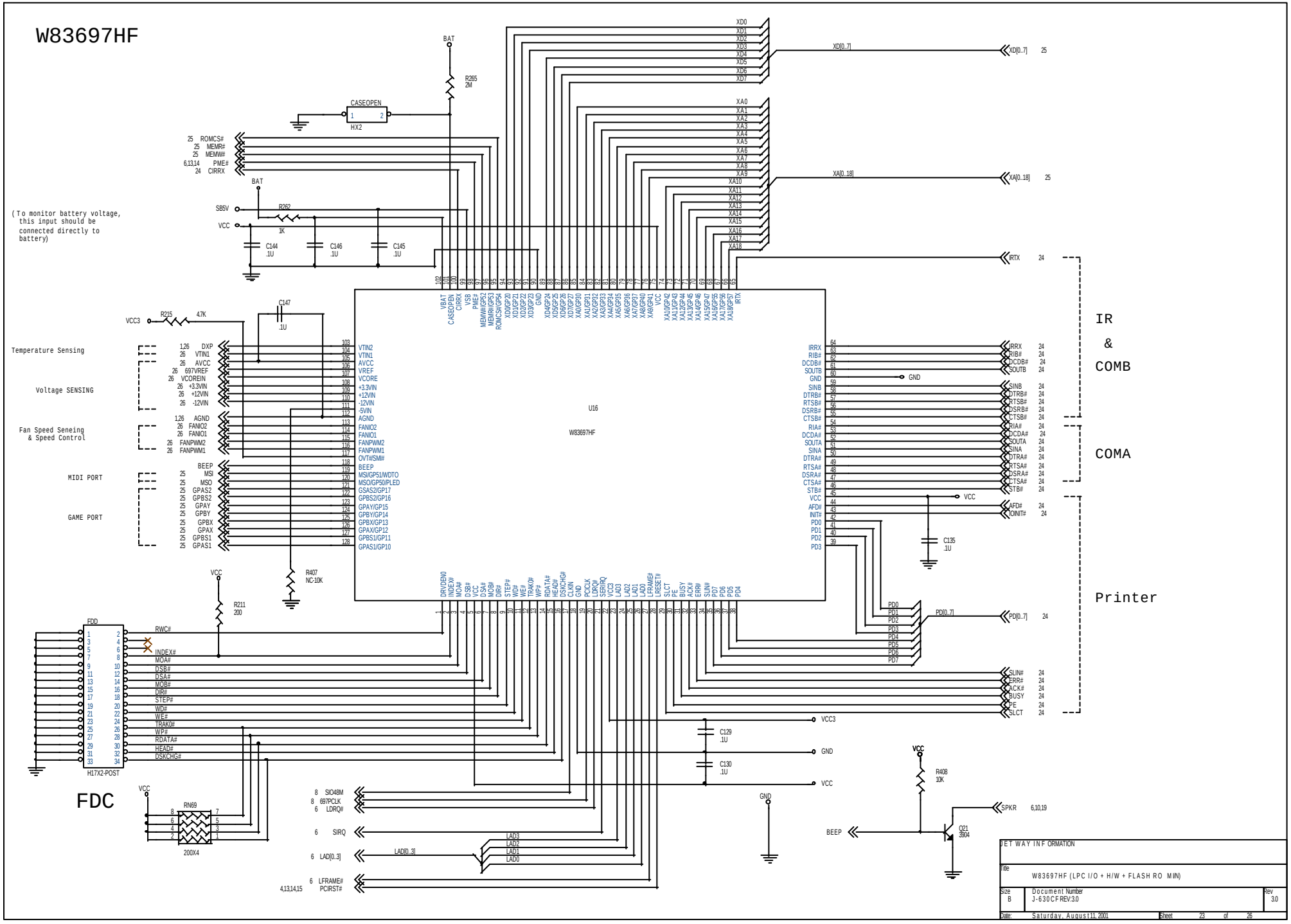
VCC and VCC3 Standby VOLTAGE SWITCH

WHEN IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

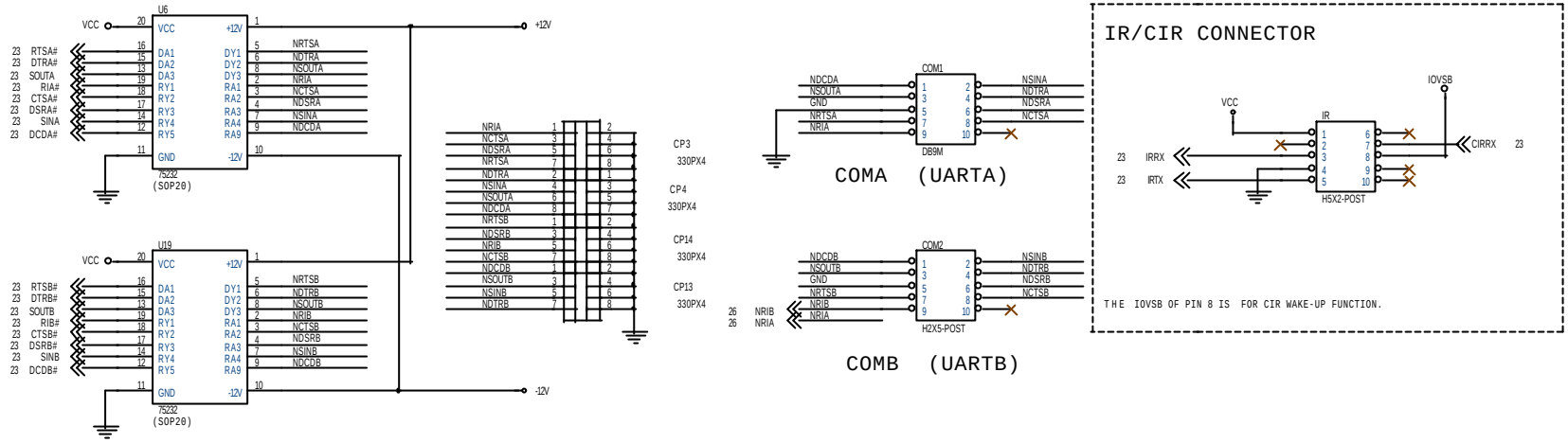
WHEN IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER



DET WAY IN FORMTION			
Title: VOLTAGE SWITCH FOR SUSPEN DTODRAM			
Size: B	Document Number: J-630CF REV:3.0		Rev: 3.0
Date: Saturday, August 11, 2001		Sheet 22 of 26	


W83697HF
BAT
R265
2M
CASEOPEN
HX2
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XD[0..7]
XD[0..7] 25
XA0
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XA8
XA9
XA10
XA11
XA12
XA13
XA14
XA15
XA16
XA17
XA18
XA[0..18]
XA[0..18] 25
25 ROMCS#
25 MEMR#
25 MEMW#
6,13,14 PME#
24 CIRRX
IRTX 24
SB5V
VCC
R262
1K
C144
.1U
C146
.1U
C145
.1U
(To monitor battery voltage, this input should be connected directly to battery)
VCC3
R215
4.7K
C147
.1U
Temperature Sensing
Voltage SENSING
Fan Speed Seneing & Speed Control
MIDI PORT
GAME PORT
1,26 DXP
26 VTIN1
26 AVCC
26 697VREF
26 VCOREIN
26 +3.3VIN
26 +12VIN
26 -12VIN
1,26 AGND
26 FANIO2
26 FANIO1
26 FANPWM2
26 FANPWM1
25 MSI
25 MSO
25 GPAS2
25 GPBS2
25 GPAY
25 GPBY
25 GPBX
25 GPAX
25 GPBS1
25 GPAS1
U16
W83697HF
VTIN2
VTIN1
AVCC
VREF
VCORE
+3.3VIN
+12VIN
-12VIN
-5VIN
AGND
FANIO2
FANIO1
FANPWM2
FANPWM1
OVT#/SMI#
BEEP
MSI/GP51/INDTO
MSO/GP50/IPLED
GSAS2/GP17
GPBS2/GP16
GPAY/GP15
GPBY/GP14
GPBX/GP13
GPAX/GP12
GPBS1/GP11
GPAS1/GP10
IRRX
RIB#
DCDB#
SOUTB
GND
SINB
DTRB#
RTSB#
DSRB#
CTSB#
RIA#
DCDA#
SOUTA
SINA
DTRA#
RTSA#
DSRA#
CTSA#
STB#
VCC
AFD#
INIT#
PD0
PD1
PD2
PD3
IR & COMB
COMA
Printer
C135
.1U
R407
NC-10K
R211
200
PD[0..7]
PD[0..7] 24
FDD
H17X2-POST
RWC#
INDEX#
MOA#
DSB#
DSA#
MOB#
DIR#
STEP#
WD#
WE#
TRAK0#
WP#
RDATA#
HEAD#
DSKCHG#
FDC
C129
.1U
C130
.1U
VCC3
GND
VCC
R408
10K
SPKR 6,10,19
BEEP
Q21
3904
RN69
200X4
8 SIO48M
8 697PCLK
6 LDRQ#
6 SIRQ
6 LAD[0..3]
LAD[0..3]
LAD3
LAD2
LAD1
LAD0
6 LFRAME#
4,13,14,15 PCIRST#
JET WAY INFORMATION
Title
W83697HF (LPC I/O + H/W + FLASH ROM)
Size B
Document Number J-630CF REV:3.0
Rev 3.0
Date: Saturday, August 11, 2001
Sheet 23 of 26

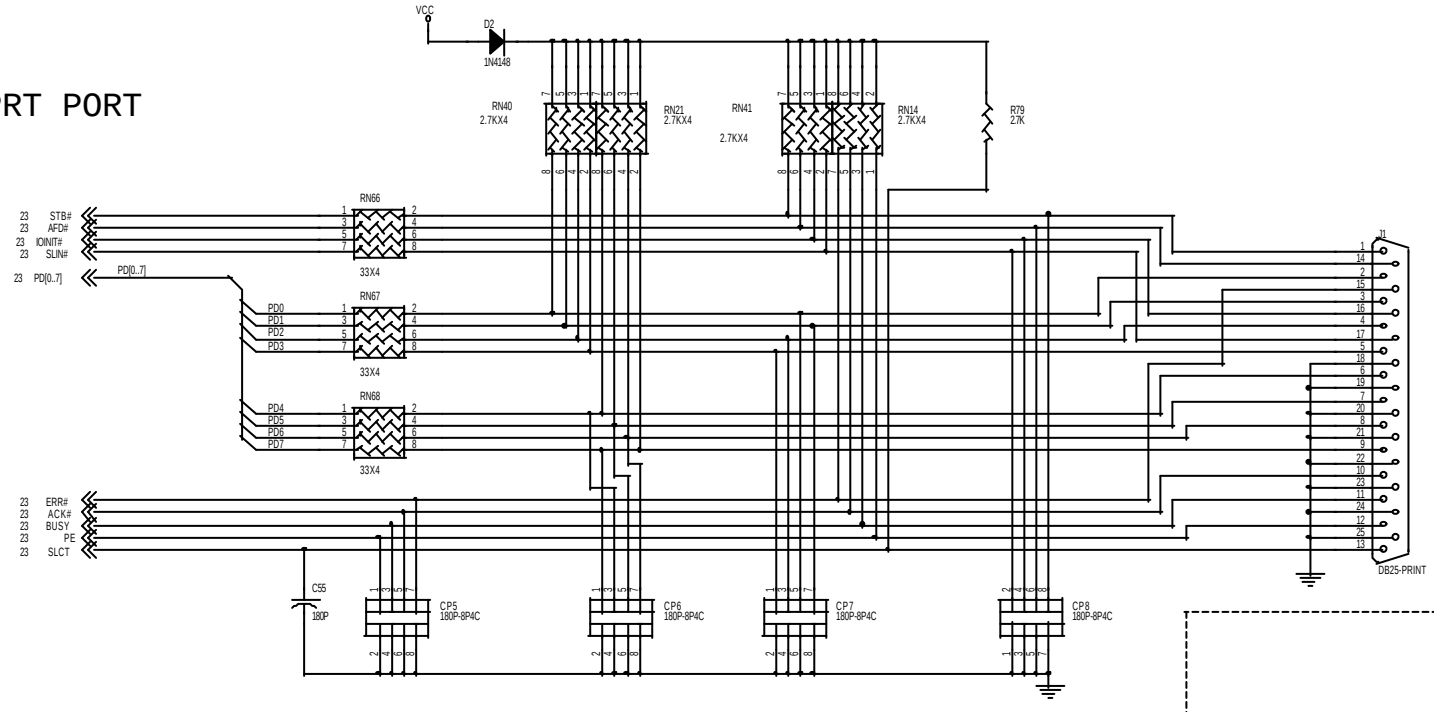
COM PORT



IR/CIR CONNECTOR

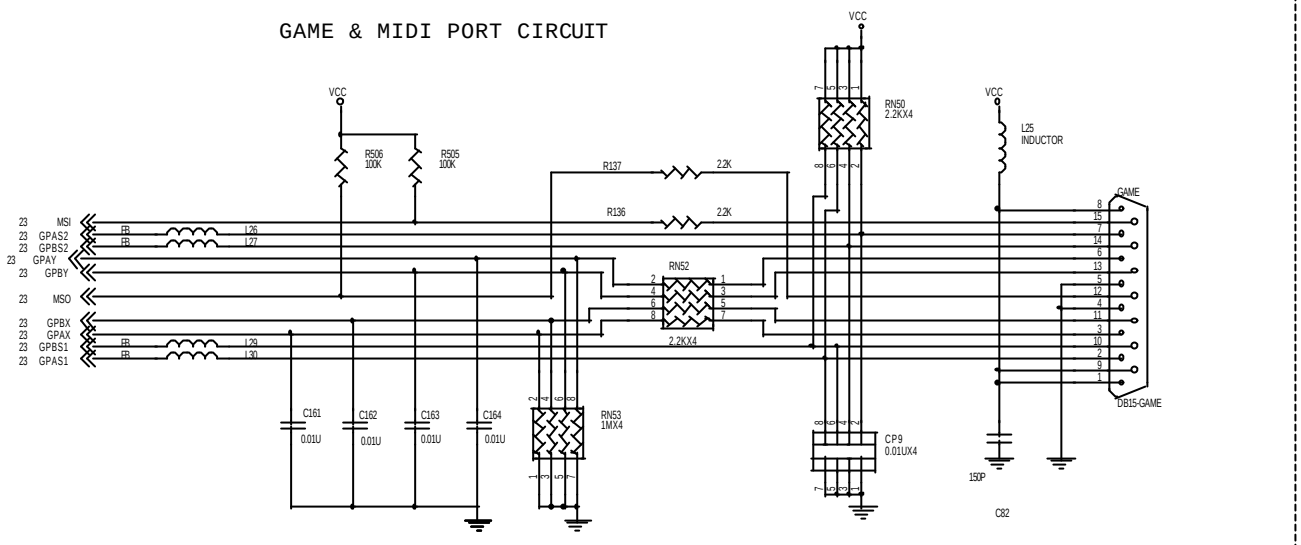
THE IOVSB OF PIN 8 IS FOR CIR WAKE-UP FUNCTION.

PRT PORT

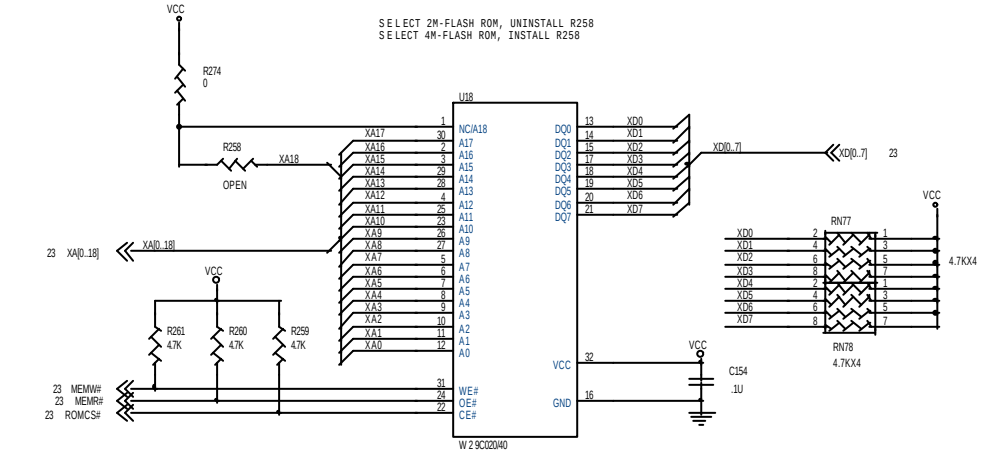


JET WAY INFORMATION		
Title	W83697HF (LPC I/O + H/W + FLASH ROM)	
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 24 of 26	

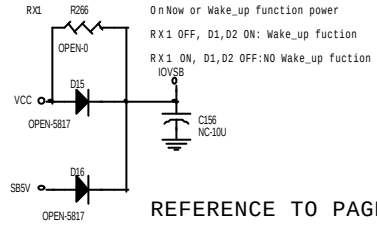
GAME & MIDI PORT CIRCUIT



FLASH ROM



IOVSB CIRCUIT

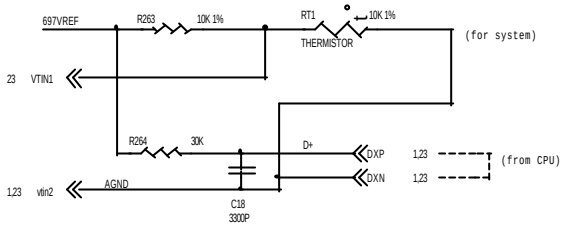


REFERENCE TO PAGE 21

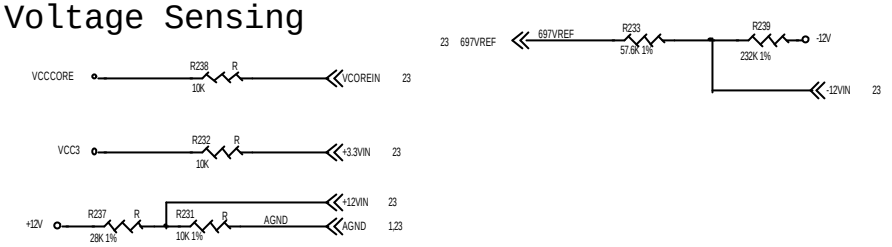
DETWAY INFORMATION		
Title: W83697HF (LPC I/O + H/W + FLASH ROM)		
Size: B	Document Number: J-630CF REV:3.0	Rev: 3.0
Date: Saturday, August 11, 2001	Sheet 25 of 26	

Hardware Monitor circuits

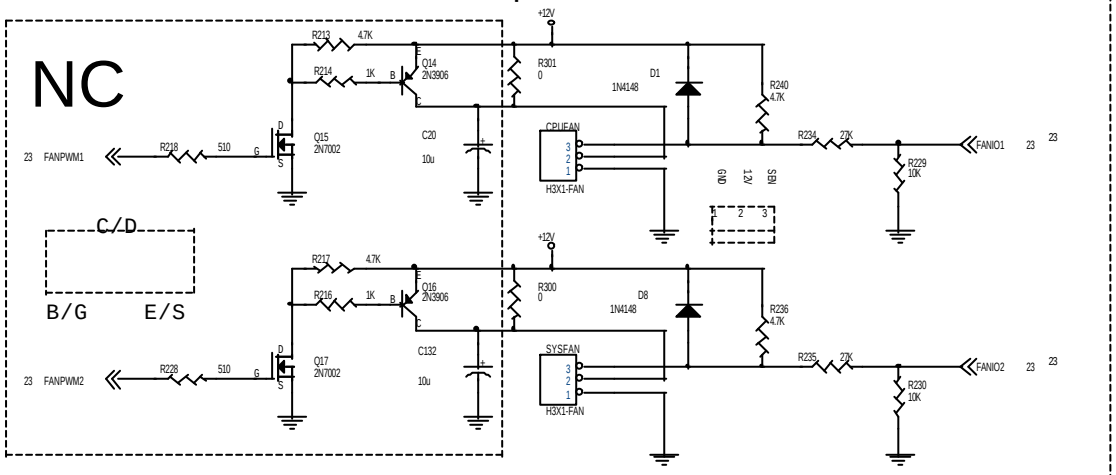
Temperature Sensing

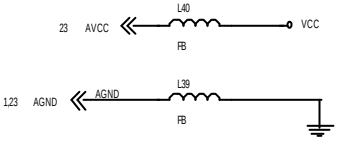


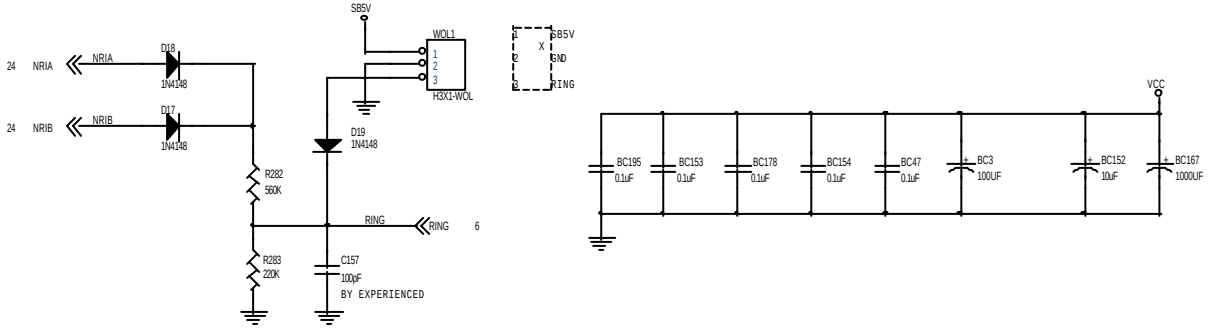
Voltage Sensing



PWM Circuit for FAN speed control







DET WAY INF ORMATION		
Title	W83697HF (LPC I/O+ H/W + FLASH RO M/F)	
Size B	Document Number J-630CF REV:3.0	Rev 3.0
Date: Saturday, August 11, 2001	Sheet 26 of 26	