

N-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME2306 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology.

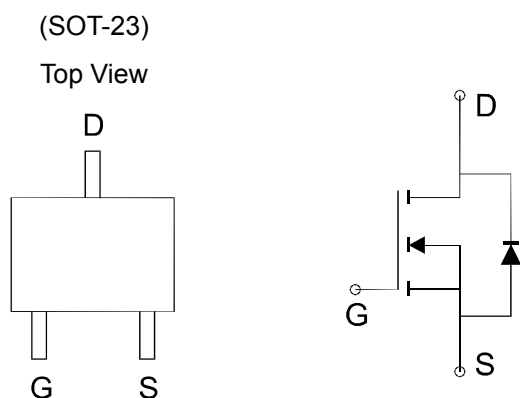
This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 37m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 49m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Ordering Information: ME2306 (Pb-free)

ME2306-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Steady State		Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current (Tj=150°C)	TA=25°C	I_D	4.7		A
	TA=70°C		3.7		
Pulsed Drain Current		I_{DM}	20		
Maximum Power Dissipation	TA=25°C	P_D	1.32		W
	TA=70°C		0.84		
Operating Junction Temperature		T_J	-55 to 150		°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T ≤ 10 sec	70	°C/W
			Steady State	95	
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	65		°C/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A = 25°C Unless Otherwise Specified)

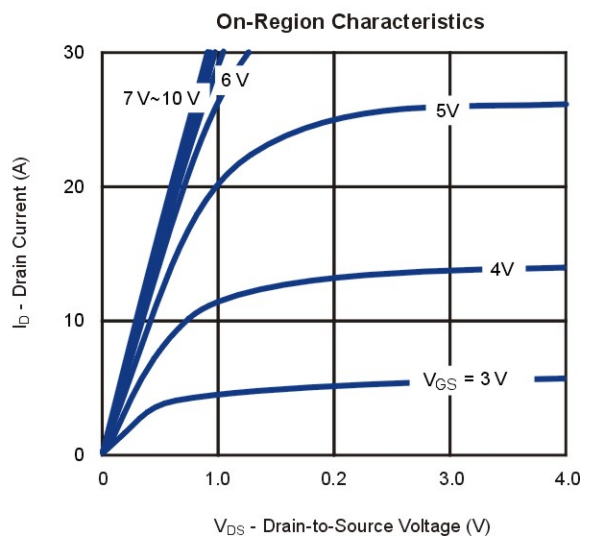
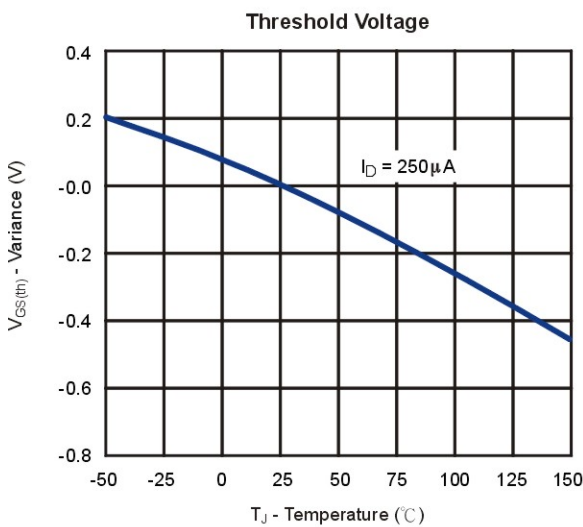
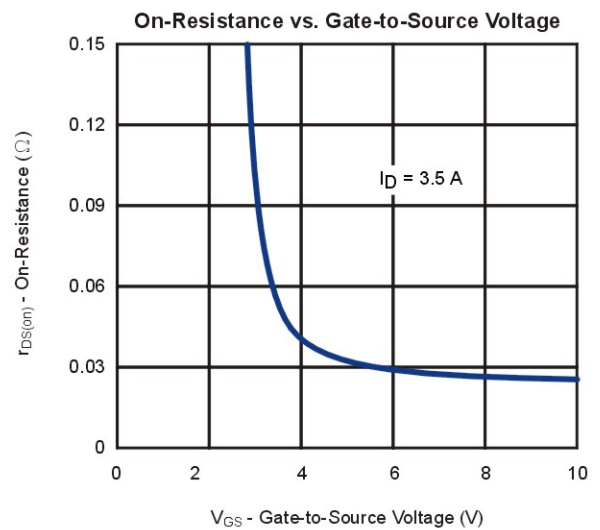
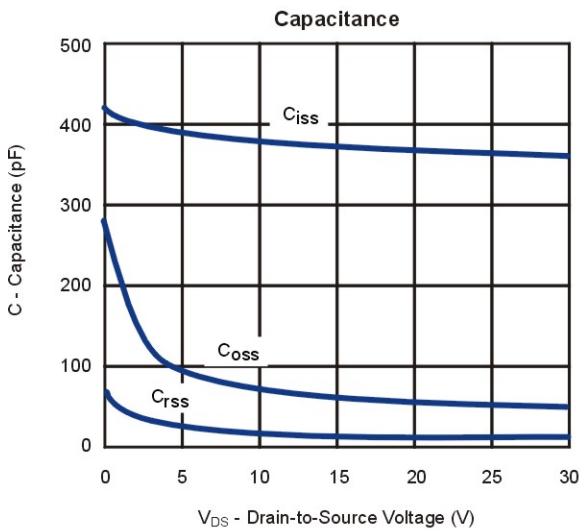
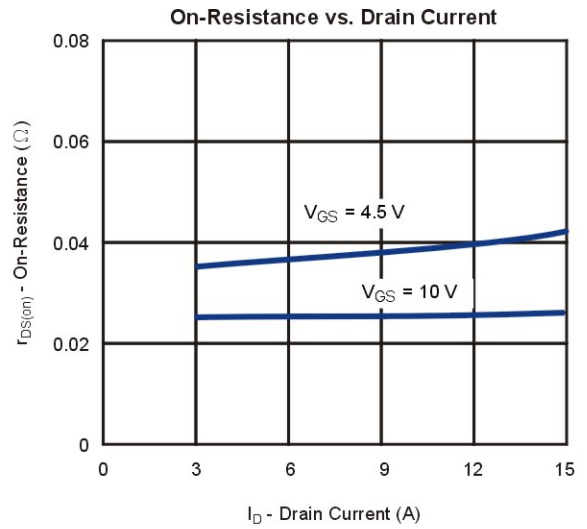
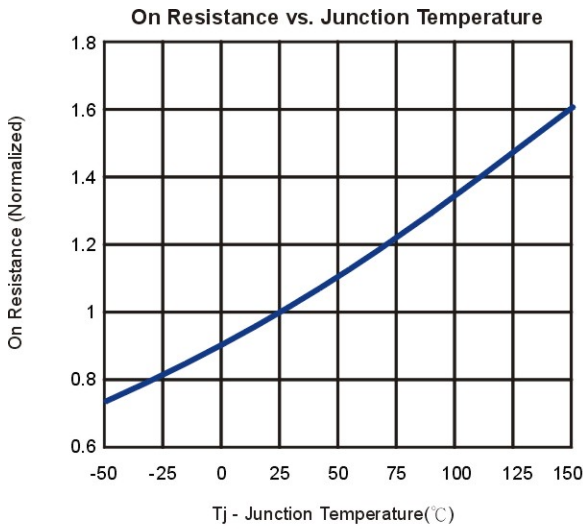
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC PARAMETERS						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	
I _{GSS}	Gate-Body Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
		V _{DS} =30V, V _{GS} =0V			10	
		T _J =55°C				
I _{D(ON)}	On-State Drain Current ^a	V _{DS} ≥ 5V, V _{GS} = 10V	20			A
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 4A		25	37	mΩ
		V _{GS} =4.5V, I _D = 3.5A		35	49	
V _{SD}	Diode Forward Voltage	I _S =1.25A, V _{GS} =0V		0.8	1.2	V
DYNAMIC PARAMETERS						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =4A		13		nC
Q _g	Total Gate Charge			6.3		
Q _{gs}	Gate-Source Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =4A		2.9		
Q _{gd}	Gate-Drain Charge			2.4		
R _g	Gate Resistance	f = 1MHz		0.6		Ω
C _{iss}	Input Capacitance			380		pF
C _{oss}	Output Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		64		
C _{rss}	Reverse Transfer Capacitance			15		
t _{d(on)}	Turn-On Delay Time			9		ns
t _r	Rise Time	V _{DD} =15V, R _L = 15Ω		14		
t _{d(off)}	Turn-Off Delay Time	I _D =1A, V _{GEN} =10V, R _G =6Ω		33		
t _f	Fall Time			3		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

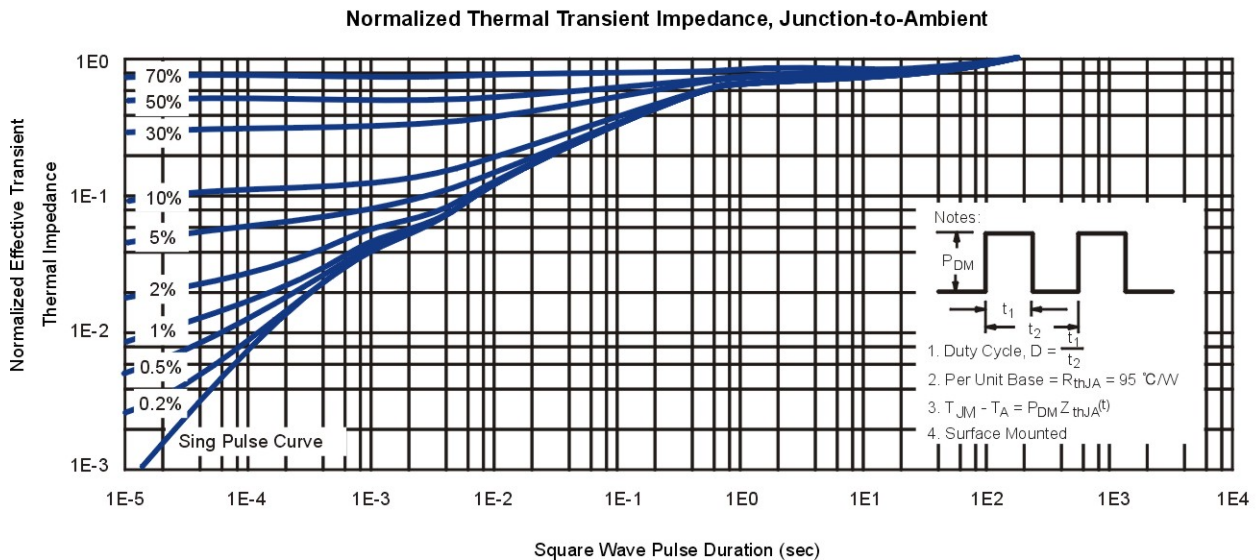
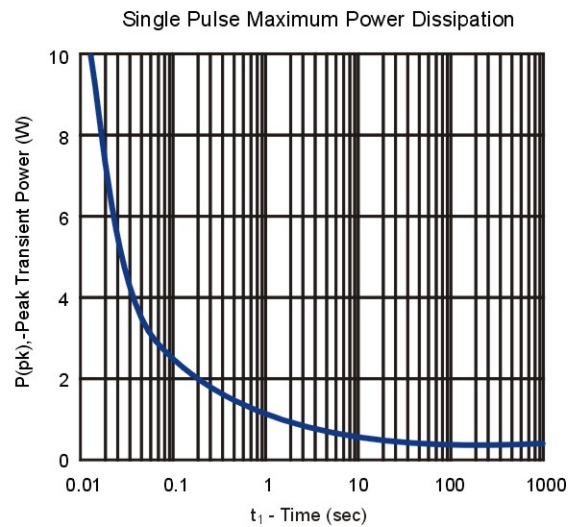
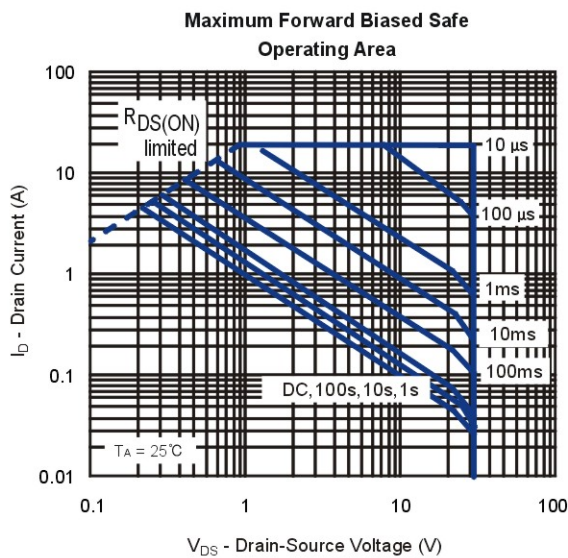
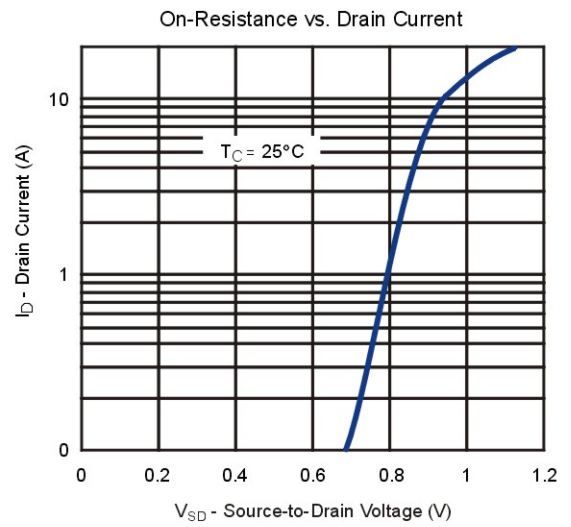
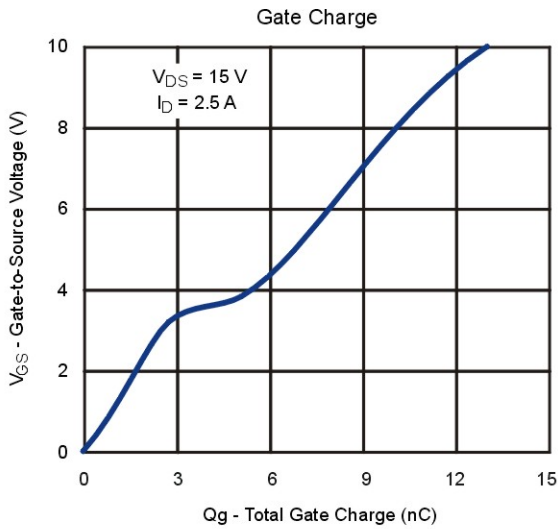
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Typical Characteristics (T_J = 25°C Noted)

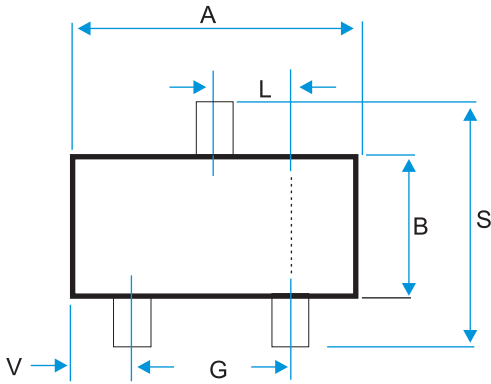


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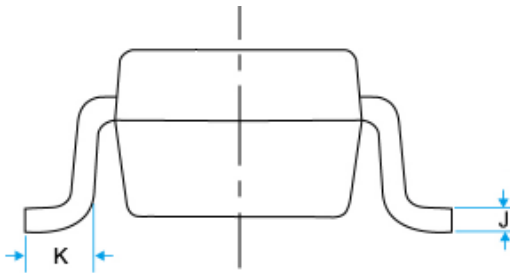
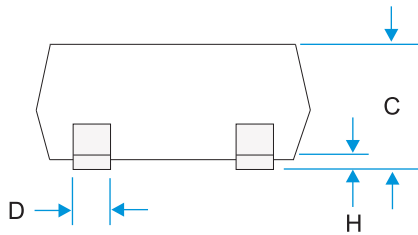
Typical Characteristics (T_J = 25°C Noted)



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60



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