# TECHNICAL MANUAL

HARRIS

COMMUNICATIONS AND INFORMATION HANDLING

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# SERVICE BULLETIN
## MAINTENANCE AND MODIFICATION DATA
### Broadcast Products Division

**Equipment:** MS-15 Exciter

**Bulletin No.** FM-144-RFB

**Date** February, 1980

Subject: MS-15 Exciter Spare Parts Lists

This Service Bulletin (FM-144-RFB) was generated to outline some spare parts and assemblies to support your MS-15 Exciter. The list on page one contains Transistors, Integrated Circuits, Diodes and a few other items to be used in resolving general maintenance as well as emergency needs. This list contains original equipment parts or engineering approved substitutes that exhibit the same characteristics as the original parts supplied. The regular and optional subassemblies we stock, sell and exchange for the MS-15 Exciter are listed on page two, along with the recommended semiconductor kits for the optional subassemblies. We will be happy to provide spares lists for other Harris products upon request.

To minimize difficulty in obtaining proven parts expeditiously, you may want to stock a complete list of spare parts (994-8130-001) at $402.55 or semiconductors only (990-0917-001) at $236.75 or you may decide to select specific items that you feel you may need in the future. In any case, the prices are valid until May 30, 1980.

If you decide to order specific parts or an entire list, just call 217-222-8200, telex 404347, TWX 910-246-3212 (domestic only), or write to Service Parts at your convenience. Our Service Group is open twenty-four hours every day to help satisfy your needs on our products. If a technical specialist you require is not on duty at the time you contact us, one can be readily located in order to resolve emergency technical problems.

If you require additional copies of this bulletin or further information, please contact the Service Parts Department at your convenience.

Sincerely,

Robert F Buck

Robert F. Buck, Manager
Service Parts Department

# RECOMMENDED SPARE PARTS KIT FOR MS15 50/60 HZ - 994-8130-001

| | PART NUMBER | DESCRIPTION | QTY | EXT. SELL |
|---|---|---|---|---|
| * | 380-0116-000 | Transistor 2N3866 | 2 | 6.60 |
| * | 380-0126-000 | Transistor 2N4403 | 1 | .45 |
| * | 380-0187-000 | Transistor 2N6055 | 2 | 6.50 |
| * | 380-0189-000 | Transistor 2N3904 | 2 | .70 |
| * | 380-0190-000 | Transistor 2N3906 | 1 | .35 |
| * | 380-0319-000 | Transistor MPS A14 | 2 | 1.20 |
| * | 380-0421-000 | Transistor 2N4258 | 1 | .60 |
| * | 380-0536-000 | Transistor 2N5179 | 2 | 3.30 |
| * | 380-0556-000 | Transistor B-3-28 | 1 | 23.25 |
| * | 380-0557-000 | Transistor B-25-28 | 1 | 41.05 |
| * | 380-0570-000 | Transistor MFE 131 | 2 | 4.30 |
| * | 380-0571-000 | Transistor | 1 | 2.95 |
| * | 382-0034-000 | IC SN7493AN TI Only | 1 | 1.20 |
| * | 382-0082-000 | Integrated Ckt | 1 | .85 |
| * | 382-0121-000 | Integrated Ckt | 2 | 1.20 |
| * | 382-0148-000 | Integrated Ckt | 1 | 1.30 |
| * | 382-0162-000 | Integrated Ckt | 2 | 3.10 |
| * | 382-0174-000 | Integrated Ckt | 1 | 5.50 |
| * | 382-0359-000 | Ckt Int MC7815CT | 2 | 4.50 |
| * | 382-0360-000 | Ckt Int MC7915CT | 2 | 6.00 |
| * | 382-0415-000 | Ckt Integrated | 2 | 4.30 |
| * | 382-0428-000 | Ckt Integrated | 2 | 2.40 |
| * | 382-0472-000 | Ckt Integrated | 2 | 4.40 |
| * | 382-0523-000 | Ckt Integrated CMOS | 2 | 1.70 |
| * | 382-0527-000 | IC Regulator | 1 | 7.80 |
| * | 382-0532-000 | Ckt Integrated | 2 | 2.30 |
| * | 382-0541-000 | Ckt Integrated | 1 | 11.75 |
| * | 384-0020-000 | Rectifier IN4005 | 2 | .80 |
| * | 384-0205-000 | Diode Silicon 1N914 | 3 | .75 |
| * | 384-0284-000 | Diode 10D4/1N2070 | 2 | 1.80 |
| * | 384-0321-000 | Diode, Hot Carrier | 4 | 10.40 |
| * | 384-0431-000 | Rect. 1N4001 | 4 | 1.00 |
| * | 384-0564-000 | Rect., Bridge 6A 600 | 2 | 39.30 |
| * | 384-0610-000 | Led, Green | 2 | 4.70 |
| * | 384-0661-000 | L. E. D. Green | 2 | 3.00 |
| * | 384-0664-000 | L. E. D. Yellow | 1 | 1.95 |
| * | 386-0077-000 | Diode Zener 1N4749A | 2 | 1.50 |
| * | 386-0092-000 | Diode Zener 1N4744 | 1 | .45 |
| * | 386-0366-000 | Diode, Zener 1N5359A | 1 | 1.70 |
| * | 386-0391-000 | Diode Zener 1N2821A | 1 | 19.85 |
| | 398-0020-000 | Fuse 3AG Fast 3A 250 | 5 | 2.00 |
| | 430-0098-000 | Fan, Tubeaxial | 1 | 101.00 |
| | 464-0026-000 | Tool, Alignment 5284 | 1 | 4.80 |
| | 574-0162-000 | Relay 4PDT 24 VDC | 1 | 14.55 |
| | 606-0547-000 | Circuit Breaker 2A | 1 | 43.45 |
| | | | TOTAL | 402.55 |

* - Starred items make up our recommended semi-conductor kit (990-0917-001) that sells for $236.75.

The Modules or subassemblies we stock, sell, and exchange for the MS-15 exciter and its' options are listed below for your convenience. New units have a zero (0) in the eighth digit of the part number while reconditioned units have a nine (9) in the eighth digit. The reconditioned units sell for eighty percent of the new unit list price and are usually available, but we do not accept back orders for reconditioned units. This is due to the unpredictable lead time to obtain one, since we have no way of knowing when a defective one will be returned to us from a previous transaction. Some customers pay for these exchange units and keep them as spares, after repairs. The Modules are:

| PART NUMBER | DESCRIPTION | PRICE |
|---|---|---|
| 992-4978-001 | RF Power Amplifier | $ 814.00 |
| 992-4981-001 | DC Metering Board | 113.00 |
| 992-4982-001 | AC Metering Board | 414.00 |
| 992-4985-001 | Auto Freq. Control | 653.00 |
| 992-4987-001 | Mod. Oscillator | 620.00 |
| 992-5000-001 | Power Supply Board | 91.20 |
| 994-7992-001 | *SCA Gen. (Optional) | 1,075.00 |
| 994-8019-001 | *Mon Aural Module (Optional) | 1,200.00 |
| 994-8020-001 | *Stereo Gen. (Optional) | 3,600.00 |

If you have any of the three options (*) listed above in your MS-15 Exciter, you may also want to purchase spare semiconductors for them as some of the semiconductors in these options are not included in the regular MS-15 Kits. The recommended semiconductors for the MS-15 options are:

| PART NUMBER | DESCRIPTION | PRICE |
|---|---|---|
| 990-0919-001 | Recommended Semiconductor Kit for Stereo Gen | 129.50 |
| 990-0921-001 | Recommended Semiconductor Kit for SCA | 58.75 |
| 990-0923-001 | Recommended Semiconductor Kit for Monaural | 44.75 |

If you prefer to select additional semiconductors to stock from any of the above lists, we will send you priced breakdowns of any lists you desire upon request.

HARRIS COMMUNICATIONS AND INFORMATION HANDLING

HARRIS CORPORATION Broadcast Products Division
123 Hampshire Street, Quincy, Illinois 62301

# MANUAL CHANGE NOTICE

PUBLICATION NO. 888 1742 001

PUBLICATION DATE June 1977 REVISED June 1979

ITEM MS-15 FM Exciter MODEL 994 7950 001 SERIAL _____

INSTRUCTIONS: Note indicated changes to manual.
File CHANGE NOTICE in front of manual.

| CHANGE NO. | DATE | AUTHORITY | REASON |
|---|---|---|---|
| 1. | 8/17/79 | ENGINEER REQUEST | 1a. Replace Page 5-7. (New Copy Attached) |

5-34. Once the trouble is isolated to a specific area, refer to the theory section of this manual for circuit discussion to aid in problem resolution. Table 5-1 lists typical trouble symptoms pertaining to the overall exciter operation with references to fault isolation diagrams listing probable causes and corrective actions. A corrective action given for a trouble symptom is not necessarily the only answer to a problem, it only tends to lead the repairman into the area that may be causing the trouble. If a particular MS-15 module is determined faulty, a reference to the individual module maintenance publication will be listed. In event parts are required, refer to Section VI, Parts List.

5-35. COMPONENT REPLACEMENT. The circuit boards used in the MS-15 are of the double-sided plated-through type. This means that there are traces on both sides of the board and the through-holes contain a metallic plating. Because of the plated-through holes, solder creeps up into the hole. This requires a more sophisticated technique for component removal in order to avoid damage to the traces on the board. Excessive heat of any point on the board will cause damage.

5-36. To remove a component from a double-sided board, the leads of the defective component should be cut from the body while the leads are still soldered to the board. The component is then discarded and each lead is heated independently and pulled out of the hole. Each hole may then be cleared of solder by carefully heating with a low wattage iron and removing the residual solder with a solder vacuum tool.

5-37. The new component is installed in the usual way and soldered from the bottom side of the board. If no damage has been done to the plated-through hole, soldering of the top side is not required. However, if the removal procedure did not progress smoothly, each lead should be soldered at the top side to prevent potential intermittent problems.

5-18. After soldering remove residual flux. There are solvents available in electronic supply houses which are useful. The board should then be checked to ensure the defluxing operation has removed the flux and not just smeared it about so that it is less visible. While rosin flux is not normally corrosive, it will absorb moisture and become conductive enough to cause deterioration in specifications over a period of time.

5-39. TECHNICAL ASSISTANCE.

5-40. Technical assistance and troubleshooting recommendations are available from Harris Field Service Department during normal working hours. Emergency technical service is available 24 hours a day. Telephone 217/222-8200 to contact the Field Service Department or address correspondence to Field Service Department, Harris Corporation Broadcast Products Division, 123 Hampshire Street, Quincy, Illinois 62301, USA.

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Table 5-1. MS-15 Fault Isolation Index

| SYMPTOM | DEFECT/REFERENCE |
|---|---|
| NO RF CARRIER OUTPUT | Figure 5-1 |
| RF CARRIER LEVEL WILL NOT ADJUST | Defective RF AMP. module. Refer to publication 888 1742 009. |
| INADEQUATE CARRIER LEVEL OUTPUT | Figure 5-2 |
| FREQUENCY CONTROL CIRCUIT WILL NOT LOCK (AFC/PLL MODULE LOCK INDICATOR NOT ILLUMINATED). | Figure 5-3 |
| EXCITER OFF FREQUENCY (AFC/PLL MODULE LOCK INDICATOR ILLUMINATED). | Defective AFC/PLL module. Refer to publication 888 1742 007. |
| HIGH AUDIO DISTORTION IN BOTH STEREO CHANNELS | Figure 5-4 |
| HIGH AUDIO DISTORTION IN ONE STEREO CHANNEL | Defective STEREO ANALOG module. Refer to publication 888 1742 005. |
| NOISY AUDIO | Figure 5-5 |
| AM NOISE ON RF CARRIER | Figure 5-6 |
| NO MODULATION | Figure 5-7 |
| CIRCUIT BREAKER CB-1 OPENS | Figure 5-8 |

# TECHNICAL MANUAL

MS-15 FM EXCITER

994 7950 001

HARRIS CORPORATION

Broadcast Products Division

T.M. No. 888 1742 001

Printed: June 1977
Rev. A: December 1977
Rev. B: March 1979
Rev. C: June 1979
Rev. D: April 1980
Rev. E: March 1981

WARNING

THE CURRENTS AND VOLTAGES IN THIS EQUIPMENT ARE DANGEROUS. PERSONNEL MUST AT ALL TIMES OBSERVE SAFETY REGULATIONS.

This manual is intended as a general guide for trained and qualified personnel who are aware of the dangers inherent in handling potentially hazardous electrical/electronic circuits. It is not intended to contain a complete statement of all safety precautions which should be observed by personnel in using this or other electronic equipment.

The installation, operation, maintenance and service of this equipment involves risks both to personnel and equipment, and must be performed only by qualified personnel exercising due care. HARRIS CORPORATION shall not be responsible for injury or damage resulting from improper procedures or from the use of improperly trained or inexperienced personnel performing such tasks.

WARNING

ALWAYS DISCONNECT POWER BEFORE OPENING COVERS, DOORS, ENCLOSURES, GATES, PANELS OR SHIELDS. ALWAYS USE GROUNDING STICKS AND SHORT OUT HIGH VOLTAGE POINTS BEFORE SERVICING. NEVER MAKE INTERNAL ADJUSTMENTS, PERFORM MAINTENANCE OR SERVICE WHEN ALONE OR WHEN FATIGUED.

Do not remove, short-circuit or tamper with interlock switches on access covers, doors, enclosures, gates, panels or shields. Keep away from live circuits, know your equipment and don't take chances.

FIRST-AID

Personnel engaged in the installation, operation, maintenance or servicing of this equipment are urged to become familiar with first-aid theory and practices. The following information is not intended to be complete first-aid procedures, it is brief and is only to be used as a reference. It is the duty of all personnel using the equipment to be prepared to give adequate Emergency First Aid and thereby prevent avoidable loss of life.

WARNING

IN CASE OF EMERGENCY ENSURE THAT POWER HAS BEEN DISCONNECTED.

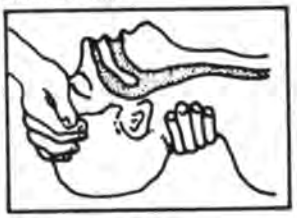
## Treatment of Electrical Shock

1. If victim is not responsive follow the A-B-Cs of basic life support.

PLACE VICTIM FLAT ON HIS BACK ON A HARD SURFACE

### (A) AIRWAY

IF UNCONSCIOUS,
OPEN AIRWAY



LIFT UP NECK
PUSH FOREHEAD BACK
CLEAR OUT MOUTH IF NECESSARY
OBSERVE FOR BREATHING

### (B) BREATHING

IF NOT BREATHING,
BEGIN ARTIFICIAL
BREATHING

TILT HEAD
PINCH NOSTRILS
MAKE AIRTIGHT SEAL

4 QUICK FULL BREATHS

REMEMBER MOUTH TO MOUTH RESUSCITATION
MUST BE COMMENCED AS SOON AS POSSIBLE

CHECK CAROTID PULSE

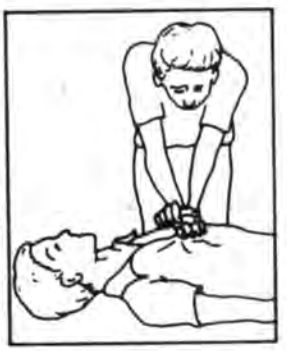
IF PULSE ABSENT,
BEGIN ARTIFICIAL
CIRCULATION

### (C) CIRCULATION

DEPRESS STERNUM 1 1/2" TO 2"


APPROX. 80 SEC. { ONE RESCUER, 15 COMPRESSIONS, 2 QUICK BREATHS

APPROX. 60 SEC. { TWO RESCUERS, 5 COMPRESSIONS, 1 BREATH



NOTE: DO NOT INTERRUPT RHYTHM OF COMPRESSIONS
WHEN SECOND PERSON IS GIVING BREATH

Call for medical assistance as soon as possible.

2. If victim is responsive.

   a. keep them warm
   b. keep them as quiet as possible
   c. loosen their clothing
      (a reclining position is recommended)

Treatment of Electrical Burns

1. Extensive burned and broken skin

   a. Cover area with clean sheet or cloth. (Cleanest available cloth article.)
   b. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply any salve or ointment.
   c. Treat victim for shock as required.
   d. Arrange transportation to a hospital as quickly as possible.
   e. If arms or legs are affected keep them elevated.

NOTE

If medical help will not be available within an hour and the victim is conscious and not vomiting, give him a weak solution of salt and soda: 1 level teaspoonful of salt and 1/2 level teaspoonful of baking soda to each quart of water (neither hot or cold). Allow victim to sip slowly about 4 ounces (a half of glass) over a period of 15 minutes. Discontinue fluid if vomiting occurs. (Do not give alcohol.)

2. Less severe burns - (1st & 2nd degree)

   a. Apply cool (not ice cold) compresses using the cleanest available cloth article.
   b. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply salve or ointment.
   c. Apply clean dry dressing if necessary.
   d. Treat victim for shock as required.
   e. Arrange transportation to a hospital as quickly as possible.
   f. If arms or legs are affected keep them elevated.

REFERENCE: ILLINOIS HEART ASSOCIATION

AMERICAN RED CROSS STANDARD FIRST AID AND PERSONAL SAFETY MANUAL (SECOND EDITION)

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WARNING: Disconnect primary power prior to servicing.

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WARNING: Disconnect primary power prior to servicing.

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WARNING: Disconnect primary power prior to servicing.

# SECTION I

## GENERAL DESCRIPTION

1-1. INTRODUCTION.

1-2. This technical manual contains information necessary to install, operate, maintain, and service the MS-15 FM Exciter. Sections in this technical manual provide the following information:

a. SECTION I, GENERAL DESCRIPTION, provides a description of equipment features, identifies major components, and lists operating parameters and specifications.

b. SECTION II, INSTALLATION, provides unpacking, inspection, and installation information, preoperational checks, and power on checks to ensure correct operation.

c. SECTION III, OPERATION, identifies controls and indicators and provides equipment setup and operation.

d. SECTION IV, PRINCIPLES OF OPERATION, provides a functional description and detailed block diagram with theory of operation.

e. SECTION V, MAINTENANCE, provides preventive and corrective maintenance information and troubleshooting with instructions for equipment servicing.

f. SECTION VI, PARTS LIST, provides information for ordering replacement components and assemblies.

g. SECTION VII, DIAGRAMS, provides block, logic, schematic diagrams, and other drawings required for equipment maintenance.

1-3. EQUIPMENT PURPOSE.

1-4. The Harris MS-15 FM exciter (figure 1-1) produces a 15 watt maximum frequency modulated signal into a 50 ohm load on any channel in the 87.5 MHz to 108 MHz commercial FM broadcast band. Operational modes include up to two SCA channels, monophonic, stereophonic, and provisions for quadraphonic transmission.

1-5. PHYSICAL DESCRIPTION.

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1-6. The MS-15 exciter is both electrically and mechanically modular in concept. Each discrete function is implemented within individual plug-in modules. Each module is provided with an insertion/extraction lever to aid in module servicing. All modules are placarded with nomenclature to prevent use in the incorrect slot. A hinged front panel drops down to access the chassis mounted and non-modular components such as the input and





WARNING: Disconnect primary power prior to servicing.

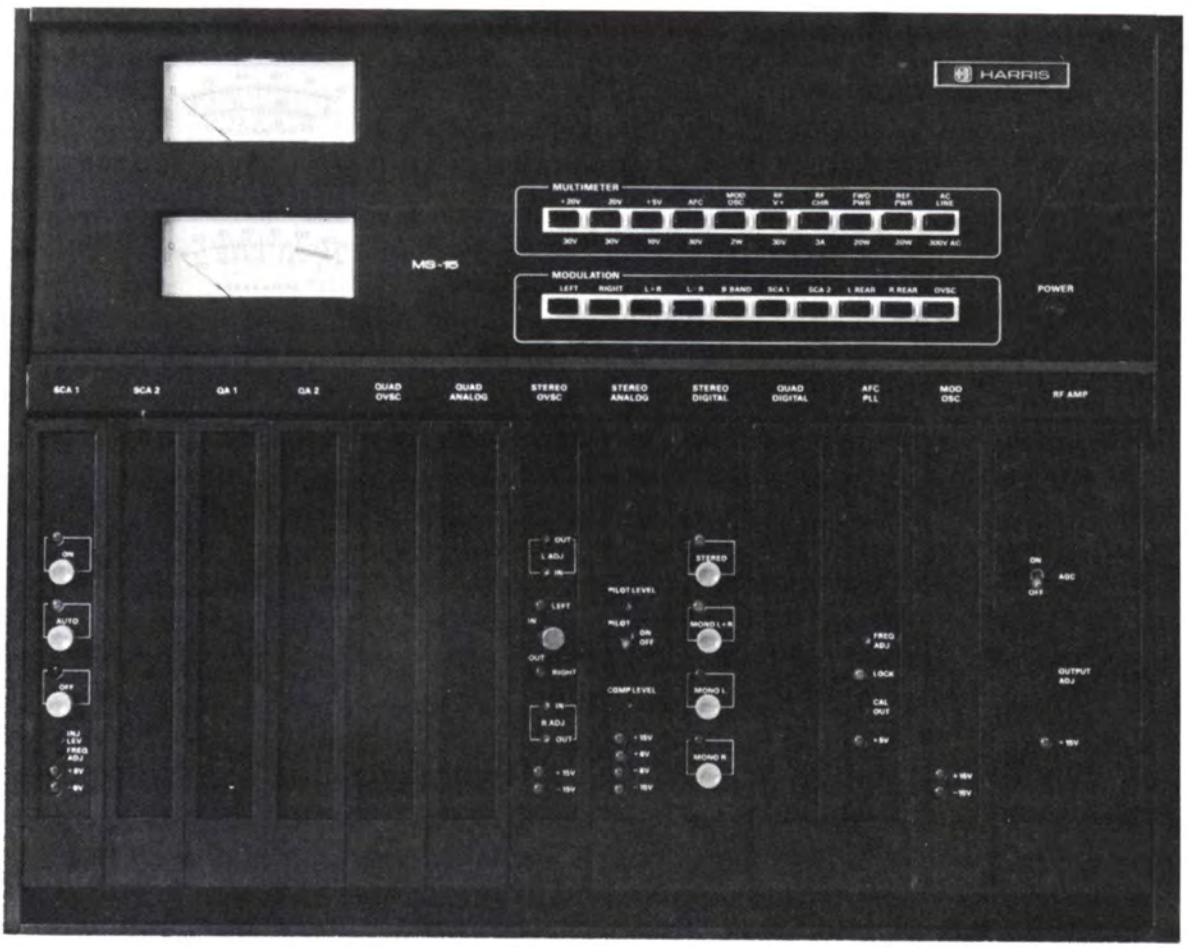


Figure 1-1. MS-15 FM Exciter





WARNING: Disconnect primary power prior to servicing.

output RFI filters, the metering circuits, and the power supply components. The entire exciter mounts in 14 vertical inches of standard 19 inch rack space.

1-7. FUNCTIONAL DESCRIPTION.

1-8. The Harris MS-15 exciter produces a frequency modulated output continuously variable from three to 15 watts for any channel assignment within the 87.5 to 108 MHz commercial FM broadcast band (see figure 1-2). Servicing is simplified as the exciter is modular in concept and discrete functions are complete within individual plug-in modules. The metering panel contains a true peak reading audio meter and a multimeter which monitors important audio, RF, and control voltages. Light emitting diode status indicators monitor critical functions on each plug-in module. Many design features provide operational characteristics superior to conventional FM equipment.

1-9. STEREOPHONIC OPTION.

1-10. The stereophonic option consists of the STEREO DIGITAL module, the STEREO ANALOG module, and the STEREO OVSC module. Features of the stereophonic option are discussed in the following text.

1-11. DIGITALLY SYNTHESIZED MODULATION (DSM) STEREOPHONIC GENERATOR. The STEREO ANALOG and STEREO DIGITAL modules comprising the DSM stereophonic generator eliminate the compromise existing between other popular types of stereophonic generators. The switching type of stereophonic modulator produces poor separation at high frequencies. Poor harmonic rejection and SCA crosstalk are problems experienced with the balanced modulator type of stereophonic generator. The Harris developed DSM stereophonic generator typically produces 45 dB of stereophonic signal separation from 20 Hz to 15 kHz with an exceptionally clean baseband signal which promotes minimal interaction between sterophonic and SCA service. An automatic phase control circuit adjusts the stereophonic pilot phase to maintain stereophonic signal separation. Selectable FLAT, 25, 50, and 75 microsecond preemphasis is provided for use as desired.

1-12. DYNAMIC TRANSIENT RESPONSE (DTR) FILTER. A Harris developed low-pass filter comprising the STEREO OVSC module operates independently of limiters or stereophonic generators to limit the overshoot on FM stereophonic or future quadraphonic transmission to two percent maximum on any input program material processed by any limiter. The filter is transparent to audio within $\pm$0.5 dB of its passband of 30 Hz to 15 kHz and provides over 50 dB of attenuation at 19 kHz and above. The filter inaudibly reduces modulation overshoots to less than two percent. Typically, elimination of overshoot allows a two to six dB increase in loudness with no other audible effect.

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WARNING: Disconnect primary power prior to servicing.

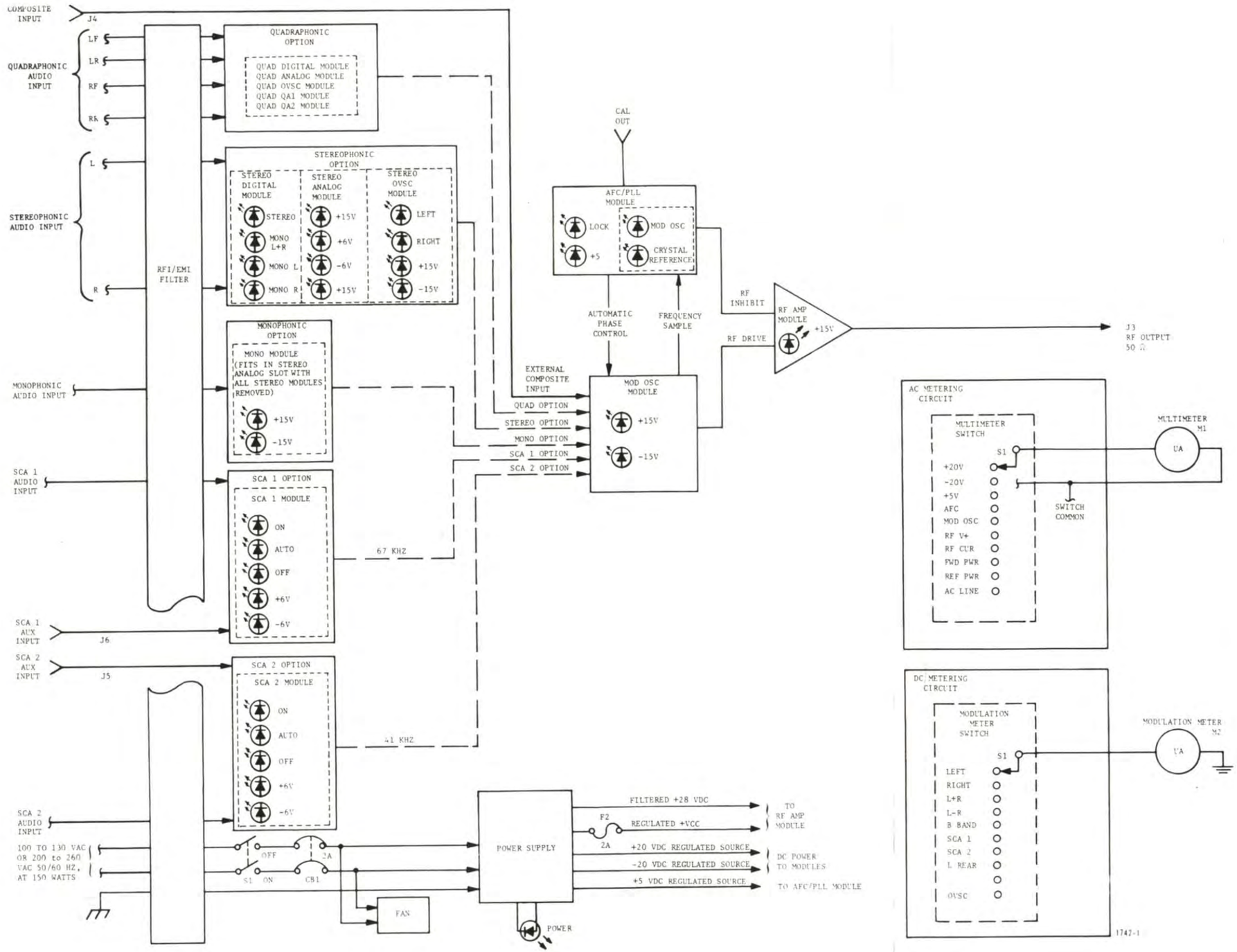


FIGURE 1-2.
SIMPLIFIED BLOCK DIAGRAM

1-13. MONOPHONIC OPTION.

1-14. When the monaural option is used, the three stereophonic modules must be removed and the MONO module plugged into the STEREO ANALOG module position. Solid state input circuitry provides high common mode rejection and selectable pre-emphasis similar to the stereophonic module is provided. A built-in defeatable linear-phase low-pass filter provides optimal linear control of overshoot and protects the 41 kHz and/or 67 kHz SCA channels.

1-15. SCA OPTION.

1-16. High quality SCA is provided by dual frequency SCA generators which operate at frequencies of 41 kHz or 67 kHz. The filter includes a seven pole Butterworth audio low-pass filter which allows use of full 150 microsecond pre-emphasis without degrading SCA to stereophonic isolation. Band-pass filters allow both the 41 kHz and 67 kHz SCA channels to be operated simultaneously without harmonic interference. Modulation can be DC coupled to allow SSTV and data transmission without special outboard units. Selectable manual or automatic variable level muting and selectable pre-emphasis are provided.

1-17. FREQUENCY SYNTHESIZER.

1-18. All FM channels are synthesized from a highly stable 10.0 mHz temperature compensated crystal oscillator (TCXO) in the AFC/PLL module which eliminates requirements for an oven, thereby reducing warmup time to zero. Channel frequency is field programmable in 50 kHz increments to accommodate future domestic or international channel assignments. As the frequency reference is obtained from 10.0 mHz, Stations may compare their frequency directly with a broadcast frequency standard such as WWV for calibration. A front panel test point provides a convenient point for frequency comparisons using a short-wave receiver.

1-19. A phase locked loop with dual characteristics provides frequency correction and reduces frequency lockup time to a minimum. The loop employs high rate feedback control when power is turned on as the loop is initially unlocked. As soon as the lock detector perceives lock, loop correction is slowed for optimum transmission of low frequencies.

1-20 The broadbanded MOD OSC module VCO assembly and a synthesizer with a wide lockup range delete the requirement for a center frequency adjustment. A predistortion network modifies the incoming signal and linearizes the VCO output to less than 0.1% distortion. The VCO assembly output is amplified to a 250 milliwatt level as required to drive the RF AMP module.

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1-21. AUTOMATIC LEVEL SWITCHING.

1-22. With many comparable systems, main channel loudness is sacrificed when the SCA channels mute or when the transmission mode is switched between monaural and stereophonic service. With the Harris automatic level switching circuit, discrepancies in total modulation caused by pilot and SCA injection are noiselessly compensated by an automatic composite gain switcher in the MOD OSC module which maintains 100% peak modulation for all standard combinations of stereophonic, monaural, L, R, or L+R, and 0, 1, or 2 SCA channels.

1-23. QUADRAPHONIC OPTION.

1-24. Because of the extremely clean baseband provided by the DSM system of stereo generation and the stable digitally synthesized nature of the system, compatibility with any of the proposed discrete quadraphonic transmission systems is assured. The Harris MS-15 FM exciter mainframe is already wired for plug-in quadraphonic modules, facilitating the transition from stereophonic to quadraphonic transmission.

1-25. POWER AMPLIFIER.

1-26. The RF AMP module is broadbanded from 87.5 MHz to 108 MHz and requires no tuning. An AGC circuit stabilizes the output power to a level which is adjustable from three watts to 15 watts. A VSWR circuit senses load faults and provides shutdown to protect the power amplifier from load mismatch. Off frequency transmission is prevented by a circuit which automatically inhibits RF output whenever the frequency synthesizer loop is in an unlocked condition.

1-27. POWER SUPPLY CIRCUIT.

1-28. All exciter inputs and outputs, including the power supply AC input, are buffered by the RFI/EMI filter with the exception of the SCA-1 AUX INPUT (J6), SCA-2 AUX INPUT (J5), COMPOSITE INPUT (J4), and the exciter RF OUTPUT (J3) which interface via coaxial (shielded) lines.

1-29. Switch S1 and circuit breaker CB1 provide power supply overload protection and control. A fan which operates when power is on provides cooling of internal high power components. The power supply develops a positive 34 Vdc potential fused at three amperes which operates the RF AMP module. Preregulated ±20 Vdc potentials and a regulated positive five volt DC potential are also produced to operate the remaining portion of the exciter internal circuitry.

1-30. EQUIPMENT CHARACTERISTICS.

1-31. ELECTRICAL CHARACTERISTICS.

1-32. Table 1-1 lists electrical operating characteristics and parameters of the MS-15 FM exciter.

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1-33. MECHANICAL/ENVIRONMENTAL CHARACTERISTICS.

1-34. Table 1-2 lists physical and environmental characteristics of the MS-15 FM exciter.





WARNING: Disconnect primary power prior to servicing.

Table 1-1. Electrical Characteristics

| FUNCTION | CHARACTERISTIC |
|---|---|
| GENERAL | |
| Primary Power Requirements | 100 to 130 Vac or 200 to 250 Vac, 50/60 Hz, single phase, 150 watts |
| RF Power Output | 3 watts to 15 watts, continuously variable |
| RF Output Impedance | 50 ohms, open and short circuit protected |
| RF Frequency Range | 87.5 to 108 MHz (programmable 50 kHz channel spacing) |
| RF Carrier Frequency Stability | ±300 Hz or less from 0°C to 50°C (TXCO)<br>Drift: ±200 Hz per year or less |
| RF Harmonic Suppression | 53 dB or greater (meets FCC requirements for 10 watt educational) |
| RF Power Amplifier Bandwidth | Linear ±1 dB (87.5 to 108 MHz at 15 watt output) |
| Type of Modulation | Direct Carrier Frequency Modulation (DCFM) |
| Modulation Capability | ±100 kHz from center frequency |
| Metering: AC | 10 circuit parameter peak reading |
| DC | 10 circuit Parameter |
| MONAURAL OPTION | |
| Audio Input Impedance | 600 ohms balanced, resistive (adaptable to other impedances) |
| Input Filter | Linear phase low-pass filter, defeatable |
| Audio Input Level | +10 dBm ±1 dB for 100% modulation at 400 Hz |
| ELECTRICAL CHARACTERISTICS SUBJECT TO CHANGE WITHOUT NOTICE | |

Table 1-1. Electrical Characteristics (Continued)

| FUNCTION | CHARACTERISTIC |
|---|---|
| MONAURAL OPTION (cont'd) | |
| Audio Frequency Response | Standard 75 microsecond FCC pre-emphasis curve ±0.5 dB from 30 Hz to 15,000 Hz. Selectable: flat, 25, 50, or 75 microsecond pre-emphasis |
| Harmonic Distortion | 0.2% or less from 30 Hz to 15,000 Hz |
| IMD | 0.2%, 60/7000 Hz, 4:1 ratio |
| FM Noise | 68 dB below 100% modulation (ref. 400 Hz @ ±75 kHz deviation, measured 30 Hz to 15 kHz with 75 microsecond de-emphasis) |
| AM Noise | 70 dB below reference carrier AM modulation 100%, at 15 watt power output |
| STEREOPHONIC OPTION | |
| Type of Modulation | Digitally Synthesized Modulation (DSM) |
| Audio Input Impedance | (left and right) 600 ohms balanced, resistive (adaptable to other impedances) |
| Audio Input Level | (left and right) +10 dBm ±1 dB for 100% modulation at 400 Hz |
| Audio Frequency Response | (left and right) Standard 75 micro-second, FCC pre-emphasis curve ±0.5 dB from 30 Hz to 15,000 Hz. Selectable: flat, 25, 50 or 75 microsecond pre-emphasis |
| Input Filtering | 15 kHz LPF, Greater than 45 dB re-jection at 19 kHz and above. |
| Overshoot Protection | Dynamic Transient Response (DTR) filter |
| ELECTRICAL CHARACTERISTICS SUBJECT TO CHANGE WITHOUT NOTICE | |

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Table 1-1. Electrical Characteristics (Continued)

| FUNCTION | CHARACTERISTIC |
|---|---|
| STEREOPHONIC OPTION (cont'd) | |
| Audio Transient Response | 2% maximum overshoot beyond steady state. Defeatable for test purposes. |
| Harmonic Distortion | (left or right) 0.4% or less from 30 Hz to 15,000 Hz |
| IMD | 0.4%, 60/7000 Hz, 4:1 ratio |
| FM Noise | (left or right) 65 dB minimum below 100% modulation. Reference (400 Hz, 75 microsecond de-emphasis, ±75 kHz deviation, measured 30 Hz to 15 kHz) |
| Pilot Oscillator | Crystal controlled |
| Pilot Stability | 19 kHz ±1 Hz, 0° to 50° C |
| Pilot Phase | Automatically controlled |
| Stereo Separation | 45 dB minimum from 30 Hz to 15,000 Hz |
| Dynamic Stereo Separation | 40 dB minimum under normal programming conditions |
| Crosstalk | (main to stereo sub-channel or stereo sub-to-main channel) 45 dB below 90% modulation |
| Sub-Carrier Suppression | 60 dB minimum below 100% Modulation |
| 76 kHz Suppression | 60 dB minimum below 100% modulation |
| Modes | Stereo, mono L + R, mono L, mono R (remotable) |
| SCA OPTION | |
| Modulation | Direct FM |
| Frequency | 41 or 67 kHz programmable, any frequency between 25 and 75 kHz on special order |
| ELECTRICAL CHARACTERISTICS SUBJECT TO CHANGE WITHOUT NOTICE | |

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Table 1-1. Electrical Characteristics (Continued)

| FUNCTION | CHARACTERISTIC |
|---|---|
| SCA OPTION (cont'd) | |
| Frequency Stability | ±500 Hz |
| Modulation Capability | ±7.5 kHz |
| Audio Input Impedance | 600 ohms balanced (AC coupled) and 2000 ohms unbalanced (DC coupled, BNC connectors on rear panel) |
| Audio Input Level | +10 dBm ±1 dB for 100% modulation at 400 Hz |
| Audio Frequency Response | 150 microsecond pre-emphasis ±1 dB, standard. Selectable: flat, 50, 75 or 150 microsecond pre-emphasis |
| Input Filtering | Programmable LPF, 4.5 kHz standard |
| Distortion | Less than 1% from 30 Hz to 4,500 Hz at ±5 kHz deviation |
| FM Noise | (Main channel not modulated) 55 dB minimum (ref: 100% = ±5 kHz deviation at 400 Hz) |
| Crosstalk | (SCA to main or stereo sub-channel) -60 dB or greater |
| Crosstalk | (Main or stereo sub-channel to SCA) 50 dB below ±5 kHz deviation of SCA, with mono or stereo channels modulated by frequencies from 30 Hz to 15,000 Hz, SCA demodulated with 150 microsecond de-emphasis |
| Crosstalk | SCA to SCA (41 kHz/67 kHz) 50 dB demodulated with 150 microsecond de-emphasis |
| Automatic Mute Level | Variable from 0 to -30 dBm |
| Mute Delay | Adjustable 0.5 to 20 seconds |
| ELECTRICAL CHARACTERISTICS SUBJECT TO CHANGE WITHOUT NOTICE | |

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Table 1-1. Electrical Characteristics (Continued)

| FUNCTION | CHARACTERISTIC |
|---|---|
| SCA OPTION (cont'd) | |
| Injection Level | Adjustable from 1% to 30% composite |
| WIDEBAND INPUT | |
| Input Impedance | Greater than 5000 ohms resistive, unbalanced |
| Input Level | 1.0 VRMS nominal for ±75 kHz deviation |
| Amplitude Response | ±0.25 dB from 30 Hz to 75 kHz |
| Phase Linearity | ±2° from 30 Hz to 75 kHz |
| ELECTRICAL CHARACTERISTICS SUBJECT TO CHANGE WITHOUT NOTICE | |

Table 1-2. Mechanical/Environmental Characteristics

| FUNCTION | CHARACTERISTIC |
|---|---|
| Weight | 51 pounds (23.13 kg), Net unpacked*<br>60 pounds (27.21 kg), Net packed* |
| Size | Width, 19 inches (48.26 cm)<br>Depth, 12 inches (30.48 cm)<br>Height, 14 inches (35.36 cm) |
| Operating Temperature Range | $0^{o}C$ to $50^{o}C$. Usable to $-20^{o}C$ with slight reduction in operating parameters. |
| Maximum Altitude | 15,000 feet (4572 meters) above sea level |
| Maximum Humidity | 95%, non condensing |
| Required Mounting Space | 14 inches (35.65 cm) of standard 19 inch (48.26 cm) rack |
| Cooling Air Requirements | 122 ft 3/minute (3.17 $m^3$/minute) |

*Depends on module complement







WARNING: Disconnect primary power prior to servicing.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information required to unpack, inspect, and install the MS-15 FM exciter. Preoperational checks and power on checks will ensure correct exciter operation. Components or modules removed from the exciter after final test, for transport, are tagged and provided with appropriate instructions for reinstallation.

2-3. UNPACKING.

2-4. Carefully unpack the MS-15 FM exciter and perform a visual inspection to determine that no apparent damage was incurred during shipment. Retain the shipping materials until it has been determined that the unit is not damaged. The contents of the shipment should be as indicated on the packing list. If the contents are incomplete or if the unit is damaged electrically or mechanically, notify the carrier and Harris Corporation Broadcast Products Division.

2-5. All packing materials must be removed from the equipment and the modules. The removal of components varies due to the method and requirements for shipment. All removed components are tagged to permit easy reinstallation in the equipment. Symbol numbers and descriptions are provided on each removed component corresponding to the schematic diagram, parts list, packing list and a reference designator or nomenclature stenciled at the cabinet location of each removed item. Cables and small parts may be taped or tied in place for shipment. Remove all tape, string, and packing materials used for this purpose. Install any removed components in the interior of the cabinet and arrange the modules in a separate container according to the order in which each module installs in the equipment.

2-6. INSTALLATION.

2-7. Prior to installation, the manual should be carefully studied to get a thorough understanding of the principles of operation, circuitry and nomenclature. This will facilitate proper installation and initial checkout. Installation of the MS-15 FM exciter will be accomplished in four steps: 1) exciter placement, 2) module installation, 3) exciter wiring, and 4) preliminary checkout.

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2-8. EXCITER PLACEMENT.

2-9. The Harris MS-15 FM exciter is manufactured to directly retrofit the Harris TE-3 FM exciter or any similiar FM exciter. The exciter requires 14 vertical inches of standard 19 inch rack space and should be placed in a location which provides convenient access to the rear panel near power, RF, and control cables. As cooling air enters the equipment through vents in the



 WARNING: Disconnect primary power prior to servicing.

bottom panel, the exciter should not be placed directly above heat generating equipment such as an amplifier stage. The equipment is thoroughly RFI shielded and no special isolation precautions are required.

2-10. MODULE INSTALLATION.

2-11. Several modules require jumper-plug programming which initializes the module to operate in a predetermined mode at power application. Refer to table 2-1 and ensure each jumper listed is correctly installed in each respective module to produce the desired mode of operation. After the module programming is completed, each module should be inserted in its respective slot in the exciter case.

2-12. EXCITER WIRING.

2-13. External wiring of the exciter will differ between units depending upon the options purchased with each individual exciter. Refer to table 2-2 and figure 2-1 for information required to connect inputs, remote control lines, and monitoring equipment to the FM exciter.

2-14. After wiring of the inputs, control lines, and monitoring equipment is completed, the following additional external connections must be made. Power connections will be wired last.

a. GROUND: Connect the GND LUG terminal on the rear of the exciter to station ground.

b. RF LOAD: Connect the exciter load to the RF OUTPUT 50Ω terminal (J3) on the rear of the exciter.

c. COMPOSITE INPUT: If a composite input is to be used with the exciter, connect the input to the COMPOSITE INPUT terminal (J4) on the rear of the exciter.

d. SCA AUXILIARY INPUT: If an auxiliary SCA input such as teletype is required, connect the inputs to SCA-1 AUX INPUT (J6) and SCA-2 AUX INPUT (J5) as necessary.

**WARNING**

Do not apply power to the exciter in step e.

e. PRIMARY AC: Prepare plug P2 for connection to either 115 Vac or 230 Vac as shown in figure 2-2. After the plug is correctly wired to either the 115 Vac or the 230 Vac configuration, connect plug P2 to the AC POWER input on the exciter rear (J2). Do not connect the power cord to the AC source at this time.

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 WARNING: Disconnect primary power prior to servicing.

Table 2-1. Module Programming

| MODULE | JUMPER | NOMENCLATURE | PURPOSE |
|---|---|---|---|
| SCA 1 and SCA 2 | J1 | 41 KHZ/67 KHZ | Selects SCA frequency. |
| | J2 | 41 KHZ/67 KHZ | Selects SCA filter freq. |
| | J3 | 41 KHZ/67 KHZ | Selects SCA filter freq. |
| | J4 | POWER UP: OFF/ON/AUTO | Determines operational status at power application |
| | J5 | PREMPH: 150/75/50/0 | Selects SCA input pre-emphasis. |
| STEREO DIGITAL | J1 | POWER UP: STEREO/LEFT/ RIGHT/L+R | Selects the mode in which the module will initialize when power is applied. |
| | J2 | SCA INTERLOCK L+R/LEFT/RIGHT | Selects monaural mode STEREO DIGITAL module will enter if simultaneous 41 KHZ SCA and stereophonic operation is attempted. |
| STEREO ANALOG | J1 | FLAT/25/50/75 | Selects stereo input pre-emphasis. |
| | J2 | FLAT/25/50/75 | Selects stereo input pre-emphasis. |
| | J3 | DTR/INT | Selects the internal low pass filter or enables the DTR filter. |
| | J4 | DTR/INT | Selects the internal low pass filter or enables the DTR filter. |
| | J5 | DTR/INT | Selects the internal low pass filter or enables the DTR filter. |
| | J6 | DTR/INT | Selects the internal low pass filter or enables the DTR filter. |
| MONO | J1 | A/B/C/D | Selects mono input pre-emphasis. A: 75 us B: 50 us C: 25 us D: FLAT |
| | J2 | A/B/C/D | Enables or bypasses the linear phase low pass filter. Enable: A to B, C to D. Bypass: A to C, B to D. |

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Table 2-2. Exciter Wiring

| TERMINAL | NOMENCLATURE | SIGNAL |
|---|---|---|
| TB1 PIN 1 | LEFT FRONT + | (red) 600 ohm balanced audio input |
| 2 | LEFT FRONT ⏚ | (shield) mono, stereo left channel, |
| 3 | LEFT FRONT - | (black) or left front channel for future quad transmission. |
| 4 | RIGHT FRONT + | (red) 600 ohm balanced audio input |
| 5 | RIGHT FRONT ⏚ | (shield) for stereo right channel or |
| 6 | RIGHT FRONT - | (black) right front channel for future quad transmission. |
| 7 | SCA-1 + | (red) |
| 8 | SCA-1 ⏚ | (shield) 600 ohm balanced audio input |
| 9 | SCA-1 - | (black) for SCA channel No. 1. |
| 10 | SCA-2 OR LEFT REAR + | (red) 600 ohm balanced audio input |
| 11 | SCA-2 OR LEFT REAR ⏚ | (shield) for SCA channel No. 2 or left |
| 12 | SCA-2 OR LEFT REAR - | (black) rear channel for future quad transmission. |
| 13 | RIGHT REAR + | (red) 600 ohm balanced audio input |
| 14 | RIGHT REAR ⏚ | (shield) for right rear channel for |
| 15 | RIGHT REAR - | (black) future quad transmission. |
| 16 | ST. | (STEREO MODE) A momentary contact to ground will cause the equipment to transmit in the stereo mode. * |
| 17 | L+R | (STEREO MODE) A momentary contact to ground will cause the equipment to transmit a mono signal from both stereo channels. * |
| 18 | LEFT MONO | (STEREO MODE) A momentary contact to ground will cause the equipment to transmit a mono signal from the left stereo channel and mute the right stereo channel. * |
| TB2 PIN 19 | RIGHT MONO | (STEREO MODE) A momentary contact to ground will cause the equipment to transmit a mono signal from the right stereo channel and mute the left stereo channel. * |
| 20 | ON | (SCA-1 MODE) A momentary contact to ground will enable SCA channel No. 1. * |

* See Note 1.



 WARNING: Disconnect primary power prior to servicing.

Table 2-2. Exciter Wiring (Continued)

| TERMINAL | NOMENCLATURE | SIGNAL |
|---|---|---|
| TB2 PIN 21 | AUTO | (SCA-1 MODE) A momentary contact to ground will enable the SCA-1 module automatic muting function. (See note 1) |
| 22 | OFF | (SCA-1 MODE) A momentary contact to ground will mute SCA channel No. 1 at all times. * |
| 23 | ON | (SCA-2 MODE) A momentary contact to ground will enable SCA channel No. 2 whenever power is on. * |
| 24 | AUTO | (SCA-2 MODE) A momentary contact to ground will enable the SCA-2 module automatic muting function. (See note 1) |
| 25 | OFF | (SCA-2 MODE) A momentary contact to ground will mute SCA channel No. 2 at all times. |
| 26 | (I) | (P.A. METER) Provision to monitor sampled power amplifier collector current. A 20 K ohm, 1/4 watt resistor and a 0-100 microammeter are required (see figure 2-1). Three amperes of supply current will produce full scale meter deflection. |
| 27 | (V) | (P.A. METER) Provision to monitor the power amplifier supply voltage. A 0-30 voltmeter is required (see figure 2-1). |
| 28 | FWD | (R.F. METER) Provision to monitor the exciter forward power output sensed by the directional coupler. A 0-100 microammeter is required (see figure 2-1). |
| 29 | REF. | (R.F. METER) Provision to monitor the exciter reflected power sensed by the directional coupler. A 0-100 microammeter is required (see figure 2-1). |

* See Note 1.





WARNING: Disconnect primary power prior to servicing.

Table 2-2. Exciter Wiring (Continued)

| TERMINAL | NOMENCLATURE | SIGNAL |
|---|---|---|
| TB2 PIN 30 | R.F. INT. | A contact to ground will inhibit the exciter carrier output until the ground is removed. |
| 31 | SPARE 1 | Spare contact. |
| 32 | S.W. COM. + | A jumper from TB2 pin 34 provides a 20 Vdc potential to operate the remote mode switching circuits (see figure 2-3). If remote mode switching is not desired, the jumper may be removed. |
| 33 | SPARE 2 | Spare contact. |
| 34 | S.W.P.S. + | Provides a 20 Vdc potential to operate the remote mode switching circuits through a jumper to TB2 pin 32 (see figure 2-3). If remote mode switching is not desired, the jumper may be removed. |
| 35 | N.O.AFC.INT. | Provides one set of normally open contacts or relay 2A1A4K1 which close when the AFC/PLL module achieves frequency lock. The contacts are rated at three amperes at 120 Vac. |
| 36 | N.O.AFC.INT. | |

*NOTES:

1. Remote control requires that terminal 34 (+ S. W. P. S.) be jumpered to terminal 32 (+ S. W. COM.) or a positive 12 Vdc to 28 Vdc potential must be jumpered between the desired terminal and terminal 32 (S. W. COM.).



 WARNING: Disconnect primary power prior to servicing.

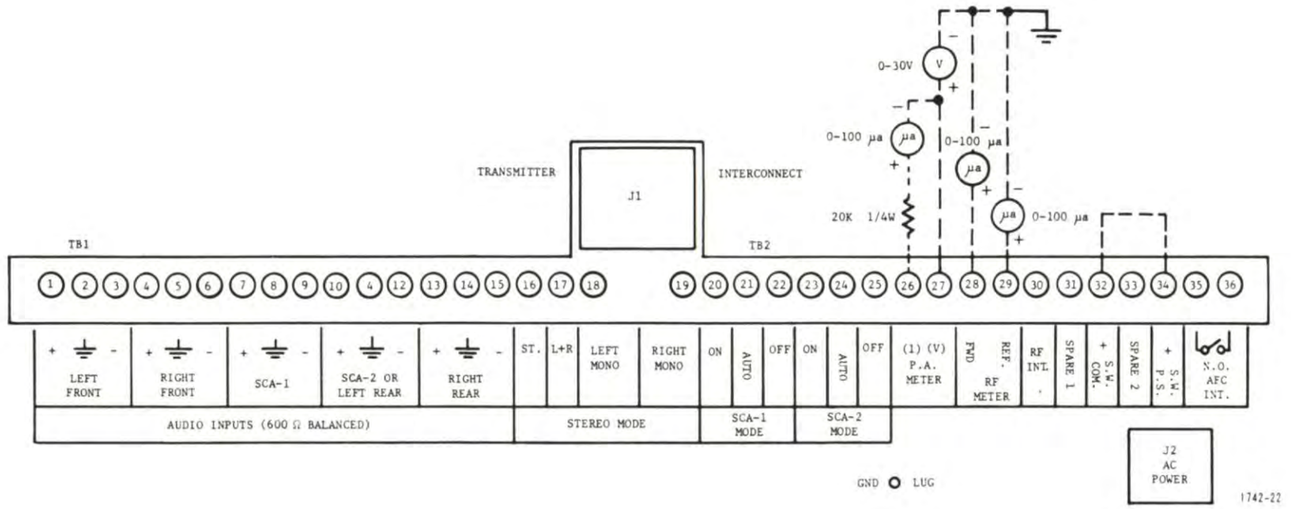


FIGURE 2-1.
EXCITER WIRING

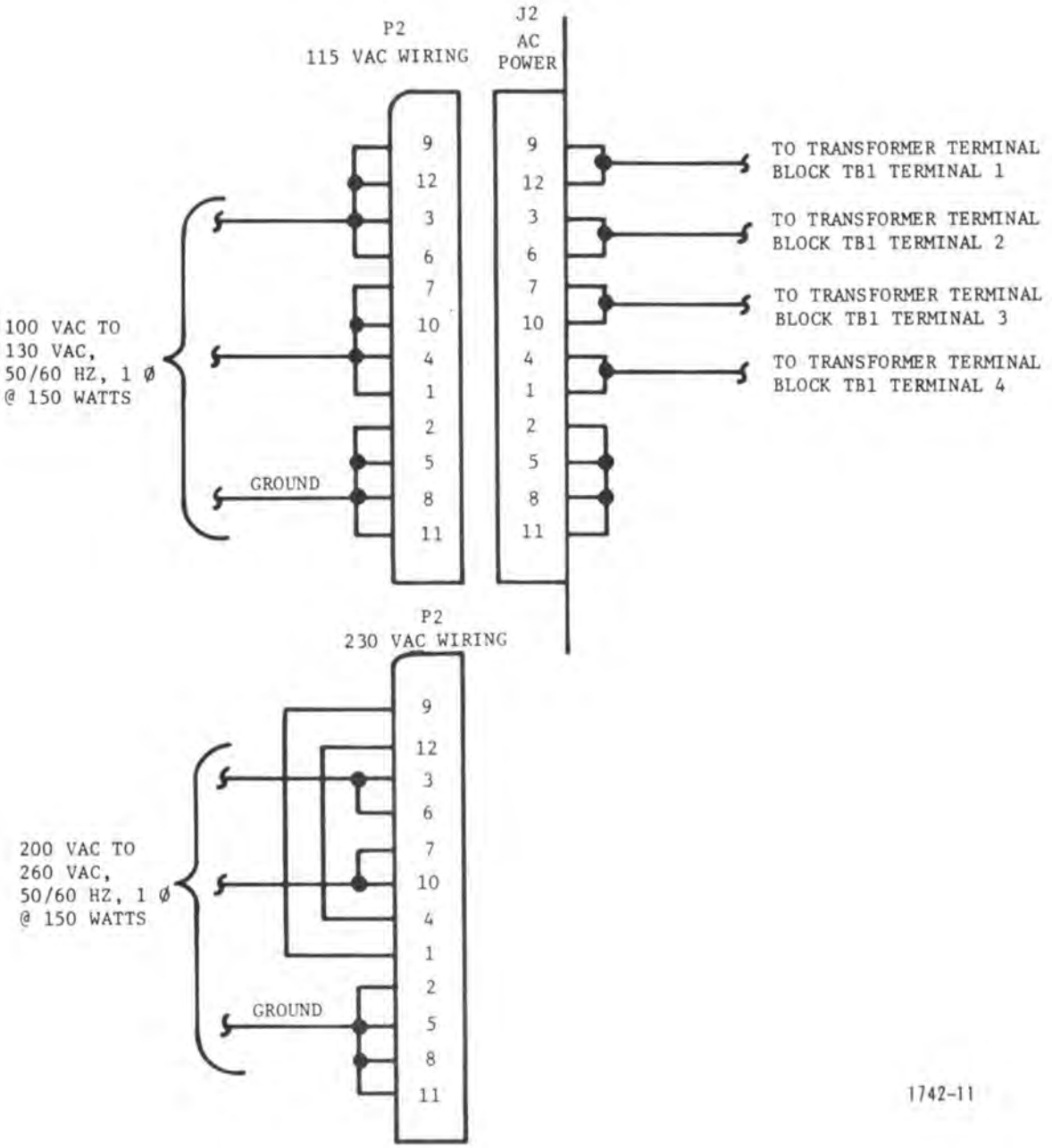


Figure 2-2. Primary AC Wiring





WARNING: Disconnect primary power prior to servicing.

**WARNING**

Ensure power is not applied to the exciter before proceeding.

2-15. The complete exciter should be inspected at this time. Check the following:

a. Ensure all connections at terminal boards and components are tight and secure and all wires are dressed properly.

b. Remove any extra hardware or wire from the area. Ensure all packing materials are removed.

c. Rotate the fan manually to be sure no obstructions are present.

2-16. Ensure the exciter POWER ON/OFF switch (2A1S1) is set to OFF and connect the power cord to the AC source.

2-17. PRELIMINARY CHECKOUT.

2-18. Adjust the RF AMP module OUTPUT ADJ control (2A2R13) fully counterclockwise (zero power output).

2-19. Depress the MULTIMETER AC LINE switch.

**CAUTION**

Ensure the exciter output is connected to a proper 50 ohm load.

2-20. Set the exciter POWER ON/OFF switch (2A1S1) to ON and note the following indications. If trouble is experienced, refer to Section V, Maintenance.

a. The MULTIMETER (2A1M1) must indicate 115 Vac ±15 Vac or 230 Vac ±30 Vac, as wired. If the primary AC voltage is out of tolerance, it must be corrected before proceeding.

b. The front panel POWER indicator (3A1DS1) will illuminate.

c. All the module front panel power indicators (+5V, +6V, -6V, +15V, and -15V) will illuminate.

2-21. Adjust the RF AMP module OUTPUT ADJ control (2A2R13) to obtain a three watt RF output. Refer to table 2-3 and check the MULTIMETER (2A1M1) and MODULATION (2A1M2) meter indications listed. If trouble is experienced, refer to Section V, Maintenance.





WARNING: Disconnect primary power prior to servicing.

Table 2-3. Preliminary Meter Indications

| MULTIMETER SWITCH POSITION | MULTIMETER INDICATION* |
|---|---|
| +20V | +22V |
| -20V | +22V |
| +5 V | +5 V |
| AFC | +3V to +12V** |
| MOD OSC | 250 mW ± 100 mW |
| RF V+ | +7.5V |
| RF CUR | 0.9 Amperes |
| FWD PWR | 3W |
| REF PWR | <0.5W |

*APPROXIMATE VALUES -- DEPENDENT ON MODULE COMPLEMENT.
**DEPENDENT UPON EXCITER FREQUENCY.

2-22. The audio inputs should be checked to ensure correct wiring. Depress the MODULATION switch (2A1A2S1) corresponding to each option purchased with the equipment and check for activity on the MODULATION meter (2A1M2). The monaural audio input may be checked by depressing the MODULATION LEFT or MODULATION RIGHT meter switch and noting activity on the MODULATION meter.

2-23. Set the POWER ON/OFF switch (2A1S1) to OFF.

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 WARNING: Disconnect primary power prior to servicing.

# SECTION III

# OPERATION

3-1. INTRODUCTION.

3-2. This section contains information pertaining to identification, location and function of the controls and indicators of the MS-15 FM exciter, setup, and operation procedures.

3-3. CONTROLS AND INDICATORS.

3-4. Figure 3-1 shows the location of each control or indicator associated with the MS-15 FM exciter and table 3-1 lists each control or indicator with a description of each item listed.

3-5. OPERATION.

3-6. Exciter power on-off is controlled by a single switch accessible from behind the exciter meter panel. As all critical functions in the exciter are stabilized by automatic control circuits and feedback loops, the only adjustments required on a daily basis are the mode controls if the mode of operation must be changed. All mode switching is remoteable from connections on the rear of the exciter.

3-7. MONITORING CAPACITY.

3-8. The metering functions are contained within the modular DC and peak reading audio metering circuits. The metering functions are listed in table 3-2.

3-9. MODE SWITCHING.

3-10. STEREOPHONIC/MONAURAL SWITCHING. Modes of operation available with the MS-15 FM exciter are STEREO, MONO L, MONO R, and MONO L+R which are selected by switches on the STEREO DIGITAL module. Indicators on the module illuminate to indicate the selected mode of operation. MONO L or MONO R allows stations which use stereophonic operation as a standard mode to broadcast in monaural if one audio channel fails during sterophonic operation or if it is desired to broadcast from a separate monaural studio feed. The MONO L+R capability is an exclusive MS-15 feature which allows monaural transmission by both stereophonic channels without changing limiters or studio consoles. Stereophonic programming in the MONO L+R mode is transmitted as monaural by mixing both stereophonic channels.

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3-11. SCA SWITCHING.

3-12. Either or both of the SCA channels may be operated automatically in the AUTO mode or manually in the ON or OFF modes by switches on each respective SCA module. Indicators on each SCA module illuminate to indicate the selected mode of operation. In the AUTO mode, SCA subcarrier presence





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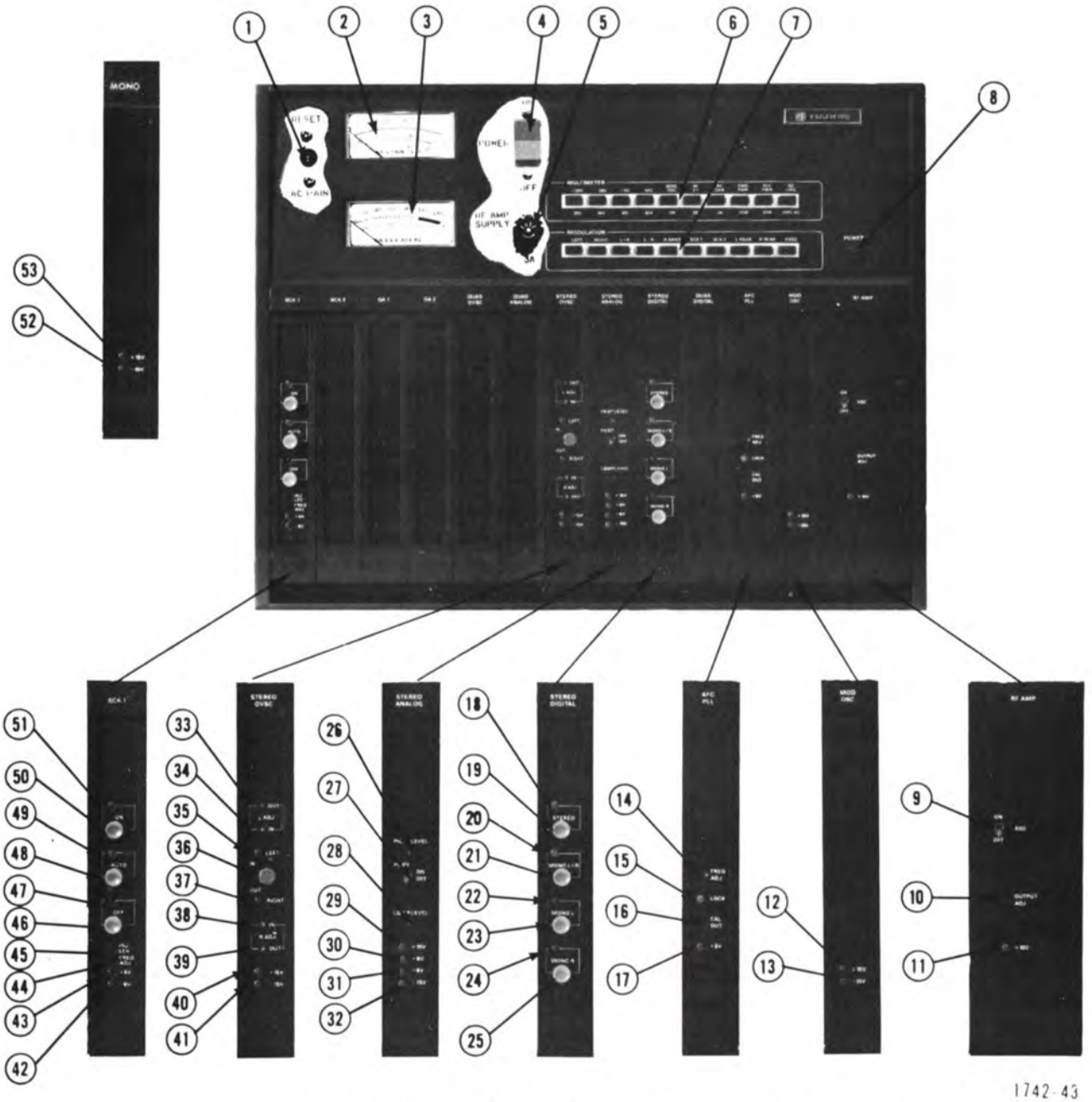


Figure 3-1. Controls and Indicators





WARNING: Disconnect primary power prior to servicing.

Table 3-1. Controls and Indicators

| REF. | CONTROL/INDICATOR | FUNCTION |
|---|---|---|
| 1 | AC MAIN RESET circuit breaker (2A1CB1) | Controls primary power and provides overload protection for the exciter power supply. |
| 2 | MULTIMETER (2A1M1) | Displays voltage, current or power as selected by the MULTIMETER switch (2A1A1S1). |
| 3 | MODULATION meter (2A1M2) | Displays the modulation signals as selected by the MODULATION meter switch (2A1A2S2). |
| 4 | POWER ON/OFF switch (2A1S1) | Controls primary power to the exciter power supply. |
| 5 | RF AMP SUPPLY fuse (2A1F1) | Provides overload protection for the RF amplifier power supply. |
| 6 | MULTIMETER switch (2A1A1S1) | Selects the desired point to monitor exciter voltage, current or power as displayed by the MULTIMETER (2A1M1). |
| 7 | MODULATION meter switch (2A1A2S1) | Selects the desired exciter modulation to be monitored on the MODULATION meter (2A1M2). |
| 8 | POWER indicator (2A1DS1) | Illuminates to indicate power is applied to the exciter power supply. |
| | RF AMP MODULE | |
| 9 | AGC ON/OFF switch (2A2S1) | Enables the power amplifier automatic output level control. |
| 10 | OUTPUT ADJUST control (2A2R13) | Adjusts the power amplifier output level. |
| 11 | +15V indicator (2A2CR5) | Illuminates to indicate the RF AMP module +15 volt regulator is operational. |
| | MOD OSC MODULE | |
| 12 | +15V indicator (2A4CR5) | Illuminates to indicate the MOD OSC module +15 volt regulator is operational. |
| 13 | -15V indicator (2A4CR6) | Illuminates to indicate the MOD OSC module -15 volt regulator is operational. |

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Warning, disconnect primary power prior to servicing.

Table 3-1. Controls and Indicators (Continued)

| REF. | CONTROL/INDICATOR | FUNCTION |
|---|---|---|
| | AFC PLL MODULE | |
| 14 | FREQ ADJ control (2A3R18) | Adjusts the FM carrier frequency. |
| 15 | LOCK indicator (2A3CR8) | Illuminates to indicate the exciter is operating within tolerance of the assigned frequency. |
| 16 | CAL OUT test point | Provides frequency components at 2.5 MHz, 5.0 MHz, 10.0 MHz, 15.0 MHz, 20.0 MHz, and 25.0 MHz for direct frequency comparisons between the internal frequency standard and a broadcast frequency standard such as WWV using a communications receiver. |
| 17 | +5V indicator (2A3CR2) | Illuminates to indicate application of the +5 volt supply to the AFC/PLL module. |
| | STEREO DIGITAL MODULE | |
| 18 | STEREO indicator (3A2CR6) | Indicates stereo mode of operation is enabled when illuminated. |
| 19 | STEREO switch (3A2S4) | Enables stereo mode operation. |
| 20 | MONO L+R indicator (3A2CR5) | Indicates mono L+R mode of operation is enabled when illuminated. |
| 21 | MONO L+R switch (3A2S3) | Enables the mono L+R mode to transmit a mono signal from both stereo channels. |
| 22 | MONO L indicator (3A2CR4) | Indicates mono L mode of operation is enabled when illuminated. |
| 23 | MONO L switch (3A2S2) | Enables mono L mode to transmit a mono signal from the left stereo channel and mute the right stereo channel. |
| 24 | MONO R indicator (3A2CR3) | Indicates the mono R mode of operation is enabled when illuminated. |
| 25 | MONO R switch (3A2S1) | Enables the mono R mode to transmit a mono signal from the right stereo channel and mute the left stereo channel. |







Warning, disconnect primary power prior to servicing.

Table 3-1. Controls and Indicators (Continued)

| REF. | CONTROL/INDICATOR | FUNCTION |
|---|---|---|
| | STEREO ANALOG MODULE | |
| 26 | PILOT LEVEL control (3A1R41) | Adjusts the modulation level of the pilot subcarrier. |
| 27 | PILOT ON/OFF switch | Enables or inhibits the pilot subcarrier. For test purposes. Pilot is automatically disabled in any of the three monaural modes. |
| 28 | COMP LEVEL control (3A1R27) | Adjusts the composite signal level output from the STEREO ANALOG module. |
| 29 | +15V indicator (3A1CR9) | Illuminates to indicate the STEREO ANALOG module +15 volt regulator is operational. |
| 30 | +6V indicator (3A1CR10) | Illuminates to indicate the STEREO ANALOG module +6 volt regulator is operational. |
| 31 | -6V indicator (3A1CR11) | Illuminates to indicate the STEREO ANALOG module -6 volt regulator is operational. |
| 32 | -15V indicator (3A1CR12) | Illuminates to indicate the STEREO ANALOG module -15 volt regulator is operational. |
| | STEREO OVSC MODULE | |
| 33 | L ADJ OUT control (3A3R87) | Adjusts the left channel output threshold of the STEREO OVSC module. |
| 34 | L ADJ IN control (3A3R64) | Adjsuts the left channel input threshold of the STEREO OVSC module. |
| 35 | LEFT indicator (3A3CR27) | Indicates left channel overshoot control when illuminated. |
| 36 | IN/OUT switch (3A3S1) | IN position: Enables operation of the DTR filter.<br>OUT position: Enables the conventional low pass filter. |
| 37 | RIGHT indicator (3ACR28) | Indicates right channel overshoot control when illuminated. |
| 38 | R ADJ IN control (3A3R10) | Adjusts the right channel input threshold of the STEREO OVSC module. |

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Table 3-1. Controls and Indicators (Continued)

| REF. | CONTROL/INDICATOR | FUNCTION |
|---|---|---|
| | STEREO OVSC MODULE (Continued) | |
| 39 | R ADJ OUT control (3A3R33) | Adjusts the right channel output threshold of the STEREO OVSC module. |
| 40 | +15V indicator (3A3CR26) | Illuminates to indicate the STEREO OVSC module +15 volt regulator is operational. |
| 41 | -15V indicator (3A3CR25) | Illuminates to indicate the STEREO OVSC module -15 volt regulator is operational. |
| | SCA 1/SCA 2 MODULE(S) | |
| 42 | ON indicator (4A1CR6) | Indicates the presence of SCA subcarrier when illuminated. |
| 43 | ON switch (4A1S1) | Enables the SCA carrier. |
| 44 | AUTO indicator (4A1CR10) | Indicates the SCA AUTO mode of operation is enabled when illuminated. |
| 45 | AUTO switch (4A1S2) | Enables the SCA module automatic muting function. |
| 46 | OFF indicator (4A1CR14) | Indicates the SCA channel is muted when illuminated. |
| 47 | OFF switch (4A1S3) | Inhibits operation of the SCA channel. |
| 48 | INJ LEV control (4A1R16) | Adjusts the injection level of the SCA subcarrier. |
| 49 | FREQ ADJ control (4A1R12) | Adjusts the center frequency of the SCA subcarrier. |
| 50 | +6V indicator (4A1CR7) | Illuminates to indicate the SCA module +6 volt regulator is operational. |
| 51 | -6V indicator (4A1CR8) | Illuminates to indicate the SCA module -6 volt regulator is operational. |

Table 3-1. Controls and Indicators (Continued)

| REF. | CONTROL/INDICATOR | FUNCTION |
|---|---|---|
| | MONO MODULE | |
| 52 | -15V indicator (5A1CR6) | Illuminates to indicate the MONO module -15 volt regulator is operational. |
| 53 | +15V indicator (5A1CR5) | Illuminates to indicate the MONO module +15 volt regulator is operational. |

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Table 3-2. AC and DC Metering

| DC METERING | |
|---|---|
| MULTIMETER SWITCH POSITION | SIGNAL DISPLAYED |
| +20V | Pre-regulated +20 volt DC bus to all module power supply regulators. |
| -20V | Pre-regulated -20 volt DC bus to all module power supply regulators. |
| +5V | Regulated +5 volt DC supply to TTL circuitry on the AFC/PLL module. |
| AFC | AFC/PLL module AFC voltage to MOD OSC module. |
| MOD OSC | MOD OSC module output power. |
| RF CUR | RF AMP module final amplifier collector current. |
| FWD PWR | FM exciter output power. |
| REF PWR | FM exciter reflected power. |
| AC LINE | AC input to FM exciter. |

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Table 3-2. AC and DC Metering (Continued)

| AC METERING | |
|---|---|
| MODULATION METER SWITCH POSITION | SIGNAL DISPLAYED |
| LEFT | Pre-emphasized audio input for mono, left channel pre-emphasized audio input for stereo, or left front pre-emphasized audio input for quad transmission. |
| RIGHT | Pre-emphasized audio input for mono, right channel pre-emphasized audio input for stereo, or right front pre-emphasized audio input for quad transmission. |
| L+R | Sum of left channel and right channel stereo audio inputs. |
| L-R | Difference between left channel and right channel stereo audio inputs. |
| B BAND | Total modulation signal applied to VCO. |
| SCA 1 | SCA channel No. 1 data or pre-emphasized audio input. |
| SCA 2 | SCA channel No. 2 data or pre-emphasized audio input. |
| L REAR | Left rear pre-emphasized audio input for quad transmission. |
| R REAR | Right rear pre-emphasized audio input for quad transmission. |
| OVSC | Overshoot compensation indication. |

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is determined by the presence of audio. An adjustable signal threshold from 0 dBm to -30 dBm enables the SCA, and SCA delay time is adjustable from 0.5 to 20 seconds. For manual operation, the SCA ON and SCA OFF switches control the presence of the SCA subcarrier.

3-13. DYNAMIC TRANSIENT RESPONSE FILTER.

3-14. The Dynamic Transient Response (DTR) filter is activated by the OVSC module IN/OUT switch when set to the IN position. When the OVSC module IN/OUT switch is set to the OUT position, filtering is accomplished by a conventional sharp-cutoff low-pass filter which is subject to considerable overshoot. For all programming situations with all types of FM limiters, use of the DTR filter is recommended to eliminate overshoot. This switch is not a normal operating control and is provided to bypass the DTR filter for the following reasons:

a. Allow comparisons between the conventional filter and the DTR filter for exciter setup.

b. Proof of performance measurements. (The DTR filter should be disabled to measure crosstalk. All other measurements may be made with the DTR filter enabled).

c. The DTR filter must be disabled for FM stations which use no peak limiting, or that use a limiter which does not compensate for pre-emphasis characteristics. Thresholds internal to the DTR filter require that the input signal must be peak limited with pre-emphasis protection to prevent audio distortion.

# SECTION IV

## PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains principles of operation of the MS-15 FM exciter. An overall block diagram and exciter description identifies and describes each modular function and sub-system operation. Additional block diagrams and descriptions are provided in this section for all non-modular components and modules mounted to the mainframe. A detailed description of each plug-in module is provided by each applicable module publication.

4-3. FUNCTIONAL DESCRIPTION.

4-4. The electrical functions of the Harris MS-15 FM exciter can be divided into the following twelve modular sections (see figure 4-1). The description assumes all options have been purchased for use.

4-5. RFI/EMI FILTER (2A1A4).

4-6. The RFI filter ensures electromagnetic compatibility by filtering and bypassing the input and output connections of audio inputs, control lines, status lines, and the AC power input. The SCA auxiliary inputs, the composite signal input, and the exciter RF output lines are shielded coaxial lines and are not routed through the filter.

4-7. Interference by the commercial AM broadcast band to each 600 ohm balanced audio input is rejected by a three pole Butterworth filter (see figure 4-2). The filter RC output section provides loading, padding, and additional RF attenuation through one GHz. The control and status lines are filtered by a low-pass RC filter which prevents external RF interference with the exciter control and status functions. The ac input is RFI filtered by a pi section LC filter. All RFI filter sections provide attenuation between 500 kHz and one GHz. The variable coils in each audio input should be adjusted to obtain the best high frequency crosstalk at 15 kHz.

4-8. POWER SUPPLY (2A1A5).

4-9. Power for each module is provided by individual module monolithic voltage regulators from the power supply pre-regulated ±20 Vdc distribution busses. Additionally, the power supply distributes +34 Vdc to the RF AMP module and positive five volts dc to the logic devices on the AFC/PLL module.

4-10. AC input power is applied through the AC POWER receptacle (J2) and the RFI filter to the AC MAIN RESET circuit breaker and the POWER ON/OFF switch which provide overload protection and power supply control (see figure 4-3). Fan B1 and transformer T1 have dual primary windings which allow operation from either 115 Vac or 230 Vac. The fan and transformer are connected so that the fan will operate whenever primary ac is applied to the power transformer. Connections from the primary of T1 to the dc meter module allow monitoring of the primary ac input voltage.

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4-11. POSITIVE FIVE VOLT SUPPLY. Full wave rectifier CR1 provides a positive 13 volt dc potential from one of the secondary windings of transformer T1. This voltage is filtered by capacitor C1 and regulated by monolithic regulator U1 to provide a stable five volt source to operate the logic circuitry on the AFC/PLL module. To ensure adequate heat dissipation, U1 is mounted on the power supply side heat sink assembly in the direct air flow from the fan. Diode CR3 provides reverse current protection for regulator U1 if a fault should occur on the input side of the regulator device.

4-12. POSITIVE 34 VOLT SUPPLY. Full wave rectifier CR2 develops a 34 volt dc potential from the second secondary winding of transformer T1. The voltage is filtered by a pi section filter consisting of C2, L1, and C4. Overload protection is provided by the RF AMP SUPPLY fuse (F1). A filtered source of 34 Vdc is applied directly to the RF AMP module to power the internal monolithic +15 volt regulator and an AGC circuit. The output of the RF AMP module AGC circuit is adjusted by the OUTPUT ADJ control (R13) and applied to the base of the power supply +28 Vdc regulator (Q1). Transistor Q1 outputs a positive VCC potential to operate the amplifiers in the RF AMP module. As the RF AMP module OUTPUT ADJ control (R13) is adjusted, the output voltage of transistor Q1 varies which controls the exciter RF output level. Current limiting is provided by circuitry in the RF AMP module which monitors the RF amplifier supply current. Zener diode CR4 provides over voltage protection for the RF output devices. To ensure adequate heat dissipation, Q1 mounts on the power supply rear heatsink assembly in the direct air flow from the fan.

4-13. POSITIVE AND NEGATIVE 20 VOLT SUPPLIES. Positive and negative 34 Vdc is applied to the ±20 Vdc regulator circuits from full wave bridge rectifier CR2. Diodes CR5 and CR6 establish a stable reference to operate the regulators (Q3 and Q4) at the correct positive and negative 20 Vdc output level. Transistors Q5 and Q6 provide foldback current limiting for the regulators by conducting whenever the voltage drop across R4 or R14 reaches a point which causes the respective transistor to turn on. Diodes CR7 and CR8 provide power supply reverse voltage protection for the exciter circuitry. The Darlington output stages (Q3 and Q4) are mounted on the front power supply heatsink assembly in the direct air flow of the fan to ensure adequate cooling. The exciter POWER indicator (2A1DS1) is connected from the negative 20 Vdc supply to ground to indicate power supply operation.

4-14. METERING CIRCUITS.

4-15. The metering circuits provide dc, ac, and peak reading audio measurements of selected critical functions. Using built-in metering functions only, peak audio levels may be established without use of external type approved monitors.

4-16. DC METERING CIRCUITS (2A1A1). All inputs are externally connected to each respective circuit for voltage or current measurements as shown in figure 4-4. A ten position push switch assembly (S1) selects the specific dc signal to be displayed by the MULTIMETER (M1). All inputs consist of dc circuits except the ac line voltage from the power supply which is rec-

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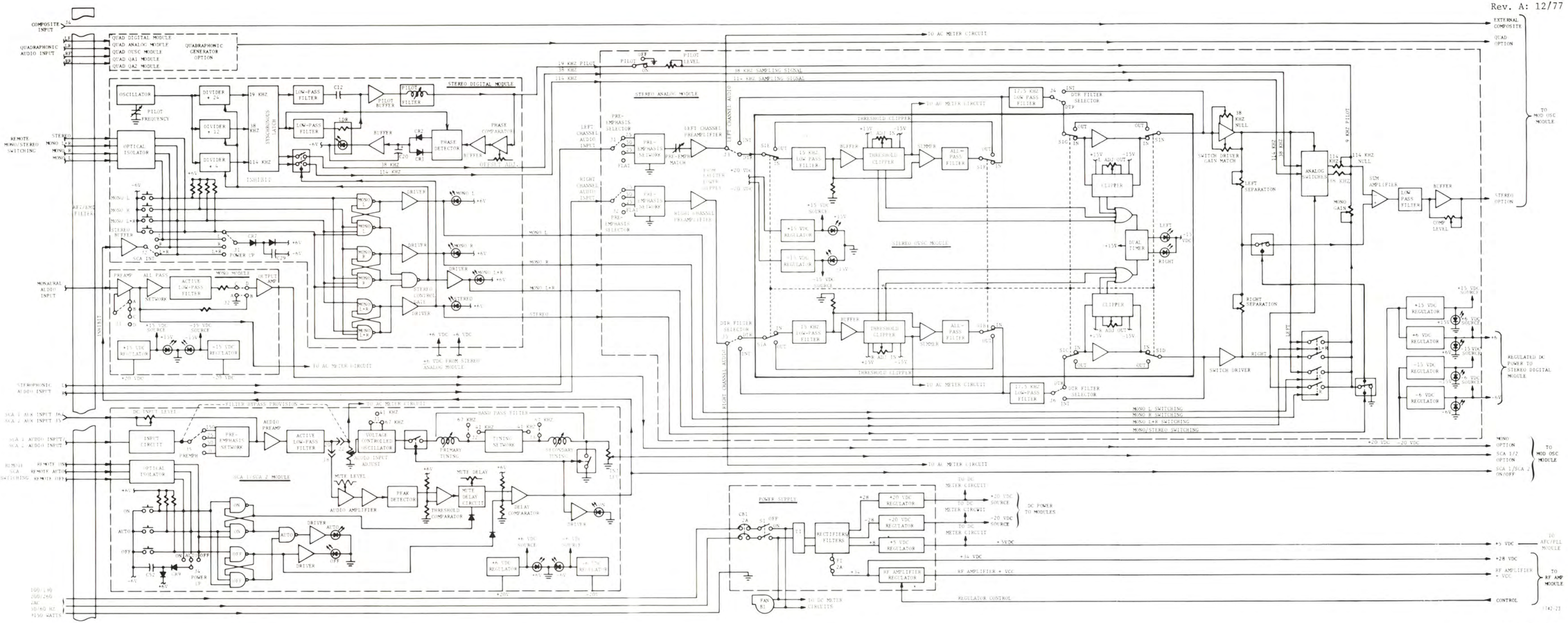


FIGURE 4-1.
OVERALL BLOCK DIAGRAM
(SHEET 1 OF 2)

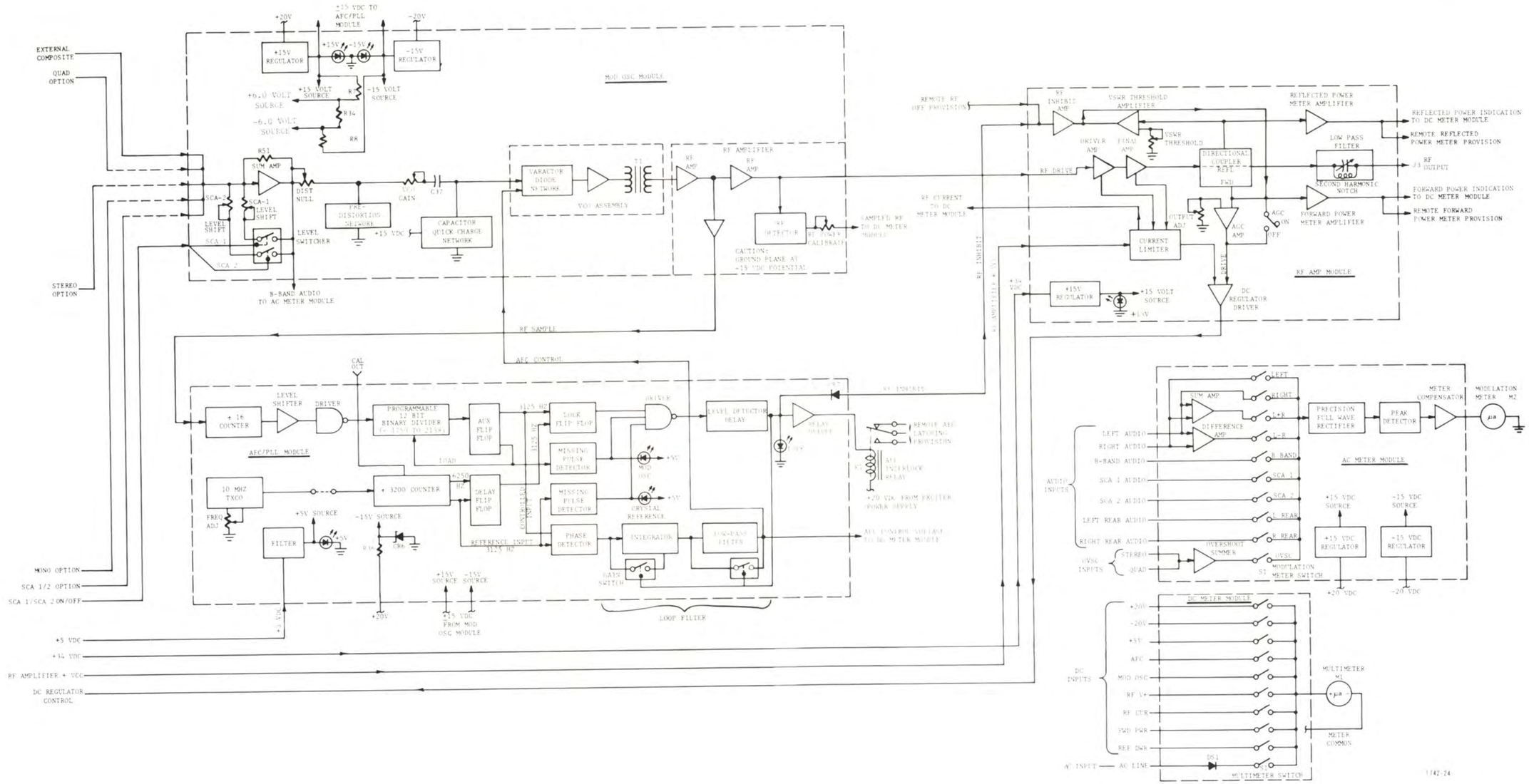


FIGURE 4-1.
OVERALL BLOCK DIAGRAM
(SHEET 2 OF 2)

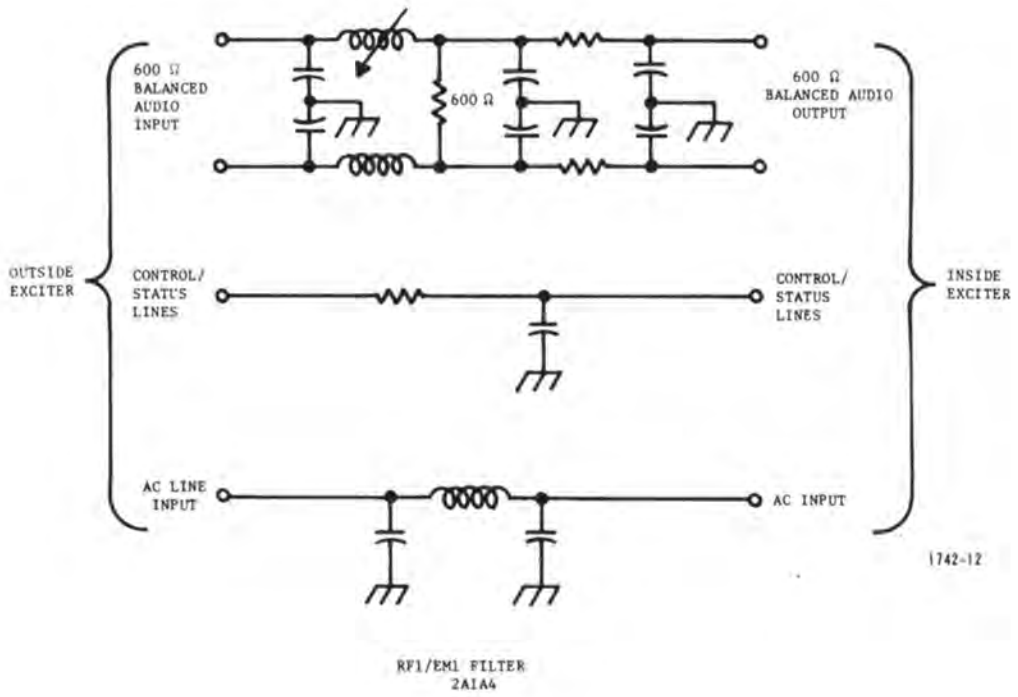


Figure 4-2. RFI Filter Detailed Block Diagram





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tified by diode CR1 for application to the meter circuit. A 100 uA meter movement provides high sensitivity and accuracy.

4-17. AC METERING CIRCUITS (2A1A2). All input signals to the ac metering circuits are connected to each respective source as shown in figure 4-4.

4-18. INPUT CIRCUITS. Each input is provided with a potentiometer to calibrate each function. The left front and right front quadraphonic inputs which function as the left channel and right channel inputs are adjusted for level and directed to the MODULATION meter switch (S1) and to a resistor network (U4) which proportions the input signals between the sum amplifier (U1A) and the difference amplifier (U1B). The sum amplifier (U1A) produces the L + R signal and the difference amplifier (U1B) produces the L - R signal. The remaining audio inputs are adjusted for level and applied to the MODULATION meter switch. The OVSC (overshoot compensator) inputs from either the STEREO OVSC or QUAD OVSC module are summed by amplifier U1C, level adjusted, and applied to the MODULATION meter switch.

4-19. SIGNAL PROCESSING. The signal selected by the MODULATION meter switch is applied to a precision full wave rectifier circuit consisting of U2, CR1, CR2, U3, and associated components. As CR1 and CR2 are enclosed in the U2 feedback loop, the forward turn on voltage characteristic of each diode is compensated. The positive going half cycles appear across R28 and the negative going half cycles appear across R29 with no diode thresholds. Control R21 adjusts the offset voltage of U1 to zero. The rectified signal is applied from the anode of CR2 to the inverting input of U3 and from the cathode of CR1 to the noninverting input of U3. Resistor R30 in the inverting input of U3 provides an adjustment to equalize the positive and negative inputs to U3. The signal is peak detected and amplified by a peak detector comprising Q1, CR3, C8, and Q2. Negative dc feedback is obtained from the output of amplifier Q2 and applied to U3. This provides fast and accurate charging of capacitor C8 in response to voltage peaks. The output amplifier (U1D) acts as a meter compensation amplifier to improve the mechanical response characteristics of the meter. Resistor R48 provides a master gain calibration control for the meter and thermistor R50 provides circuit temperature compensation to maintain meter accuracy over the entire range of operating temperatures.

4-20. POWER. Inputs of positive and negative regulated 20 Vdc are re-regulated into positive and negative 15 Vdc sources to operate the ac meter module internal circuitry.

4-21. MOTHER BOARD ASSEMBLY (2A1A3).

4-22. The mother board provides power, signal, and control inputs, interconnections, and outputs for all plug-in modules through strip con-





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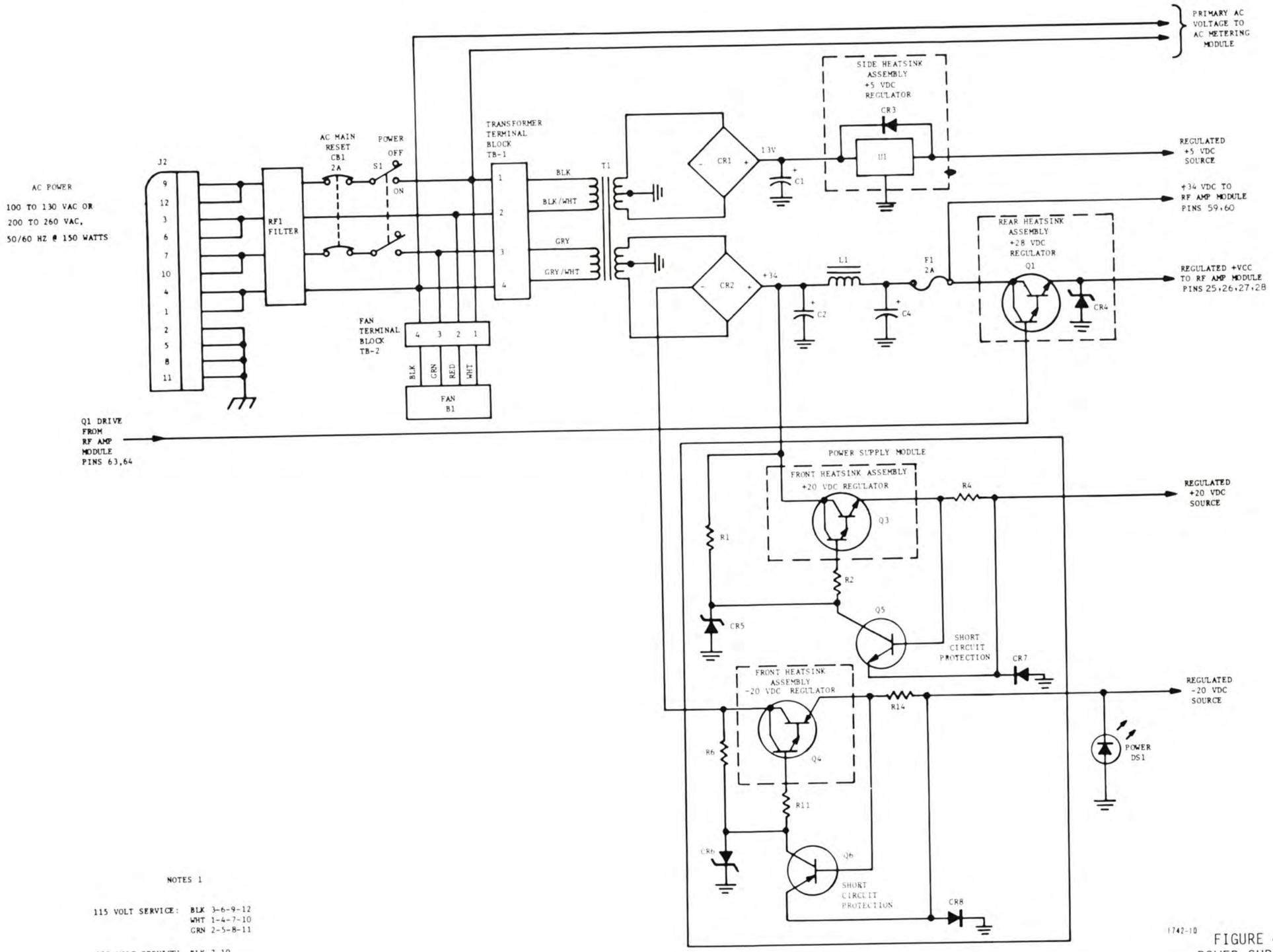


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FIGURE 4-3.
POWER SUPPLY
DETAILED BLOCK DIAGRAM

NOTES 1

115 VOLT SERVICE: BLK 3-6-9-12
WHT 1-4-7-10
GRN 2-5-8-11

230 VOLT SERVICE: BLK 7-10
WHT 3-6
GRN 2-5-8-11
JUMPER 1-9, 4-12

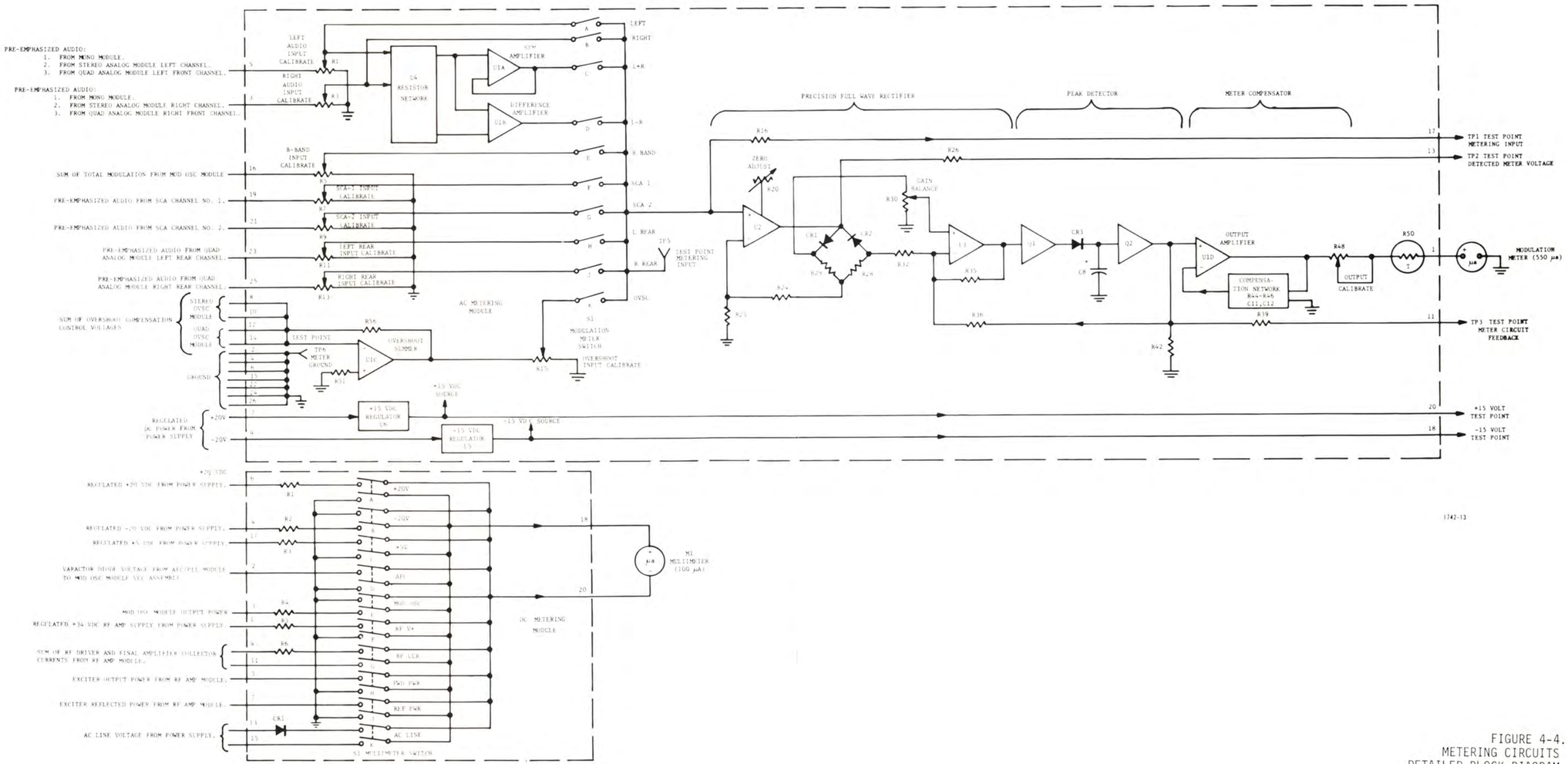


FIGURE 4-4.
METERING CIRCUITS
DETAILED BLOCK DIAGRAM

nectors soldered to the mother board. RF interconnections are provided by 50 ohm micro-strips etched onto the circuit board.

4-23. MONO MODULE (5A1).

4-24. The MONO module accepts an audio input through the RFI filter and provides selectable pre-emphasis and defeatable linear phase low-pass filtering. The resultant signal drives the MOD OSC module.

4-25. INPUT CIRCUIT. A solid state input circuit used in place of a conventional input transformer provides high common mode hum rejection. Pre-emphasis selectable by J1 provides 75 us, 50 us, 25 us, or flat pre-emphasis characteristics. Pre-emphasized monaural audio is applied to the ac meter module and subsequent low-pass filter sections.

4-26. FILTER CIRCUIT. A linear phase low-pass filter comprising an all-pass network (phase equalizer) and an eight pole Butterworth low-pass filter are provided following the input preamplifier. The filters can be used to protect the SCA subcarrier and eliminate ultrasonic audio components or the filter may be jumpered out of the circuit with J2 as desired. The all-pass network has a flat frequency response and tailors the phase characteristics so that the algebraic sum of the phase functions of the all-pass network and the low-pass filter will approximate linear phase. The active low-pass filter protects the SCA channels from high frequency interference and the delay compensator minimizes filter overshoot. A unity gain amplifier provides buffering to drive the MOD OSC module.

4-27. POWER. Inputs of positive and negative regulated 20 Vdc are re-regulated to positive and negative 15 Vdc sources to operate the MONO module internal circuitry. Light emitting diodes provide status indications for the positive (+15V) and negative (-15V) power supplies.

4-28. SCA MODULE (4A1).

4-29. The SCA module includes a dual frequency (41 kHz or 67 kHz) FM subcarrier generator. AC and DC coupled inputs allow audio inputs and SSTV or data transmission on the SCA channels without special additional units. Each SCA module includes a seven pole Butterworth active low-pass filter which allows the use of 150 microsecond pre-emphasis without degrading SCA to stereo crosstalk specifications and allows both the 41 kHz and 67 kHz SCA channels to be operated simultaneously without harmonic interference. Variable automatic or manual muting and remote or local mode switching is also provided.

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4-30. INPUT CIRCUIT. Two inputs are available for each SCA module. An ac coupled input through the RFI filter is applied through the input circuit to the pre-emphasis selector (J5) which allows selection of 150, 75, 50 microsecond pre-emphasis or flat response. The dc coupled input bypasses the RFI filter and pre-emphasis network and is level adjusted by the DC INPUT LEVEL control. Both audio signals are applied to the audio preamplifier and

processed by the low-pass filter. Pre-emphasis audio from the low-pass filter is applied to the ac meter circuit, the audio muting amplifiers, and the voltage controlled oscillator. The filter may be bypassed if desired for special SCA applications.

4-31. FM CIRCUIT. The input signal is level adjusted by the AUDIO INPUT LEVEL control and applied to the voltage controlled oscillator which produces a 41 kHz or 67 kHz frequency modulated RF output as programmed by jumper J1. The FM signal is applied to a doubly tuned band-pass filter in which J2 and J3 determine the filter coupling and center frequency. The INJ LEV control allows adjustment of the module output to the 100 millivolt RMS level required to drive the MOD OSC module. When the SCA is disabled, CMOS switches disconnect the input of the filter and short the filter output to ground.

4-32. MUTE CIRCUIT. Amplification of the low level audio signal from the active low-pass filter to the level required to drive the SCA muting circuit is provided by a two stage high gain amplifier. After amplification, the audio is peak detected and operates a threshold comparator which is referenced to a fixed dc level. As long as the detected peak level of the audio is greater than the comparator dc reference, an output is applied to the mute delay circuit and operates the delay comparator which is also referenced to a fixed dc level. As long as the mute delay circuit outputs a dc level, the delay comparator feeds an SCA ON signal to the MOD OSC module, operates a driver which illuminates the ON indicator, and activates the CMOS control switches. The SCA ON signal from SCA module No. 2 is also applied to the STEREO DIGITAL module to prevent simultaneous 41 kHz SCA and stereophonic operation. The SCA channel is given priority in this situation.

4-33. If the audio input level falls below the threshold comparator dc reference or the audio input is interrupted for longer than the time constant for the delay circuit, the delay comparator will inhibit SCA operation and the ON indicator will go out. The SCA threshold is adjusted by the MUTE level control and the SCA delay is adjusted by the MUTE DELAY control.

4-34. MODE SELECTION. Mode selection is performed by two DC flip flops implemented by four cross-coupled NAND gates. The DC flip flops are controlled by levels rather than transitions.

4-35. When a mode is selected, either by depressing a mode switch or applying a positive 18 to 24 Vdc potential on the selected remote control input, the respective flip flop will latch and inhibit all other functions. The condition will persist until another mode is selected.

4-36. When the ON mode is selected, a connection from the ON flip flop to the mute delay circuit will inhibit the automatic muting function, illuminate the ON indicator and activate the CMOS switches in the FM circuit. When the OFF function is selected, a connection from the OFF flip flop to the





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mute delay comparator inhibits SCA operation. In the AUTO mode, both flip flops are reset and the muting delay circuitry will control the module operation. Light emitting diodes provide indications of the ON, AUTO, and OFF modes.

4-37. Power Up Mode Selection. When power is applied, capacitor C52 is initially discharged. Charging current through jumper J4 will produce a LOW condition until the capacitor is charged on the mode selection line selected by the position of J4, initializing the SCA module in the desired mode. Diode CR9 functions as a disconnect diode which allows manual mode switching after capacitor C52 is charged.

4-38. INDICATORS. Light emitting diodes connected to the control gates through drivers illuminate to indicate selection of a specific mode. The ON indicator illuminates to indicate selection of the ON mode and functions as a mute circuit status indicator when the AUTO mode is selected.

4-39. POWER. Inputs of positive and negative regulated 20 Vdc are re-regulated into positive and negative six Vdc sources to operate the SCA generator internal circuitry.

4-40. STEREO DIGITAL MODULE (3A2).

4-41. The STEREO DIGITAL module produces the signals required to generate the digitally synthesized modulated stereophonic signal, generates the phase controlled 19 kHz pilot signal, and provides stereophonic/monaural mode switching.

4-42. SAMPLING SIGNALS. All frequencies used in the STEREO DIGITAL module are derived from a 456 kHz crystal oscillator. The PILOT FREQUENCY control provides an oscillator frequency adjustment. Synchronous dividers divide the oscillator signal by 24, 12, and 4 to respectively produce the 19 kHz pilot signal and the 38 kHz and 114 kHz sampling signals. The correct phase relationship of each signal is ensured by a synchronous latch. The 38 kHz and 114 kHz signals are output from the module through a CMOS switch which is closed by the stereo-on signal from the module control circuitry.

4-43. PILOT SIGNAL. The 19 kHz pilot frequency is differentially applied to two low-pass filters. Outputs are obtained across capacitor C12 and the light dependent resistor. The sum of the two voltages produces a constant voltage at the input to the pilot buffer amplifier with the pilot signal phase shift controlled by the resistance of the light dependent resistor. The pilot frequency is buffered and applied to a second low-pass filter to ensure the pilot frequency output will be pure sinewave. The center frequency of the second low-pass filter is adjusted by the PILOT FILTER control.

4-44. Pilot Phase Control. The pilot frequency output is sampled by a phase comparator in which the dc offset is adjusted by the AUTOMATIC

PHASE CONTROL OFFSET adjustment. The phase comparator senses zero voltage crossings of the pilot signal and generates a square wave with the same phase. The signal is amplified and applied to a phase detector. As long as the phase of the generated square wave and the reference obtained from the synchronous latch remains the same, neither CR1 or CR2 will conduct. If the phase of the pilot lags the reference, CR2 will conduct and charge C20. If the pilot leads the reference, CR1 will conduct. The charge on C20 is buffered by an amplifier which drives the light dependent resistor and produces a phase shift at the input to the pilot buffer amplifier. Pulses from CR1 or CR2 will continue to charge C20 and operate the light dependent resistor until the pilot phase is corrected.

4-45. CONTROL CIRCUITS. Stereophonic and monaural switching is controlled by three DC flip flops implemented by six cross coupled NAND gates. The flip flops are controlled by levels rather than transitions. When a monaural or stereophonic mode is selected, either by depressing a mode switch or by applying a positive 18 to 24 Vdc potential on the selected remote control input, the respective flip flop latch and reset all other functions. Mode selection for the STEREO ANALOG module is provided by the STEREO DIGITAL module control circuits.

4-46. If the MONO L switch is depressed, the Mono L flip flop will set and reset the remaining flip flop. The remaining flip flops are controlled in a similiar manner and remain reset until another mode is selected. The output of each flip flop is applied to the stereo control gate which outputs a LOW condition that inhibits output of the stereo sampling signals to the STEREO ANALOG module and halts the synchronous divider. When the STEREO switch is depressed all the gates are reset and the inhibit from the stereo control gate is removed. This enables stereophonic operation and stereo sampling signals are output to the STEREO ANALOG module. Individual logic levels output from the STEREO DIGITAL module provide automatic mono/stereo mode switching for the STEREO ANALOG module circuitry.

4-47. SCA-2 Interlock. Operation of two SCA channels (67 kHz and 41 kHz) during stereophonic programming is not desired as interaction between the stereophonic signal and the 41 kHz SCA channel will produce mutual interference. If operation of the SCA-2 module (41 kHz) is attempted during stereophonic programming, a positive six volt dc potential from the SCA-2 module applied to the SCA INTERLOCK (J2) circuit of the STEREO DIGITAL module will cause the stereo generator to default to the monaural mode programmed by J2. Operation of the module mode selection circuit is inhibited until SCA-2 is switched off. Then the STEREO DIGITAL module may be manually switched to the desired monaural or stereo mode.

4-48. Power Up Mode Selection. When power is applied, capacitor C29 is initially discharged. Charging current through jumper J1 will produce a LOW condition until the capacitor is charged on the mode selection line selected by the position of J1, initializing the SCA module in the desired mode. Diode CR7 functions as a disconnect diode which allows manual mode switching after capacitor C29 is charged.





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4-49. INDICATORS. Light emitting diodes connected to the control gates through drivers illuminate to indicate the mode of operation.

4-50. POWER. Inputs of positive and negative six Vdc from regulators in the STEREO ANALOG module function as voltage sources to operate the STEREO DIGITAL module internal circuitry.

4-51. STEREO ANALOG MODULE (3A1).

4-52. The STEREO ANALOG module accepts the stereophonic audio inputs and generates the stereophonic composite signal with switching and pilot signals input from the STEREO DIGITAL module. Solid state circuits used in place of conventional input transformers provide high common mode hum rejection and selectable pre-emphasis. Dynamic transient response (DTR) low-pass filtering is accomplished by the STEREO OVSC module and the two conventional 17.5 kHz audio low-pass filters in the STEREO ANALOG module. The digitally synthesized modulation sampling circuits and the composite filters are also included within the module.

4-53. INPUT CIRCUIT. The two stereo audio signals are input through the RFI filter to individual preamplifiers. A solid state input circuit used in place of conventional input transformer provides high common mode hum rejection. Pre-emphasis of 75 us, 50 us, 25 us, or flat response is selectable by J1 for the left channel and by J2 for the right channel. The PRE-EMPH MATCH control in the input to the left channel preamplifier allows adjustment of the left channel pre-emphasis circuit to match the right channel pre-emphasis characteristics for stereo crosstalk adjustments.

4-54. FILTER CIRCUIT. Normally the STEREO ANALOG module will be used with a STEREO OVSC module in which the STEREO ANALOG module filters are used as part of the DTR filtering process. However, the STEREO ANALOG module includes its own audio low-pass filters and can function without the STEREO OVSC module if desired. The pre-emphasized audio from the input preamplifiers is applied to the ac meter circuit and the DTR filter selectors (J3 and J4 for the right channel and J5 and J6 for the left channel). The DTR filter selectors select the OVSC MODULE DTR filter circuitry or allow use of the STEREO ANALOG module 17.5 kHz low-pass filters as desired.

4-55. The pre-emphasized and filtered audio is next applied to the switch driver in each channel. The gain of the left channel driver is adjustable with the GAIN MATCH control. The 38 KHZ NULL control minimizes amplifier dc offset between the left and right channel switch drivers. The LEFT SEPARATION and RIGHT SEPARATION controls allow adjustment to obtain maximum channel separation.

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4-56. OUTPUT CIRCUIT. The output of the switch drivers is applied to the analog switches. The 114 kHz and 38 kHz signals from the STEREO DIGITAL module controls the analog switches which generate the DSM sampling function. The 114 KHZ NULL control adjusts the 114 kHz switch output to

cancel the third harmonic component of the 38 kHz switch (114 kHz). The 19 kHz pilot signal from the STEREO DIGITAL module is controlled by the PILOT ON/OFF switch and level adjusted by the PILOT LEVEL control. The DSM sampling signal and the pilot signal are applied to the inverting input of the sum amplifier. A portion of the L + R signal obtained from the separation controls is applied to the non-inverting input of the sum amplifier drives the composite low-pass filter to eliminate the fifth harmonic and higher ordered harmonics of the 38 kHz signal. The output buffer provides signal amplification and isolation. The COMP LEVEL control adjusts the composite signal level output to suit the input requirements of the MOD OSC module.

4-57. In monaural operation the sampling signals and the pilot signal are inhibited. The mode switching arrangement selects the desired monaural signal. The monaural level is adjusted by the MONO GAIN control.

4-58. MODE SWITCHING. Mode switching is accomplished by CMOS dc flip flops controlled by discrete individual inputs for stereo, mono left, mono right, and mono left plus right.

4-59. Stereophonic Operation. If stereophonic operation is selected, a positive six volt dc level output from the STEREO DIGITAL module closes two CMOS switches between the separation controls which applies a portion of the L + R signal required for stereo operation to the non-inverting input of the sum amplifier. A second CMOS switch pair inhibits monaural operation by grounding the monaural audio line. The 114 kHz and 38 kHz sampling signals and the pilot signal are enabled in the STEREO DIGITAL module.

4-60. Monaural Operation. If a monaural mode is selected, a LOW placed on the stereo line will open the stereo sampling switches. A HIGH output from the STEREO DIGITAL module on the selected monaural mode line will close the appropriate CMOS switch and connect the selected audio source to the sum amplifier input through the MONO GAIN control. The 114 kHz and 38 kHz sampling signals and the pilot signal are automatically inhibited by control circuitry in the STEREO DIGITAL module which prevents stereo sampling.

4-61. POWER. Inputs of positive and negative regulated 20 Vdc are re-regulated into positive and negative fifteen and six Vdc sources to operate the STEREO ANALOG module internal circuitry. Positive and negative six Vdc is applied to the STEREO DIGITAL module internal circuitry. The STEREO DIGITAL module CMOS logic operates between the positive and negative six Vdc potentials and is not referenced to common ground. The +15V, -15V, +6V, and -6V light emitting diodes indicate operation of each power supply.

4-62. STEREO OVSC MODULE.

4-63. The STEREO OVSC (overshoot compensator) module provides 15 kHz low-pass filtering of the left and right channel audio signals to prevent interference with the 19 kHz pilot signal and eliminates interference be-

tween the L + R and L - R signals. A special filtering process limits overshoot to a maximum of two percent to prevent overmodulation. This minimum overshoot allows high levels of modulation to be maintained without degrading signal quality. Indicators on the module front panel and outputs to the ac meter module aid in level setup and provide overshoot limiting indications during operation.

4-64. Normally the STEREO ANALOG module will be used with a STEREO OVSC module in which the STEREO ANALOG module filters are used as part of the DTR filtering process. However, the STEREO ANALOG module includes its own audio low-pass filters and can function without the STEREO OVSC module. The IN/OUT switch (S1) is provided on the STEREO OVSC module to bypass the overshoot control circuitry and provide conventional low-pass filtering if desired.

4-65. INPUT THRESHOLD. Transformerless input amplifiers on the STEREO ANALOG module drive a dual 15 kHz low-pass filter on the STEREO OVSC module. The low-pass filter output is amplified by a buffer and applied to a threshold clipper which contains an active programmable zener diode. The active zener voltage is adjusted by the L ADJ IN or R ADJ IN controls to the peak voltage level corresponding to 100% modulation. The threshold clipper passes only peaks exceeding 100% modulation (overshoots). The sum amplifier subtracts the overshoots from the 15 kHz low-pass filter output. The sum is applied to an all-pass filter phase equalizer which is flat in frequency response but produces a phase shift dependent upon frequency.

4-66. OUTPUT THRESHOLD. The output of the all-pass filter is looped out of the STEREO OVSC module, through the STEREO ANALOG module 17.5 kHz low-pass filter, and back to the STEREO OVSC module. The all-pass filter phase characteristic is added to the 17.5 kHz low-pass filter phase characteristic to yield linear phase. The filtered audio drives a clipper circuit containing an active programmable zener diode which is adjusted by the L ADJ OUT and R ADJ OUT controls to pass audio levels corresponding to less than 100% modulation only. The overshoot compensated audio is then output to the STEREO ANALOG module.

4-67. INDICATORS. Outputs from the left and right clipper circuits are applied to wired OR comparators. Whenever an overshoot limiting condition exists, an output from the respective OR circuit will drive half of the dual timer used as a one shot to illuminate the LEFT and RIGHT indicators.

4-68. POWER. Inputs of positive and negative regulated 20 Vdc are re-regualted into positive and negative fifteen volt dc sources to operate the STEREO OVSC module internal circuitry.

4-69. AFC/PLL MODULE.

4-70. The AFC/PLL module provides phase locked control of and 50 kHz channel frequency between 87.5 MHz and 108 MHz. All FM channels are synthe-

sized from a stable 10 MHz temperature compensated crystal oscillator (TXCO). As the frequency reference is established at 10.0 MHz, the station frequency may be compared directly with a broadcast frequency standard such as WWV using a communications receiver and the front panel CAL OUT test point. Channel spacing is field programmable in 50 kHz increments to accommodate any domestic or international channel assignment. The AFC/PLL module interfaces with the MOD OSC module for accurate frequency control.

4-71. INTERNAL REFERENCE. A frequency reference is provided by a 10.0 MHz temperature compensated crystal oscillator (TXCO). The unit comprises a sealed modular oscillator with a matched compensation network to ensure accuracy throughout a wide range of ambient temperatures. The TXCO frequency is adjusted by the FREQ ADJ control. A wire jumper allows substitution and isolation of the TXCO for troubleshooting purposes.

4-72. The TXCO drives a divide by 3200 counter. Frequency multiples of 2.5 MHz up to 25.0 MHz are available at the CAL OUT front panel jack to assist in calibration. The divider outputs two 3125 Hz square waves in quadrature. The leading signal is used as a reference for the phase detector and the crystal reference missing pulse detector. The $90^{\circ}$ lagging signal is used by the lock detector flip-flop to determine when the carrier is correctly locked on frequency.

4-73. RF FREQUENCY DIVIDERS. An on-frequency RF output from the MOD OSC module is input to the divide by 16 counter which divides the input frequency down to the 6 MHz range. A level shifter couples the emitter-coupled-logic (ECL) signal to transistor-transistor logic (TTL) levels.

4-74. Programmable Divider. A 12 bit programmable binary divider provides division of the 6 MHz signal to 3125 Hz. The counter is programmable with wire jumpers to the flip-flop data inputs to divide the input by a programmable factor between 1750 and 2158. The counter is originally set to the programmed number. When the counter fills to all ONES, a pulse is output to the auxiliary flip-flop. On the next clock pulse, an output from the auxiliary flip-flop resets the counter to the number entered at the data inputs by the wire program jumpers. The counter begins its count again with the succeeding clock pulse.

4-75. LOCK CIRCUIT. Three requirements must be met before the lock detector will recognize a frequency locked condition. The programmable divider chain must be producing a signal, the reference divider chain must be producing a signal, and the two chains must have less than $90^{\circ}$ phase difference. After these three conditions are acheived for five seconds, the lock circuit will indicate a locked condition exists.

4-76. Lock Detector. The $90^{\circ}$ delayed pulse from the delay flip-flop (reference) is input to the lock flip-flop D input and the output of the auxiliary flip-flop (programmable divider) operates as the lock flip-flop clock. As long as the leading 3125 Hz reference and the programmable divider

negative transitions are separated $0^{\circ} \pm 90^{\circ}$ in phase, the output of the lock flip-flop remains HIGH. If the loop becomes unlocked, the signal from the programmable divider will drift in phase with respect to the reference. If the clock occurs when the delayed 3125 Hz signal is LOW, the lock flip-flop will output a LOW state and signal a frequency unlocked condition.

4-77. Missing Pulse Detectors. A dual retriggerable one-shot used as the missing pulse detectors watches the programmable divider reset line and the crystal reference divider. As long as pulses are present at the inputs to the detectors, the one-shots will remain HIGH. If missing pulses occur in either source, the respective one-shot will not be retriggered and output a LOW condition to signal a frequency unlocked condition. The MOD OSC and the CRYSTAL REFERENCE indicators provide visual indications of the status of the two divider chains.

4-78. Output Circuit. The outputs of the lock flip-flop and the missing pulse detectors are applied to a NAND gate. If all the inputs are present at the NAND gate, the output of the level detector/delay circuit will illuminate the LOCK indicator to signify a frequency locked condition. The output also operates the AFC interlock relay (K1) which provides remote AFC latching. Any missing input to the NAND gate will be detected by the level detector/delay circuit. If a frequency unlocked condition is detected, the level detector delay circuit immediately outputs an inhibit signal which turns off the LOCK indicator, deenergizes the AGC interlock relay, and provides a signal to the RF AMP module which inhibits the exciter RF output.

4-79. PHASE LOCKED LOOP. The phase detector is a flip-flop type with a three level output. If both reference and controlled inputs have zero phase difference, a 1.4 volt reference potential is output. If the controlled input lags in phase, the phase detector will output pulses negative with respect to 1.4 volts with the pulse width proportional to the lagging phase angle. If the controlled input leads in phase, the phase detector will generate positive pulses with the pulse width proportional to the leading phase angle. The pulses are filtered and applied to the DC meter module and the MOD OSC module VCO assembly varactor diodes which control the exciter RF frequency. A positive voltage to the MOD OSC module will increase the frequency and a negative voltage to the MOD OSC module will decrease the frequency. The phase locked loop is closed by the connection from the MOD OSC module output to the AFC/PLL module divide by 16 counter input.

4-80. Bistable Loop. The phase locked loop used in the module has bistable characteristics which reduce lock-up time to a minimum. When the loop is out of lock, a CMOS switch arrangement operated by the lock detector enables a high rate of correction. When the lock detector senses a locked condition the loop correction characteristic is slowed for optimum transmission of low frequencies.

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4-81. POWER. An input of positive five volts dc from the exciter power supply is internally filtered to operate the logic circuitry. The +5V indicator provides an indication of the operation of the five volt source. An additional input of +20 Vdc applied through R36 is stabilized by zener diode CR6 to +15 Vdc. Re-regulated ±15 Vdc inputs from the MOD OSC module provide ±15 Vdc potentials to operate the AFC/PLL module loop filter circuitry.

4-82. MOD OSC MODULE (2A4).

4-83. The MOD OSC module contains the voltage controlled oscillator (VCO) assembly which generates the frequency modulated RF carrier from a composite signal input. The RF output frequency is controlled by a dc control voltage obtained from the AFC/PLL module as part of the phase locked loop. The module also provides automatic level switching for different combinations of SCA, stereophonic, and monaural operation.

4-84. INPUT CIRCUIT. The dc coupled quadraphonic, stereophonic, or monaural composite signals and the ac coupled SCA and external composite signals are input to the module and combined in the summing amplifier to obtain a total modulation signal. Whenever an SCA module is enabled, a corresponding CMOS switch is closed by a positive six volt potential on the appropriate control line from the specific SCA module. The CMOS switches shunt the feedback resistor (R51) with additional resistance to reduce the gain of the amplifier. The gain reduction is adjusted to the injection level of the particular SCA signal to maintain 100% total modulation for all combinations of SCA, stereophonic, or monaural modes.

4-85. PREDISTORTION NETWORK. The modulating signal from the composite amplifier is applied to a diode-resistor predistortion network. The total modulation signal is slightly stretched in the positive direction and slightly compressed in the negative direction. This effect is required to cancel the slightly nonlinear characteristics of the VCO assembly. The amount of predistortion is adjusted by the DIST. NULL control.

4-86. VCO ASSEMBLY (2A4A1). The voltage controlled oscillator comprises a varactor diode tuned oscillator using field effect devices in an individual encapsulated subassembly. The unit accepts inputs of predistorted total modulation and an AFC signal from the AFC/PLL module and generates an FM signal on the operating frequency. In event of VCO failure, it is possible to repair the encapsulated assembly by cutting the clear resin from the faulty component and pouring in new resin after the repair is complete.

4-87. Modulation Input. Predistorted total modulation is applied to the VCO GAIN control which compensates for VCO modulation sensitivity variations and is coupled through capacitor C37 to the VCO input. As the time constant of capacitor C37 is many times the AFC/PLL module lockup time, the capacitor must be quickly charged to ensure a stable locked condition. When power is first applied, C37 is quickly charged to a potential very close to the steady state value by a fast charge circuit. The circuit then decouples itself from the modulation circuit and presents a high impedance input to the varactor diode network.





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4-88. AFC Input. The frequency output of the VCO is determined by the AFC voltage to the VCO assembly from the AFC/PLL. If the VCO frequency is lower than the internal reference in the AFC/PLL module, a positive going potential is input to the VCO assembly to increase the output frequency. If the VCO frequency is higher than the internal reference in the AFC/PLL module, a negative going potential is input to the VCO assembly to decrease the output frequency. A steady dc potential on the correction line indicates the VCO frequency and the frequency of the internal reference agree.

4-89. Output Circuit. A frequency modulated RF carrier is output from the oscillator stage, amplified, and inductively coupled by transformer T1 to an RF amplifier chain.

4-90. OUTPUT. Two RF outputs from the module are provided. One output drives the AFC/PLL module divide by 16 counter. The remaining output is amplified to the level required to drive the RF AMP module input circuitry. An RF detector circuit samples the RF drive voltage to provide an indication of the RF output level. The RF POWER CALIBRATE control provides an adjustment to calibrate the meter indication.

4-91. POWER. Inputs of positive and negative regulated 20 Vdc are re-regulated into ±15 Vdc sources to operate the MOD OSC module and the AFC/PLL module internal circuitry. Light emitting diodes provide a status indication of the operation of the positive (+15V) and negative (-15V) fifteen volt power supplies. Additionally, positive and negative 6.0 Vdc sources are produced from a series circuit consisting of R7, R34, and R8 from the ±15 volt potentials to operate the CMOS level switching circuits.

4-92. RF AMP MODULE.

4-93. The RF AMP module comprises two class C stages which accept an RF input from the MOD OSC module and provide a continuously variable three to fifteen watt RF output. An internal AGC circuit ensures a stable RF output level. Automatic VSWR shutdown, off frequency inhibit provisions, and power supply current limiting provide automatic module operation.

4-94. RF CIRCUIT. Drive is input to the RF amplifier from the MOD OSC module at a level of 250 milliwatts. The RF amplifier provides approximately 20 dB of gain to output a continuously adjustable level from three to fifteen watts. Amplifier tuning is not required as wideband impedance matching is used throughout the amplifier circuits. The RF is output along a microstrip through a directional coupler and low-pass filter implemented with microstrip techniques. The low-pass filter is tuned by the SECOND HARMONIC NOTCH adjustment to reduce RF harmonics to a minimum level. The RF carrier is output from J3 on the rear of the exciter at an impedance of 50 ohms.

4-95. DIRECTIONAL COUPLER. The RF power amplifier includes a directional coupler produced in printed circuit form using microstrip techniques

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which samples the forward and reflected power. The power is detected and coupled to the metering circuits. The forward and reflected power indicaitons may be remotely monitored from connections on the rear of the exciter.

4-96. AMPLIFIER INHIBIT. The directional coupler reflected power output is monitored by an adjustable threshold device. Whenever the reflected power exceeds a preset level, the RF amplifier output is limited to prevent overdissipation of the RF amplifier devices. If a frequency unlocked condition exists between the AFC/PLL module and the MOD OSC module, an input from the AFC/PLL module will inhibit the RF output until the frequency is again within tolerance. The RF shutdown provision is remoteable from connections on the rear of the exciter.

4-97. RF AMPLIFIER AGC. The directional coupler forward power output applies a dc voltage proportional to forward power output to the AGC amplifier inverting input. The AGC reference applied to the non-inverting input is adjusted by the OUTPUT ADJ control. As the RF output power increases or decreases, the AGC amplifier output to the dc regulator will decrease or increase proportionally. The dc regulator compares the drive from the AGC amplifier with a sample of the RF amplifier collector voltage and drives the transistor in the exciter power supply which in turn lowers or raises the voltage to the RF amplifier. A current limiting stage samples RF amplifier current and initiates limiting at two amperes of supply current. The automatic level control is disabled by the AGC ON/OFF switch which allows manual carrier level control.

4-98. POWER. Filtered positive 34 Vdc obtained from the exciter power supply is regulated into a positive 15 Vdc source to operate the RF AMP module internal circuitry. The +15V indicator provides a status indication of the internal power supply.





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SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2. This section provides preventive maintenance checks, cleaning, corrective maintenance and troubleshooting information.

5-3. PURPOSE.

5-4. The information contained in this section is intended to provide guidance to establish a comprehensive maintenance program to promote operational readiness and eliminate downtime. Particular emphasis is placed on preventive maintenance and record keeping functions.

5-5. STATION RECORDS.

5-6. The importance of keeping station performance records cannot be overemphasized. Separate logbooks should be maintained by operation and maintenance activities. These records can provide data for predicting potential problem areas and analyzing equipment malfunctions.

5-7. TRANSMITTER LOGBOOK.

5-8. As a minimum performance characteristic, the exciter should be monitored (using front panel indicators) and results recorded in the transmitter logbook at each shift change or at least once per day.

5-9. MAINTENANCE LOGBOOK.

5-10. The maintenance logbook should contain a complete description of all maintenance activities required to keep the exciter operational. A list of maintenance information to be recorded and analyzed to provide a data base for a failure reporting system is as follows:

| | |
|---|---|
| DISCREPANCY | Describe the nature of the malfunction. Include all observable symptoms and performance characteristics. |
| CORRECTIVE ACTION | Describe the repair procedure used to correct the malfunction. |
| DEFECTIVE PART(S) | List all parts and components replaced or repaired. Include the following details:<br>a. COMPONENT TIME IN USE<br>b. COMPONENT PART NUMBER<br>c. COMPONENT MAJOR ASSEMBLY<br>d. COMPONENT REFERENCE DESIGNATOR |

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| | |
|---|---|
| SYSTEM ELAPSED TIME | Total exciter time on. |
| NAME OF REPAIRMAN | Person who actually made the repair. |
| STATION ENGINEER | Indicates chief engineer noted and approved the repair. |

5-11. SAFETY PRECAUTIONS.

5-12. The exciter design provides safety features which ensure that no potentials are accessible to operational personnel from the front panel with the access door closed. Additionally, no high voltage points are readily accessible to personnel unless the exciter case is disassembled. Low voltages are used throughout the module circuitry, however maintenance with power energized is always hazardous and caution should be observed. This is particularly true of the RF amplifier module where high RF potentials exist at high impedance points. It is possible to receive painful but usually not injurious RF burns from the 15 watt output stage. Component or module replacement with power on is not recommended.

5-13. PREVENTIVE MAINTENANCE.

5-14. Preventive maintenance is a systematic series of operations performed periodically on equipment. As these procedures cannot be applied indiscriminately, specific instructions are necessary.

a. Visual inspection is the most important preventive maintenance operation because it determines the necessity for the others. Become thoroughly acquainted with normal operating conditions in order to recognize and identify abnormal conditions readily. The remedy for most visible defects is obvious, however care must be taken if heat damaged components are located. Overheating is usually a symptom of trouble. It is essential to determine the actual cause of overheating before the heat damaged component is replaced, otherwise the damage will be repeated.

b. Check parts for overheating, especially mechanical parts such as the fan. The lack of proper ventilation or the existence of some defect can be detected and corrected before serious trouble occurs. Become familiar with operating temperatures in order to recognize deviations from normal temperature.

c. Tighten loose hardware. Do no tighten indiscriminately as fittings may be damaged or broken when they are tightened beyond the pressure for which they are designed.

d. Clean parts when inspection shows that cleaning is required.

e. Make adjustments when inspection shows that adjustments are necessary to maintain normal operation.

f. Lubricate mechanical surfaces to prevent wear and to keep the equipment operating normally. Do not over lubricate.

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g. Paint surfaces with the original type of paint (use prime coat if necessary) when inspection shows worn or broken paint film.

5-15. FAN MAINTENANCE.

5-16. Inspect the fan and equipment for dust accumulation monthly. Remove dust with a vacuum cleaner and brush. Check the fan for wear. The fan bearings are sealed and fans which are noisy or show wear require replacement of the fan.

5-17. MAINTENANCE OF COMPONENTS.

5-18. The following paragraphs provide information for component maintenance.

5-19. SEMICONDUCTORS. The best check of semiconductor performance is actual circuit operation. When semiconductors are replaced, the operation of associated circuits may be affected and should be checked. Replacement semiconductors should be of the original type or a recommended direct replacement. Preventive maintenance of semiconductors is accomplished by performing the following steps:

a. Inspect the semiconductors and surrounding area for accumulations of dirt or dust.

b. Use compressed dry air and a brush to remove dust from the area.

c. Examine all semiconductors for loose connections or corrosion.

5-20. CAPACITORS. Preventive maintenance of capacitors is accomplished as follows:

a. Examine all capacitor terminals for loose connections or corrosion.

b. Ensure that component mountings are tight.

c. Examine the body of each capacitor for swelling, discoloration or other evidence of breakdown.

d. Inspect electrolytic capacitors for signs of leakage.

e. Use compressed dry air and a brush to remove dust from the area.

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5-21. FIXED RESISTORS. Preventive maintenance of fixed resistors is accomplished by the following steps:

a. Examine resistors for dirt or signs of overheating. Discolored, cracked or chipped components indicate a possible overload.

b. When replacing a resistor ensure the replacement value corresponds to the original component.

c. Use compressed air and a brush to remove dust from the area.

5-22. VARIABLE RESISTORS. Preventive maintenance of variable resistors follows:

a. Inspect and tighten all loose mountings and connections.

b. If necessary, clean components with a brush and dry compressed air.

5-23. TRANSFORMERS. Preventive maintenance of transformers is accomplished by performing the following:

a. Feel each transformer soon after power removal for signs of overheating.

b. Inspect each transformer for dirt, loose mounting brackets and rivets, loose terminal connections and insecure connecting lugs. Dust, dirt or moisture between terminals may cause flashovers.

c. Tighten loose mounting lugs, terminals or rivets.

d. Use compressed air and a brush to remove dirt from the area.

5-24. FUSES. Preventive maintenance of fuses is accomplished by the following:

a. When a fuse blows determine the cause before installing a replacement.

b. Inspect fuse caps and mounts for charring and corrosion.

c. Examine fuse clips for dirt, improper tension, and loose connections.

d. Dust with a small brush if cleaning is required.





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5-25. METERS. Preventive maintenance of meters is accomplished as follows:

a. Inspect meters for loose, dirty or corroded mountings and connections.

b. Check for defective cases and cover glasses.

c. Tighten loose mountings or connections. Since meter cases are made of plastic, exercise care to prevent breakage.

d. Clean meter cases and glass cover with a dry cloth.

e. Remove dirt from mountings and connections with a brush if required.

5-26. RELAYS. Replace hermetically sealed relays if defective. Non-hermetically sealed relays are considered normal if:

a. The relay is mounted securely.

b. Connecting leads are not frayed and the insulation is not damaged.

c. Terminal connections are tight and clean.

d. Moving parts travel freely.

e. Spring tension is correct.

f. Contacts are clean, adjusted properly, and make good contact.

g. The coil shows no signs of overheating.

h. The assembly parts are clean and not corroded.

5-27. SWITCHES. Preventive maintenance of switches is accomplished by checking the following:

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a. Inspect switches for defective mechanical action or looseness of mounting and connections.

b. Examine cases for chips or cracks.

c. Operate the switches to determine if each moves freely and is positive in action. In gang and wafer switches, the wiper should make good contact with the stationary member.





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d. Tighten all loose connections and mountings.

e. Clean any dirty connection or switch with dry compressed air and a brush as required.

5-28. PRINTED CIRCUIT BOARDS. Preventive maintenance of printed circuit boards is accomplished by checking the following:

a. Inspect the printed circuit boards for cracks or breaks.

b. Inspect the wiring for open circuits or raised foil.

c. Check components for breakage or discoloration due to overheating.

d. Clean off dust and dirt with dry compressed air and a brush as required.

e. Use standard practices to repair solder connections with a low wattage soldering iron.

5-29. CORRECTIVE MAINTENANCE.

5-30. The maintenance philosophy of the MS-15 FM exciter consists of problem isolation to a specific area or replaceable module and subsequent isolation and replacement of the defective component or module. Further troubleshooting in each applicable module publication provides isolation to specific components.

5-31. Corrective maintenance for the transmitter is limited by the objective of minimum down time. Maintainability and care are considerably simplified for operation and maintenance personnel as the MS-15 FM exciter is designed and built with highly reliable and proven elements to minimize down time. All controls are adjustable in view of the meters. Internal components may be accessed through the front panel and the removable top and rear panels. An extender board (Harris PN 992 4989 001) is provided with the exciter to assist in troubleshooting.

5-32. TROUBLESHOOTING.

5-33. In event of problems, the trouble area must first be isolated to an exciter input, the MS-15 power supply, an exciter module, or the exciter load. Most troubleshooting consists of visual checks. The MODULATION meter, MULTIMETER, fuse F1, circuit breaker CB1, and the indicators should be used to determine in which area the malfunction exists. All module power supplies are equipped with LEDs to indicate the module power supply status. If all LEDs are out or a consistent pattern of dark LEDs exists, a power supply malfunction or distribution bus fault exists. If a single LED is out, either the monolithic voltage regulator on the module has failed in the open condition or a short exists on the module and the module regulator is in the current limiting mode.





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5-34. Once the trouble is isolated to a specific area, refer to the theory section of this manual for circuit discussion to aid in problem resolution. Table 5-1 lists typical trouble symptoms pertaining to the overall exciter operation with references to fault isolation diagrams listing probable causes and corrective actions. A corrective action given for a trouble symptom is not necessarily the only answer to a problem, it only tends to lead the repairman into the area that may be causing the trouble. If a particular MS-15 module is determined faulty, a reference to the individual module maintenance publication will be listed. In event parts are required, refer to Section VI, Parts List.

5-35. COMPONENT REPLACEMENT. The circuit boards used in the MS-15 are of the double-sided plated-through type. This means that there are traces on both sides of the board and the through-holes contain a metallic plating. Because of the plated-through holes, solder creeps up into the hole. This requires a more sophisticated technique for component removal in order to avoid damage to the traces on the board. Excessive heat of any point on the board will cause damage.

5-36. To remove a component from a double-sided board, the leads of the defective component should be cut from the body while the leads are still soldered to the board. The component is then discarded and each lead is heated independently and pulled out of the hole. Each hole may then be cleared of solder by carefully heating with a low wattage iron and removing the residual solder with a solder vacuum tool.

5-37. The new component is installed in the usual way and soldered from the bottom side of the board. If no damage has been done to the plated-through hole, soldering of the top side is not required. However, if the removal procedure did not progress smoothly, each lead should be soldered at the top side to prevent potential intermittent problems.

5-38. After soldering remove residual flux. There are solvents available in electronic supply houses which are useful. The board should then be checked to ensure the defluxing operation has removed the flux and not just smeared it about so that it is less visible. While rosin flux is not normally corrosive, it will absorb moisture and become conductive enough to cause deterioration in specifications over a period of time.

5-39. TECHNICAL ASSISTANCE.

5-40. Technical assistance and troubleshooting recommendations are available from Harris Field Service Department during normal working hours. Emergency technical service is available 24 hours a day. Telephone 217/222-8200 to contact the Field Service Department or address correspondence to Field Service Department, Harris Corporation Broadcast Products Division, 123 Hampshire Street, Quincy, Illinois 62301, USA.

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Table 5-1. MS-15 Fault Isolation Index

| SYMPTOM | DEFECT/REFERENCE |
|---|---|
| NO RF CARRIER OUTPUT | Figure 5-1 |
| RF CARRIER LEVEL WILL NOT ADJUST | Defective RF AMP. module. Refer to publication 888 1742 009. |
| INADEQUATE CARRIER LEVEL OUTPUT | Figure 5-2 |
| FREQUENCY CONTROL CIRCUIT WILL NOT LOCK (AFC/PLL MODULE LOCK INDICATOR NOT ILLUMINATED). | Figure 5-3 |
| EXCITER OFF FREQUENCY (AFC/PLL MODULE LOCK INDICATOR ILLUMINATED). | Defective AFC/PLL module. Refer to publication 888 1742 007. |
| HIGH AUDIO DISTORTION IN BOTH STEREO CHANNELS | Figure 5-4 |
| HIGH AUDIO DISTORTION IN ONE STEREO CHANNEL | Defective STEREO ANALOG module. Refer to publication 888 1742 005. |
| NOISY AUDIO | Figure 5-5 |
| AM NOISE ON RF CARRIER | Figure 5-6 |
| NO MODULATION | Figure 5-7 |
| CIRCUIT BREAKER CB-1 OPENS | Figure 5-8 |





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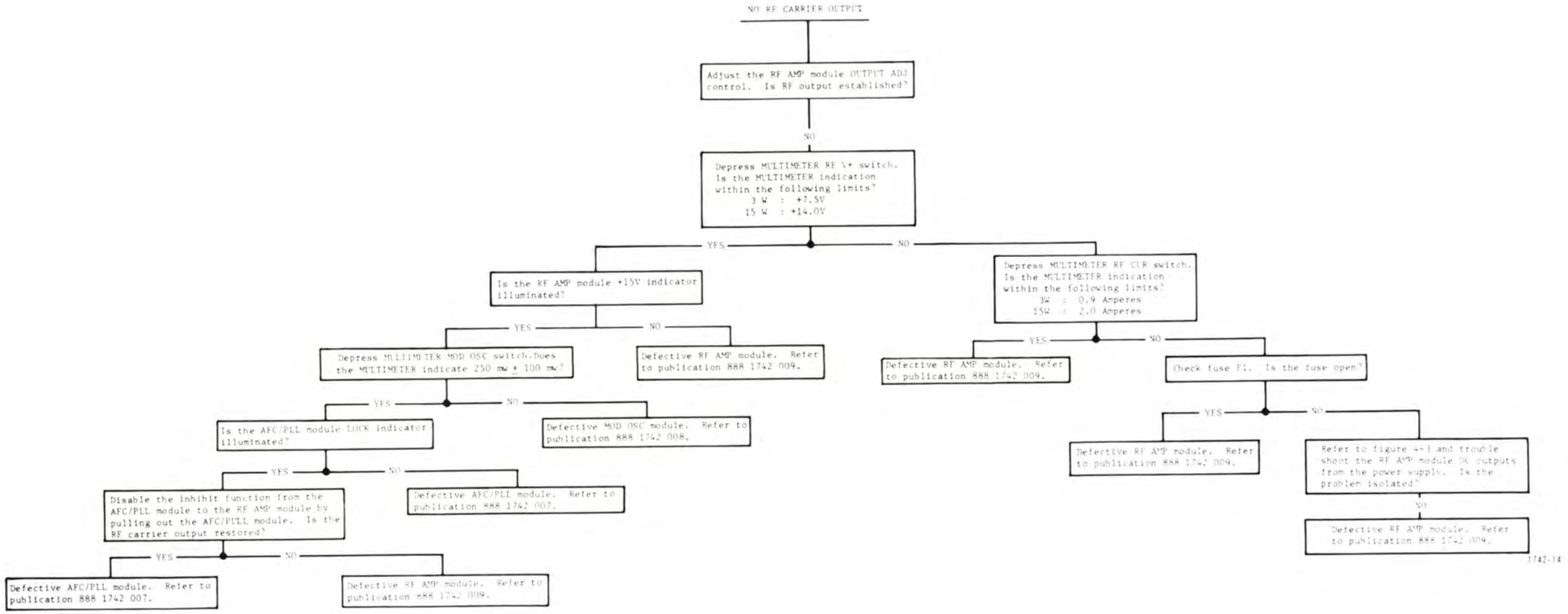


FIGURE 5-1.
NO RF CARRIER OUTPUT

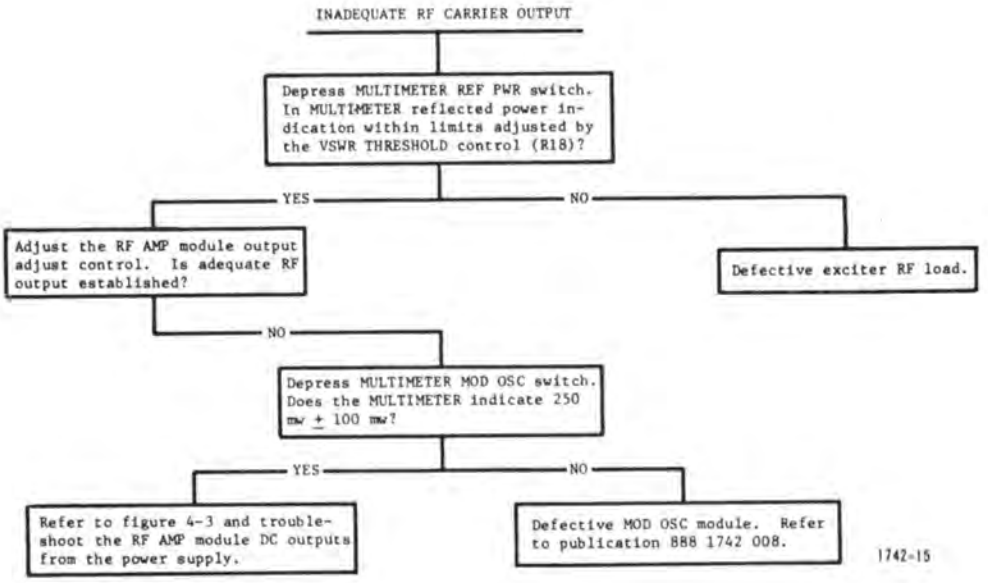


Figure 5-2. Inadequate RF Carrier Level Output

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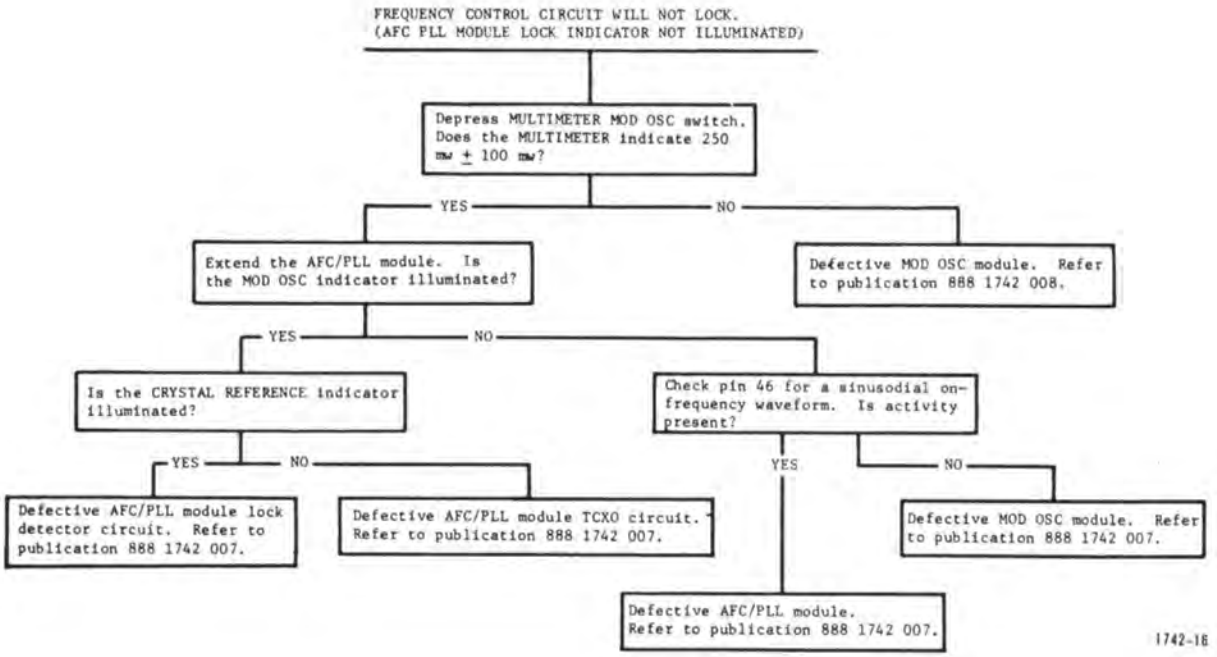


Figure 5-3. Frequency Control Circuit Will Not Lock (AFC/PLL Module Lock Indicator Not Illuminated)





WARNING: Disconnect primary power prior to servicing.

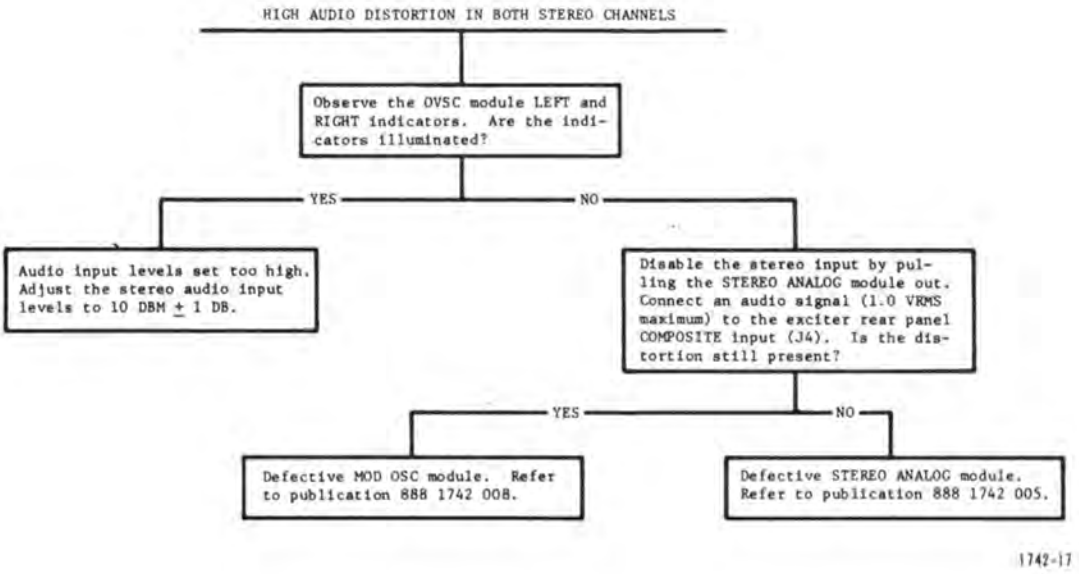


Figure 5-4. High Audio Distortion in Both Stereo Channels







WARNING: Disconnect primary power prior to servicing.

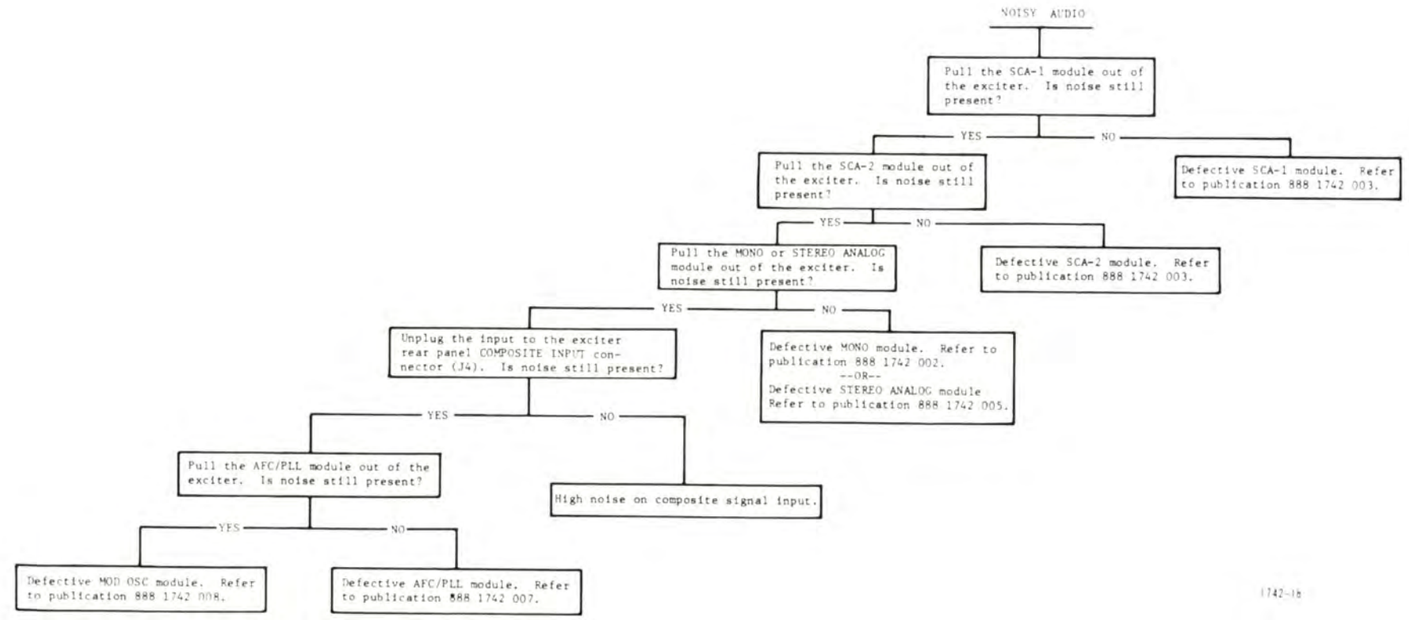


FIGURE 5-5.
NOISY AUDIO

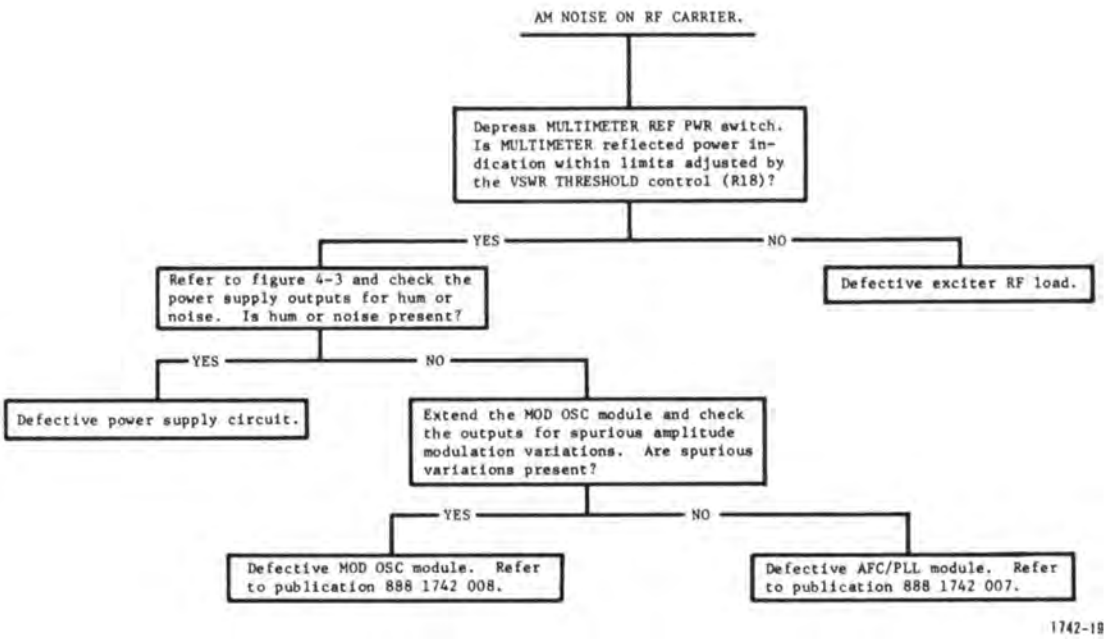


Figure 5-6. AM Noise on RF Carrier







WARNING: Disconnect primary power prior to servicing.

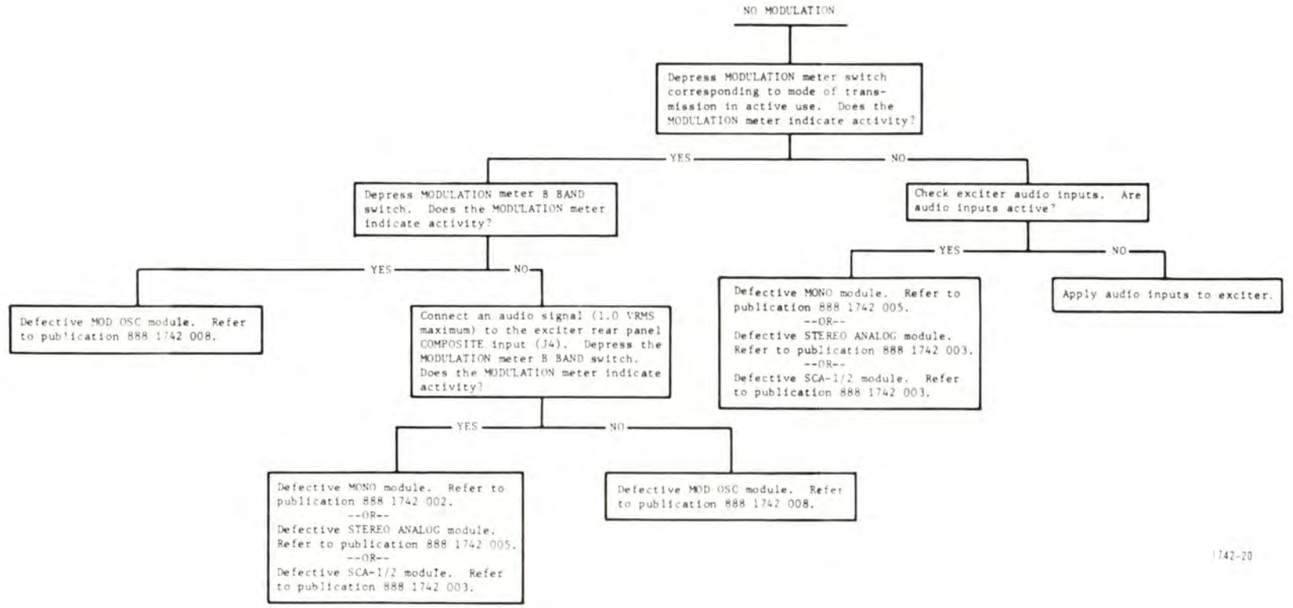


FIGURE 5-7.
NO MODULATION

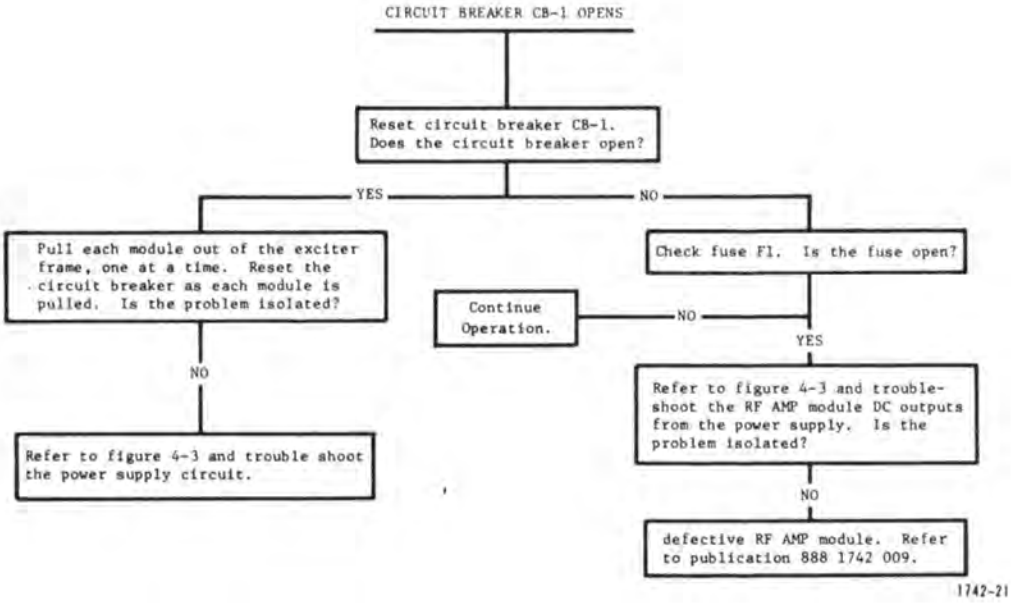


Figure 5-8. Circuit Breaker CB-1 Opens

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WARNING: Disconnect primary power prior to servicing.

# SECTION VI

# PARTS LIST

## 6-1. INTRODUCTION.

6-2. This section provides a description, reference designator and part number for selected replaceable parts and assemblies required for proper maintenance of the MS-15 FM Exciter. Table 6-1 lists assemblies having replaceable parts, the table number listing the parts, and the page number on which the table is located. Identity of the assembly nomenclaure in table 6-1 signifies the equipment level within the overall equipment configuration.

NOTE

Actual component values may vary slightly from component values listed on schematics and parts lists. Due to industry-wide shortages, it is sometimes necessary to use parts other than those specified. In every vase, however, a substitute part is selected for conformance to overall design specifications so that equipment performance is not affected. Components that are frequency determined or peculiar to an individual exciter are identified by a Harris part number and MS-15 component number on the final test addendum sheets shipped with the quipment.

## 6-3. REPLACEABLE PARTS SERVICE.

6-4. Replacement parts are available 24 hours a day, seven days a week from the HARRIS Service Parts Department. Telephone 217/222-8200 to contact the Service Parts Department or address correspondence to Service Parts Department, HARRIS CORPORATION, Broadcast Products Division, P.O. Box 4290, Quincy, Illinois 62301, USA. The HARRIS factory may also be contacted through a TXW faciltiy (910-246-3312) or a TELEX service (40-4347).

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Table 6-1. Replaceable Parts List Index



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WARNING: Disconnect primary power prior to servicing.

Table 6-2. FM Exciter (2) - 994 7950 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| 2A1 | 992 4980 002 | Main Frame | 1 |
| 2A2 | 992 4978 001 | RF Power Amplifier Module | 1 |
| 2A3 | 992 4985 001 | Automatic Frequency Control Module | 1 |
| 2A4 | 992 4987 001 | Modulated Oscillator Module | 1 |
| 2A5 | 939 3524 001 | Extender Board Assembly | 1 |
| 2A6 | 992 4990 001 | Access Cables Extender Pack | 1 |
| | 410 0232 000 | Insulators | 3 |

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Table 6-3. Main Frame (2A1) - 992 4980 002

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| 2A1A1 | 992 4981 001 | DC Meter Module | 1 |
| 2A1A2 | 992 4982 001 | AC Meter Module | 1 |
| 2A1A3 | 992 4983 001 | Mother Board | 1 |
| 2A1A4 | 992 4984 001 | RFI Filter Module | 1 |
| 2A1A5 | 992 5000 001 | Power Supply Module | 1 |
| B1 | 430 0098 000 | Fan, Tubeaxial, 50/60 Hz, 115/230V | 1 |
| C1 | 524 0223 000 | Capacitor, 4900 uF, 30V | 1 |
| C2 | 524 0337 000 | Capacitor, 5100 uF, 50V | 1 |
| C3 | 524 0336 000 | Capacitor, 2900 uF, 50V | 1 |
| C4 | 524 0337 000 | Capacitor, 5100 uF, 50V | 1 |
| C5,C6,C7,C8 | 516 0082 000 | Capacitor, .01 uF, 1 kV | 4 |
| C9,C14 | 526 0351 000 | Capacitor, 6.8 uF, 50V | 2 |
| C15,C16 | 516 0082 000 | Capacitor, .01 uF, 1 kV | 2 |
| CB1 | 606 0547 000 | Circuit Breaker, 2 Ampere | 1 |
| CR1,CR2 | 384 0564 000 | Rectifier, Bridge, 6 A, 600V | 2 |
| CR3 | 384 0020 000 | Rectifier, 1N4005 | 1 |
| CR4 | 386 0391 000 | Diode, Zener, 1N2821A | 1 |
| CR5 | 406 0479 000 | Light, Indicator, Red | 1 |
| F1 | 398 0020 000 | Fuse, Fast, 3 AG, 3 Ampere | 1 |
| L1 | 476 0399 000 | Choke, Filter, 5 mH, 2 Ampere | 1 |
| M1 | 632 0961 000 | Multimeter, 0-100 UADC Movement | 1 |
| M2 | 632 0962 000 | Meter, Modulation, 0-550 UADC Movement | 1 |

Table 6-3. Main Frame (2A1) - 992 4980 002 (Continued)

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| Q1,Q3 | 380 0187 000 | Transistor, 2N6055 | 2 |
| Q4 | 380 0571 000 | Transistor, 2N6053 | 1 |
| R7 | 548 1437 000 | Resistor, 665k ohm, 1/4W, 1% | 1 |
| R8,R9 | 548 0314 000 | Resistor, 75k ohm, 1/4W, 1% | 2 |
| R10 | 548 1437 000 | Resistor, 665k ohm, 1/4W, 1% | 1 |
| S1 | 604 0868 000 | Switch, Rocker, DPDT | 1 |
| T1 | 472 1117 000 | Transformer, Power | 1 |
| TB1,TB2 | 614 0004 000 | Terminal Board, 4 Terminal | 2 |
| TB3 | 614 0147 000 | Terminal Strip, 6 Terminal | 1 |
| U1 | 382 0527 000 | Regulator, Integrated Circuit, LM 340K-5 | 1 |
| XCR4 | 404 0661 000 | Socket, Transistor for TO-3 Case | 1 |
| XF1 | 402 0023 000 | Fuse, Holder, 342004 | 1 |
| XQ1,XQ2,XQ3,XQ4 | 404 0661 000 | Socket, Transistor for TO-3 Case | 4 |
| | 929 2191 001 | Ribbon Cable, 20 Cond. | 1 |
| | 929 2192 001 | Ribbon Cable, 26 Cond. | 1 |
| | 929 2193 001 | Ribbon Cable, 40 Cond. | 1 |
| | 938 3828 126 | Cable, Coax | 4 |
| | 929 2440 001 | Cable, Main | 1 |

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Table 6-4. Ribbon Cable, 20 Conductor - 929 2191 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| | 612 0895 000 | Receptacle Connector Kit, 20 Pin | 2 |





WARNING: Disconnect primary power prior to servicing.

Table 6-5. Ribbon Cable Assembly, 26 Conductor - 929 2192 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| | 612 0896 000 | Receptacle Connector Kit, 26 Pin | 2 |

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WARNING: Disconnect primary power prior to servicing.

Table 6-6. Ribbon Cable, 40 Conductor - 929 2193 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| | 612 0897 000 | Receptacle Connector Kit, 40 Pin | 2 |





WARNING: Disconnect primary power prior to servicing.

Table 6-7. Coaxial Cable - 938 3828 126

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| | 620 1510 000 | BNC Connector | 1 |
| | 620 0566 000 | Plug, Right Angle, UG 1466/ | 1 |





WARNING: Disconnect primary power prior to servicing.

Table 6-8. DC Metering Module (2A1A1) - 992 4981 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| CR1 | 384 0321 000 | Diode, Hot Carrier, 5082-2800 | 1 |
| R1,R2 | 548 0317 000 | Resistor, 301k ohm, 1/4W, 1% | 2 |
| R3 | 548 0392 000 | Resistor, .123 ohm, 1W, 1% | 1 |
| R4 | 540 1109 000 | Resistor, 33k ohm, 1/2W, 5% | 1 |
| R5 | 548 0317 000 | Resistor, 301k ohm, 1/4W, 1% | 1 |
| R6 | 548 0997 000 | Resistor, 20k ohm, 1/4W, 1% | 1 |
| S1 | 604 0862 000 | Switch, Pushbutton, 10 Section | 1 |
| | 610 0746 000 | Header Assembly, 20 Pin | 1 |
| | 839 2836 001 | Printed Board | 1 |

Table 6-9. AC Metering Module (2A1A2) - 992 4982 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| C1 | 526 0049 000 | Capacitor, 6.8 uF, 35V, 20% | 1 |
| C2 | 500 0813 000 | Capacitor, Mica, 33 pF, 500V | 1 |
| C3 | 526 0049 000 | Capacitor, 6.8 uF, 35V, 20% | 1 |
| C4 | 500 0817 000 | Capacitor, Mica, 47 pF, 500V | 1 |
| C5,C6 | 526 0049 000 | Capacitor, 6.8 uF, 35V, 20% | 2 |
| C8 | 526 0340 000 | Capacitor, 1 uF, 35V, 10% | 1 |
| C9,C10 | 526 0049 000 | Capacitor, 6.8 uF, 35V, 20% | 2 |
| C11 | 526 0342 000 | Capacitor, 2.7 uF, 35V, 10% | 1 |
| C12 | 526 0106 000 | Capacitor, 27 uF, 35V, 10% | 1 |
| C13,C14,C15,C16 | 526 0049 000 | Capacitor, 6.8 uF, 35V, 20% | 4 |
| CR1,CR2,CR3 | 384 0321 000 | Diode, Hot Carrier, 5082-2800 | 3 |
| CR4,CR5,CR6,CR7 | 384 0431 000 | Diode, 1N4001 | 4 |
| Q1,Q2 | 380 0319 000 | Transistor, MPS A14 | 2 |
| R1 | 550 0913 000 | Potentiometer, 4 Turn, 5K ohm, 1/2W, 20% | 1 |
| R2 | 540 1113 000 | Resistor, 18K ohm, 1/2W, 5% | 1 |
| R3 | 550 0913 000 | Potentiometer, 4 Turn, 5K ohm, 1/2W, 20% | 1 |
| R4 | 540 1113 000 | Resistor, 18K ohm, 1/2W, 5% | 1 |
| R5 | 550 0398 000 | Potentiometer, 1K ohm, 1/2W, 10% | 1 |
| R6 | 540 1179 000 | Resistor, 3600 ohm, 1/2W, 5% | 1 |
| R7 | 550 0928 000 | Potentiometer, 4 Turn, 20K ohm, 1/2W, 10% | 1 |
| R8 | 540 1165 000 | Resistor, 3300 ohm, 1/2W, 5% | 1 |

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Table 6-9. AC Metering Module (2A1A2) - 992 4982 001 (Continued)

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| R9 | 550 0928 000 | Potentiometer, 4 Turn, 20K ohm, 1/2W, 10% | 1 |
| R10 | 540 1165 000 | Resistor, 3300 ohm, 1/2W, 5% | 1 |
| R11 | 550 0913 000 | Potentiometer, 4 Turn, 5K ohm, 1/2W, 20% | 1 |
| R12 | 540 1113 000 | Resistor, 18K ohm, 1/2W, 5% | 1 |
| R13 | 550 0913 000 | Potentiometer, 4 Turn, 5K ohm, 1/2W, 20% | 1 |
| R14 | 540 1113 000 | Resistor, 18K ohm, 1/2W, 5% | 1 |
| R15 | 550 0928 000 | Potentiometer, 4 Turn, 20K ohm, 1/2W, 10% | 1 |
| R16 | 540 1160 000 | Resistor, 22K ohm, 1/2W, 5% | 1 |
| R17 | 540 1328 000 | Resistor, 560K ohm, 1/2W, 5% | 1 |
| R18 | 540 1111 000 | Resistor, 10K ohm, 1/2W, 5% | 1 |
| R19 | 540 1151 000 | Resistor, 10 ohm, 1/2W, 5% | 1 |
| R20 | 540 1144 000 | Resistor, 200K ohm, 1/2W, 5% | 1 |
| R21 | 550 0930 000 | Potentiometer, 4 Turn, 200K ohm, 1/2W, 10% | 1 |
| R22 | 540 1105 000 | Resistor, 5100 ohm, 1/2W, 5% | 1 |
| R23 | 540 1151 000 | Resistor, 10 ohm, 1/2W, 5% | 1 |
| R24 | 540 1251 001 | Resistor, 300K ohm, 1/2W, 5% | 1 |
| R25,R26 | 540 1159 000 | Resistor, 100K ohm, 1/2W, 5% | 2 |
| R27 | 540 1129 000 | Resistor, 1500 ohm, 1/2W, 5% | 1 |
| R28,R29 | 540 1111 000 | Resistor, 10K ohm, 1/2W, 5% | 2 |
| R30 | 550 0935 000 | Potentiometer, 4 Turn, 2K ohm, 1/2W, 10% | 1 |

Table 6-9. AC Metering Module (2A1A2) - 992 4982 001 (Continued)

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| R31 | 540 1145 000 | Resistor, 6800 ohm, 1/2W, 5% | 1 |
| R32 | 540 1111 000 | Resistor, 10K ohm, 1/2W, 5% | 1 |
| R33,R34 | 540 1151 000 | Resistor, 10 ohm, 1/2W, 5% | 2 |
| R35 | 540 1162 000 | Resistor, 1 megohm, 1/2W, 5% | 1 |
| R36 | 540 1111 000 | Resistor, 10K ohm, 1/2W, 5% | 1 |
| R37 | 540 1134 000 | Resistor, 33 Ohm, 1/2W, 5% | 1 |
| R38 | 540 1160 000 | Resistor, 22K ohm, 1/2W, 5% | 1 |
| R39 | 540 1159 000 | Resistor, 100K ohm, 1/2W, 5% | 1 |
| R40 | 540 1337 000 | Resistor, 12 megohm, 1/2W, 5% | 1 |
| R41 | 540 1160 000 | Resistor, 22K ohm, 1/2W, 5% | 1 |
| R42 | 540 1114 000 | Resistor, 4.7k ohm, 1/2W, 10% | 1 |
| R43 | 540 1165 000 | Resistor, 3300 ohm, 1/2W, 5% | 1 |
| R44 | 540 1210 000 | Resistor, 150K ohm, 1/2W, 5% | 1 |
| R45 | 540 1107 000 | Resistor, 20K ohm, 1/2W, 5% | 1 |
| R46 | 540 1104 000 | Resistor, 2000 ohm, 1/2W, 5% | 1 |
| R47 | 540 1201 000 | Resistor, 910 ohm, 1/2W, 5% | 1 |
| R48 | 550 0935 000 | Potentiometer, 4 Turn, 2K ohm, 1/2W, 10% | 1 |
| R49 | 540 1129 000 | Resistor, 1500 ohm, 1/2W, 5% | 1 |
| R50 | 559 0043 000 | Thermistor, 2K ohm, @25°C, 10% | 1 |
| R51 | 540 1107 000 | Resistor, 20K ohm, 1/2W, 5% | 1 |
| R52 thru R55 | 548 0076 000 | Resistor, 100K ohm, 1/2W, 1% | 4 |
| R56 thru R58 | 540 1159 000 | Resistor, 100K ohm, 1/2W, 5% | 3 |
| R59 | 540 1129 000 | Resistor, 1500 ohm, 1/2W, 5% | 1 |

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WARNING: Disconnect primary power prior to servicing.

Table 6-9. AC Metering Module (2A1A2) - 992 4982 001 (Continued)

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| S1 | 604 0862 000 | Switch, Pushbutton, 10 Section | 1 |
| U1 | 382 0415 000 | Integrated Circuit, LM324N | 1 |
| U2, U3 | 382 0472 000 | Integrated Circuit, LM318N | 2 |
| U4 | 540 1332 000 | Network, Resistor (8 each 100K ohm, 1/4W, 2% in Pin DIP Package) | 1 |
| U5 | 382 0360 000 | Integrated Circuit, MC7915CP | 1 |
| U6 | 382 0359 000 | Integrated Circuit MC7815CP | 1 |
| XU1 | 404 0675 000 | Socket, IC, 16 Contact | 1 |
| XU2, XU3 | 404 0673 000 | Socket, IC, 8 Contact | 2 |
| XU4 | 404 0674 000 | Socket, IC, 14 Contact | 1 |
| | 610 0747 000 | Header Assembly, 26 Pin | 1 |
| | 939 2851 001 | PC Board | 1 |

Table 6-10. Mother Board (2A1A3) - 992 4983 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| P1 thru P13 | 612 0887 000 | Connector, PC Board, 72 Contact | 13 |
| R1,R2,R3,R4,R5 | 540 0864 000 | Resistor, 10 ohm, 1/4W, 5% | 5 |
| | 610 0746 000 | Header Assembly, 20 Pin | 1 |
| | 610 0747 000 | Header Assembly, 26 Pin | 1 |
| | 610 0748 000 | Header Assembly, 40 Pin | 1 |
| | 620 0515 000 | Receptacle, 50-051-0000 | 4 |
| | 952 8329 001 | Printed Circuit Board | 1 |

Table 6-11. RFI Filter Module (2A1A4) - 992 4984 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| C1,C2 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C3 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C4,C5 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C6 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C7,C8 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C9 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C10,C11 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C12 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C13,C14 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C15 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C16,C17 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C18 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C19,C20 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C21 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C22,C23 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C24 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C25,C26 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C27 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C28,C29 | 516 0370 000 | Capacitor, .005 uF, 500V, 10% | 2 |
| C30 | 500 0756 000 | Capacitor, Mica, 330 pF, 500V | 1 |
| C31 thru C46 | 516 0074 000 | Capacitor, Disc., .005 uF, 1kV | 16 |
| C47 | 516 0084 000 | Capacitor, Disc., .02 uF, 600V | 1 |
| C48 | 516 0074 000 | Capacitor, Disc., .005 uF, 1kV | 1 |

Table 6-11. RFI Filter Module (2A1A4) - 992 4984 001 (Continued)

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| C49,C50,C51,C52 | 516 0084 000 | Capacitor, Disc., .02 uF, 600V | 4 |
| C53,C54,C55,C56, C57,C58,C59,C60, C61 | 516 0074 000 | Capacitor, Disc., .005 uF, 1 kV | 9 |
| CR1 | 384 0020 000 | Rectifier, 1N4005 | 1 |
| J1 | 610 0740 000 | Header, Pin, 36 Circuit | 1 |
| J2 | 610 0748 000 | Header Assembly, 40 Pin | 1 |
| J3 | 610 0739 000 | Header, Pin, 12 Circuit | 1 |
| K1 | 574 0162 000 | Relay, 24 Vdc, 4PDT | 1 |
| L1,L3,L5,L6,L7, L9 | 494 0419 000 | Choke, RF, Shielded, 1000.0 uH | 6 |
| L2,L4,L8,L10 | 492 0627 000 | Inductor, Variable, .65 to 1.3 mH | 4 |
| L11,L12,L13,L14 | 414 0212 000 | Torroid, F867-1-Q1 | 4 |
| R1 | 540 0900 000 | Resistor, 330 ohm, 1/4W, 5% | 1 |
| R2 | 540 0915 000 | Resistor, 1300 ohm, 1/4W, 5% | 1 |
| R3,R4 | 540 0900 000 | Resistor, 330 ohm, 1/4W, 5% | 2 |
| R5 | 540 0915 000 | Resistor, 1300 ohm, 1/4W, 5% | 1 |
| R6,R7 | 540 0900 000 | Resistor, 330 ohm, 1/4W, 5% | 2 |
| R8 | 540 0915 000 | Resistor, 1300 ohm, 1/4W, 5% | 1 |
| R9,R10 | 540 0900 000 | Resistor, 330 ohm, 1/4W, 5% | 2 |
| R11 | 540 0915 000 | Resistor, 1300 ohm, 1/4W, 5% | 1 |
| R12,R13,R14 | 540 0900 000 | Resistor, 330 ohm, 1/4W, 5% | 3 |
| R15,R16,R17,R18, R19,R20,R21,R22, R23,R24 | 540 0920 000 | Resistor, 2200 ohm, 1/4W, 5% | 10 |

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Table 6-11. RFI Filter Module (2A1A4) - 992 4984 001 (Continued)

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| R25,R26 | 548 0263 000 | Resistor, 1K ohm, 1/8W, 1% | 2 |
| R27,R28 | 540 0920 000 | Resistor, 2200 ohm, 1/4W, 5% | 2 |
| R29 | 540 0912 000 | Resistor, 1000 ohm, 1/4W, 5% | 1 |
| R30 | 540 0880 000 | Resistor, 47 ohm, 1/4W, 5% | 1 |
| R31 | 540 0017 000 | Resistor, 47 ohm, 1/2W, 5% | 1 |
| R32 | 540 0912 000 | Resistor, 1000 ohm, 1/4W, 5% | 1 |
| R33 | 540 0017 000 | Resistor, 47 ohm, 1/2W, 5% | 1 |
| R34 | 540 0915 000 | Resistor, 1300 ohm, 1/4W, 5% | 1 |
| XK1 | 404 0161 000 | Socket, Relay, 9 KH2 | 1 |
| TB1,TB2 | 614 0040 000 | Terminal Board, 18 Terminals | 2 |
| | 943 1715 001 | PC Board | 1 |

Table 6-12. Power Supply Module (2A1A5) - 992 5000 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| C10,C11,C12,C13 | 526 0349 000 | Capacitor, 2.2 uF, 50V, 20% | 4 |
| CR5,CR6 | 386 0077 000 | Diode, Zener, 1N4749A | 2 |
| CR7,CR8 | 384 0020 000 | Rectifier, 1N4005 | 2 |
| Q5 | 380 0189 000 | Transistor, 2N3904 | 1 |
| Q6 | 380 0190 000 | Transistor, 2N3906 | 1 |
| R1 | 540 0339 000 | Resistor, 2000 ohm, 1W, 5% | 1 |
| R2 | 540 1102 000 | Resistor, 100 ohm, 1/2W, 5% | 1 |
| R3 | 540 1216 000 | Resistor, 330 ohm, 1/2W, 5% | 1 |
| R4 | 542 0002 000 | Resistor, 2 ohm, 5W, 5% | 1 |
| R5 | 540 1137 000 | Resistor, 3900 ohm, 1/2W, 5% | 1 |
| R6 | 540 0339 000 | Resistor, 2000 ohm, 1W, 5% | 1 |
| R11 | 540 1102 000 | Resistor, 100 ohm, 1/2W, 5% | 1 |
| R12 | 540 1137 000 | Resistor, 3900 ohm, 1/2W, 5% | 1 |
| R13 | 540 1216 000 | Resistor, 330 ohm, 1/2W, 5% | 1 |
| R14 | 542 0002 000 | Resistor, 2 ohm, 5W, 5% | 1 |
| R15 | 540 0332 000 | Resistor, 1000 ohm, 1W, 5% | 1 |
| | 929 2219 001 | PC Board | 1 |

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WARNING: Disconnect primary power prior to servicing.

Table 6-13. Extender Board Assembly (2A5) - 939 3524 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| J1 | 612 0916 000 | Connector, 72 Pin | 1 |
| | 943 2258 001 | Printed Circuit Board | 1 |

Table 6-14. Access Cables Extender Pack (2A6) - 992 4990 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| ------ | 929 2816 001 | Cord, AC Power | 1 |







WARNING: Disconnect primary power prior to servicing.

Table 6-15. Wide Band Option (6) - 994 7983 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| | 994 7983 001 | Blank Module | 5 |





WARNING: Disconnect primary power prior to servicing.

Table 6-16. Stereo Option (3) - 994 8020 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| 3A1 | 994 7989 001 | Stereo Analog Module | 1 |
| 3A2 | 994 7990 001 | Stereo Digital Module | 1 |
| 3A3 | 994 7991 001 | Stereo Overshoot Module | 1 |

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Table 6-17. SCA Option (4) - 994 7992 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| | 992 4977 001 | PC Board Assembly | 1 |





WARNING: Disconnect primary power prior to servicing.

Table 6-18. Mono Option (5) - 994 8019 001

| REF. SYMBOL | HARRIS PART NO. | DESCRIPTION | QTY. |
|---|---|---|---|
| 5A1 | 994 7988 001 | Monaural Module | 1 |
| | 994 7983 001 | Blank Module | 2 |

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WARNING: Disconnect primary power prior to servicing.

SECTION VII

DIAGRAMS

7-1. INTRODUCTION.

7-2. This section provides schematic, interconnection, and wiring diagrams required for maintenance of the MS-15 FM Exciter. The following diagrams are contained in this section:



1/42





WARNING: Disconnect primary power prior to servicing.

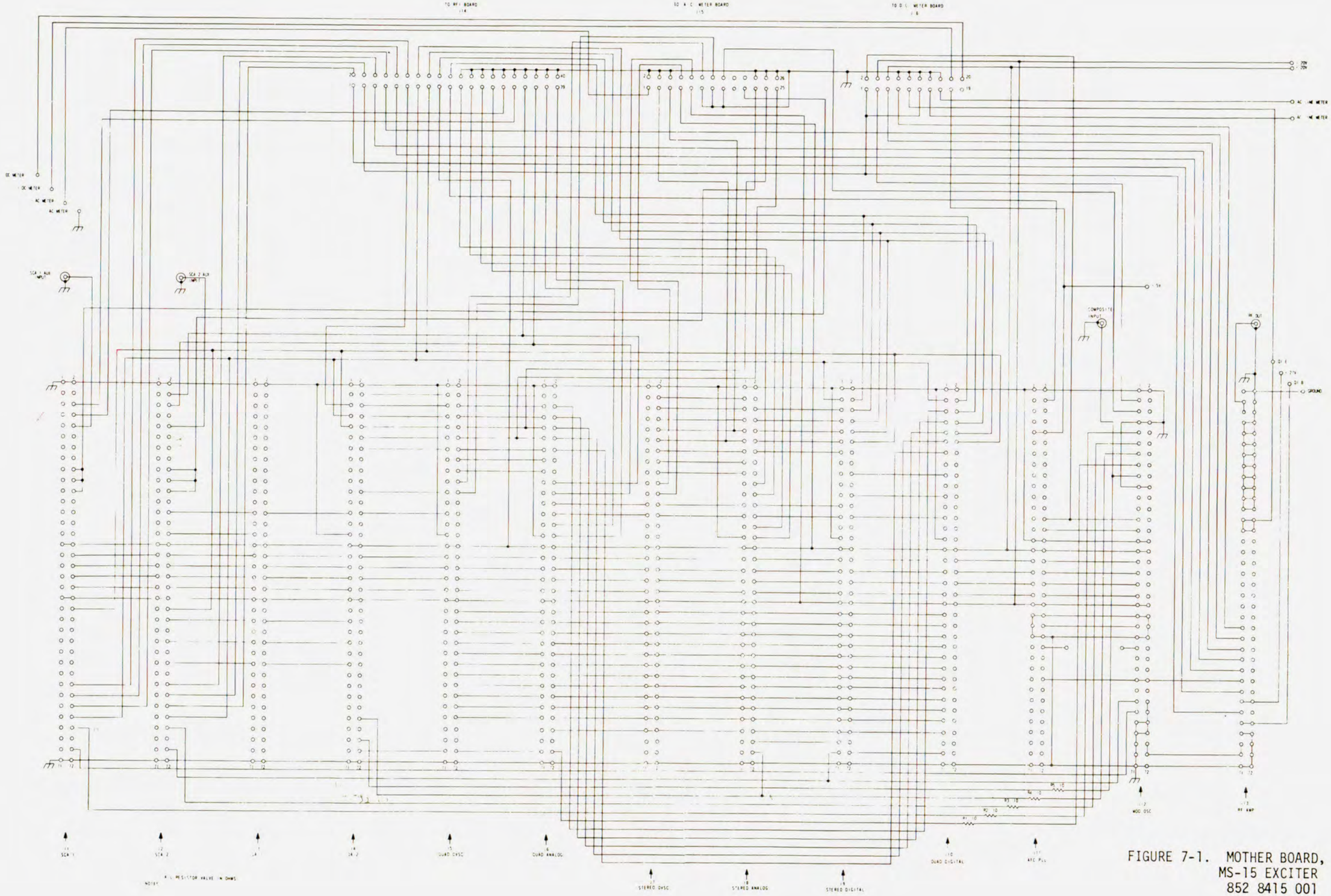
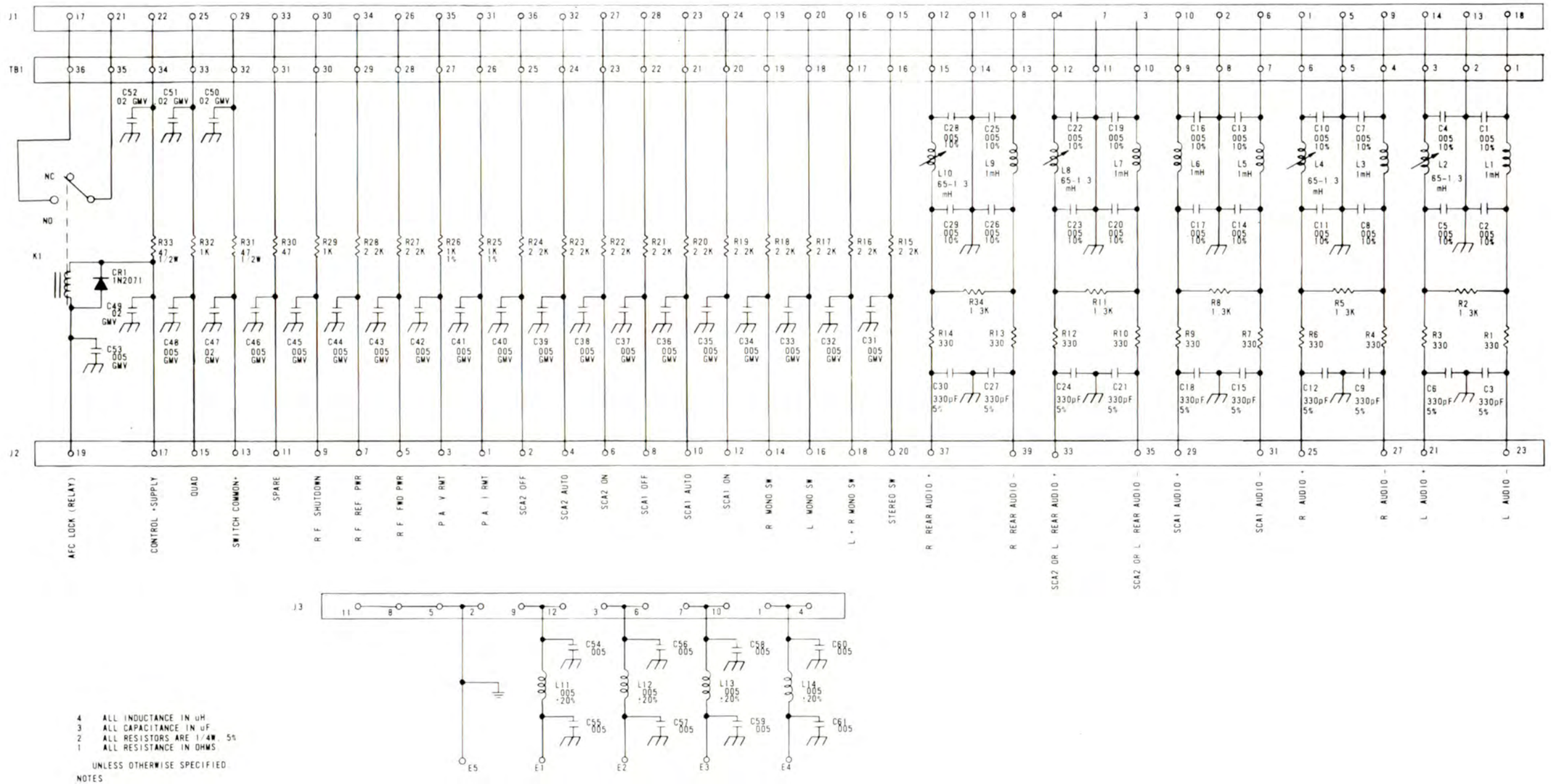


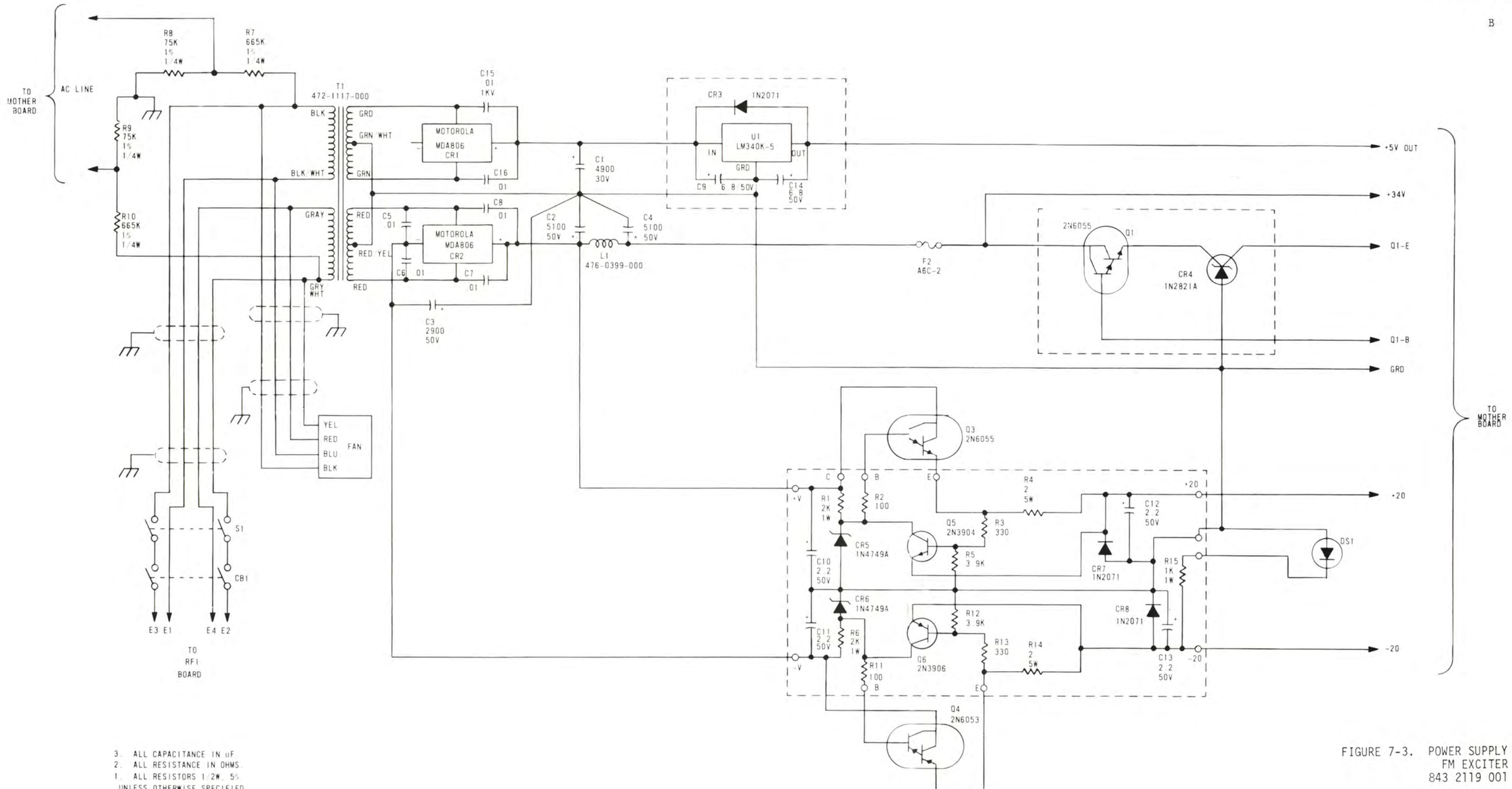

FIGURE 7-1. MOTHER BOARD, MS-15 EXCITER 852 8415 001




NOTES

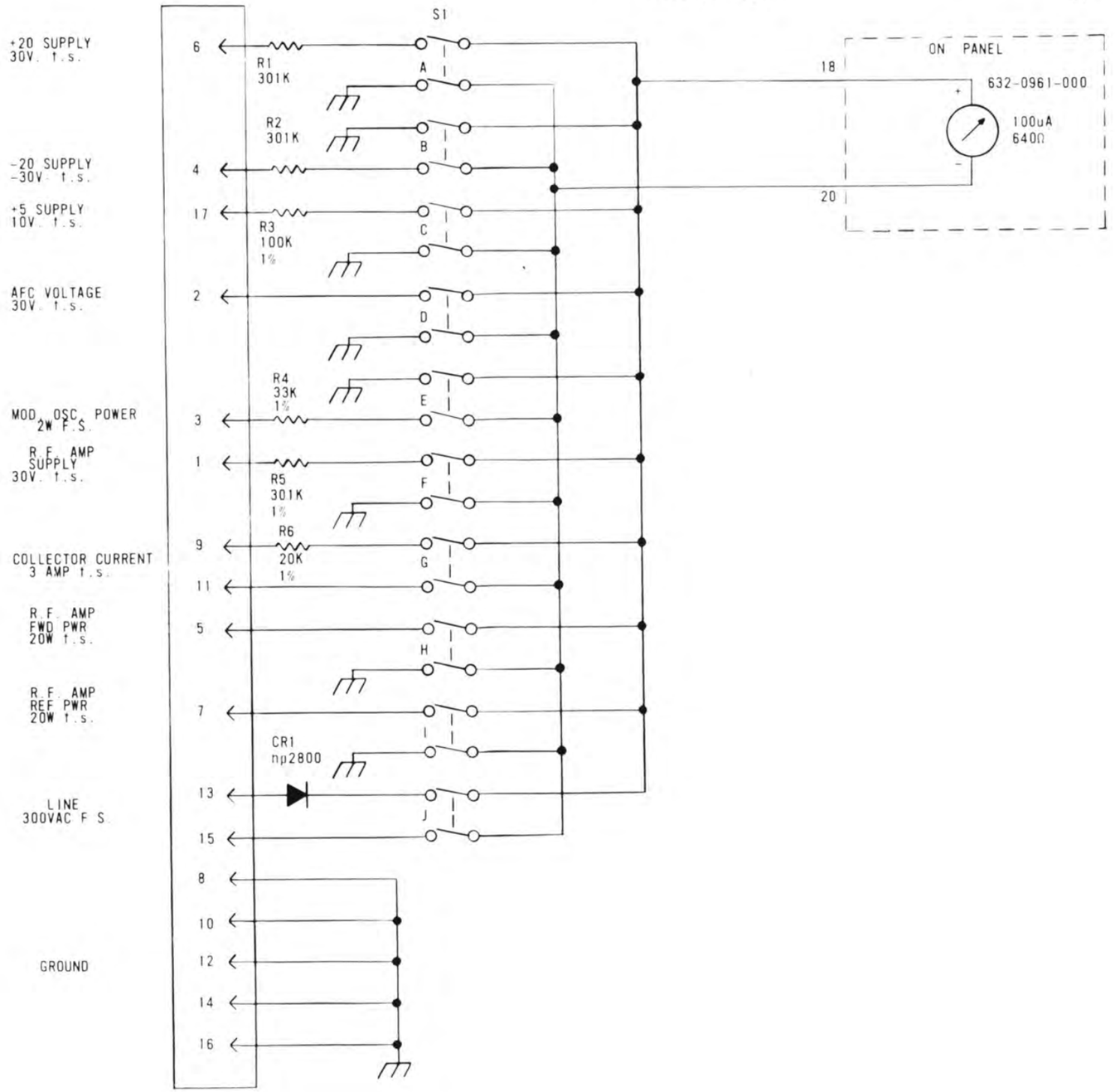
1. ALL RESISTANCE IN OHMS
2. ALL RESISTORS ARE 1/4W, 5%
3. ALL CAPACITANCE IN uF
4. ALL INDUCTANCE IN uH

FIGURE 7-2. RFI FILTER, FM EXCITER 843 1714 001




NOTES
1. ALL RESISTORS 1/2W, 5% UNLESS OTHERWISE SPECIFIED
2. ALL RESISTANCE IN OHMS
3. ALL CAPACITANCE IN uF

FIGURE 7-3. POWER SUPPLY FM EXCITER 843 2119 001

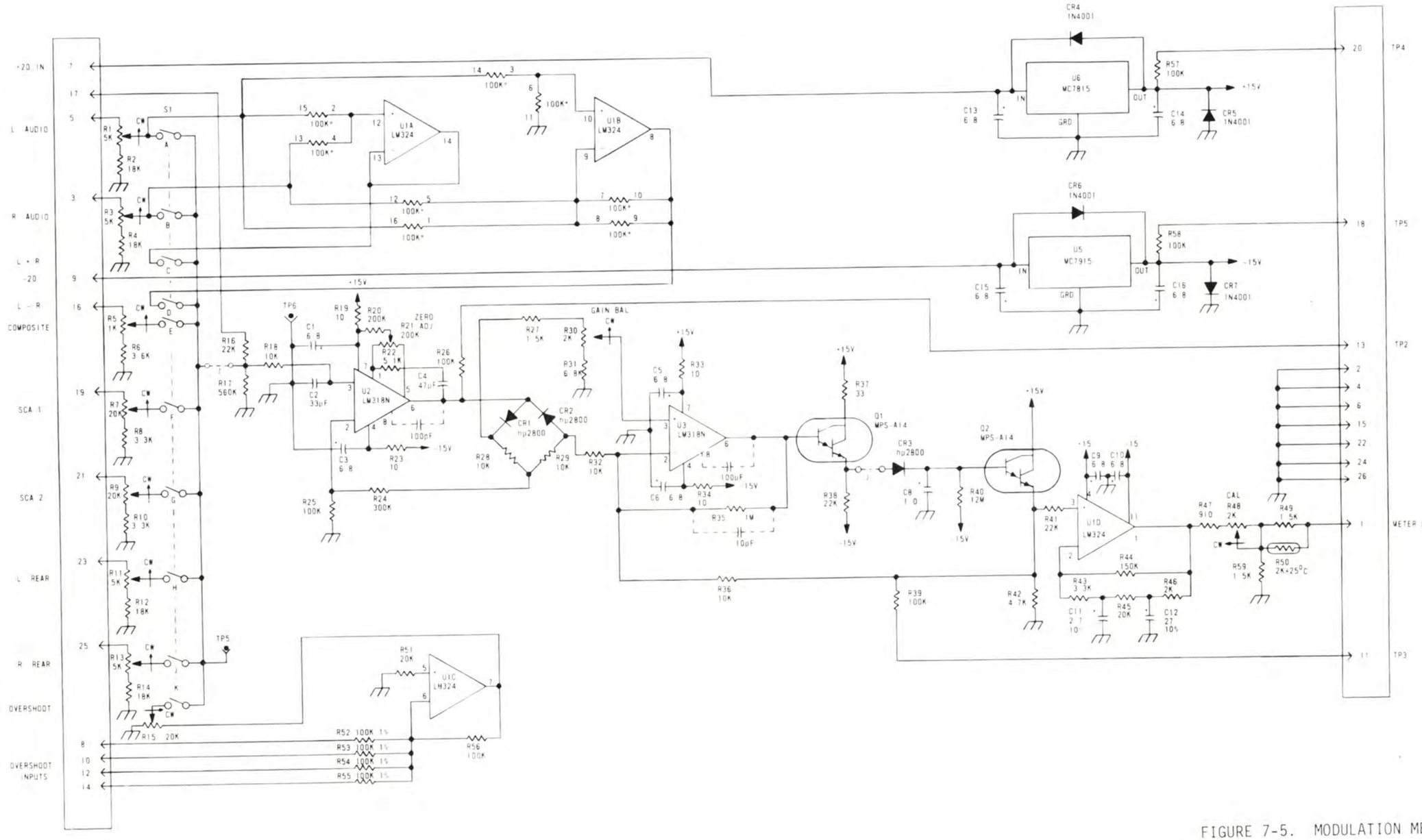



2. RESISTANCE IN OHMS.
1. RESISTORS ARE 1/4W 1%

NOTES:

FIGURE 7-4. DC METER BOARD
FM EXCITER
839 2835 001

7-9/7-10




4 PART OF U4 RA08 100KN
3 ALL CAPACITANCE IN uF
2 ALL RESISTANCE IN OHMS
1 ALL RESISTORS ARE 1/2 W 5% LOW NOISE UNLESS OTHERWISE SPECIFIED
NOTES

FIGURE 7-5. MODULATION METER BOARD
FM EXCITER
843 2118 001

# APPENDIX A

## MANUFACTURERS DATA

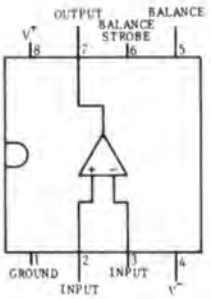
# APPENDIX A

## MANUFACTURERS DATA

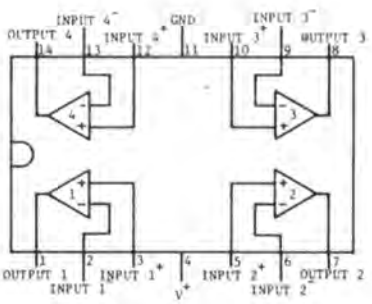
A-1. INTRODUCTION.

A-2. This appendix consists of the following technical data which identifies operating characteristics and parameters for various replaceable items used throughout the MS-15 circuitry.

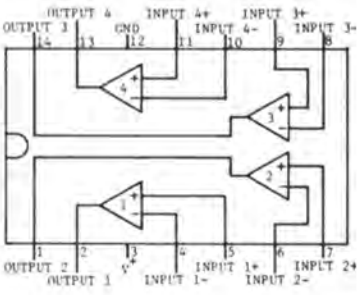
1. Integrated Circuit Connection Diagrams
2. Technical Data Sheet, AD521-JD Instrumentation Amplifier
3. Technical Data Sheet, XR2206 CP Function Generator
4. Technical Data Sheet, HA-4741 Quad Operational Amplifier
5. Technical Data Sheet, ILQ74 Quad Optical Isolator
6. Technical Data Sheet, LM318-N Operational Amplifier
7. Technical Data Sheet, DM-74LS161 Programmable Divider
8. Technical Data Sheet, TL430C Programmable Zener Diode
9. Technical Data Sheet, MC4044 Phase Detector
10. Engineering Report, A New Filtering Process For Optimal Overshoot Control



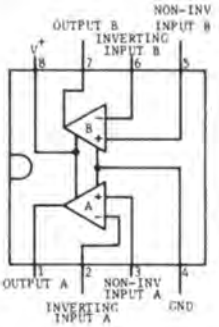

LM311N
VOLTAGE COMPARATOR



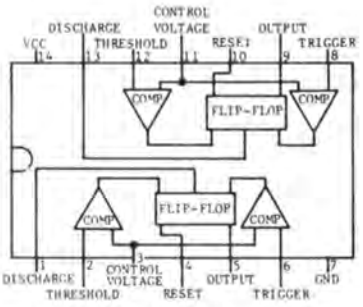

LM324N
QUAD OPERATIONAL AMPLIFIER



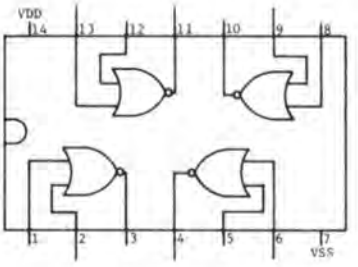

LM339N
QUAD VOLTAGE COMPARATOR




LM358N
DUAL OPERATIONAL AMPLIFIER




LM556CN
DUAL TIMER

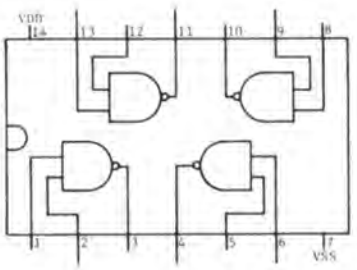



4001B
QUAD 2-INPUT NOR GATE

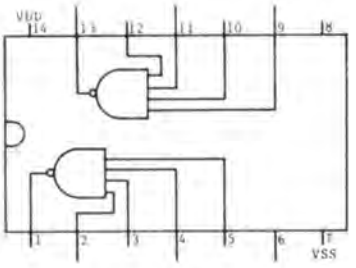
1742

1742-27

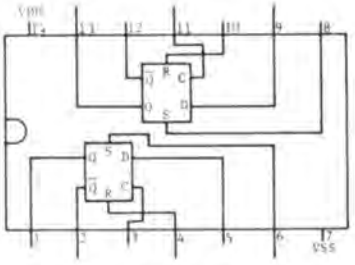
INTEGRATED CIRCUIT CONNECTION DIAGRAMS (SHEET 1 OF 3)



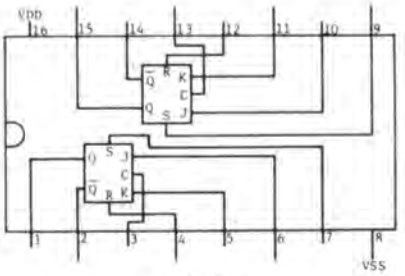

4011B
QUAD 2-INPUT NAND GATE



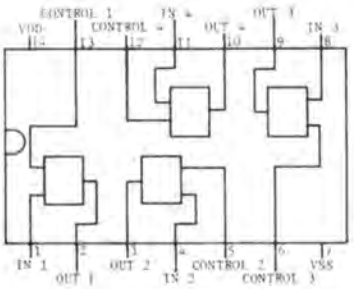

4012B
DUAL 4-INPUT NAND GATE



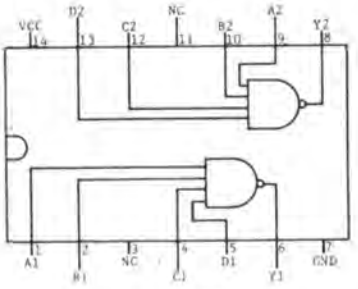

4013B
DUAL D FLIP-FLOP




4027B
DUAL J-K FLIP-FLOP




4066B
QUAD ANALOG SWITCH/MULTIPLEXER




7420N
DUAL 4-INPUT NAND GATE

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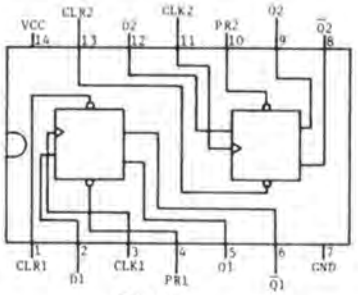
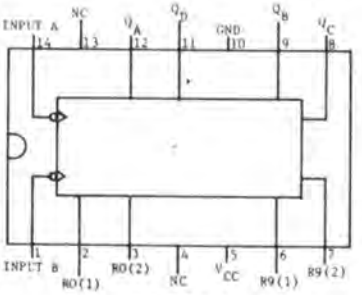
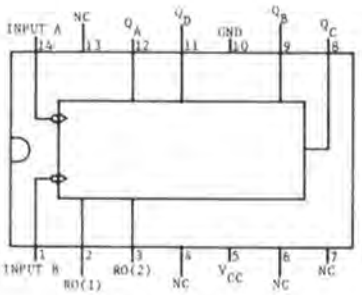
INTEGRATED CIRCUIT CONNECTION DIAGRAMS (SHEET 2 OF 3)



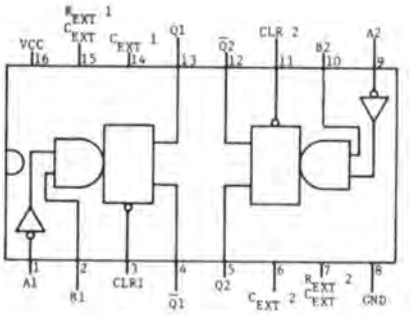

7474N
POSITIVE EDGE TRIGGERED
DUAL D FLIP-FLOP WITH
PRESET AND CLEAR




7490AN
DIVIDE BY 10 COUNTER



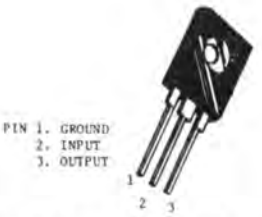

7493AN
DIVIDE BY 16 COUNTER




74123N
DUAL RETRIGGERABLE ONE SHOT

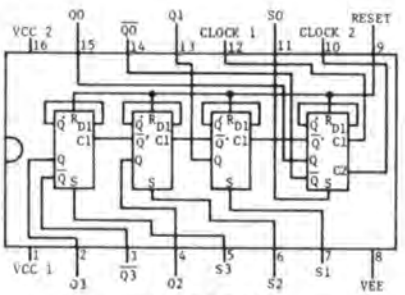

MC7806CT-POSITIVE 6 VOLT FIXED
VOLTAGE REGULATOR

MC7815CT-POSITIVE 15 VOLT FIXED
VOLTAGE REGULATOR




MC7906CT-NEGATIVE 6 VOLT FIXED
VOLTAGE REGULATOR

MC7915CT-NEGATIVE 15 VOLT FIXED
VOLTAGE REGULATOR




MC10178L
DIVIDE BY 16 COUNTER

1742-29

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INTEGRATED CIRCUIT CONNECTION DIAGRAMS (SHEET 3 OF 3)

ANALOG DEVICES

# Integrated Circuit Precision Instrumentation Amplifier

# AD521

**FEATURES**

**Programmable Gains from 0.1 to 1000**
**Floating Differential Inputs**
**High CMRR: 110dB min**
**Complete Input Protection, Power ON and Power OFF**
**Functionally Complete with the Addition of Two Resistors**
**Internally Compensated**
**Gain Bandwidth Product: 40MHz**
**Output Current Limited: 25mA**
**Extremely Low Cost: $8.50 (100's, J)**


## PRODUCT DESCRIPTION

The AD521 is the second generation, low cost, monolithic I.C. instrumentation amplifier developed by Analog Devices. A true instrumentation amplifier, the AD521 is a controlled gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521, like its predecessor the AD520, should not be confused with an operational amplifier, even though several manufacturers (including Analog Devices) offer op amps that can be used as building blocks in variable gain instrumentation amplifier circuits. An op amp is merely a high gain component requiring the addition of external feedback to complete the amplification function. Because of the limitations of resistor matching in the external feedback circuit and the relatively low input impedance resulting from the input resistors, an instrumentation amplifier circuit designed around op amps frequently provides less than satisfactory performance. Since the AD521 is a complete amplification circuit which does not depend upon external resistor matching for input/output isolation it maintains its high CMRR (110dB min) in any application. In addition, the high impedance inputs are fully protected against over voltages up to 15V greater than the supply voltage.

The AD521 can be operated at gains from 0.1 to greater than 1000 with the addition of only two programming resistors. Excellent d.c. characteristics are realized through the device's inherently low offset and gain drift and optional one-pot nulling. Dynamic performance is also outstanding with a gain bandwidth product of 40MHz, full peak response of 100kHz and a 10V/μsec slew rate.

The AD521 I.C. instrumentation amplifier is available in three different versions, depending on accuracy and operating temperature range: the economical "J" specified from 0°C to +70°C, the low drift "K", also specified from 0°C to +70°C and the "S", guaranteed over the full MIL-temperature range, -55°C to +125°C. All versions are packaged in a 14 pin DIP.

## PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
3. The AD521 is fully protected for input levels up to 15V beyond the supply voltage and 30V differential at the inputs.
4. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
5. Offset nulling can be achieved with an optional trim pot.
6. The AD521 offers superior dynamic performance with a gain bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μsec to 0.1% of a 10V step.
7. Every AD521 is baked for 40 hours at +150°C and temperature cycled ten times from -65°C to +150°C.



Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 Mid-West 312/894-3300 Texas 214/231-5094

# SPECIFICATIONS (typical @ $V_S$ = ±15V, $R_L$ = 2kΩ and $T_A$ = 25°C unless otherwise specified)

| MODEL | AD521J | AD521K | AD521S |
|---|---|---|---|
| **GAIN** | | | |
| Range (For Specified Operation, Note 1.) | 1 to 1000 | * | * |
| Equation | $G = R_S/R_G V/V$ | * | * |
| Error from Equation | (±0.25−0.004G)% | * | * |
| Nonlinearity (Note 2) | | | |
| 1≤G≤1000 | 0.2% max | * | * |
| Gain Temperature Coefficient | ±(3 ±0.05G)ppm/°C | * | ±(15 ±0.4G)ppm/°C |
| **OUTPUT CHARACTERISTICS** | | | |
| Rated Output | ±10V, ±10mA min | * | * |
| Output at Maximum Operating Temperature | ±10V @ 5mA min | * | * |
| Impedance | 0.1Ω | * | * |
| **DYNAMIC RESPONSE** | | | |
| Small Signal Bandwidth (±3dB) | | | |
| G = 1 | >2MHz | * | * |
| G = 10 | 300kHz | * | * |
| G = 100 | 200kHz | * | * |
| G = 1000 | 40kHz | * | * |
| Small Signal, ±1.0% Flatness | | | |
| G = 1 | 75kHz | * | * |
| G = 10 | 26kHz | * | * |
| G = 100 | 24kHz | * | * |
| G = 1000 | 6kHz | * | * |
| Full Peak Response (Note 3) | 100kHz | * | * |
| Slew Rate, 1≤G≤1000 | 10V/μsec | * | * |
| Settling Time (any 10V step to within 10mV of Final Value) | | | |
| G = 1 | 7μsec | * | * |
| G = 10 | 5μsec | * | * |
| G = 100 | 10μsec | * | * |
| G = 1000 | 35μsec | * | * |
| Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4) | | | |
| G = 1000 | 50μsec | * | * |
| Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5) | | | |
| G = 1000 | 10μsec | * | * |
| **VOLTAGE OFFSET (may be nulled)** | | | |
| Input Offset Voltage ($V_{os_I}$) | 3mV max (2mV typ) | 1.5mV max (0.5mV typ) | ** |
| vs. Temperature | 15μV/°C max (7μV/°C typ) | 5μV/°C max (1.5μV/°C typ) | ** |
| vs. Supply | 3μV/% | * | * |
| Output Offset Voltage ($V_{os_O}$) | 400mV max (200mV typ) | 200mV max (30mV typ) | ** |
| vs. Temperature | 400μV/°C max (150μV/°C typ) | 150μV/°C max (50μV/°C typ) | ** |
| vs. Supply (Note 6) | $0.005V_{os_O}$/% | * | * |
| **INPUT CURRENTS** | | | |
| Input Bias Current (either input) | 80nA max | 40nA max | ** |
| vs. Temperature | 1nA/°C max | 500pA/°C max | ** |
| vs. Supply | 2%/V | * | * |
| Input Offset Current | 20nA max | 10nA max | ** |
| vs. Temperature | 250pA/°C max | 125pA/°C max | ** |
| **INPUT** | | | |
| Differential Input Impedance (Note 7) | $3 \times 10^9 \Omega \| 1.8pF$ | * | * |
| Common Mode Input Impedance (Note 8) | $6 \times 10^{10} \Omega \| 3.0pF$ | * | * |
| Input Voltage Range for Specified Performance | ±10V | * | * |
| Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9) | 30V | * | * |
| Voltage at either input (Note 10) | $V_S$ ±15V | * | * |
| Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance | | | |
| G = 1 | 70dB min (74dB typ) | 74dB min (80dB typ) | ** |
| G = 10 | 90dB min (94dB typ) | 94dB min (100dB typ) | ** |
| G = 1000 | 100dB min (104dB typ) | 104dB min (114dB typ) | ** |
| G = 1000 | 100dB min (110dB typ) | 110dB min (120dB typ) | ** |
| **NOISE** | | | |
| Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10) | $\sqrt{(0.5G)^2 + (225)^2}\,\mu V$ | * | * |
| RMS RTO, 10Hz to 10kHz | $\sqrt{(1.2G)^2 + (50)^2}\,\mu V$ | * | * |
| Input Current, rms, 10Hz to 10kHz | 15pA (rms) | * | * |
| **REFERENCE TERMINAL** | | | |
| Bias Current | 3μA | * | * |
| Input Resistance | 10MΩ | * | * |
| Voltage Range | ±10V | * | * |
| Gain to Output | 1 | * | * |
| **POWER SUPPLY** | | | |
| Operating Voltage Range | ±5 to ±18 | * | * |
| Quiescent Supply Current | 5mA max | * | * |
| **TEMPERATURE RANGE** | | | |
| Specified Performance | 0 to +70°C | * | -55 to +125°C |
| Operating | -25 to +85°C | * | -55 to +125°C |
| Storage | -65 to +150°C | * | * |
| **PRICE** | | | |
| (1-24) | $12.75 | $18.00 | $30.00 |
| (25-99) | $10.20 | $14.40 | $24.00 |
| (100-999) | $8.50 | $12.00 | $20.00 |

*Specification same as AD521J.
**Specification same as AD521K.

Specifications and prices subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, input voltage should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output of ±9 volts to 18 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the typical frequency below which the amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μsec pulse at a 1kHz rate.(When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is a 30V, 10μsec pulse at a 1kHz rate. (When a common mode signal greater than $V_S$ - 0.5V) is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

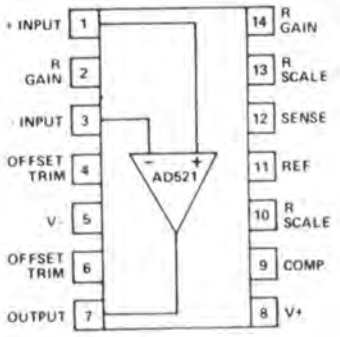
6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S$ = 0) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 6.




TOP VIEW

*Figure 1. AD521 Pin Configuration*

TO-116

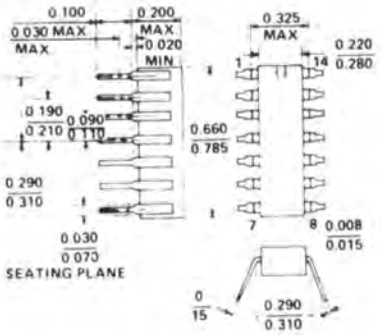



*Figure 2. Physical Dimensions*

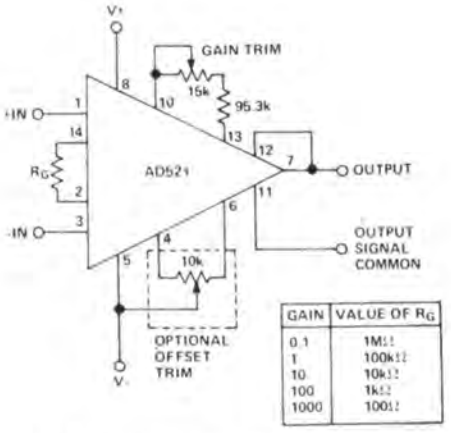



*Figure 3. Operating Connections for AD521*

## INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output under any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain, can be classi-

fied as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error with respect to either the input or output by the following formulae:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

As shown in Figure 4, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, $R_S/R_G$). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by $R_1$ and $R_2$. This gain factor is $1 + R_2/R_1$.

Where offset errors are critical, a resistor equal to the parallel combination of $R_1$ and $R_2$ should be placed between pin 11 and $V_{REF}$. This minimized the offset errors resulting from the input currents at the sense terminal flowing in $R_1$ and $R_2$. Note that gain changes introduced by changing the $R_1/R_2$ attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, $V_{REF}$ can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 4.

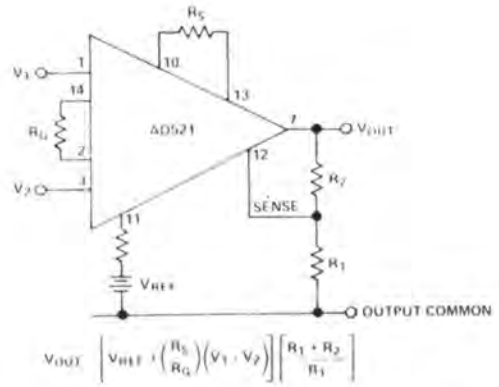



*Figure 4. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing $R_1$ and $R_2$ will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.*

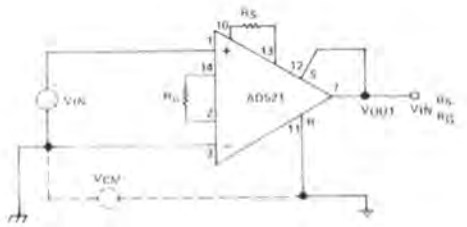



*Figure 5. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the 521.*

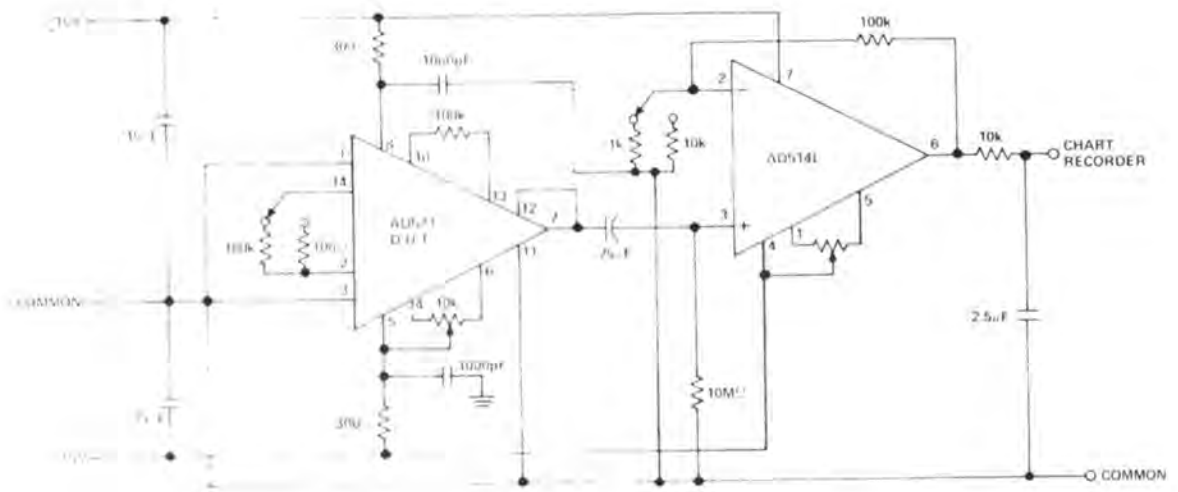



*Figure 6. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.*

# XR-2206

# Monolithic Function Generator

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The XR-2206 is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000: 1 frequency range with an external control voltage with very little affect on distortion.

As shown in Figure 1, the monolithic circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The internal current switches transfer the oscillator current to any one of the two external timing resistors to produce two discrete frequencies selected by the logic level at the FSK input terminal (pin 9).

## FEATURES

- Low Sinewave Distortion (THD .5%) – insensitive to signal sweep
- Excellent Stability (20 ppm/°C, typ)
- Wide Sweep Range (2000:1, typ)
- Low Supply Sensitivity (0.01%/V, typ)
- Linear Amplitude Modulation
- Adjustable Duty-Cycle (1% to 99%)
- TTL Compatible FSK Controls
- Wide Supply Range (10V to 26V)

## APPLICATIONS

- Waveform Generation
  - Sine, Square, Triangle, Ramp
- Sweep Generation
- AM/FM Generation
- FSK and PSK Generation
- Voltage-to-Frequency Conversion
- Tone Generation
- Phase-Locked Loops

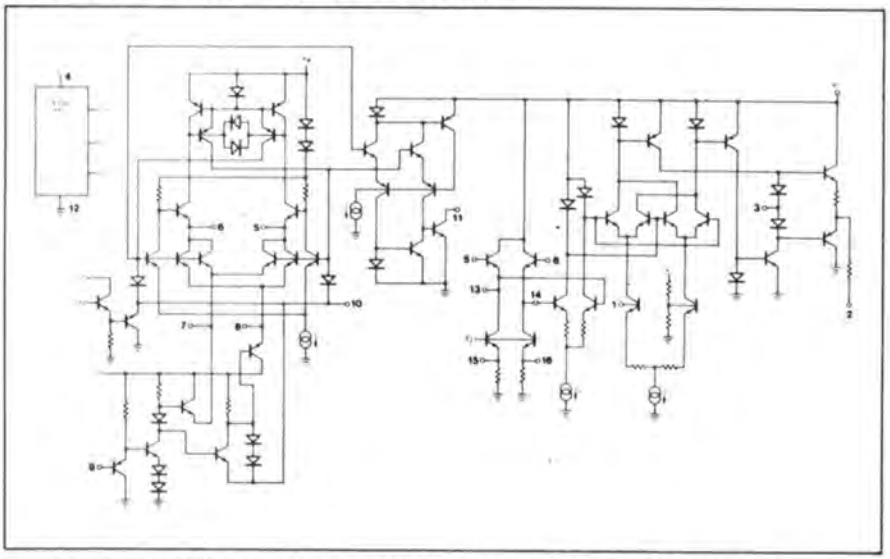
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | 26V |
| Power Dissipation | 750 mW |
| Derate above 25°C | 5 mW/°C |
| Total Timing Current | 6 mA |
| Storage Temperature | −65°C to +150°C |

## AVAILABLE TYPES

| Part Number | Package Types (16 Pin DIP) | Operating Temperature Range |
|---|---|---|
| XR-2206M | Ceramic | −55°C to +125°C |
| XR-2206N | Ceramic | 0°C to +75°C |
| XR-2206P | Plastic | 0°C to +75°C |
| XR-2206CN | Ceramic | 0°C to +75°C |
| XR-2206CP | Plastic | 0°C to +75°C |

## EQUIVALENT SCHEMATIC DIAGRAM



## FUNCTIONAL BLOCK DIAGRAM

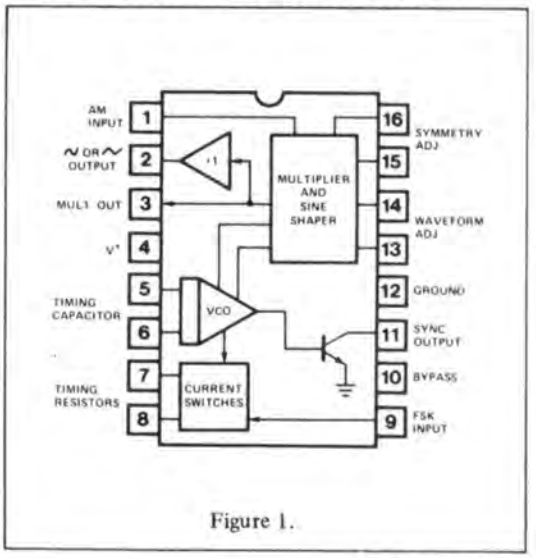



Figure 1.


**EXAR INTEGRATED SYSTEMS, INC.**
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(408) 732-7970 TWX 910-339-9233


10-75 REV 1

## ELECTRICAL CHARACTERISTICS

**Test Conditions:** Test Circuit of Fig. 2, $V^+ = 12V$, $T_A = 25°C$, $C = 0.01\ \mu F$, $R_1 = 100\ K\Omega$, $R_2 = 10\ K\Omega$ $R_3 = 25\ K\Omega$ unless otherwise specified. $S_1$ open for triangle, closed for sinewave.

| CHARACTERISTICS | XR-2206/XR-2206M | | | XR-2206C | | | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | |
| Supply Voltage | | | | | | | | |
| Single Supply | 10 | | 26 | 10 | | 26 | V | |
| Split Supply | ±5 | | ±13 | ±5 | | ±13 | V | |
| Supply Current | | 12 | 17 | | 14 | 20 | mA | $R_1 \geq 10\ K\Omega$ |
| Oscillator Section | | | | | | | | |
| Max. Operating Frequency | 0.5 | 1 | | 0.5 | 1 | | MHz | C=1000 pF, $R_1$=1 KΩ |
| Lowest Practical Frequency | | 0.01 | | | 0.01 | | Hz | C=50 μF, $R_1$=2 MΩ |
| Frequency Accuracy | | ±1 | ±4 | | ±2 | | % of $f_o$ | $f_o = 1/R_1C$ |
| Temperature Stability | | ±10 | ±50 | | ±20 | | ppm/°C | $0°C \leq T_A \leq 75°C$, $R_1=R_2=20\ K\Omega$ |
| Supply Sensitivity | | 0.01 | 0.1 | | 0.01 | | %/V | $V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20\ K\Omega$ |
| Sweep Range | 1000:1 | 2000:1 | | | 2000:1 | | $f_H = f_L$ | $f_H$ @ $R_1$ = 1 KΩ<br>$f_L$ @ $R_1$ = 2 MΩ |
| Sweep Linearity | | | | | | | | |
| 10:1 Sweep | | 2 | | | 2 | | % | $f_L$ = 1 kHz, $f_H$ = 10 kHz |
| 1000:1 Sweep | | 8 | | | 8 | | % | $f_L$ = 100 Hz, $f_H$ = 100 kHz |
| FM Distortion | | 0.1 | | | 0.1 | | % | ±10% Deviation |
| Recommended Timing Components | | | | | | | | |
| Timing Capacitor: C | 0.001 | | 100 | 0.001 | | 100 | μF | See Figure 5 |
| Timing Resistors: $R_1$ & $R_2$ | 1 | | 2000 | 1 | | 2000 | KΩ | |
| Triangle/Sinewave Output | | | | | | | | See Note 1, Fig. |
| Triangle Output | | 160 | | | 160 | | mV/KΩ | Fig. 2 $S_1$ Open |
| Sinewave Output | 40 | 60 | 80 | | 60 | | mV/KΩ | Fig. 2 $S_1$ Closed |
| Max. Output Swing | | 6 | | | 6 | | Vpp | |
| Output Impedance | | 600 | | | 600 | | Ω | |
| Triangle Linearity | | 1 | | | 1 | | % | |
| Amplitude Stability | | 0.5 | | | 0.5 | | dB | For 1000:1 Sweep |
| Sinewave Distortion | | | | | | | | $R_1$ = 30 KΩ |
| Without Adjustment | | 2.5 | | | 2.5 | | % | See Figure 11. |
| With Adjustment | | 0.4 | 1.0 | | 0.5 | 1.5 | % | See Figure 12 |
| Amplitude Modulation | | | | | | | | |
| Input Impedance | 50 | 100 | | 50 | 100 | | KΩ | |
| Modulation Range | | 100 | | | 100 | | % | |
| Carrier Suppression | | 55 | | | 55 | | dB | |
| Linearity | | 2 | | | 2 | | % | For 95% modulation |
| Square Wave Output | | | | | | | | Measured at Pin 11 |
| Amplitude | | 12 | | | 12 | | Vpp | |
| Rise Time | | 250 | | | 250 | | nsec | $C_L$ = 10 pF |
| Fall Time | | 50 | | | 50 | | nsec | $C_L$ = 10 pF |
| Saturation Voltage | | 0.2 | 0.4 | | 0.2 | 0.4 | V | $I_L$ = 2 mA |
| Leakage Current | | 0.1 | 20 | | 0.1 | 100 | μA | $V_{11}$= 26V |
| FSK Keying Level (Pin 9) | 0.8 | 1.4 | 2.4 | 0.8 | 1.4 | 2.4 | V | See Section on Circuit Controls |
| Reference Bypass Voltage | 2.9 | 3.1 | 3.3 | 2.5 | 3 | 3.5 | V | Measured at Pin 10. |

Note 1: Output Amplitude is inversely proportional to the resistance $R_3$ on Pin 3. See Figure 3

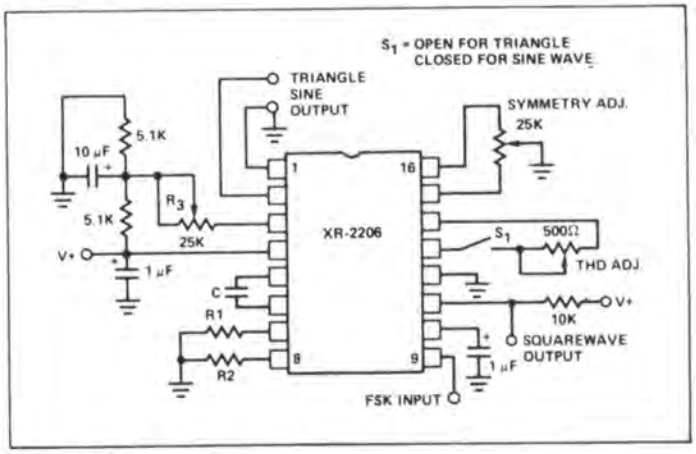



Figure 2. Basic Test Circuit

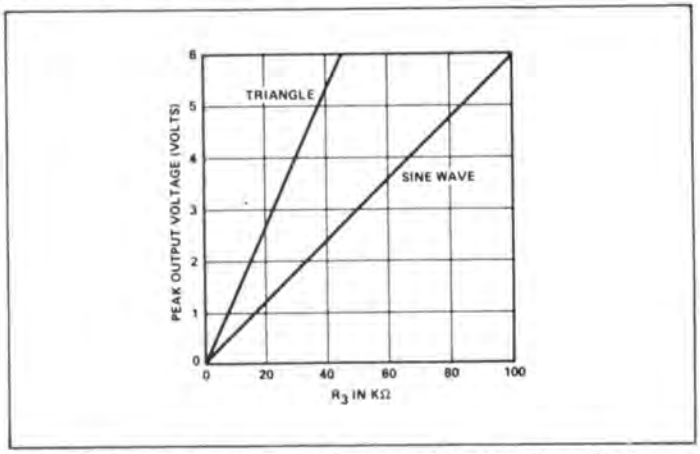



Figure 3. Output Amplitude as a Function of Resistor $R_3$ at Pin 3.

## TYPICAL OPTOELECTRONIC CHARACTERISTIC CURVES FOR EACH CHANNEL

**FIGURE 1. RELATIVE OUTPUT VS TEMPERATURE**

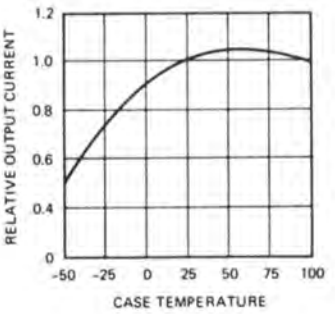



**FIGURE 2. DARK CURRENT VS TEMPERATURE**

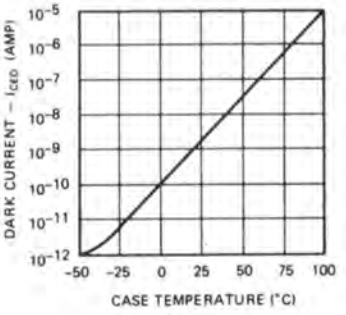



**FIGURE 3. TRANSFER CHARACTERISTICS**

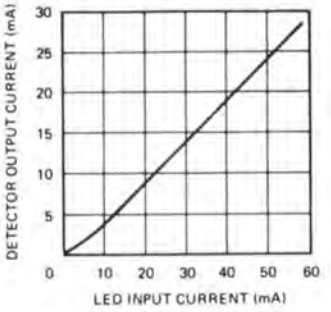



**FIGURE 4. DETECTOR OUTPUT CHARACTERISTICS**

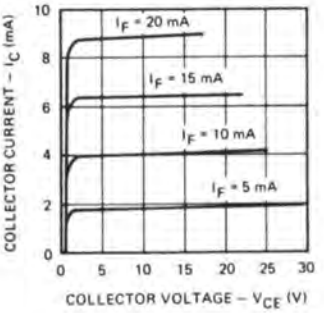
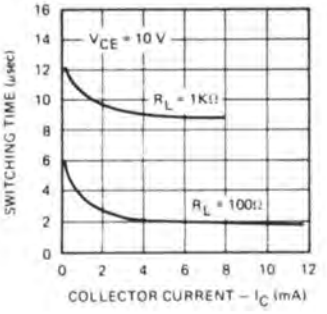


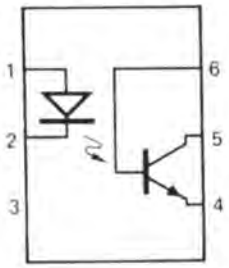

**FIGURE 5. SWITCHING TIME VS COLLECTOR CURRENT**



## PIN CONFIGURATIONS

### ISO-LIT 74

(TOP VIEW)

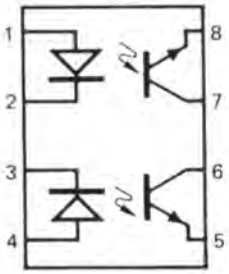



LED CHIP ON PIN 2
PT CHIP ON PIN 5

| PIN NO. | FUNCTION |
|---|---|
| 1 | ANODE |
| 2 | CATHODE |
| 3 | NC |
| 4 | EMITTER |
| 5 | COLLECTOR |
| 6 | BASE |

### ISO-LIT D74

(TOP VIEW)

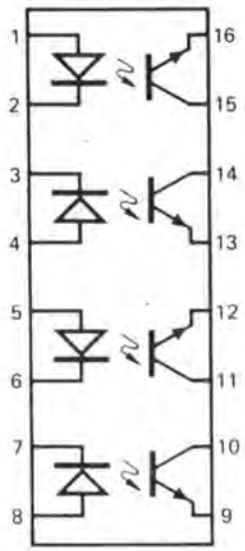



LED CHIPS ON PINS 2 AND 3
PT CHIPS ON PINS 6 AND 7

| PIN NO. | FUNCTION |
|---|---|
| 1 | ANODE |
| 2 | CATHODE |
| 3 | CATHODE |
| 4 | ANODE |
| 5 | EMITTER |
| 6 | COLLECTOR |
| 7 | COLLECTOR |
| 8 | EMITTER |

### ISO-LIT Q74

(TOP VIEW)




LED CHIPS ON PINS 2, 3, 6, 7
PT CHIPS ON PINS 10, 11, 14, 15

| PIN NO. | FUNCTION |
|---|---|
| 1 | ANODE |
| 2 | CATHODE |
| 3 | CATHODE |
| 4 | ANODE |
| 5 | ANODE |
| 6 | CATHODE |
| 7 | CATHODE |
| 8 | ANODE |
| 9 | EMITTER |
| 10 | COLLECTOR |
| 11 | COLLECTOR |
| 12 | EMITTER |
| 13 | EMITTER |
| 14 | COLLECTOR |
| 15 | COLLECTOR |
| 16 | EMITTER |

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

# HA-4741

## Quad Operational Amplifier

## FEATURES

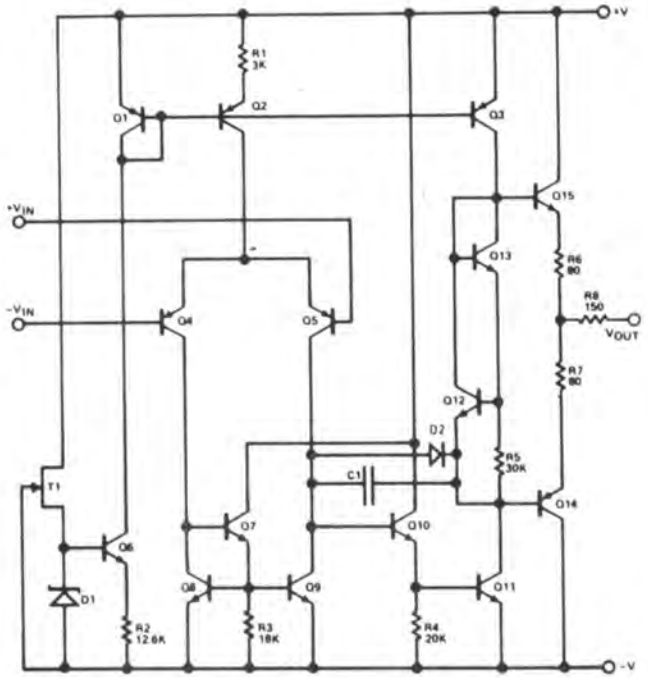
- SLEW RATE — 1.6 $V/\mu S$ (TYP.)
- BANDWIDTH — 3.5 MHz (TYP.)
- INPUT VOLTAGE NOISE (f = 1KHz) — 9 $NV/\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5 mV (TYP.)
- INPUT BIAS CURRENT — 60 nA (TYP.)
- SUPPLY RANGE — $\pm$2V to $\pm$20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

## DESCRIPTION

The HA-4741 contains four general purpose operational amplifiers on a monolithic chip. The performance of each amplifier is equal to or better than the 741 type amplifier in all respects. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

The HA-4741-2 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C.

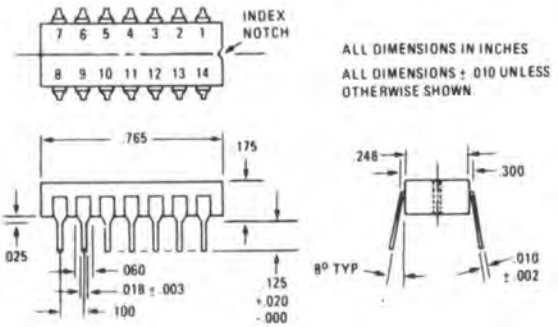
## SCHEMATIC DIAGRAM



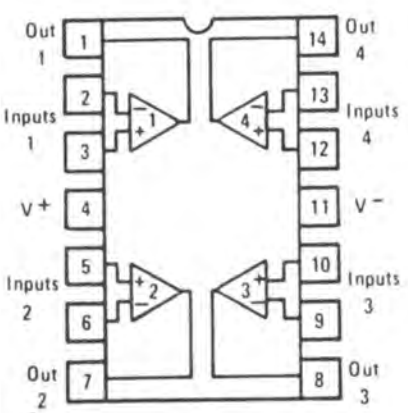

(¼) HA-4741

## PACKAGE/PIN OUT

14 LEAD CERAMIC D. I. P. (CERDIP)




PIN OUT



# SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

$T_A$ = +25°C Unless Otherwise Stated

| | |
|---|---|
| Voltage Between V+ and V− Terminals | 40.0V |
| Differential Input Voltage | ±30.0V |
| Input Voltage (Note 1) | ±15.0V |
| Output Short Circuit Duration (Note 2) | Indefinite |
| Power Dissipation (Note 3) | 880mW |
| Operating Temperature Range | |
| HA-4741-2 | $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ |
| HA-4741-5 | $0^{\circ}C \leq T_A \leq +75^{\circ}C$ |
| Storage Temperature Range | $-65^{\circ}C \leq T_A \leq +150^{\circ}C$ |

## ELECTRICAL CHARACTERISTICS

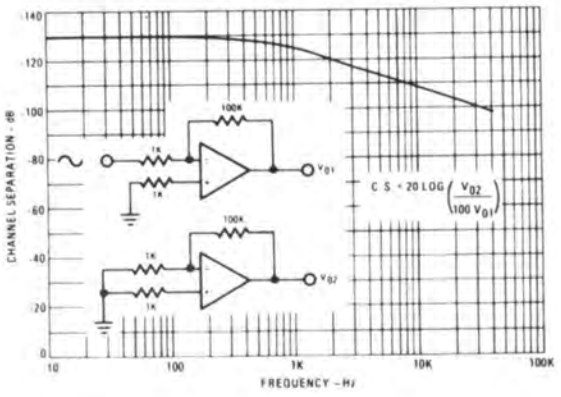
V+ = 15V, V− = −15V

| PARAMETER | TEMP. | HA-4741-2 −55°C to +125°C MIN. | TYP. | MAX. | HA-4741-5 0°C to +75°C MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | | |
| Offset Voltage | +25°C | | 0.5 | 3.0 | | 1.0 | 5.0 | mV |
| | Full | | 4.0 | 5.0 | | 5.0 | 6.5 | mV |
| Av. Offset Voltage Drift | Full | | 5 | | | 5 | | µV/°C |
| Bias Current | +25°C | | 60 | 200 | | 60 | 300 | nA |
| | Full | | | 325 | | | 400 | nA |
| Offset Current | +25°C | | 15 | 30 | | 30 | 50 | nA |
| | Full | | | 75 | | | 100 | nA |
| Common Mode Range | Full | ±12 | | | ±12 | | | V |
| Differential Input Resistance | +25°C | | 5 | | | 5 | | MΩ |
| Input Noise Voltage (f = 1KHz) | +25°C | | 9 | | | 9 | | $nV/\sqrt{Hz}$ |
| **TRANSFER CHARACTERISTICS** | | | | | | | | |
| Large Signal Voltage Gain (Note 4) | +25°C | 50K | 100K | | 25K | 50K | | V/V |
| | Full | 25K | | | 15K | | | V/V |
| Common Mode Rejection Ratio (Note 8) | +25°C | 80 | | | 80 | | | dB |
| | Full | 74 | | | 74 | | | dB |
| Channel Separation (Note 5) | +25°C | | −108 | | | −108 | | dB |
| Small Signal Bandwidth | +25°C | | 3.5 | | | 3.5 | | MHz |
| **OUTPUT CHARACTERISTICS** | | | | | | | | |
| Output Voltage Swing ($R_L$ = 10K) | Full | ±12 | ±13.7 | | ±12 | ±13.7 | | V |
| ($R_L$ = 2K) | Full | ±10 | ±12.5 | | ±10 | ±12.5 | | V |
| Full Power Bandwidth (Note 4) | +25°C | | 25 | | | 25 | | KHz |
| Output Current (Note 6) | Full | ±5 | ±15 | | ±5 | ±15 | | mA |
| Output Resistance | +25°C | | 300 | | | 300 | | Ω |
| **TRANSIENT RESPONSE (Note 7)** | | | | | | | | |
| Rise Time | +25°C | | 75 | | | 75 | | ns |
| Overshoot | +25°C | | 25 | | | 25 | | % |
| Slew Rate | +25°C | | ±1.6 | | | ±1.6 | | V/µs |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | | | |
| Supply Current ($I^+$ or $I^-$) | +25°C | | | 5.0 | | | 7.0 | mA |
| Power Supply Rejection Ratio (Note 8) | Full | 80 | | | 80 | | | dB |

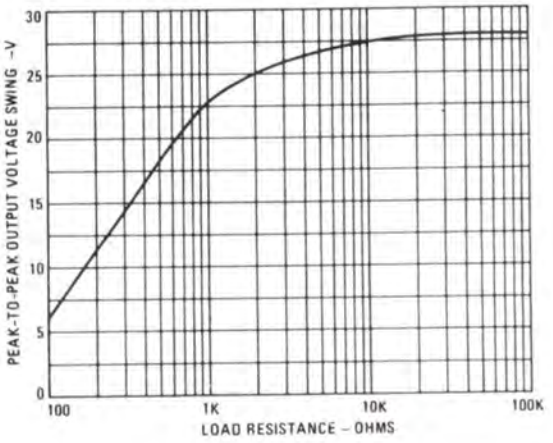
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above $T_A$ = +25°C.
4. $V_{OUT}$ = ±10, $R_L$ = 2K
5. Referred to input; f = 10KHz, $R_S$ = 1K
6. $V_{OUT}$ = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

## PERFORMANCE CURVES (cont'd.)

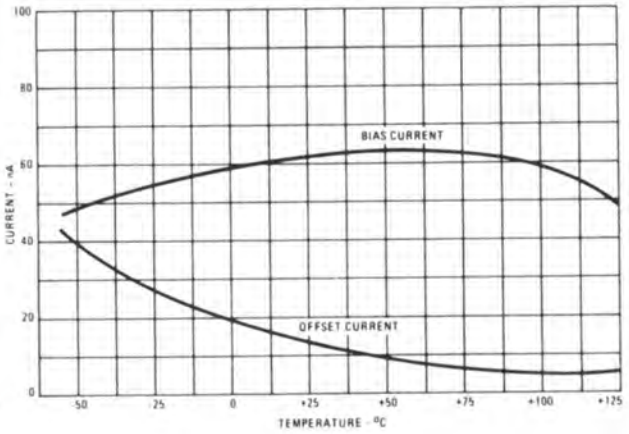
### CHANNEL SEPARATION VS. FREQUENCY



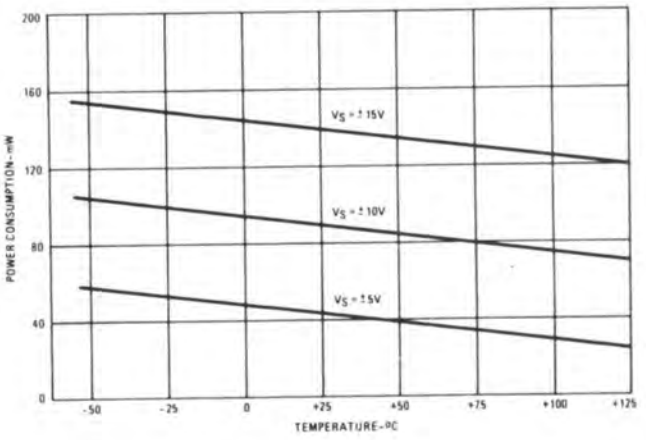

### MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE




### INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

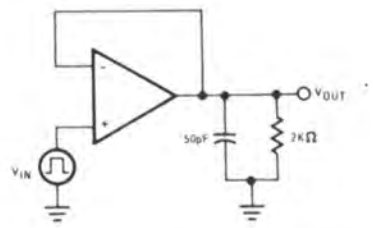



### POWER CONSUMPTION VS. TEMPERATURE

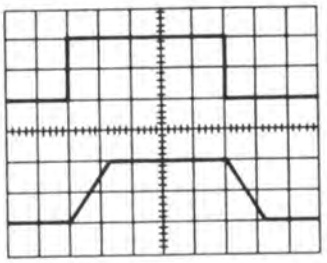



## PULSE RESPONSE

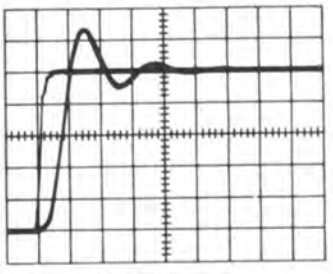
### TRANSIENT RESPONSE/SLEW RATE CIRCUIT




### SLEW RESPONSE (Volts: 5V/Div, Time: 5μs/Div)



### TRANSIENT RESPONSE (Volts: 10mv/Div , Time: 100ns/Div )



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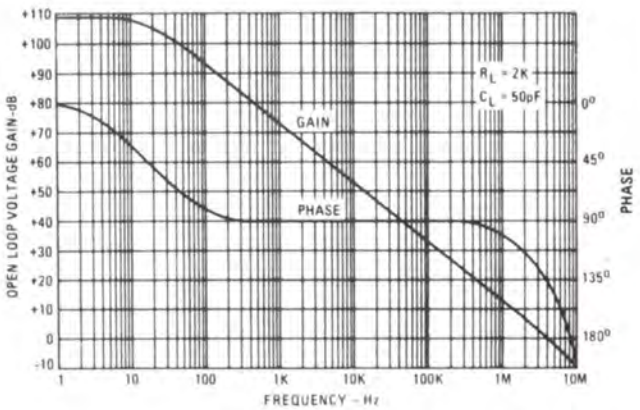
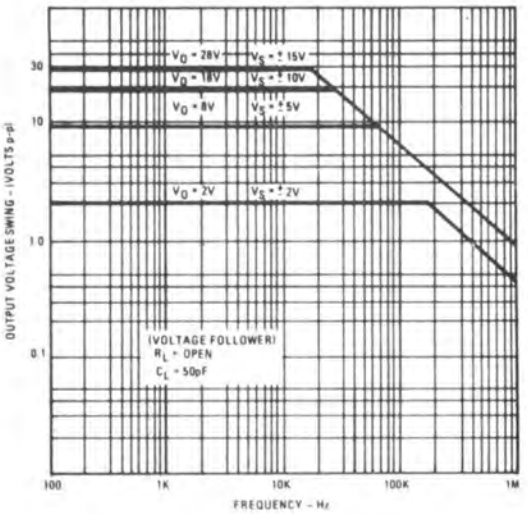
## PERFORMANCE CURVES

$V+ = +15V$, $V- = -15V$, $T_A = +25^oC$
Unless Otherwise Stated.

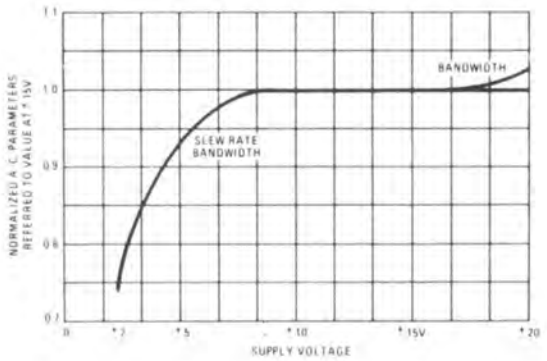
### OPEN LOOP FREQUENCY RESPONSE



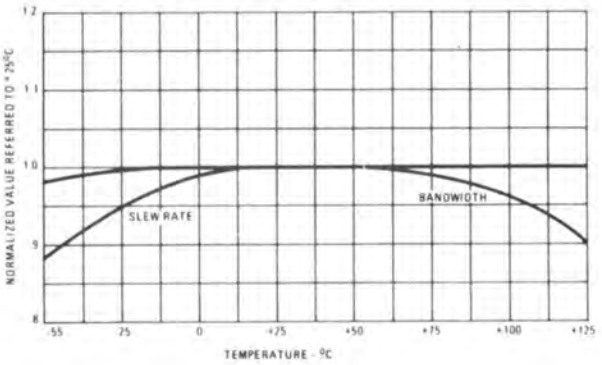

### OUTPUT VOLTAGE SWING VS. FREQUENCY



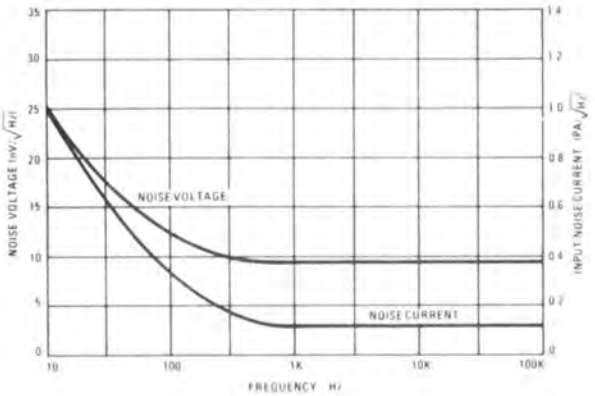

### NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



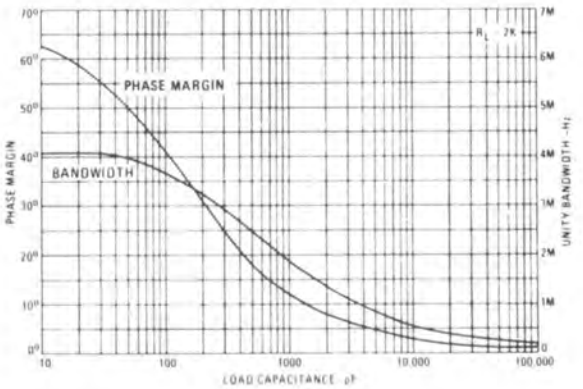

### NORMALIZED AC PARAMETERS VS. TEMPERATURE




### INPUT NOISE VS. FREQUENCY

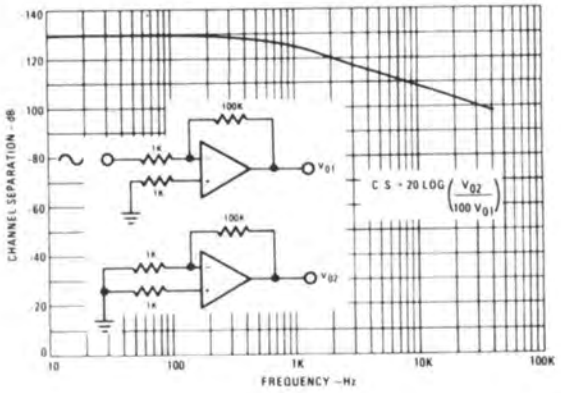



### SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE

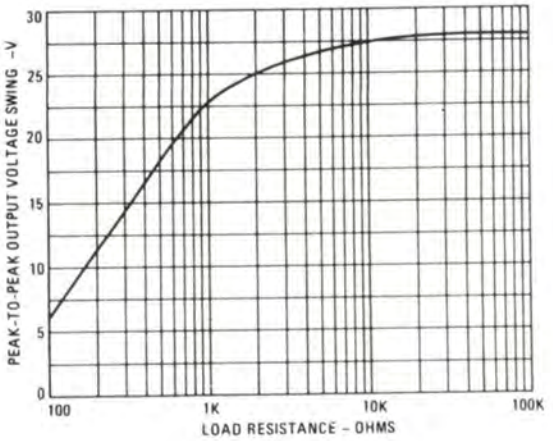


## PERFORMANCE CURVES (cont'd.)

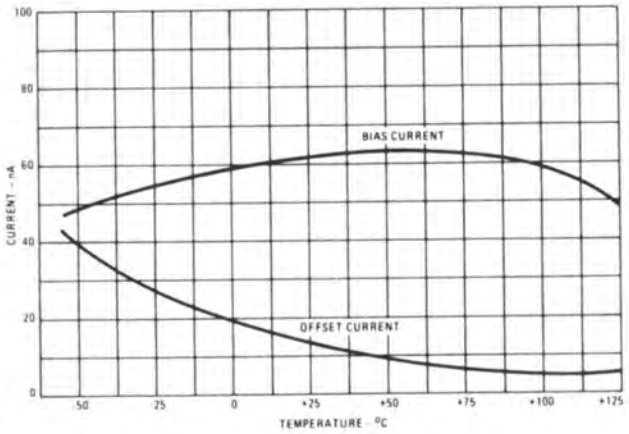
### CHANNEL SEPARATION VS. FREQUENCY



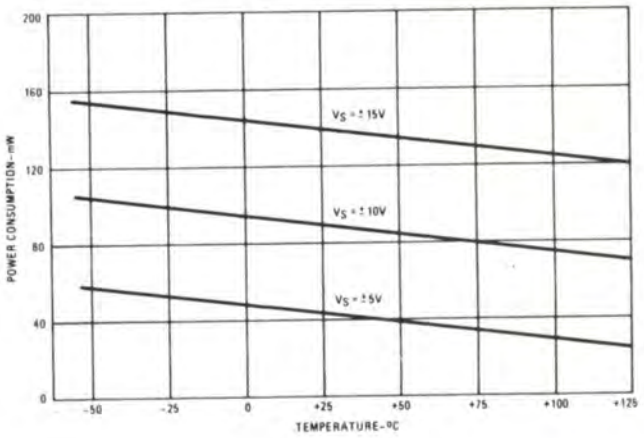

### MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE




### INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE




### POWER CONSUMPTION VS. TEMPERATURE




## PULSE RESPONSE

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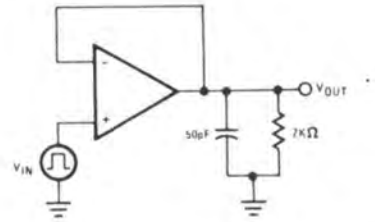


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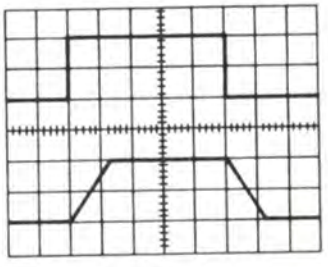

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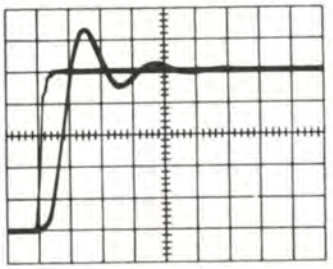

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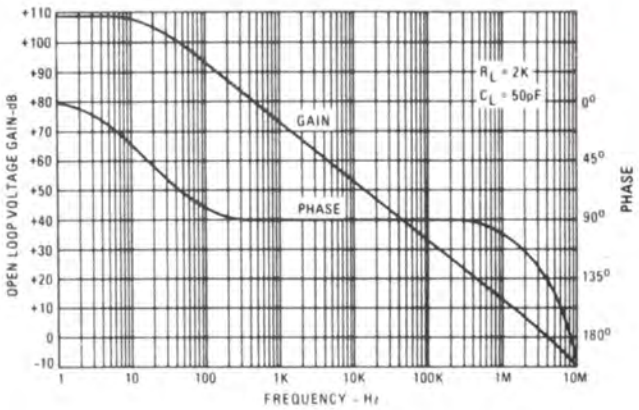
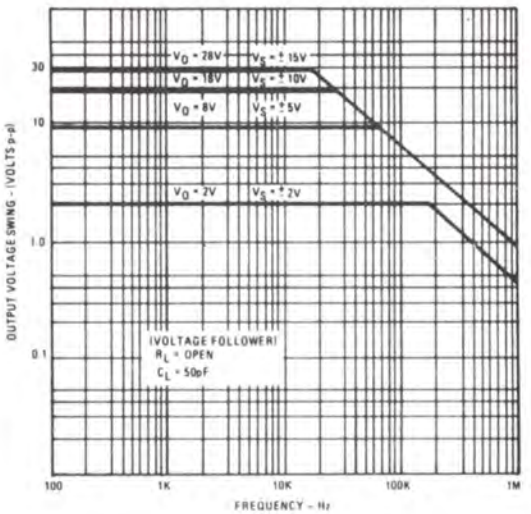
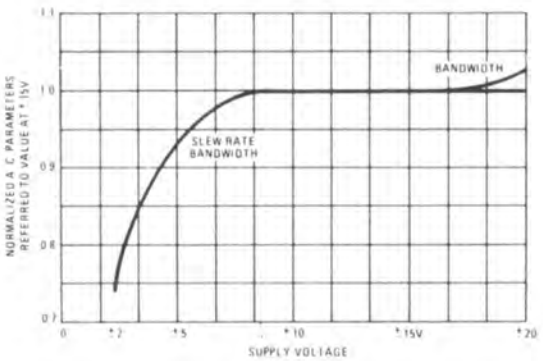


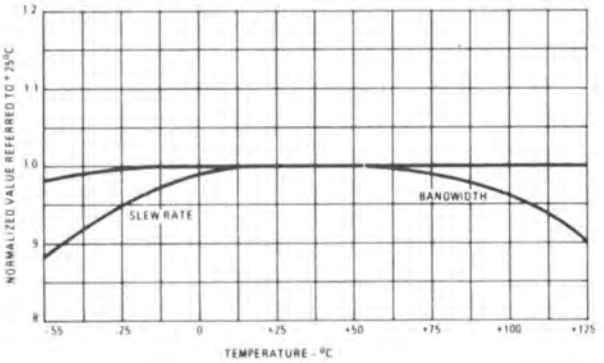

### OUTPUT VOLTAGE SWING VS. FREQUENCY



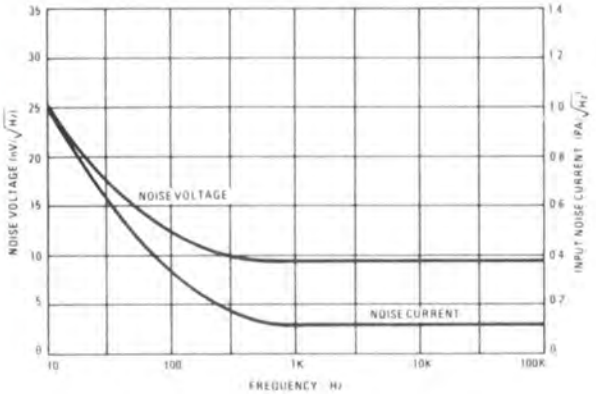

### NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



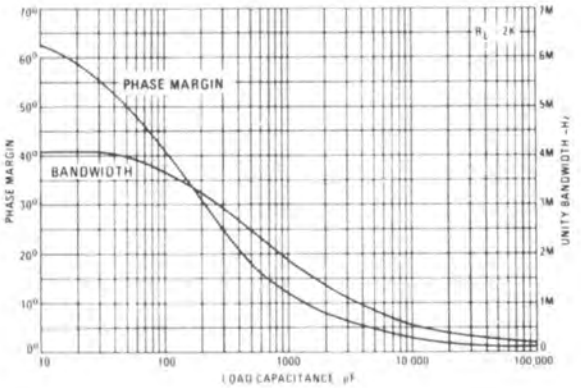

### NORMALIZED AC PARAMETERS VS. TEMPERATURE




### INPUT NOISE VS. FREQUENCY



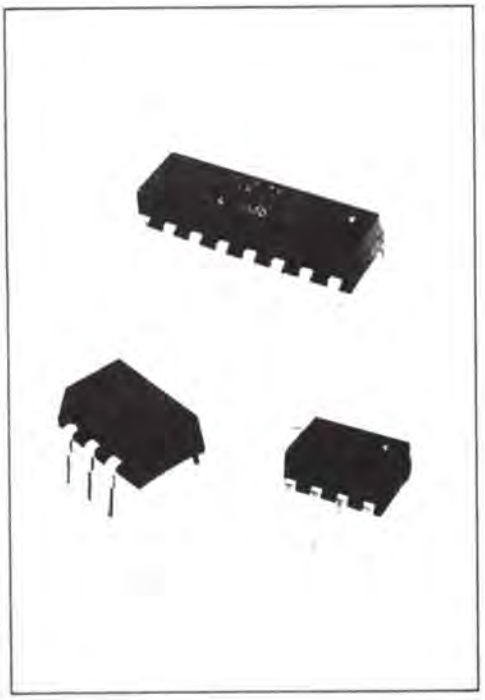

### SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



litronix

# Iso-Lit 74 Series
## IL-74, ILD-74, ILQ-74

### LOGIC-DRIVE OPTO-ISOLATOR



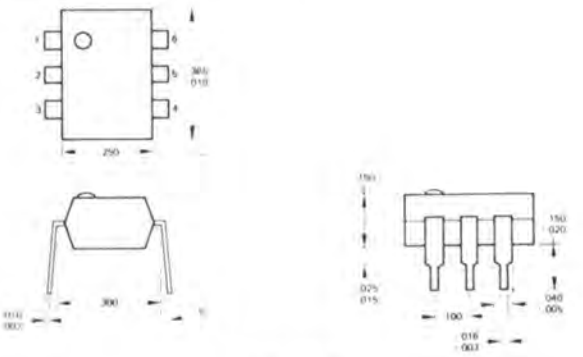
### FEATURES

- 7400 series $T^2L$ compatible
- 1500 volt breakdown voltage
- 35% typical transfer ratio
- 0.5 pF coupling capacitance
- Industry standard dual-in-line package
- Single channel, dual, and quad configurations

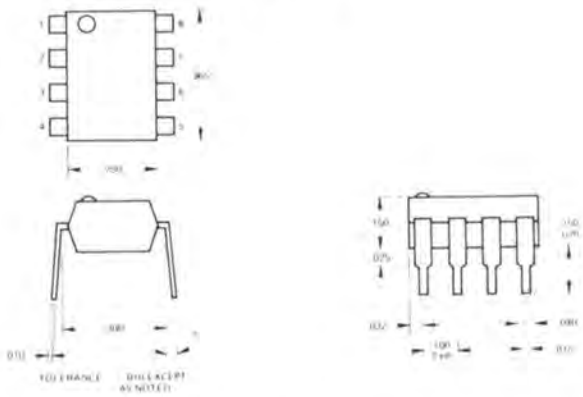
### DESCRIPTION

IL-74 is an optically coupled pair employing a Gallium Arsenide infrared LED and a silicon NPN phototransistor. Signal information, including a DC level, can be transmitted by the device while maintaining a high degree of electrical isolation between input and output. The IL-74 is especially designed for driving medium-speed logic, where it may be used to eliminate troublesome ground loop and noise problems. It can also be used to replace relays and transformers in many digital interface applications, as well as analog applications such as CRT modulation. The ILD-74 offers two isolated channels in a single DIP package while the ILQ-74 provides four isolated channels per package.

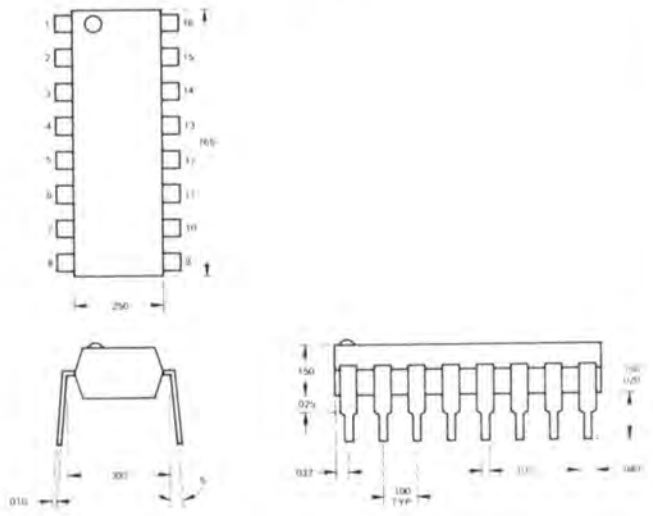
**Package Dimensions** (in inches)



ISO-LIT 74



ISO-LIT D74



ISO-LIT Q74

ISO-LIT 74, ISO-LIT D74, ISO-LIT Q74 LOGIC-DRIVE OPTO-ISOLATOR/FEBRUARY 1976

LITRONIX, INC., 19000 HOMESTEAD ROAD / VALLCO PARK / CUPERTINO, CALIF. 95014 / (408) 257-7910 / TWX 910-338-0022

## MAXIMUM RATINGS

Gallium Arsenide LED (each channel)
- Power Dissipation @ 25°C . . . . . 150 mW
- Derate Linearly from 25°C . . . . . −1.33 mW/°C
- Continuous Forward Current . . . . . 100 mA
- Peak Inverse Voltage . . . . . 3.0V

Detector-Silicon Phototransistor (each channel)
- Power Dissipation @ 25°C . . . . . 150 mW
- Derate Linearly from 25°C . . . . . 2.0 mW/°C
- Collector-Emitter Breakdown Voltage ($BV_{CEO}$) . . . . . 20V

Package
- Total Package Dissipation at 25°C Ambient (LED Plus Detector)
  - IL-74 . . . . . 200 mW
  - ILD-74 . . . . . 400 mW
  - ILQ-74 . . . . . 500 mW
- Derate Linearly From 25°C
  - IL-74 . . . . . 3.3 mW/°C
  - ILD-74 . . . . . 5.33 mW/°C
  - ILQ-74 . . . . . 6.67 mW/°C
- Storage Temperature . . . . . −55°C to +150°C
- Operating Temperature . . . . . −55°C to +100°C
- Lead Soldering Time @ 260°C . . . . . 7.0 sec

## ELECTRICAL CHARACTERISTICS PER CHANNEL (at 25°C Ambient)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| Gallium Arsenide LED | | | | | |
| Forward Voltage | | 1.3 | | V | $I_F$ = 100 mA |
| Reverse Current | | 0.1 | | μA | $V_R$ = 3.0V |
| Capacitance | | 100 | | pF | $V_R$ = 0 |
| Phototransistor Detector | | | | | |
| $BV_{CEO}$ | 20 | | | V | $I_C$ = 1 mA |
| $I_{CEO}$ | | 5.0 | 500 | nA | $V_{CE}$ = 5V, $I_F$ = 0 |
| Collector-Emitter Capacitance | | 2.0 | | pF | $V_{CE}$ = 0 |
| Coupled Characteristics | | | | | |
| DC Current Transfer Ratio | 0.125 | 0.35 | | | $I_F$ = 16 mA, $V_{CE}$ = 5V |
| Capacitance, Input to Output | | 0.5 | | pF | |
| Breakdown Voltage | 1500 | | | V | |
| Resistance, Input to Output | | 100 | | GΩ | |
| $V_{SAT}$ | | | 0.5 | V | $I_C$ = 2 mA, $I_F$ = 16 mA |
| Propagation Delay | | | | | |
| $t_{D\,ON}$ | | 6.0 | | μs | $R_L$ = 2.4KΩ, $V_{CE}$ = 5V |
| $t_{D\,OFF}$ | | 25 | | μs | $I_F$ = 16 mA |

**NOTE:** IL-74 only, does not apply to the ILD-74 or ILQ-74.

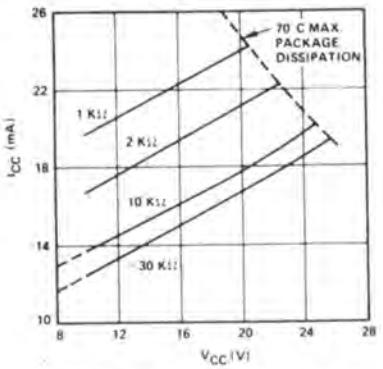



Figure 4. Supply Current vs Supply Voltage, Timing R

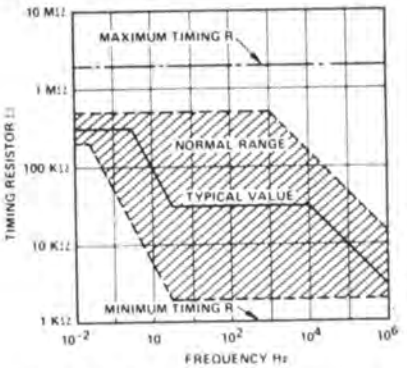



Figure 5. R vs Oscillation Frequency

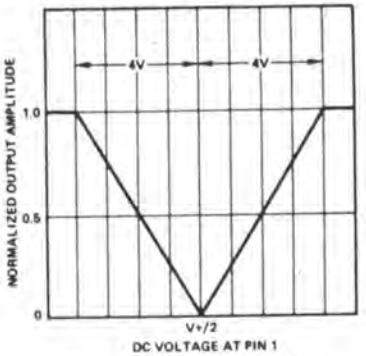



Figure 6. Normalized Output Amplitude vs DC Bias at AM Input (Pin 1).

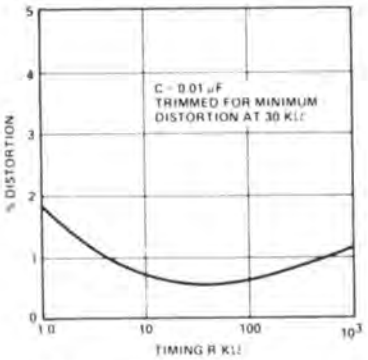



Figure 7. Trimmed Distortion vs Timing Resistor

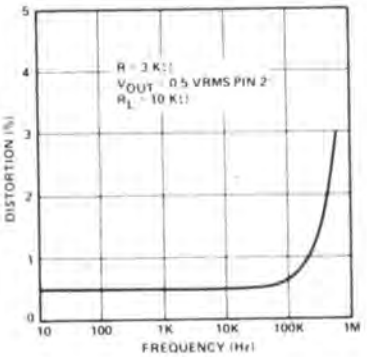



Figure 8. Signwave Distortion vs Operating Frequency With Timing Capacitors Varied

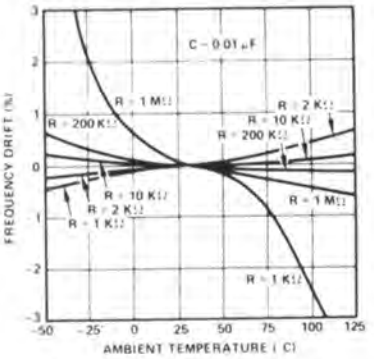



Figure 9. Frequency Drift vs Temperature

## DESCRIPTION OF CIRCUIT CONTROLS

### FREQUENCY OF OPERATION:

The frequency of oscillation, $f_o$, is determined by the external timing capacitor C across pins 5 and 6, and by the timing resistor R connected to either pin 7 or pin 8. The frequency is given as

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R for a given frequency range are shown in Figure 5. Temperature-stability is optimum for 4 KΩ < R < 200 KΩ. Recommended values of C are from 1000 pF to 100 μF.

### FREQUENCY SWEEP AND MODULATION

Frequency of oscillation is porportional to the *total* timing current $I_T$ drawn from pin 7 or 8

$$f = \frac{320 I_T \text{ (mA)}}{C \text{ (}\mu\text{F)}} \text{ Hz}$$

Timing terminals (pins 7 or 8) are low impedance points and are internally biased at +3V, with respect to pin 12. Frequency varies linearly with $I_T$ over a wide range of current values, from 1 μA to 3 mA. The frequency can be controlled by applying a control voltage, $V_C$, to the activated timing pin as shown in Figure 10. The frequency of oscillation is related to $V_C$ as:

$$f = \frac{1}{RC}\left[1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right] \text{ Hz}$$

where $V_C$ is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_C C} \text{ Hz/V}$$

NOTE: For safe operation of the circuit $I_T$ should be limited to ⩽3 mA.

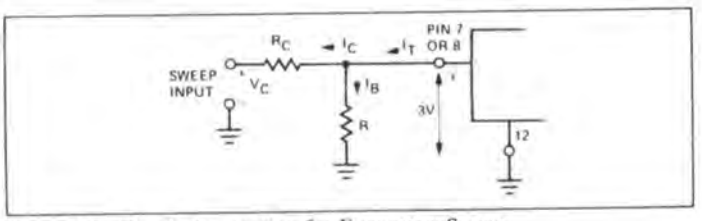



Figure 10. Circuit Connection for Frequency Sweep

### OUTPUT CHARACTERISTICS:

**Output Amplitude:** Maximum output amplitude is inversely porportional to external resistor $R_3$ connected to Pin 3 (See Fig. 3). For sinewave output, amplitude is approximately 60 mV peak per KΩ of $R_3$; for triangle, the peak amplitude is approximately 160 mV peak per KΩ of $R_3$. Thus, for example, $R_3$ = 50 KΩ would produce approximately ±3V sinusoidal output amplitude.

**Amplitude Modulation:** Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100 KΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ±4 volts of $V^+/2$ as shown in Fig. 6. As this bias level approaches $V^+/2$, the phase of the output signal is reversed; and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

Note: AM control must be used in conjunction with a well-regulated supply since the output amplitude now becomes a function of $V^+$.

### FREQUENCY-SHIFT KEYING

The XR-2206 can be operated with two separate timing resistors, $R_1$ and $R_2$, connected to the timing pins 7 and 8, respectively, as shown in Figure 13. Depending on the polarity of the logic signal at pin 9, either one or the other of these timing

resistors is activated. If pin 9 is open-circuited or connected to a bias voltage $\geq 2V$, only $R_1$ is active. Similarly, if the voltage level at pin 9 is $\leq 1V$, only $R_2$ is activated. Thus, the output frequency can be keyed between two levels, $f_1$ and $f_2$ as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at pin 9 is referenced to $V^-$.

### OUTPUT DC LEVEL CONTROL

The dc level at the output (pin 2) is approximately the same as the dc bias at pin 3. In Figures 11, 12 and 13, pin 3 is biased mid-way between $V^+$ and ground, to give an output dc level of $\approx V^+/2$.

## APPLICATIONS INFORMATION

### SINEWAVE GENERATION

**A) Without External Adjustment**

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer $R_1$ at pin 7 provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$ and the

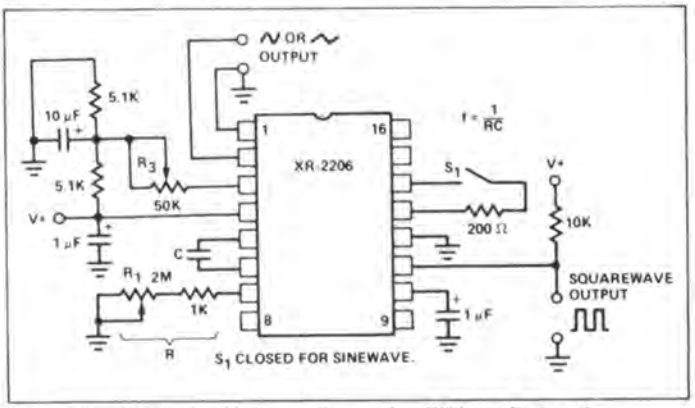



Figure 11. Circuit for Sinewave Generation Without External Adjustment. (See Fig. 3 for choice of $R_3$)

typical distortion (THD) is $< 2.5\%$. If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split supply operation simply by replacing all ground connections with $V^-$. For split supply operation, $R_3$ can be directly connected to ground.

**B) With External Adjustment**

The harmonic content of sinusoidal output can be reduced to $\approx 0.5\%$ by additional adjustments as shown in Figure 12. The potentiometer $R_A$ adjusts the sine-shaping resistor;

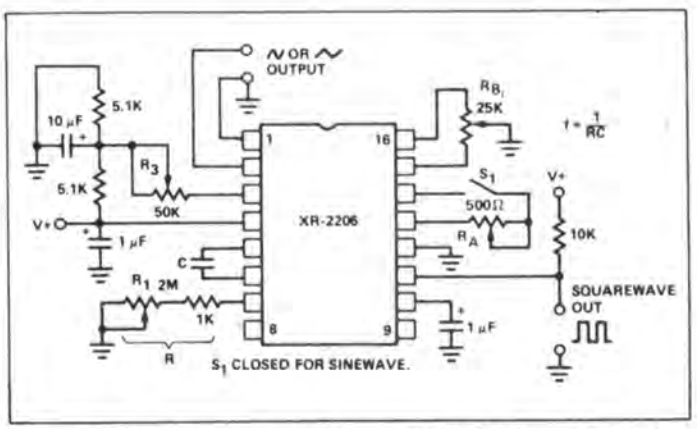



Figure 12. Circuit for Sinewave Generation With Minimum Harmonic Distortion. ($R_3$ Determines output Swing – See Fig. 3)

and $R_B$ provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set $R_B$ at mid-point and adjust $R_A$ for minimum distortion.
2. With $R_A$ set as above, adjust $R_B$ to further reduce distortion.

### TRIANGLE WAVE GENERATION

The circuits of Figures 11 and 12 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., $S_1$ open). Amplitude of the triangle is approximately twice the sinewave output.

### FSK GENERATION

Figure 13 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors $R_1$ and $R_2$; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with $V^-$.

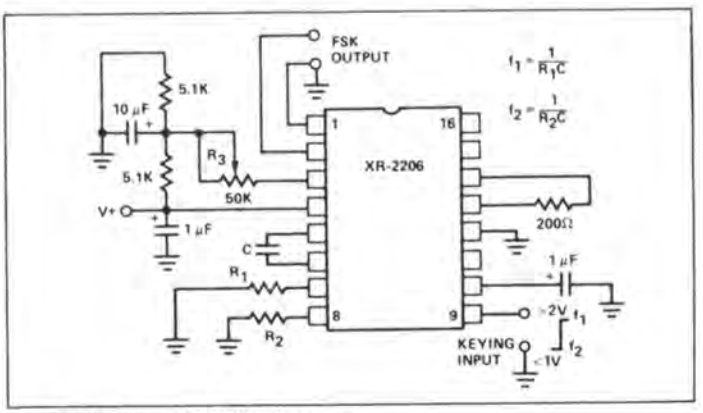



Figure 13. Sinusoidal FSK Generator

### PULSE AND RAMP GENERATION

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of $R_1$ and $R_2$. The values of $R_1$ and $R_2$ should be in the range of 1 KΩ to 2 MΩ.

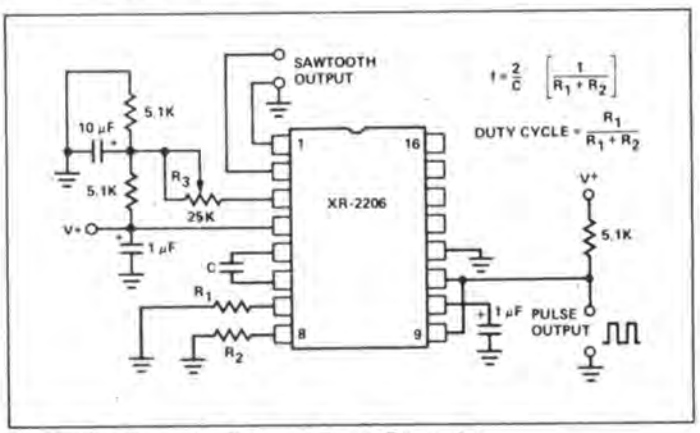



Figure 14. Circuit for Pulse and Ramp Generation

# Operational Amplifiers

## LM318 operational amplifier general description

The LM318 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

## features

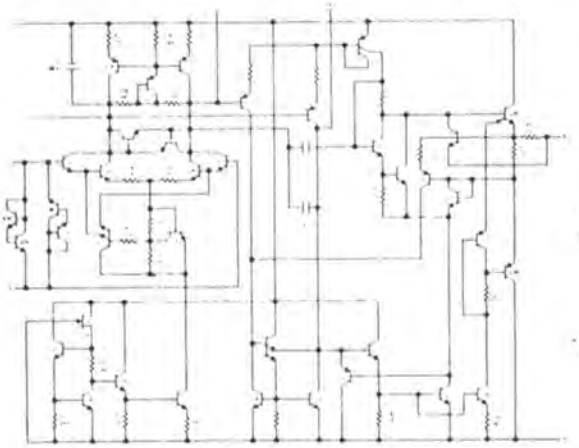
- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 500 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

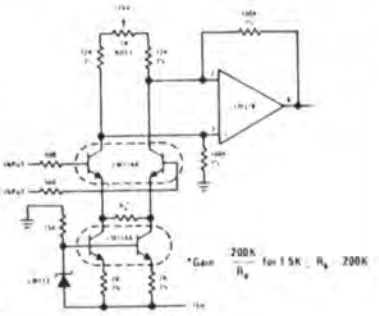
The LM318 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM318 is specified for operation over 0°C to 70°C.

## schematic diagram and typical application



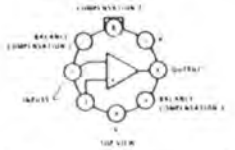


*Gain $\frac{200K}{R_g}$ for 1 5K < $R_g$ < 200K

Instrumentation Amplifier

## connection diagrams

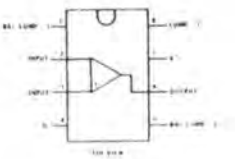
Metal Can Package*



*Pin connections shown on schematic diagram and typical applications are for TO 5 package.

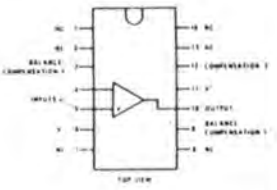
Order Number LM318H
See Package 11

Dual-In-Line Package



Order Number LM318N
See Package 20

Dual In Line Package



Order Number LM318D
See Package 1

## absolute maximum ratings

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

## electrical characteristics (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$ | | 4 | 10 | mV |
| Input Offset Current | $T_A = 25°C$ | | 30 | 200 | nA |
| Input Bias Current | $T_A = 25°C$ | | 150 | 500 | nA |
| Input Resistance | $T_A = 25°C$ | 0.5 | 3 | | MΩ |
| Supply Current | $T_A = 25°C$ | | 5 | 10 | mA |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = ±15V$<br>$V_{OUT} = ±10V$, $R_L \geq 2\ k\Omega$ | 25 | 200 | | V/mV |
| Slew Rate | $T_A = 25°C$, $V_S = ±15V$, $A_V = 1$ | 50 | 70 | | V/μs |
| Small Signal Bandwidth | $T_A = 25°C$, $V_S = ±15V$ | | 15 | | MHz |
| Input Offset Voltage | | | | 15 | mV |
| Input Offset Current | | | | 300 | nA |
| Input Bias Current | | | | 750 | nA |
| Large Signal Voltage Gain | $V_S = ±15V$, $V_{OUT} = ±10V$<br>$R_L \geq 2\ k\Omega$ | 20 | | | V/mV |
| Output Voltage Swing | $V_S = ±15V$, $R_L = 2\ k\Omega$ | ±12 | ±13 | | V |
| Input Voltage Range | $V_S = ±15V$ | ±11.5 | | | V |
| Common Mode Rejection Ratio | | 70 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 65 | 80 | | dB |

**Note 1:** The maximum junction temperature of the LM318 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

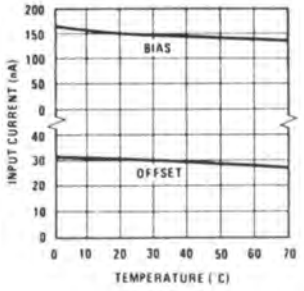
**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

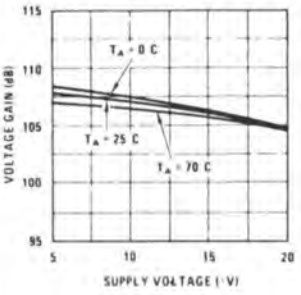
**Note 4:** These specifications apply for $±5V \leq V_S \leq ±20V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified. For proper operation, the power supplies must be bypassed with 0.1 μF disc capacitors.

## typical performance characteristics

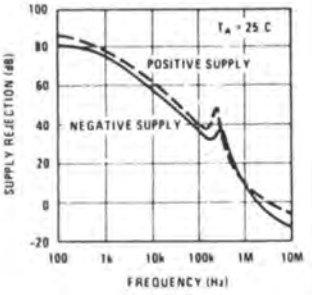
Input Current



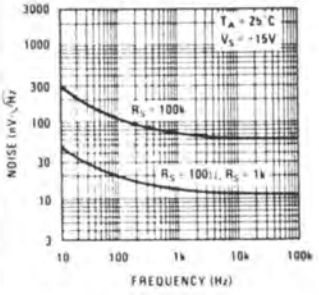

Voltage Gain



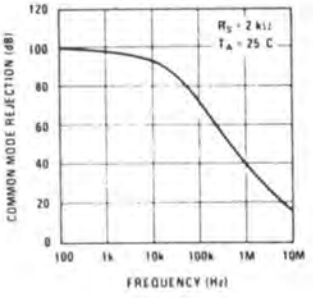

Power Supply Rejection



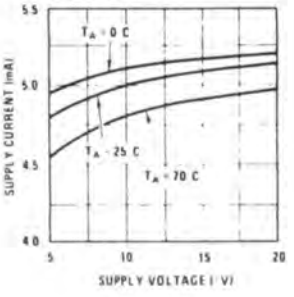

Input Noise Voltage



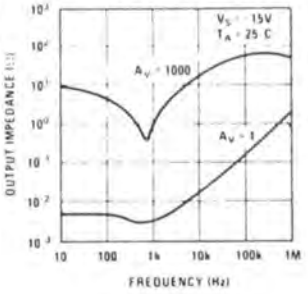

Common Mode Rejection



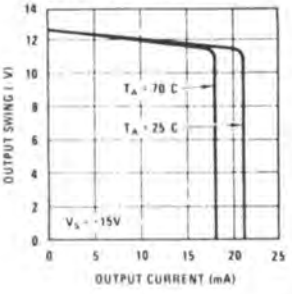

Supply Current



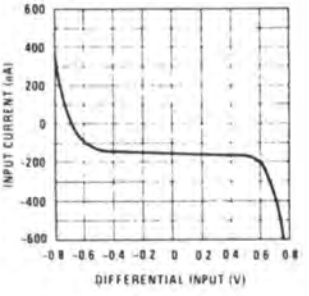

Closed Loop Output Impedance



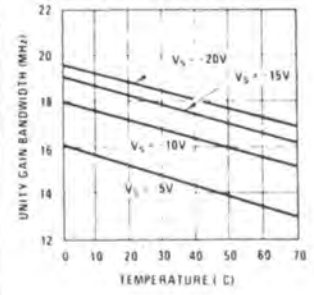

Current Limiting



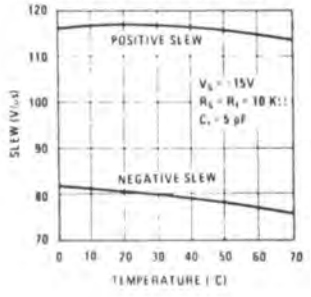

Input Current



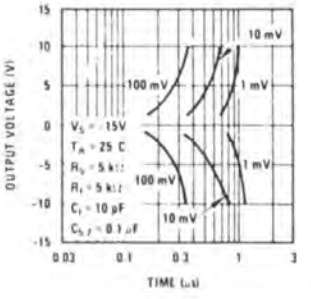

Unit Gain Bandwidth




Voltage Follower Slew Rate

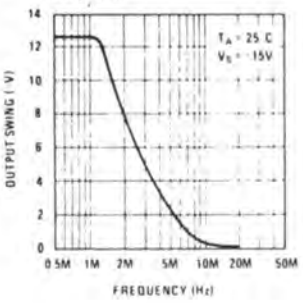



Inverter Settling Time

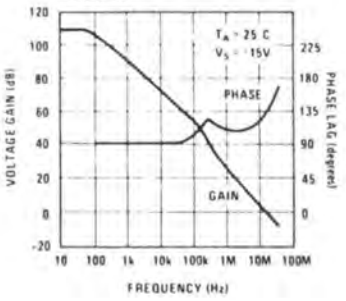


## typical performance characteristics (con't)

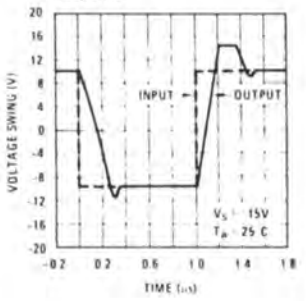
Large Signal Frequency Response



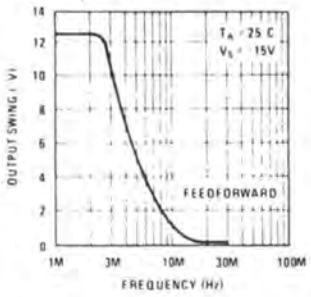

Open Loop Frequency Response



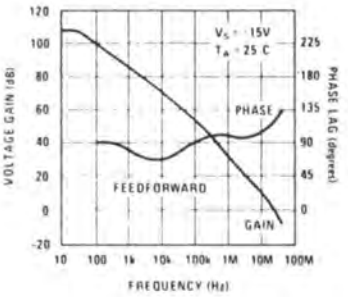

Voltage Follower Pulse Response



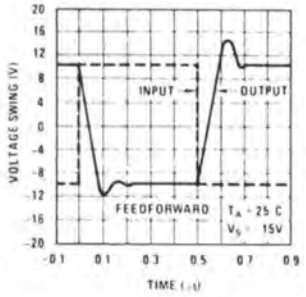

Large Signal Frequency Response



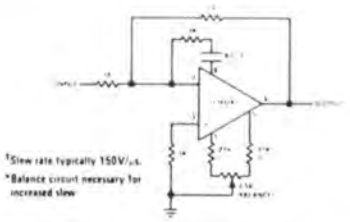

Open Loop Frequency Response



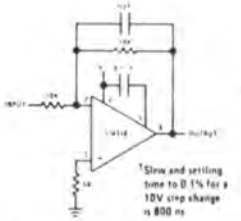

Inverter Pulse Response



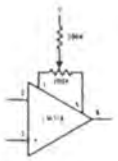

## auxiliary circuits



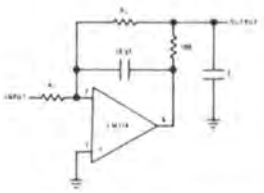

Feedforward Compensation for Greater Inverting Slew Rate†



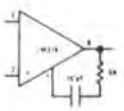

Compensation for Minimum Settling† Time



Offset Balancing

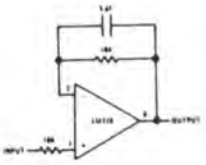


Isolating Large Capacitive Loads

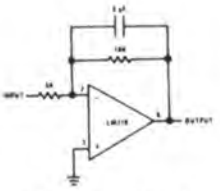


Overcompensation

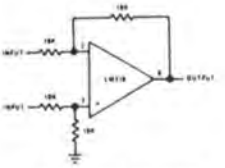
## typical applications (con't)



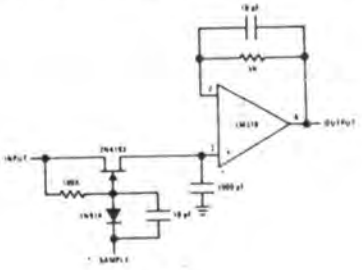
Fast Voltage Follower



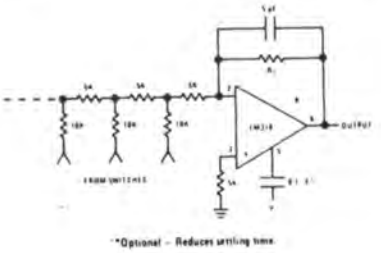
Fast Summing Amplifier



Differential Amplifier

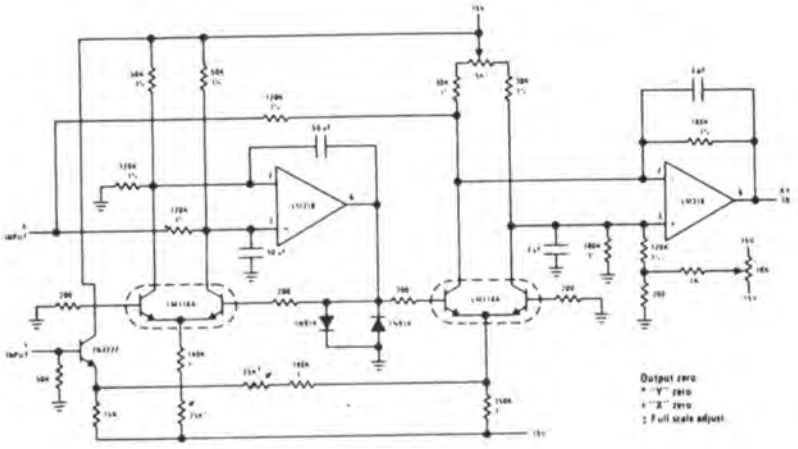


Fast Sample and Hold

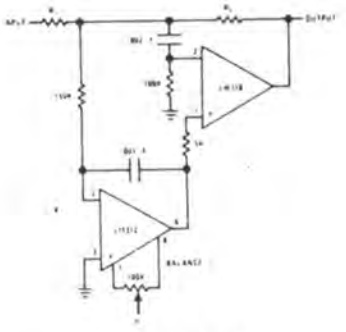


**Optional – Reduces settling time.

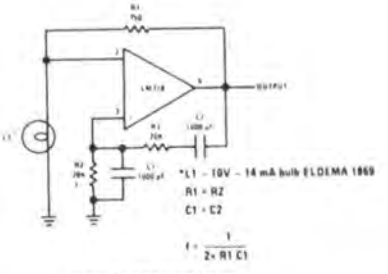
D/A Converter Using Ladder Network



Four Quadrant Multiplier



Fast Summing Amplifer with Low Input Current



Wein Bridge Sine Wave Oscillator

# SYNCHRONOUS 4-BIT BINARY COUNTER

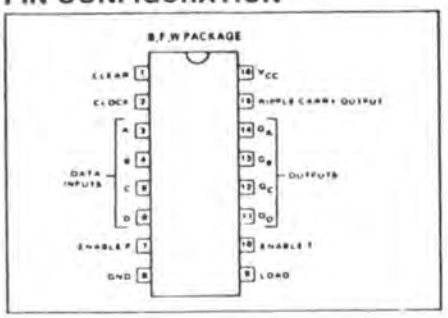


54LS161-F,W • 74LS161-B,F

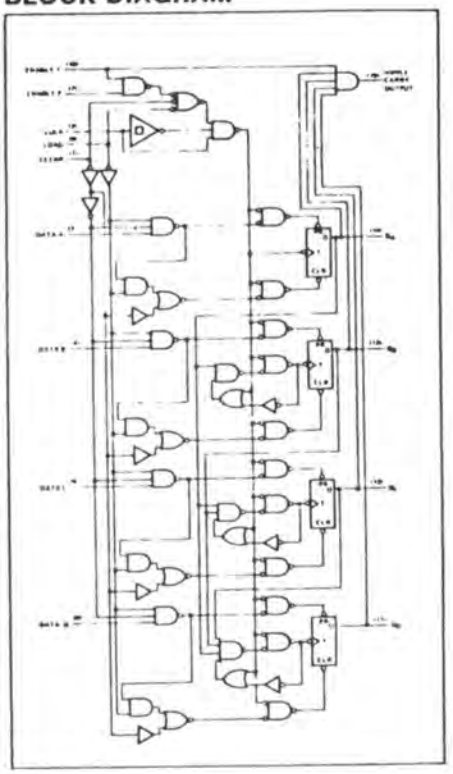
## DESCRIPTION

This synchronous presettable y counter features an internal carry - ahead for applications in high-speed t- ing designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

## PIN CONFIGURATION




## BLOCK DIAGRAM



This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the $Q_A$ output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS161 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER* | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | LIMITS MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{Clock}$ | | | | | 25 | 32 | | MHz |
| $t_{w\ (Clock)}$ | Width of clock pulse | | | | 25 | | | ns |
| $t_{w\ (Clear)}$ | Width of clear pulse | | | | 20 | | | ns |
| $t_{Setup}$ | Input setup time | A,B,C,D | Q | $C_L$ = 15pF, | 0↑ | | | |
| | | Enable P or T | Q | $R_L$ = 2kΩ, | 20↑ | | | |
| | | Load | Q | | 20↑ | | | ns |
| | | | | See Figures | 25↑[2] | | | ns |
| $t_{Hold}$ | Input hold time | A,B,C,D | | 1 and 2 and | 10↑[2] | | | ns |
| | | Others | | Notes 1 and 2 | | 23 | 35 | ns |
| $t_{PLH}$ | | | Ripple | | | 23 | 35 | |
| $t_{PHL}$ | | Clock | carry | | | | | |
| $t_{PLH}$ | | Clock | Any | | | 16 | 24 | ns |
| $t_{PHL}$ | | (load input high) | Q | | | 18 | 27 | |
| $t_{PLH}$ | | Clock | Any | | | 17 | 25 | ns |
| $t_{PHL}$ | | (load input low) | Q | | | 19 | 29 | |
| $t_{PLH}$ | | Enable T | Ripple carry | | | 15 | 23 | ns |
| $t_{PHL}$ | | | | | | 15 | 23 | |
| $t_{PHL}$ | | Clear | Any Q | | | 26 | 38 | ns |

* $f_{max}$ - Maximum clock frequency
$t_{PLH}$ - propagation delay time, low-to high-level output
$t_{PHL}$ - propagation delay time, high-to-low level output

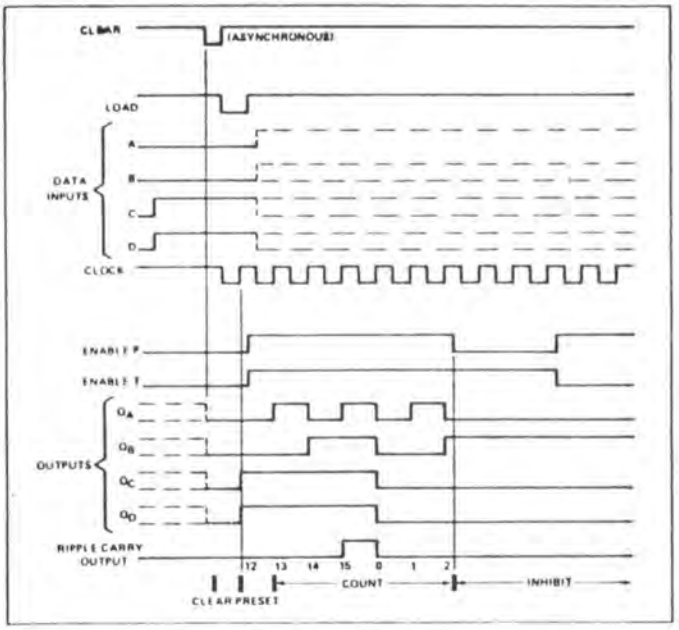
NOTES:
1. Propagation delay for clearing is measured from the clear input.
2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V to 2.0V, whichever is longer.

## PARAMETER MEASUREMENT INFORMATION

### TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit




NOTES

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, Duty Cycle ≤ 50%, $Z_{out}$ ≈ 50Ω, $t_r$ ≤ 15ns, $t_f$ ≤ 6ns.

B. Outputs $Q_D$ and carry are tested at $t_{n+16}$, where $t_n$ is the bit time when all outputs are low.

C. $V_{ref}$ = 1.3V

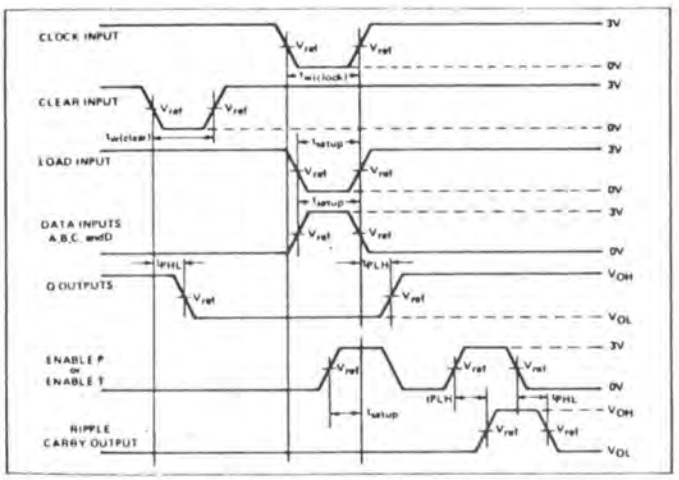



FIGURE 2—VOLTAGE WAVEFORMS

NOTES

A. The input pulses are supplied by generators having the following characteristics: PRR≤ 1MHz, Duty cycle ≤ 50%, $Z_{out}$ ≈ 50Ω, $t_r$ ≤ 15ns, $t_f$ ≤ 6ns.

B. Enable P and T setup times are measured at $t_{n+0}$.

C. $V_{ref}$ = 1.3V.

Load circuit is shown at front of book (totem pole output).

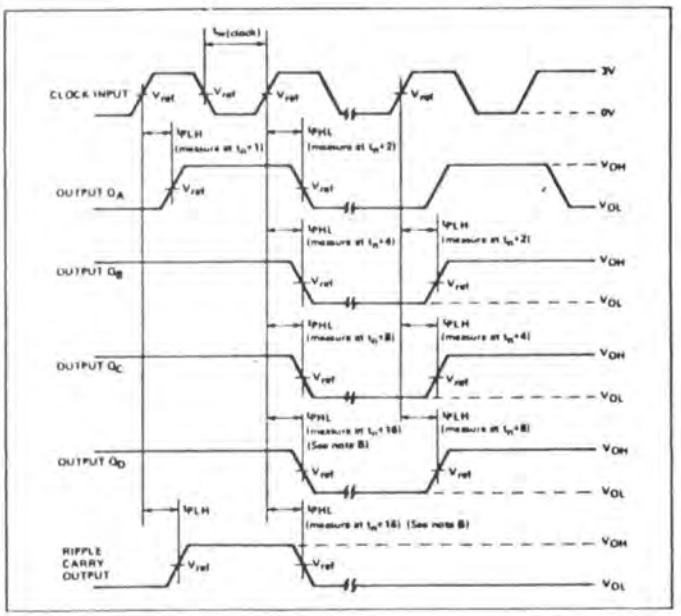
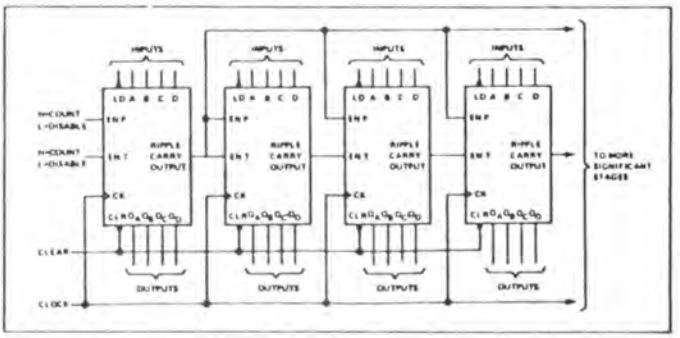



FIGURE 1—VOLTAGE WAVEFORMS

## TYPICAL APPLICATION DATA

### N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS161 will count in binary. Virtually any count mode (modulo-N, $N_1$-to$N_2$, $N_1$-to-maximum) can be used with this fast look-ahead circuit.



# CIRCUIT TYPE TL 430
# PROGRAMMABLE SHUNT REGULATOR

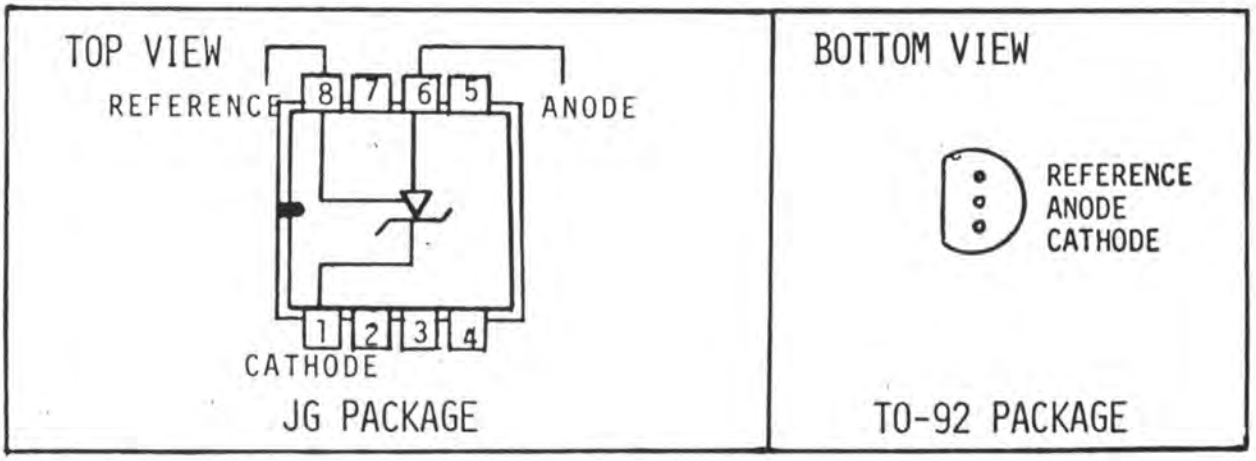
- Temperature Compensated
- Programmable Output Voltage
- Low Output Resistance
- Low Output Noise
- Sink Capability To 100 mA

## DESCRIPTION

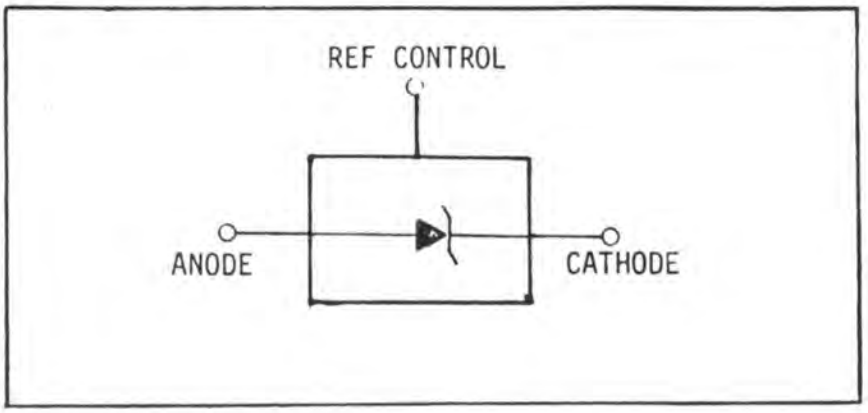
The TL430 is a three terminal "Programmable" shunt regulator featuring excellent stability over temperature, wide operating current range, and low output noise. The output voltage may be set, by two external resistors, to any desired value between 3.0 volts and 30 volts.

The TL430 can replace zener diodes in many applications providing improved performance.

## TERMINAL ASSIGNMENTS




## FUNCTIONAL BLOCK DIAGRAM



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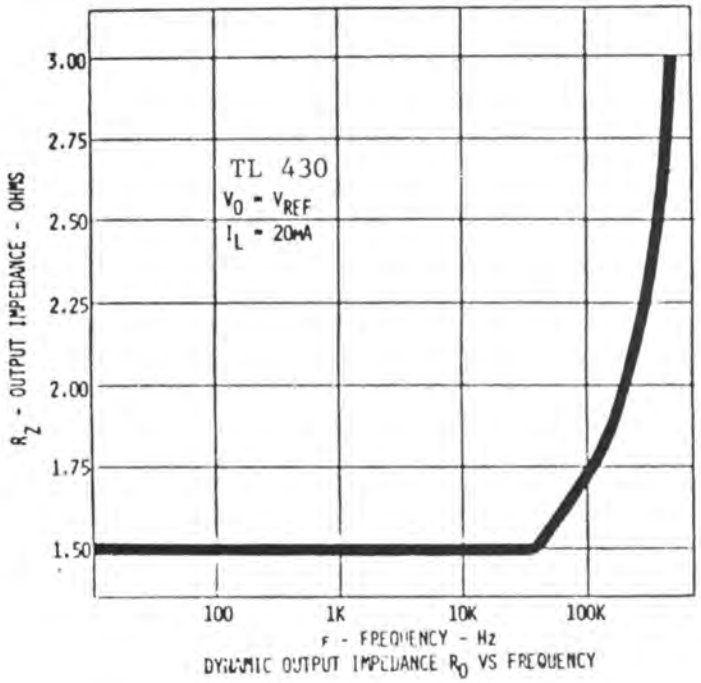
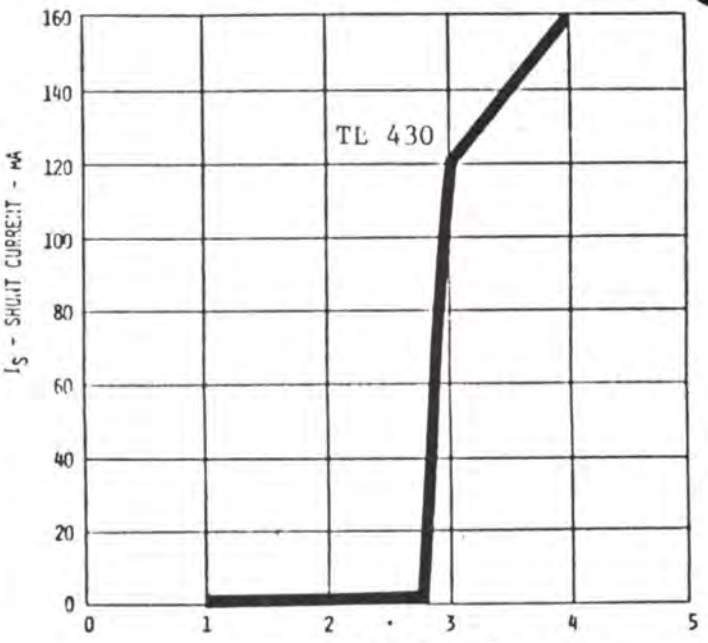


DYNAMIC OUTPUT IMPEDANCE $R_O$ VS FREQUENCY



SHUNT CURRENT VS OUTPUT VOLTAGE

## DEFINITION OF TERMS

$V_{REF}$ REFERENCE VOLTAGE: The voltage at the reference input terminal with respect to the anode terminal.

$I_R$ REFERENCE INPUT CURRENT: Current required into the reference input, during an on condition, to insure output regulation.

$R_{OUT}$ OUTPUT RESISTANCE: The on resistance from the cathode to anode when $V_O = V_{REF}$. The output resistance, $R_O$, for $V_O > V_{REF}$ is given by the equation:

$$R_O = 1 + \frac{R_1}{R_2} R_{OUT}$$

$I_S$ SHUNT CURRENT: Minimum cathode to anode current the device can sink and maintain output regulation.

$I_B$ BIAS CURRENT: The shunt current required to insure output regulation.

## ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

| | |
|---|---|
| Peak Operating Voltage | 30V |
| Peak Shunt Current | 100mA |
| Free-Air Power Dissipation | 775mW |
| Storage Temperature Range | -65°C to 150°C |
| Operating Free-Air Temperature | 0°C to 70°C |

## RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNITS |
|---|---|---|---|
| Output Voltage | $V_{REF}$ | 30 | V |
| Output Current | $I_B$ | 100 | mA |

## ELECTRICAL CHARACTERISTICS AT 25°C UNLESS OTHERWISE NOTED

| PARAMETER | TEST FIG | TEST CONDITIONS | TL 430 MIN | TL 430 TYP | TL 430 MAX | UNIT |
|---|---|---|---|---|---|---|
| Reference Voltage | 1 | $V_O = V_{REF}$, $I_S$ = 10mA | 2.5 | 2.75 | 3.0 | V |
| Temperature Coefficient of Input Reference $\left(\frac{\Delta V_{REF}}{V_{REF}\,\Delta t}\right)$ | 1 | $V_O = V_{REF}$, $I_S$ = 10mA, $0°C<T_A<70°C$ | | ±50 | | ppm/°C |
| Voltage Reference Input Current, $I_R=\frac{V_O-V_{REF}}{R_1}$ | 2 | $R_1$ = 10KΩ, $R_2$ = ∞, $I_S$ = 10mA | | 3 | 10 | μA |
| Output Resistance, $R_{OUT}$ $R_{OUT} = \Delta V_O/\Delta I_S$ | 1 | $V_O = V_{REF}$, $\Delta I_S$=(52-2)mA=50mA | | 1.5 | 3 | Ω |
| Bias Current ($I_B$) | 1 | See Note 1 | | 0.6 | 2 | mA |
| Shunt Current $I_S$ | 1 | $V_{OUT} = V_{REF}$ | 50 | | | mA |
| | | $5V<V_O<30V$, $P_D$ < 775mW | 100 | | | mA |
| Noise "0.1 to 10 Hz" | 2 | $V_O$ = 3V | | 50 | | μV |
| | | $V_O$ = 12V | | 200 | | μV |
| | | $V_O$=30V | | 650 | | μV |

NOTE 1: Min. required for regulation

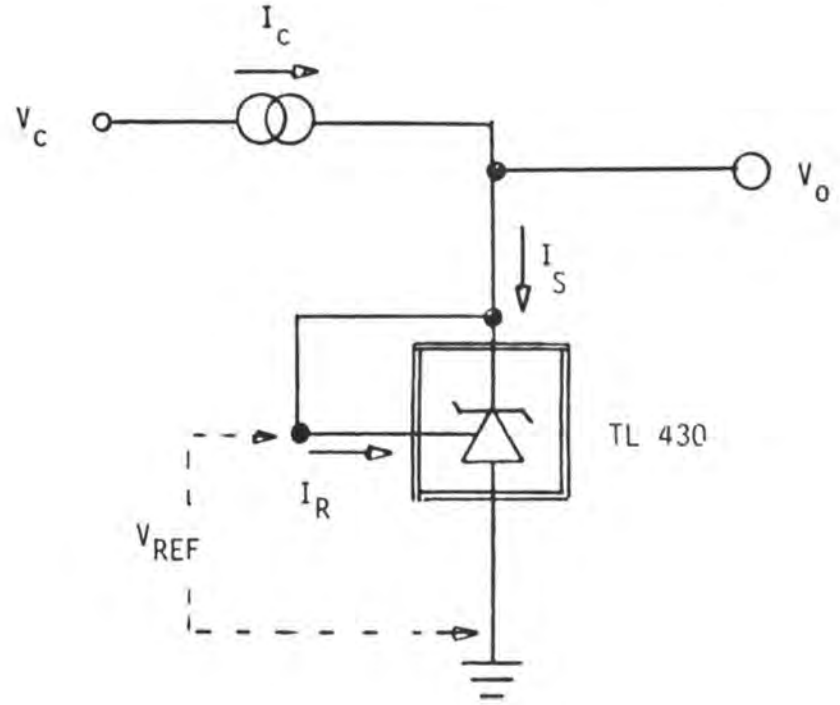



FIGURE 1. $V_O = V_{REF}$ TEST CIRCUIT

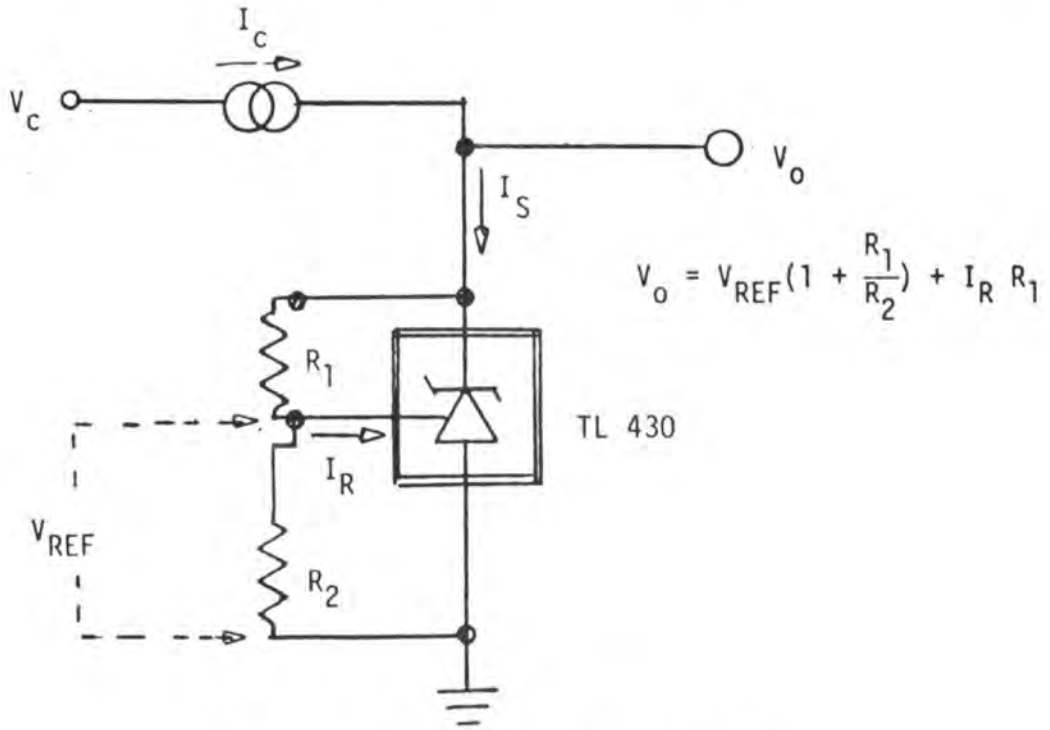



FIGURE 2. $V_O > V_{REF}$ TEST CIRCUIT



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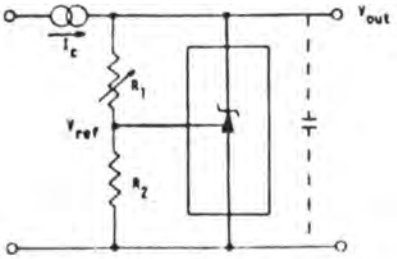
## TYPICAL APPLICATIONS




NOTE: A. $V_{out} = (1 + \frac{R_1}{R_2}) V_{ref}$

FIGURE 3 - SHUNT REGULATOR

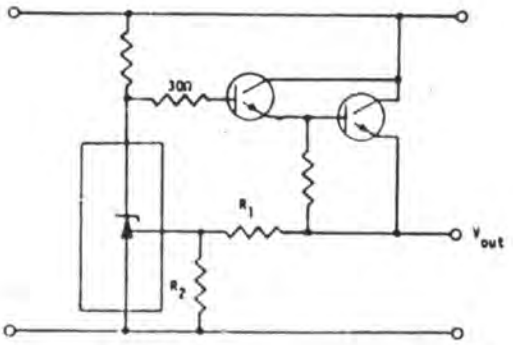
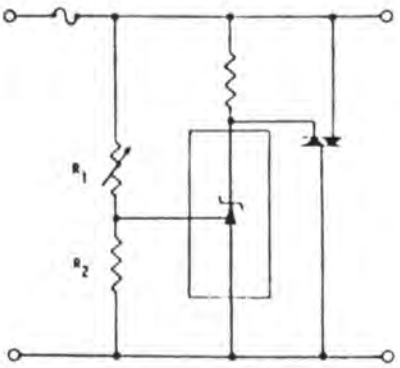



FIGURE 4 - SERIES REGULATOR




NOTE: A. $V_{out\ max} = (1 + \frac{R_1}{R_2}) V_{ref}$

FIGURE 5 - CROW BAR

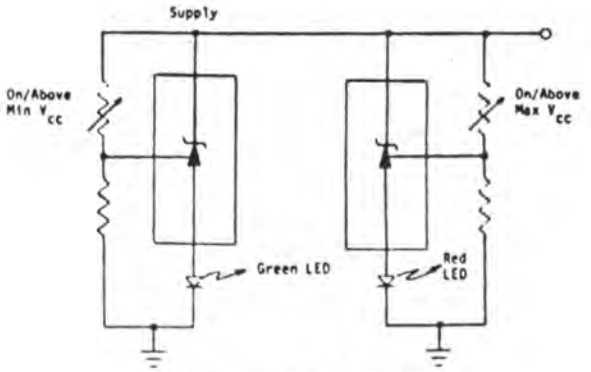
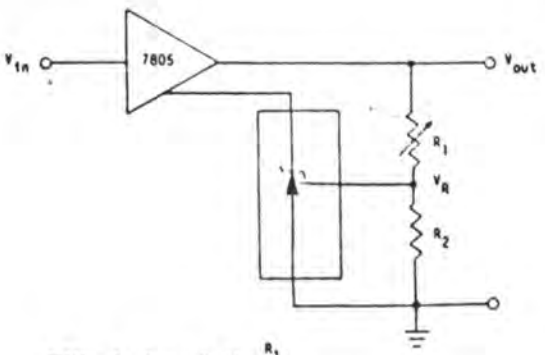



FIGURE 6 - SUPPLY MIN/MAX DETECTOR




NOTES: A. $V_{out} = V_R (1 + \frac{R_1}{R_2})$

B. $V_{out\ (min)} = V_R + 5V$

FIGURE 7 - CONTROL OUTPUT VOLTAGE OF FIXED V.R.

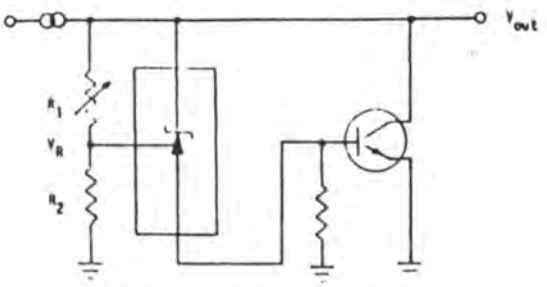



FIGURE 8 - HIGHER CURRENT APPLICATIONS



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PHASE-FREQUENCY DETECTOR

# MC4344 • MC4044

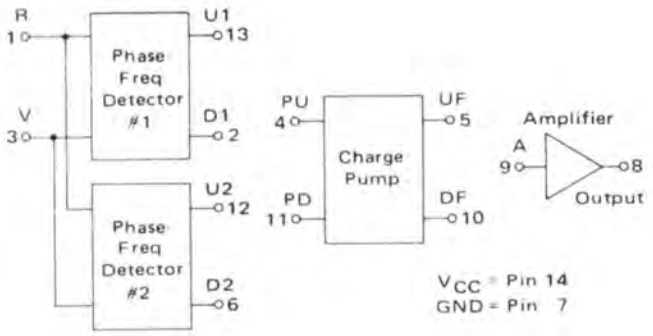
ISSUE A

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts MTTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

F SUFFIX
CERAMIC PACKAGE
CASE 607

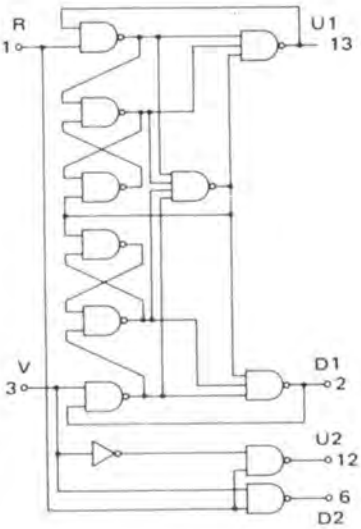
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only

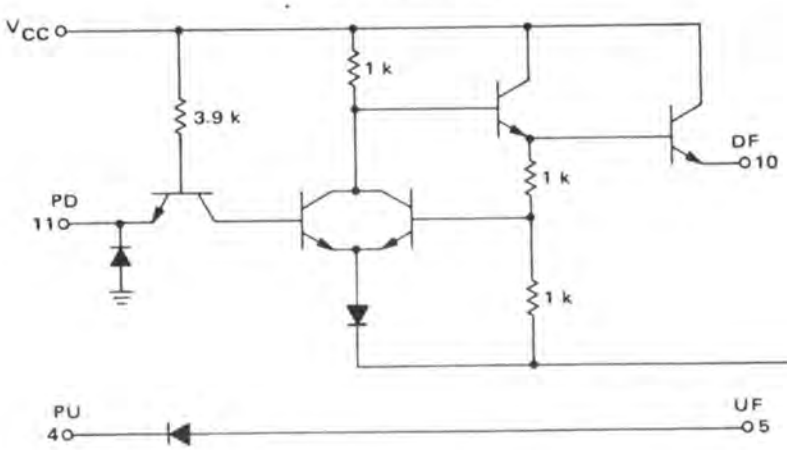



Input Loading Factor. R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

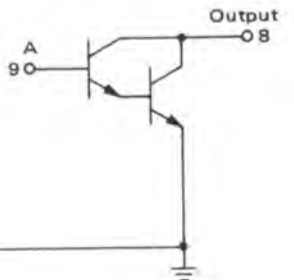
PHASE DETECTOR




CHARGE PUMP




AMPLIFIER



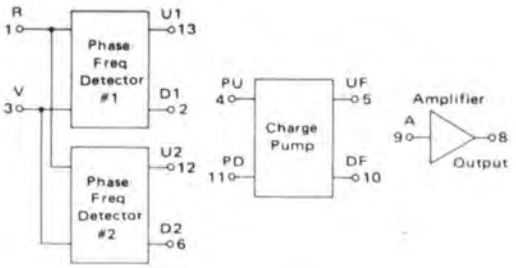
| INPUT STATE | INPUT RI | INPUT VI | OUTPUT U1 | OUTPUT D1 | OUTPUT U2 | OUTPUT D2 |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | X | X | 1 | 1 |
| 2 | 1 | 0 | X | X | 0 | 1 |
| 3 | 1 | 1 | X | X | 1 | 0 |
| 4 | 1 | 0 | X | X | 0 | 1 |
| 5 | 0 | 0 | X | X | 1 | 1 |
| 6 | 1 | 0 | X | X | 0 | 1 |
| 7 | 0 | 0 | X | X | 1 | 1 |
| 8 | 1 | 0 | X | X | 0 | 1 |
| 9 | 0 | 0 | 0 | 1 | 1 | 1 |
| 10 | 0 | 1 | 0 | 1 | 1 | 1 |
| 11 | 0 | 0 | 1 | 1 | 1 | 1 |
| 12 | 0 | 1 | 1 | 1 | 1 | 1 |
| 13 | 0 | 0 | 1 | 0 | 1 | 1 |
| 14 | 0 | 1 | 1 | 0 | 1 | 1 |
| 15 | 0 | 0 | 1 | 0 | 1 | 1 |
| 16 | 1 | 0 | 1 | 0 | 0 | 1 |
| 17 | 0 | 0 | 1 | 1 | 1 | 1 |

**TRUTH TABLE**

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

## ELECTRICAL CHARACTERISTICS




| | Test Temperature | TEST CURRENT/VOLTAGE VALUES mA $I_{OL}$ | $I_{OH1}$ | $I_{OH2}$ | $I_{in}$ | $I_{IC}$ | $I_A$ | Volts $V_{IL}$ | $V_{IH}$ | $V_{IHH}$ | $V_{ILT}$ | $V_{IHT}$ | $V_{out}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MC4344 | -55°C | 20 | -1.6 | -1.0 | | | 0.002 | 0.4 | 2.4 | | 1.1 | 2.0 | 1.5 | 5.0 | 4.5 | 5.5 |
| MC4344 | +25°C | 20 | -1.6 | -1.0 | 1.0 | -10 | 0.002 | 0.4 | 2.4 | 5.5 | 1.1 | 1.8 | 1.5 | 5.0 | 4.5 | 5.5 |
| MC4344 | +125°C | 20 | -1.6 | -1.0 | | | 0.002 | 0.4 | 2.4 | | 0.9 | 1.8 | 1.5 | 5.0 | 4.5 | 5.5 |
| MC4044 | 0°C | 20 | -1.6 | -1.0 | | | 0.002 | 0.4 | 2.5 | | 1.1 | 2.0 | 1.5 | 5.0 | 4.75 | 5.25 |
| MC4044 | +25°C | 20 | -1.6 | -1.0 | 1.0 | -10 | 0.002 | 0.4 | 2.5 | 5.5 | 1.1 | 1.8 | 1.5 | 5.0 | 4.75 | 5.25 |
| MC4044 | +75°C | 20 | -1.6 | -1.0 | | | 0.002 | 0.4 | 2.5 | | 0.9 | 1.8 | 1.5 | 5.0 | 4.75 | 5.25 |

| Characteristic | Symbol | Pin Under Test | MC4344 Test Limits -55°C Min | -55°C Max | +25°C Min | +25°C Max | +125°C Min | +125°C Max | MC4044 Test Limits 0°C Min | 0°C Max | +25°C Min | +25°C Max | +75°C Min | +75°C Max | Unit | TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW $I_{OL}$ | $I_{OH1}$ | $I_{OH2}$ | $I_{in}$ | $I_{IC}$ | $I_A$ | $V_{IL}$ | $V_{IH}$ | $V_{IHH}$ | $V_{ILT}$ | $V_{IHT}$ | $V_{out}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | Pulse 1 | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Forward Current | $I_{IL}$ | 1 | | -4.8 | | -4.8 | | -4.8 | | -4.8 | | -4.8 | | -4.8 | mAdc | | | | | | | 1 | | | | | | | | 14 | | 7 |
| | | 3 | | -4.8 | | -4.8 | | -4.8 | | -4.8 | | -4.8 | | -4.8 | | | | | | | | 3 | | | | | | | | | | |
| | | 11 | | -1.6 | | -1.6 | | -1.6 | | -1.6 | | -1.6 | | -1.6 | | | | | | | | 11 | | | | | | | | | | |
| Leakage Current | $I_{IH}$ | 1 | | 120 | | 120 | | 120 | | 120 | | 120 | | 120 | μAdc | | | | | | | | 1 | | | | | | | 14 | | 7 |
| | | 3 | | 120 | | 120 | | 120 | | 120 | | 120 | | 120 | | | | | | | | | 3 | | | | | | | 14 | | 7 |
| | | 4 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | | | | | | | | | | | | | | | 4 | | 5,7 |
| | | 11 | | 40 | | 40 | | 40 | | 40 | | 40 | | 40 | | | | | | | | | 11 | | | | | | | 14 | | 7 |
| | $I_{IHH}$ | 1 | | | 1.0 | | | | | | 1.0 | | | | mAdc | | | | | | | | | 1 | | | | | | 14 | | 7 |
| | | 3 | | | | | | | | | | | | | | | | | | | | | | 3 | | | | | | | | |
| | | 11 | | | | | | | | | | | | | | | | | | | | | | 11 | | | | | | | | |
| Clamp Voltage | $V_{IC}$ | 1 | | | | -1.5 | | | | | | -1.5 | | | Vdc | | | | | 1 | | | | | | | | | 14 | | | 7 |
| | | 1 | | | | -1.5 | | | | | | -1.5 | | | Vdc | | | | | 3 | | | | | | | | | 14 | | | 7 |
| Output (Note 1) Output Voltage | $V_{OH}$ | 6 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 6 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | | 12 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 12 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | | .. | | | | | | | | | | | | | | | | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | $V_{OL}$ | 6 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | Vdc | 6 | | | | | | | | | | 1.3 | | | 14 | | | 7 |
| | $V_{OH}$ | 12 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 12 | | | | | | | | | 1.3 | | | 14 | | | 7 |
| | | .. | | | | | | | | | | | | | Vdc | | | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | | .. | | | | | | | | | | | | | Vdc | | | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | $V_{OH}$ | 6 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 6 | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | $V_{OL}$ | 12 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | Vdc | 12 | | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | | .. | | | | | | | | | | | | | | | | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | | .. | | | | | | | | | | | | | | | | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | $V_{OH}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 7 | | | | | | | | 1.3 | | | | 11 | | | 7 |
| | $V_{OL}$ | 13 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | Vdc | 13 | | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | $V_{OH}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | | | | | | | | | 1 | 3 | | | 14 | | | 7 |
| | $V_{OL}$ | 13 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | Vdc | 13 | | | | | | | | | 1 | 3 | | | 14 | | | 7 |
| | $V_{OH}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 2 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | | 13 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 13 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | $V_{OH}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 2 | | | | | | | | 1 | 3 | | | 14 | | | 7 |
| | | 13 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 13 | | | | | | | | 1 | 3 | | | 14 | | | 7 |
| | $V_{OL}$ | 2 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | Vdc | 2 | | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | $V_{OH}$ | 13 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 13 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | $V_{OL}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | 2 | | | | | | | | | 1 | 3 | | | 14 | | | 7 |
| | $V_{OH}$ | 13 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 13 | | | | | | | | 1 | 3 | | | 14 | | | 7 |
| | $V_{OL}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | 2 | | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | $V_{OH}$ | 13 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 13 | | | | | | | | 3 | 1 | | | 14 | | | 7 |
| | $V_{OH}$ | 2 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 2 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| | | 13 | 2.4 | | 2.4 | | 2.4 | | 2.5 | | 2.5 | | 2.5 | | Vdc | | 13 | | | | | | | | 1.3 | | | | 14 | | | 7 |
| Short Circuit Current | $I_{OS}$ | 2 | -2.0 | -6.5 | -2.0 | -6.5 | -2.0 | -6.5 | -2.0 | -6.5 | -2.0 | -6.5 | -2.0 | -6.5 | mAdc | | | | | | | | | | | 1 | | | | | 14 | 2,3,7 |
| | | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | 14 | | | | 1,3,6,7 |
| | | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1,3,7,12 |
| | | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 3,7,13 |
| Leakage Current | $I_{OLK}$ | 2 | | 2.5.0 | | 2.5.0 | | 2.5.0 | | 2.5.0 | | 2.5.0 | | 2.5.0 | μAdc | | | | | | | | | | | 1 | | 2.14 | | | | 3,7 |
| | | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | 6,14 | | | | 1,3,7 |
| | | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | 12,14 | | | | 1,3,7 |
| | | 13 | | | | | | | | | | | | | | | | | | | | | | | | 1 | | 13,14 | | | | 3,7 |
| Collector Emitter Voltage | $V_{CE}$ | 5 | | | | 0.5 | | | | | | 0.5 | | | Vdc | | | | 5 | | | | | | | | | | | | | 4,7 |
| Output Voltage | $V_{EH}$ | 10 | 1.5 | | 1.5 | | 1.5 | | 1.5 | | 1.5 | | 1.5 | | Vdc | | | 10 | | | | | | | 11 | | | | 14 | | | 7 |
| Output Current | $I_O$ | 8 | 0.2 | | 0.8 | | 1.0 | | 0.5 | | 0.8 | | 1.0 | | mAdc | | | | | 9 | | | | | | | | | | 8 | | |
| Leakage Current | $I_{OLK}$ | 8 | | 120 | | 120 | | 120 | | 120 | | 120 | | 120 | μAdc | | | | | | | | 11 | | | | | 10 | | | 8 | | 7,9 |
| | | 10 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | μAdc | | | | | | | | | | | | | | | | 14 | | 7 |
| **Power Requirements (Total Device)** Power Supply Drain | $I_{CC}$ | 14 | | 40 | | 40 | | 40 | | 40 | | 40 | | 40 | mAdc | | | | | | | | | | | | | | 14 | | | | 7 |

**Note 1.** The outputs of the device must be tested by sequencing through the indicated input states according to the truth table and functional diagram. All input, power supply, and ground voltages must be maintained between tests unless otherwise noted. Procedures identified by a double asterisk (**) in the Symbol column are necessary to change the state of the sequential logic.

Pulse 1 $V_{CCL}$ — $V_{CC}$ Used to change power supply voltage from previous test.

## MAXIMUM RATINGS

| Rating | | Value | Unit |
|---|---|---|---|
| Supply Operating Voltage Range | MC4344<br>MC4044 | 4.5 to 5.5<br>4.75 to 5.25 | Vdc |
| Supply Voltage | | +7.0 | Vdc |
| Input Voltage | | +5.5 | Vdc |
| Output Voltage | | +5.5 | Vdc |
| Operating Temperature Range | MC4344<br>MC4044 | -55 to +125<br>0 to +75 | °C |
| Storage Temperature Range — Ceramic Package<br>Plastic Package | | -65 to +150<br>-55 to +125 | °C |
| Maximum Junction Temperature | MC4344<br>MC4044 | +175<br>+150 | °C |
| Thermal Resistance – Junction To Case ($\theta_{JC}$)<br>Flat Ceramic Package<br>Dual In-Line Ceramic Package<br>Plastic Package | | <br>0.06<br>0.05<br>0.07 | °C/mW |
| Thermal Resistance – Junction To Ambient ($\theta_{JA}$)<br>Flat Ceramic Package<br>Dual In-Line Ceramic Package<br>Plastic Package | | <br>0.21<br>0.15<br>0.15 | °C/mW |

## CONTENTS

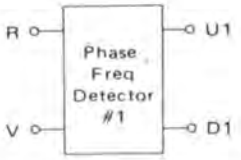


## OPERATING CHARACTERISTICS

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

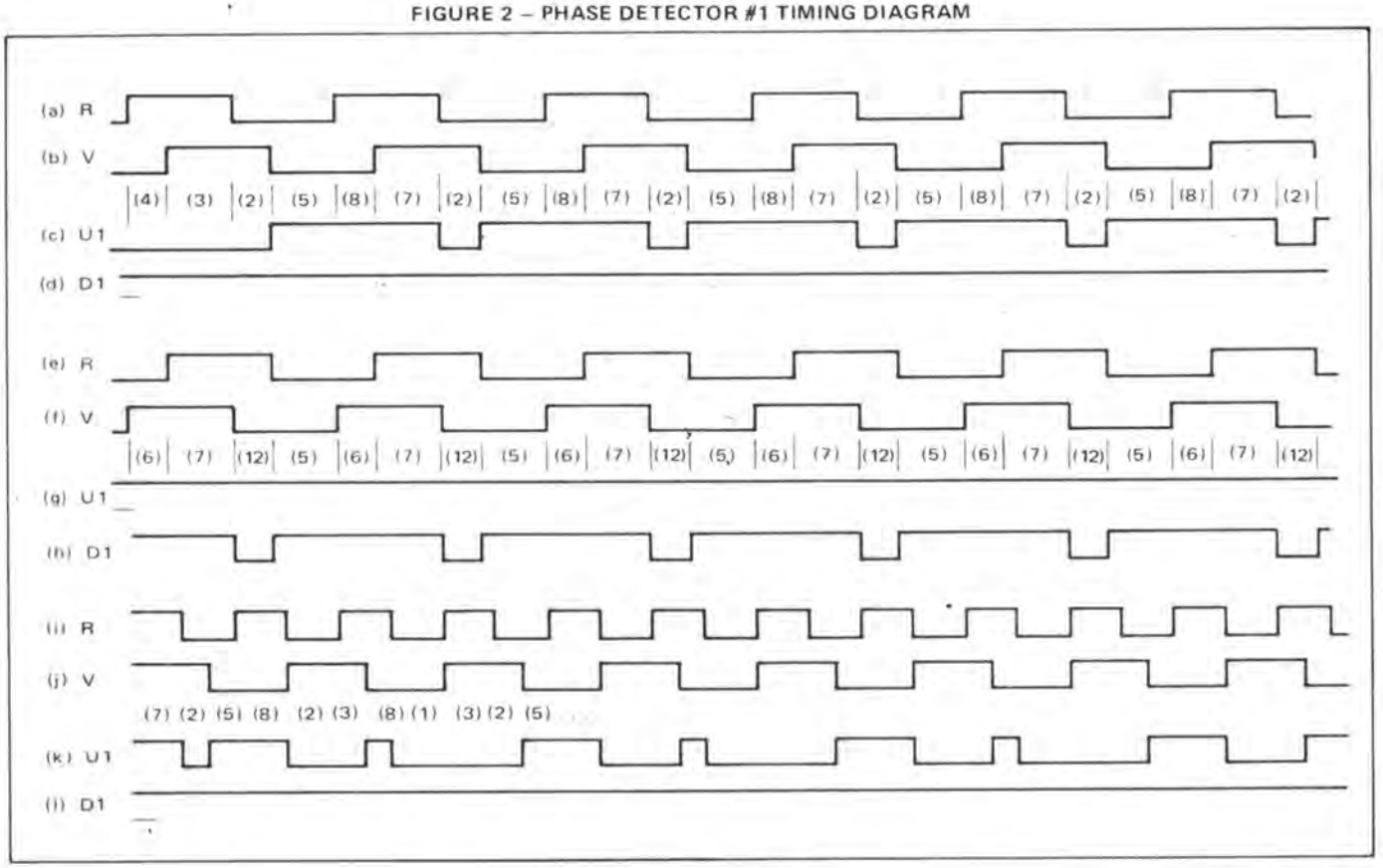
When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that

**FIGURE 1 – PHASE DETECTOR #1 FLOW TABLE**




| R-V 0-0 | R-V 0-1 | R-V 1-1 | R-V 1-0 | U1 | D1 |
|---|---|---|---|---|---|
| (1) | 2 | 3 | (4) | 0 | 1 |
| 5 | (2) | (3) | 8 | 0 | 1 |
| (5) | 6 | 7 | 8 | 1 | 1 |
| 9 | (6) | 7 | 12 | 1 | 1 |
| 5 | 2 | (7) | 12 | 1 | 1 |
| 1 | 2 | 7 | (8) | 1 | 1 |
| (9) | (10) | 11 | 12 | 1 | 0 |
| 5 | 6 | (11) | (12) | 1 | 0 |

FIGURE 2 – PHASE DETECTOR #1 TIMING DIAGRAM




location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

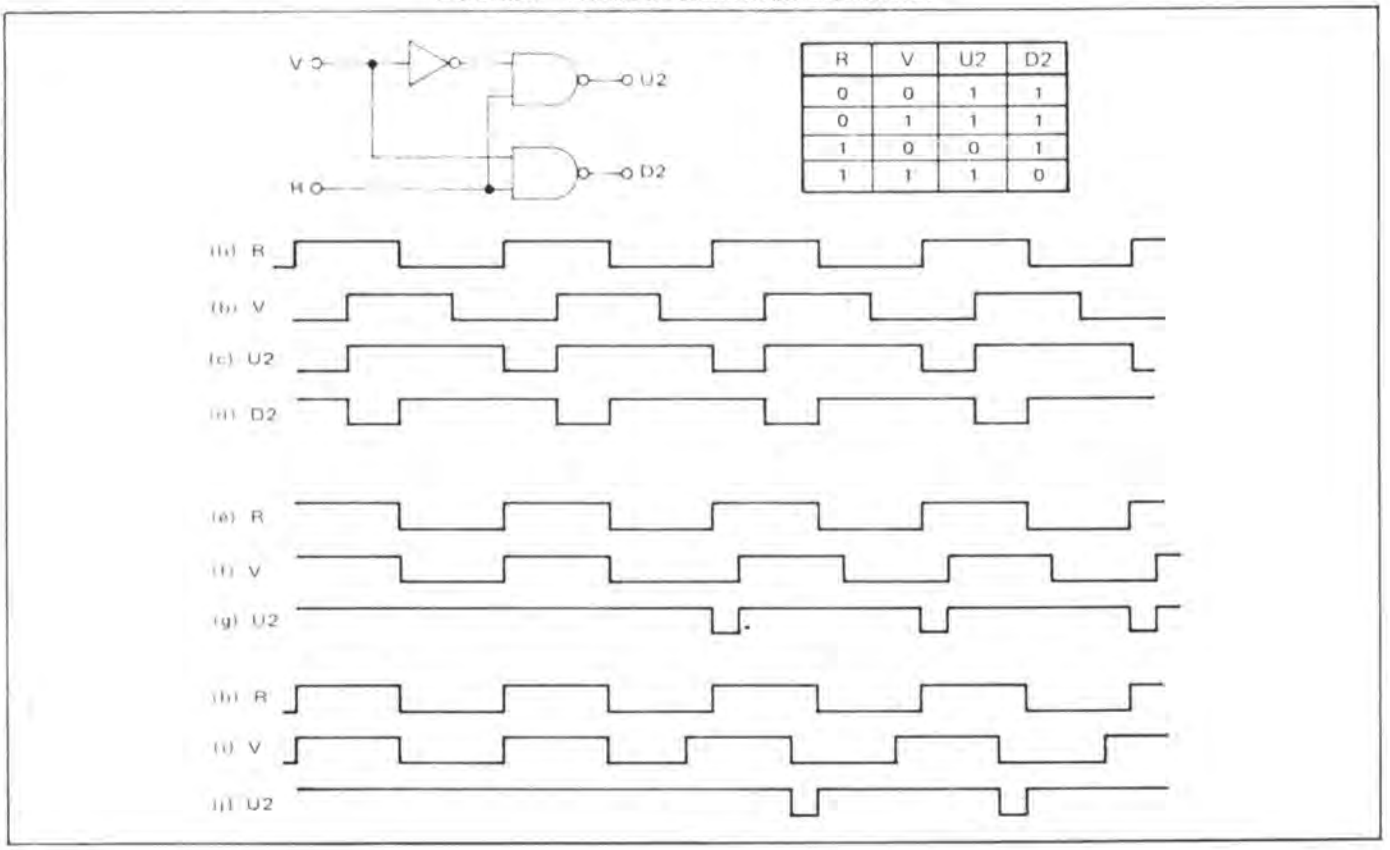
Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" and "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc. as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e-h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i-l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the

FIGURE 3 – PHASE DETECTOR #2 OPERATION



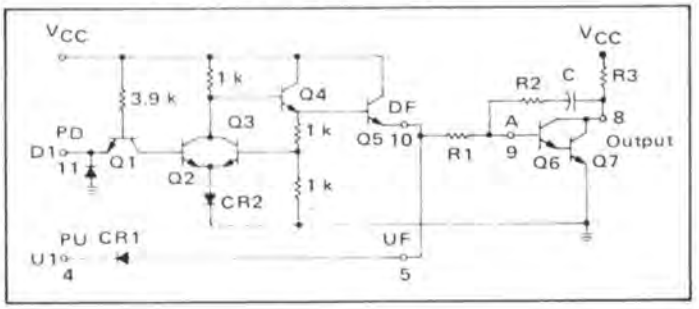

| R | V | U2 | D2 |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a-d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e-j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two $V_{BE}$ drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be

FIGURE 4 – CHARGE PUMP OPERATION



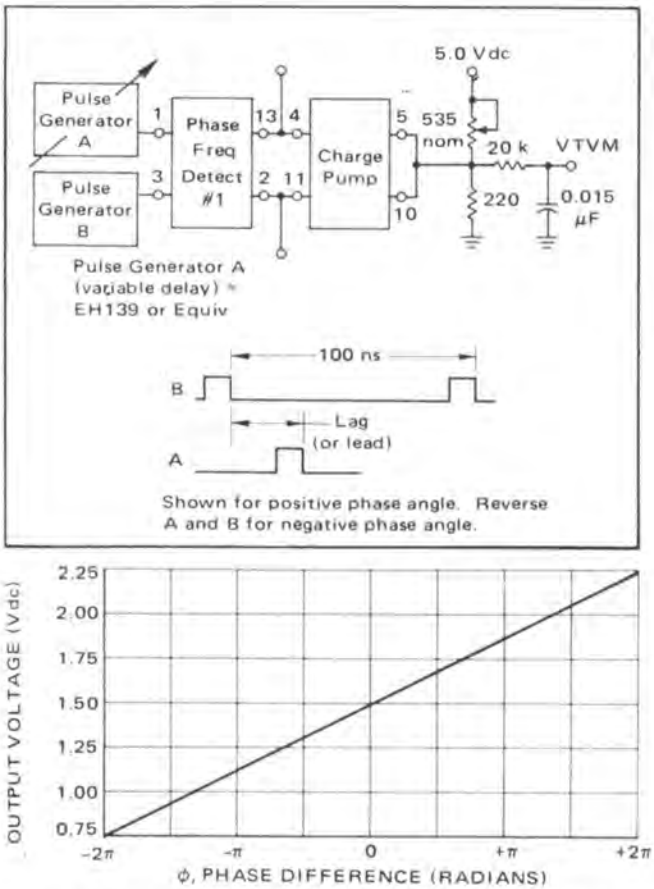

approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be one $V_{BE}$ below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

When PU is low and PD is high, CR1 is forward biased and UF will be approximately one $V_{BE}$ above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the

collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one $V_{BE}$ and three $V_{BE}$ as the phase difference of R and V varies from minus $2\pi$ to plus $2\pi$. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, $K_\phi$, of approximately 0.12 volt/radian is obtained (see Figure 5).

FIGURE 5 – PHASE DETECTOR TEST







The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by $V_{BE}$'s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower $V_{BE}$'s – on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

## PHASE-LOCKED LOOP COMPONENTS

### General

A basic phase-locked loop, when operating properly, will acquire ("lock on") an input signal, track it in frequency, and exhibit a fixed phase relationship relative to the input. In this basic loop, the output frequency will be identical to the input frequency (Figure 6). A fundamental loop consists of a phase detector, amplifier/filter, and voltage-controlled oscillator (Figure 7). It appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between $f_{in}$ and $f_{out}$ is amplified and applied to the VCO in a corrective direction.

FIGURE 6 – BASIC PHASE-LOCKED LOOP FREQUENCY RELATIONSHIP

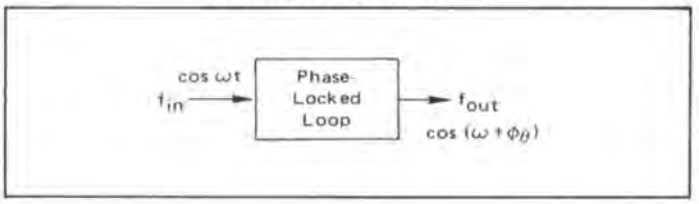
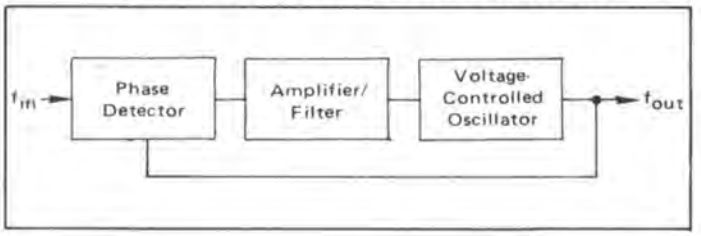



FIGURE 7 – FUNDAMENTAL PHASE-LOCKED LOOP




Simple phase detectors in digital phase-locked loops usually put out a series of pulses. The average value of these pulses is the "gain constant", $K_\phi$, of the phase detector – the volts out for a given phase difference, expressed as volts/radian.

The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The ratio of change in output frequency to input control voltage is called "gain constant", $K_O$. If the slope of $f_{out}$ to $V_{in}$ is not linear (i.e., changes greater than 25%) over the expected frequency range, the

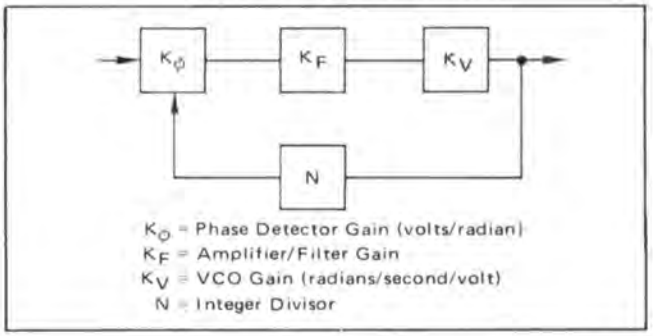
curve should be piece-wise approximated and the appropriate constant applied for "best" and "worst" case analysis of loop performance.

System dynamics when in lock are determined by the amplifier/filter block. Its gain determines how much phase error exists between $f_{in}$ and $f_{out}$, and filter characteristics shape the capture range and transient performance. This will be discussed in detail later.

## Loop Filter

Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block of Figure 8.

**FIGURE 8 – GAIN CONSTANTS**




The output to input ratio reflects a second order low pass filter in frequency response with a static gain of N:

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{K_\phi K_F K_V}{s + \frac{K_\phi K_F K_V}{N}} \quad (1)$$

where:
$$K_F = \frac{1 + T_1 s}{T_2 s} \quad (2)$$

$T_1 = R_2C$ and $T_2 = R_1C$ of Figure 4. Therefore,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2 N T_2}{K_\phi K_V} + T_1 s + 1} \quad (3)$$

Both $\omega_n$ (loop bandwidth or natural frequency) and $\zeta$ (damping factor) are particularly important in the transient response to a step input of phase or frequency (Figure 9), and are defined as:

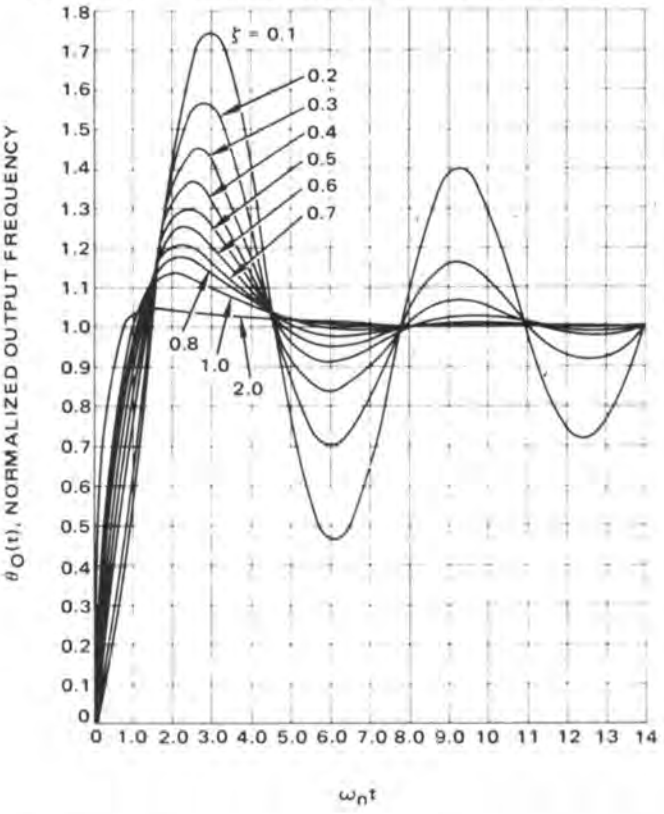
$$\omega_n = \sqrt{\frac{K_\phi K_V}{NT_2}} \quad (4)$$

$$\zeta = \sqrt{\frac{K_\phi K_V}{NT_2}} \left(\frac{T_1}{2}\right) \quad (5)$$

Using these terms in Equation 3,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \quad (6)$$

**FIGURE 9 – TYPE 2 SECOND ORDER STEP RESPONSE**




In a well defined system controlling factors such as $\omega_n$ and $\zeta$ may be chosen either from a transient basis (time domain response) or steady state frequency plot (roll-off point and peaking versus frequency). Once these two design goals are defined, synthesis of the filter is relatively straight-forward.

Constants $K_\phi$, $K_V$, and N are usually fixed due to other design constraints, leaving $T_1$ and $T_2$ as variables to set $\omega_n$ and $\zeta$. Since only $T_2$ appears in Equation 4, it is the easiest to solve for initially.

$$T_2 = \frac{K_\phi K_V}{N\omega_n^2} \quad (7)$$

From Equation 5, we find

$$T_1 = \frac{2\zeta}{\omega_n} \quad (8)$$

Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K_\phi K_V}{N\omega_n^2 C} \quad (9)$$

$$R_2 = \frac{2}{\omega_n C} \quad (10)$$

Although fundamentally the range of $R_1$ and $R_2$ may be from several hundred to several thousand ohms, sideband considerations usually force the value of $R_1$ to be set first, and then $R_2$ and C computed.

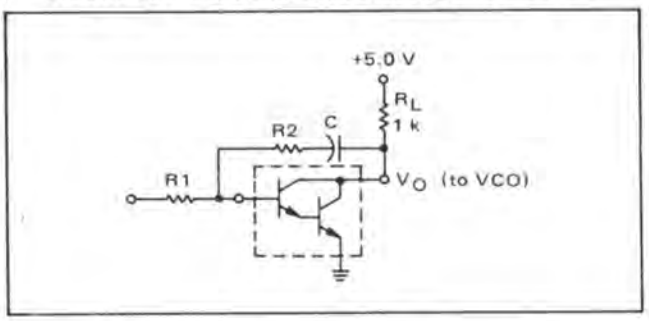
$$C = \frac{K_\phi K_V}{N\omega_n^2 R_1} \qquad (11)$$

Calculation of passive components $R_2$ and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of $\omega_n$ and $\zeta$ during that variance. Equally important are changes in $K_V$ over the output frequency range. Minimum and maximum values of $\omega_n$ and $\zeta$ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between $f_{in}$ and $f_{out}$, and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make $f_{in}$ equal $f_{out}$. Unnecessarily high gains can cause problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the

FIGURE 10 – USING MC4344/4044 LOOP AMPLIFIER




placement of $R_1$, $R_2$, C, and load resistor $R_L$ (1 kΩ). Due to the non-infinite gain of this stage ($A_V \approx 30$) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of $R_2$ and an upper limit on $R_1$. Placed in order of priority, the recommendations are as follows: (a) $R2 > 50\ \Omega$, (b) $R2/R1 \leq 10$, (c) $1\ k\Omega < R1 < 5\ k\Omega$.

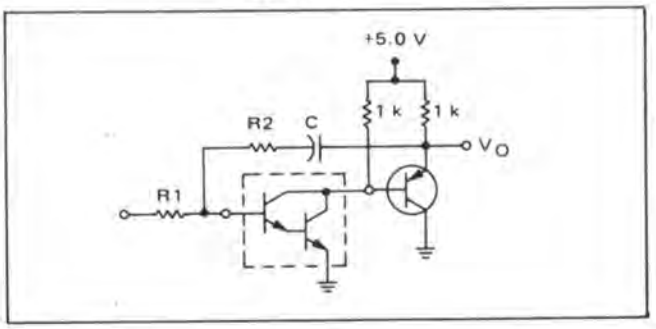
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error ($R_1 > 5\ k\Omega$) or lower phase detector gain ($R_1 < 1\ k\Omega$). If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because $T_1$ in Equation 5 is in reality composed of three elements:

$$T_1 = C\left(R_2 - \frac{1}{g_m}\right) \qquad (12)$$

where $g_m$ = transconductance of the common emitter amplifier.

Normally $g_m$ is large and $T_1$ nearly equals $R_2C$, but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may

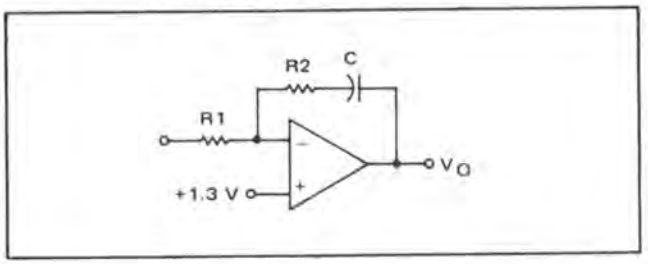
FIGURE 11 – AMPLIFIER CAPABLE OF HANDLING LOWER R2




then be reduced by at least an order of magnitude ($R_2 > 5\ \Omega$) keeping in mind that electrolytic capacitors used as C may approach this value by themselves at the frequency of interest ($\omega_n$).

Larger values of $R_1$ may be accommodated by either using an operational amplifier with a low bias current ($I_b < 1.0\ \mu A$) as shown in Figure 12 or by buffering the internal

FIGURE 12 – USING AN OPERATIONAL AMPLIFIER TO EXTEND THE VALUE OF R1




Darlington pair with an FET (Figure 13). It is vitally important, however, that the added device be operated at zero $V_{GS}$. Source resistor $R_4$ should be adjusted for this condition (which amounts to $I_{DSS}$ current for the FET). This insures that the overall amplifier input threshold remains at the proper potential of approximately two base-emitter drops. Use of an additional emitter follower instead of the FET and $R_4$ (Figure 14) gives a threshold near the upper limit of the phase detector charge pump, resulting in an extremely unsymmetrical phase detector gain in the pump up versus pump down mode. It is not unusual to

FIGURE 13 – FET BUFFERING TO RAISE AMPLIFIER INPUT IMPEDANCE

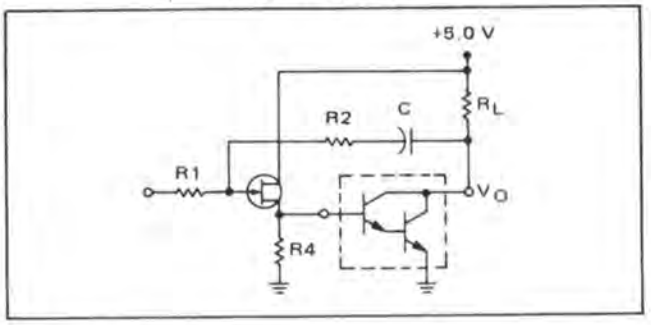
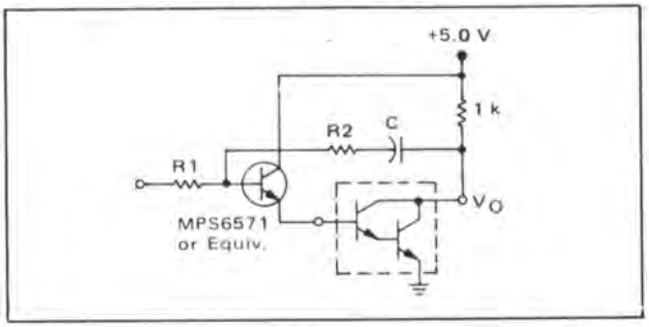



FIGURE 14 – EMITTER FOLLOWER BUFFERING OF AMPLIFIER INPUT




note a 5:1 difference in $K_\phi$ for circuits having the bipolar buffer stage. If the initial design can withstand this variation in loop gain and remain stable, the approach should be considered since there are no critical adjustments as in the FET circuit.

## DESIGN PROBLEMS AND THEIR SOLUTIONS

### Dynamic Range

A source of trouble for all phase-locked loops, as well as most electronics is simply overload or lack of sufficient dynamic range. One limit is the amplifier output drive to the VCO. Not only must a designer note the outside limits of the dc control voltage necessary to give the output frequency range, he must also account for the worst case of overshoot expected for the system. Relatively large damping factors ($\zeta$ = 0.5) can contribute significant amounts of overshoot (30%). To be prepared for the worst case output swing the amplifier should have as much margin to positive and negative limits as the expected swing itself. That is, if a two-volt swing is sufficient to give the desired output frequency excursion, there should be at least a two-volt cushion above and below maximum expected steady-state values on the control line.

This increase in range, in order to be effective, must of course be followed by an equivalent range in the VCO or there is little to be gained. Any loss in loop gain will in general cause a decrease in $\zeta$ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the problem tends to accelerate towards a situation where the system settles in not only a slow but oscillatory manner as well.

Loss of amplifier gain may not be due entirely to normal system damping considerations. In loops employing digital phase detectors, an additional problem is likely to appear. This is due to amplifier saturation during a step input when there is a maximum phase detector output simultaneous with a large transient overshoot. The phase detector square wave rides on top of the normal transient and may even exceed the amplifier output limits imposed above. Since the input frequency will exceed the $R_2C$ time constant, gain $K_F$ for these annoying pulses will be $R_2/R_1$. Ordinarily this ratio will be less than 1, but some circumstances dictate a low loop gain commensurate with a fairly high $\omega_n$. For these cases, $R_2/R_1$ may be higher than 10 and cause pulse-wise saturation of the amplifier. Since the dc control voltage is an average of phase detector pulses, clipping can be translated into a reduction in gain with all the "benefits" already outlined, i.e., poor settling time. An easy remedy to apply in many cases is a simple RC low pass section preceding or together with the integrator-lag section. To make transient suppression independent of amplifier response, the network may be imbedded within the input resistor $R_1$ (Figure 15) or be implemented

FIGURE 15 – IMPROVED TRANSIENT SUPPRESSION WITH R1 – $C_c$

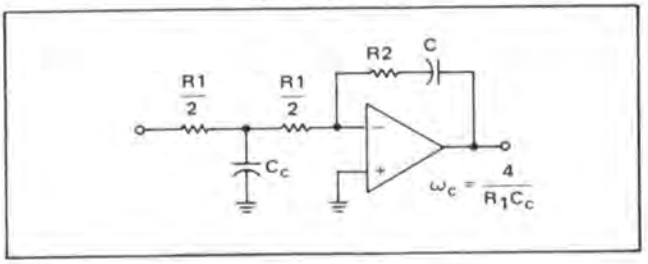
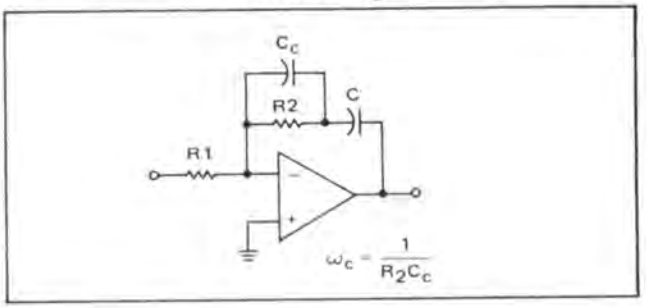



FIGURE 16 – IMPROVED TRANSIENT SUPPRESSION WITH R2 – $C_c$




by placing a feedback capacitor across $R_2$ (Figure 16). Besides rounding off and inhibiting pulses, these networks add an additional pole to the loop and may cause further overshoot if the cutoff frequency ($\omega_c$) is too close to $\omega_n$. If at all possible the cutoff point should be five to ten times $\omega_n$. How far $\omega_c$ can be placed from $\omega_n$ depends on the input frequency relationship to $\omega_n$ since $f_{in}$ is, after all, what is being filtered. A side benefit of this simple RC pulse "flattener" is a reduction in $f_{in}$ sidebands around $f_{out}$ for synthesizers with N > 1. However, a series of RC filters is not recommended for either extended

pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

## Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components – the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals – loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{ref} K_V}{2\omega_{ref}} \qquad (13)$$

where $V_{ref}$ = peak voltage value of spurious freuqency at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where $\omega_{ref}$ is higher than $1/T_2$, the $K_F$ function amounts to a simple resistor ratio:

$$K_F(j\omega)\Big|_{\omega=\omega_{ref}} \cong -\frac{R_2}{R_1} \qquad (14)$$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_F(j\omega)\Big|_{\omega=\omega_{ref}} \cong \frac{2\zeta N\omega_n}{K_\phi K_V} = \frac{V_{ref}}{V_\phi} \qquad (15)$$

where $V_{ref}$ = peak value of reference voltage at the VCO input, and
$V_\phi$ = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{f_{out}\text{ level}} = V_\phi\left(\frac{\zeta N\omega_n}{\omega_{ref}K_\phi}\right) \qquad (16)$$

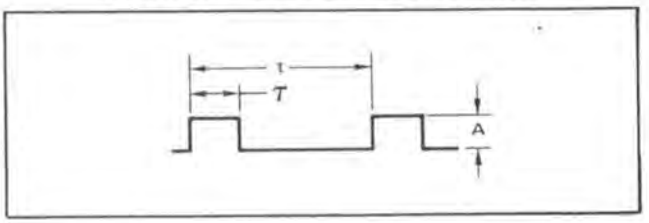
From Equation 16 we find that for a given phase detector, a given value of $R_1$ (which determines $V_\phi$), and given basic system constraints (N, $f_{ref}$), only $\zeta$ and $\omega_n$ remain as variables to diminish the sidebands. If there are few limits on $\omega_n$, it may be lowered indefinitely until the desired degree of suppression is obtained. If $\omega_n$ is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

One item worthy of note is the absence of $K_V$ in Equation 16. From Equation 15 it might be concluded that decreasing $K_V$ would be another means for reducing spurious sidebands, but for constant values of $\zeta$ and $\omega_n$ this is not a free variable. In a given loop, varying $K_V$ will certainly affect sideband voltage, but will also vary $\zeta$ and $\omega_n$.

On the other hand, the choice of $\omega_n$ may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

In computing sideband levels, the value of $V_\phi$ must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves $\tau$ seconds wide repeated at t second intervals (Figure 17). A Fourier analysis can be summarized for small ratios of $\tau/t$ by:

**FIGURE 17 – PHASE DETECTOR OUTPUT**




(1) the average voltage ($V_{avg}$) is $A(\tau/t)$
(2) the peak reference voltage value ($V_\phi$) is twice $V_{avg}$, and
(3) the second harmonic ($2f_{ref}$) is roughly equal in amplitude to the fundamental.

By knowing the requirements for (1) due to amplifier bias and leakage currents, values for (2) and (3) are uniquely determined.

An example of this sideband approximation technique can be illustrated using the parameters specified for the synthesizer design included in the applications information section.

$N_{max} = 30$ $\quad \omega_n = 4500$
$K_V = 11.2 \times 10^6$ rad/s/V $\quad R_1 = 2\ k\Omega$
$K_\phi = 0.12$ V/rad $\quad f_{ref} = 100$ kHz
$\zeta = 0.8$

Substituting these numbers into Equation 16:

$$\frac{\text{sideband}}{f_{out}} = V_\phi \frac{(0.8)(30)(4500)}{2\pi(10^5)(0.111)} \quad (17)$$

$$= V_\phi (1.55) \quad (18)$$

The result illustrates how much reference feedthrough will affect sideband levels. If 1.0 mV peak of reference appears at the output of the phase detector, the nearest sideband will be down 56.2 dB.

If the amplifier section included in the MC4344/4044 is used, with $R_L$ = 1 kΩ, some approximations of the value of $V_\phi$ can be made based on the input bias current and the value of $R_1$. The phase detector must provide sufficient average voltage to supply the amplifier bias current, $I_b$, through $R_1$; when the bias current is about 5.0 μA and $R_1$ is 2 kΩ, $V_{avg}$ must be 10 mV. From the assumptions earlier concerning the Fourier transform, and with the help of Figure 18, we can see that the phase detector duty cycle will be about 1.7% (A = 0.6 V), giving

**FIGURE 18 – OUTPUT ERROR CHARACTERISTICS**

| DUTY CYCLE (%) | PHASE ERROR (Deg) | $V_{avg}$ (mV) | $V_{\phi(peak)}$ (mV) |
|---|---|---|---|
| 0.1 | 0.36 | 0.6 | 1.2 |
| 0.2 | 0.72 | 1.2 | 2.4 |
| 0.3 | 1.08 | 1.8 | 3.6 |
| 0.4 | 1.44 | 2.4 | 4.8 |
| 0.5 | 1.80 | 3.0 | 6.0 |
| 0.6 | 2.16 | 3.6 | 7.2 |
| 0.7 | 2.52 | 4.2 | 8.4 |
| 0.8 | 2.88 | 4.8 | 9.6 |
| 0.9 | 3.24 | 5.4 | 10.8 |
| 1.0 | 3.60 | 6.0 | 12.0 |
| 2.0 | 7.2 | 12.0 | 24.0 |
| 3.0 | 10.8 | 18.0 | 35.9 |
| 4.0 | 14.4 | 24.0 | 47.9 |
| 5.0 | 18.0 | 30.0 | 59.8 |
| 6.0 | 21.6 | 36.0 | 71.6 |
| 7.0 | 25.2 | 42.0 | 83.3 |
| 8.0 | 28.8 | 48.0 | 95.0 |
| 9.0 | 32.4 | 54.0 | 106.6 |
| 10.0 | 36.0 | 60.0 | 118.0 |

a fundamental (reference) of 20 mV peak. If this value for $V_\phi$ is substituted into Equation 18, the resulting sideband ratio represents 30 dB suppression due to this component alone.

For loop amplifiers having very high gains and relatively low bias currents, another factor to consider is reverse leakage current, $I_L$, of the MC4344/4044 charge pump. This is generally less than 1.0 μA although it is no more than 5.0 μA over the temperature range. A typical value for design for room temperature operation is 0.1 μA. To minimize the effects of amplifier bias and leakage currents a relatively small value of $R_1$ should be chosen. A minimum value of 1 kΩ is a good choice.

After values for C and $R_2$ have been computed on the basis of loop dynamic properties, the overall sideband to $f_{out}$ ratio computation can be simplified.

Since

$$V_\phi = 2\,V_{avg}$$
$$V_{avg} = (I_b + I_L)\,R_1$$
$$V_\phi = 2\,(I_b + I_L)\,R_1$$
$$V_{ref} = V_\phi \left(\frac{R_2}{R_1}\right)$$
$$= 2R_1\,(I_b + I_L)\left(\frac{R_2}{R_1}\right) = 2R_2\,(I_b + I_L)$$

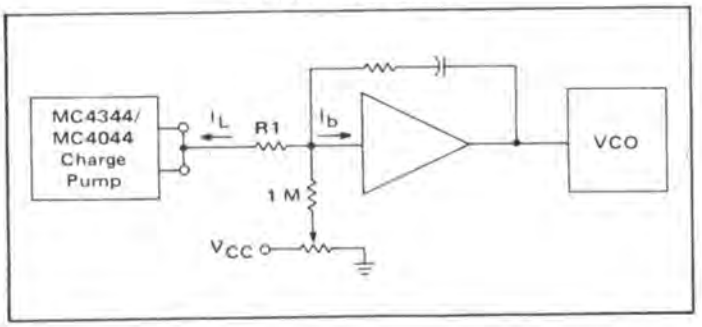
we find that

$$\frac{\text{sideband}}{f_{out}} = \frac{V_{ref} K_V}{2\omega_{ref}} \quad (19)$$

$$\frac{\text{sideband}}{f_{out}} = \frac{2R_2(I_b + I_L)K_V}{2\omega_{ref}} \quad (20)$$

Equation 20 indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input (Figure 19). This

**FIGURE 19 – COMPENSATING FOR BIAS AND LEAKAGE CURRENT**




has indeed proved to be the case. Experimental results indicate that greater than 60 dB rejection can routinely be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

## Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency ($\omega_n$). On one hand, the "corner" should be well below (lower than) $\omega_{ref}$ and yet far removed (above) from $\omega_n$. Although no easy method for placing the rolloff point exists, a rule of thumb that usually works is:

$$\omega_c = 5\omega_n \quad (21)$$

Reference frequency suppression per pole is the ratio of $\omega_c$ to $\omega_{ref}$.

$$SB_{dB} \cong n\ 20 \log_{10} \left( \frac{\omega_c}{\omega_{ref}} \right) \qquad (22)$$

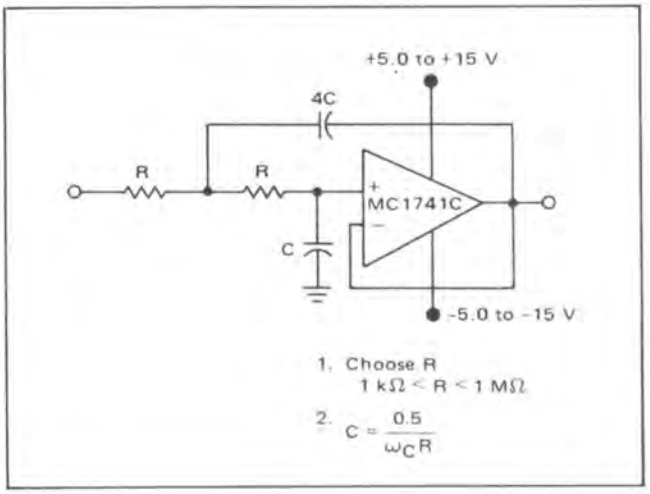
where n is the number of poles in the filter.

Equation 22 gives the additional loop suppression to $\omega_{ref}$; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

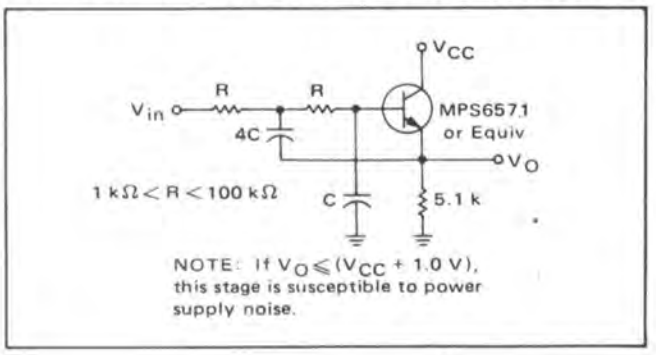
A suitable alternative is an active RC section, Figure 20,

**FIGURE 20 – OPERATIONAL AMPLIFIER LOW PASS FILTER**




compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff ($\omega_c$), without peaking enough to cause any danger of raising the loop gain for frequencies above $\omega_n$. A fairly non-critical section may simply use an emitter follower as the active device with two resistors and capacitors completing the circuit (Figure 21). This provides a -12 dB/octave (-40 dB/decade) rolloff characteristic above $\omega_n$, though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint

**FIGURE 21 – EMITTER FOLLOWER LOW PASS FILTER**

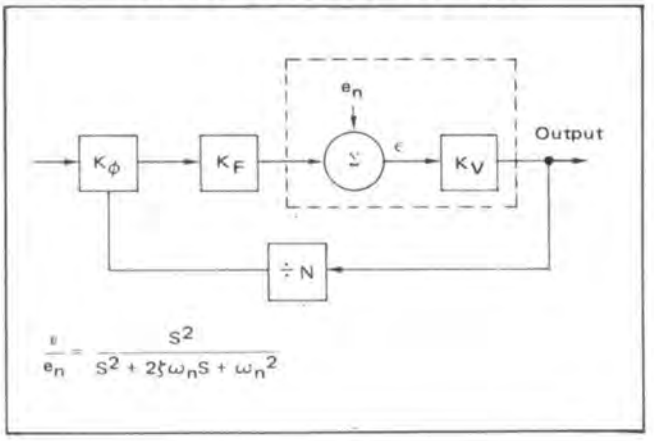



between $\omega_n$ and $\omega_{ref}$ is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

## VCO Noise

Effects of noise within the VCO itself can be evaluated by considering a closed loop situation with an external noise source, $e_n$, introduced at the VCO (Figure 22). Re-

**FIGURE 22 – EFFECTS OF VCO NOISE**




sultant modulation of the VCO by error voltage, $\epsilon$, is a second order high pass function:

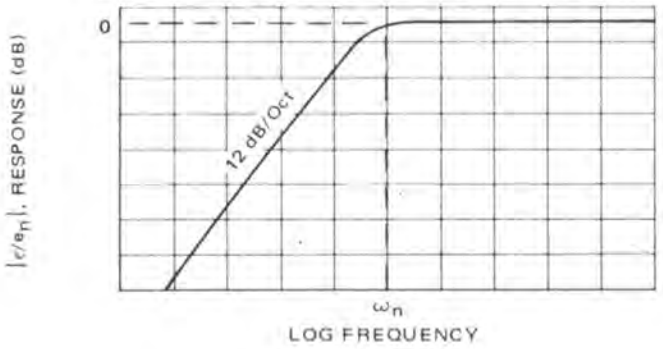
$$\frac{\epsilon}{e_n} = \frac{S^2}{S^2 + \frac{ST_2K_\phi K_V}{T_1N} + \frac{K_\phi K_V}{T_1N}} = \frac{S^2}{S^2 + 2\zeta\omega_n + \omega_n^2} \qquad (23)$$

This function has a slope of 12 dB/octave at frequencies less than $\omega_n$ (loop natural frequency), as shown in Figure 23. This means that noise components in the VCO above $\omega_n$ will pass unattenuated and those below will have some degree of suppression. Therefore choice of loop natural frequency may well rest on VCO noise quality.

## Other Spurious Responses

Spurious components appearing in the output spectrum are seldom due to reference frequency feedthrough alone.

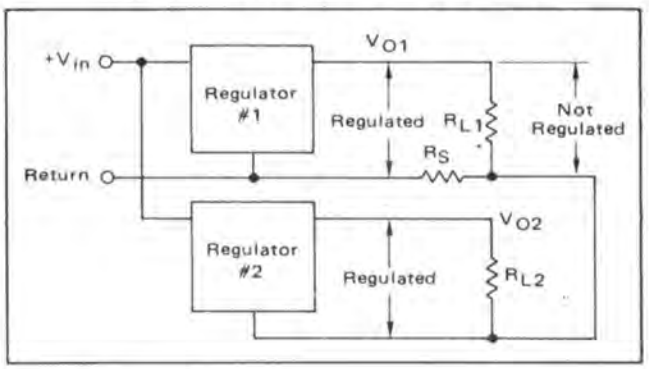
FIGURE 23 – LOOP RESPONSE TO VCO NOISE




Modulation of any kind appearing on the VCO control line will cause spurious sidebands and can come in through the loop amplifier supply, bias circuitry in the control path, a translator, or even the VCO supply itself. Some VCO's have a relatively high sensitivity to power supply variation. This should be investigated and its effects considered. Problems of this nature can be minimized by operating all devices except the phase detector, charge pump, and VCO from a separate and well isolated supply. A common method uses a master supply of about 10 or 12 volts and two regulators to produce voltages for the PLL – one for all the logic (including the phase detector) and the other for all circuitry associated with the VCO control line.

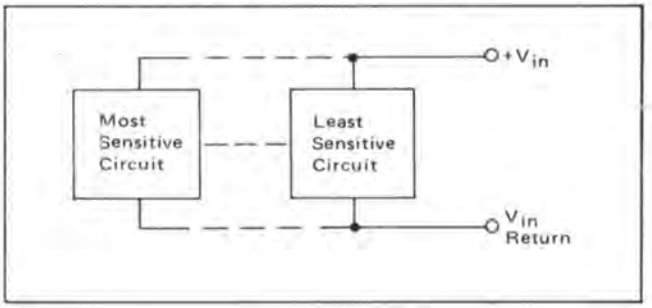
Sideband and noise performance is also a function of good power supply and regulator layout. As mentioned earlier, extreme care should be exercised in isolating the control line voltage to the VCO from influences other than the phase detector. This not only means good voltage regulation but ac bypassing and adherence to good grounding techniques as well. Figure 24 shows two separate

FIGURE 24 – LOOP VOLTAGE REGULATION



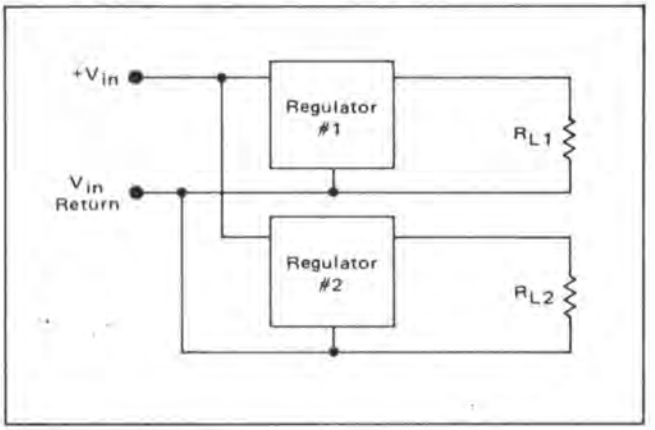

regulators and their respective loads. Resistor $R_S$ is a small stray resistance due to a common thin ground return for both $R_{L1}$ and $R_{L2}$. Any noise in $R_{L2}$ is now reproduced (in a suppressed form) across $R_{L1}$. Load current from $R_{L1}$ does not affect the voltage across $R_{L2}$. Even though the regulators may be quite good, they can hold $V_O$ constant only across their outputs, not necessarily across the load (unless remote sensing is used). One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 25.

FIGURE 25 – REGULATOR LAYOUT



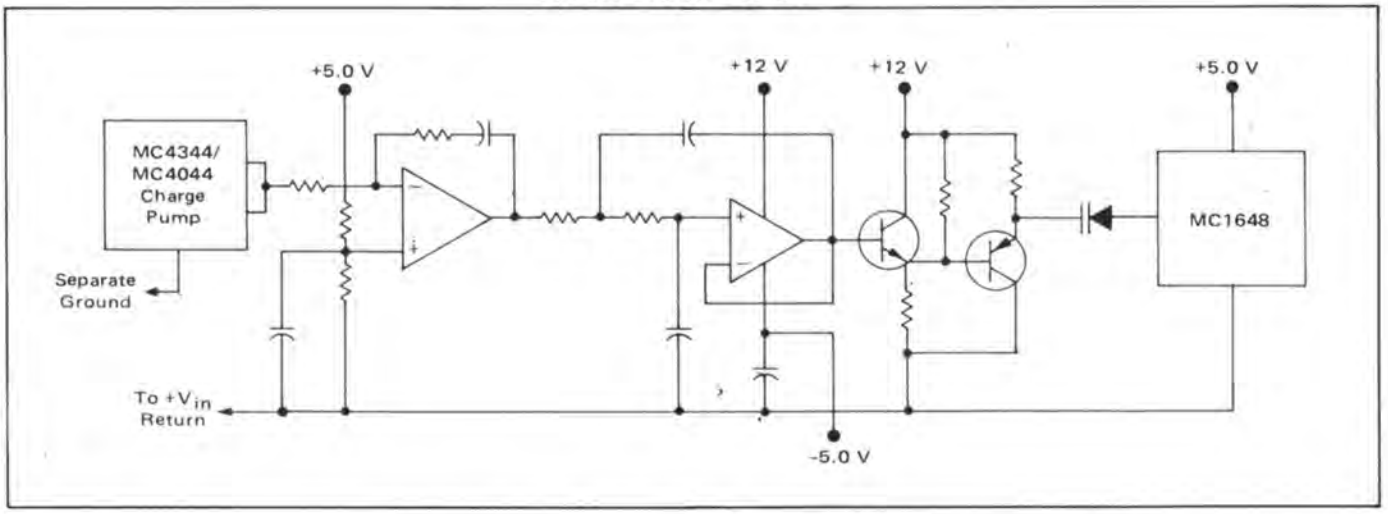

Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 26.

FIGURE 26 – REGULATOR GROUND CONNECTION




In Figures 24 and 26, $R_{L1}$ and $R_{L2}$ represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 27 to illustrate the common grounding technique.

FIGURE 27 – PARTIAL SCHEMATIC OF LOOP AMPLIFIER AND FILTER




Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 28). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 28 – SUGGESTED BYPASSING PROCEDURE

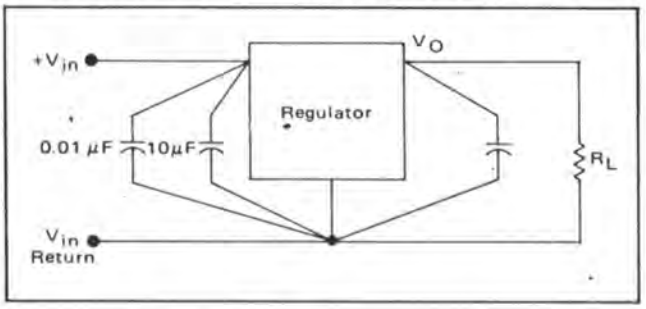
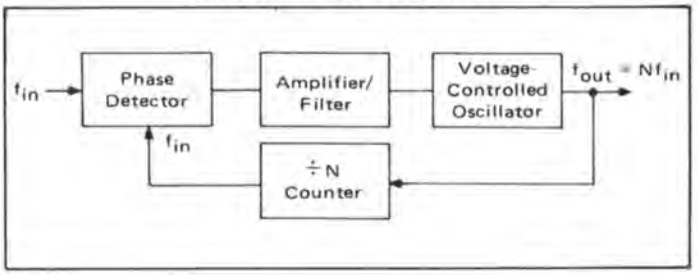



FIGURE 29 – PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER




## APPLICATIONS INFORMATION

### Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{out} = f_{in}$, although normally a programmable counter in the feedback loop insures the general rule that $f_{out} = Nf_{in}$ (Figure 29). In the synthesizer $f_{in}$ is usually constant (crystal controlled) and $f_{out}$ is changed by varying the programmable divider (÷ N). By stepping N in integer increments, the output frequency is changed by $f_{in}$ per increment. In communication use, this input frequency is called the "channel spacing" or, in general, it is the reference frequency.

There is essentially no difference in loop dynamic problems between the basic PLL and synthesizers except that synthesizer designers must contend with problems peculiar to loops where N is variable and greater than 1. Also, sidebands or spectral purity usually require special attention. These and other aspects are discussed in greater detail in AN-535. The steps for a suitable synthesis procedure may be summarized as follows:

### Synthesis Procedure

1. Choose input frequency. ($f_{ref}$ = channel spacing)
2. Compute the range of digital division:

$$N_{max} = \frac{f_{max}}{f_{ref}}$$

$$N_{min} = \frac{f_{min}}{f_{ref}}$$

3. Compute needed VCO range:

$$(2f_{max} - f_{min}) < f_{VCO} < (2f_{min} - f_{max})$$

4. Choose minimum ζ from transient response plot, Figure 9. A good starting point is ζ = 0.5.

5. Choose $\omega_n$ from needed response time (Figure 9):

$$\omega_n = \frac{\omega_n t}{t}$$

6. Compute C:

$$C = \frac{K_\phi K_V}{N_{max}\omega_n^2 R_1}$$

7. Compute $R_2$:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C}$$

8. Compute $\zeta_{max}$:

$$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}}$$

9. Check transient response of $\zeta_{max}$ for compatibility with transient specification.
10. Compute expected sidebands:

$$\frac{\text{sideband}}{f_{out}} \cong \frac{(I_b + I_L)R_2 K_V}{\omega_{ref}} \qquad (A)$$

($I_L$ is about 100 nA at $T_J = 25^oC$.)

11. If step 10 yields larger sidebands than are acceptable, add a single pole at the loop amplifier by splitting $R_1$ and adding $C_c$ as shown in Figure 15:

$$C_c \cong \frac{0.8}{R_1\omega_n}$$

Added sideband suppression (dB) is:

$$dB \cong 20\log_{10}\frac{1}{\sqrt{1+\frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad (B)$$

12. If step 11 still does not give the desired results, add a second order section at $\omega_c = 5\ \omega_n$ using either the configuration of Figure 20 or 21. The expected improvement is twice that of the single pole in step 10.

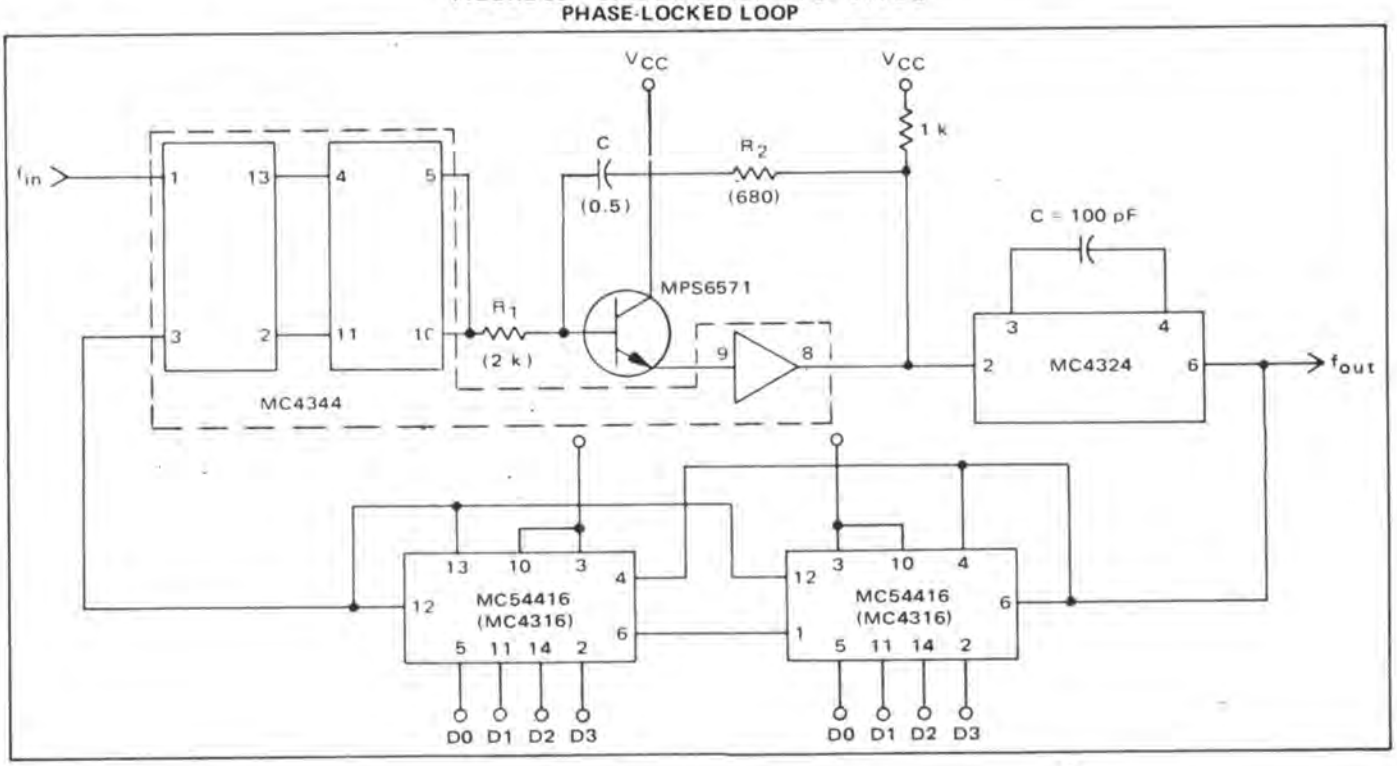
$$dB \cong 40\log_{10}\frac{1}{\sqrt{1+\frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad (C)$$

Total sideband rejection is then the total of $20\log_{10}$(A) + (B) + (C).

**Design Example** (Figure 30)

Assume the following requirements:
Output frequency, $f_{out}$ = 2.0 MHz to 3.0 MHz
Frequency steps, $f_{in}$ = 100 kHz

**FIGURE 30 – CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP**



Lockup time between channels (to 5%) = 1.0 ms
Overshoot < 20%.
Minimum sideband suppression = -30 dB

From the steps of the synthesis procedure:

1. $f_{ref} = f_{in} = 100\ kHz$

2. $N_{max} = \frac{f_{max}}{f_{ref}} = \frac{3.0\ MHz}{0.1\ MHz} = 30$

$N_{min} = \frac{f_{min}}{f_{ref}} = \frac{2.0\ MHz}{0.1\ MHz} = 20$

3. VCO range:
The VCO output frequency range should extend beyond the specified minimum-maximum limits to accommodate the overshoot specification. In this instance $f_{out}$ should be able to cover an additional 20% on either end. End limits on the VCO are:

$f_{out}max \geqslant 3.0 + 0.2(3.0) = 3.6\ MHz$
$f_{out}min \leqslant 2.0 - 0.2(2.0) = 1.6\ MHz$

This VCO range ($\approx 2.25:1$) is realizable with the MC4324/4024 voltage controlled multivibrator. From Figure 7 of the MC4324/4024 data sheet we find the required tuning capacitor value to be 120 pF and the VCO gain, $K_V$, typically $11 \times 10^6$ rad/s/v.

4. From the step response curve of Figure 5, $\zeta = 0.8$ will produce a peak overshoot less than 20%.

5. Referring to Figure 9, overshoot with $\zeta = 0.8$ will settle to within 5% at $\omega_n t = 4.5$. Since the required lock-up time is 1.0 ms,

$$\omega_n = \frac{\omega_n t}{t} = \frac{4.5}{t} = \frac{4.5}{0.001} = (4.5)(10^3)\ rad/s$$

6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, $K_\phi$, for the MC4344/4044 is approximately 0.1 volt/radian with $R_1 = 1\ k\Omega$. Therefore,

$$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)^2(10^3)} = 2.0\ \mu F$$

7. At this point, $R_2$ can be computed:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(2 \times 10^{-6})} = 180\ \Omega$$

8. $\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}} = 0.98$

9. Figure 9 shows that $\zeta = 0.98$ will meet the settling time requirement.

10. Sidebands may be computed for two cases: (1) with $I_L$ (charge pump leakage current) nominal (100 nA), and (2) with $I_L$ maximum (5.0 μA).

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{max} = \frac{(5 \times 10^{-6})(180)(11 \times 10^6)}{4.5 \times 10^3} \cong 2.2$$

Since $I_L$ (nominal) is 50 times lower than $I_L$ (maximum), the sideband-to-center frequency ratio nominally would be:

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{nom} = \frac{2.2}{50} = 0.044$$

$$= 20\log_{10}(0.044) \cong -27\ dB$$

This suppression figure does not meet the original design requirement. Therefore further improvements will be made.

11. By splitting $R_1$ and $C_C$, further attenuation can be gained. The magnitude of $C_C$ is approximately:

$$C_C \cong \frac{0.8}{R_1\omega_n} = \frac{0.8}{(10^3)(4.5)(10^3)} \cong 0.2\ \mu F$$

Improvement in sidebands will be:

$$20\log_{10}\frac{1}{1 + \frac{105^2}{25(4.5 \times 10^3)^2}} = -13\ dB$$

Nominal suppression is now -40 dB. Worst-case is 34 dB higher than nominal suppression (50:1 ratio), or -6.0 dB. Therefore additional filtering is required.

12. Additional filters such as second order sections are exactly double the single order sections as designed in step 11. Adding such a filter would give an additional -26 dB rejection factor. Therefore, one second order filter section would result in an overall sideband suppression of -67 dB nominal and -32 dB maximum.

Design of the passive components for the added section with R assigned a value of 10 kΩ is:

$$C = \frac{0.1}{\omega_n R} = \frac{0.1}{(4.5 \times 10^{-3})(10^4)} = 0.2\ \mu F$$

See Figures 20 and 21 for two configurations that will satisfy this filter requirement.

## Clock Recovery from Phase-Encoded Data

The electro-mechanical system used for recording digital data on magnetic tape often introduces random variations in tape speed and data spacing. Because of this and the encoding technqiue used, it is usually necessary to regenerate a synchronized clock from the data during this read cycle. One method for doing this is to phase-lock a voltage controlled multivibrator to the data as it is read (Figure 31).

FIGURE 31 – CLOCK RECOVERY FROM PHASE-ENCODED DATA

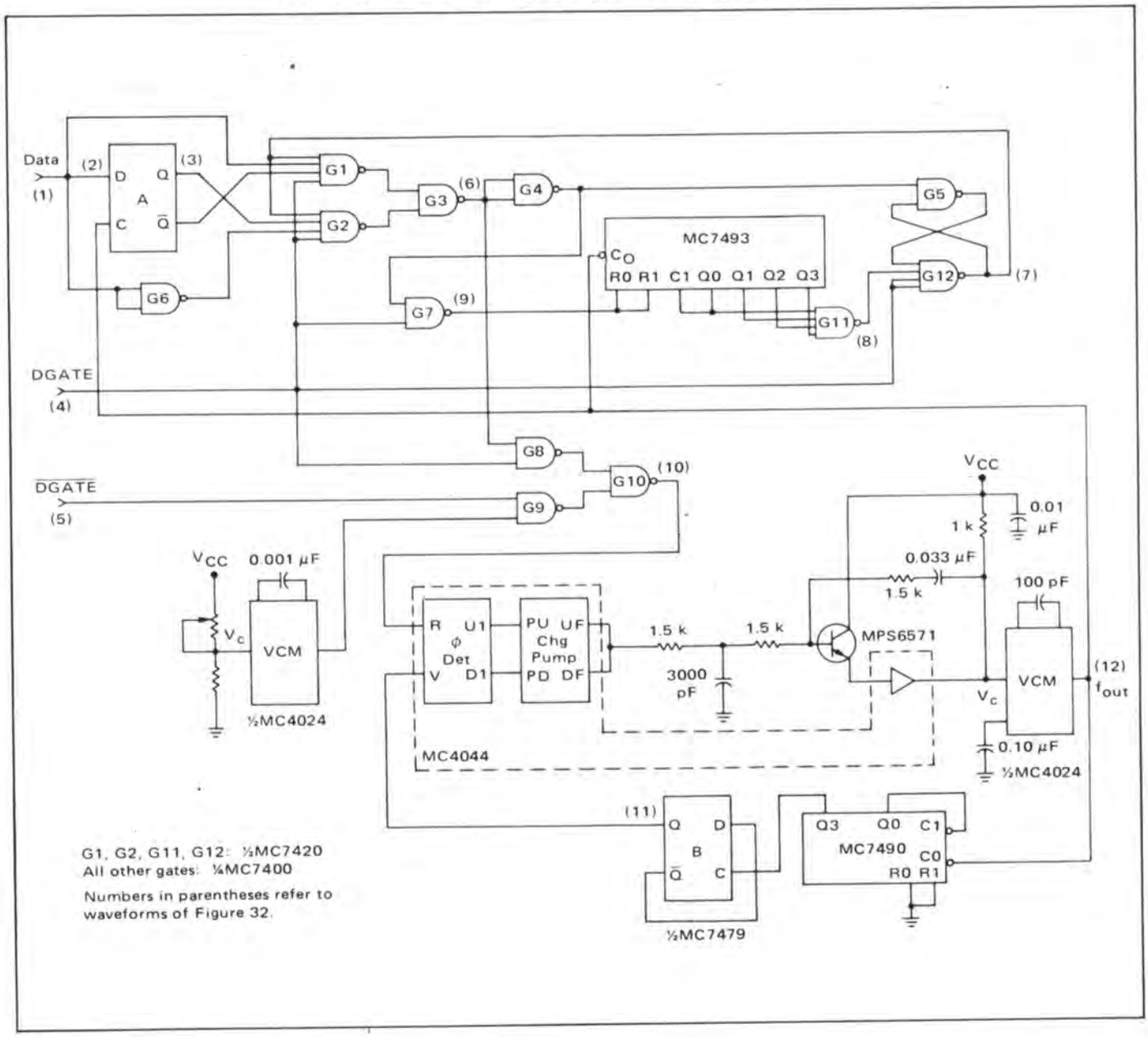
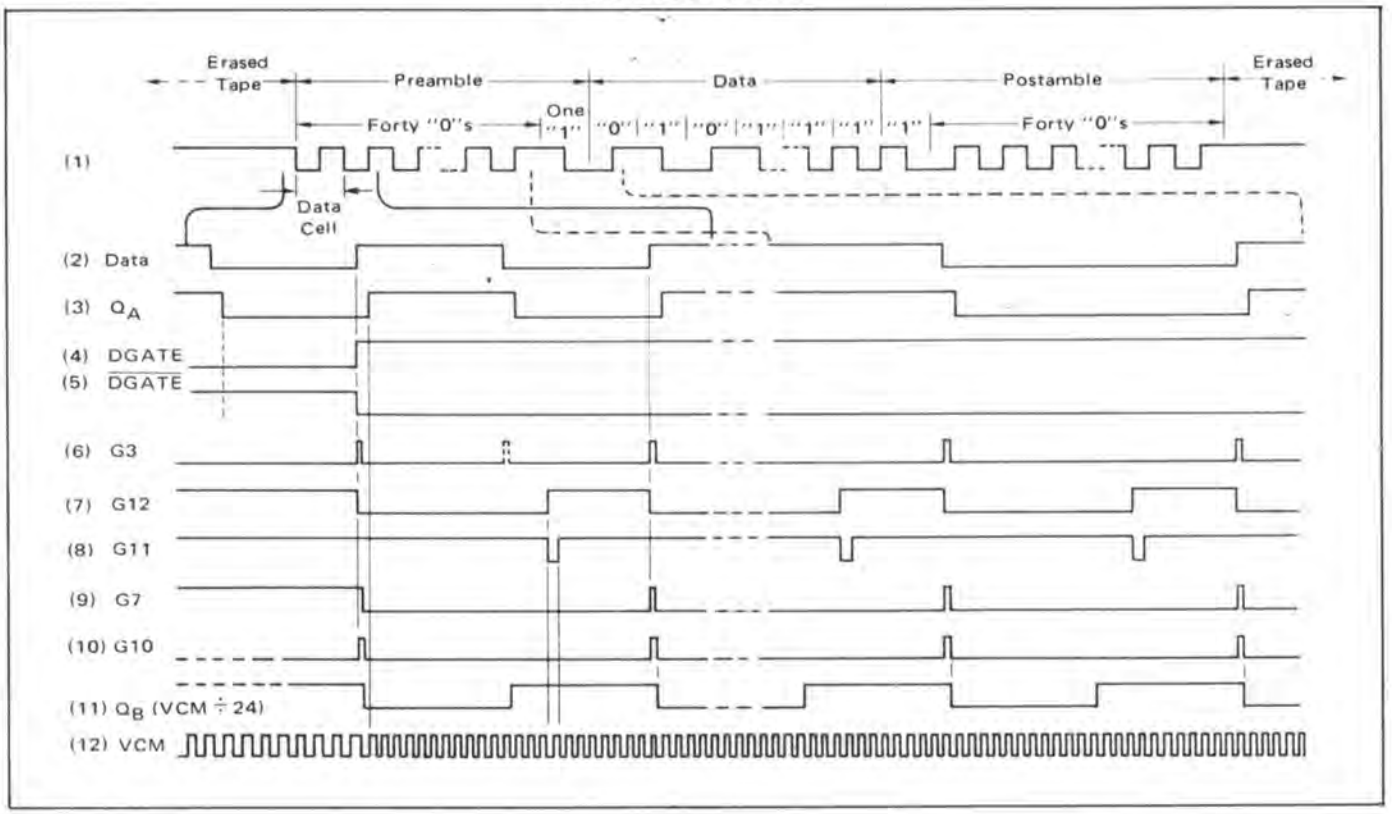


FIGURE 32 – TIMING DIAGRAM – CLOCK RECOVERY FROM PHASE-ENCODED DATA




A typical data block using the phase encoded format is shown in row 1 of Figure 32. The standard format calls for recording a preamble of forty "0"s followed by a single "1"; this is followed by from 18 to 2048 characters of data and a postamble consisting of a "1" followed by forty "0"s. The encoding format records a "0" as a transition from low to high in the middle of a data cell. A "1" is indicated by a transition from high to low at the data cell midpoint. When required, phase transitions occur at the end of data cells. If a string of either consecutive "0"s or consecutive "1"s is recorded, the format duplicates the original clock; the clock is easily recovered by straight forward synchronization with a phase-locked loop. In the general case, where the data may appear in any order, the phase-encoded data must be processed to obtain a single pulse during each data cell before it is applied to the phase detector. For example, if the data consisted only of alternating "1"s and "0"s, the phase-encoded format would result in a waveform equal to one-half the original clock frequency. If this were applied directly to the loop, the VCM would of course move down to that frequency. The encoding format insures that there will be a transition in the middle of each data time. If only these transitions are sensed they can be used to regenerate the clock. The schematic diagram of Figure 31 indicates one method of accomplishing this.

The logic circuitry generates a pulse at the midpoint of each data cell which is then applied to the reference input of the phase detector. The loop VCM is designed to operate at some multiple of the basic clock rate. The VCM frequency selected depends on the decoding resolution desired and other system timing requirements. In this example, the VCM operates at twenty-four times the clock rate (Figure 32, Row 12).

Referring to Figure 31 and the timing diagram of Figure 32, the phase-encoded data (Figure 32, Row 1) is combined with a delayed version of itself (output of flip-flop A row 3) to provide a positive pulse out of G3 for every transition of the input signal. Portions of the data block are shown expanded in row 2 of Figure 32. Flip-flop A delays the incoming data of one-half of a VCM clock period. Gates G1, G2, and G3 implement the logic Exclusive OR of waveforms 1 and 3 except when inhibited by DGATE (row 4) or the output of G12 (row 7). DGATE and its complement, $\overline{DGATE}$, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the

counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 31, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and $\overline{\text{DGATE}}$ cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 31 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a -3.0 dB loop bandwidth much less than the input data rate ($\approx$ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, $\omega_n$, calculate $\omega_n$ as:

$$\omega_{-3\,dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \quad (24)$$

or for $\omega_{-3\,dB} = (2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_n = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40-bit preamble, or for twenty 8.34 $\mu$s data periods.

$$\omega_n t = (3.05)10^4\,(20)(8.34)10^{-6} = 5.1 \quad (26)$$

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_\phi K_V}{R_1 CN} = \omega_n^2 \quad (27)$$

and

$$\frac{K_\phi K_V R_2}{R_1 N} = 2\zeta\omega_n \quad (28)$$

where $K_\phi = 0.015$ v/rad
$K_V = (18.2)10^6$ rad/s/volt
$N = 24$ = Feedback divider ratio
$\omega_n = (3.05)10^4$ rad/s
$\zeta = 0.707$

$$\frac{K_\phi K_V}{N} = \frac{(0.115)(18.2)10^6}{24} = (8.72)10^4$$

From Equation 27:

$$R_1 C = \frac{K_\phi K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^2 10^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta\omega_n N}{K_\phi K_V} = \frac{2(0.707)(3.04)10^4}{(8.72)10^4} = 0.494 \approx \tfrac{1}{2}$$

Let $R_1 = 3.0\,k\Omega$; then $R_2 = 1.5\,k\Omega$ and

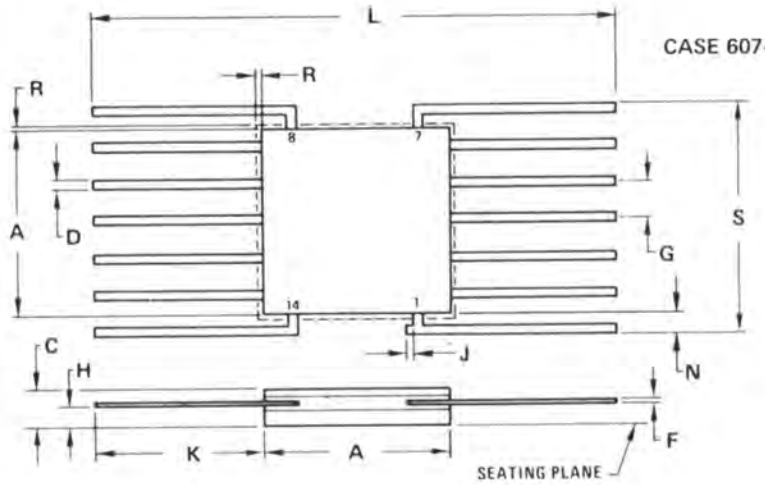
$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

or using a close standard value, use $C = 0.0033\,\mu F$. Now add the additional prefiltering by splitting $R_1$ and selecting a time constant for the additional section so that it is large with respect to $R_2C_2$.

$$10(\tfrac{1}{2}R_1)C_s = R_2C$$

or

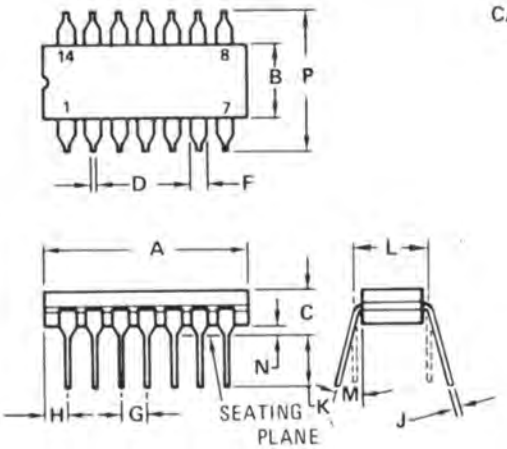
$$C_s = \frac{2R_2C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300\text{ pF}$$




CASE 607-05

NOTES:
1. ALL NOTES ASSOCIATED WITH TO-86 OUTLINE SHALL APPLY.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION.

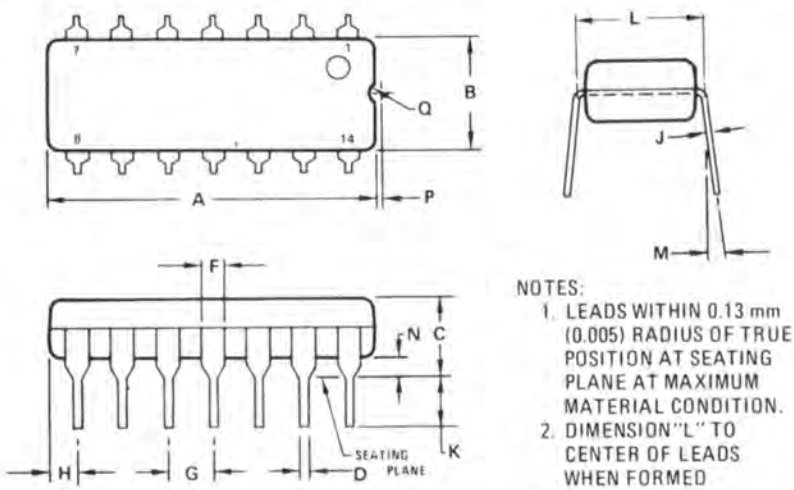
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 0.76 | 1.78 | 0.030 | 0.070 |
| D | 0.33 | 0.48 | 0.013 | 0.019 |
| F | 0.08 | 0.15 | 0.003 | 0.006 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.30 | 0.89 | 0.012 | 0.035 |
| J | – | 0.38 | – | 0.015 |
| K | 6.35 | 9.40 | 0.250 | 0.370 |
| L | 18.80 | – | 0.740 | – |
| N | 0.25 | – | 0.010 | – |
| R | – | 0.38 | – | 0.015 |
| S | 7.62 | 8.38 | 0.300 | 0.330 |




CASE 632
TO-116

NOTES:
1. ALL RULES & NOTES ASSOCIATED WITH TO-116 OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 16.8 | 19.9 | 0.660 | 0.785 |
| B | 5.59 | 7.11 | 0.220 | 0.280 |
| C | – | 5.08 | – | 0.200 |
| D | 0.381 | 0.584 | 0.015 | 0.023 |
| F | 0.77 | 1.77 | 0.030 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.203 | 0.381 | 0.008 | 0.015 |
| K | 2.54 | – | 0.100 | – |
| L | 7.62 BSC | | 0.300 BSC | |
| M | – | 15° | – | 15° |
| N | 0.51 | 0.76 | 0.020 | 0.030 |
| P | – | 8.25 | – | 0.325 |




NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 646

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 18.16 | 18.80 | 0.715 | 0.740 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 4.06 | 4.57 | 0.160 | 0.180 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.32 | 1.83 | 0.052 | 0.072 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.37 | 7.87 | 0.290 | 0.310 |
| M | – | 10° | – | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |
| P | 0.13 | 0.38 | 0.005 | 0.015 |
| Q | 0.51 | 0.76 | 0.020 | 0.030 |



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ENGINEERING
REPORT

# A NEW FILTERING PROCESS FOR OPTIMAL OVERSHOOT CONTROL

HARRIS
COMMUNICATIONS AND
INFORMATION HANDLING

# A NEW FILTERING PROCESS FOR OPTIMAL OVERSHOOT CONTROL

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## ABSTRACT

When both peak amplitude (in the time domain) and bandwidth constraints are placed upon a signal as in FM stereo broadcasting, there are conflicts among the requirements for limiting modulation peaks, attenuating components beyond 15 kHz, and maintaining a flat amplitude characteristic to 15 kHz. Previous attempts at overshoot control do not simultaneously satisfy all of the above requirements. Furthermore, some techniques currently in use can cause severe audible distortion under certain programming conditions.

Lowpass filters by design change the frequency distribution of a signal and by consequence change the phase relationships of the same signal. Both changes are causes of overshoot. Elimination of harmonic terms deletes components that serve to reduce the peak amplitude of the signal. Phase distortion rearranges signal components as a function of time to form overmodulating peaks.

Optimal overshoot control must perform all of the following under all programming conditions:

1. Flat frequency response to 15 kHz at all levels up to 100% modulation.
2. High attenuation of frequencies above 15 kHz.
3. Suppress overmodulation due to overshoot to an insignificant level.
4. Insignificant THD and IM distortion at any level up to 100% modulation.
5. No degradation of audio quality.

A new technique that eliminates overmodulation due to overshoot is presented and explained.

## I. INTRODUCTION

**BACKGROUND:** FM stereo radio broadcasting is rapidly becoming a highly competitive medium. This change manifests itself in many ways, including the effort to have a technically superior sound. This objective usually involves a tradeoff between quality and quantity, or fidelity vs. loudness. Most audio processing innovations to date sacrifice some amount of fidelity for some degree of loudness increase. The Harris Dynamic Transient Response (DTR) filter, an integral part of the Harris MS-15 exciter, allows a loudness increase of 2-6 dB (dependent on limiter type) with absolutely no degradation of fidelity.

**PRINCIPLES OF STEREO FM:** FM stereophonic broadcasting is a frequency domain multiplexed (FDM) system. A left-plus-right (L+R) signal is transmitted in the band 50 Hz-15 kHz. This is the monaural baseband signal. A double sideband suppressed carrier (DSB) signal modulated with left-minus-right information is transmitted at 38 kHz. To properly demodulate the DSB 38 kHz signal, a 19 kHz pilot tone is transmitted with a phase such that when it is frequency-doubled, L-R information can be synchronously detected. The composite stereo signal is shown in Fig. 1.

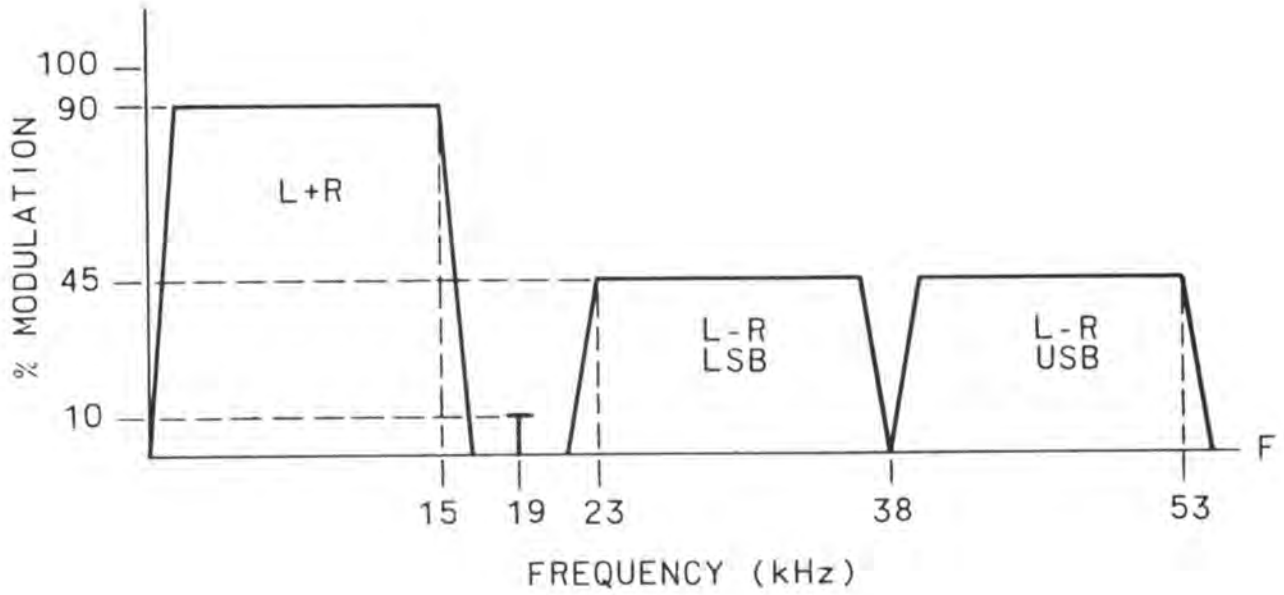



FIGURE 1
FM STEREO MULTIPLEX SIGNAL SPECTRUM

**WHY AUDIO LOWPASS FILTERS ARE REQUIRED:** There are constraints placed upon the amplitude and bandwidth characteristics of the left- and right-channel audio signals such that the resultant L+R and L-R signals will exceed neither their amplitude bounds nor bandwidth allocations. Otherwise the multiplexed signals would suffer distortion and mutual interference.

To control the amplitude of the L and R channel signals AGC amplifiers, peak limiters, and clipping devices are customarily used. Typically these processors add to the harmonic content of the program, producing a signal which would result in excessive bandwidth. In the better stereo generators, lowpass filters have been included to attenuate harmonics beyond the 15 kHz bandwidth of the system.

Some inexpensive switching type stereo generators omit the audio lowpass filters in an attempt to eliminate overshoot. With no audio filters, the stereo composite lowpass filter will overshoot instead. This is absurd. Not only has the overshoot problem been left unsolved, but the stereo generator is vulnerable to pilot interference and aliasing.

## II. CAUSES AND EFFECTS OF OVERSHOOT

**MECHANISMS OF OVERSHOOT IN LOWPASS FILTERS:** Although the input to a lowpass filter may be accurately amplitude-limited, such is not necessarily the case at the filter's output. Ringing and overshoot of the filter can seriously degrade the accuracy of the limiting action. Lowpass filters may overshoot 6 dB (100%) on some signals which are not uncommon at the output of audio processing equipment.

A lowpass filter changes two independent qualities of its input signal. In addition to the obvious change of the amplitude vs. frequency characteristic the filter also changes phase relationships among different frequencies in the filter's passband. This is equivalent to stating that different frequencies take different lengths of time to propagate through the filter. Associated with these two changes to the signal are two mechanisms causing overshoot.

1. ATTENUATION OF HARMONICS

Consider the ideal case of a lowpass filter with rectangular frequency response and zero time delay. This filter is in fact unrealizable but nevertheless would exhibit overshoot due to elimination of harmonics. The frequency response of this filter is shown in Fig. 2.

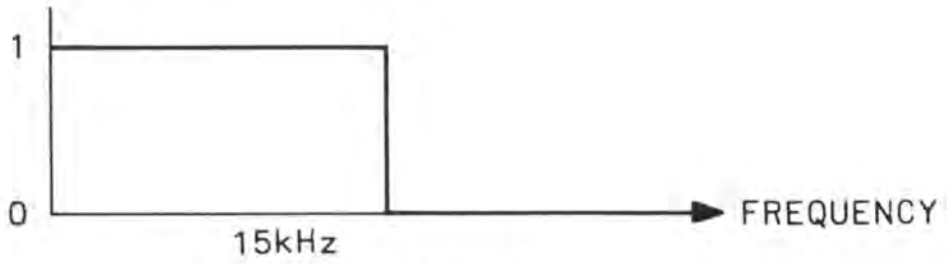



FIGURE 2
IDEAL FILTER FREQUENCY RESPONSE

Assume that the input signal is a 10 kHz squarewave of amplitude A. The Fourier expansion of this signal is:

$$v(t) = A\frac{4}{\pi}\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}\sin(2\pi fnt)$$

where f is frequency.

The squarewave signal has components at the fundamental and odd harmonic frequencies only, i.e., 10, 30, 50, 70, etc. kHz. Since the filter cuts off at 15 kHz only the fundamental (10 kHz) component of the squarewave appears at the filter output. Note that if the squarewave amplitude (A) is one volt, then the peak value of the fundamental component (identically equal to the output signal) is 4/pi or 1.273. This constitutes an overshoot of 27%. The squarewave and its fundamental component are shown superposed in Fig. 3.

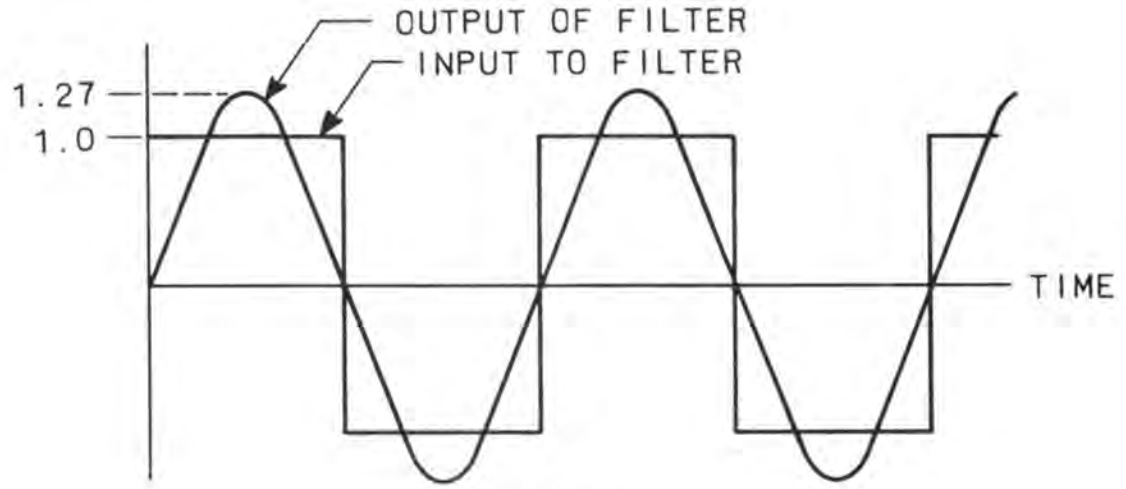



FIGURE 3
SQUAREWAVE AND FUNDAMENTAL COMPONENT

This is only one example of many possible signals that would cause a linear phase lowpass filter to overshoot.

2. NON-UNIFORM TIME DELAY

If different signals propagate through the filter with different time delays, it is possible for input signals separated in time to become coincident at the filter's output. This could result in an overshoot.

Continuing with the example of the squarewave, consider the case where only the fundamental and third harmonic fall within the filter's passband. Squarewaves in the range of 3-5 kHz satisfy this condition. The input and output of the ideal filter discussed in part 1 are shown in Fig. 4.

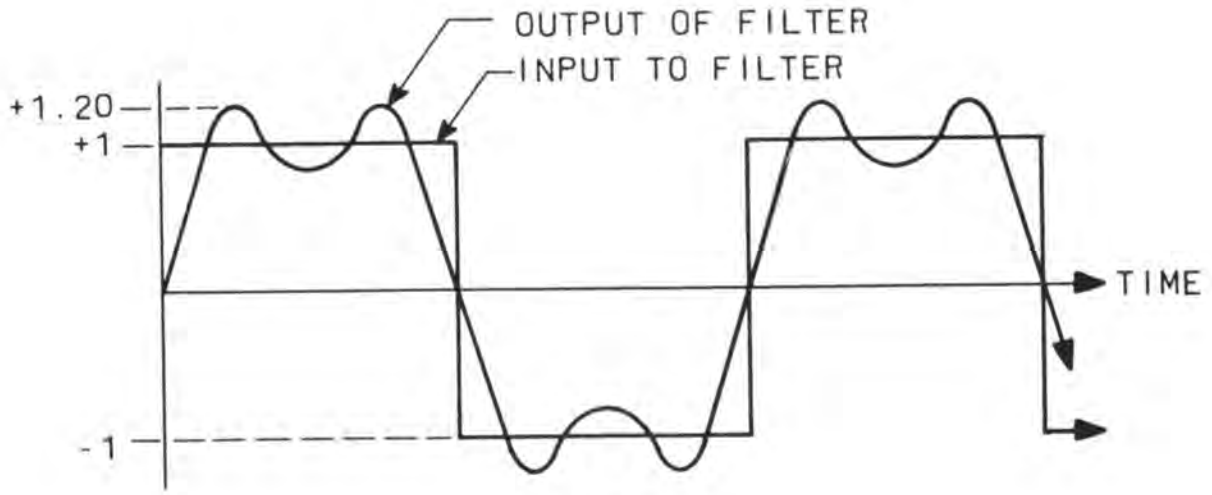



FIGURE 4

3-5kHz SQUAREWAVE RESPONSE: FUNDAMENTAL PLUS 3rd HARMONIC

Overshoot is 20.0%. Since such a filter is impossible to build, the response of Fig. 4 in general cannot be produced. Rather, time delay will vary as a function of frequency, thereby upsetting the phase relationship between the fundamental and third harmonic. If the phase of the third harmonic is shifted 180 degrees relative to the fundamental, the waveform of Fig. 5 results. Overshoot is 70% or 4.6 dB.

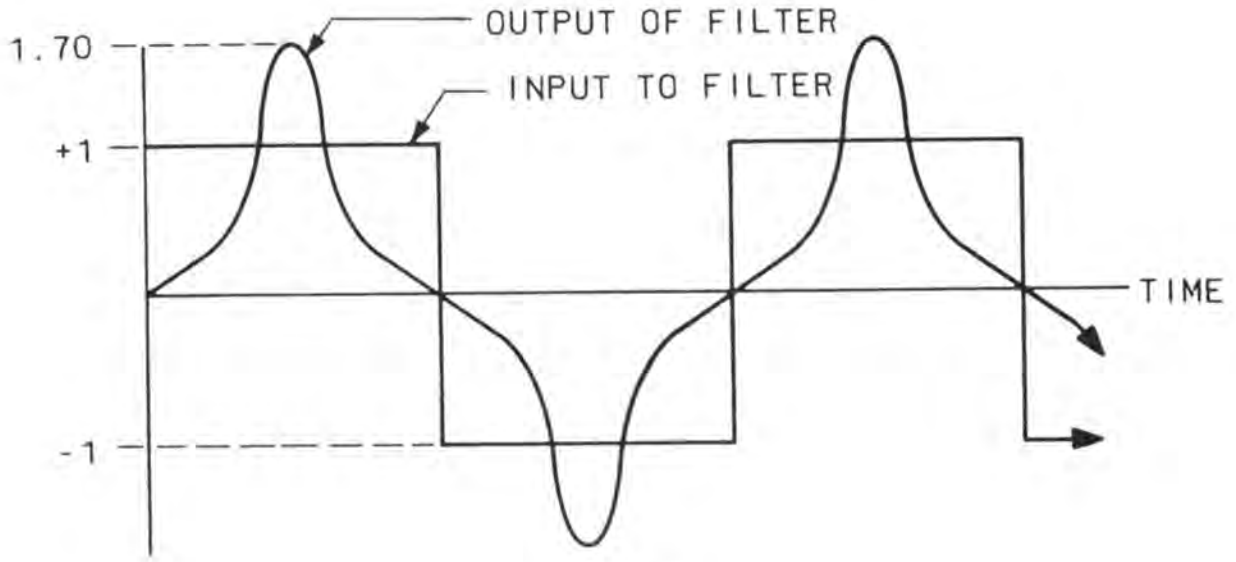



FIGURE 5

EFFECT OF PHASE DISTORTION

**EXAMPLES**: A typical filter specification may require frequency response to be flat within ±0.1 dB from 0-15 kHz and -50 dB at 19 kHz and above. By far the most practical filter meeting these specifications will be an elliptic function type filter. This filter exhibits a very sharp rate of cutoff and a highly nonuniform time delay characteristic.

A seventh order filter meeting these specifications has group delay (time delay) of approximately 43 microseconds which is uniform from DC to 3.5 kHz, 45 microseconds at 5 kHz, 53 microseconds at 7.5 kHz, 62 usec. at 10 kHz, increasing to 238 microseconds at 15 kHz which corresponds to 1,285 degrees of phase distortion (3½ rotations). Therefore the squarewave response of Fig. 5 is certainly possible with this filter.

Time delay generally increases with frequency within the passband of an elliptic filter. Minimum time delay is at DC while maximum time delay within the passband occurs at the cutoff frequency. A test signal has been devised which causes filters to overshoot primarily as a function of their time delay distortion. The test signal consists of a sinewave burst immediately followed by a DC step signal. The sinewave will accumulate maximum time delay (238 usec.) while the DC step signal will accumulate a minimal time delay (43 usec.). At the filter's output the sinewave will coincide with the beginning of the DC step signal. This phenomenon is shown in Fig. 6. Note that the overshoot is 100% (6 dB)!

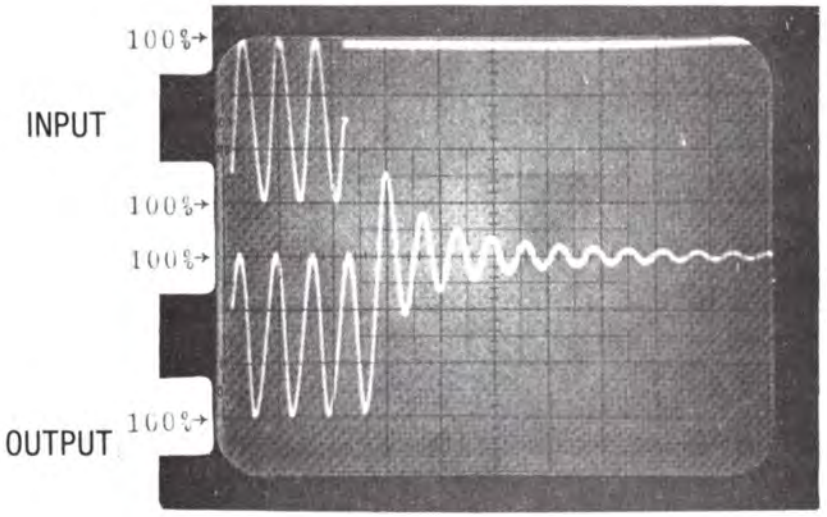



FIGURE 6

SINE/STEP FILTER RESPONSE

Through a combination of effects (both attenuation of harmonics and nonuniform time delay) a myriad of signal types can cause a typical elliptic lowpass filter to overshoot. A low frequency squarewave response is shown in Fig. 7.

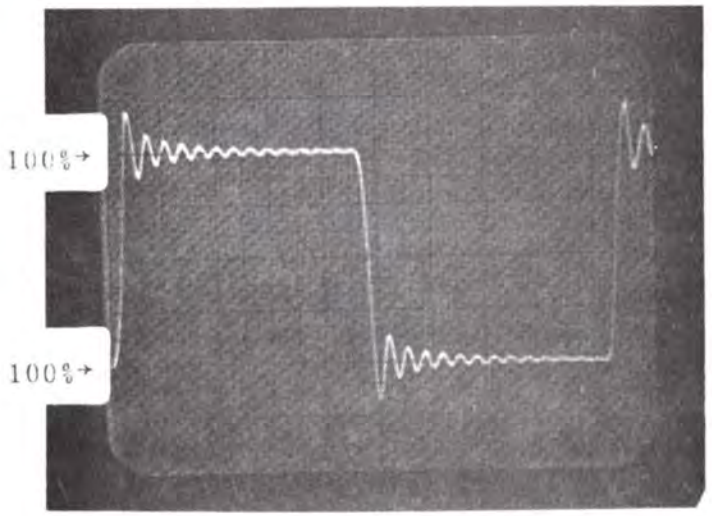



FIGURE 7

TYPICAL FILTER
SQUAREWAVE RESPONSE

The waveforms of Fig. 6 and Fig. 7 are common with certain types of music and/or certain types of FM limiters. To offset overshoot audio levels are simply turned down to a point where overshoots "of frequent recurrence" do not exceed 100% modulation. This can mean a sizeable reduction in modulation effectiveness, usually on the order of 2.5 - 6 dB!

## III. DEVELOPMENT OF A SOLUTION

**NEED FOR A NEW APPROACH:** There have been several previous approaches to the problem. Although existing systems do control overshoot, they also contribute unwanted side effects to the signal.

One method for overshoot control uses a delay line and an AGC stage. This system can cause gain "pumping". Another popular system uses alternate clipping and filtering combined with a complementary high frequency boost and cut. This system suffers from excessive intermodulation distortion and a high frequency rolloff which is dependent upon signal level.

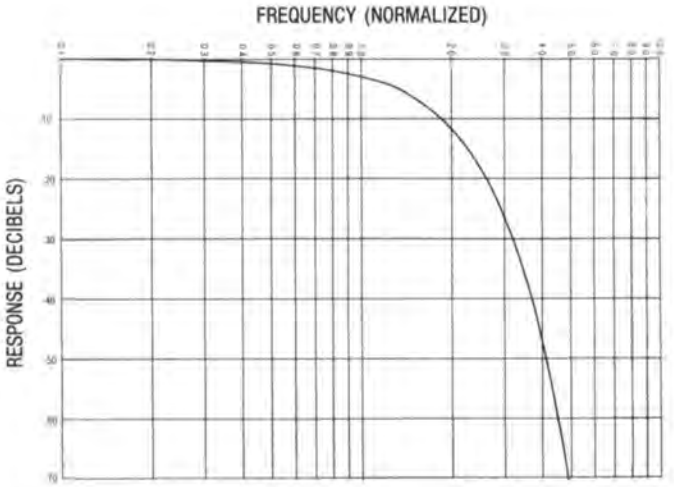
**CONSTRAINTS:** It is clearly desirable to have a filter which will eliminate harmonics above 15 kHz yet preserve the peak amplitude-limited nature of its input signal. Note that it is not necessary to have a filter that does not overshoot. Ringing and overshoot are completely unobjectionable provided that the overshoots do not exceed the 100% modulation level. From this point on, the term "overshoot" will denote only overshoots above 100% modulation. The filter requirements are:

1. Frequency response flat ±0.5 dB 20 Hz-15 kHz at all levels up to 100% modulation.
2. Attenuation above 19 kHz inclusive: 50 dB minimum.
3. Overshoots not exceeding 102% modulation.
4. Filter shall be transparent to steady state sinewave signals: THD and IM distortion 0.1% or less.
5. Any effect of eliminating overmodulating overshoots shall be inaudible.

**BESSEL FILTER UNSATISFACTORY:** One filter that does not overshoot is the Bessel type.The Bessel filter has maximally flat time delay for a minimum phase filter. However, its frequency response is inadequate. It has a very gradual rate of cutoff shown in Fig. 8.

FIGURE 8

IDEAL BESSEL FILTER RESPONSE
(GAUSSIAN FILTER)




**NON MINIMUM PHASE FILTER UNSATISFACTORY:** If one were to start with a filter with sufficiently sharp cutoff and attempt to find a phase function resulting in minimum overshoot, the result would be a lowpass filter that approximates linear phase, yet still overshoots. Even in the case of the ideal filter discussed under "Causes and Effects of Overshoot", the filter still overshoots.

**FILTER MUST BE NONLINEAR:** It would appear that there is no filter that satisfies all the above conditions. There is no linear time-invariant filter that satisfies all the above conditions. The statement that we can tolerate overshoots below a certain level implies that a nonlinear filter may work. That is, the filter may have one set of characteristics up to a certain level and other characteristics above that level. The requirements that the action be inaudible and that the filter be transparent to sinewaves (no harmonic or intermodulation distortion) imply that the filter must be perfectly linear up to 100% modulation. It is feasible to have a filter which is linear up to 100% modulation and nonlinear only when an overshoot above 100% is imminent.

## IV. SOLUTION: DYNAMIC TRANSIENT RESPONSE FILTER

**THEORY, IDEAL CASE:** Assume that we have two identical lowpass filters. The filters have a cutoff frequency of 15 kHz with infinite attenuation above and zero attenuation below, and a uniform time delay of 100 microseconds for all frequencies. (Such a filter is of course non-causal and impossible to build.) Consider the situation of Fig. 9 where the filters are cascaded; that is, the output of one filter drives the second.

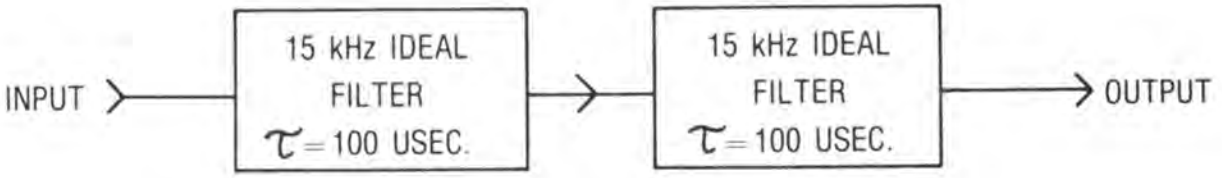



FIGURE 9
CASCADED IDEAL FILTERS

After application of a signal to the first filter, the output appears 100 usec. later with all components above 15 kHz removed. Phase relationships and amplitudes of components below 15 kHz are preserved; the only change to the signal will be the elimination of components above 15 kHz and 100 usec. of time delay. When the first filters's output is applied to the second, the second filter will function only as a 100 usec. delay line. Since there are no components above 15 kHz at the second filter's input, the second filter does not change the signal except for the addition of time delay. Therefore, **the first filter predicts the output of the second filter.** This prediction technique is employed in the Harris DTR filter.

**IMPLEMENTATION:** The DTR filter is a system which comprises two lowpass filters, an allpass filter (phase equalizer), and nonlinear compensation circuitry. A block diagram is given in Fig. 10.

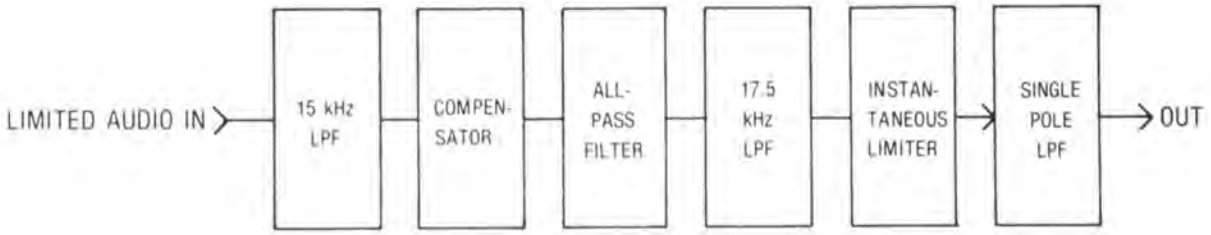



FIGURE 10
DYNAMIC TRANSIENT RESPONSE LOWPASS FILTER

The first filter (at extreme left) in Fig.10 is a seventh order elliptic type with a cutoff frequency of 15 kHz. The second filter is also seventh order elliptic but the cutoff frequency is 17.5 kHz. The second lowpass filter is preceded by an allpass filter which linearizes the lowpass filter's phase from DC to the cutoff frequency of the first filter (15 kHz). The combination of the allpass filter and the second lowpass filter presents an approximately uniform time delay of 100 usec. between DC and 15 kHz.

Since the passband of the first filter is contained within the linear phase passband of the second filter, the second filter changes neither the phase nor amplitude relationships of the first filter's output

but only adds time delay. Therefore, the first filter predicts the output of the second filter. If the first filter overshoots, the second filter will overshoot 100 microseconds later. The inverse is also true: if the first filter does not overshoot, the second filter will not overshoot.

The compensator functions only when the first filter overshoots. The compensator is designed to take the appropriate evasive action to stop the second filter's predicted overshoot. This nonlinear action is discussed below.

**EVASIVE ACTION: SUBTRACTING OVERSHOOTS:** A block diagram of the compensator is shown in Fig. 11.

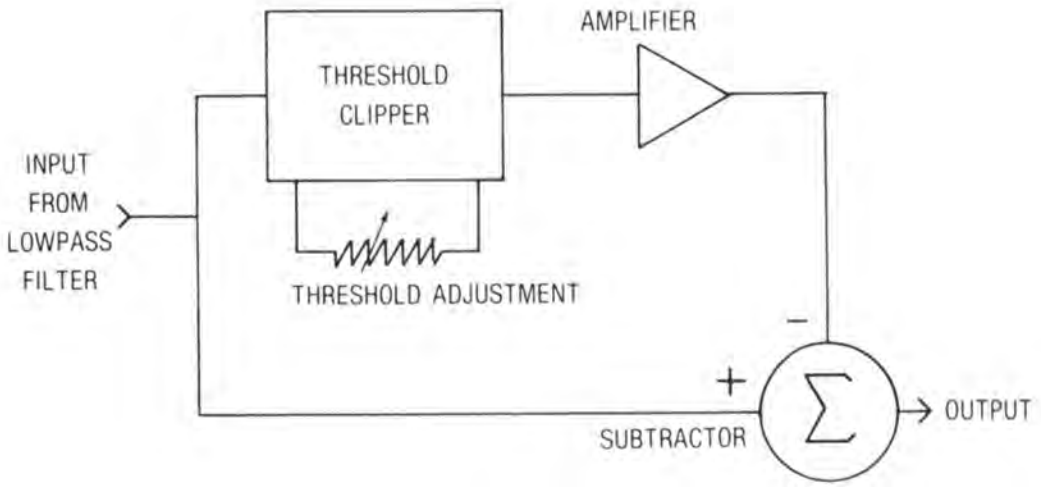
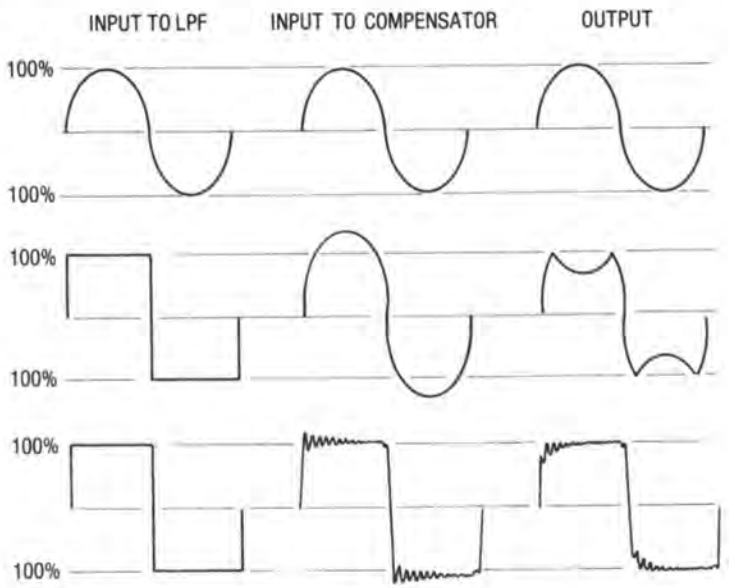



FIGURE 11
COMPENSATOR

Up to the 100% modulation level, the compensator causes no change to the signal. If the first filter overshoots above the 100% modulation level, that part of the signal which exceeds the threshold will be separated from the input and applied to the amplifier. The overshoots, having been separated and amplified, are subtracted from the original signal. Typical inputs and outputs are shown in Fig. 12.



The effect of this action is to subtract a component at the frequency of the offending overshoot.

The output of the compensator contains frequency components above and below 15 kHz. The compensator subtracts signal components below 15 kHz to eliminate overshoot. Incidental extraneous components above 15 kHz are generated in the process. These high frequency products must be removed in such a manner that phase relationships are preserved. For this reason the processed signal is filtered by an allpass/lowpass combination which approximates linear phase to 15 kHz.

**INSTANTANEOUS LIMITER/FILTER:** Due to several approximations in the process, the second filter may occasionally overshoot several percent. An instantaneous limiter follows the second filter for this reason. Harmonics generated by this device are very low in amplitude since overshoot has been nearly eliminated. The limiter drives a single pole filter which does not overshoot. Even severely processed audio results in harmonic components that are at least 60 dB down.

## V. RESULTS

**OPERATION:** The DTR filter is highly effective in its operation. Overmodulation due to overshoot has been reduced to 2%, approximately the accuracy of a modulation monitor. Operation is possible with **any** limiter and any program material including Dolby® processed audio. Setup is easy. All one does is to apply a signal that is known not to overshoot at 100% peak modulation. This can be a 400 Hz sinewave. Using this signal as a reference the compensation thresholds are set to a level corresponding to 100% modulation. LED indicators are provided to indicate when an overshoot is compensated, thereby facilitating setup.

Extensive listening and A-B tests have shown that on all type of programming the DTR filter produces no audible effect. Unlike other techniques using AGC, delay lines, or conventional clippers, the DTR filter takes action if and only if an overshoot is imminent. Because the energy contained in the overshoots is inappreciable, deletion of that energy is imperceptible to the ear. The modulation monitor, however, does not respond to average energy but rather peak voltage. The perception of the modulation monitor (and the FCC) is unlike that of the ear and **does** respond to low energy, high instantaneous amplitude transients.

The overshoot compensator removes the transients above 100% modulation. It does no more and no less.

**WAVEFORMS:** When a 600 Hz squarewave is applied to a conventional 15 kHz elliptic function lowpass filter the output rings and overshoots as shown by the top trace of Fig. 13.

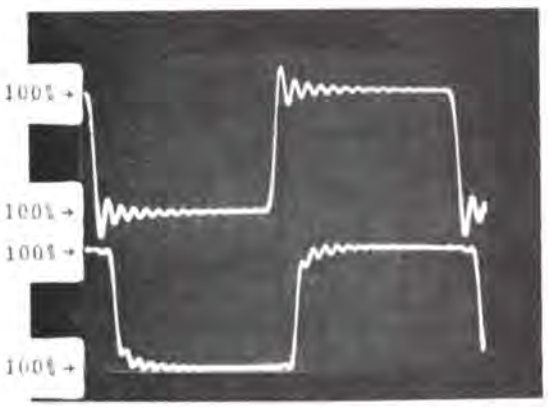



FIGURE 13

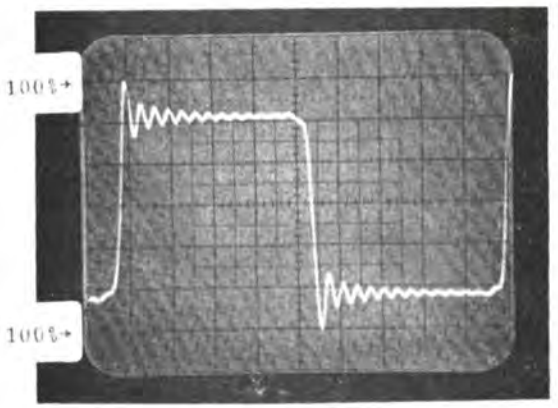
SQUAREWAVE RESPONSES

The DTR filter is shown in the bottom trace. There is a small amount of ringing; however, none of this causes overmodulation.

Fig. 14 shows the same squarewave but applied at 65% modulation. The system is completely linear at this level and no compensation is taking place.

FIGURE 14

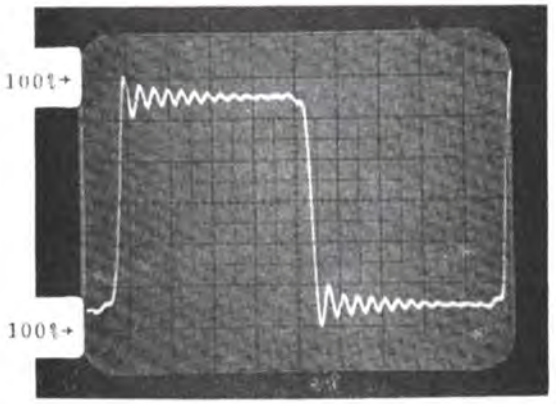
DTR FILTER RESPONSE:
SQUAREWAVE AT 65% MODULATION




In Fig. 15 the level has been increased to 90% modulation. Here there is some action taking place to limit the first cycle of ringing to 100%.

FIGURE 15

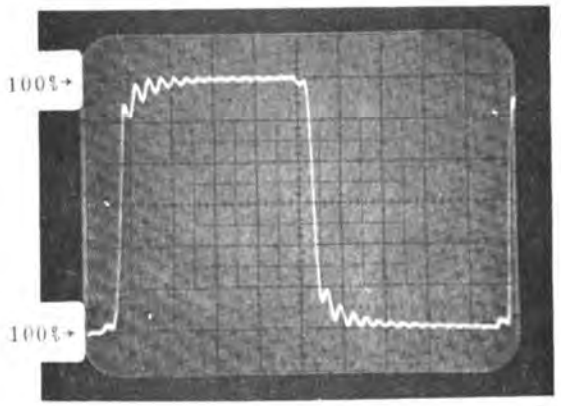
DTR FILTER RESPONSE:
SQUAREWAVE AT 90% MODULATION



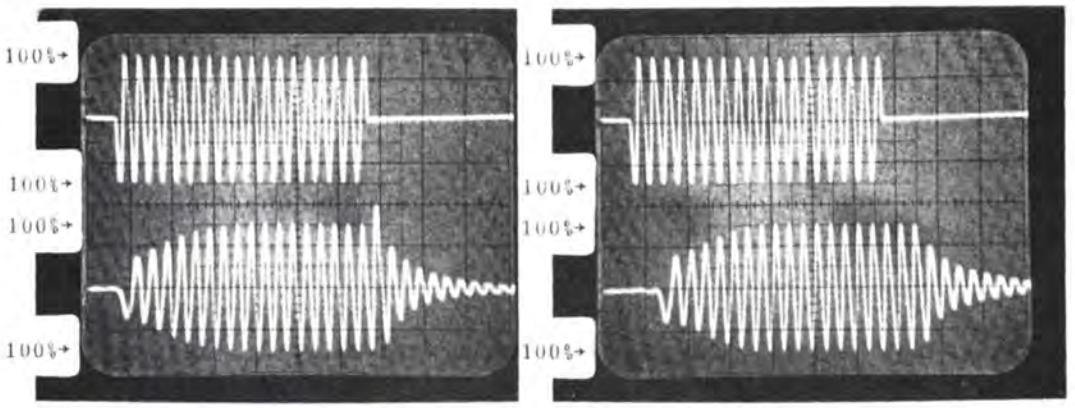

Finally in Fig. 16 the overshoot compensator is completely enabled as the squarewave is applied at 100% modulation.

FIGURE 16

DTR FILTER RESPONSE:
SQUAREWAVE AT 100% MODULATION



Tone bursts also demonstrate the capabilities of the DTR filter. Fig. 17 shows a 15.0 kHz tone burst input signal, the output of a conventional filter, and the output of the DTR filter.



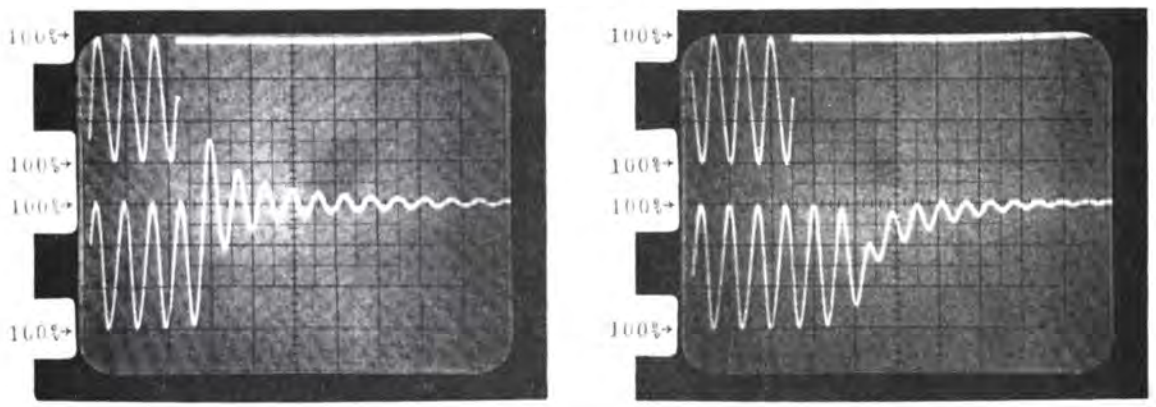

A. CONVENTIONAL FILTER B. DTR FILTER

TOP TRACE: INPUT
BOTTOM TRACE: OUTPUT

TONE BURST TESTS

FIGURE 17

One of the most difficult tests to be contrived for a filter is the signal described under "Examples", Causes and Effects of Overshoot. The signal consists of a sinewave at 100% modulation at a frequency very close to cutoff (15.0 kHz) applied for a time sufficiently long to ensure steady-state filter response, followed immediately by a transition to a step signal. The sinewave signal, being close to cutoff, will accumulate a long time delay with respect to the low-frequency step. At the filter's output, the signals will coincide at the transition. Fig. 18a shows the input and output of a conventional filter. Overshoot is 100%. If the modulation level of the transmitter were to be turned down to accommodate such overshoots without causing overmodulation, a full 6 dB of signal would be lost! The compensated filter response to the same test signal is shown in Fig. 18b. Overshoot is less than 2%. Notice that the DTR filter has no effect on the sinewave.




A. CONVENTIONAL FILTER B. DTR FILTER

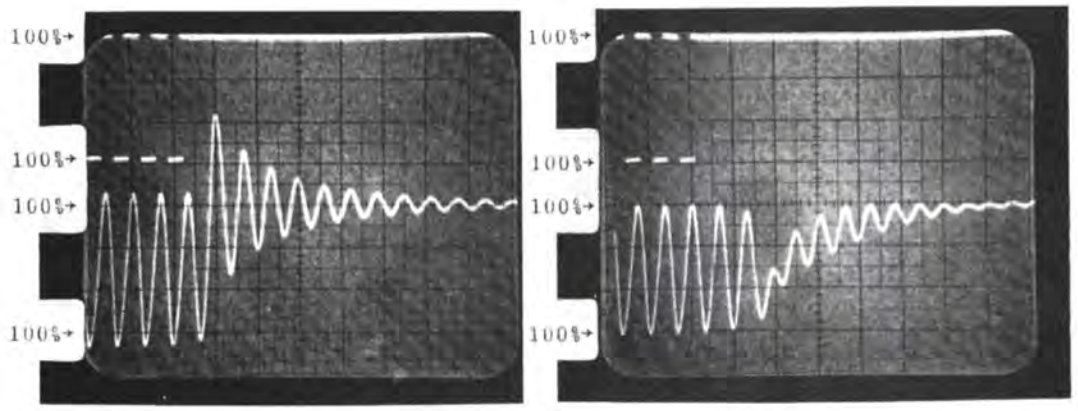
TOP TRACE: INPUT
BOTTOM TRACE: OUTPUT

SINE/STEP TESTS

FIGURE 18

It is possible to cause even more overshoot by substituting a squarewave for the sinewave part of the test signal of Fig. 18. Fig. 19a shows the resultant squarewave/ step test signal applied to a conventional filter which overshoots 150%, or 8 dB!

The response of the DTR filter to the same test signal is shown in Fig. 19b.




A. CONVENTIONAL FILTER B. DTR FILTER

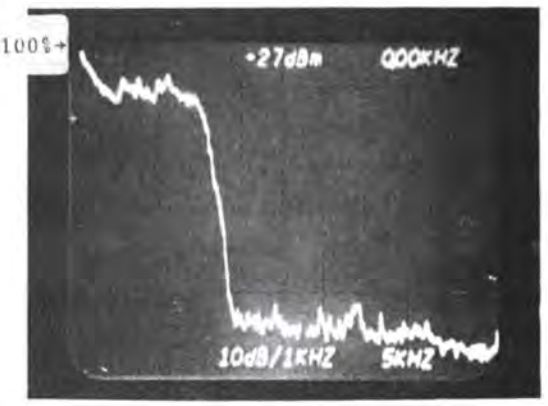
TOP TRACE: INPUT
BOTTOM TRACE: OUTPUT

SQUAREWAVE/STEP TESTS
FIGURE 19

This kind of signal is not uncommon with many types of limiters. Bass note attacks simultaneous with sibilance have been known to cause 100% overshoots when processed by a clipping-type limiter.

**DYNAMIC SPECTRUM**: Fig. 20 shows the output spectrum of the DTR filter under near "worst case" programming conditions. The input signal had extreme high frequency content, and was processed by several limiters, the last being a hard clipper. The spectrum analyzer, a Tektronix 7L5, is equipped with a microprocessor and memory which was used to produce a mixiumum-hold display.

FIGURE 20
DYNAMIC SPECTRUM




Over a 3 minute period the output spectrum of the DTR filter was continuously monitored; each time that a frequency contained more energy than previously, the display would be updated. Therefore, the display of Fig. 20 does not represent a typical instantaneous spectrum but rather the maximum spectral amplitude reached over a 3 minute period.

**CONCLUSION**: It has been shown that the DTR filter is a universally effective method for eliminating overmodulation due to overshoot. Because the compensator takes action **only** when necessary to remove low-energy overshoots, there is no audible distortion under any conditions. Because the compensated filter stands alone, a "systems approach" is not required; any FM limiter may be used.

A typical procedure for setting FM modulation levels has been to apply a sinewave through the program limiter at 100% modulation. A sinewave signal will not cause overshoot. Upon application of programming, the exciter filters will overshoot. With programming the modulation level must be reduced 2.5 to 6 dB to ensure that "peaks of frequent recurrence" do not cause overmodulation. With the Harris MS-15 exciter this last step of turning down the modulation has been eliminated.

The amount of loudness increase is a function of limiter type. The amount of overshoot that a limiter causes in a conventional filter is the amount of overshoot that is eliminated by the DTR filter. This same amount of overshoot is the increase in loudness that can be obtained. Some limiters, due to their excessive rolloff of highs, may only cause overshoots of 35% (2.6 dB). Other limiters, which rely more exclusively on clipping for pre-emphasis protection, can cause 100% overshoots (6 dB). Processors which rely upon a combination of clipping and rolloff will benefit from an intermediate loudness increase.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