AX2/7 SYSTEM DIAGRAM

AMD Smarter Choice

01

DDR3-SODIMM1 PAGE 6

DDR3-SODIMM2 PAGE 7

DDR3 channel A

DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)35W/25W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

HT3

PCI-E

PCI-Express 16X

NORTH BRIDGE
RS880M A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

HDMI PAGE 25

CRT PAGE 24

LVDS PAGE 23

ATI PARK-LP
23mm X 23mm
PAGE 17,18,19 20,21

DDR3

VRAM PAGE 22

Side port

DDR3 RAM for UMA only PAGE 8

X1

LAN
Realtek
PCIE-LAN
RTL8103E
(10/100)
PAGE 30

X1

Mini PCI-E Card
(Wireless LAN)
PAGE 33

RJ45 PAGE 30

ALINK X4

SOUTH BRIDGE
SB820 A12
21mm X 21mm, 605pin FCBGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13,14,15,16

SATA - HDD PAGE 29

SATA0 150MB

SATA - CD-ROM PAGE 29

SATA4 150MB

USB2.0

0,5,8 USB2.0 Ports X3 PAGE 29

15 BT softbreeze PAGE 29

2 Webcam X1 PAGE 23

3 Flash Media RTS5159 PAGE 26

10 PCI-E WLAN Card x1 PAGE 33

Azalia

MDC CONN PAGE 28

RJ11

Realtek ALC270-GR PAGE 27

Ang MIC PAGE 27

AUDIO CONN (Phone/ MIC) PAGE 28

LPC

ENE KBC
KB3926 Dx
PAGE 32

Keyboard PAGE 31
Touch Pad PAGE 31

FAN PAGE 28

SPI PAGE 31

SYSTEM CHARGER(ISL6251) PAGE 40

SYSTEM POWER ISL6237 PAGE 34

DDR II SMDDR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37

VCCP +1.1V AND +1.2V(RT8204) PAGE 35

VGACORE(1.1V~1.2V)Oz8118 PAGE 38

CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE

SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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PV,delete all external clock GEN reserve material

VLDT use 1.5A Max current

+1.1V — R164 *0_6/S — +1.1V_VLDT

+1.1V — R83 *0_6/S — +1.1V_VLDT_R

+2.5V — L34 BLM21PG221SN1D(220,100M,2A)_8 — +CPUVDDA

W/S= 15 mil/20mil

C418 4.7U/6.3V_6 LS0805-100M-N C392 4.7U/6.3V_6 C302 0.22U/25V_6 C304 3300P/50V_4

U21A

HT LINK

SOCKET_638_PIN

C396 10U/6.3V_8 C390 0.22U/6.3V_4 C389 180P/50V_4

+1.1V_VLDT_R 10U/6.3V_8 C99
+1.1V_VLDT_R 0.22U/6.3V_4 C113
+1.1V_VLDT_R 180P/50V_4 C120
+1.1V_VLDT_R 10U/6.3V_8 C594

8 HT_NB_CPU_CAD_H[15..0] — HT_NB_CPU_CAD_H[15..0]
8 HT_NB_CPU_CAD_L[15..0] — HT_NB_CPU_CAD_L[15..0]
8 HT_NB_CPU_CLK_H[1..0] — HT_NB_CPU_CLK_H[1..0]
8 HT_NB_CPU_CLK_L[1..0] — HT_NB_CPU_CLK_L[1..0]
8 HT_NB_CPU_CTL_H[1..0] — HT_NB_CPU_CTL_H[1..0]
8 HT_NB_CPU_CTL_L[1..0] — HT_NB_CPU_CTL_L[1..0]
8 HT_CPU_NB_CAD_H[15..0] — HT_CPU_NB_CAD_H[15..0]
8 HT_CPU_NB_CAD_L[15..0] — HT_CPU_NB_CAD_L[15..0]
8 HT_CPU_NB_CLK_H[1..0] — HT_CPU_NB_CLK_H[1..0]
8 HT_CPU_NB_CLK_L[1..0] — HT_CPU_NB_CLK_L[1..0]
8 HT_CPU_NB_CTL_H[1..0] — HT_CPU_NB_CTL_H[1..0]
8 HT_CPU_NB_CTL_L[1..0] — HT_CPU_NB_CTL_L[1..0]

FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

CPU CLK

12 CPUCLKP — CPUCLKP
12 CPUCLKN — CPUCLKN

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

CPUCLKIN R149 169/F_4 CPUCLKIN#
CPUCLKP C402 3900P/25V_4 CPUCLKIN
CPUCLKN C401 3900P/25V_4 CPUCLKIN#

H_THRMDC 5
H_THRMDA 5

CPU_PWRGD 300_4 R146
CPU_LDT_RST# 300_4 R148
CPU_LDT_STOP# 300_4 R166
CPU_LDT_REQ# CPU *300/F_4 R144 +1.5V

+CPUVDDA 250mA

W/S= 15 mil/20mil

U21D

SOCKET_638_PIN

12 CPU_LDT_RST#
12 CPU_PWRGD
10,12 CPU_LDT_STOP#
CPU_LDT_REQ# CPU C6

SideBand Temp sense I2C

5 CPU_SIC
5 CPU_SID
5 CPU_ALERT

+1.5VSUS — R163 510/F_4 — CPUTEST25H — CPUTEST25L — R162 510/F_4

+1.1V_VLDT — R114 44.2/F_4 R115 44.2/F_4 — CPU_HTREF0 CPU_HTREF1 — place them to CPU within 1.5"

36 CPU_VDD0_RUN_FB_H
36 CPU_VDD0_RUN_FB_L
36 CPU_VDD1_RUN_FB_H
36 CPU_VDD1_RUN_FB_L

CPU_DBRDY CPU_TMS CPU_TCK CPU_TRST# CPU_TDI

T7 CPUTEST23 AD7
T26 CPUTEST18 H10
T30 CPUTEST19 G9
CPUTEST25H E9
CPUTEST25L E8
place them to CPU within 1.5"
T127 CPUTEST21 AB8
CPUTEST20 AE7
CPUTEST24 AE7
T8 CPUTEST22 AE8
T6 CPUTEST12 AC8
CPUTEST27 AF8

R157 *0_4/S C2 AA6

+1.5VSUS — R172 300/F_4 CPU_DBREQ# — R338 1K/F_4 CPUTEST27 — R339 *300/F_4

CPU_VDDNB_RUN_FB_H 36
CPU_VDDNB_RUN_FB_L 36

CPU_DBREQ#
CPU_TDO

T37 T38 T29 T49

R156 *300/F_4 +1.1V_VLDT

T46 R130 80.6/F_4 T45

Route as 80ohm, diff

MV can remove reserve for debug

+1.5VSUS — R207 10K/F_4 CNTR_VREF — Q19 MMBT3904 — CPU_LDT_RST# — CPU_LDT_RST_HTPA# — +3V — R186 1K/F_4

Serial VID

+1.5VSUS — R170 *1K/F_4 — +1.5V — R171 *1K/F_4

R189 1K/F_4 R190 1K/F_4 — +1.5VSUS +1.5V

CPU_SVC_R R176 0_4 CPU_SVC
CPU_SVD_R R175 0_4 CPU_SVD
CPU_PWRGD R177 0_4 CPU_PWRGD_SVID_REG

CPU_SVC 36
CPU_SVD 36
CPU_PWRGD_SVID_REG 36

R184 *220_4
R183 *220_4
R185 *220_4

VFIX MODE — VID Override table (VDD)

SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

CPUTEST20 R340 1K/F_4
CPUTEST21 R81 1K/F_4
CPUTEST22 R80 1K/F_4
CPUTEST24 R69 1K/F_4

HDT Connector

+1.5VSUS — R224 10K/F_4 — R225 300_4

CPU_PROCHOT_L# R205 0_4 — Q22 MMBT3904 — R219 0_4

32 CPU_PROCHOT# — CPU_PROCHOT_R# — CPU_PROCHOT_R 12

EC new option

SI , add R205 for P-state implement

+1.5VSUS — R181 10K/F_4 — R180 1K/F_4 — Q18 MMBT3904

5 CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — CPU_THERMTRIP# 13

CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO

C74 *0.1U/10V_4

KEY

CN6 *HDT CONN

CPU_LDT_RST_HTPA#

CPUTEST12 R70 1K/F_4
CPUTEST19 R124 1K/F_4
CPUTEST18 R125 1K/F_4

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G4 HT,CTL I/F 1/3	1A

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Processor Memory Interface

04

VDDR = 0.9V for 25W & 35W CPU

VDDR = 1.05V for 35V & 45W CPU

PLACE THEM CLOSE TO CPU WITHIN 1"

PV,change to short pad

SI , change from 0.01u to 0.1u from AMD recommand

Place close to socket

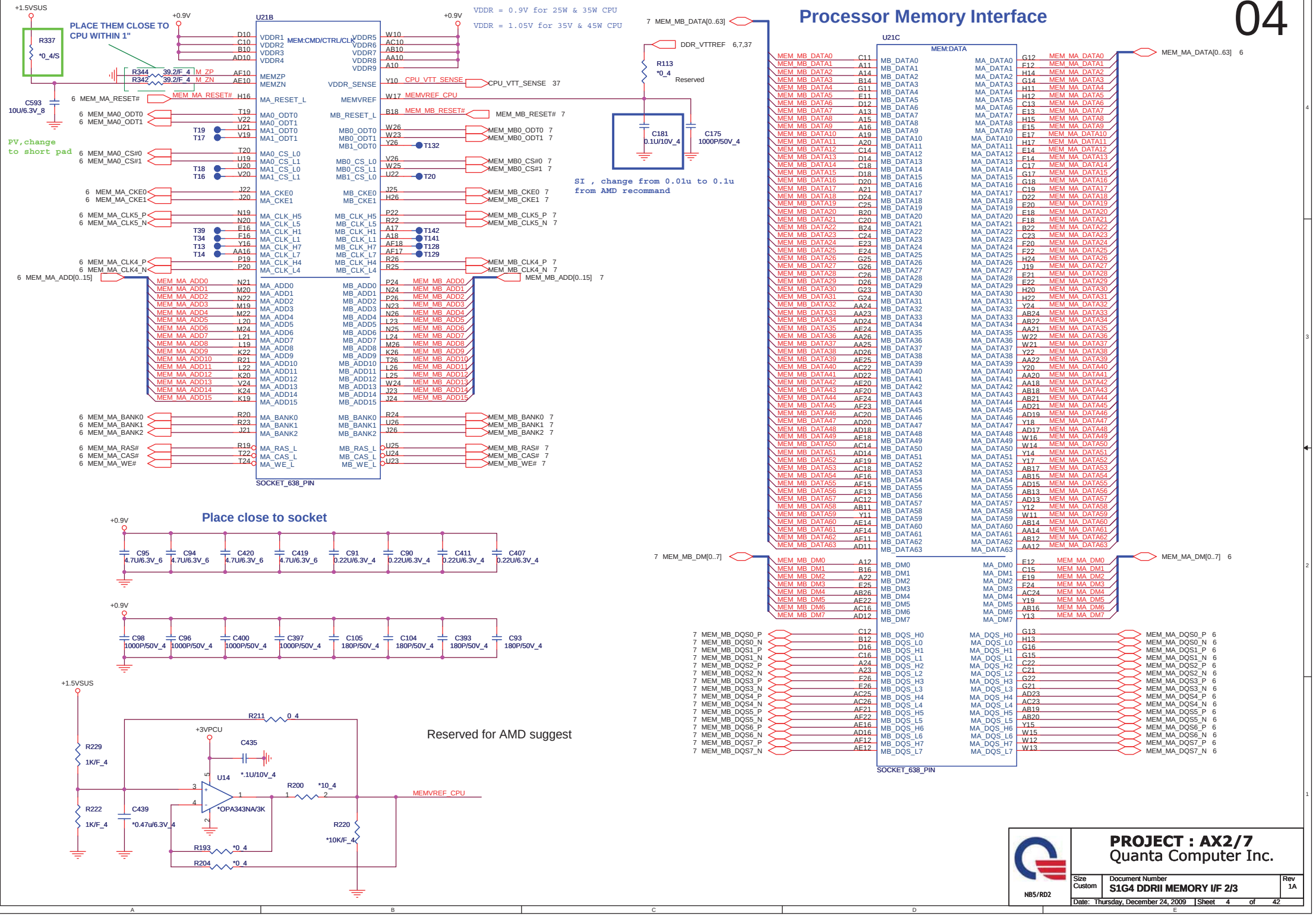
Reserved for AMD suggest

U21B MEM:CMD/CTRL/CLK

SOCKET_638_PIN

U21C MEM:DATA

SOCKET_638_PIN



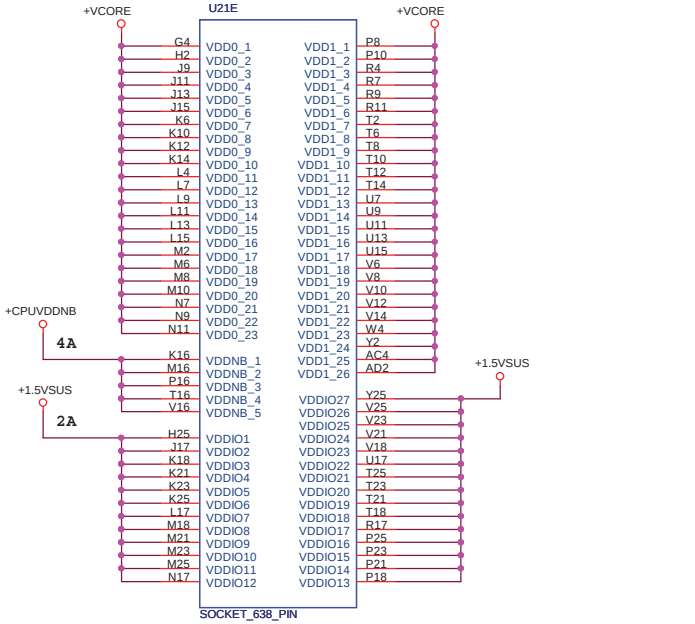
NB5/RD2

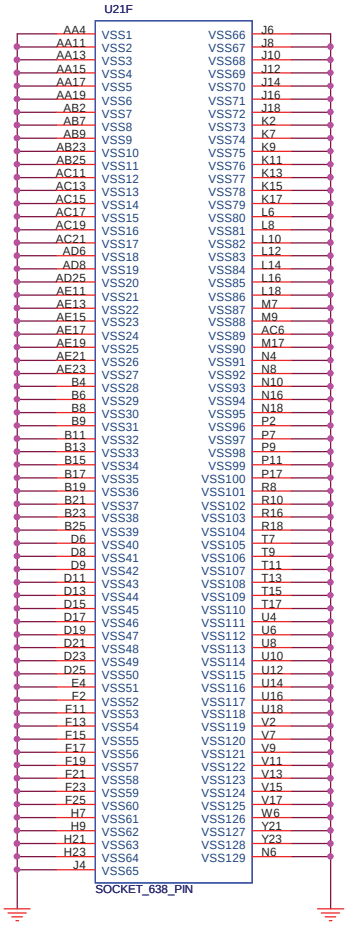
PROJECT : AX2/7
Quanta Computer Inc.

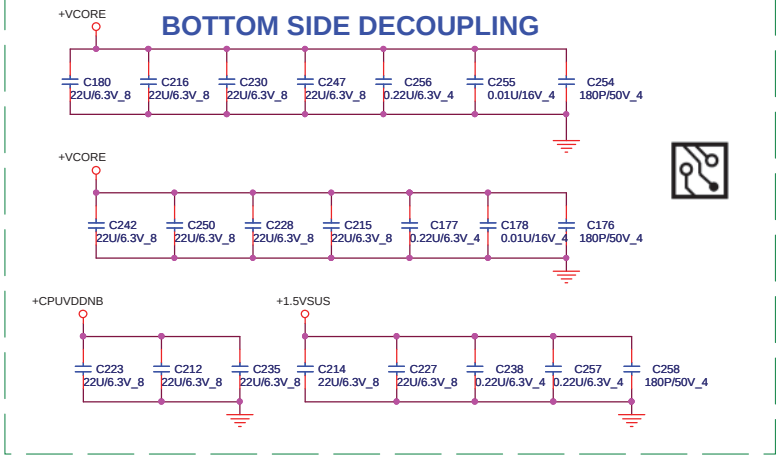
Size	Document Number	Rev
Custom	S1G4 DDRII MEMORY I/F 2/3	1A

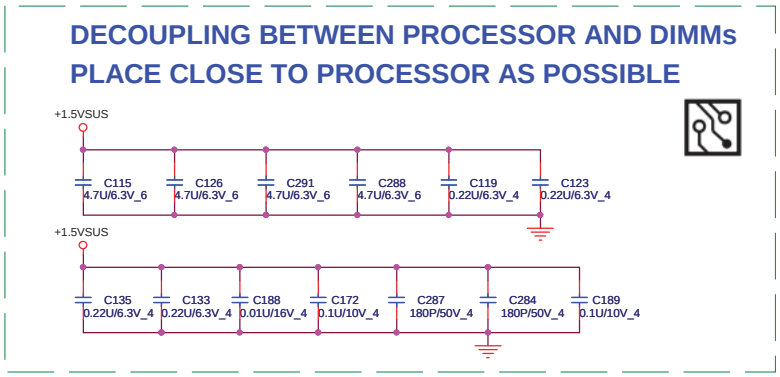
Date: Thursday, December 24, 2009 Sheet 4 of 42

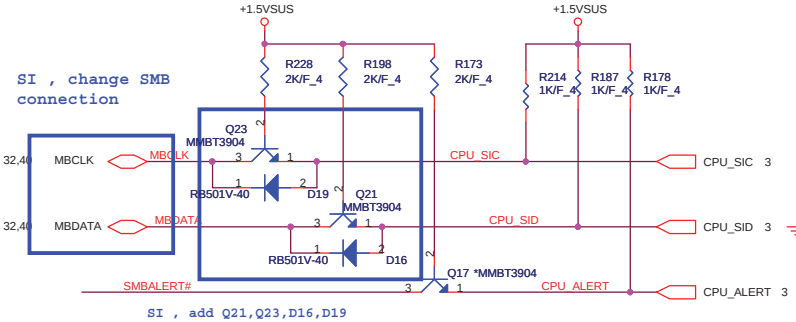
PROCESSOR POWER AND GROUND

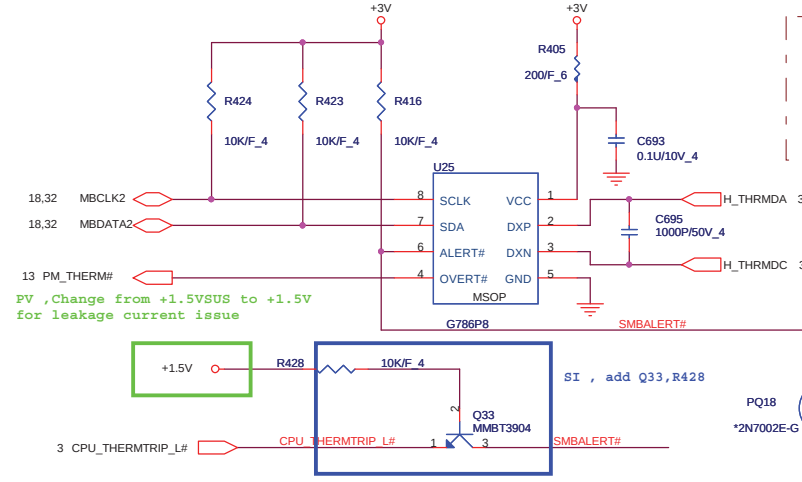


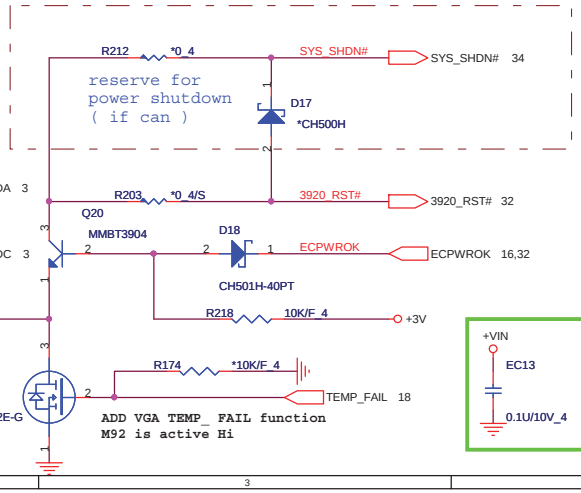


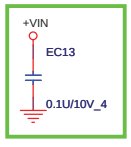




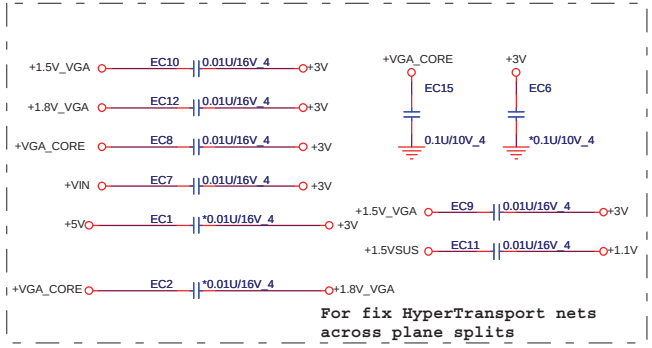




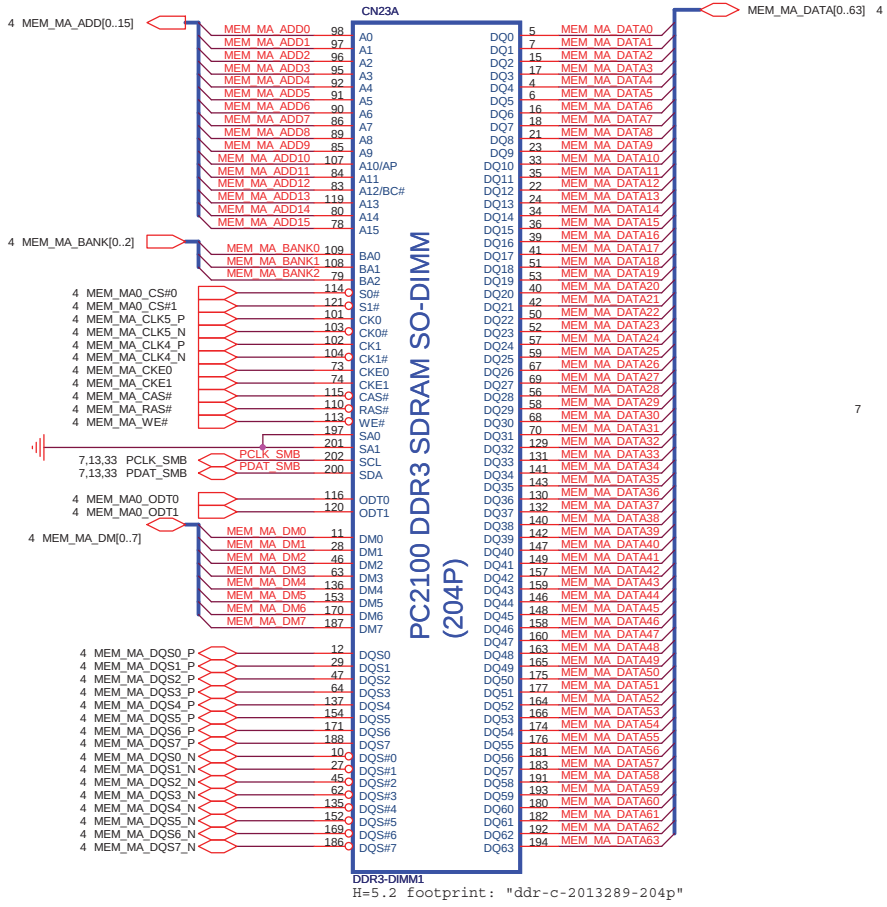


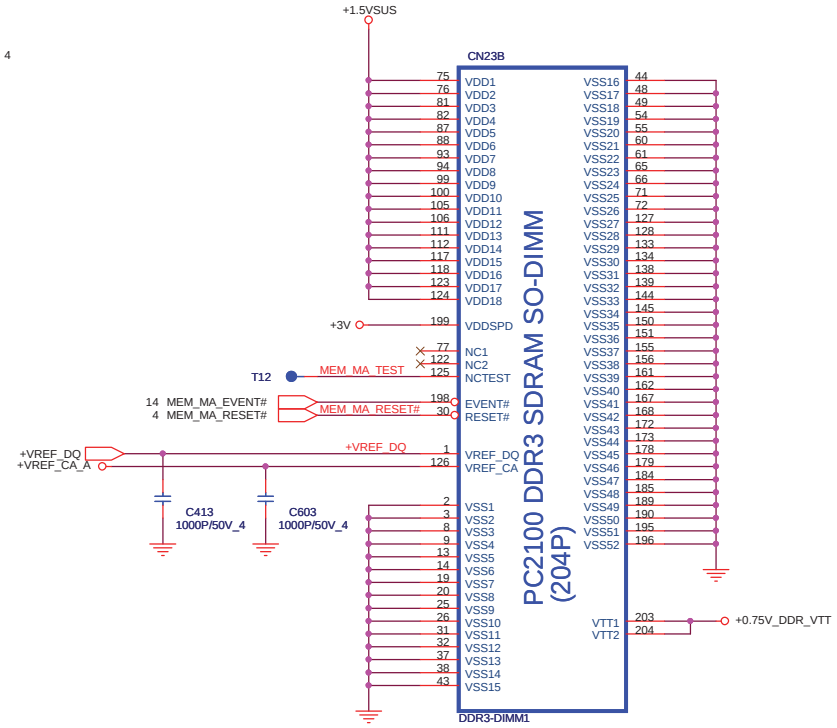


PV,add for EMI suggest



NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.		
	Size: Custom	Document Number: S1G4 PWR & GND 3/3	Rev: 1A
	Date: Thursday, December 24, 2009	Sheet 5 of 42	

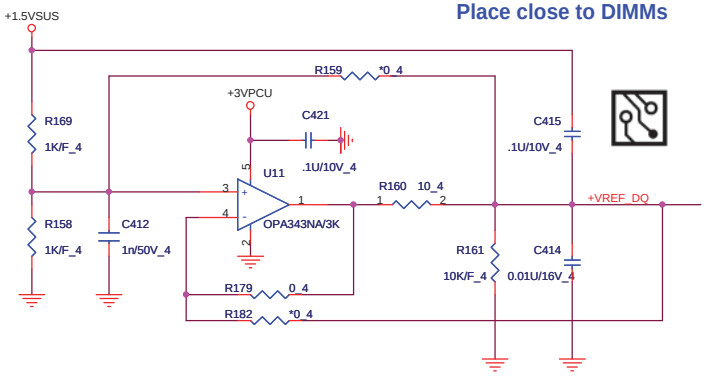




SO-DIMM BYPASS PLACEMENT :

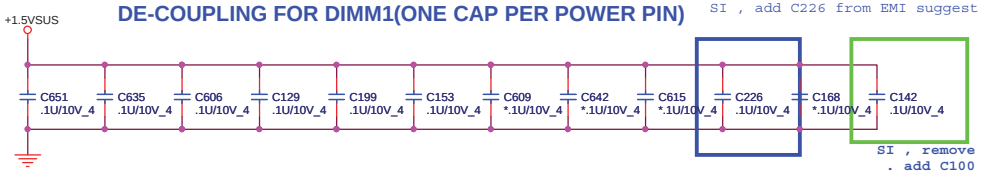
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.



DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

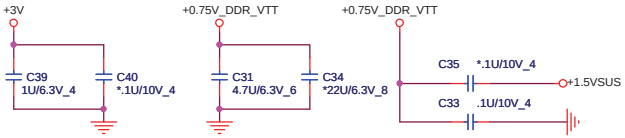
SI , add C226 from EMI suggest

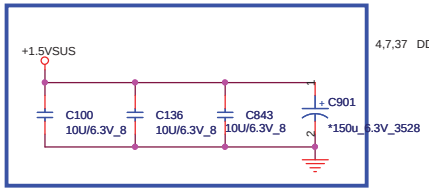


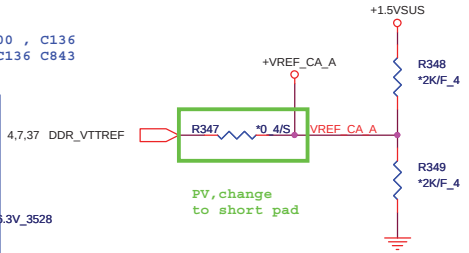
PV,add from EMI suggestion

SI , remove C100 , C136
. add C100 , C136 C843
Reserve C901

DE-COUPLING FOR DIMM1







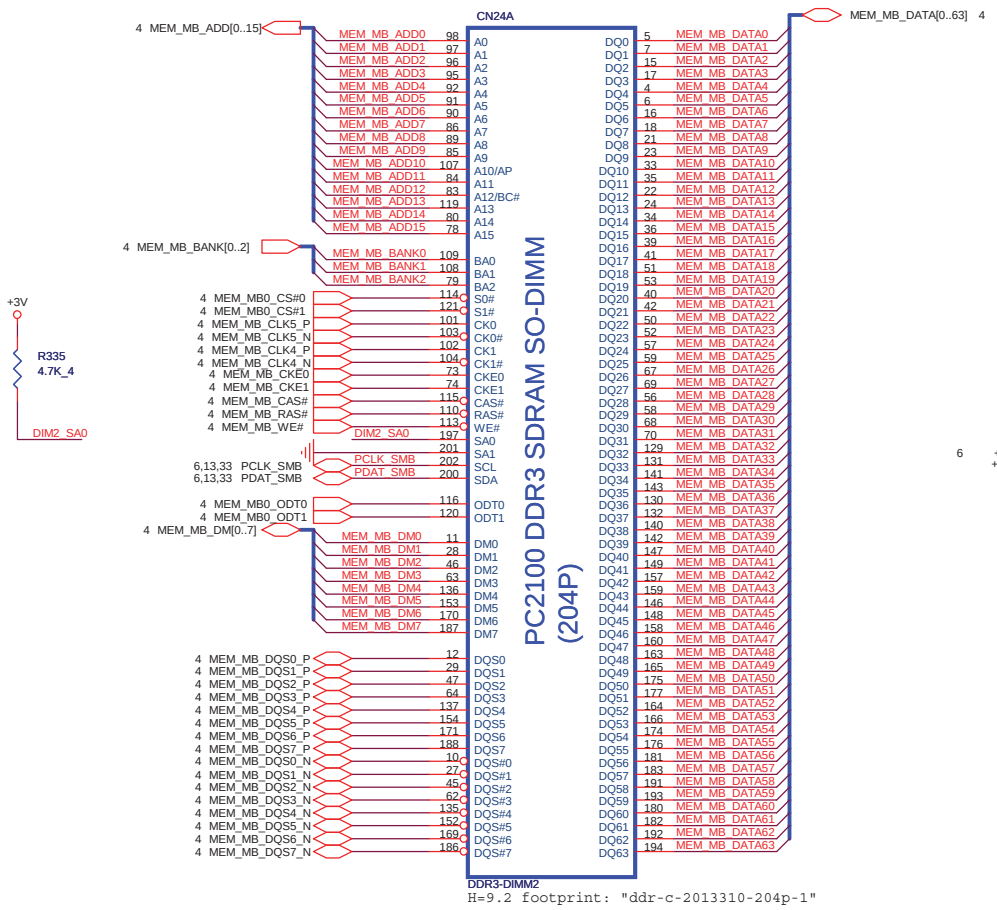
PV,change
to short pad

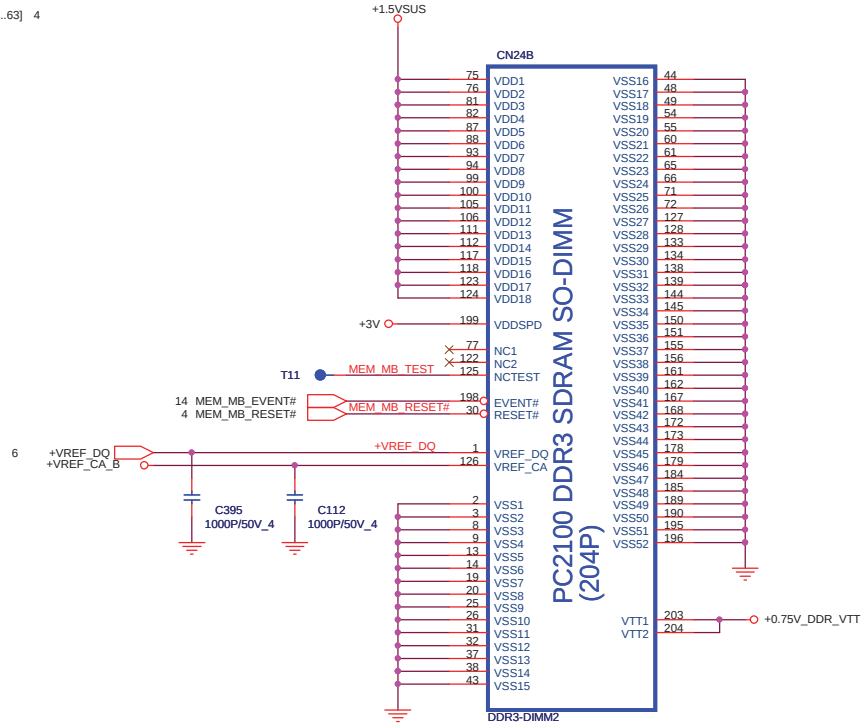
PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SODIMMS: A/B CHANNEL	1A

Date: Thursday, December 24, 2009 | Sheet 6 of 42

NB5/RD2



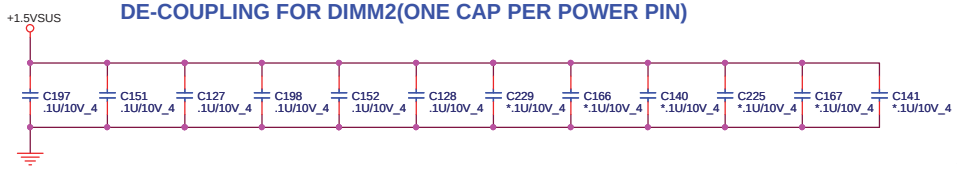


SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

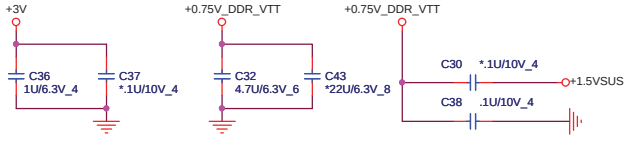
No Vias Between the Trace of PIN to CAP.

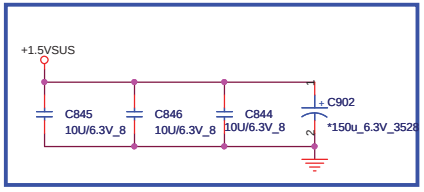
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)

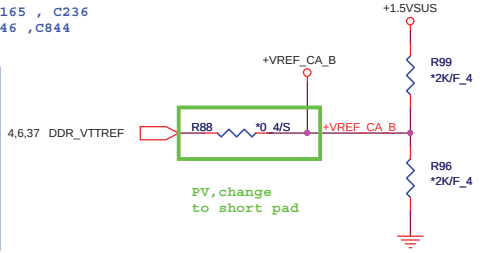


SI , remove C165 , C236
add C845 , C846 ,C844
Reserve C902

DE-COUPLING FOR DIMM2







NB5/RD2	**PROJECT : AX2/7** Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 SODIMMS TERMINATIONS	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 7 of 42	

HT_CPU_NB_CAD_H[15..0] — HT_CPU_NB_CAD_H[15..0] 3
HT_CPU_NB_CAD_L[15..0] — HT_CPU_NB_CAD_L[15..0] 3
HT_CPU_NB_CLK_H[1..0] — HT_CPU_NB_CLK_H[1..0] 3
HT_CPU_NB_CLK_L[1..0] — HT_CPU_NB_CLK_L[1..0] 3
HT_CPU_NB_CTL_H[1..0] — HT_CPU_NB_CTL_H[1..0] 3
HT_CPU_NB_CTL_L[1..0] — HT_CPU_NB_CTL_L[1..0] 3
HT_NB_CPU_CAD_H[15..0] — HT_NB_CPU_CAD_H[15..0] 3
HT_NB_CPU_CAD_L[15..0] — HT_NB_CPU_CAD_L[15..0] 3
HT_NB_CPU_CLK_H[1..0] — HT_NB_CPU_CLK_H[1..0] 3
HT_NB_CPU_CLK_L[1..0] — HT_NB_CPU_CLK_L[1..0] 3
HT_NB_CPU_CTL_H[1..0] — HT_NB_CPU_CTL_H[1..0] 3
HT_NB_CPU_CTL_L[1..0] — HT_NB_CPU_CTL_L[1..0] 3

U22A

HYPER TRANSPORT CPU I/F — PART 1 OF 6

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1
		HT_RXCALP	HT_TXCALP	B24	HT_TXCALP
		HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

R412 301/F_4 HT_RXCALP — HT_RXCALN
R411 301/F_4 HT_TXCALP — HT_TXCALN

RS880

signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

U18

SPM_VREF1 M9 — VREFCA
SPM_VREF2 H2 — VREFDQ

SPM_A0	N4	A0	DQL0	E4	SPM_DQ2
SPM_A1	P8	A1	DQL1	F8	SPM_DQ1
SPM_A2	P4	A2	DQL2	F3	SPM_DQ5
SPM_A3	N3	A3	DQL3	F9	SPM_DQ3
SPM_A4	P9	A4	DQL4	H4	SPM_DQ7
SPM_A5	P3	A5	DQL5	H9	SPM_DQ0
SPM_A6	R9	A6	DQL6	G3	SPM_DQ4
SPM_A7	R3	A7	DQL7	H8	SPM_DQ6
SPM_A8	T9	A8	DQU0	D8	SPM_DQ13
SPM_A9	R4	A9	DQU1	C4	SPM_DQ8
SPM_A10	L8	A10/AP	DQU2	C9	SPM_DQ10
SPM_A11	R8	A11	DQU3	C3	SPM_DQ12
SPM_A12	N8	A12/BC	DQU4	A8	SPM_DQ15
SPM_A13	T4	A13	DQU5	A3	SPM_DQ11
	T8	A14	DQU6	B9	SPM_DQ14
	M8	A15	DQU7	A4	SPM_DQ9

SPM_BA0 M3 — BA0
SPM_BA1 N9 — BA1
SPM_BA2 M4 — BA2

SPM_CLKP J8 — CK
SPM_CLKN K8 — CK
SPM_CKE K10 — CKE

SPM_ODT K2 — ODT
SPM_CS# L3 — CS
SPM_RAS# J4 — RAS
SPM_CAS# K4 — CAS
SPM_WE# L4 — WE

SPM_DQS0P F4 — DQSL
SPM_DQS1P C8 — DQSU

SPM_DM0 E8 — DML
SPM_DM1 D4 — DMU

SPM_DQS0N G4 — DQSL
SPM_DQS1N B8 — DQSU

13 SP_DDR3_RST# — T3 RESET

VMA_ZQ2 L9 — ZQ

		VDD#B3	B3
		VDD#D10	D10
		VDD#G8	G8
		VDD#K3	K3
		VDD#K9	K9
		VDD#N2	N2
		VDD#N10	N10
		VDD#R2	R2
		VDD#R10	R10
		VDDQ#A2	A2
		VDDQ#A9	A9
		VDDQ#C2	C2
		VDDQ#C10	C10
		VDDQ#D3	D3
		VDDQ#E10	E10
		VDDQ#F2	F2
		VDDQ#H3	H3
		VDDQ#H10	H10
		VSS#A10	A10
		VSS#B4	B4
		VSS#E2	E2
		VSS#G9	G9
		VSS#J3	J3
		VSS#J9	J9
		VSS#M2	M2
		VSS#M10	M10
		VSS#P2	P2
		VSS#P10	P10
		VSS#T2	T2
		VSS#T10	T10
		VSSQ#B2	B2
		VSSQ#B10	B10
		VSSQ#D2	D2
		VSSQ#D9	D9
		VSSQ#E3	E3
		VSSQ#E9	E9
		VSSQ#F10	F10
		VSSQ#G2	G2
		VSSQ#G10	G10

NC#J2 J2
NC#L2 L2
NC#J10 J10
NC#L10 L10

100-BALL SDRAM DDR3
*H5TQ1G63AFR-14C

+1.5V_MEM_VDDQ

SI,exchange net name

R95 *100_4

R343 *10K/F_4

R91 *243/F_4

R73 *1K/F_4 R75 *1K/F_4 C85 *0.1U/10V_4 C77 *0.1U/10V_4 +1.5V_MEM_VDDQ
SPM_VREF1

R100 *1K/F_4 R101 *1K/F_4 C121 *0.1U/10V_4 C138 *0.1U/10V_4 +1.5V_MEM_VDDQ
SPM_VREF2

This block is for UMA only , DIS can remove all component

U22D

SBD_MEM/DVO_I/F — PAR 4 OF 6

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22	SPM_DQ10
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18	SPM_DQ11
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22	SPM_DQ13
T21			MEM_DQ14/DVO_D10(NC)	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)			
SPM_BA2	AD17	MEM_BA2(NC)			
			MEM_DQS0P/DVO_IDCKP(NC)	Y17	SPM_DQS0P
			MEM_DQS0N/DVO_IDCKN(NC)	W18	SPM_DQS0N
SPM_RAS#	W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20	SPM_DQS1P
SPM_CAS#	Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21	SPM_DQS1N
SPM_WE#	AD18	MEM_WEb(NC)			
SPM_CS#	AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17	SPM_DM0
SPM_CKE	AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19	SPM_DM1
SPM_ODT	V14	MEM_ODT(NC)			
			IOPLLVDD18(NC)	AE23	+1.8V_IOPLLVDD18
SPM_CLKP	V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24	+1.1V_IOPLLVDD
SPM_CLKN	W14	MEM_CKN(NC)			
			IOPLLVSS(NC)	AD23	
R357 *40.2/F_4 SPM_COMPP	AE12	MEM_COMPP(NC)		AE18	SPM_VREF
R352 *40.2/F_4 SPM_COMPN	AD12	MEM_COMPN(NC)	MEM_VREF(NC)		

+1.5V_MEM_VDDQ

RS880

40mils wdith or more

+1.5V_MEM_VDDQ — R341 *0_6 — +1.5V

C86 *1U/10V_4 C71 *10U/6.3V_8 C66 *10U/6.3V_8
C84 *0.1U/10V_4 C92 *0.1U/10V_4 C87 *1U/10V_4

*PBY160808T-221Y-N L54 +1.8V
*PBY160808T-221Y-N L16 +1.1V

C630 *2.2U/6.3V_6 C146 *2.2U/6.3V_6

R356 *1K/F_4 R355 *1K/F_4
C619 *0.1U/10V_4 C620 *0.1U/10V_4 +1.5V_MEM_VDDQ

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	RS880-HT LINK I/F 1/5	1A

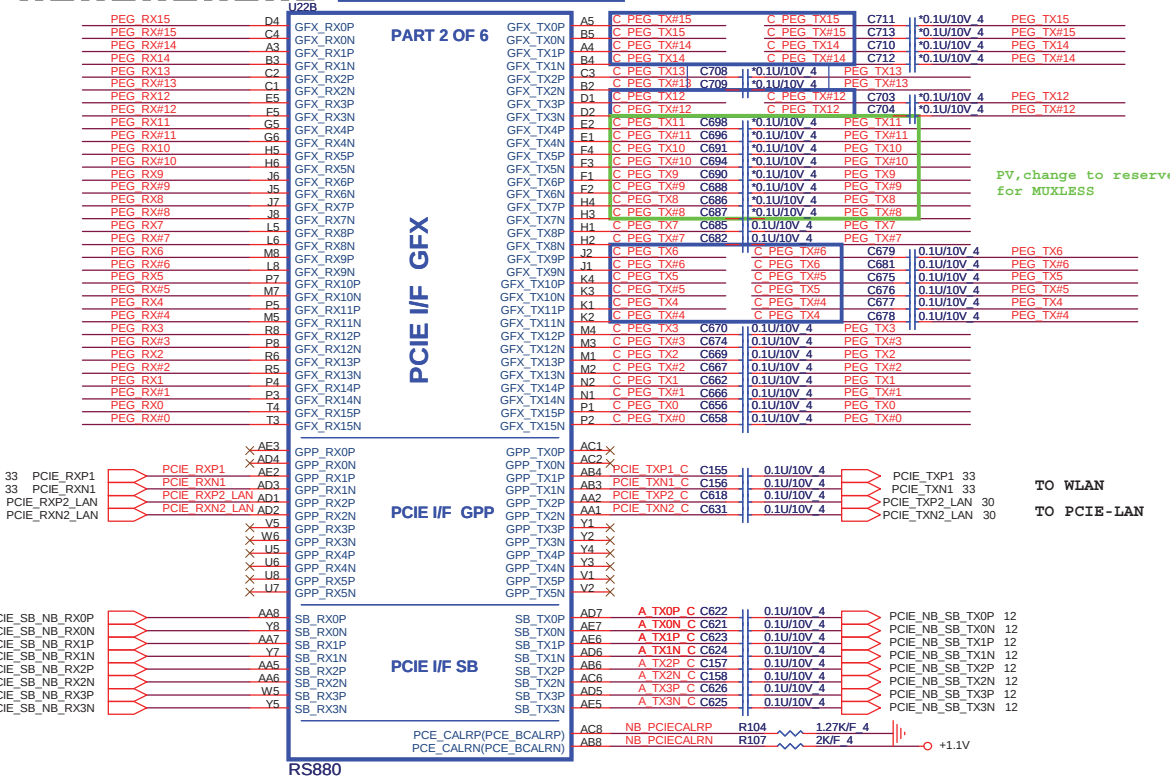
Date: Thursday, December 24, 2009 | Sheet 8 of 42

GFX_RX can remove
at next stage for MUXLESS

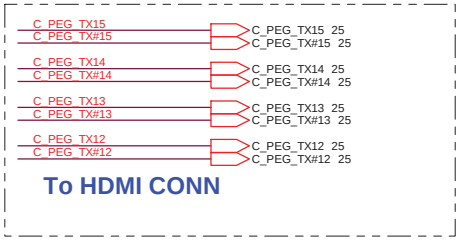
SI , for routing smooth
GFX_TX 0/1/3/9/10/11

UMA can remove all GFX_TX CAP

SI remove C711,C713,C710,
C712,C708,C709,C703,C704
for MUXLESS



Close to North Bridge



RS880 Display Port Support (muxed on GFX)

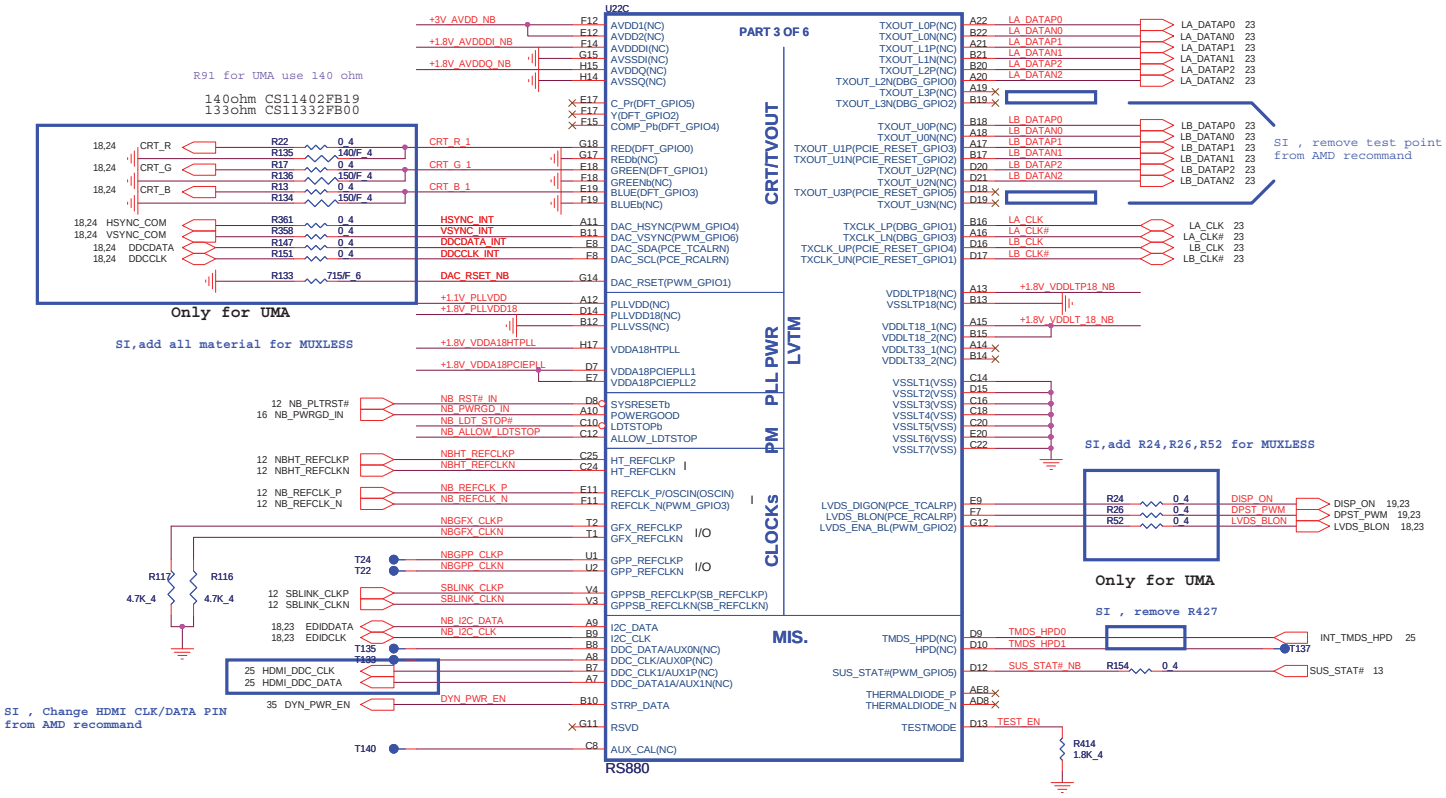
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

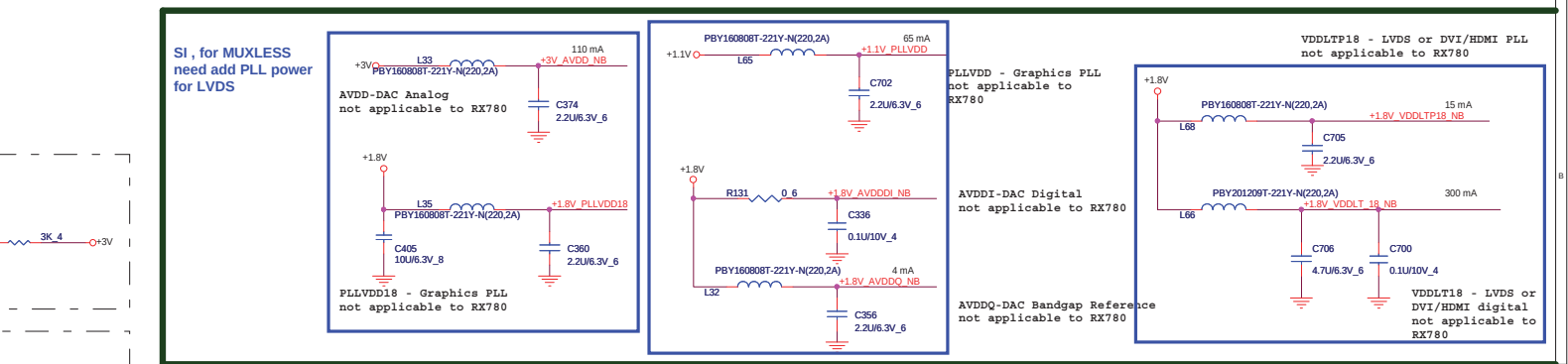
NB5/RD2

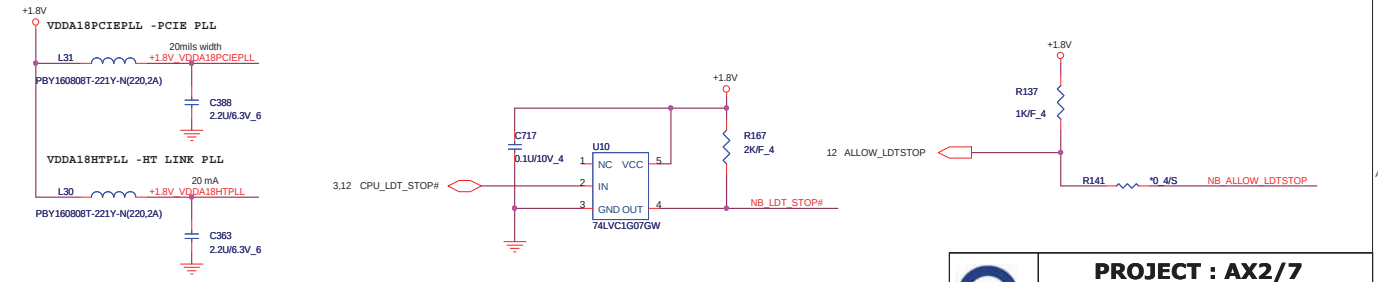
PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880-PCIE I/F 2/5	1A

Date: Thursday, December 24, 2009 | Sheet 9 of 42







STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable

RS880M: Enables Side port memory

RS880M:HSYNC#

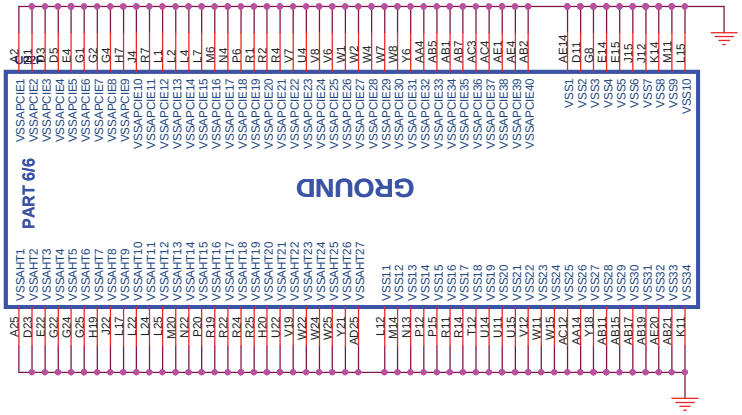
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

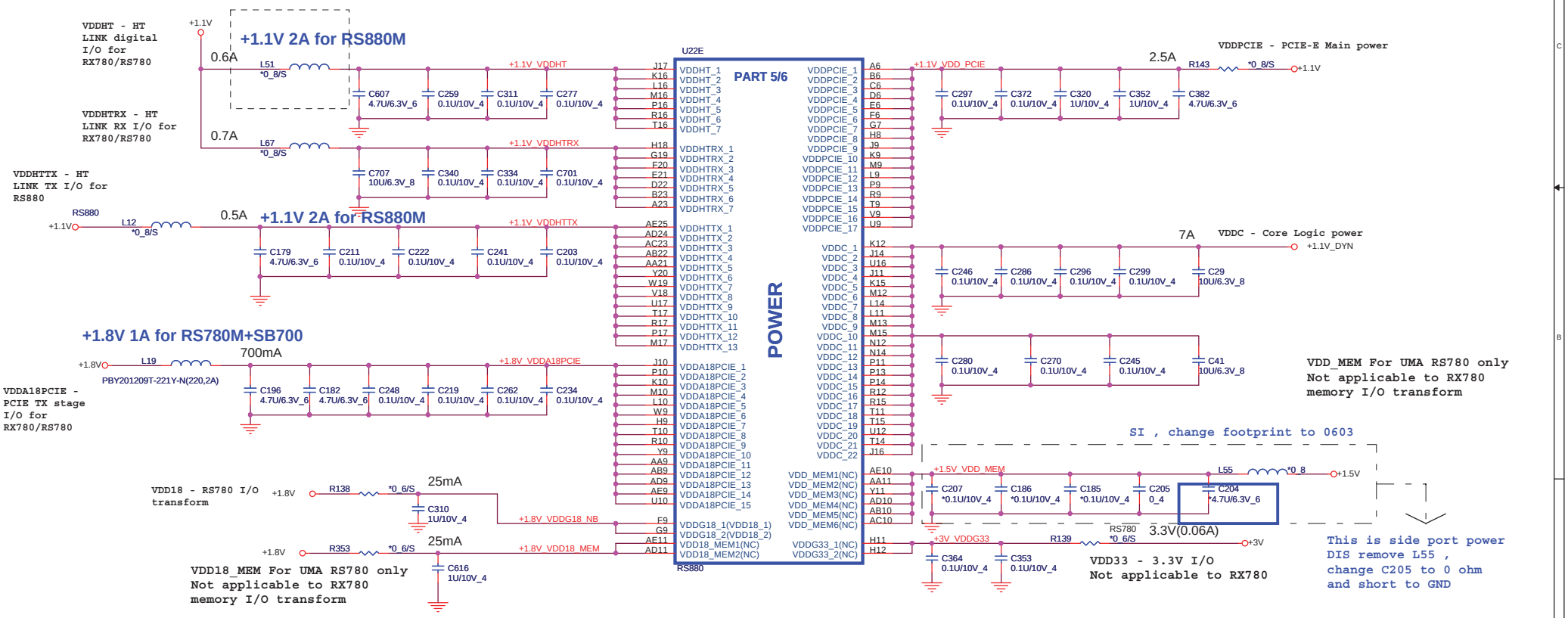
For external EEPROM Debug only

RS780/RX780

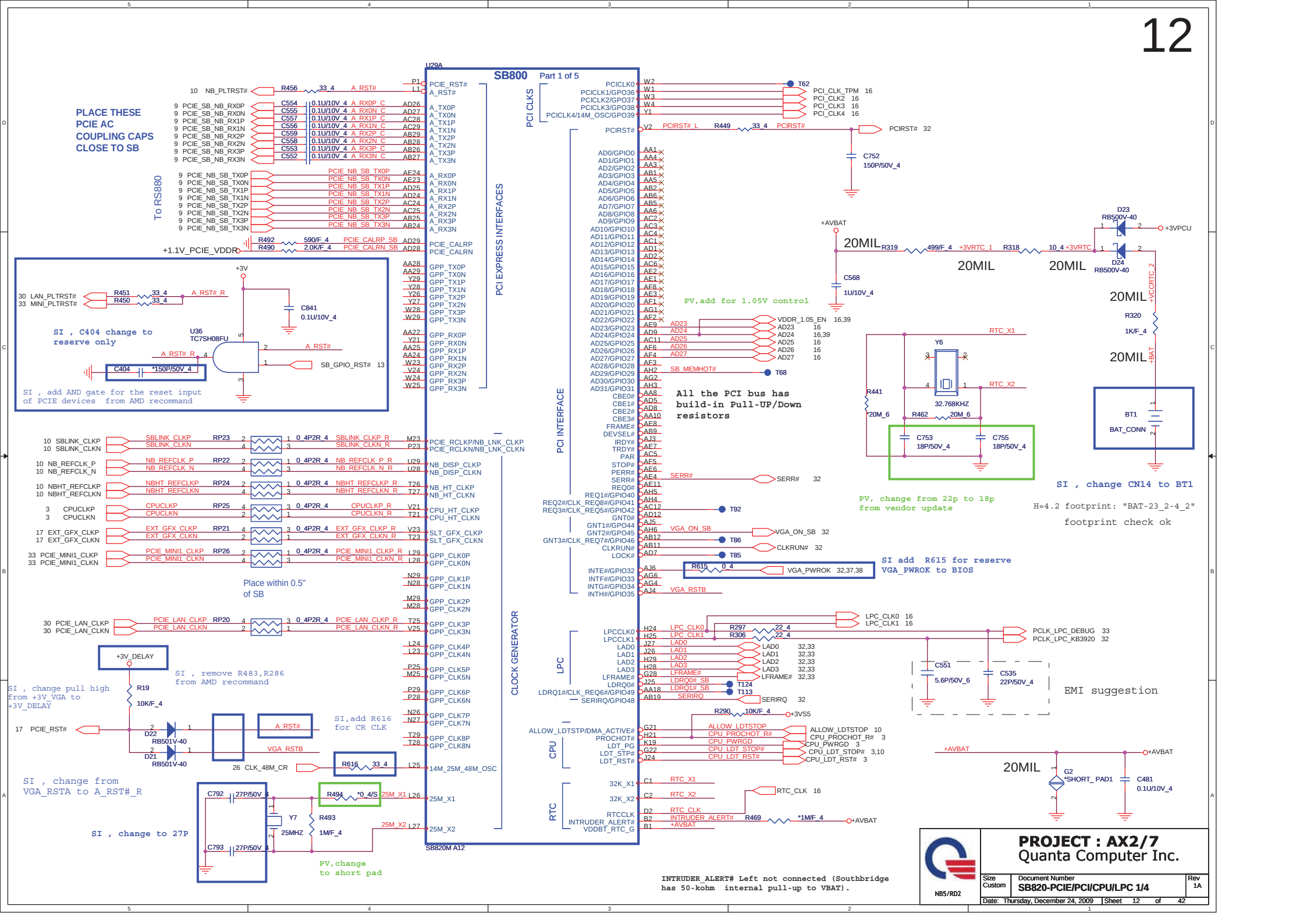
RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC





NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
	Size: Custom Document Number: RS880-POWER5/5	Rev: 1A
	Date: Tuesday, December 22, 2009	Sheet 11 of 42


SB800 Part 1 of 5
U29A
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB
To RS880
PCI EXPRESS INTERFACES
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
SI , C404 change to reserve only
SI , add AND gate for the reset input of PCIE devices from AMD recommand
Place within 0.5" of SB
SI , remove R483,R286 from AMD recommand
SI , change pull high from +3V_VGA to +3V_DELAY
SI,add R616 for CR CLK
SI , change from VGA_RSTA to A_RST#_R
SI , change to 27P
PV,change to short pad
PV,add for 1.05V control
All the PCI bus has build-in Pull-UP/Down resistors
PV, change from 22p to 18p from vendor update
SI , change CN14 to BT1
H=4.2 footprint: "BAT-23_2-4_2"
footprint check ok
SI add R615 for reserve VGA_PWROK to BIOS
EMI suggestion
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
SB820M A12
PROJECT : AX2/7
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number SB820-PCIE/PCI/CPU/LPC 1/4
Rev 1A
Date: Thursday, December 24, 2009 Sheet 12 of 42

NC,no install by default
+3VS5
R253 *2.2K_4 SB_TEST0
R470 *2.2K_4 SB_TEST1
R245 *2.2K_4 SB_TEST2
remove pull hi (chip internal have pull hi)

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it
R459 2.2K_4 SB_SMBCLK1
R460 2.2K_4 SB_SMBDATA1

SI , Add SB_GPIO_RST# form AMD recommand

+3V SCL0/SDATA0 is 3V tolerance AMD datasheet define it
R312 2.2K_4 PCLK_SMB
R311 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

30,33 PCIE_WAKE#
3 CPU_THERMTRIP#
16 WD_PWRGD
32 RSMRST#
C500 100P/50V_4

+3V
R561 10K/F_4
RB501V-40 D38
37 VGA_REQ
SI , add R561,D38 for VGA_CLK_REQ

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it
R296 2.2K_4 SB_SCLK2
R292 2.2K_4 SB_SDATA2
R576 *10K_4 SYS_RST#
PV,Reserve for system stable

+3VS5
R458 2.2K_4 DNBSWON#

+3V
R457 4.7K_4 SUS_STAT#
R332 8.2K_4 WLAN_CLKREQ#
R334 8.2K_4 LAN_CLKREQ#
SI , add from HP request

To Azalia

ACZ_SDOUT R247 33_4 C478 *10P/50V_4 ACZ_SDOUT_AUDIO 27
ACZ_SYNC R251 33_4 C484 *10P/50V_4 ACZ_SYNC_AUDIO 27
PV, change to 27P from EMI suggest
ACZ_BCLK R254 33_4 C479 27P/50V_4 BIT_CLK_AUDIO 27
ACZ_RST# R242 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27
Remove short pad

To Modem Board

ACZ_SDOUT R246 33_4 C477 *10P/50V_4 ACZ_SDOUT_AUDIO_MDC 28
ACZ_SYNC R248 33_4 C473 *10P/50V_4 ACZ_SYNC_AUDIO_MDC 28
ACZ_BCLK R256 33_4 C486 27P/50V_4 BIT_CLK_AUDIO_MDC 28
PV, change to 27P from EMI suggest
ACZ_RST# R249 33_4 ACZ_RST#_AUDIO_MDC 28
ACZ_SDIN1 ACZ_SDIN1 28
Remove short pad

EMI suggestion

R255 *10K/F_4
16 ACZ_SDOUT
HD audio interface is 3.3S5 voltage
R455 *10K/F_4 ACZ_SDIN0
R453 *10K/F_4 ACZ_SDIN1
R454 *10K/F_4 ACZ_SDIN2_R
R452 *10K/F_4 ACZ_SDIN3_R
ACZ_SYNC
ACZ_RST#

PV,change from pull high to pull low from AMD update
SI , add pull up resistor from AMD recommend
+3VS5
R483 10K/F_4
R505 10K/F_4
R509 10K/F_4
R511 10K/F_4
R545 10K/F_4

CN32
+3VSUS
C833 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
SB JTAG
*S/W JTAG DEBUG

R243 *0_4 SMBALERT# 1
R244 10K/F_4
5 PM_THERM#
+3VS5
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

R444 *0_4 LAN_DISABLE# SB

U29D
SB800
Part 4 of 5
SB820M A12

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQGG#/GPIO65/OSCIN
GPIO
USB 2.0

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
EMBEDDED CTRL

PV,remove workaround
A10 CLK_48M_USB
PV,delete R272
G19 USB_RCOMP_SB R291 11.8K/F_6
SI,add R272 for PARK LP 14M CLK source
CLK_48M_USB
C509 *2.2P/50V_4
for EMI

USB_FSD1P/GPIO186 J10 USBP15+ 29
USB_FSD1N H11 USBP15- 29 BLUETOOTH
USB_FSD0P/GPIO185 H9 T83
USB_FSD0N J8 T82
USB_HSD13P B12 T99
USB_HSD13N A12 T88
USB_HSD12P F11 T90
USB_HSD12N E11 T100
USB_HSD11P E14 USBP11+ 26
USB_HSD11N E12 USBP11- 26 USB card reader
USB_HSD10P J12 USBP10+ 33
USB_HSD10N J14 USBP10- 33 WLAN Min-Card
USB_HSD9P A13 T103
USB_HSD9N B13 T87
USB_HSD8P D13 T105
USB_HSD8N C13 T94
USB_HSD7P G12 T101
USB_HSD7N G14 T96
USB_HSD6P G16 USBP6+ 29
USB_HSD6N G18 USBP6- 29 USB Connector
USB_HSD5P D16 USBP5+ 29
USB_HSD5N C16 USBP5- 29 USB Connector
USB_HSD4P B14 T148
USB_HSD4N A14 T150
USB_HSD3P E18 T109
USB_HSD3N E16 T112
USB_HSD2P J16 USBP2+ 23
USB_HSD2N J18 USBP2- 23 Carama USB
USB_HSD1P B17 T107
USB_HSD1N A17 T149
USB_HSD0P A16 USBP0+ 29
USB_HSD0N B16 USBP0- 29 USB Connector

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_SCLK3
SDA3_LV/GPIO196 E26 5159_RST_R# T168 5159_RST_R# 26
EC_PWM2/EC_TIMER2/GPIO199 F22 SB_GPIO199 SB_GPIO199 16
EC_PWM3/EC_TIMER3/GPIO200 F21 SB_GPIO200 SB_GPIO200 16
SPI/LPC define

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	1A

Date: Thursday, December 24, 2009 | Sheet 13 of 42

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SI define side port ID

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

SATA1

SATA ODD

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

U29B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB820M A12

SI , remove test point from AMD recommand

PV,change to short pad

SI , change to reserve only

For blue tooth & wireless merge card

SI define board ID

ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	AX2 UMA DF
0	0	0	0	1	AX7 UMA DF
0	0	0	1	0	AX2 PARK DF
0	0	0	1	1	AX7 PARK DF
0	0	1	0	0	AX2 UMA FF
0	0	1	0	1	AX7 UMA FF
0	0	1	1	0	AX2 PARK FF
0	0	1	1	1	AX7 PARK FF
0	1	0	1	0	AX2 M93 DF
0	1	0	1	1	AX7 M93 DF
0	1	1	1	0	AX2 M93 FF
0	1	1	1	1	AX7 M93 FF

PV define for M93

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size: Custom | Document Number: SB820-ACPI/GPIO/USB 2/4 | Rev: 1A

Date: Thursday, December 24, 2009 | Sheet 14 of 42

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

SB800 Part 3 of 5 (U29C)

VDDQ--3.3V I/O power 131mA
VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power 71mA
Delete Cap and change +1.8V to pull low from AMD command , due to no IDE & flash mode
PCIE_VDDR--PCIE I/O power 600mA
93mA
AVDD_SATA--SATA phy power 567mA
AVDDTX--USB Phy Analog I/O power 658mA
TBDmA
510mA
VDD-- S/B CORE power
CKVDD_1.1V-- Internal clock Generator I/O power
TBDmA
32mA
S5_3.3--3.3v standby power
S5_1.1V--1.1V standby power 113mA
TBDmA
197mA
47mA
62mA
17mA
5mA
32mA

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

PV,change to short pad

For support USB wakeup-->3V_S5

SI , remove R272 from AMD recommand

SI , remove L48

To meet SB800 SCL1.02: Separate ferrite bead is not required for VDDPL_33_USB_S, Del B603/600ohm bead.

SB820M A12

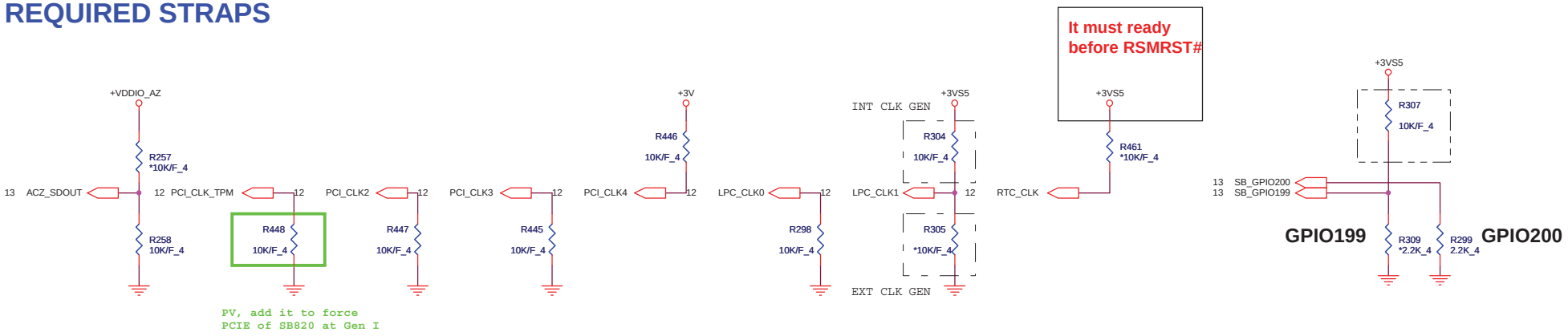
SB800 GROUND Part 5 of 5 (U29E)

SB820M A12

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

REQUIRED STRAPS

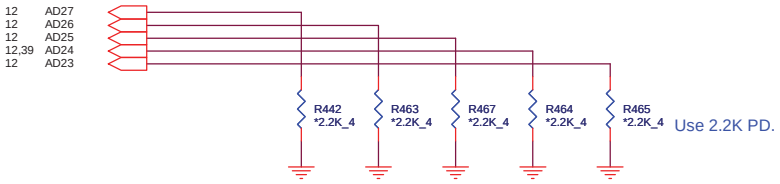


REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

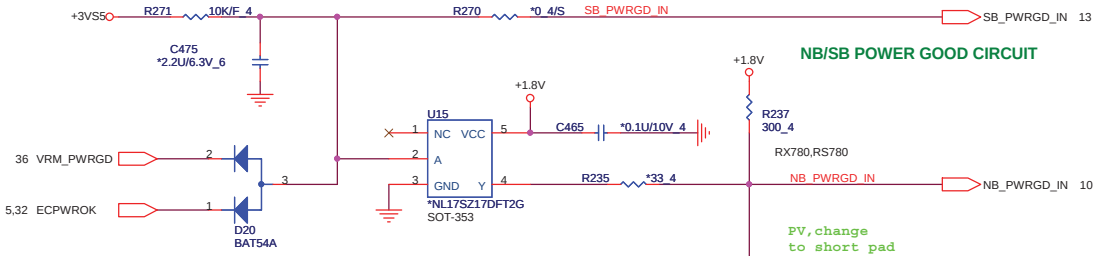
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-STRAPS	1A

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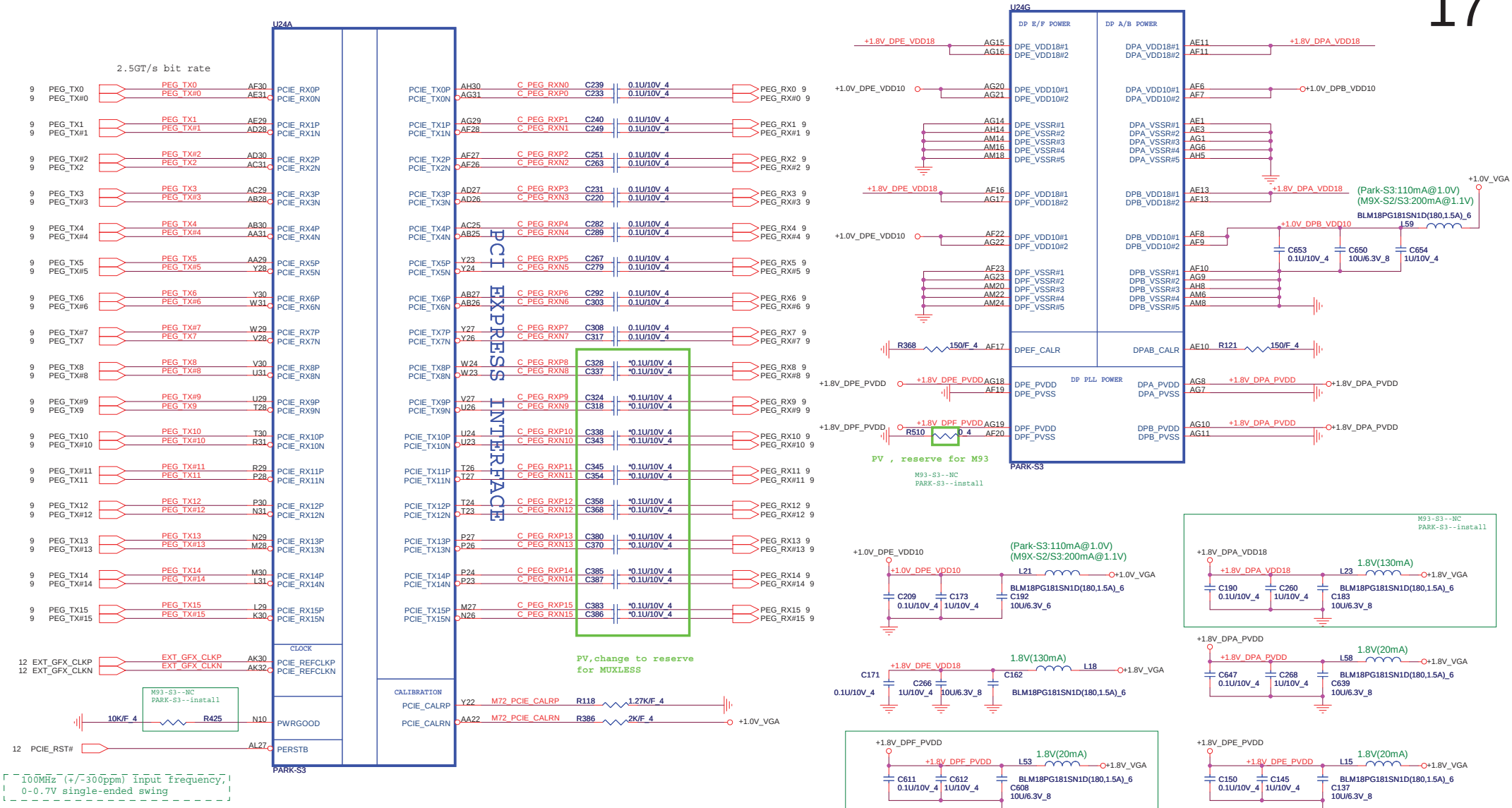
U24A
2.5GT/s bit rate
PCI EXPRESS INTERFACE
PARK-S3
CLOCK
CALIBRATION
PWRGOOD
PERSTB
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing
PV,change to reserve
for MUXLESS
M93-S3--NC
PARK-S3--install
U24G
DP E/F POWER
DP A/B POWER
DP PLL POWER
DPEF_CALR
DPAB_CALR
PV , reserve for M93
(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)
1.8V(130mA)
1.8V(20mA)

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix - Orion	64*16-800MHZ	H5TQ1G63BFR-12C
0010	Reserved		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V

GPIO22(ROMCS#)
PD without external VBIOS ROM

PV,change to reserv only for delete workaround

SI, R128 change to reserve only for MUXLESS

SI , add R409 , R543 from AMD update

SI , provide 14M CLK source to slove Park JTAG test block intermittently fails to initialize correctly issue

SI , AMD Document Update change PU to PD

SI , reserve EEPROM to slove Park JTAG test block intermittently fails to initialize correctly issue

PV,delete workaround EEPROM

SI , add R103 , remove R165 from AMD update

PV,change to pull low for delete workaround

PV,change to short pad

PV,add it from AMD nda update If no contact this pin to LVDS need pull low

For M93-S3: Use 150 Ohms Pull Down
For M92-S2: Use 0R to VDDR4
For Park-S3: NC

SI,change to reserve only for MUXLESS

SI , reserve R46,R48 for MUXLESS

SI , reserve R321 , R331 for MUXLESS

PV,reserve for M93

SI , need pull high near chip side for MUXLESS change to reserve only

Pure DIS need install

For Int Clk 27Mhz

I2C ADDRESS: 9AH

w/s 10/10

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PARK_Main	1A

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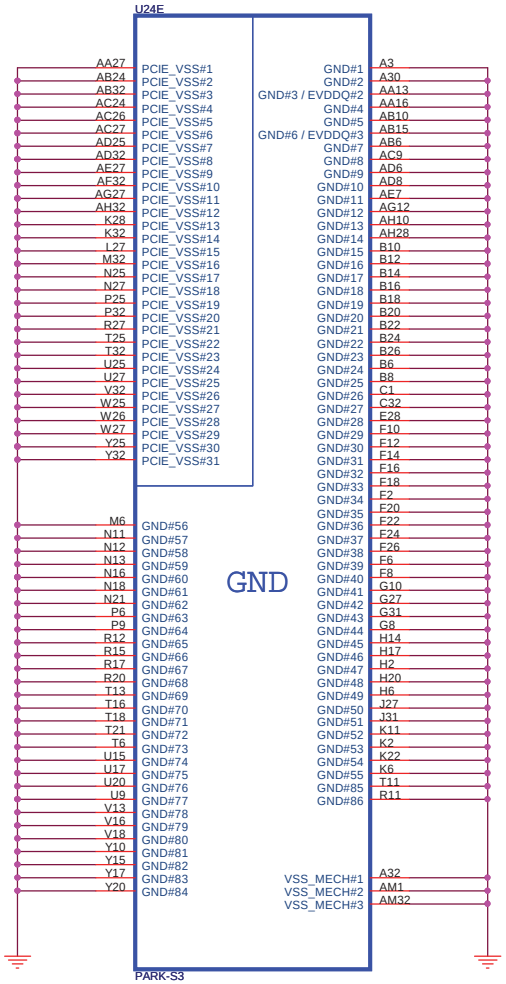
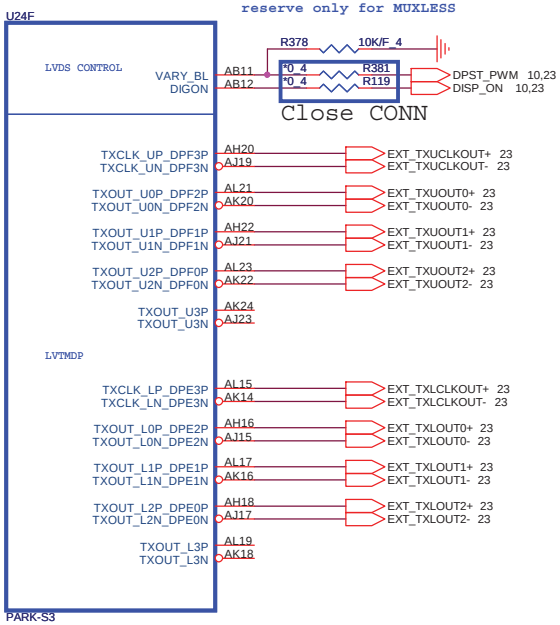
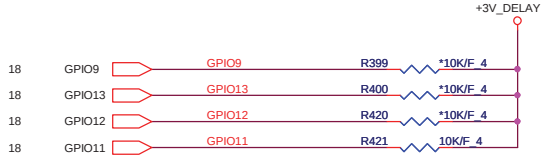
N85/RD2



SI, R119,R381 change to reserve only for MUXLESS





CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

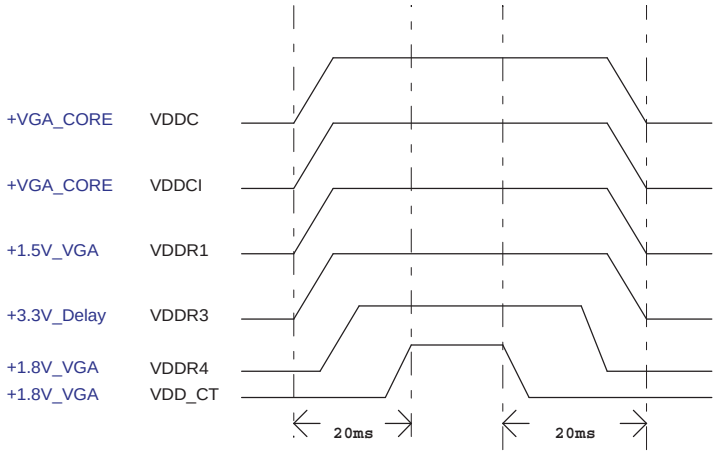
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

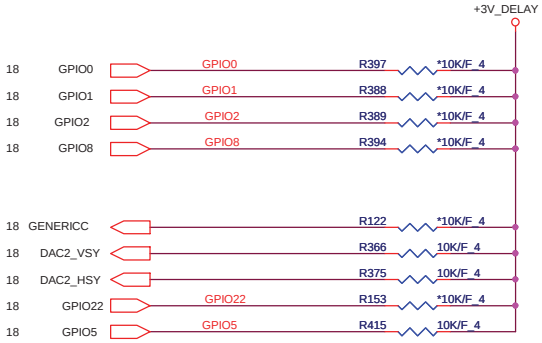
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	PARK_GND / LVDS/ Straps	1A

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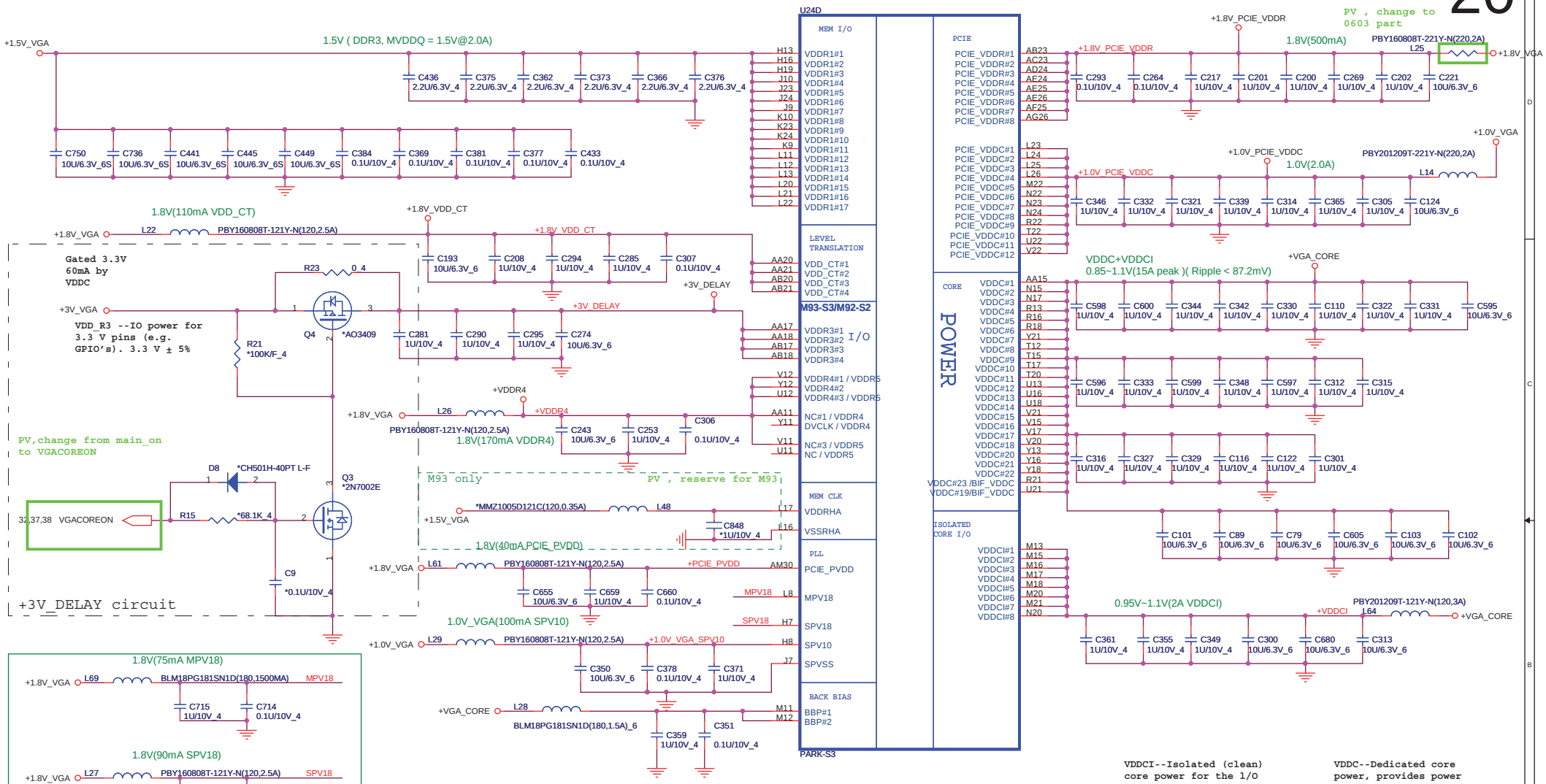
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	PARK_Power_and_NC	1A

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22 VMA_ODT0 — VMA_ODT0
22 VMA_ODT1 — VMA_ODT1
22 VMA_RAS0# — VMA_RAS0#
22 VMA_RAS1# — VMA_RAS1#
22 VMA_CAS0# — VMA_CAS0#
22 VMA_CAS1# — VMA_CAS1#
22 VMA_WE0# — VMA_WE0#
22 VMA_WE1# — VMA_WE1#
22 VMA_CS0# — VMA_CS0#
22 VMA_CS1# — VMA_CS1#
22 VMA_CKE0 — VMA_CKE0
22 VMA_CKE1 — VMA_CKE1
22 VMA_CLK0 — VMA_CLK0
22 VMA_CLK0# — VMA_CLK0#
22 VMA_CLK1 — VMA_CLK1
22 VMA_CLK1# — VMA_CLK1#
22 VMA_WDQS[7..0] — VMA_WDQS[7..0]
22 VMA_RDQS[7..0] — VMA_RDQS[7..0]
22 VMA_DM[7..0] — VMA_DM[7..0]
22 VMA_DQ[63..0] — VMA_DQ[63..0]
22 VMA_MA[13..0] — VMA_MA[13..0]
22 VMA_BA0 — VMA_BA0
22 VMA_BA1 — VMA_BA1
22 VMA_BA2 — VMA_BA2

support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

U24C — MEMORY INTERFACE — PARK-S3

Signal	Pin	Signal	Pin	Signal
VMA_DQ0	K27	DQA_0	MAA_0	K17	VMA_MA0
VMA_DQ1	J29	DQA_1	MAA_1	J20	VMA_MA1
VMA_DQ2	H30	DQA_2	MAA_2	H23	VMA_MA2
VMA_DQ3	H32	DQA_3	MAA_3	G23	VMA_MA3
VMA_DQ4	G29	DQA_4	MAA_4	G24	VMA_MA4
VMA_DQ5	F28	DQA_5	MAA_5	H24	VMA_MA5
VMA_DQ6	F32	DQA_6	MAA_6	J19	VMA_MA6
VMA_DQ7	F30	DQA_7	MAA_7	K19	VMA_MA7
VMA_DQ8	C30	DQA_8	MAA_8	J14	VMA_MA8
VMA_DQ9	F27	DQA_9	MAA_9	K14	VMA_MA9
VMA_DQ10	A28	DQA_10	MAA_10	J11	VMA_MA10
VMA_DQ11	C28	DQA_11	MAA_11	J13	VMA_MA11
VMA_DQ12	E27	DQA_12	MAA_12	H11	VMA_MA12
VMA_DQ13	G26	DQA_13	MAA_13/BA2	G11	VMA_BA2
VMA_DQ14	D26	DQA_14	MAA_14/BA0	J16	VMA_BA0
VMA_DQ15	F25	DQA_15	MAA_15/BA1	L15	VMA_BA1
VMA_DQ16	A25	DQA_16			
VMA_DQ17	C25	DQA_17	DQMA_0	E32	VMA_DM0
VMA_DQ18	E25	DQA_18	DQMA_1	E30	VMA_DM1
VMA_DQ19	D24	DQA_19	DQMA_2	A21	VMA_DM2
VMA_DQ20	E23	DQA_20	DQMA_3	C21	VMA_DM3
VMA_DQ21	F23	DQA_21	DQMA_4	E13	VMA_DM4
VMA_DQ22	D22	DQA_22	DQMA_5	D12	VMA_DM5
VMA_DQ23	F21	DQA_23	DQMA_6	E3	VMA_DM6
VMA_DQ24	E21	DQA_24	DQMA_7	F4	VMA_DM7
VMA_DQ25	D20	DQA_25			
VMA_DQ26	F19	DQA_26	RDQSA_0	H28	VMA_RDQS0
VMA_DQ27	A19	DQA_27	RDQSA_1	C27	VMA_RDQS1
VMA_DQ28	D18	DQA_28	RDQSA_2	A23	VMA_RDQS2
VMA_DQ29	F17	DQA_29	RDQSA_3	E19	VMA_RDQS3
VMA_DQ30	A17	DQA_30	RDQSA_4	E15	VMA_RDQS4
VMA_DQ31	C17	DQA_31	RDQSA_5	D10	VMA_RDQS5
VMA_DQ32	E17	DQA_32	RDQSA_6	D6	VMA_RDQS6
VMA_DQ33	D16	DQA_33	RDQSA_7	G5	VMA_RDQS7
VMA_DQ34	F15	DQA_34			
VMA_DQ35	A15	DQA_35	WDQSA_0	H27	VMA_WDQS0
VMA_DQ36	D14	DQA_36	WDQSA_1	A27	VMA_WDQS1
VMA_DQ37	F13	DQA_37	WDQSA_2	C23	VMA_WDQS2
VMA_DQ38	A13	DQA_38	WDQSA_3	C19	VMA_WDQS3
VMA_DQ39	C13	DQA_39	WDQSA_4	C15	VMA_WDQS4
VMA_DQ40	E11	DQA_40	WDQSA_5	E9	VMA_WDQS5
VMA_DQ41	A11	DQA_41	WDQSA_6	C5	VMA_WDQS6
VMA_DQ42	C11	DQA_42	WDQSA_7	H4	VMA_WDQS7
VMA_DQ43	F11	DQA_43			
VMA_DQ44	A9	DQA_44	ODTA0	L18	VMA_ODT0
VMA_DQ45	C9	DQA_45	ODTA1	K16	VMA_ODT1
VMA_DQ46	F9	DQA_46			
VMA_DQ47	D8	DQA_47	CLKA0	H26	VMA_CLK0
VMA_DQ48	E7	DQA_48	CLKA0B	H25	VMA_CLK0#
VMA_DQ49	A7	DQA_49			
VMA_DQ50	C7	DQA_50	CLKA1	G9	VMA_CLK1
VMA_DQ51	F7	DQA_51	CLKA1B	H9	VMA_CLK1#
VMA_DQ52	A5	DQA_52			
VMA_DQ53	E5	DQA_53	RASA0B	G22	VMA_RAS0#
VMA_DQ54	C3	DQA_54	RASA1B	G17	VMA_RAS1#
VMA_DQ55	E1	DQA_55			
VMA_DQ56	G7	DQA_56	CASA0B	G19	VMA_CAS0#
VMA_DQ57	G6	DQA_57	CASA1B	G16	VMA_CAS1#
VMA_DQ58	G1	DQA_58			
VMA_DQ59	G3	DQA_59	CSA0B_0	H22	VMA_CS0#
VMA_DQ60	J6	DQA_60	CSA0B_1	J22	
VMA_DQ61	J1	DQA_61			
VMA_DQ62	J3	DQA_62	CSA1B_0	G13	VMA_CS1#
VMA_DQ63	J5	DQA_63	CSA1B_1	K13	
K26	MVREFDA		CKEA0	K20	VMA_CKE0
J26	MVREFSA		CKEA1	J17	VMA_CKE1
J25	MEM_CALRN0		WEA0B	G25	VMA_WE0#
K7	NC/TESTEN#2		WEA1B	H10	VMA_WE1#
J8	MEM_CALRP1/DPC_CALR		PX_EN	AB16	
K25	MEM_CALRP0		RSVD#2	G14	
			RSVD#3	G20	
L10	DRAM_RST				
K8	CLKTESTA				
L7	CLKTESTB				

Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

+1.5V_VGA
R221 *2.2K_4 Rc
DRAM_RST — R202 51/F_4 — DRAM_RST_M — DRAM_RST_M 22
Rb
C437 Ca — 68P/50V_4
R194 Ra — 10K/F_4
PV , update from AMD ref136-rev10

+1.5V_VGA
R209 40.2/F_4 Rd
PLACE MVREFD DIVIDERS AND CAPS CLOSE TO ASIC
MVREFD
C432 0.1U/10V_4
R201 100/F_4 Re
+1.5V_VGA
R226 40.2/F_4 Rd
MVREFS
C442 0.1U/10V_4
R215 100/F_4 Re
18 TESTEN
+1.5V_VGA
TESTEN — R430 243/F_4 — R550 0_4 Note 3
R132 150/F_4 Note 2
Note 1
R431 243/F_4
PV , reserve for M93
DRAM_RST
CLKTESTA
CLKTESTB
R547 *4.7K_4
R548 *4.7K_4
PV , reserve for M93
For M93-S3 only
C692 0.1U/10V_4
C689 0.1U/10V_4
R403 51.1/F_4
R401 51.1/F_4
route 50ohms single-ended/100ohms diff and keep short
For PARK-S3 only

R551 0_4 VMA_MA13
PV,reserve for M93
For PARK-S3 only
For M9X-S2/S3 with DDR3: this pin is not in use.

Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

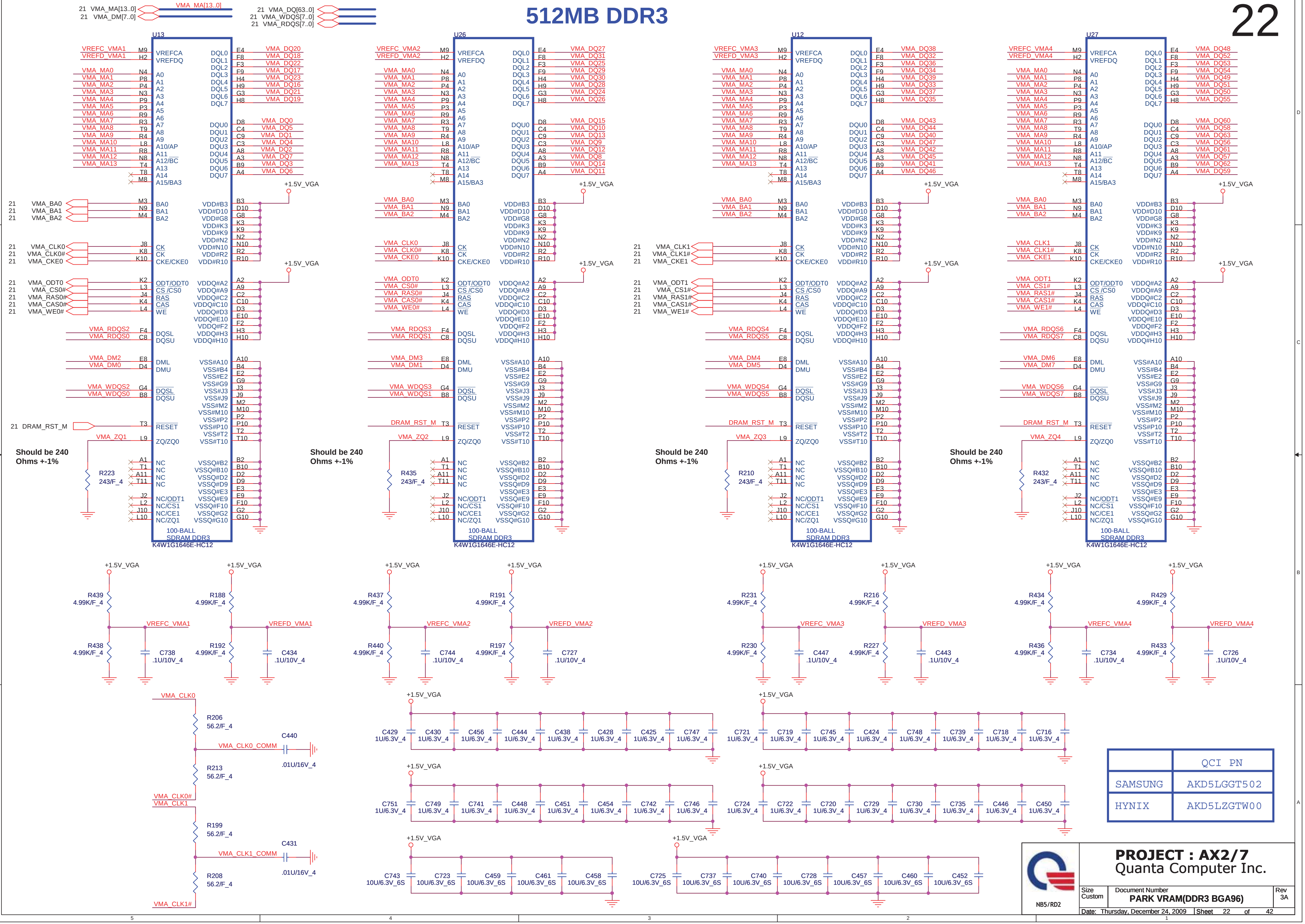
NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PARK/MEM_Interface	1A

Date: Thursday, December 24, 2009 | Sheet 21 of 42

512MB DDR3


U13
U26
U12
U27
VREFCA
VREFDQ
DQL0
DQU0
A0
A10/AP
A12/BC
A15/BA3
BA0
BA1
BA2
CK
CKE/CKE0
ODT/ODT0
CS/CS0
RAS
CAS
WE
DQSL
DQSU
DML
DMU
RESET
ZQ/ZQ0
NC
NC/ODT1
NC/CS1
NC/CE1
NC/ZQ1
VDD#B3
VDDQ#A2
VSS#A10
VSSQ#B2
+1.5V_VGA
100-BALL
SDRAM DDR3
K4W1G1646E-HC12
Should be 240 Ohms +-1%
R223 243/F_4
R435 243/F_4
R210 243/F_4
R432 243/F_4
VREFC_VMA1
VREFD_VMA1
VREFC_VMA2
VREFD_VMA2
VREFC_VMA3
VREFD_VMA3
VREFC_VMA4
VREFD_VMA4
4.99K/F_4
.1U/10V_4
VMA_CLK0
VMA_CLK0#
VMA_CLK0_COMM
VMA_CLK1
VMA_CLK1#
VMA_CLK1_COMM
56.2/F_4
.01U/16V_4
1U/6.3V_4
10U/6.3V_6S
DRAM_RST_M

	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	PARK VRAM(DDR3 BGA96)	3A

Date: Thursday, December 24, 2009 Sheet 22 of 42

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

OPTION SIGNAL FROM PARK to LVDS for discrete

SI, new option for MUXLESS

SI , add C21 from EMI suggest

SI, R34,R35 change to reserve only and add R33,R37 for MUXLESS

PV, add Q9 for BIOS check

Vari bright function

Do not use it

CAMERA

SI , update foortprint to 88266-05001-06-5P-L-SMT

Reserve for EMI

PROJECT : AX2/7	Quanta Computer Inc.
Size: Custom	Document Number: LCD CONN
Rev: 1A	
NB5/RD2	Date: Thursday, December 24, 2009 Sheet 23 of 42

CRT PORT

PV , change footprint to F3_2X1_65-2_8

PV , change footprint to dsub-dsd-15aebb-15p-v-smt

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)

+5V F1 40 mils +5VCRT
FUSE1A6V_POLY

+5VCRT C6 0.1U/10V_4

40 MIL

CRT_R L3 BK1608LL680(0.2A,68)_6 CRT_R1
CRT_G L2 BK1608LL680(0.2A,68)_6 CRT_G1
CRT_B L1 BK1608LL680(0.2A,68)_6 CRT_B1

R20 140/F_4 R16 150/F_4 R11 150/F_4 C13 5.6P/50V_6 C10 5.6P/50V_6 C7 5.6P/50V_6 C8 5.6P/50V_6 C11 5.6P/50V_6 C12 5.6P/50V_6

close conn within 600mils

EMI

CRT CONN CN17

10,18 CRT_R CRT_R
10,18 CRT_G CRT_G
10,18 CRT_B CRT_B

C3 0.1U/10V_4

U1 AHCT1G125DCH
U2 AHCT1G125DCH

10,18 VSYNC_COM
10,18 HSYNC_COM

PR_VSYNC R5 33_4 CRTVSYNC
PR_HSYNC R6 33_4 CRTHSYNC
R1 *0_4/S CRTDDCCLK2
R8 *0_4/S CRTDDCDAT2

C1 *470P/50V_4 C2 *47P/50V_4 C4 *47P/50V_4 C5 *47P/50V_4

+3V_DELAY R4 *4.7K_4
+3V R3 4.7K_4

10,18 DDCCLK DDCCLK Q1 2N7002E DDCCLK2

+3V_DELAY R10 *4.7K_4
+3V R9 4.7K_4

10,18 DDCDATA DDCDATA Q2 2N7002E DDCDAT2

SI, R4,R10 change to reserve only and add R3,R9 for MUXLESS

R2 6.81K_4 R7 6.81K_4

+5VCRT +5VCRT D3 CH501H-40PT +5V_CRT2

+3V
D9 BAV99W CRT_R1
D7 BAV99W CRT_G1
D5 BAV99W CRT_B1
+5V
D1 BAV99W DDCCLK2
D2 BAV99W CRTVSYNC
D4 BAV99W CRTHSYNC
D6 BAV99W DDCDAT2

PV,add for ESD

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

NB5/RD2

Date: Thursday, December 24, 2009 | Sheet 24 of 42

UMA/DISCRETE select for HDMI

From RS880M

SI , all add for MUXLESS

for Layout concern ,placement close north bridge

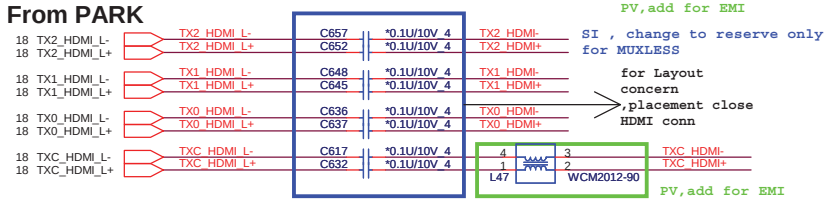
for Layout concern ,placement close HDMI conn

From PARK

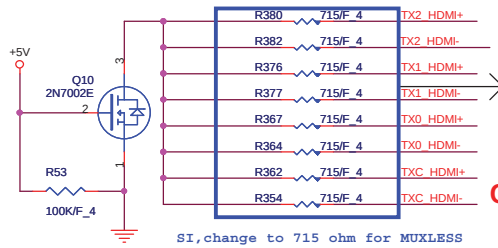
PV,add for EMI

SI , change to reserve only for MUXLESS

for Layout concern ,placement close HDMI conn



PV,add for EMI



UMA RS780M
上 715 ohm CS17152FB17

DIS M92-S
上 499 ohm CS14992FB24

Close to HDMI Connector

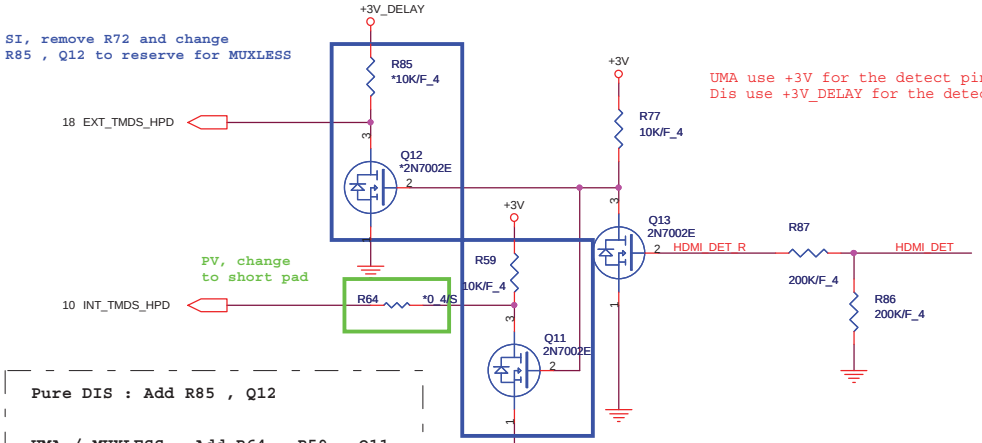
SI,change to 715 ohm for MUXLESS

HDMI HPD SENSE

SI, remove R72 and change R85 , Q12 to reserve for MUXLESS

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin

PV, change to short pad



Pure DIS : Add R85 , Q12

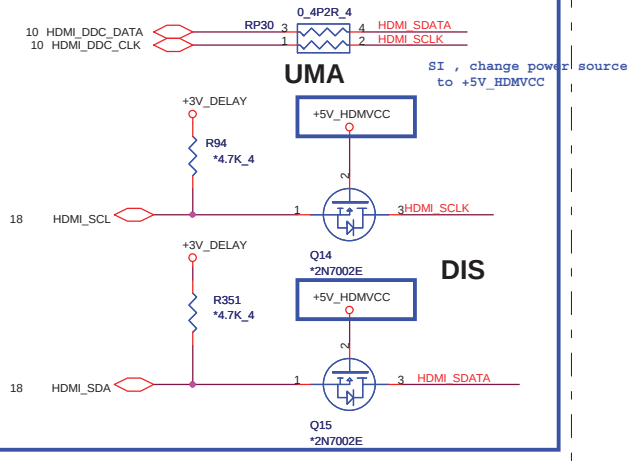
UMA / MUXLESS : Add R64 , R59 , Q11

SI , add R64,R59,Q11 for MUXLESS

UMA DDC4 is 5V tolerance , the MOSFET level shifter no need
Discrete DDC is 3V tolerance,the MOSFET level shifter is need

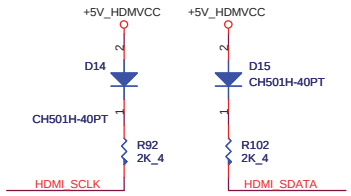
UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector

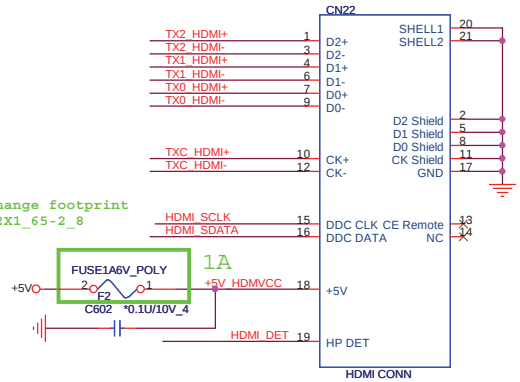


SI, remove R93 , R350 . Add RP30 R94,R351,Q14,Q15 change to reserve only for MUXLESS

HDMI PORT



PV , change footprint to F3_2X1_65-2_8



PIN 13	CLK source	Remark
Floating	12M Hz	Xtal
Pull high	48M Hz	Input to RTS5159 pin48

SI , change CLK source from SB internal CLK GEN

AL005158B10 -->RTS5158E
AL005159B00 -->RTS5159GR

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

PV,change to short pad

SP7	R517	*0_4/S	MS-D0_SD-D0_XD-D6
SP6	R515	*0_4/S	MS-D1_XD-D3_SD_D1
SP8	R520	*0_4/S	MS-D2_XD-D2
SP16	R535	*0_4/S	XD-RE#_SD-D2
SP5	R513	*0_4/S	MS-BS_XD-D5
SP15	R539	*0_4/S	SD-D3_XD-WE
SP11	R527	*0_4/S	SD_CLK_MS_CLK
SP2	R504	*0_4/S	SD_WP
SP13	R533	*0_4/S	XD-WP#
SP19	R541	*0_4/S	XD-CLE
SP4	R507	*0_4/S	XD-D4
SP10	R521	*0_4/S	MS-D3_XD-D7
SP14	R534	*0_4/S	XD-RB#
SP12	R528	*0_4/S	XD-D0
SP17	R540	*0_4/S	XD-ALE
SP18	R536	*0_4/S	XD-CE#
SD_CMD_R	R529	*0_4/S	SD-CMD

SI , change to 22P then change to reserve only

SI , Add R537 from vendor suggestion

Internal have pull Hi 200K

RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA

SI, change power source from +3VSUS to +3V

Close to Chipset

Can not more than 10p

PV, change to short pad

*RB501V-40

Add diode for 5158E cardreader driver lost issue

5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

PV , change footprint to 4in1-cm4s-125-36p-r-v-smt

CARD READER SOCKET

SI , update foortprint to spad-ax2-1np

VGA Hole

CPU Hole

SI, add CPU & VGA hold pad from EMI request

SI , add for ESD testing

PV,add new pad for new outline

CLOSE CONN

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET &HOLE	1A

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PV , change to short pad

+3V R519 *0_6/S C830 1U/6.3V_4

+3V_DVDD
C819 1U/10V_4 C821 10U/6.3V_8 — Close to Pin1
C816 10U/6.3V_8 C817 1U/10V_4 — Close to Pin9

+5V
C812 10U/6.3V_8 C810 .1U/10V_4 — Close to Pin46
C822 10U/6.3V_8 C809 .1U/10V_4 — Close to Pin39

+5VAVDD
C782 10U/6.3V_6 C780 1U/10V_4 — AGND AGND — Close to Pin25
C784 10U/6.3V_8 C786 1U/10V_4 — AGND AGND — Close to Pin38

PV,delete C824
ACZ_SDIN0_R C815 *27P/50V_4
FOR EMI

PV, change to reserve only
+5V L74 *PBY201209T-221Y-N 1.3A
+5VAVDD
C772 10U/6.3V_6
C774 4.7U/6.3V_6
C775 1U/6.3V_4
C783 .1U/10V_4
AGND

PV , change from 220 to 47

PV, change footprint and value

MIC1-VERFL MIC1-VERFR MIC2-VERFO
28 EARP_L R489 47/F_4 HP-L
28 EARP_R R488 47/F_4 HP-R
AGND C777 2.2U/6.3V_6 CPVEE
269CBN C776 2.2U/6.3V_6 269CBP
C778 10U/6.3V_6 AGND
C781 .1U/10V_4 C779 1U/10V_4 — Close to Pin27
AGND
AGND
+5VAVDD

PV , add LDO
+5VAVDD U33 Vout Vin BYP GND EN G9191-475T1U
C842 1U/6.3V_4 AGND
R571 10K/F_4
+5V C847 0.047U/25V_4

SI , remove L79,L80,L83,L84

Place near CODEC
SPKR- C802 *180p/50V_4 C806 *1U/16V_6
SPKR+ C808 *180p/50V_4
SPKL- C798 *180p/50V_4 C796 *1U/16V_6
SPKL+ C794 *180p/50V_4

SI , change L6,L7,L8,L9 to CX5AG601001 from EMI suggest

SPEAKER
Place near SPEAKER CONN
L9 L7 L6 L8 BLM15AG601SS1D
C45 C42 C46 C47 220P/50V_6
CN3 INT SPEAKER CONN

SI , add C42,C45,C46,C47 from EMI suggestion

U32 Ditigal Analog ALC270A-GR

AGND +5VAVDD +5V EAPD# PD# +3V_DVDD
SPKL+ SPKL- SPKR- SPKR+
AVSS2 AVDD2 PVDD1 SPK-L+ SPK-L- PVSS1 PVSS2 SPK-R- SPK-R+ PVDD2 EAPD SPDIFO PGND
CBP CBN CPVEE HP-OUT-R HP-OUT-L MIC1-VREFO-L MIC1-VREFO-R MIC2-VREFO LDO-CAP VREF AVSS1 AVDD1
DVDD1 GPIO0 GPIO1 PD# SDATA-OUT BIT-CLK DVSS2 SDATA-IN DVDD-IO SYNC RESET# PCBEEP

LINE1-R LINE1-L MIC1-R MIC1-L MONO-OUT JDREF Sense-B MIC2-R MIC2-L LINE2-R LINE2-L Sense A

MIC1-VERFL R497 4.7K_4
MIC1-VERFR R491 4.7K_4
EXT_MIC1-R_C C789 4.7U/6.3V_6 EXT_MIC1-R_R R495 1K/F_4 EXT_MIC_R 28
EXT_MIC1-L_C C795 4.7U/6.3V_6 EXT_MIC1-L_R R496 1K/F_4 EXT_MIC_L 28
R498 20K/F_4 AGND — Place near CODEC
INT_MIC_R C801 4.7U/6.3V_6 INT_MIC
INT_MIC_L C803 4.7U/6.3V_6
Place near CODEC
SENSEA R502 39.2K/F_4 SA_A# — SA_A# 28
R501 20K/F_4 SA_B# — SA_B# 28

SA_A# -->EXT Ear Phone
SA_B# -->EXT MIC

T169 T170
PCBEEP
ACZ_RST#_AUDIO 13
ACZ_SYNC_AUDIO 13
+3V_DVDD
13 ACZ_SDOUT_AUDIO
13 BIT_CLK_AUDIO
ACZ_SDIN0_R R512 33_4 ACZ_SDIN0 13

SI, remove R511
C814 *27P/50V_4
SI , change to reserve only

Place near CODEC
+5VAVDD +INTMIC_BIAS
R485 *10K/F_4
R484 *10K/F_4
C768 *1U/6.3V_4
U31 *TLV2461IDBVRG4
C762 *100P/50V_4
INT_MIC INT_MIC_IN_C_R
R481 *10K/F_4
C761 *100P/50V_4
R480 *10K/F_4
C763 *270P/25V_4
PV, change to reserve only

MIC2-VERFO
R302 3K_4
C540 *.22U/25V_6
INT_MIC_IN_C
INT_MIC_IN L79 BLM15AG601SS1D
CN10 88266-020L
R301 *3K_4
PV,add for EMI
C541 *1U/6.3V_4
R300 *3K_4
C165 *220P/50V_6
AGND AGND
+5VAVDD
R427 0_6
PV , add R427
TO Internal Mic

SI , update foortprint to 88266-020L-2P-R-SMT

PV,add for test
Place Under CODEC
R328 0_6 RC0603
R315 *0_6/S short0603
R261 *0_6/S short0603
R473 *0_6/S short0603
R313 *0_6/S short0603
R482 *0_6/S short0603
R506 *0_6/S short0603
AGND

PC-BEEP
+5VAVDD
AGND C825 *0.047U/10V
C835 close to C820 and C820 close to chip
PV , remove U33,C825,C811 C820,R523,R524 R510,R514
Add this circuit same as AX1/3
R566 10K/F_4
C811 .1U/10V_4 PCBBEP_R2 R546 47K_4 PCBBEP_L C820 .1U/10V_4 PCBEEP
Q36 2N7002E
13 ACZ_SPKR
R549 4.7K_4
C835 .1U/10V_4
R549 close to R546
AGND AGND

+3V_DVDD
R516 *10K_4
SI,remove U35,C681 , add D40 for audio function not stable
EAPD# ACZ_RST#_AUDIO
R522 R518 0_4 *0_4 EAPD#_R
32 VOLMUTE#
D40 BAT54A PD#

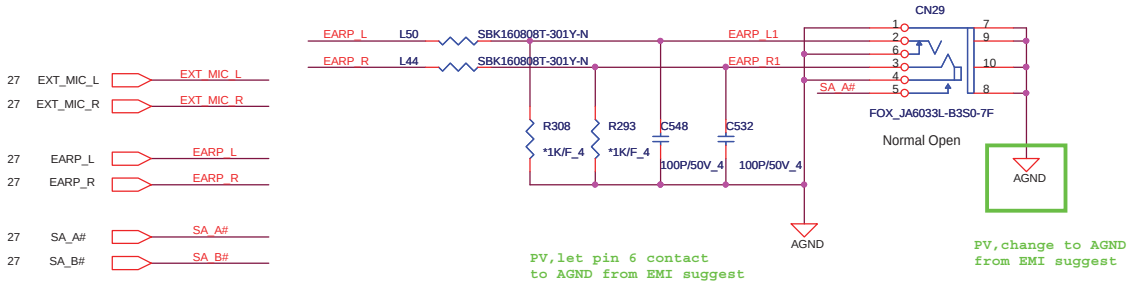
NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia 92HD75B2X5	1A

Date: Thursday, December 24, 2009 | Sheet 27 of 42

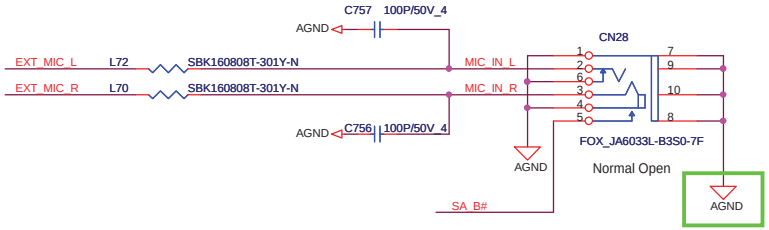
Line out



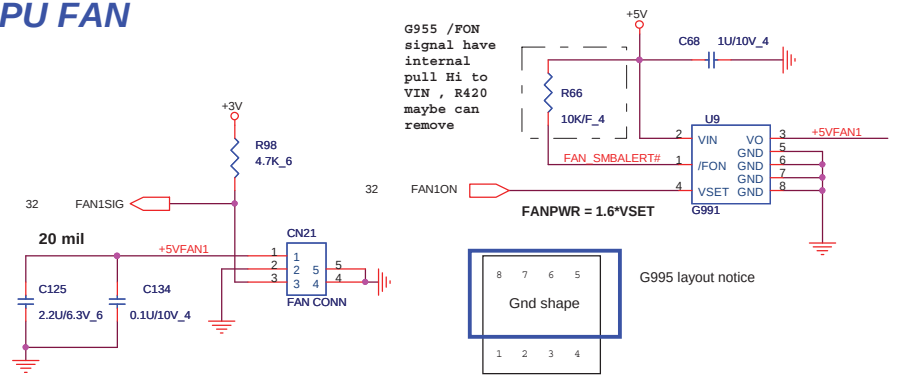
SA_A# -->EXT Ear Phone

SA_B# -->EXT MIC

MIC

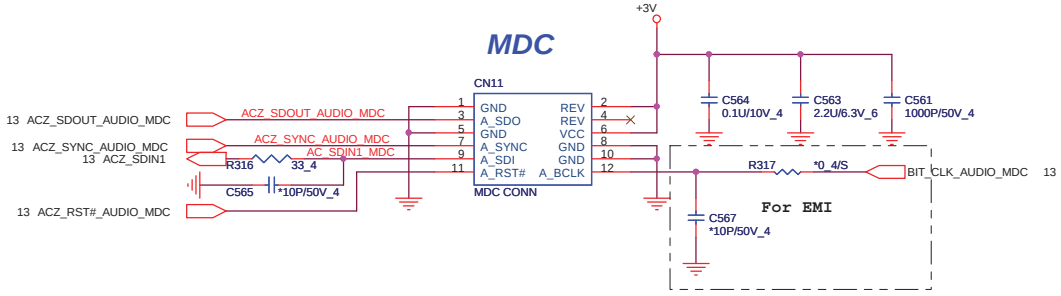


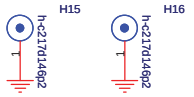
CPU FAN



Modem CONN

MDC

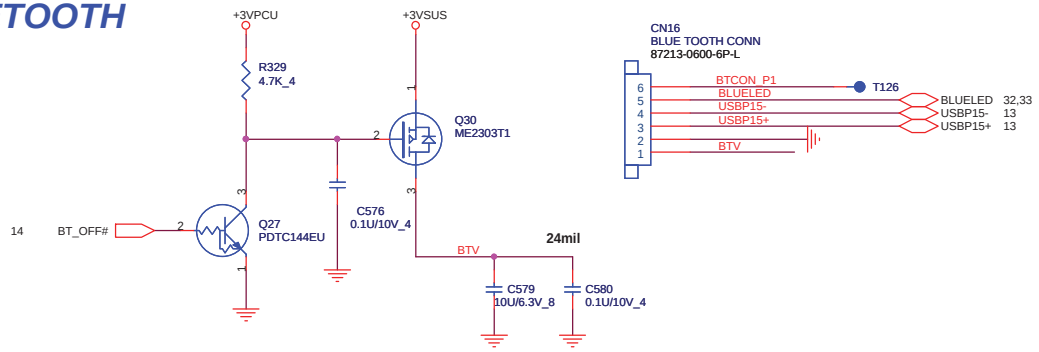




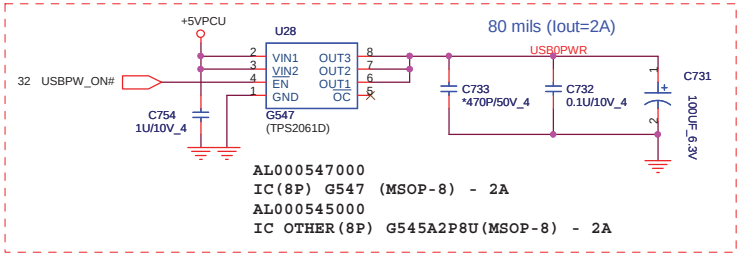
Nut PN:MBCA6002013

NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
Size: Custom	Document Number: AMP_TPA6017/MDC1.5/CPU FAN	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 28 of 42	

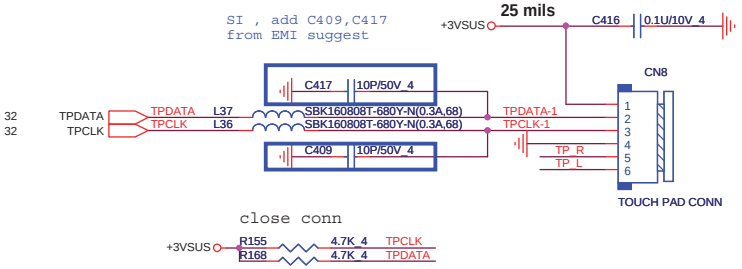
BLUETOOTH



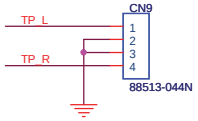
LEFT SIDE USBX2

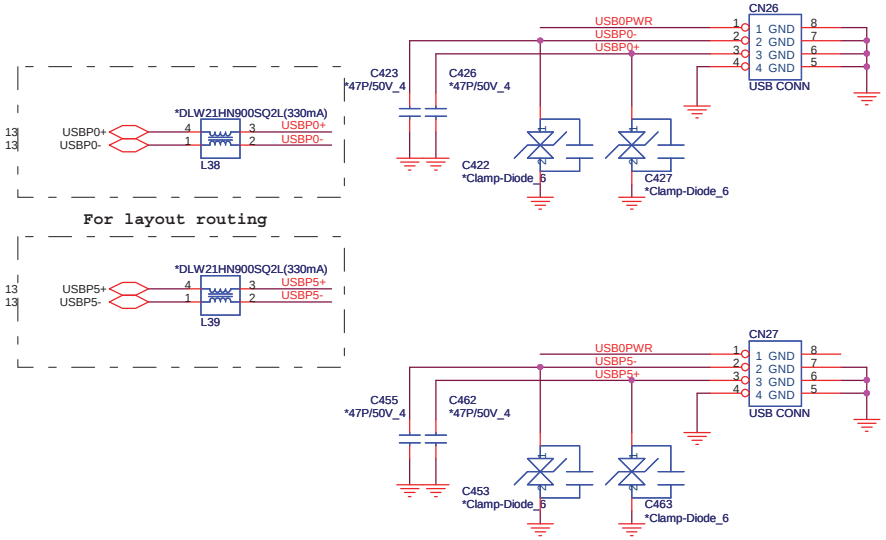


TOUCH PAD CONN



To TOUCH PAD SW board

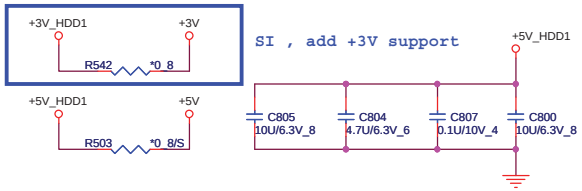


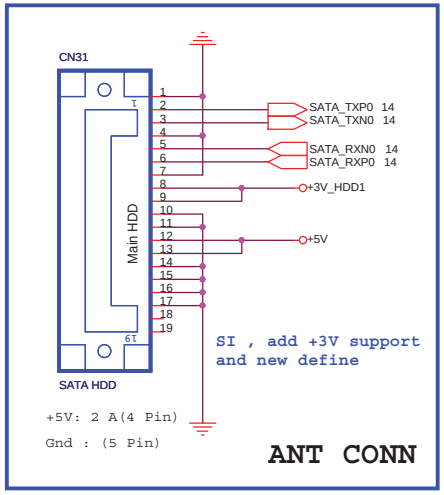


SATA HDD CONNECTOR

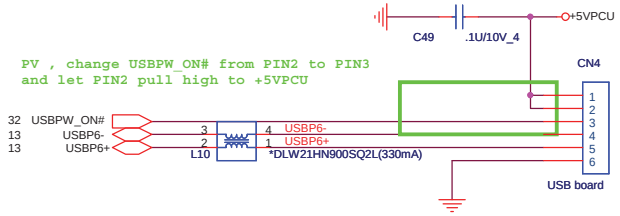
SI , update P/N : DFHS13FS019

SI , delete CN30 change to ANT CONN





Right SIDE USBX1



NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/USBX3/TP/HDD	1A

Date: Thursday, December 24, 2009 | Sheet 29 of 42

+CTRL12DVDD R40 *0_6/S

Power trace Layout 寬度> 30mil

+DVDD12

C54 .1U/10V_4 C52 .1U/10V_4 C107 .1U/10V_4 C88 .1U/10V_4

CLOSE to Pin 10, 13, 30, 36

+EVDD12

C67 1U/10V_4 C76 1U/10V_4

LAN-AGND

close to pin 19

SI , remove EEPROM
U5,C48,R42,R50

Power trace Layout 寬度> 30mil

+3VLANVCC

LANVCC
1.2W
364mA

C53 4.7U/6.3V_6 C109 .1U/10V_4

+3V_LAN

C56 .1U/10V_4 C55 .1U/10V_4

CLOSE to Pin 29,37

+3V_A_LAN

C604 .1U/10V_4 C601 *.1U/10V_4

CLOSE to Pin 1

+CTRL12DVDD

C97 10U/6.3V_8 C83 .1U/10V_4

R97 2.49K/F_4 LANRSET

+CTRL12A

C111 10U/6.3V_8 C108 .1U/10V_4

XTAL2 XTAL1

C62 33P/50V_4 Y2 25MHZ C69 33P/50V_4

LAN_WLED# +3V_LAN

U7

RTL8103EL

+3V_A_LAN MDI0+ MDI0- MDI1+ MDI1-

AVDD33 MDIP0 MDIN0 NC/FB12 MDIP1 MDIN1 GND1 NC/MDIP2 NC/MDIN2 DVDD12/AVDD12 NC/MDIP3 NC/MDIN3

VCTRL12A/SROUT12 GND4 RSET VCTR12DVDDSR NCVDDSR NC/ENSWREG CKTAL2 CKTAL1 NC/AVDD33 NC/LV_PLL LED0 VDD33B

DVDD12B LED1/EESK LED2/EEDI LED3/EEDO EECS GND3 DVDD12A VDD33A ISOLATEB PERSTB LANWAKEB CLKREQB

DVDD12 GND2 HSIP HSIN REFCLK_P REFCLK_N HSOP HSON EGND NC/SMCLK NC/SMDATA

+DVDD12

EESK_LED100# EEDI_LED10# EECS ISOLATEB LAN_REST_R# PCIE_WAKE#

R333 3.6K_4 +3V_LAN

R350 1K/F_4

PV , add R333 pull high and R350 pull low to fix LAN LED behavior abnormal

+DVDD12 +3V_LAN

R45 *0_4 R569 0_4

LAN_REST# 32
PCIE_WAKE# 13,33
LAN_CLKREQ# 13

PV, add for debug SI , add from HP request

SI , add for DSM

LAN CABLE DETECT 32

+DVDD12 LAN-AGND

9 PCIE_TXP2_LAN
9 PCIE_TXN2_LAN

12 PCIE_LAN_CLKP
12 PCIE_LAN_CLKN

PCIE_LAN_CLKP
PCIE_LAN_CLKN

PCIE_RXN2_LAN_L
PCIE_RXP2_LAN_L

C70 .1U/10V_4
C78 .1U/10V_4

PCIE_RXN2_LAN 9
PCIE_RXP2_LAN 9

+EVDD12

SI , change to AL08103EB01
for support DSM chip

+3V

Delete R261 and add D38 as current loss issue

R55 *1K/F_4

ISOLATEB

R51 15K/F_4

R44 100/F_4

D13 *RB501V-40

LAN_DISABLE# 13,32

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

+3V_LAN

C64 0.1U/10V_4

U6

12 LAN_PLTRST#

TC7SH08FU

LAN_REST_R#

R60 *0_6/S

R57 *0_6/S

LAN-AGND

DB modified to short-pad

HP request reserve
white LED driver circuit

LAN_WLED#

Q31 *DTC144EUA

R404 *10K/F_4 +3VLANVCC

Q32 *DTC144EUA

LAN_WLED# Q

LAN_WLED# R413 *0_4/S

PV, change
to short pad

SI , rotate 180 degree
for EMI suggestion

LAN_Transformer

U20

LAN_MX1- LAN_MX1+ LAN_MCT1 LAN_MX0- LAN_MX0+ LAN_MCT0

RD+ RD- CT TD+ TD- CT

RX+ CT RX- TX- CMT TX+

MDI1- V_DAC_2 MDI1+ MDI0+ V_DAC_1 MDI0-

NS681684

75/F_4 R112 LAN_MCT0_2 C161 0.01U/100V_0603

75/F_4 R111 LAN_MCT0_1 C159 0.01U/100V_0603

C610 1000P/3KV_1808

C117 .01U/16V_4

C118 .01U/16V_4

SI , change footprint
to CC1808

Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	
LED1	O	56	35	
LED2	O	55	34	
LED3	O	54	33	

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

Bios need change

EEDI_LED10# R392 *0_6

EESK_LED100# R391 *0_6/S

LAN_AMLED#

LAN_WLED#

LAN_WLED#

C668 *.01U/16V_4 C699 *.01U/16V_4

EMI suggestion

C663 .1U/10V_4

RJ45

CN25

+3V_LAN R387 330_4 LAN_AMLED LAN_AMLED#

LED_AMBER_P LED_AMBER_N

LAN_MX1- LAN_MX1+ LAN_MX0- LAN_MX0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND1 GND

+3V_LAN R403 330_4 LAN_WLED LAN_WLED# Q

LED_WHITE_P LED_WHITE_N

RJ45_CONN

C697 .1U/10V_4

EMI suggestion

Link

Fixed RJ45 Pin define (0829)

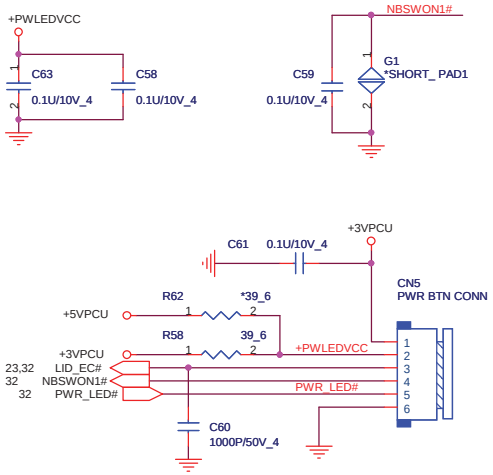
PROJECT : AX2/7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	RTL8102EL/RJ45	1A

Date: Thursday, December 24, 2009 | Sheet 30 of 42

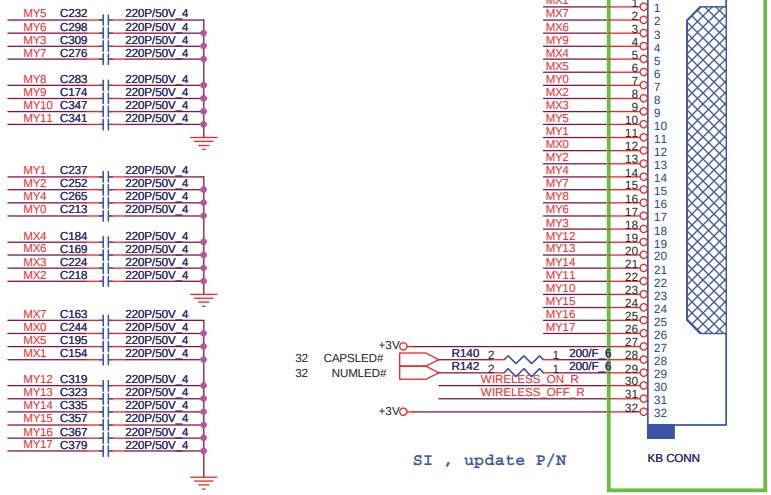
POWER BUTTON CONNECTOR



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

KEYBOARD CONN

PV,update footprint to bl135h-32rla-tand-32p-l-smt

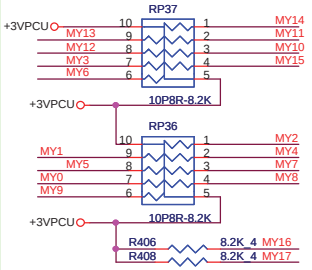


SI , update P/N

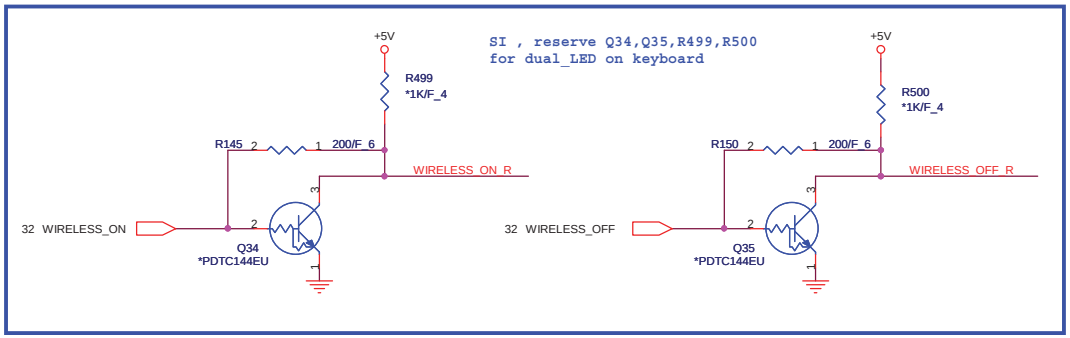
32 MY[0..17] MY[0..17]

32 MX[0..7] MX[0..7]

KEYBOARD PULL-UP

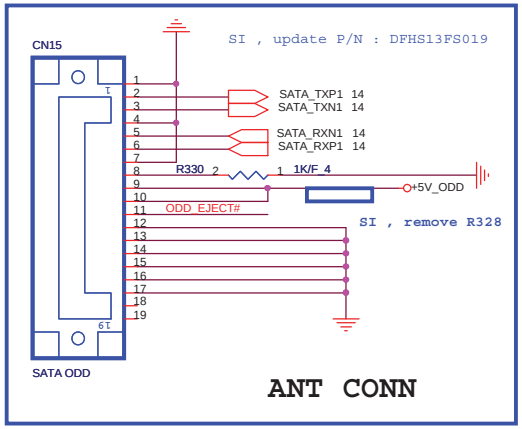


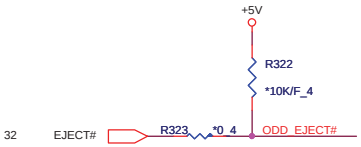
SI , reserve Q34,Q35,R499,R500 for dual_LED on keyboard

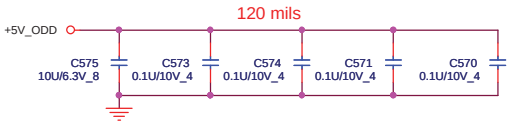


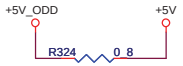
SATA CD-ROM

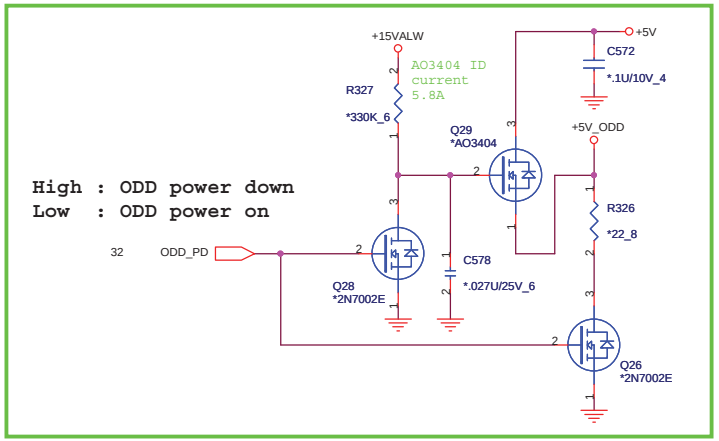
SI , delete CN13 change to ANT CONN





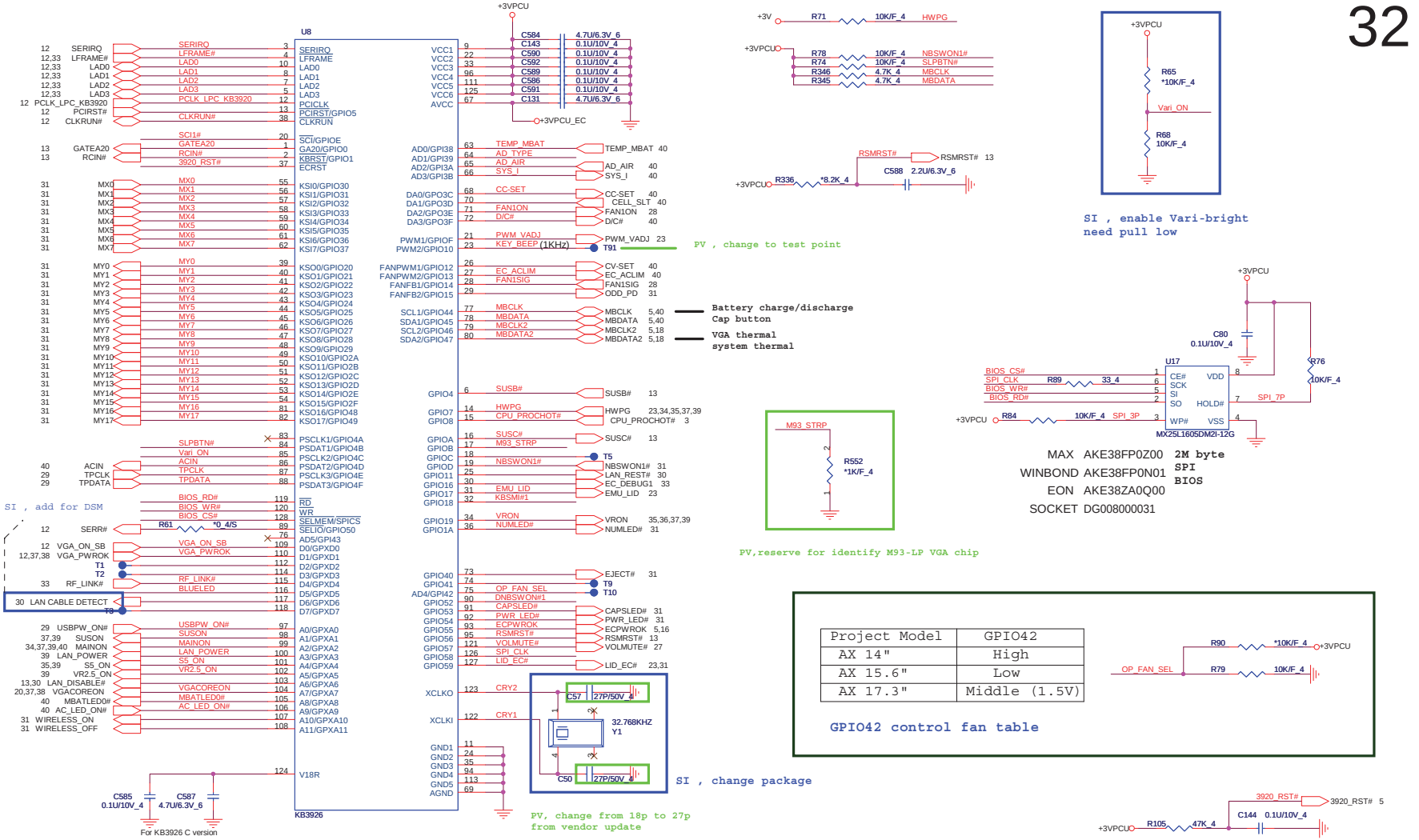




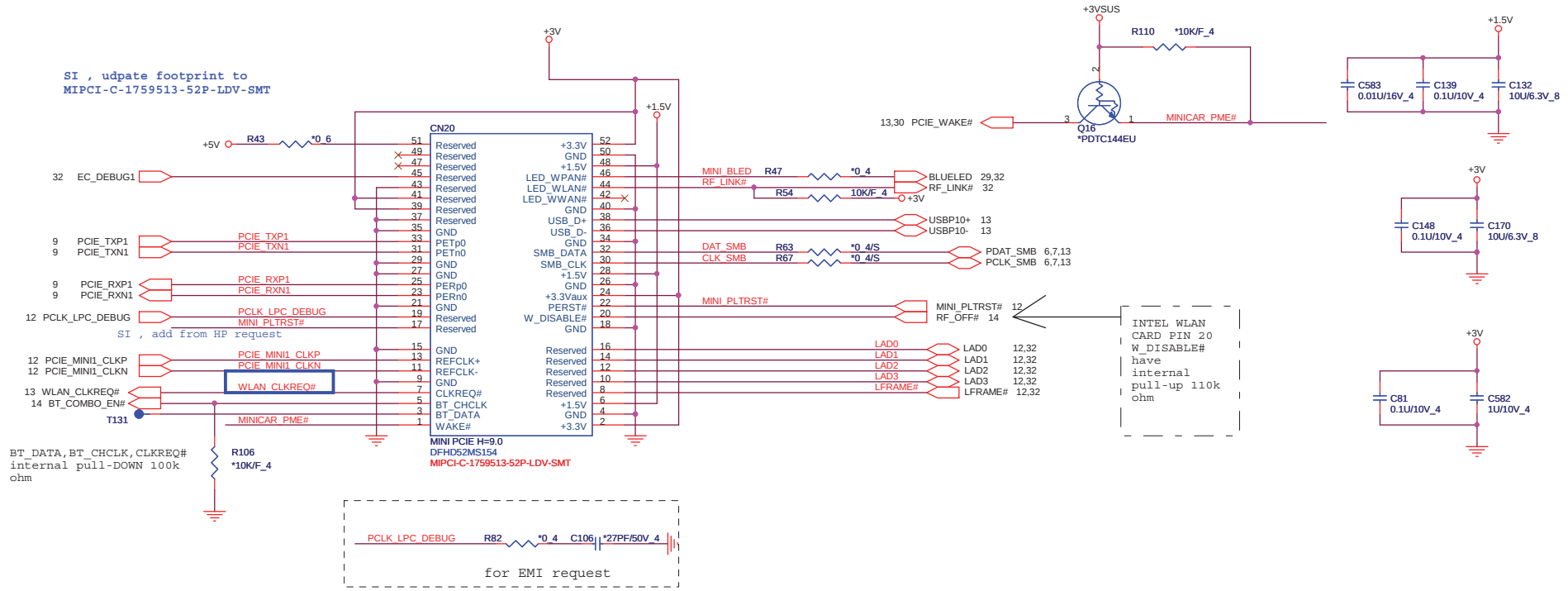


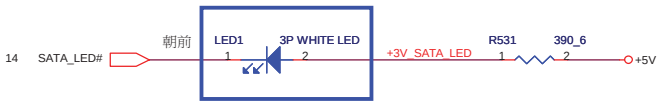
PV, change to reserve only

NB5/RD2	**PROJECT : AX2/7** Quanta Computer Inc.	
Size Custom	Document Number KEYBOARD/SW_BOARD/ODD	Rev 1A
Date: Thursday, December 24, 2009	Sheet 31 of 42	


U8
KB3926
SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
PCICLK
PCIRST/GPIO5
CLKRUN
SCI/GPIOE
GA20/GPIO0
KBRST/GPIO1
ECRST
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
PSCLK1/GPIO4A
PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
PSCLK3/GPIO4E
PSDAT3/GPIO4F
RD
WR
SELMEM/SPICS
SELIO/GPIO50
AD5/GPI43
D0/GPXD0
D1/GPXD1
D2/GPXD2
D3/GPXD3
D4/GPXD4
D5/GPXD5
D6/GPXD6
D7/GPXD7
A0/GPXA0
A1/GPXA1
A2/GPXA2
A3/GPXA3
A4/GPXA4
A5/GPXA5
A6/GPXA6
A7/GPXA7
A8/GPXA8
A9/GPXA9
A10/GPXA10
A11/GPXA11
V18R
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
GND1
GND2
GND3
GND4
GND5
AGND
XCLKO
XCLKI
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
PWM1/GPIOF
PWM2/GPIO10
FANPWM1/GPIO12
FANPWM2/GPIO13
FANFB1/GPIO14
FANFB2/GPIO15
SCL1/GPIO44
SDA1/GPIO45
SCL2/GPIO46
SDA2/GPIO47
GPIO4
GPIO7
GPIO8
GPIOA
GPIOB
GPIOC
GPIOD
GPIO11
GPIO16
GPIO17
GPIO18
GPIO19
GPIO1A
GPIO40
GPIO41
AD4/GPI42
GPIO52
GPIO53
GPIO54
GPIO55
GPIO56
GPIO57
GPIO58
GPIO59
+3VPCU
+3VPCU_EC
C584 4.7U/6.3V_6
C143 0.1U/10V_4
C590 0.1U/10V_4
C592 0.1U/10V_4
C589 0.1U/10V_4
C586 0.1U/10V_4
C591 0.1U/10V_4
C131 4.7U/6.3V_6
TEMP_MBAT
AD_TYPE
AD_AIR
SYS_I
CC-SET
CELL_SLT
FAN1ON
D/C#
PWM_VADJ
KEY_BEEP (1KHz)
T91
EC_ACLIM
FAN1SIG
ODD_PD
MBCLK
MBDATA
MBCLK2
MBDATA2
Battery charge/discharge
Cap button
VGA thermal
system thermal
SUSB#
HWPG
CPU_PROCHOT#
SUSC#
M93_STRP
T5
NBSWON1#
LAN_REST#
EC_DEBUG1
EMU_LID
KBSMI#1
VRON
NUMLED#
EJECT#
T9
T10
OP_FAN_SEL
DNBSWON#1
CAPSLED#
PWR_LED#
ECPWROK
RSMRST#
VOLMUTE#
SPI_CLK
LID_EC#
CRY2
CRY1
C57 27P/50V
C50 27P/50V
32.768KHZ
Y1
C585 0.1U/10V_4
C587 4.7U/6.3V_6
For KB3926 C version
SI , add for DSM
PV, change from 18p to 27p
from vendor update
SI , change package
PV , change to test point
PV,reserve for identify M93-LP VGA chip
R71 10K/F_4 HWPG
R78 10K/F_4 NBSWON1#
R74 10K/F_4 SLPBTN#
R346 4.7K_4 MBCLK
R345 4.7K_4 MBDATA
RSMRST#
R336 *8.2K_4
C588 2.2U/6.3V_6
R65 *10K/F_4
Vari_ON
R68 10K/F_4
SI , enable Vari-bright
need pull low
C80 0.1U/10V_4
U17
BIOS_CS#
SPI_CLK
BIOS_WR#
BIOS_RD#
R89 33_4
R84 10K/F_4 SPI_3P
SPI_7P
R76 10K/F_4
MX25L1605DM2I-12G
MAX AKE38FP0Z00 2M byte
WINBOND AKE38FP0N01 SPI
EON AKE38ZA0Q00 BIOS
SOCKET DG008000031
R552 *1K/F_4
Project Model | GPIO42
AX 14" | High
AX 15.6" | Low
AX 17.3" | Middle (1.5V)
GPIO42 control fan table
R90 *10K/F_4
R79 10K/F_4
3920_RST#
R105 47K_4
C144 0.1U/10V_4
BLUELED
R41 100K/F_4
SCI1# D25 CH501H-40PT
DNBSWON#1 D12 RB500V-40
KBSMI#1 D27 RB500V-40
Change D12, D16 to RB500
for current loss
MAINON C464 2200P/50V_4
PV,add for EMI
+3VPCU_EC
+3VPCU
L13
*SBK160808T-680Y-N(0.3A,68)
U19
TPS73133
C114 4.7U/6.3V_6
C130 *1U/6.3V_4
C613 *1U/6.3V_4
+5VPCU
D26 1SS355
R109 100/F_4
R108 24.3K/F_4
C147 0.1U/10V_4
AD_ID
PROJECT : AX2/7
Quanta Computer Inc.
KB3926/ROM/TP
Rev 1A
Date: Thursday, December 24, 2009
Sheet 32 of 42
NB5/RD2

Mini PCI-E Card 1 WLAN



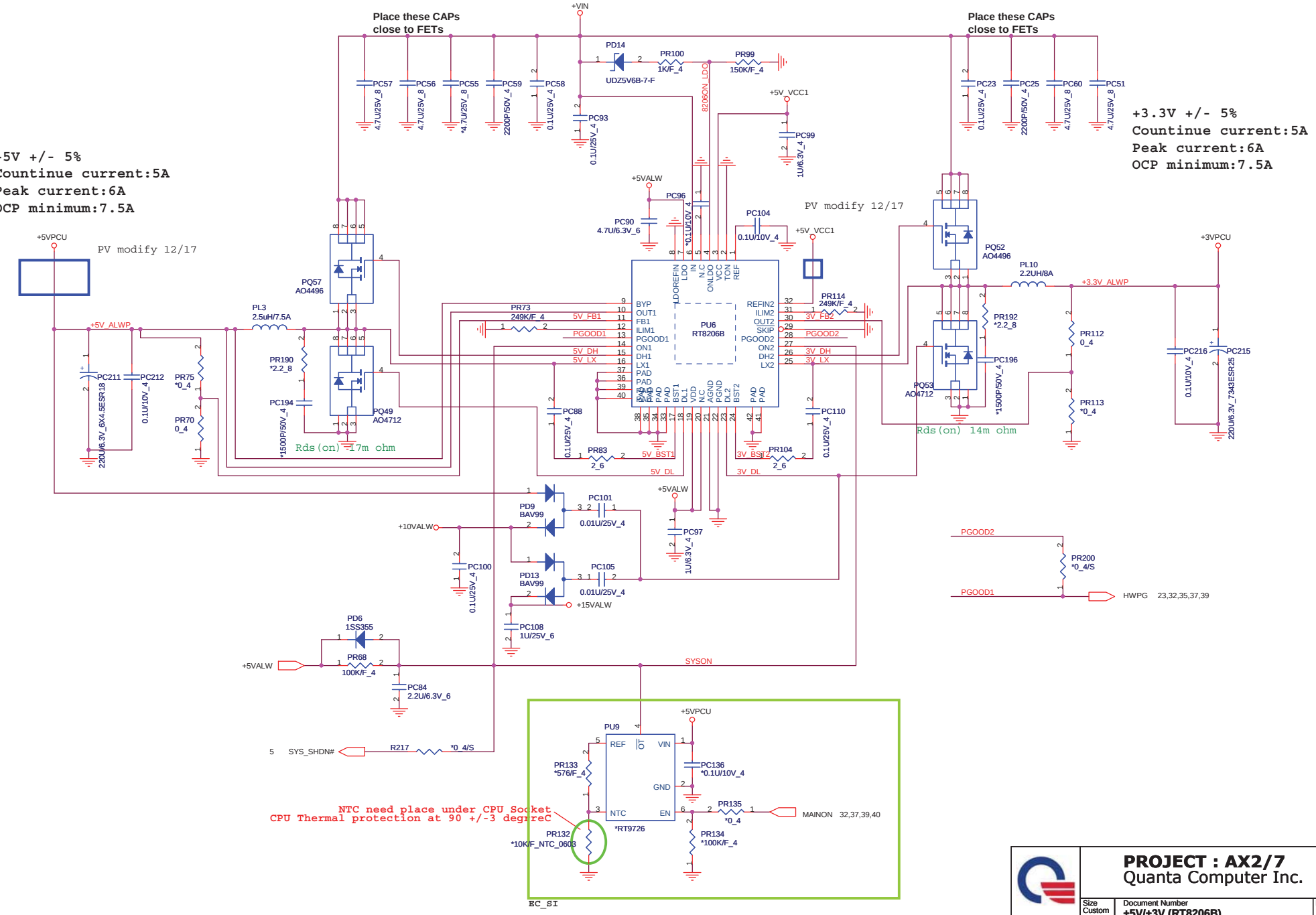


PROJECT :	AX2/7
	Quanta Computer Inc.
Size	Custom
Document Number	Mini CARD/LED
Rev	1A
Date:	Thursday, December 24, 2009
Sheet	33 of 42
	NB5/RD2

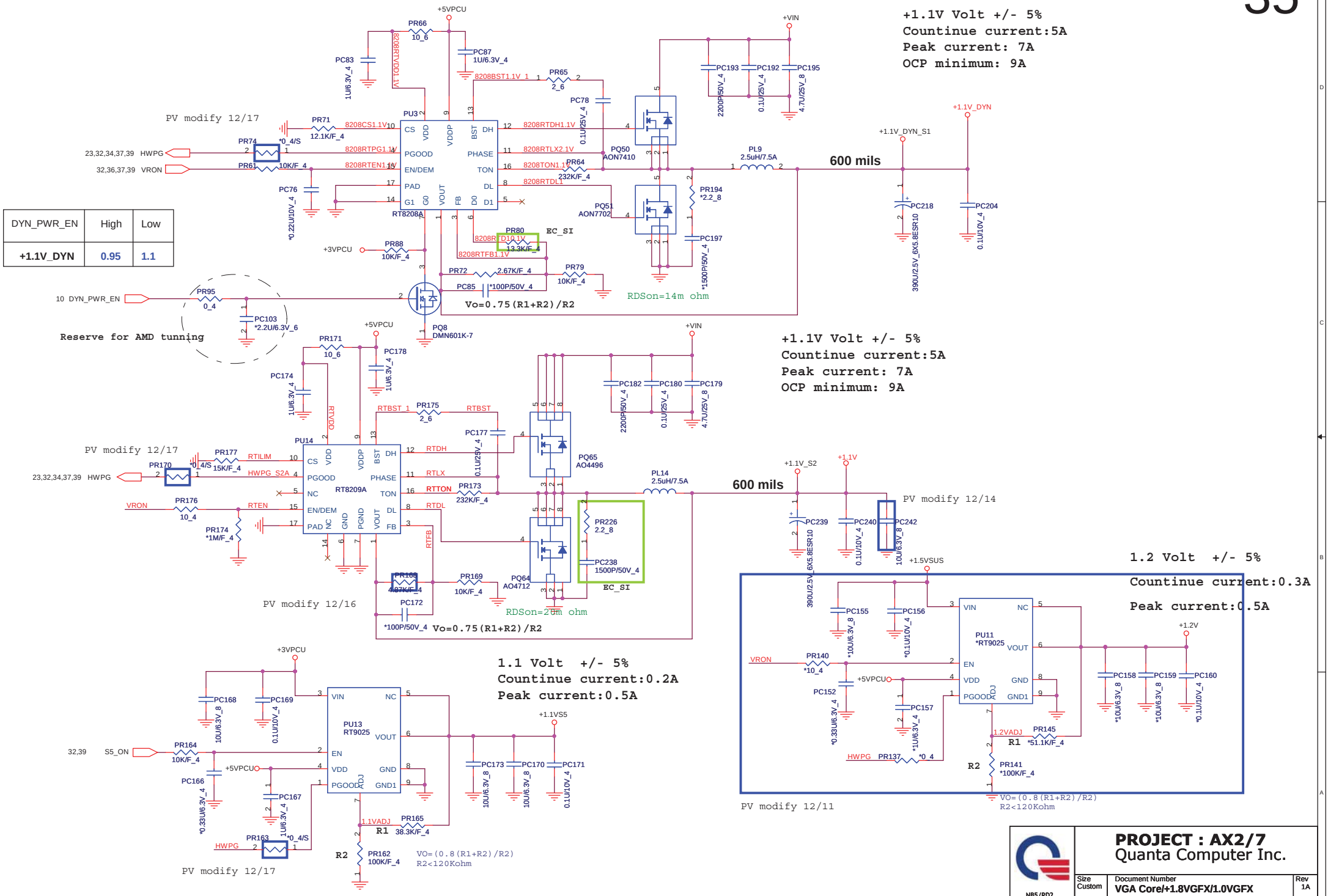
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A

+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A



NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Thursday, December 24, 2009	Sheet 34 of 42	



DYN_PWR_EN	High	Low
+1.1V_DYN	0.95	1.1

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	1A

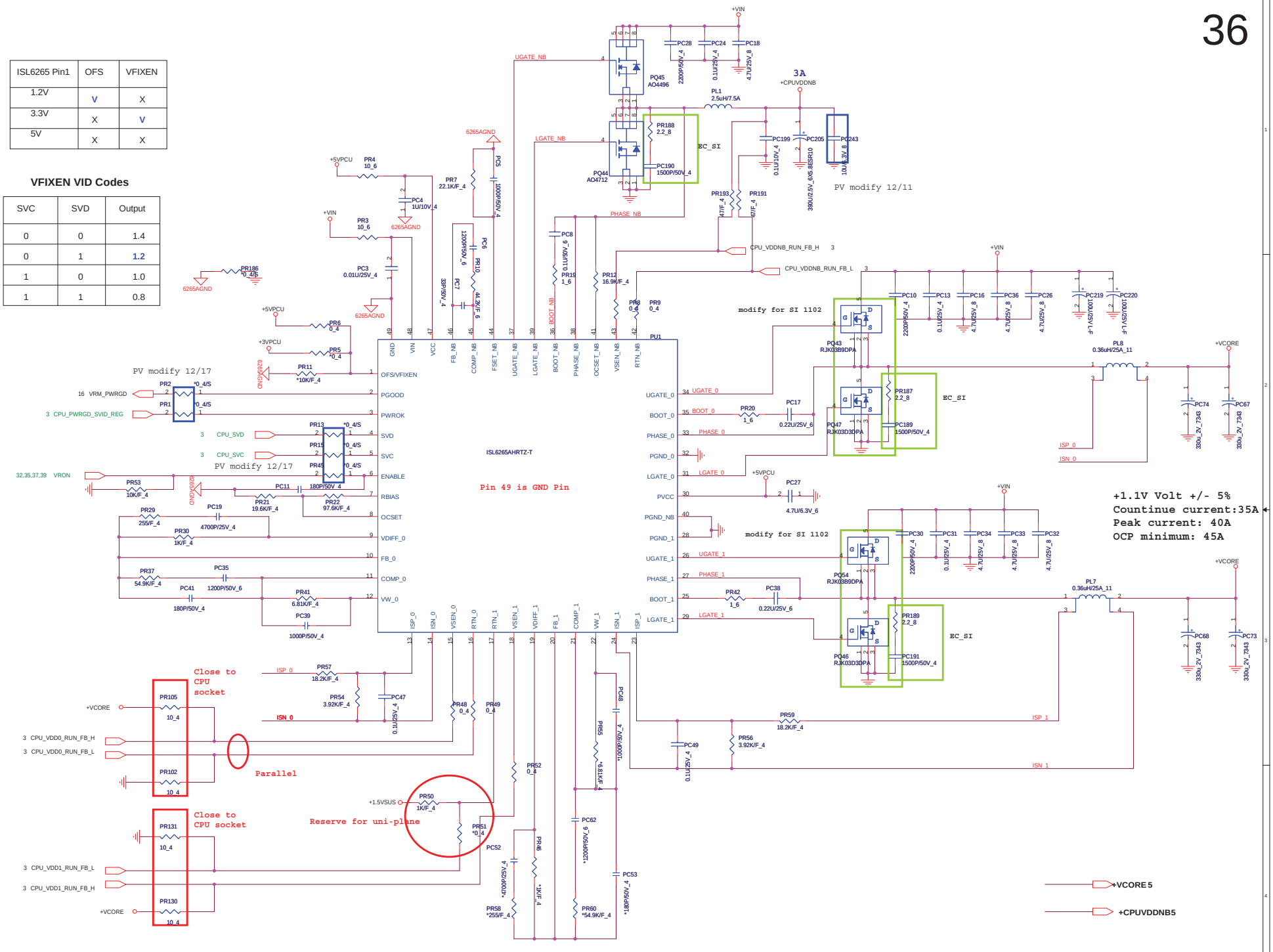
NB5/RD2

Date: Thursday, December 24, 2009 | Sheet 35 of 42

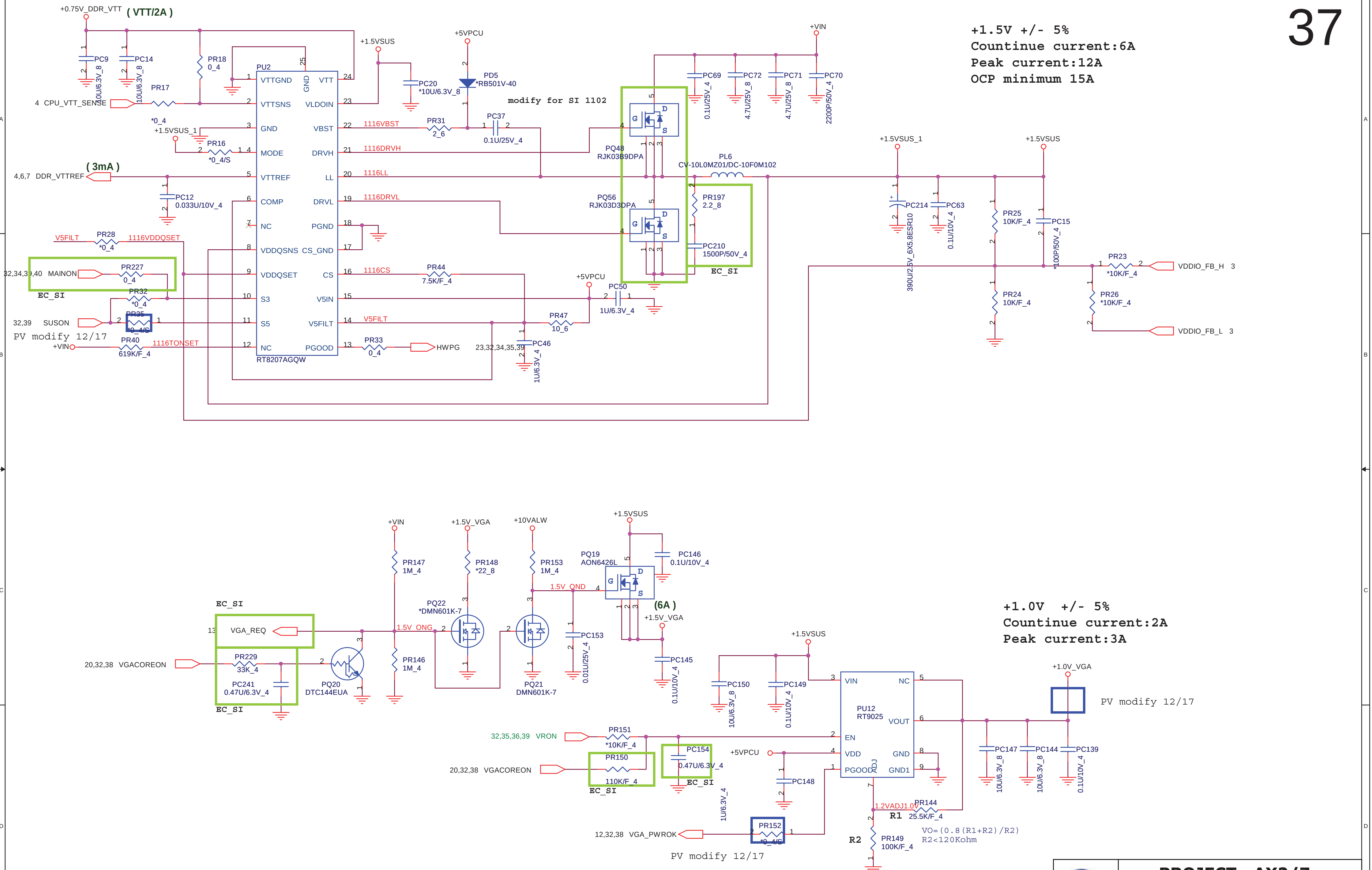
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A



+1.0V +/- 5%
Countinue current:2A
Peak current:3A

PROJECT : AX2/7
Quanta Computer Inc.
SANTOS INTEL

Size	Document Number	Rev
	DDR3 (RT8207)	1A

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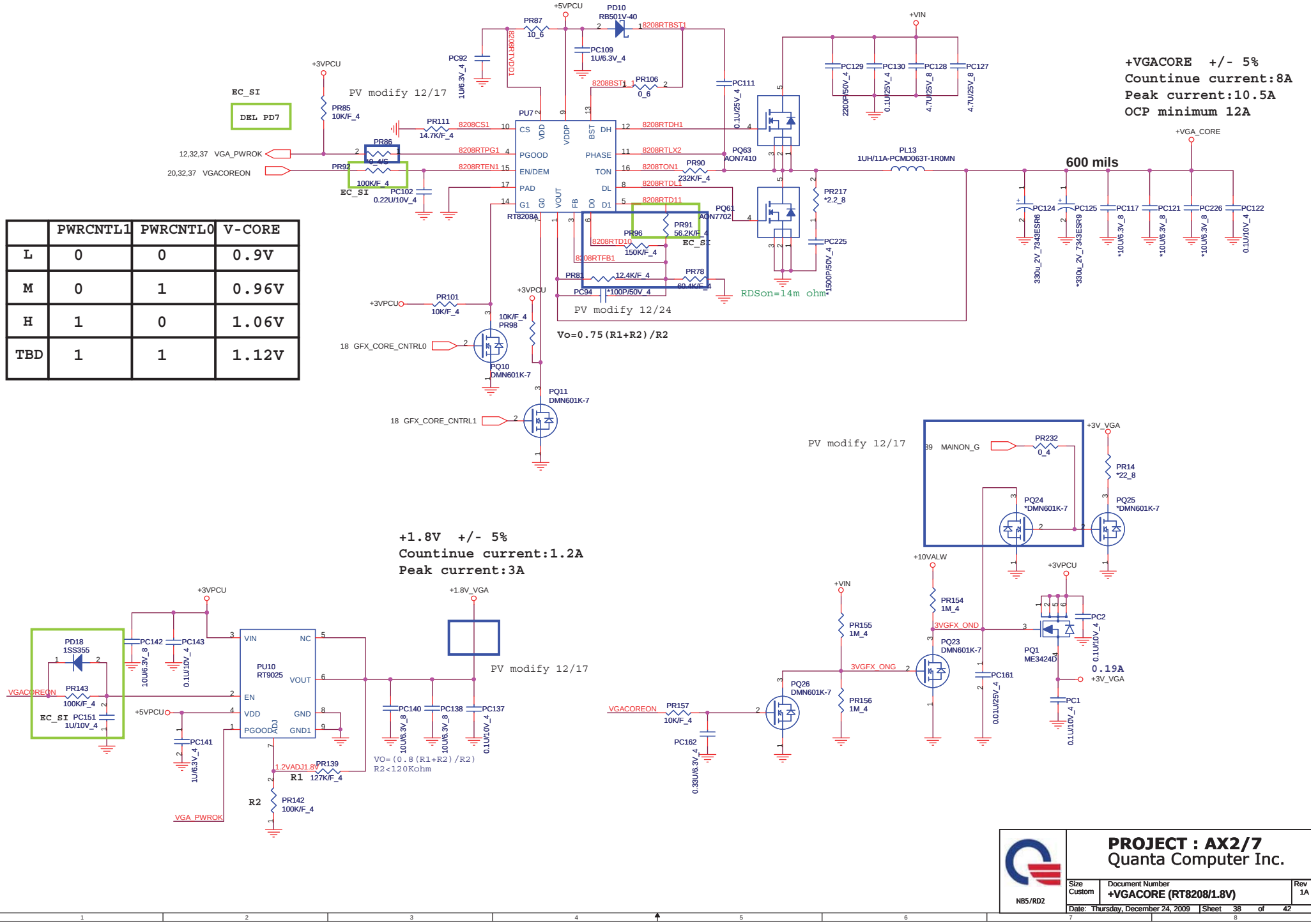
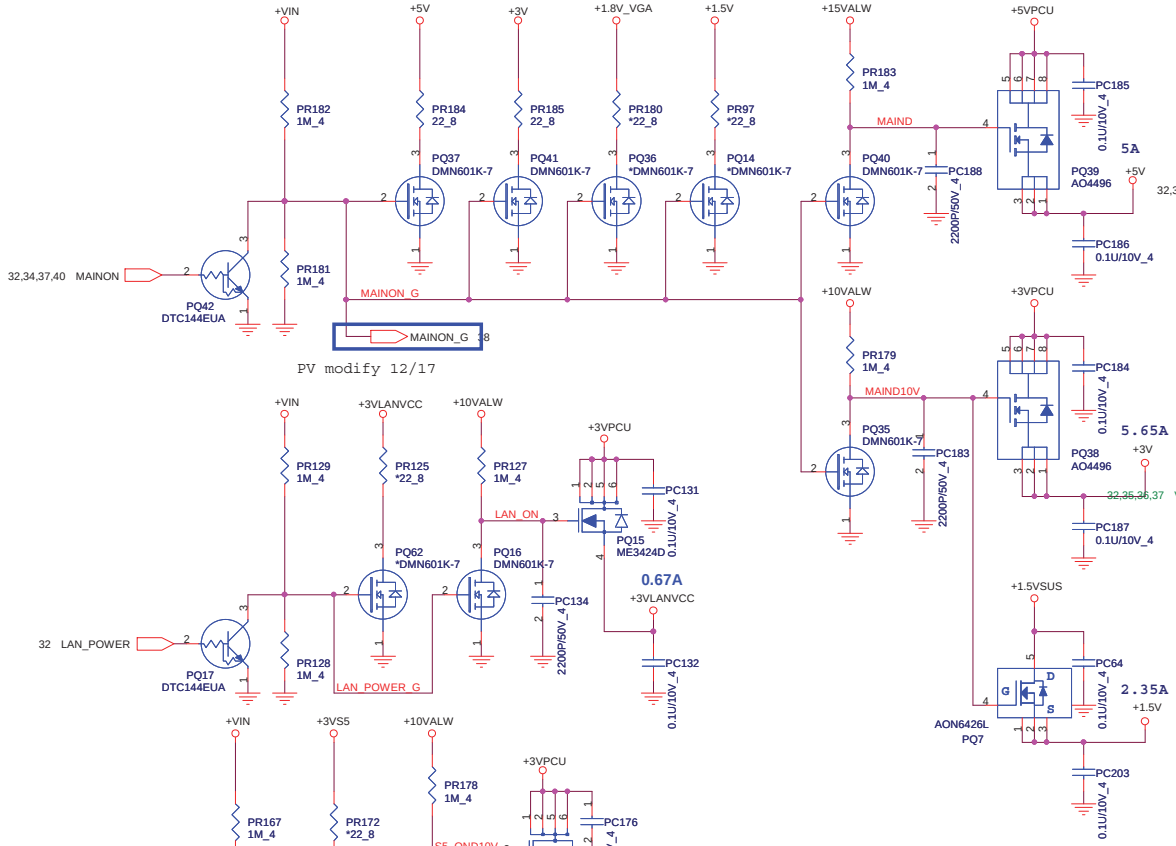
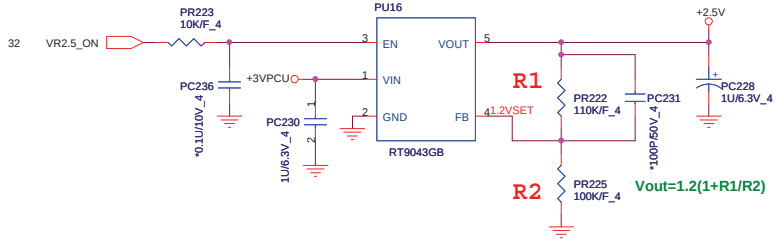
VGA Core

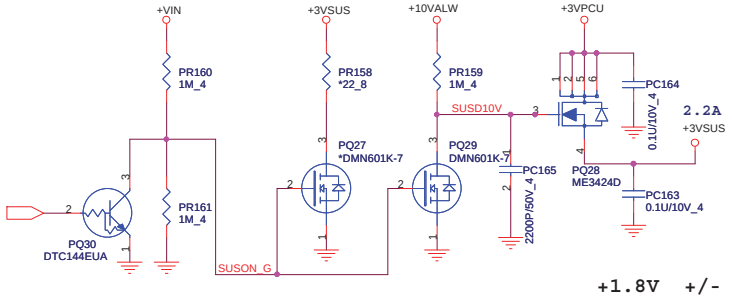


	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V

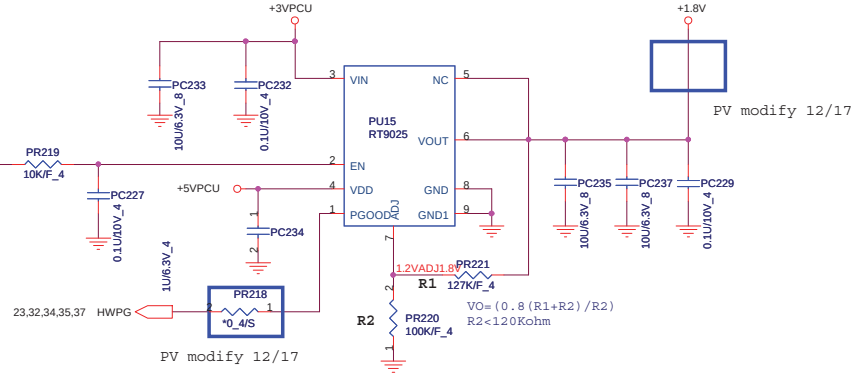


+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA

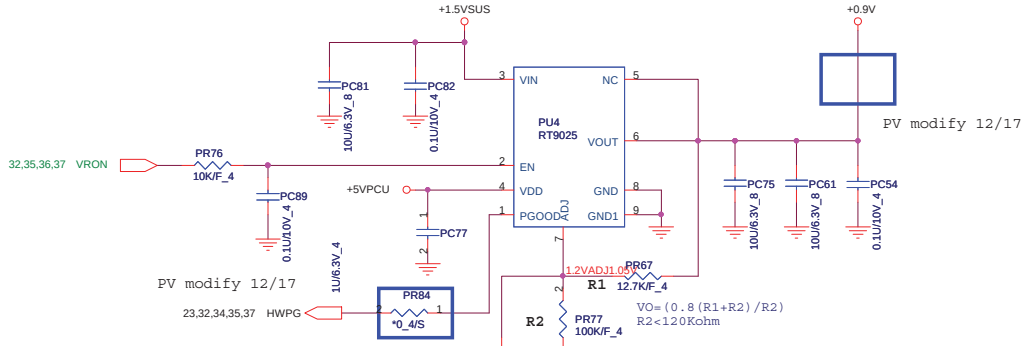


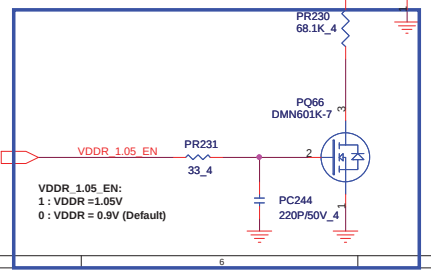


+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A



+0.9V +/- 5%
Countinue current:1.5A
Peak current:2A





PV modify 12/16

For VDDR 1.05 control

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	?
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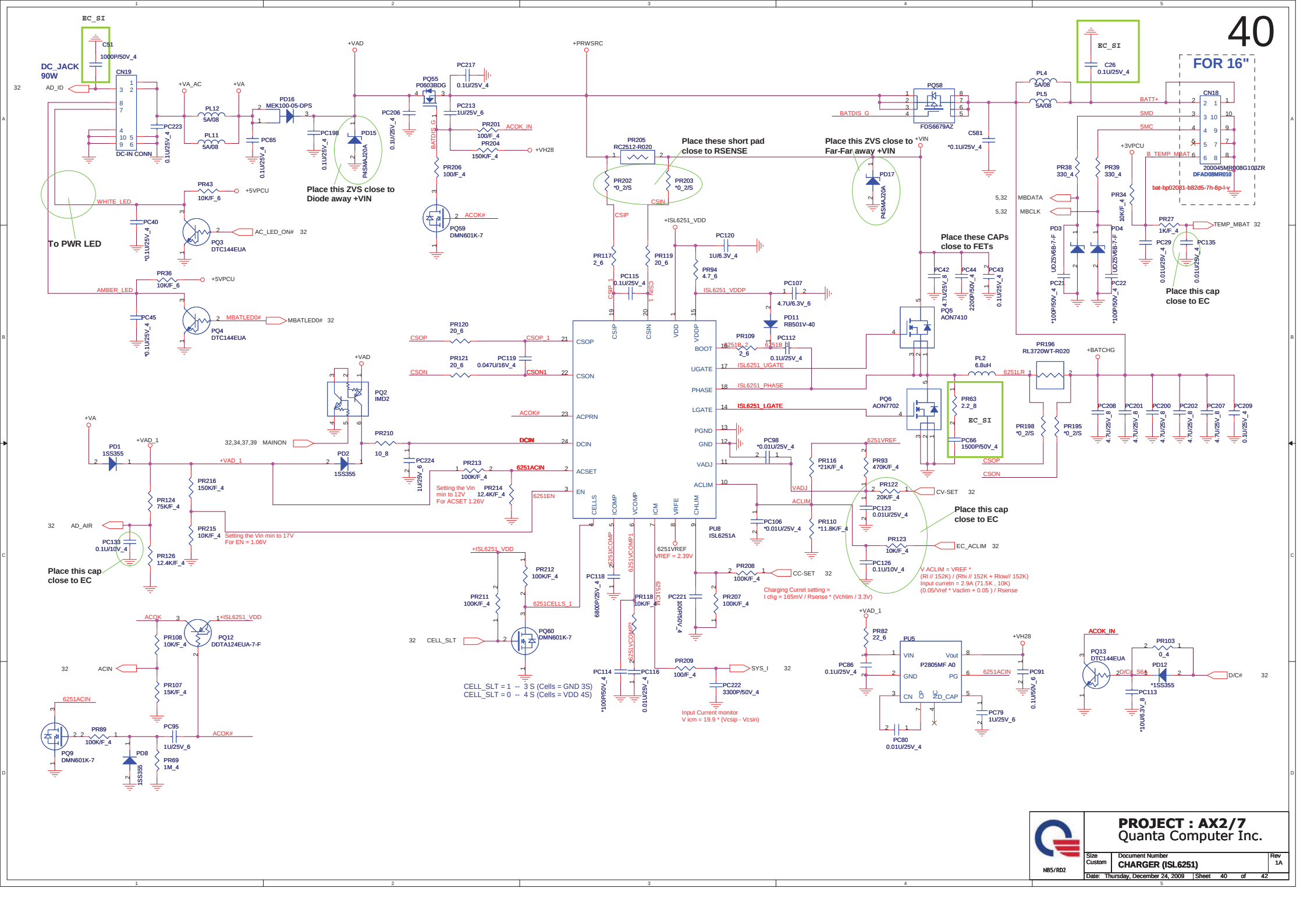
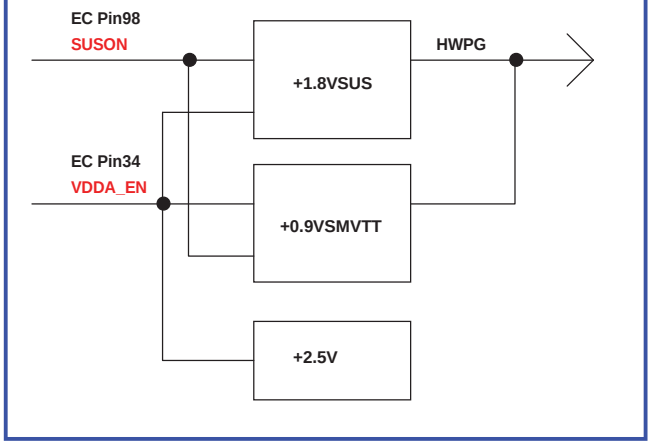
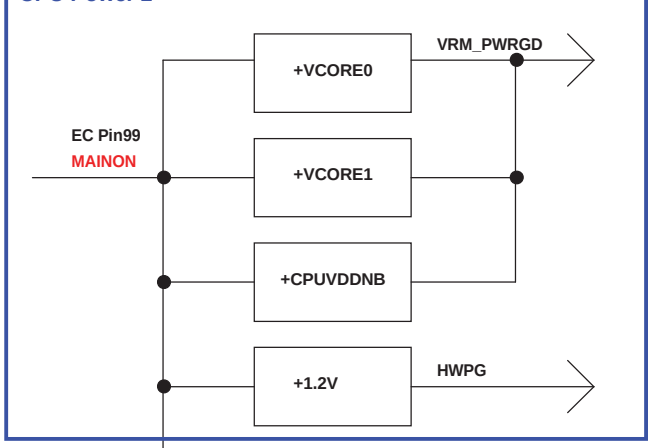
NB5/RD2

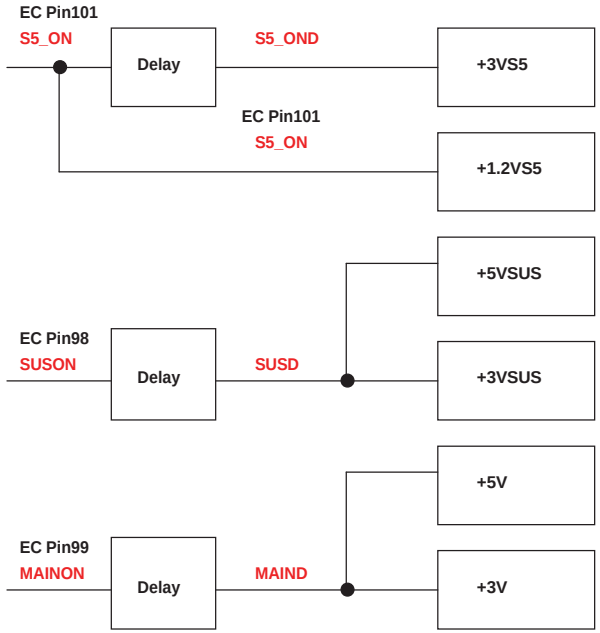

DC_JACK 90W
DC-IN CONN
To PWR LED
Place this ZVS close to Diode away +VIN
Place these short pad close to RSENSE
Place this ZVS close to Far-Far away +VIN
Place these CAPs close to FETs
Place this cap close to EC
FOR 16"
ISL6251A
Setting the Vin min to 12V For ACSET 1.26V
Setting the Vin min to 17V For EN = 1.06V
Charging Curret setting = I chg = 165mV / Rsense * (Vchlim / 3.3V)
V ACLIM = VREF * (RI // 152K) / (Rhi // 152K + Rlow// 152K) Input curretn = 2.9A (71.5K , 10K) (0.05/Vref * Vaclim + 0.05) / Rsense
CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)
Input Current monitor V icm = 19.9 * (Vcsip - Vcsin)
PROJECT : AX2/7
Quanta Computer Inc.
NB5/RD2
CHARGER (ISL6251)
Thursday, December 24, 2009

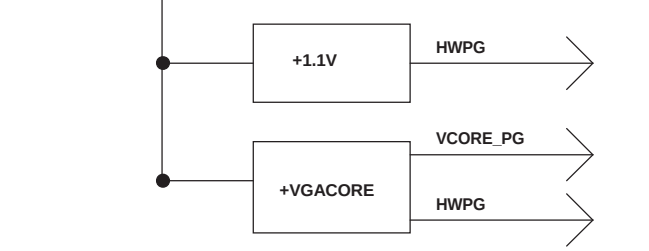
CPU Power 1

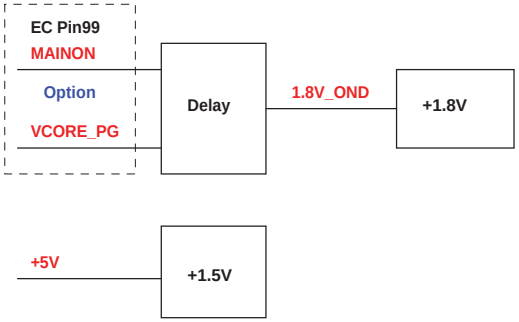


CPU Power 2









1 S5_ON S5_OND RSMRST# → 2 SUSON SUSD → 3 MAINON MAIND → 4 HWPG VCORE_PG VRM_PWRGD → EC Pin76 ECPWROK Delay 600ms → SB_PWRGD_IN 3.3V → NB_PWRGD_IN 1.8V

NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Power control**	3A

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Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

Custom<Doc>
NB5/RD2

PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
		1A

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