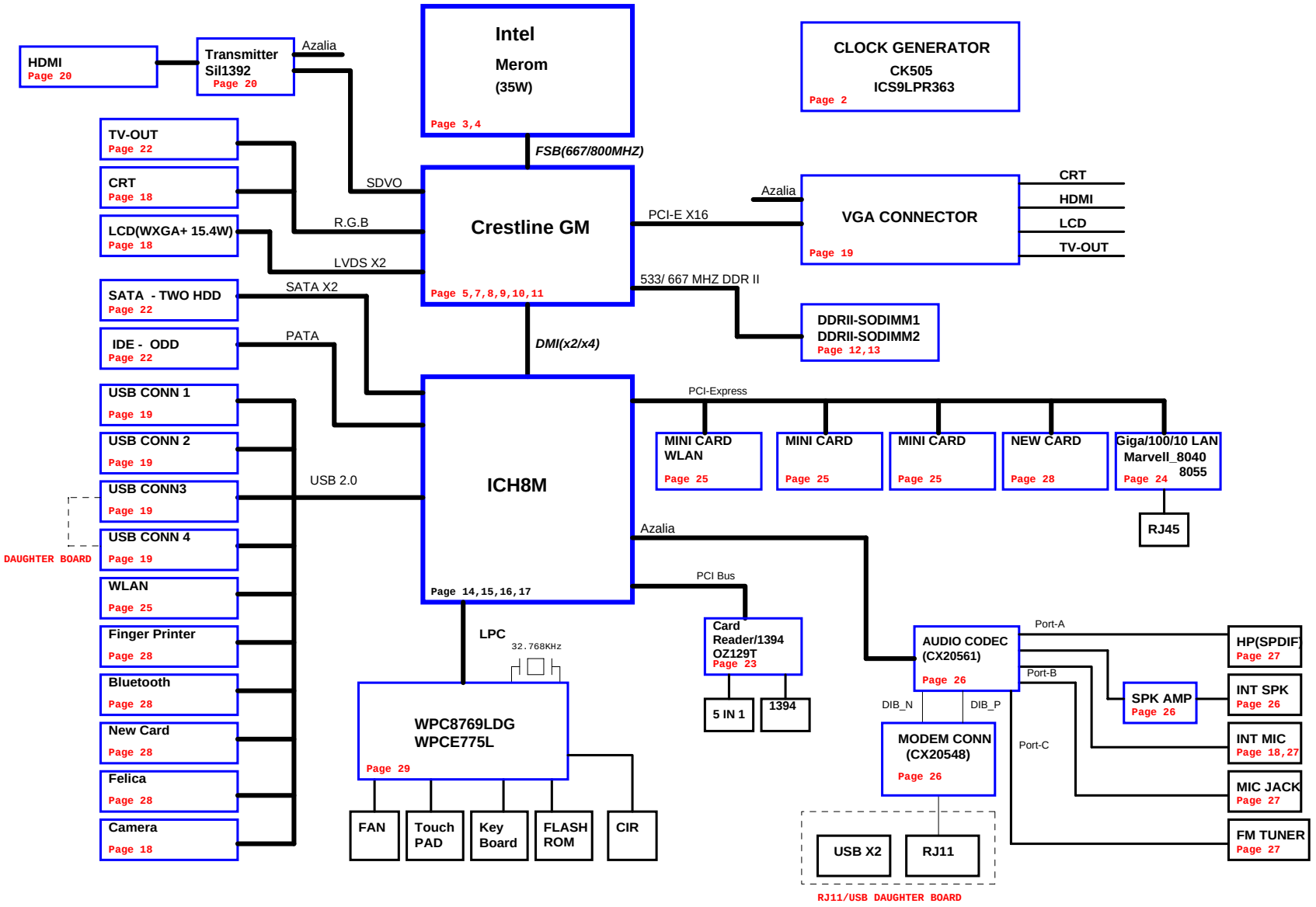
BL5S Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
  +3V_S5
  +3VSUS
  +3V
  +5VPCU
  +5V_S5
  +5V
  SMDDR_VTERM
  SMDDR_VREF



Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Block Diagram	1A

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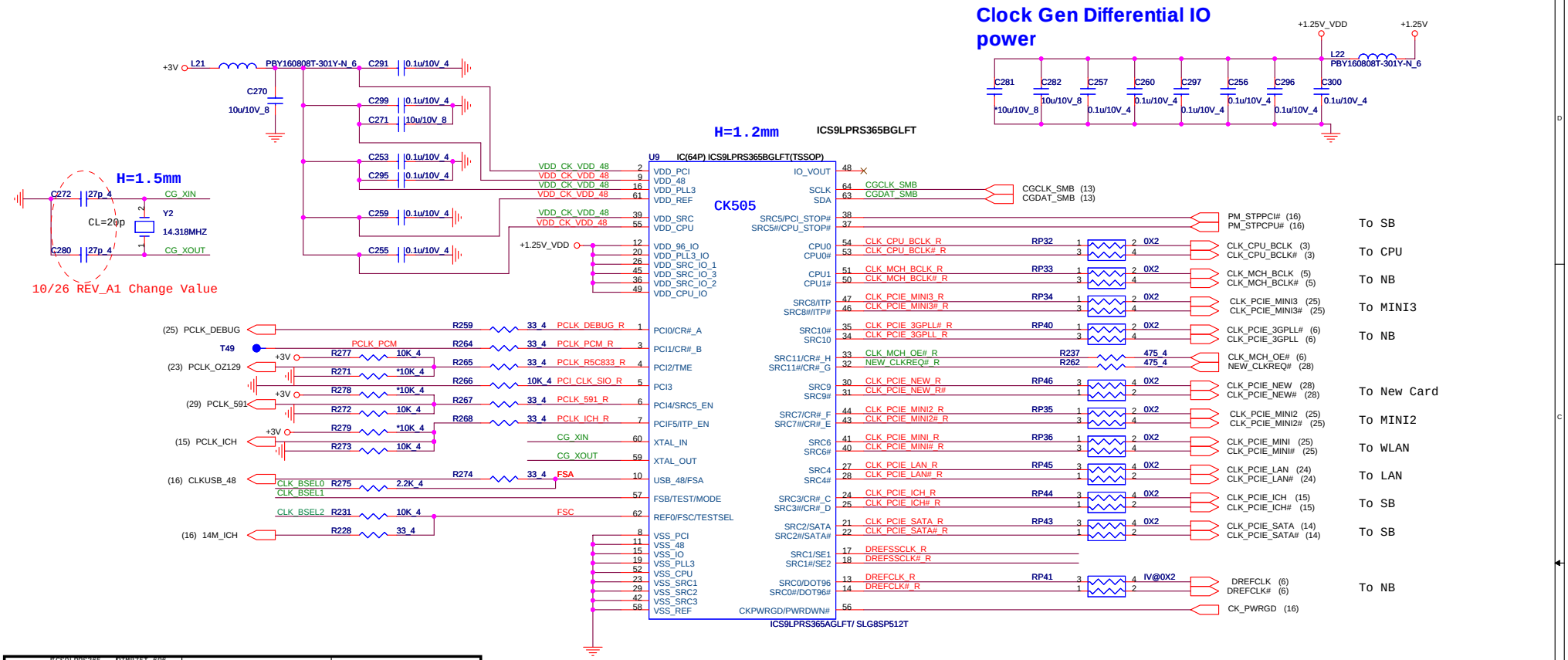
Clock Generator



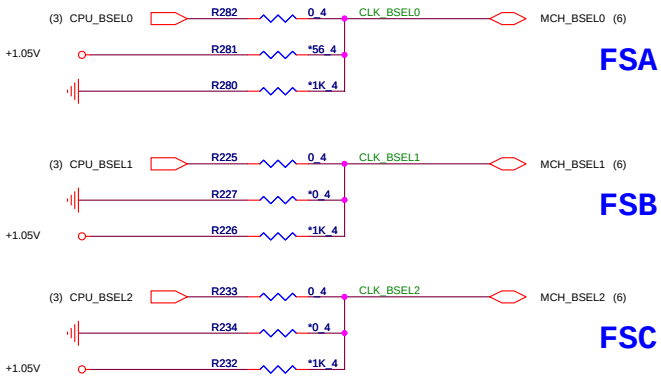
Clock Gen Differential IO power

	ICS9LPRS365 (ALPRS365K13)	RTM8751-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

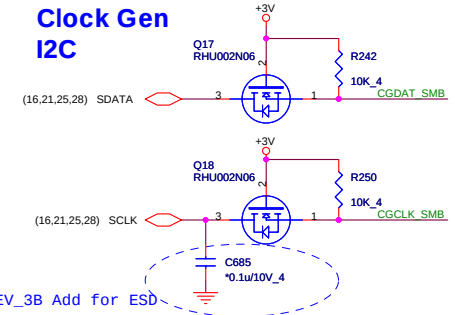
CPU Clock select

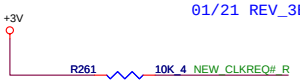
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C





Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	CLK. GEN./ CK505	1A

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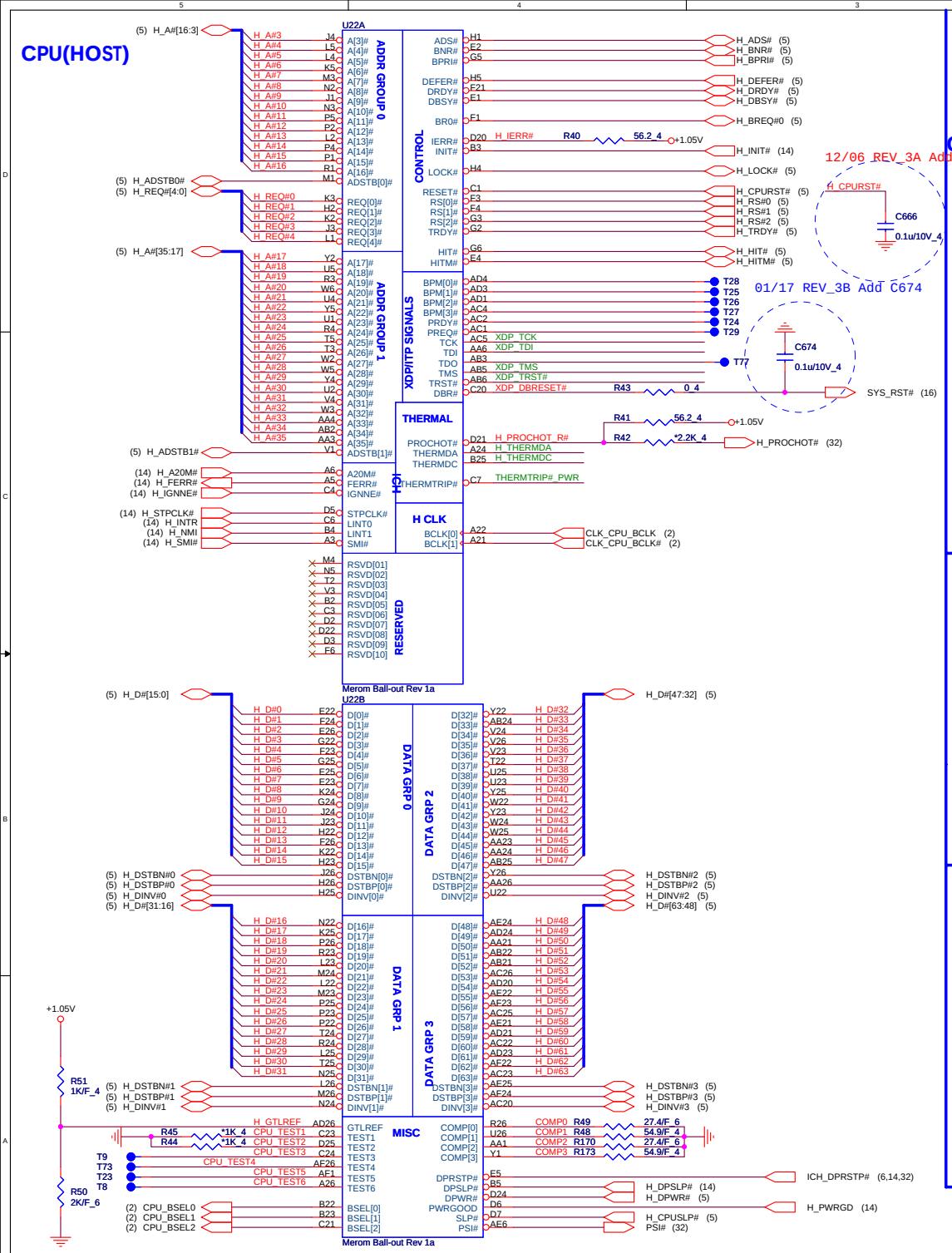
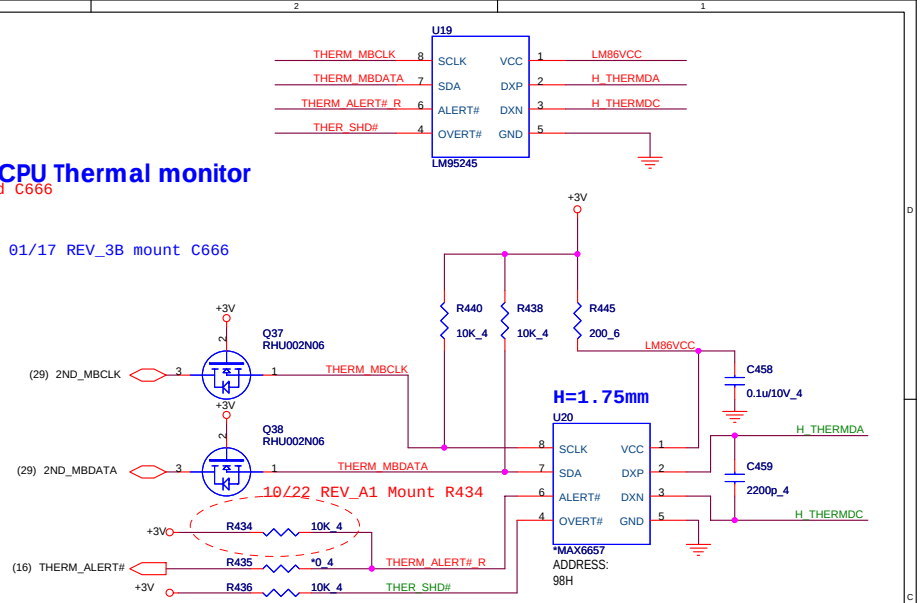
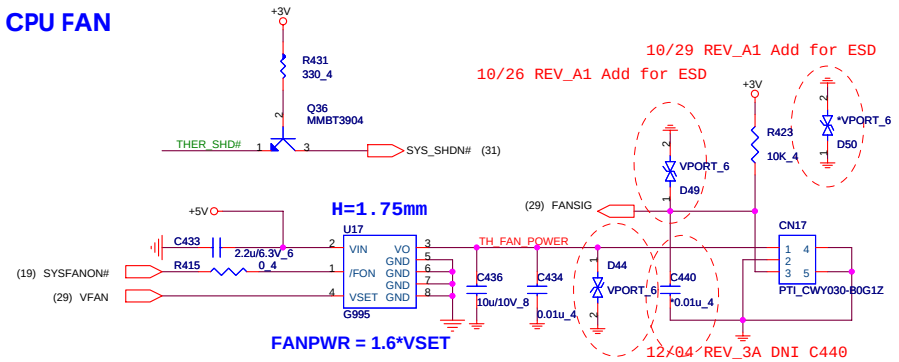
CPU(HOST)



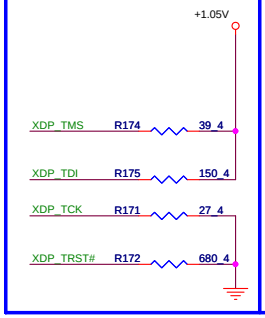
CPU Thermal monitor



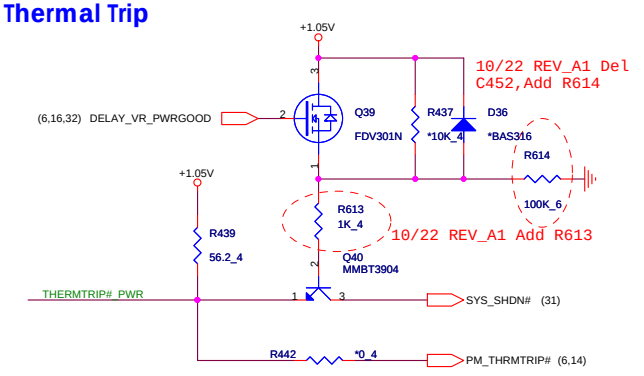
CPU FAN



PU/PD (ITP700)



Thermal Trip



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PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	CPU(1 of 2)/FAN/Thermal		1A
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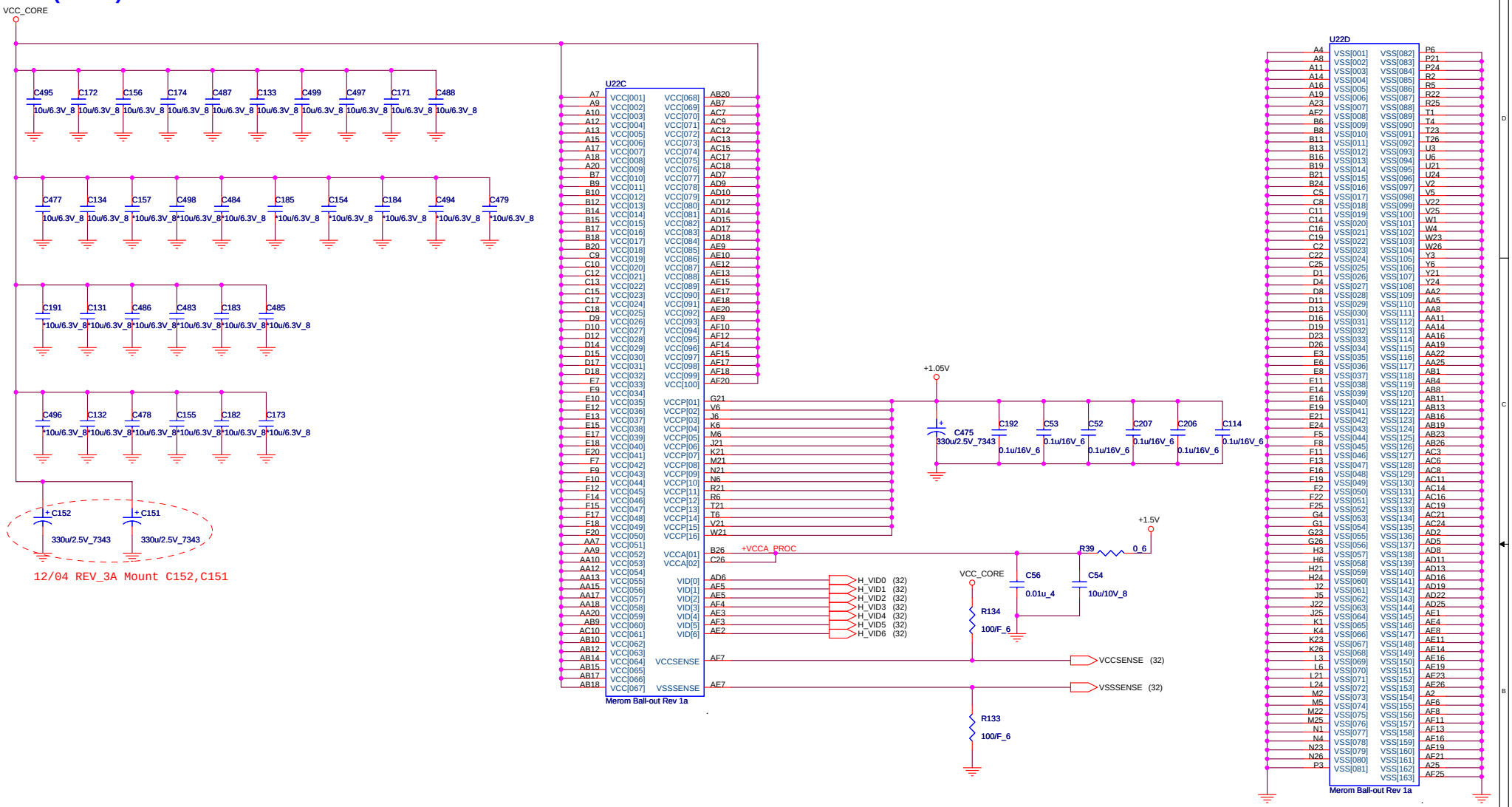
CPU(Power)



12/04 REV_3A Mount C152,C151

Quanta Computer Inc.		
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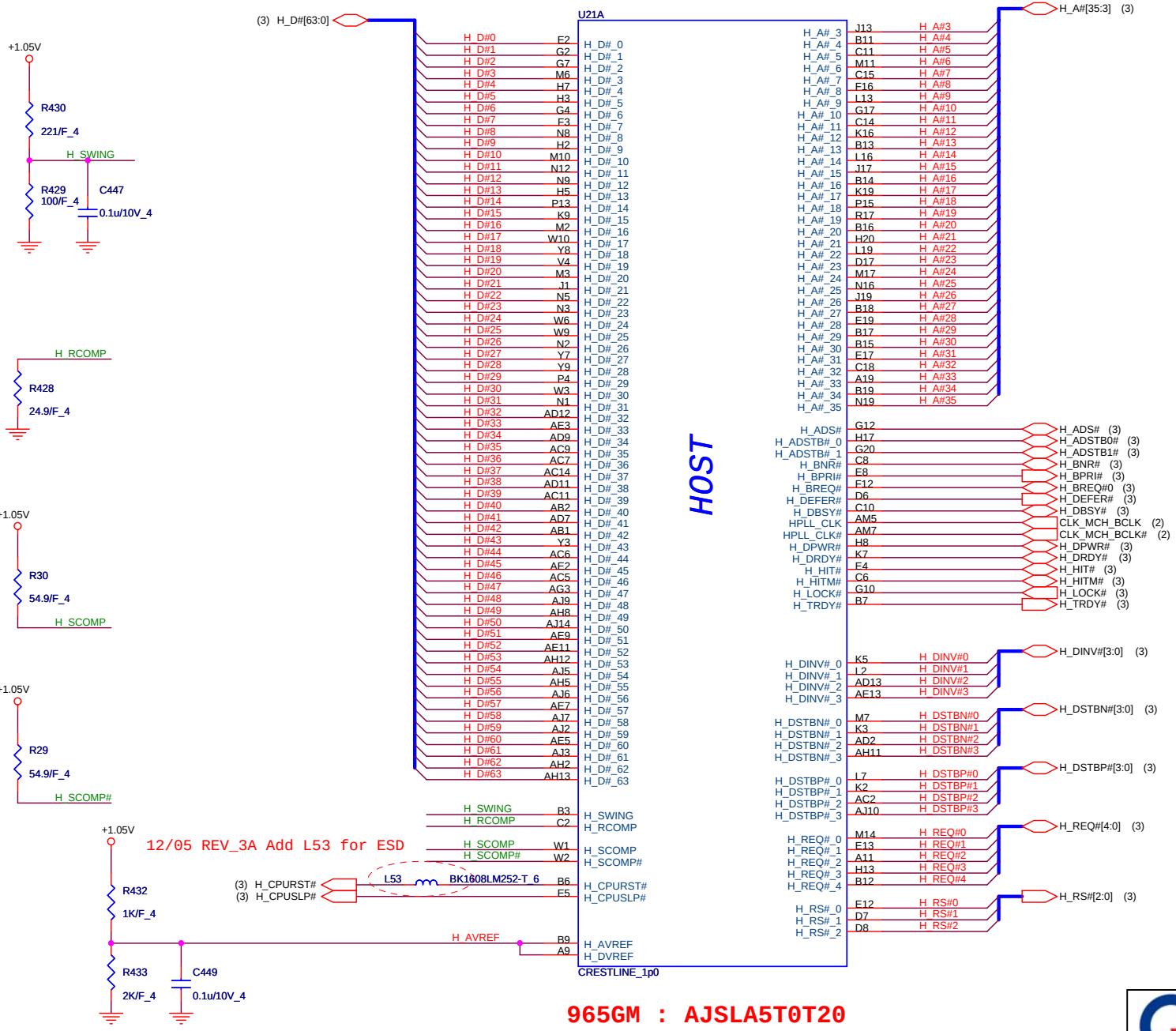
NB(HOST)



965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GL : AJSLA5V0T09

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Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A
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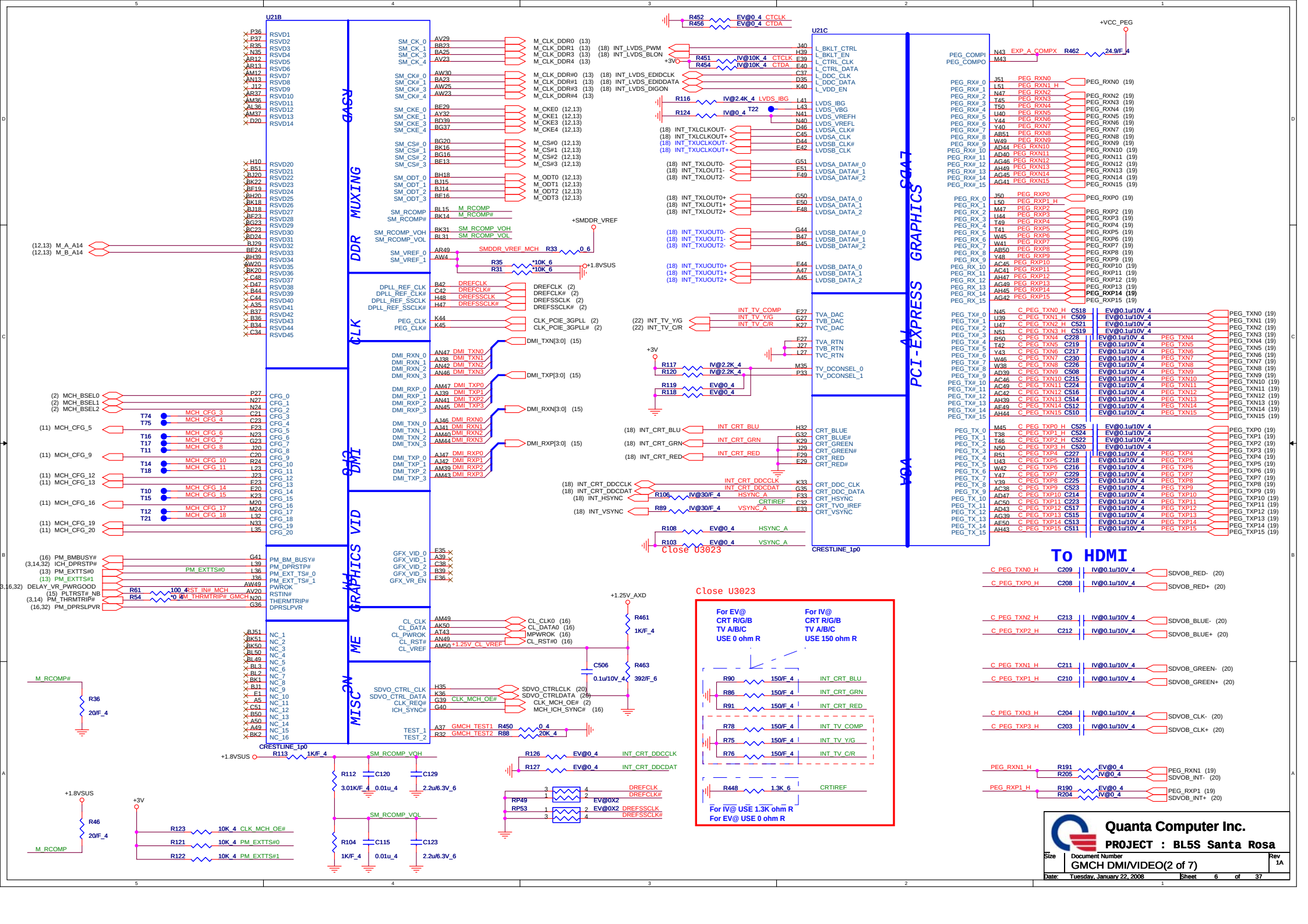
U21B
EASY
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
U21C
PCI-EXPRESS GRAPHICS
VGA
CRESTLINE_1p0
Close U3023
For EV@ CRT R/G/B TV A/B/C USE 0 ohm R
For IV@ CRT R/G/B TV A/B/C USE 150 ohm R
For IV@ USE 1.3K ohm R
For EV@ USE 0 ohm R
To HDMI
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GMCH DMI/VIDEO(2 of 7)
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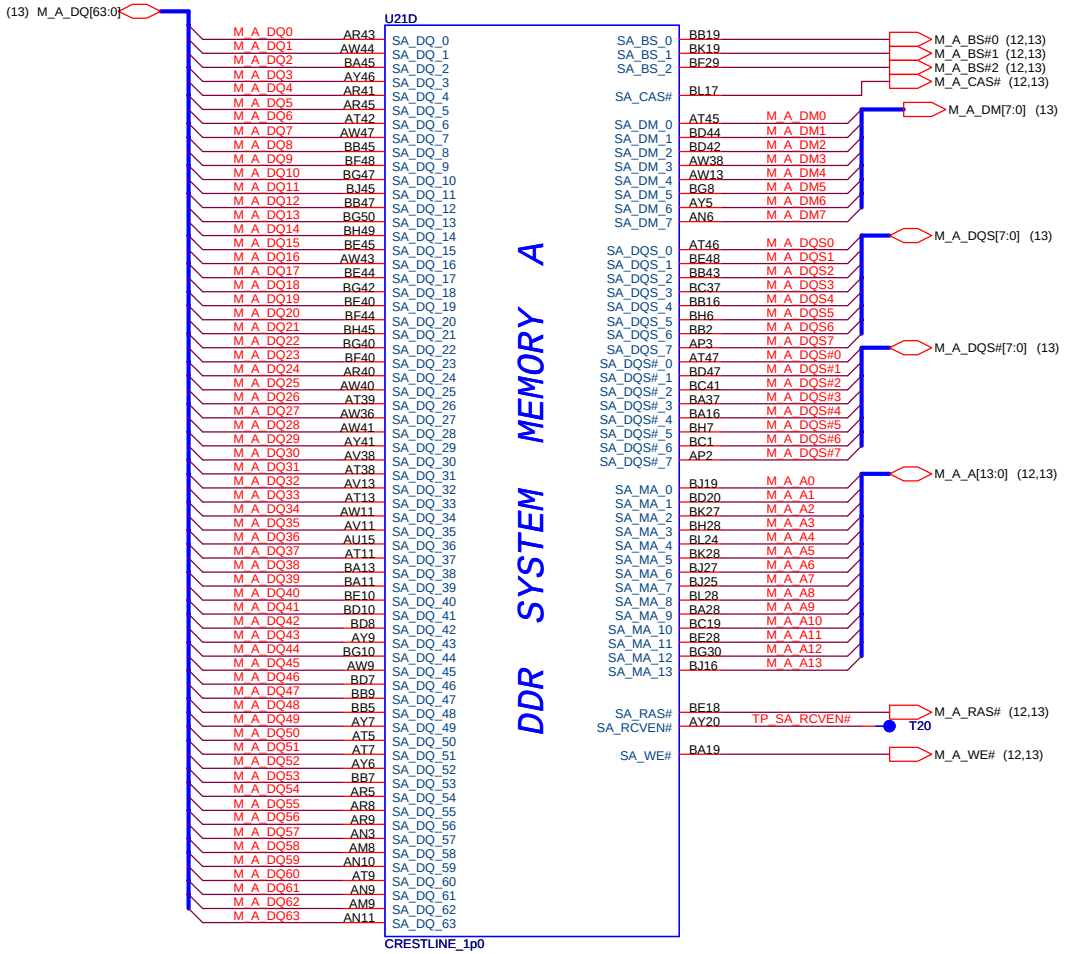
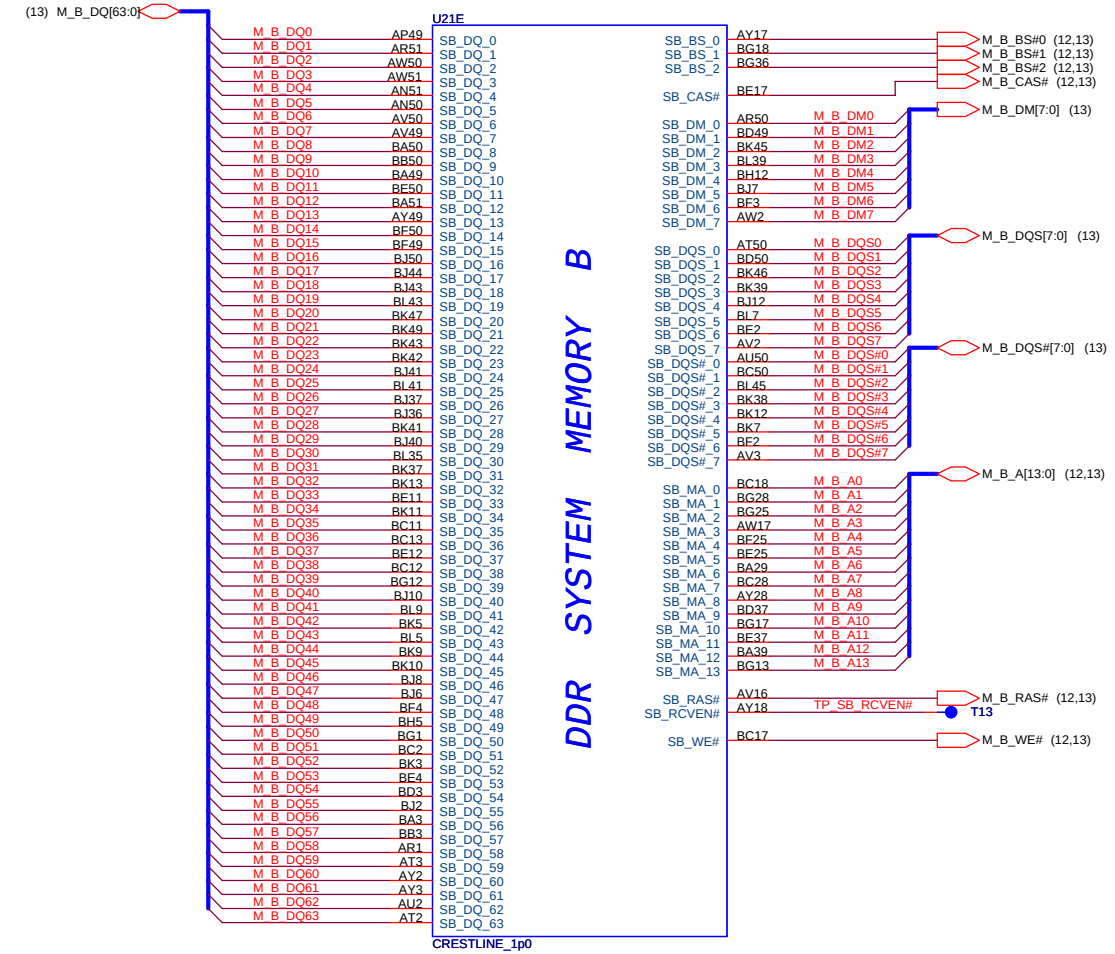
NB(Memory controller)





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Size	Document Number	Rev
	MCH DDR(3 of 7)	1A

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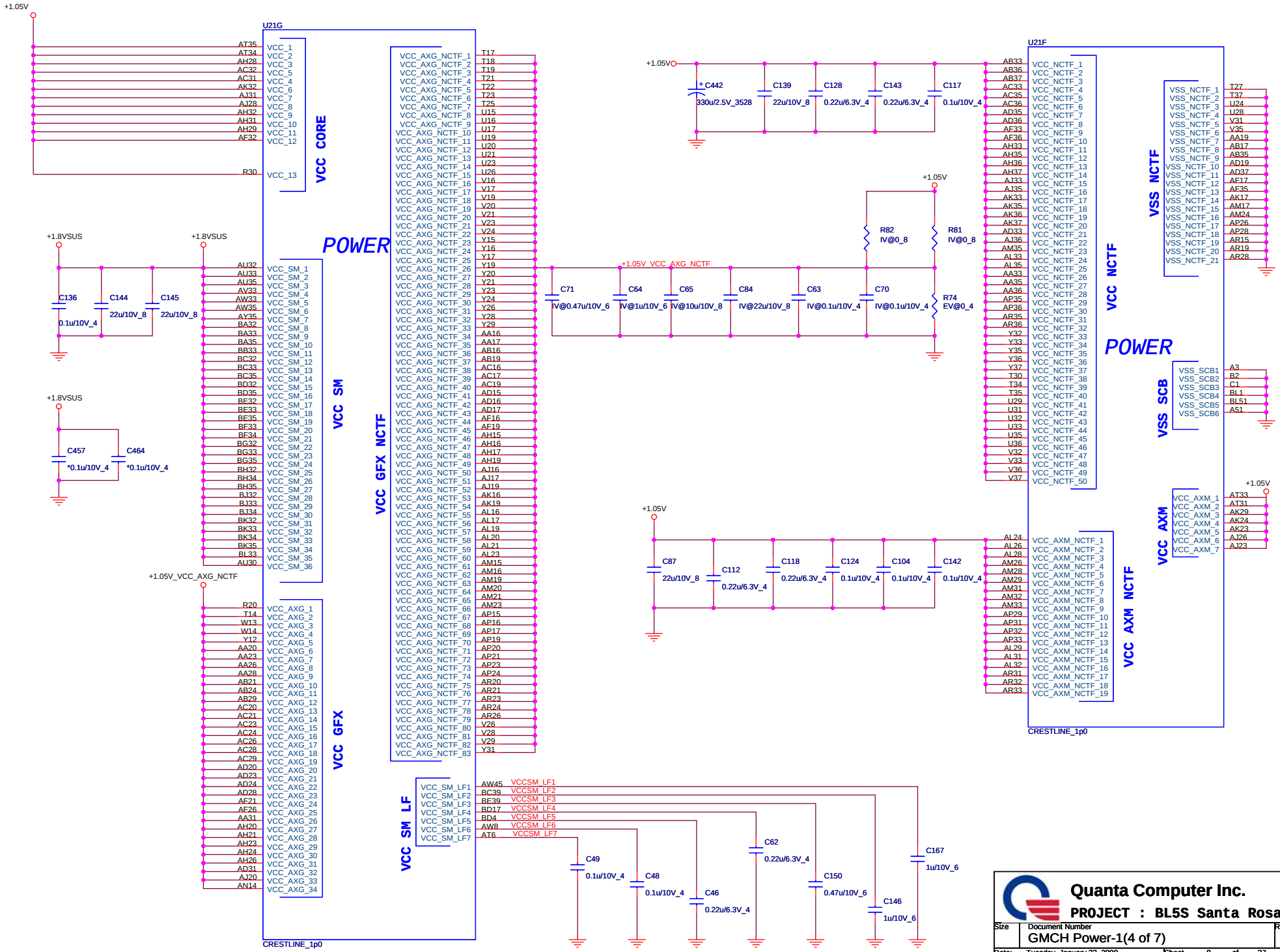
NB(Power-1)


+1.05V
U21G
VCC CORE
VCC_1
VCC_2
VCC_3
VCC_5
VCC_4
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
R30
POWER
+1.8VSUS
VCC SM
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36
C136
0.1u/10V_4
C144
22u/10V_8
C145
22u/10V_8
C457
*0.1u/10V_4
C464
*0.1u/10V_4
+1.05V_VCC_AXG_NCTF
VCC GFX
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC GFX NCTF
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
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VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
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VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
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VCC_AXG_NCTF_33
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VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
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VCC_AXG_NCTF_40
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VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
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VCC_AXG_NCTF_63
VCC_AXG_NCTF_64
VCC_AXG_NCTF_65
VCC_AXG_NCTF_66
VCC_AXG_NCTF_67
VCC_AXG_NCTF_68
VCC_AXG_NCTF_69
VCC_AXG_NCTF_70
VCC_AXG_NCTF_71
VCC_AXG_NCTF_72
VCC_AXG_NCTF_73
VCC_AXG_NCTF_74
VCC_AXG_NCTF_75
VCC_AXG_NCTF_76
VCC_AXG_NCTF_77
VCC_AXG_NCTF_78
VCC_AXG_NCTF_79
VCC_AXG_NCTF_80
VCC_AXG_NCTF_81
VCC_AXG_NCTF_82
VCC_AXG_NCTF_83
VCC SM LF
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCCSM_LF1
VCCSM_LF2
VCCSM_LF3
VCCSM_LF4
VCCSM_LF5
VCCSM_LF6
VCCSM_LF7
C49
0.1u/10V_4
C48
0.1u/10V_4
C46
0.22u/6.3V_4
C62
0.22u/6.3V_4
C150
0.47u/10V_6
C146
1u/10V_6
C167
1u/10V_6
CRESTLINE_1p0
+1.05V_VCC_AXG_NCTF
C71
IV@0.47u/10V_6
C64
IV@1u/10V_6
C65
IV@10u/10V_8
C84
IV@22u/10V_8
C63
IV@0.1u/10V_4
C70
IV@0.1u/10V_4
R82
IV@0_8
R81
IV@0_8
R74
EV@0_4
+1.05V
C442
330u/2.5V_3528
C139
22u/10V_8
C128
0.22u/6.3V_4
C143
0.22u/6.3V_4
C117
0.1u/10V_4
U21F
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
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VCC_NCTF_35
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VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC_NCTF_45
VCC_NCTF_46
VCC_NCTF_47
VCC_NCTF_48
VCC_NCTF_49
VCC_NCTF_50
VCC NCTF
VSS NCTF
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
POWER
VSS SCB
VSS_SCB1
VSS_SCB2
VSS_SCB3
VSS_SCB4
VSS_SCB5
VSS_SCB6
VCC AXM
VCC_AXM_1
VCC_AXM_2
VCC_AXM_3
VCC_AXM_4
VCC_AXM_5
VCC_AXM_6
VCC_AXM_7
VCC AXM NCTF
VCC_AXM_NCTF_1
VCC_AXM_NCTF_2
VCC_AXM_NCTF_3
VCC_AXM_NCTF_4
VCC_AXM_NCTF_5
VCC_AXM_NCTF_6
VCC_AXM_NCTF_7
VCC_AXM_NCTF_8
VCC_AXM_NCTF_9
VCC_AXM_NCTF_10
VCC_AXM_NCTF_11
VCC_AXM_NCTF_12
VCC_AXM_NCTF_13
VCC_AXM_NCTF_14
VCC_AXM_NCTF_15
VCC_AXM_NCTF_16
VCC_AXM_NCTF_17
VCC_AXM_NCTF_18
VCC_AXM_NCTF_19
C87
22u/10V_8
C112
0.22u/6.3V_4
C118
0.22u/6.3V_4
C124
0.1u/10V_4
C104
0.1u/10V_4
C142
0.1u/10V_4
CRESTLINE_1p0
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Size
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NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL INTERNAL

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

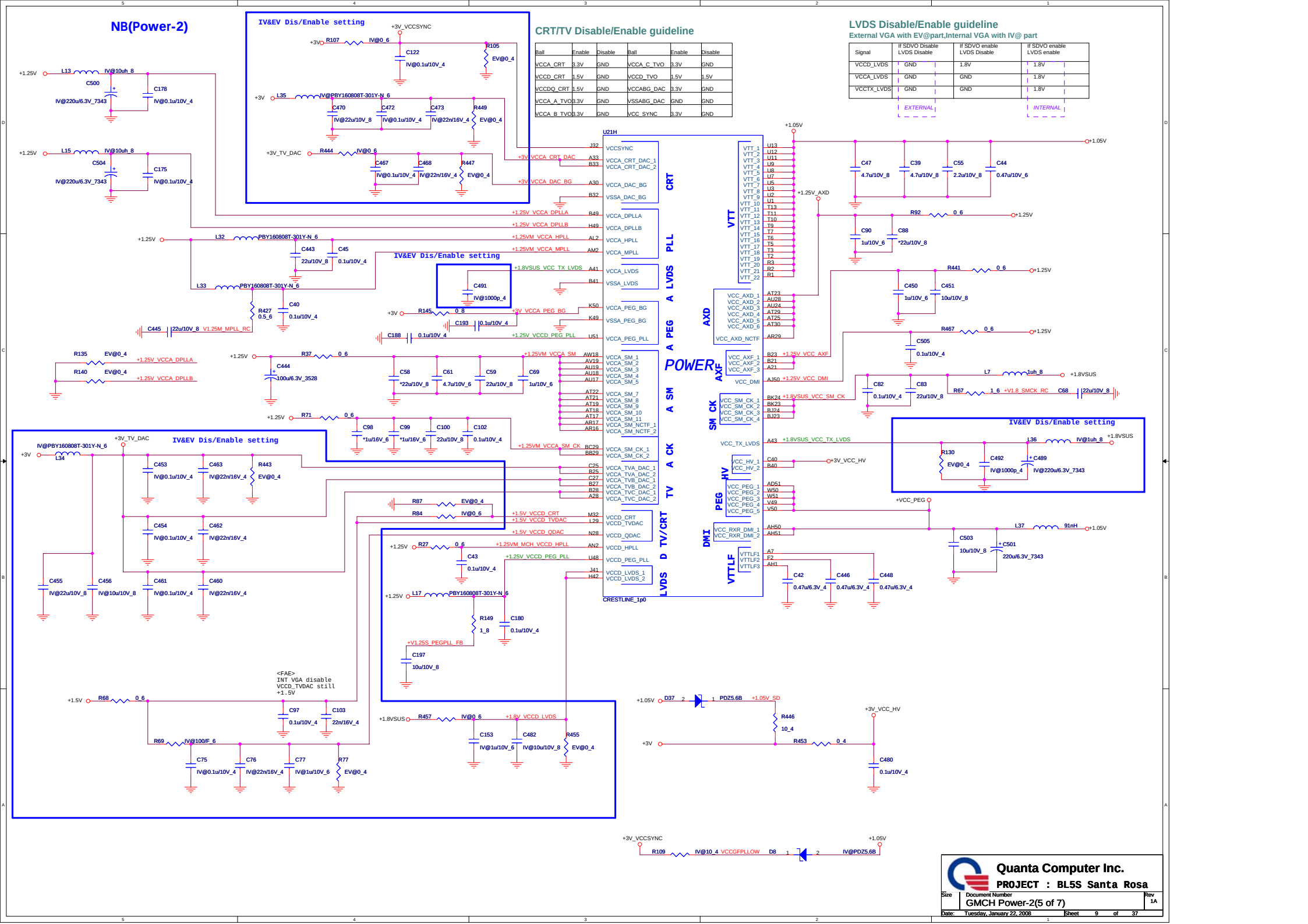
IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

U21H

CRESTLINE_1p0

<FAE>
INT VGA disable
VCCD_TVDAC still
+1.5V



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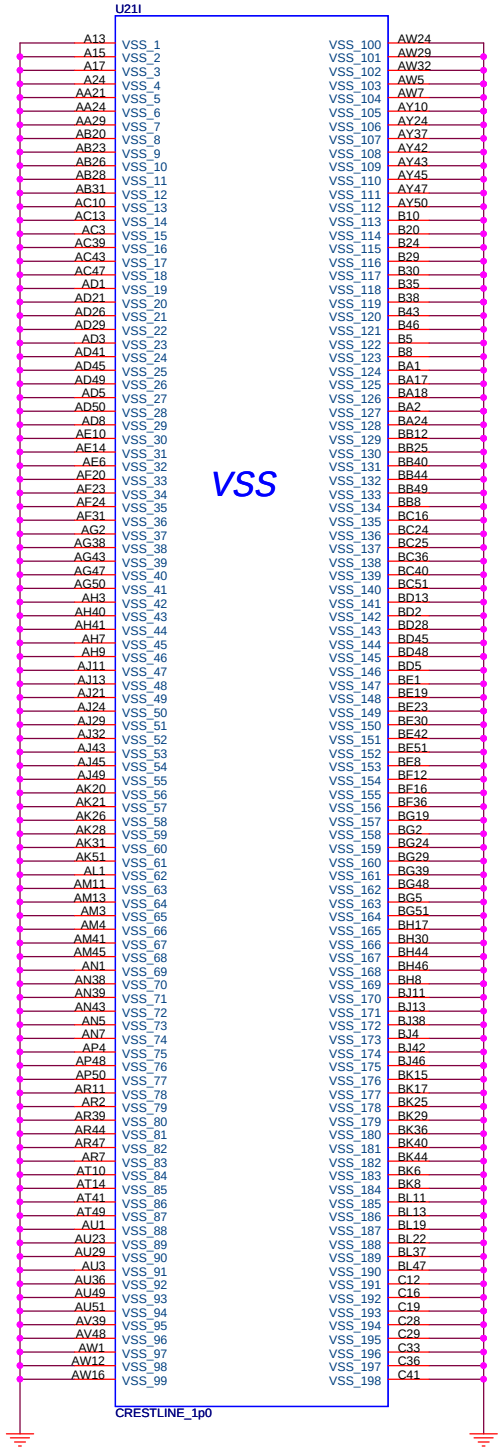
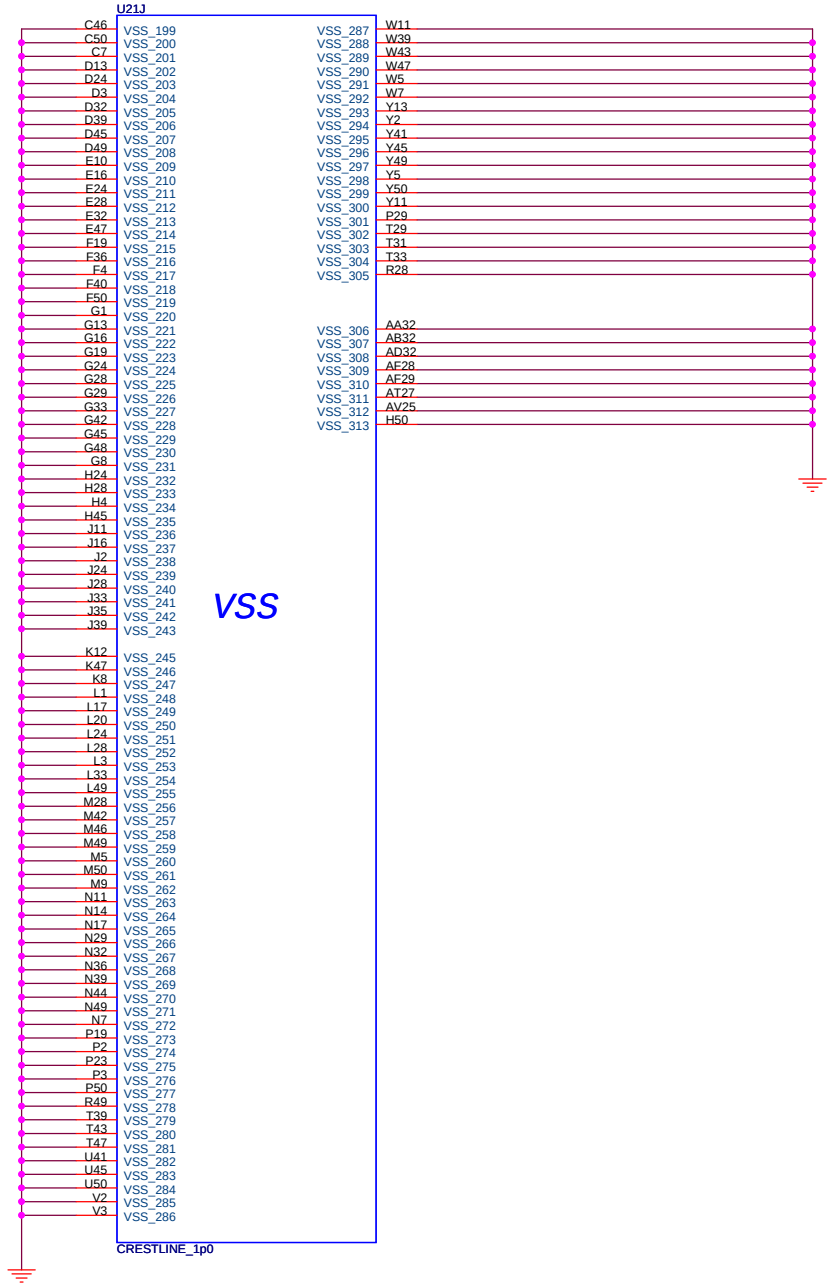
NB(Power-3)





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Strap table

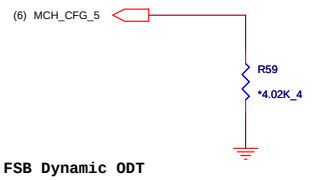
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

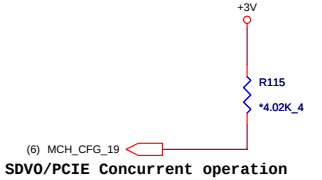
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

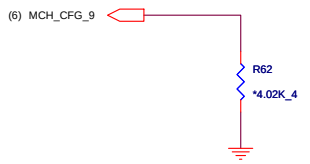


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

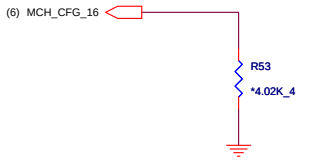


SDVO Present

Strap define at External DVI control page

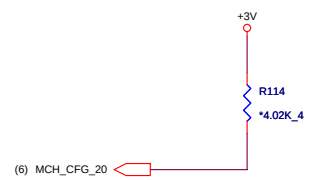
FSB Dynamic ODT

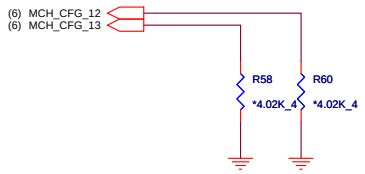
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A

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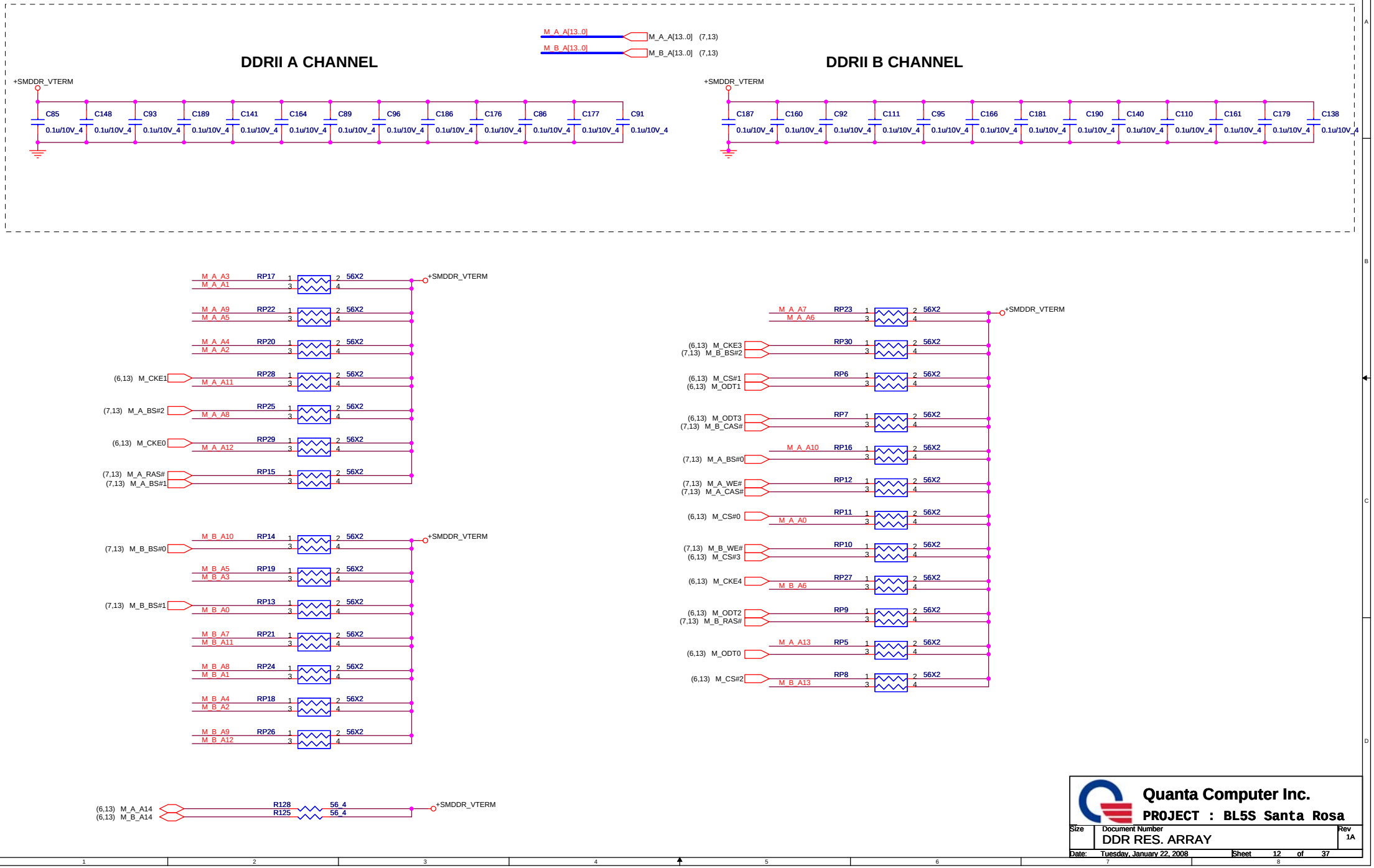
DDR2 Dual channel A/B PU



Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	DDR RES. ARRAY	1A

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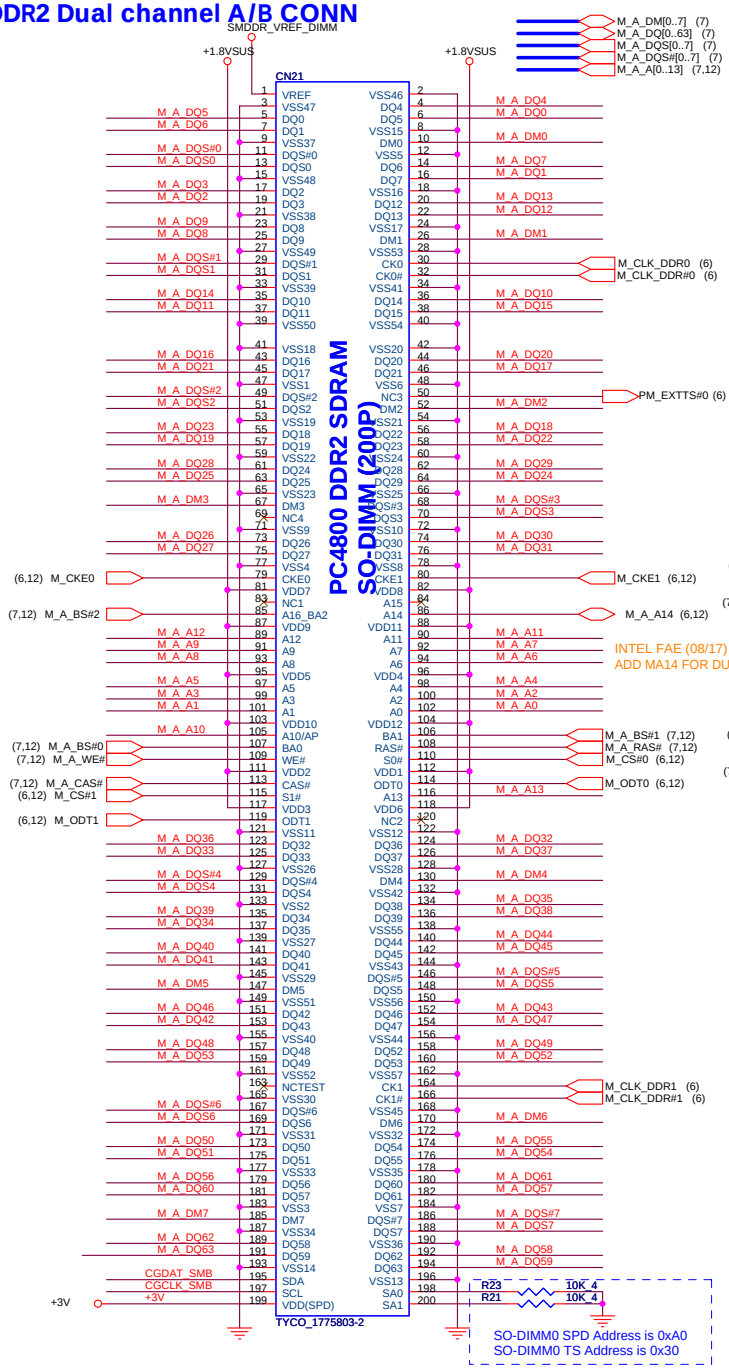
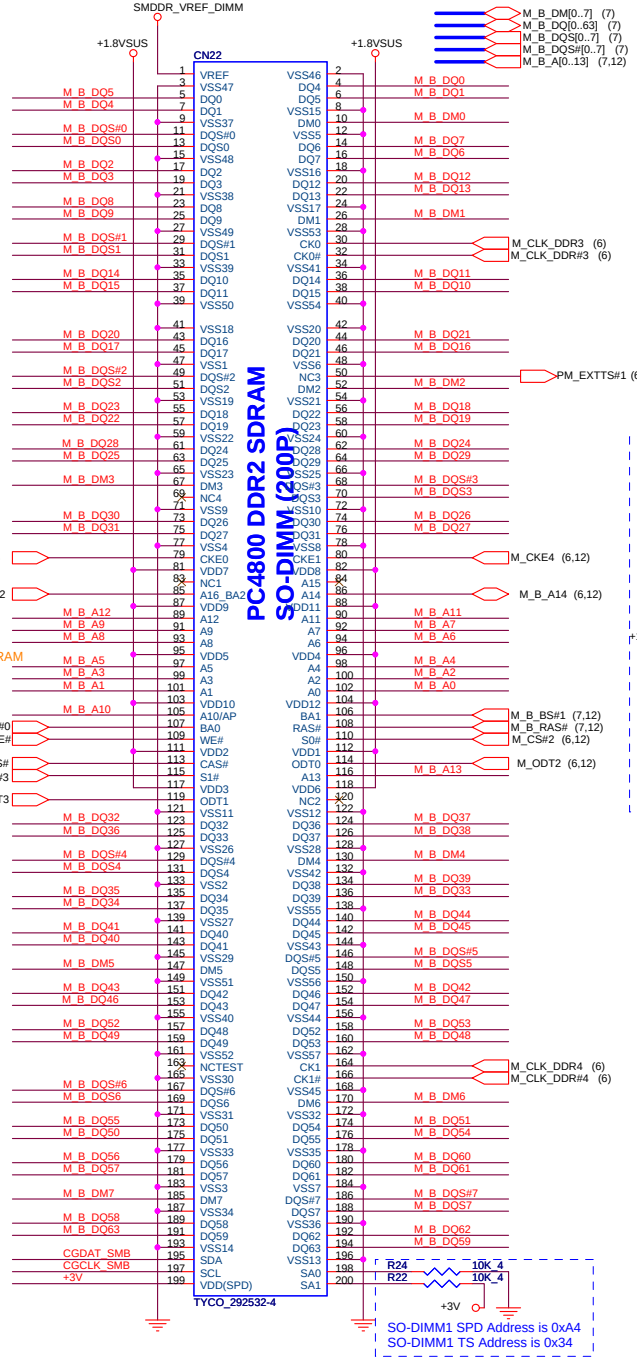
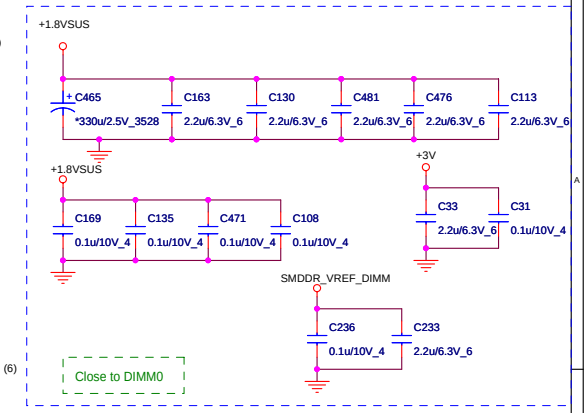
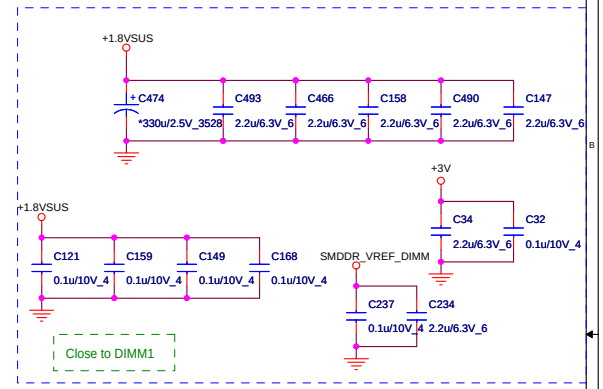
DDR2 Dual channel A/B CONN



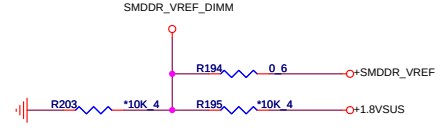
INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM







CGCLK_SMB — CGCLK_SMB (2)
CGDAT_SMB — CGDAT_SMB (2)



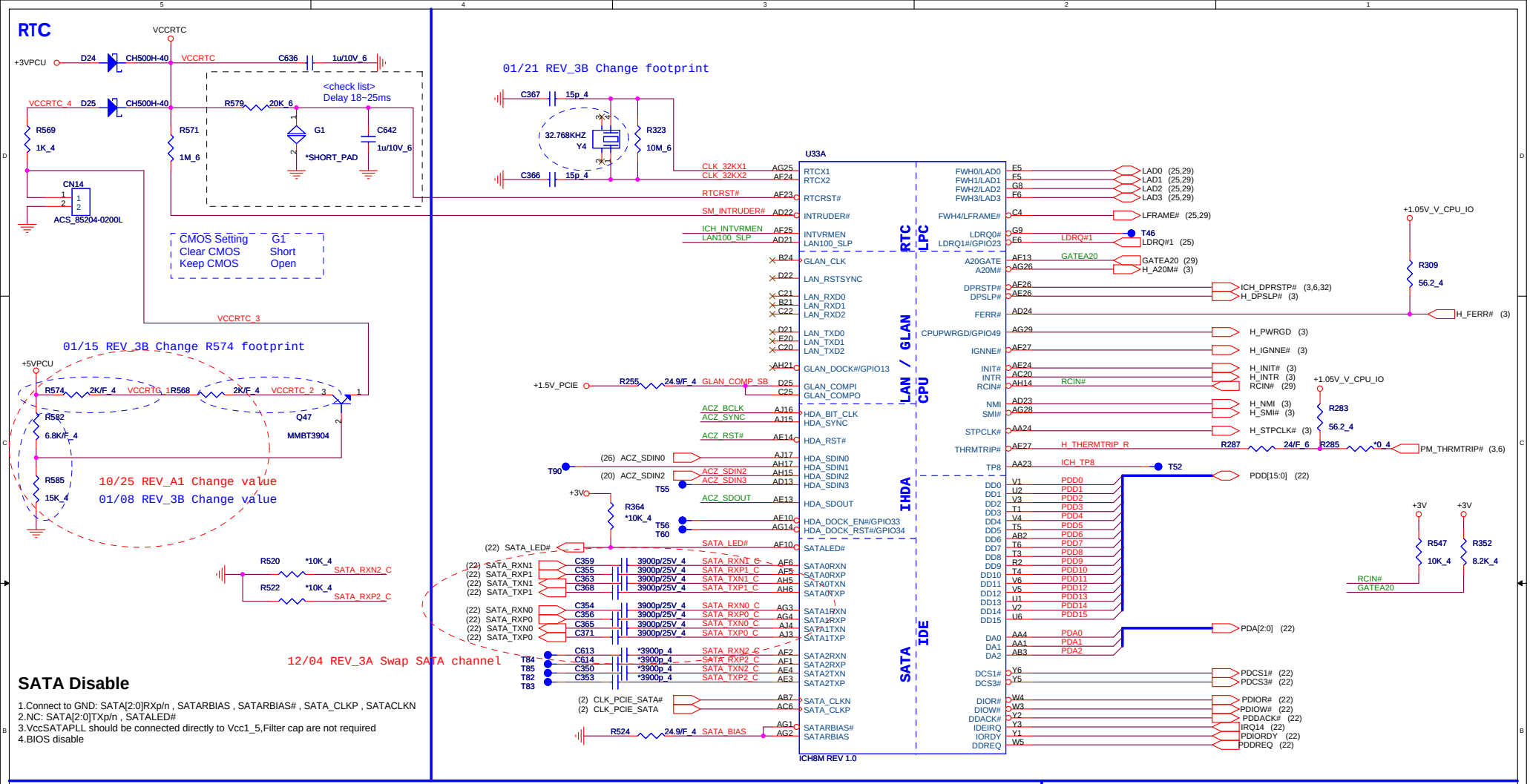
Standard Type H: 6.5mm

CLOCK 0,1
CKE 0,1

Standard Type H: 11mm

CLOCK 3,4
CKE 2,3

Quanta Computer Inc.	
PROJECT : BL5S Santa Rosa	
Size	Document Number: DDR SO-DIMM(200P) — Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 13 of 37



SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

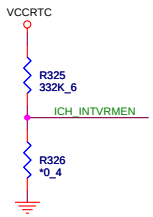
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

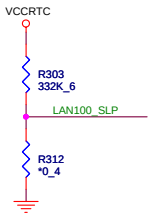
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

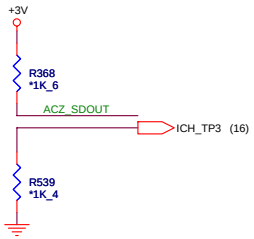
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

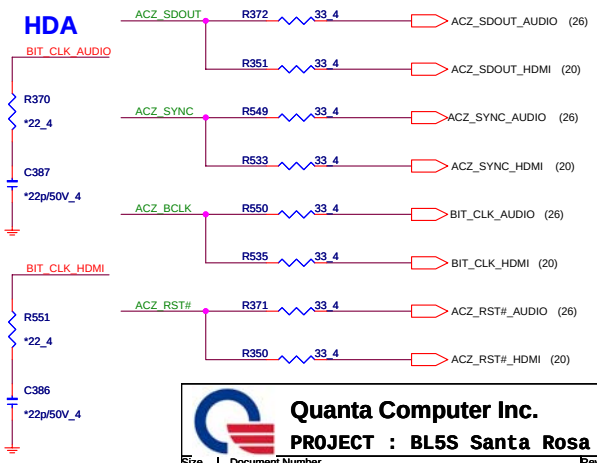
XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1









Quanta Computer Inc.
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Size	Document Number	Rev
	ICH8M HOST(1 of 4)	1A

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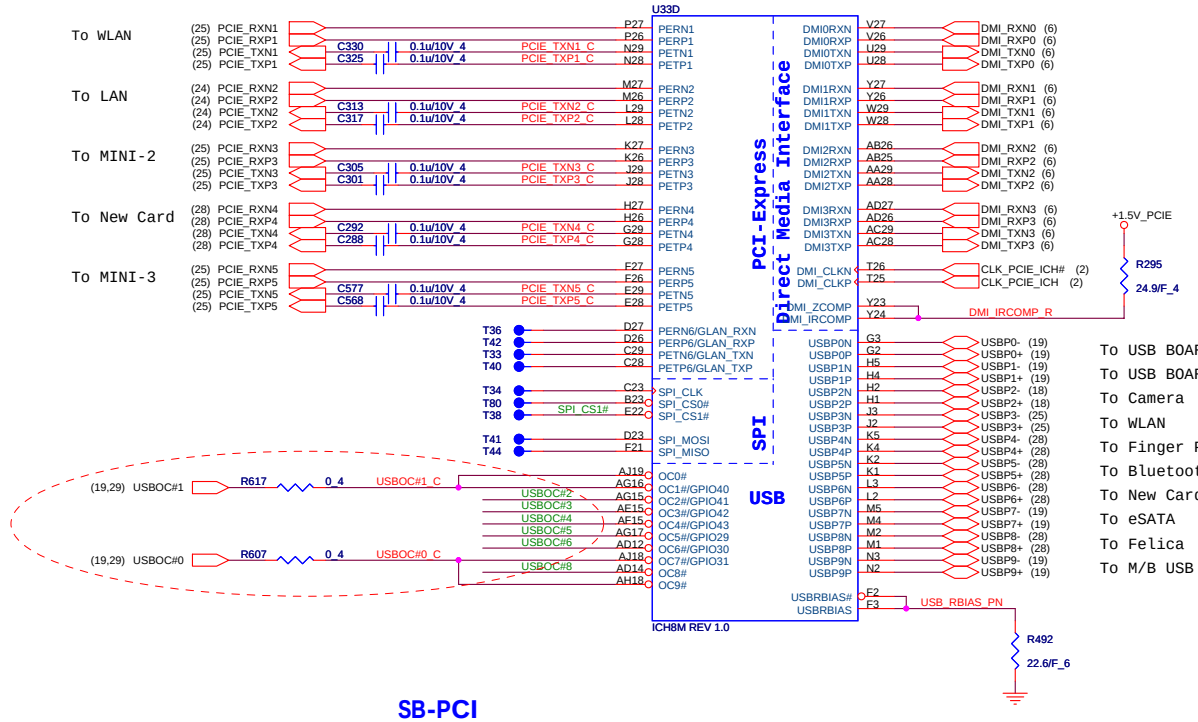
SB-PCIE/USB/DMI



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R251 *1K_4

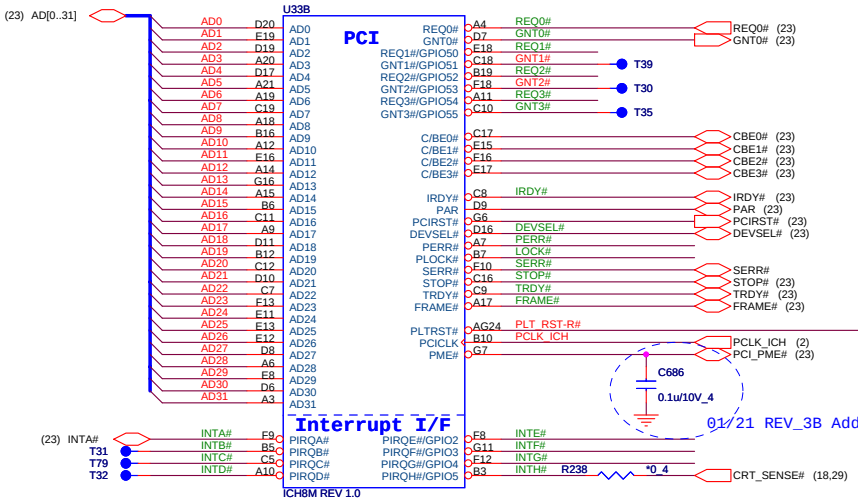
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R258 *1K_4

GNT0# R253 *1K_4

SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129

Quanta Computer Inc.
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Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	1A
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SB-GPIO

U33C

ICH8M REV 1.0

09/29 REV_A1 Del D44

10/22 REV_A1 Add FM_DET net

No Reboot strap

SPKR	Low = Default High = No Reboot

01/09 REV_3B Add

R365 Always mount

High : Main Strem
Low : Low Cost

10/22 REV_A1 Add FM_DET function

10/25 REV_A1 Change power

R298 Always mount

High : W/O FM
Low : W/ FM

BL5 W/O LED panel ,BOARD_ID1 always keep low

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS						H L
LED Panel CCFL Panel					H L	
W/ G-SENSOR W/O G-SENSOR				H L		
W/ S-VIDEO W/O S-VIDEO			H L			
W/ HDMI W/O HDMI		H L				
W/ FM W/O FM	L H					

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Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	1A

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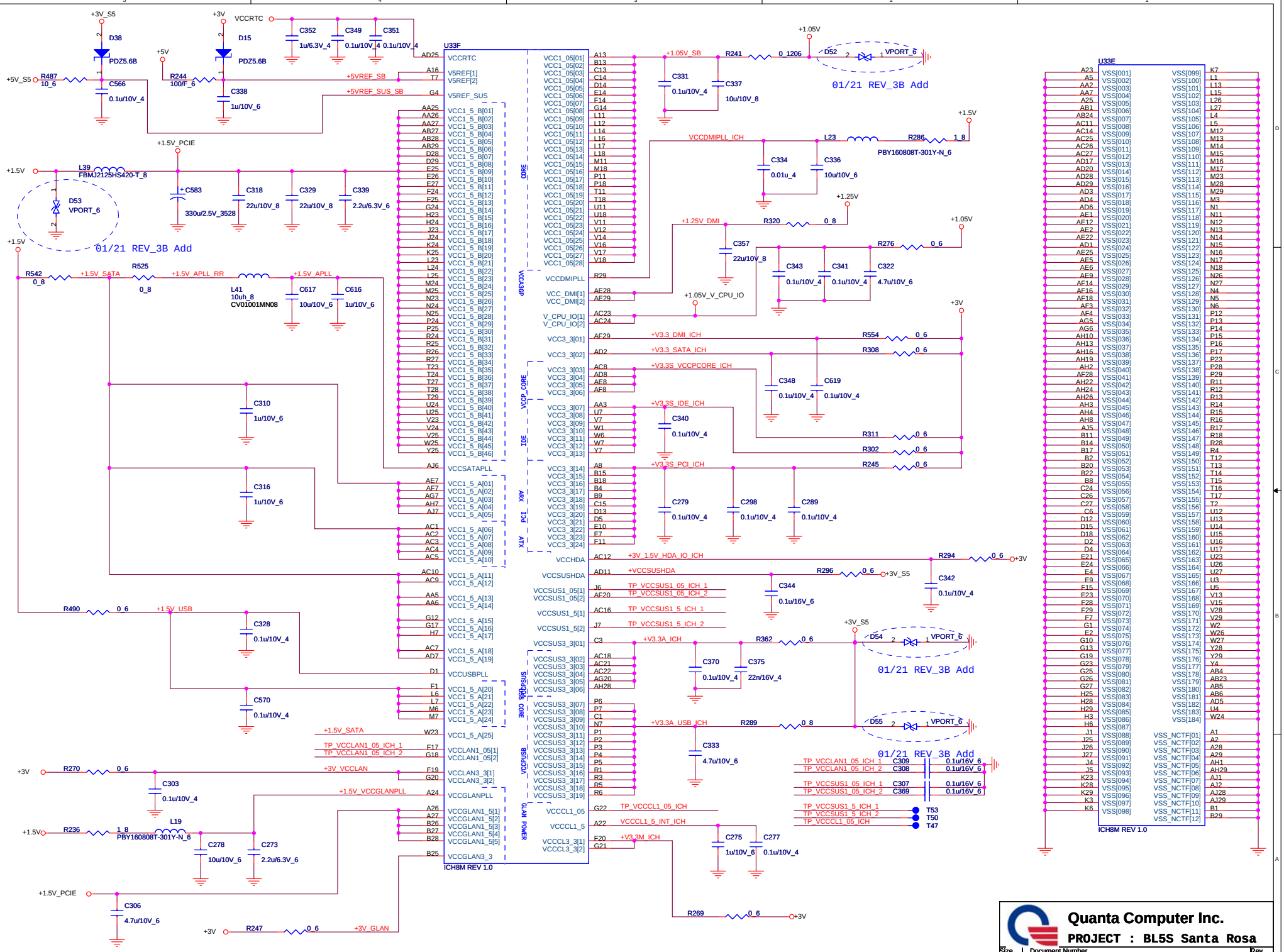
U33F
ICH8M REV 1.0
U33E
ICH8M REV 1.0
01/21 REV_3B Add
01/21 REV_3B Add
01/21 REV_3B Add
01/21 REV_3B Add
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
ICH8M Power(4 of 4)
Rev
1A
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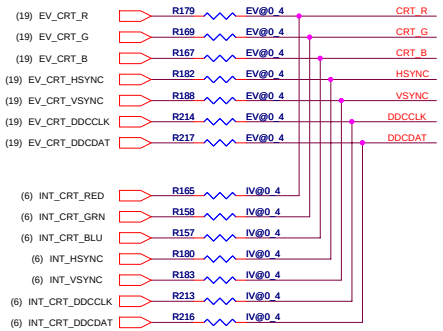
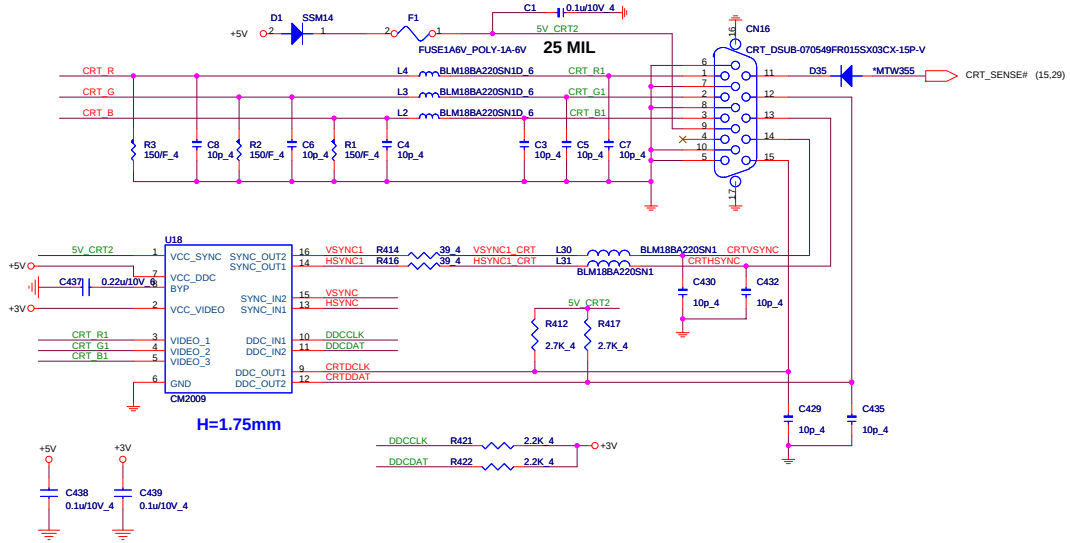
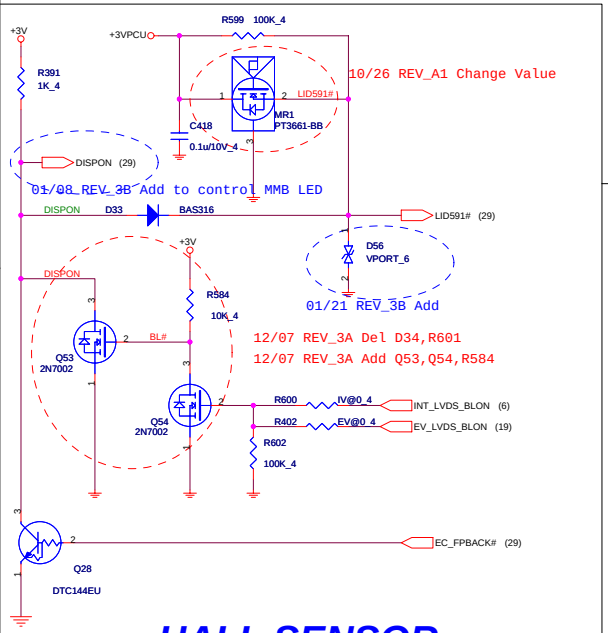
CRT PORT

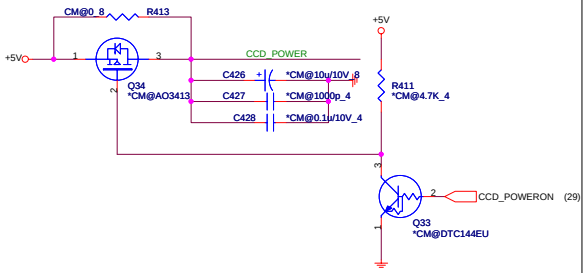


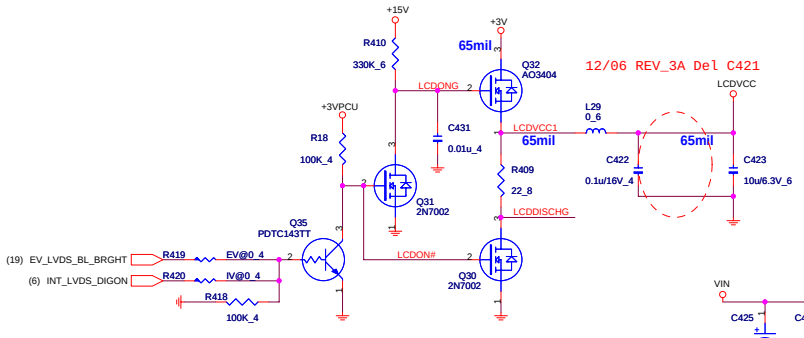




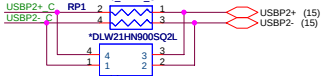
HALL SENSOR

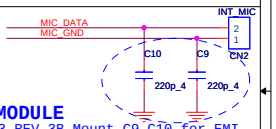
CAMERA MODULE





12/06 REV_3A Del C421

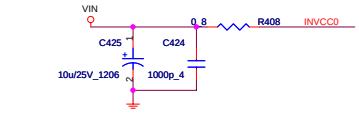


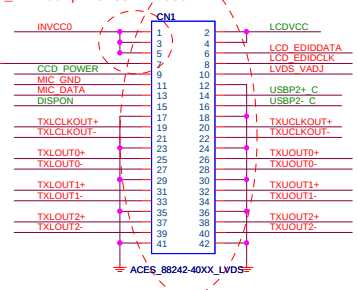


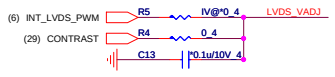
LCD PANEL MODULE

01/03 REV_3B Mount C9,C10 for EMI

10/22 REV_A1 Add pin3 to INVCC0

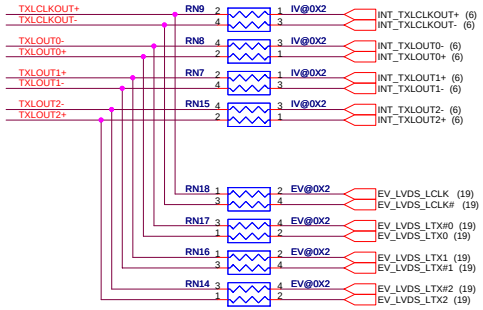


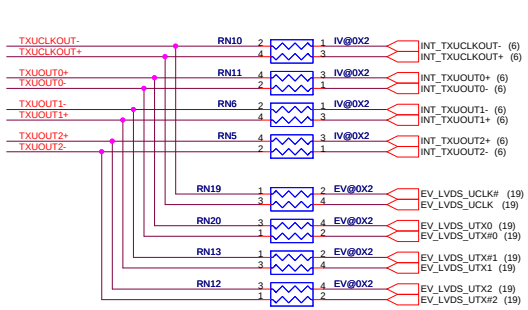


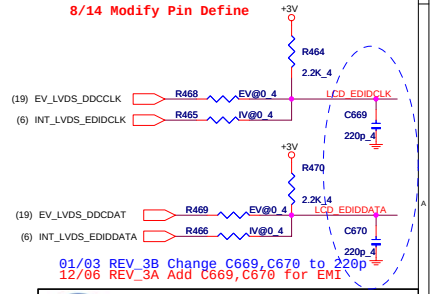


10/22 REV_A1 Change P/N

8/14 Modify Pin Define







01/03 REV_3B Change C669,C670 to 220p

12/06 REV_3A Add C669,C670 for EMI

Quanta Computer Inc.

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	LCD/CRT/LID/CAMERA	1A

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VGA

CN25

(6) PEG_TXN15 / (6) PEG_TXP15 — PEG_TXN15 / PEG_TXP15 — PEG_RXN15 / PEG_RXP15 — (6) PEG_RXN15 / (6) PEG_RXP15
(6) PEG_TXN14 / (6) PEG_TXP14 — PEG_TXN14 / PEG_TXP14 — PEG_RXN14 / PEG_RXP14 — (6) PEG_RXN14 / (6) PEG_RXP14
(6) PEG_TXN13 / (6) PEG_TXP13 — PEG_TXN13 / PEG_TXP13 — PEG_RXN13 / PEG_RXP13 — (6) PEG_RXN13 / (6) PEG_RXP13
(6) PEG_TXN12 / (6) PEG_TXP12 — PEG_TXN12 / PEG_TXP12 — PEG_RXN12 / PEG_RXP12 — (6) PEG_RXN12 / (6) PEG_RXP12
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(18) EV_CRT_DDCCLK / (18) EV_CRT_DDCDAT — EV_CRT_DDCCLK / EV_CRT_DDCDAT — CLK_MXM# (2) / CLK_MXM (2)
(21) EV_HDMI_DDCCLK / (21) EV_HDMI_DDCDATA — EV_HDMI_DDCCLK / EV_HDMI_DDCDAT — GFXRST# (15) / SYSFANON# (3)
(18) EV_LVDS_DDCCLK / (18) EV_LVDS_DDCDAT — EV_LVDS_DDCCLK / EV_LVDS_DDCDAT — GFXPG (29) / 3ND_MBDATA (21,28,29) / 3ND_MBCLK (21,28,29) / EV_LVDS_BLON (18) / EV_LVDS_BL_BRGHT (18) / DVI_HPD (21)
(18) EV_CRT_R — EV_CRT_R — EV_CRT_HSYNC (18) / EV_CRT_VSYNC (18)
(18) EV_CRT_G — EV_CRT_G
(18) EV_CRT_B — EV_CRT_B
(18) EV_LVDS_LTX#2 / (18) EV_LVDS_LTX2 — EV_LVDS_LTX#2 / EV_LVDS_LTX2 — EV_LVDS_UTX#2 (18) / EV_LVDS_UTX2 (18)
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(18) EV_LVDS_LCLK# / (18) EV_LVDS_LCLK — EV_LVDS_LCLK# / EV_LVDS_LCLK — EV_LVDS_UCLK# (18) / EV_LVDS_UCLK (18)
(22) EV_TV_C/R — EV_TV_C/R
(22) EV_TV_Y/G — EV_TV_Y/G
T94 — EV_TV_COMP
(21) EV_HDMICLK- / (21) EV_HDMICLK+ — EV_HDMICLK- / EV_HDMICLK+
(21) EV_HDMITX2N / (21) EV_HDMITX2P — EV_HDMITX2N / EV_HDMITX2P
(21) EV_HDMITX1N / (21) EV_HDMITX1P — EV_HDMITX1N / EV_HDMITX1P
(21) EV_HDMITX0N / (21) EV_HDMITX0P — EV_HDMITX0N / EV_HDMITX0P

10/24 REV_A1 Modify

VIN_VGA — VIN — R478 *0_8 — VIN_VGA / VIN

*Tyco

10/16 REV_A1 Modify

MAINON (29,33,34,35)

VIN
C536 0.1u/50V_6
+5V
C532 0.1u/10V_4
C535 10u/10V_6
+3V
C533 0.1u/10V_4
C534 10u/10V_6

USB

+5VPCU — F3 POLY SWITCH 1.5A/6V_1206 — USBPOWER
C419 4.7u/10V_6

U16 RT9711BPF
IN1, IN2 — OUT3, OUT2, OUT1 — USBPWR0
(29) USB_EN# — EN#
GND, GND-C — OC#
R394 *100K_6 +5VPCU
USBOC#0 (15,29)

09/20 REV_A1 Modify

(15) USBP9+ / (15) USBP9- — USBP9+ / USBP9-
(15) USBP7+ / (15) USBP7- — USBP7+ / USBP7-

01/17 REV_3B Del R513,R494,R523,R521,L38,L40

USBPWR0 — C565 100u/6.3V_3528 — USBP7- / USBP7+ — CN28 USB
09/23 REV_A1 Change footprint

USBPWR0 — C606 100u/6.3V_3528 — USBP9- / USBP9+ — CN32 USB
09/23 REV_A1 Change footprint

USB board connector

10/24 REV_A1 Add for EMI

+5VPCU — C663 0.1u/10V_4 — USB_EN#1 — C664 0.1u/10V_4

09/20 REV_A1 Modify

CN11
(15,29) USBOC#1 — +5VPCU
(15) USBP1+ / (15) USBP1- / (15) USBP0+ / (15) USBP0- — USBP1+ / USBP1- / USBP0+ / USBP0-
(29) USB_EN#1 — +5VPCU
BT@88266-100XX-XXX-10P-R

09/29 REV_A1 Modify

USB

01/09 REV_3B Add

Close CN12

USBP9- D42 — EGA_4 — D19 — EGA_4 — USBP0-
USBP9+ D43 — EGA_4 — D18 — EGA_4 — USBP0+
USBP7- D39 — EGA_4 — D17 — EGA_4 — USBP1-
USBP7+ D40 — EGA_4 — D16 — EGA_4 — USBP1+
USBPWR0 D41 — VPORT_6 — D20 — VPORT_6 — +5VPCU

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	VGA CONNECTOR/USB/ESATA	1A

Date: Tuesday, January 22, 2008 Sheet 19 of 37

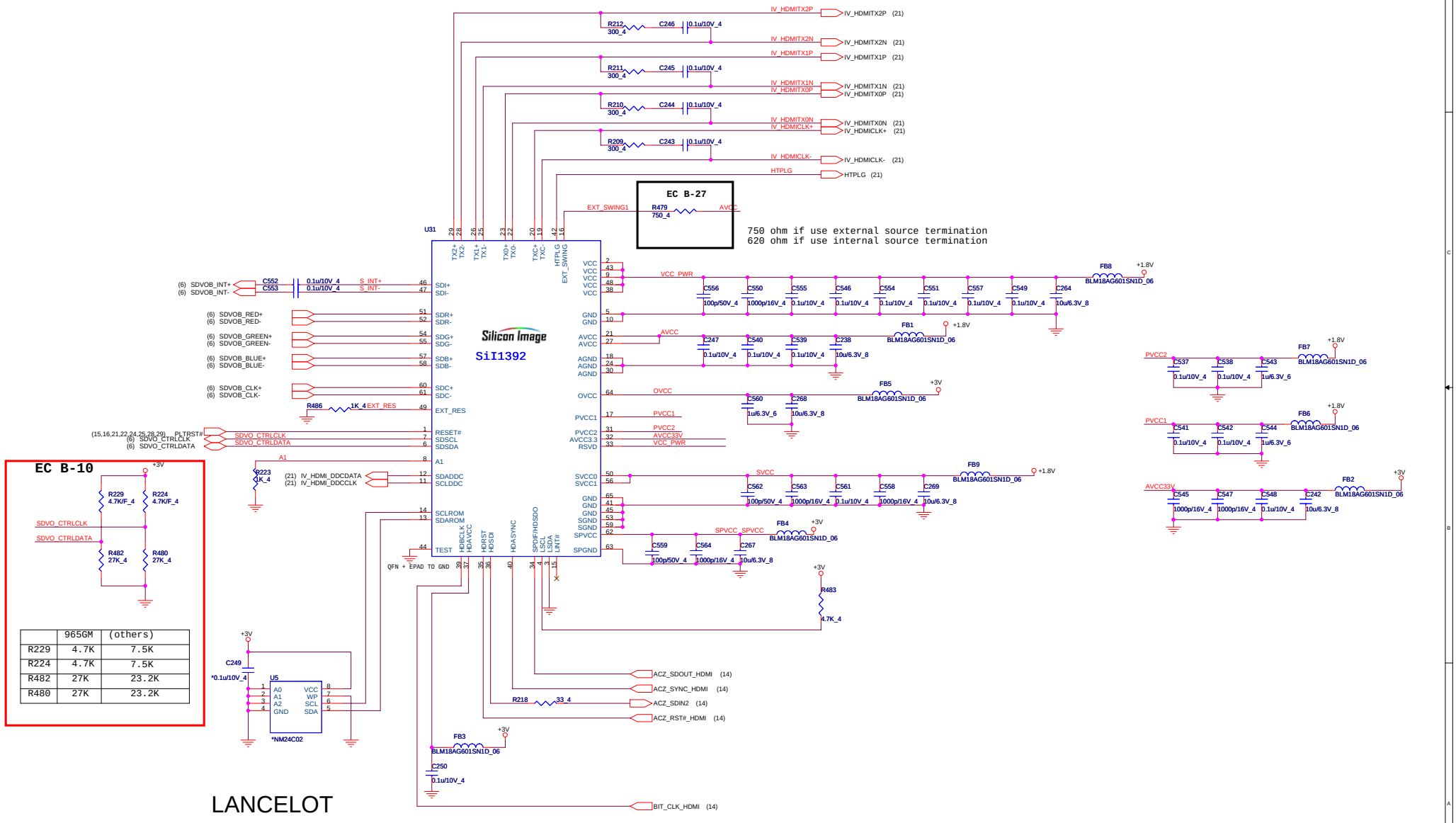
SiI1392 HDMI TX

LAYOUT RULES:

Route traces with 100 Ohm Differential Impedance

Avoid placing GND Copper or traces adjacent to TMDS Trace

Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392



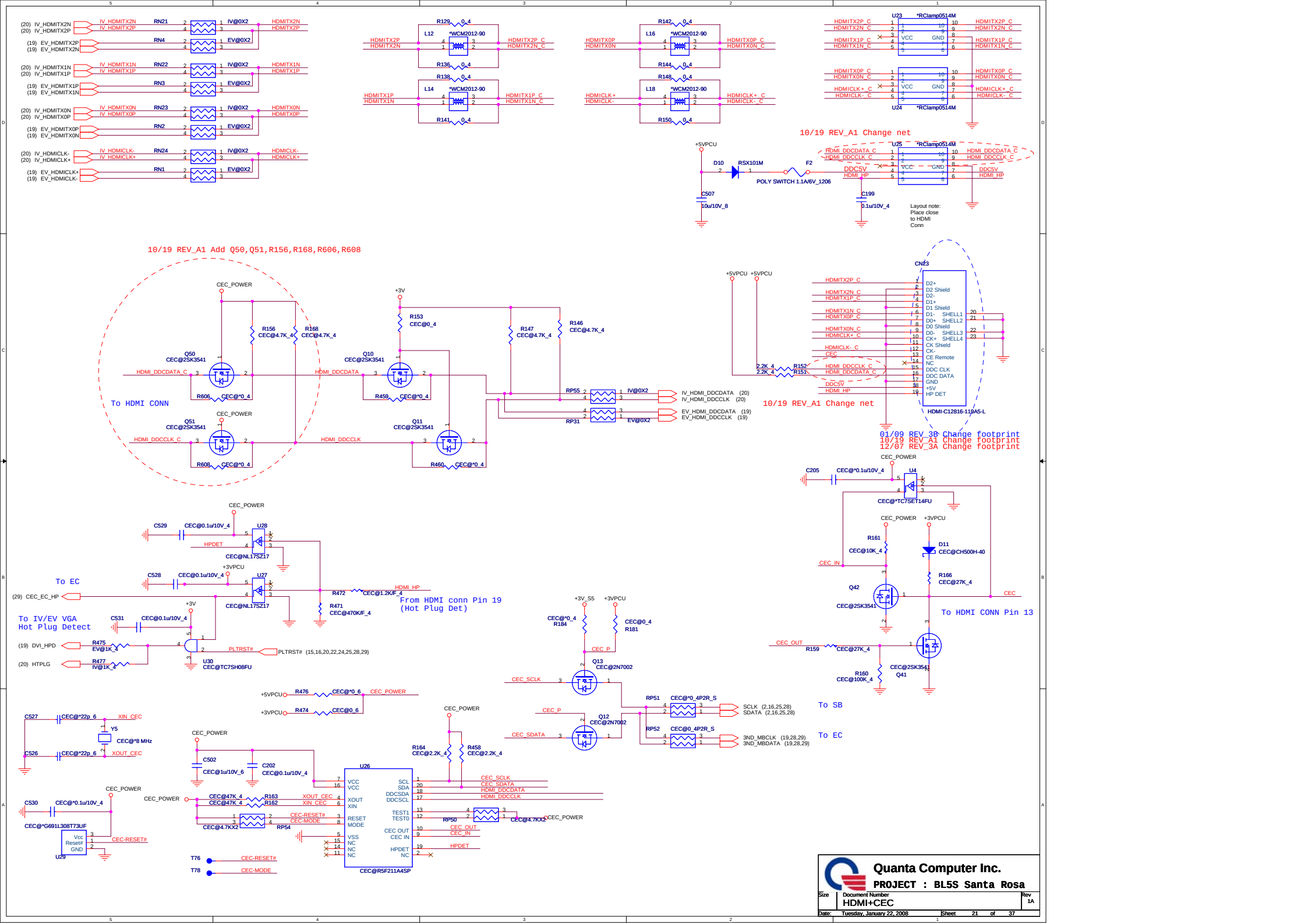
	965GM	(others)
R229	4.7K	7.5K
R224	4.7K	7.5K
R482	27K	23.2K
R480	27K	23.2K

Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Sil1392(HDMI)	1A

Date: Tuesday, January 22, 2008 Sheet 20 of 37


(20) IV_HDMITX2N
(20) IV_HDMITX2P
(19) EV_HDMITX2P
(19) EV_HDMITX2N
RN21
RN4
IV@0X2
EV@0X2
HDMITX2N
HDMITX2P
(20) IV_HDMITX1N
(20) IV_HDMITX1P
(19) EV_HDMITX1P
(19) EV_HDMITX1N
RN22
RN3
HDMITX1N
HDMITX1P
(20) IV_HDMITX0N
(20) IV_HDMITX0P
(19) EV_HDMITX0P
(19) EV_HDMITX0N
RN23
RN2
HDMITX0N
HDMITX0P
(20) IV_HDMICLK-
(20) IV_HDMICLK+
(19) EV_HDMICLK+
(19) EV_HDMICLK-
RN24
RN1
HDMICLK-
HDMICLK+
R129 0_4
L12 *WCM2012-90
R136 0_4
R138 0_4
L14 *WCM2012-90
R141 0_4
HDMITX2P_C
HDMITX2N_C
HDMITX1P_C
HDMITX1N_C
R142 0_4
L16 *WCM2012-90
R144 0_4
R148 0_4
L18 *WCM2012-90
R150 0_4
HDMITX0P_C
HDMITX0N_C
HDMICLK+_C
HDMICLK-_C
U23 *RClamp0514M
U24 *RClamp0514M
VCC
GND
10/19 REV_A1 Change net
+5VPCU
D10
RSX101M
F2
POLY SWITCH 1.1A/6V_1206
C507
10u/10V_8
C199
0.1u/10V_4
DDC5V
HDMI_HP
HDMI_DDCDATA_C
HDMI_DDCCLK_C
U25 *RClamp0514M
Layout note:
Place close
to HDMI
Conn
10/19 REV_A1 Add Q50,Q51,R156,R168,R606,R608
CEC_POWER
+3V
R153 CEC@0_4
R156 CEC@4.7K_4
R168 CEC@4.7K_4
R147 CEC@4.7K_4
R146 CEC@4.7K_4
Q50 CEC@2SK3541
Q10 CEC@2SK3541
Q51 CEC@2SK3541
Q11 CEC@2SK3541
HDMI_DDCDATA_C
HDMI_DDCDATA
HDMI_DDCCLK_C
HDMI_DDCCLK
R606 CEC@*0_4
R459 CEC@*0_4
R608 CEC@*0_4
R460 CEC@*0_4
To HDMI CONN
RP55 IV@0X2
RP31 EV@0X2
IV_HDMI_DDCDATA (20)
IV_HDMI_DDCCLK (20)
EV_HDMI_DDCDATA (19)
EV_HDMI_DDCCLK (19)
+5VPCU +5VPCU
2.2K_4
R152
R151
CN23
HDMI-C12816-119A5-L
D2+
D2 Shield
D2-
D1+
D1 Shield
D1- SHELL1
D0+ SHELL2
D0 Shield
D0- SHELL3
CK+ SHELL4
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
01/09 REV_3B Change footprint
10/19 REV_A1 Change footprint
12/07 REV_3A Change footprint
C205 CEC@*0.1u/10V_4
U4 CEC@*TC7SET14FU
+3VPCU
R161 CEC@10K_4
D11 CEC@CH500H-40
R166 CEC@27K_4
Q42 CEC@2SK3541
Q41 CEC@2SK3541
R159 CEC@27K_4
R160 CEC@100K_4
CEC_IN
CEC_OUT
CEC
To HDMI CONN Pin 13
To SB
To EC
C529 CEC@0.1u/10V_4
U28 CEC@NL17SZ17
HPDET
C528 CEC@0.1u/10V_4
U27 CEC@NL17SZ17
R472 CEC@1.2K/F_4
R471 CEC@470K/F_4
HDMI_HP
To EC
(29) CEC_EC_HP
From HDMI conn Pin 19
(Hot Plug Det)
To IV/EV VGA
Hot Plug Detect
C531 CEC@0.1u/10V_4
(19) DVI_HPD
(20) HTPLG
R475 EV@1K_4
R477 IV@1K_4
U30 CEC@TC7SH08FU
PLTRST#
PLTRST# (15,16,20,22,24,25,28,29)
+3V_S5
R184 CEC@*0_4
R181 CEC@0_4
Q13 CEC@2N7002
Q12 CEC@2N7002
CEC_P
CEC_SCLK
CEC_SDATA
RP51 CEC@*0_4P2R_S
RP52 CEC@0_4P2R_S
SCLK (2,16,25,28)
SDATA (2,16,25,28)
3ND_MBCLK (19,28,29)
3ND_MBDATA (19,28,29)
+5VPCU R476 CEC@*0_6
+3VPCU R474 CEC@0_6
C527 CEC@*22p_6
C526 CEC@*22p_6
Y5
CEC@*8 MHz
XIN_CEC
XOUT_CEC
C502 CEC@1u/10V_6
C202 CEC@0.1u/10V_4
R164 CEC@2.2K_4
R458 CEC@2.2K_4
U26 CEC@R5F211A4SP
VCC
XOUT
XIN
RESET
MODE
VSS
NC
CEC OUT
CEC IN
HPDET
SCL
SDA
DDCSDA
DDCSCL
TEST1
TEST0
C530 CEC@*0.1u/10V_4
CEC@*G691L308T73UF
U29
CEC-RESET#
R163 CEC@47K_4
R162 CEC@47K_4
XOUT_CEC
XIN_CEC
CEC-RESET#
CEC-MODE
RP54 CEC@4.7KX2
RP50 CEC@4.7KX2
T76
T78
HDMI_DDCDATA
HDMI_DDCCLK
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
HDMI+CEC
Rev
1A
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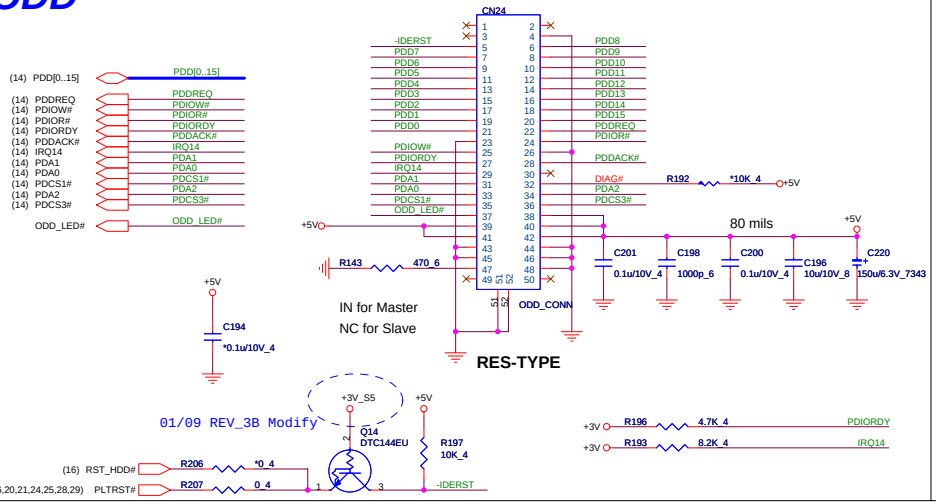
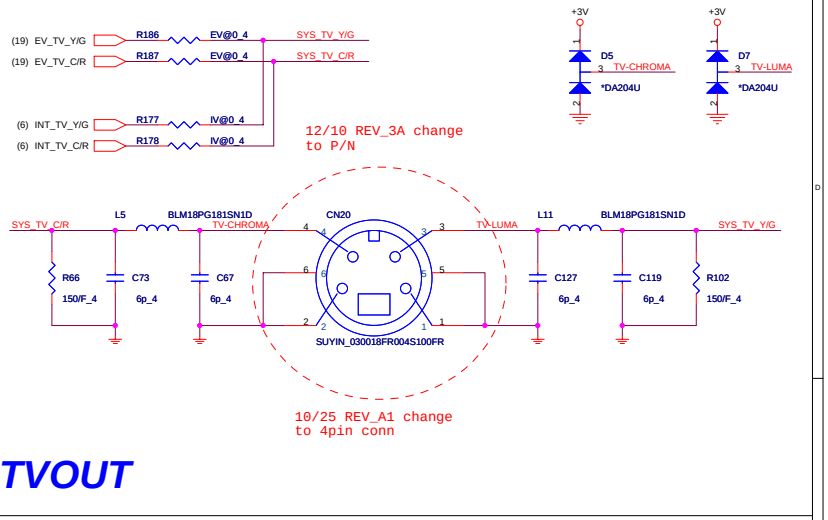
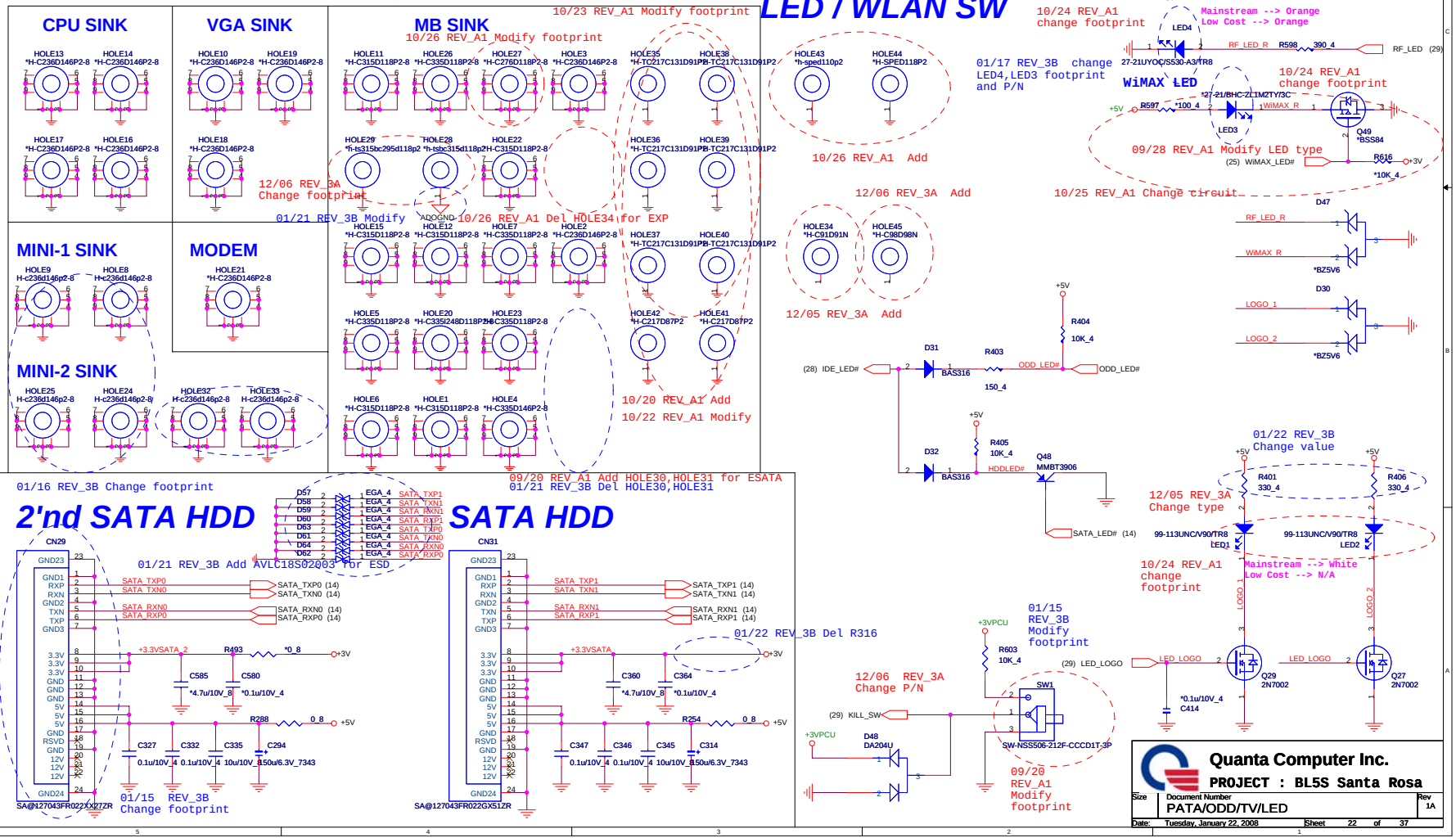
ODD



TVOUT



LED / WLAN SW



Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	PATA/ODD/TV/LED		1A
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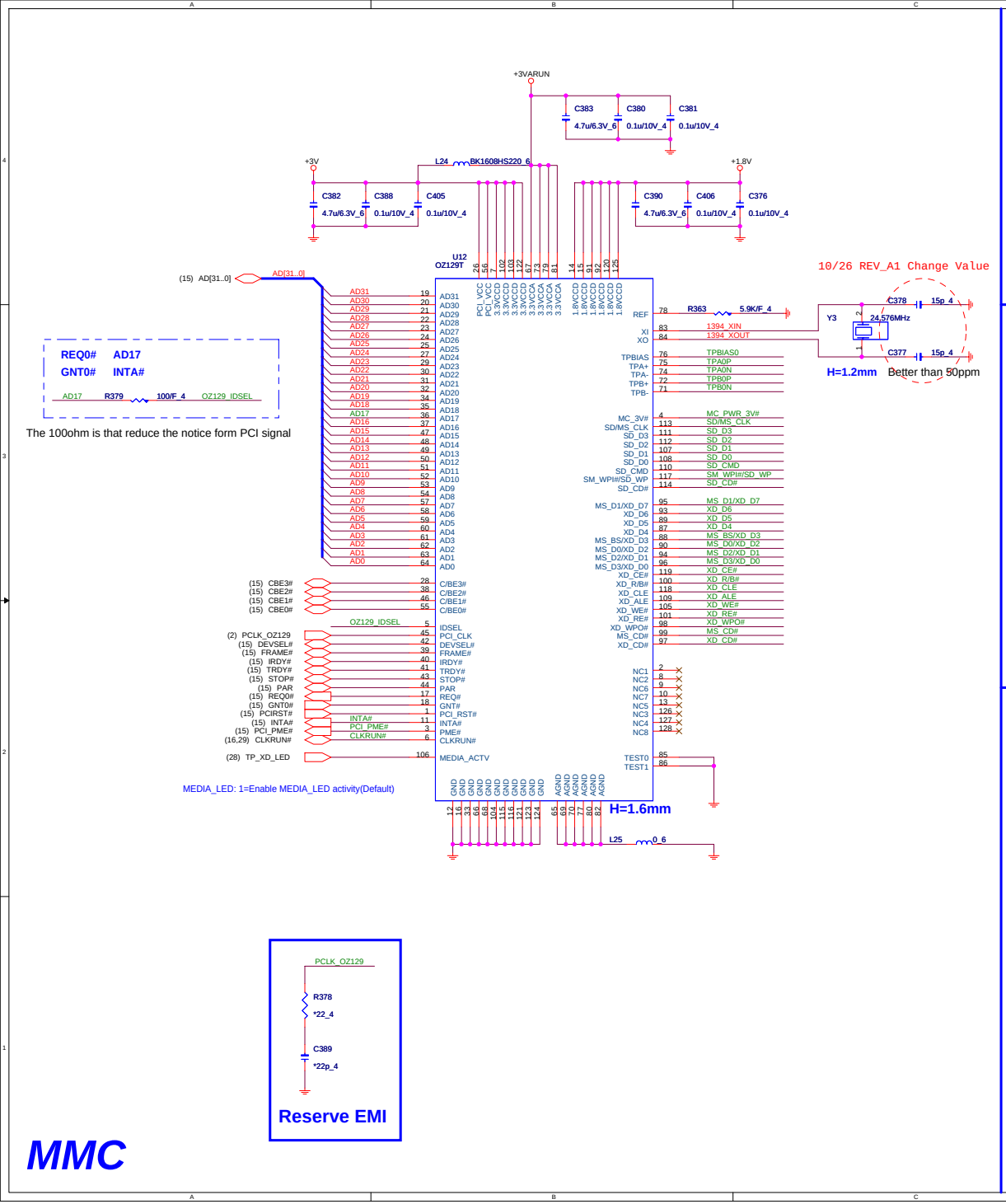
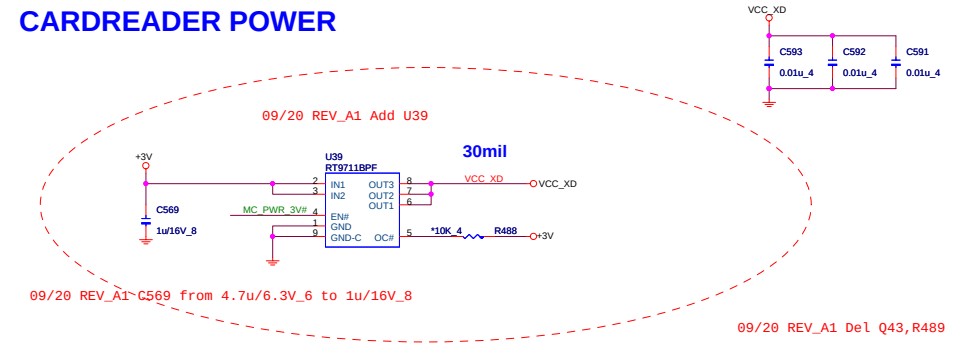
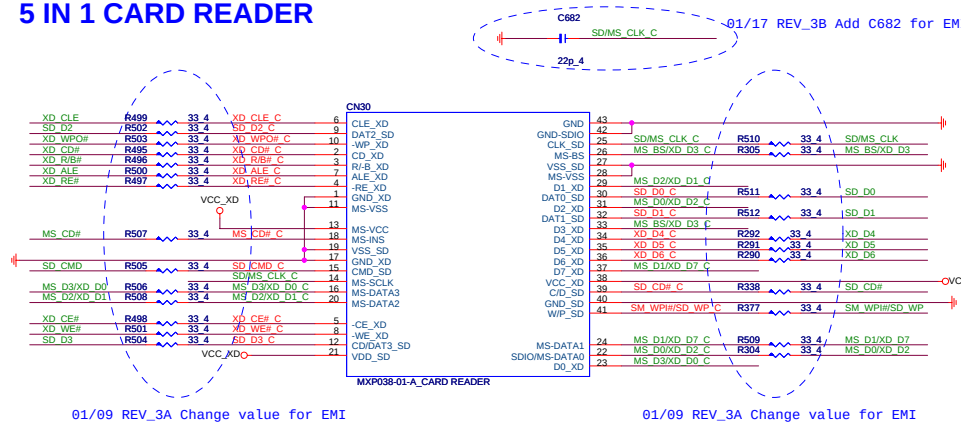


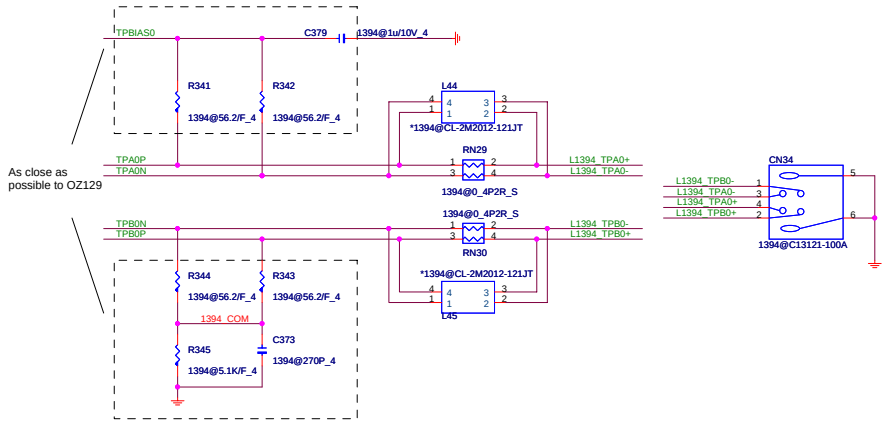
CARDREADER POWER



5 IN 1 CARD READER



1394



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PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	OZ129T (Card Reader/1394)	1A

Date: Tuesday, January 22, 2008 Sheet 23 of 37

LAN_MARVELL_88E8040/88E8055/88E8072

10/100 : 88E8040 P/N : AL008040001
GIGA : 88E8055 P/N : AJ080550000
GIGA : 88E8072 P/N : AL008072000

U32

88E805X

88E8040T

LAN_RSET
2K Ohm for 8040
4.87K Ohm for 8055/8072

12/05 REV_3A Add D6

10/24 REV_A1 Add

10/24 REV_A1 Modify

H = 0.8mm

DELTA ~~10/100 : LFE8696-R~~ ~~P/N : DB0MA8LAN00~~
H = 4mm ~~GIGA : LFE9249-R~~ ~~P/N : DB0ZR1LAN11~~

HWS ~~10/100 : HPL-4001B~~ ~~P/N : DB0SA1LAN01~~
H = 4mm GIGA : HPL-68 P/N : DB0ZB1LAN12

BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24
H = 4mm ~~GIGA : GST5009-LF~~ ~~P/N : DB0KN1LAN03~~

25 mil Trace width

25 mil Trace width

12/10 REV_3A DNI R485,R484,U7
Mount R481

EEPROM No Use
VPD_DATA Pull Down

01/16 REV_3B change footprint

TERMINATION PLANE

RJ45-CONN

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PROJECT : BL5S Santa Rosa		
Size	Document Number: LAN_Marvell_8040/8055	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 24 of 37	

Mini PCI-E Card
WLAN

MINI-Card I

09/28 REV_A1 Modify

10/26 REV_A1 Modify

09/28 REV_A1 Modify

To BT

MINI-Card II

09/20 REV_A1 Modify

MINI-Card III

01/18 REV_3B Add PAD

12/07 REV_3A Add

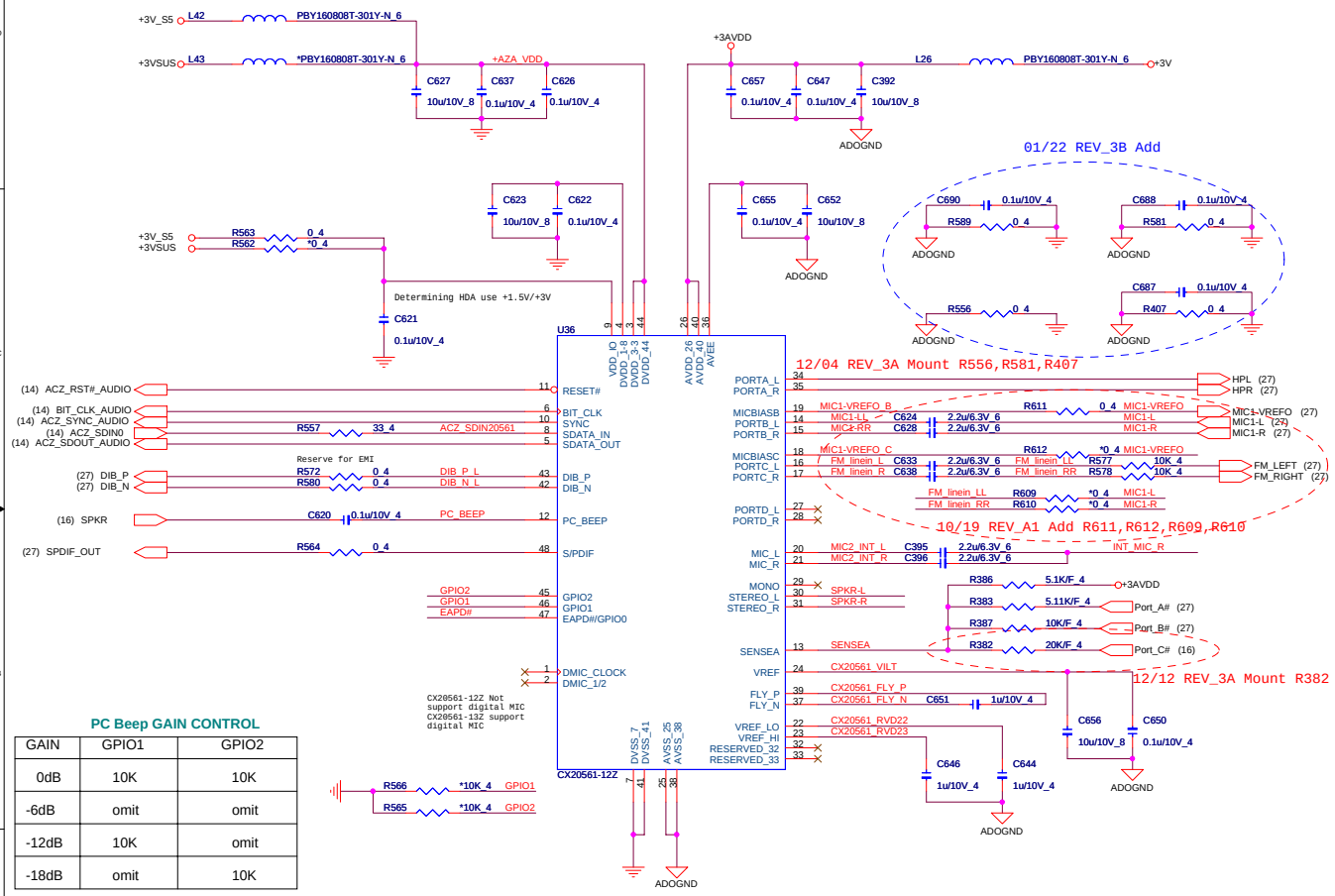
EMI

12/07 REV_3A Add

H= 8mm

Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number: MINI PCIE/HOLE		Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 25 of 37		

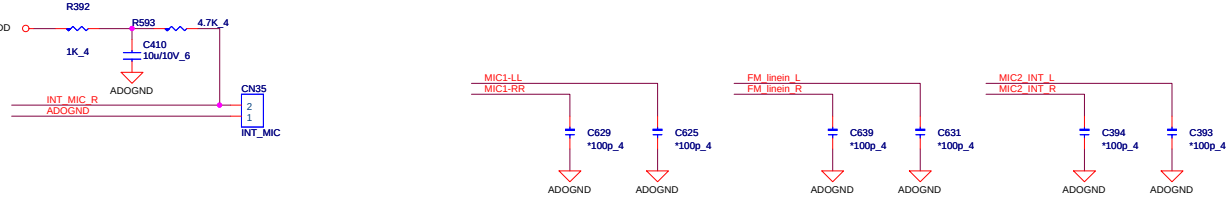
Codec(CX20561)



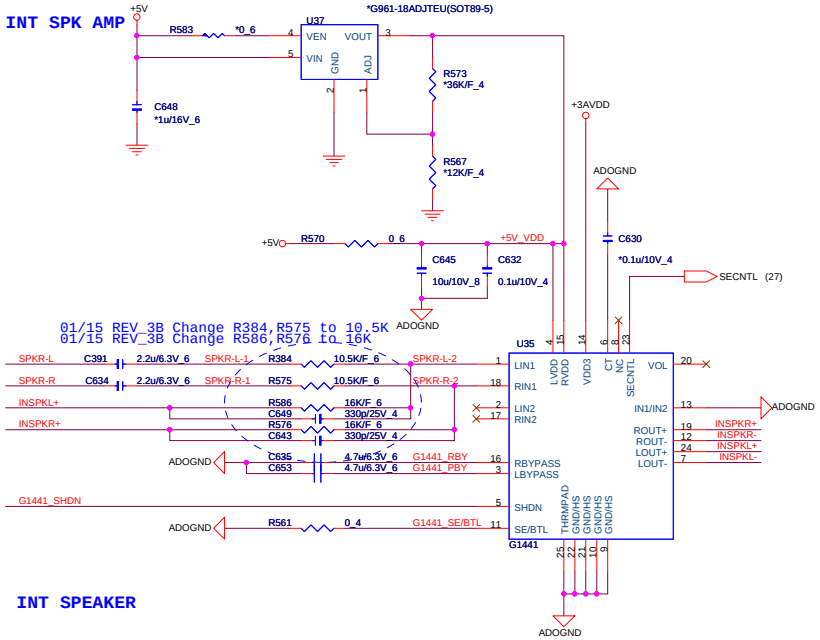
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

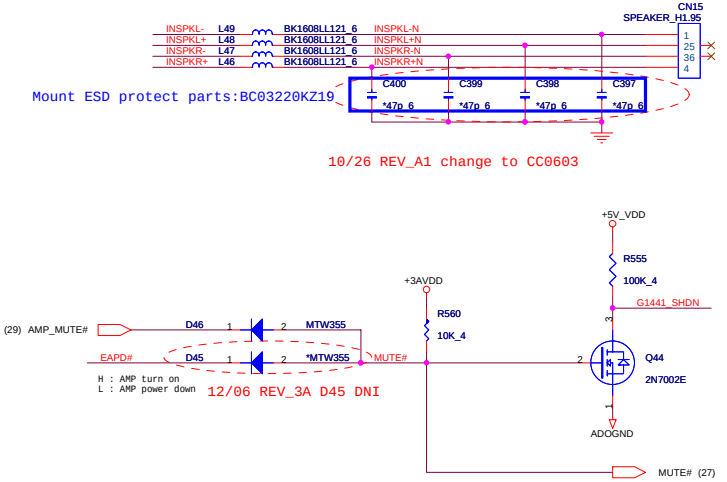
INT_MIC



INT SPK AMP



INT SPEAKER



Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: Conexant CX205601	Rev: 1A
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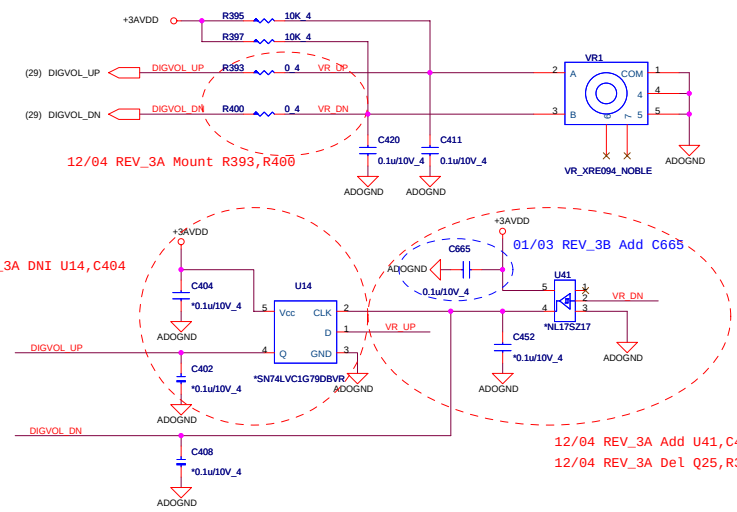
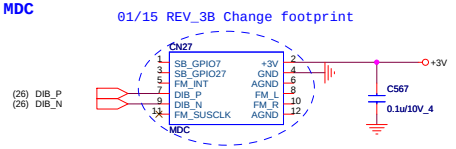
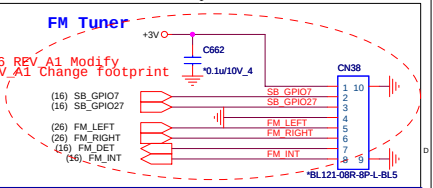
VR



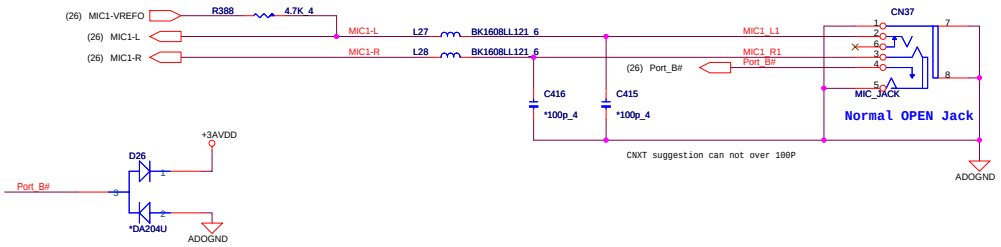
MDC



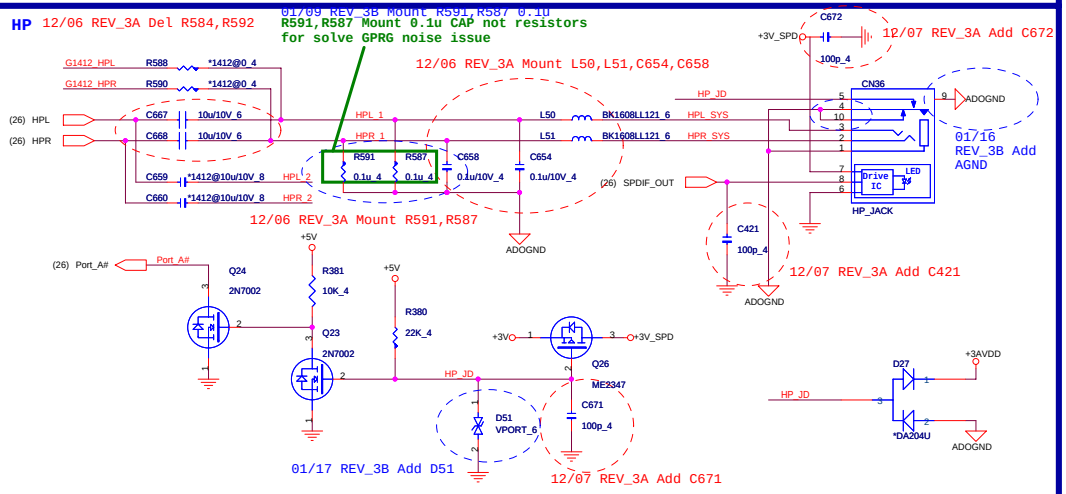
FM Tuner



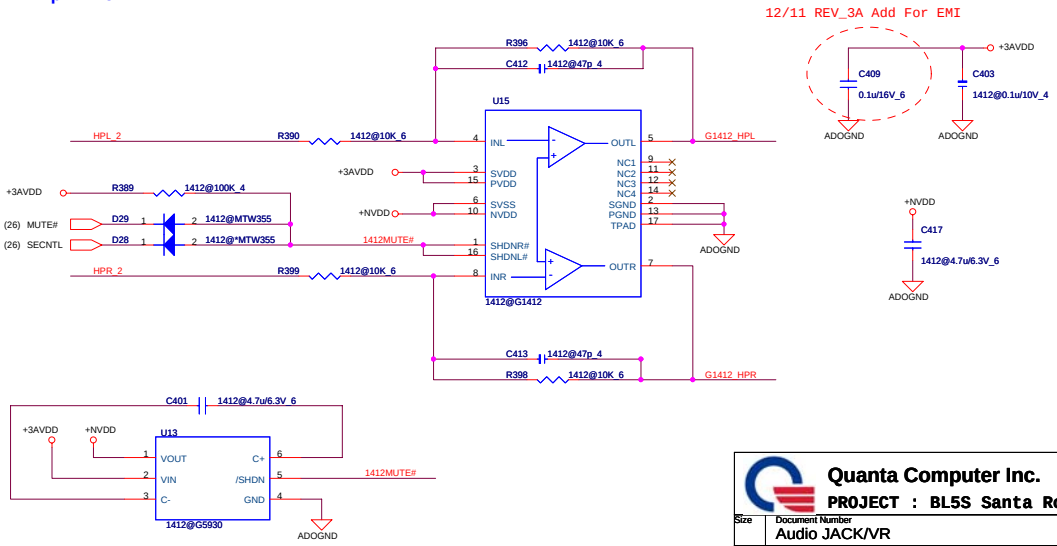
SYSTEM MIC



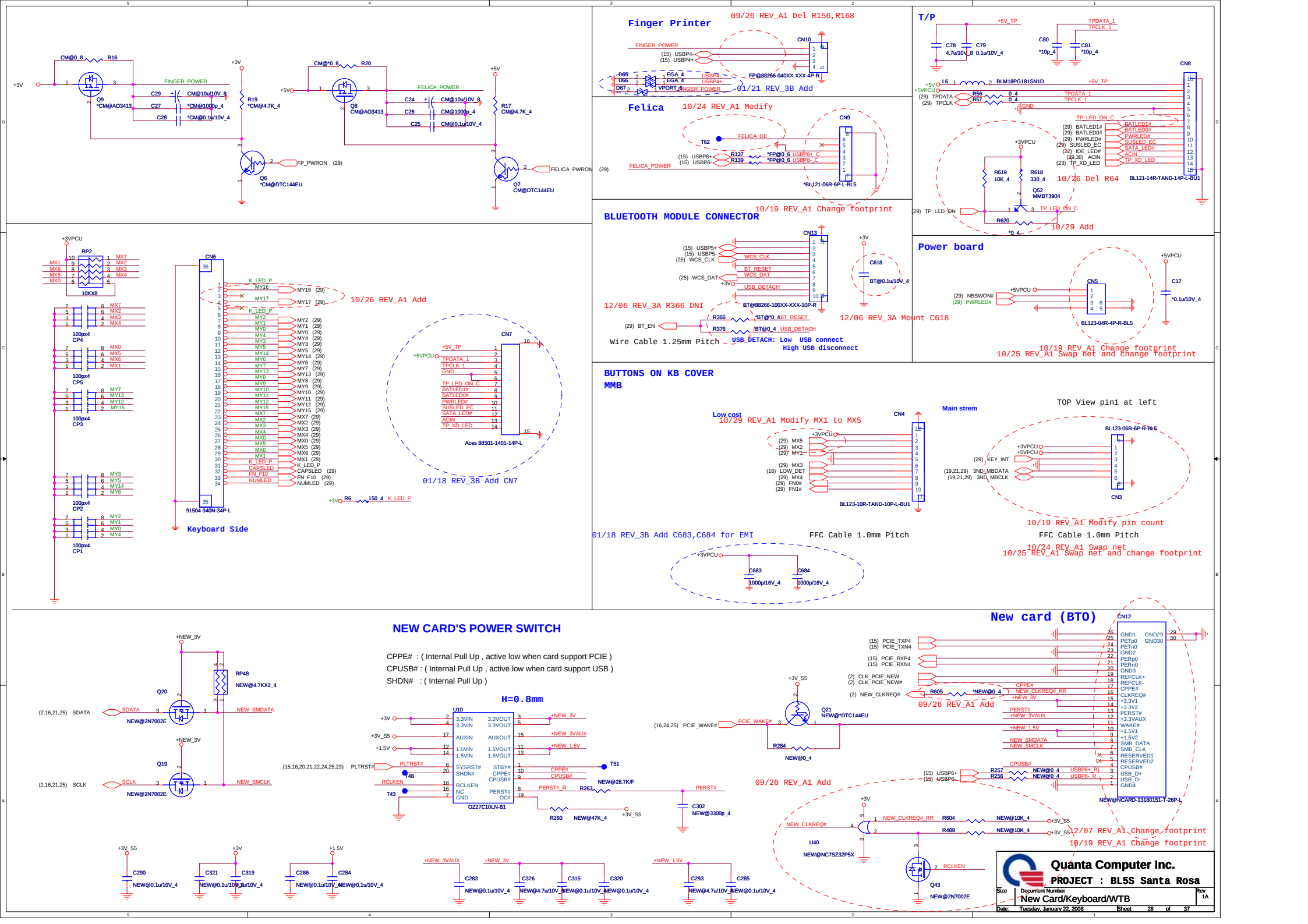
HP



HP Amplifier



Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number: Audio JACK/VR		Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 27 of 37		


Finger Printer
09/26 REV_A1 Del R156,R168
01/21 REV_3B Add
Felica
10/24 REV_A1 Modify
10/19 REV_A1 Change footprint
T/P
10/26 Del R64
10/29 Add
BLUETOOTH MODULE CONNECTOR
12/06 REV_3A R366 DNI
12/06 REV_3A Mount C618
Wire Cable 1.25mm Pitch
USB_DETACH: Low USB connect
High USB disconnect
Power board
10/19 REV_A1 Change footprint
10/25 REV_A1 Swap net and change footprint
Keyboard Side
10/26 REV_A1 Add
01/18 REV_3B Add CN7
BUTTONS ON KB COVER
MMB
Low cost
10/29 REV_A1 Modify MX1 to MX5
Main strem
TOP View pin1 at left
10/19 REV_A1 Modify pin count
FFC Cable 1.0mm Pitch
10/24 REV_A1 Swap net
10/25 REV_A1 Swap net and change footprint
01/18 REV_3B Add C683,C684 for EMI
FFC Cable 1.0mm Pitch
NEW CARD'S POWER SWITCH
CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)
H=0.8mm
New card (BTO)
09/26 REV_A1 Add
09/26 REV_A1 Add
12/07 REV_A1 Change footprint
10/19 REV_A1 Change footprint
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
New Card/Keyboard/WTB
Tuesday, January 22, 2008
Sheet 28 of 37

SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

10/26 REV_A1 Add R64,R73,R176

09/20 REV_A1 Modify

09/29 REV_A1 Modify

10/26 REV_A1 Modify

10/22 REV_A1 Modify

10/24 REV_A1 Add

09/20 REV_A1 Modify

01/08 REV_3B Add to control MMB LED

10/22 REV_A1 Modify

SM BUS PU

I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

12/05 REV_3A R38 DNI,R47 mount

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

ADDRESS: A0H

SPI FLASH

INTERNAL KEYBOARD STRIP SET

CIR (Copy from PB2A)

Only for 8769/775C

10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define
12/07 REV_3A Change P/N

WPC8763LDG:	AL008763B00
WPC8769LDG:	AJ087690F08
WPCE775L:	AJ007750F00
WPCE775C:	AJ007750F01

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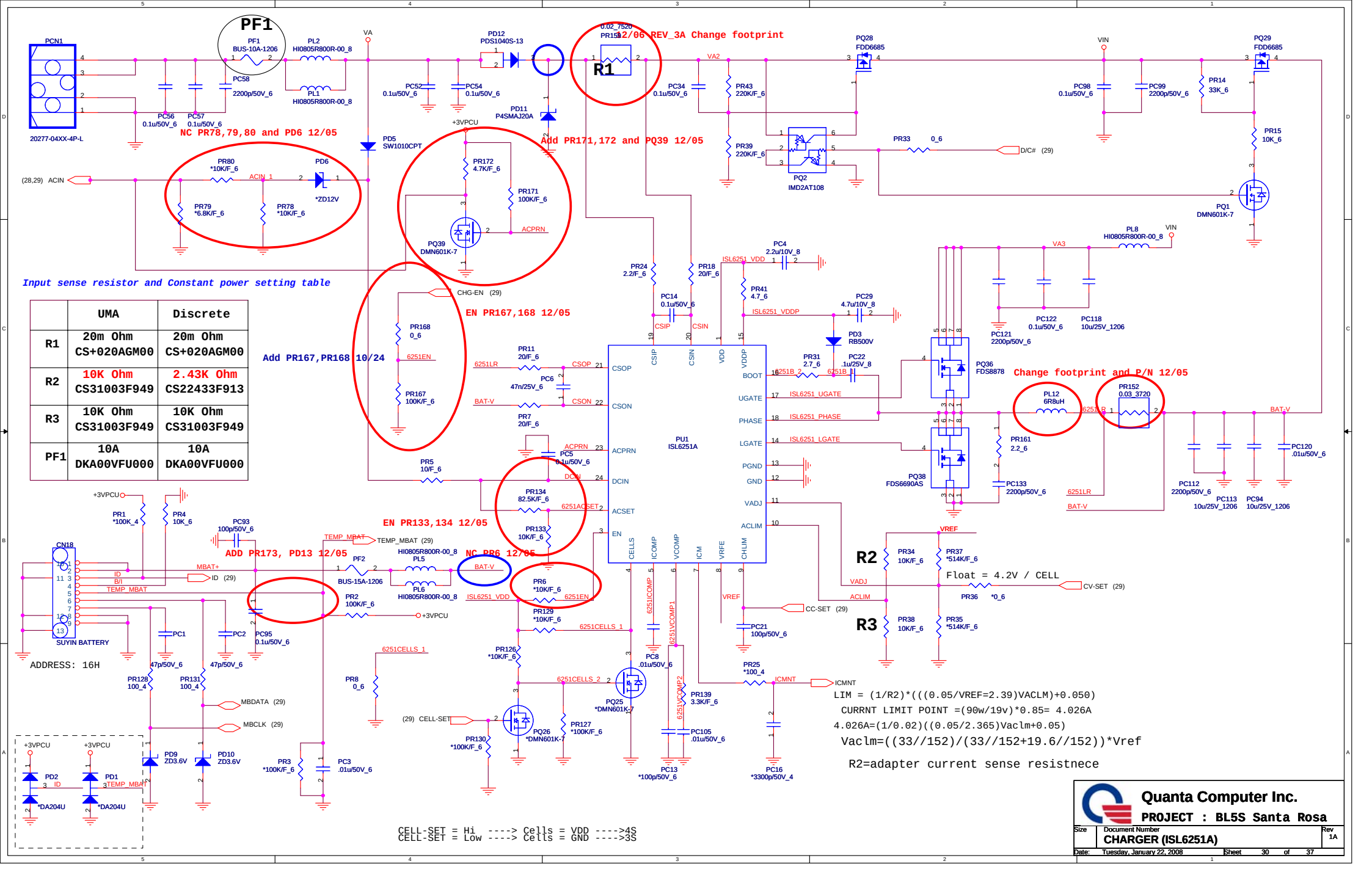
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	EC-WPCE775C	1A
Date: Tuesday, January 22, 2008	Sheet 29 of 37	



	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000

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PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	CHARGER (ISL6251A)	1A

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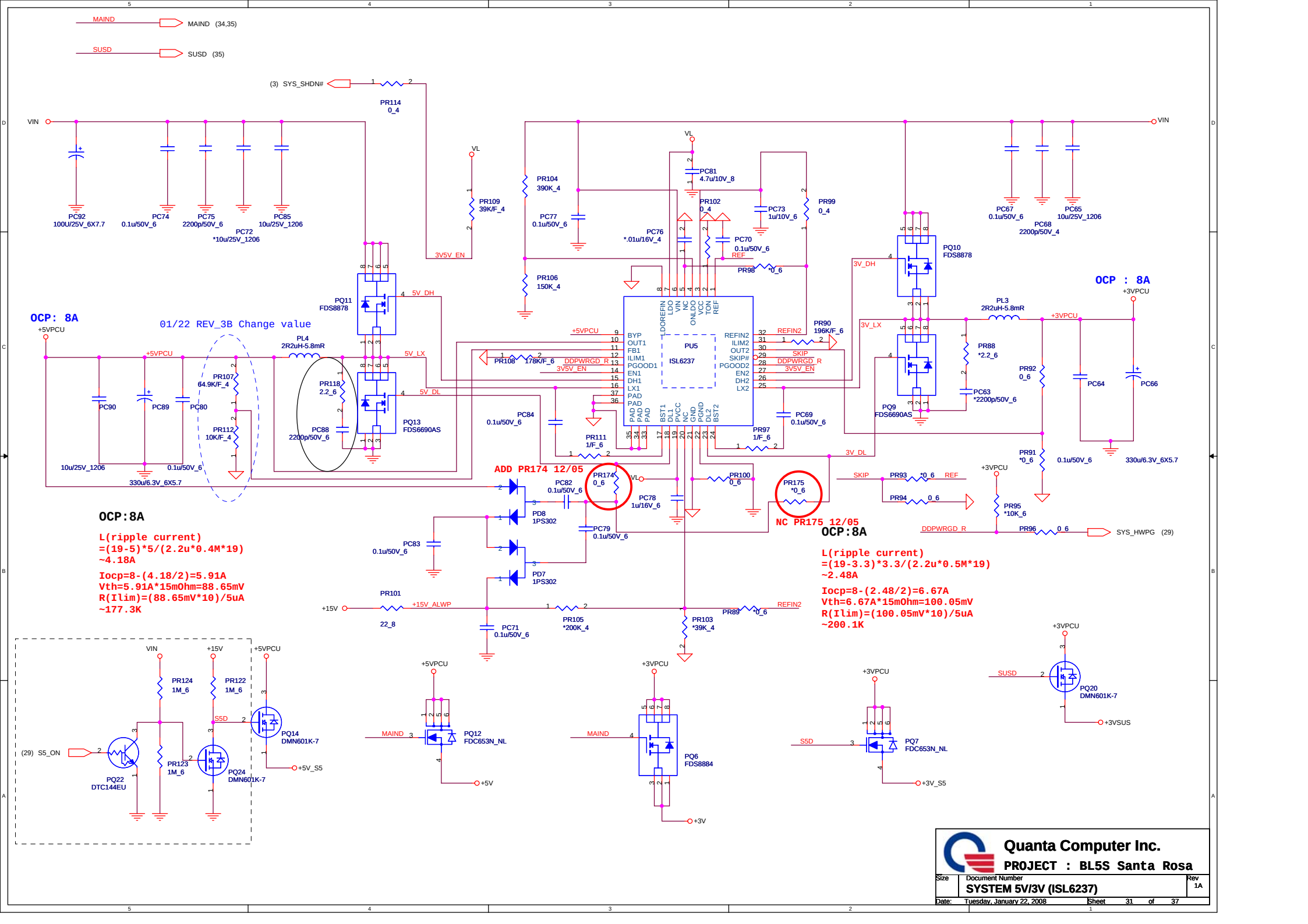
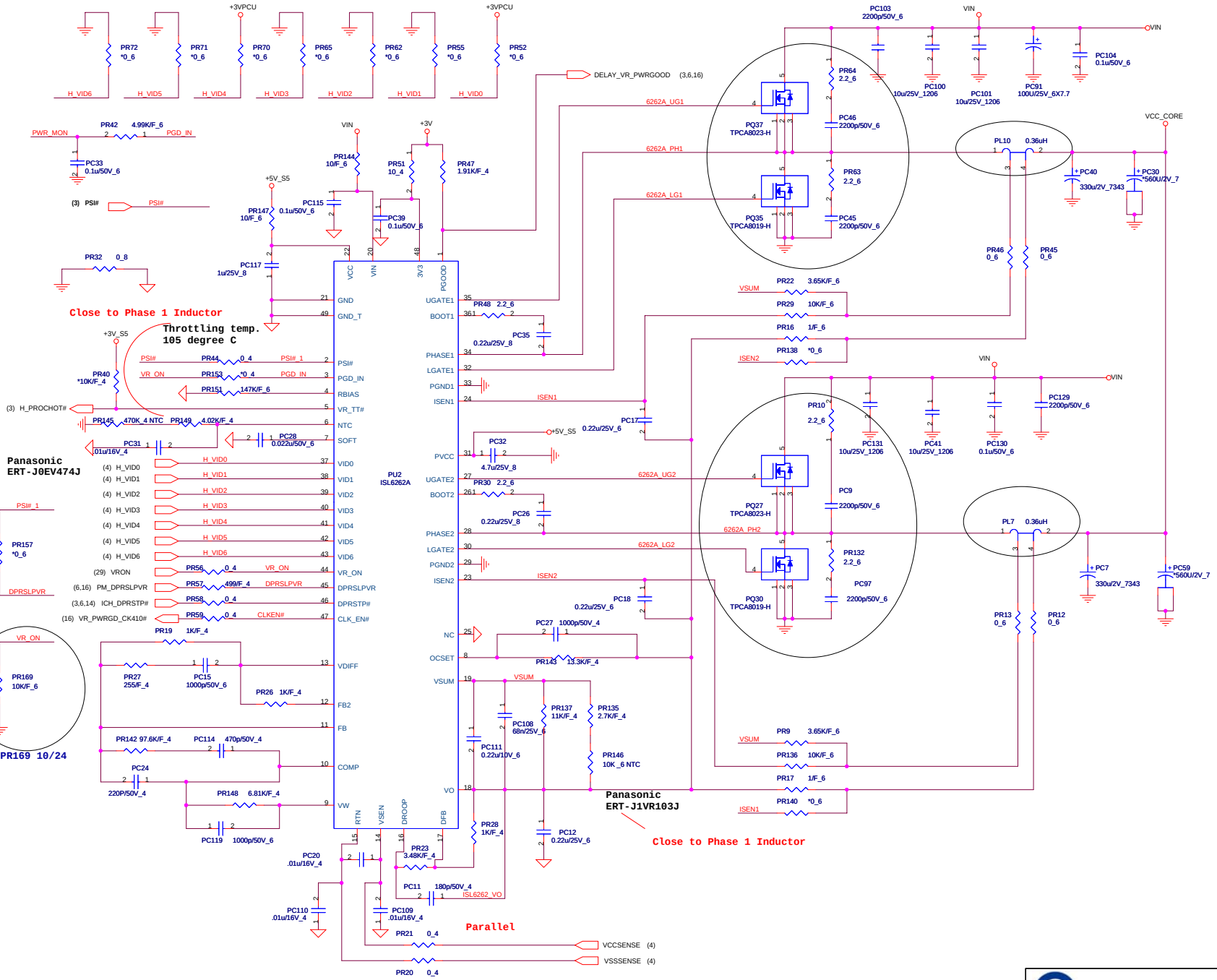

MAIND
MAIND (34,35)
SUSD
SUSD (35)
(3) SYS_SHDN#
PR114 0_4
VIN
VL
3V5V_EN
PC92 100U/25V_6X7.7
PC74 0.1u/50V_6
PC75 2200p/50V_6
PC72 *10u/25V_1206
PC85 10u/25V_1206
PR109 39K/F_4
PR104 390K_4
PC77 0.1u/50V_6
PR106 150K_4
PC81 4.7u/10V_8
PR102 0_4
PC73 1u/10V_6
PR99 0_4
PC76 *.01u/16V_4
PC70 0.1u/50V_6
REF
PR98 *0_6
PC67 0.1u/50V_6
PC68 2200p/50V_4
PC65 10u/25V_1206
PQ10 FDS8878
3V_DH
OCP : 8A
+3VPCU
PL3 2R2uH-5.8mR
3V_LX
PR88 *2.2_6
PC63 *2200p/50V_6
PR92 0_6
PC64
PC66
PQ9 FDS6690AS
PR91 *0_6
0.1u/50V_6
330u/6.3V_6X5.7
OCP: 8A
+5VPCU
01/22 REV_3B Change value
PL4 2R2uH-5.8mR
5V_LX
5V_DH
PQ11 FDS8878
PR107 64.9K/F_4
PR112 10K/F_4
PR118 2.2_6
PC88 2200p/50V_6
5V_DL
PQ13 FDS6690AS
PC90
PC89
PC80
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PU5
ISL6237
LDOREFIN
LDO
VIN
NC
ONLOD
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
BST1
DL1
PVCC
NC
PGND
DL2
BST2
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR108 178K/F_6
DDPWRGD_R
PR90 196K/F_6
SKIP
PC84 0.1u/50V_6
PR111 1/F_6
PC69 0.1u/50V_6
PR97 1/F_6
3V_DL
ADD PR174 12/05
PR174 0_6
PR100 0_6
PR175 *0_6
NC PR175 12/05
PC82 0.1u/50V_6
PD8 1PS302
PC78 1u/16V_6
PC79 0.1u/50V_6
PD7 1PS302
PC83 0.1u/50V_6
PR93 *0_6
PR94 0_6
PR95 *10K_6
PR96 0_6
SYS_HWPG (29)
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=5.91A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA
~177.3K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
PR101
+15V
+15V_ALWP
22_8
PR105 *200K_4
PC71 0.1u/50V_6
PR103 *39K_4
PR89 *0_6
REFIN2
PR124 1M_6
PR122 1M_6
S5D
(29) S5_ON
PR123 1M_6
PQ22 DTC144EU
PQ24 DMN601K-7
PQ14 DMN601K-7
+5V_S5
PQ12 FDC653N_NL
+5V
PQ6 FDS8884
+3V
PQ7 FDC653N_NL
+3V_S5
PQ20 DMN601K-7
+3VSUS
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Tuesday, January 22, 2008
Sheet 31 of 37


+3VPCU
PR72 *0_6
PR71 *0_6
PR70 *0_6
PR65 *0_6
PR62 *0_6
PR55 *0_6
PR52 *0_6
H_VID6
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
DELAY_VR_PWRGOOD (3,6,16)
PWR_MON
PR42 4.99K/F_6
PGD_IN
PC33 0.1u/50V_6
(3) PSI#
PSI#
VIN
+3V
+5V_S5
PR144 10/F_6
PR51 10_4
PR47 1.91K/F_4
PR147 10/F_6
PC115 0.1u/50V_6
PC39 0.1u/50V_6
PC117 1u/25V_8
PR32 0_8
Close to Phase 1 Inductor
Throttling temp.
105 degree C
+3V_S5
PR40 *10K/F_4
(3) H_PROCHOT#
PR145 470K_4 NTC
PR149 4.02K/F_4
PC28 0.022u/50V_6
PC31 .01u/16V_4
Panasonic
ERT-J0EV474J
PU2
ISL6262A
VCC
VIN
3V3
PGOOD
GND
GND_T
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
DPRSTP#
CLK_EN#
VDIFF
FB2
FB
COMP
VW
RTN
VSEN
DROOP
DFB
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
NC
OCSET
VSUM
VO
PR44 0_4
PR153 *0_4
PR151 147K/F_6
PR157 *0_6
PR56 0_4
PR57 499/F_4
PR58 0_4
PR59 0_4
PR19 1K/F_4
PR27 255/F_4
PC15 1000p/50V_6
PR26 1K/F_4
PR142 97.6K/F_4
PC114 470p/50V_4
PC24 220P/50V_4
PR148 6.81K/F_4
PC119 1000p/50V_6
PR169 10K/F_6
Add PR169 10/24
PR48 2.2_6
PC35 0.22u/25V_8
PR30 2.2_6
PC26 0.22u/25V_8
PC32 4.7u/25V_8
PC17 0.22u/25V_6
PC18 0.22u/25V_6
PC27 1000p/50V_4
PR143 13.3K/F_4
PR137 11K/F_4
PR135 2.7K/F_4
PC108 68n/25V_6
PC111 0.22u/10V_6
PR146 10K_6 NTC
PR28 1K/F_4
PC12 0.22u/25V_6
PR23 3.48K/F_4
PC11 180p/50V_4
ISL6262_VO
PC20 .01u/16V_4
PC110 .01u/16V_4
PC109 .01u/16V_4
Parallel
PR21 0_4
PR20 0_4
VCCSENSE (4)
VSSSENSE (4)
6262A_UG1
6262A_PH1
6262A_LG1
6262A_UG2
6262A_PH2
6262A_LG2
PQ37 TPCA8023-H
PQ35 TPCA8019-H
PQ27 TPCA8023-H
PQ30 TPCA8019-H
PR64 2.2_6
PC46 2200p/50V_6
PR63 2.2_6
PC45 2200p/50V_6
PC9 2200p/50V_6
PR132 2.2_6
PC97 2200p/50V_6
PC103 2200p/50V_6
PC100 10u/25V_1206
PC101 10u/25V_1206
PC91 100U/25V_6X7.7
PC104 0.1u/50V_6
PL10 0.36uH
PL7 0.36uH
PC40 330u/2V_7343
PC30 560U/2V_7
PC7 330u/2V_7343
PC59 560U/2V_7
VCC_CORE
PR46 0_6
PR45 0_6
PR13 0_6
PR12 0_6
PR22 3.65K/F_6
PR29 10K/F_6
PR16 1/F_6
PR138 *0_6
PR10 2.2_6
PC131 10u/25V_1206
PC41 10u/25V_1206
PC130 0.1u/50V_6
PC129 2200p/50V_6
PR9 3.65K/F_6
PR136 10K/F_6
PR17 1/F_6
PR140 *0_6
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
VSUM
ISEN1
ISEN2
VIN
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
CPU CORE(ISL6262A)
Rev
1A
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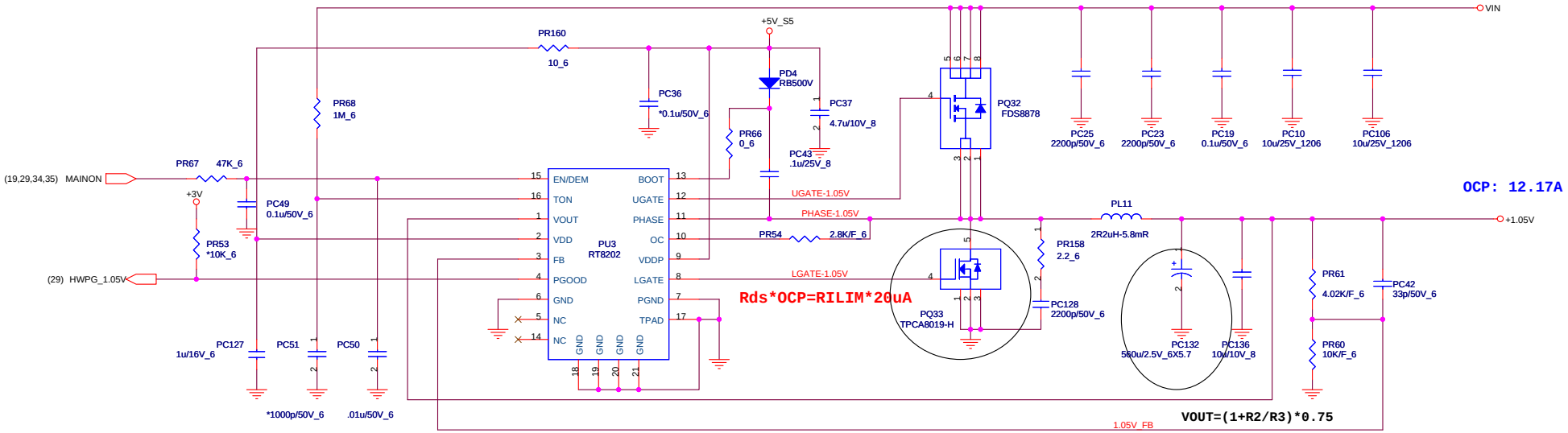

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

AOL1412 Rds=4.6mOhm
12.17A OCP --- OC=2.8K

SI7636 Rds=4.8mOhm
11.67A OCP --- OC=2.8K

Quanta Computer Inc.
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Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A

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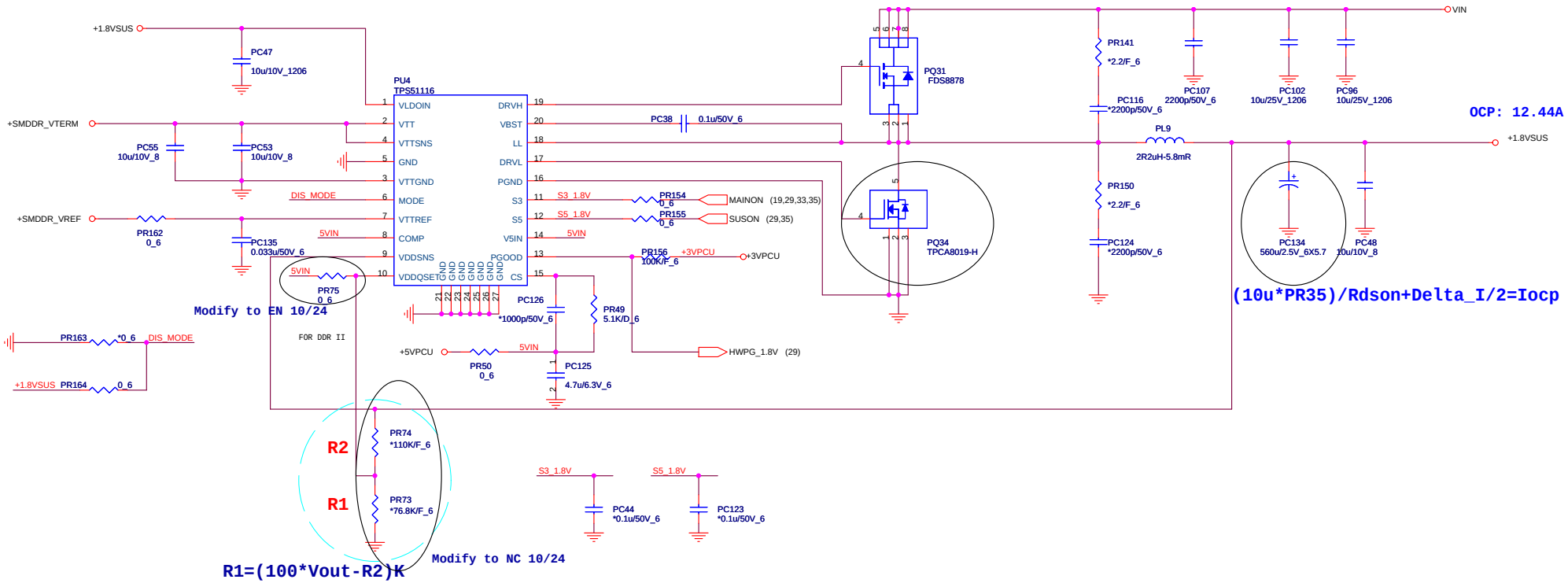
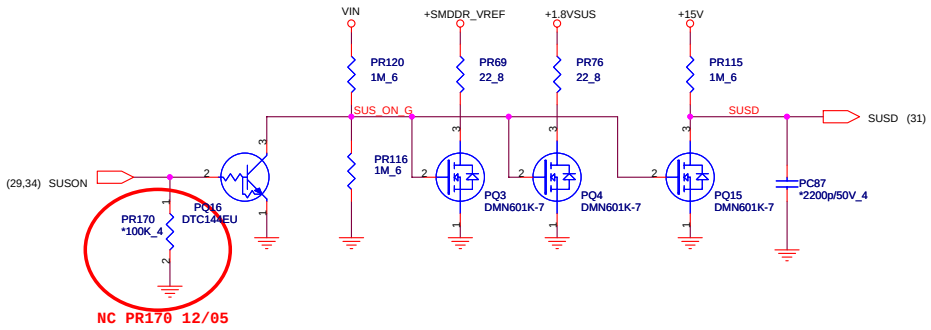
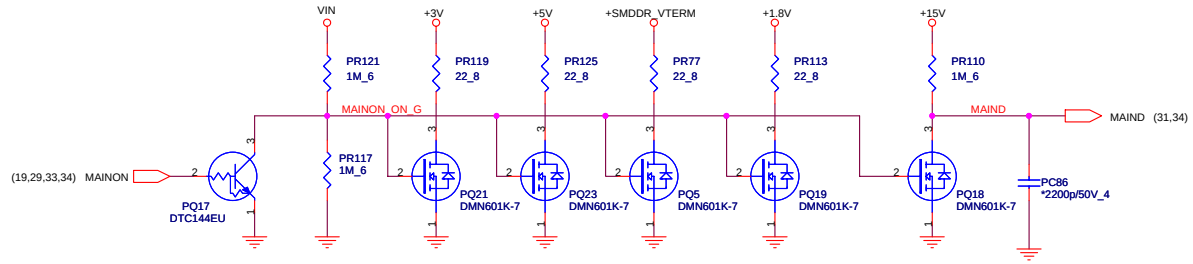
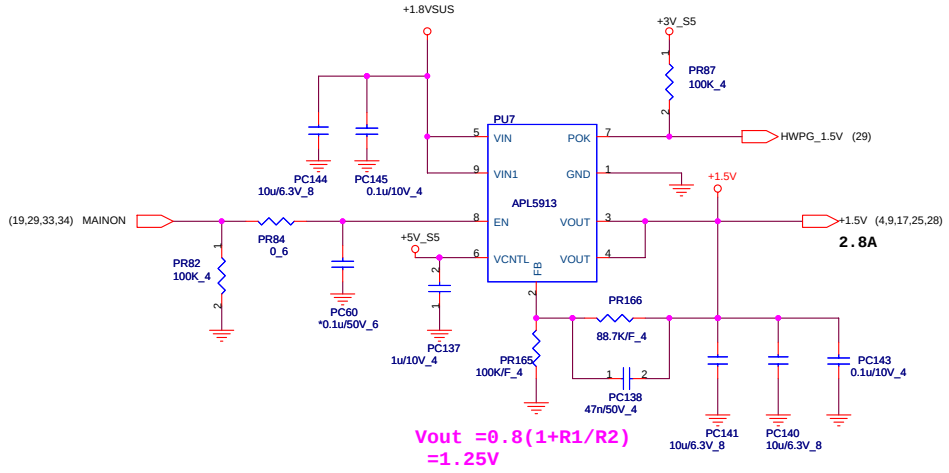
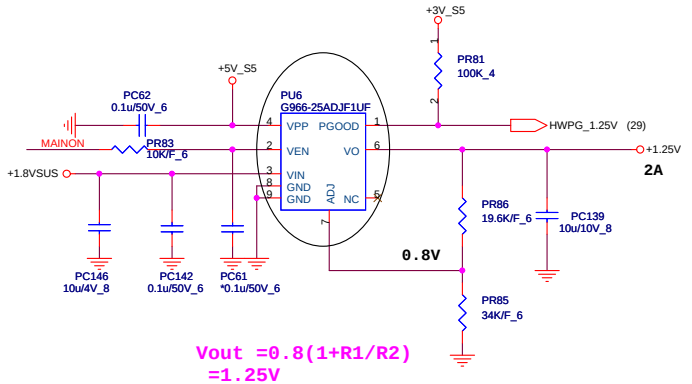


Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 34 of 37	









Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A

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Model	REV	DATE	CHANGE LIST	NOTE
BL5S	00	20070824	FIRST RELEASED : 20070824	
	1A	20070914	FIRST RELEASED : E200709-2519	

Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Change List	1A

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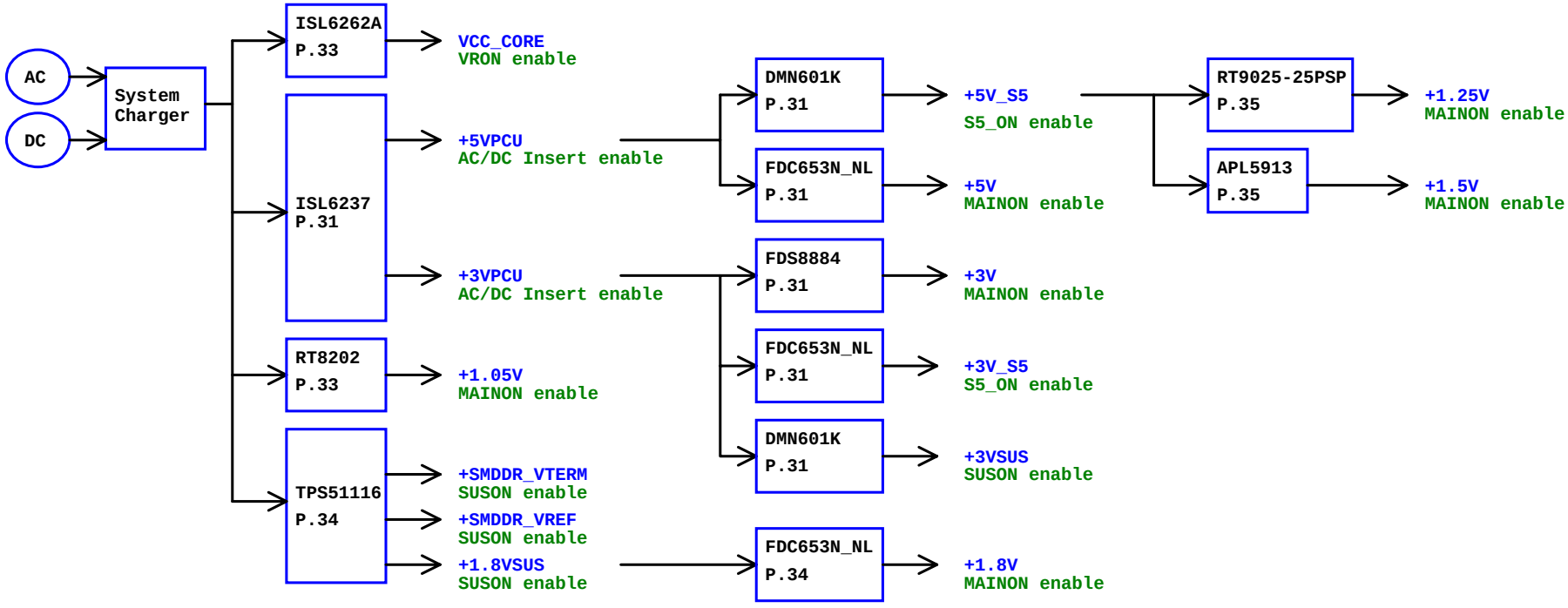

Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M