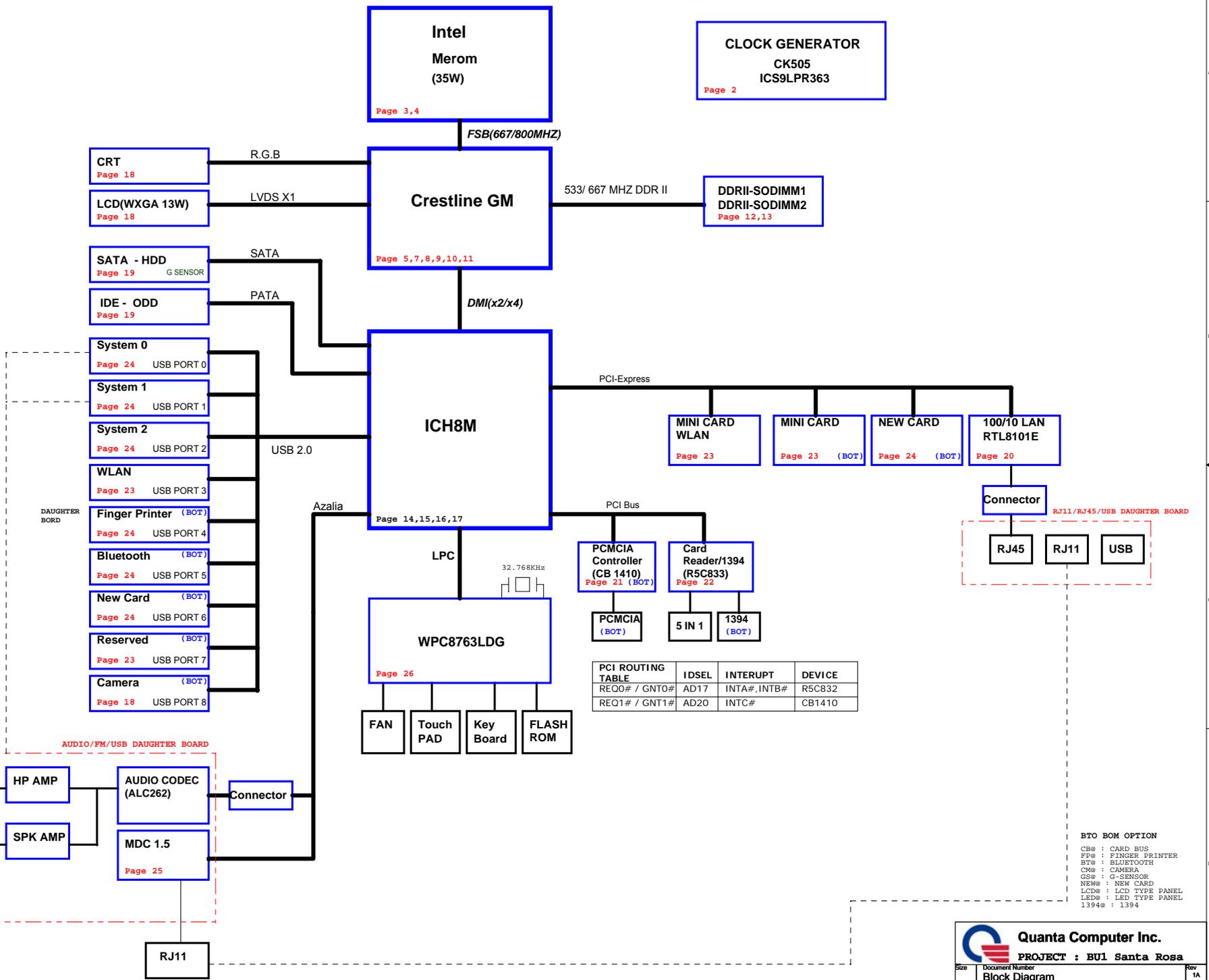


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
- +3V_S5
- +3VSUS
- +3V
- +5VPCU
- +5V_S5
- +5V
- SMDDR_VTERM
- SMDDR_VREF

BU1 Block Diagram



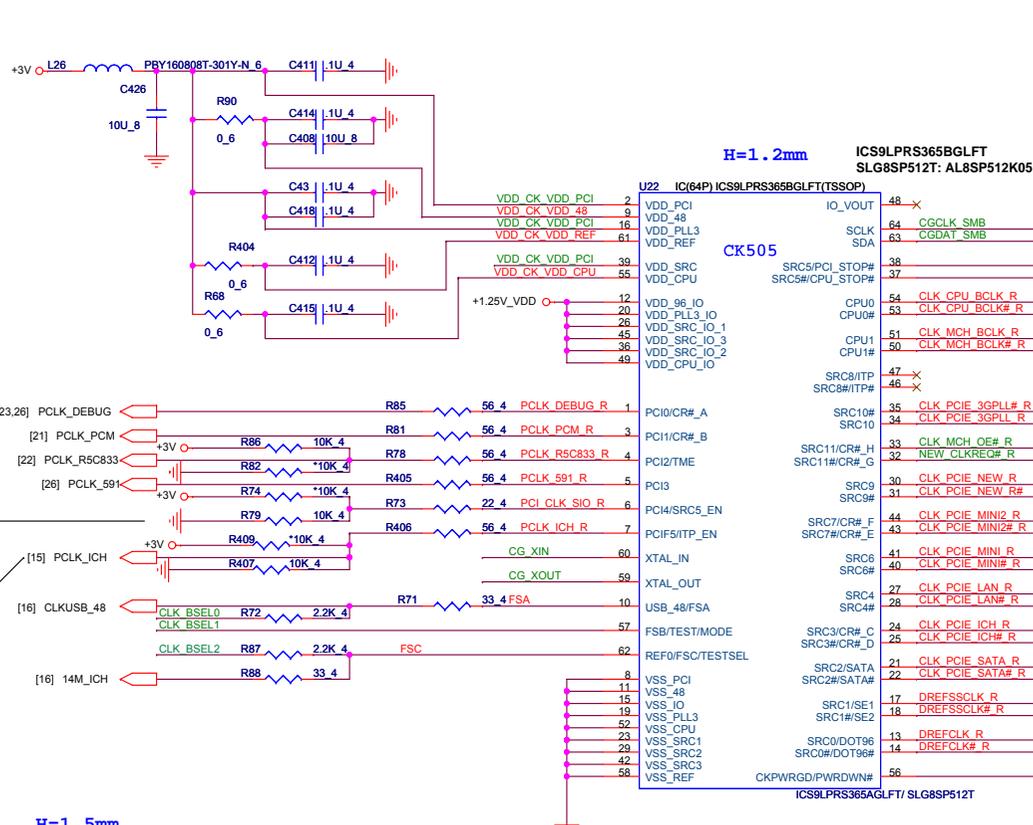
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#, INTB#	R5C832
REQ1# / GNT1#	AD20	INTC#	CB1410

BTO BOM OPTION

- CB@ : CARD BUS
- FP@ : FINGER PRINTER
- BT@ : BLUETOOTH
- CM@ : CAMERA
- GS@ : G-SENSOR
- NEW@ : NEW CARD
- LCID@ : LCD TYPE PANEL
- LED@ : LED TYPE PANEL
- 1394@ : 1394

Clock Generator

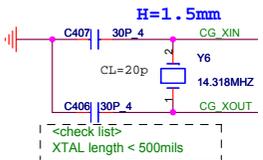
Clock Gen Differential IO power



<check list>
 PC14/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock. If PD be detect at power-on the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP(Default is setting to PCI_STOP/CUP_SOTP)

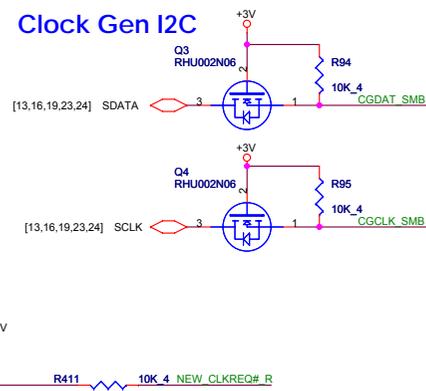
<check list>
 PC15/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock. If PD be detect at power-on the CK505 will setting Pin 46/47 to SRC8(Default is setting to SRC8)

During initial power-up be used to sample FSB speed with FSA/B/C



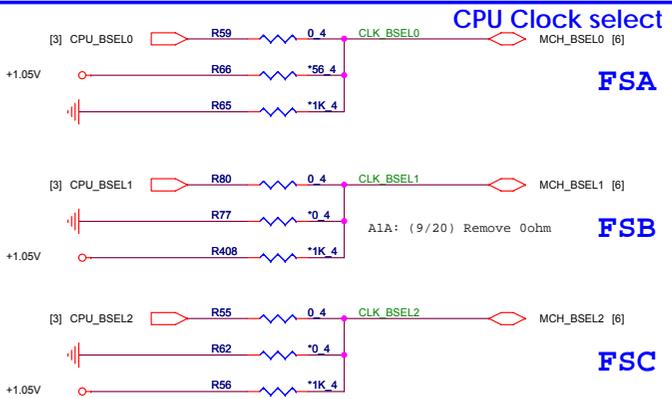
- <check list>
- (1)PC12/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.
- (2)PC14/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock. If PD be detect at power-on the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP (Default is setting to PCI_STOP/CUP_SOTP)
- (3)PC15/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock. If PD be detect at power-on the CK505 will setting Pin 46/47 to SRC8 (Default is setting to SRC8)
- (4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M, Pin 37, 38 will fixed be use CPU_Stop and PCI_Stop.
- (5)SLG505YC64 CK505 Standar parts follow standar setting

Clock Gen I2C

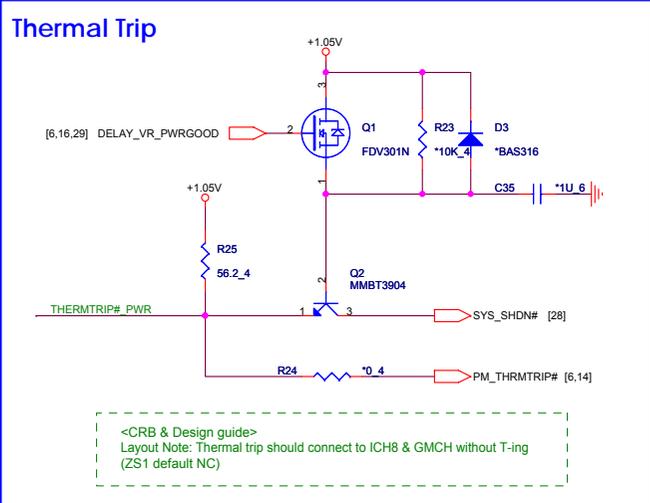
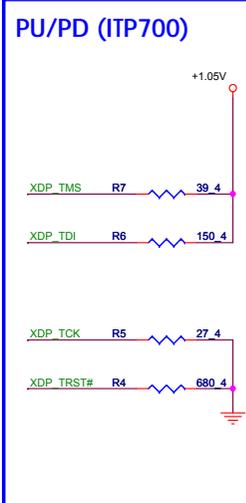
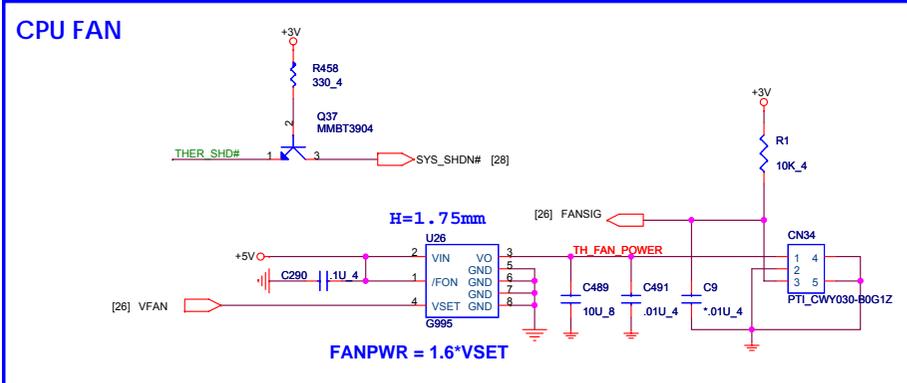
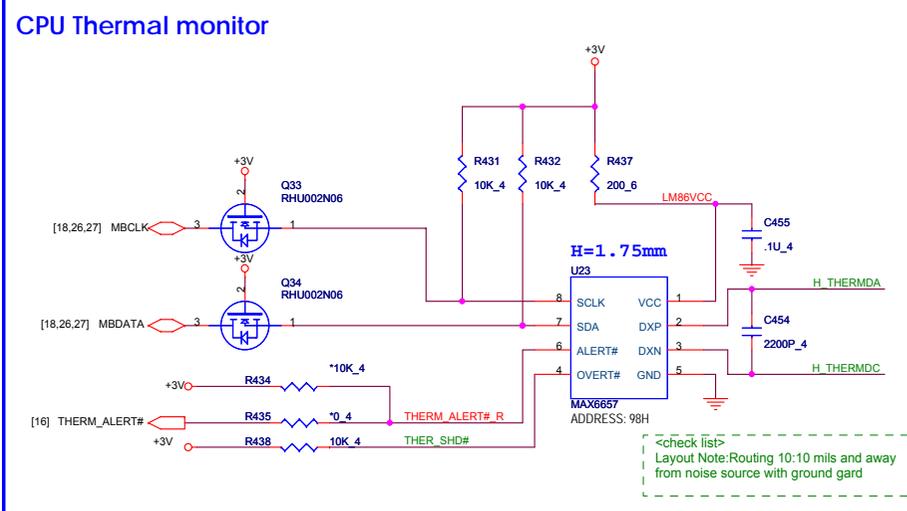
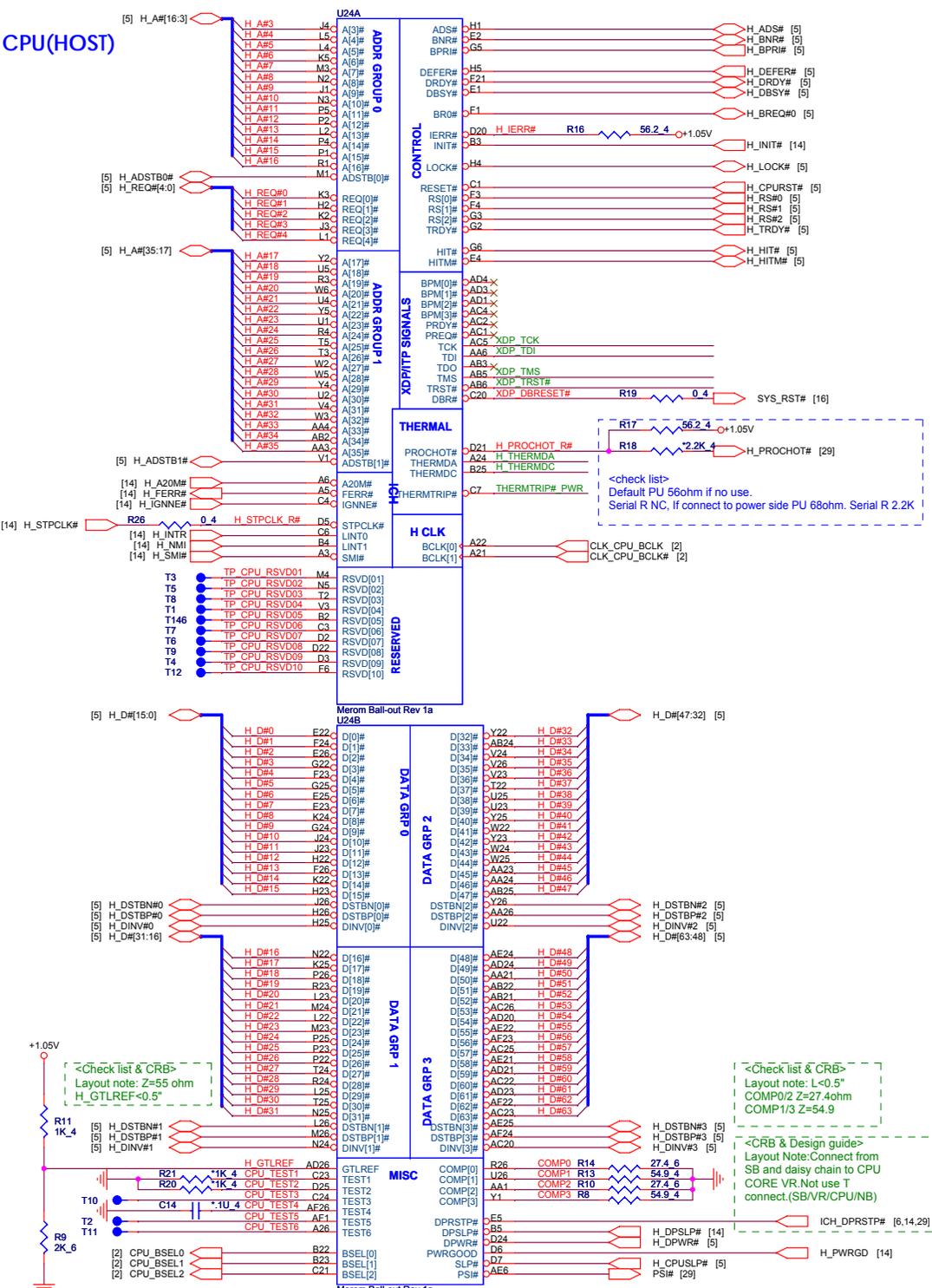


BSEL Frequency Select Table

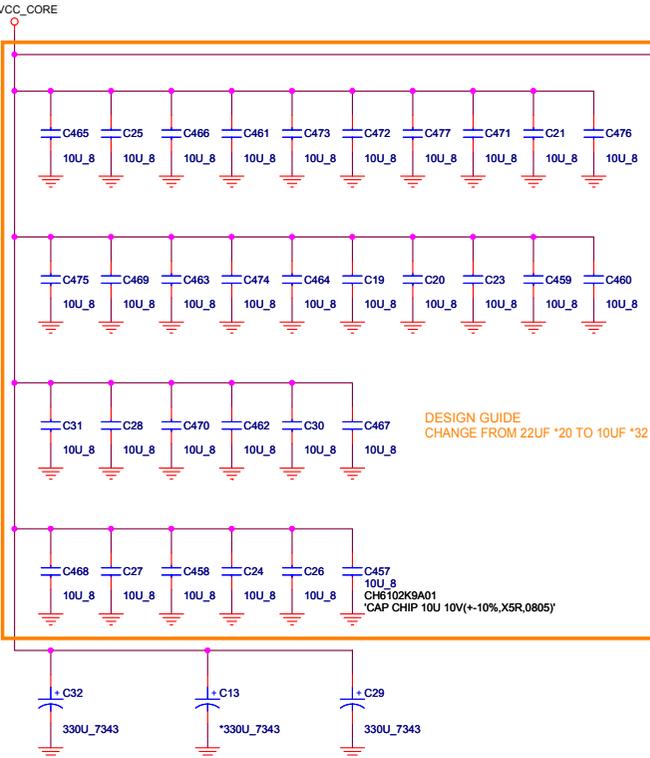
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
 Size: _____ Document Number: **CLK_GEN./ CK505** Rev: 1A
 Date: Monday, March 26, 2007 Sheet 2 of 33



CPU(Power)



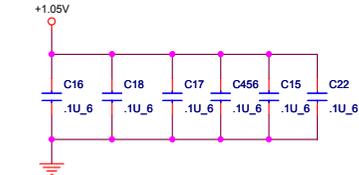
<Check list>
 Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
 Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

DESIGN GUIDE
 CHANGE FROM 22UF *20 TO 10UF *32

10U 8
 CH6102K9A01
 CAP CHIP 10U 10V(+10%,X5R,0805)

U24C		U24D	
A7	VCC[001]	AB20	VCC[068]
A9	VCC[002]	AB7	VCC[069]
A10	VCC[003]	AC7	VCC[070]
A12	VCC[004]	AC9	VCC[071]
A13	VCC[005]	AC12	VCC[072]
A15	VCC[006]	AC15	VCC[073]
A17	VCC[007]	AC17	VCC[074]
A18	VCC[008]	AC18	VCC[075]
A20	VCC[009]	AD7	VCC[076]
B7	VCC[010]	AD9	VCC[077]
B9	VCC[011]	AD10	VCC[078]
B10	VCC[012]	AD12	VCC[079]
B12	VCC[013]	AD14	VCC[080]
B14	VCC[014]	AD17	VCC[081]
B15	VCC[015]	AD18	VCC[082]
B17	VCC[016]	AE9	VCC[083]
B18	VCC[017]	AE10	VCC[084]
B20	VCC[018]	AE12	VCC[085]
C9	VCC[019]	AE13	VCC[086]
C10	VCC[020]	AE15	VCC[087]
C12	VCC[021]	AE17	VCC[088]
C13	VCC[022]	AE18	VCC[089]
C15	VCC[023]	AE20	VCC[090]
C17	VCC[024]	AF9	VCC[091]
C18	VCC[025]	AF10	VCC[092]
D9	VCC[026]	AF12	VCC[093]
D10	VCC[027]	AF15	VCC[094]
D12	VCC[028]	AF17	VCC[095]
D14	VCC[029]	AF18	VCC[096]
D15	VCC[030]	AF20	VCC[097]
D17	VCC[031]	AG7	VCC[098]
D18	VCC[032]	AG9	VCC[099]
E7	VCC[033]	AG10	VCC[100]
E9	VCC[034]		
E10	VCC[035]	G21 CPU G21	VCCP[011]
E12	VCC[036]	V6 CPU V6	VCCP[02]
E13	VCC[037]	J6	VCCP[03]
E15	VCC[038]	K6	VCCP[04]
E17	VCC[039]	M6	VCCP[05]
E18	VCC[040]	J21	VCCP[06]
E20	VCC[041]	N21	VCCP[07]
F7	VCC[042]	N6	VCCP[08]
F9	VCC[043]	R6	VCCP[09]
F10	VCC[044]	T21	VCCP[10]
F12	VCC[045]	T6	VCCP[11]
F14	VCC[046]	V21	VCCP[12]
F15	VCC[047]	W21	VCCP[13]
F17	VCC[048]		VCCP[14]
F18	VCC[049]		VCCP[15]
F20	VCC[050]		VCCP[16]
AA7	VCC[051]		
AA9	VCC[052]		
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]		
AA15	VCC[056]		
AA17	VCC[057]		
AA18	VCC[058]		
AA20	VCC[059]		
AB9	VCC[060]		
AC10	VCC[061]		
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]		
	VCC[068]		
	VCC[069]		
	VCC[070]		
	VCC[071]		
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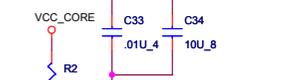
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 Ivcc Max 52A
 Ivccp Max 6A(VCCP supply before Vcc stable)
 Max 2A(VCCP supply after Vcc stable)
 Ivcca Max 130mA



<CRB>
 R for test only



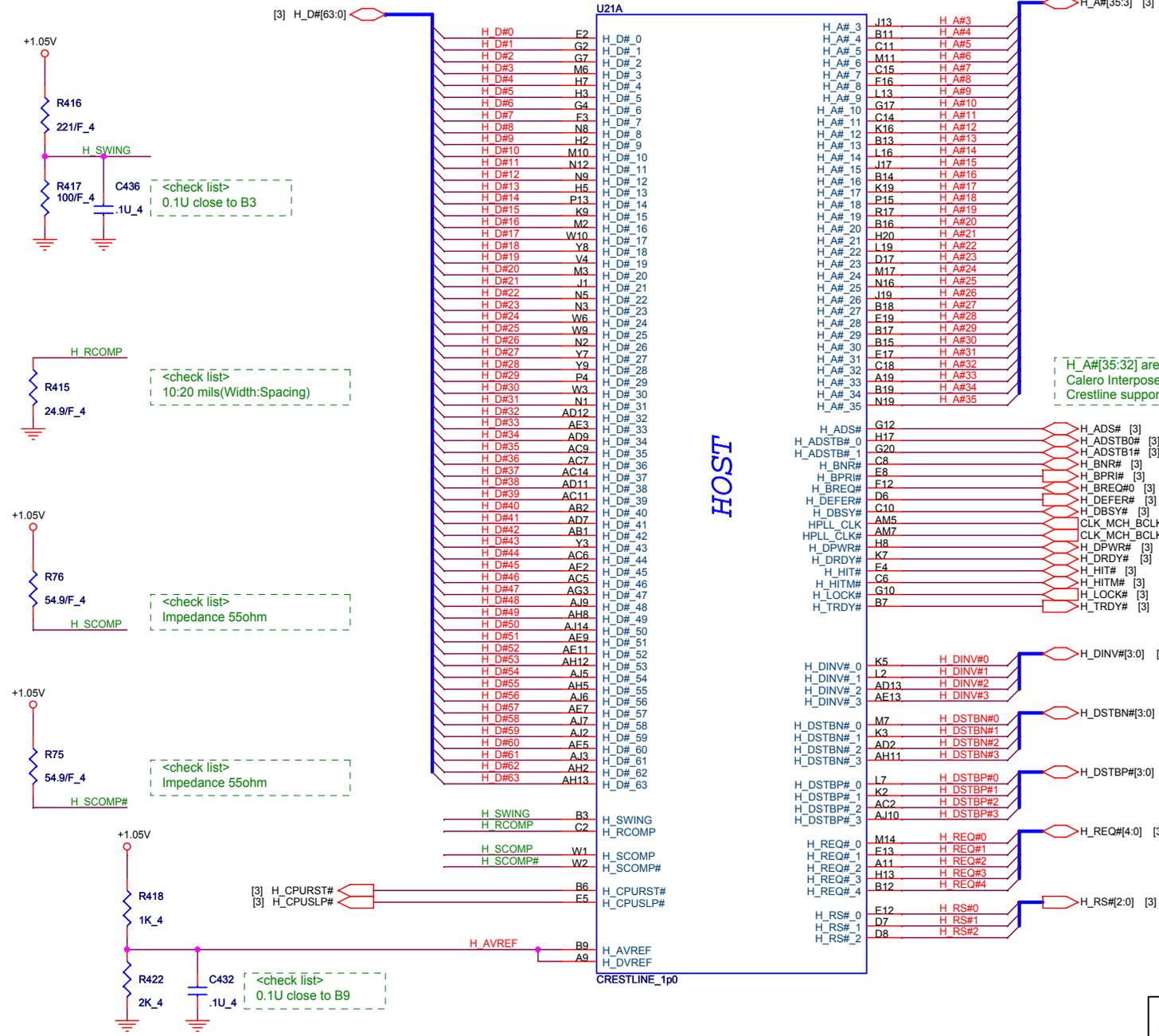
<CRB>
 .01U near to B26 ball



<Demo board>
 Routing 27.4ohm with 50mils spacing
 PU/PD near to CPU 1"



U24D		U24D	
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
AE2	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	VW1
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W4
C19	VSS[021]	VSS[102]	W23
C2	VSS[022]	VSS[103]	W26
C22	VSS[023]	VSS[104]	Y3
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D19	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E19	VSS[038]	VSS[119]	AB8
E14	VSS[039]	VSS[120]	AB13
E16	VSS[040]	VSS[121]	AB16
E21	VSS[041]	VSS[122]	AB19
E24	VSS[042]	VSS[123]	AB23
E5	VSS[043]	VSS[124]	AB26
F8	VSS[044]	VSS[125]	AC3
F11	VSS[045]	VSS[126]	AC6
F13	VSS[046]	VSS[127]	AC11
F16	VSS[047]	VSS[128]	AC14
F19	VSS[048]	VSS[129]	AC16
F2	VSS[049]	VSS[130]	AC19
F22	VSS[050]	VSS[131]	AC21
F25	VSS[051]	VSS[132]	AC24
G1	VSS[052]	VSS[133]	AD5
G4	VSS[053]	VSS[134]	AD8
G11	VSS[054]	VSS[135]	AD11
G23	VSS[055]	VSS[136]	AD13
G26	VSS[056]	VSS[137]	AD16
H3	VSS[057]	VSS[138]	AD19
H6	VSS[058]	VSS[139]	AD21
H21	VSS[059]	VSS[140]	AD22
H24	VSS[060]	VSS[141]	AD25
J5	VSS[061]	VSS[142]	AE1
J22	VSS[062]	VSS[143]	AE4
J25	VSS[063]	VSS[144]	AE8
K1	VSS[064]	VSS[145]	AE11
K4	VSS[065]	VSS[146]	AE14
K23	VSS[066]	VSS[147]	AE16
K26	VSS[067]	VSS[148]	AE19
L3	VSS[068]	VSS[149]	AE23
L6	VSS[069]	VSS[150]	AE26
L21	VSS[070]	VSS[151]	A2
L24	VSS[071]	VSS[152]	AF6
M2	VSS[072]	VSS[153]	AF8
M5	VSS[073]	VSS[154]	AF11
M22	VSS[074]	VSS[155]	AF13
M25	VSS[075]	VSS[156]	AF16
N1	VSS[076]	VSS[157]	AF19
N4	VSS[077]	VSS[158]	AF21
N23	VSS[078]	VSS[159]	A25
N26	VSS[079]	VSS[160]	A25
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	A25
	VSS[082]	VSS[163]	A25



H_A#[35:32] are not supported in Calero Interposer
Crestline support 36 bit address

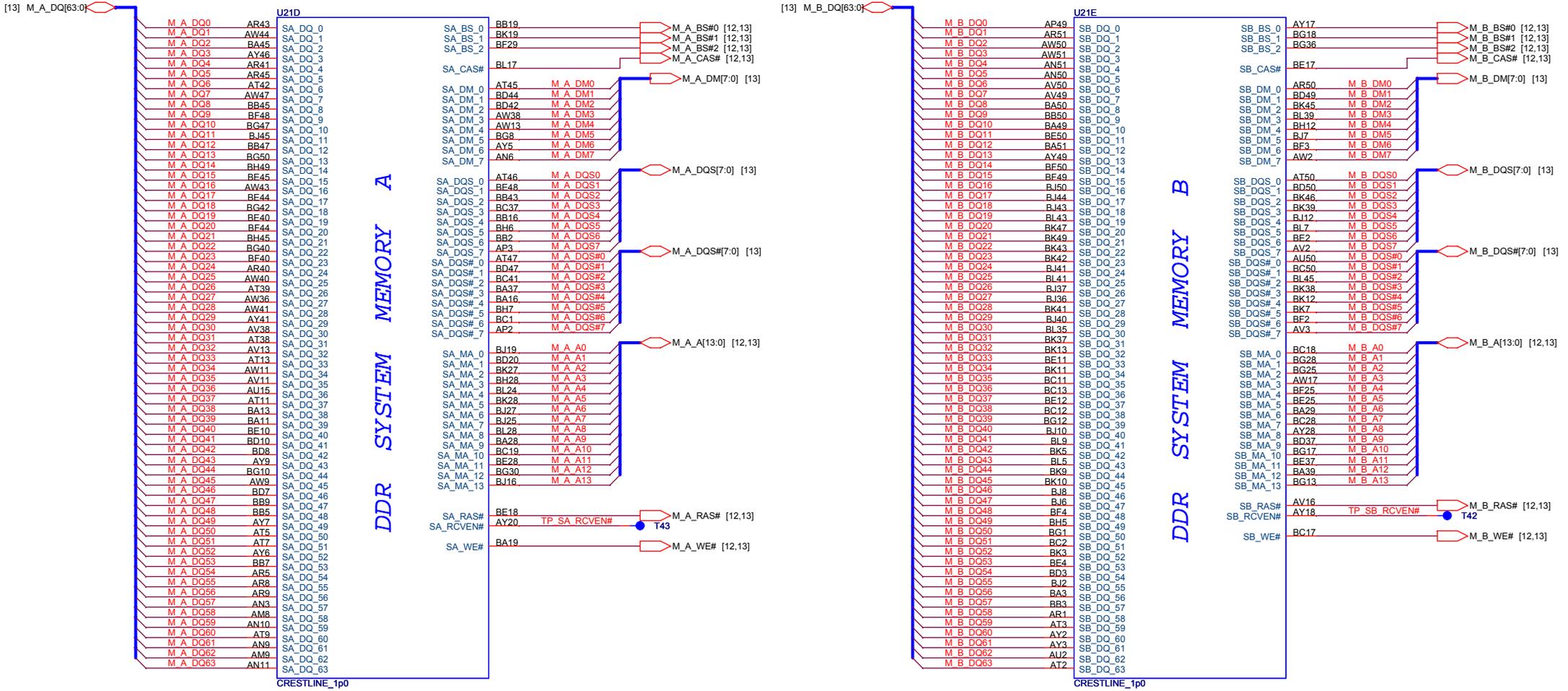
HOST

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

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GMCH HOST(1 of 7)

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NB(Memory controller)



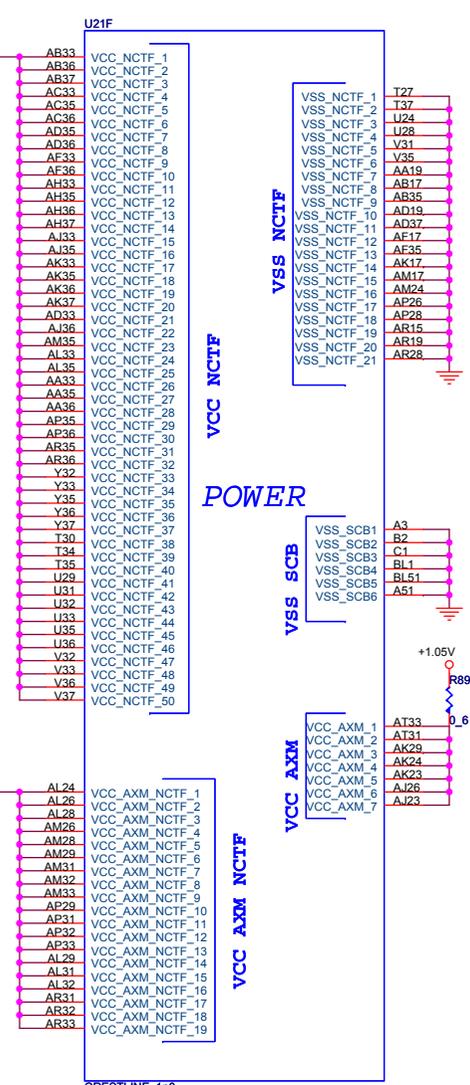
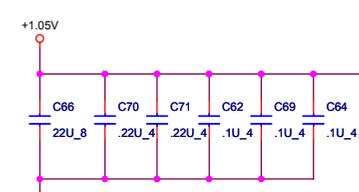
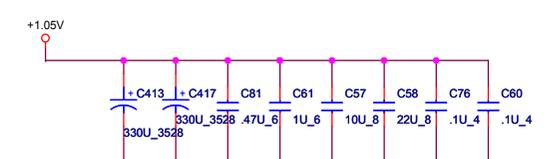
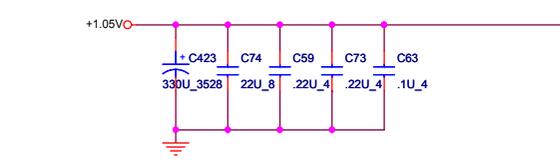
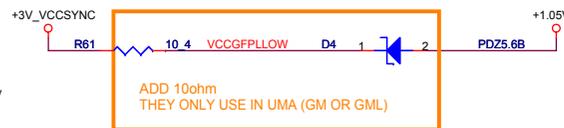
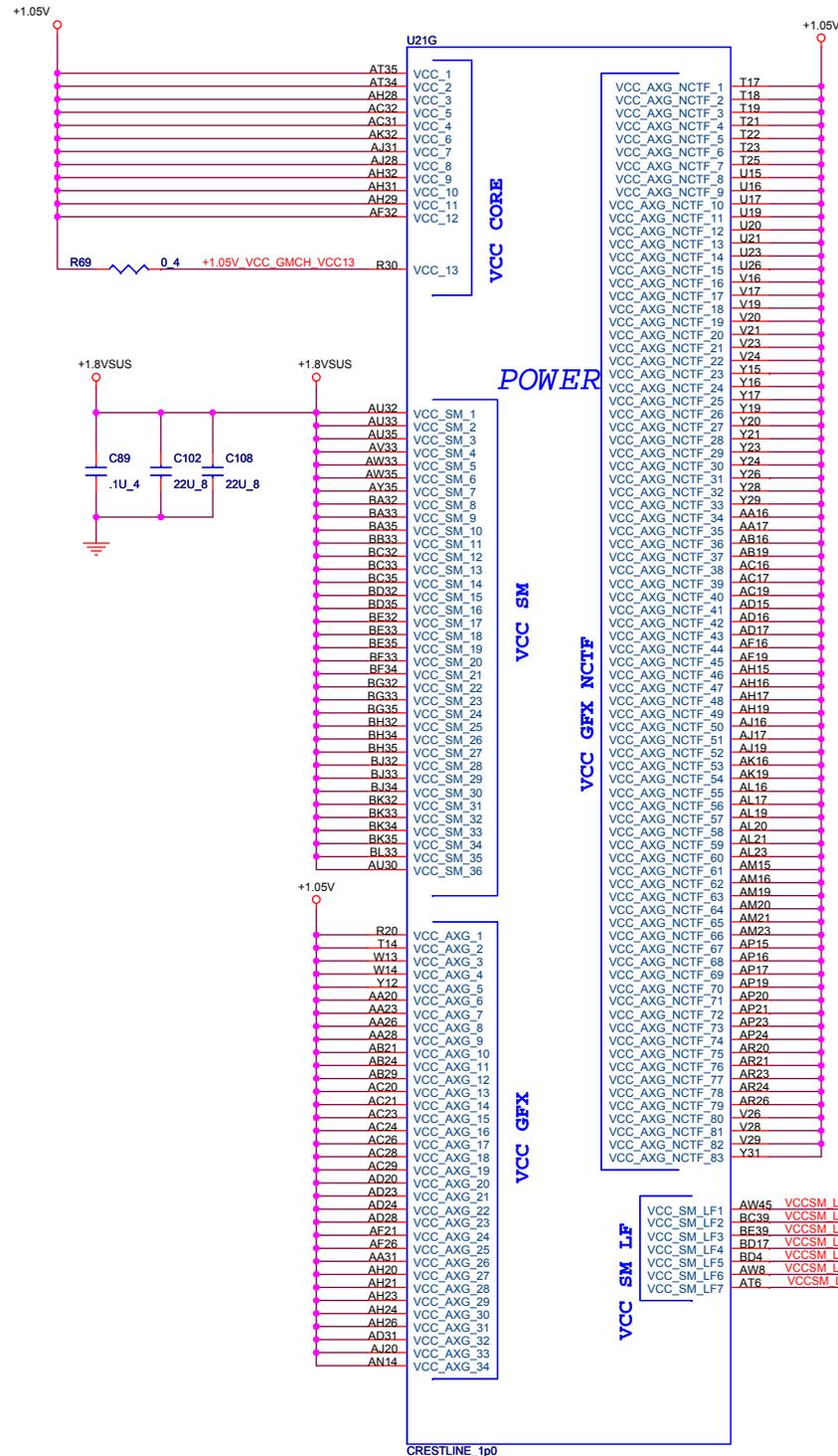
CRESTLINE_1p0

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size: MCH DDR(3 of 7) Rev 1A

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NB(Power-1)



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size Document Number
GMCH Power-1(4 of 7)

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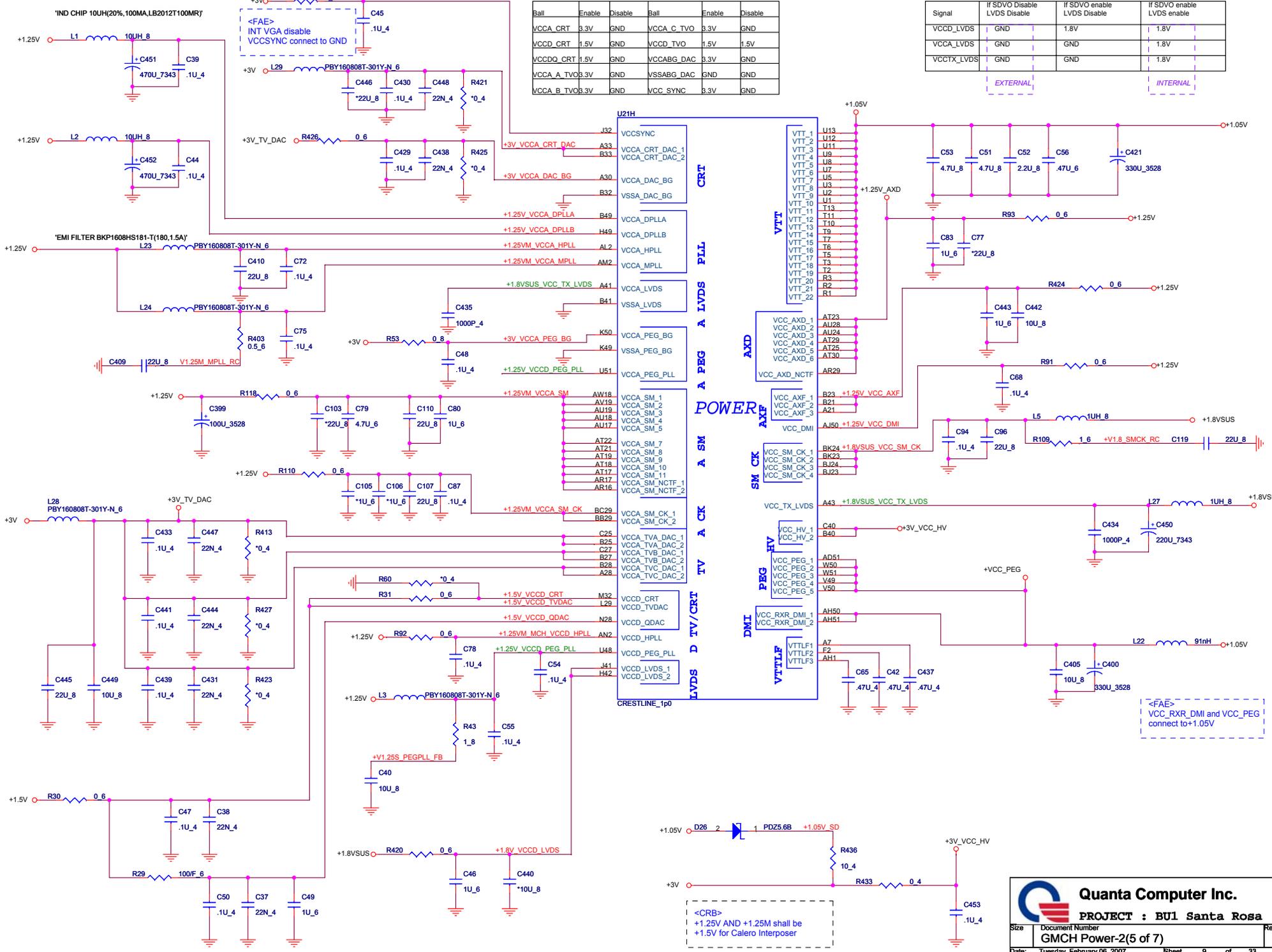
CRT/TV Disable/Enable guideline

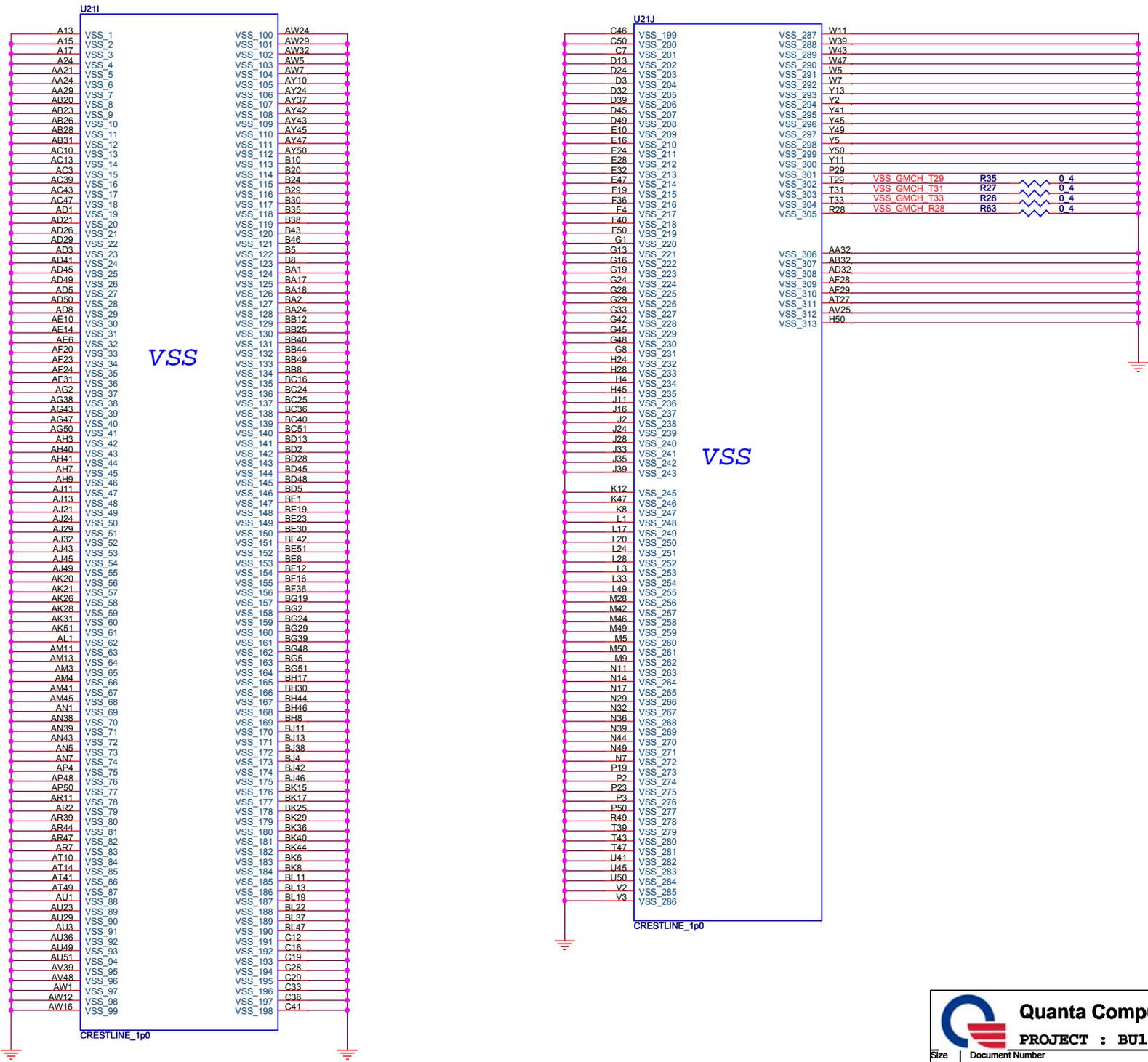
Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TV0	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TV0	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCCTX_LVDS	GND	GND	1.8V





Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
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GMCH Power-3(6 of 7) Rev 1A
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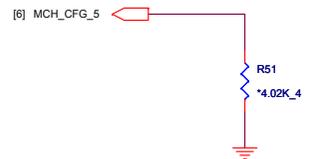
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMX4(Default)
-----------	--------------------------------------



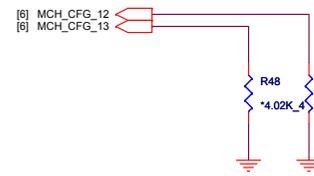
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



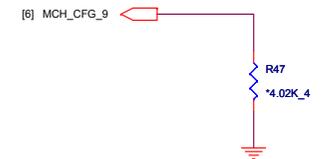
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

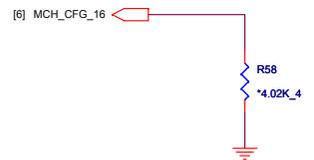


SDVO Present

Strap define at External DVI control page

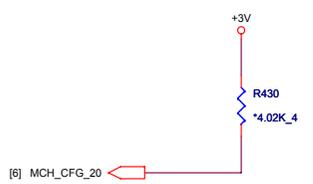
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



SDVO/PCIE Concurrent operation

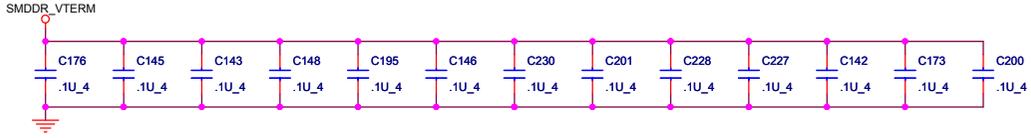
MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port
------------	--



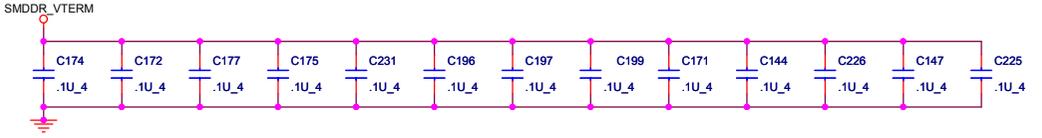
Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A
Date:	Monday, March 26, 2007	Sheet 11 of 33

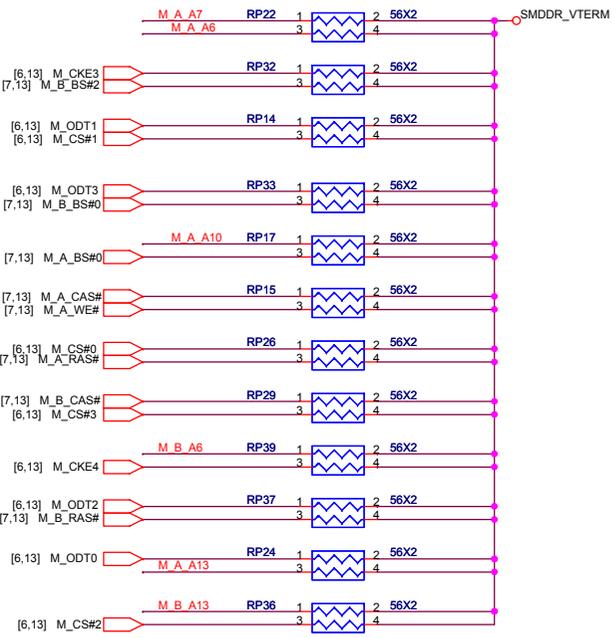
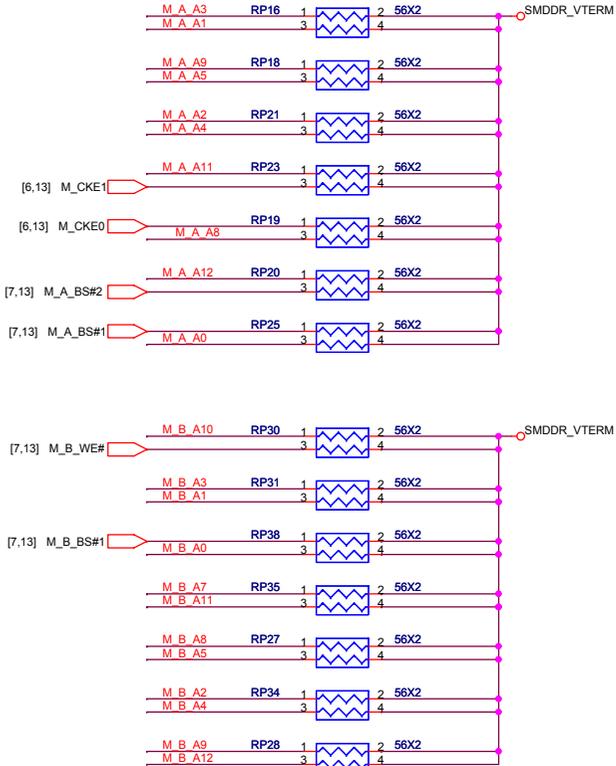
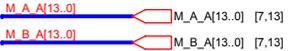
DDRII A CHANNEL



DDRII B CHANNEL

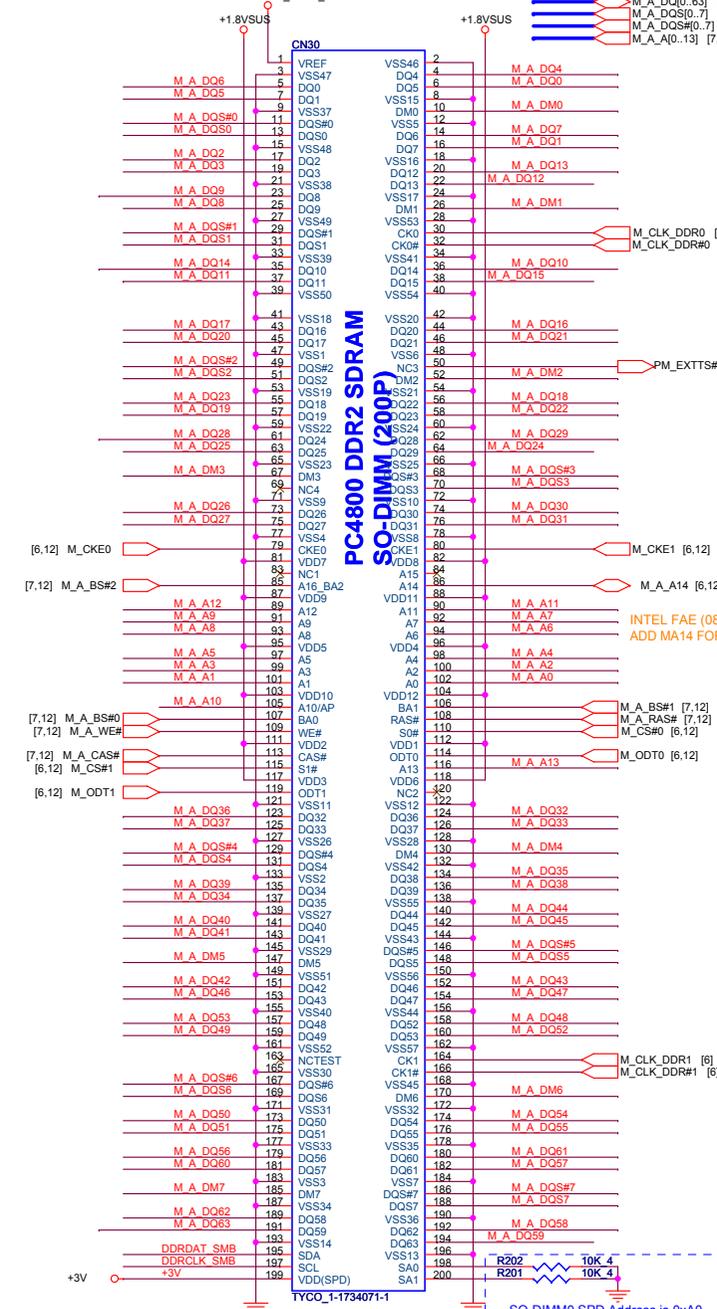


Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM



INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

DDR2 Dual channel A/B CONN



H: 5.6mm

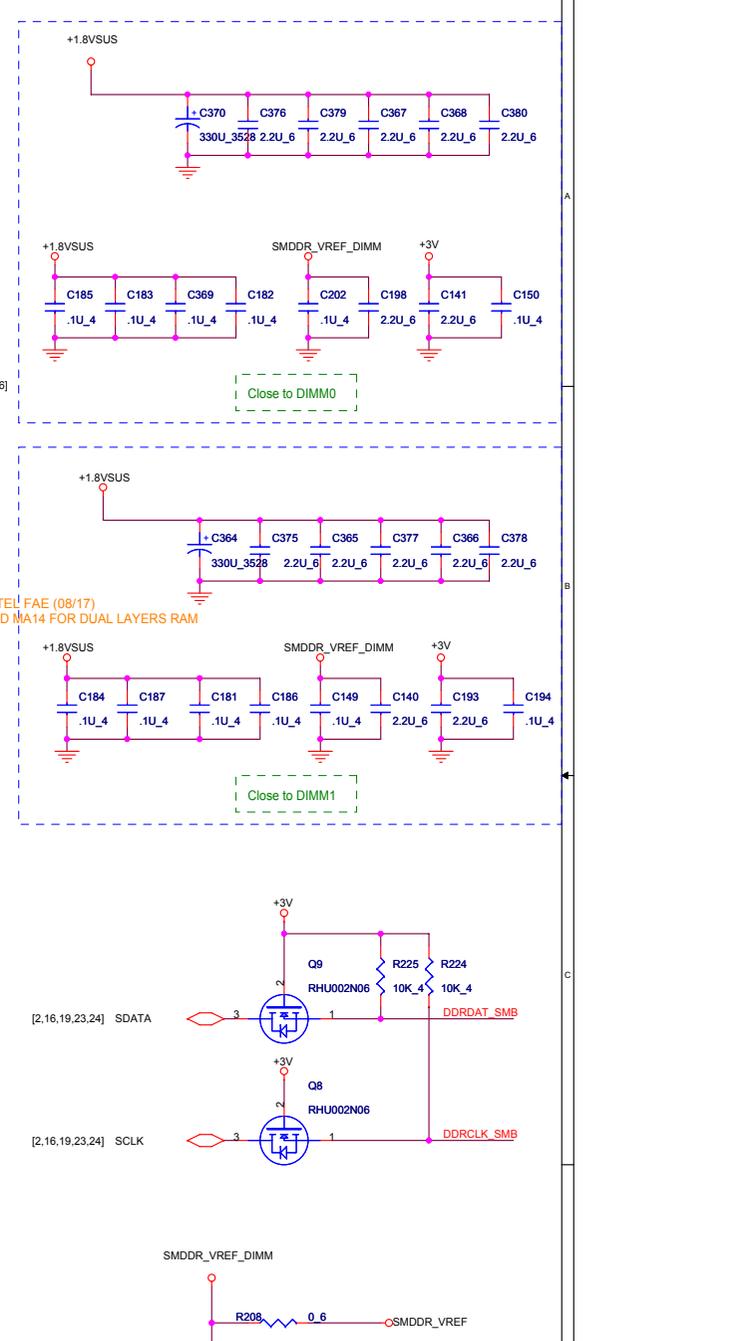
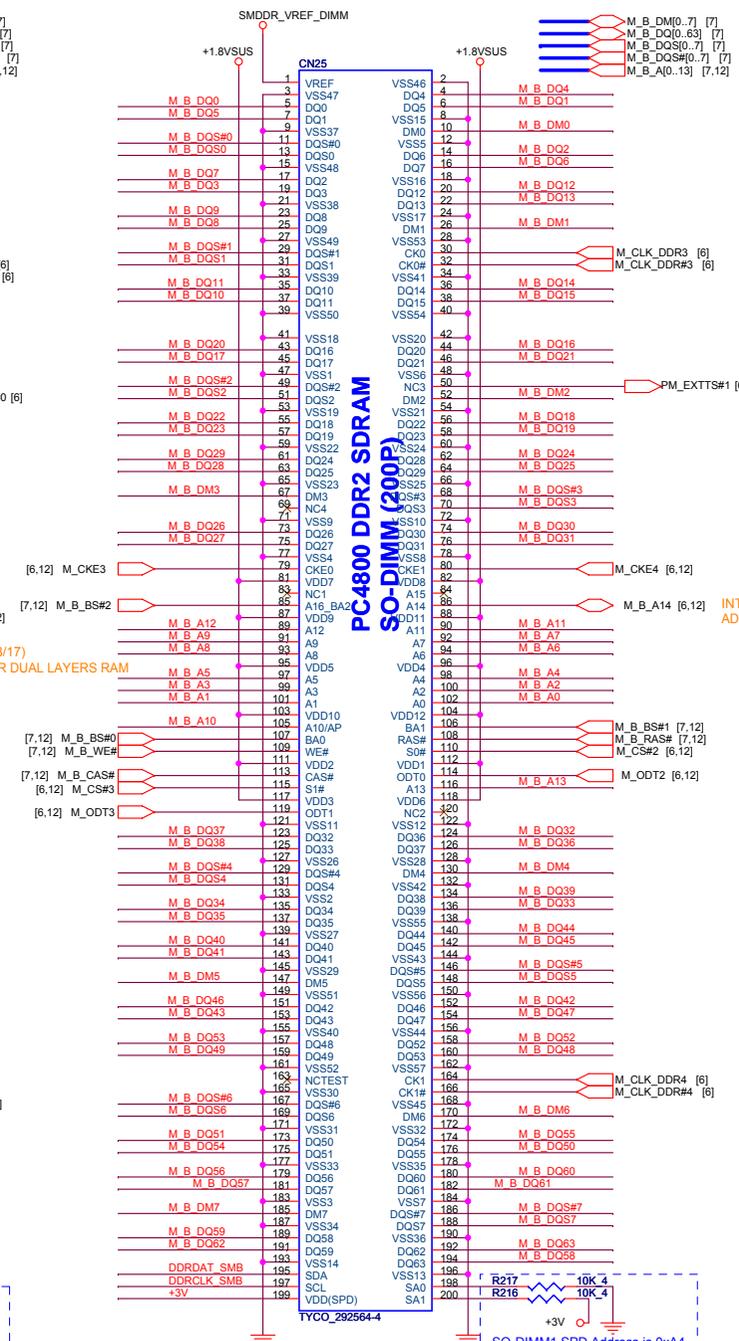
**CLOCK 0,1
CKE 0,1**

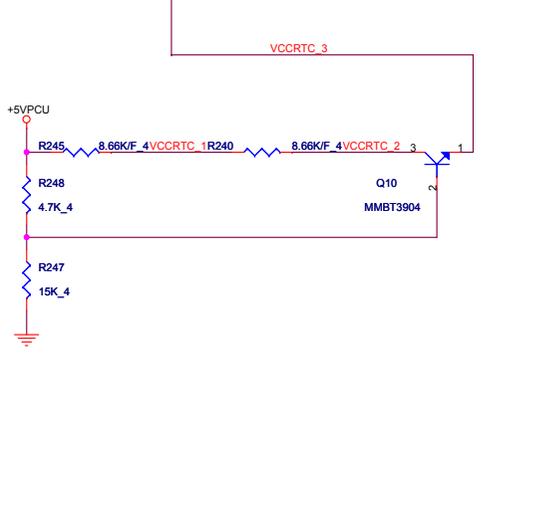
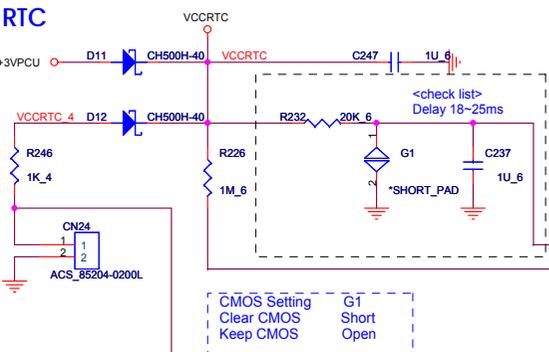
SO-DIMM0 SPD Address is 0xA0
SO-DIMM0 TS Address is 0x30

H: 10.1mm

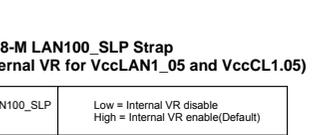
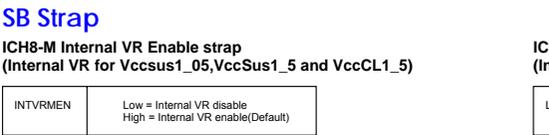
**CLOCK 3,4
CKE 2,3**

SO-DIMM1 SPD Address is 0xA4
SO-DIMM1 TS Address is 0x34



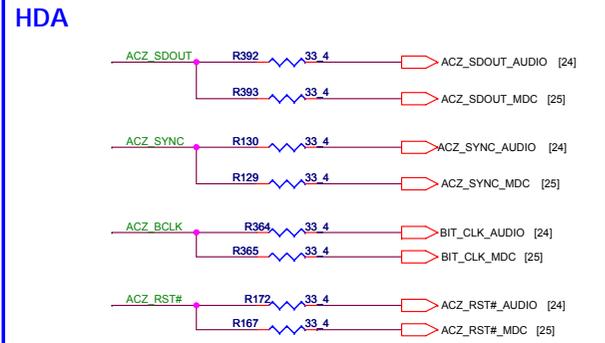
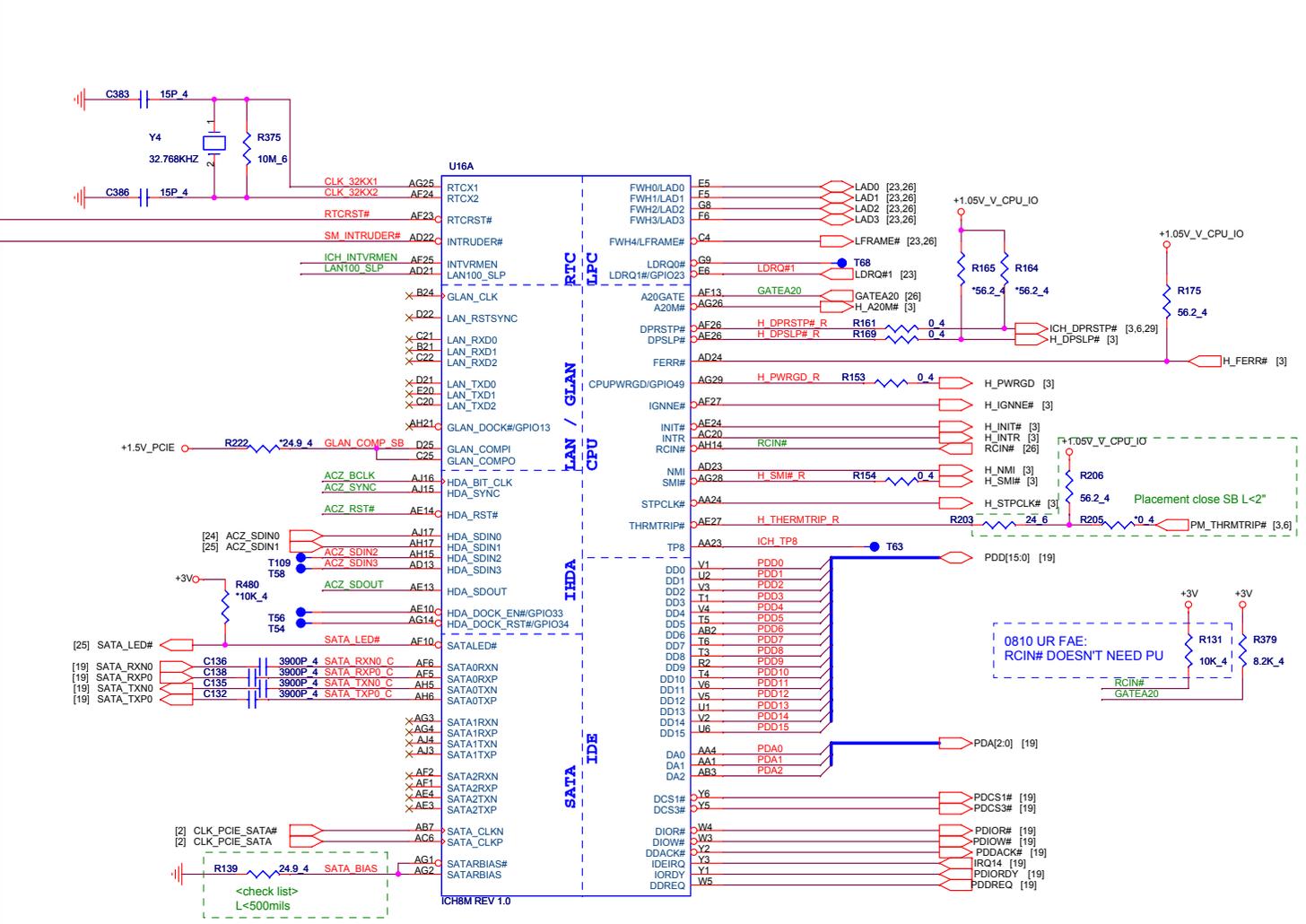
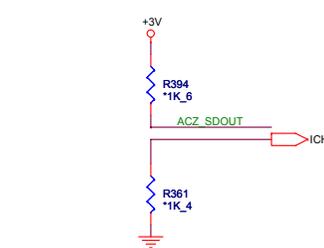


- SATA Disable**
- 1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
 - 2.NC: SATA[2:0]TXp/n , SATALED#
 - 3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
 - 4.BIOS disable



XOR Chain Entrance Strap

ICH_RSVD0	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

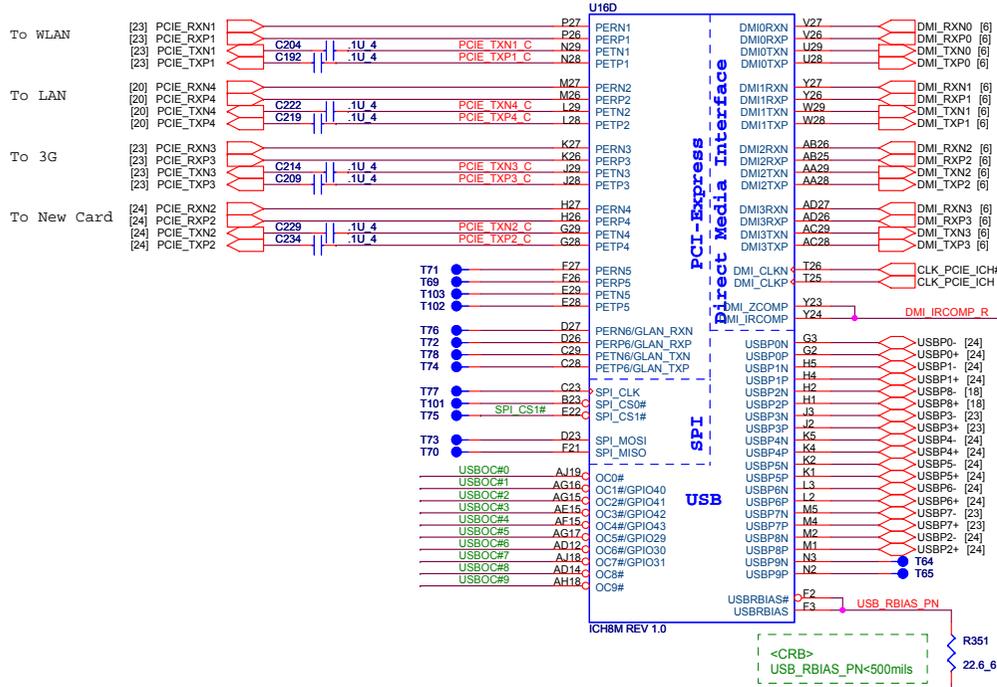


Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	2A

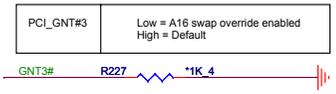
Date: Tuesday, March 27, 2007 Sheet 14 of 33

SB-PCIE/USB/DMI



- To USB BOARD(Audio)
- To USB BOARD(Audio)
- To Camera
- To WLAN
- To Finger Printer
- To Bluetooth
- To New Card
- To 3G
- To USB BOARD(LAN)

A16 SWAP Override strap

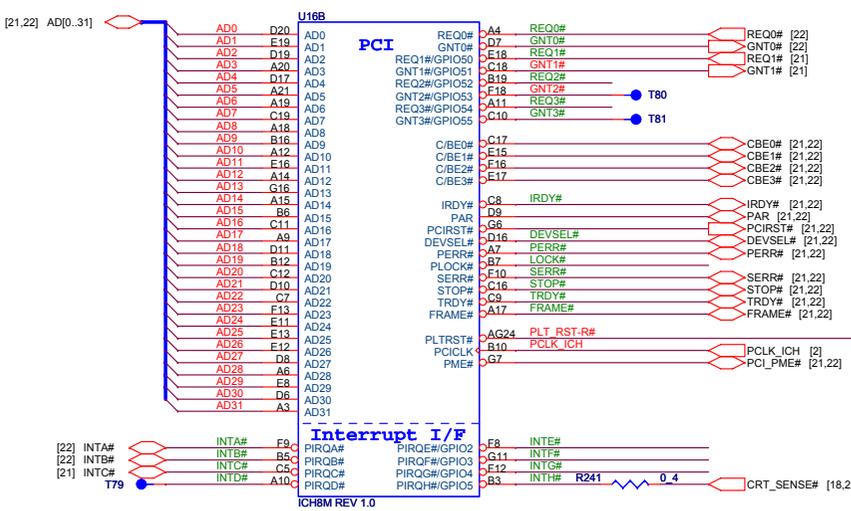


ICH8 Boot BIOS select

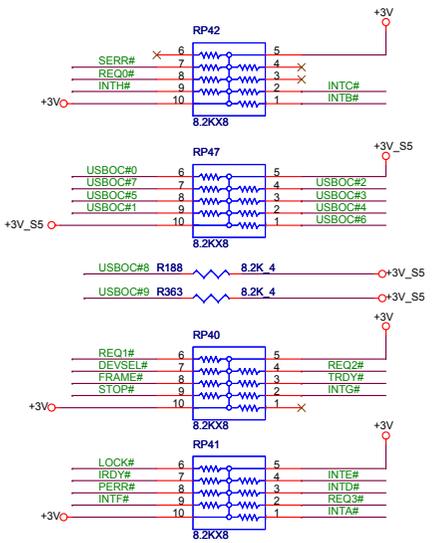
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC



SB-PCI

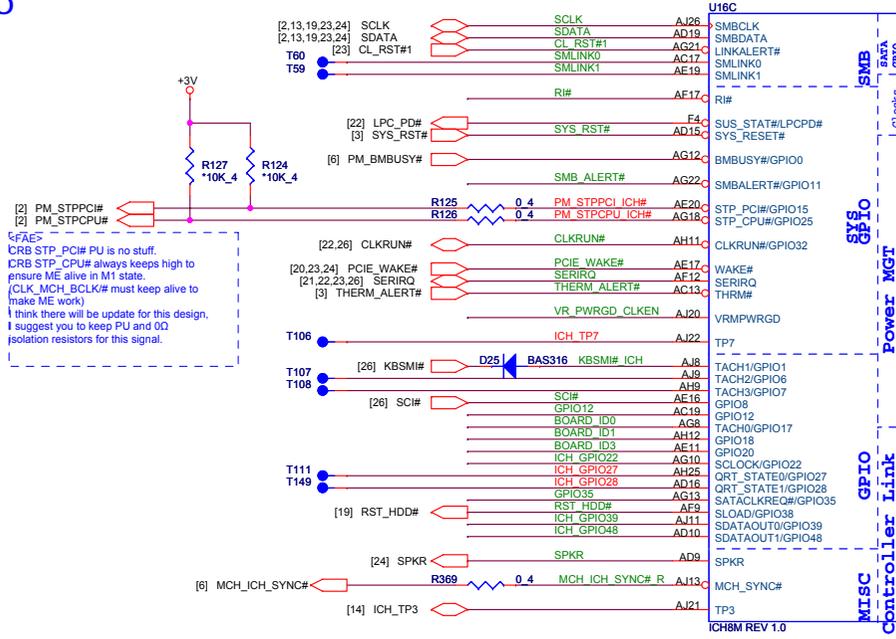


PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#, INTB#	R5C833
REQ1# / GNT1#	AD20	INTC#	CB1410



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PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	1A
Date:	Monday, March 26, 2007	Sheet 15 of 33

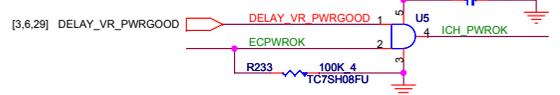
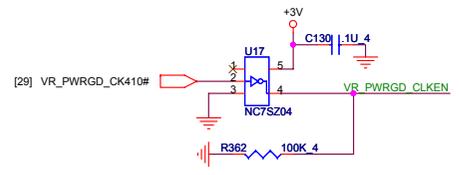


<FAE>
 CRB STP_PCH# PU is no stuff.
 CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
 [CLK_MCH_BCLK# must keep alive to make ME work]
 I think there will be updates for this design.
 I suggest you to keep PU and O3 isolation resistors for this signal.

<FAE>
 Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSPLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
 Use internal LAN MAC connect LAN_RST# to RSMRST#
 should go high no sooner than 10ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

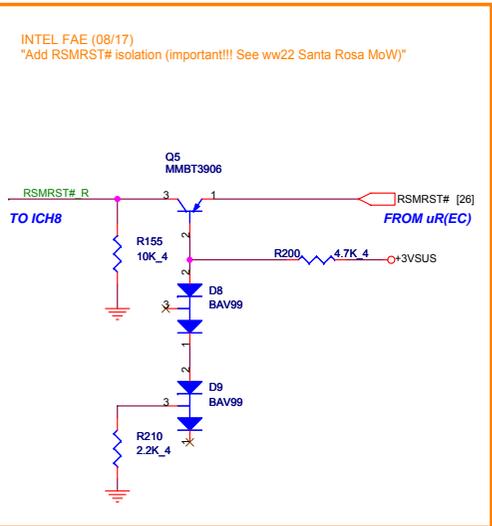
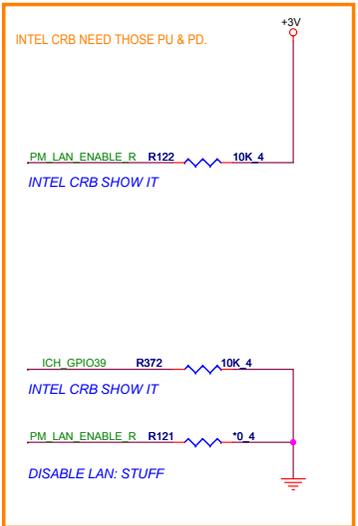
Controller Link 1 VREF for IAMT support only



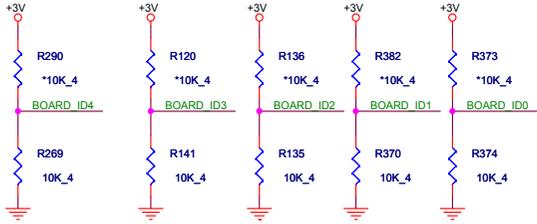
No Reboot strap

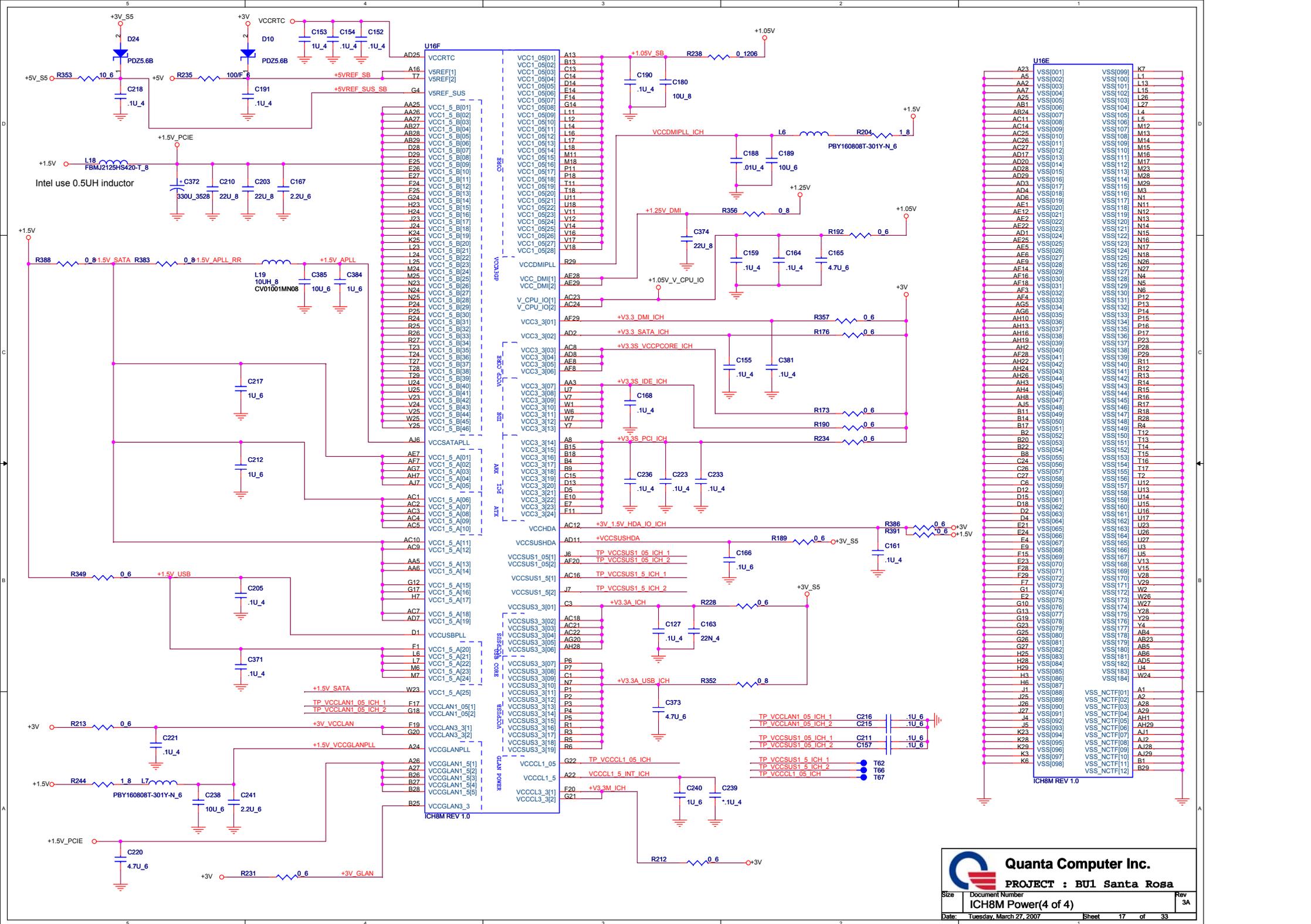
SPKR	Low = Default High = No Reboot	
BIOS/ERIC: UNSTUFF		
SPKR	R178	*10K_4
GPIO35	R380	10K_4
THERM_ALERT#	R187	8.2K_4
SERIRO	R157	10K_4
CLKRUN#	R371	8.2K_4
MCH_ICH_SYNC#_R	R381	*10K_4
CL_RST#1	R151	10K_4
KBSM#_ICH	R390	10K_4
SCI#	R366	10K_4
ICH_GPIO22	R134	10K_4
ICH_GPIO48	R138	10K_4
RST_HDD#	R137	10K_4
GPIO36	R133	8.2K_4
GPIO37	R132	8.2K_4

SMLINK0	R185	10K_4
SMLINK1	R184	10K_4
SYS_RST#	R179	10K_4
DNBSWON#	R239	*10K_4
ICH_GPIO24	R358	*10K_4
HDPACT	R140	*10K_4
R#	R145	10K_4
Internal Pull up		
SCLK	R359	2.2K_4
SDATA	R128	2.2K_4
SMB_ALERT#	R360	10K_4
PCIE_WAKE#	R146	1K_4
PM_BATLOW#_R	R158	8.2K_4
GPIO12	R183	10K_4

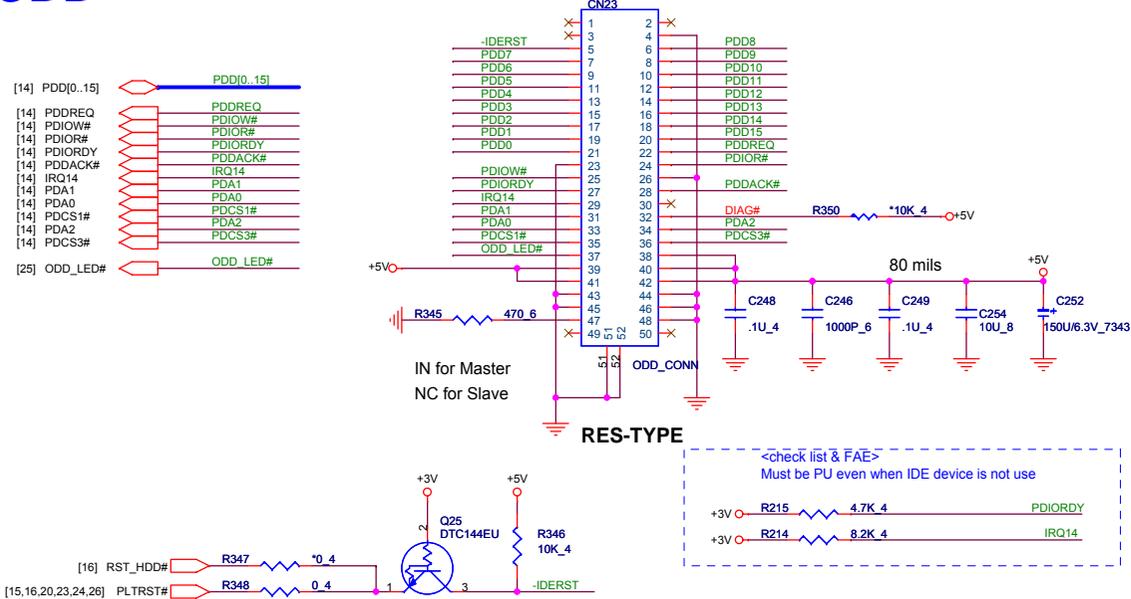


Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD	0	0	0	0	1
CARD BUS	0	0	0	1	0
G-SENSOR	0	0	1	0	0
CCD	0	1	0	0	0
ROBSON	1	0	0	0	0

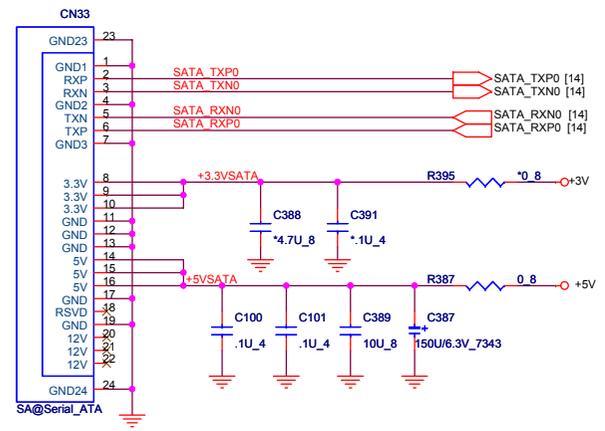




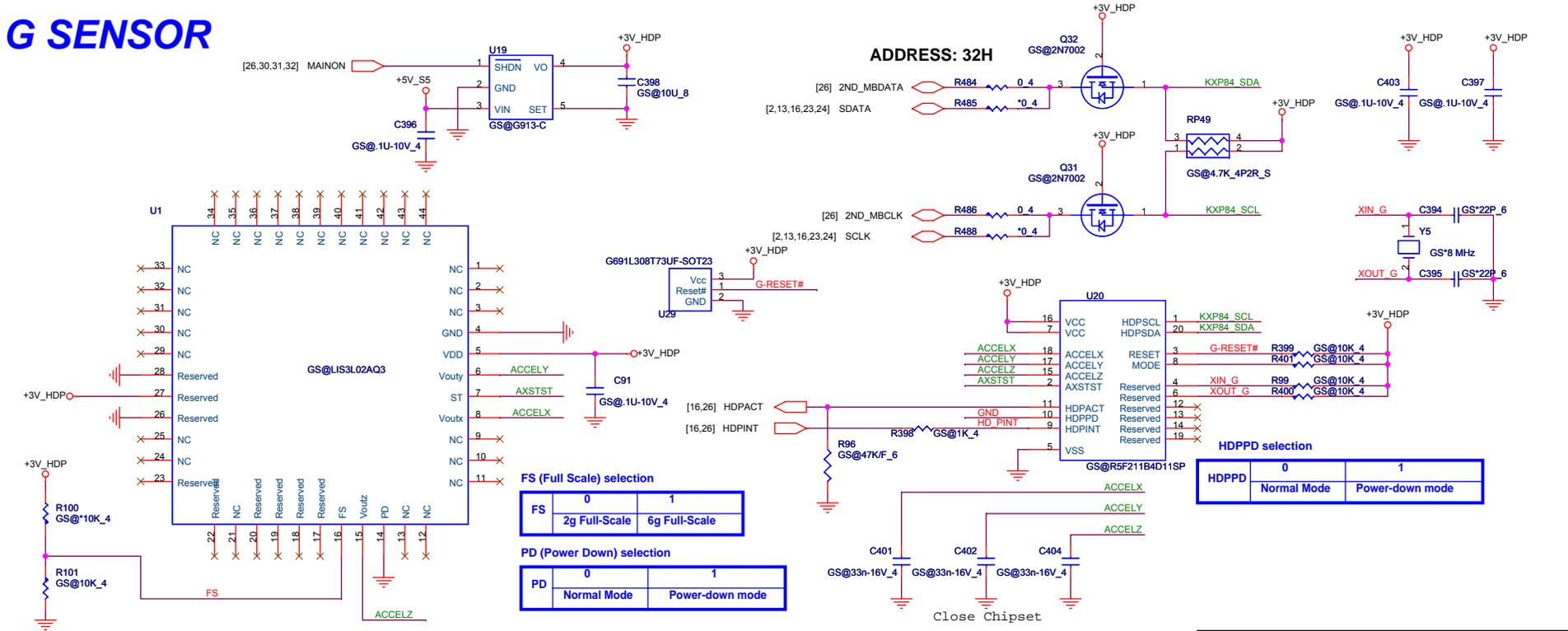
ODD



SATA HDD



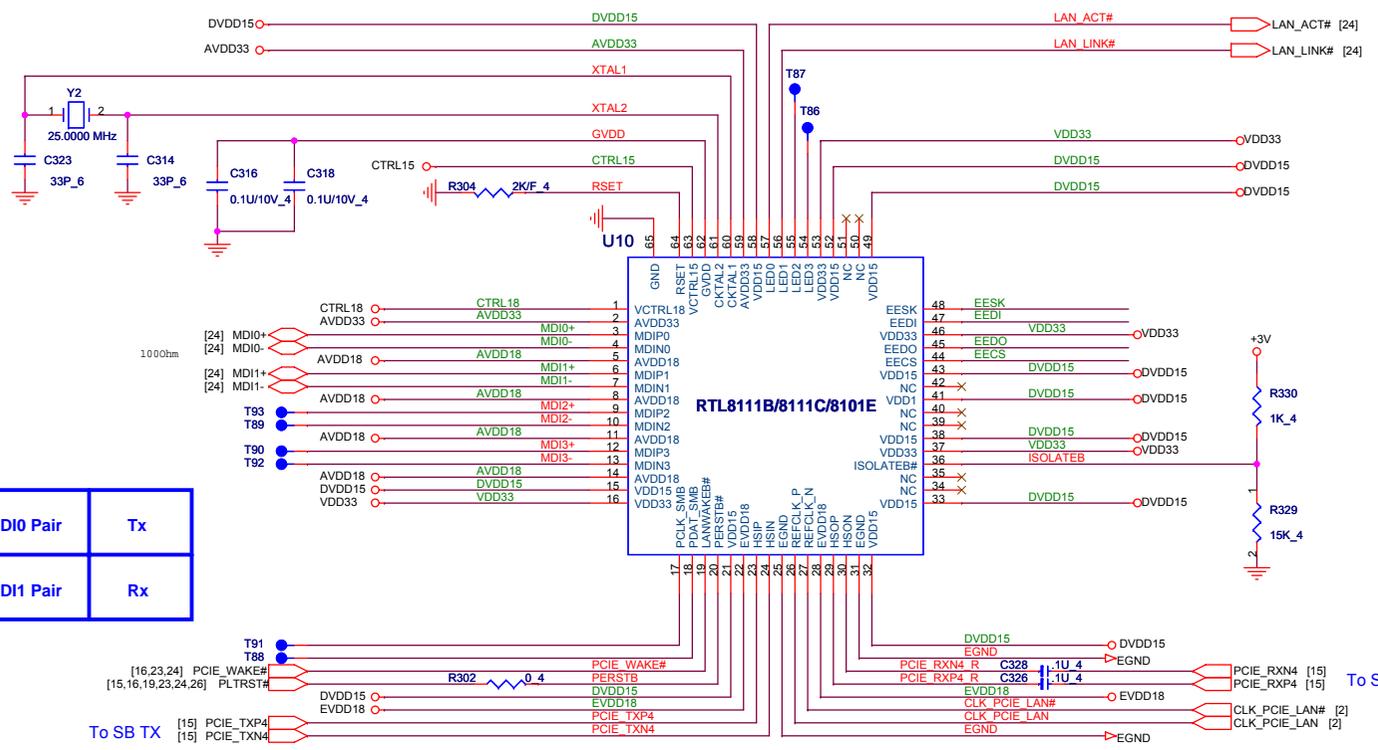
G SENSOR



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PROJECT : BU1 Santa Rosa

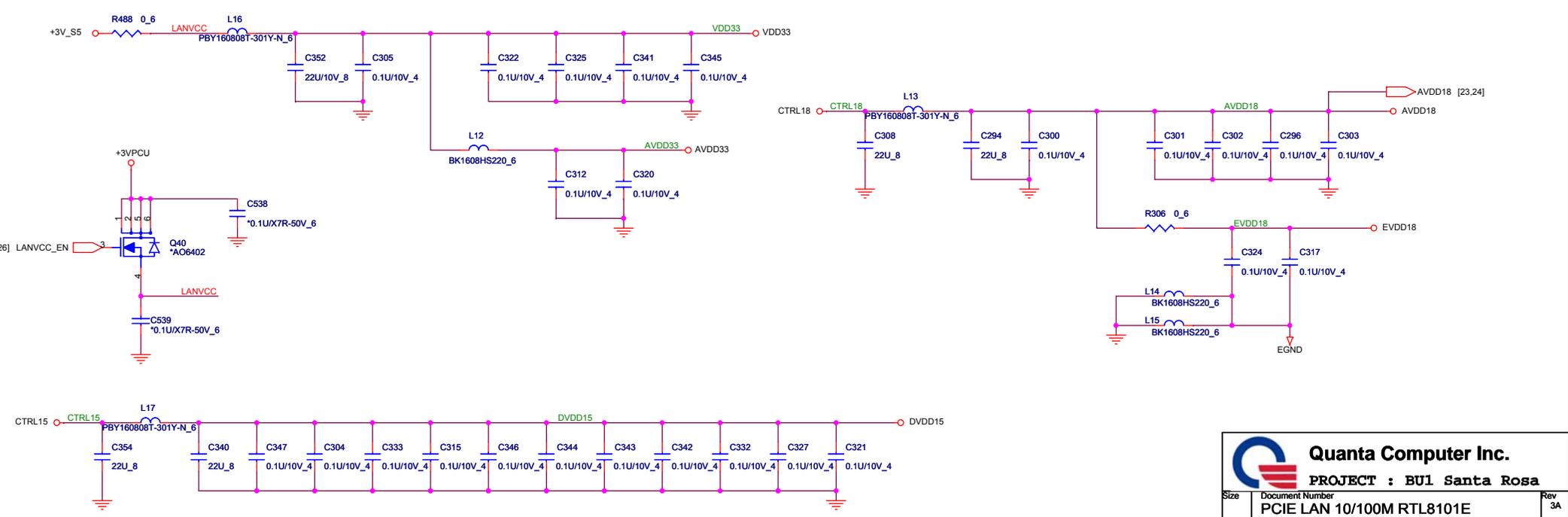
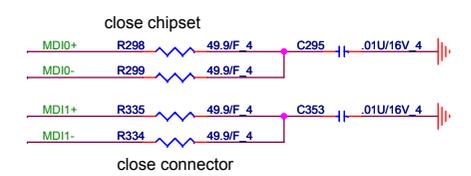
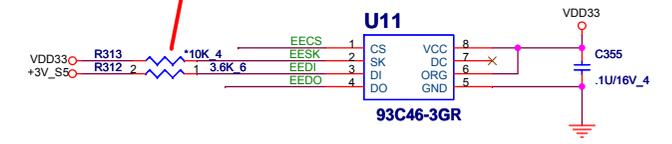
Size Document Number
PATA/ODD/G SENSOR Rev 2A

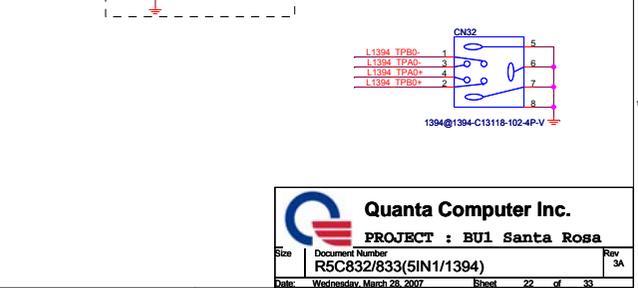
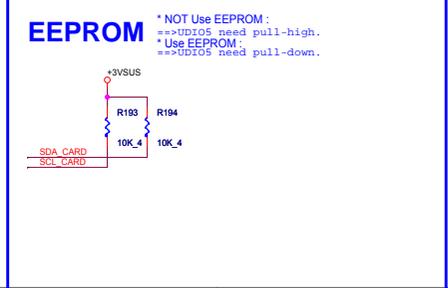
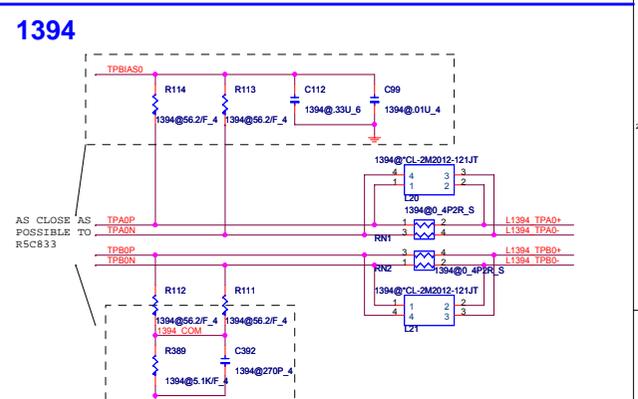
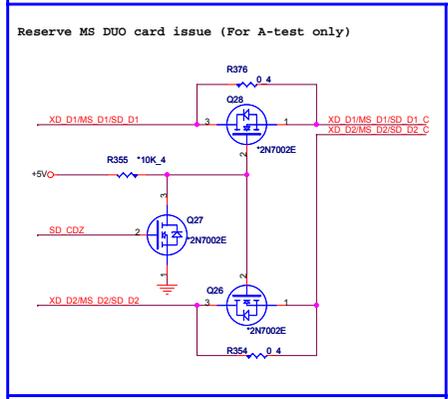
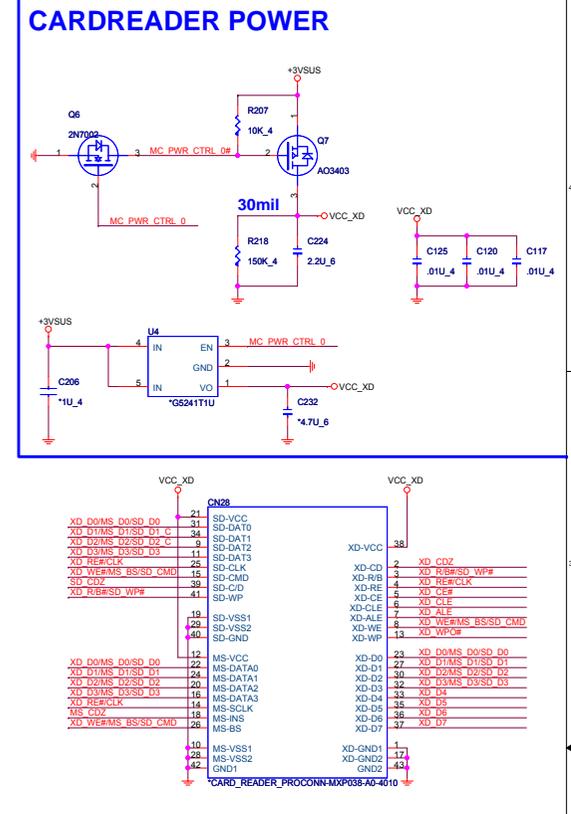
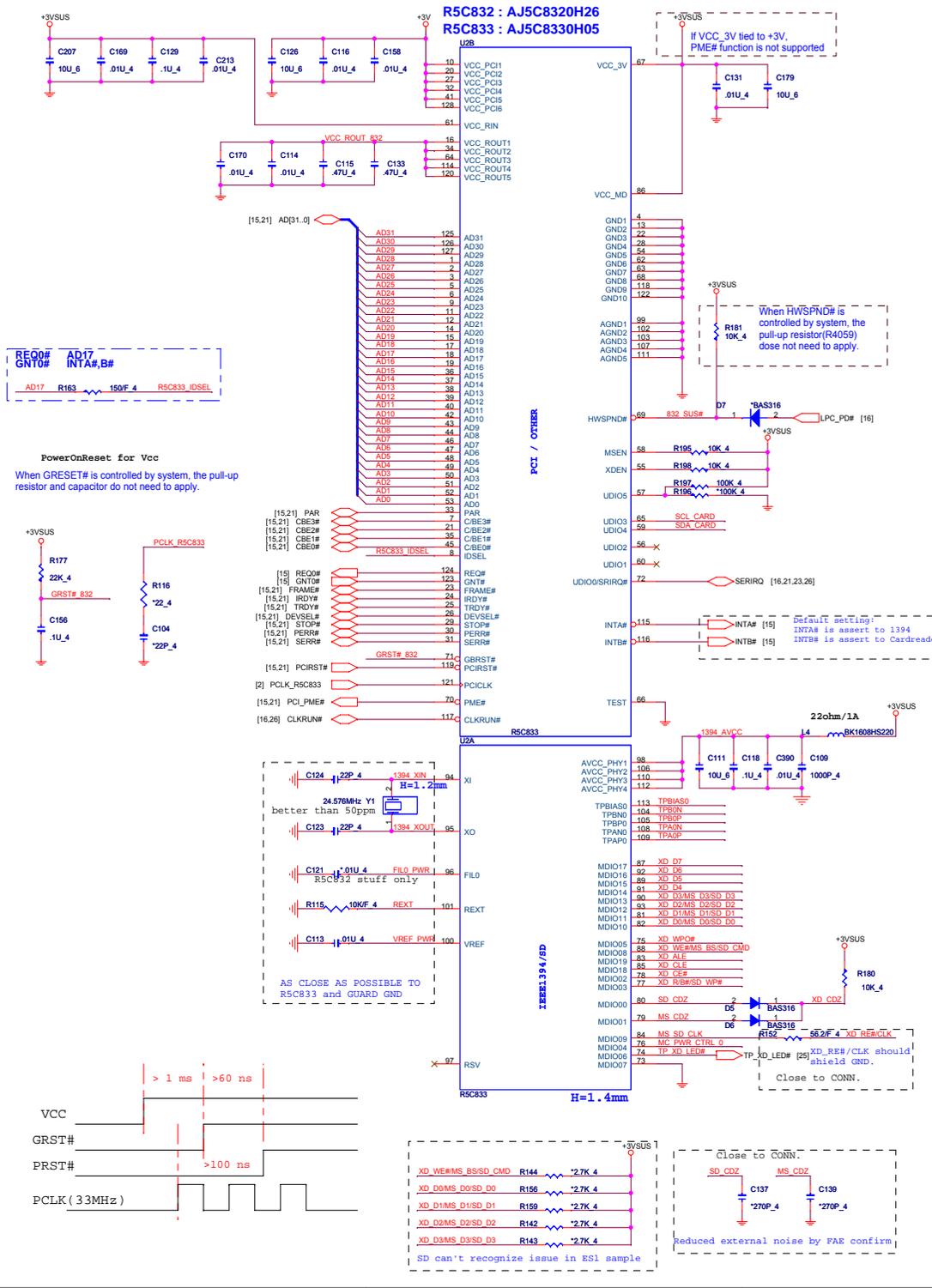
Date: Monday, March 26, 2007 Sheet 19 of 33



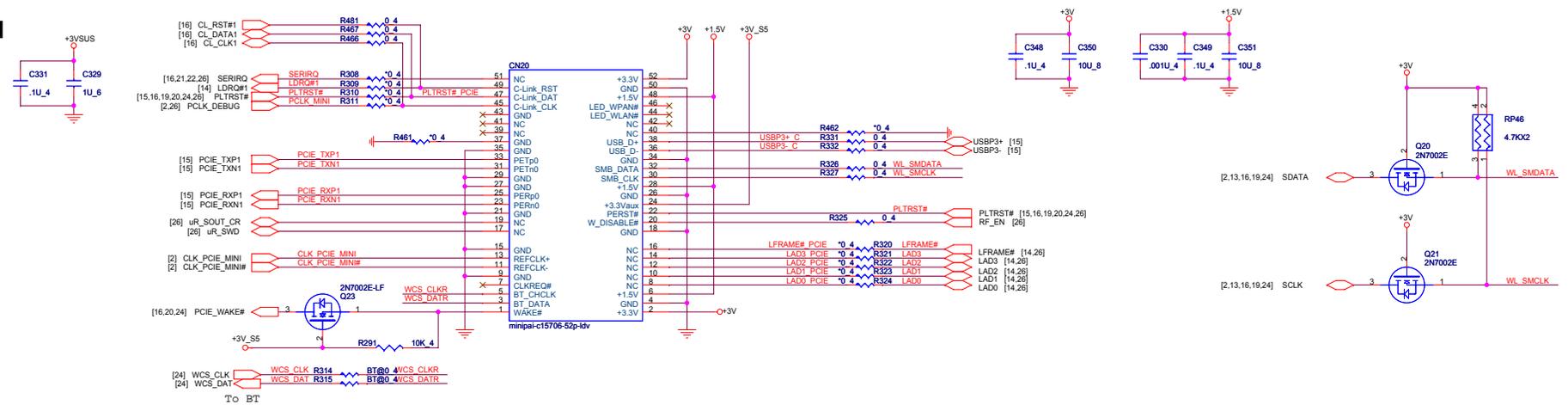
MDIO Pair	Tx
MDI1 Pair	Rx

93C56: STUFF
93C46: NOSTUFF

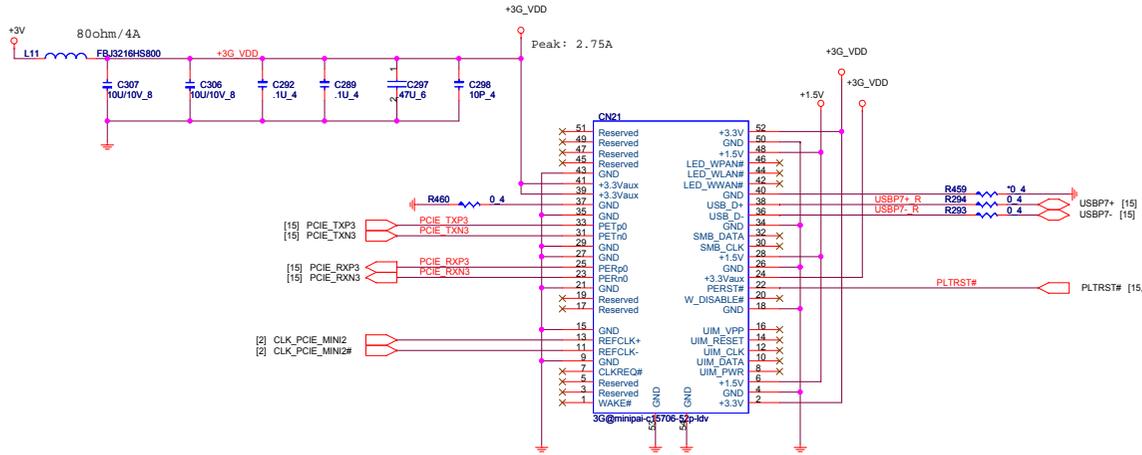




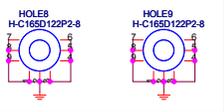
Mini PCI-E Card WLAN



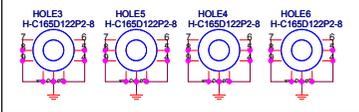
MINI-Card



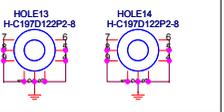
NB SINK



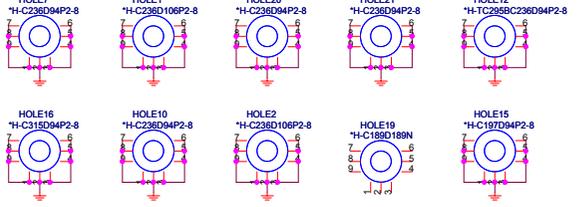
CPU SINK



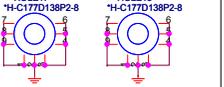
MINI CARD SINK



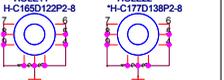
MB SINK



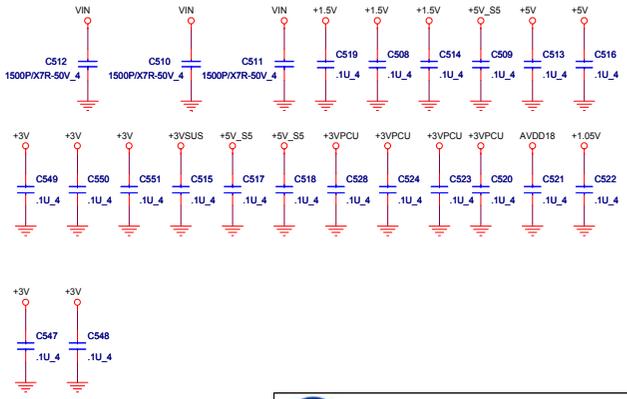
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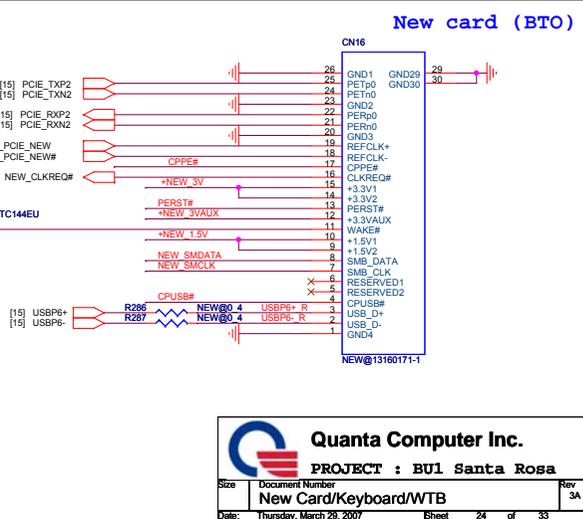
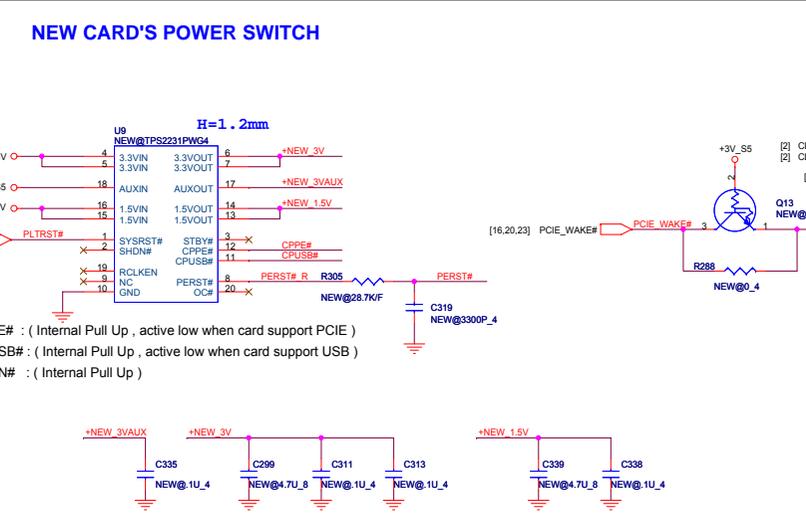
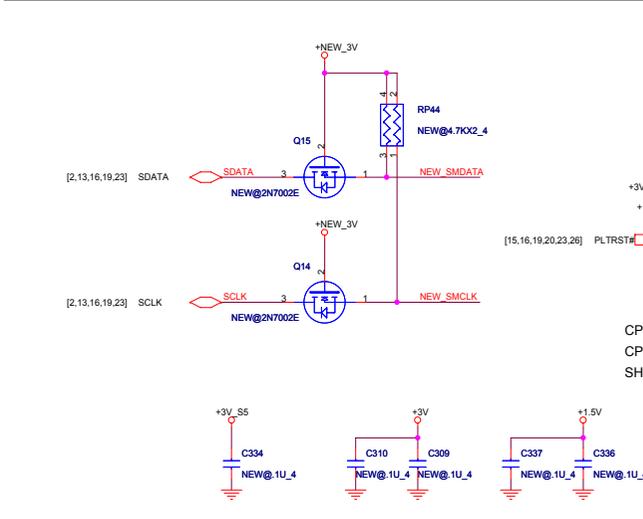
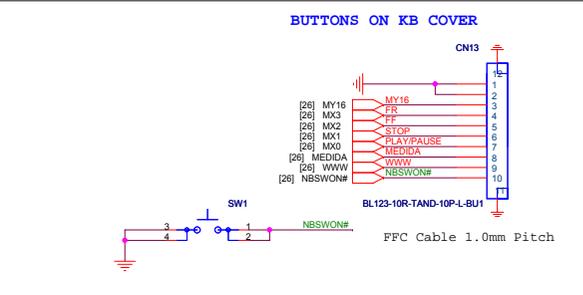
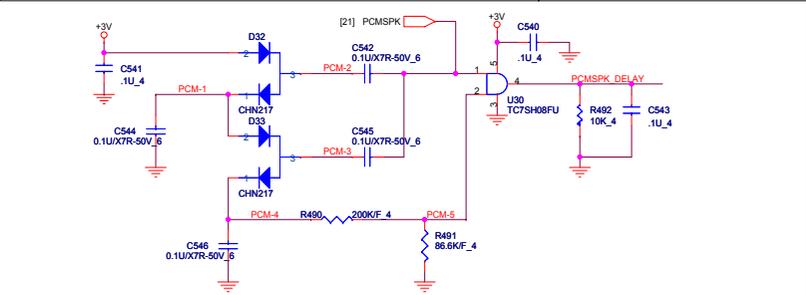
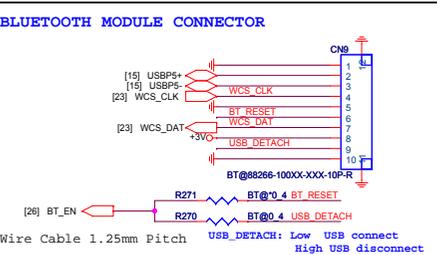
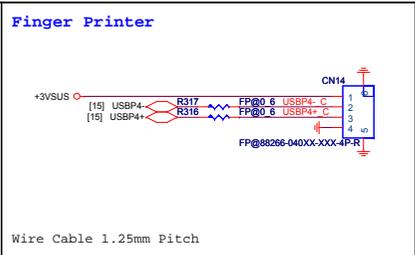
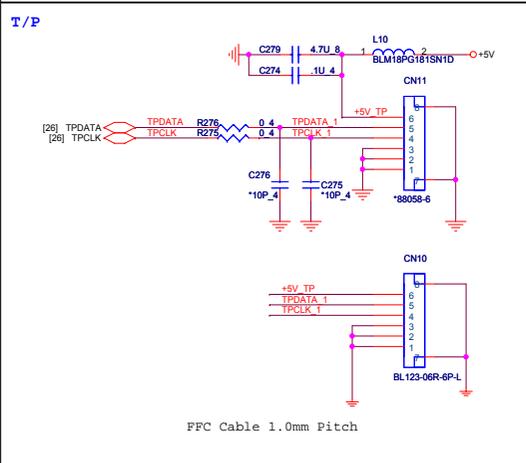
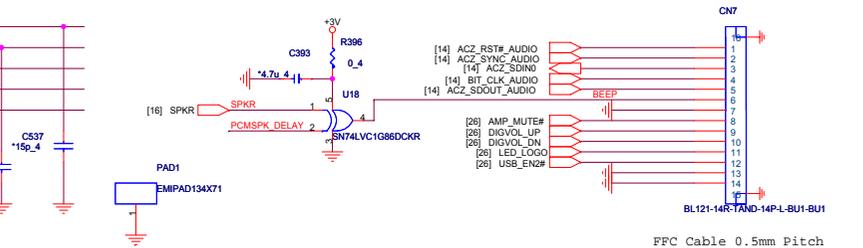
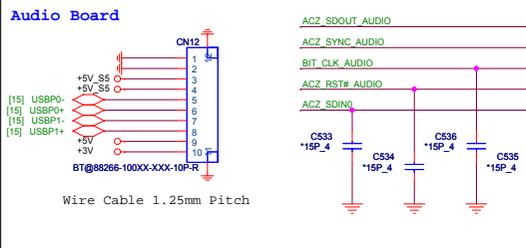
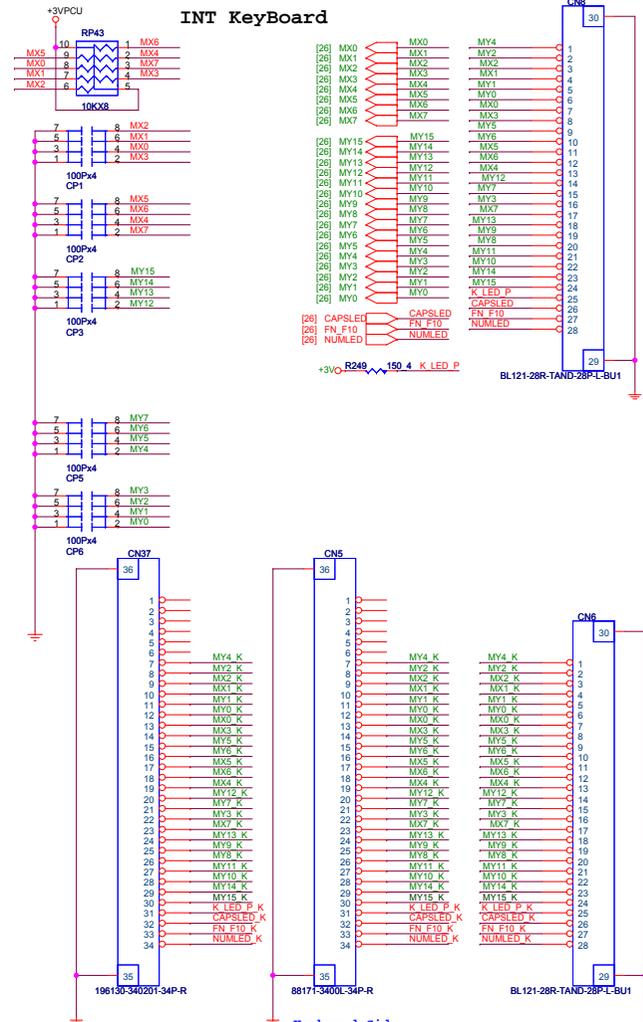


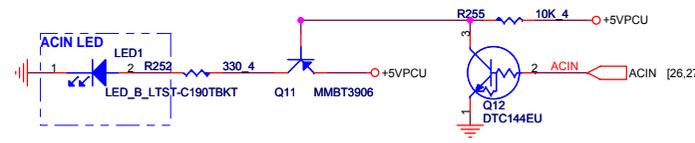
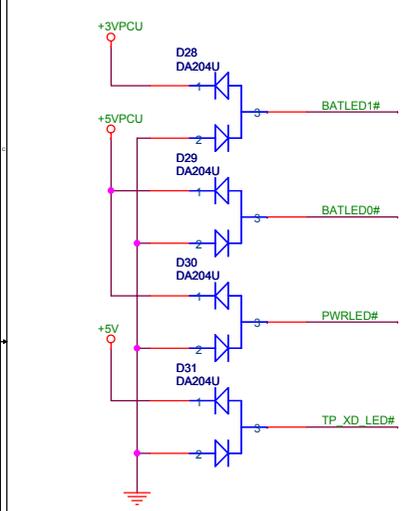
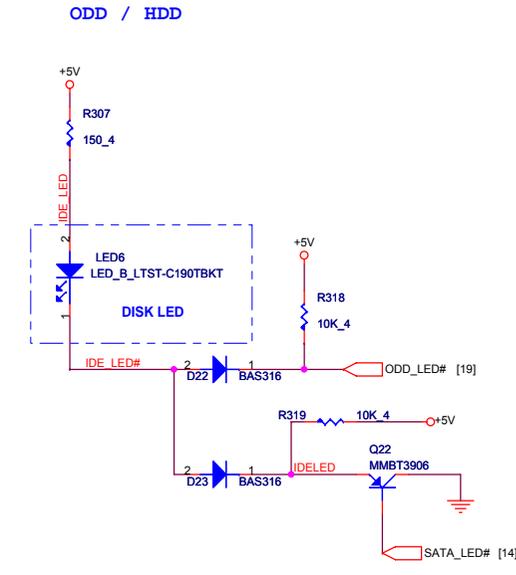
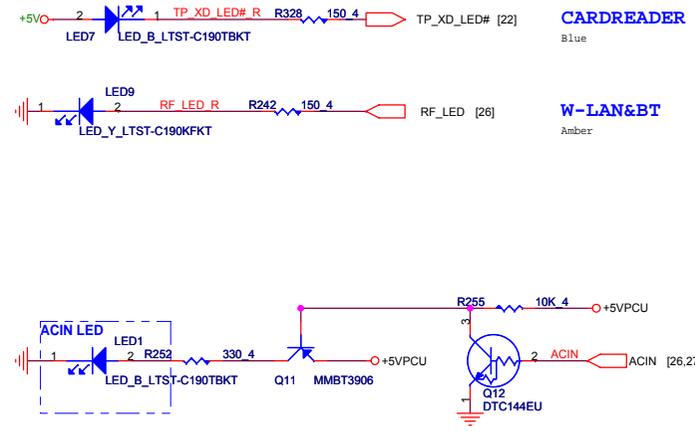
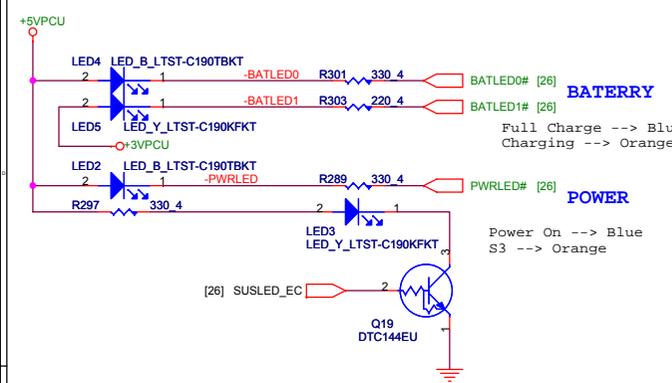
MDC PCMCIA SINK



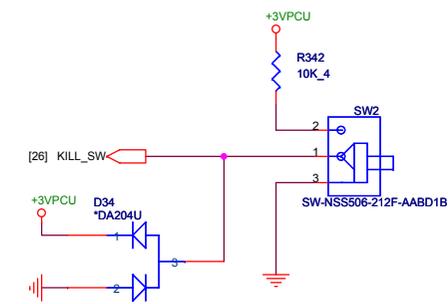
EMI



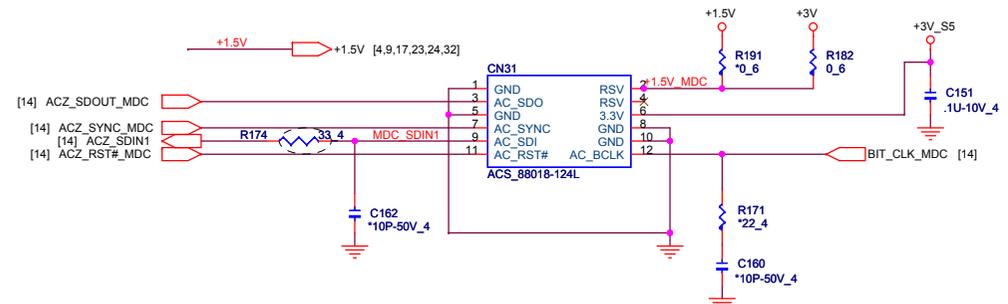




W_LAN&BT / 3G DC-IN / Power / Battery /HDD(ODD) / Bridge Media access
 (Amber) (Blue) (Blue)(Blue) (Blue) (Blue) (Blue) (Blue)
 (Amber) (Amber)

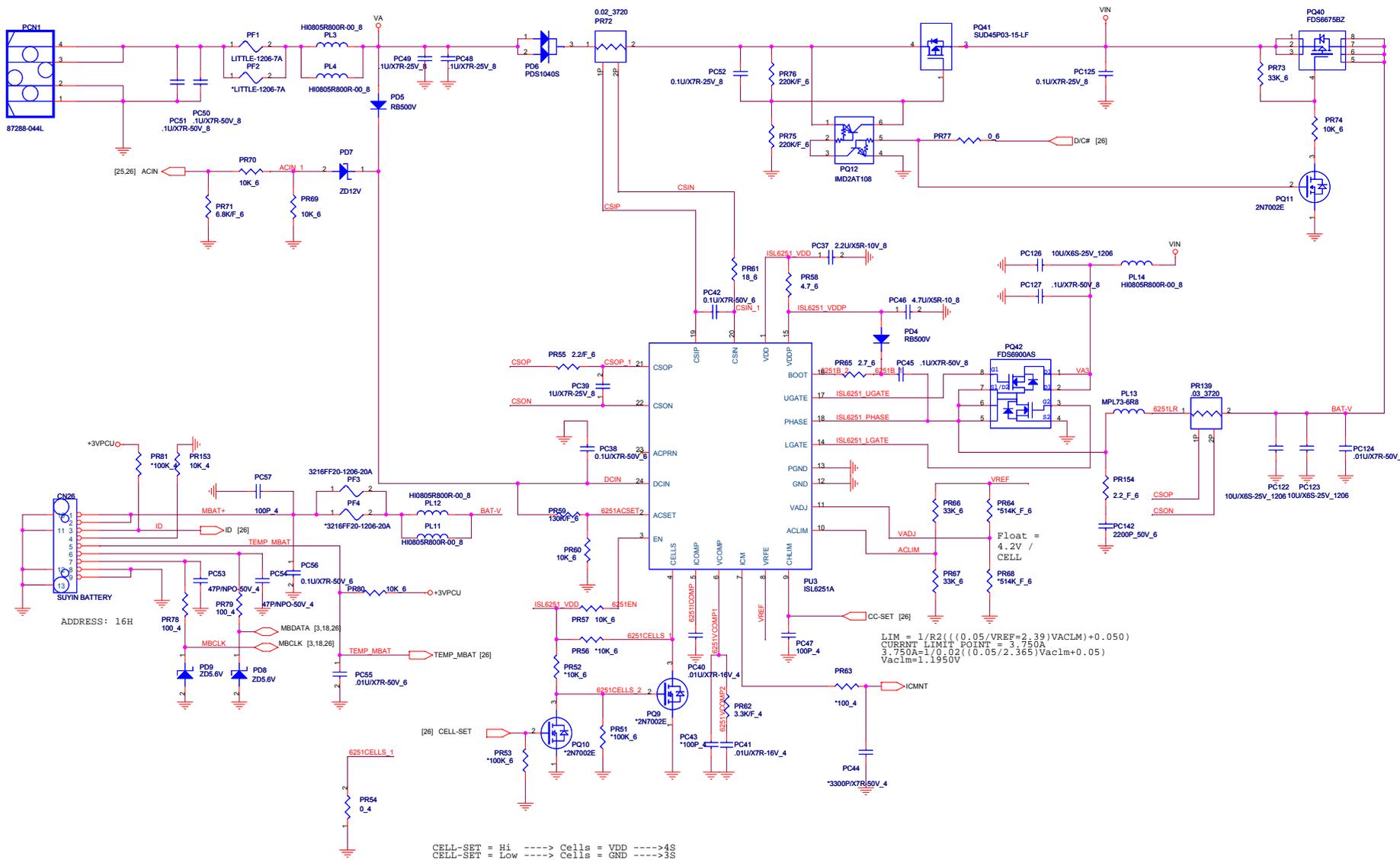


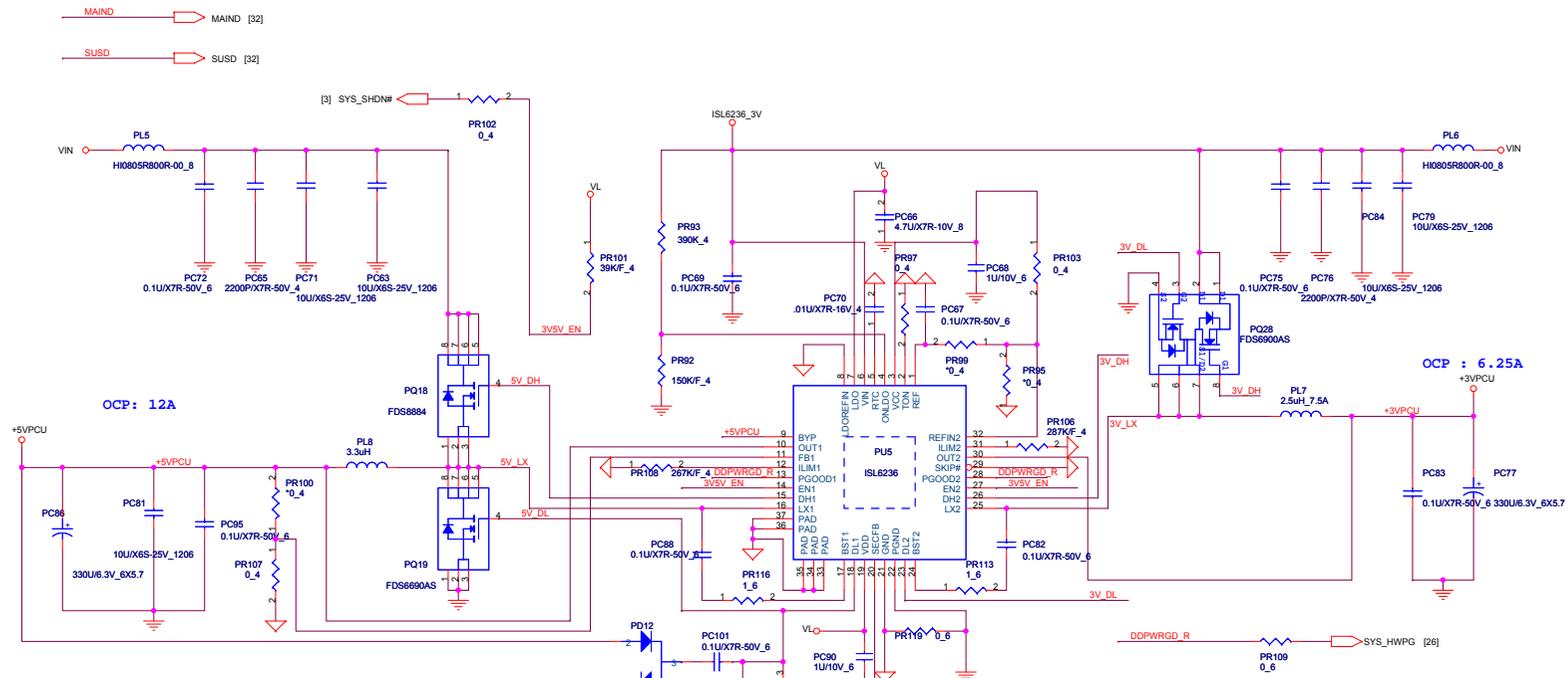
MDC



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	TP/SW/LED	3A
Date:	Sunday, April 01, 2007	Sheet 25 of 33

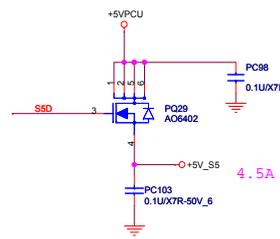




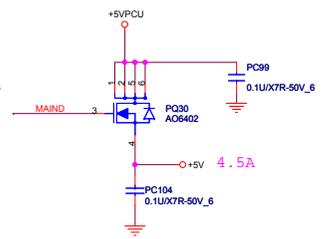
OCP: 12A

OCP:12A
 $L(\text{ripple current}) = (19-5) * 5 / (1.5u * 0.4M * 19) \sim 6A$
 $I_{ocp} = 12 - (6/2) = 9A$
 $V_{th} = 9A * 15m\Omega = 135mV$
 $R(I_{lim}) = (135mV * 10) / 5uA \sim 270K$

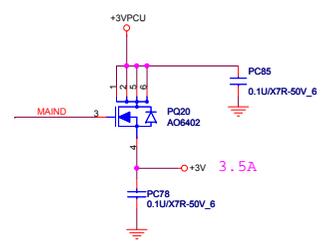
OCP: 6.25A
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (2.5u * 0.5M * 19) \sim 2.18A$
 $I_{ocp} = 6.25 - (2.18/2) = 5.16A$
 $V_{th} = 5.16A * 28m\Omega = 145mV$
 $R(I_{lim}) = (145mV * 10) / 5uA \sim 294K$



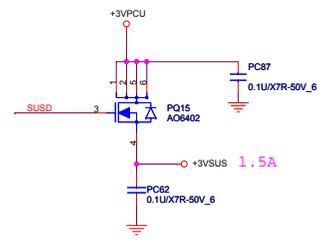
4.5A



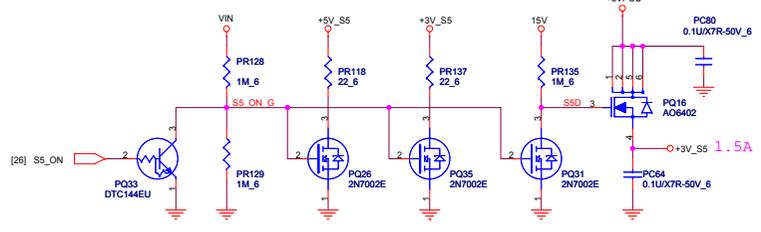
4.5A



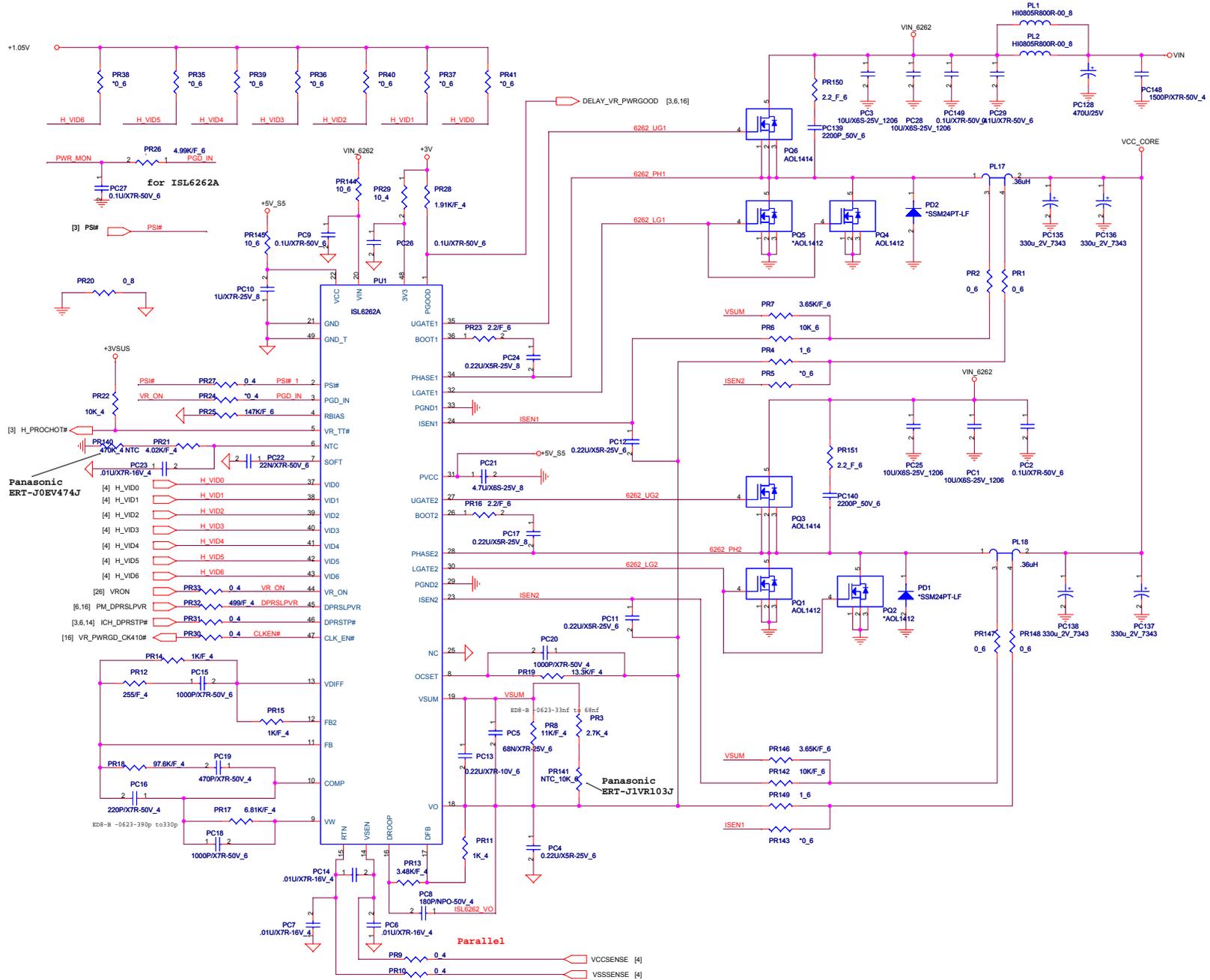
3.5A



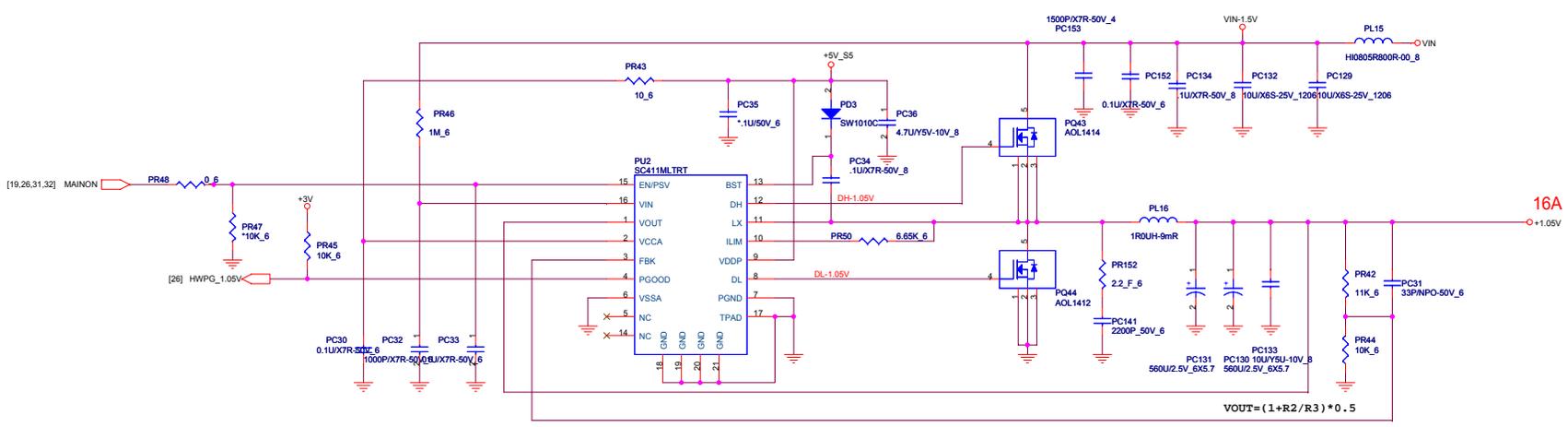
1.5A

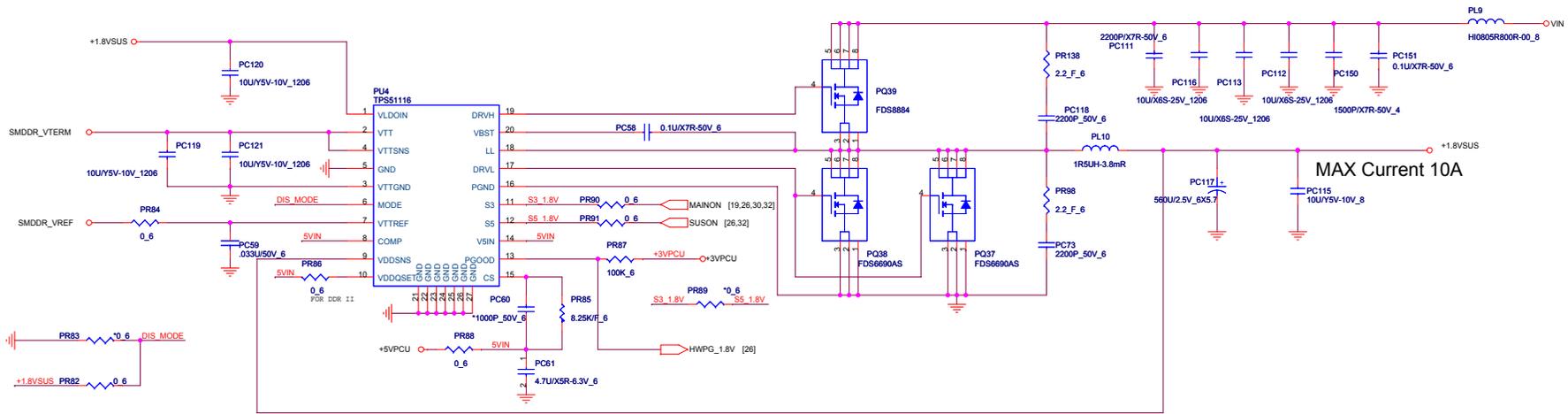


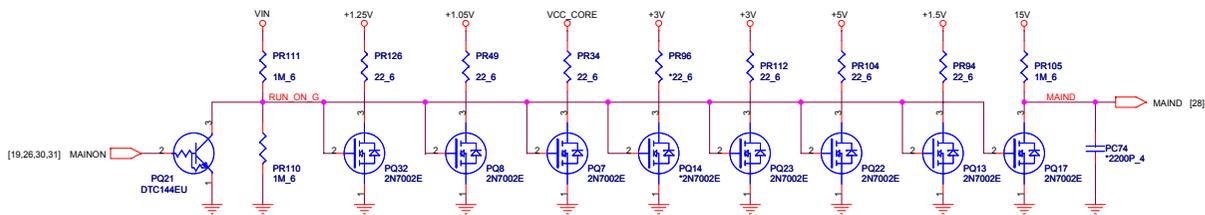
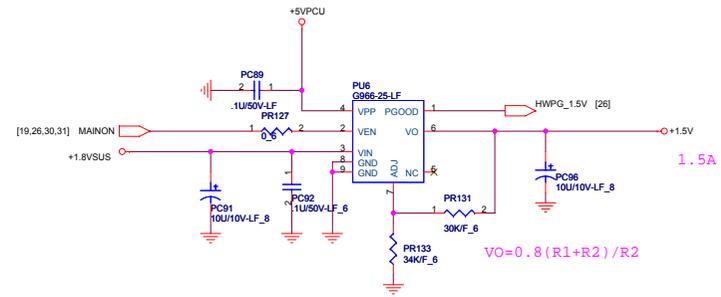
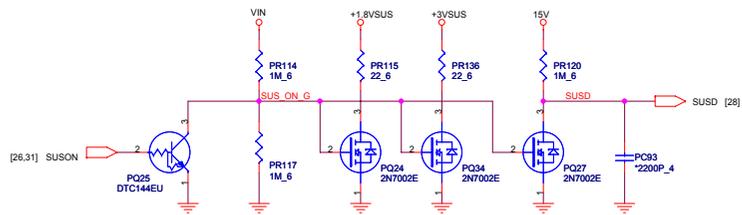
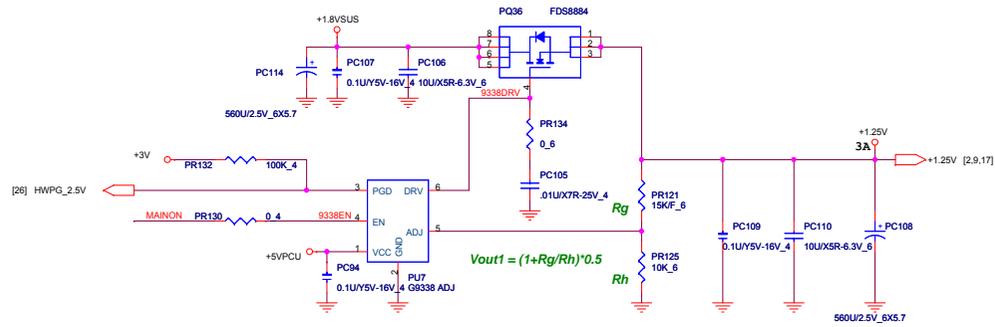
1.5A



Merom: VCC_CORE/ 44A







Model	REV	DATE	CHANGE LIST	NOTE
BU1	00	20061218	FIRST RELEASED : 20061218	
	01	20061225	Page02: Change CLK GEN. low power outs from +1.05V to +1.25V.Because VDD_IO will drop out when high loading	Circuit modify
			Page02: REV_01 Remove CLK_MCH_OE#_R had pull up resistor,because had be pull up at NB side	Circuit modify
			Page03: Del R382,R383,Q60,D39	Circuit modify
			Page04: Del R176 for FBS signals batter return path under +1.05V plane	Circuit modify
			Page08: Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW. reserved 0 ohm resister	Circuit modify
			Page16: Add D43 to avoid leakage from EC to SB,Del R242	Circuit modify
			Page18: REV_01 Reserved LCD/LED type panel module and Digital/analogy MIC	Circuit modify
			Page19: Modify G-Sensor circuit	Circuit modify
			Page22: Reserved LPC_PD# control signal from SB to R5C833	Circuit modify
			Page23: Increase HOLE	Circuit modify
			Page24: Add 0.1u CAP. C810 from +5VPCU to GND	Circuit modify
			Page25: Modify IDE LED circuit	Circuit modify
Page26: Reserved R756,R766 for EC control G-Sensor	Circuit modify			
Page27: Add 3 cell Battery always setting circuit	Circuit modify			
Page28: Add +3V_S5 discharge circuit	Circuit modify			
Page30: Reserved PD resistor to avoid leakage voltage	Circuit modify			
Page32: Reserve +3V discharge circuit	Circuit modify			
1A	20061227	A TEST (PCB REV_1A) RELEASED : 20061227		
2A	20070201	Page03: Modify thermal protect circuit and FAN control	Circuit modify	
		Page14: Modify RTC charge current / SB strip setting / Reserved PU resistor on SATALED# signal / Change XTAL capacitor value	BOM/Circuit modify	
		Page16: Reserver Pull down resistor on HDPINT signal / Reserved C-Link to WLAN / Delete FM function / Add Board ID	Circuit modify	
		Page18: Change panel backlight signal pull up resistor / Change camera power source / Add LED type panel circuit / Add fuse on CRT power / Reserved EMI choke on USB signals and add EMI solution / Add RC circuit on LED panel driver IC	BOM/Circuit modify	
		Page19: Modify LDO power source / Add Microprocessor reset IC / Reserved G-sensor SMBUS to SB chipset	Circuit modify	
		Page22: Reserved Cardreader external EEPROM	Circuit modify	
		Page23: Separate RF enable/disable pin from WLAN and 3G card / Add EMI solution and Reserved C-Link circuit / Delete 3G card function / Add HOLE for card Bus connector	Circuit modify	
		Page24: Increase CN7 pin for control illumination logo and enable/disable USB port power / Add capacitor on keyboard signals for EMI / Change LAN/B cable connector / Delete FM function	Circuit modify	
		Page25: Modify battery LED and RF SW power source / Delete 3G card LED	Circuit modify	
		Page26: Modify EC control circuit / Add EMI solution / Change XTAL capacitor value	BOM/Circuit modify	
		Page27: Change fuse rating and switch MOS	Circuit modify	
		Page29: Add EMI solution	Circuit modify	
Page30: Add EMI solution	Circuit modify			
Page31: Add EMI solution	Circuit modify			
Page32: Add EMI solution	Circuit modify			
3A	20070326	Page03: Add CAP to GND for FAN controller IC U12 power pin decoupling	Circuit modify	
		Page13: Change DDR socket height	Circuit modify	
		Page18: Exchange Dioid and Fuse placement	Circuit modify	
		Page20: Add control LAN power circuit to enable/disable LAN	Circuit modify	
		Page22: Change 1394 connector type and delete card reader connector 2nd source	Circuit modify	
		Page23: Change mini-card 3V power source from +3VSUS to +3V_S5 for support wake on WLAN from S3/S4 / Change HOLE pad size	Circuit modify	
	20070327	Page24: Reserve EMI capacitor / add solve insert PCMCIA Card speaker has bo sound circuit	Circuit modify	
		Page25: Add ESD protect circuit	Circuit modify	
		Page27: Change MOS footprint	Circuit modify	
		Page14: Modify RTC short pad footprint	Circuit modify	
		Page17: Modify inductance type	Circuit modify	
		Page23: Add capacitors for EMI	Circuit modify	
20070328	Page24: Modify FFC connector footprint	Circuit modify		
	Page26: Add capacitor for EMI	Circuit modify		
20070329	Page27: Reserve EMI circuit	Circuit modify		
	Page22: Delete card reader external EEPROM	Circuit modify		
	Page23: Add pull up resistor on PCIE_WAKE# signal	Circuit modify		
	Page18: Delete CMO LED type connector	Circuit modify		
20070329	Page25: Reserve ESD protect on kill-switch	Circuit modify		
	Page31: Stuff R/C Snubber for EMI	BOM modify		

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