

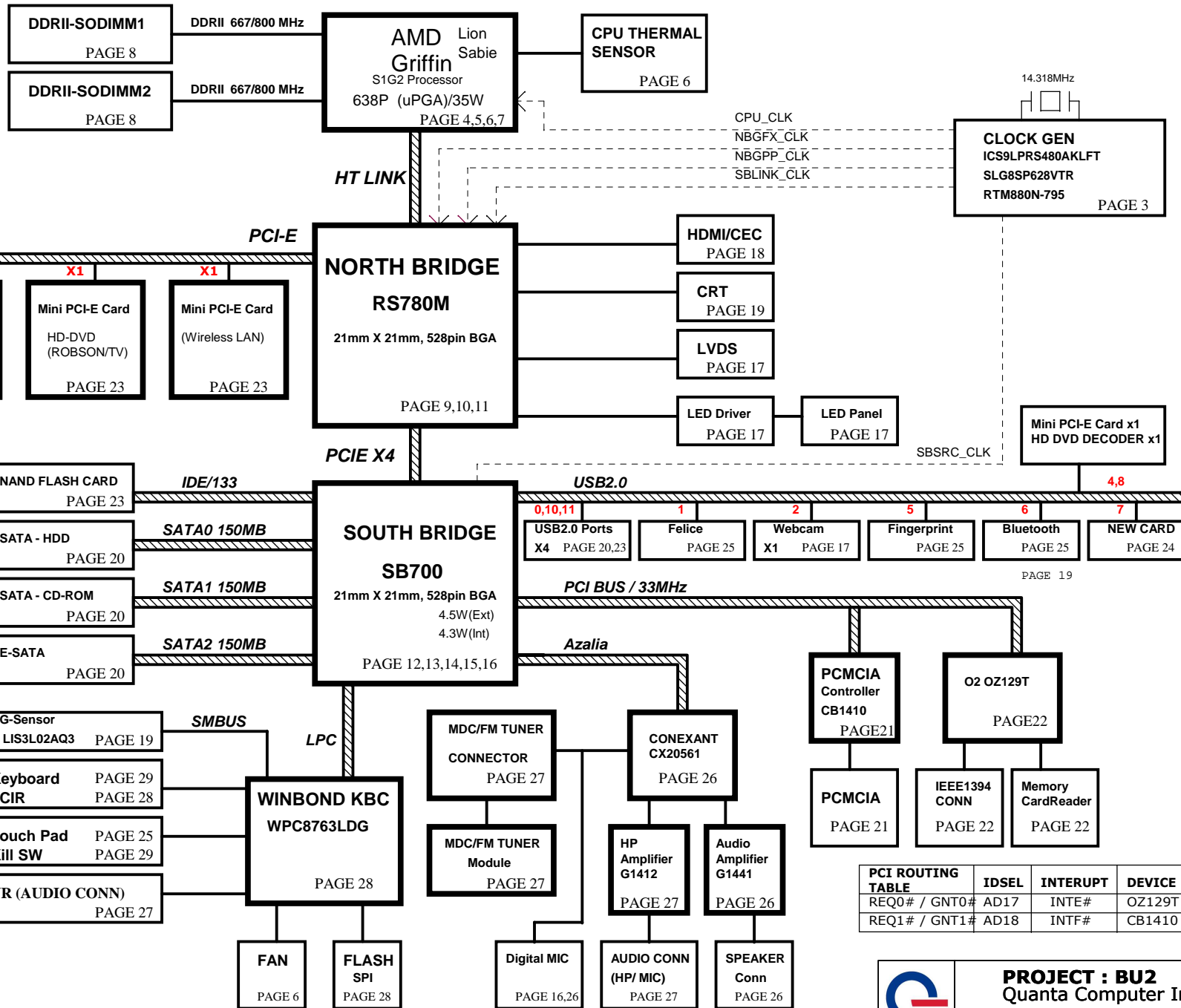
# BU2 SYSTEM DIAGRAM



01

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



- SYSTEM CHARGER (ISL88731) PAGE 30
- SYSTEM POWER ISL6237IRZA-T PAGE 31
- CPU CORE ISL6265A PAGE 32
- VCCP +1.1V AND +1.2V (MAX8717) PAGE 33
- DDR II SMDR\_VTERM 1.8V/1.8VSUS (TPS51116REGR) PAGE 34
- DISCHARGE 1.5/1.25/1.2/1.1V PAGE 35

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410

**PROJECT : BU2**  
Quanta Computer Inc.

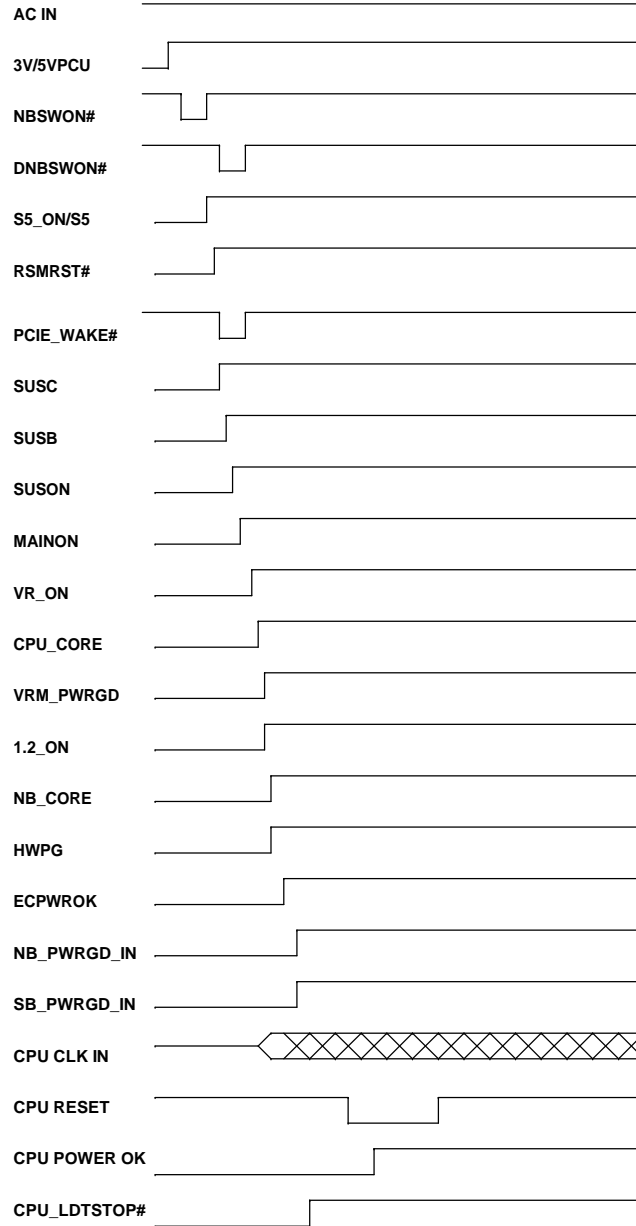
Size Custom Document Number  
NB4 **BLOCK DIAGRAM** Rev 1A

Date: Wednesday, January 30, 2008 Sheet 1 of 35

# INDEX

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1	SCHEMATIC BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
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4	S1G2 HT I/F 1/4	
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10	RS740/RS780-SYSTEM I/F 3/5	
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14	SB700-ACPI/GPIO/USB 2/4	
15	SB700-PWR/DECOUPLING 4/4	
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17	LCD/LED PANEL/LID/CAMERA	
18	HDMI/HDMI-CEC(R5F211A)	
19	CRT & G-SENSOR(LIS3L02A)	
20	SATA HDD/ODD & ESATA/USB	
21	PCMCIA(CB1410) -OPTION	
22	OZ129T(5IN1/1394)	
23	MINI CARD & NAND FLASH CARD	
24	NEW CARD & RJ45 BOARD/BEEP	
25	TP/FP/BT/PB/FELICA/MMB CONN	
26	CONEXANT(CX205601)/SPK/AMP	
27	JACK/VR/FM/MIC/MDC/AMPLIFIER	
28	EC(KBC)-WPCPC8763/WPC8769	
29	KEYBOARD/LED/KILL SW/HOLE	
30	CHARGER (ISL6251A)	
31	SYSTEM 5V/3V (ISL6237)	
32	AMD GRIFFIN (ISL6265)	
33	+NB_CORE (RT8202)	
34	DDR 1.8V(TPS51116)	
35	DISCHARGE (1.25V/1.5V)	

# Power Sequence



# 02

## SB700 SM BUS

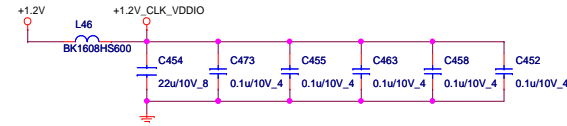
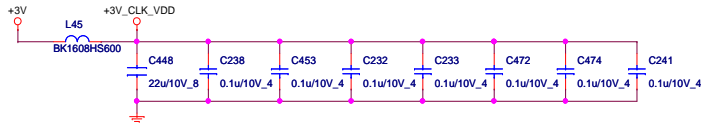
SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

## KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)



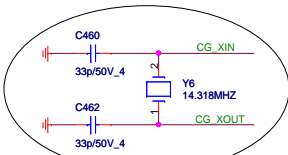
**PROJECT : BU2**  
Quanta Computer Inc.



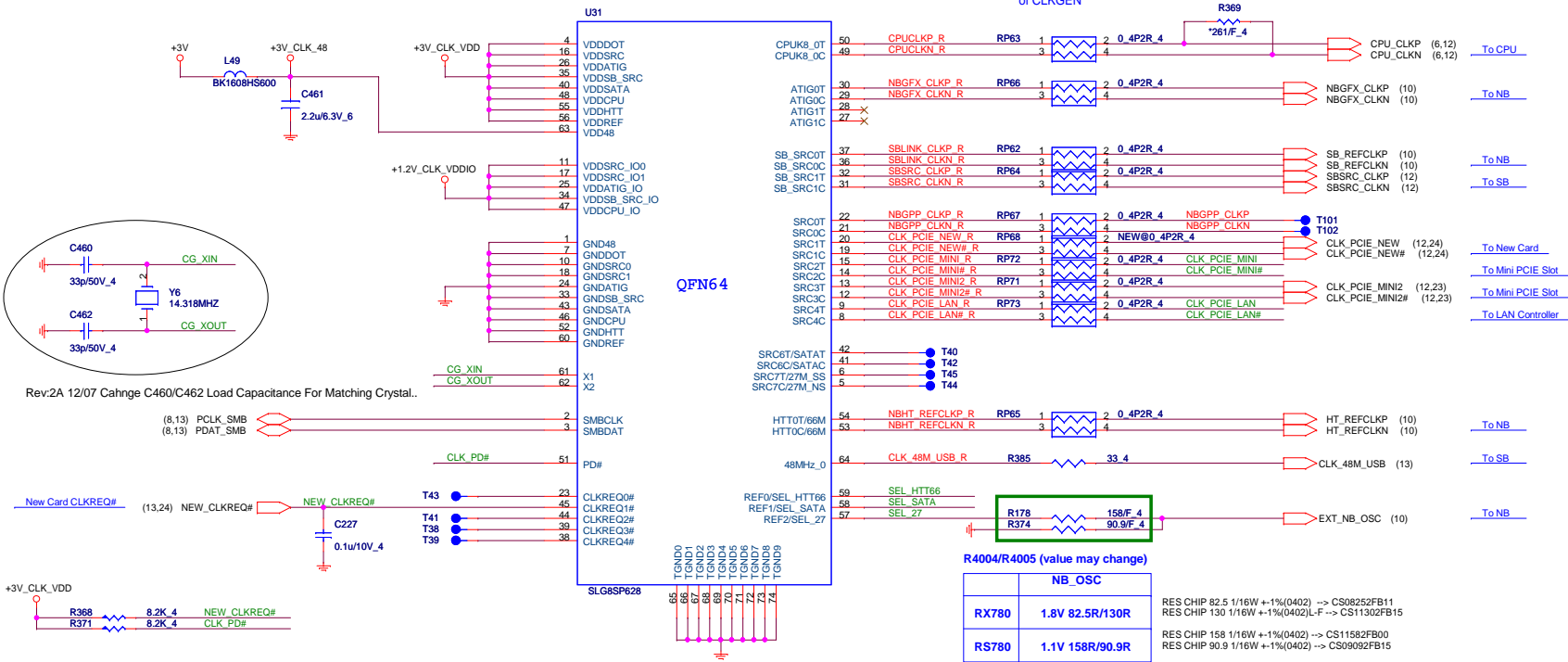
ICS9LPRS480 P/N :  
 SLG8SP628 P/N : AL8SP628000  
 RTM880N-796 P/N : AL00880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



Rev.2A 12/07 Cahnge C460/C462 Load Capacitance For Matching Crystal..



### NB CLOCK INPUT TABLE

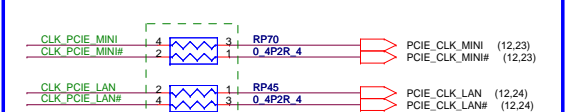
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

### R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) -> CS08252FB11  
 RES CHIP 130 1/16W +-1%(0402)L.F -> CS11302FB15  
 RES CHIP 158 1/16W +-1%(0402) -> CS11582FB00  
 RES CHIP 90.9 1/16W +-1%(0402) -> CS09092FB15

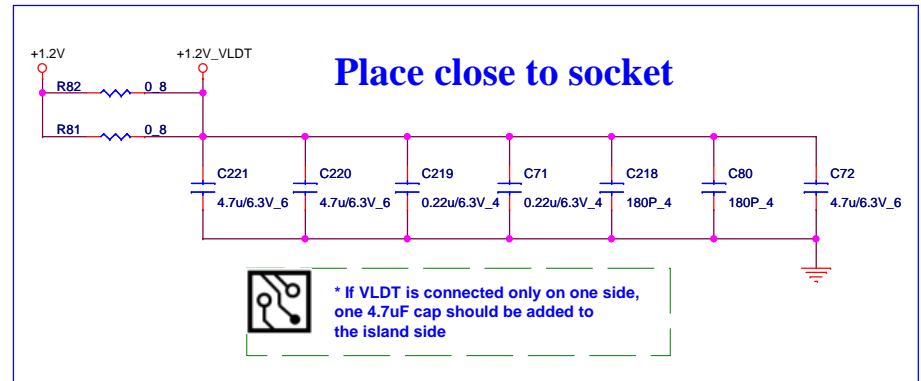
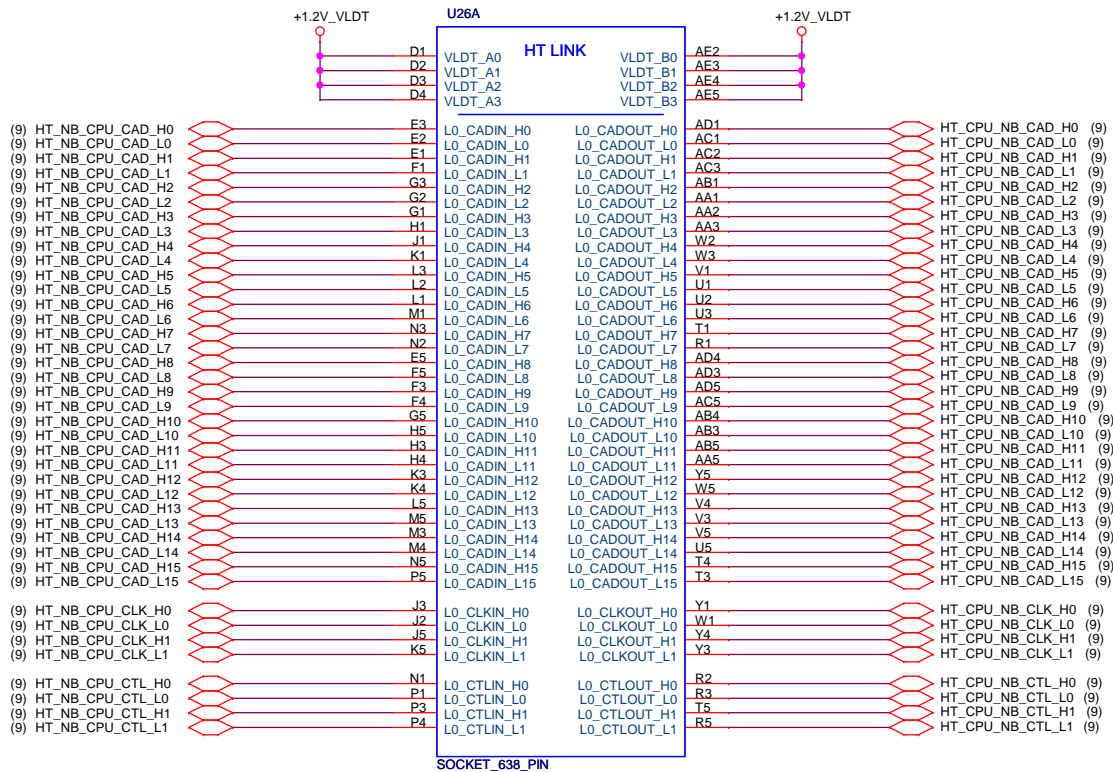
### FOR EXTERNAL/INTERNAL CLOCK



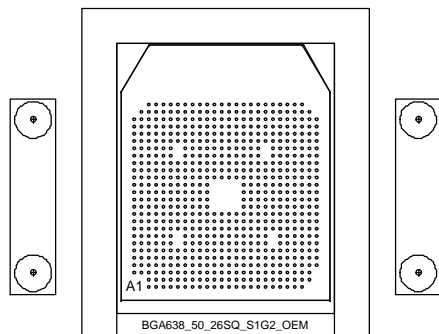
Place Close to Drivers Side

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

\* default

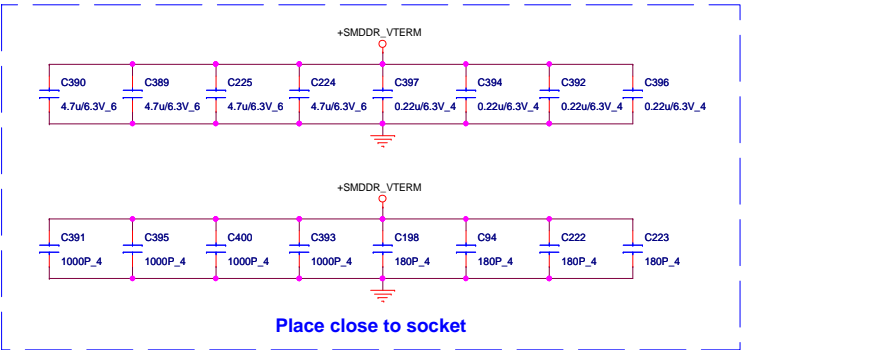
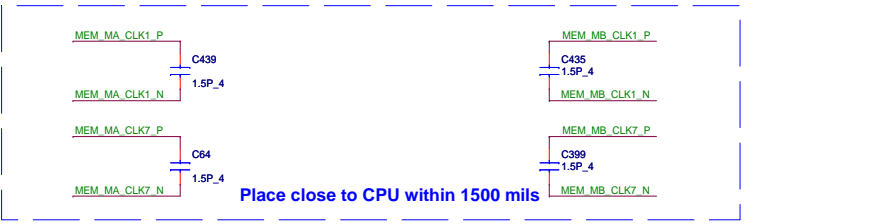
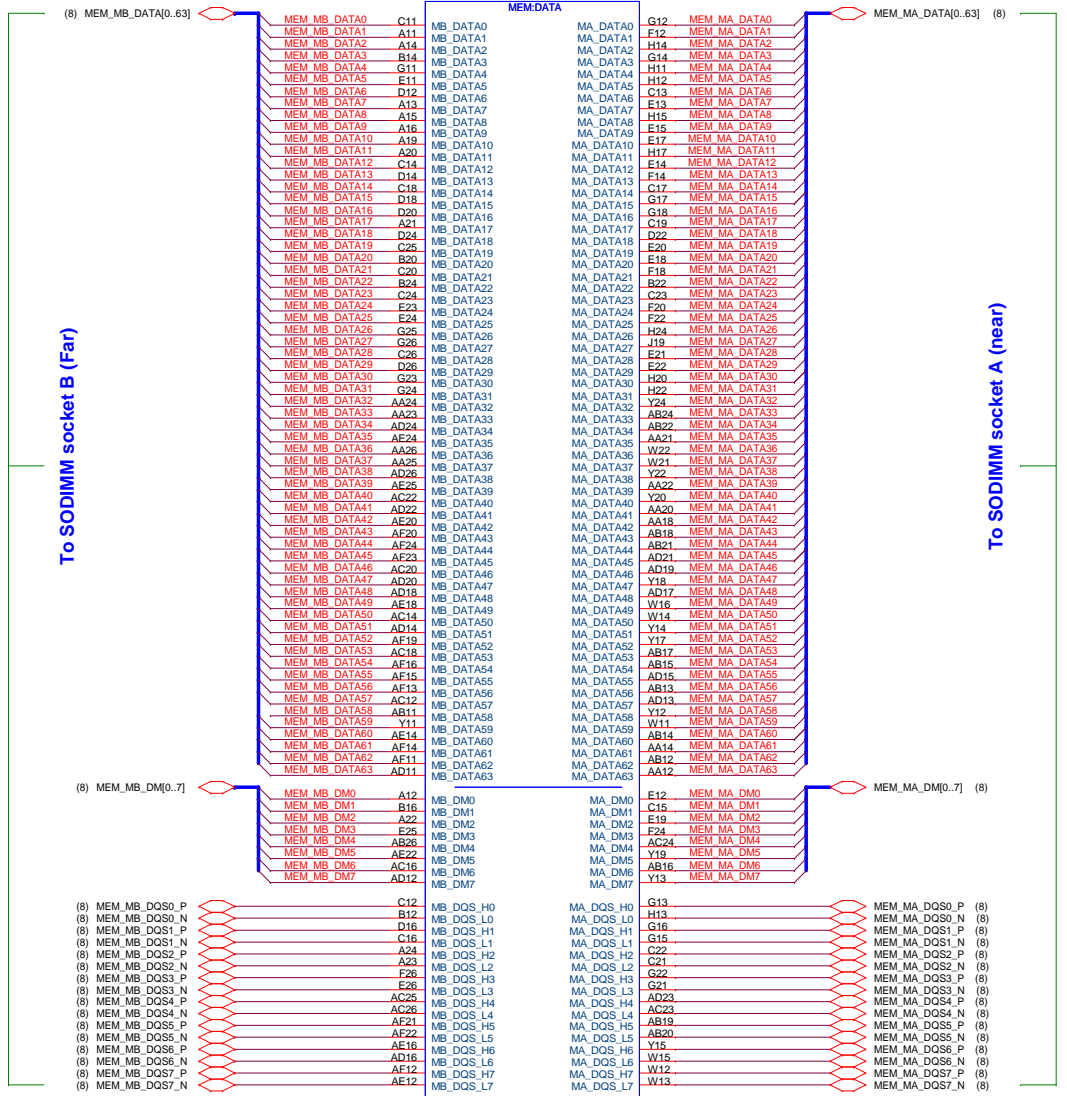
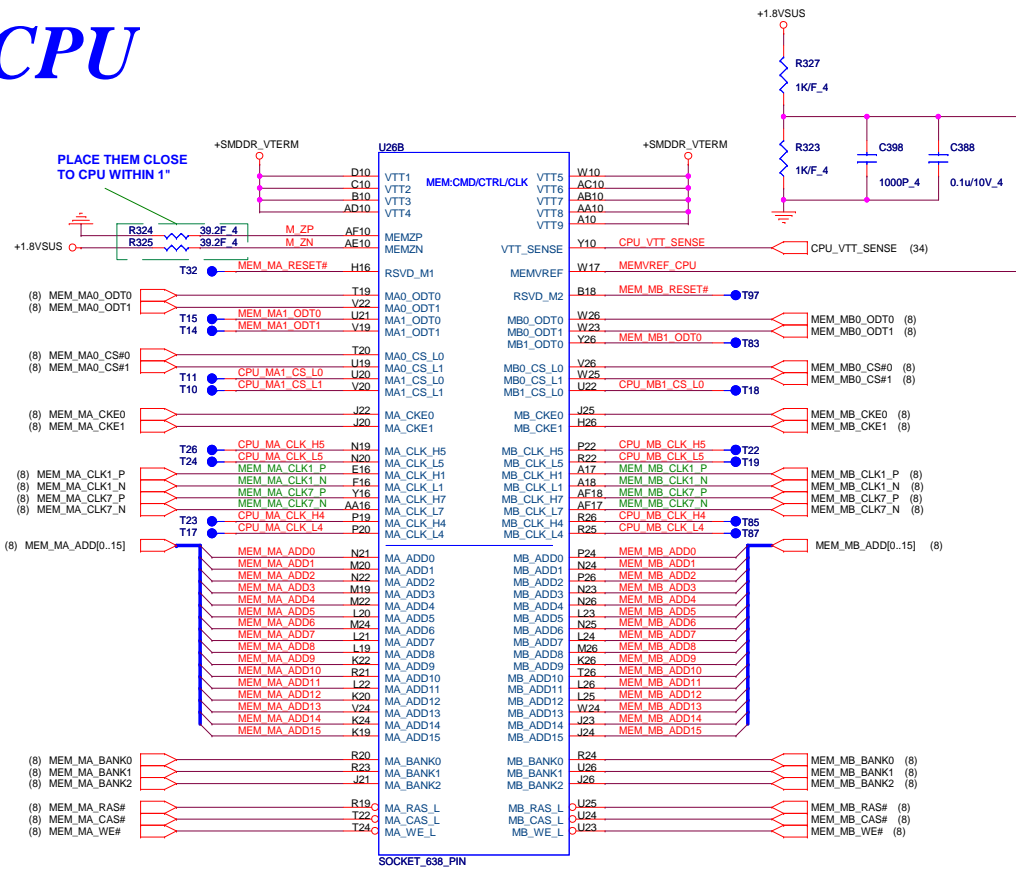


# CPU



	<b>PROJECT : BU2</b>		Rev 1A
	Quanta Computer Inc.		
Size B	Document Number	S1G2 HT I/F 1/4	
Date: Thursday, July 24, 2008		Sheet 4	of 35

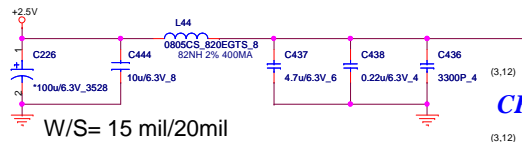
## Processor Memory Interface



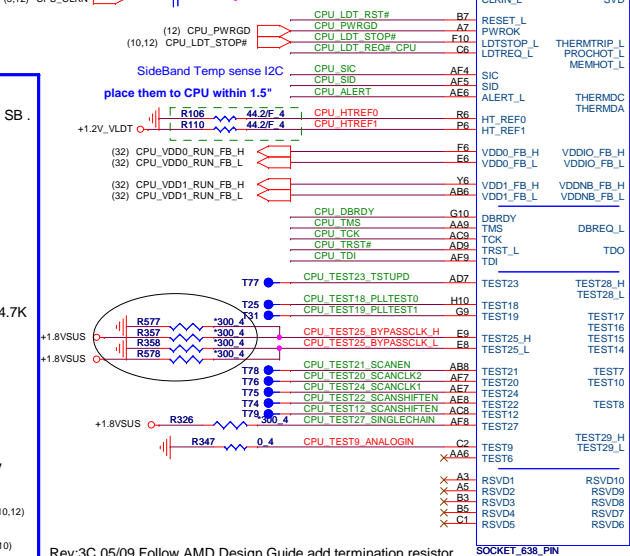
**PROJECT : BU2**  
**Quantia Computer Inc.**

Size Custom	Document Number	Rev 1A
	<b>S1G2 DDR1 MEMORY I/F 2/4</b>	
Date: Thursday, July 24, 2008	Sheet 5 of 35	

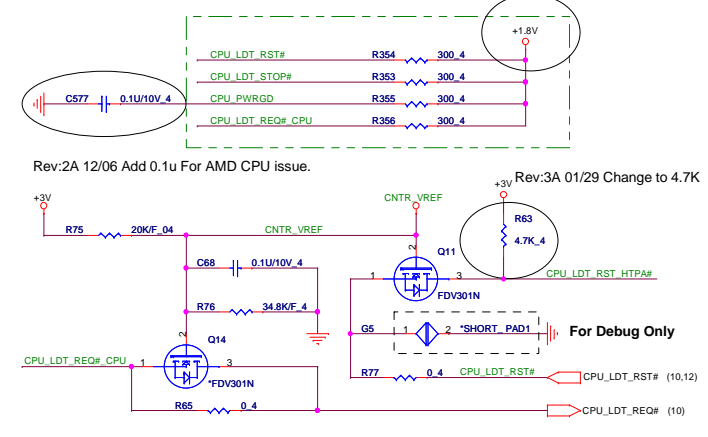
# CPU



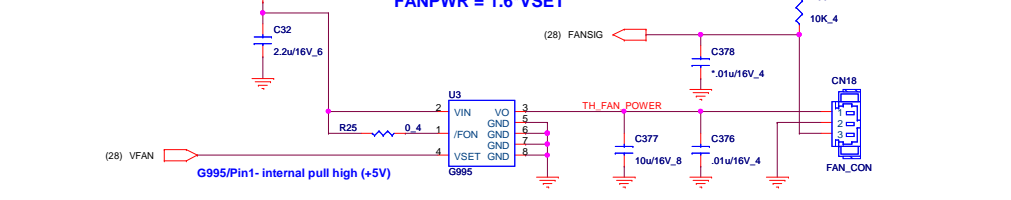
## CPU CLK



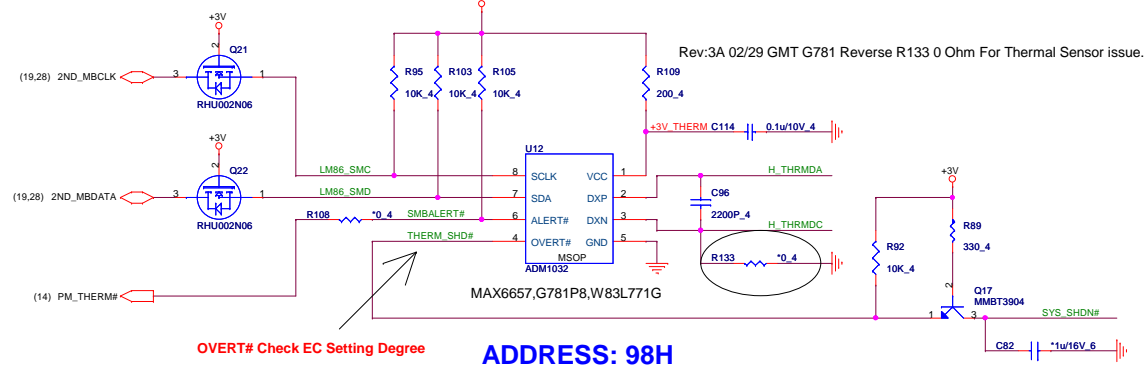
## CPU POWER-UP



## CPU FAN

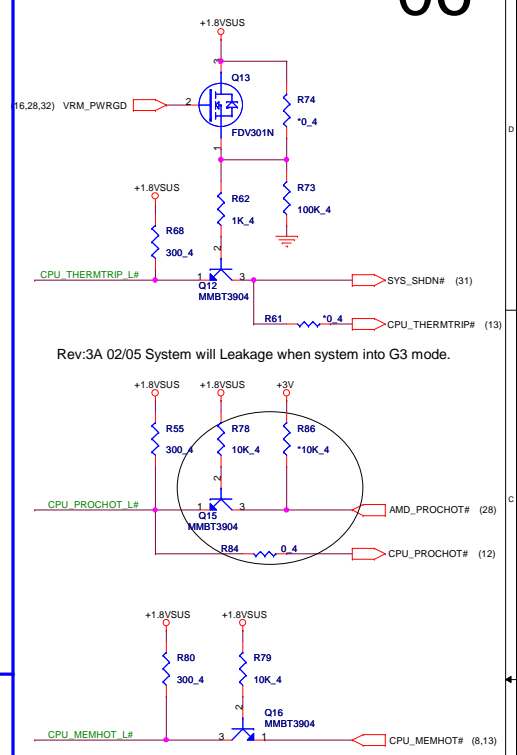


## CPU H/W MONITOR

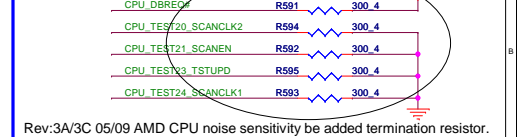


# CPU THERM

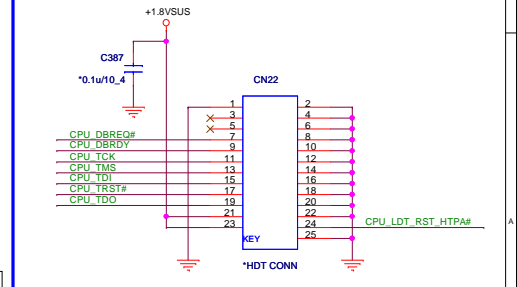
06



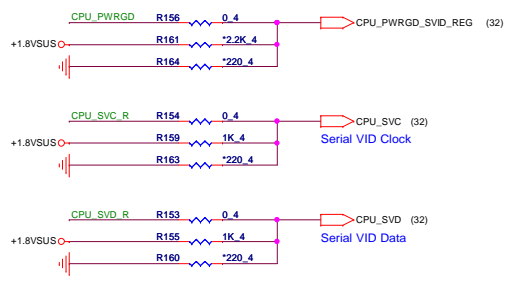
## Reserve Test Port



## HDT Connector



## Serial VID

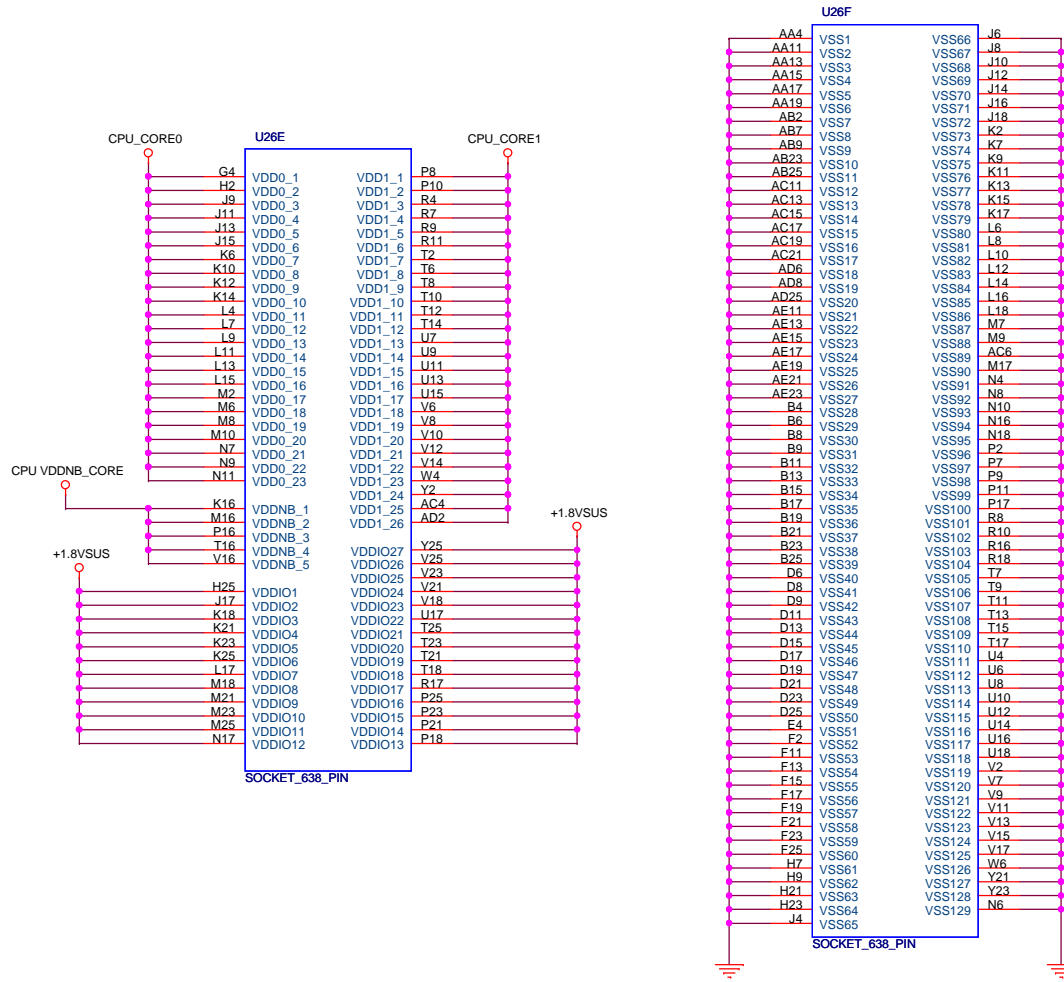


**PROJECT : BU2**  
Quanta Computer Inc.

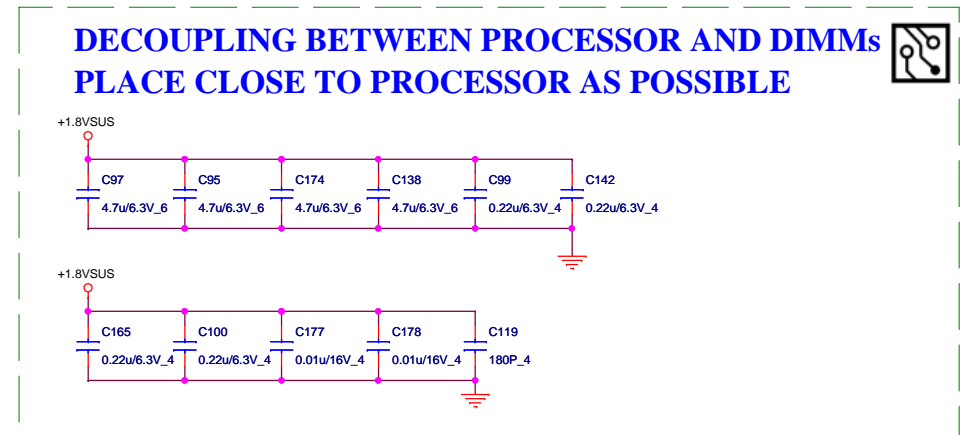
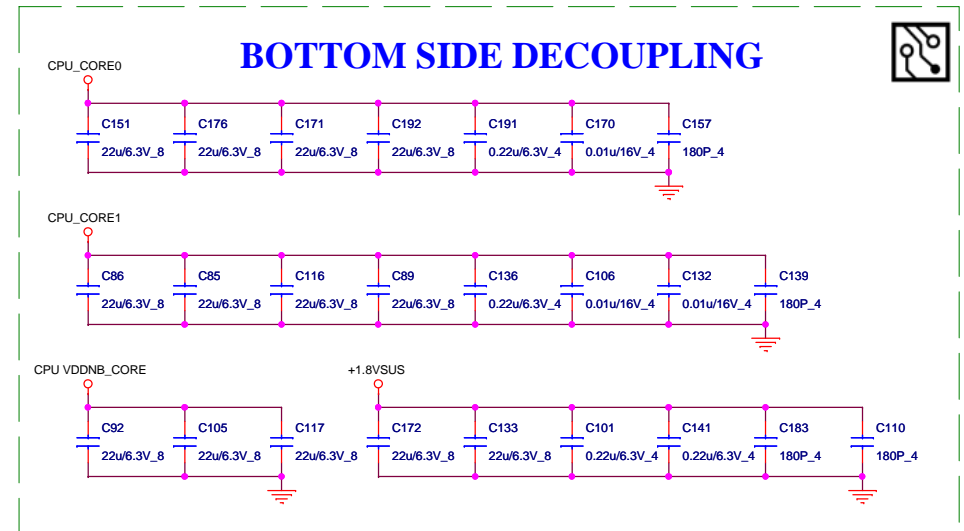
Size Custom Document Number **S1G2 CTRL & DEBUG 3/4** Rev 1A

Date: Thursday, July 24, 2008 Sheet 6 of 35

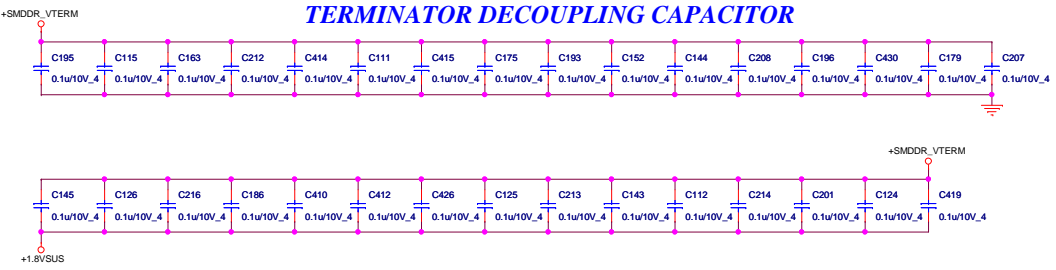




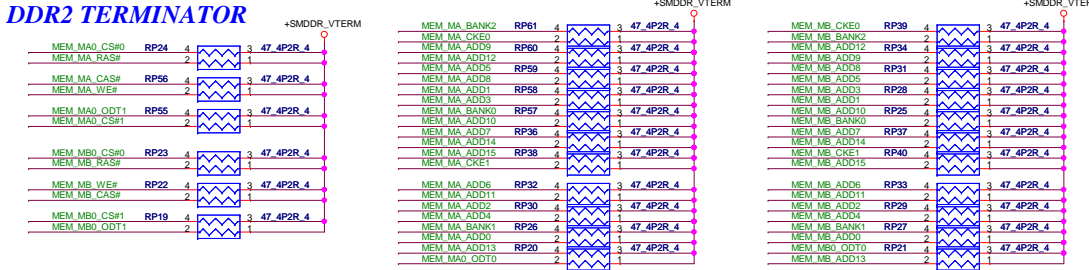
## PROCESSOR POWER AND GROUND



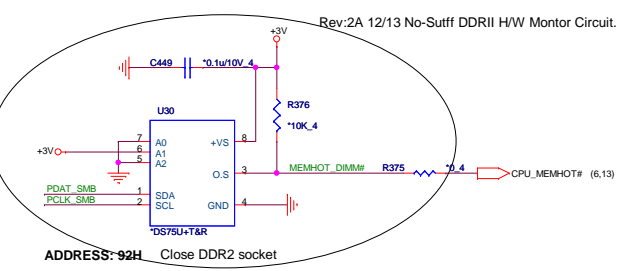
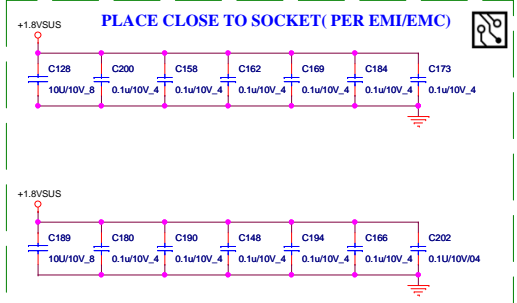
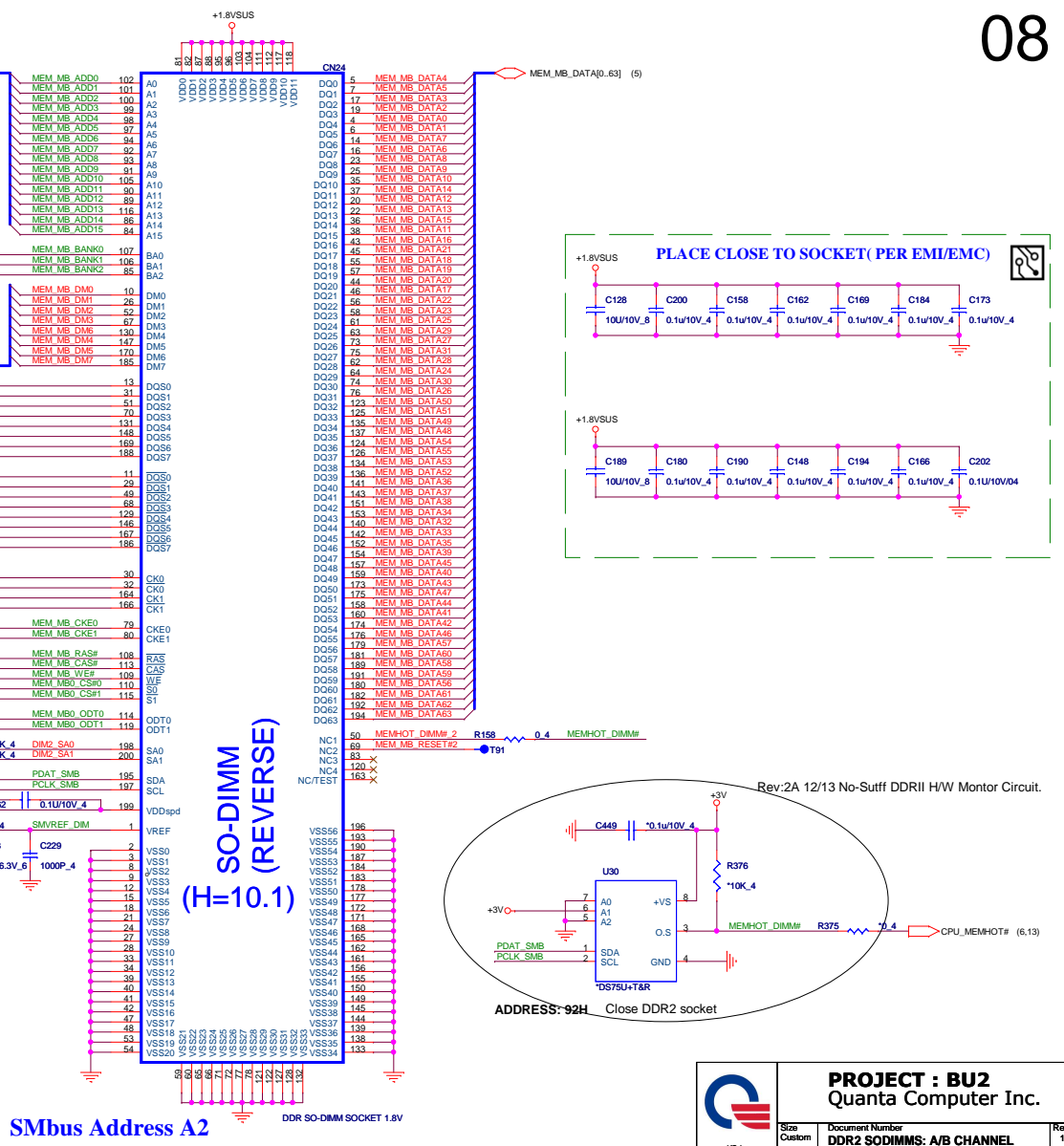
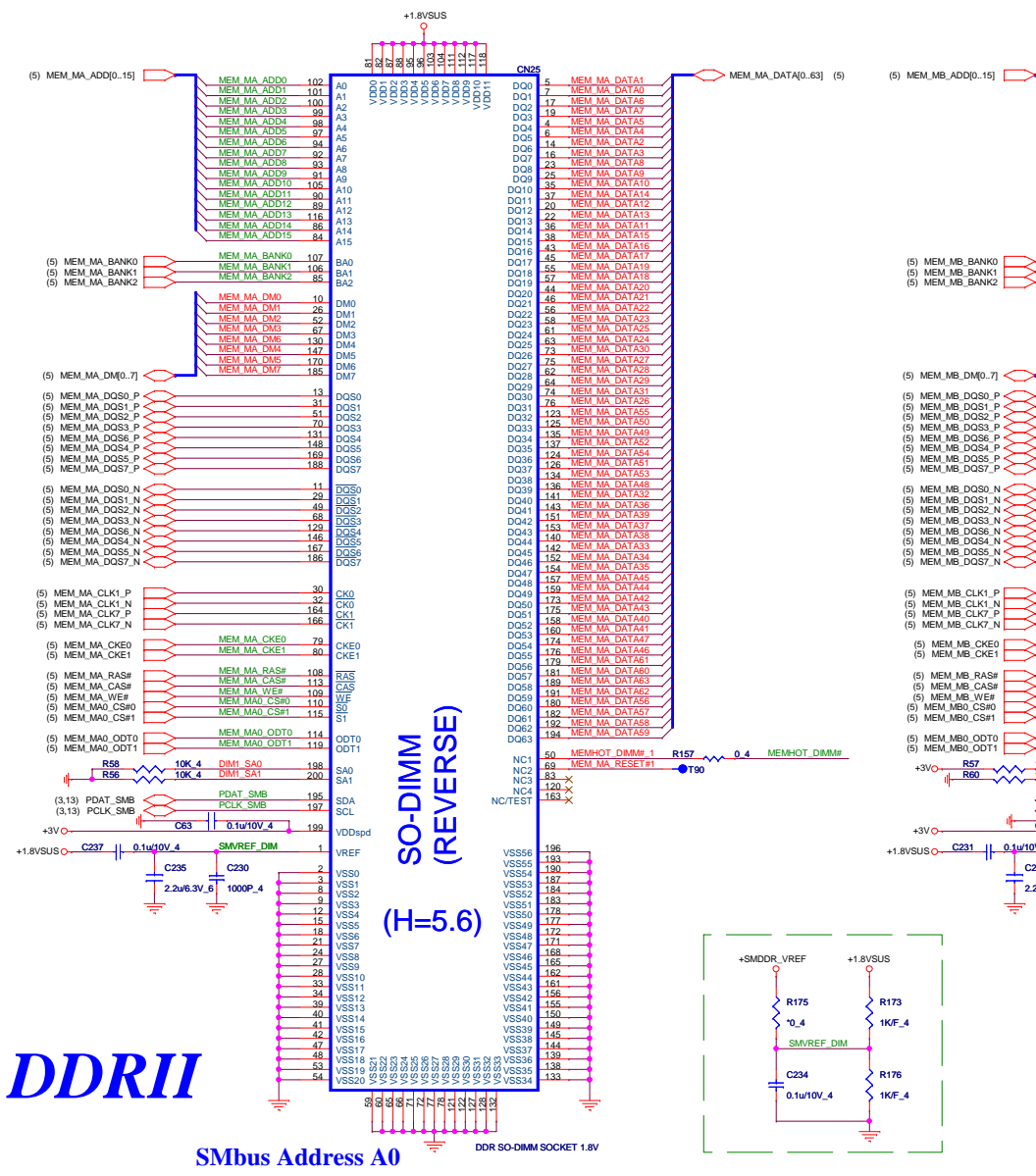
# TERMINATOR DECOUPLING CAPACITOR



# DDR2 TERMINATOR



08



**DDRII**

SMBus Address A0

SMBus Address A2

**PROJECT : BU2**  
**Quanta Computer Inc.**

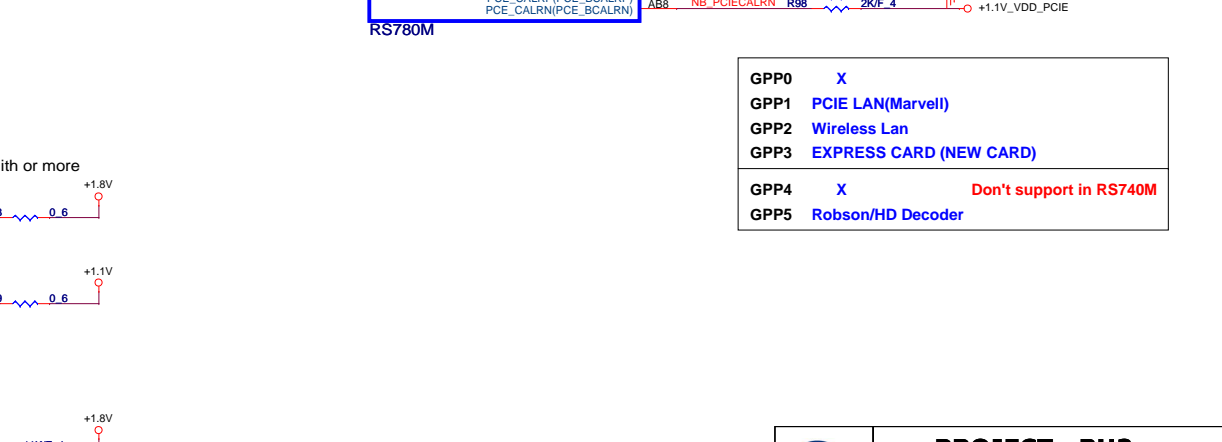
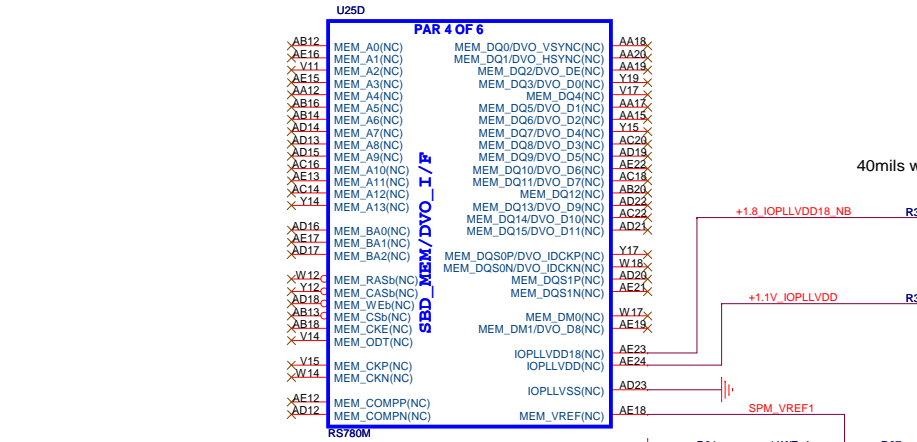
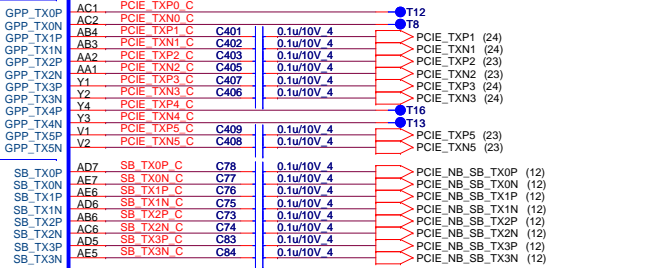
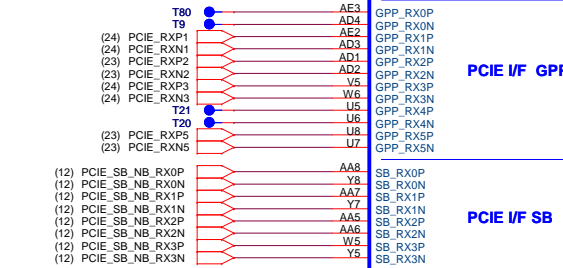
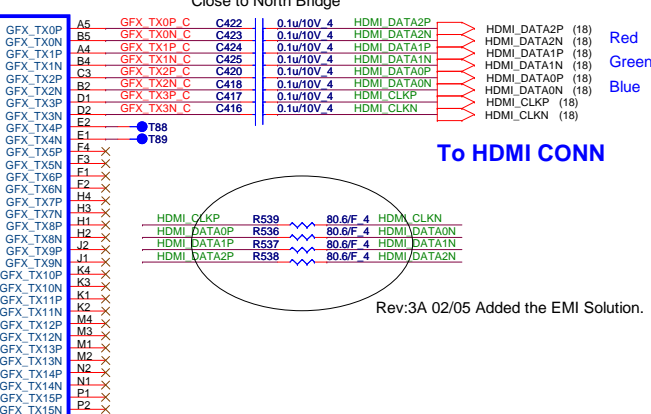
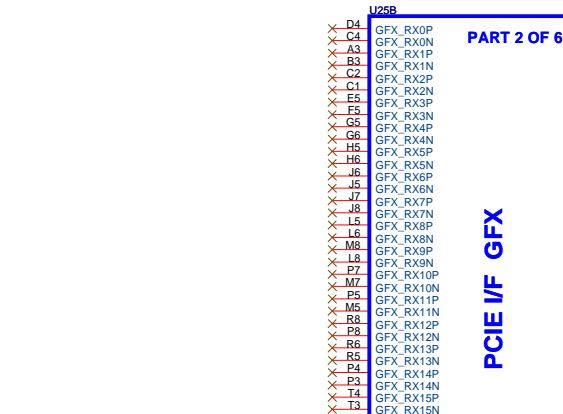
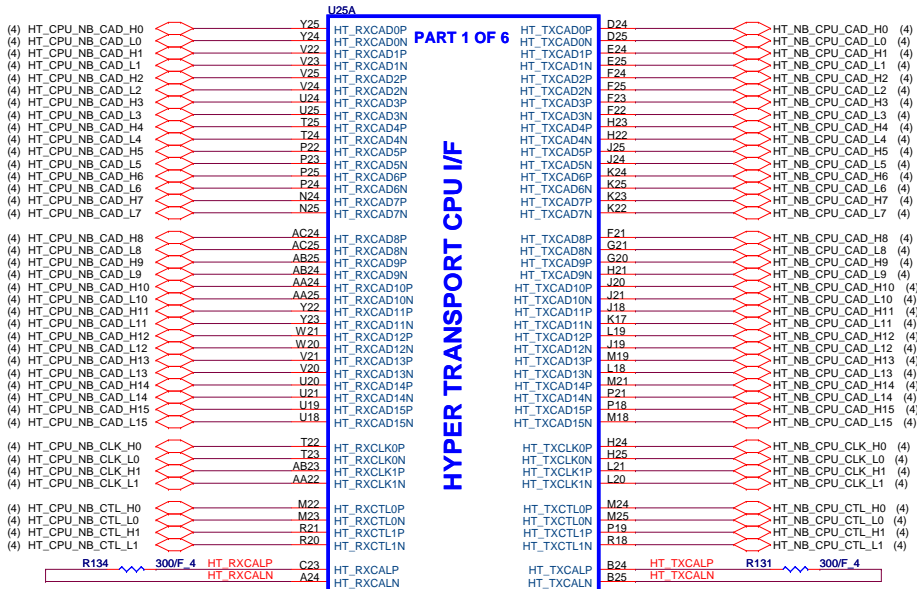
Size Custom    Document Number **DDR2 SODIMMS: A/B CHANNEL**    Rev 1A

Date: Thursday, July 24, 2008    Sheet 6 of 35



### RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



GPP0	X	
GPP1	PCIE LAN(Marvell)	
GPP2	Wireless Lan	
GPP3	EXPRESS CARD (NEW CARD)	
GPP4	X	Don't support in RS740M
GPP5	Robson/HD Decoder	

**PROJECT : BU2**  
Quanta Computer Inc.

Size: Custom Document Number: RS740/RS780-HT LINK/PCIE I/F 1/4 Rev: 1A

Date: Thursday, July 24, 2008 Sheet 9 of 35

Rev:3A 02/13 Follow A13 silicon Change R120 From 150 To 140ohm For Unbalanced power bus IR drop.

150R Termination < 1000 mils trace

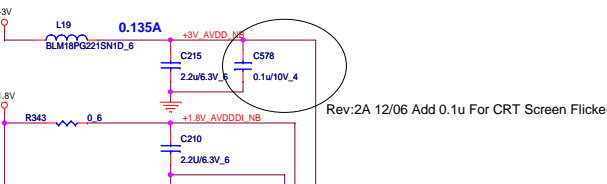
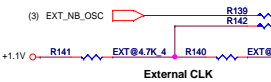
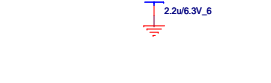
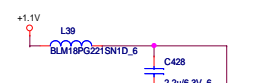
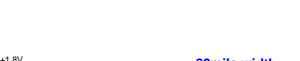
CLOSE TO NB



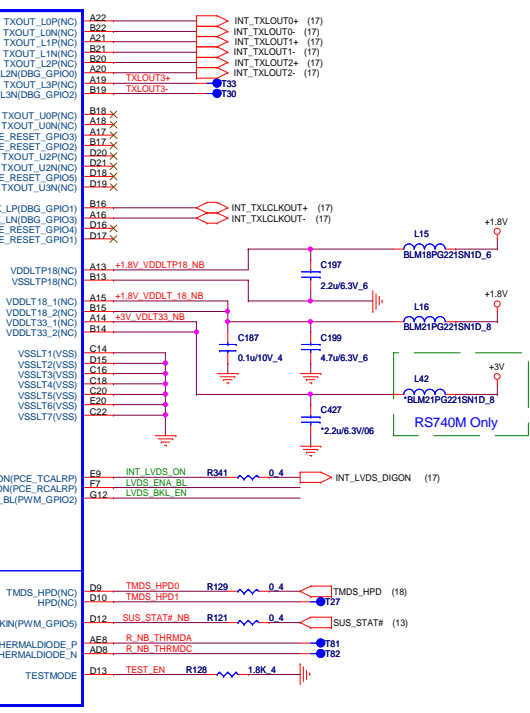
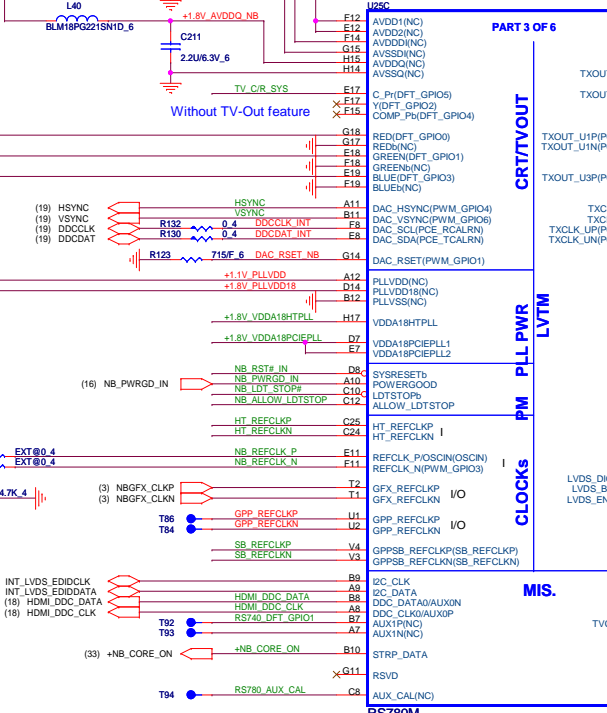
20mils width



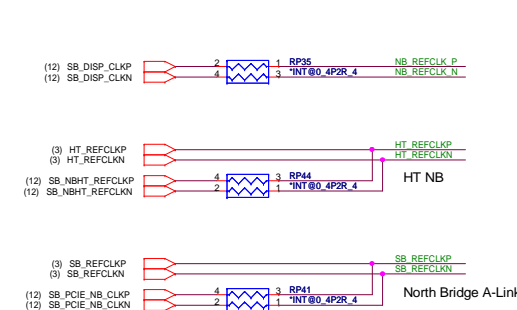
20mils width



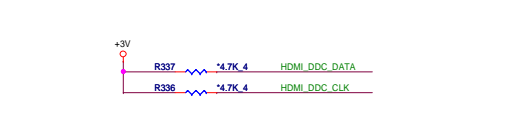
Rev:2A 12/06 Add 0.1u For CRT Screen Flicker.



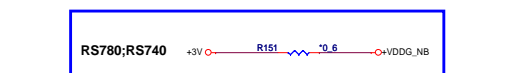
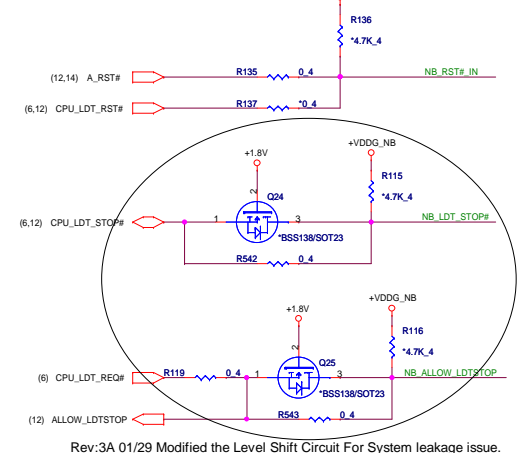
FOR SB INTERNAL CLOCK



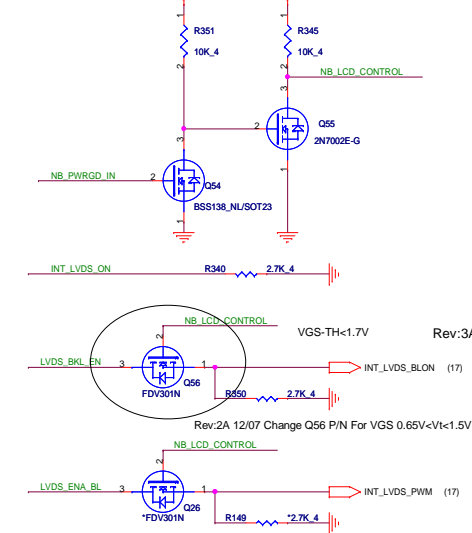
Reserve Pin



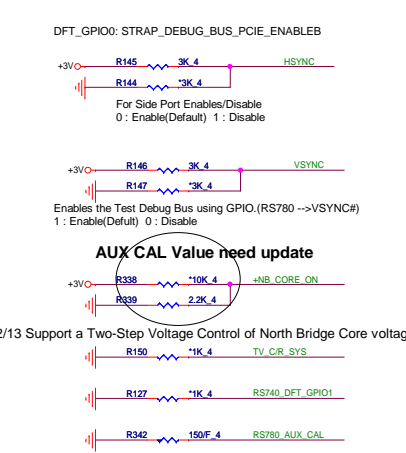
North Bridge RESET



LVDS BLON



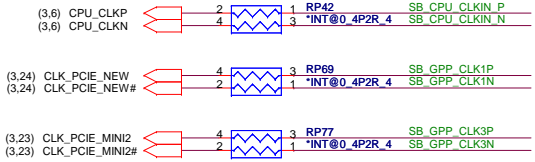
STRAP DEBUG BUS GPIO



PROJECT : BU2 Quanta Computer Inc. RS740/RS780-SYSTEM I/F 3/5



## FOR INTERNAL CLOCK



Place close to CLK GEN

1. PCIE Reference Clk (Ext Clk Gen)
2. A-Link Clk to North Bridge (Int Clk Gen)

From Clk Gen Input

To NB A-Link CLK

For North Bridge

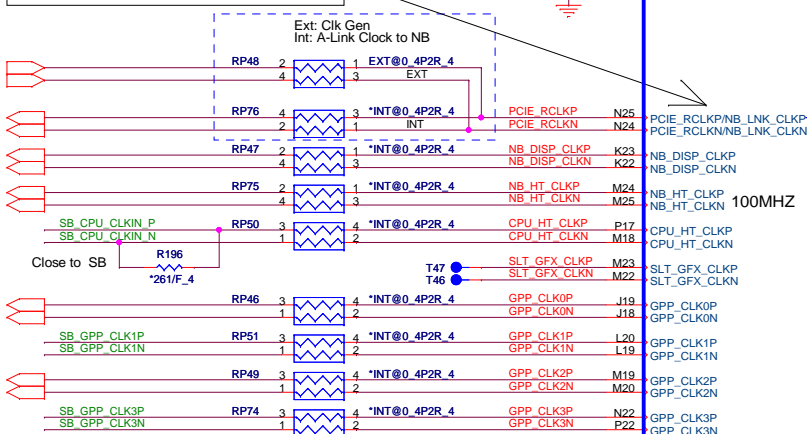
For North Bridge

For CPU Host Clk

To Marvell Lan

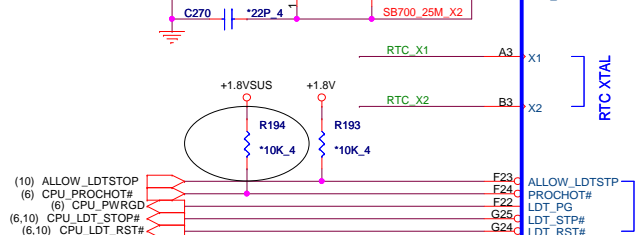
To New Card

To Mini Card 1,2

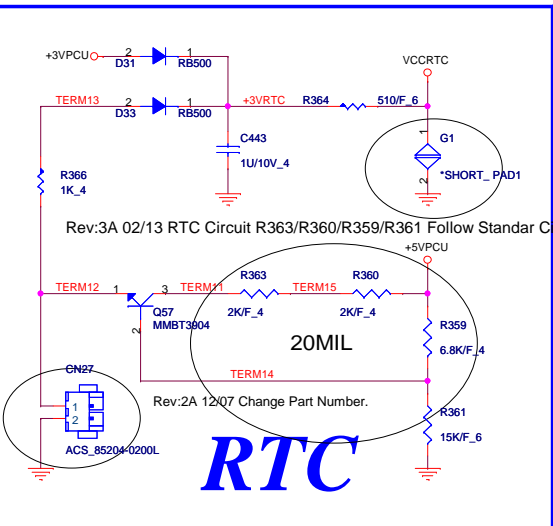


Rev:3B 04/02 As the same location Name(G1) For Toshiba Service Team Request.

Install for Int Clk Gen



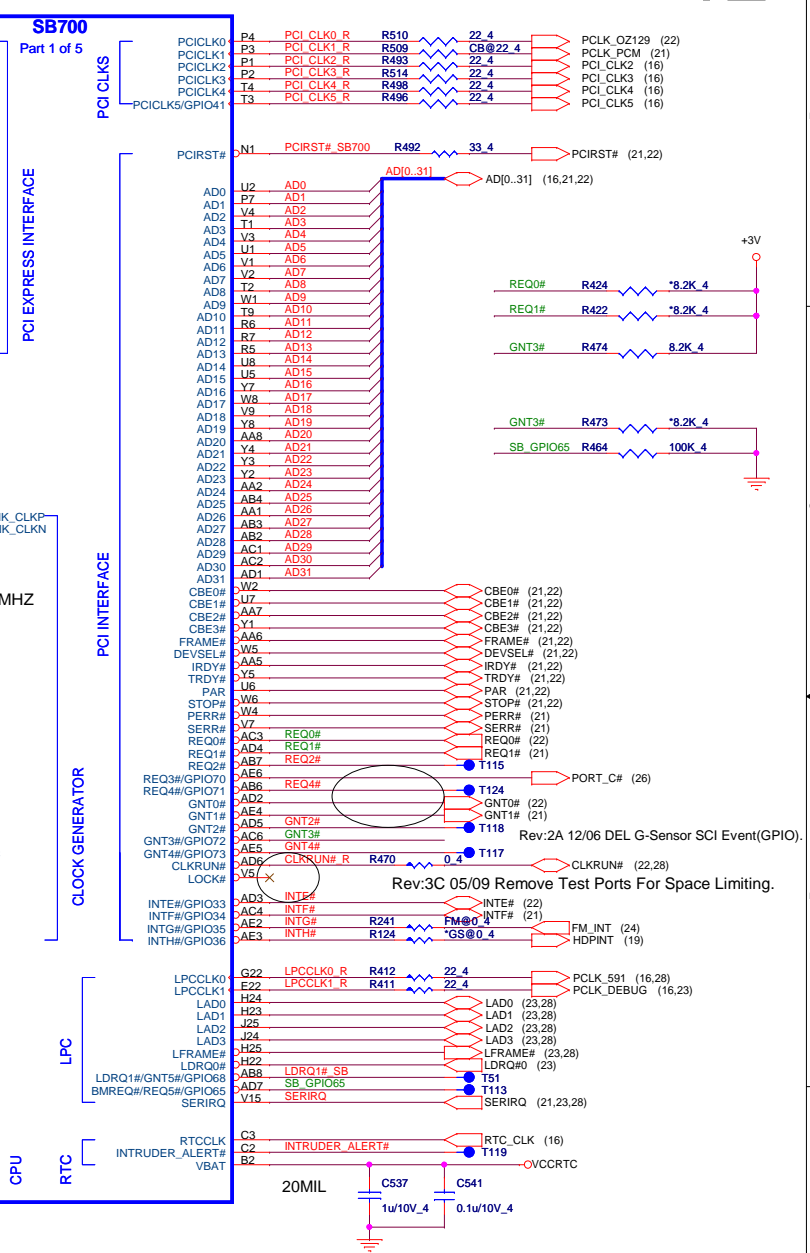
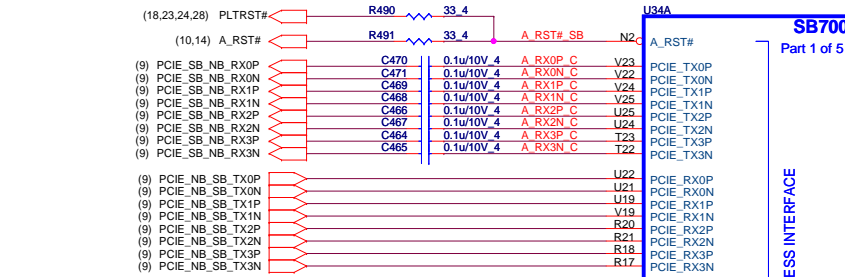
Rev:3A 02/05 No-Stuff R194 For Leakage when system into G3 mode.



Rev:3A 02/13 RTC Circuit R363/R360/R359/R361 Follow Standar Circuit Value.

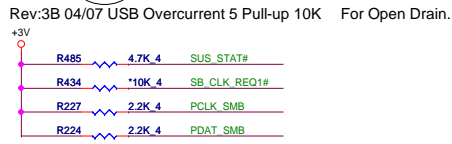
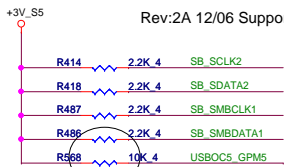
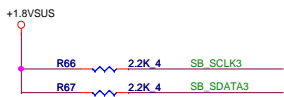
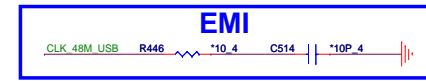
# RTC

## AC COUPLING CAPS CLOSE TO SB700

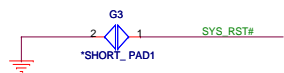


**PROJECT : BU2**  
Quanta Computer Inc.

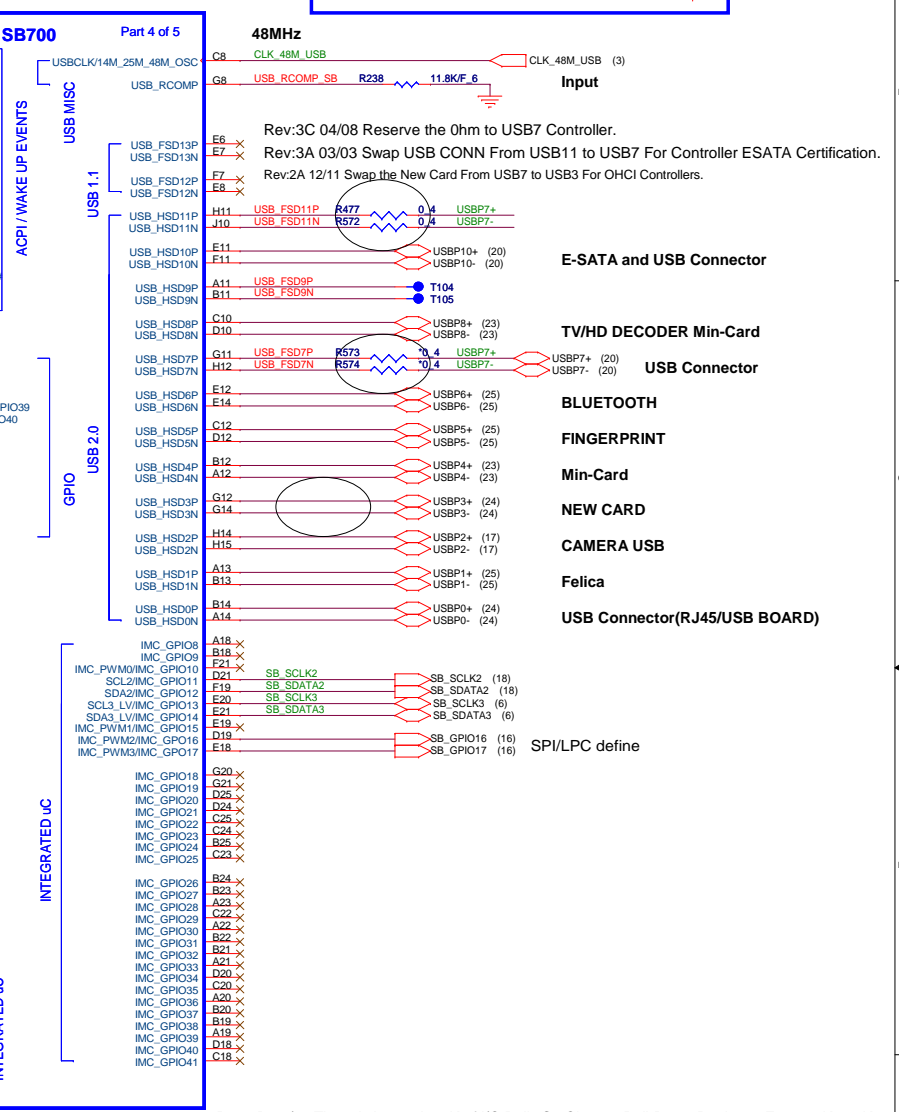
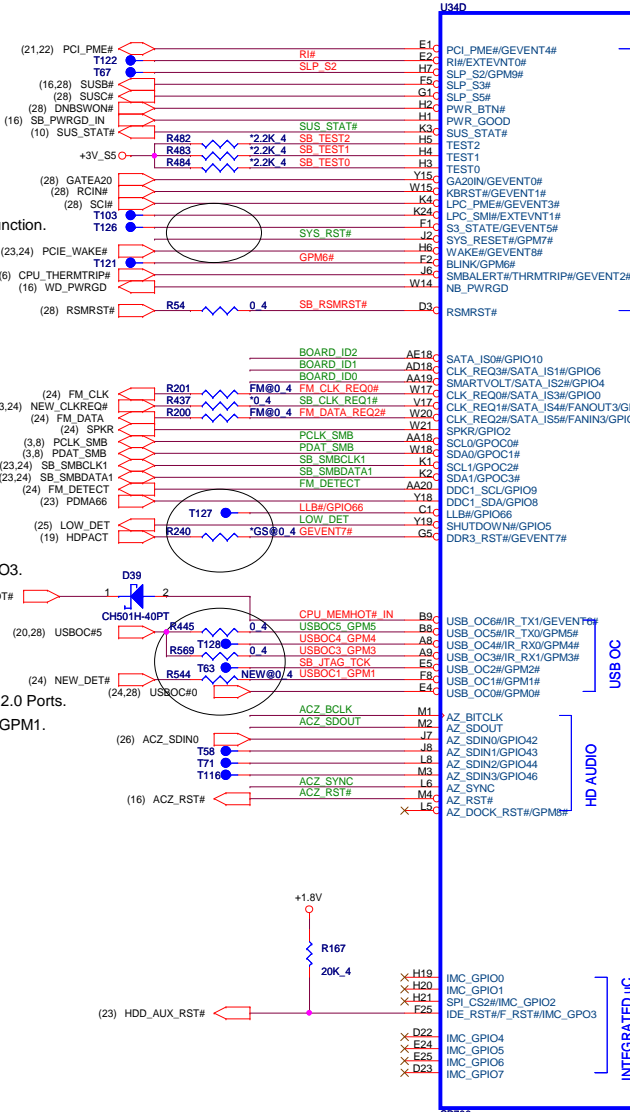
Size Custom  
Document Number  
**SB700-PCIE/PCU/LPC 1/4**  
Date: Thursday, July 24, 2008 | Sheet 12 of 35



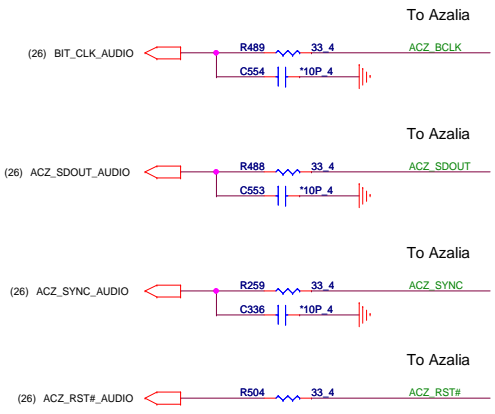
Rev:2A 12/06 Support the New Card Hot Plug Function.  
 Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.



Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.  
 Rev:3A 02/05 Move Hot Plug Pin Name From EVENT5# to GPM1#.



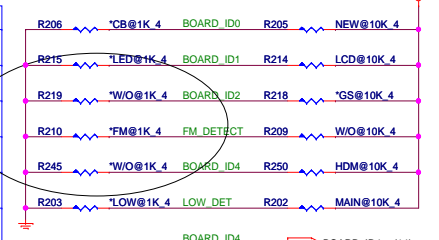
## HD Audio Interface



## MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H	L				
W/ CCFL Panel W/ LED Panel		H	L			
W/ G-Sensor W/O G-Sensor			H	L		
W/O FM W/FM				H	L	
W/ HDMI W/O HDMI					H	L
Main Stream Low Cost						H

## MB ID



Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K.

**PROJECT : BU2**  
**Quanta Computer Inc.**

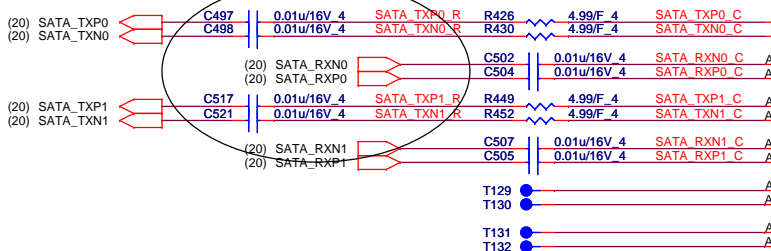
Size Custom	Document Number <b>SB700-ACPI/GPIO/USB 2/4</b>	Rev 1A
Date: Thursday, July 24, 2008		Sheet 13 of 35



# SB700

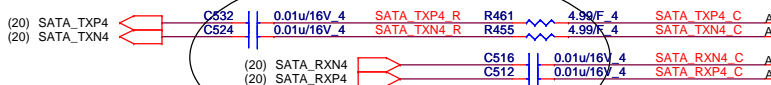
PLACE SATA AC COUPLING CAPS CLOSE TO SB700

### SATA HDD



Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

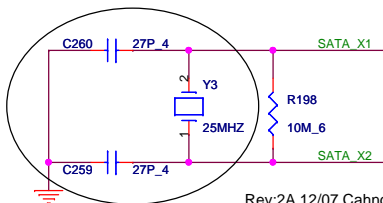
### SATA ODD



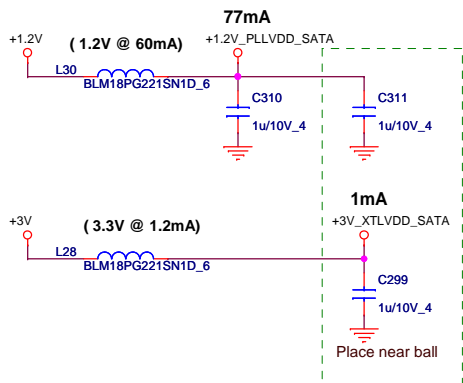
Rev:3A 02/22 Change Setting the SATA ODD to be IDE Legacy class Mode..

#### NOTE:

R635 IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK



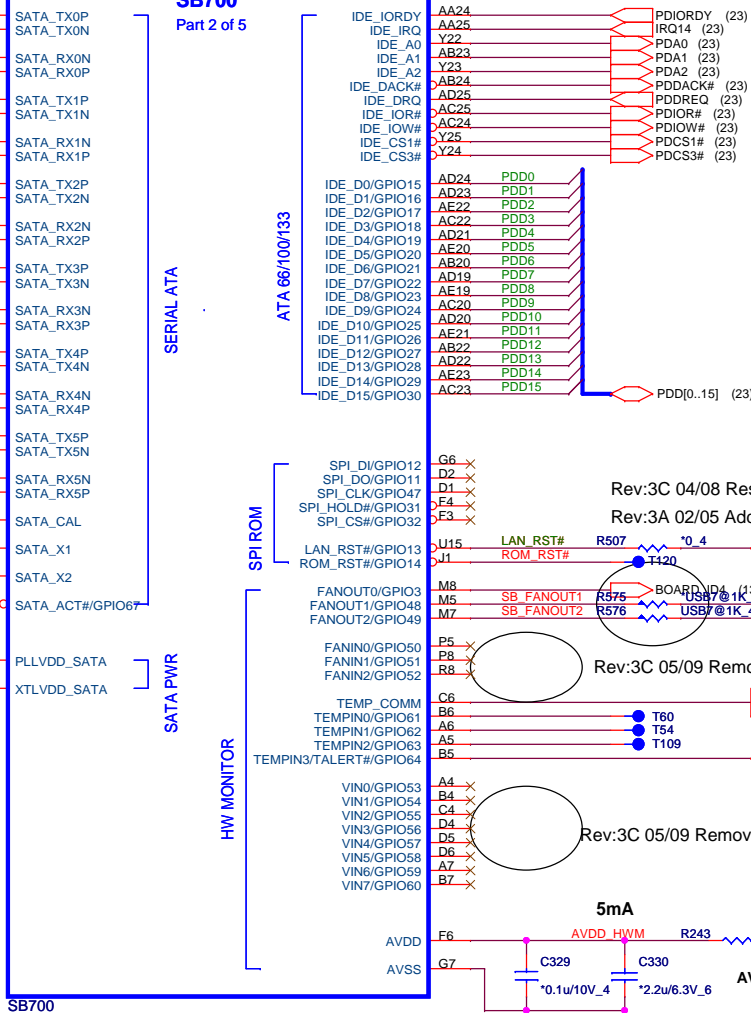
Rev:2A 12/07 Cahnge C259/C260 Load Capacitance For Matching Crystal.



U34B

### SB700

Part 2 of 5



Rev:3C 04/08 Reserve the Board ID For USB Controller.  
Rev:3A 02/05 Added the Board ID4 to GPIO3.

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:2A 12/07 Change +3V Domain For System Leakage When System into S5 Mode.



**PROJECT : BU2**  
Quanta Computer Inc.

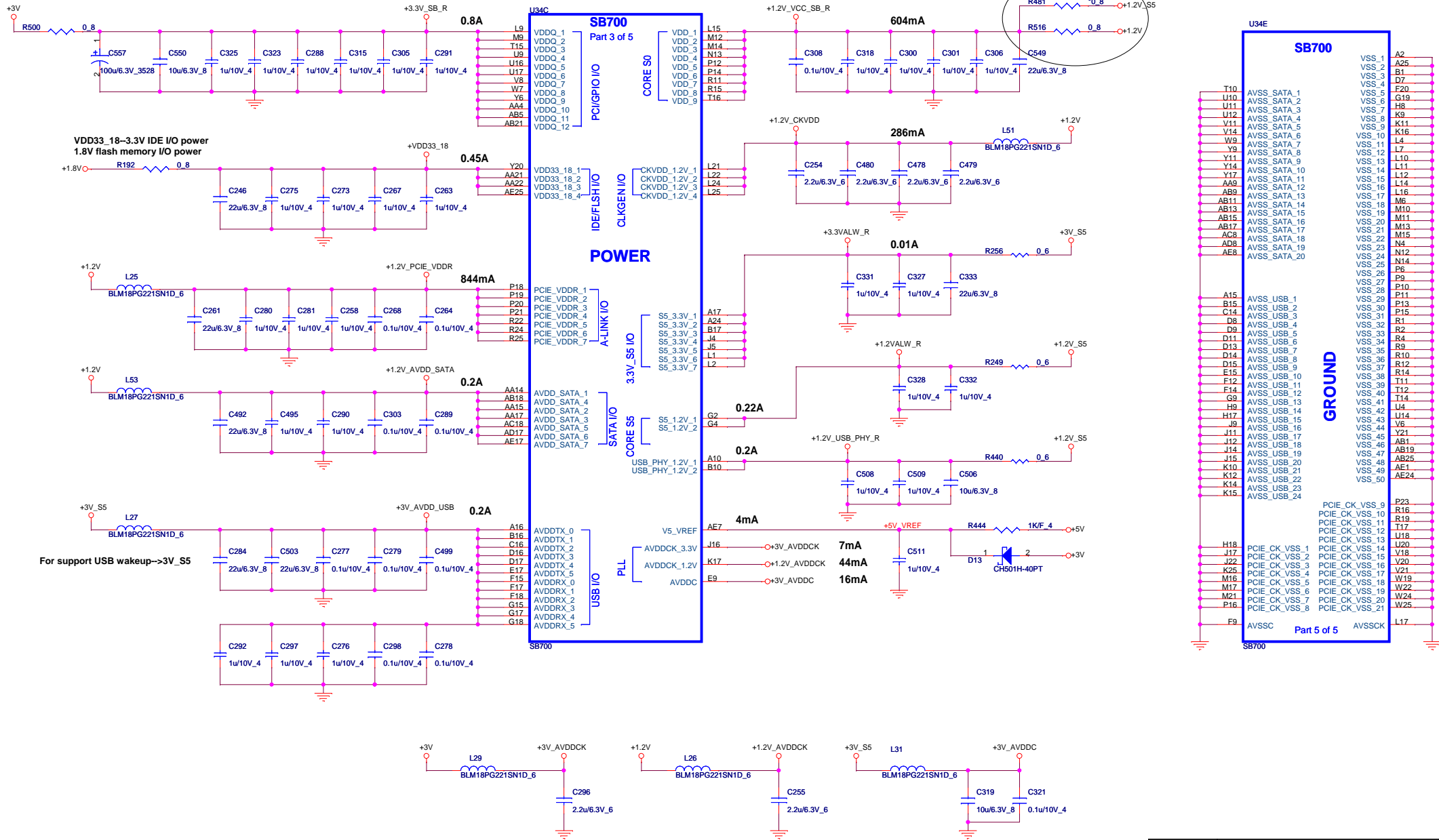
Size Custom	Document Number <b>SB700-ACPI/GPIO/USB 2/4</b>	Rev 1A
Date: Thursday, July 24, 2008		Sheet 14 of 35

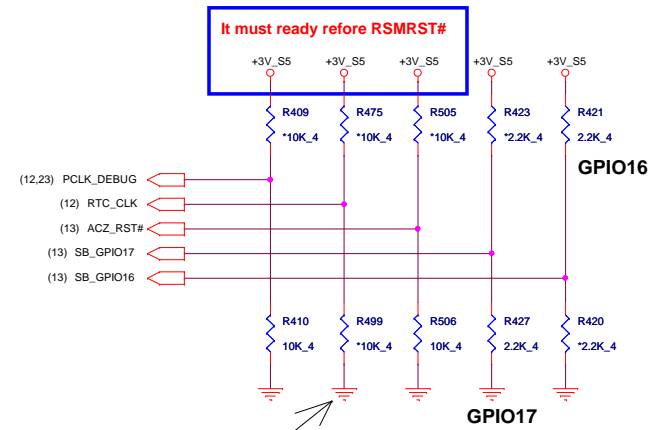
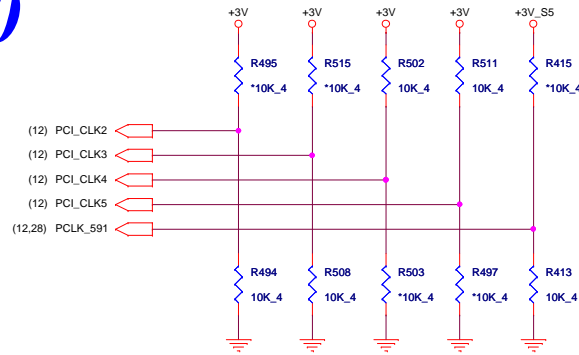


Rev:2A 12/10 The VDD Power Pin to be connected to S0\_1.2V Power For A12 Chip.

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

A11 Chip Bug use A12 Chip Can Remove





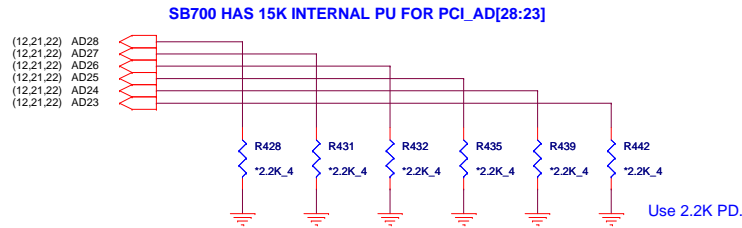
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

## REQUIRED STRAPS

PULL HIGH	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED <i>DEFAULT</i>	IGNORE DEBUG STRAPS <i>DEFAULT</i>			DISABLE PCI MEM BOOT <i>DEFAULT</i>

PULL HIGH	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
	CLKGEN ENABLED	INTERNAL RTC <i>DEFAULT</i>	EC ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	CLKGEN DISABLED <i>DEFAULT</i>	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED <i>DEFAULT</i>		L, H = LPC ROM L, L = FWB ROM <i>DEFAULT</i>

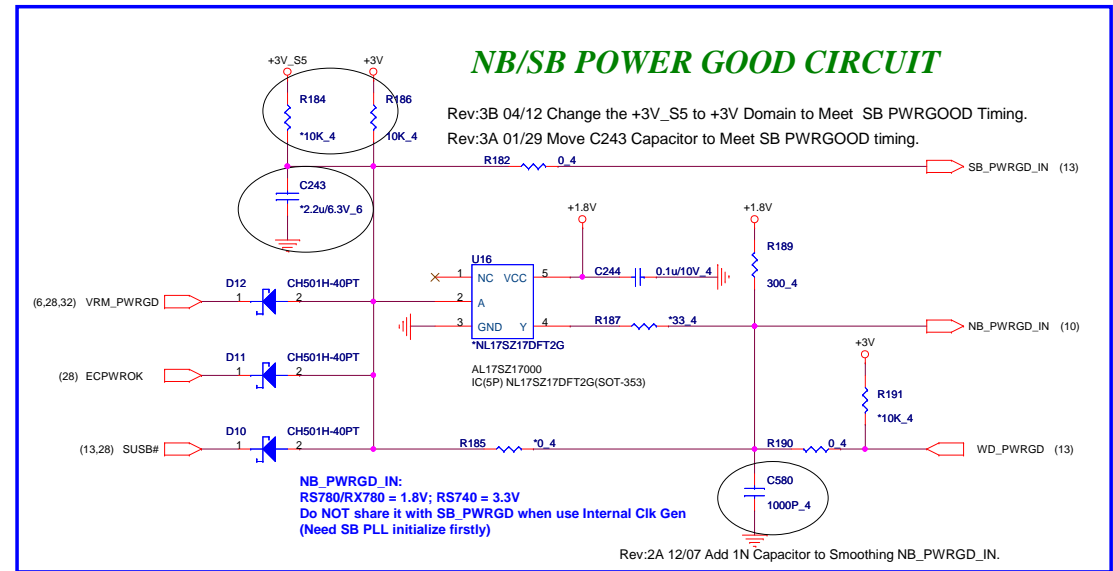
## DEBUG STRAPS



## REQUIRED STRAPS

PULL HIGH	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
	USE LONG RESET <i>DEFAULT</i>	USE PCI PLL <i>DEFAULT</i>	USE ACPI BCLK <i>DEFAULT</i>	USE IDE PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

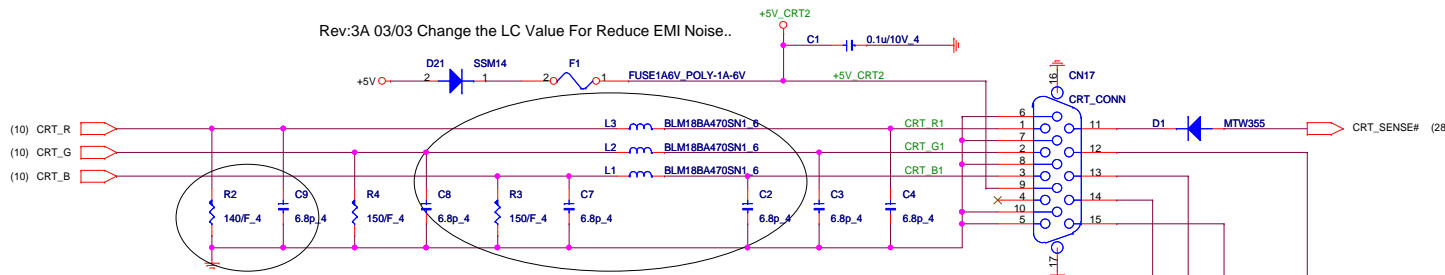
## NB/SB POWER GOOD CIRCUIT



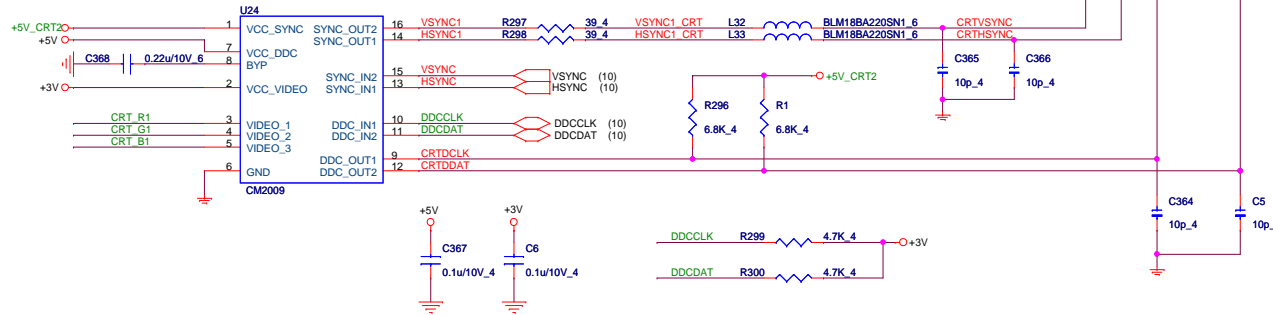




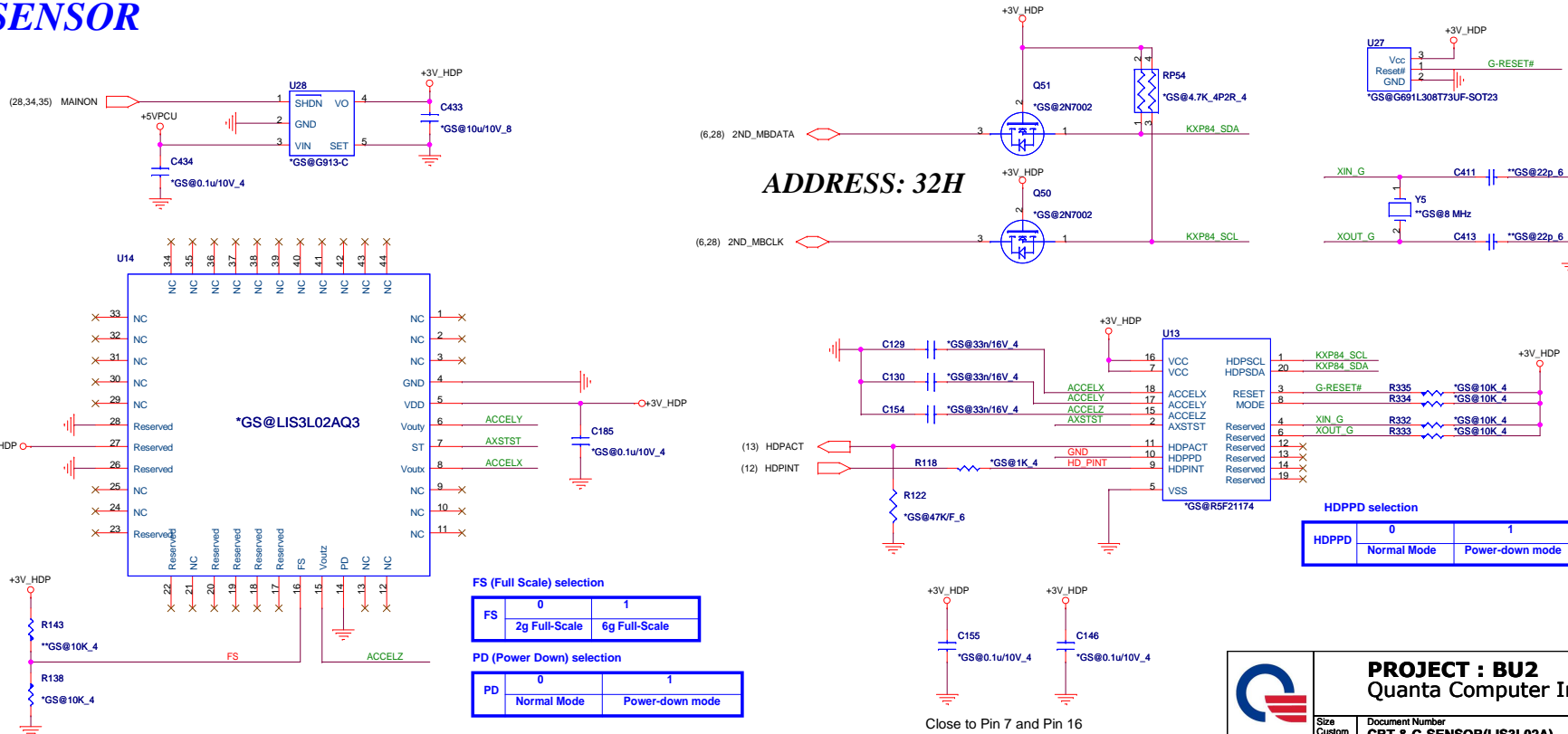
Rev:3A 03/03 Change the LC Value For Reduce EMI Noise..



Rev:3A 02/13 Follow A13 silicon Change R2 From 150 To 140ohm For Unbalanced power bus IR drop..



G-SENSOR



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

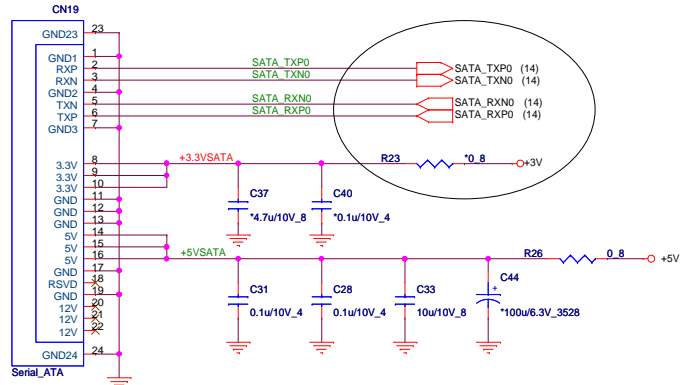
HDPDP selection

HDPDP	0	1
	Normal Mode	Power-down mode

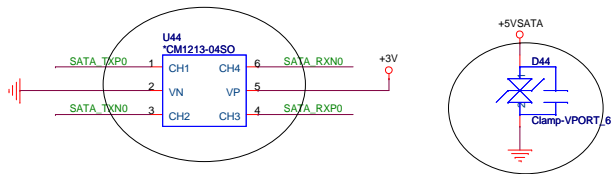
**PROJECT : BU2**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	<b>CRT &amp; G-SENSOR(LIS3L02A)</b>	
Date: Thursday, July 24, 2008	Sheet 19 of 35	

# SATA HDD

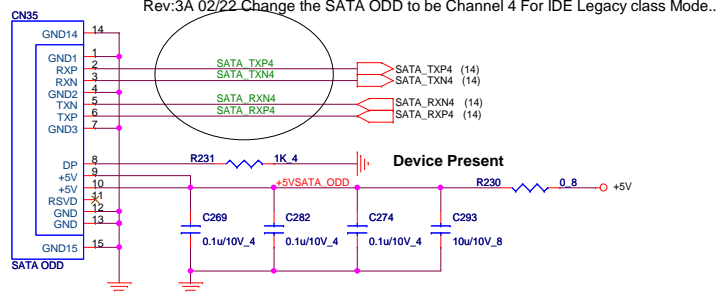


Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

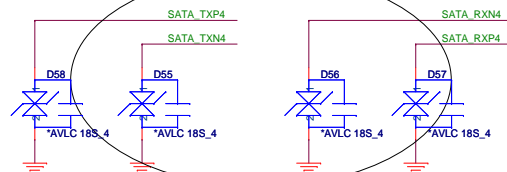


Rev:3B 04/18 Remove D51/D52/D53/D54 Varistor And Change to U44 CM1213-04SO ESD Protection Arrays.

# SATA ODD

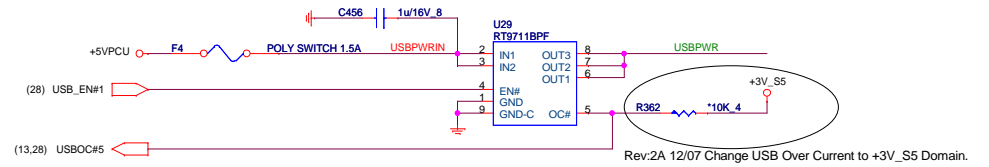


Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode..



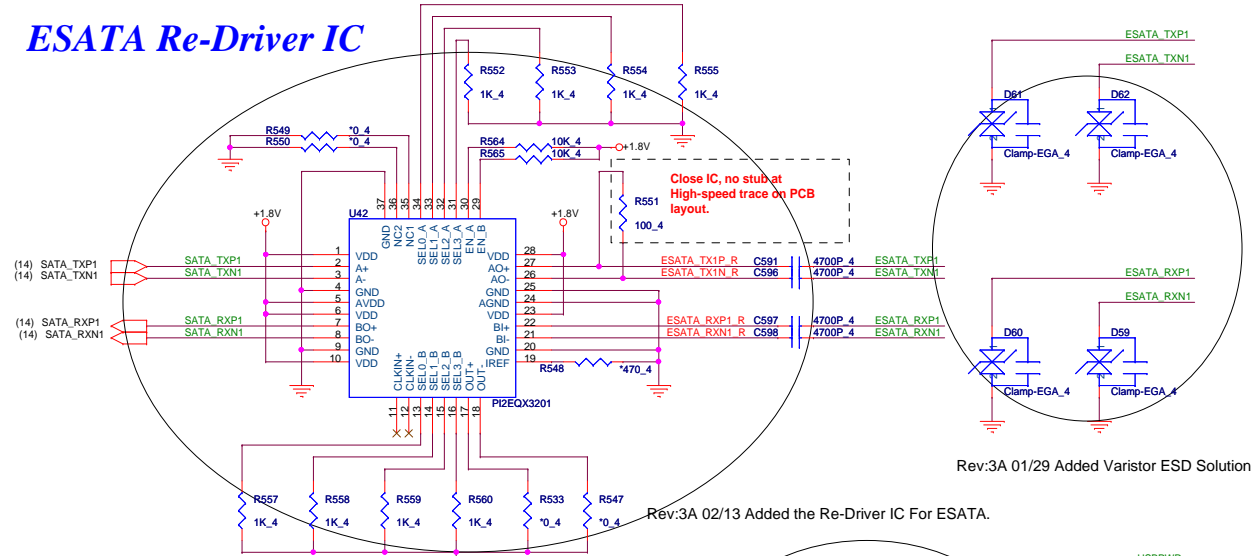
Rev:3A 01/29 Added Varistor ESD Solution.

# USB & ESATA



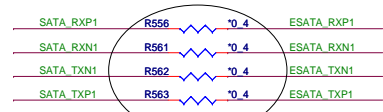
Rev:2A 12/07 Change USB Over Current to +3V\_S5 Domain.

## ESATA Re-Driver IC

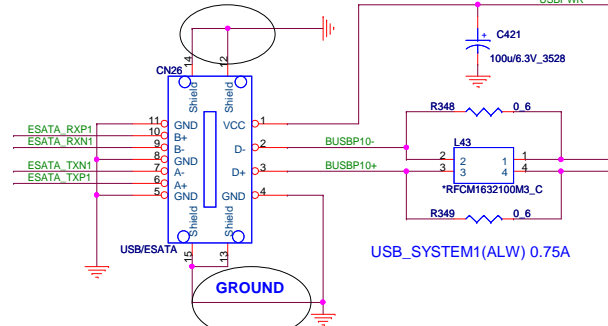


Rev:3A 02/13 Added the Re-Driver IC For ESATA.

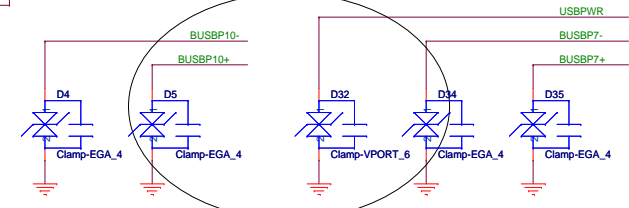
SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				



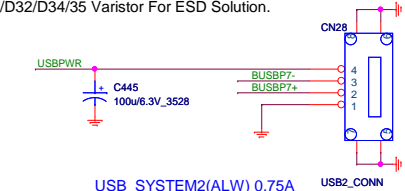
Rev:3A 02/05 Added PIN12/14 To Ground For ESD.



Rev:3A 01/29 Delete R133 For ESD Solution.



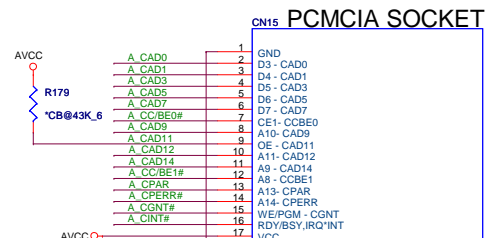
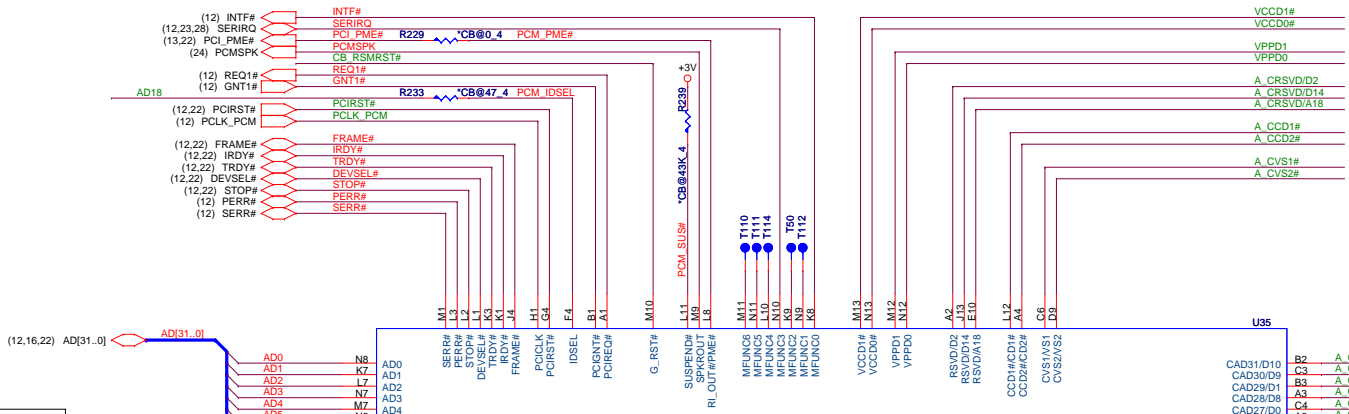
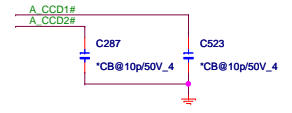
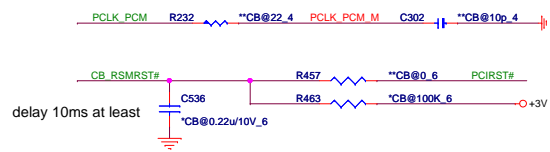
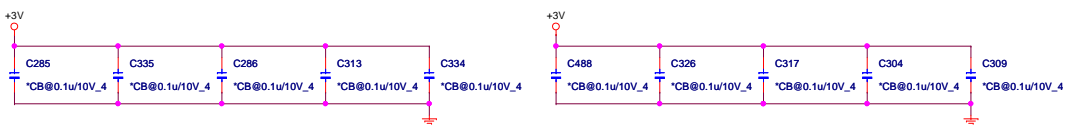
Rev:3A 03/03 Stuff the D4/D5/D32/D34/35 Varistor For ESD Solution.



PROJECT : BU2  
Quantal Computer Inc.

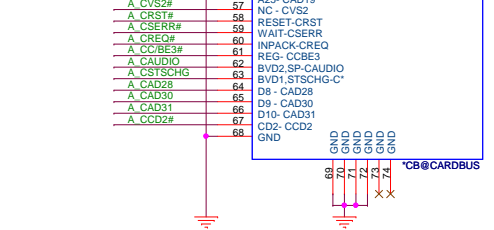
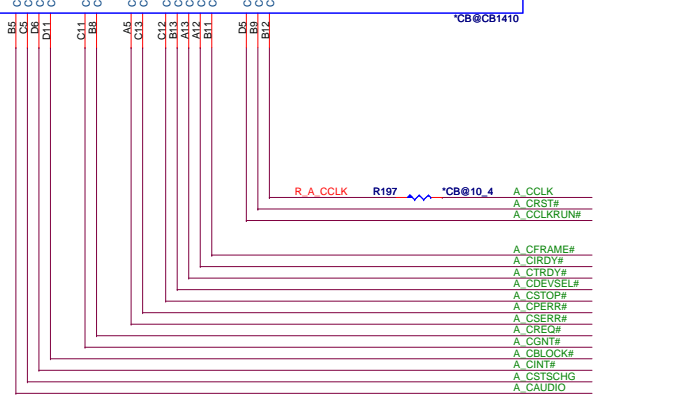
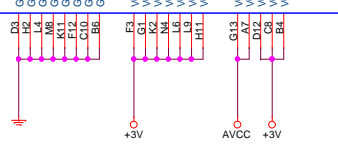
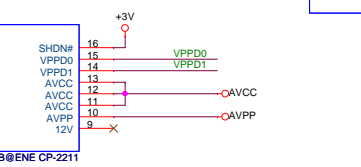
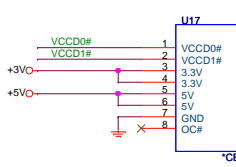
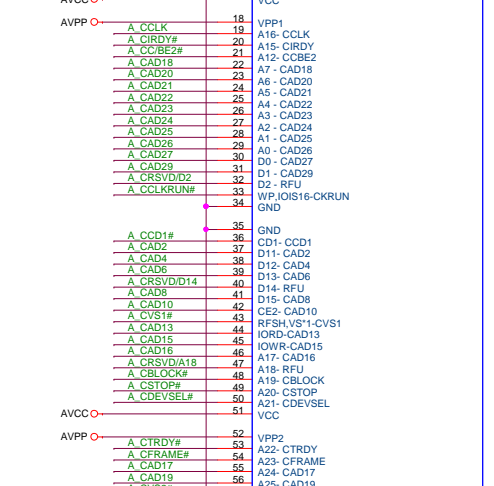
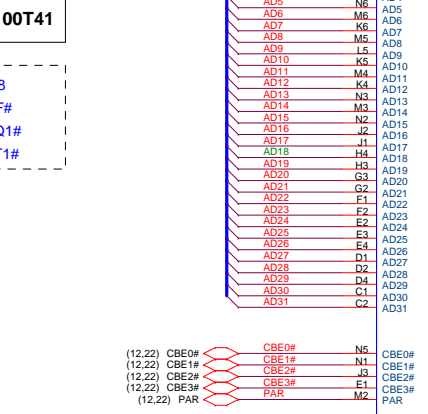
Size Custom	Document Number	Rev 1A
SATA HDD/ODD & ESATA/USB		
Date: Tuesday, August 19, 2008	Sheet 20 of 35	





<b>ENE1410</b>	<b>AJ014100T41</b>
----------------	--------------------

ID Select : AD18  
 Interrupt Pin : INTF#  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#



# CARDBUS

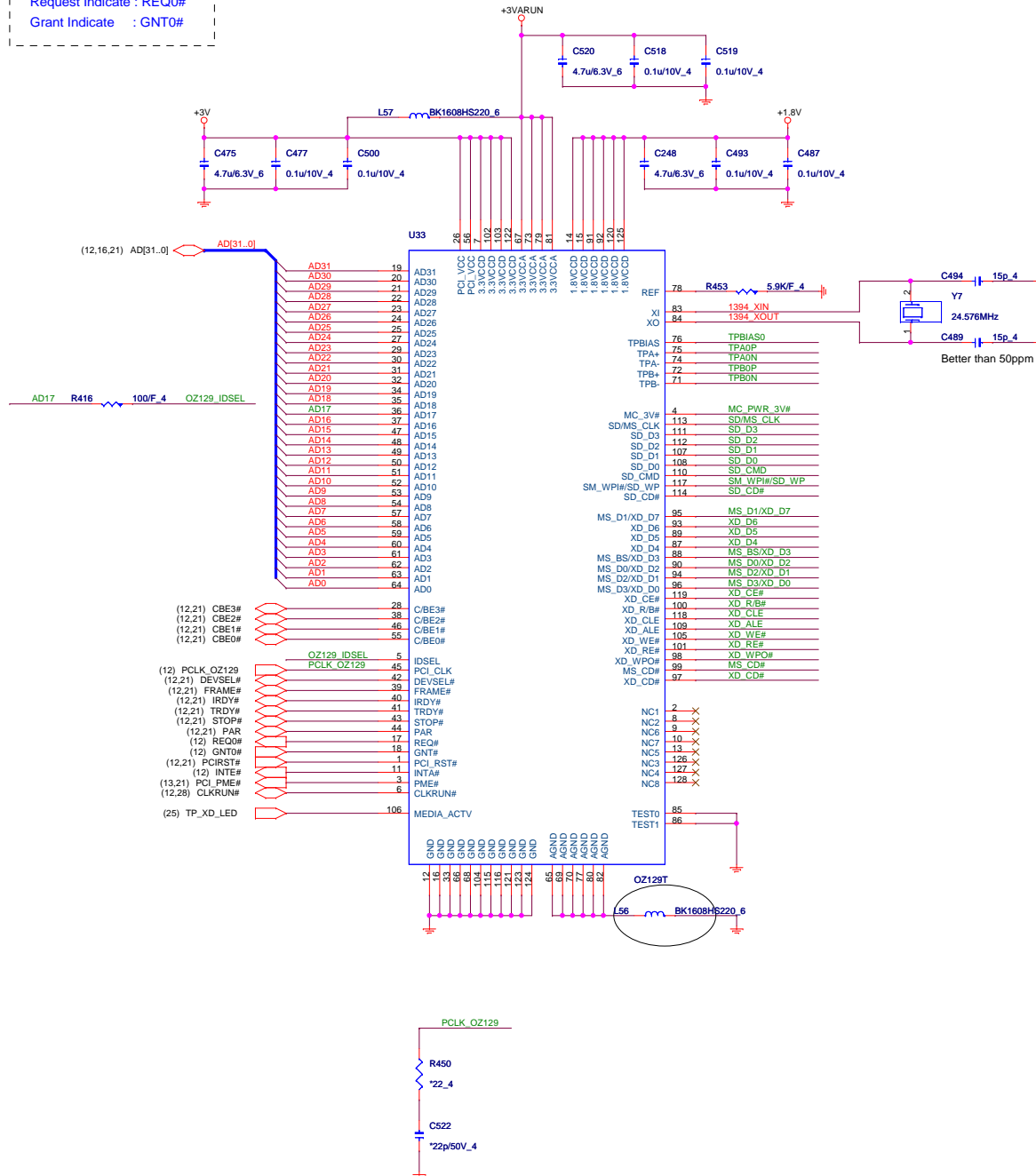
**PROJECT : BU2**  
**Quanta Computer Inc.**

Size Custom    Document Number **PCMCIA(CB1410)-OPTION**    Rev 1A

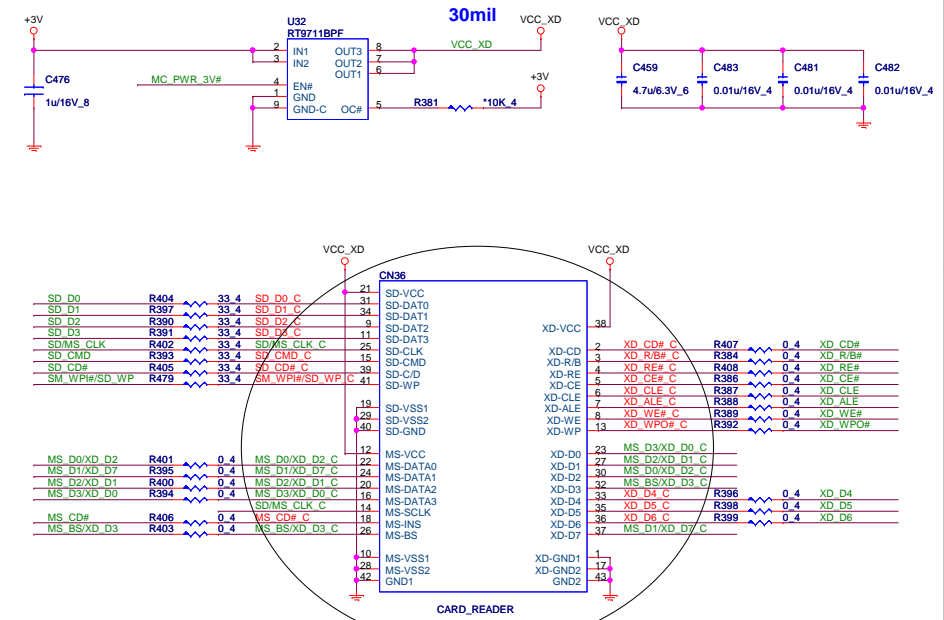
Date: Thursday, July 24, 2008    Sheet 21 of 35

# OZ129 CardReader/1394

ID Select : AD17  
 Interrupt Pin : INTE#  
 Request Indicate : REQ#  
 Grant Indicate : GNT0#

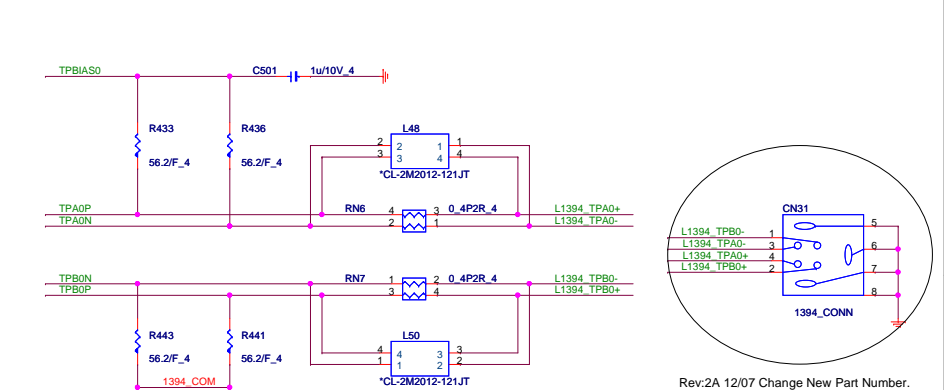


# 5 IN 1 Card Reader



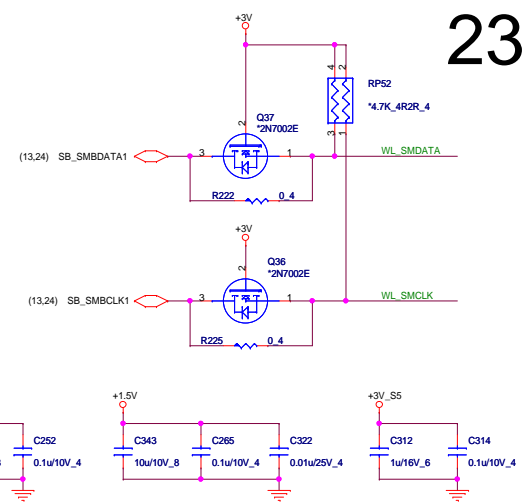
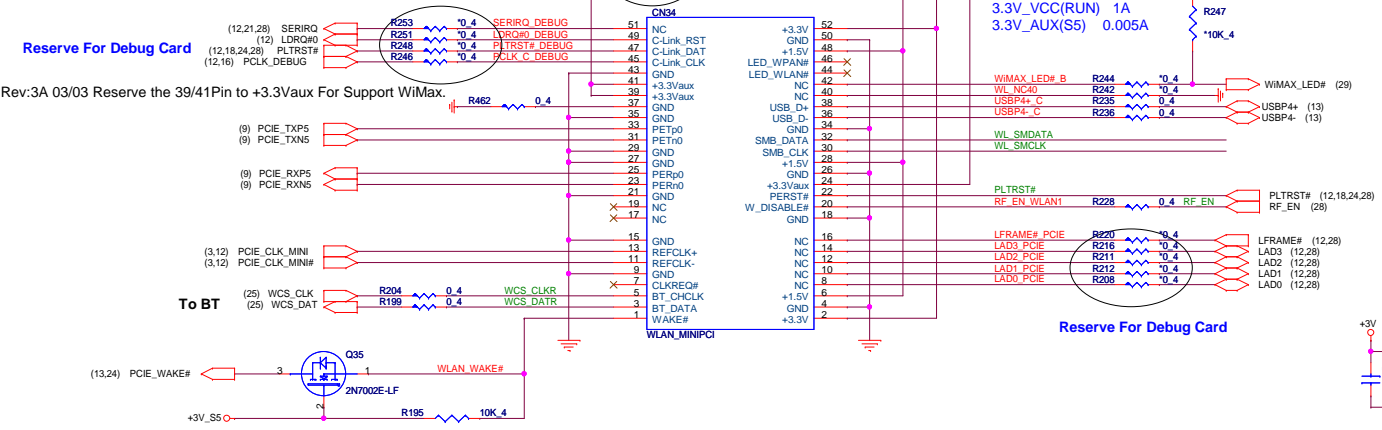
Rev:2A 12/07 Modified the CN36 Footprint For Open Issue.

# 1394

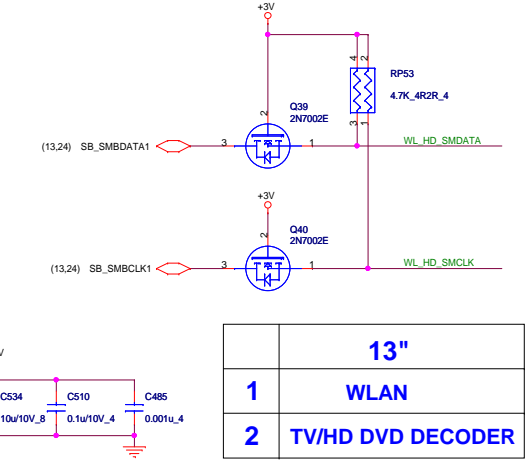
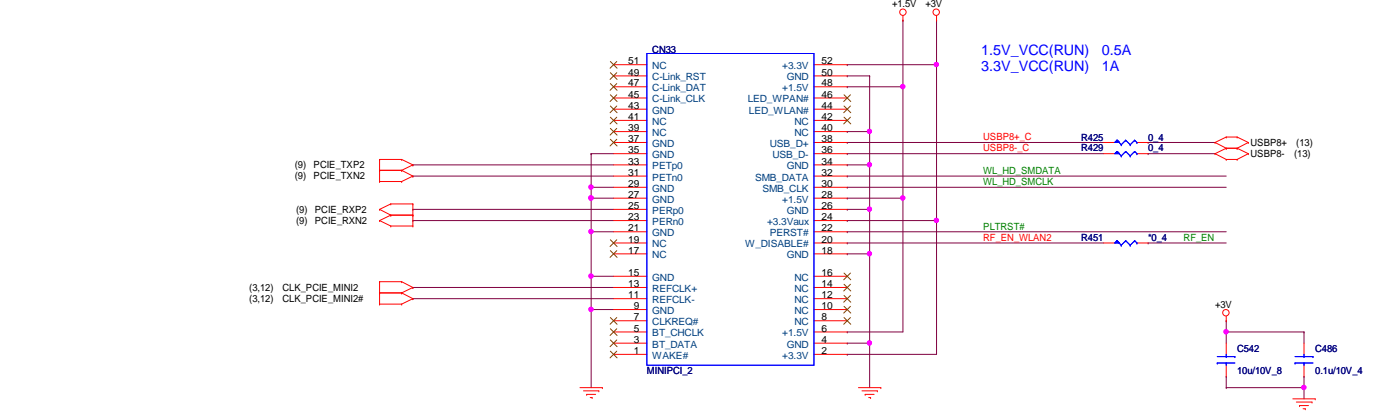


Rev:2A 12/07 Change New Part Number.

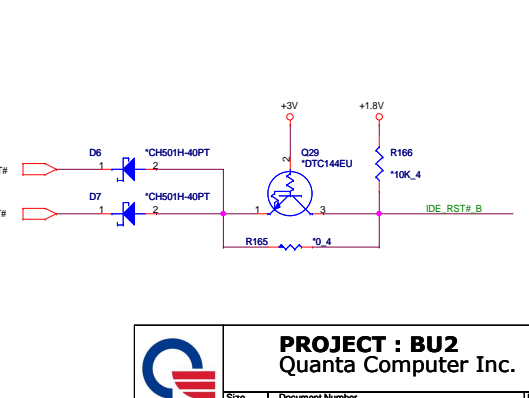
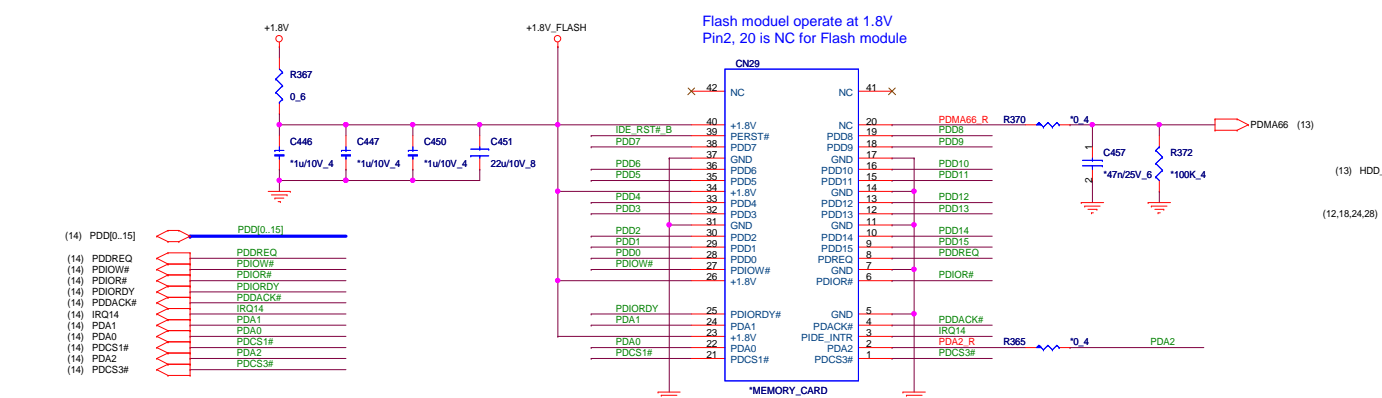
# MINI CARD 1 5.6H\_WLAN



# MINI Card 2 5.6H\_TV/HD DVD DECODER



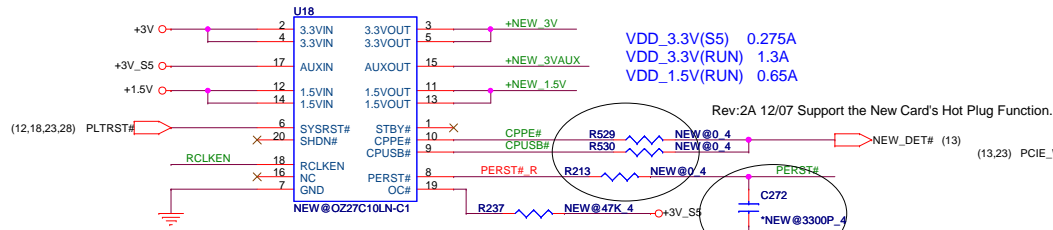
# NAND FLASH MEMORY CARD



**PROJECT : BU2**  
Quanta Computer Inc.

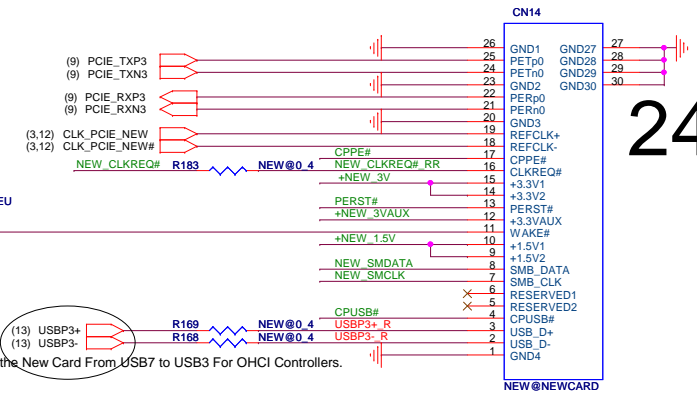
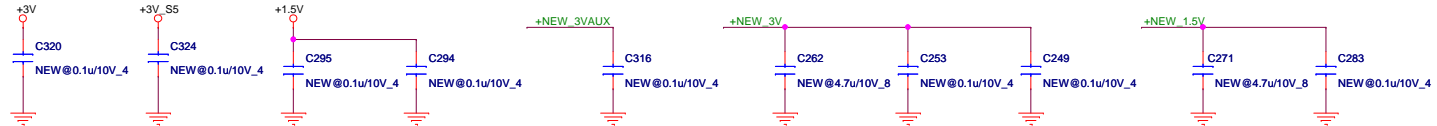
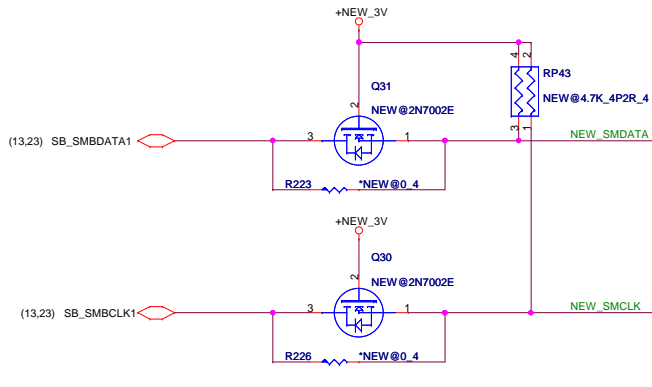
Size Custom	Document Number <b>MINI CARD &amp; NAND FLASH CARD</b>	Rev 1A
Date: Thursday, July 24, 2008 Sheet 23 of 35		

# NEW CARD(BTO)



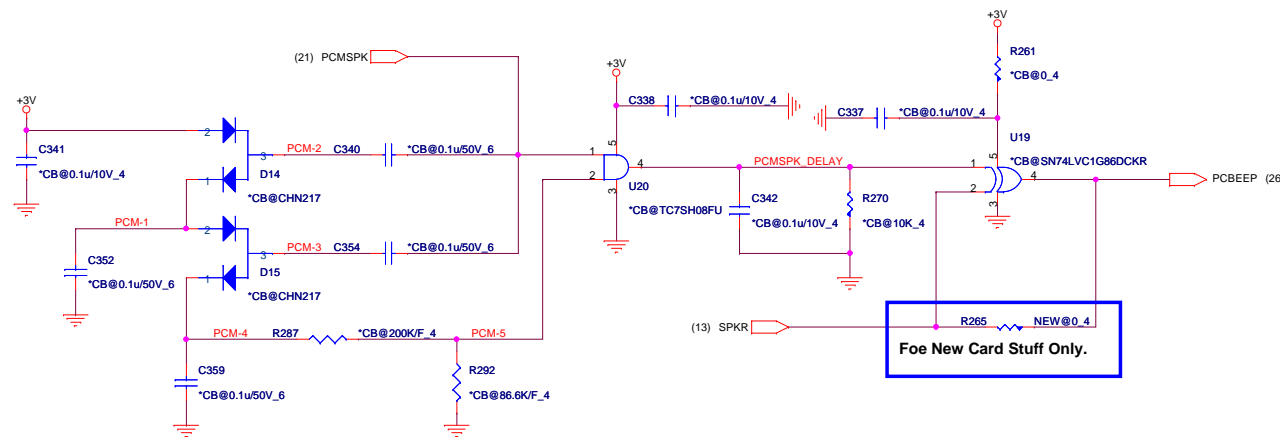
## NEW CARD'S POWER SWITCH

Rev:3A 03/03 As check with AE regarding to PERST# do not add any delay into PERST#



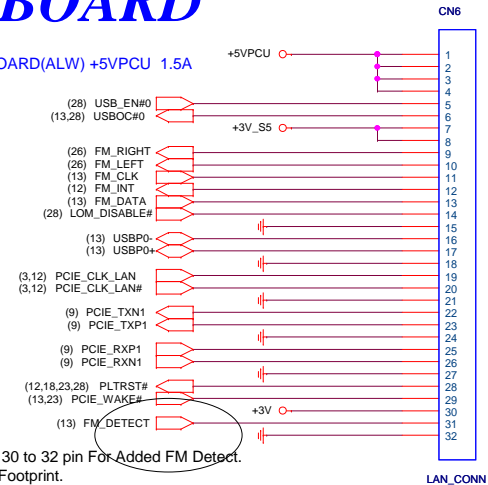
24

# PC-BEEP



# RJ45/USB BOARD

USB & LAN BOARD(ALW) +5VPCU 1.5A

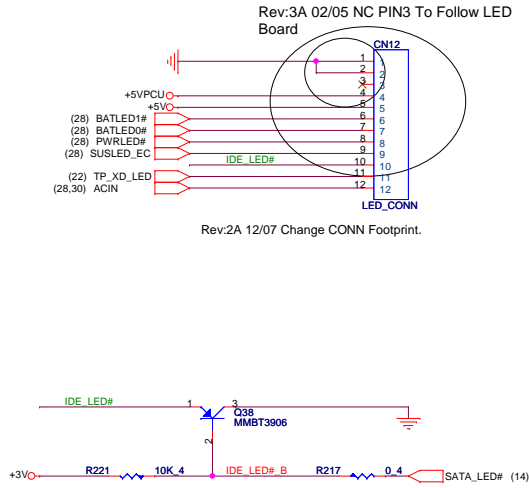


Rev:2A 12/07 Change Connector From 30 to 32 pin For Added FM Detect.  
Rev:3A 02/05 Change Connector PCB Footprint.

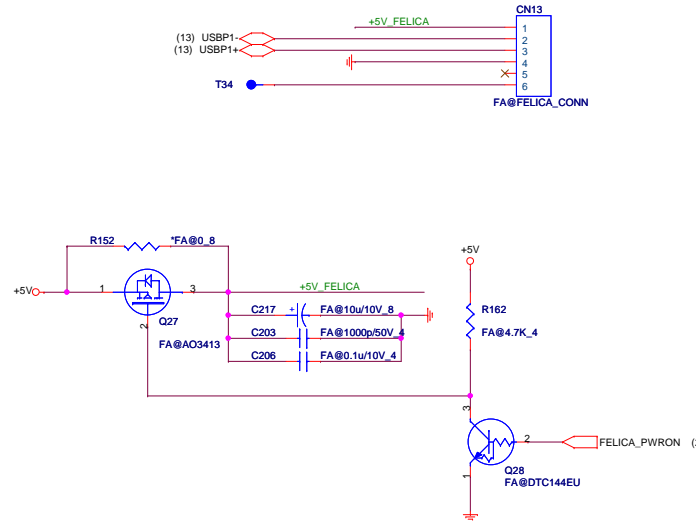
**PROJECT : BU2**  
**Quanta Computer Inc.**

NB4	<p>Size Custom    Document Number <b>NEW CARD &amp; RJ45 BOARD/BEEP</b></p>	Rev 1A
Date: Thursday, July 24, 2008    Sheet 24 of 35		

# LED BOARD

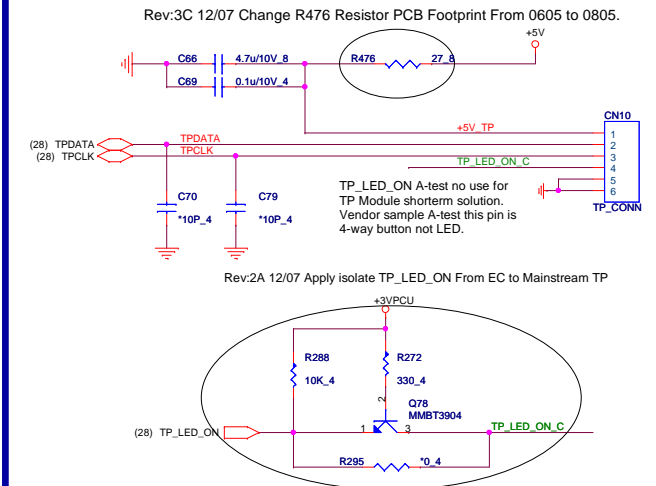


# Felica



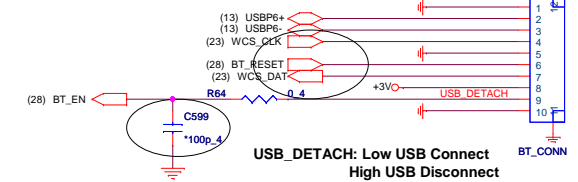
# TP BOARD

25



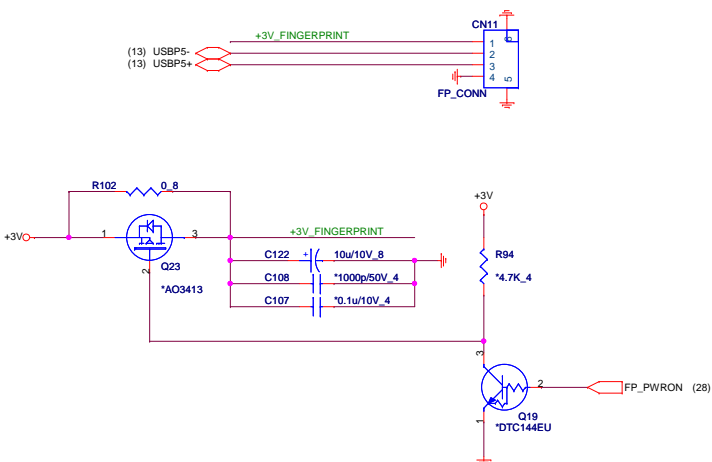
# Bluetooth Module

Rev:3D 07/23 Remove R59 and Added control BT Reset by EC GPIO77



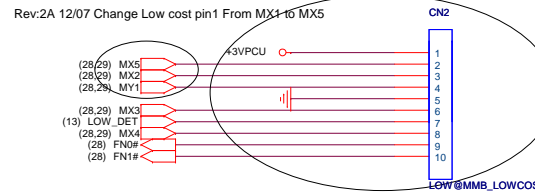
Rev:3A 03/03 Reserve C599 Capacitors to Bluetooth Enable For EMI..

# FINGER-PRINT



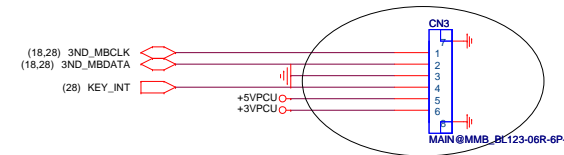
# MMB

Low cost

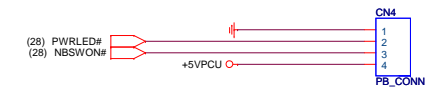


Rev:2A 12/07 Change CONN Footprint.

Main stream



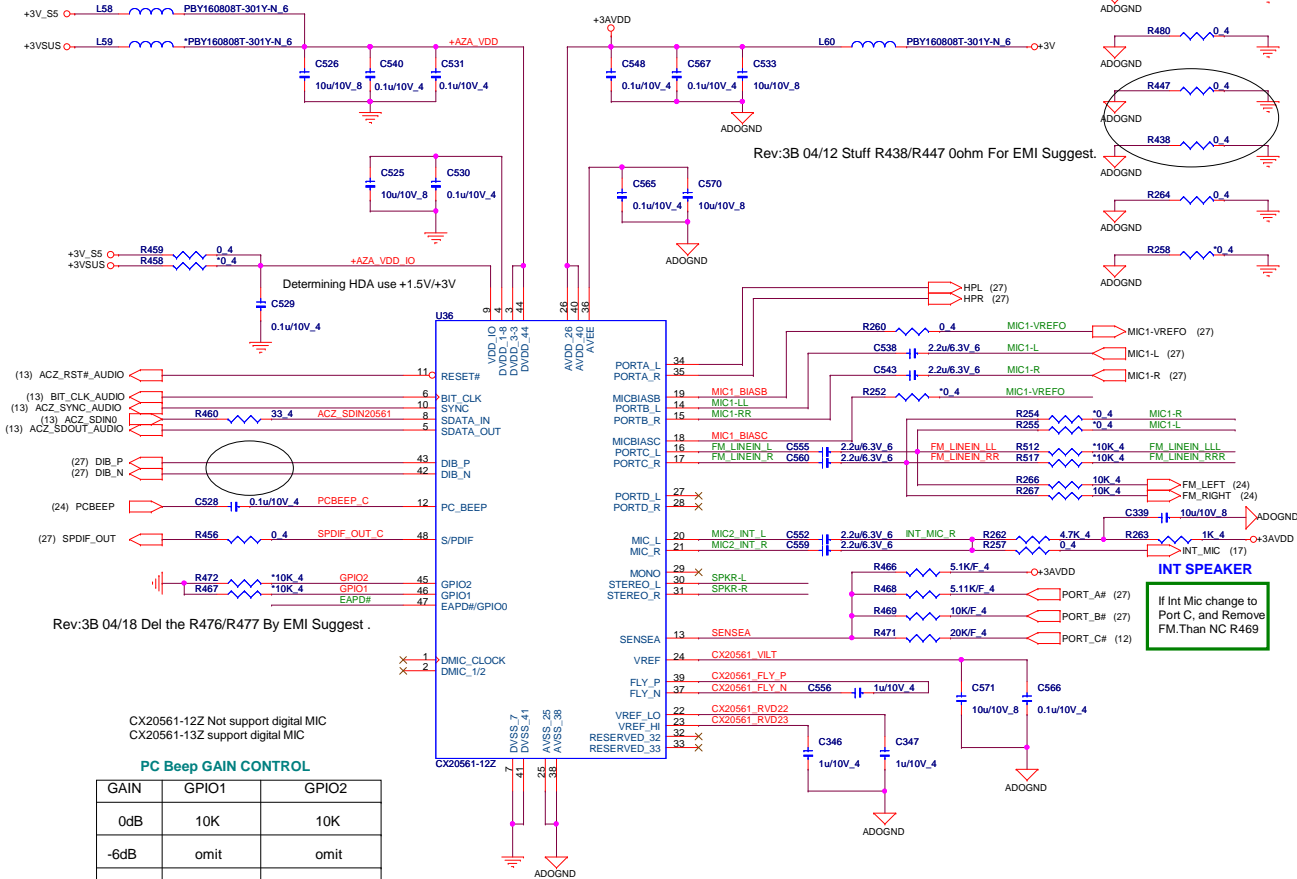
# POWER BOARD



	<b>PROJECT : BU2</b>		Rev 1A
	Quantia Computer Inc.		
Size Custom	Document Number	TP/FP/BT/PB/FELICA/MMB CONN	Sheet 25 of 35
NB4	Date: Tuesday, August 19, 2008		

# CODEC(CX20561)

Rev:3A 02/05 Added the EMI Solution.

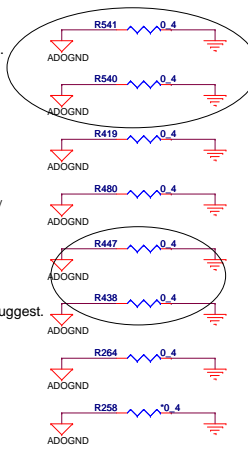


Rev:3B 04/18 Del the R476/R477 By EMI Suggest .

### PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

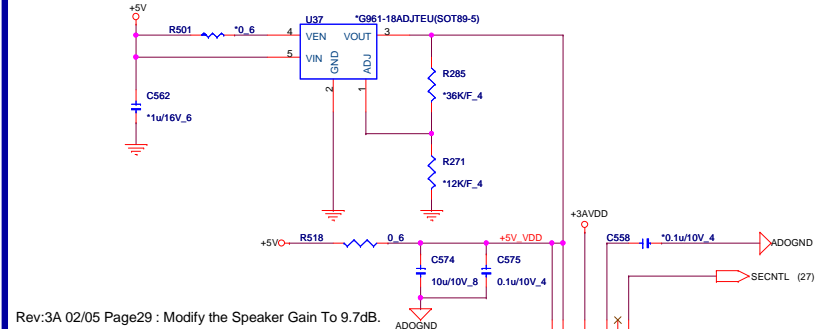
Rev:3B 04/12 Stuff R438/R447 Ohm For EMI Suggest.



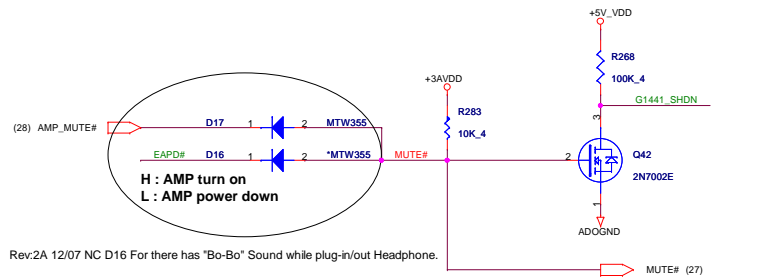
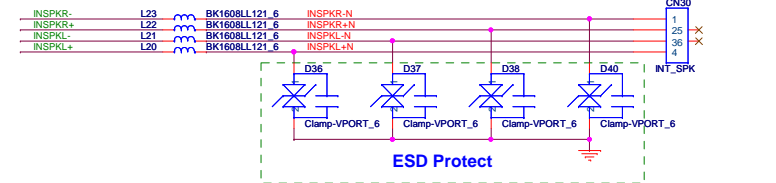
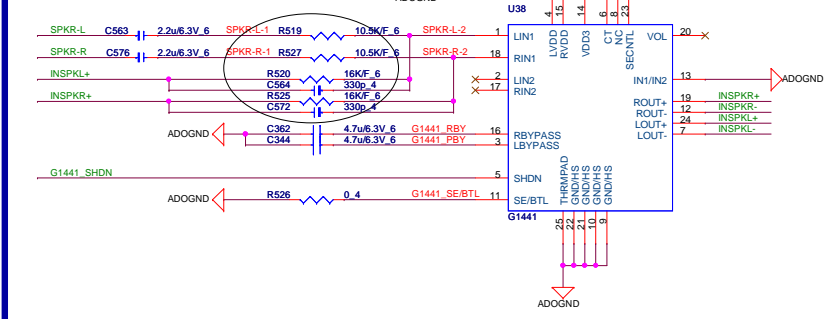
### INT SPEAKER

If Int Mic change to Port C, and Remove FM. Than NC R469

# INT SPK AMP

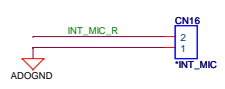


Rev:3A 02/05 Page29 : Modify the Speaker Gain To 9.7dB.

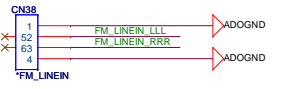


Rev:2A 12/07 NC D16 For there has "Bo-Bo" Sound while plug-in/out Headphone.

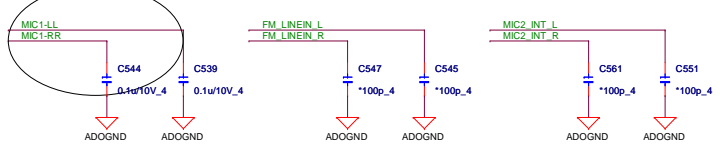
### Reserve INTMIC



### Reserve FM



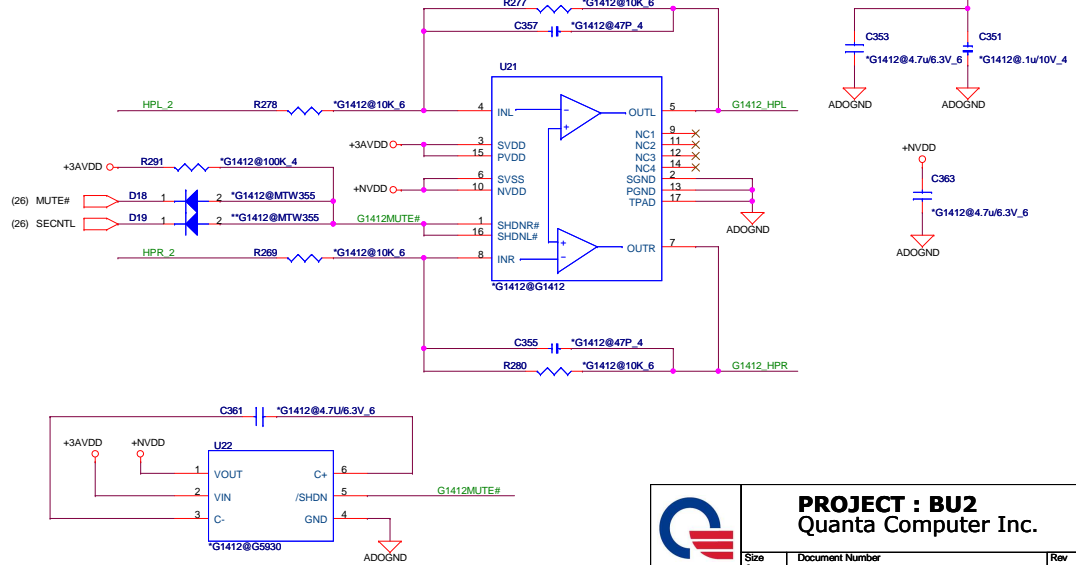
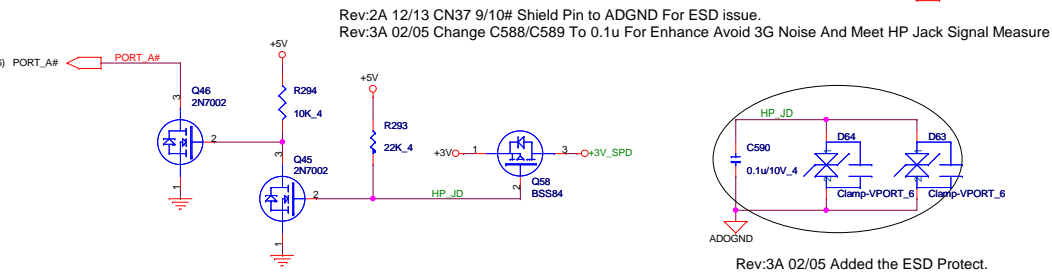
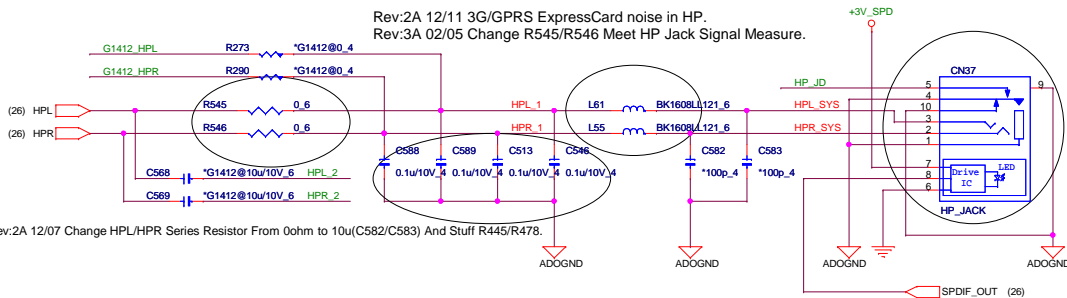
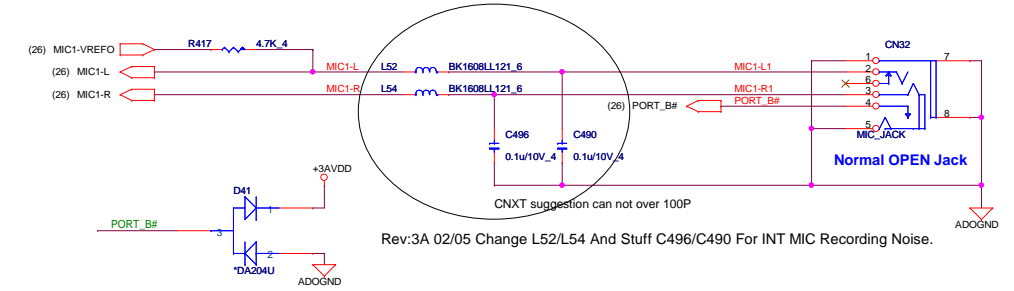
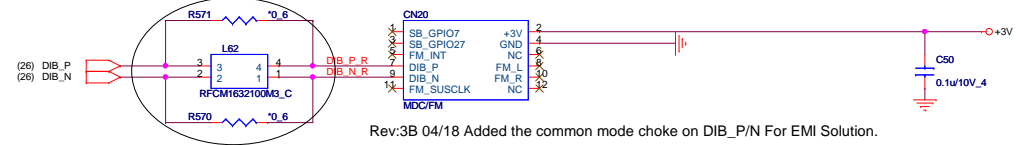
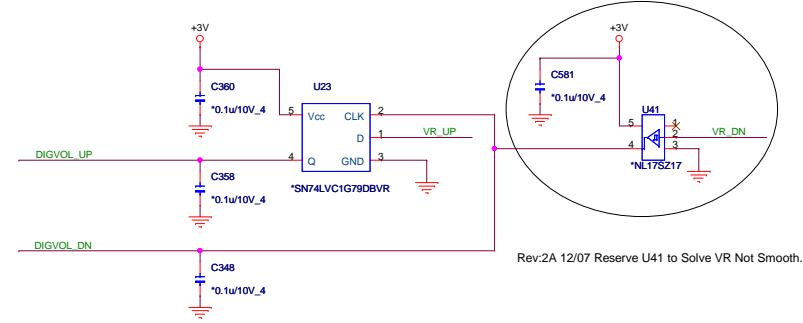
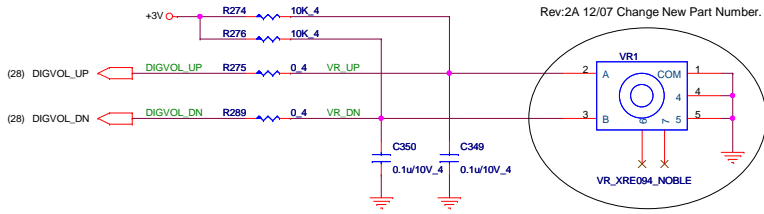
Rev:3A 02/05 Stuff C539/C544 For INT MIC Recording Noise.

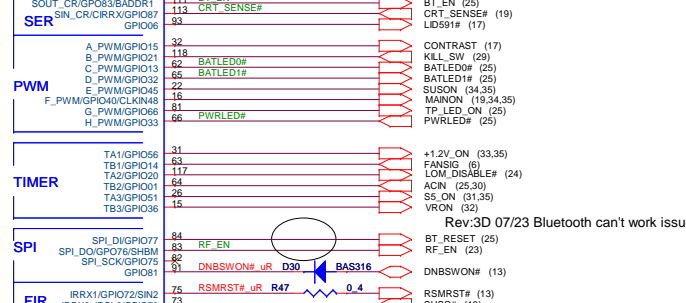
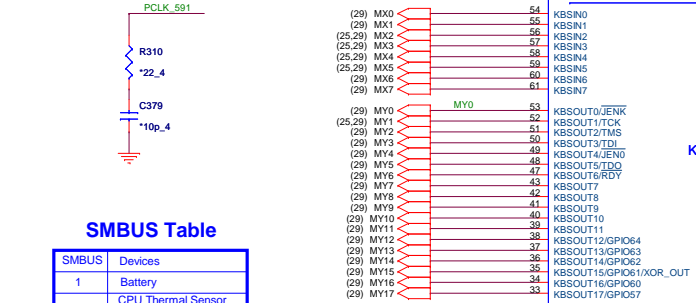
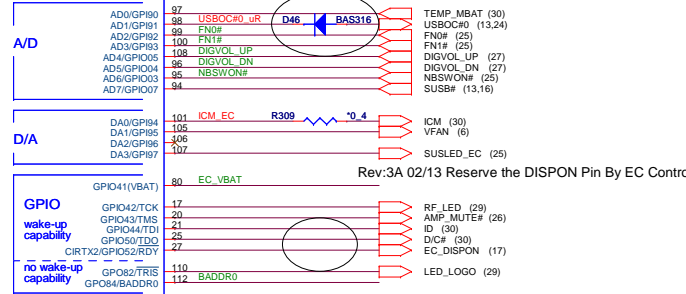
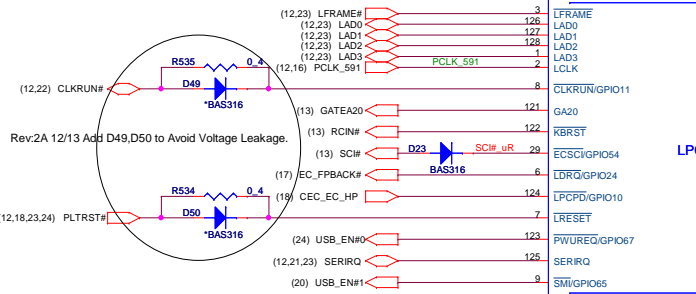
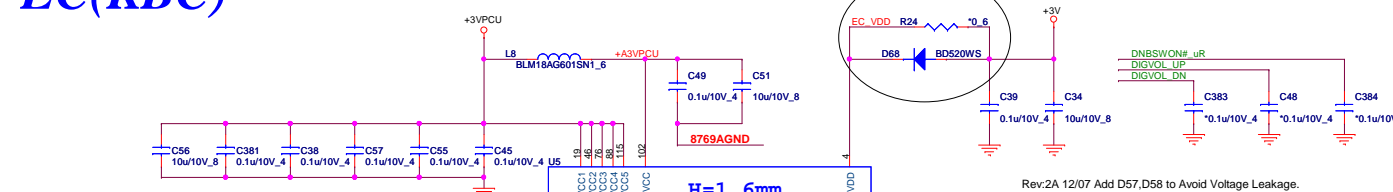
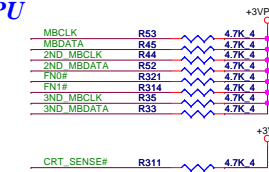


**PROJECT : BU2**  
**Quanta Computer Inc.**

Size Custom	Document Number CONEXANT(CX205601)/SPK/AMP	Rev 1A
Date: Thursday, July 24, 2008   Sheet 26 of 35		

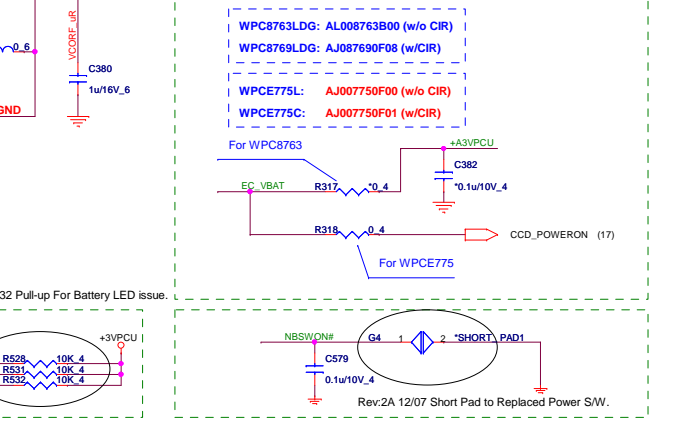
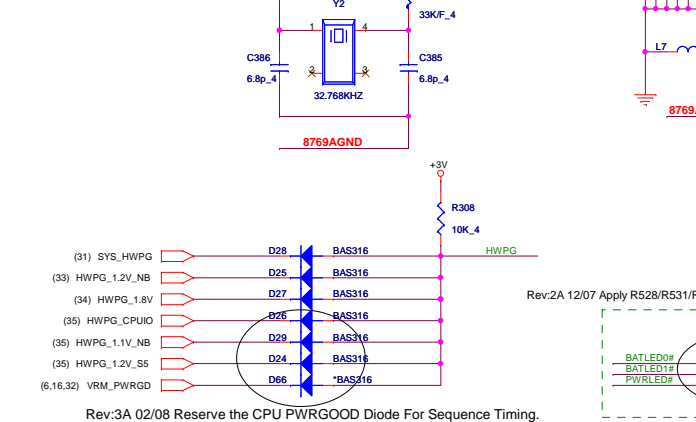
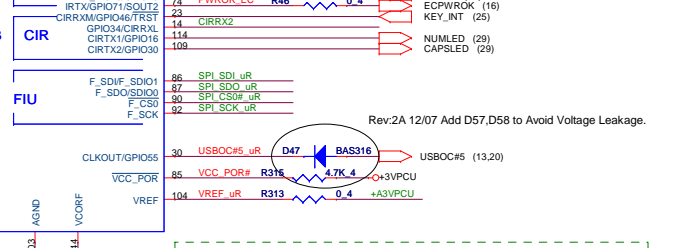
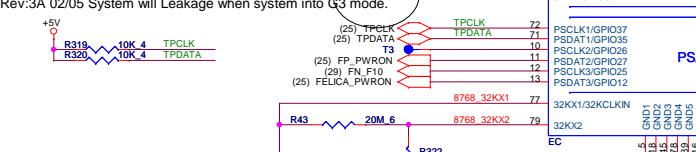






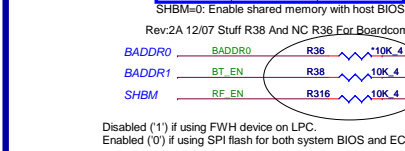
### SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	HDMI CEC Touch Sensor

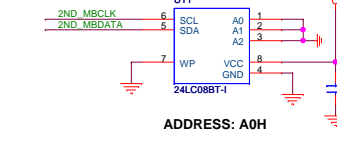


## I/O Base Address

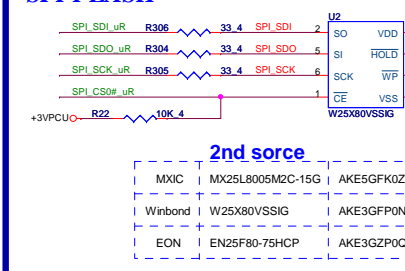
BADDR1-0	Index	Data
0 0		XOR TREE TEST MODE
0 1		CORE DEFINED
1 0	2Eh	2Fh
1 1	164Eh	164Fh



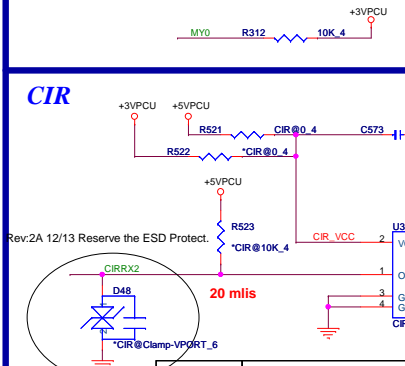
## ID



## SPI FLASH



## INTERNAL KEYBOARD STRIP SET



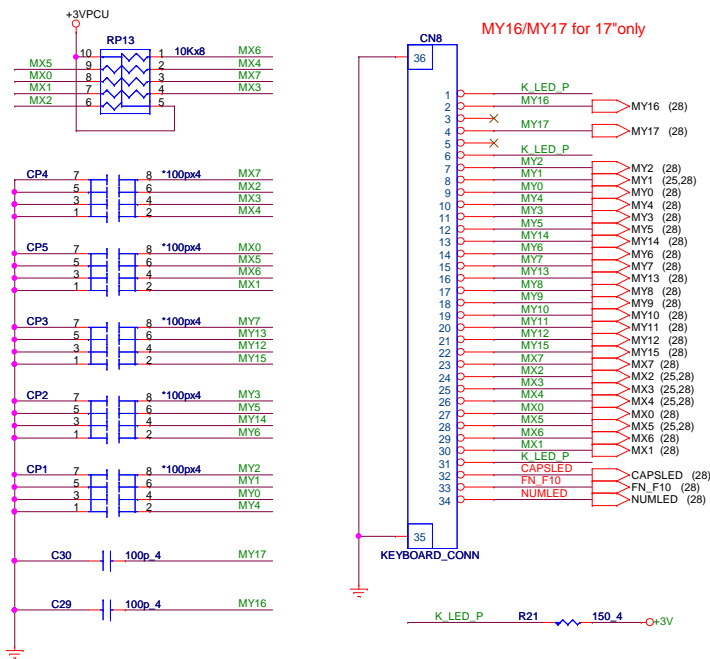
**PROJECT : BU2**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>EC(KBC)-WPCPC8763/WPC8769</b>	Rev 1A
Date: Friday, August 01, 2008   Sheet 28 of 35		

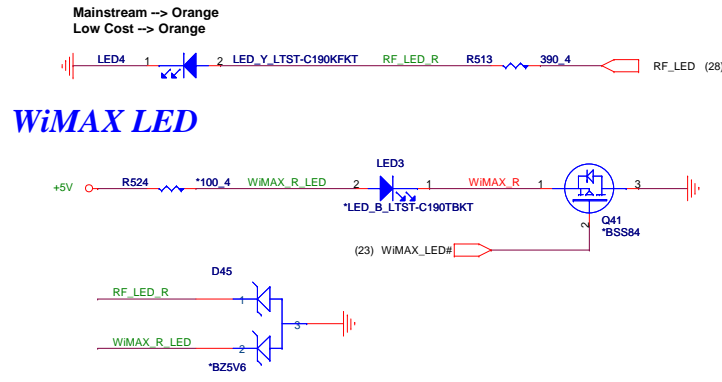
Rev:3A 02/08 Reserve the CPU PWRGOOD Diode For Sequence Timing.

Rev:2A 12/07 Short Pad to Replaced Power SW.

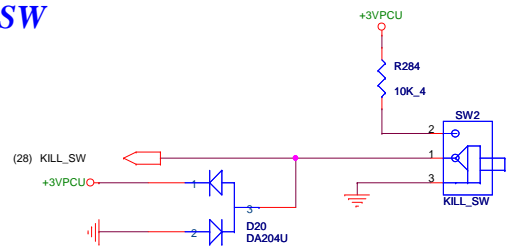
# INT KEYBOARD



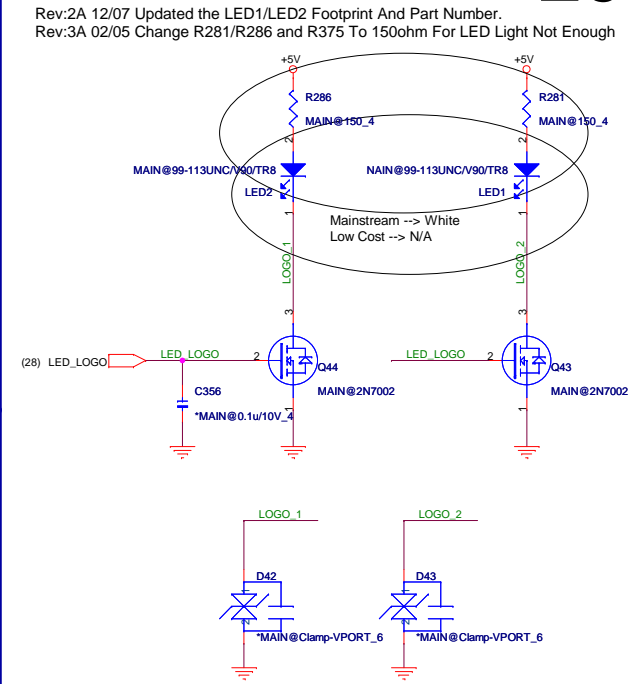
# W-LAN&BT LED



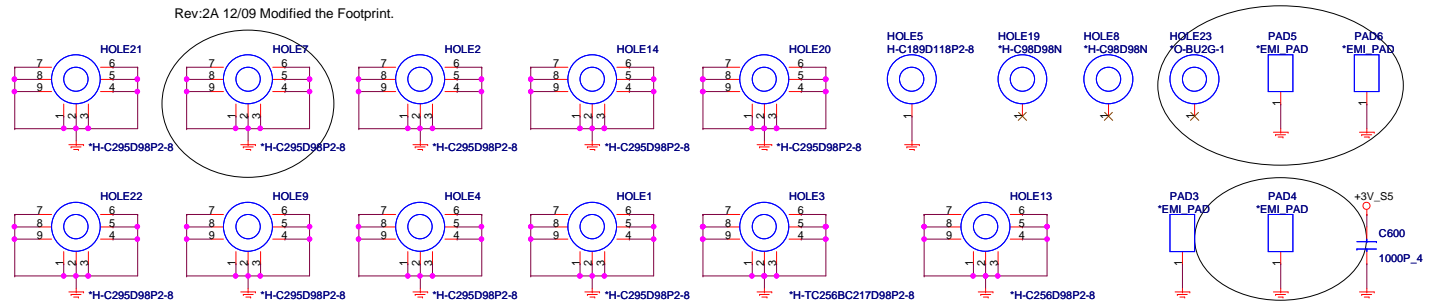
# KILL SW



# Satellite LED

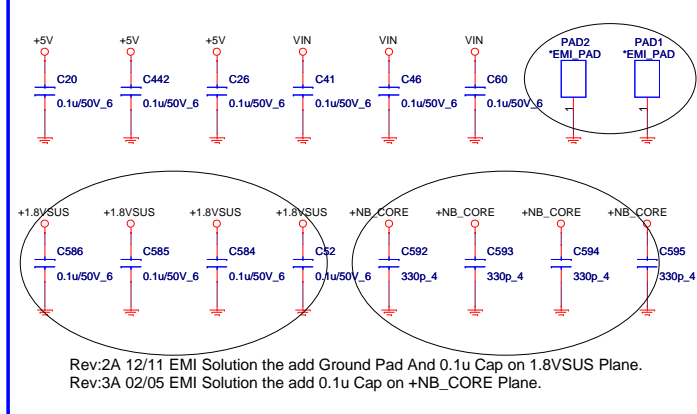


# HOLE



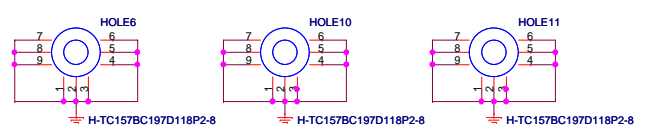
Rev:3B 04/18 ESD Solution the Added the Ground Pad.

# EMI

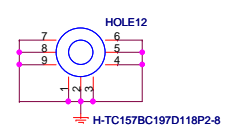


Rev:2A 12/11 EMI Solution the add Ground Pad And 0.1u Cap on 1.8VSUS Plane.  
Rev:3A 02/05 EMI Solution the add 0.1u Cap on +NB\_CORE Plane.

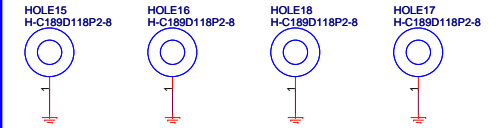
# CPU



# NB

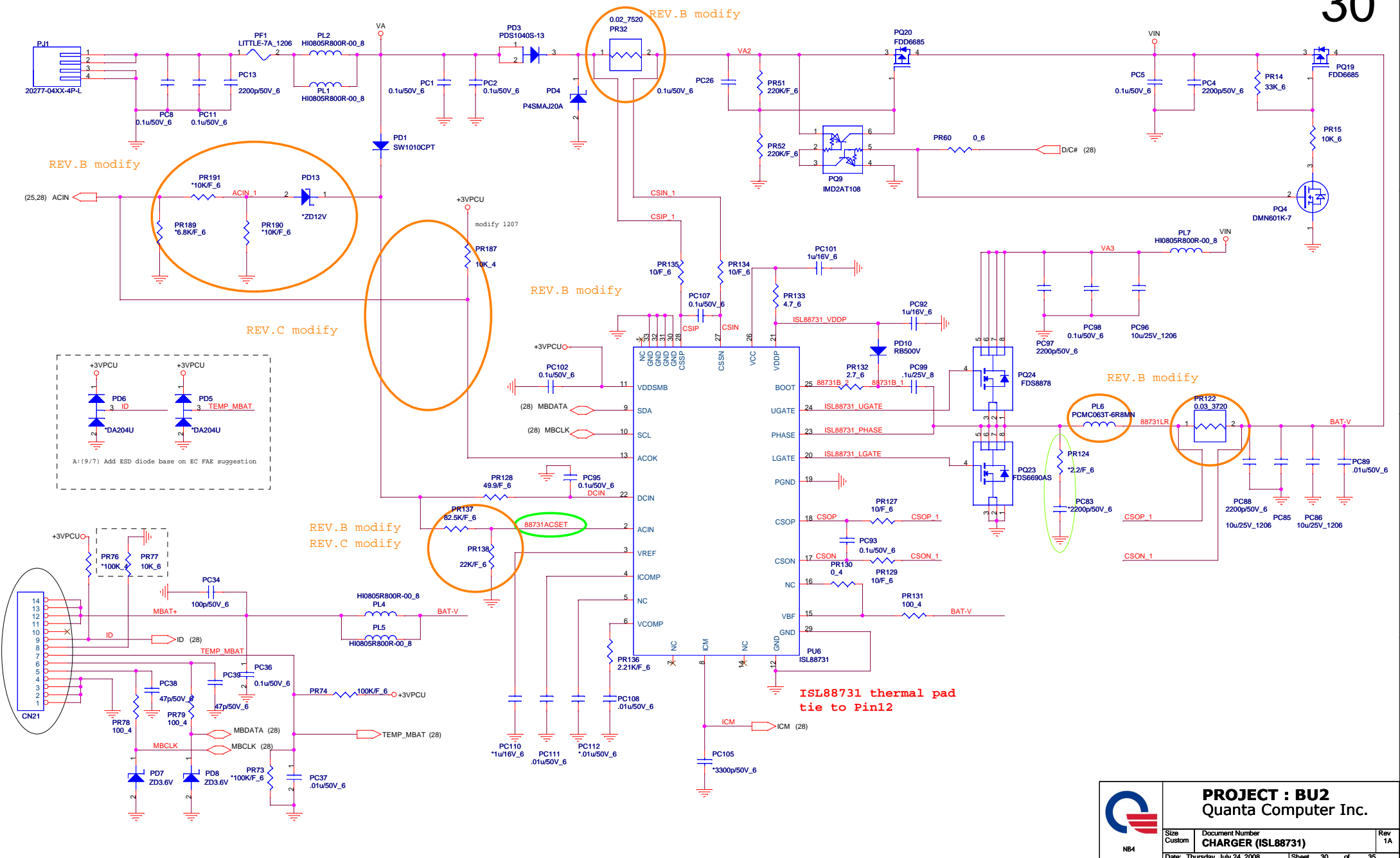



# MINI CARD



**PROJECT : BU2**  
Quanta Computer Inc.

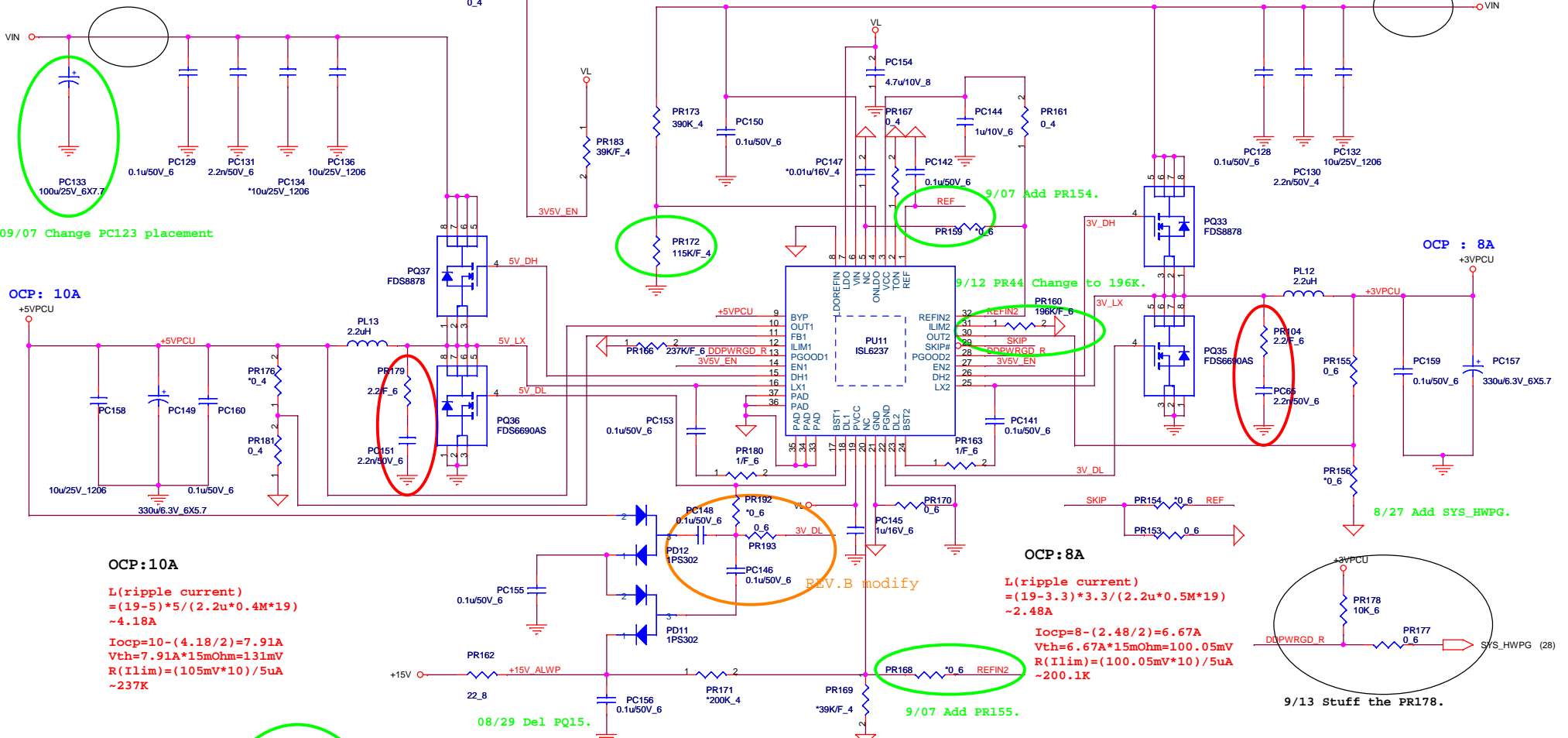
Size Custom	Document Number	Rev 1A
Date: Thursday, July 24, 2008	<b>KEYBOARD/LED/KILL SW/HOLE</b>	Sheet 29 of 35



 NB4	<b>PROJECT : BU2</b> <b>Quanta Computer Inc.</b>	
	Size Custom Document Number <b>CHARGER (ISL88731)</b>	Rev 1A
Date: Thursday, July 24, 2008   Sheet 30 of 35		



Rev:2A 12/12 Move the Short Pad.



OCP: 10A

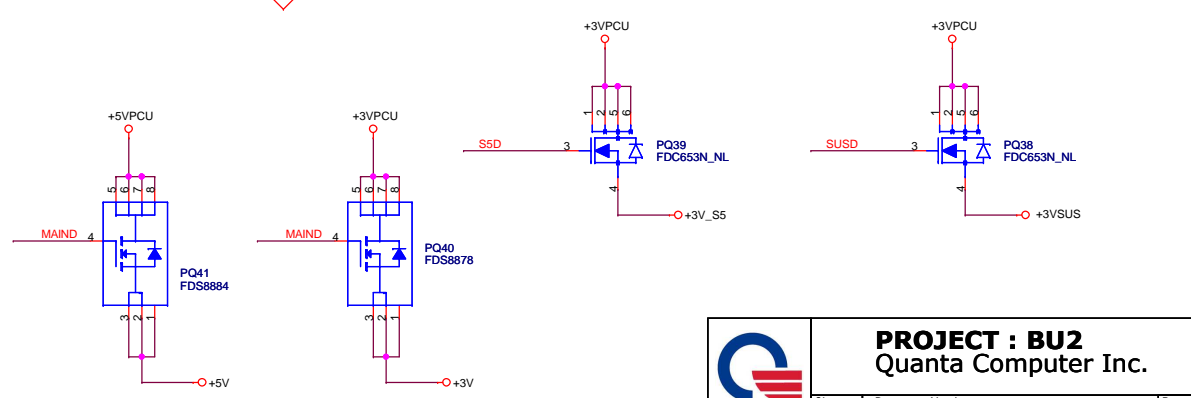
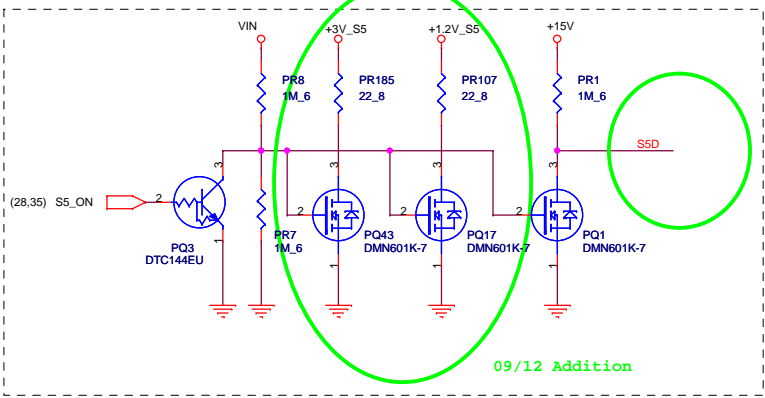
L(ripple current)  
 $= (19-5) * 5 / (2.2u * 0.4M * 19)$   
 $\sim 4.18A$

$I_{ocp} = 10 - (4.18 / 2) = 7.91A$   
 $V_{th} = 7.91A * 15mOhm = 131mV$   
 $R(I_{lim}) = (105mV * 10) / 5uA$   
 $\sim 237K$

OCP: 8A

L(ripple current)  
 $= (19-3.3) * 3.3 / (2.2u * 0.5M * 19)$   
 $\sim 2.48A$

$I_{ocp} = 8 - (2.48 / 2) = 6.67A$   
 $V_{th} = 6.67A * 15mOhm = 100.05mV$   
 $R(I_{lim}) = (100.05mV * 10) / 5uA$   
 $\sim 200.1K$



	<b>PROJECT : BU2</b>		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	SYSTEM 5V/3V (ISL6237)	
NB4	Date: Thursday, July 24, 2008	Sheet 31 of 35	

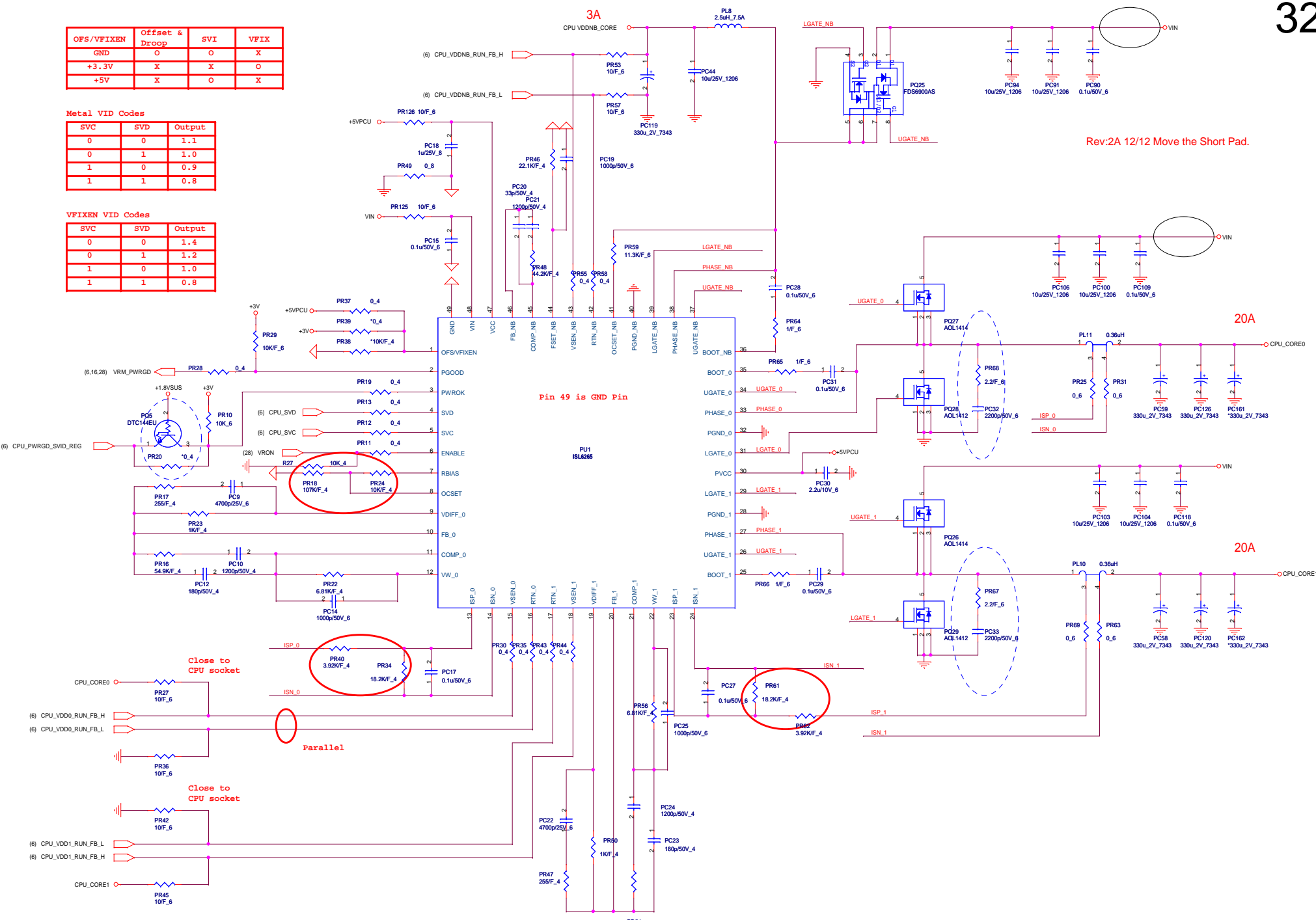
OFS/VFIXEN	Offset & Droop	SVC	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

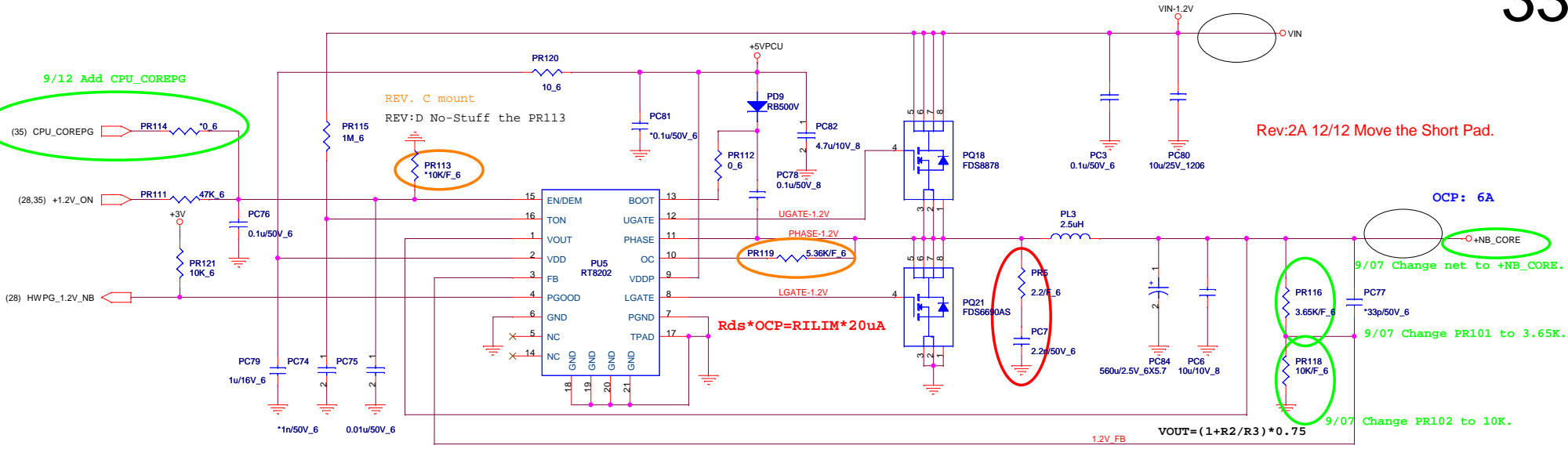
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8







9/12 Add CPU\_COREPG  
(35) CPU\_COREPG → PR114 10K\_6

REV. C mount  
REV:D No-Stuff the PR113

Rev:2A 12/12 Move the Short Pad.

OCP: 6A

9/07 Change net to +NB\_CORE.

9/07 Change PR101 to 3.65K.

9/07 Change PR102 to 10K.

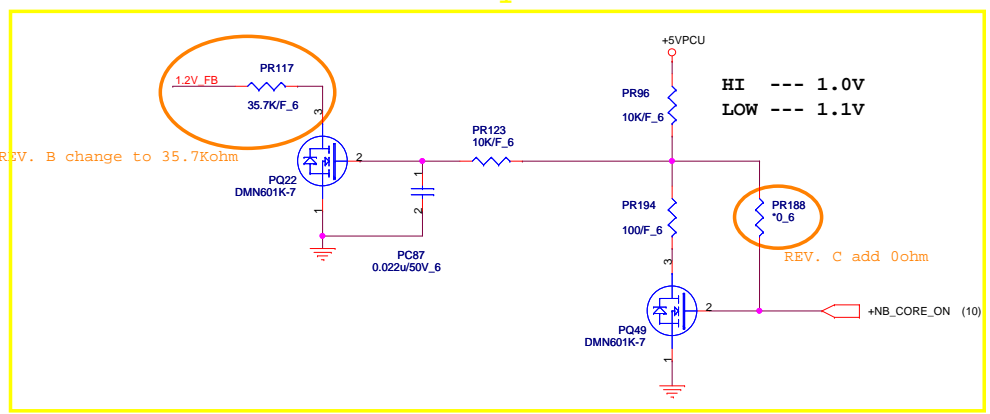
$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$   
 $Frequency = V_{out} / (V_{in} * T_{ON})$

6A OCP --- OC=4.53K  
 FDS6690AS Rds=15mOhm

REV. C PR119 change to 5.36Kohm

$V_{OUT} = (1 + R2/R3) * 0.75$

1/30 modify



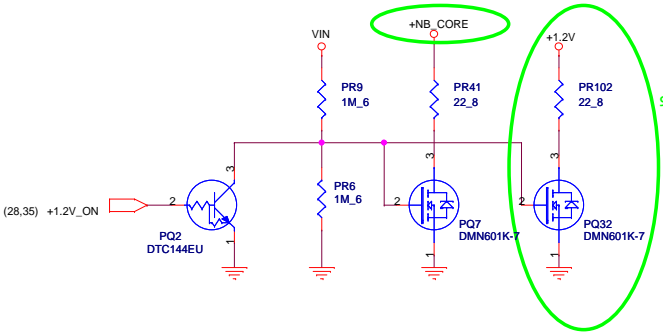
REV. B change to 35.7Kohm

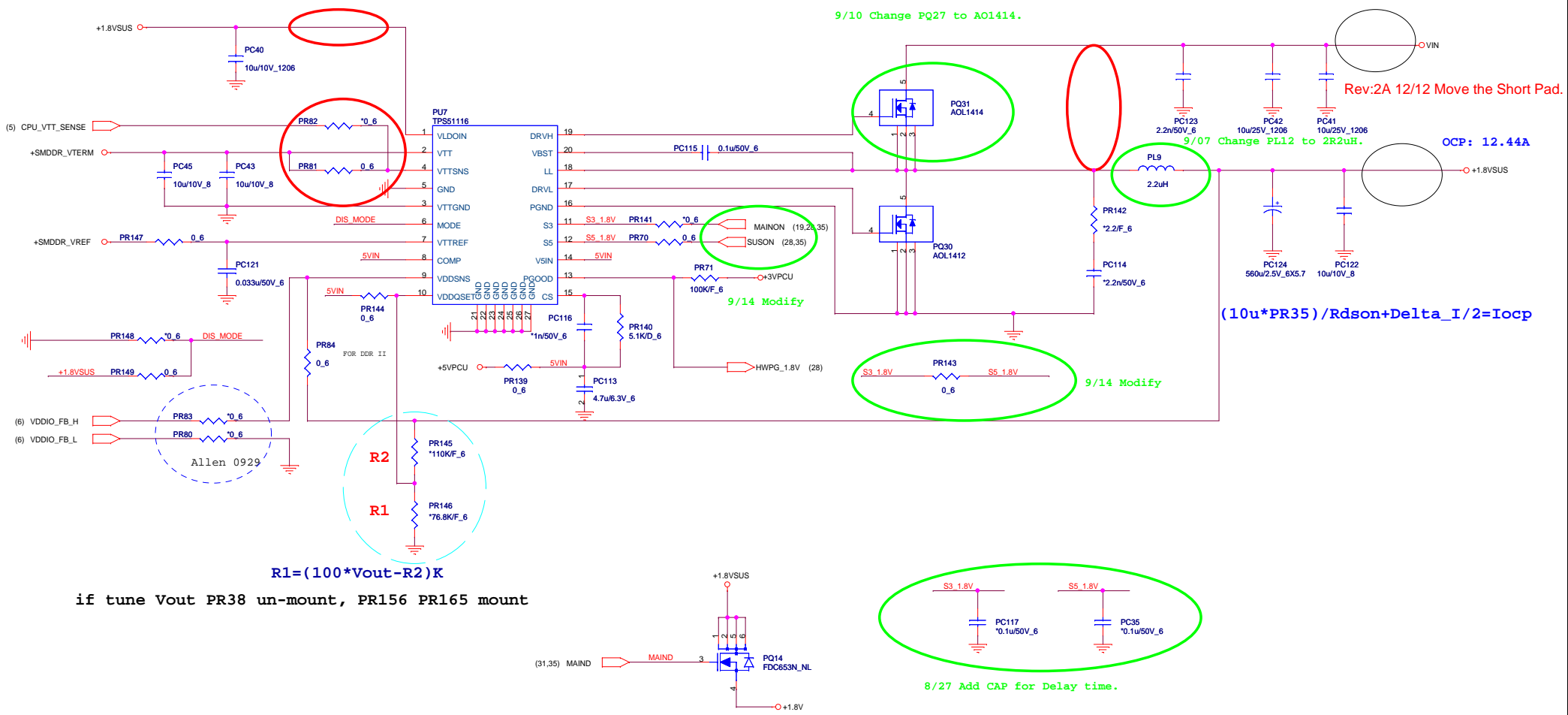
HI --- 1.0V  
 LOW --- 1.1V

REV. C add 0ohm

9/07 Change net to +NB\_CORE.

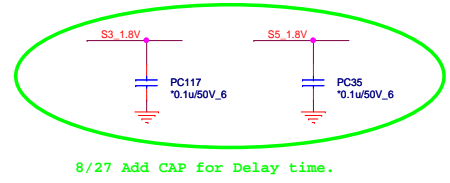
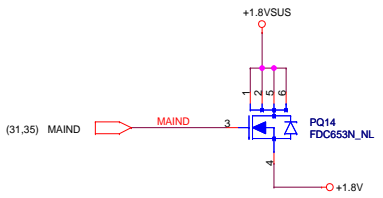
9/12 Addition PR156, PQ43.

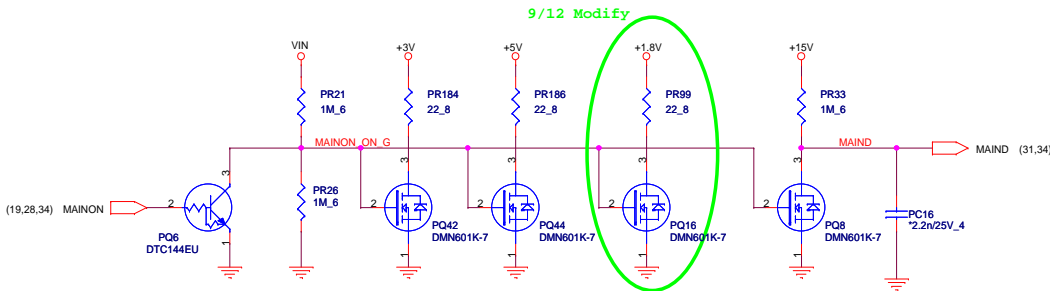
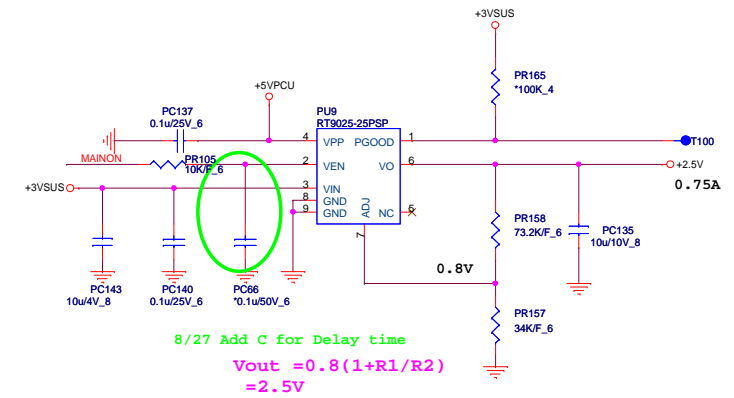
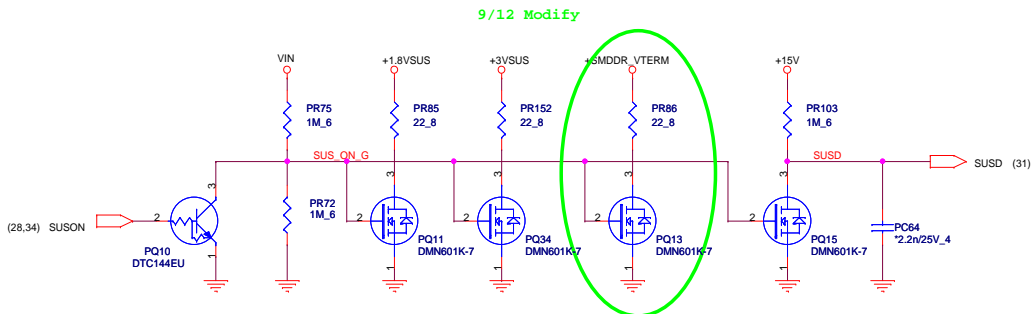
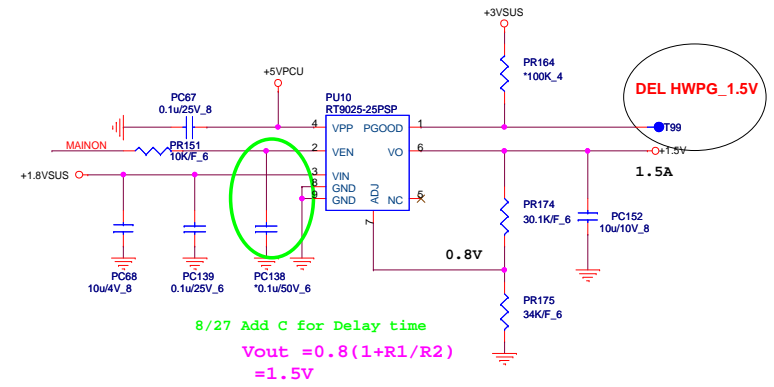
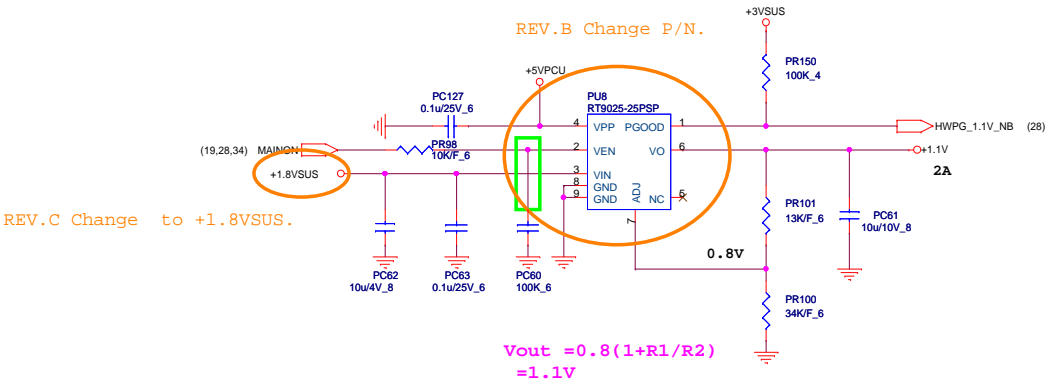
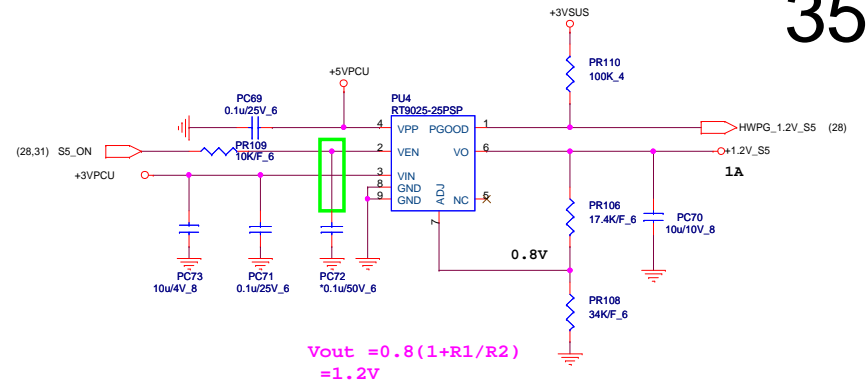
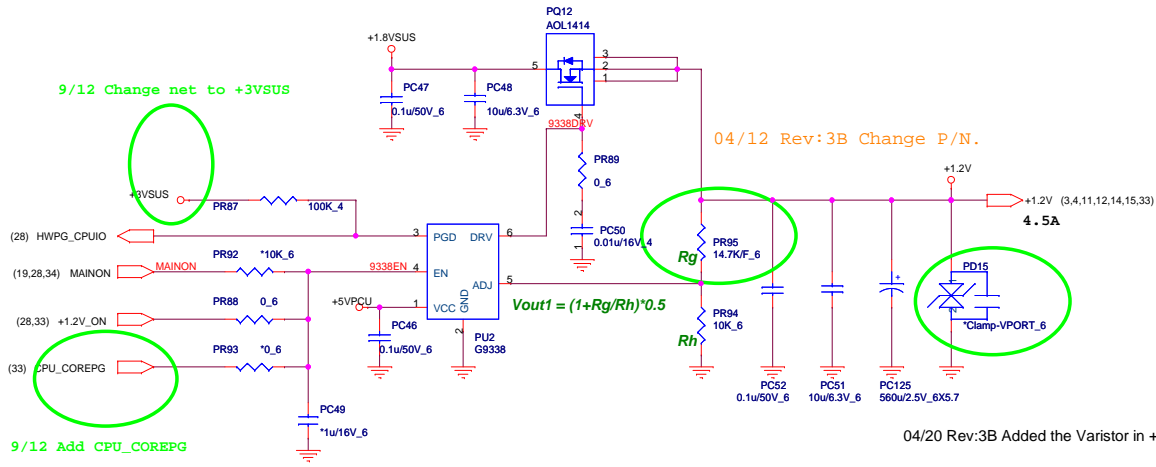




$R1 = (100 * V_{out} - R2) K$

if tune Vout PR38 un-mount, PR156 PR165 mount





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