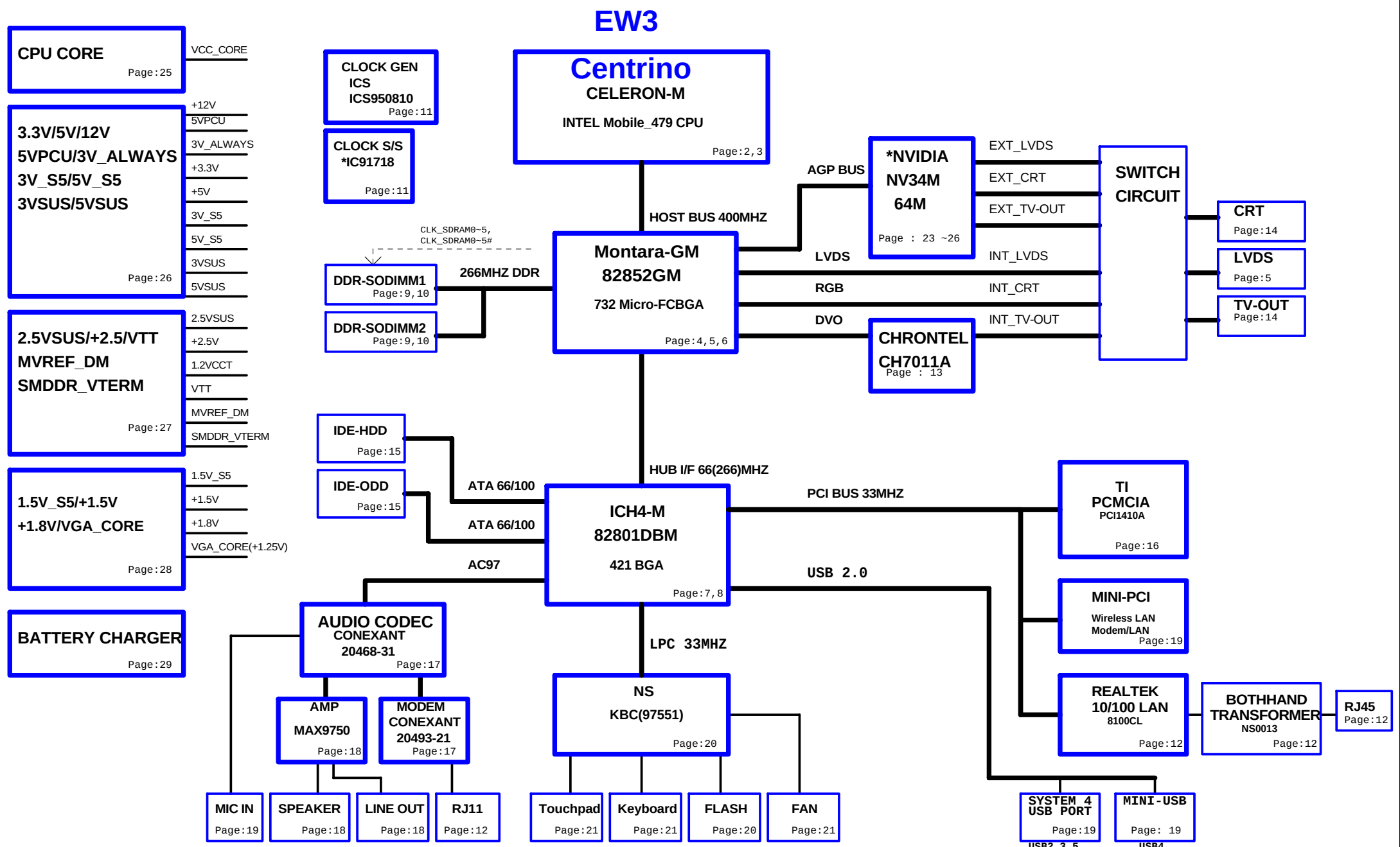
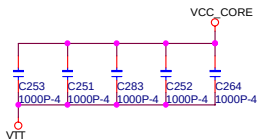
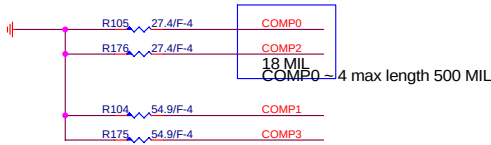
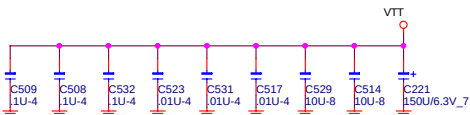
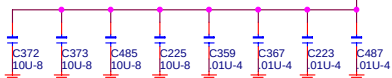




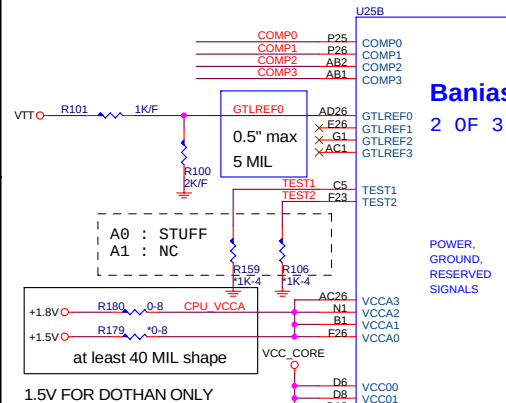
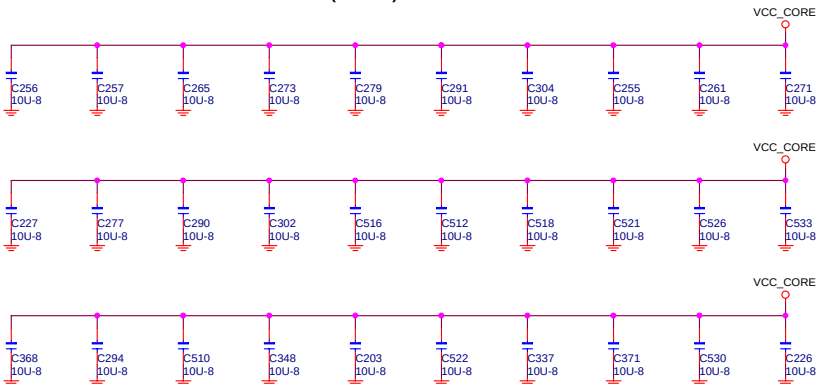
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD18	INTD#	REALTEK LAN
REQ1# / GNT1#	AD20	INTB# , INTC#	MINI-PCI
REQ3# / GNT3#	AD17	INTE#	TI 1410A



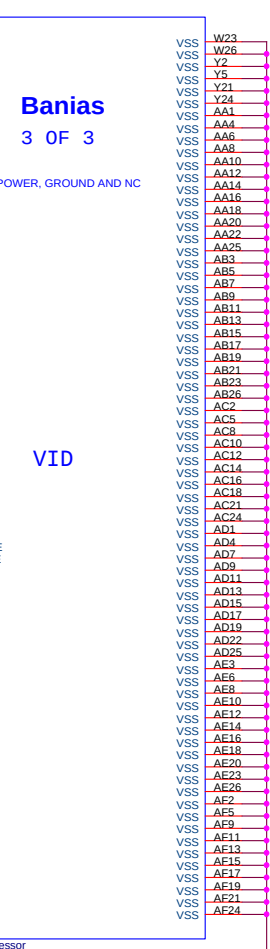
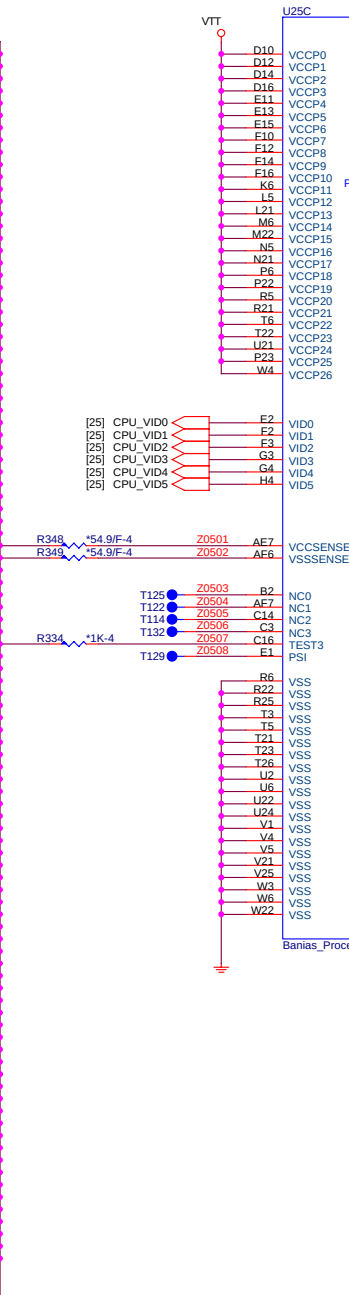
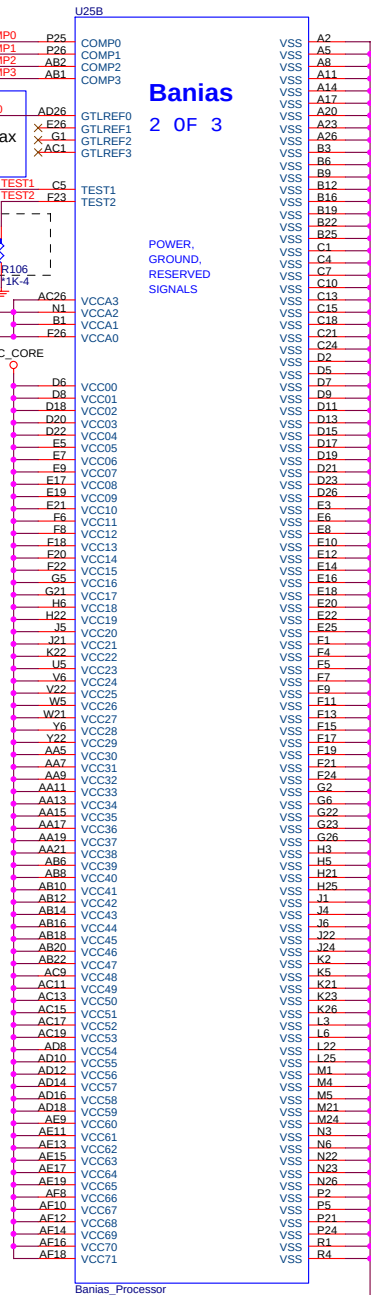
PLACE one 10U & one 0.01U for each VCCA pin



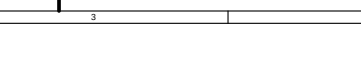
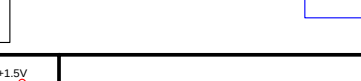
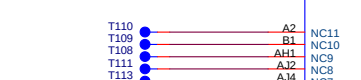
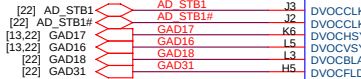
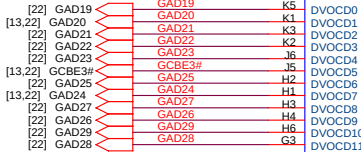
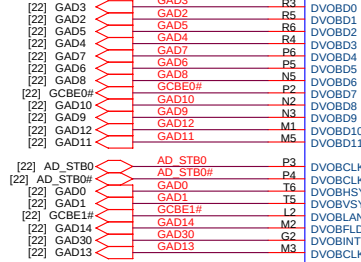
10U.6.3V/X5R(CC0805) *30



1.5V FOR DOTHAN ONLY



PROJECT : EW3
Quanta Computer Inc.



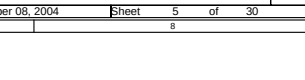
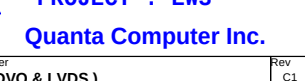
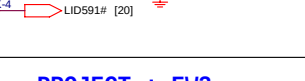
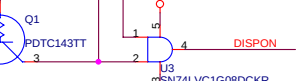
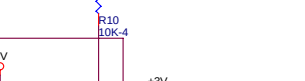
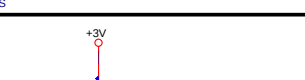
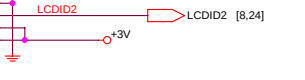
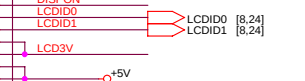
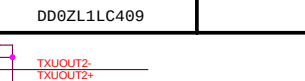
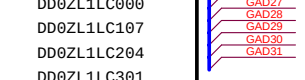
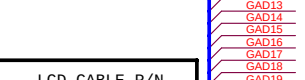
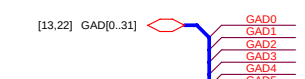
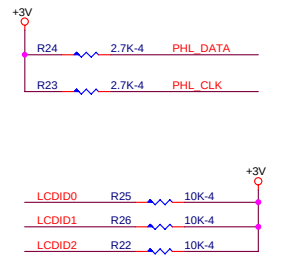
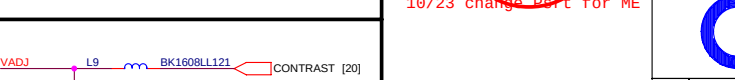
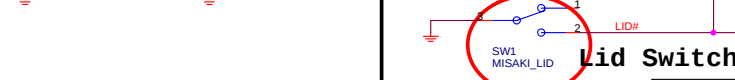
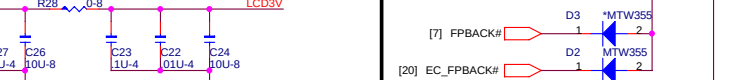
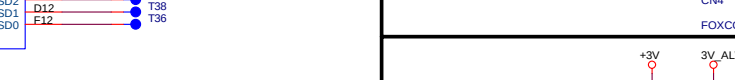
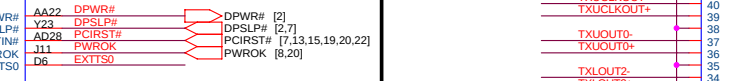
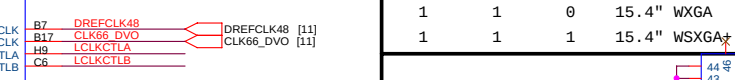
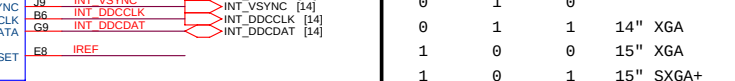
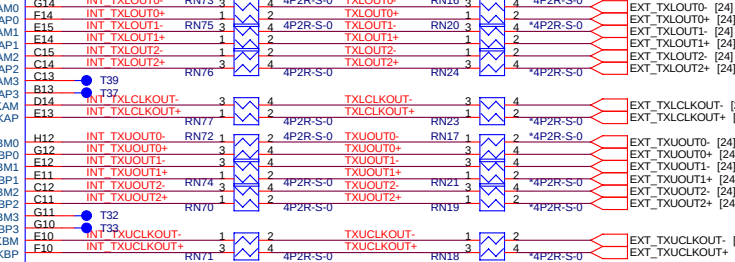
U26B Montara-852GM

DVO

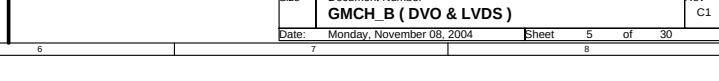
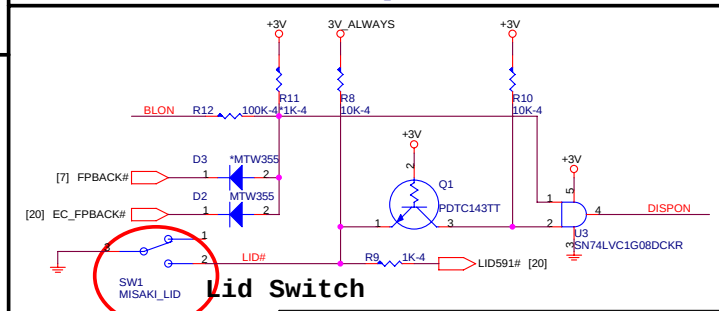
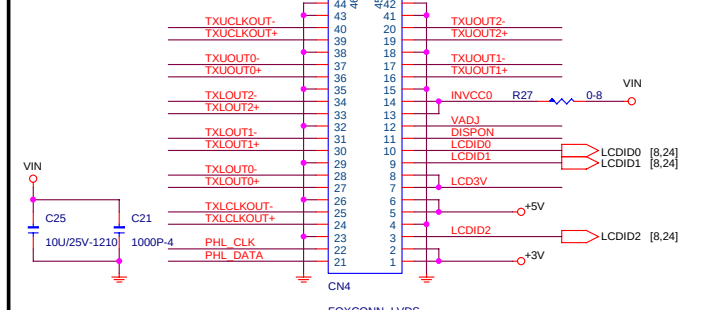
LVDS

DAC

MISC

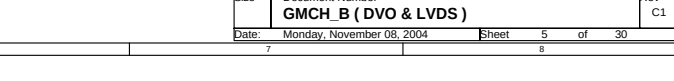
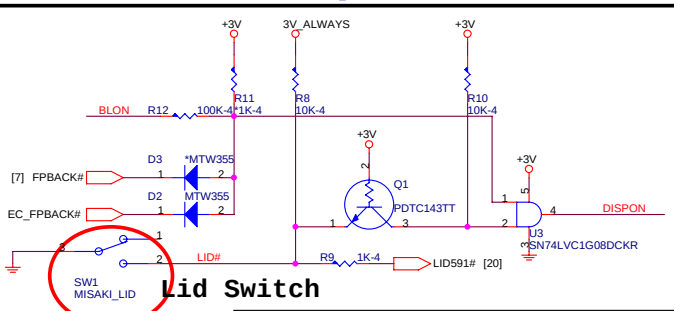
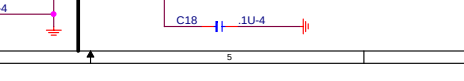
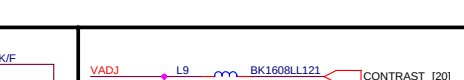
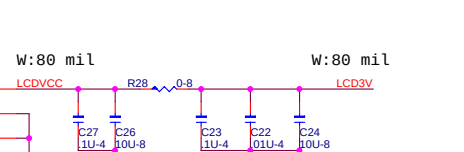
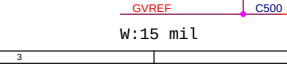
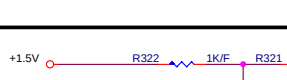
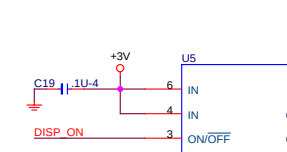
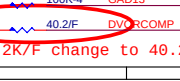
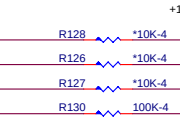


LCDID2	LCDID1	LCDID0	LCD TYPE	LCD CABLE P/N
0	0	0		
0	0	1		
0	1	0		
0	1	1	14" XGA	DD0ZL1LC000
1	0	0	15" XGA	DD0ZL1LC107
1	0	1	15" SXGA+	DD0ZL1LC204
1	1	0	15.4" WXGA	DD0ZL1LC301
1	1	1	15.4" WSXGA+	DD0ZL1LC409



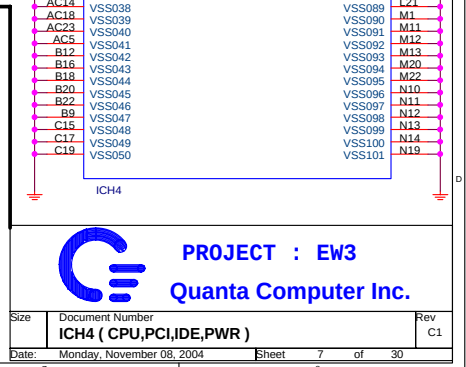
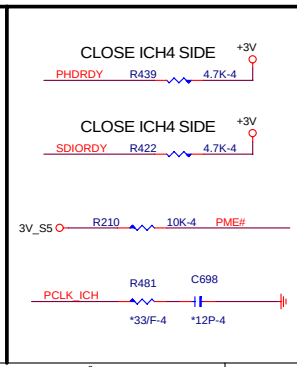
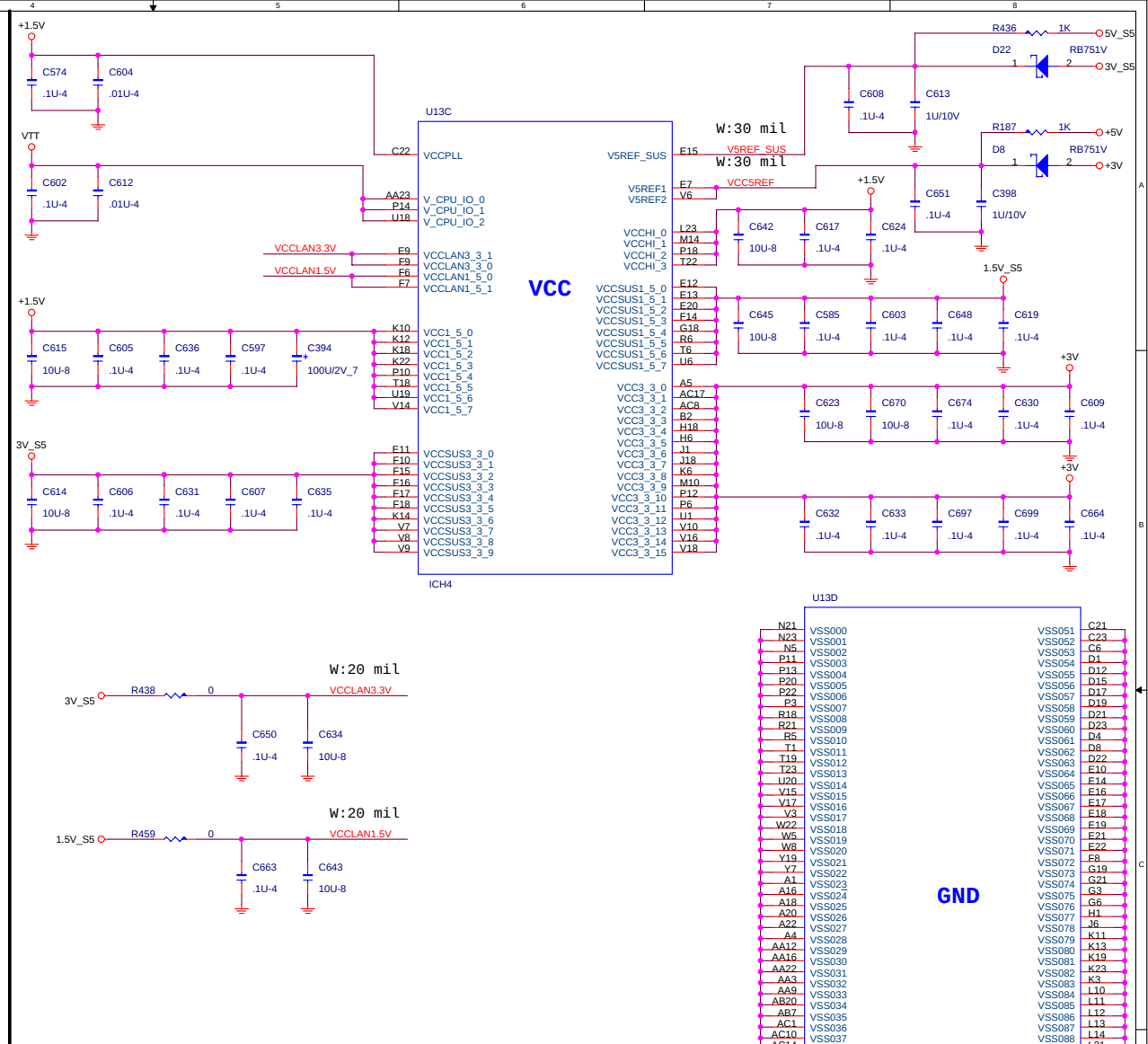
stuff for DVO
Un-stuff for 852GM

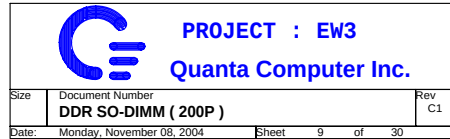
ST2	ST1	ST0	PSB Frequency	Memory Frequency	6FX Core Clock - Low	6FX Core Clock - High
0	0	0	400MHz	260MHz	133MHz	200MHz
0	0	1	400MHz	260MHz	100MHz	100MHz
0	1	0	400MHz	260MHz	100MHz	133MHz
0	1	1	400MHz	260MHz	133MHz	260MHz
1	0	0	533MHz	260MHz	133MHz	260MHz
1	0	1	533MHz	260MHz	133MHz	260MHz
1	1	0	533MHz	333MHz	166MHz	260MHz
1	1	1	400MHz	333MHz	166MHz	250MHz

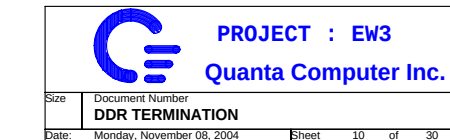
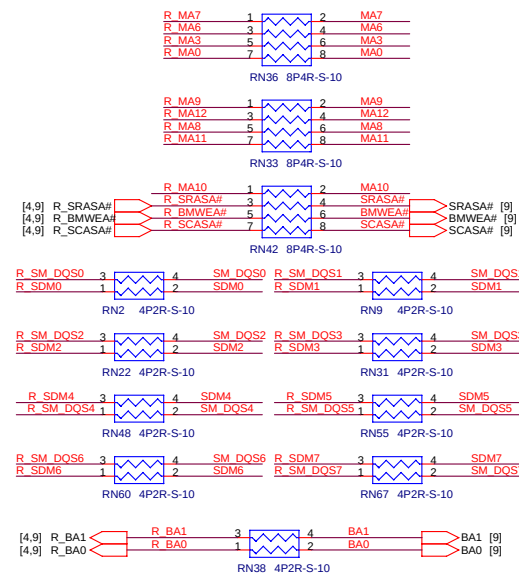
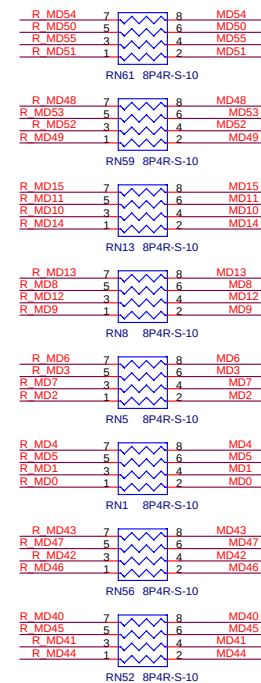
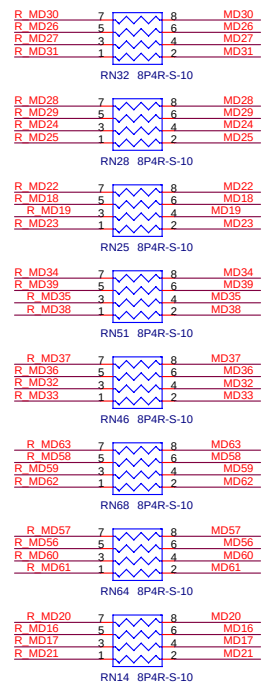
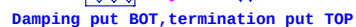


PROJECT : EW3
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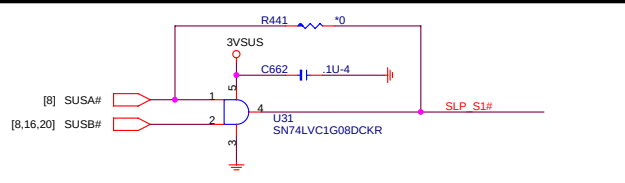
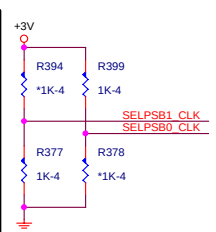
Size Document Number
GMCH_B (DVO & LVDS)
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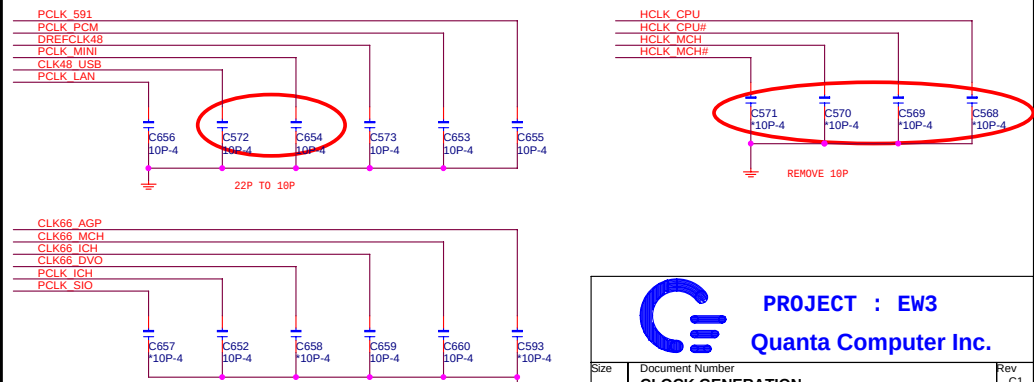
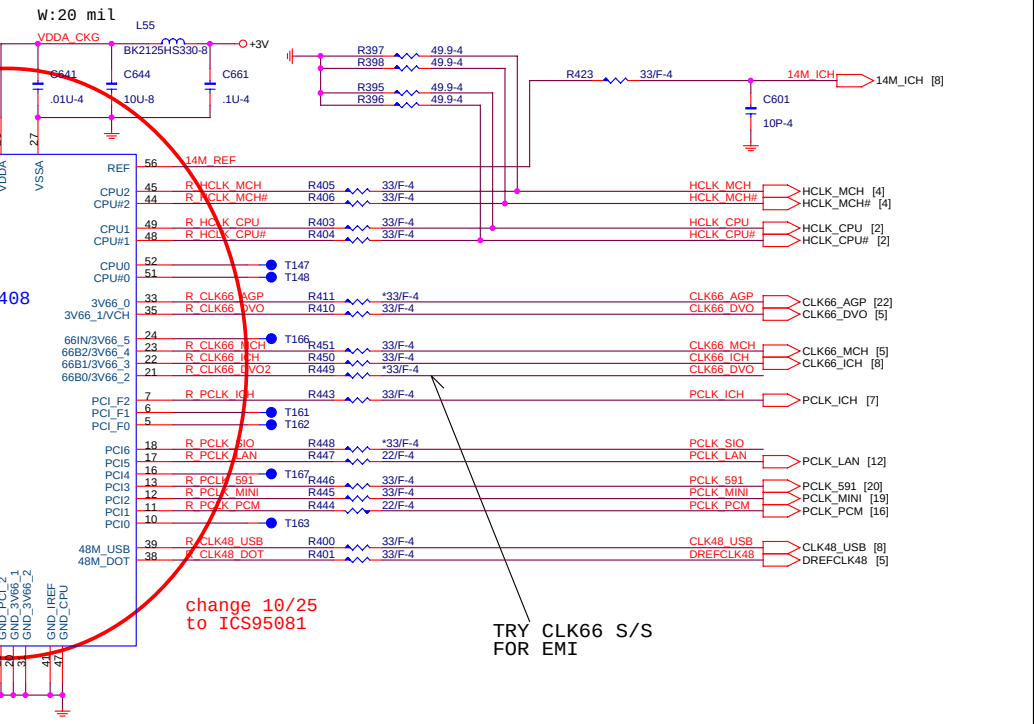
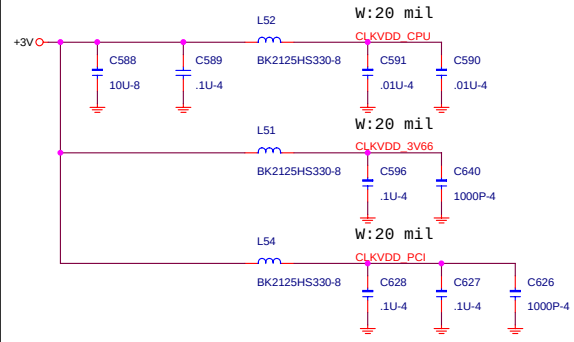
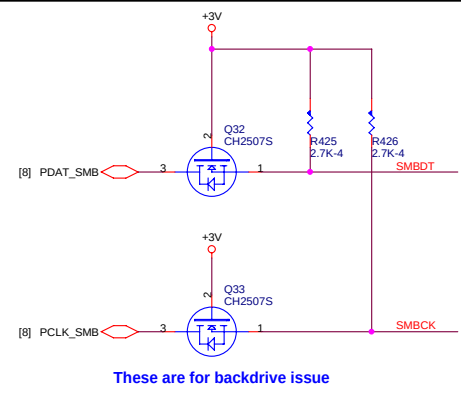
S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66
0	0	1	100	66	66
0	1	0	200	66	66
0	1	1	133	66	66



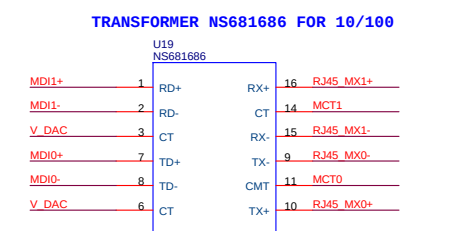
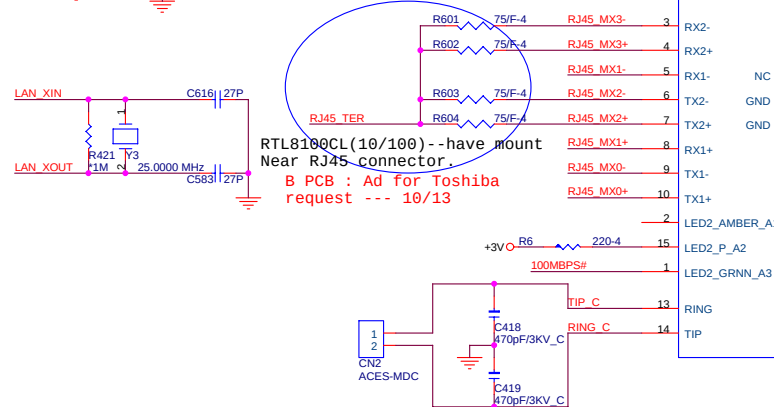
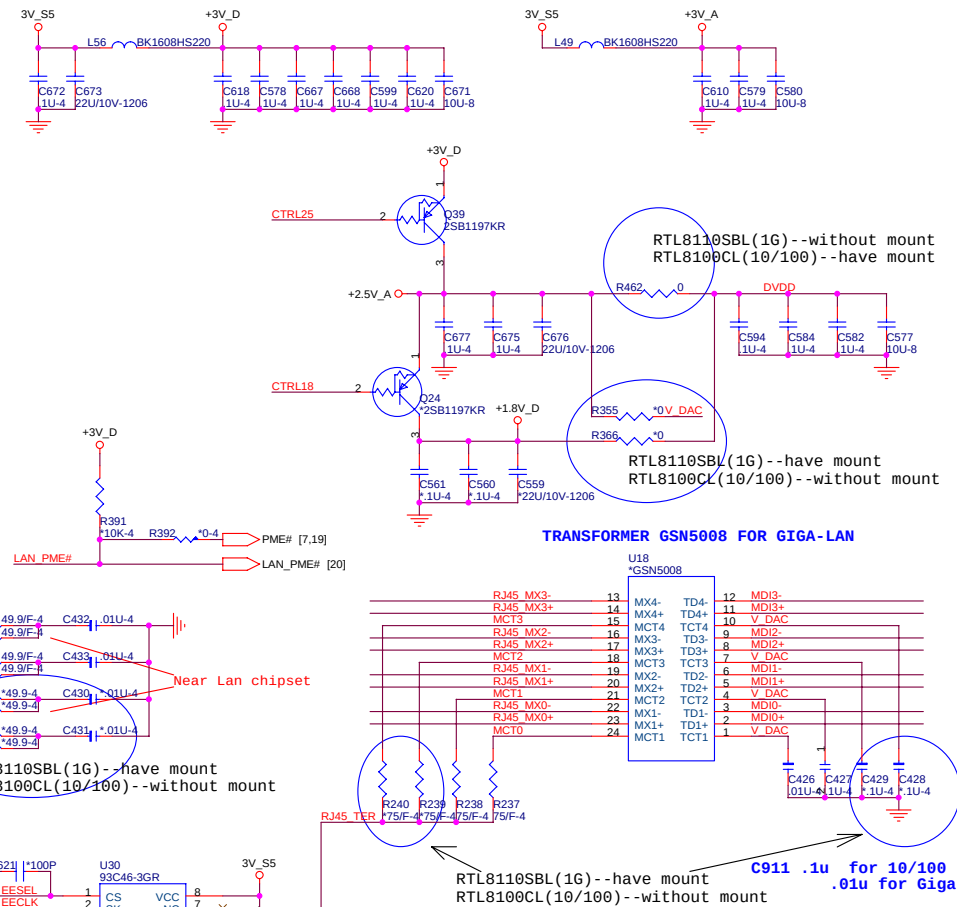
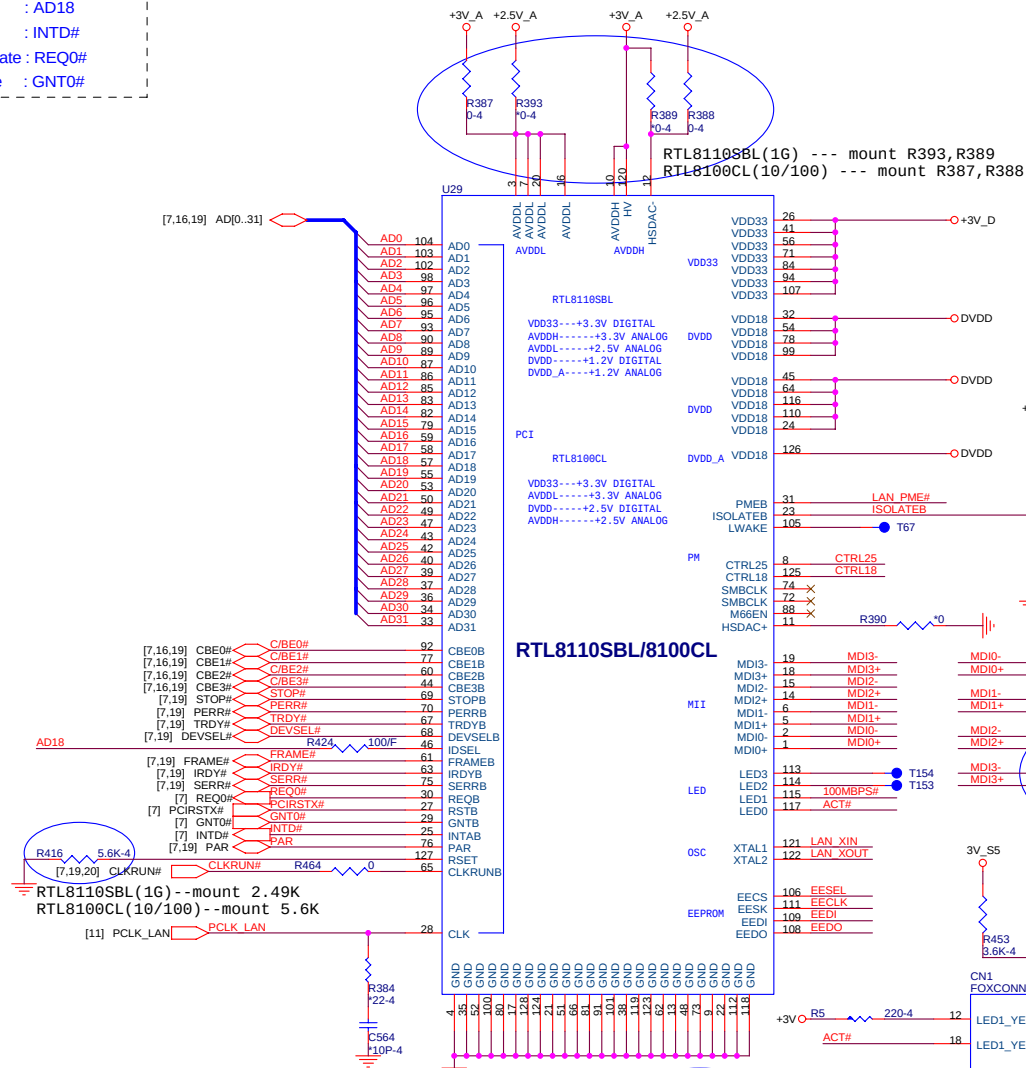
SMBus Byte 0 , Bit 5 = 0	3V66_1/VCH	66 MHz	W	S/S
SMBus Byte 0 , Bit 5 = 1		48 MHZ	W/O	S/S

Byte 0 , Bit 7 = 0 Disable Spread Spectrum
Byte 0 , Bit 7 = 1 Enable Spread Spectrum

Byte 4 Bit 7	Byte 5 Bit 7	Byte 5 Bit 6	Spread Mode	Spread %
SS2	SS1	SS0		
0	0	0	DOWN	+0.00 , -0.25
0	0	1	DOWN	+0.00 , -0.50
0	1	0	DOWN	+0.00 , -0.75
0	1	1	DOWN	+0.00 , -1.00
1	0	0	CENTER	+0.13 , -0.13
1	0	1	CENTER	+0.25 , -0.25
1	1	0	CENTER	+0.37 , -0.37
1	1	1	CENTER	+0.50 , -1.50



ID Select : AD18
Interrupt Pin : INTD#
Request Indicate : REQ0#
Grant Indicate : GNT0#



PROJECT : EW3
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CRT PORT

INT_VGA_RED, INT_VGA_GRN, INT_VGA_BLU, INT_VSYNC, INT_HSYNC, INT_DDCCLK, INT_DDCDAT, VGA_RED, VGA_GRN, VGA_BLU, VSYNC, HSYNC, DDCCLK, DDCDAT

10/13 for ME

10/12 for signal

10/25 change to B68 for EMI

10/12 for signal

10/25 change to B68 for EMI

FOR M/B HOLE

10/8 Spec change

S-VIDEO

TV_C/R, TV_CHROMA, TV_LUMA, TV_Y/G, TV_COMP

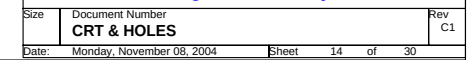
FOR MODEM MODULE

FOR CPU HEATSINK

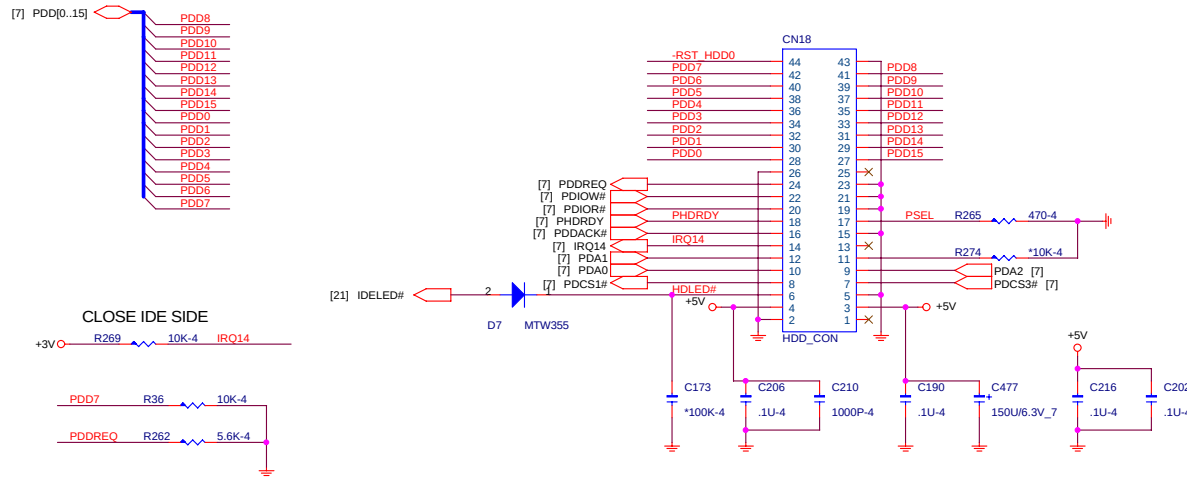
NEAR NORTHBRIDGE

PROJECT : EW3
Quanta Computer Inc.

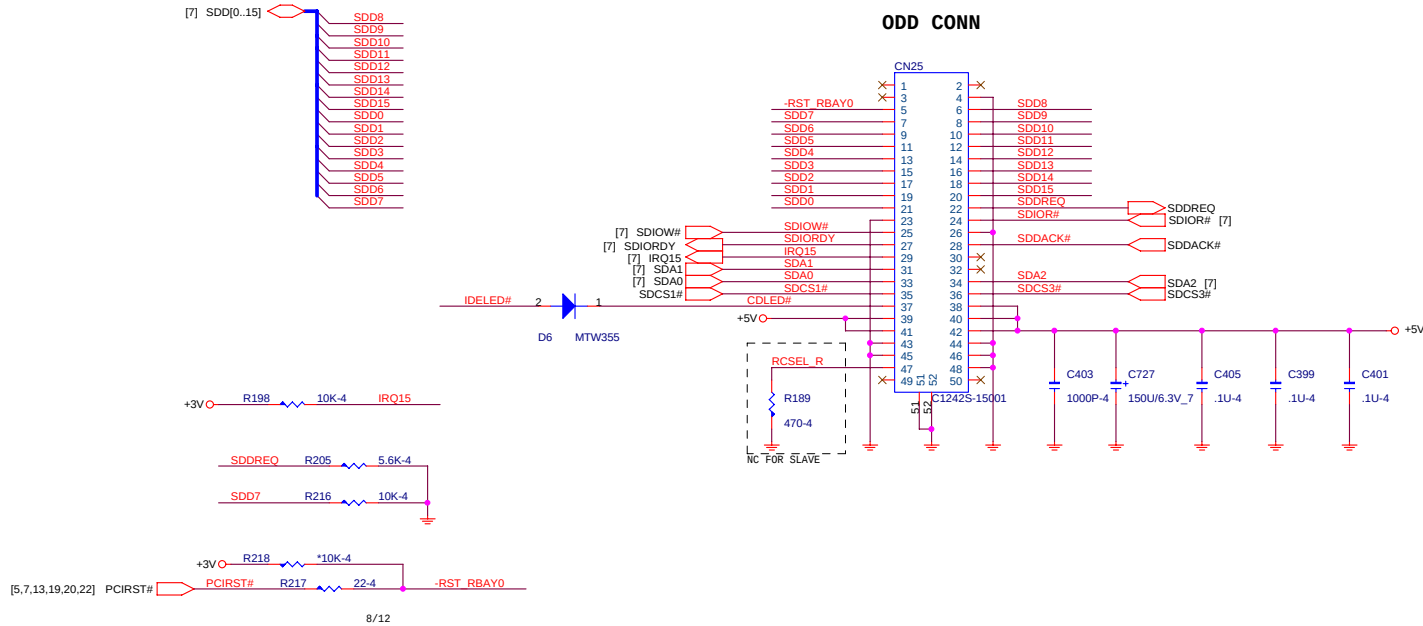
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HDD CONN



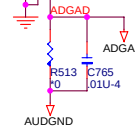
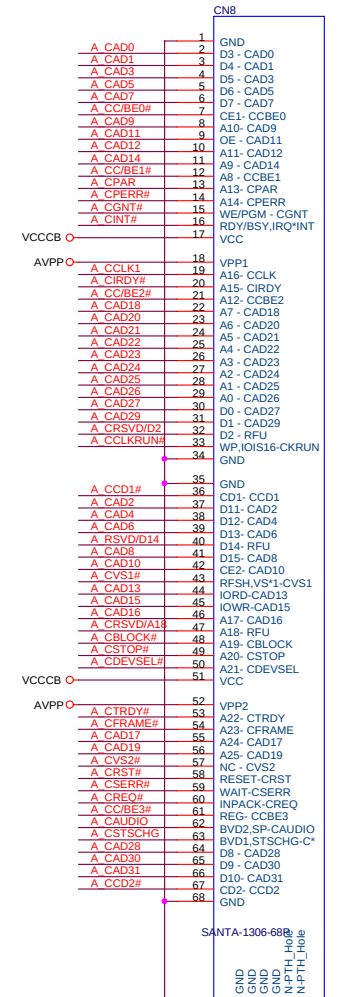
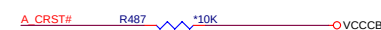
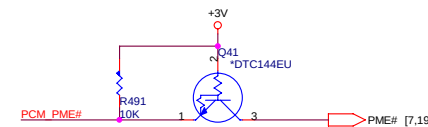
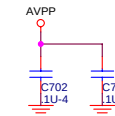
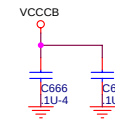
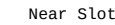
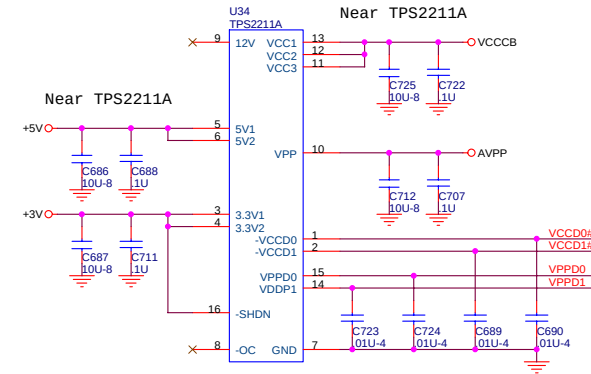
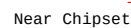
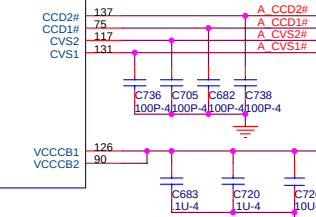
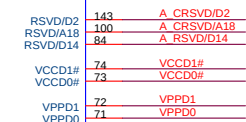
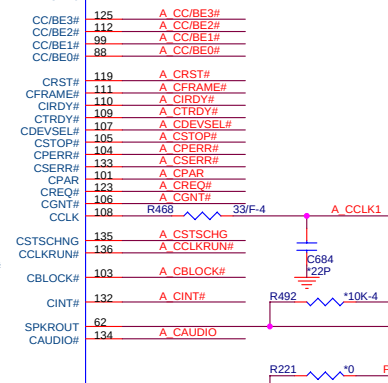
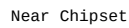
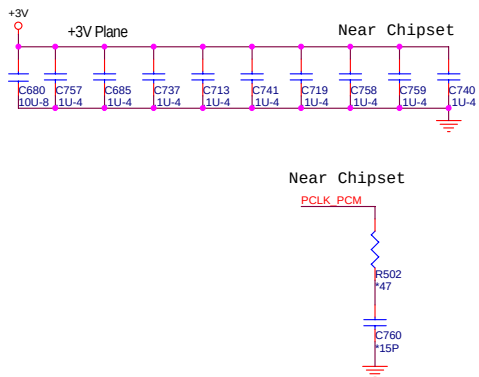
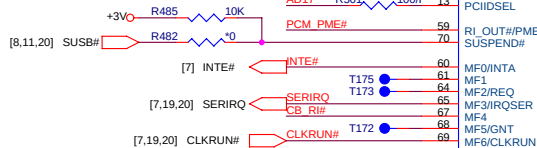
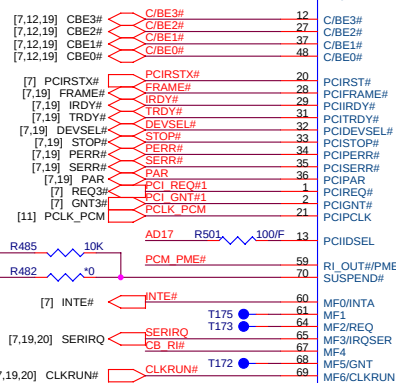
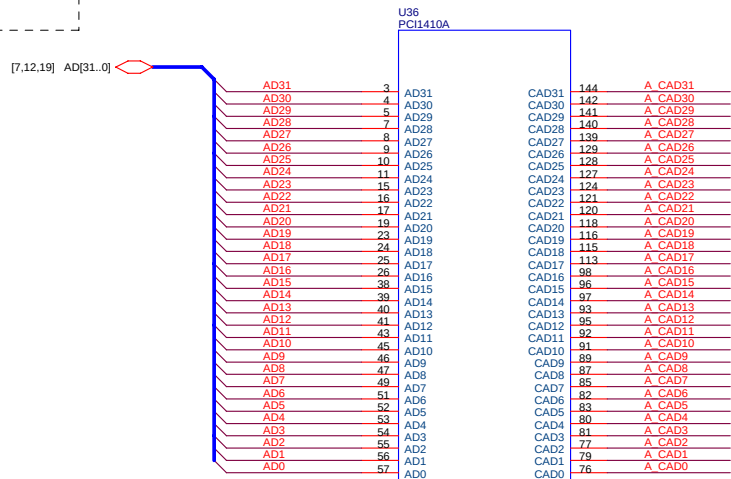
ODD CONN



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ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ3#
Grant Indicate : GNT3#



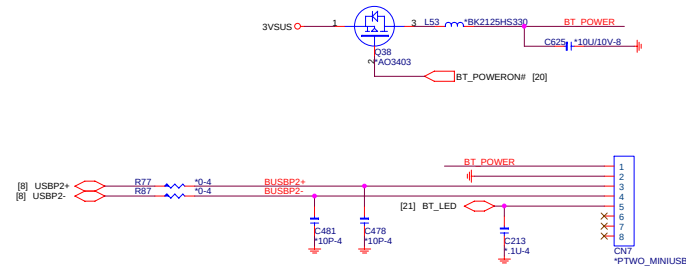
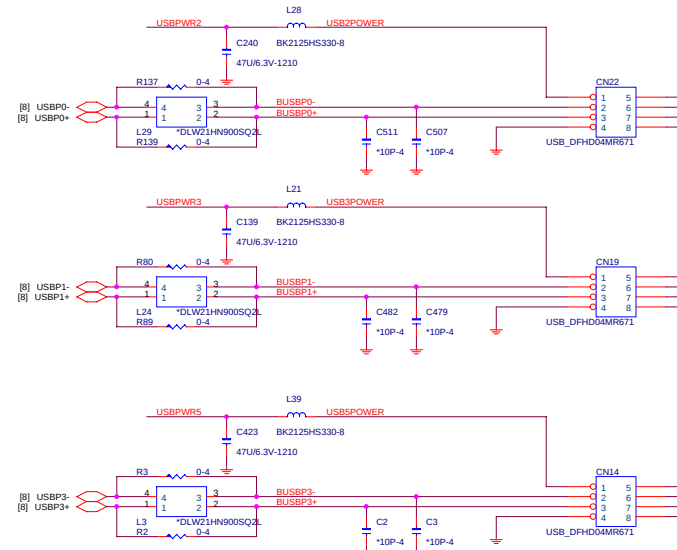
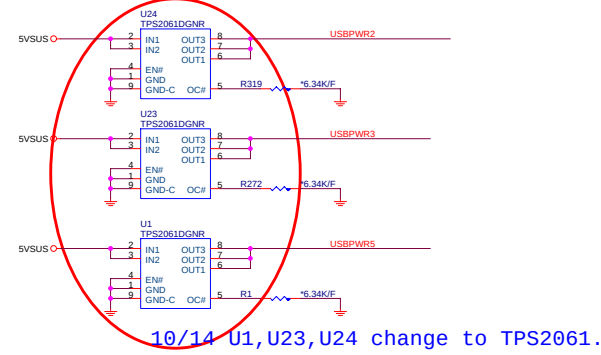
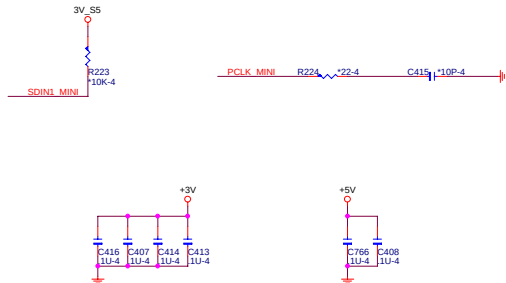
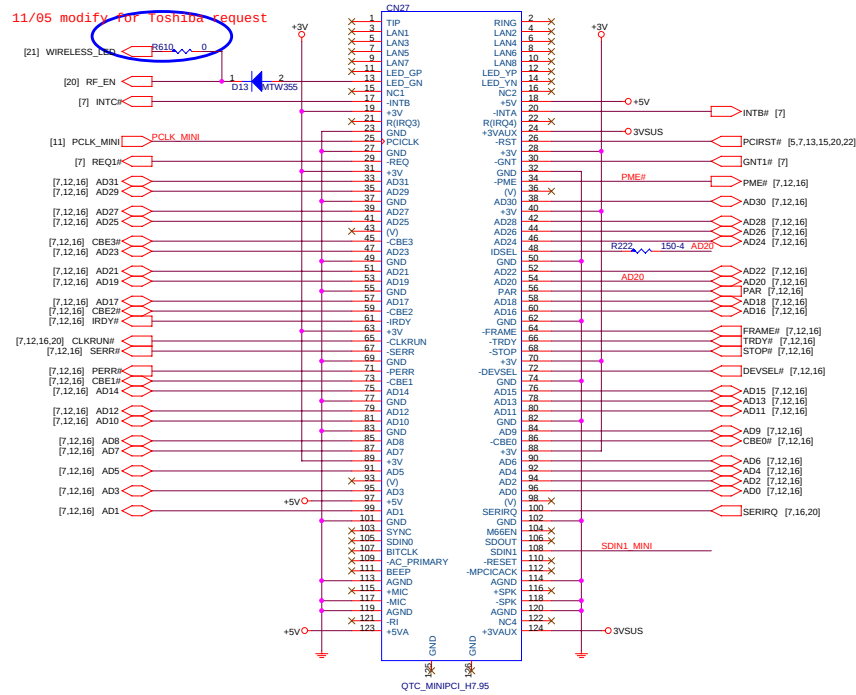
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Quanta Computer Inc.

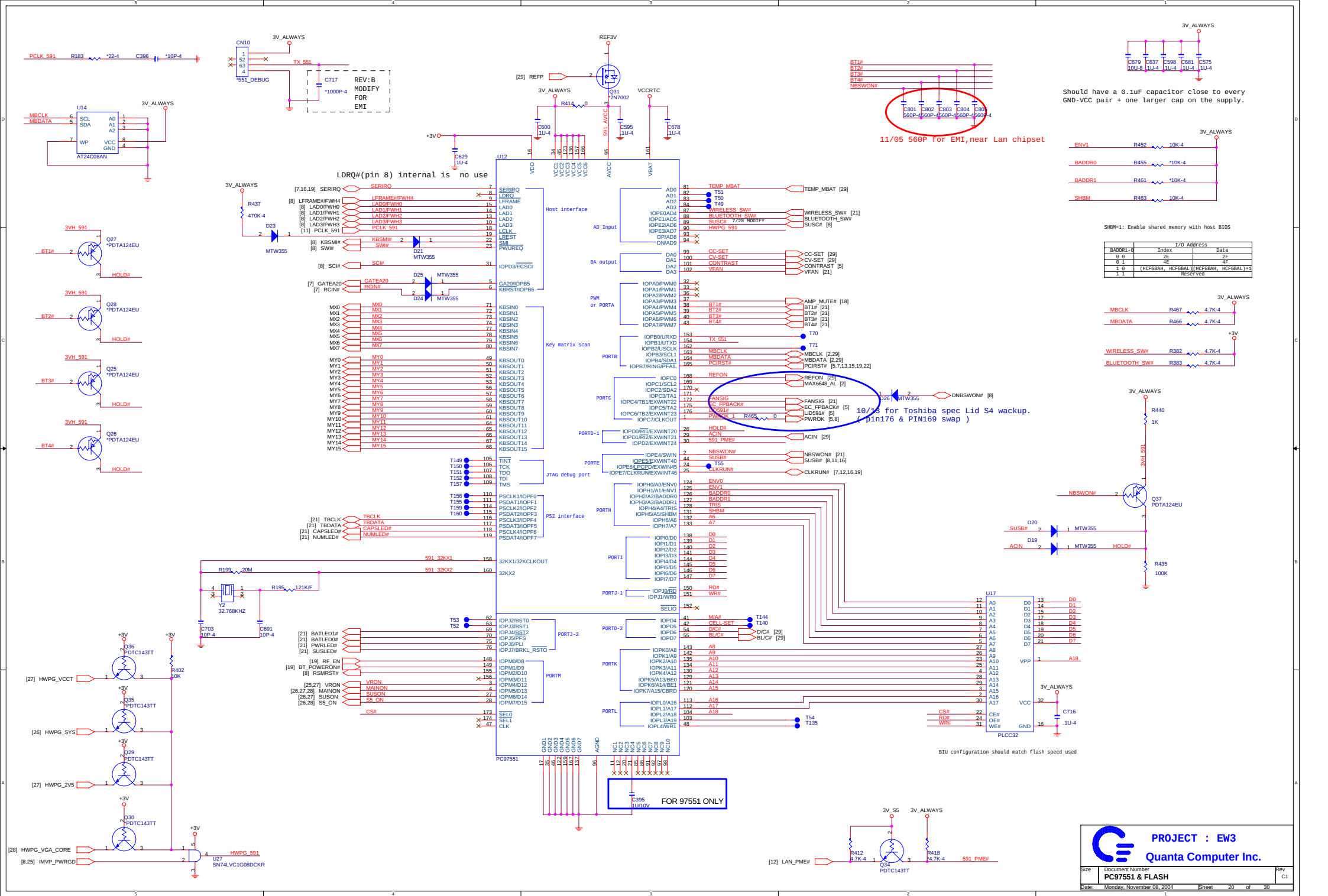
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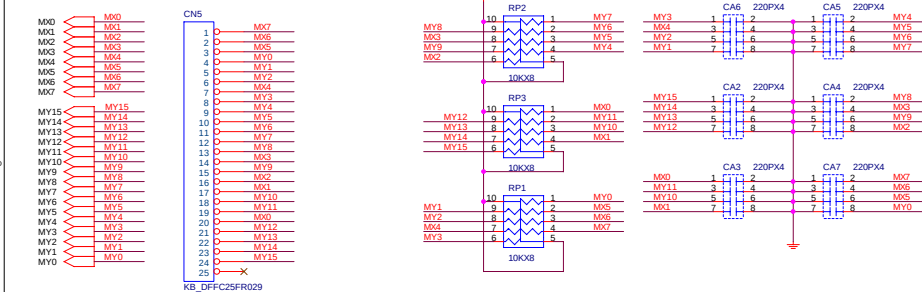
ID Select : AD20
Interrupt Pin : INTB#, INTA#
Request Indicate : REQ1#
Grant Indicate : GNT1#

MINI-PCI

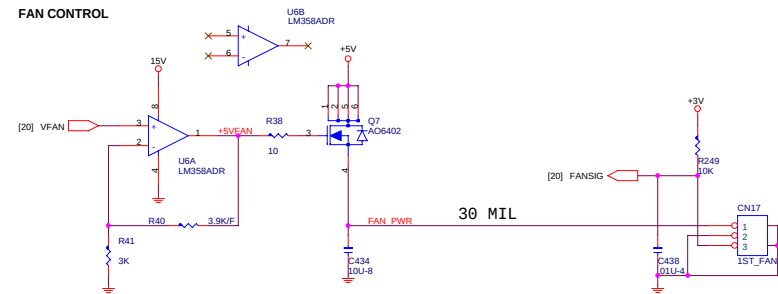
11/05 modify for Toshiba request





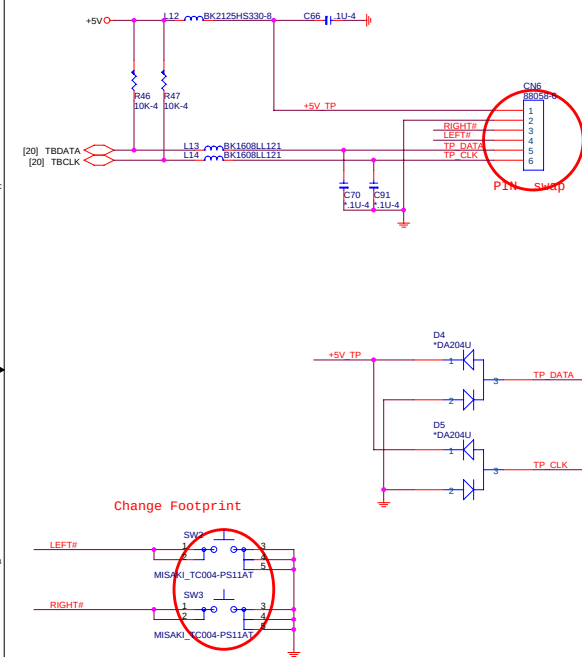


FAN CONTROL

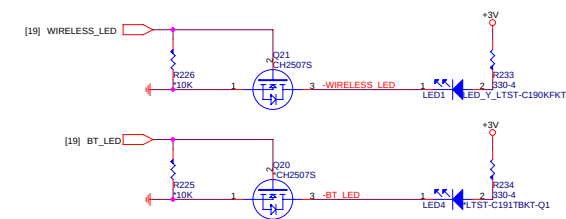
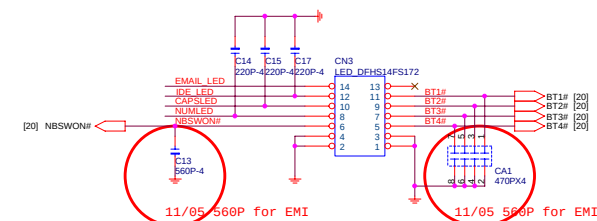
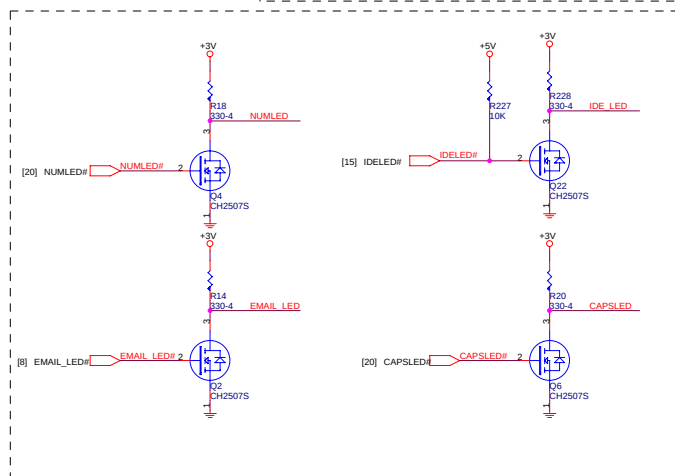
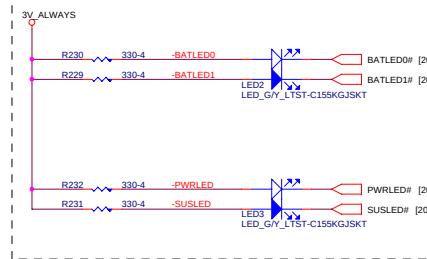


TOUCH PAD

20 MIL



SWITCH



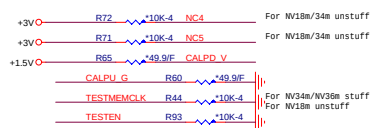
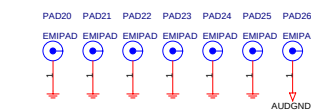
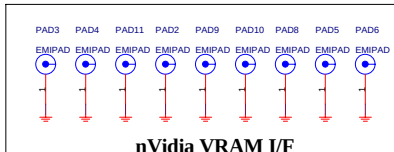
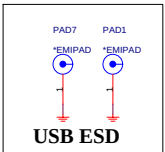
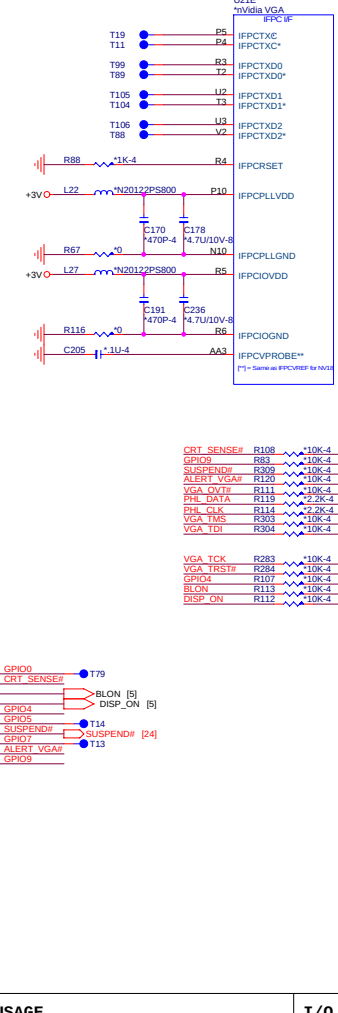
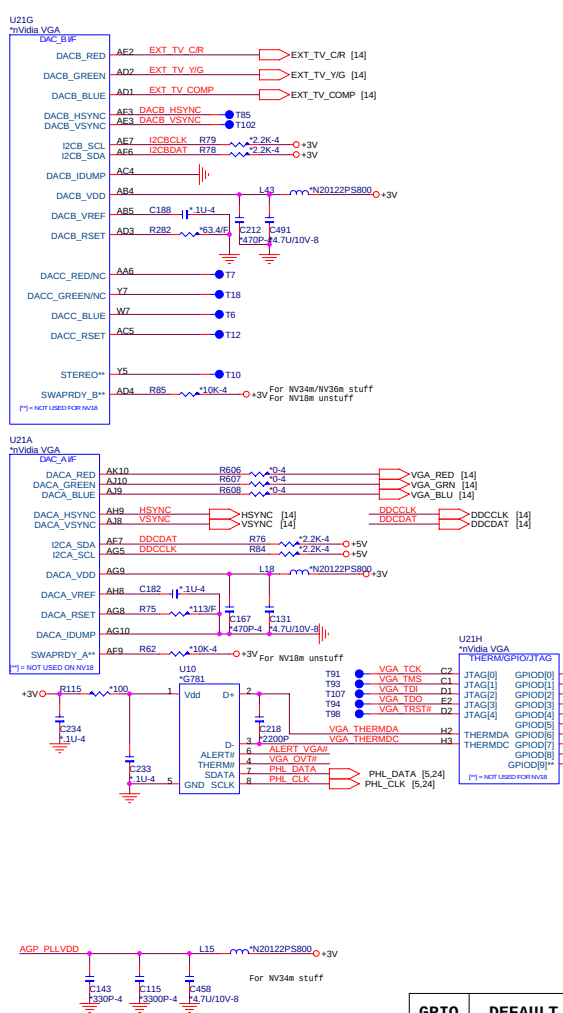
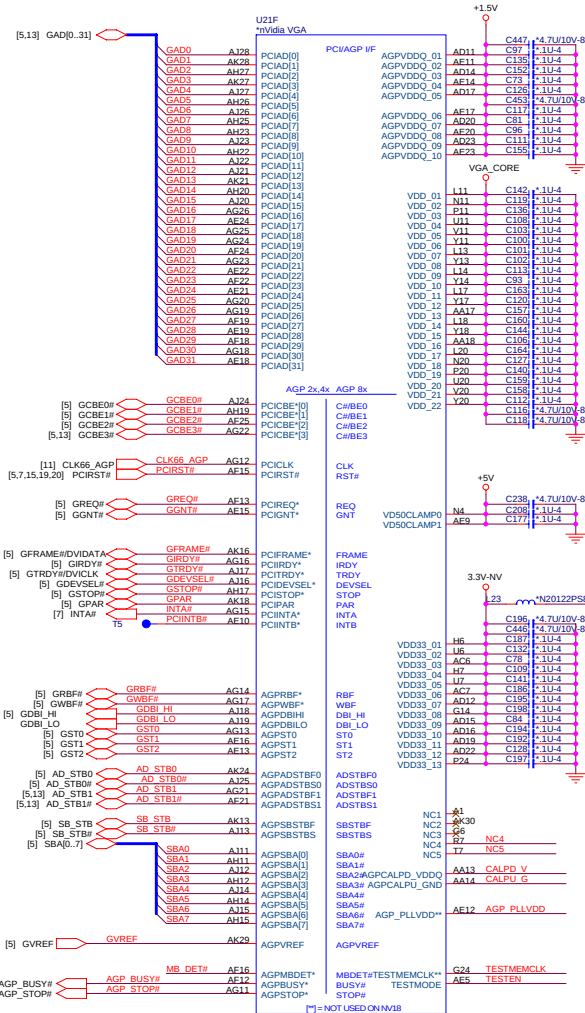
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	T/P,FAN,SWITCH,LED,K/B

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nVidia AGP I/F

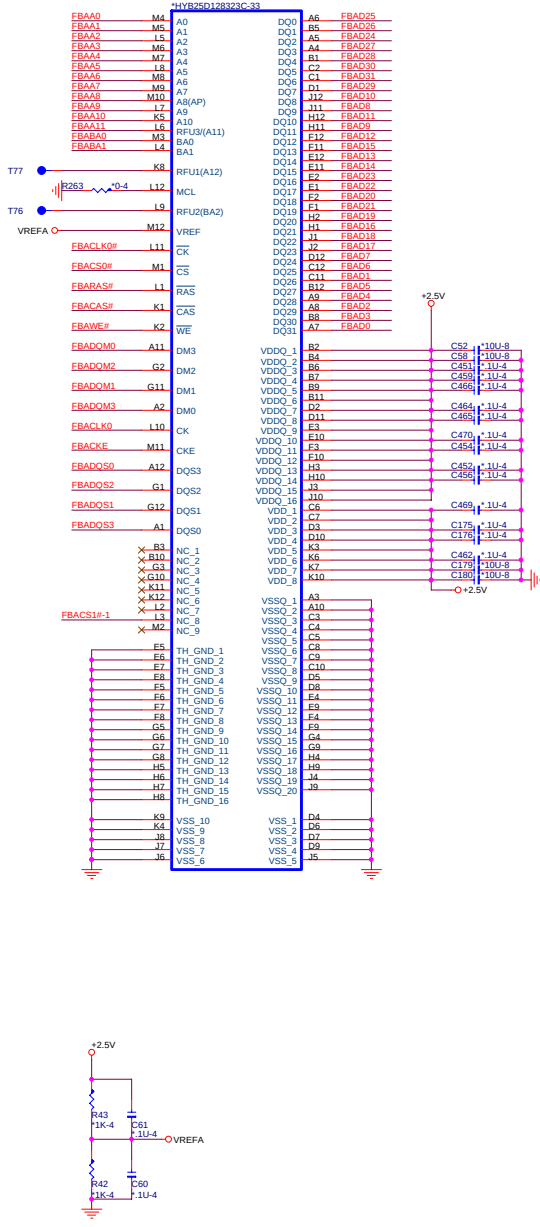


GPI0	DEFAULT STATE	USAGE	I/O
0	PD	Spread spectrum control	0
1	PD	Hot plug/unplug	I/O
2	PD	Panel backlight enable	0
3	PD	Panel power enable	0
4	PD	TBD	I/O
5	PD	Spread spectrum control	0
6	PU	HW suspend	I
7	PU	Dynamic NVDD voltage control	0
8	PU	Thermal monitor	I
9	PU	Fan Control	I/O

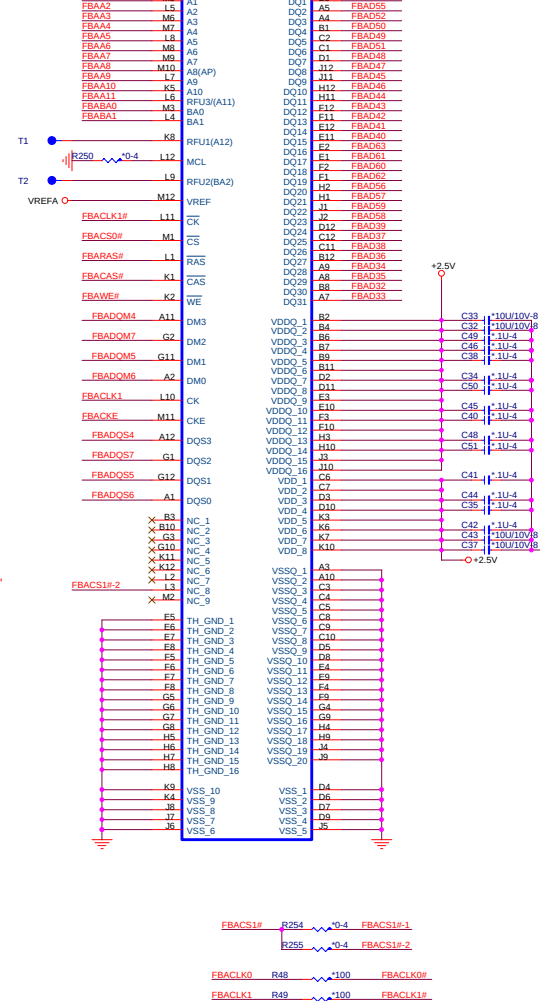
nVidia MEMORY B



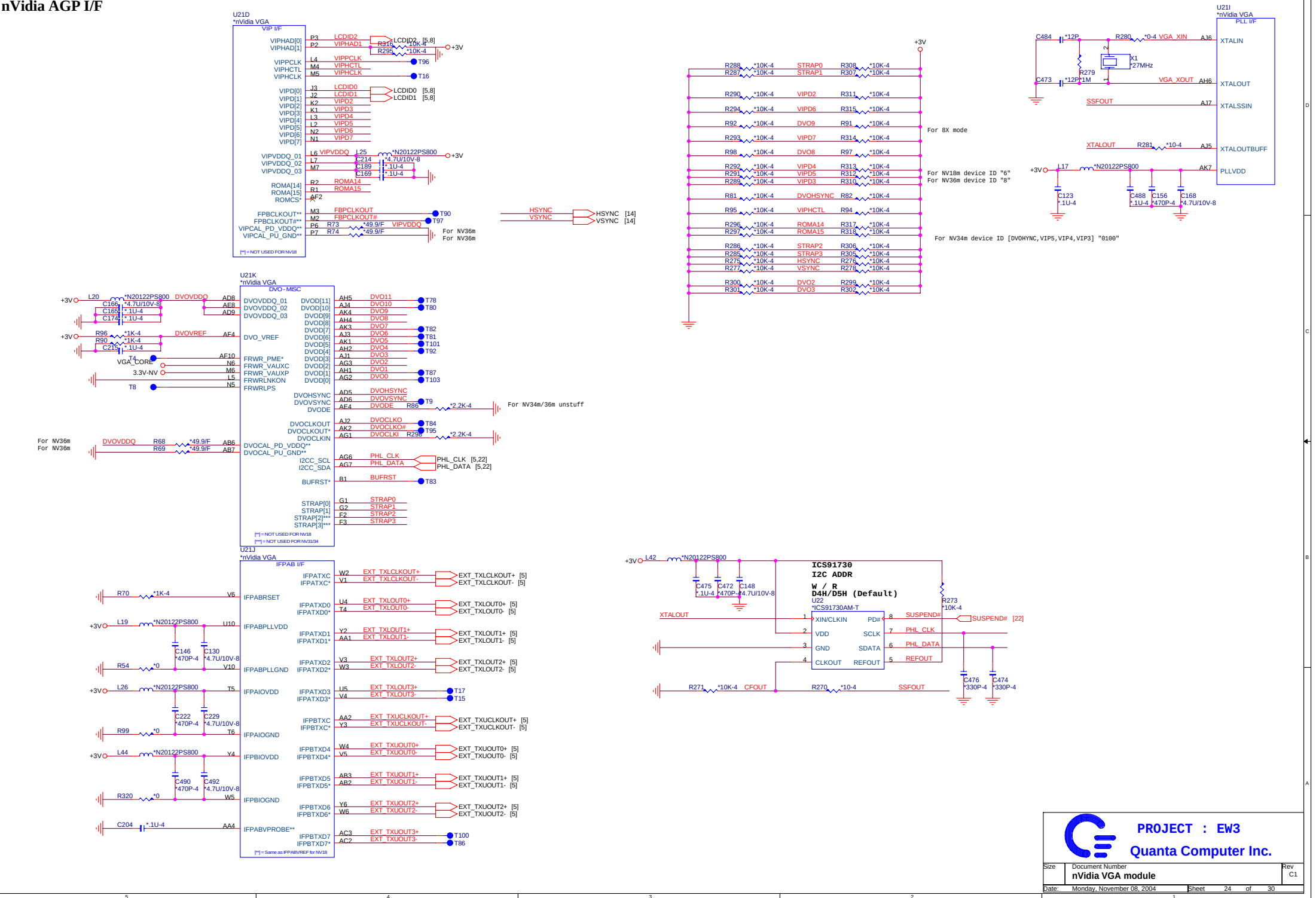
nVidia MEMORY A

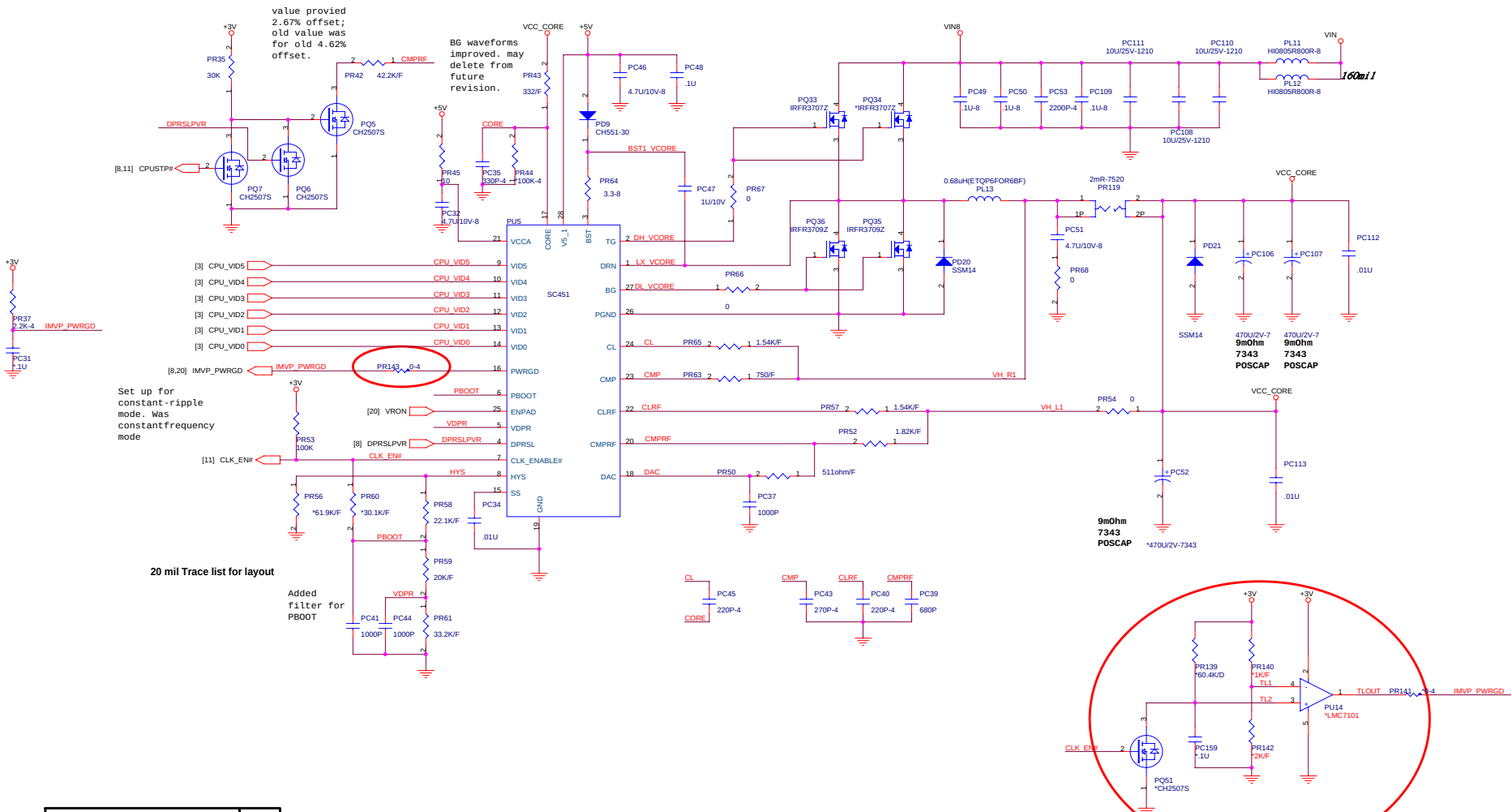


M4



nVidia AGP I/F





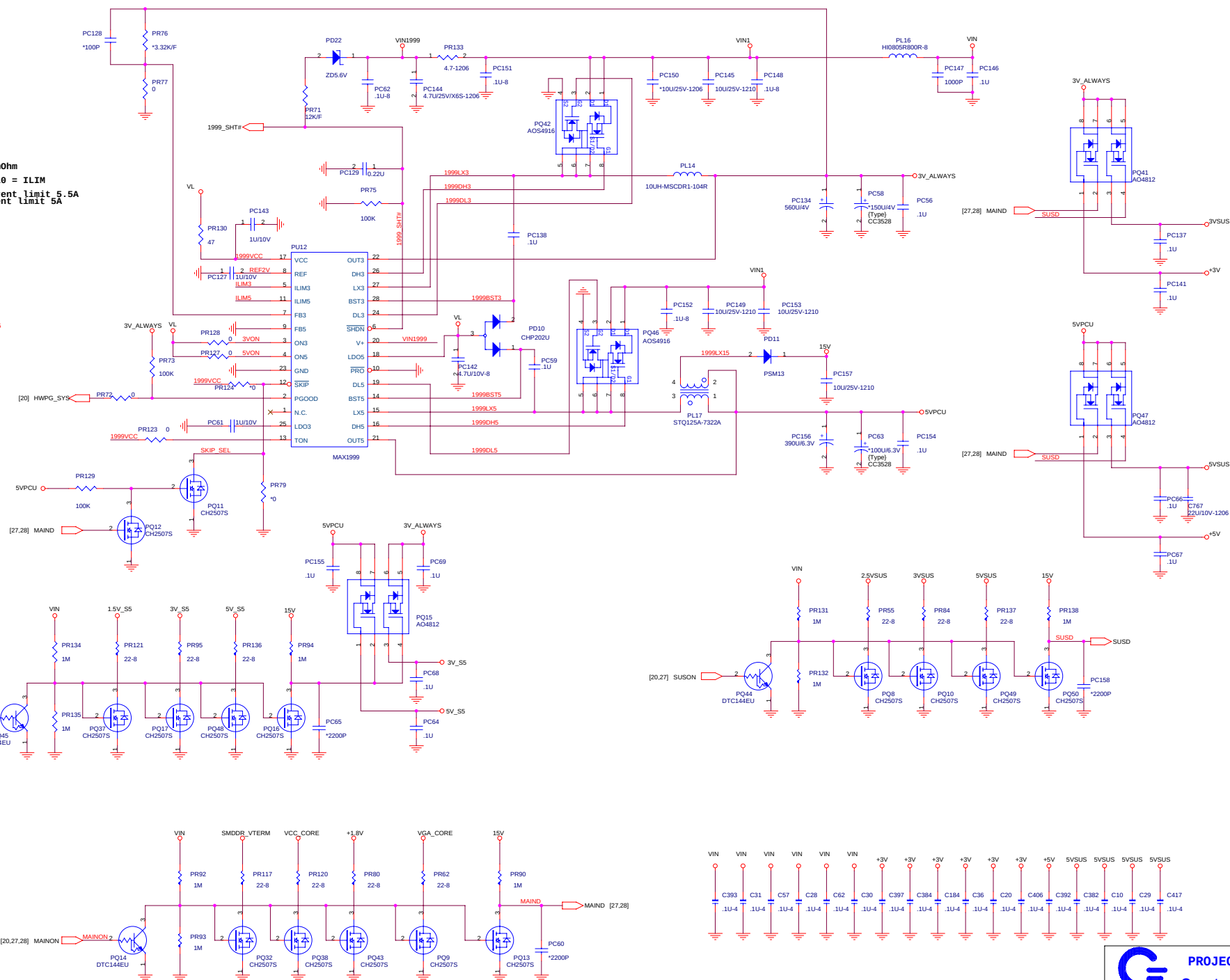
V I D										Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0					v
0	1	0	1	1	1					1.340
0	1	1	0	0	0					1.324
0	1	1	0	1	0					1.292
0	1	1	1	0	0					1.260
0	1	1	1	1	0					1.244
0	1	1	1	1	1					1.212
1	0	0	0	0	1					1.180
1	0	0	0	1	1					1.148
1	0	0	1	1	0					1.100
1	0	1	0	0	1					1.052
1	0	1	0	1	1					1.020
1	0	1	1	1	0					0.972
1	1	0	0	0	0					0.940

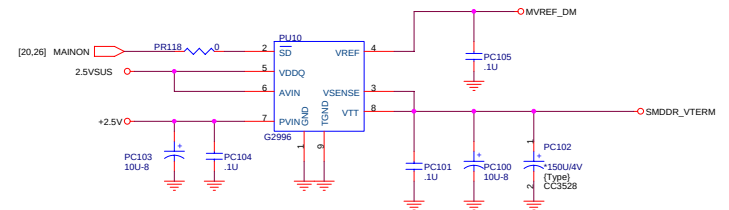
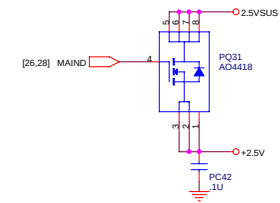
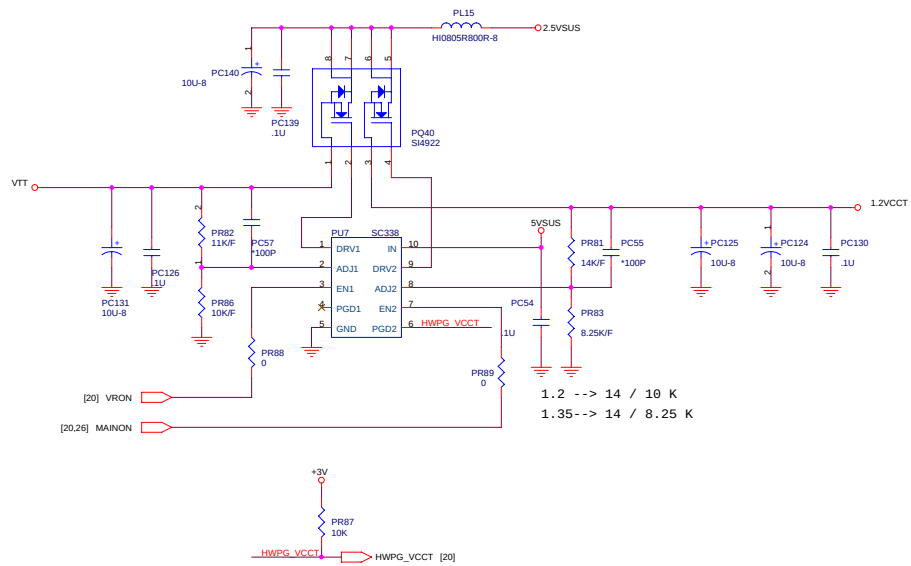
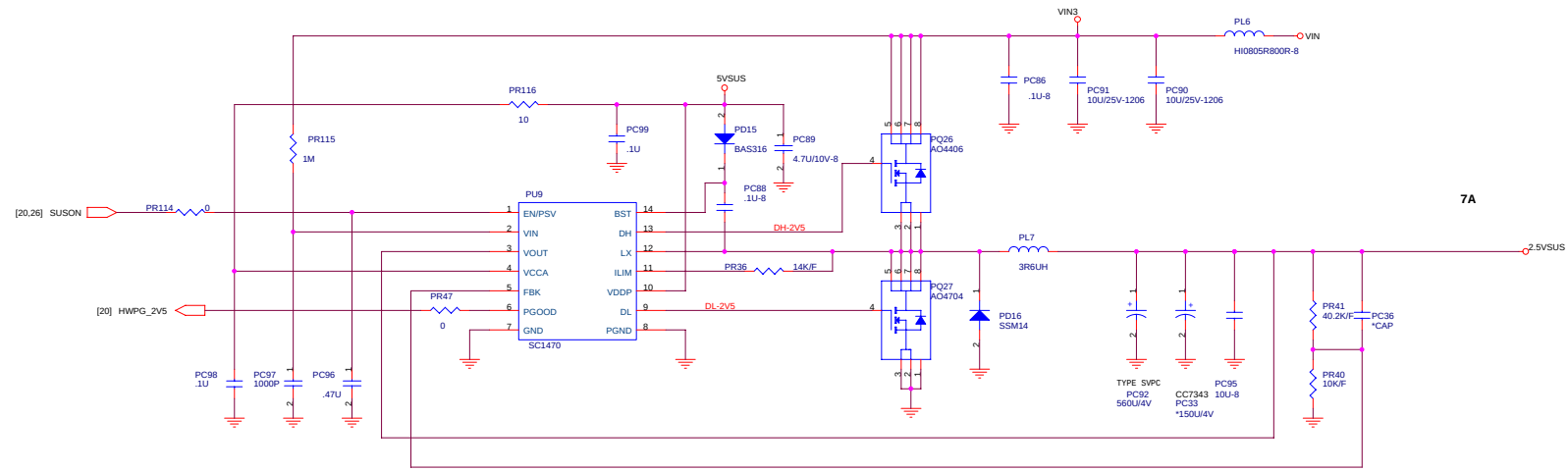
100 mil Trace list for layout

- DH_VCORE
- LX_VCORE
- DL_VCORE
- DH_VCORE2
- LX_VCORE2
- DL_VCORE2

10 mil Trace list for layout

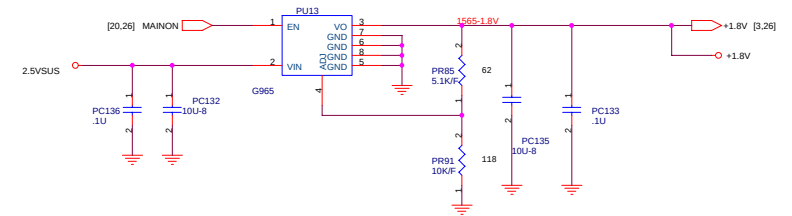
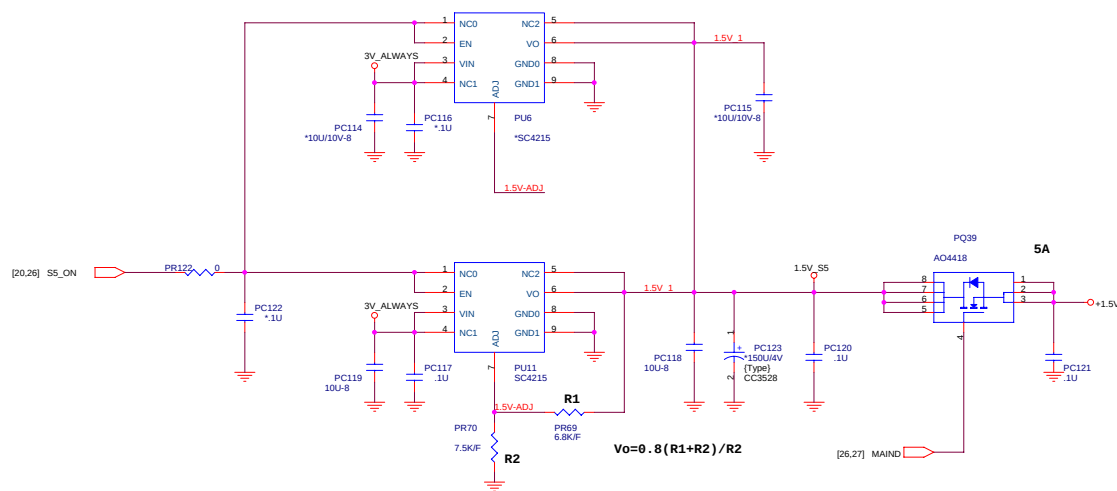
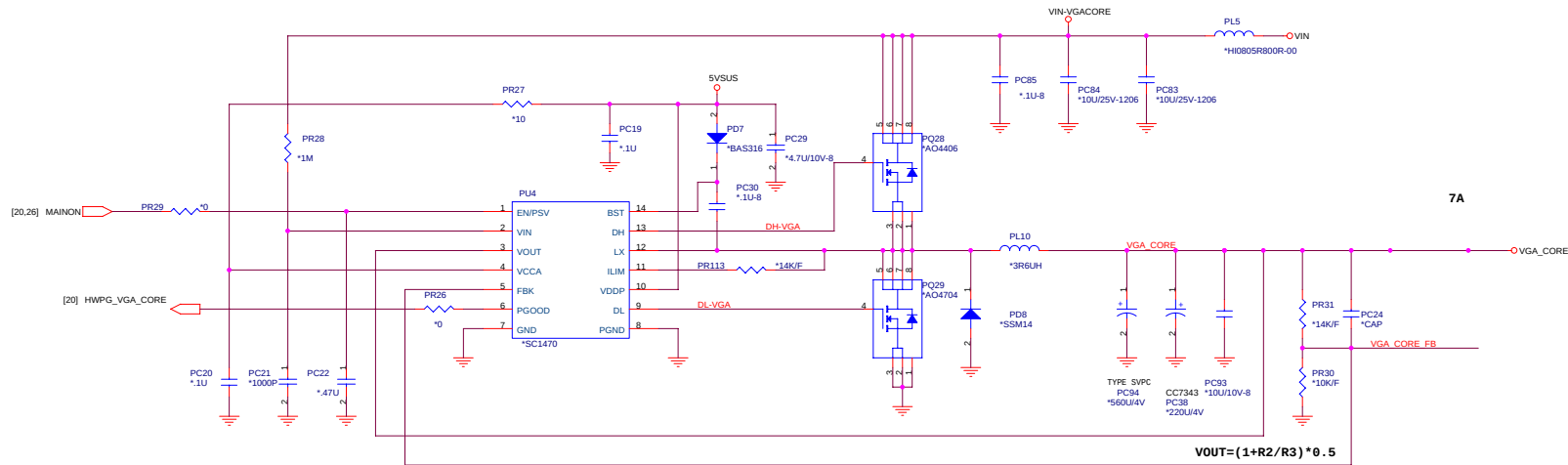






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DATE_VER.	MODIFIED BY	CHANGE LIST						
09/08_REVA1		First Version						
09/14_REVA2	for Toshiba spec change for Toshiba spec change for Toshiba spec change	(1) Page 21 del buleetooth function switch. (2) Page 21 update led circuit. (3) Add RTC clear jump.						
09/17_REVA3	for Toshiba spec change for Toshiba spec change for Toshiba spec change	(1) G781 change to ADM1032AR. (2) THER_OVT# net change to 1999_SHT#. (3) USB Port current change to 1A.						
09/21_REVA4	for Toshiba change for Toshiba add	(1) GND_LAN_CHASIS change to GND. (2) MIC JACK add net to MIBIAS.						
10/06_REVB1	EE design issue ME issue EE design issue EE design issue EE design issue EE design issue MIC gain adj ME issue Power design issue	(1) Page5 & Page13 change CH7011A DVO source to DVOC from DV0B, R148 & R145 mount 1K, R140 change to 40.2 Ohm from 40.2K Ohm. (2) Page5 CN4 change footprint & swap pin. (3) Page8 change USB port singal to USB0-3 from USB2-5. (4) page8 SW4 pin1 & pin3 swap. (5) Page12 RJ45&RJ11 connector footprint change. (6) Page12 Y3 footprint change. (7) Page15 CN18 change footprint & swap pin. (8) Page17 add R514 for MIC GAIN adj. (9) Page21 CN6 pin change to 6-1 from 1-6. (10) Page25-29 modify for Power. ###Changer function: 1. PR17 CHANGE TO 60.4K/D.....CS36043D9005 2. PR99 CHANGE TO 7.5K/F.....CS27503F9009 3. PC76 CHANGE TO 1000P.....CH21006K917 4. PC9 CHANGE TO 4700P.....CH24706K911 5. PR11 CHANGE TO NC 6. PL4 CHANGE TO 10UH.....CV01044M218 ###CPU OCP function: 1. PR65 , PR57 CHANGE TO 1.2K/F.....CS21203F901 2. PR64 CHANGE TO 0.....CS00004JA07 ###2.5VSUS OCP function: 1. PR57 CHANGE TO 1.2K/F.....CS21203F901 2. PC36 CHANGE TO 100P.....CH11006J901 ###1.2VCC VOLTAGE REF: 1. PR83 CHANGE TO 10K/F.....CS31003F906 ###5VPCU RIPPLE 1. PC63 CHANGE TO 10U/25V.....CH61004M3E5 ###Shortage item: 1. PU13 CHANGE TO SC1565.....AL001565003 2. PU8 CHANGE TO LM339AD.....AL0M339M003 3. PD11 CHANGE TO 05FA20.....BC05FA20Z01 4. PD22 , PD17 , PD18 , PD19 CHANGE TO ZD5.6V....BDRLZ56BZ05 5. PD4 CHANGE TO ZD12V.....BDRLZ12BZ05						
10/08_REVB2	for Toshiba Spec change	(1) Page14 S-Video change to 4Pin from 7Pin. (CN12)						
10/13_REVB3	for Toshiba change for Toshiba spec add for Toshiba spec add for ME request	(1) Page8 clear switch change to jump pad.(del SW4 add JP1) (2) Page12 add 75ohm termination for RJ45 not use pin. (add R601-R604) (3) Page20 add Q10,R606 for Lid S4 wackup. (4) Page14 add HOLE24 for ME						
10/14_REVB4	for 5VSUS drop.	(1) Page19 Del R1,R272,R319 and U1,U23,U24 change to TI TPS2061.						
11/05_REVC1	for H/W protect for Toshiba wireless LED spec for modem cable for EMI for EMI for Lan transformer EMI for Lan waveform overshoot	(1) Page2 change R154 to 0ohm for H/W protect. (2) Page19 modify wireless-led trace. (3) Page15 add pad28-30. (4) Page20 add C801-C805-560pf. (5) Page21 add C13-560pf, CA1-470pf*4. (6) Page12 U19 change to NS681686 from NS681680. (7) Page12 move R245,R246,R241,R242 close to Lan chip.						
 PROJECT : EW3 Quanta Computer Inc. <table> <tr> <td>Size</td> <td>Document Number</td> <td>Rev</td> </tr> <tr> <td></td> <td>CHANGE LIST</td> <td>C1</td> </tr> </table> Date: Monday, November 08, 2004 Sheet 30 of 30			Size	Document Number	Rev		CHANGE LIST	C1
Size	Document Number	Rev						
	CHANGE LIST	C1						

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