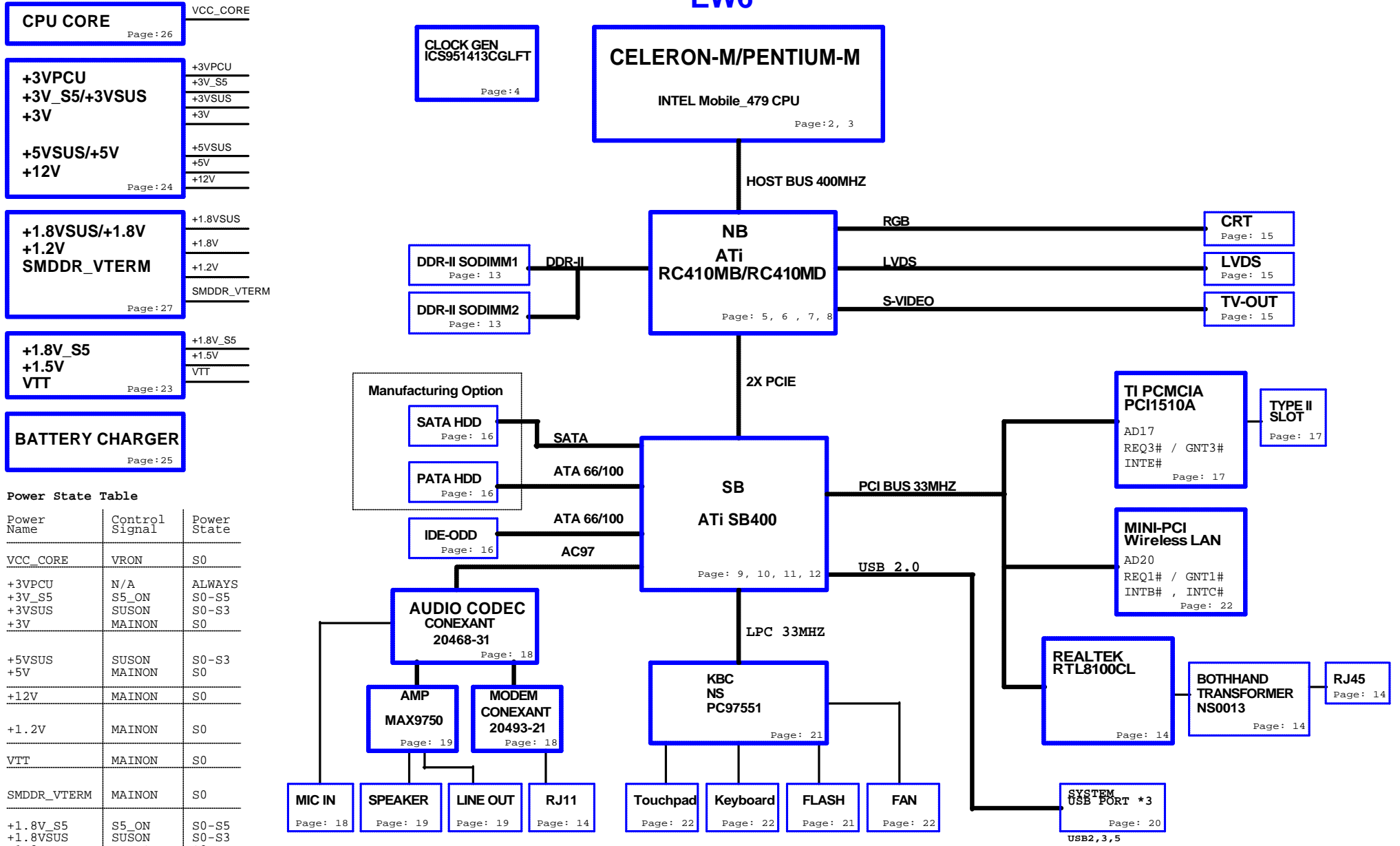


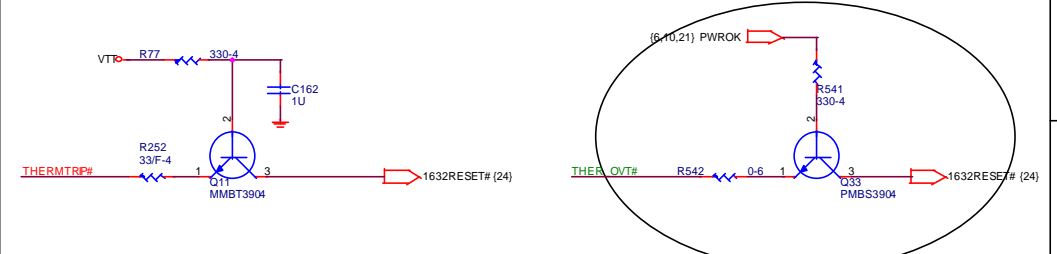
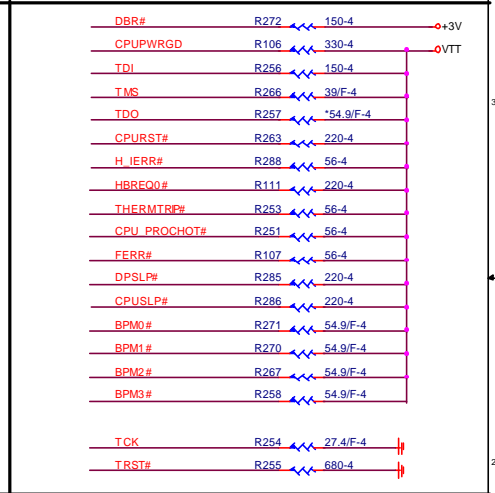
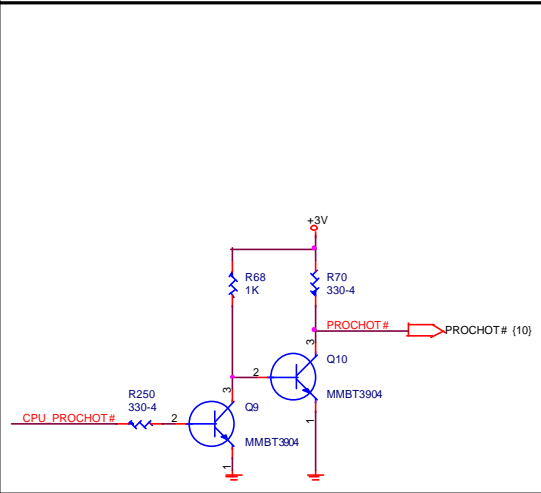
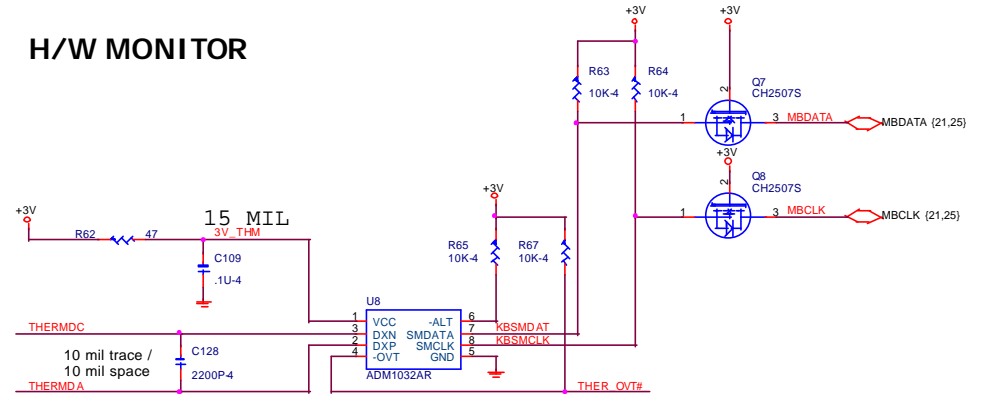
EW6



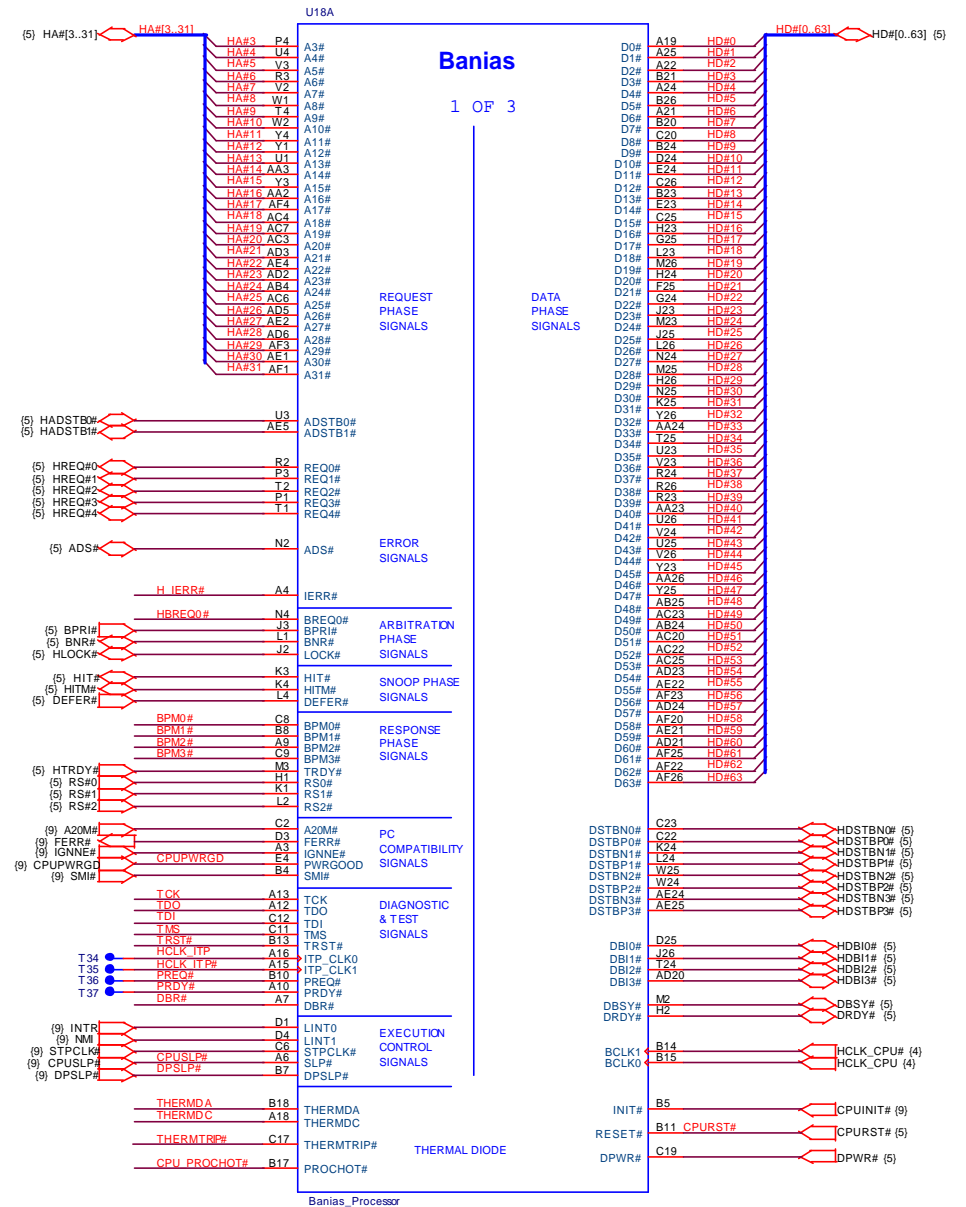
Power State Table

Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0-S5
+3VSUS	SUSON	S0-S3
+3V	MAINON	S0
+5VSUS	SUSON	S0-S3
+5V	MAINON	S0
+12V	MAINON	S0
+1.2V	MAINON	S0
VTT	MAINON	S0
SMDDDR_VTERM	MAINON	S0
+1.8V_S5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAINON	S0
+1.5V	MAINON	S0

H/W MONITOR



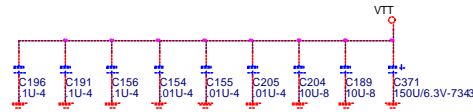
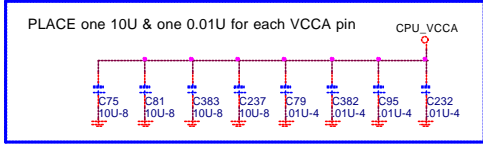
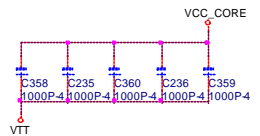
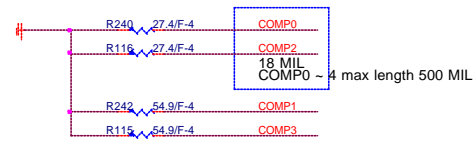
Addition Thermal shunt down 6/21 Sagem



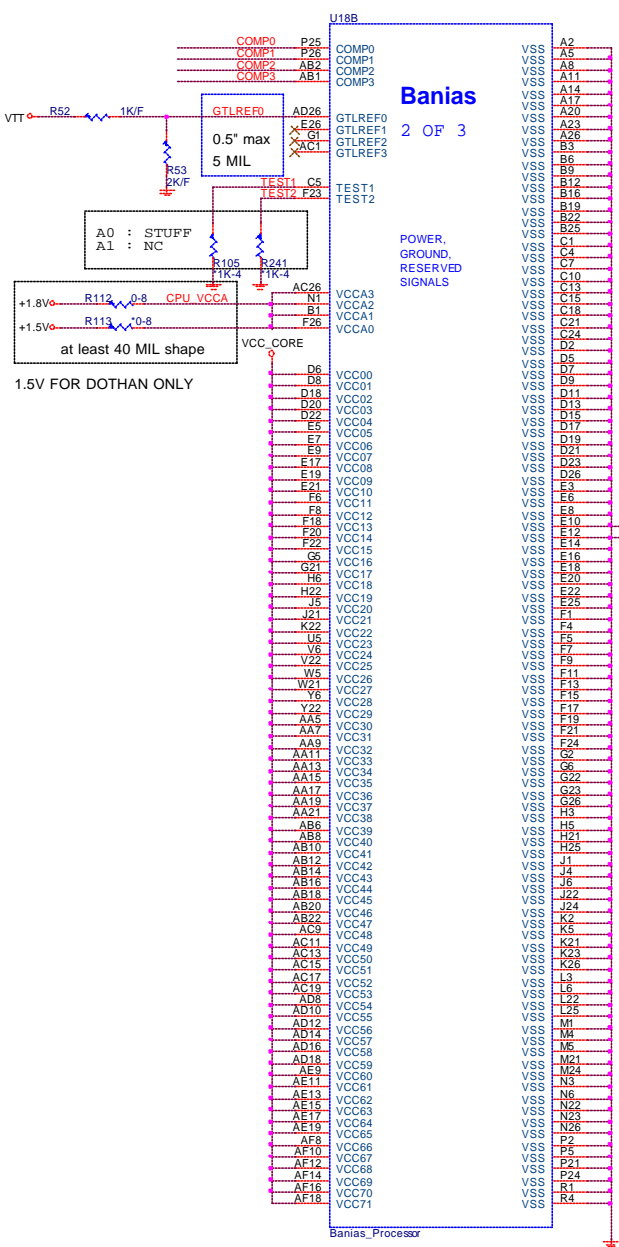
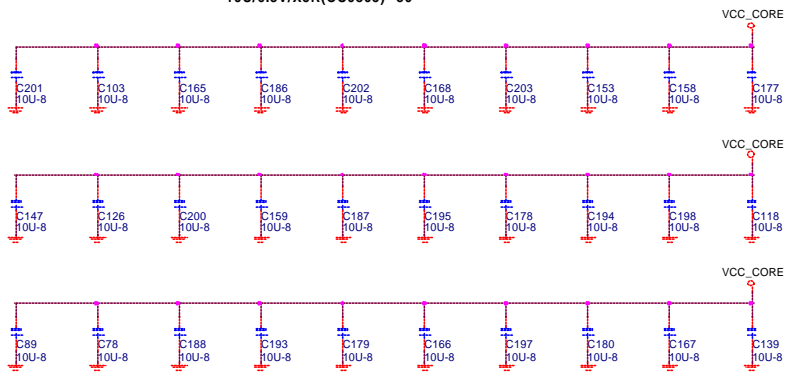
CPU

PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	CPU (HOST BUS)-1	3A
Date:	Monday, June 27, 2005	Sheet 2 of 29



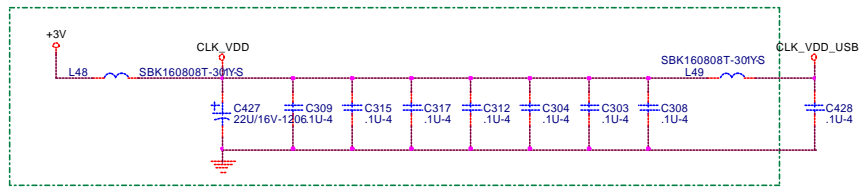
10U/6.3V/X5R(CC0805) *30



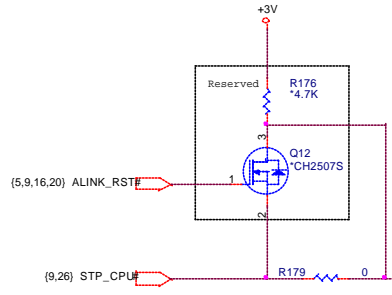
CPU

PROJECT : EW6
Quanta Computer Inc.

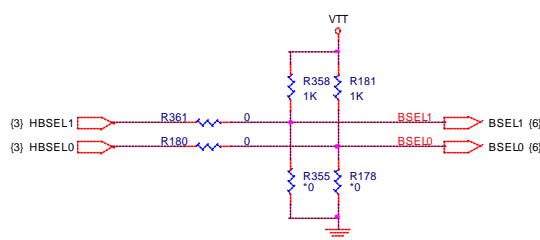
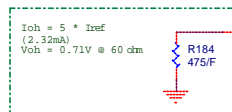
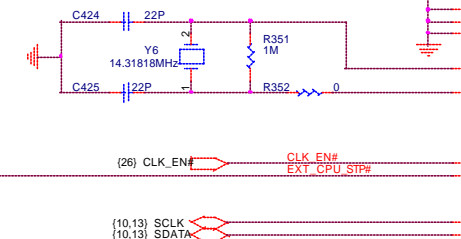
Size	Document Number	Rev
	CPU (POWER)-2	1A
Date:	Monday, June 27, 2006	Sheet 3 of 29



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U300 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U300 POWER PIN



Parallel Resonance Crystal

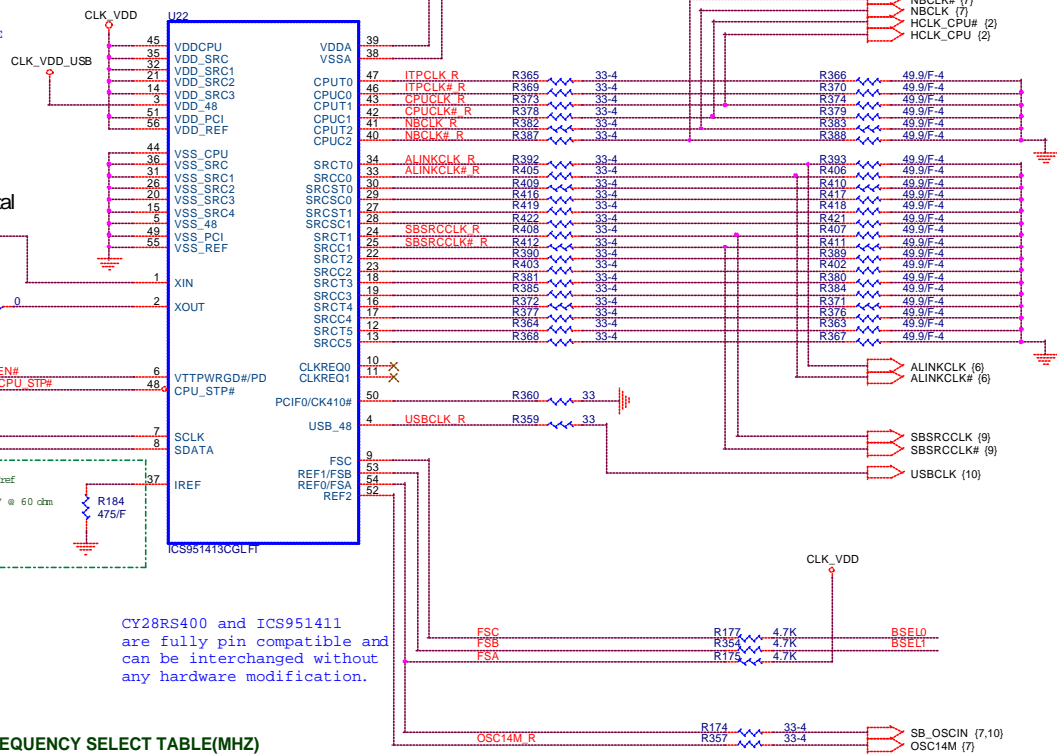


HBSEL1	HBSEL0	Frequency
0	0	133 MHz
0	1	100 MHz

CK410 FREQUENCY SELECT TABLE(MHZ)

FSC	FSA	FSA	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Rsvd

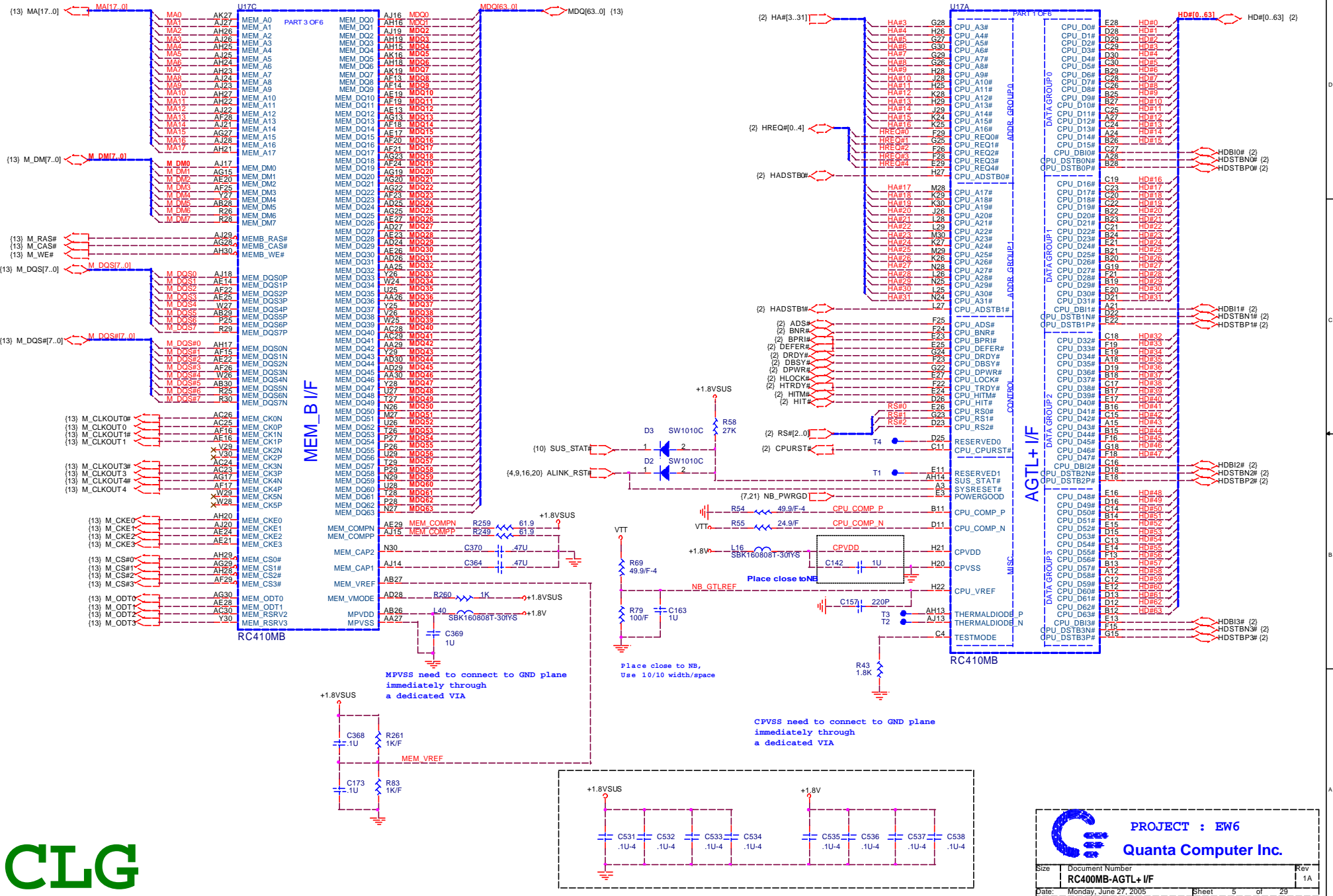
CY28RS400 and ICS951411 are fully pin compatible and can be interchanged without any hardware modification.

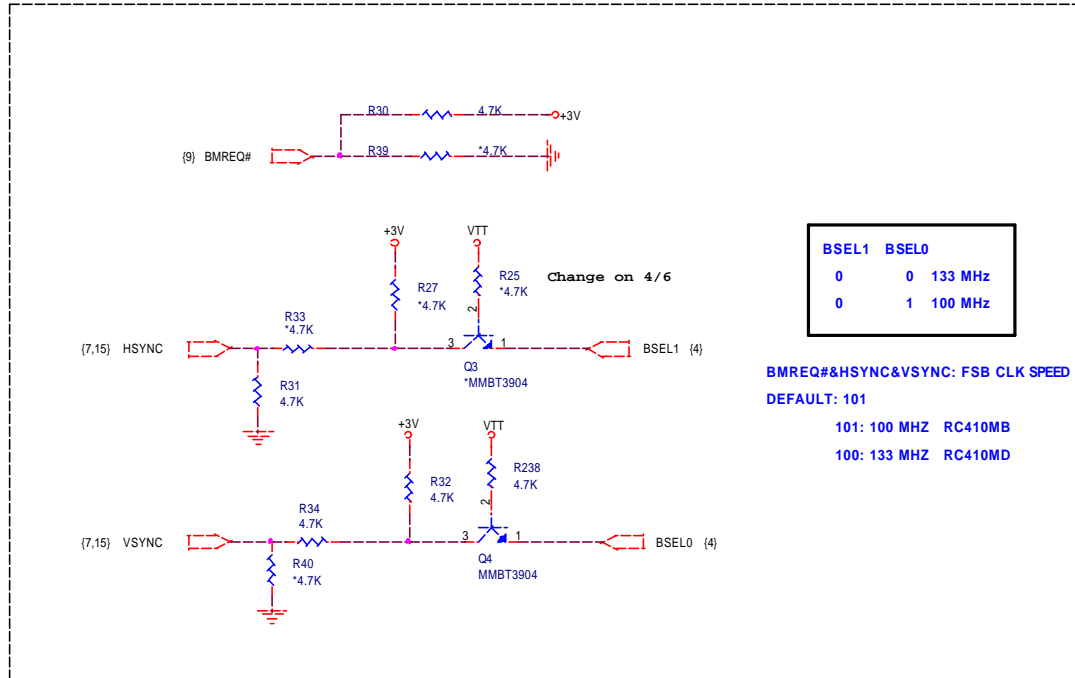


CLK

PROJECT : EW6
Quanta Computer Inc.

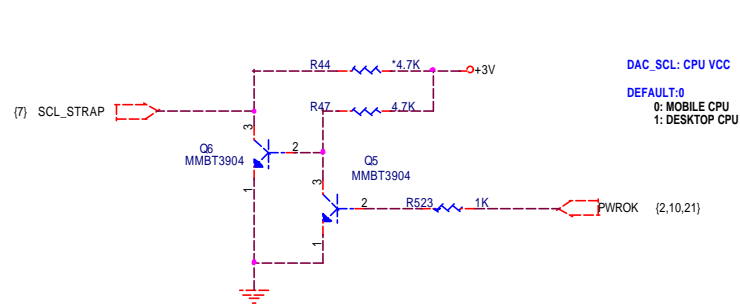
Size: Document Number: **EXTERNAL CLKNG** Rev: 1B
 Date: Monday, June 27, 2005 Sheet: 4 of 29





BSEL1	BSEL0	FSB CLK SPEED
0	0	133 MHz
0	1	100 MHz

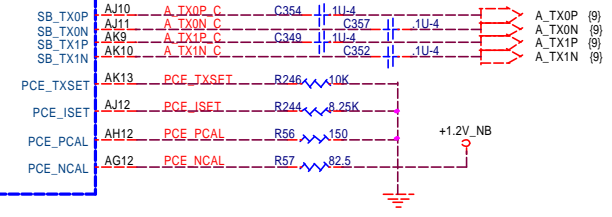
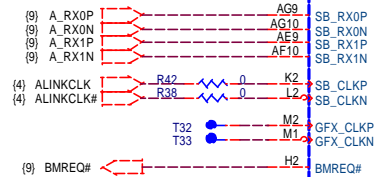
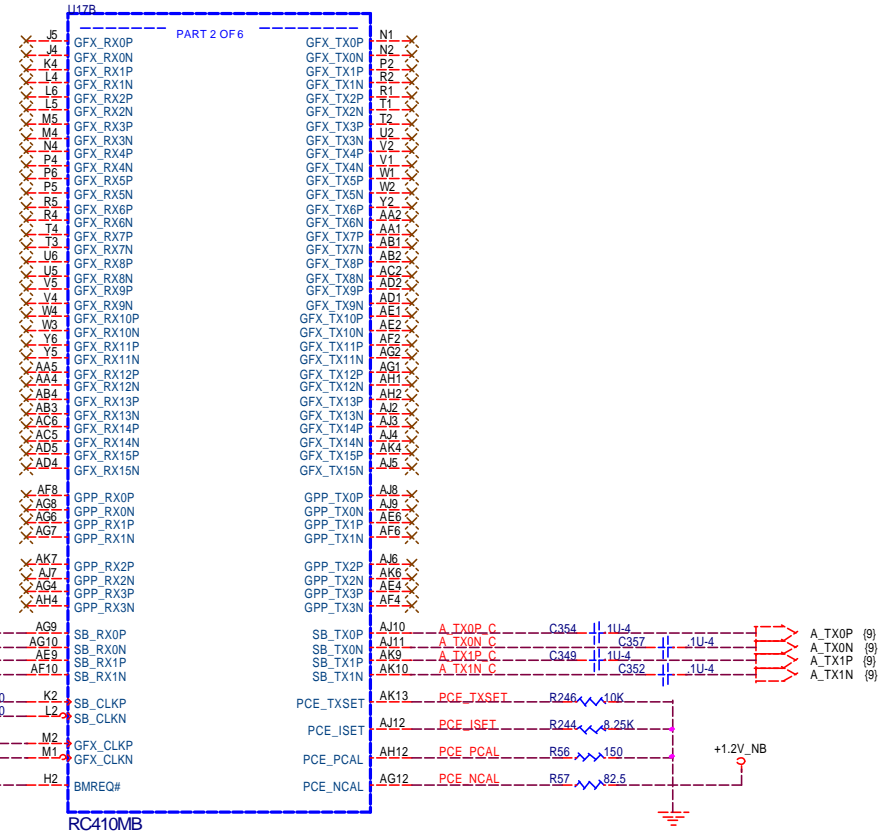
BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
DEFAULT: 101
 101: 100 MHZ RC410MB
 100: 133 MHZ RC410MD



DAC_SCL: CPU VCC
DEFAULT: 0
 0: MOBILE CPU
 1: DESKTOP CPU

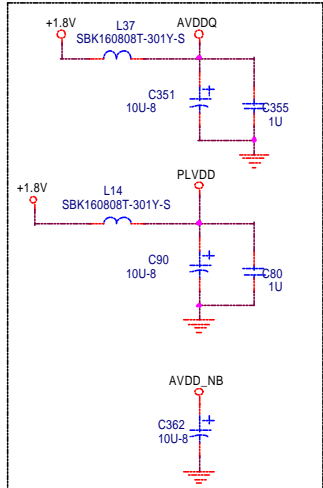


STRP_DATA: Debug strap
DEFAULT: 1
 0: MEMORY CHANNEL STRAPING
 1: EPROM STRAPING



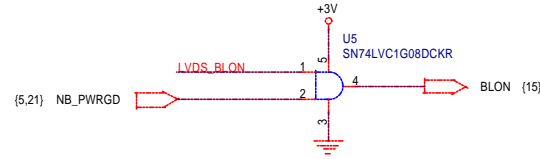
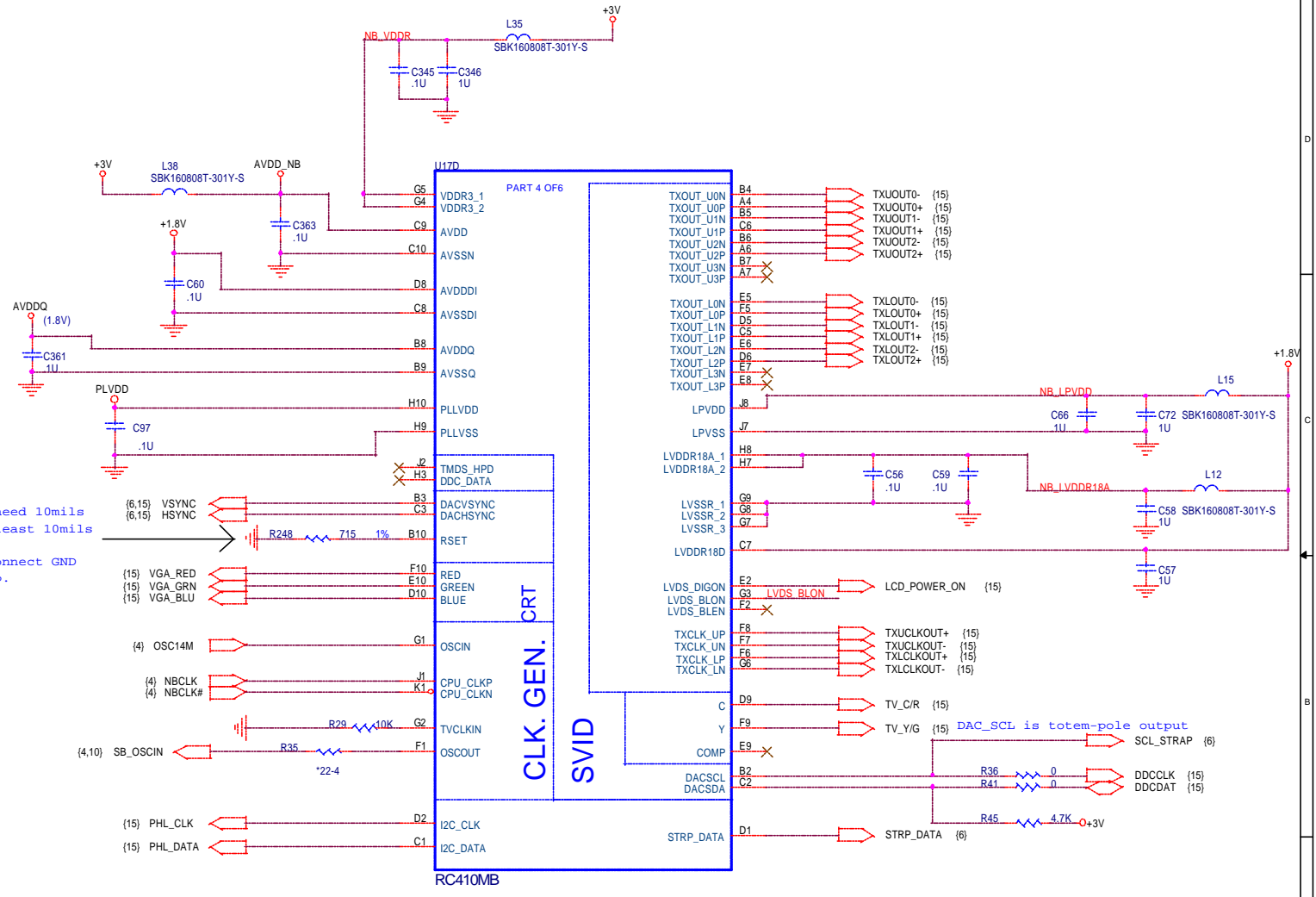
PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	RC400MB-PCIE LINK I/F	2A
Date	Monday, June 27, 2005	Sheet 6 of 29



PUT AVDD_NB, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS

RSET resistor need 10mils trace with at least 10mils spacing. Also need to connect GND at AVSSQ HF cap.

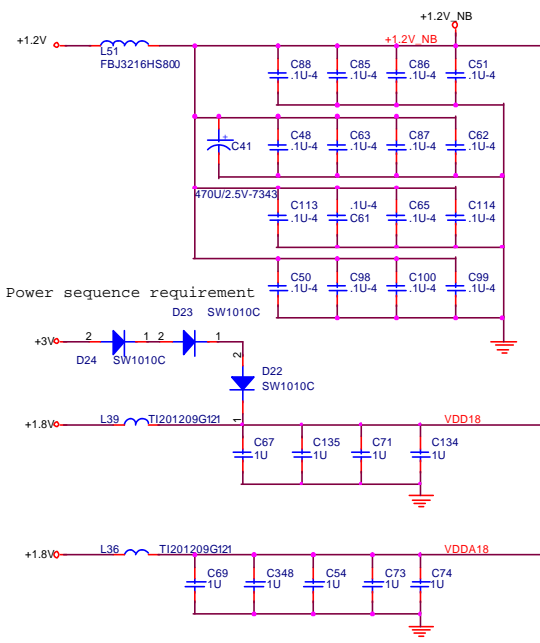


PROJECT : EW6
Quanta Computer Inc.

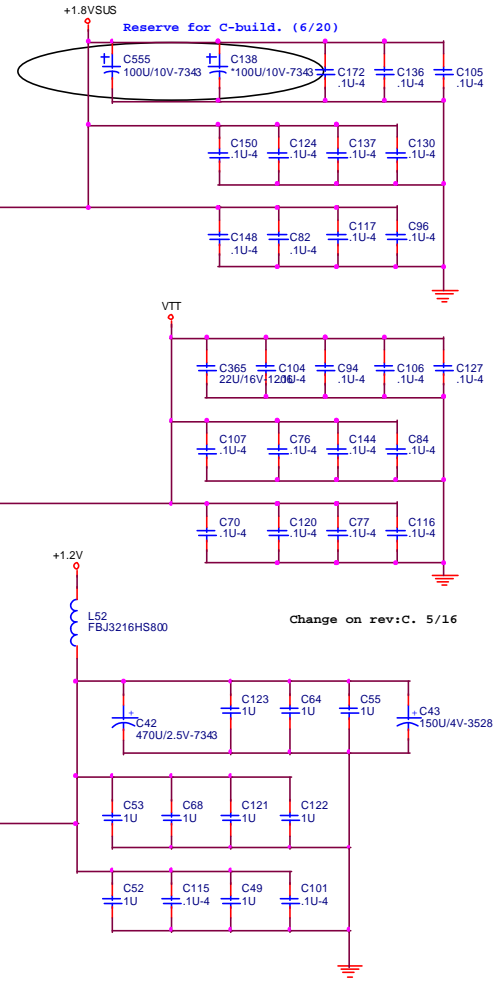
Size	Document Number	Rev
	RC400MB-VIDEO & CLKGEN	1B
Date:	Monday, June 27, 2005	Sheet 7 of 29

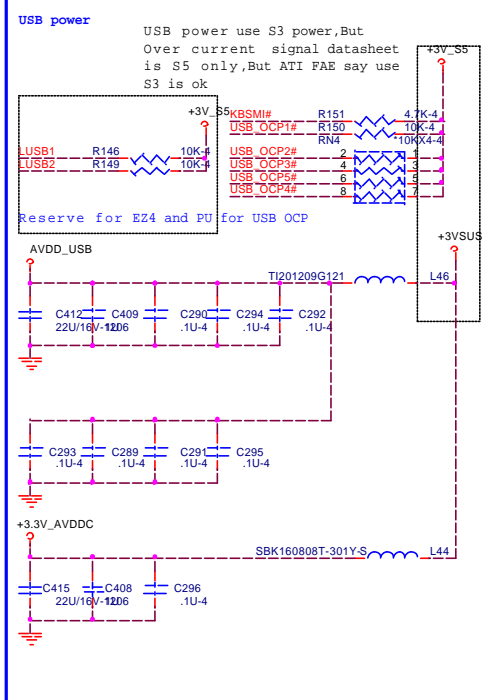
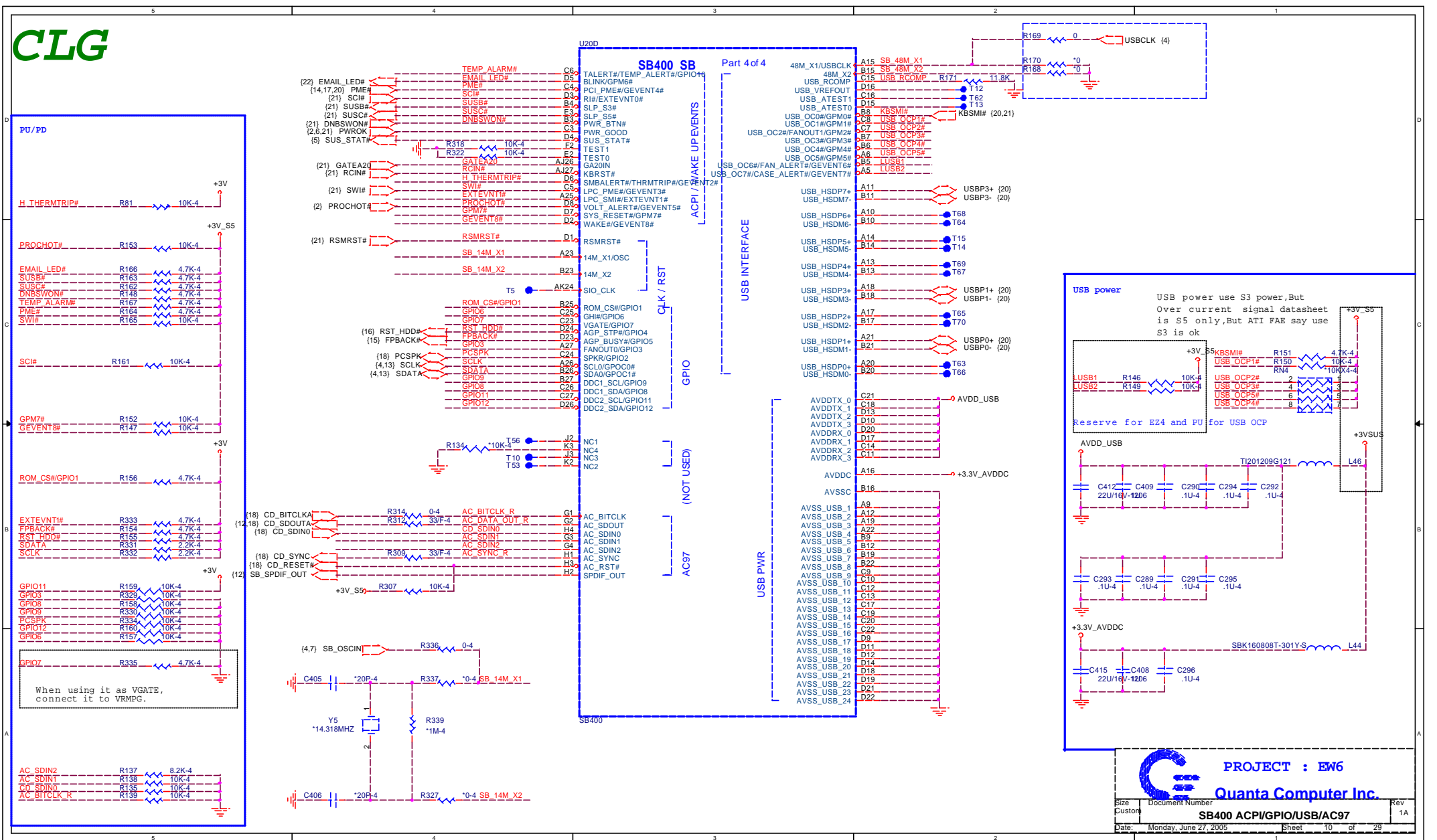
Change on rev:C. 5/16

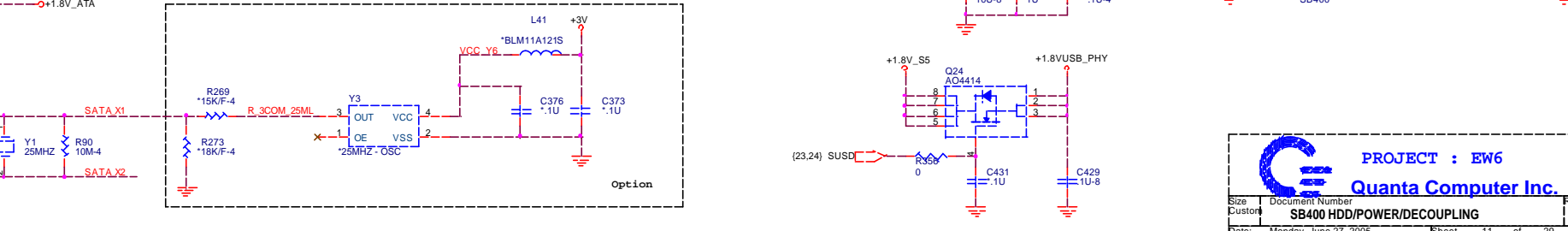
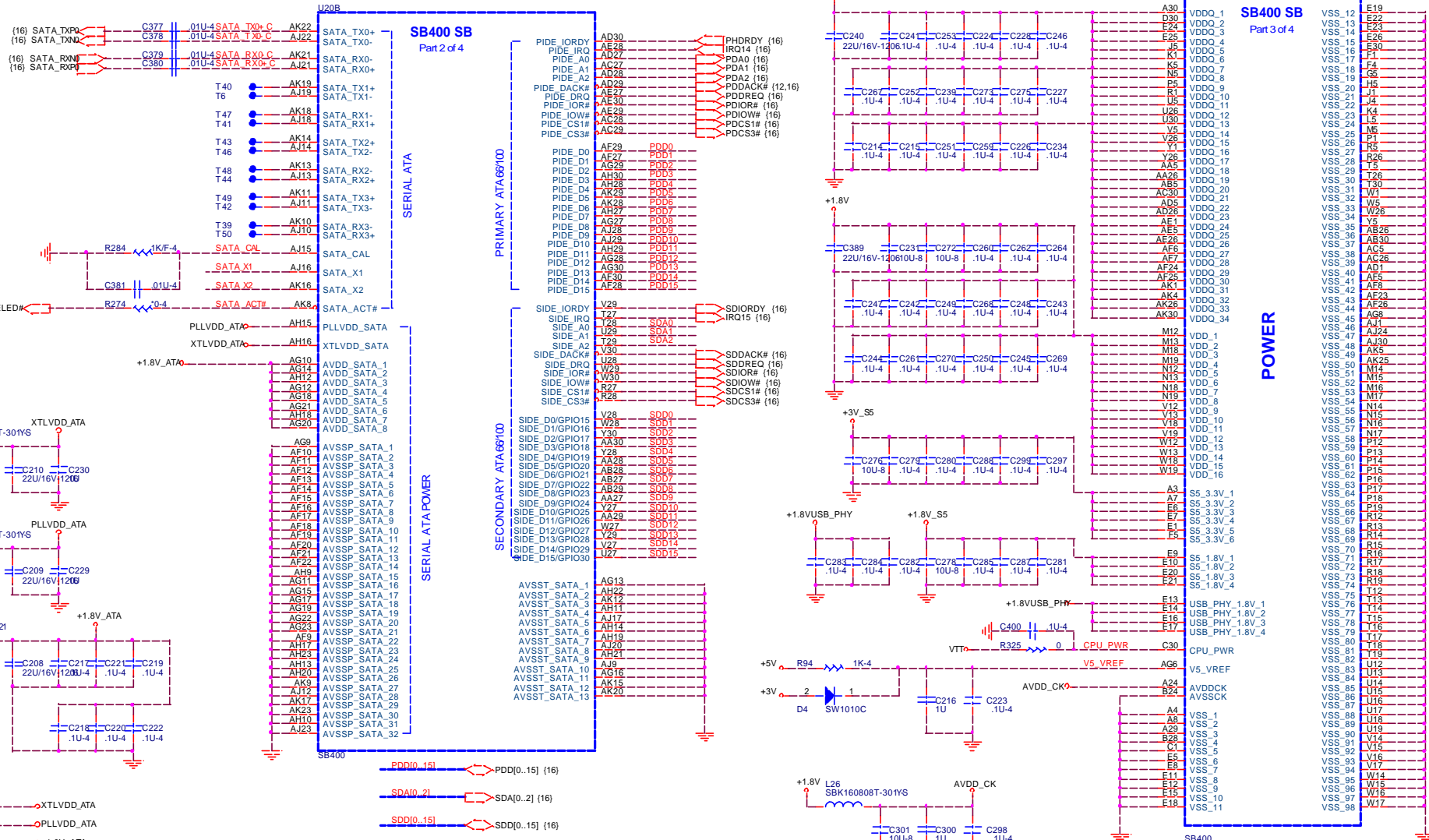
W5	VSS#U5	VSS#M15	M14
W6	VSSA#U6	VSS#C14	AC14
AB5	VSSA#Y5	VSS#R18	AC16
Y8	VSSA#Y6	VSS#G27	A22
V7	VSSA#P8	VSS#G3	D27
AA8	VSSA#P7	VSS#H13	AC26
AA7	VSSA#U8	VSS#H14	H18
AD7	VSSA#U7	VSS#H18	A16
AD8	VSSA#Y7	VSS#H23	A9
R8	VSSA#Y8	VSS#H4	AD17
N8	VSSA#L8	VSS#J24	J24
R7	VSSA#K7	VSS#J24	R27
N7	VSSA#AD7	VSS#J30	D24
AF7	VSSA#A2	VSS#K27	T30
AE8	VSSA#AF5	VSS#U19	M16
AG5	VSSA#AC6	VSS#U19	AD11
T6	VSSA#AC5	VSS#M16	VSS#AD11
T5	VSSA#P6	VSS#M30	VSS#M30
N6	VSSA#P5	VSS#N15	H15
N5	VSSA#L6	VSS#N15	N15
AH5	VSSA#L5	VSS#N16	D3
K5	VSSA#H6	VSS#N23	A25
AH3	VSSA#H6	VSS#N27	F3
AH7	VSSA#P4	VSS#G5	F3
AH7	VSSA#AE3	VSS#P15	P16
AD3	VSSA#AD3	VSS#P16	P16
AH6	VSSA#AC3	VSS#P23	G10
AC3	VSSA#AA3	VSS#P24	M24
AA3	VSSA#Y3	VSS#R12	R13
Y3	VSSA#P3	VSS#R13	P12
U3	VSSA#U3	VSS#R14	P14
U3	VSSA#R3	VSS#R15	P13
R3	VSSA#P3	VSS#R16	R17
P3	VSSA#M3	VSS#R17	V18
M3	VSSA#L3	VSS#R18	R18
L3	VSSA#J3	VSS#R19	R23
AF5	VSSA#H3	VSS#R23	R24
AF3	VSSA#F3	VSS#R24	M24
AF9	VSSA#N3	VSS#R30	J30
AH9	VSSA#AG3	VSS#T12	T12
AH10	VSSA#AE9	VSS#T13	T14
AC20	VSSA#H7	VSS#T14	M13
J23	VSSA#A15	VSS#T15	P18
A29	VSSA#A24	VSS#T16	P18
W30	VSSA#A29	VSS#T17	U17
W23	VSSA#A23	VSS#T18	V19
AA28	VSSA#A24	VSS#T19	J27
AJ30	VSSA#A30	VSS#T27	J27
AC12	VSSA#AB27	VSS#U15	N17
AC15	VSSA#C12	VSS#U16	M18
K8	VSSA#C16	VSS#V15	M18
AD12	VSSA#C8	VSS#V16	V17
AD15	VSSA#D12	VSS#W16	M26
AD18	VSSA#D16	VSS#W27	V12
AC17	VSSA#D19	VSS#Y12	U13
AE50	VSSA#D23	VSS#Y13	V14
AD14	VSSA#D30	VSS#Y14	W15
AC11	VSSA#D9	VSS#Y23	U23
AF12	VSSA#E12	VSS#Y24	A13
AF27	VSSA#E27	VSS#Y19	V28
AC18	VSSA#E19	VSS#Y28	V28
AG14	VSSA#C19	VSS#C17	VSS#AH26
F4	VSSA#G12	VSS#AH26	AG24
AG18	VSSA#F7	VSS#AH25	AA24
AG21	VSSA#G18	VSS#AG25	AA23
AK25	VSSA#G21	VSS#F30	F30
V27	VSSA#G9	VSS#F25	K23
A11	VSSA#H28	VSS#D27	D20
AD20	VSSA#J1	VSS#D25	A19
AK12	VSSA#K10	VSS#D23	D14
AK15	VSSA#K13	VSS#D20	F27
AK18	VSSA#K16	VSS#D17	D4
AK2	VSSA#K19	VSS#C3	M23
AH11	VSSA#K2	VSS#C28	B30
13	VSSA#H11	VSS#B30	B1
AC27	VSSA#J11	VSS#B1	AK29
	VSSA#K25	VSS#AK29	AK22
		VSS#AK22	



U16	VDD_CORE#M12	VDD_MEM#AB30	Y24
M13	VDD_CORE#M13	VDD_MEM#A121	AC21
M15	VDD_CORE#M14	VDD_MEM#AK21	AD21
M17	VDD_CORE#M17	VDD_MEM#AC13	AC13
R16	VDD_CORE#M18	VDD_MEM#AC14	AC16
V15	VDD_CORE#M19	VDD_MEM#AC15	AD19
N12	VDD_CORE#N12	VDD_MEM#AC18	AD22
T15	VDD_CORE#N13	VDD_MEM#AD15	V23
N14	VDD_CORE#N14	VDD_MEM#AD16	AD13
N16	VDD_CORE#N17	VDD_MEM#AD17	AD16
N18	VDD_CORE#N18	VDD_MEM#AD18	AC19
N19	VDD_CORE#N19	VDD_MEM#AD18	AB24
R12	VDD_CORE#P12	VDD_MEM#AE15	AK24
P13	VDD_CORE#P13	VDD_MEM#AE15	T24
P15	VDD_CORE#P15	VDD_MEM#AE18	AK28
P17	VDD_CORE#P17	VDD_MEM#AE18	AB23
P19	VDD_CORE#P19	VDD_MEM#AG27	Y23
U12	VDD_CORE#U12	VDD_MEM#A130	AC19
T13	VDD_CORE#U13	VDD_MEM#AK18	AK21
U14	VDD_CORE#U14	VDD_MEM#AK24	T23
T17	VDD_CORE#U17	VDD_MEM#AK24	V24
U18	VDD_CORE#U18	VDD_MEM#AK9	AC22
T19	VDD_CORE#U19		
Y13	VDD_CORE#V13	VDD_CPU#H17	H11
R14	VDD_CORE#V14	VDD_CPU#H19	H13
V17	VDD_CORE#V17	VDD_CPU#K23	G20
R18	VDD_CORE#V18	VDD_CPU#L23	L24
Y19	VDD_CORE#V19	VDD_CPU#L24	P23
W12	VDD_CORE#W12	VDD_CPU#M23	N23
W14	VDD_CORE#W14	VDD_CPU#M24	G17
W16	VDD_CORE#W16	VDD_CPU#T23	G17
W18	VDD_CORE#W18	VDD_CPU#U23	H14
J9	VDD_18	VDD_CPU#U24	F17
AB22	VDD_18#AF26	VDD_CPU#V24	G14
J22	VDD_18#AF9	VDD_CPU#W23	A10
Y3	VDDA_18#J26	VDD_CPU#X23	H16
U8	VDDA_18#U8	VDD_CPU#Y22	H23
AB8	VDDA_18#AD8	VDD_CPU#Z22	H12
Y7	VDDA_18#W6	VDD_CPU#F19	F12
U7	VDDA_18#AA8	VDD_CPU#F15	G12
AE11	VDDA_18#AA7	VDD_CPU#E15	F11
AC9	VDDA_18#AE7	VDD_CPU#E16	P24
AD10	VDDA_18#AD7	VDD_CPU#H16	H19
AC10	VDDA_18#AC8	VDD_CPU#H16	H19
AG11	VDDA_18#AC7	VDD_CPU#H15	G11
AF11	VDDA_18#AG6	VDD_CPU#G22	H24
	VDDA_18#AF6	VDD_CPU#G19	G13
H5	VDDA_12#N8	VDDA_12#N8	AC8
H4	VDDA_12#K6	VDDA_12#C3	K6
P8	VDDA_12#K4	VDDA_12#R7	T8
P7	VDDA_12#F6	VDDA_12#R8	T7
L7	VDDA_12#F5	VDDA_12#U7	U7
L8	VDDA_12#B3	VDDA_12#B2	W8
J6	VDDA_12#A3	VDDA_12#W7	W7
AC7	VDDA_12#A4	VDDA_12#L7	AD9
AB7	VDDA_12#M8	VDDA_12#L8	

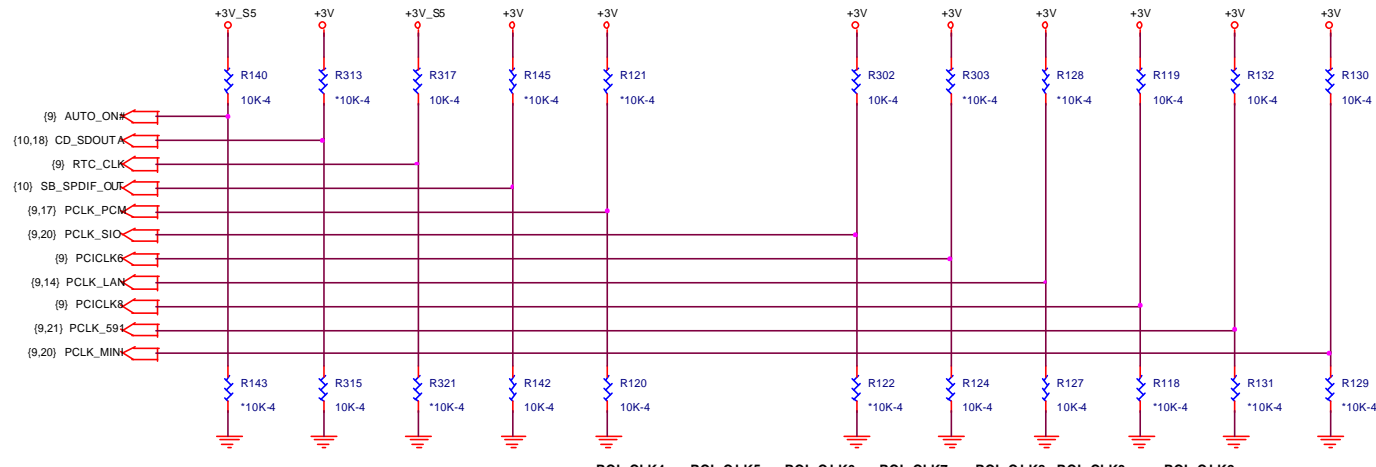






PROJECT : EW6
Quanta Computer Inc.

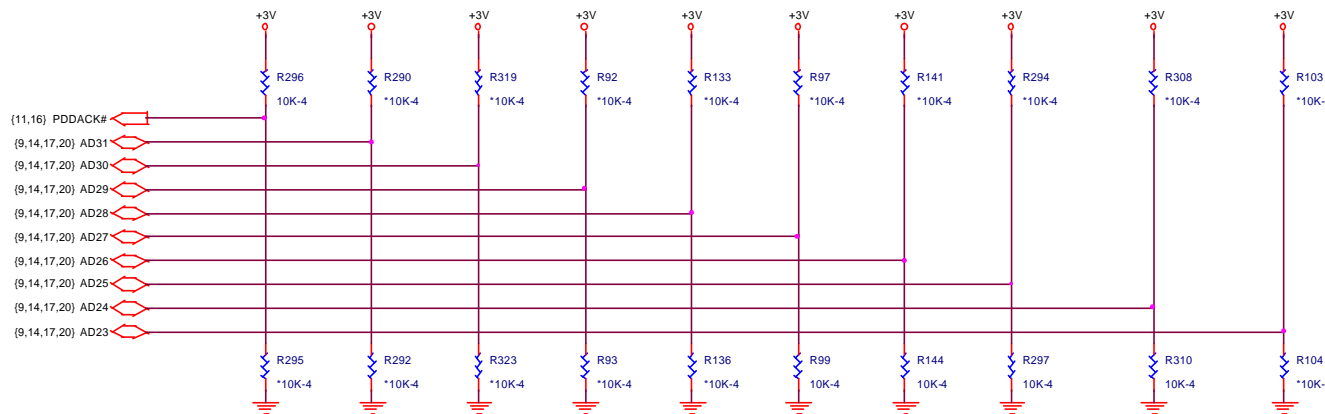
Size: Document Number: SB400 HDD/POWER/DECOUPLING Rev: 1A
 Date: Monday, June 27, 2005 Sheet: 11 of 29



REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3	PCI_CLK2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space) L,H = LPC ROM II DEFAULT (addresses mapped to below 1M) L,L = FWH ROM	USB PHY PW RDOWN DISABLE DEFAULT		48MHz OSC/Clock Buffer
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT		USB PHY PW RDOWN ENABLE		48MHz Crystal Pad DEFAULT

*This strap is only required if the strap on PCICLK4 is configured for External Clock.



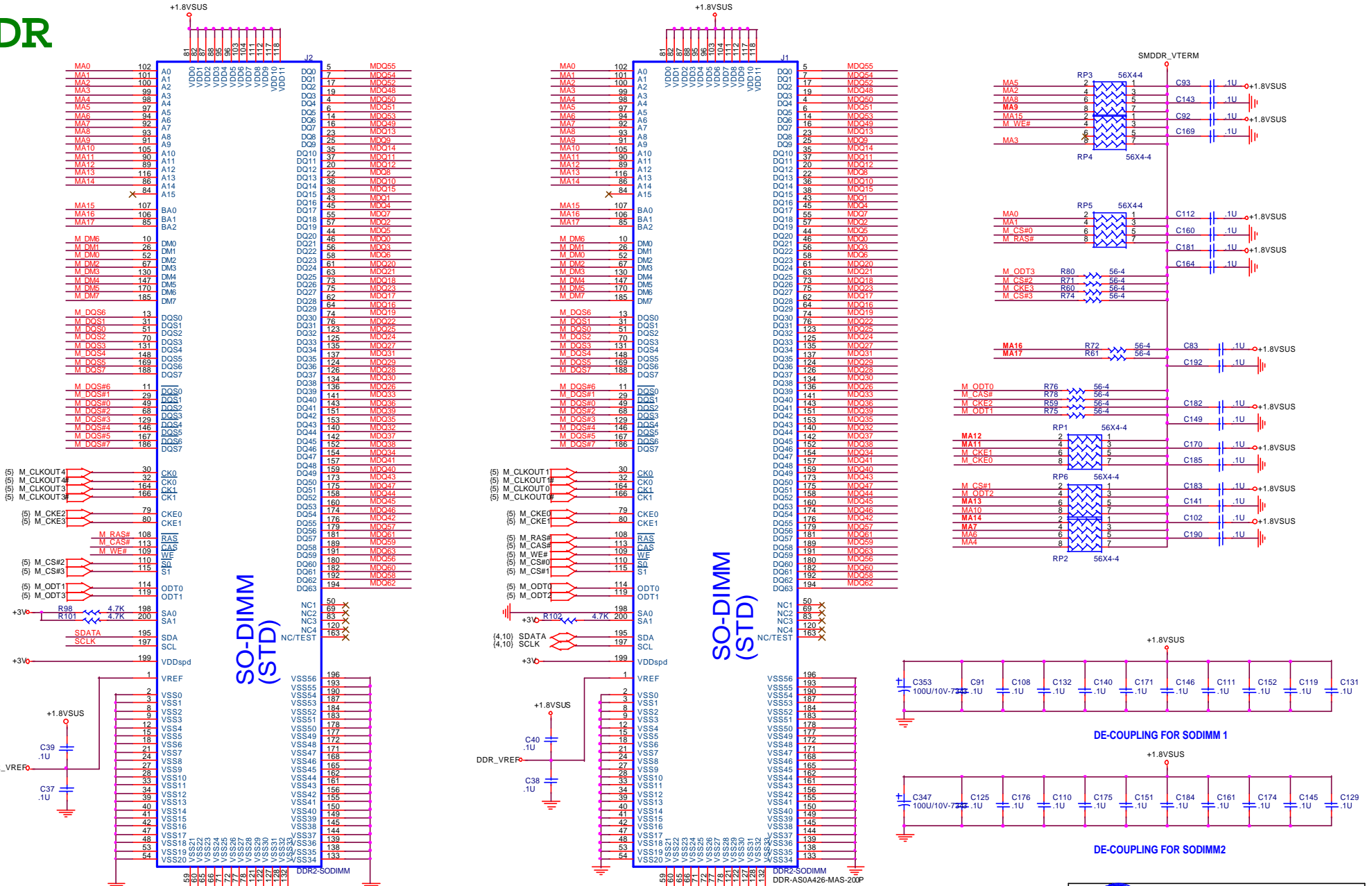
DEBUG STRAPS

	PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

DDR

+1.8VSUS

+1.8VSUS



SO-DIMM (STD)

SO-DIMM (STD)

PROJECT : EW6
Quanta Computer Inc.

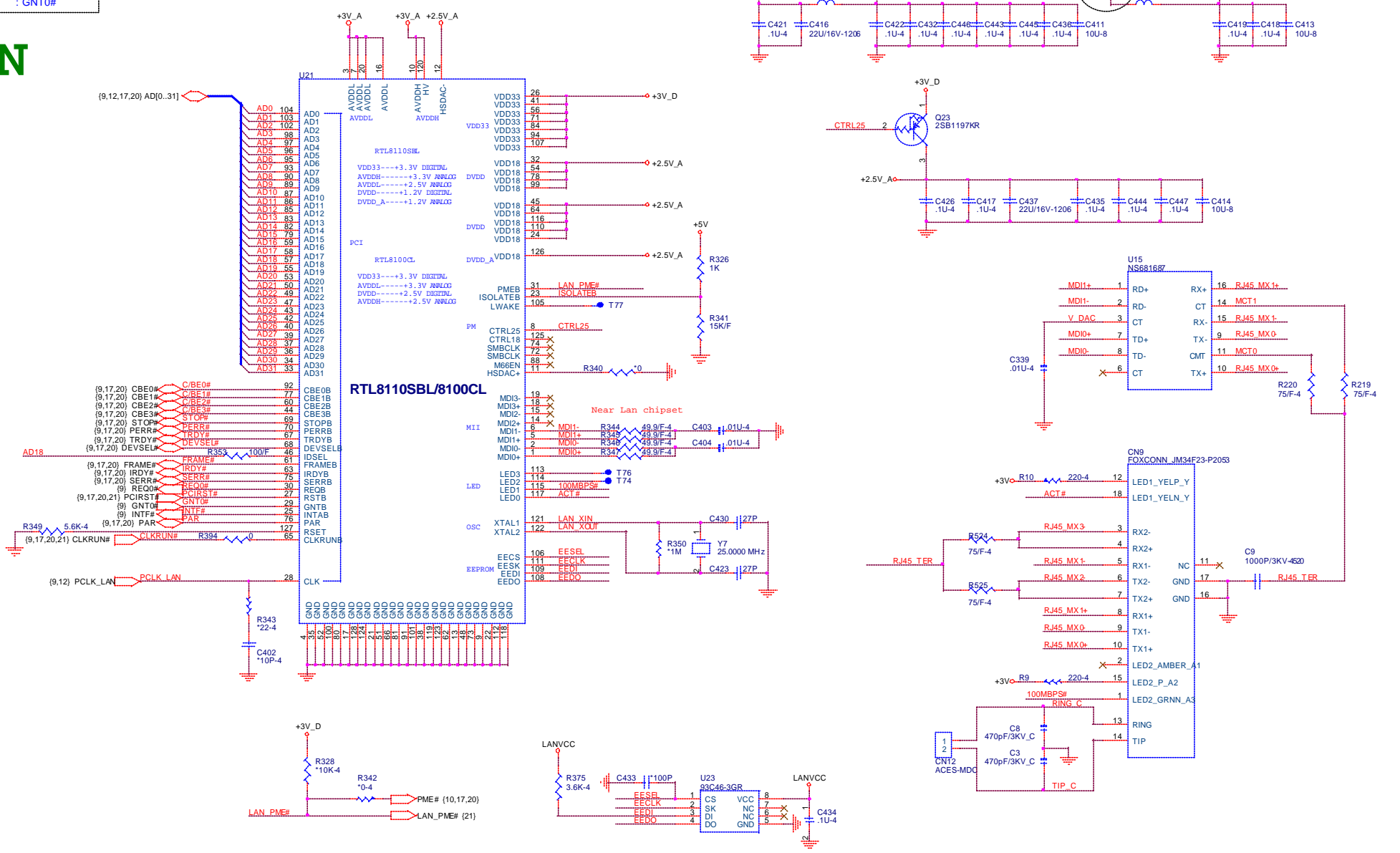
Size: Document Number
DDR2 SO-DIMM

Date: Monday, June 27, 2005 Sheet 13 of 29 Rev 1B

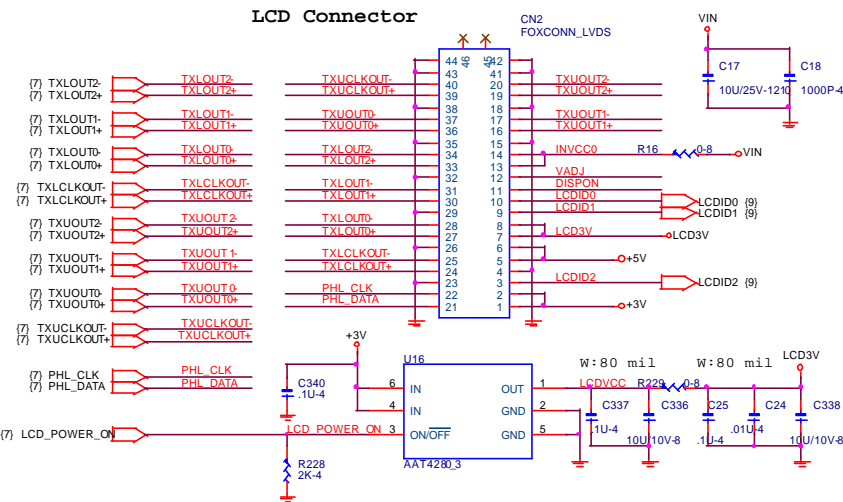
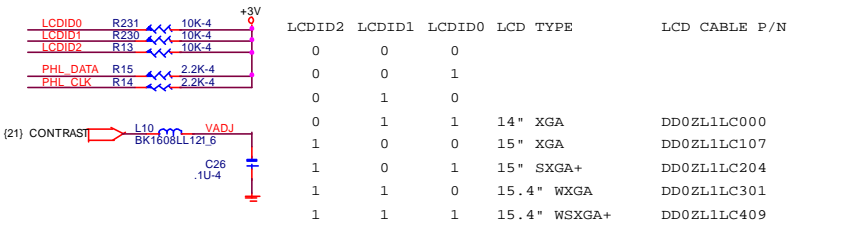
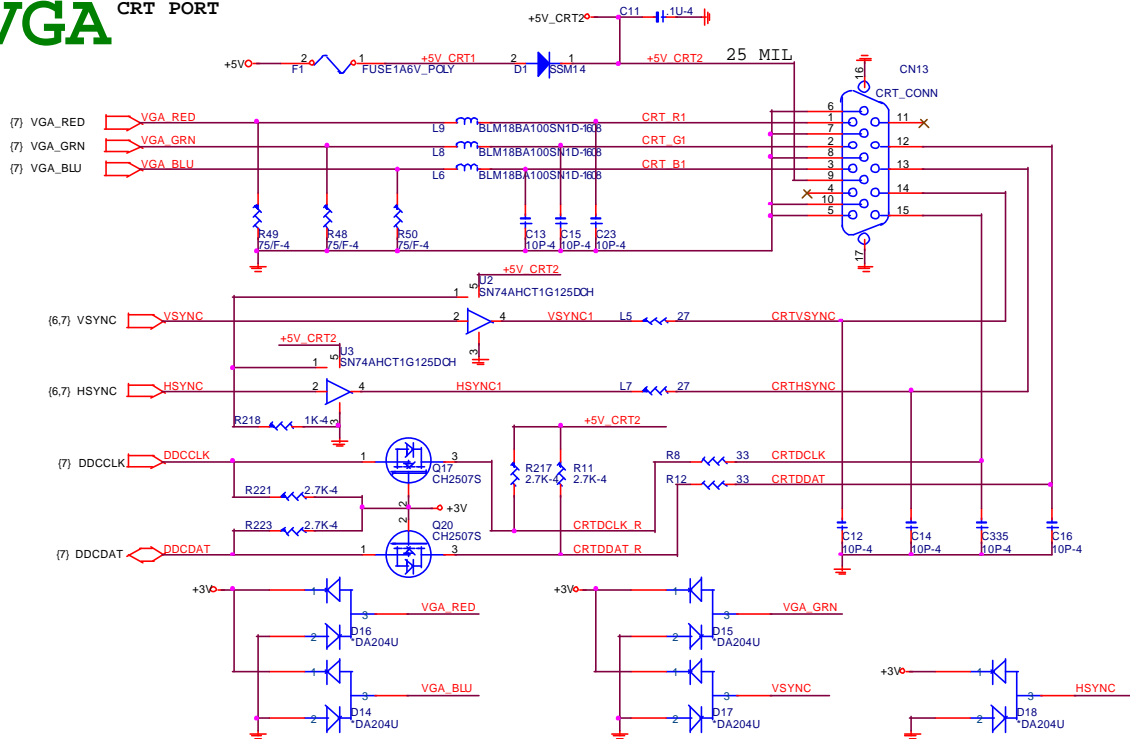
- (5) MDQ[63..0] M_DQI63_01
- (5) M_DM[7..0] M_DM17_01
- (5) M_DQS[7..0] M_DQSI7_01
- (5) M_DQS#1[7..0] M_DQS#17_01
- (5) MA[17..0] MA117_01

ID Select : AD18
 Interrupt Pin : INTD#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#

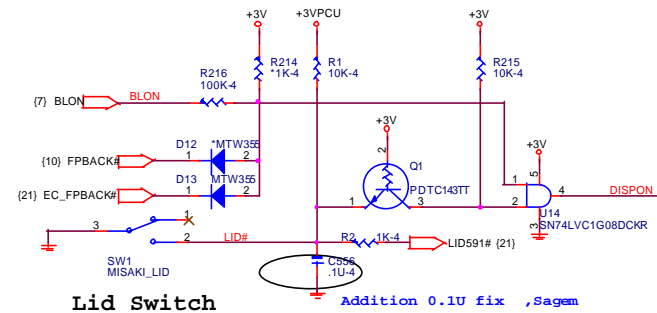
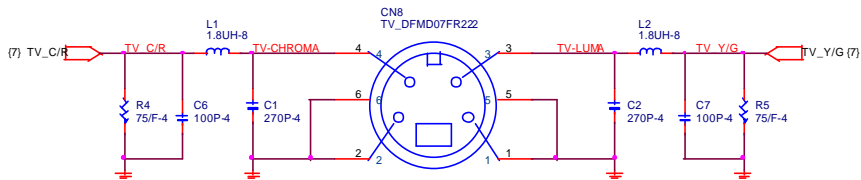
LAN



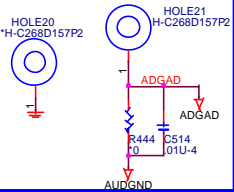
VGA CRT PORT



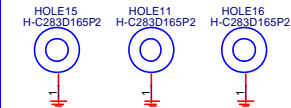
S-VIDEO



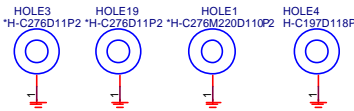
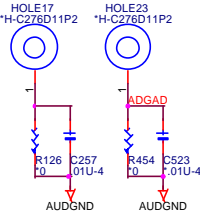
FOR MODEM MODULE



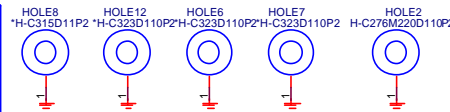
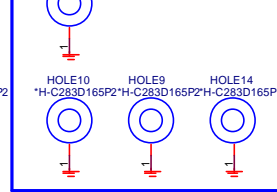
FOR CPU HEATSINK



OTH

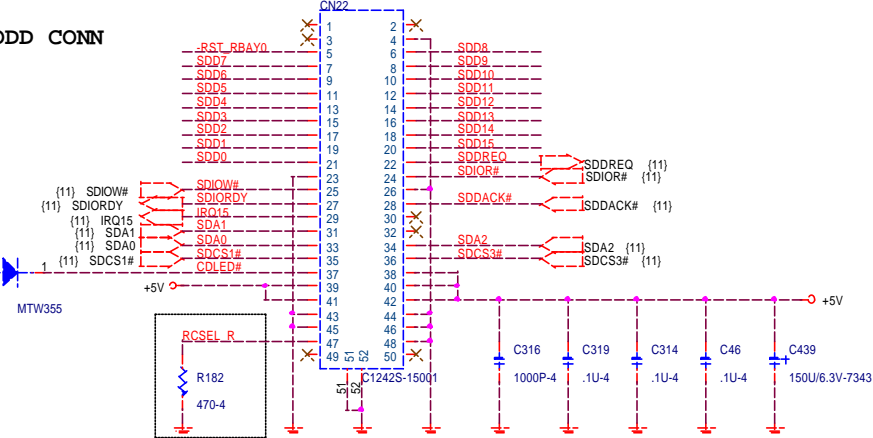
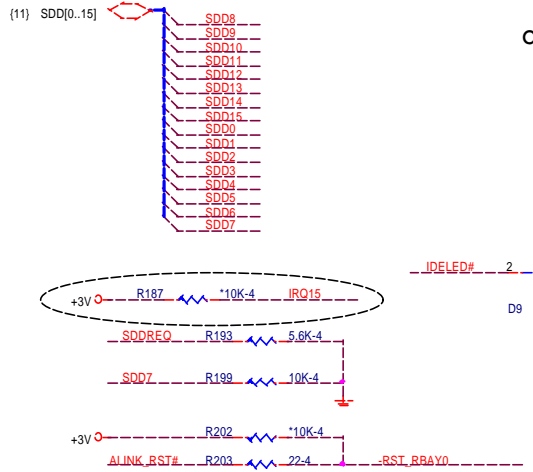
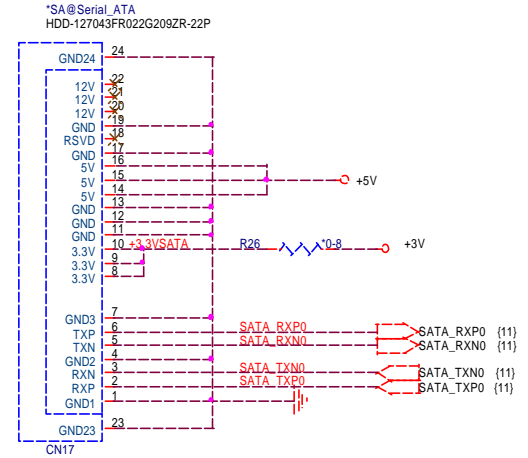
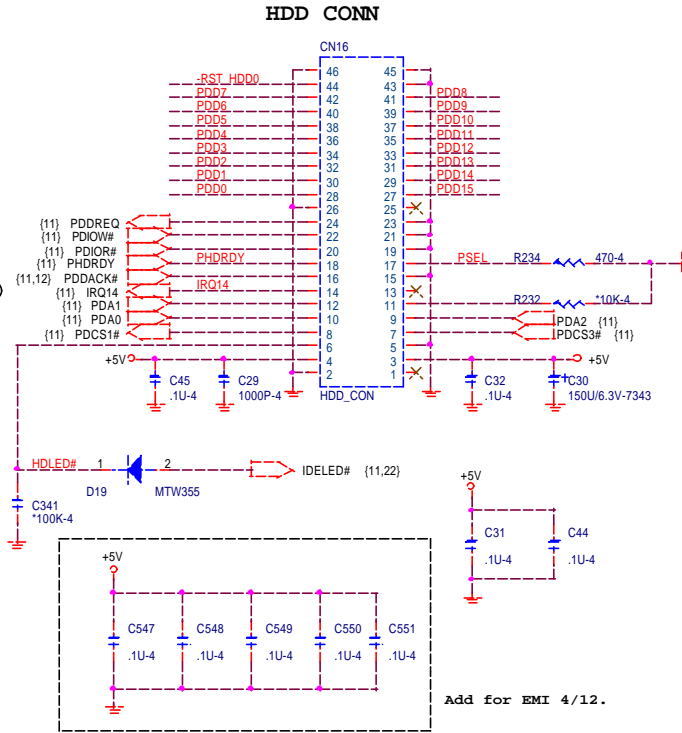
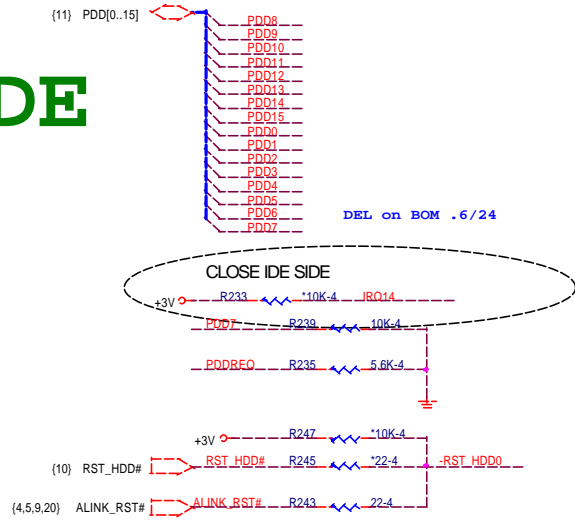


FOR NB HEATSINK



FOR M/B HOLE

IDE

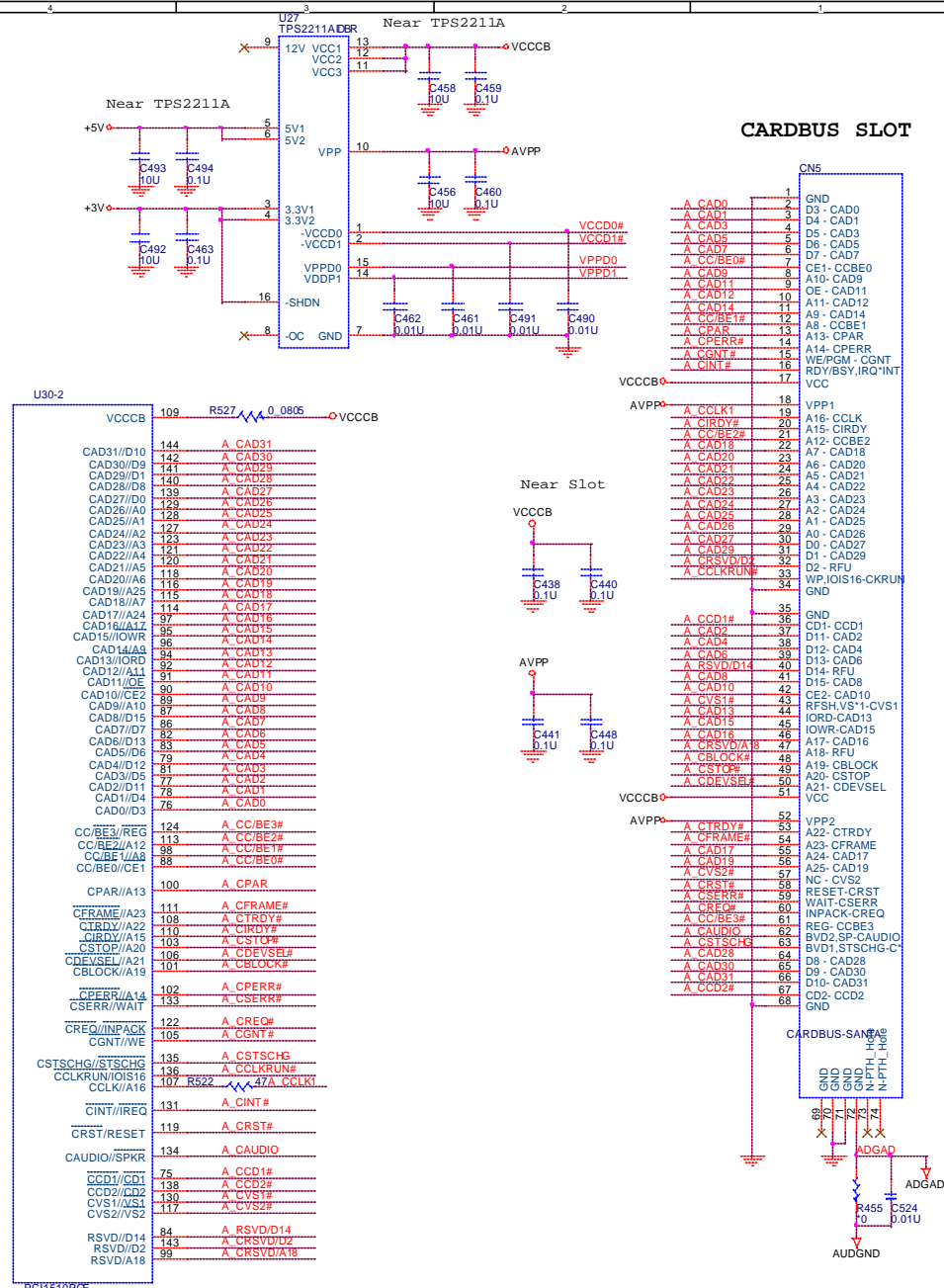
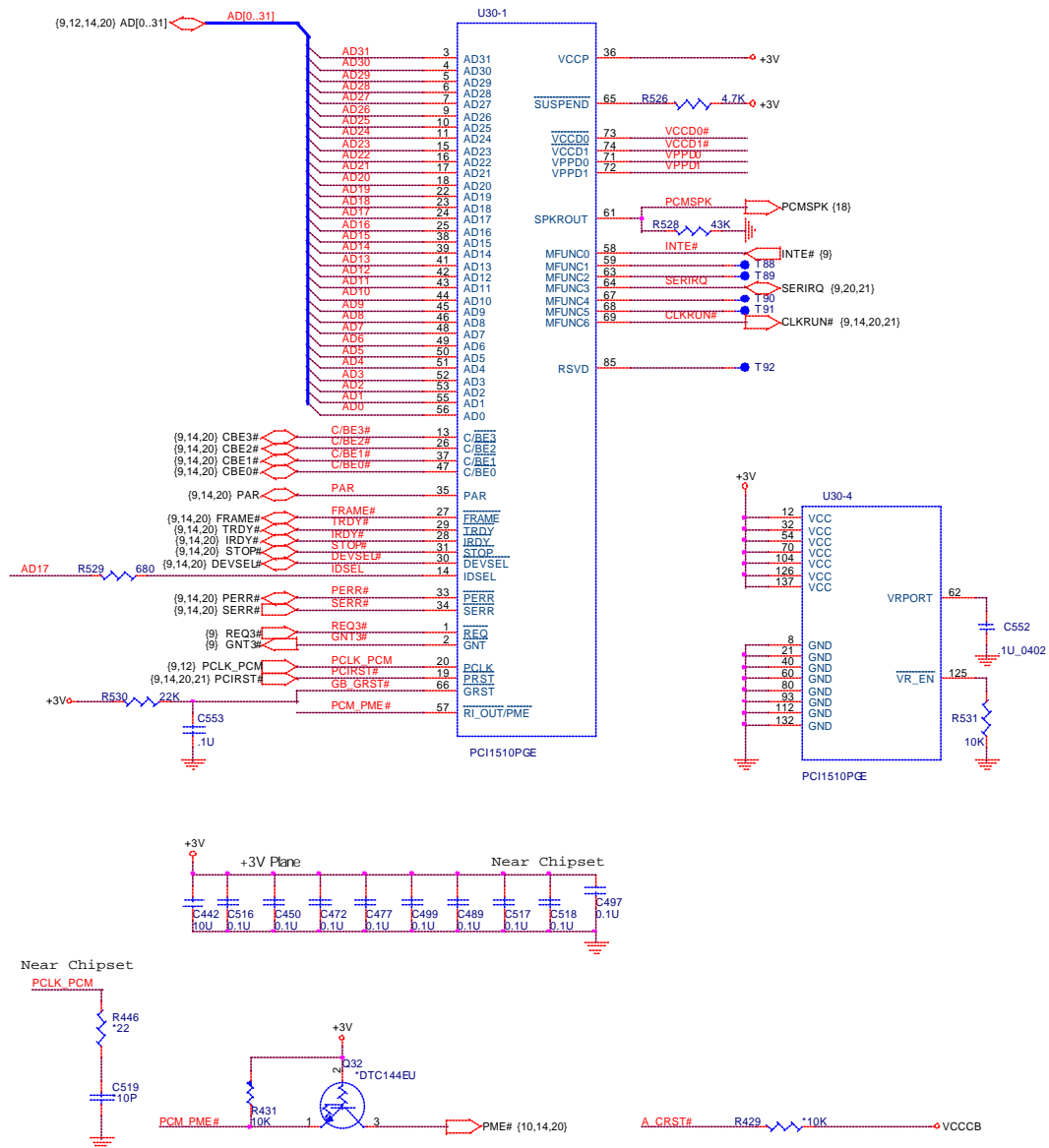


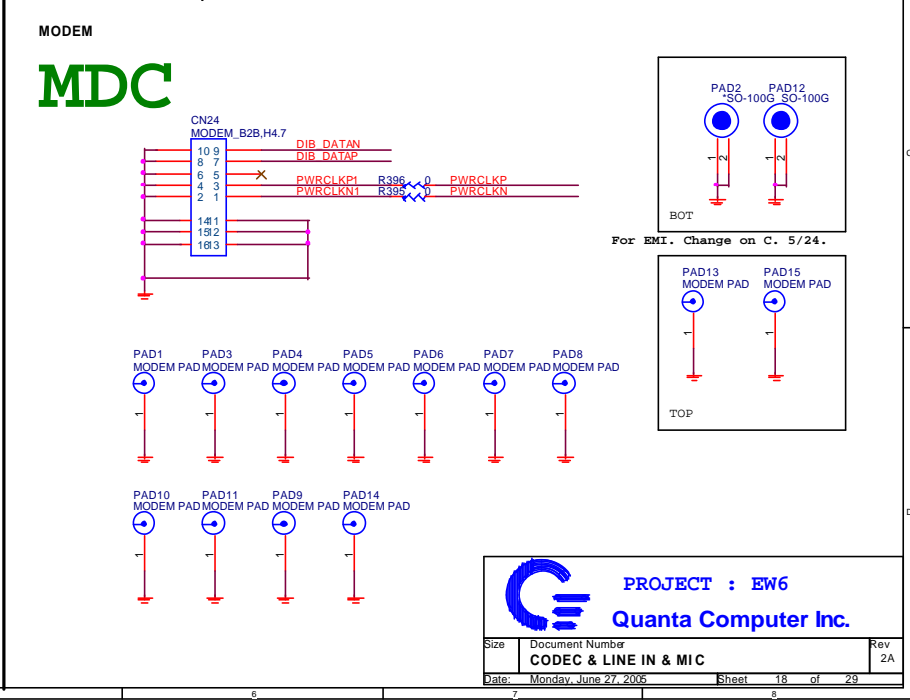
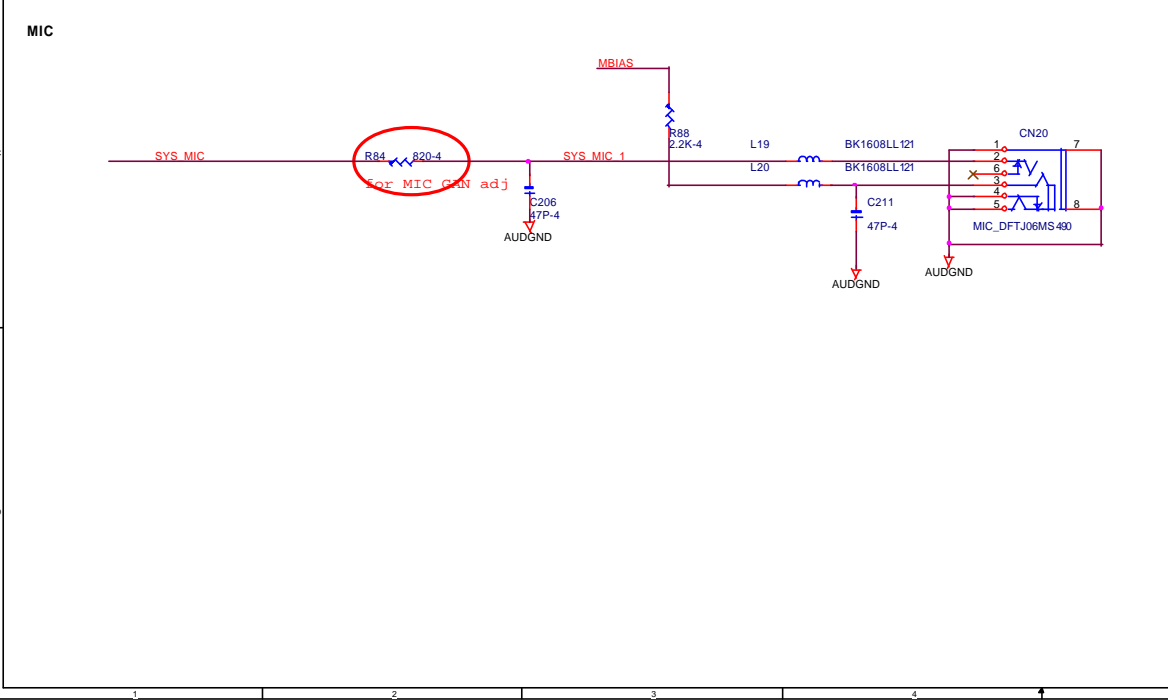
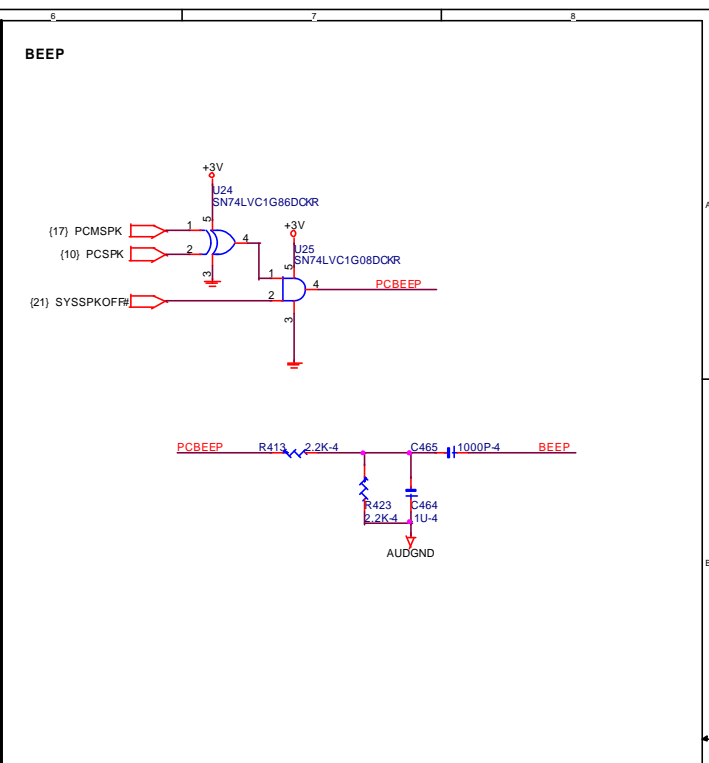
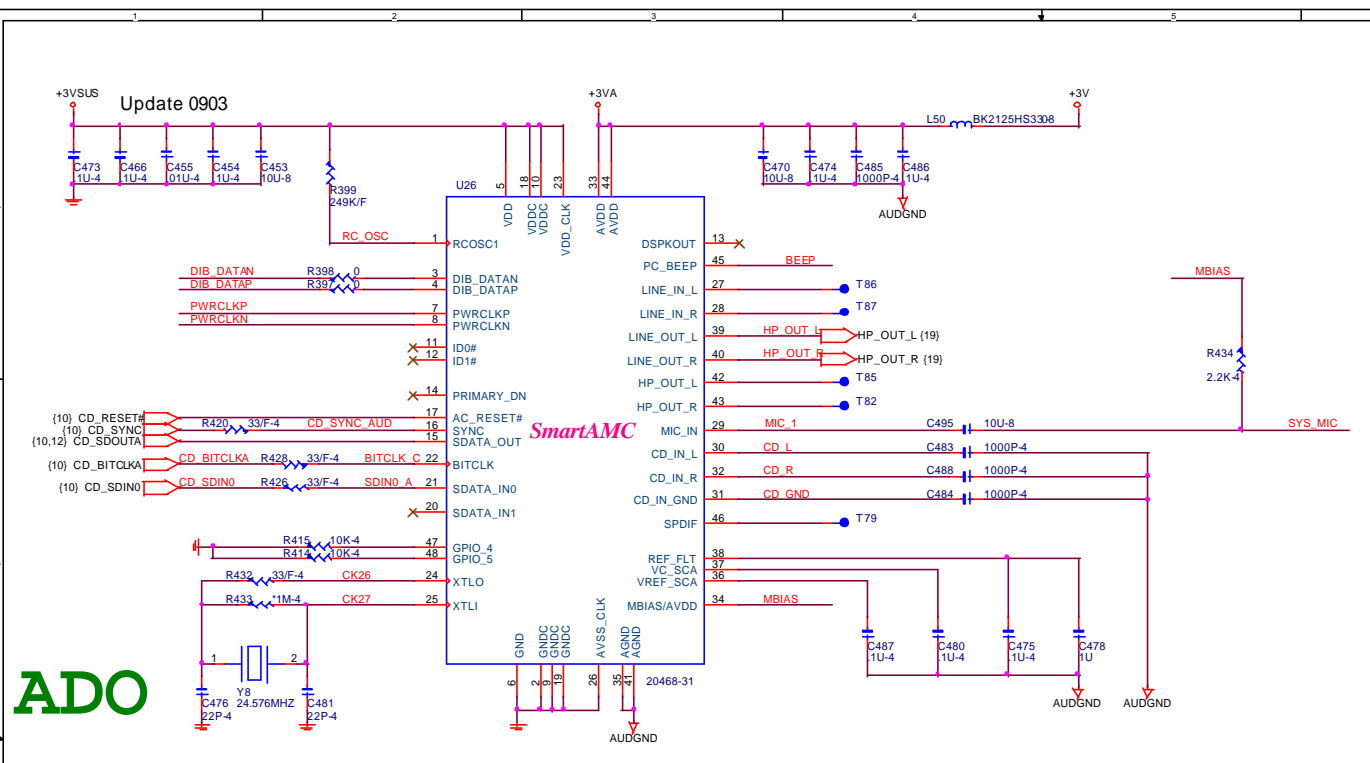
PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM	3A
Date:	Monday, June 27, 2005	Sheet 16 of 29

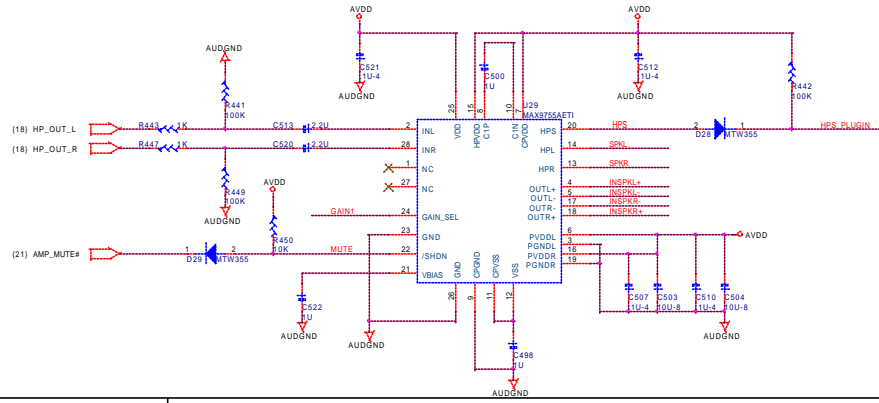
ID Select : AD17
 Interrupt Pin : INTE#
 Request Indicate : REQ3#
 Grant Indicate : GNT3#

CBS

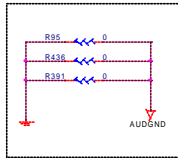
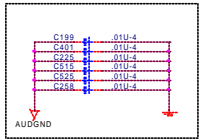
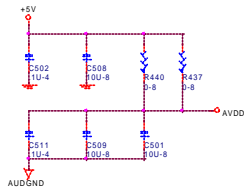




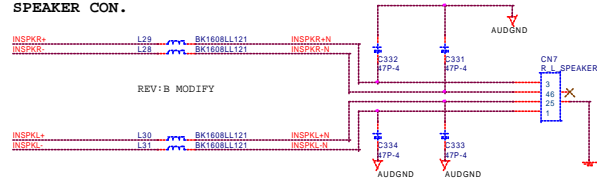
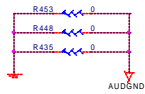
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



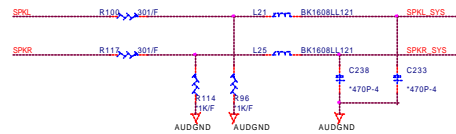
AMP POWER



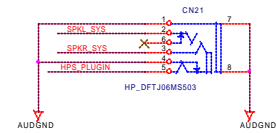
SPEAKER CON.



LINE-OUT



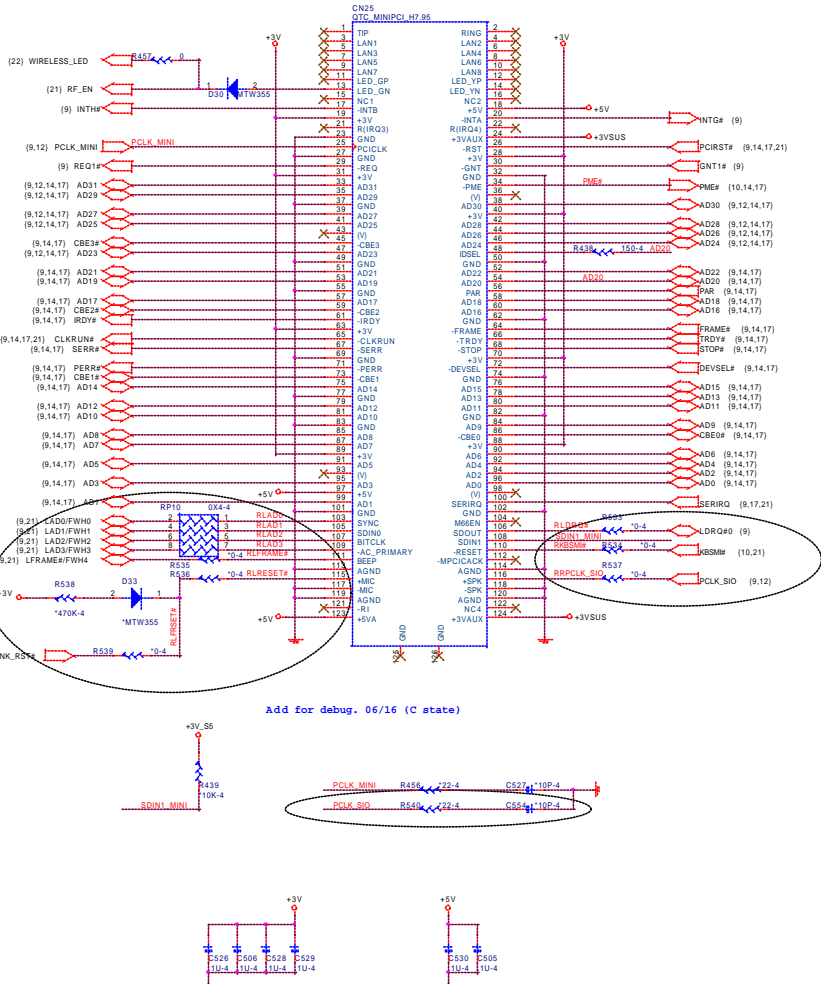
LINE OUT



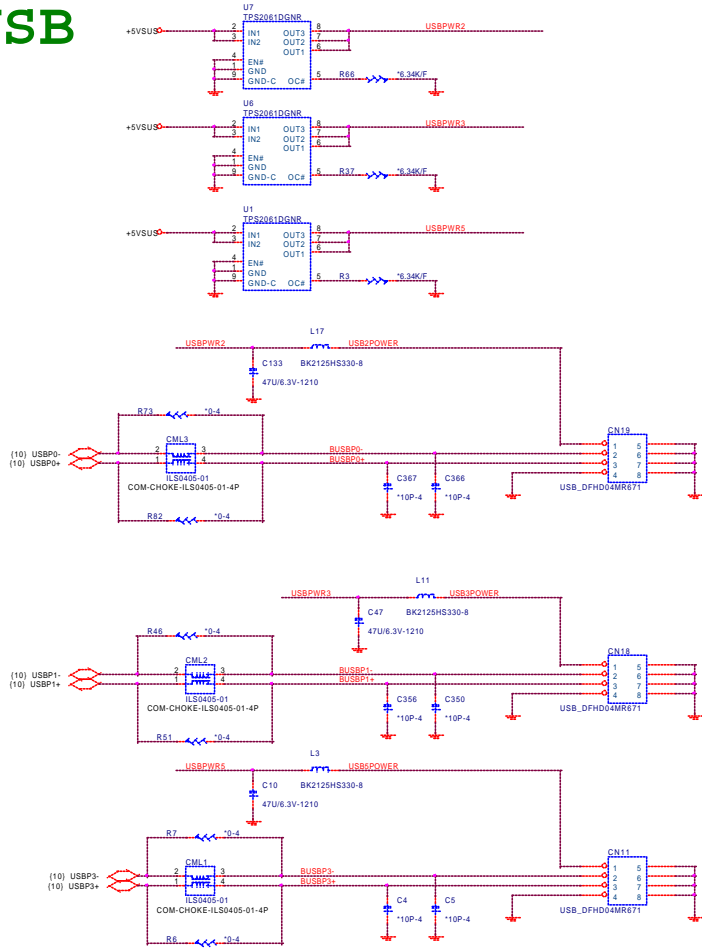
MPC

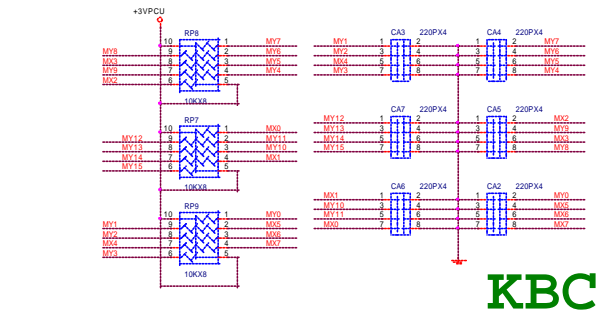
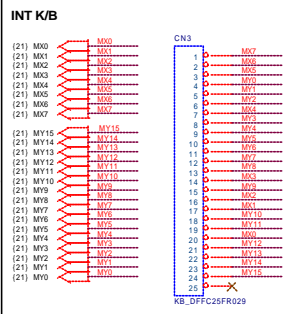
ID Select : AD20
 Interrupt Pin : INTB#, INTD#
 Request Indicate : REQ1#
 Grant Indicate : GNT1#

MINI-PCI

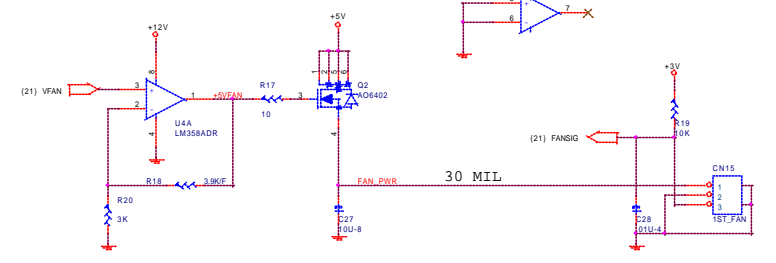


USB

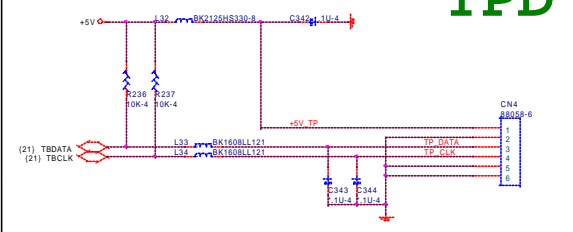




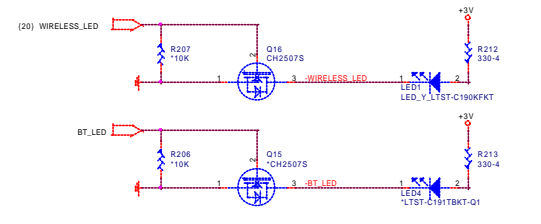
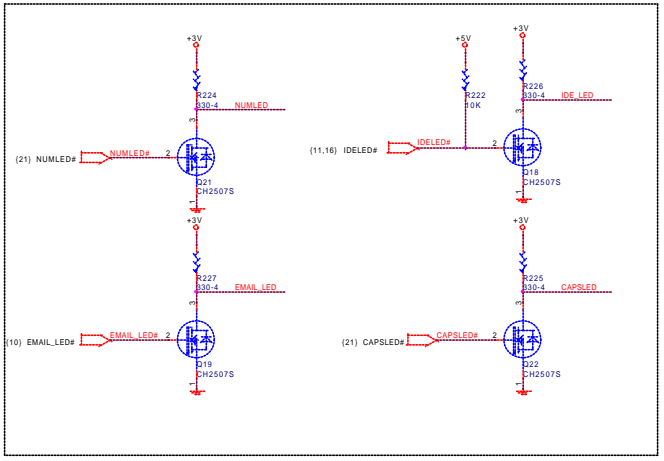
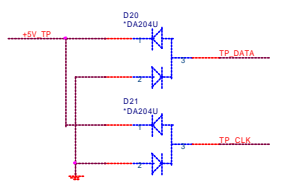
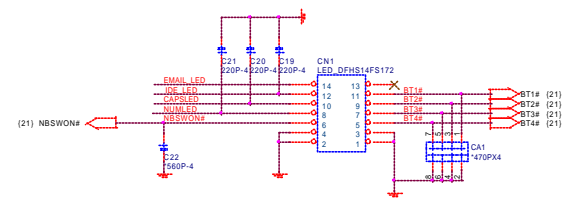
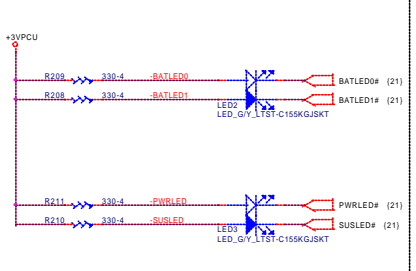
FAN CONTROL



TOUCH PAD **20 MIL**

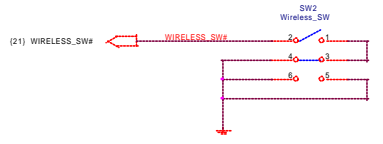


TPD **UIF**

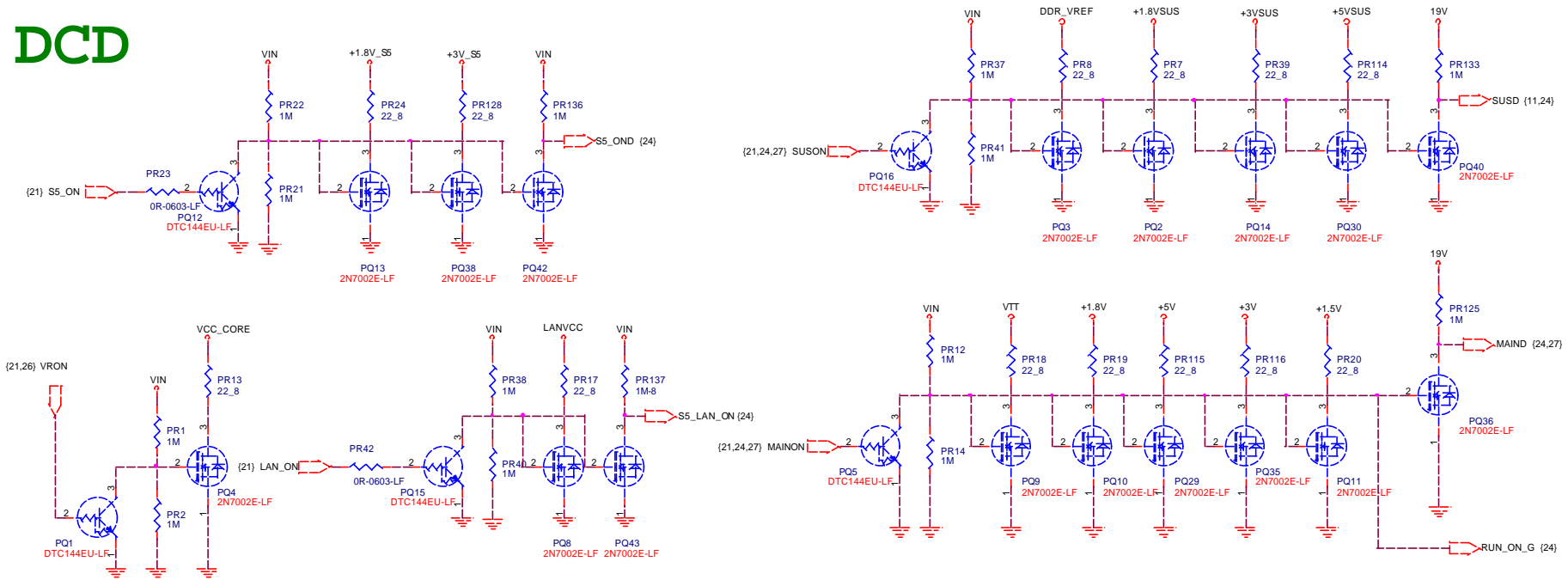


SWITCH

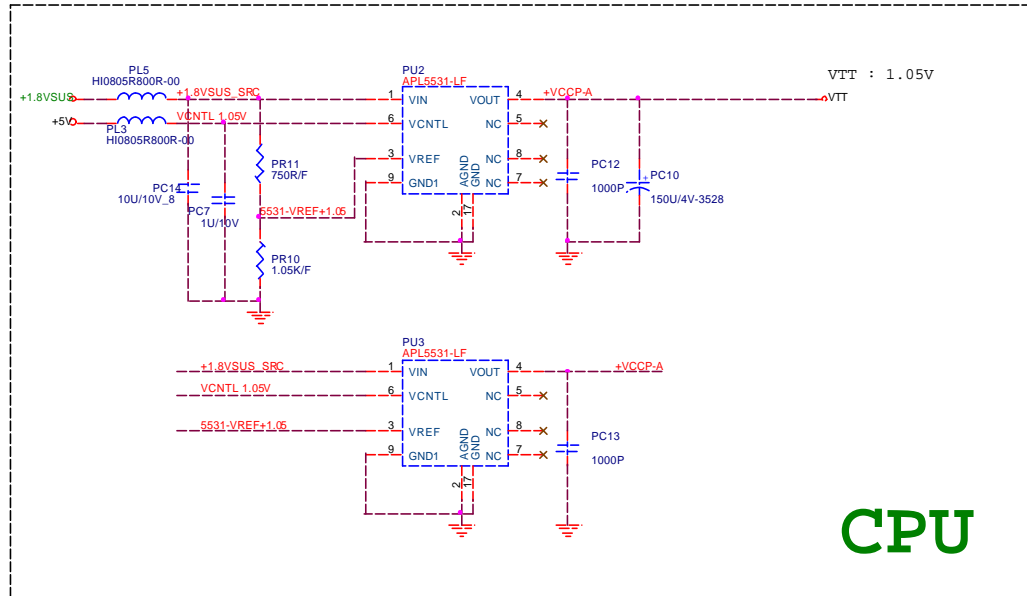
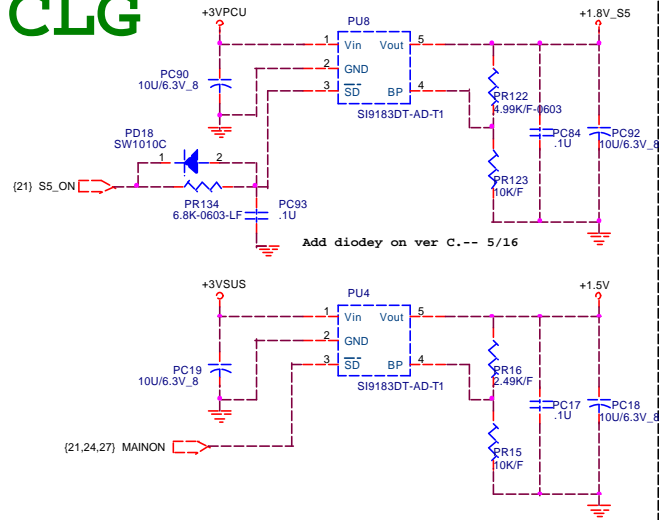
UIF



DCD



CLG



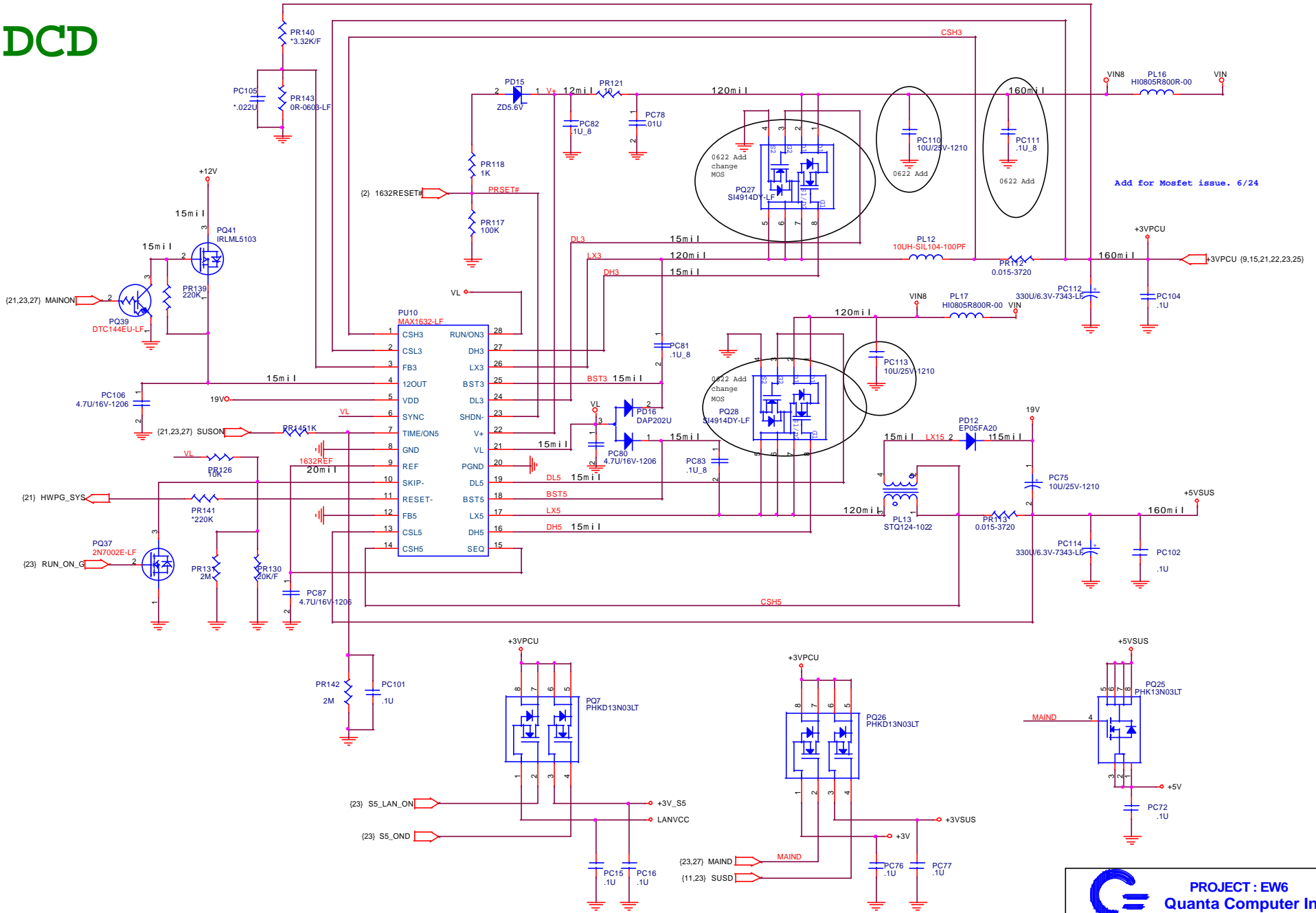
CPU




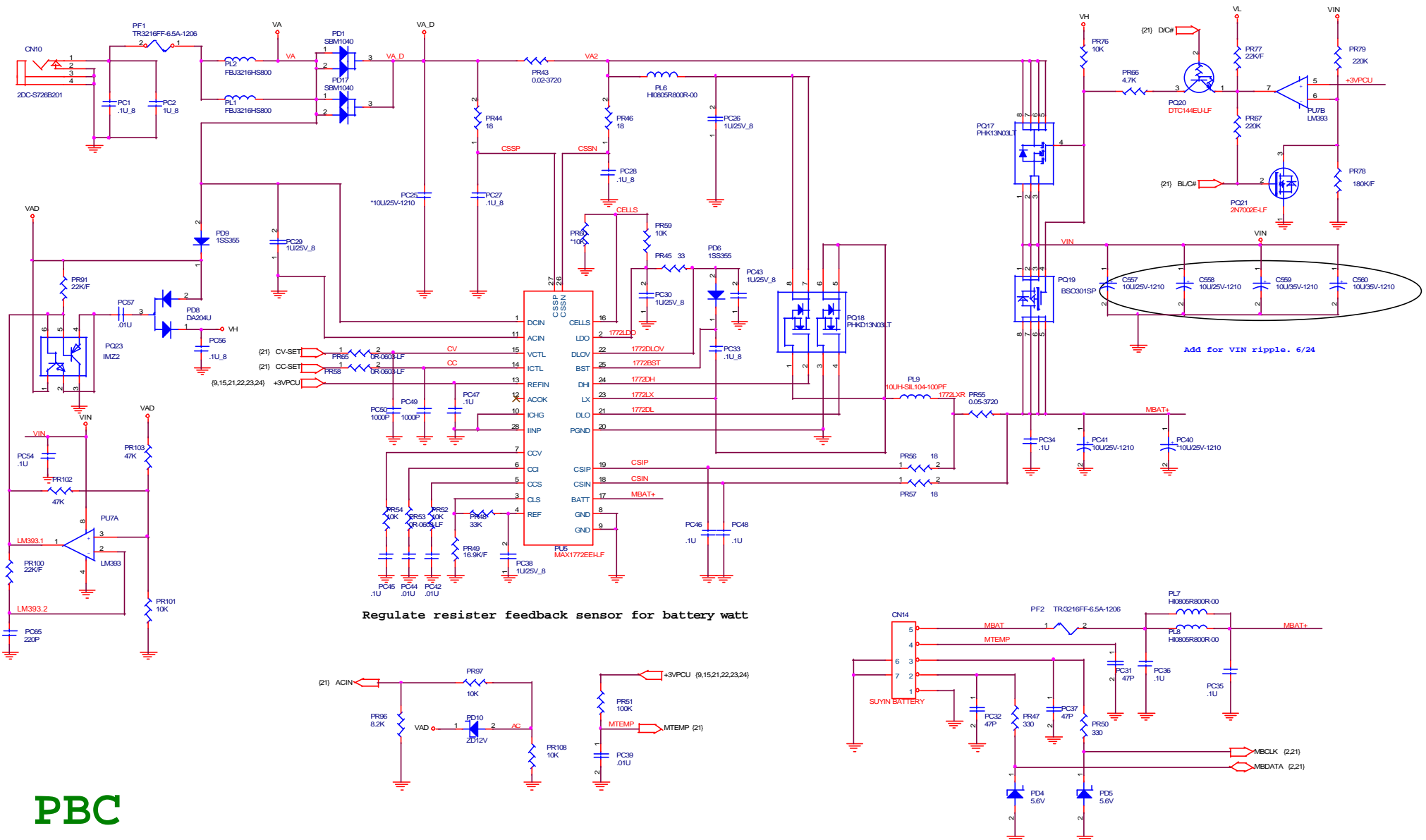
PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE+1.8V	2A
Date:	Monday, June 27, 2005	Sheet 23 of 29

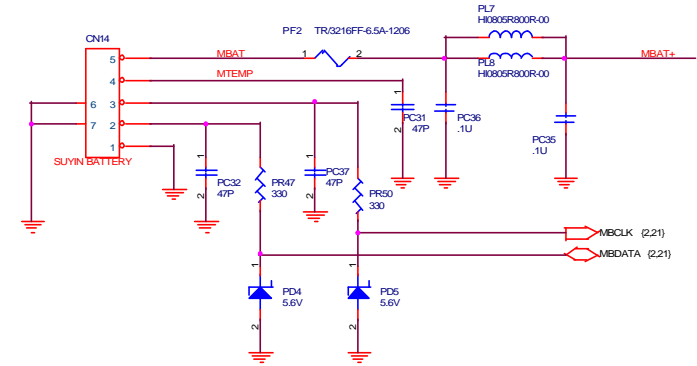
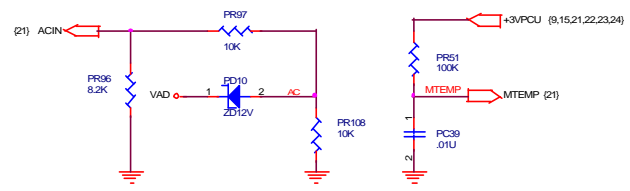
DCD



 PROJECT : EW6 Quanta Computer Inc.		Size	Document Number	Rev
		Custom	SYSTEM POWER MAX1632	3A
Date:	Monday, June 27, 2005	Sheet	24 of 29	



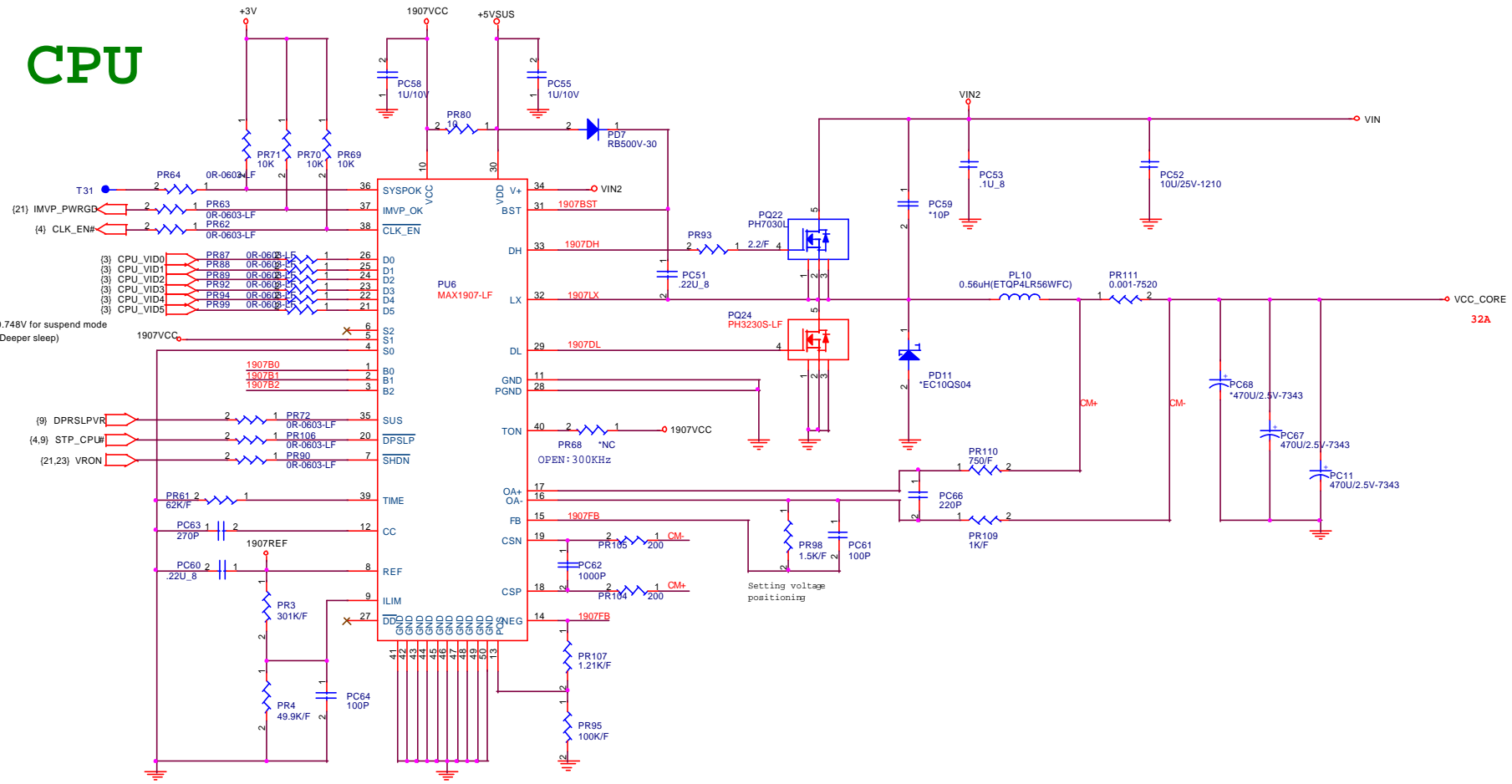
Regulate resistor feedback sensor for battery watt



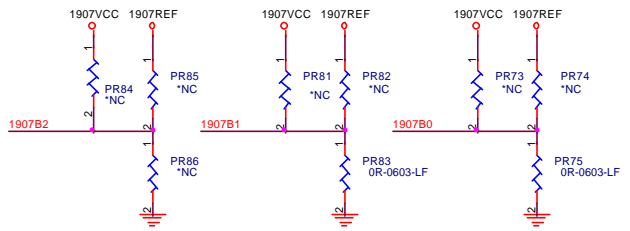
PBC

		PROJECT : EW6	
		Quanta Computer Inc.	
Size	Document Number	Rev	3A
Custom	BATTERY CHARGER		
Date	Monday, June 27, 2005	Sheet	25 of 29

CPU



0.748V for suspend mode (Deeper sleep)



Setting boot voltage=1.2V

SUSPEND MODE (SUS=HIGH)				
S2	S1	S0	Output	
✓	OPEN	VCC	GND	0.748V

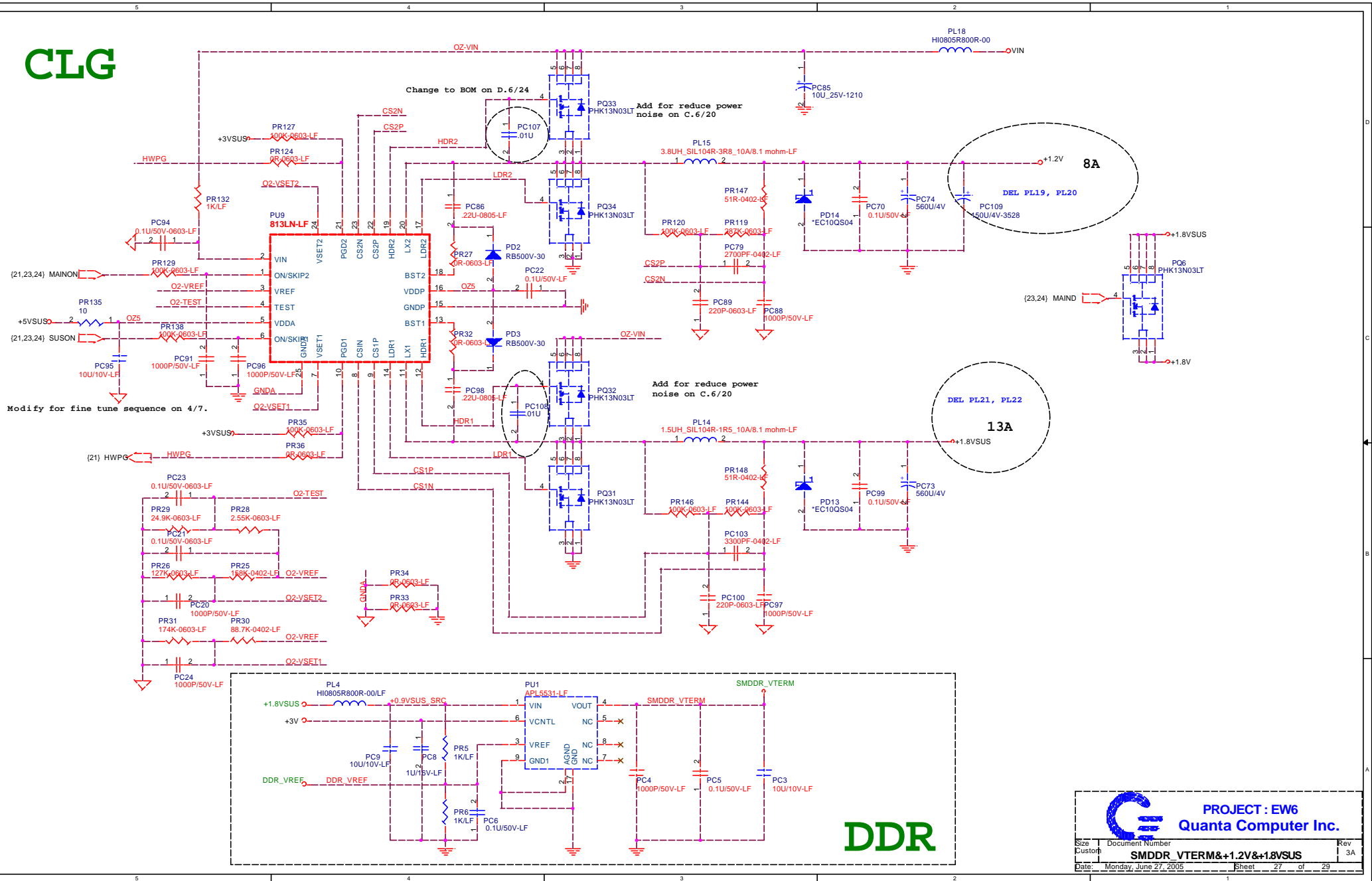
VCC_BOOT				
B2	B1	B0	Output	
✓	OPEN	GND	GND	1.708V
	REF	REF	REF	1.372V
	OPEN	OPEN	OPEN	1.036V
	VCC	VCC	VCC	0.700V
	REF	VCC	VCC	1.212V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	1	0	0	1.148V	0	0	0	1	0	0	1.660V
1	0	0	1	0	1	1.132V	0	0	0	1	0	1	1.644V
1	0	0	1	1	0	1.116V	0	0	0	1	0	0	1.628V
1	0	0	1	1	1	1.100V	0	0	0	1	1	0	1.612V
1	0	1	0	0	0	1.084V	0	0	1	0	0	0	1.596V
1	0	1	0	0	1	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	1	0	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	1	1.036V	0	0	1	0	1	0	1.548V
1	0	1	1	0	0	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	1	1.004V	0	0	1	0	1	0	1.516V
1	0	1	1	1	0	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	1	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

PROJECT : EW6
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
CPU CORE		
Date: Monday, June 27, 2005	Sheet 26 of 29	

CLG



DDR

PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Customer	SMDR_VTERM&+1.2V&+1.8VSUS	3A
Date	Monday, June 27, 2005	Sheet 27 of 29

www.s-manuals.com