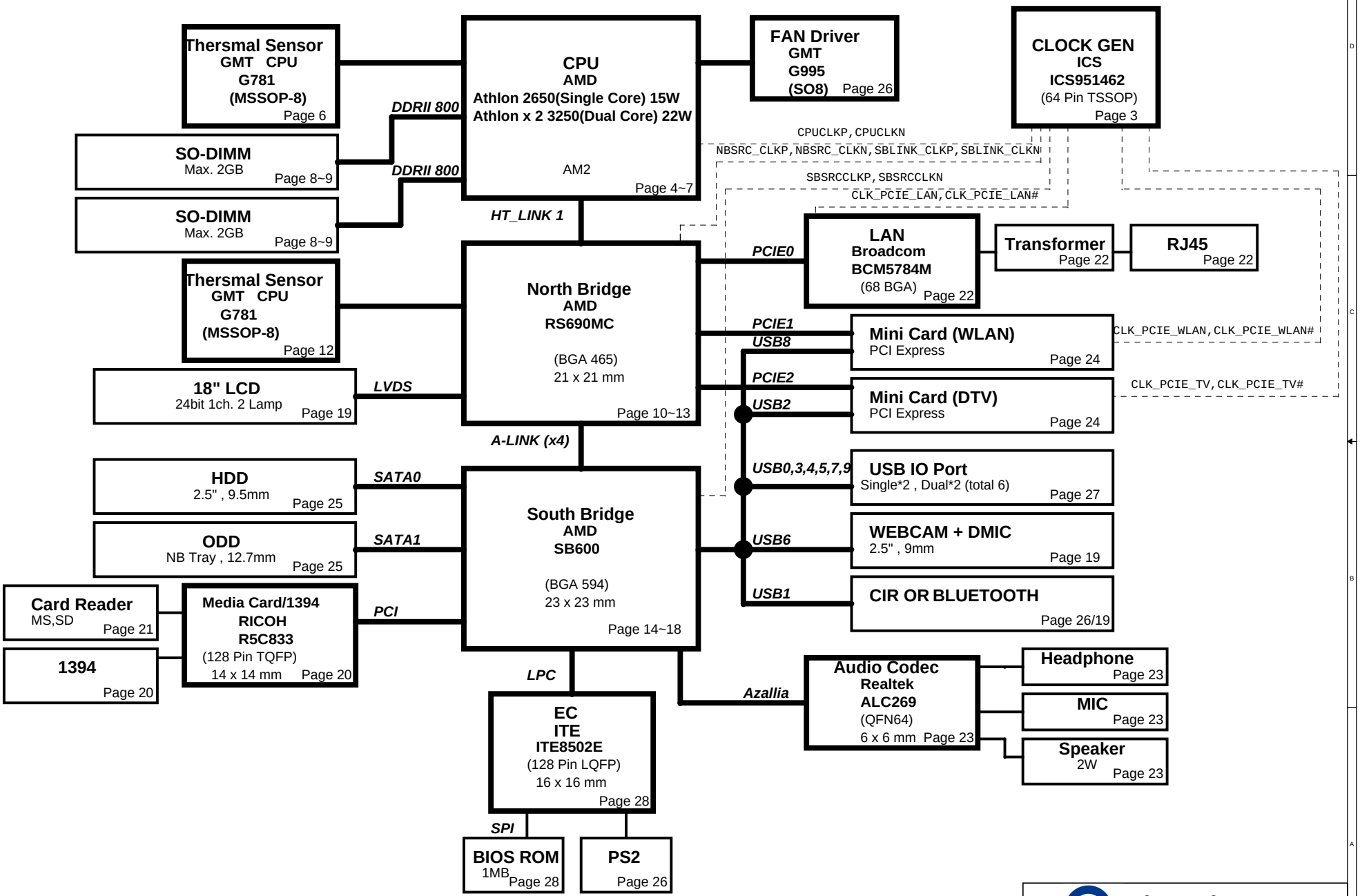
GT1 SYSTEM BLOCK DIAGRAM



Quanta Computer Inc.

PROJECT : GT1

Size	Document Number	Rev
	BLOCK DIAGRAM	A
Date:	Sheet 1 of 36	

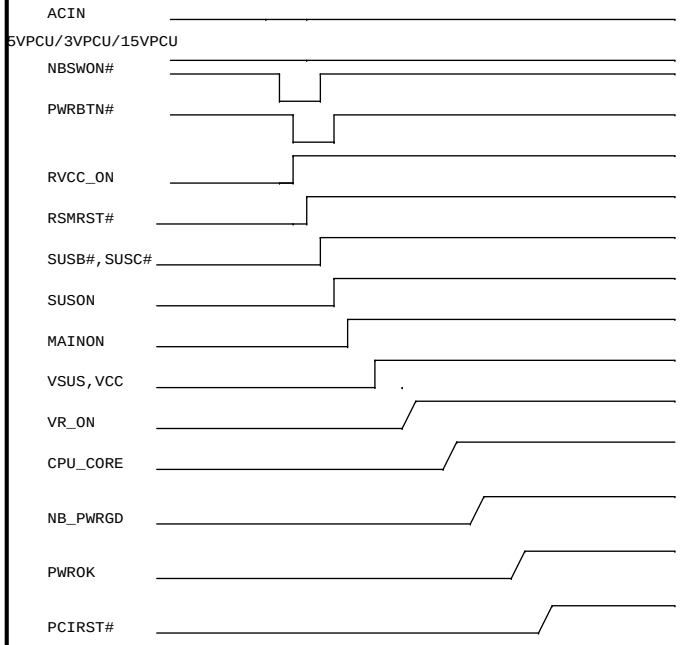
Voltage Rails

Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
VCCRTC	3V	V	V	V	V	
+3.3VALW	3V	V	V	V	V	STB_ON_D
+1.2VALW	1.2V	V	V	V	V	STB_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
SMDDR_VTERM	0.9V	V				SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
VLDT_RUN	1.2V	V				VLDT_ON_D
CPU_VCCA	2.5V	V				MAINON
CPU_CORE	0.9V	V				VRON

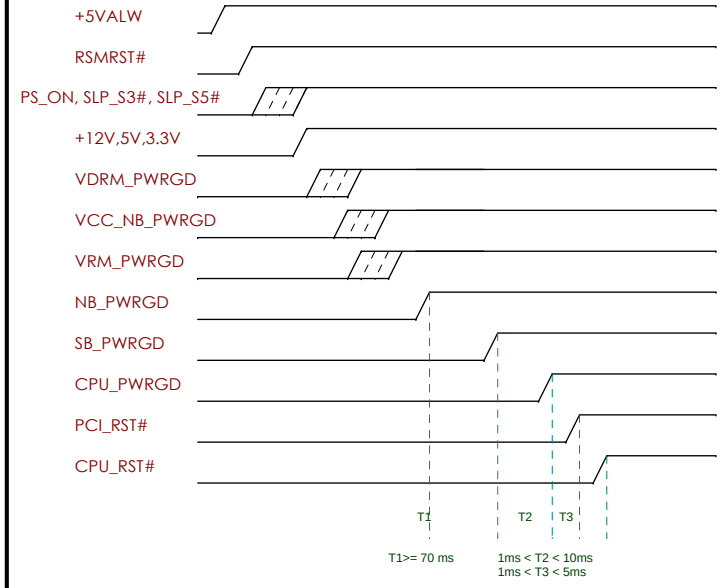
PCI DEVICES IRQ ROUTING

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLK
NB(RS690)	NA	NA	NA	NA
SB(SB600)	DEVSEL#	REQ0#/GNT0#	INTE#	PCICLK0
R5C833	IDSEL	REQ#/GNT#	INTA#/INTB#	PCICLK

Power On Sequence



BONEFISH POWER UP SEQUENCE

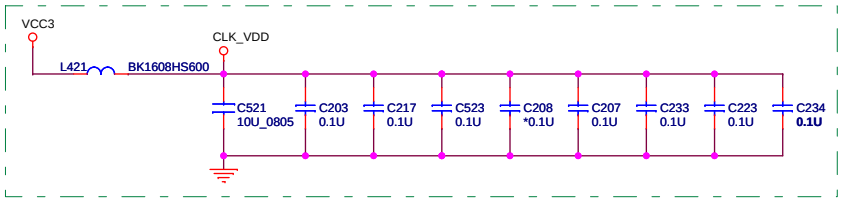


PCB STACK UP

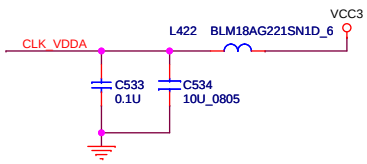
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

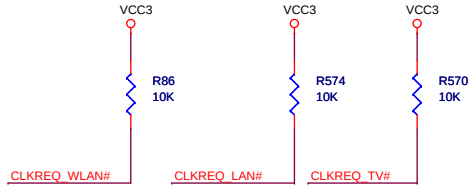
Quanta Computer Inc.
PROJECT : GT1

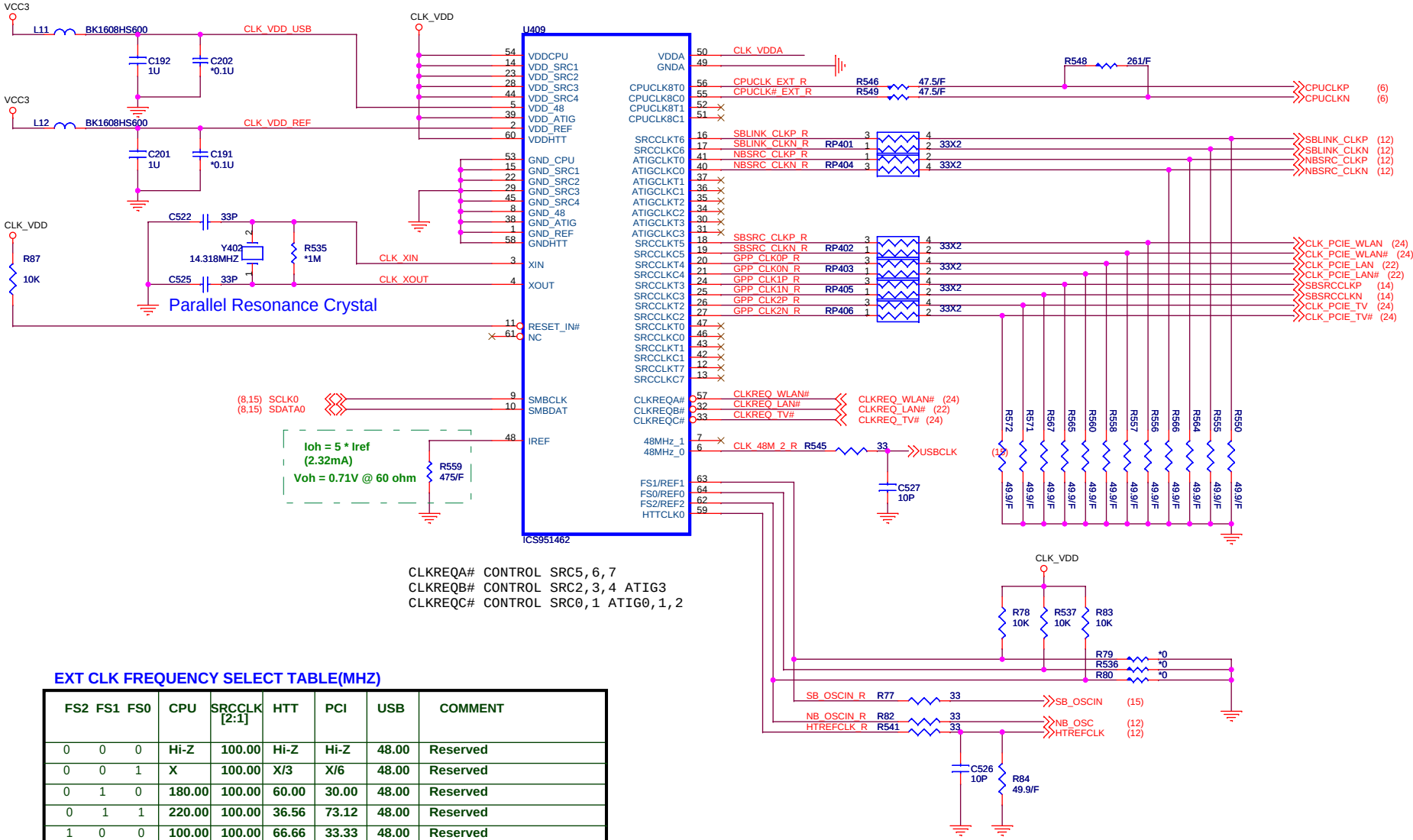
Size	Document Number	Rev
	System Infromation	A
Date: Thursday, April 09, 2009	Sheet 2 of 36	



Put Decoupling Caps close to Clock Fen. power pin







CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

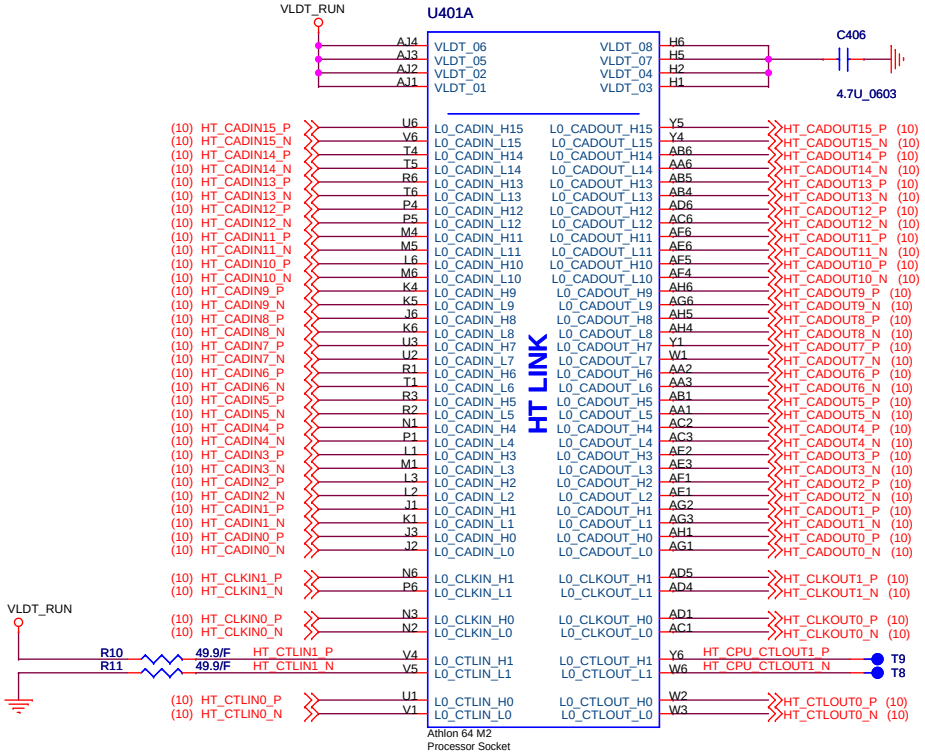
Check AMD clock

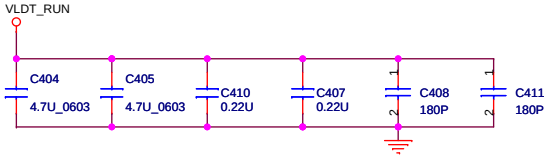
Quanta Computer Inc.
PROJECT : GT1

Size	Document Number	Rev
	Clock Generator	A
Date: Thursday, April 09, 2009	Sheet 3 of 36	

CPU HyperTransport Interface

VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.





Quanta Computer Inc.		
PROJECT : GT1		
Size	Document Number: AMD M2+ HT I/F	Rev: A
Date: Thursday, April 09, 2009	Sheet 4 of 36	

Processor DDR2 Memory Interface

To SODIMM socket B (Far)

To SODIMM socket A (near)

U401C

DDRII: DATA

(8) M_B_DQ[0..63]

M_A_DQ[0..63] (8)

(8) M_B_DM[0..7]

M_A_DM[0..7] (8)

(8) M_B_DQS[0..7]

M_A_DQS[0..7] (8)

(8) M_B_DQS#[0..7]

M_A_DQS#[0..7] (8)

Athlon 64 M2
Processor Socket

PLACE THEM CLOSE TO
CPU WITHIN 1"

1.8VSUS

R17 39.2F

R15 39.2F

R22 2K/F

R25 2K/F

CPU_M_VREF

C47 0.1U

C46 1000P

SMDDR_VTERM

U401B

DDR II: CMD/CTRL/CLK

T21

VTT_SENSE

M_ZN

M_ZP

(8,9) M_A_CS#3
(8,9) M_A_CS#2
(8,9) M_A_CS#1
(8,9) M_A_CS#0

(8,9) M_B_CS#3
(8,9) M_B_CS#2
(8,9) M_B_CS#1
(8,9) M_B_CS#0

(8,9) M_CKE3
(8,9) M_CKE2
(8,9) M_CKE1
(8,9) M_CKE0

(8,9) M_A_A[0..15]

(8,9) M_A_BS#2
(8,9) M_A_BS#1
(8,9) M_A_BS#0

(8,9) M_A_RAS#
(8,9) M_A_CAS#
(8,9) M_A_WE#

M_CLKOUT1 (8)
M_CLKOUT1# (8)
M_CLKOUT0 (8)
M_CLKOUT0# (8)

M_CLKOUT4 (8)
M_CLKOUT4# (8)
M_CLKOUT3 (8)
M_CLKOUT3# (8)

M_ODT3 (8,9)
M_ODT2 (8,9)
M_ODT1 (8,9)
M_ODT0 (8,9)

M_B_A[0..15] (8,9)

M_B_BS#2 (8,9)
M_B_BS#1 (8,9)
M_B_BS#0 (8,9)

M_B_RAS# (8,9)
M_B_CAS# (8,9)
M_B_WE# (8,9)

Athlon 64 M2
Processor Socket

SMDDR_VTERM

C61 4.7U_0603
C50 4.7U_0603
C67 4.7U_0603
C45 4.7U_0603
C75 0.22U
C32 0.22U
C83 0.22U
C41 0.22U

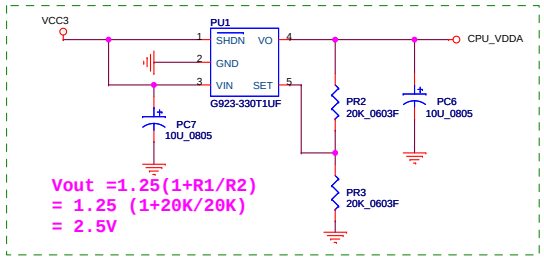
C455 1000P
C433 1000P
C457 1000P
C436 1000P
C463 180P
C439 180P
C464 180P
C452 180P

Quanta Computer Inc.

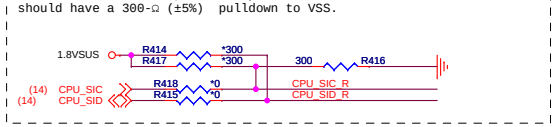
PROJECT : GT1

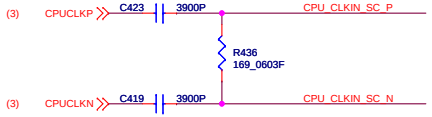
Size	Document Number	Rev
	AMD M2+ DDR II Memory I/F	A
Date: Thursday, April 09, 2009	Sheet 5 of 36	

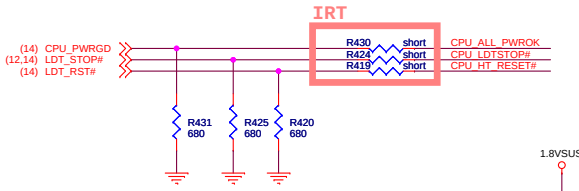
ATHLON Control and Debug

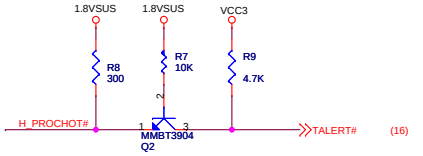


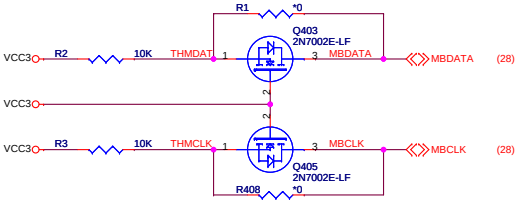
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

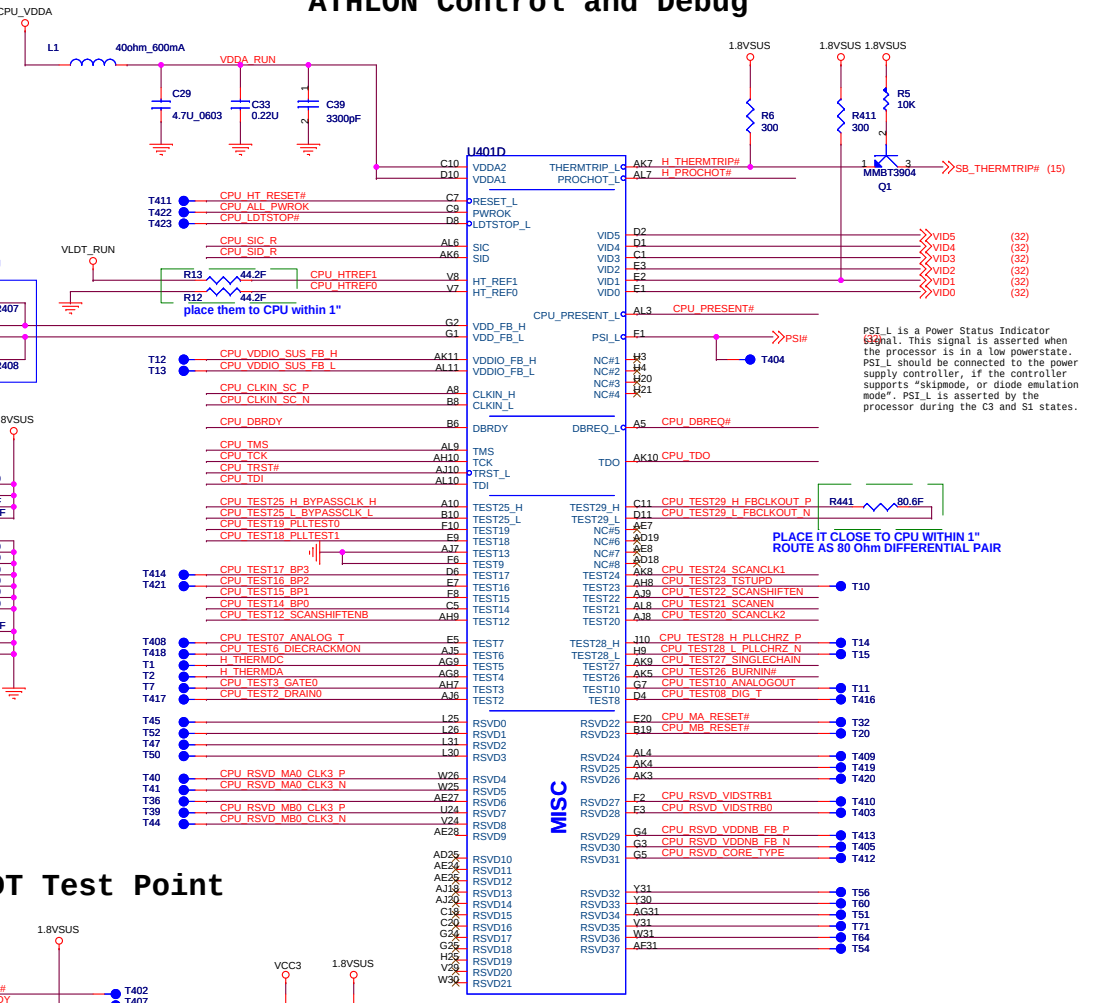




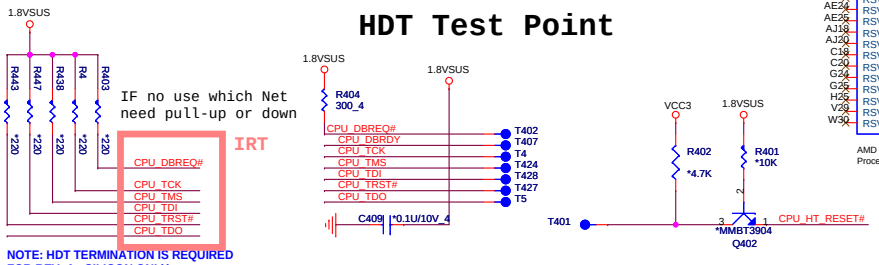




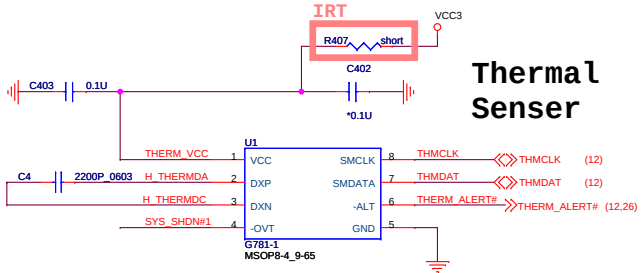


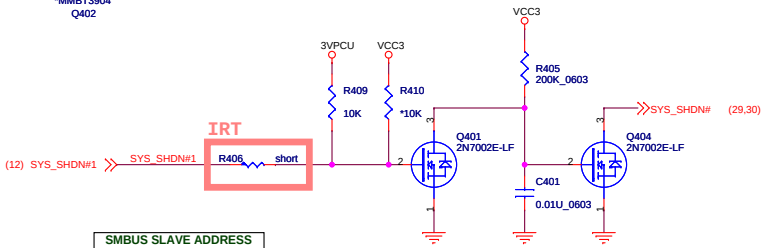


HDT Test Point



Thermal Senser





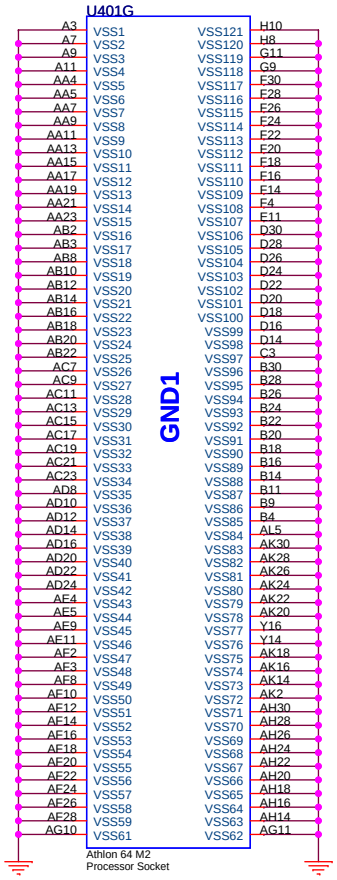
SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

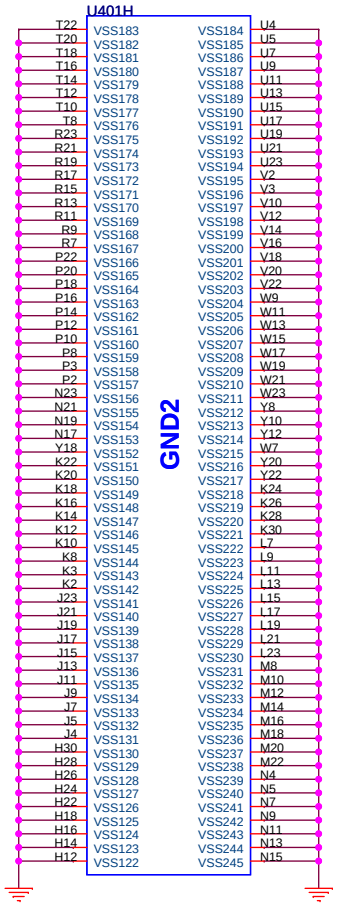
Quanta Computer Inc.
PROJECT : GT1

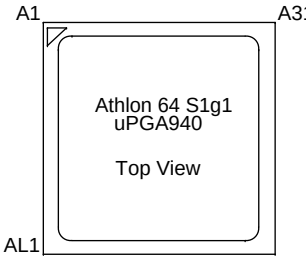
Size	Document Number	Rev
	AMD M2+ CTRL & DEBUG	A

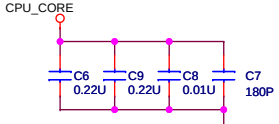
Date: Thursday, April 09, 2009 Sheet 6 of 36

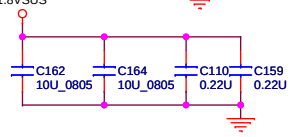
PROCESSOR POWER AND GROUND



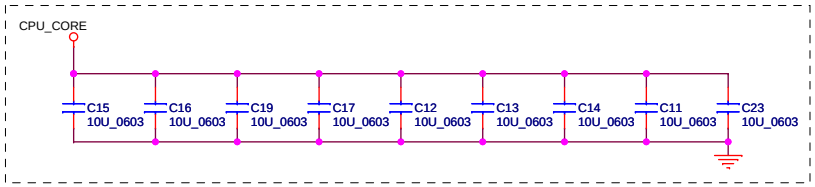


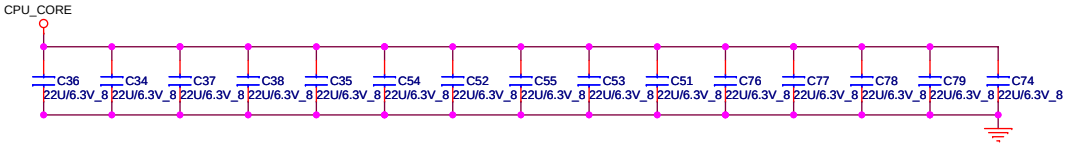




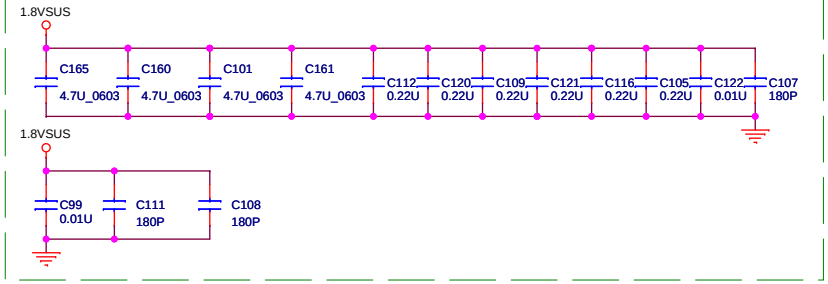


BOTTOMSIDE DECOUPLING





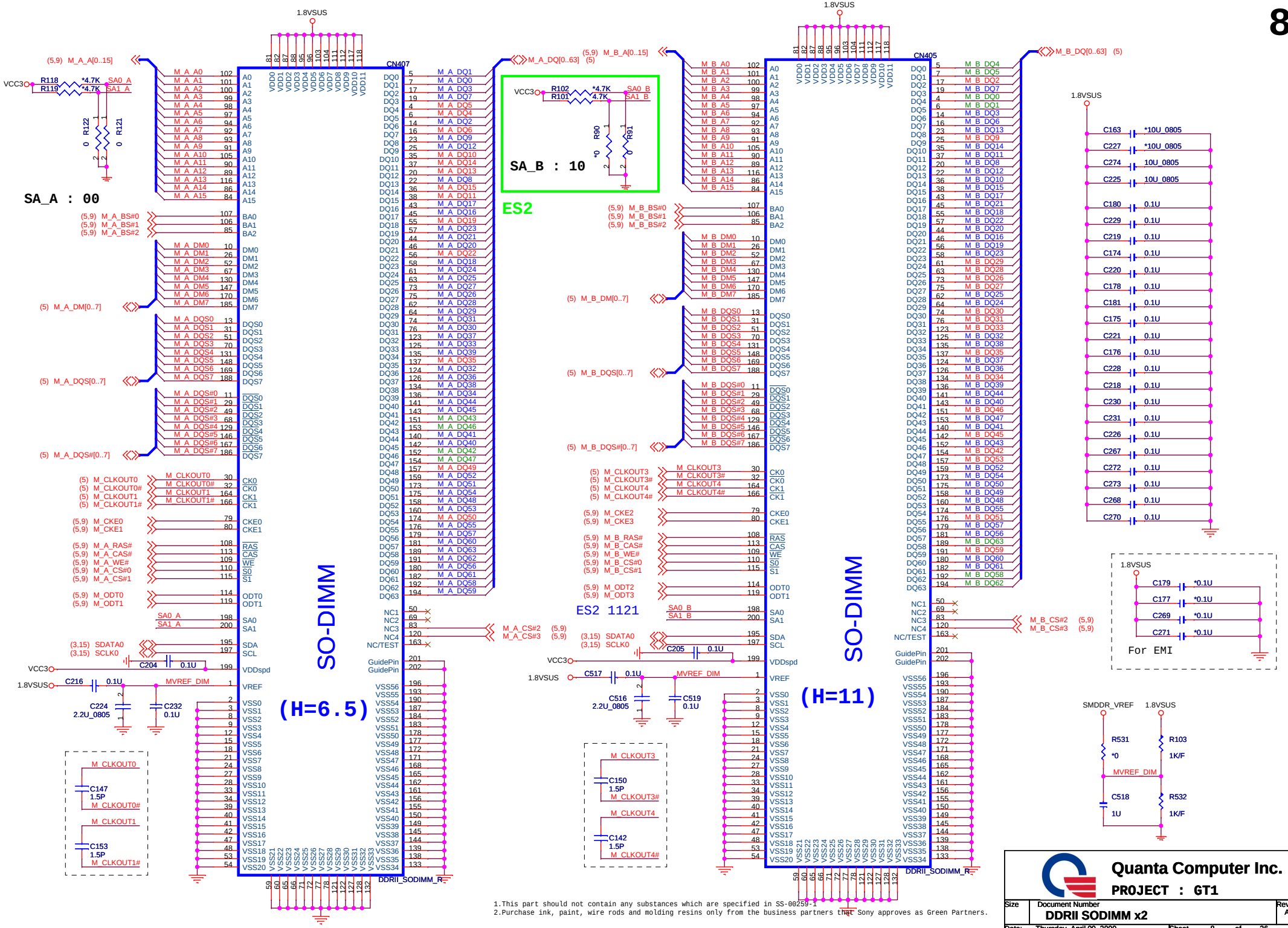
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



Quanta Computer Inc.

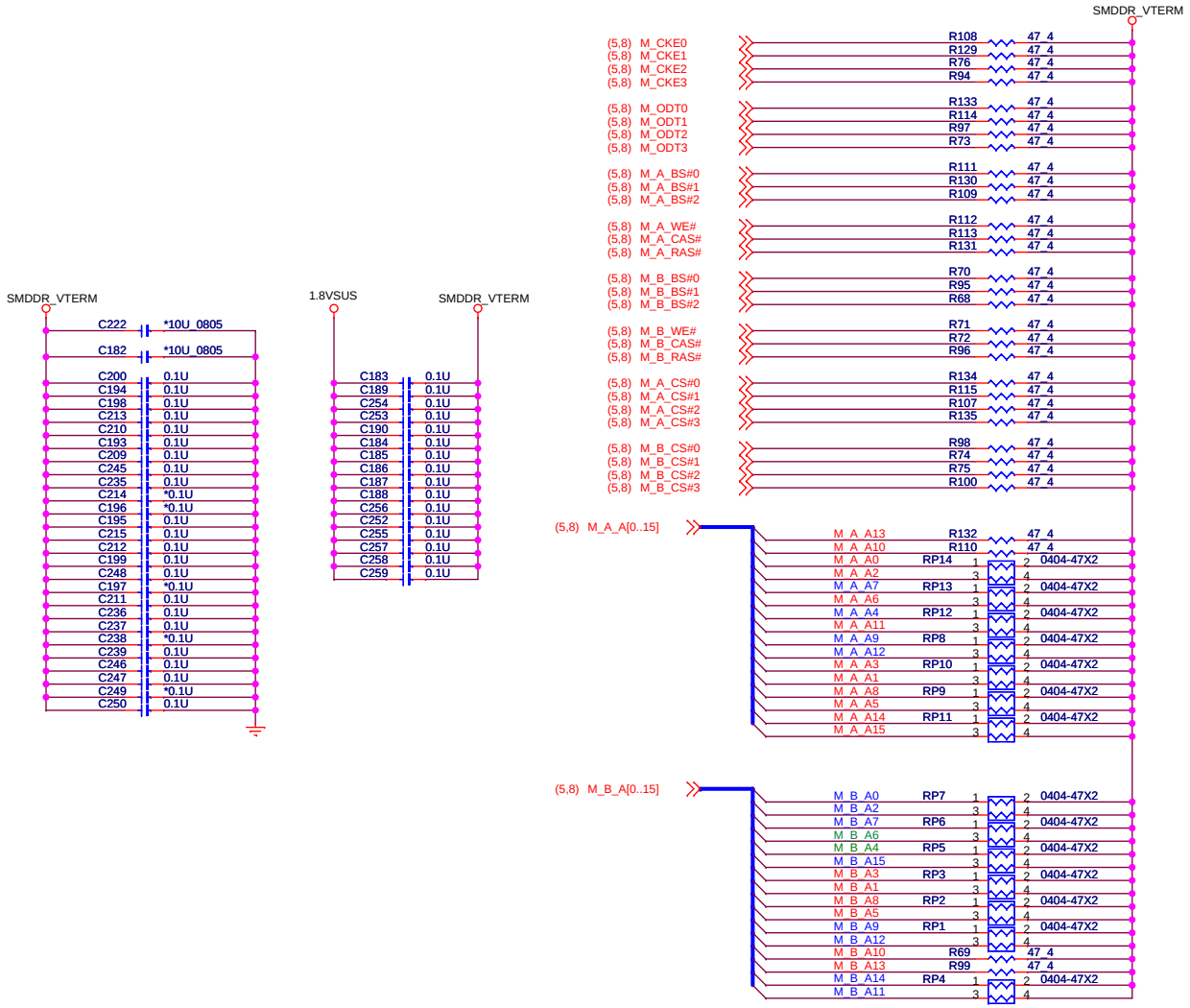
PROJECT : GT1

Size	Document Number	Rev
	AMD M2+ PWR & GND	A
Date: Thursday, April 09, 2009	Sheet 7 of 36	



1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

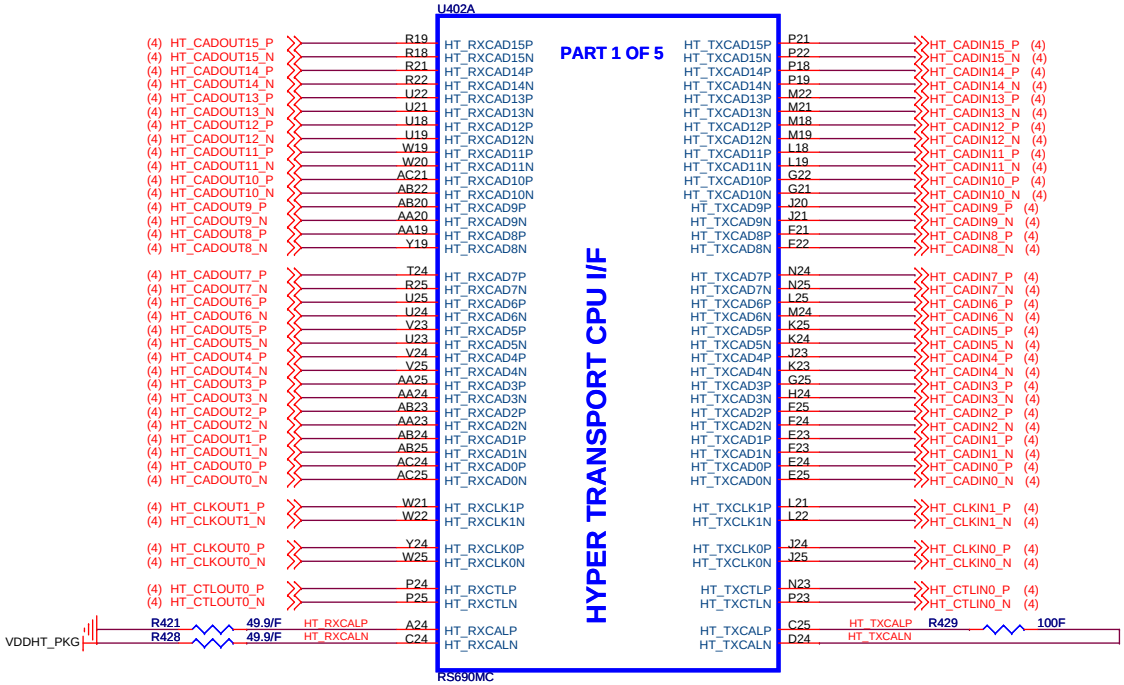
Quanta Computer Inc.		
PROJECT : GT1		
Size	Document Number: DDRII SODIMM x2	Rev: A
Date: Thursday, April 09, 2009	Sheet 8 of 36	



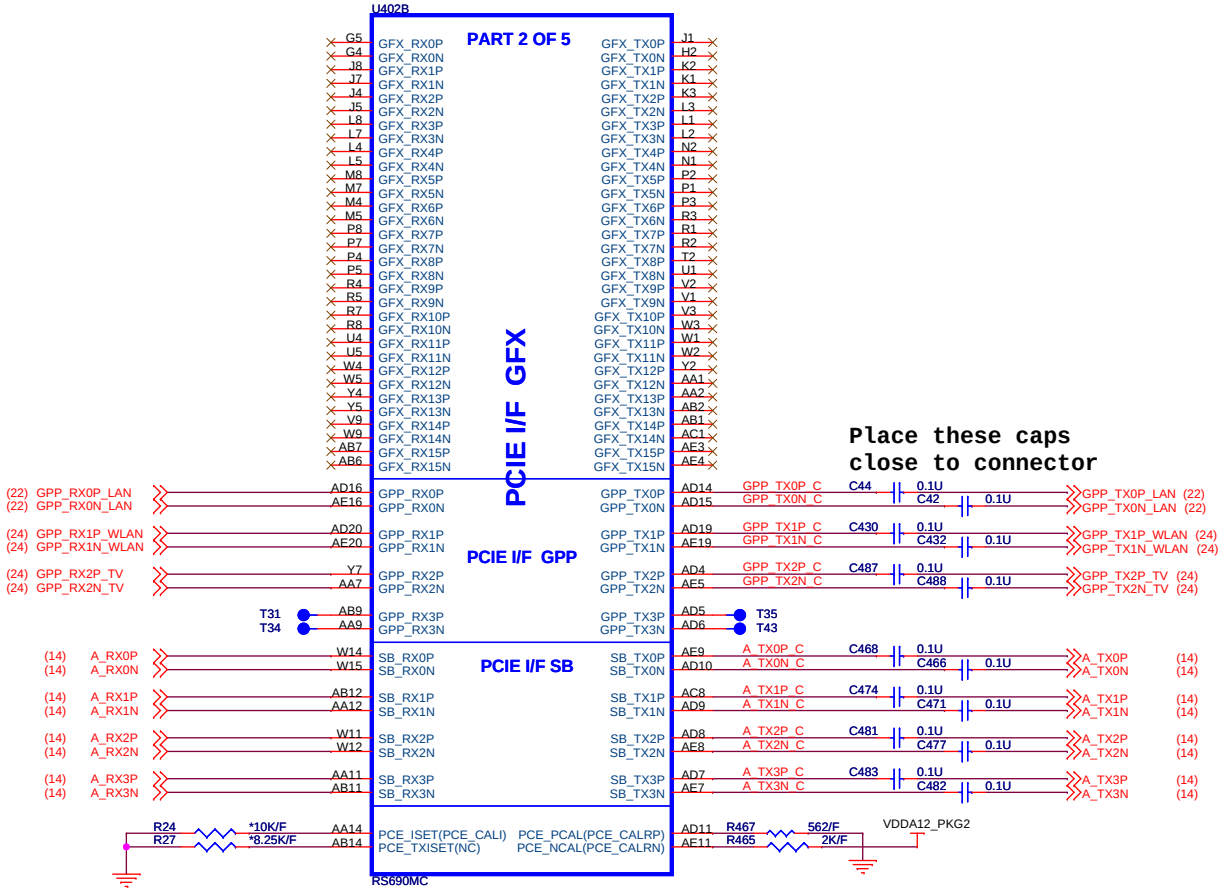
Quanta Computer Inc.

PROJECT : GT1

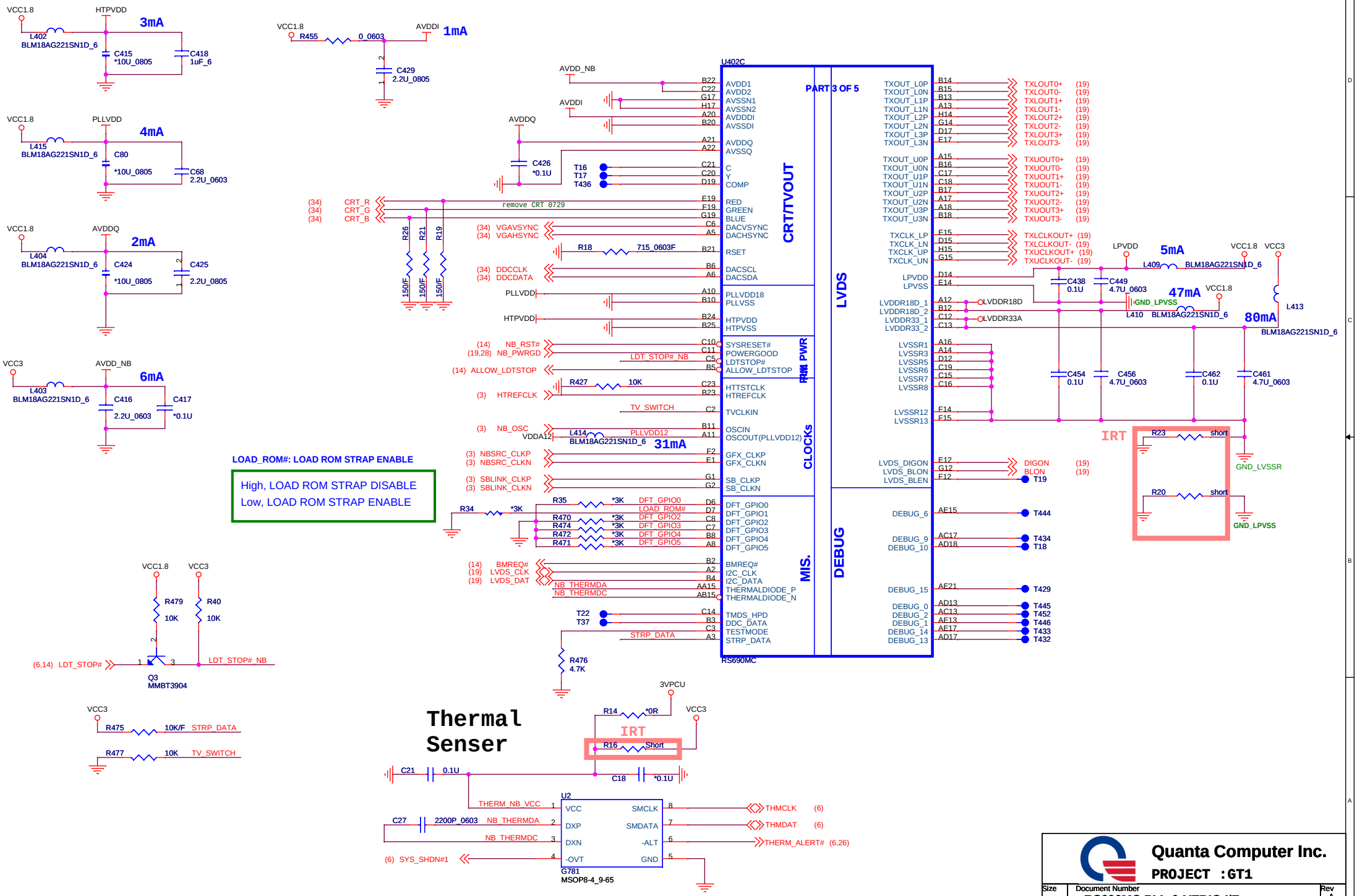
Size	Document Number	Rev
	DDRII TERMINATION	A
Date: Thursday, April 09, 2009	Sheet 9 of 36	



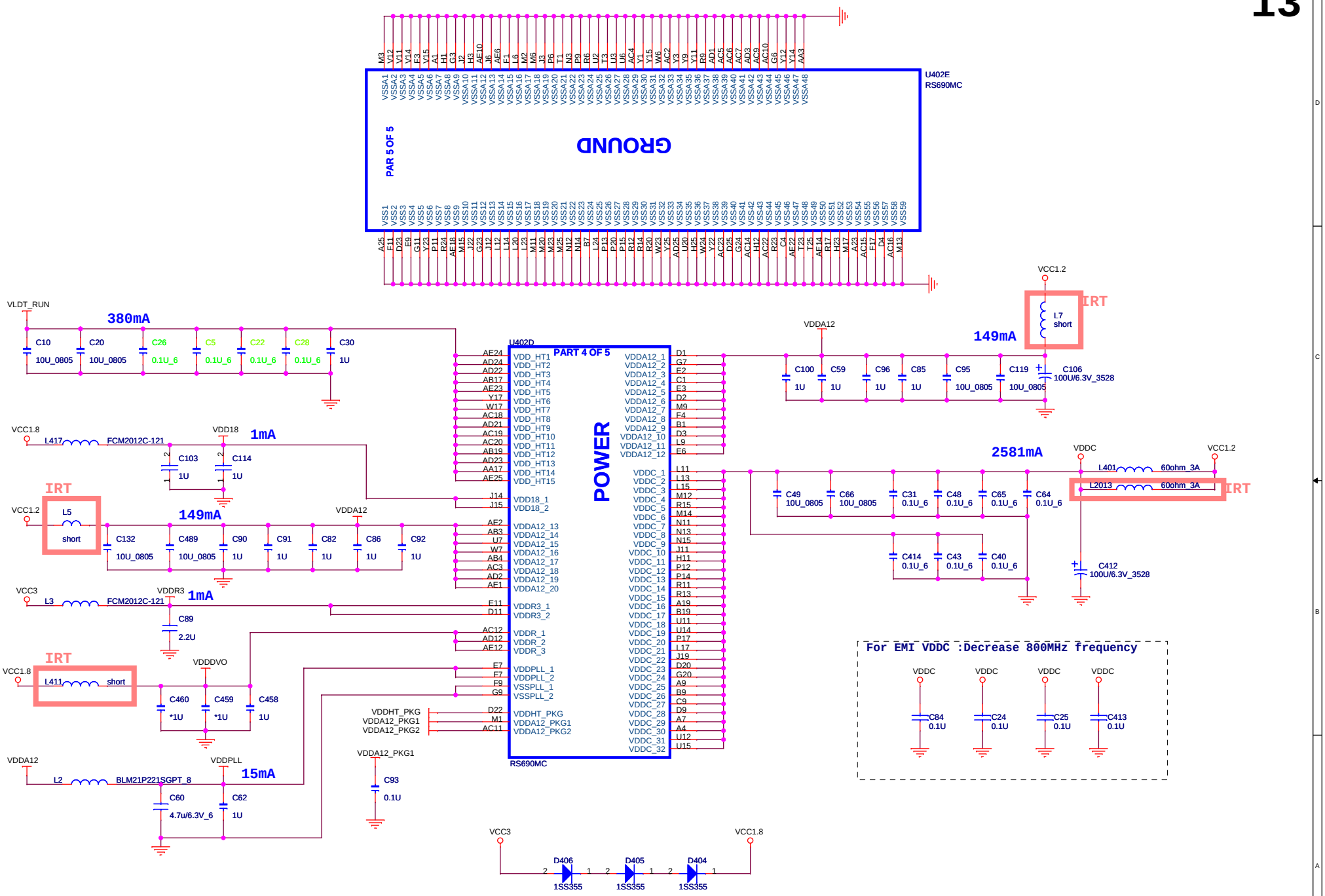
Quanta Computer Inc.		
PROJECT : GT1		
Size	Document Number: RS690MC HT LINK I/F	Rev: A
Date: Thursday, April 09, 2009	Sheet 10 of 36	

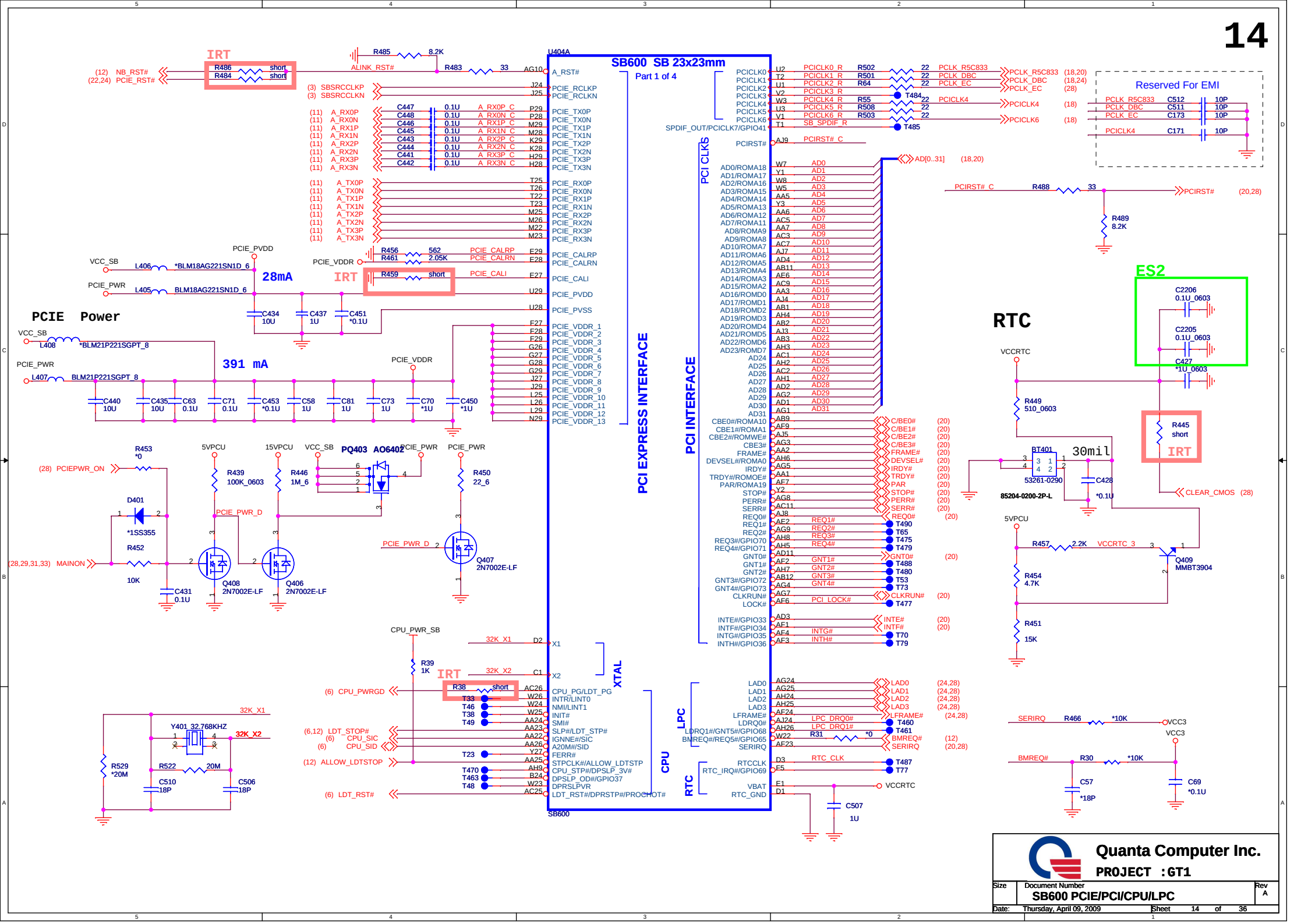


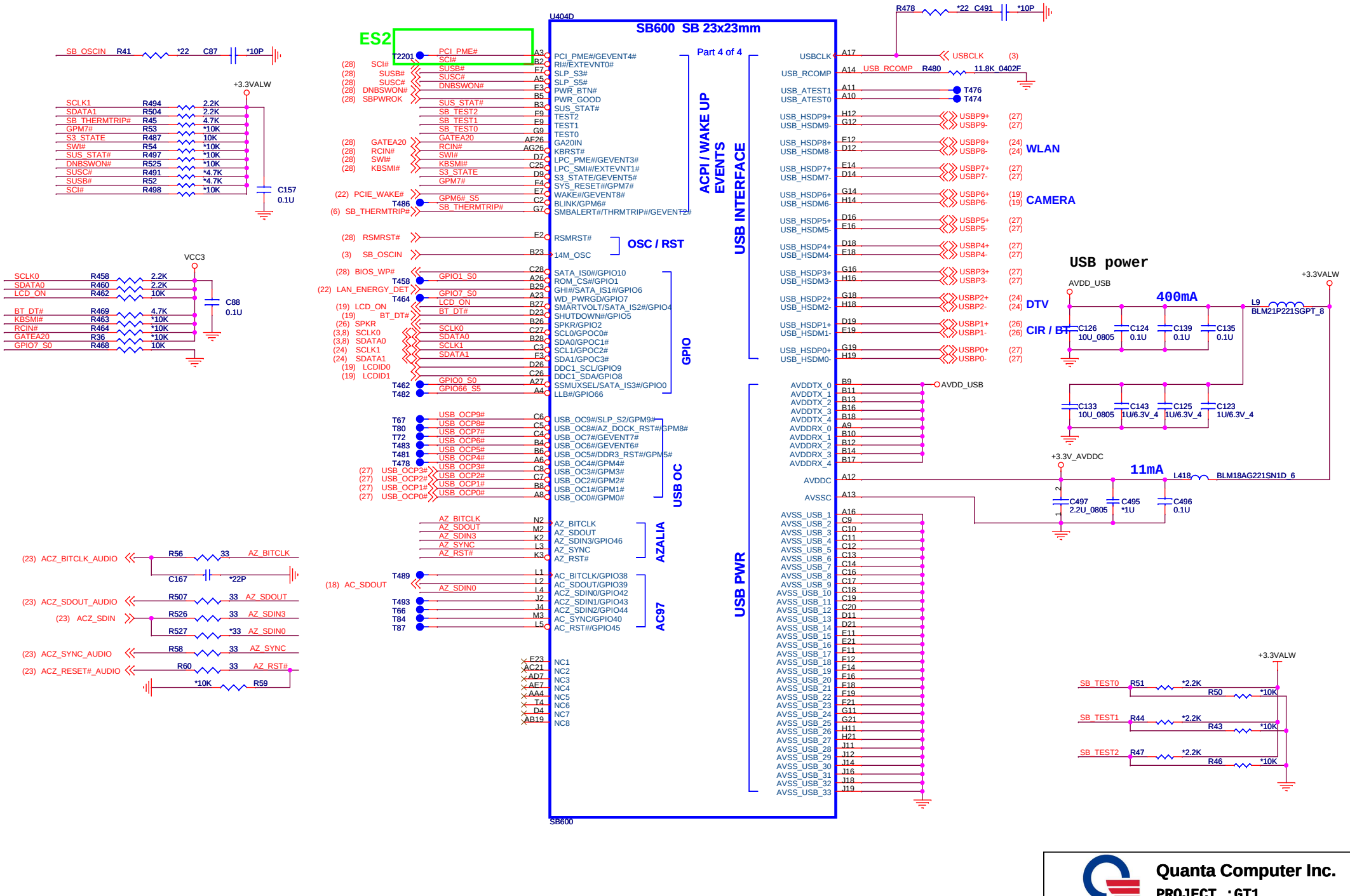
Quanta Computer Inc.		
PROJECT : GT1		
Size	Document Number: RS690MC PCIE LINK I/F	Rev: A
Date: Thursday, April 09, 2009	Sheet 11 of 36	



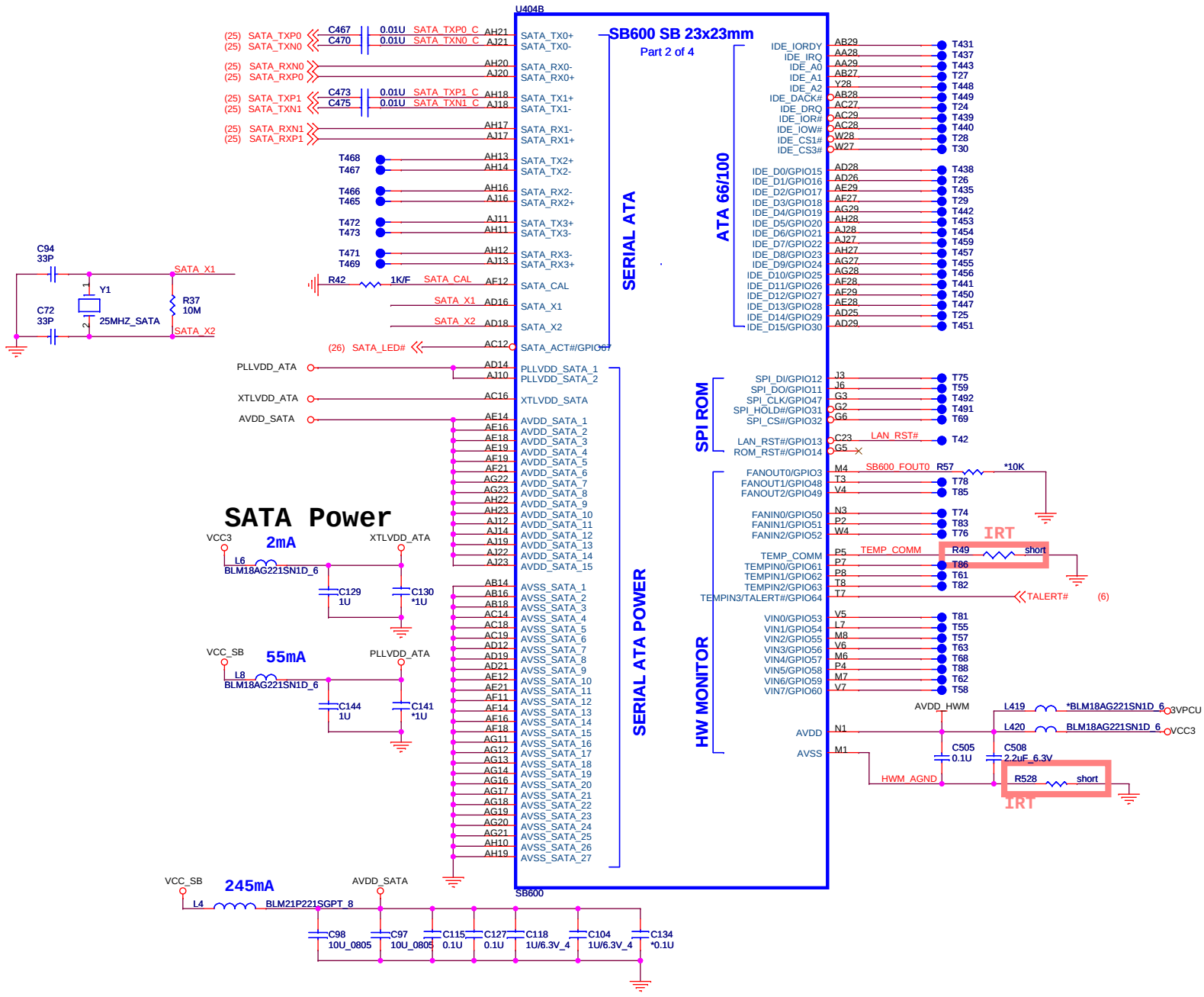
Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number		Rev
	RS690MC PLL & VEDIO I/F		A
Date: Thursday, April 09, 2009	Sheet 12 of 36		


PAR 5 OF 5
GROUND
U402E
RS690MC
PART 4 OF 5
POWER
U402D
RS690MC
VLDT_RUN
380mA
149mA
1mA
2581mA
15mA
IRT
short
VCC1.2
VDDA12
VDDC
VDDR3
VDDDVO
VDDPLL
VDD18
VCC1.8
VCC3
L7
L5
L3
L2
L411
L417
L401
L2013
FCM2012C-121
BLM21P221SGPT_8
60ohm_3A
For EMI VDDC :Decrease 800MHz frequency
D406
D405
D404
1SS355
Quanta Computer Inc.
PROJECT :GT1
RS690MC POWER
Rev A
Thursday, April 09, 2009
Sheet 13 of 36

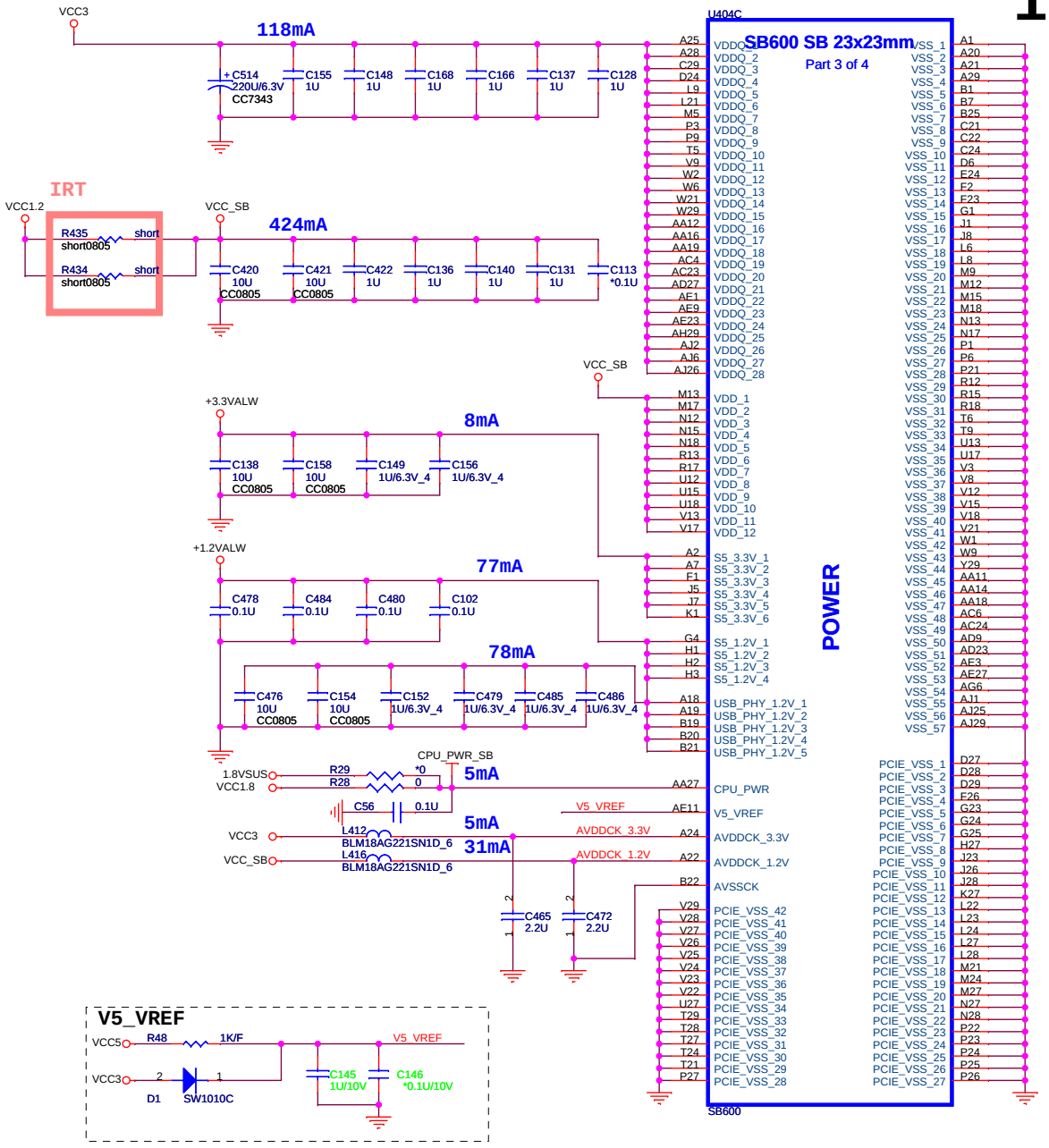

SB600 SB 23x23mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
SB600
PCIE Power
RTC
ES2
IRT
28mA
391 mA
PQ403 AO6402
Reserved For EMI
Quanta Computer Inc.
PROJECT :GT1
SB600 PCIE/PCI/CPU/LPC
Rev A
Thursday, April 09, 2009
Sheet 14 of 36



Quanta Computer Inc.	
PROJECT : GT1	
Size	Document Number: SB600 ACPI/GPIO/USB/AC97 — Rev: A
Date: Thursday, April 09, 2009	Sheet 15 of 36

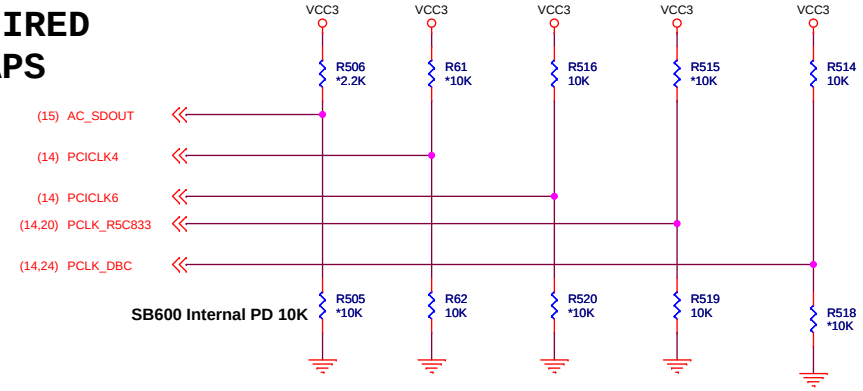


Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number		Rev
	SB600 HDD		A
Date:	Thursday, April 09, 2009	Sheet 16 of 36	



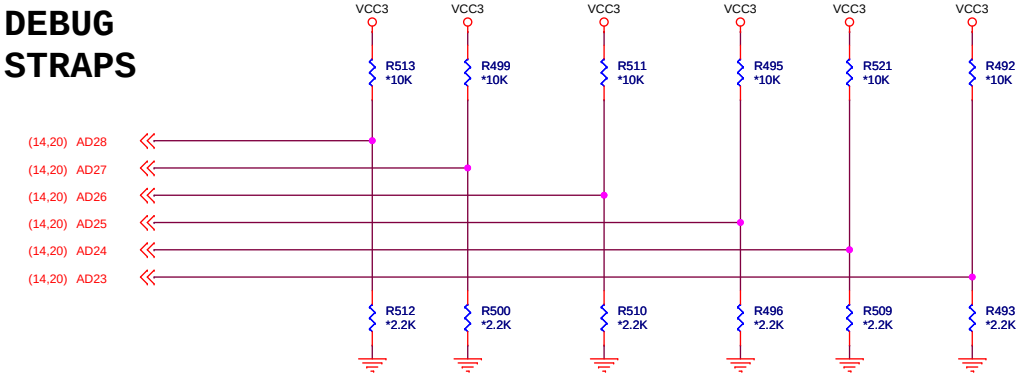
Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number		Rev
	SB600 POWER/DECOUPLING		A
Date: Thursday, April 09, 2009		Sheet 17 of 36	

REQUIRED STRAPS



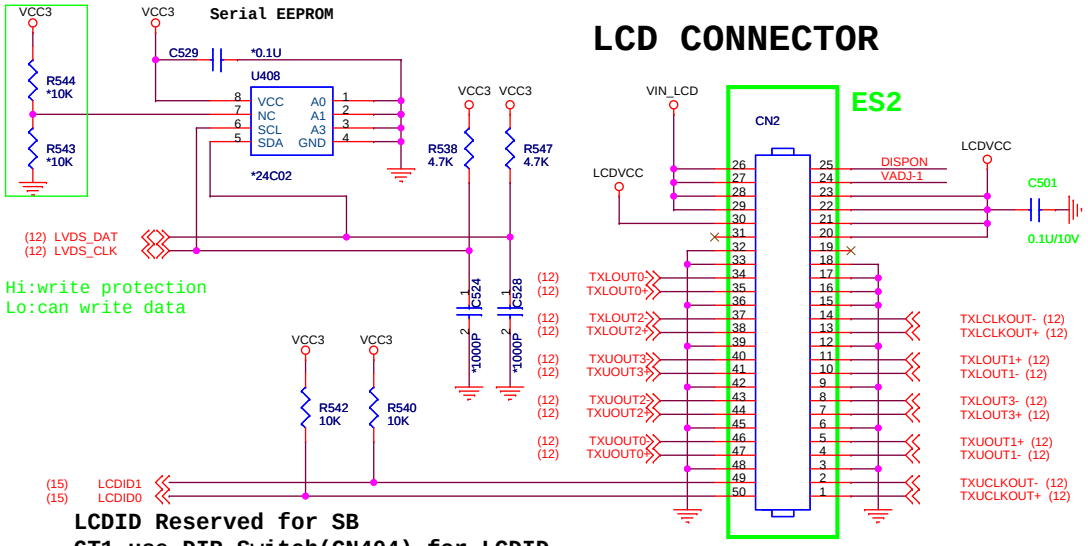
	AC_SDOUT	PCICLK4	PCICLK6	PCLK_R5C833 PCI_CLK0	PCLK_DBC PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

DEBUG STRAPS



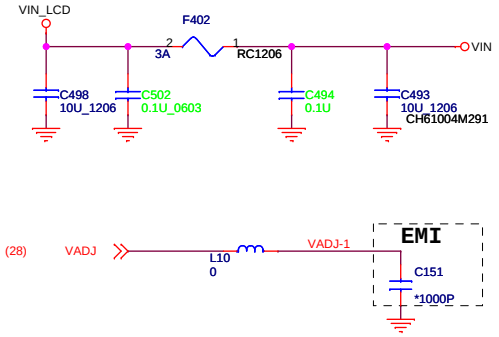
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

LCD CONNECTOR

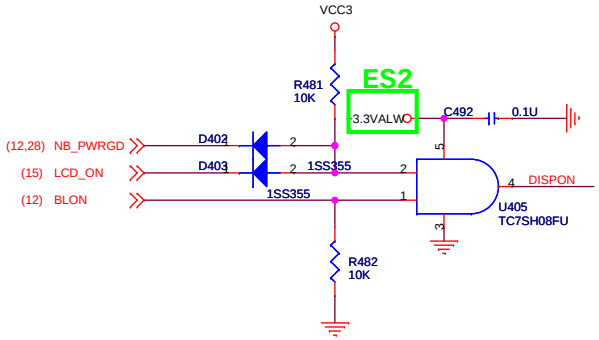


LCDID Reserved for SB
GT1 use DIP Switch(CN404) for LCDID

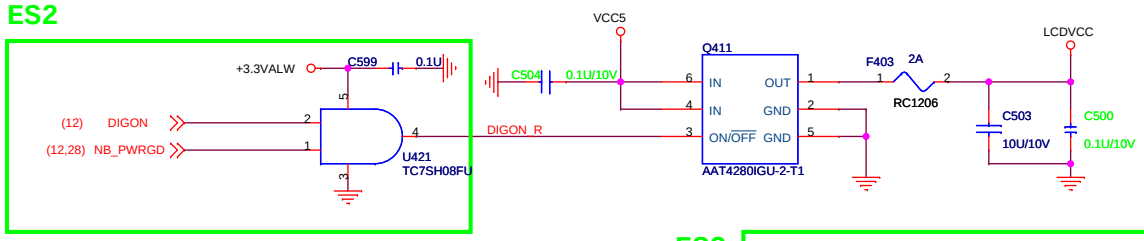
INVERTER POWER

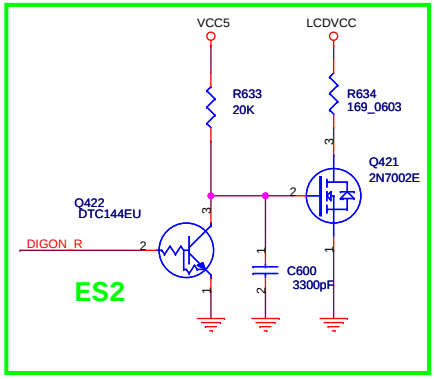


BACKLIGHT CONTROL

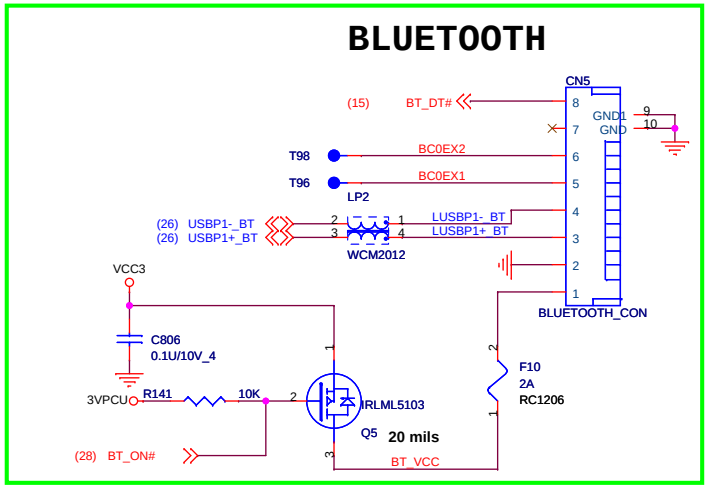


PANEL VCC CONTROL



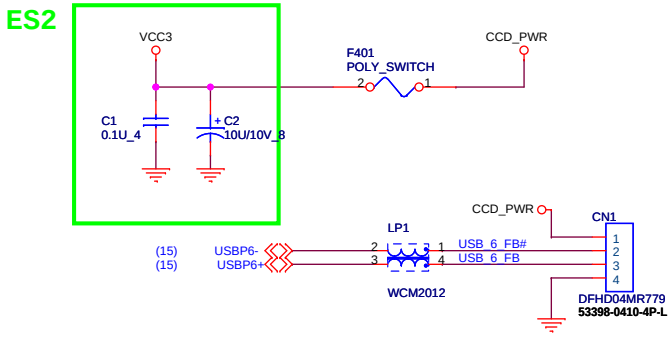


BLUETOOTH



BT_ON#	High	low
	No device	Bluetooth IN

CAMERA



Quanta Computer Inc.	PROJECT : GT1	
Size	Document Number: CCD & LCD PANEL I/F	Rev A
Date: Thursday, April 09, 2009	Sheet 19 of 36	

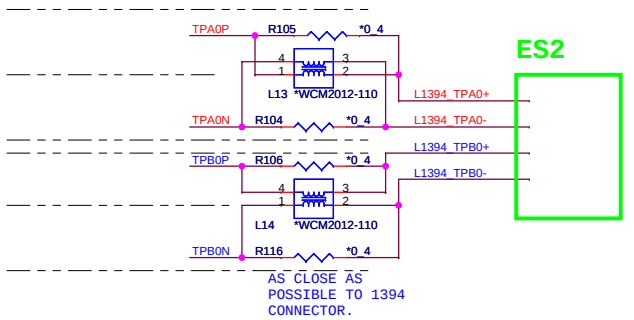
PCI Routing

AD24

INTE# , INTF#

REQ0#,GNT0#

1394 Reserved for Debug only

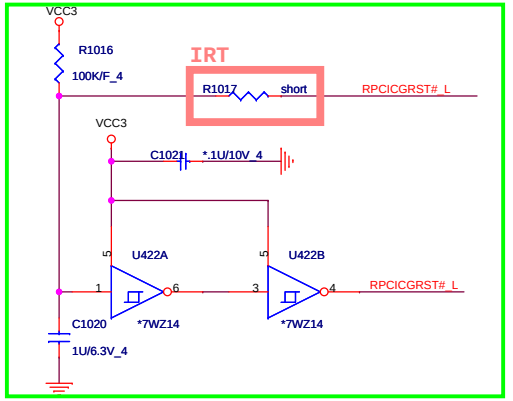


AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

*TPA/TPA#,TPB/TPB# pair trace : As close as possible.

*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layout with shields.

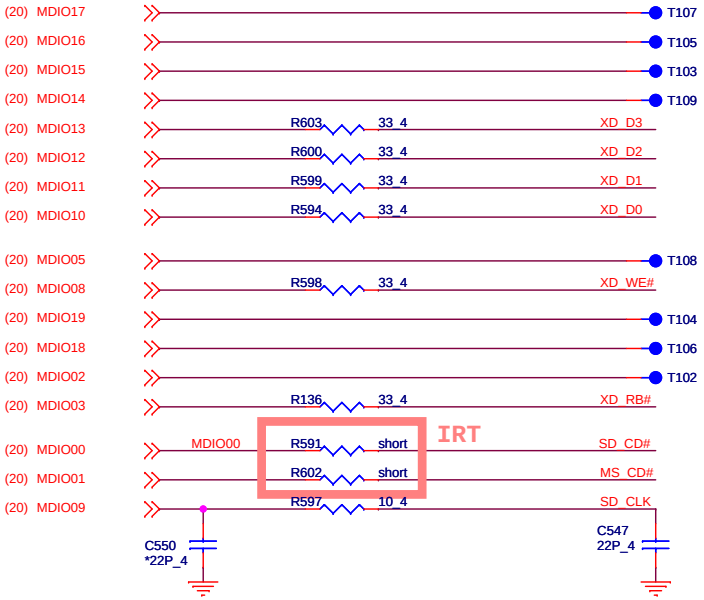
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.

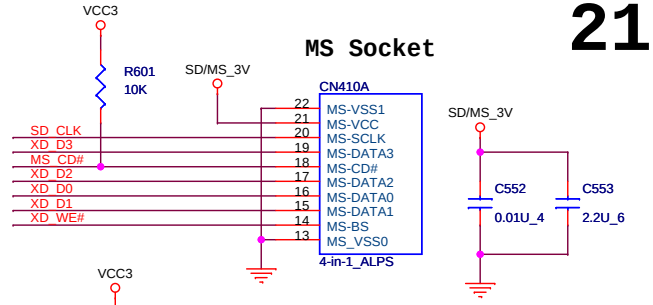
R5C833 not stuff

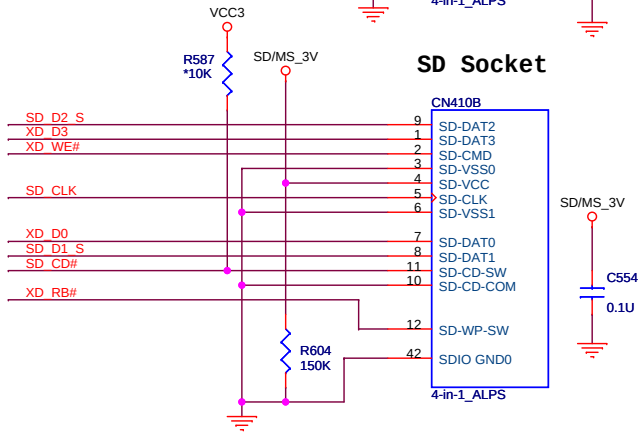
Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number: Card Reader R5C833		Rev A
Date: Thursday, April 09, 2009		Sheet 20 of 36	

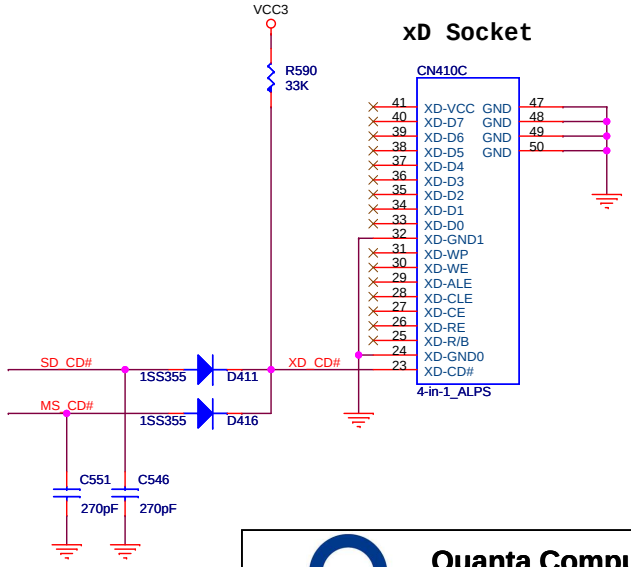


Card Detect

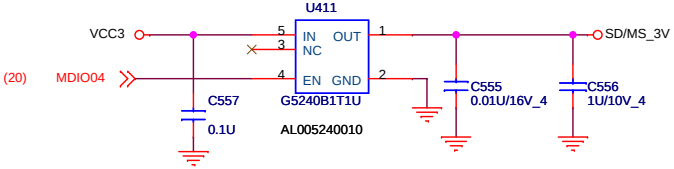
	MDIO00	MDIO01
SD/MMC	L	H
MS	H	L



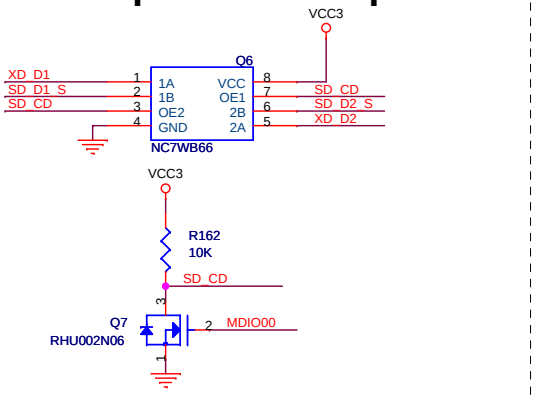




Flash Card Power SW



MSDuo pin short protect

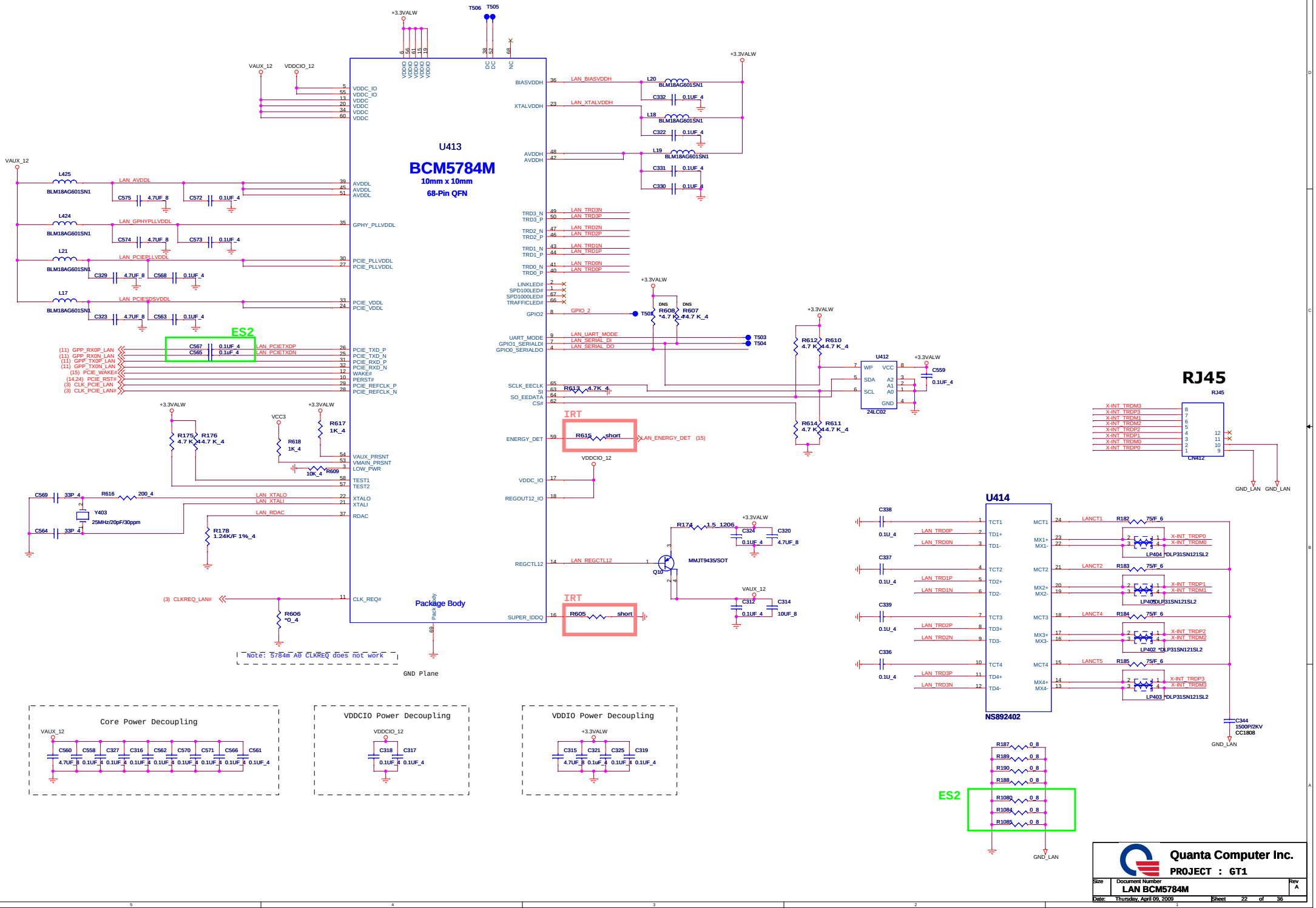


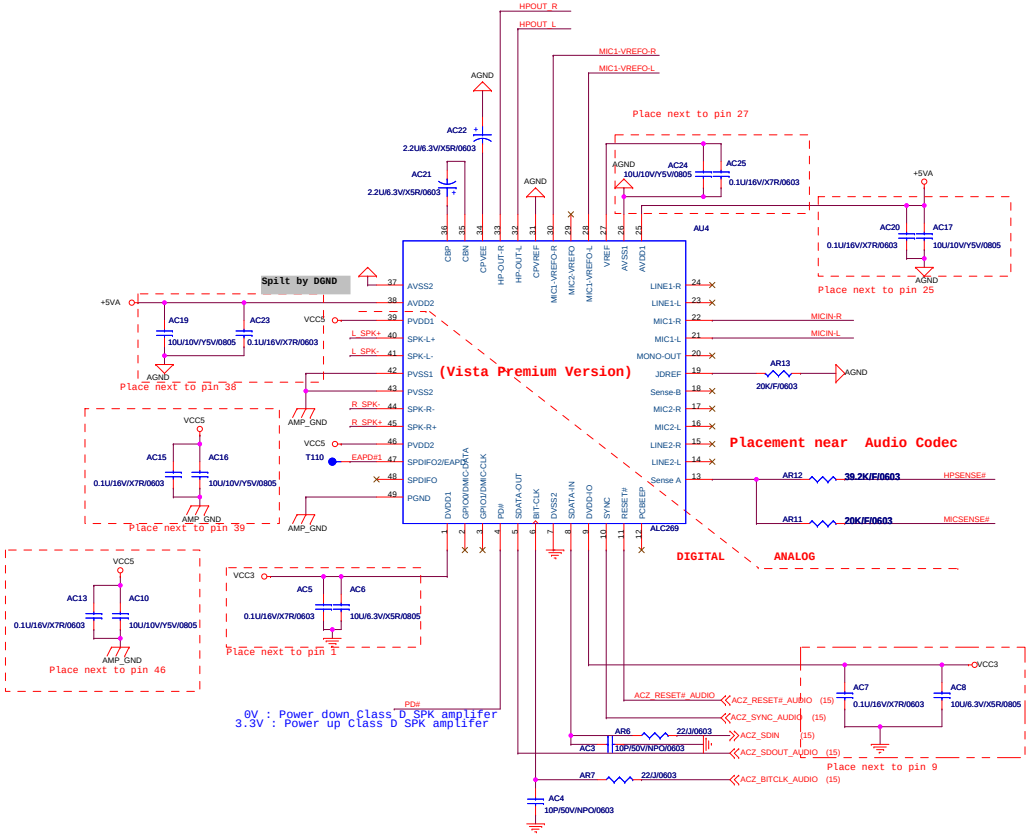
Quanta Computer Inc.

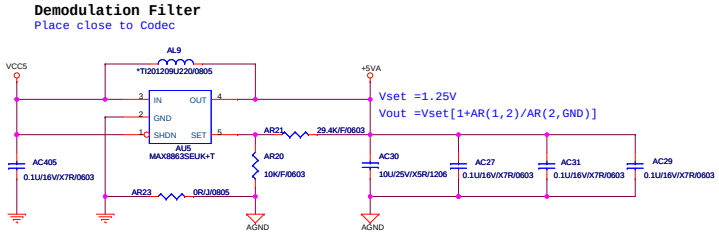
PROJECT : GT1

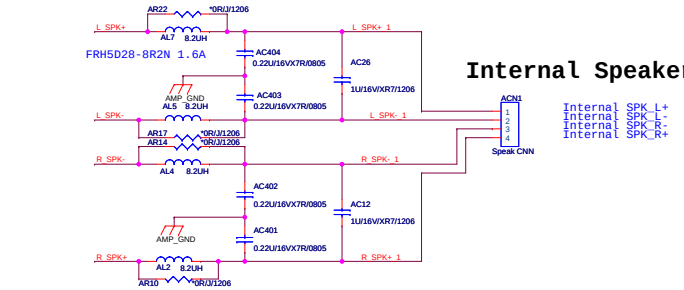
Size	Document Number	Rev
	Card Reader CONN	A

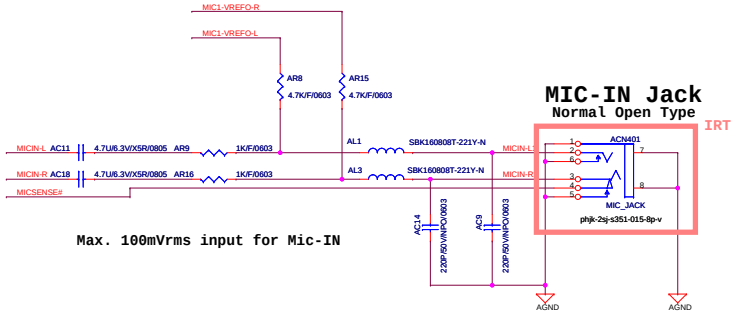
Date: Thursday, April 09, 2009 Sheet 21 of 36

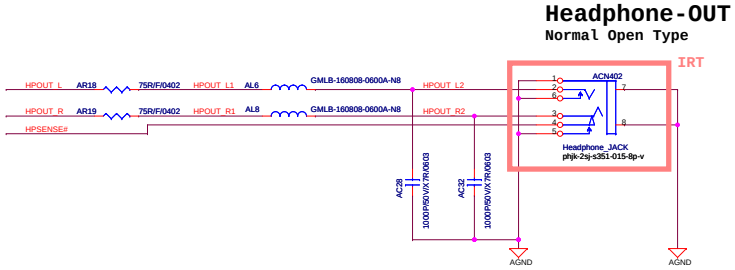

U413
BCM5784M
10mm x 10mm
68-Pin QFN
Package Body
ES2
IRT
RJ45
U414
NS892402
Core Power Decoupling
VDDCIO Power Decoupling
VDDIO Power Decoupling
Note: 5784m A0 CLKREQ does not work
GND Plane
Quanta Computer Inc.
PROJECT : GT1
LAN BCM5784M
Thursday, April 09, 2009

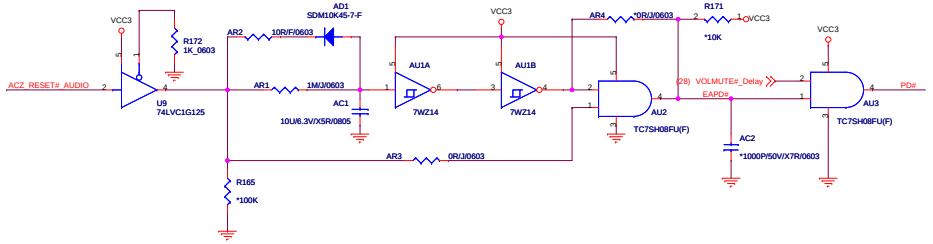






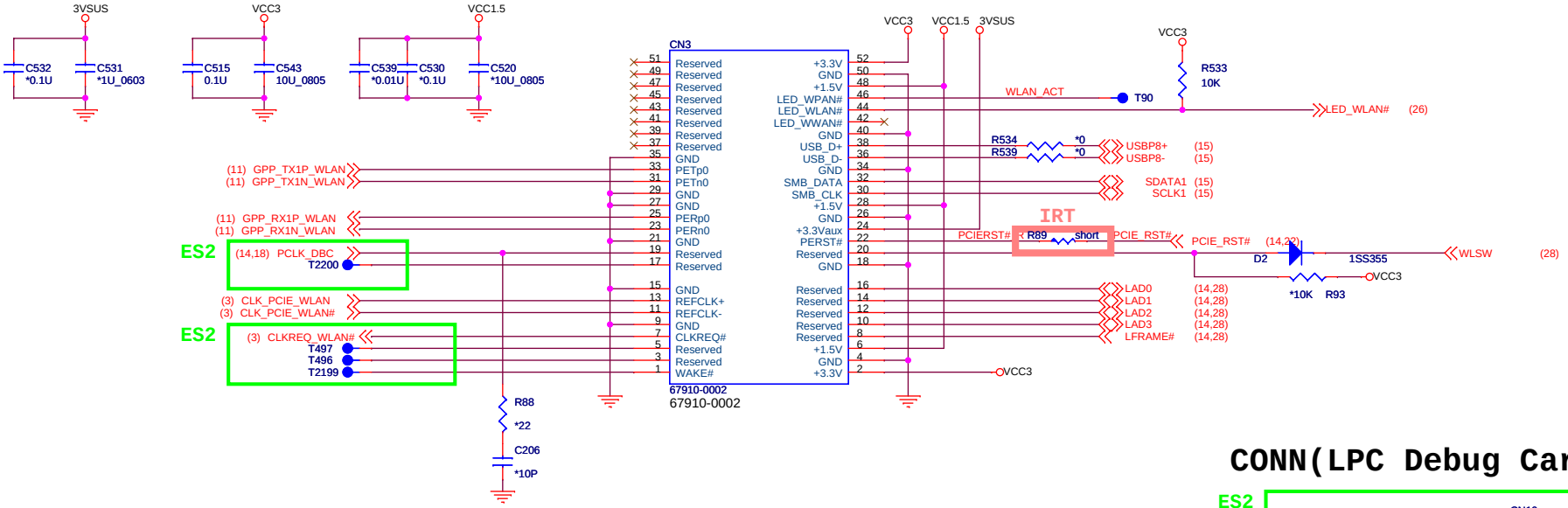




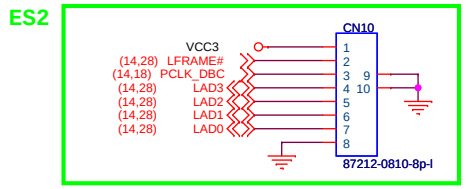


Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number		Rev
	HD ALC269		A
Date: Thursday, April 09, 2009		Sheet 23 of 36	

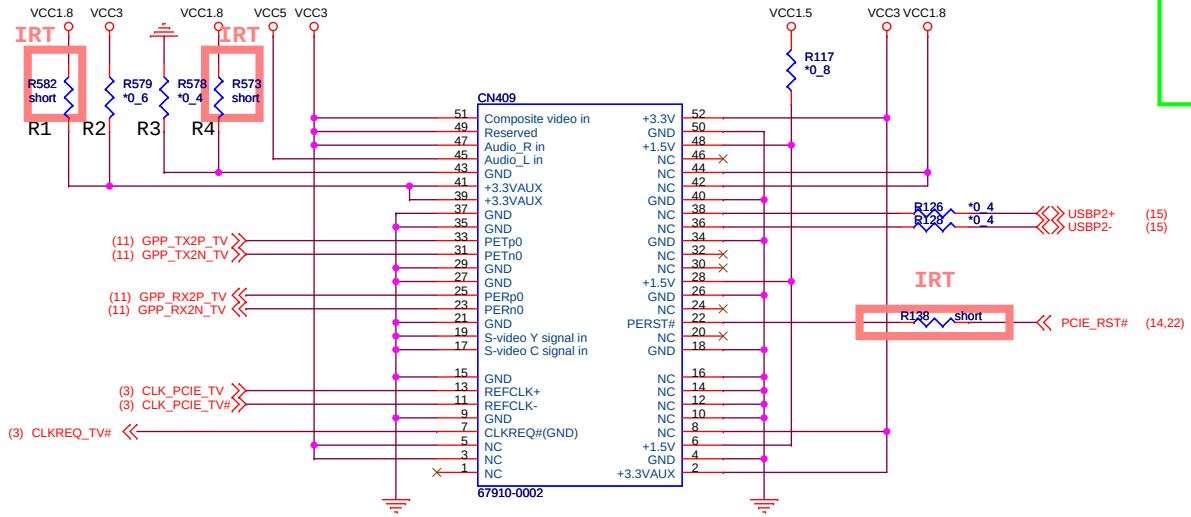
Mini Card (WLAN)

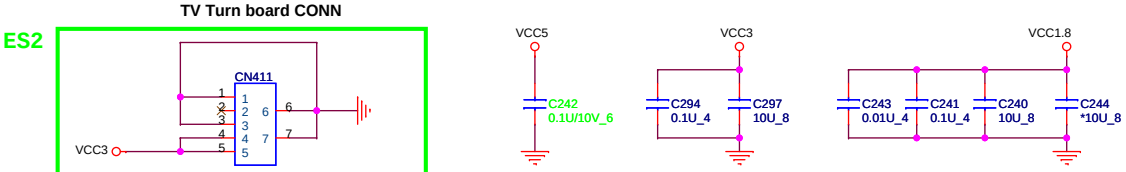


CONN(LPC Debug Card)



MINICARD CONN for S/W DTV

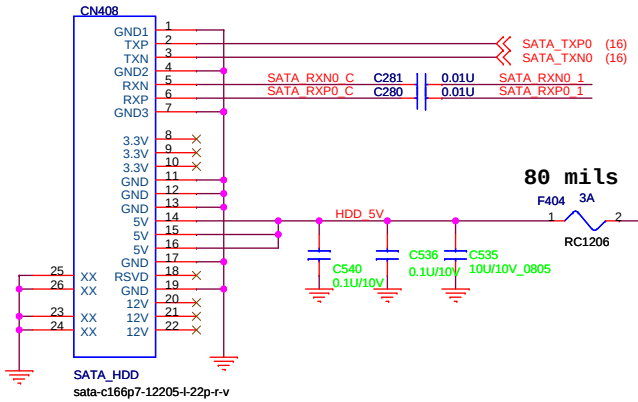




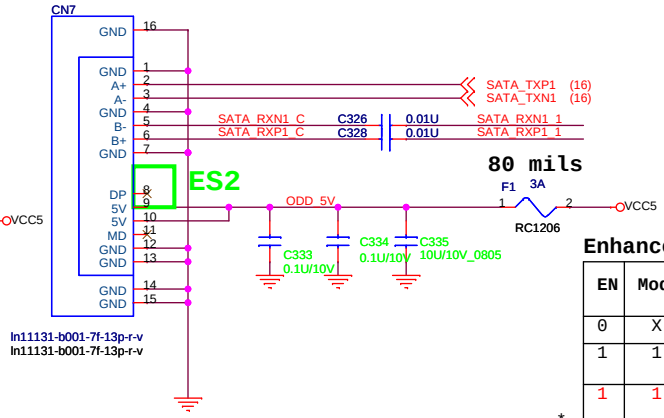
Quanta Computer Inc.
PROJECT : GT1

Size	Document Number	Rev
	MINI PCIE & FAN	A
Date: Thursday, April 09, 2009	Sheet 24 of 36	

SATA HDD



SATA ODD



Standard mode

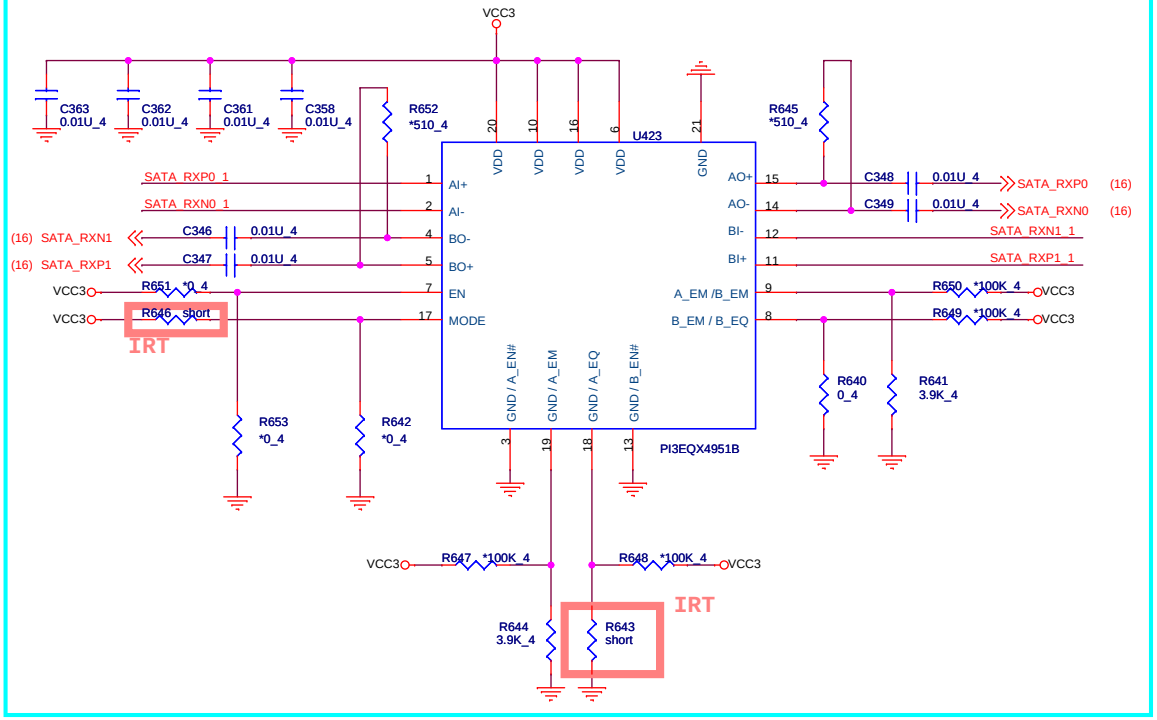
EN	Mode	B_EM	A_EM	Output B	Output A	Input B	Input A
0	X	X	X	Disable	Disable	Disable	Disable
1	0	0	0	0dB	0dB	2.5dB	2.5dB
1	0	0	1	0dB	3dB	2.5dB	2.5dB
1	0	1	0	3dB	0dB	2.5dB	2.5dB
* 1	0	1	1	3dB	3dB	2.5dB	2.5dB

Enhanced mode

EN	Mode	x_EN#	x_EQ	Input X Equalization	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	chip power down
1	1	1	X	n/a	X	n/a	chip enabled Channel x disabled
* 1	1	0	0	2.5dB	1.5K~20K resistor	resistor controlled (table A)	chip and channel enableed,low input equalization
1	1	0	1	6.5dB	1.5K~20K resister	resistor controlled (table A)	chip and channel enableed,low input equalization

SATA Re-driver IC

(Default---PI3EQX4951B Enhanced mode, Emphasis is +3dB)



PP

table A

Pre-emphasis	R_EX(K-Ohm)
0dB	Do Not Cnnect
+1.5dB	6.98
+2.0dB	5.76
+2.5dB	4.7
* +3.0dB	3.9
+3.5dB	3.4
+4.0dB	2.94
+4.5dB	2.49
+5.0dB	2.21
+5.5dB	1.91
+6.0dB	1.69

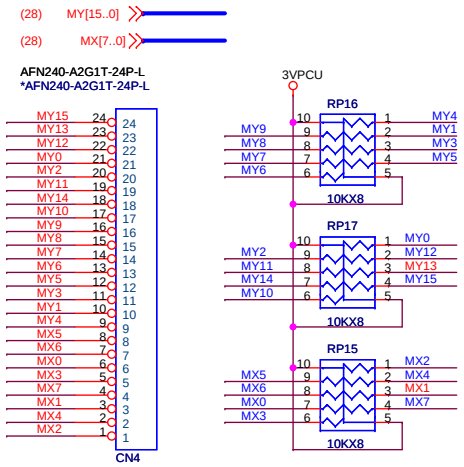
table B

	Standard mode	* Enhanced mode	MAX4951(Boost)
R640	NC	0 ohm	NC
R641	NC	3.9K	NC
R642	0 ohm	NC	0 ohm
R643	0 ohm	0 ohm	0 ohm
R644	0 ohm	3.9K	0 ohm
R645	NC	NC	NC
R646	NC	0 ohm	NC
R647	NC	NC	NC
R648	NC	NC	NC
R649	100K ohm	NC	100K ohm
R650	100K ohm	NC	100K ohm
R651	NC	NC	100K ohm
R652	NC	NC	NC
R653	NC	NC	NC

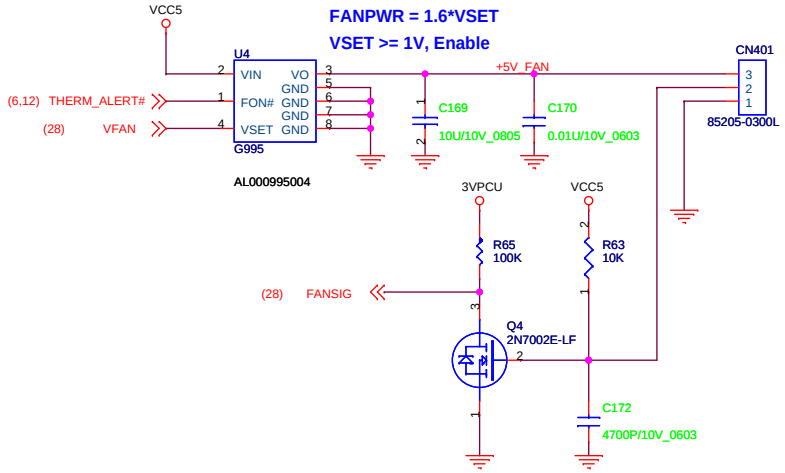
MAX4951

EN	A_EM	B_EM	Output A	Output B
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

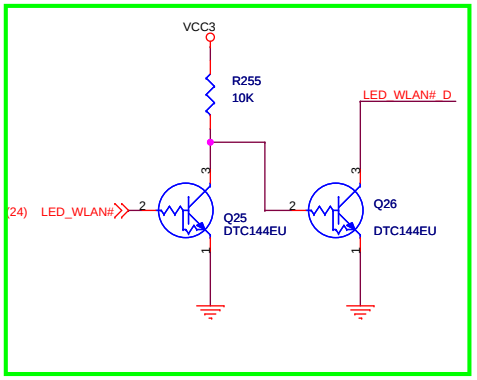
KB CONN(Reserved for EC debug)



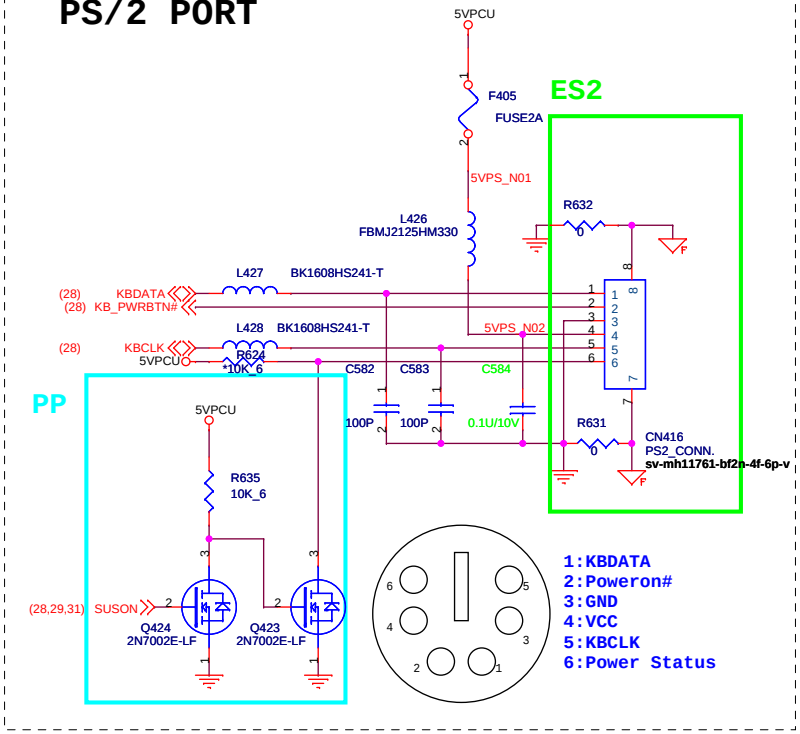
FAN Driver



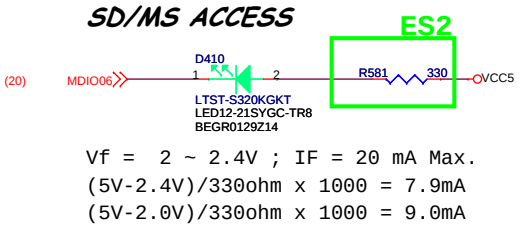
ES2



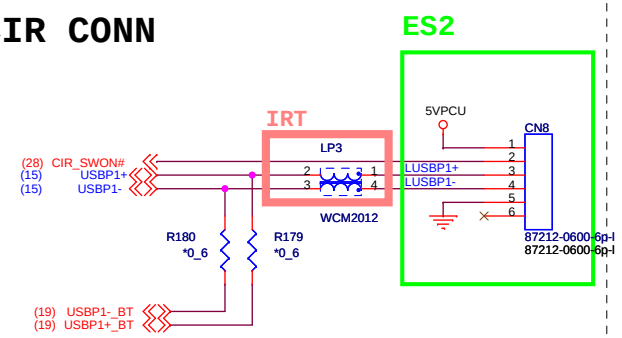
PS/2 PORT



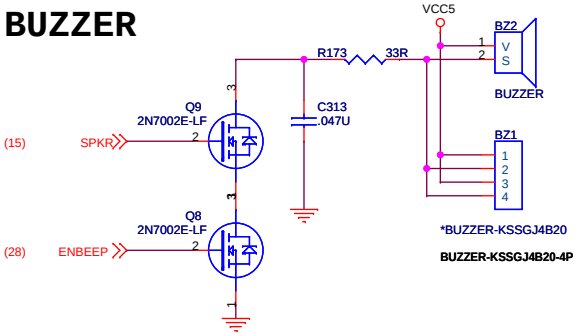
Media Card Access LED



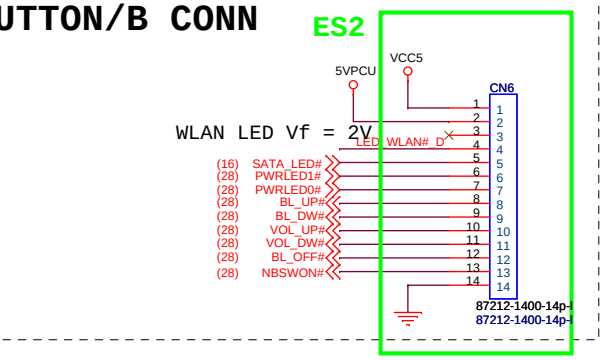
CIR CONN

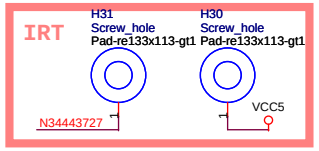


BUZZER



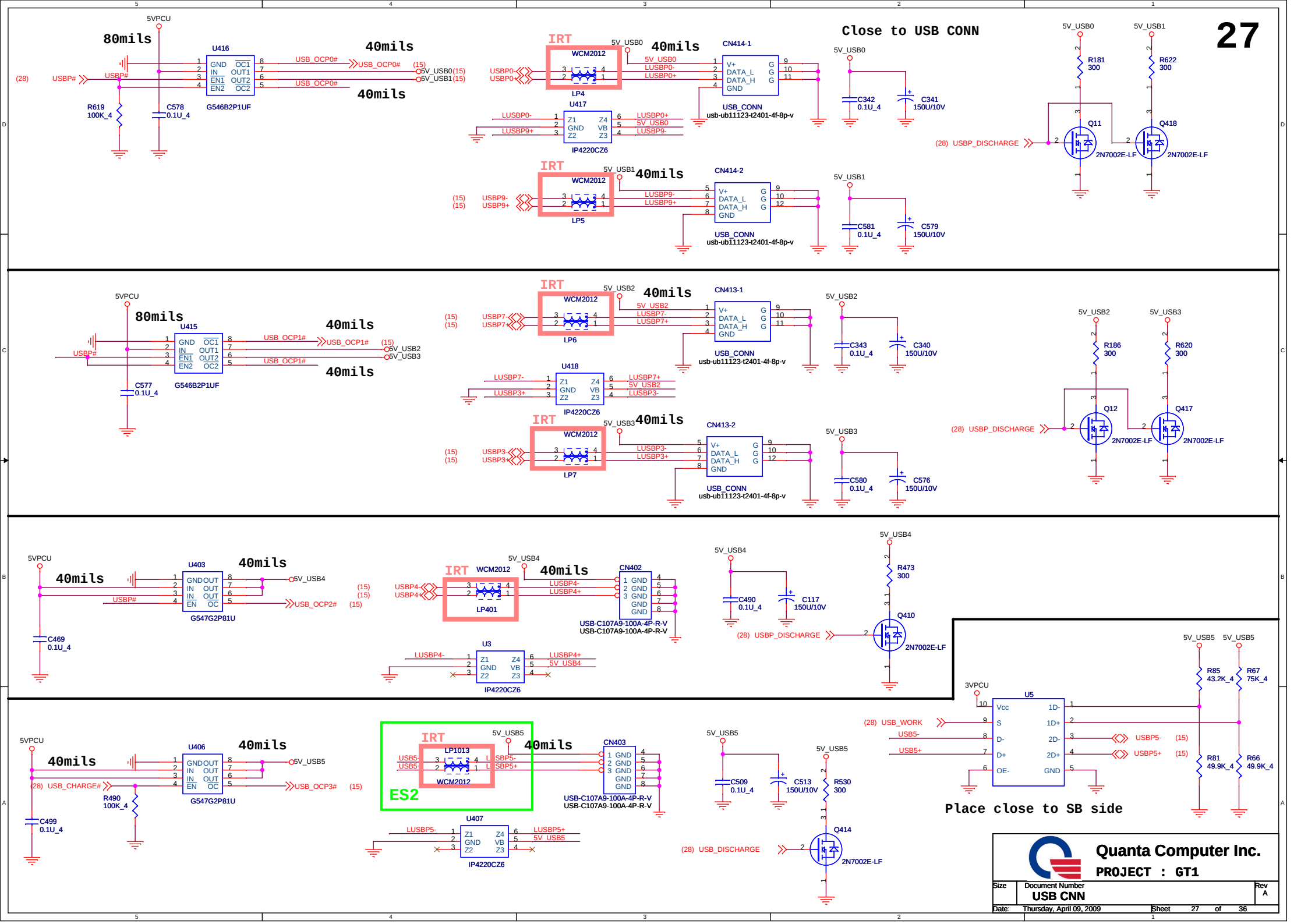
BUTTON/B CONN

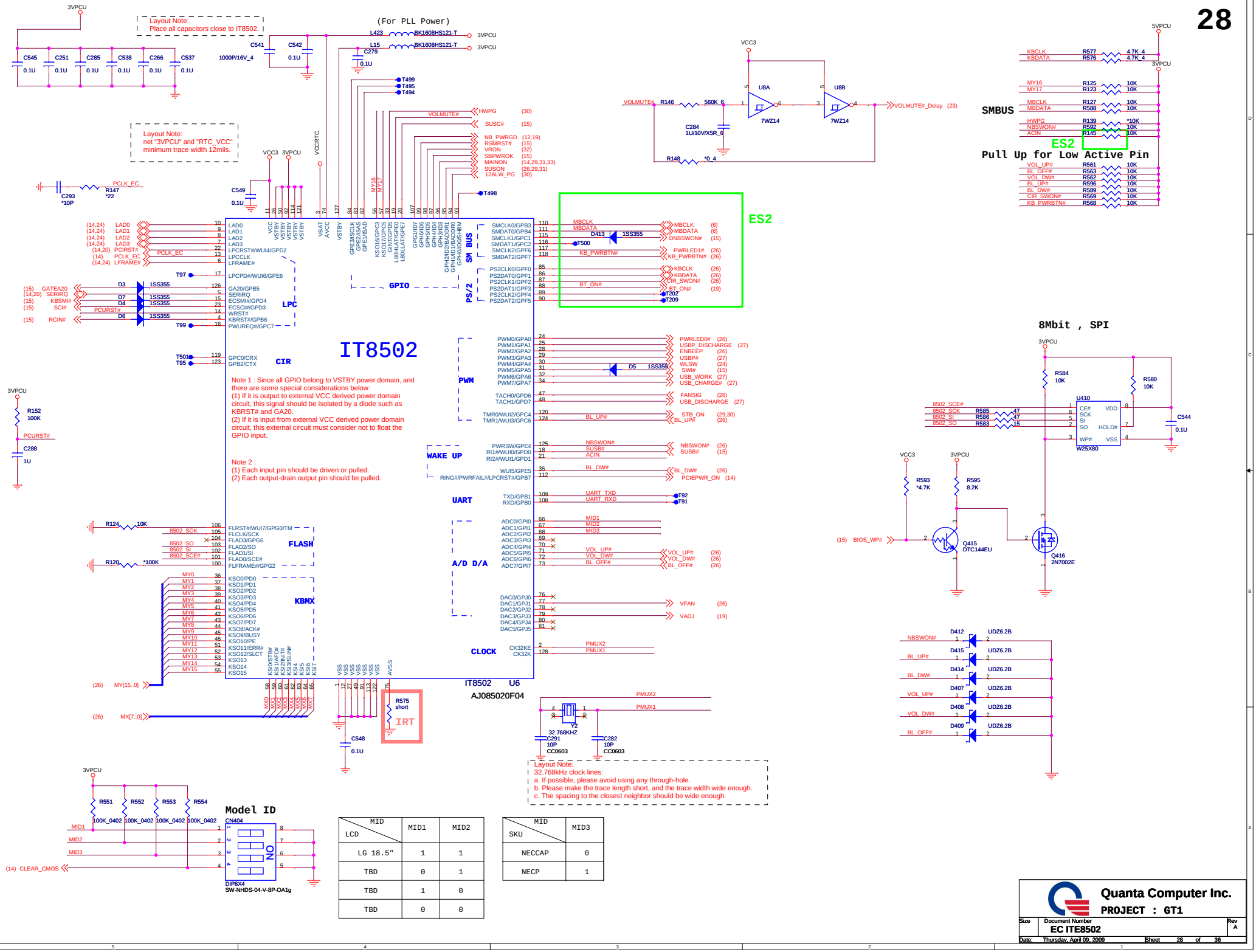




Quanta Computer Inc.
PROJECT : GT1

Size	Document Number	Rev
	PS2/ FAN /UI	A
Date: Thursday, April 09, 2009	Sheet 26 of 36	


Close to USB CONN
5VPCU
80mils
U416
G546B2P1UF
USBP#
USB_OCP0#
40mils
R619 100K_4
C578 0.1U_4
IRT
WCM2012
LP4
5V_USB0
USBP0-
USBP0+
U417
IP4220CZ6
LUSBP0-
LUSBP9+
LUSBP9-
CN414-1
USB_CONN
usb-ub11123-t2401-4f-8p-v
C342 0.1U_4
C341 150U/10V
R181 300
R622 300
Q11
Q418
2N7002E-LF
USBP_DISCHARGE
LP5
CN414-2
5V_USB1
C581 0.1U_4
C579 150U/10V
U415
G546B2P1UF
USB_OCP1#
C577 0.1U_4
LP6
CN413-1
C343 0.1U_4
C340 150U/10V
R186 300
R620 300
Q12
Q417
LP7
CN413-2
C580 0.1U_4
C576 150U/10V
U403
G547G2P81U
C469 0.1U_4
LP401
CN402
USB-C107A9-100A-4P-R-V
C490 0.1U_4
C117 150U/10V
R473 300
Q410
3VPCU
U5
Vcc
S
D-
D+
OE-
1D-
1D+
2D-
2D+
GND
USB_WORK
R85 43.2K_4
R67 75K_4
R81 49.9K_4
R66 49.9K_4
Place close to SB side
U406
G547G2P81U
USB_CHARGE#
R490 100K_4
C499 0.1U_4
LP1013
WCM2012
ES2
CN403
U407
IP4220CZ6
C509 0.1U_4
C513 150U/10V
R530 300
Q414
USB_DISCHARGE
Quanta Computer Inc.
PROJECT : GT1
Size
Document Number
USB CNN
Rev
A
Date: Thursday, April 09, 2009
Sheet 27 of 36



MID / LCD	MID1	MID2
LG 18.5"	1	1
TBD	0	1
TBD	1	0
TBD	0	0

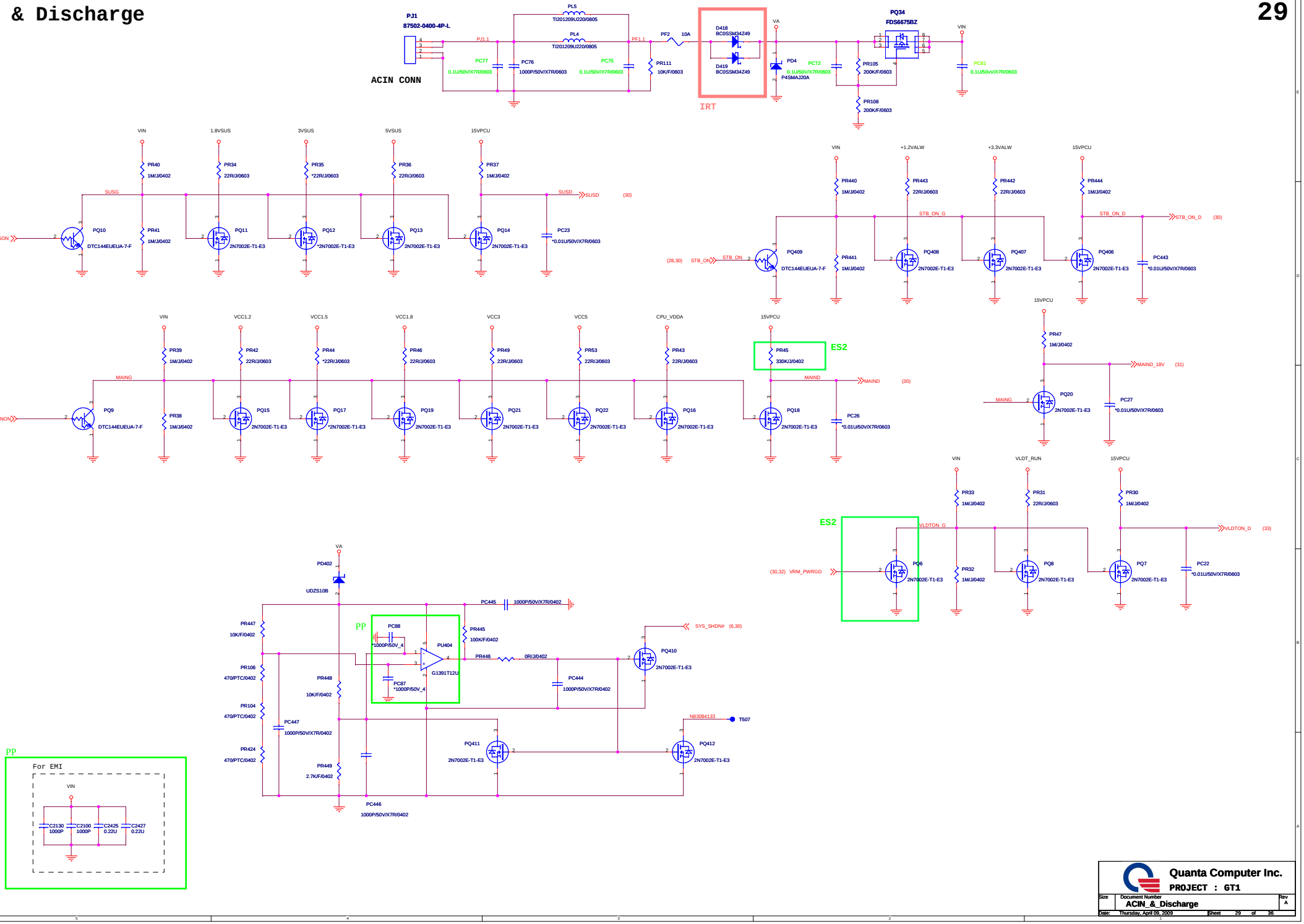
MID / SKU	MID3
NECCAP	0
NECP	1

Quanta Computer Inc.
PROJECT : GT1

Size	Document Number	Rev
	EC ITE8502	A

Date: Thursday, April 09, 2009 Sheet 28 of 36

ACIN & Discharge



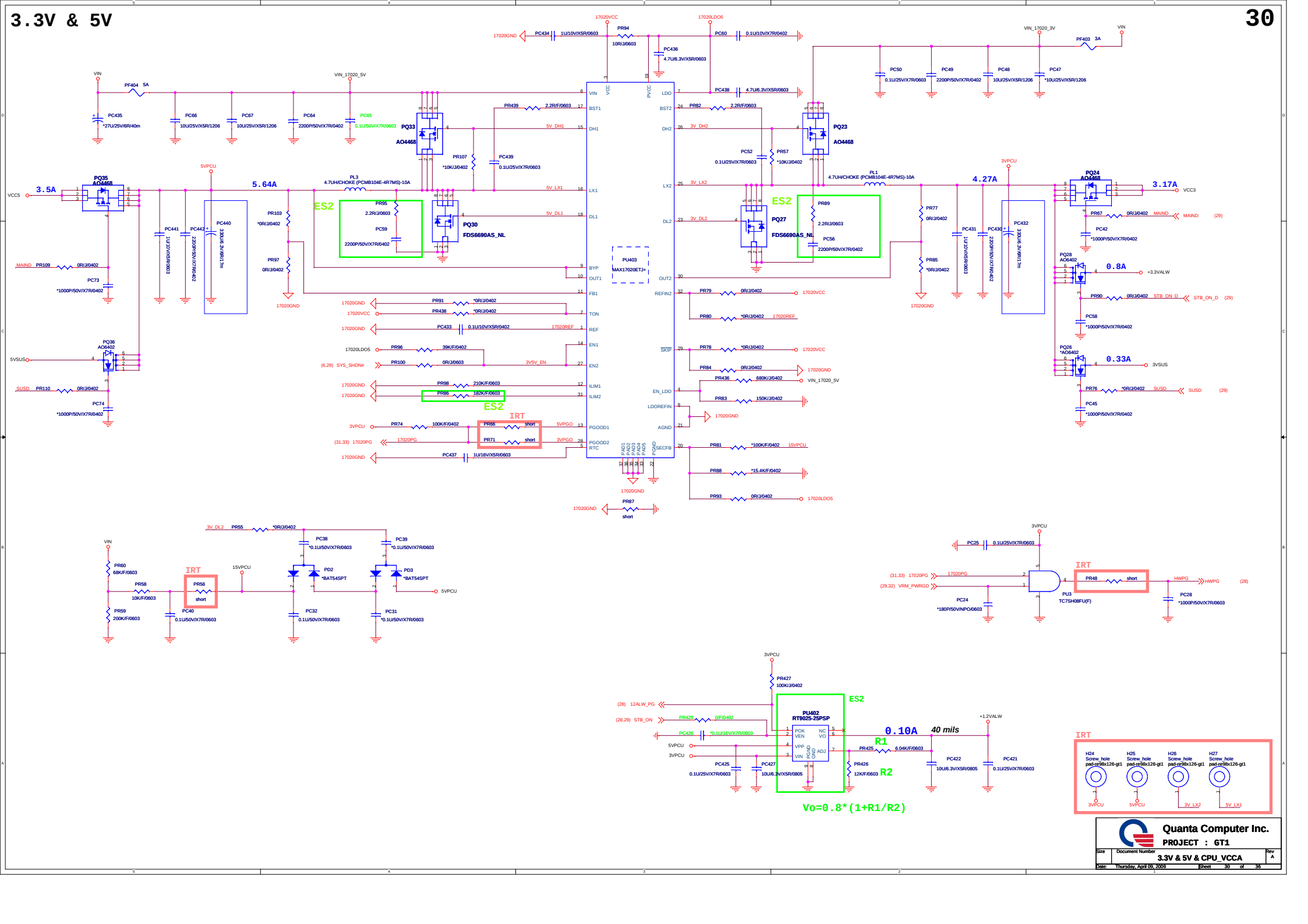
Quanta Computer Inc.

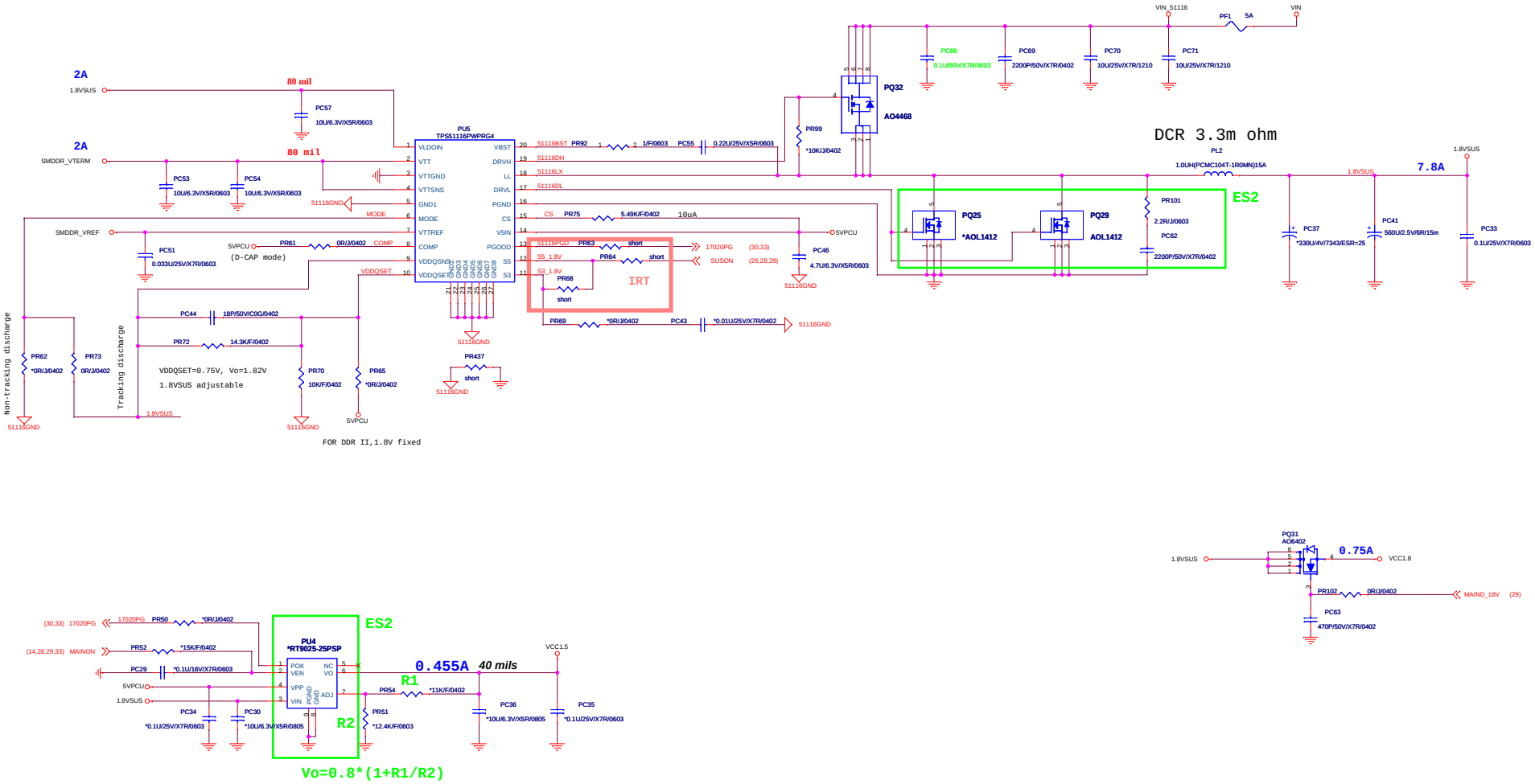
PROJECT : GT1

Size	Document Number	Rev
	ACIN_&_Discharge	A

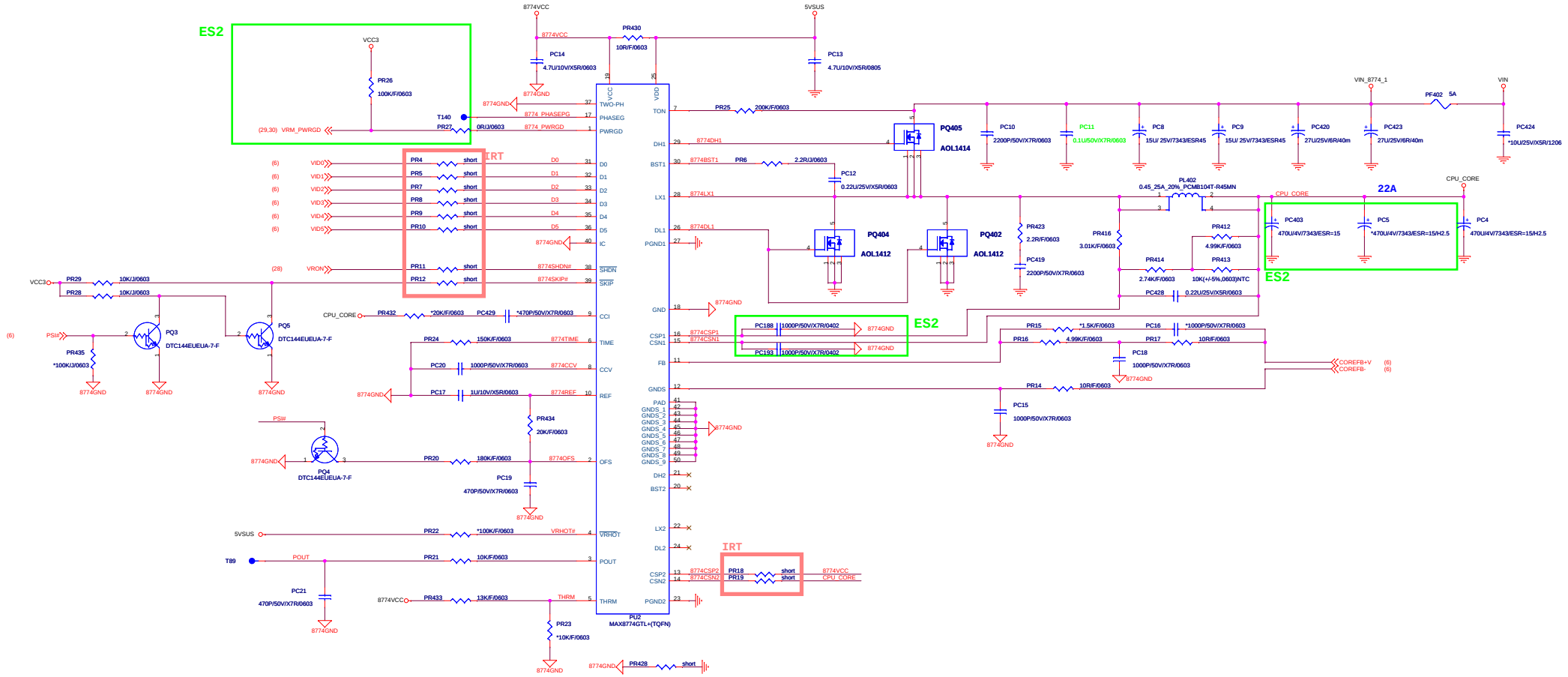
Date: Thursday, April 09, 2009 Sheet 29 of 36

3.3V & 5V

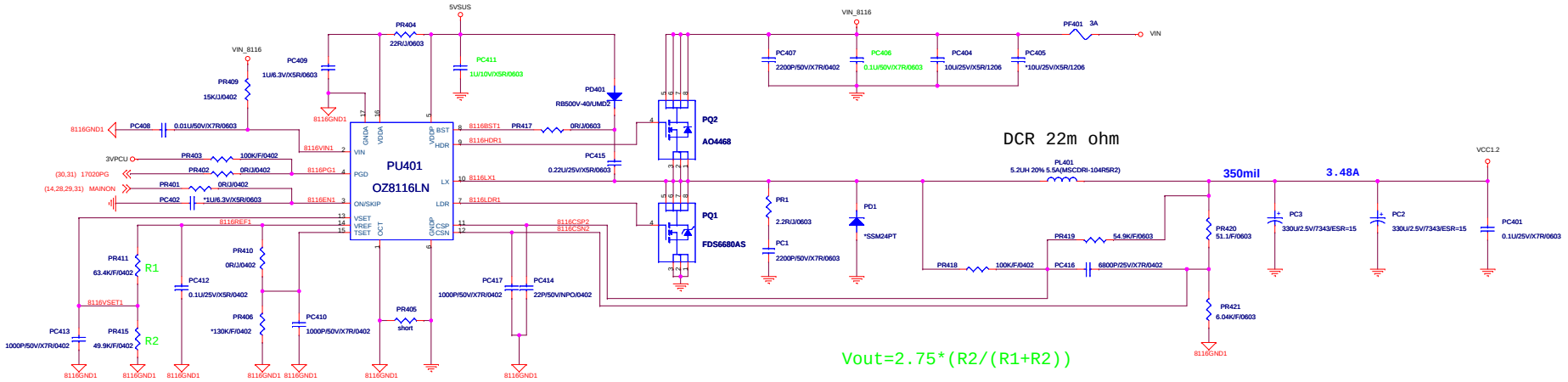

PU403 MAX17020ETJ+
PQ33 AO4468
PQ35 AO4468
PQ30 FDS6690AS_NL
PQ23 AO4468
PQ27 FDS6690AS_NL
PQ24 AO4468
PQ28 AO6402
PQ26 AO6402
PQ36 AO6402
PL3 4.7UH/CHOKE (PCMB104E-4R7MS)-10A
PL1 4.7UH/CHOKE (PCMB104E-4R7MS)-10A
ES2
IRT
3.5A
5.64A
4.27A
3.17A
0.8A
0.33A
0.10A
40 mils
R1
R2
Vo=0.8*(1+R1/R2)
PU402 RT9025-25PSP
PU3 TC7SH08FU(F)
Quanta Computer Inc.
PROJECT : GT1
3.3V & 5V & CPU_VCCA
Thursday, April 09, 2009

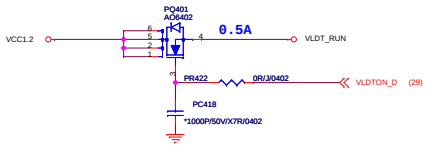


Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number		Rev
	1.8VSUS & VCC1.8 & VCC1.5		A
Date: Thursday, April 09, 2009	Sheet 31 of 36		



Quanta Computer Inc.			
PROJECT : GT1			
Size	Document Number		Rev
	CPU CORE(MAX8774)		A
Date: Thursday, April 09, 2009		Sheet 32 of 36	





Quanta Computer Inc.

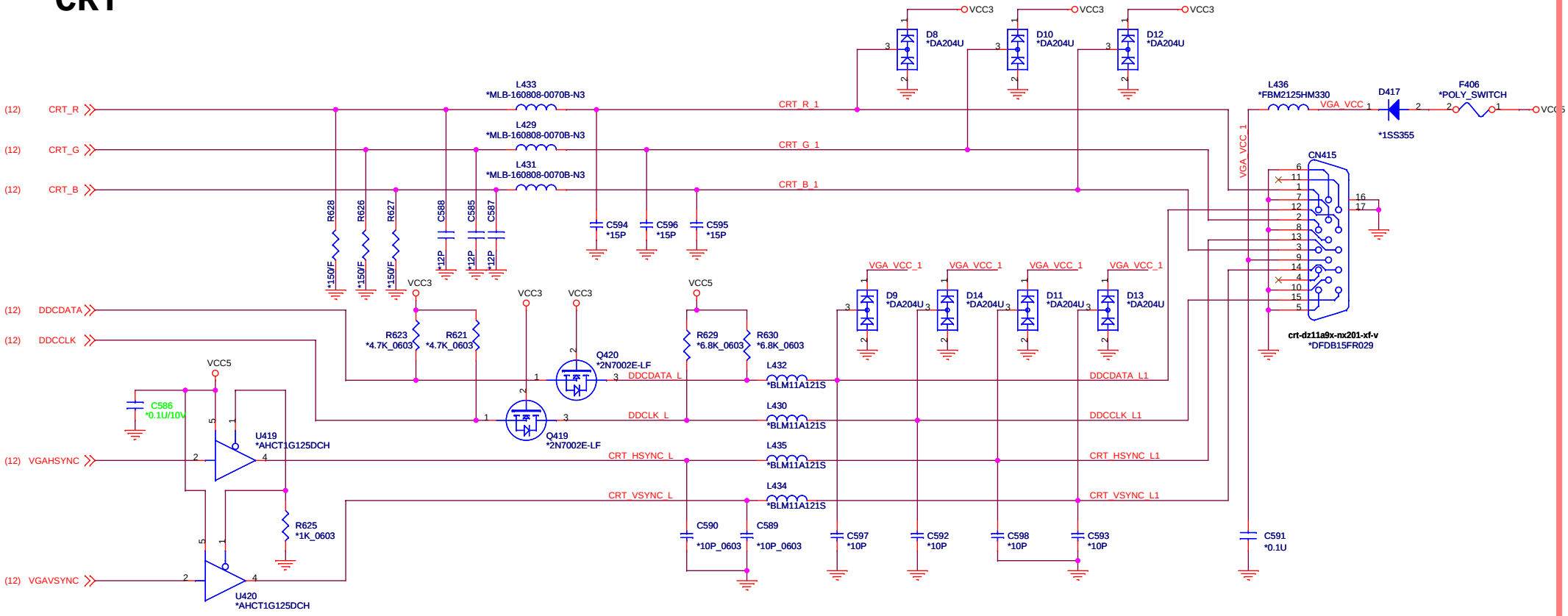
PROJECT : GT1

Size	Document Number	Rev
	VCC1.2 & VLDT_RUN & 12V	A

Date: Thursday, April 09, 2009 Sheet 33 of 36

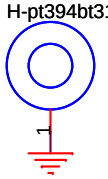
All Component in This Page is Reserved for Debug Only

CRT

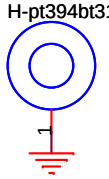


Quanta Computer Inc.		
PROJECT : GT1		
Size	Document Number: CRT	Rev: A
Date: Thursday, April 09, 2009	Sheet 34 of 36	

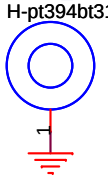
H2
Screw_hole
H-pt394bt315d240p2



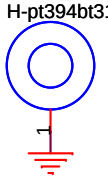
H9
Screw_hole
H-pt394bt315d240p2



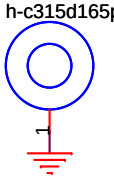
H8
Screw_hole
H-pt394bt315d240p2



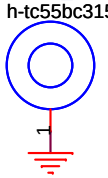
H3
Screw_hole
H-pt394bt315d240p2



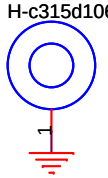
H14
Screw_hole
h-c315d165p2



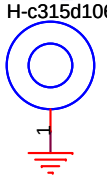
H4
Screw_hole
h-tc55bc315d55i55p2



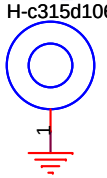
H17
Screw_hole
H-c315d106p2



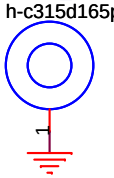
H5
Screw_hole
H-c315d106p2



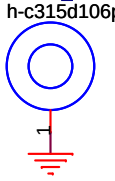
H7
Screw_hole
H-c315d106p2



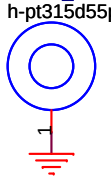
H11
Screw_hole
h-c315d165p2



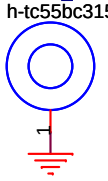
H13
Screw_hole
h-c315d106p2



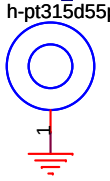
H12
Screw_hole
h-pt315d55pt



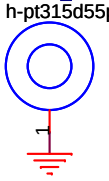
H6
Screw_hole
h-tc55bc315d55i55p2



H10
Screw_hole
h-pt315d55pt

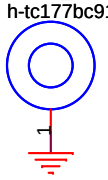


H401
Screw_hole
h-pt315d55pt

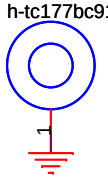


ES2

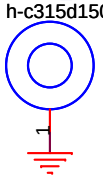
H19
Screw_hole
h-tc177bc91d91p2



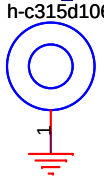
H18
Screw_hole
h-tc177bc91d91p2



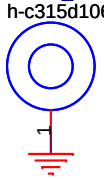
H15
Screw_hole
h-c315d150p2



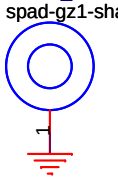
H20
Screw_hole
h-c315d106p2



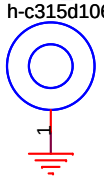
H21
Screw_hole
h-c315d106p2



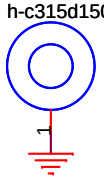
PAD1
Screw_hole
spad-gz1-shape1np



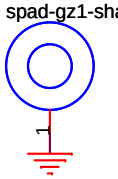
H1
Screw_hole
h-c315d106p2



H16
Screw_hole
h-c315d150p2

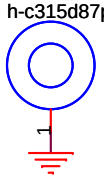


PAD2
Screw_hole
spad-gz1-shape1np

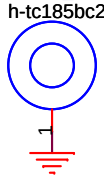


IRT

H22
Screw_hole
h-c315d87p2



H23
Screw_hole
h-tc185bc236d106p2



Quanta Computer Inc.

PROJECT : GT1

Size	Document Number	Rev
	History	A

Date: Thursday, April 09, 2009 Sheet 35 of 36

GT1 Mother Board Schematics Revision History

PCB Rev	Sch Rev	BOM Rev	DATE	Change List & Description
A	1A	A1A	Jan/06/09'	* 1st Release
B	2A	B1A	Feb/06/09'	Page 08 Mount R91 and R101 , demount R90 and R102 for memory can't be recognized Page 14 Add C2205 C2206 for EMI Page 15 Remove PCIE_PME# for S3 auto boot issue by Ricoh suggest Page 19 Change panel VCC control by DIGON and NB_PWRGD Page 19 Change CN2 footprint.Add F10 Page 20 Remove 1394 connector then add test point Page 20 Reserve 2 inverter for GBRST# timing of R5C833 Page 20 Add U422,C1021,Delete 1394 connector location Page 22 Change C567,C565 to X5R type Page 22 Add R1080 R1084 R1085 for GND_LAN Page 24 Change PCIRST# to pin22 of CN3, Add T2200 to pin17 on CN3 Page 24 Add CN10 for debug card Page 24 Change CLKREQ_WLAN# to PIN7 from PIN1,Add T2199 on PIN1 on CN3 Page 24 Delete PCIERST# and R89 on PIN22, Add T2200 on PIN22 of CN3 Page 25 Delete R177,change pin7 of CN7 to NC Page 26 Correct R581 to 330 ohm from 220 ohm Page 27 Add LP1013 on CN403 for EMI Page 28 Modify PS/2 function Page 29 Change PR45 to 330k ohm, make VCC3 assertion before VCC1.8 assertion Page 29 Change PQ6 to 2N7002,because former design make power on shut down Page 30 Add PR95 PR89 PC59 PC56 for power signal Page 30 Change PU402 to RT9025,because there is internal PU resistor in G966 which make leakage from 5VPCU to 3VPCU Page 31 Mount PQ29 for 1.8VSUS signal quality Page 32 VLDT_RUN no power issue Page 32 Add PC188 PC193 for CPU_CORE quality
C	3A	C2A	Mar/05/09'	Page 25 Add SATA Re-dricer circuit to fixed RX singal Page 26 Add Q423 and Q424 to meet some short-cut key power on function . Page 29 Chage PU404 form G1331T11U to G1391T12U for fitting SPEC Page 29 Add PC87 and PC88 for EMI interference Page 29 Add C2425 C2427 C2100 C2130 for EMI request
D	4A	D3A	Apr/04/09'	Page 06 R430,R424,R419,R407 change to default short pad Save one set HDT test points Page 12 R16,R20,R23 change to default short pad Page 13 L5,L7, L411 change to default short pad Add L2013 for NB VCC1.2V plane Page 14 R459,R445,R484,R486,R38 change to default short pad Page 16 R49,R528 change to default short pad Page 17 R434,R435 change to default short pad Page 20 R144,R143,R1017 change to default short pad Page 21 R591,R602 change to default short pad Page 23 ACN401,ACN402 change footprint for SMT solder hole issue Page 22 R605,R615 change to default short pad Page 23 ACN401 ACN402 change footprint to fit SMT request Page 24 R89,R138,R573,R582 change to default short pad Page 25 R643,R646 change to default short pad Page 26 LP3 change footprint to meet SMT parts lost issue Add Pad H30,H31 to increas pad size for SMT more easy to check if choke is cold solder or not Page 27 LP4,LP5,LP6,LP7,LP401,LP1013 change footprint to meet SMT parts lost issue Page 28 R575 change to default short pad Page 29 Add D418 D419 prevent DC-in inverse Page 30 PR48,PR56,PR66,PR77 change to default short pad Add Pad H24,H25,H26,H27 to increas pad size of PL1,PL3 for SMT more easy to check if choke is cold solder or not Page 31 PR63,PR64,PR68 change to default short pad Page 32 PR4,PR5,PR7~PR12,PR18,PR19 change to default short pad Page 34 All CRT compoenets do not staff Page 35 Add 2 screw hole : H22,H23 for ME request

Quanta Computer Inc.
PROJECT : GT1

Size	Document Number	Rev
	History	A

Date: Thursday, April 09, 2009 Sheet 36 of 36