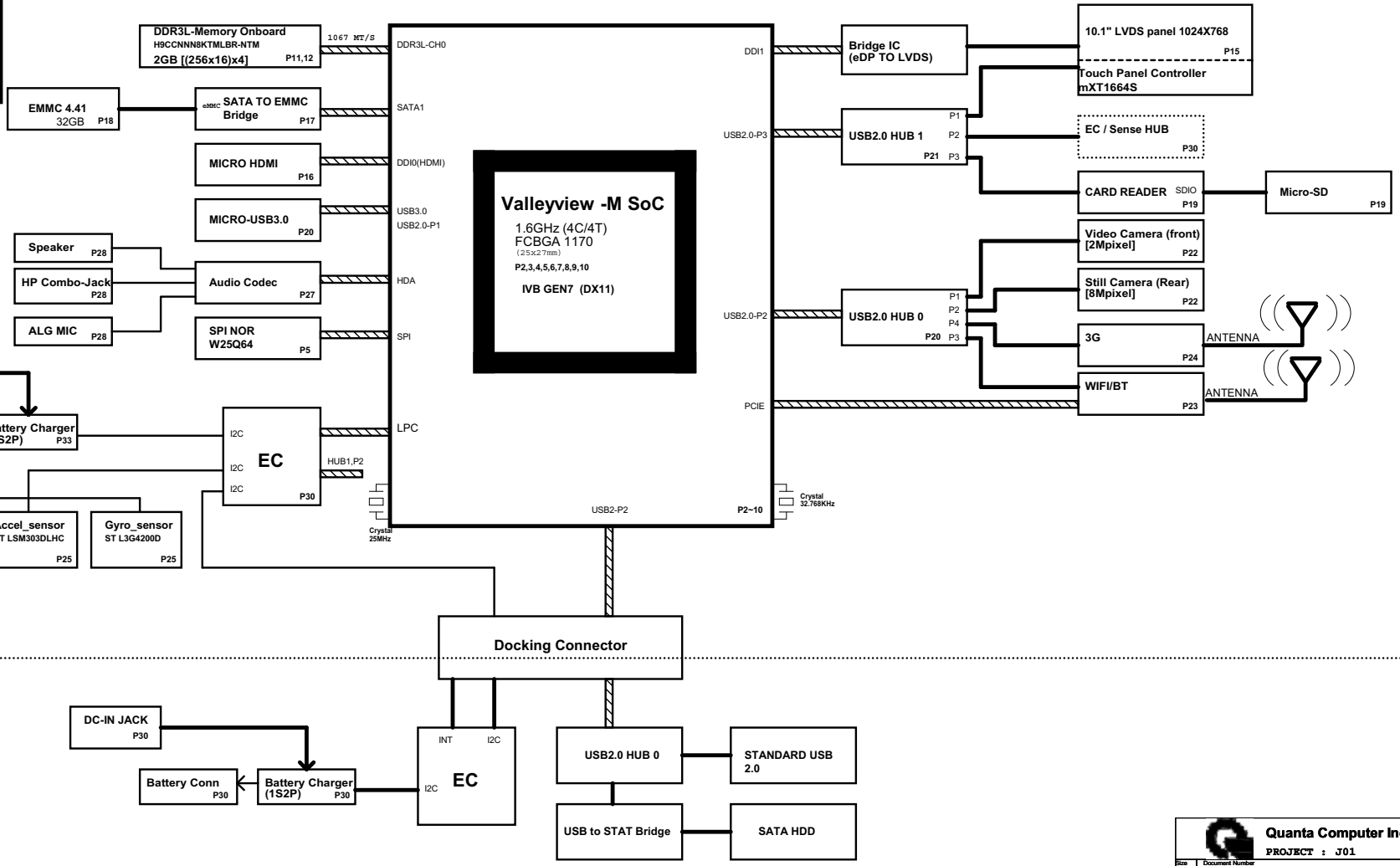
Block Diagram (Intel Bay Trail-M Platform)

01

VER : 1A

BOM P/N	Description



Schematic Marks

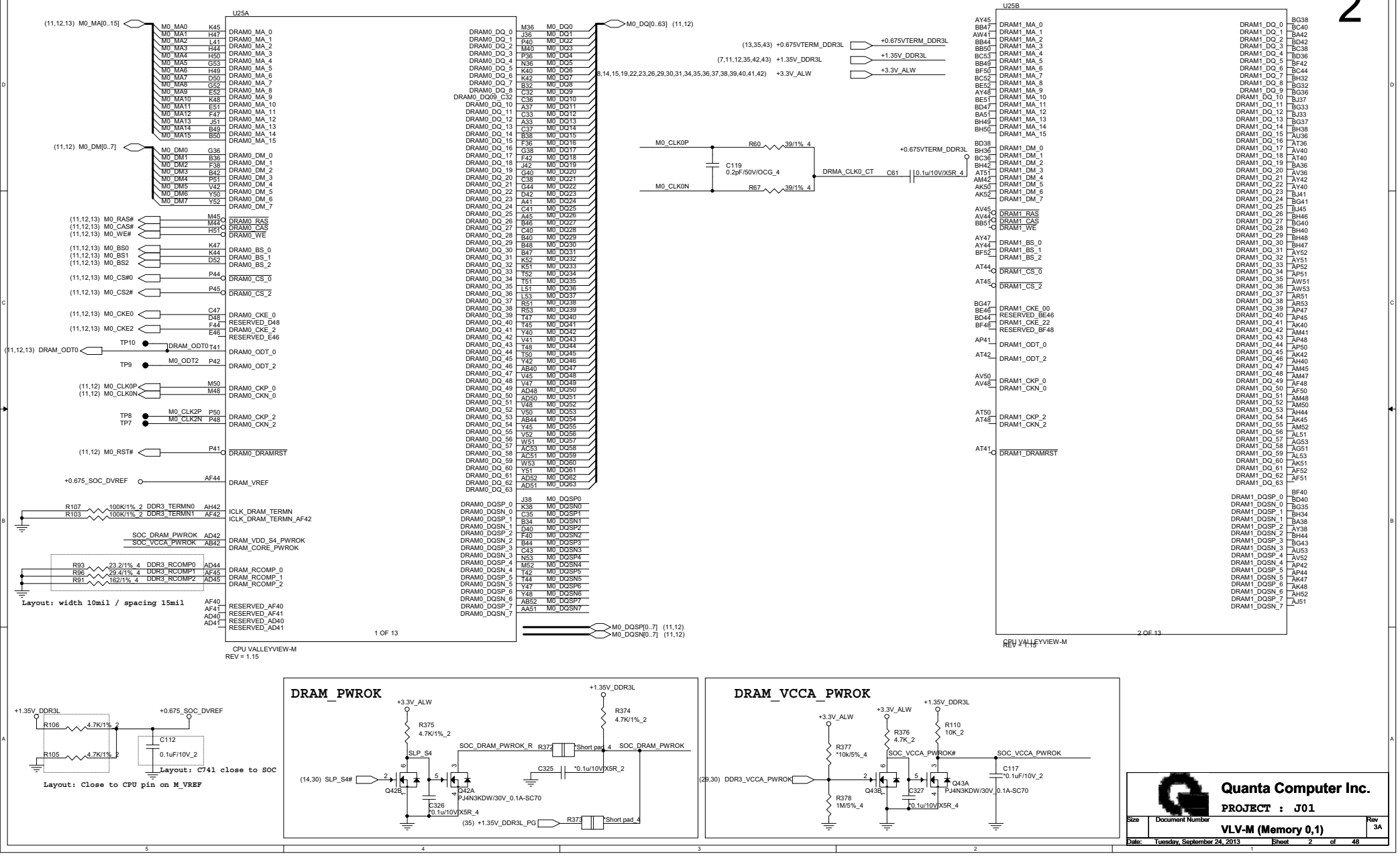
Reference	Description
*	do not stuff
/F	1% esistance

Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	BLOCK DIAGRAM	3A

Date: Tuesday, September 24, 2013 Sheet 1 of 48

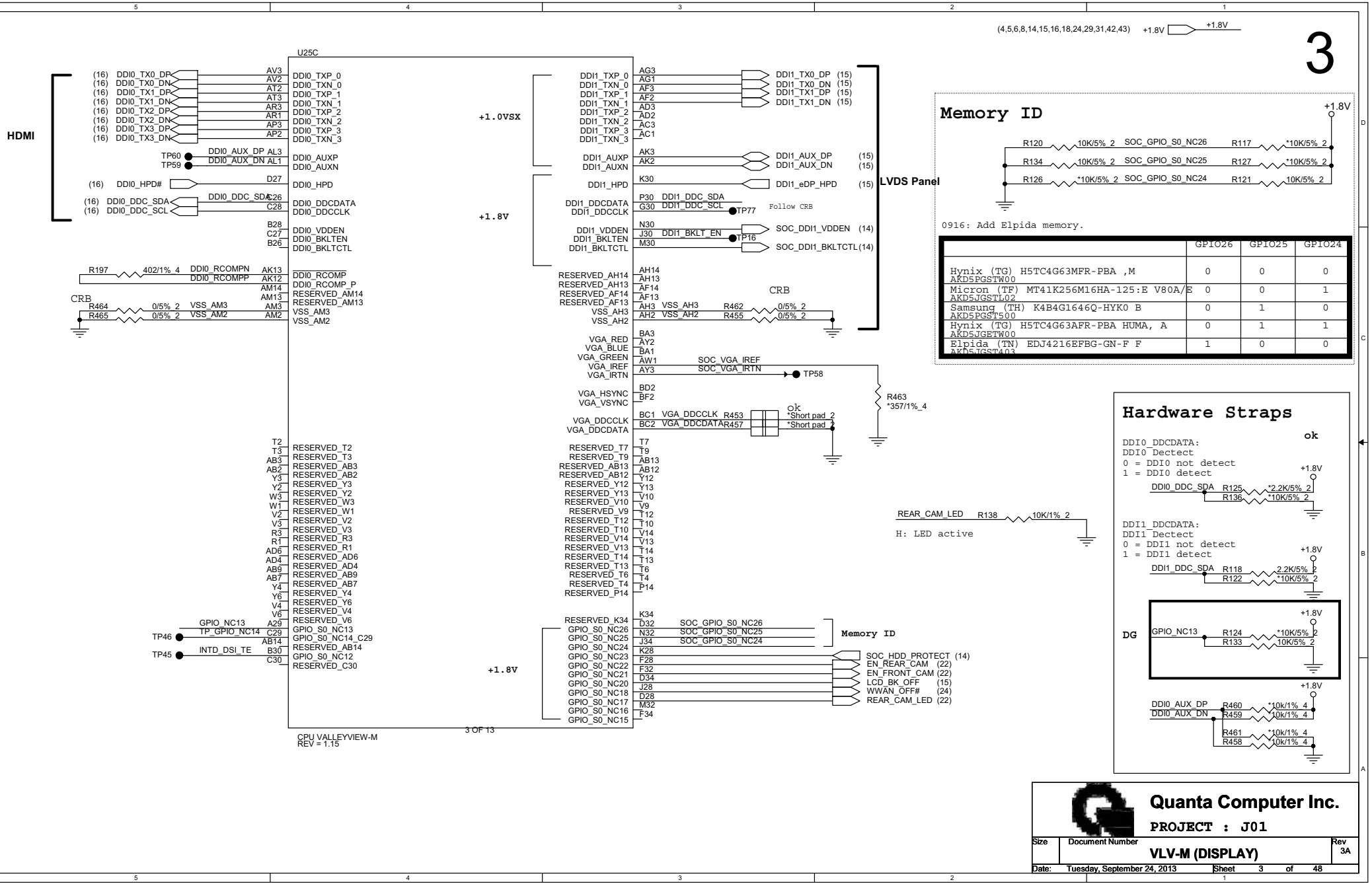


Quanta Computer Inc.

PROJECT : J01

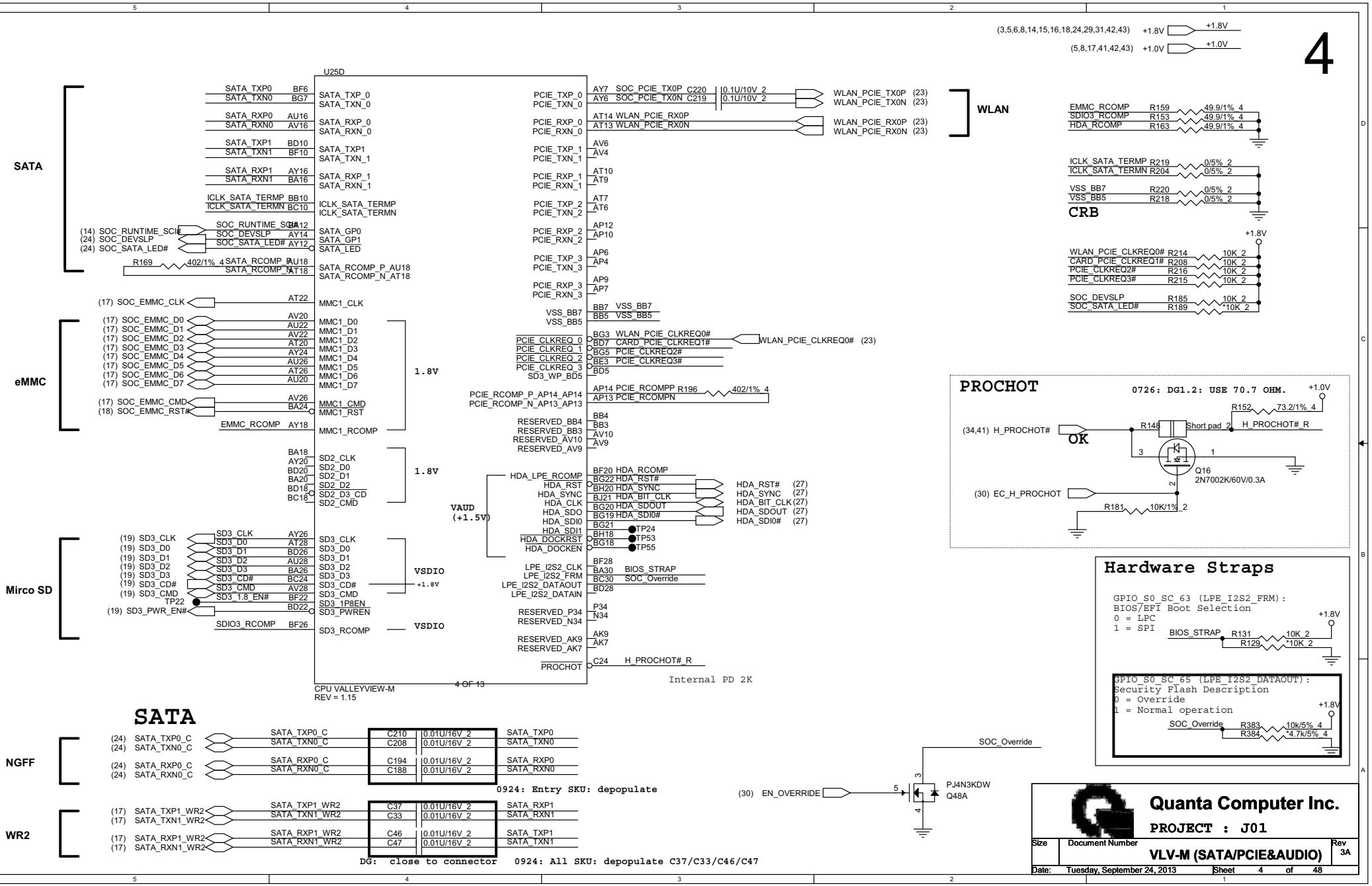
Size	Document Number	Rev
	VLV-M (Memory 0,1)	3A

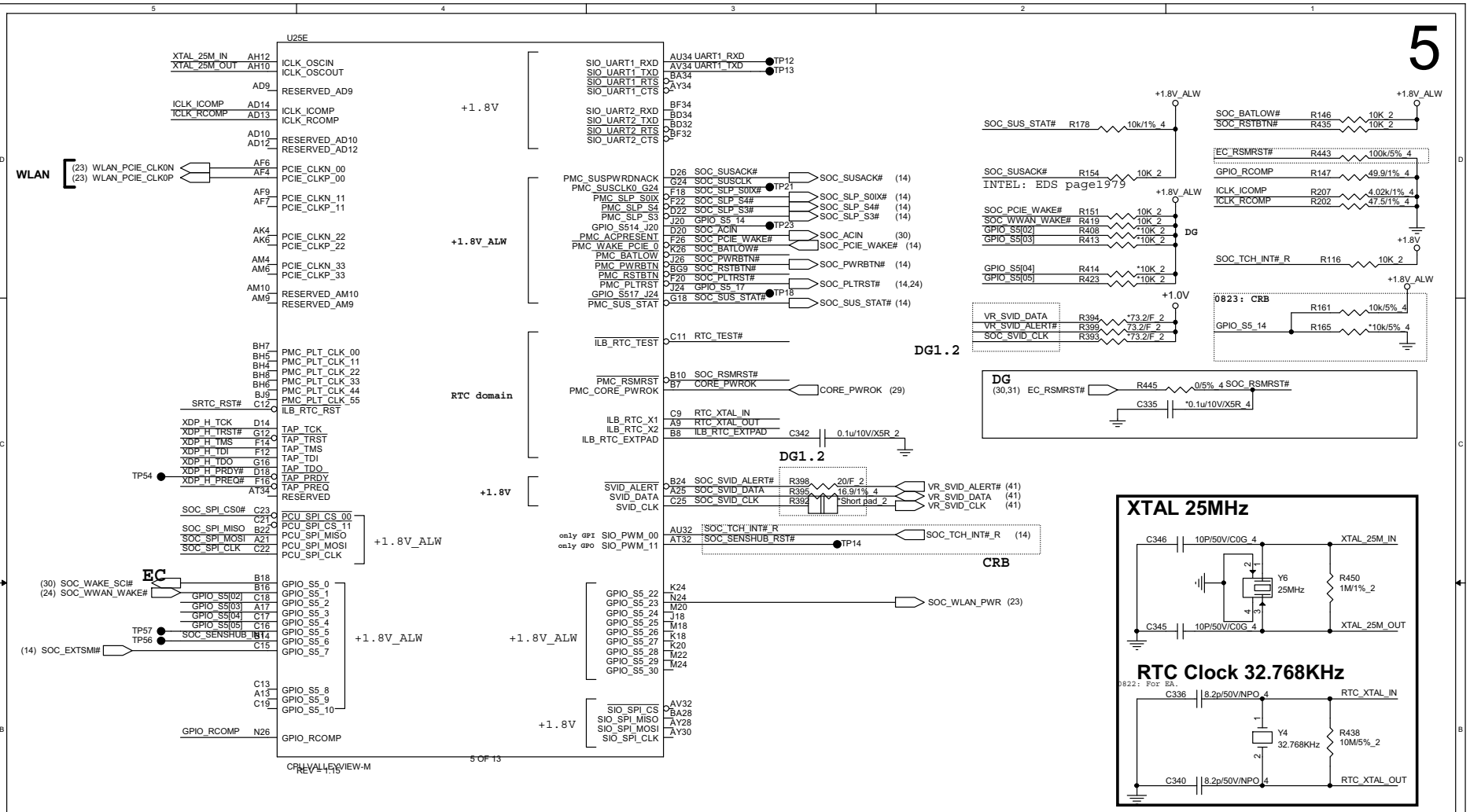
Date: Tuesday, September 24, 2013 Sheet 2 of 48

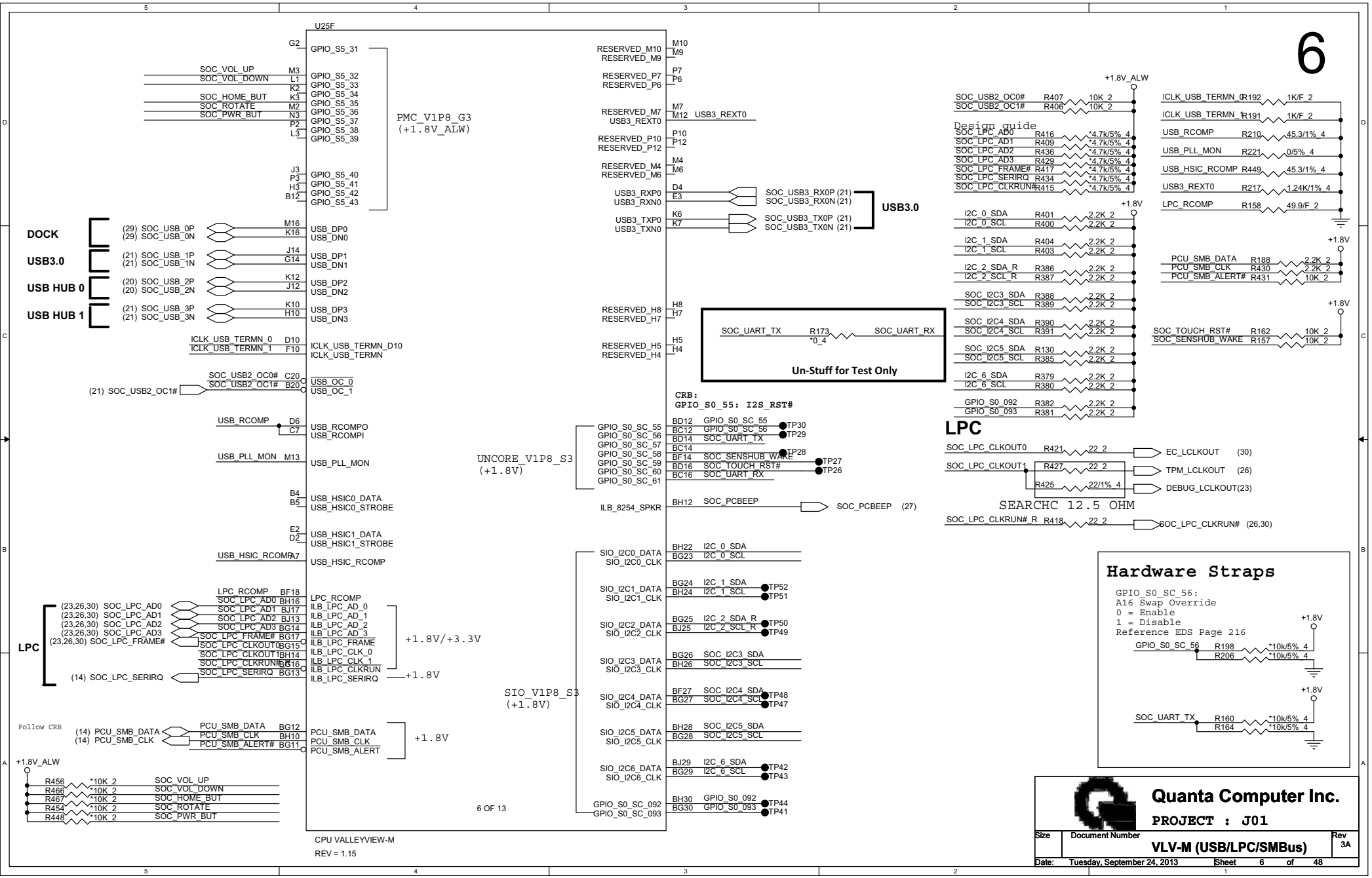


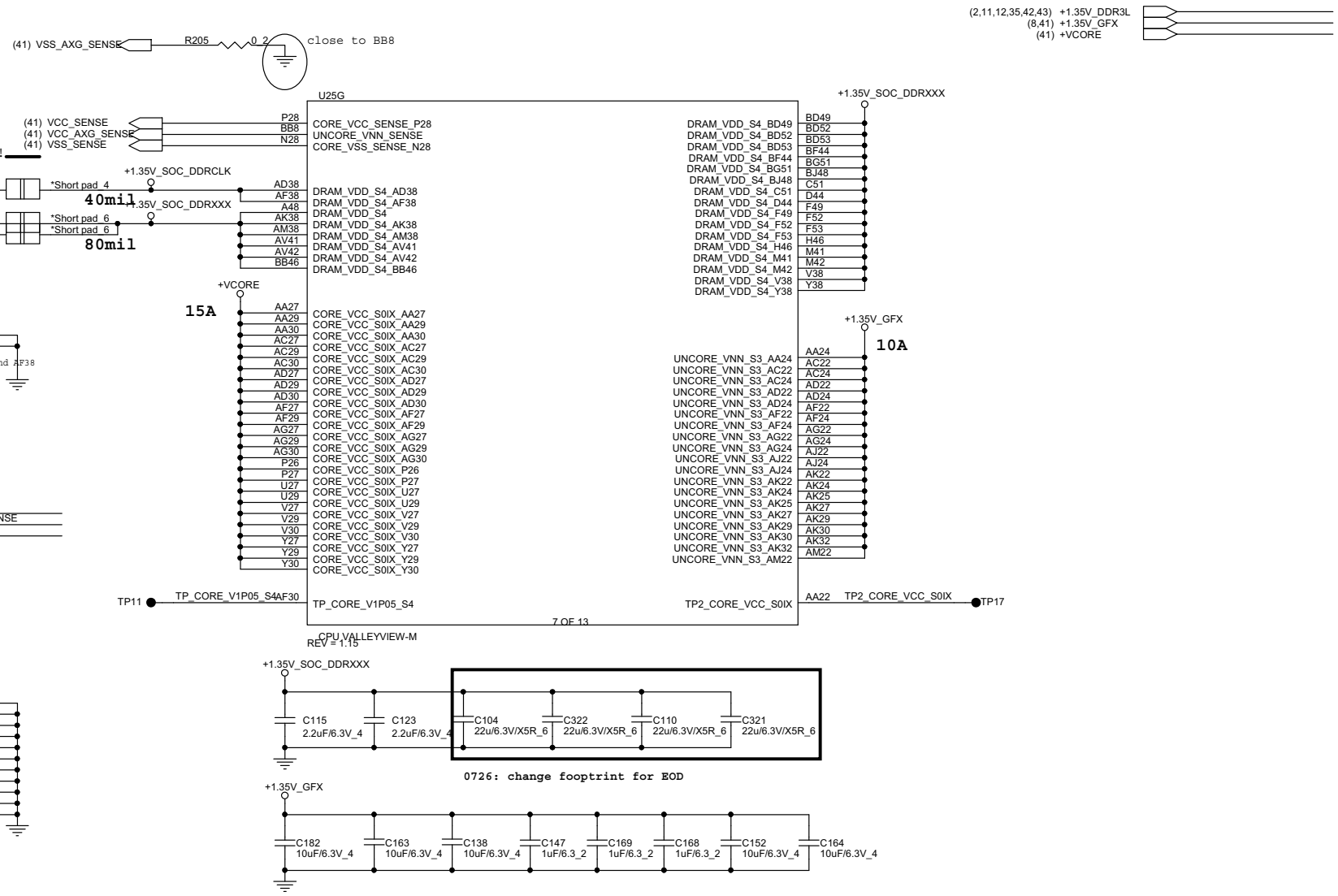
0916: Add Elpida memory.

	GPIO26	GPIO25	GPIO24
Hynix (TG) H5TC4G63MFR-PBA ,M AKD5PGSTW00	0	0	0
Micron (TF) MT41K256M16HA-125:E V80A/E AKD5JGSTL02	0	0	1
Samsung (TH) K4B4G1646Q-HYK0 B AKD5PGSP500	0	1	0
Hynix (TG) H5TC4G63AFR-PBA HUMA, A AKD5JGETW00	0	1	1
Elpida (TN) EDJ4216EFBG-GN-F F AKD5JGST403	1	0	0


4
U25D
SATA
eMMC
Mirco SD
WLAN
CRB
PROCHOT
Hardware Straps
CPU VALLEYVIEW-M
REV = 1.15
4 OF 13
Internal PD 2K
1.8V
VSDIO
VAUD
(+1.5V)
0726: DG1.2: USE 70.7 OHM.
OK
Q16
2N7002K/60V/0.3A
BIOS_STRAP
SOC_Override
GPIO_S0_SC_63 (LPE_I2S2_FRM):
BIOS/EFI Boot Selection
0 = LPC
1 = SPI
GPIO_S0_SC_65 (LPE_I2S2_DATAOUT):
Security Flash Description
0 = Override
1 = Normal operation
SATA
NGFF
WR2
0924: Entry SKU: depopulate
DG: close to connector
0924: All SKU: depopulate C37/C33/C46/C47
PJ4N3KDW
Q48A
Quanta Computer Inc.
PROJECT : J01
Size
Document Number
VLV-M (SATA/PCIE&AUDIO)
Rev
3A
Date: Tuesday, September 24, 2013
Sheet 4 of 48


5
U25E
XTAL_25M_IN AH12 ICLK_OSCIN
XTAL_25M_OUT AH10 ICLK_OSCOUT
AD9 RESERVED_AD9
ICLK_ICOMP AD14 ICLK_ICOMP
ICLK_RCOMP AD13 ICLK_RCOMP
AD10 RESERVED_AD10
AD12 RESERVED_AD12
WLAN
(23) WLAN_PCIE_CLK0N AF6 PCIE_CLKN_00
(23) WLAN_PCIE_CLK0P AF4 PCIE_CLKP_00
AF9 PCIE_CLKN_11
AF7 PCIE_CLKP_11
AK4 PCIE_CLKN_22
AK6 PCIE_CLKP_22
AM4 PCIE_CLKN_33
AM6 PCIE_CLKP_33
AM10 RESERVED_AM10
AM9 RESERVED_AM9
+1.8V
+1.8V_ALW
BH7 PMC_PLT_CLK_00
BH5 PMC_PLT_CLK_11
BH4 PMC_PLT_CLK_22
BH6 PMC_PLT_CLK_33
BJ9 PMC_PLT_CLK_44
SRTC_RST# C12 PMC_PLT_CLK_55
ILB_RTC_RST
XDP_H_TCK D14 TAP_TCK
XDP_H_TRST# G12 TAP_TRST
XDP_H_TMS F14 TAP_TMS
XDP_H_TDI F12 TAP_TDI
XDP_H_TDO G16 TAP_TDO
TP54 XDP_H_PRDY# D18 TAP_PRDY
XDP_H_PREQ# F16 TAP_PREQ
AT34 RESERVED
RTC domain
SOC_SPI_CS0# C23 PCU_SPI_CS_00
C21 PCU_SPI_CS_11
SOC_SPI_MISO B22 PCU_SPI_MISO
SOC_SPI_MOSI A21 PCU_SPI_MOSI
SOC_SPI_CLK C22 PCU_SPI_CLK
+1.8V_ALW
EC
(30) SOC_WAKE_SCI# B18 GPIO_S5_0
(24) SOC_WWAN_WAKE# B16 GPIO_S5_1
GPIO_S5[02] C18 GPIO_S5_2
GPIO_S5[03] A17 GPIO_S5_3
GPIO_S5[04] C17 GPIO_S5_4
TP57 GPIO_S5[05] C16 GPIO_S5_5
TP56 SOC_SENSHUB_IN B14 GPIO_S5_6
(14) SOC_EXTSMI# C15 GPIO_S5_7
+1.8V_ALW
C13 GPIO_S5_8
A13 GPIO_S5_9
C19 GPIO_S5_10
GPIO_RCOMP N26 GPIO_RCOMP
SIO_UART1_RXD AU34 UART1_RXD TP12
SIO_UART1_TXD AV34 UART1_TXD TP13
SIO_UART1_RTS BA34
SIO_UART1_CTS AY34
SIO_UART2_RXD BF34
SIO_UART2_TXD BD34
SIO_UART2_RTS BD32
SIO_UART2_CTS BF32
PMC_SUSPWRDNACK D26 SOC_SUSACK# SOC_SUSACK# (14)
PMC_SUSCLK0_G24 G24 SOC_SUSCLK
PMC_SLP_S0IX F18 SOC_SLP_S0IX# TP21 SOC_SLP_S0IX# (14)
PMC_SLP_S4 F22 SOC_SLP_S4# SOC_SLP_S4# (14)
PMC_SLP_S3 D22 SOC_SLP_S3# SOC_SLP_S3# (14)
GPIO_S514_J20 J20 GPIO_S5_14 TP23
PMC_ACPRESENT D20 SOC_ACIN SOC_ACIN (30)
PMC_WAKE_PCIE_0 F26 SOC_PCIE_WAKE# SOC_PCIE_WAKE# (14)
PMC_BATLOW K26 SOC_BATLOW#
PMC_PWRBTN J26 SOC_PWRBTN# SOC_PWRBTN# (14)
PMC_RSTBTN BG9 SOC_RSTBTN#
PMC_PLTRST F20 SOC_PLTRST# SOC_PLTRST# (14,24)
GPIO_S517_J24 J24 GPIO_S5_17 TP18
PMC_SUS_STAT G18 SOC_SUS_STAT# SOC_SUS_STAT# (14)
ILB_RTC_TEST C11 RTC_TEST#
DG1.2
PMC_RSMRST B10 SOC_RSMRST#
PMC_CORE_PWROK B7 CORE_PWROK CORE_PWROK (29)
ILB_RTC_X1 C9 RTC_XTAL_IN
ILB_RTC_X2 A9 RTC_XTAL_OUT
ILB_RTC_EXTPAD B8 ILB_RTC_EXTPAD C342 0.1u/10V/X5R_2
DG1.2
SVID_ALERT B24 SOC_SVID_ALERT# R398 20/F_2 VR_SVID_ALERT# (41)
SVID_DATA A25 SOC_SVID_DATA R395 16.9/1%_4 VR_SVID_DATA (41)
SVID_CLK C25 SOC_SVID_CLK R392 Short pad_2 VR_SVID_CLK (41)
+1.8V
only GPI SIO_PWM_00 AU32 SOC_TCH_INT#_R SOC_TCH_INT#_R (14)
only GPO SIO_PWM_11 AT32 SOC_SENSHUB_RST# TP14
CRB
GPIO_S5_22 K24
GPIO_S5_23 N24 SOC_WLAN_PWR (23)
GPIO_S5_24 M20
GPIO_S5_25 J18
GPIO_S5_26 M18
GPIO_S5_27 K18
GPIO_S5_28 K20
GPIO_S5_29 M22
GPIO_S5_30 M24
+1.8V_ALW
SIO_SPI_CS AV32
SIO_SPI_MISO BA28
SIO_SPI_MOSI AY28
SIO_SPI_CLK AY30
+1.8V
CPU-VALLEYVIEW-M
REV 1.15
5 OF 13
+1.8V_ALW
SOC_SUS_STAT# R178 10k/1%_4
SOC_SUSACK# R154 10K_2
INTEL: EDS page1979
SOC_PCIE_WAKE# R151 10K_2
SOC_WWAN_WAKE# R419 10K_2
GPIO_S5[02] R408 *10K_2
GPIO_S5[03] R413 *10K_2
DG
GPIO_S5[04] R414 *10K_2
GPIO_S5[05] R423 10K_2
+1.0V
VR_SVID_DATA R394 *73.2/F_2
VR_SVID_ALERT# R399 73.2/F_2
SOC_SVID_CLK R393 *73.2/F_2
SOC_BATLOW# R146 10K_2
SOC_RSTBTN# R435 10K_2
EC_RSMRST# R443 100K/5%_4
GPIO_RCOMP R147 49.9/1%_4
ICLK_ICOMP R207 4.02k/1%_4
ICLK_RCOMP R202 47.5/1%_4
+1.8V
SOC_TCH_INT#_R R116 10K_2
0823: CRB
R161 10k/5%_4
GPIO_S5_14 R165 *10k/5%_4
DG
(30,31) EC_RSMRST# R445 0/5%_4 SOC_RSMRST#
C335 *0.1u/10V/X5R_4
XTAL 25MHz
C346 10P/50V/C0G_4 XTAL_25M_IN
Y6 25MHz
R450 1M/1%_2
C345 10P/50V/C0G_4 XTAL_25M_OUT
RTC Clock 32.768KHz
0822: For EA.
C336 8.2p/50V/NPO_4 RTC_XTAL_IN
Y4 32.768KHz
R438 10M/5%_2
C340 8.2p/50V/NPO_4 RTC_XTAL_OUT
64M-bit (+1.8V SPI ROM)
SOC_SPI_MOSI R412 22/1%_4 SPI_MOSI
SOC_SPI_CS0# R402 22/1%_4 SPI_CS0#
SOC_SPI_CLK R410 22/1%_4 SPI_CLK
LAYOUT: CLOSE TO SOC
SOC_SPI_MISO R405 22/1%_4 SPI_MISO
LAYOUT: CLOSE TO SPI ROM
U27
+1.8V_ALW
SPI_MOSI 5 SPI_SI
SPI_MISO 2 SPI_SO
SPI_CS0# 1 CS#
SPI_CLK 6 SPI_SCK
VCC 8
WP# 3 SPI_WP#
GND 4 SPI_HOLD 7 SPI_HOLD
SPI_FLASH
C339 0.1u/10V/X5R_2
C337 *1u/6.3V/X5R_4
soic8-7_9-1_27
IC FLASH (8P) W25Q64FWSSIG (SOIC)
AKE5EZN0N00
+1.8V_ALW
SPI_HOLD R441 3.3K/F_4
SPI_WP# R397 3.3K/F_4
SPI_CS0# R396 3.3K/F_4
SPI_CLK C334 *47p/50V/NPO_4
XDP
+1.8V_ALW
XDP_H_TDO R177 51/5%_4
LAYOUT: PLACE WITHIN .25' FROM XDP CONN
XDP_H_TRST# R200 51/5%_4
+1.8V_ALW
XDP_H_TMS R186 51/5%_4
XDP_H_TDI R201 51/5%_4
XDP_H_TCK R424 51/5%_4
LAYOUT: PLACE WITHIN 1.1' FROM SOC CONN
+1.8V_ALW
XDP_H_PREQ# R180 200/5%_4
LAYOUT: PLACE WITHIN 1.1' OF BUFFER PIN
RTC Circuit
20mils
+3.3VPCU
+3.3V_RTC
R289 20k/1%_4 RTC_TEST#
C271 1uF/6.3_2
+V_COIN_BAT
OLB?
D9 BAT54CW
R298 1k/1%_4
R290 20k/1%_4 SRTC_RST#
C273 1u/6.3V/X5R_4
C272 1uF/6.3_2
RTC Power trace width 20mils.
RTC well reset
CN18
BAT_CONN
DFHD02MR045
Quanta Computer Inc.
PROJECT : J01
Size Document Number Rev
VLV-M (CLK/PMU/SPI/RTC) 3A
Date: Tuesday, September 24, 2013 Sheet 5 of 48


6
U25F
PMC_V1P8_G3 (+1.8V_ALW)
UNCORE_V1P8_S3 (+1.8V)
SIO_V1P8_S3 (+1.8V)
+1.8V/+3.3V
+1.8V
USB3.0
DOCK
USB HUB 0
USB HUB 1
LPC
Un-Stuff for Test Only
CRB:
GPIO_S0_55: I2S_RST#
Design guide
SEARCHC 12.5 OHM
Hardware Straps
GPIO_S0_SC_56:
A16 Swap Override
0 = Enable
1 = Disable
Reference EDS Page 216
Follow CRB
6 OF 13
CPU VALLEYVIEW-M
REV = 1.15
Quanta Computer Inc.
PROJECT : J01
Size
Document Number
VLV-M (USB/LPC/SMBus)
Rev 3A
Date: Tuesday, September 24, 2013
Sheet 6 of 48

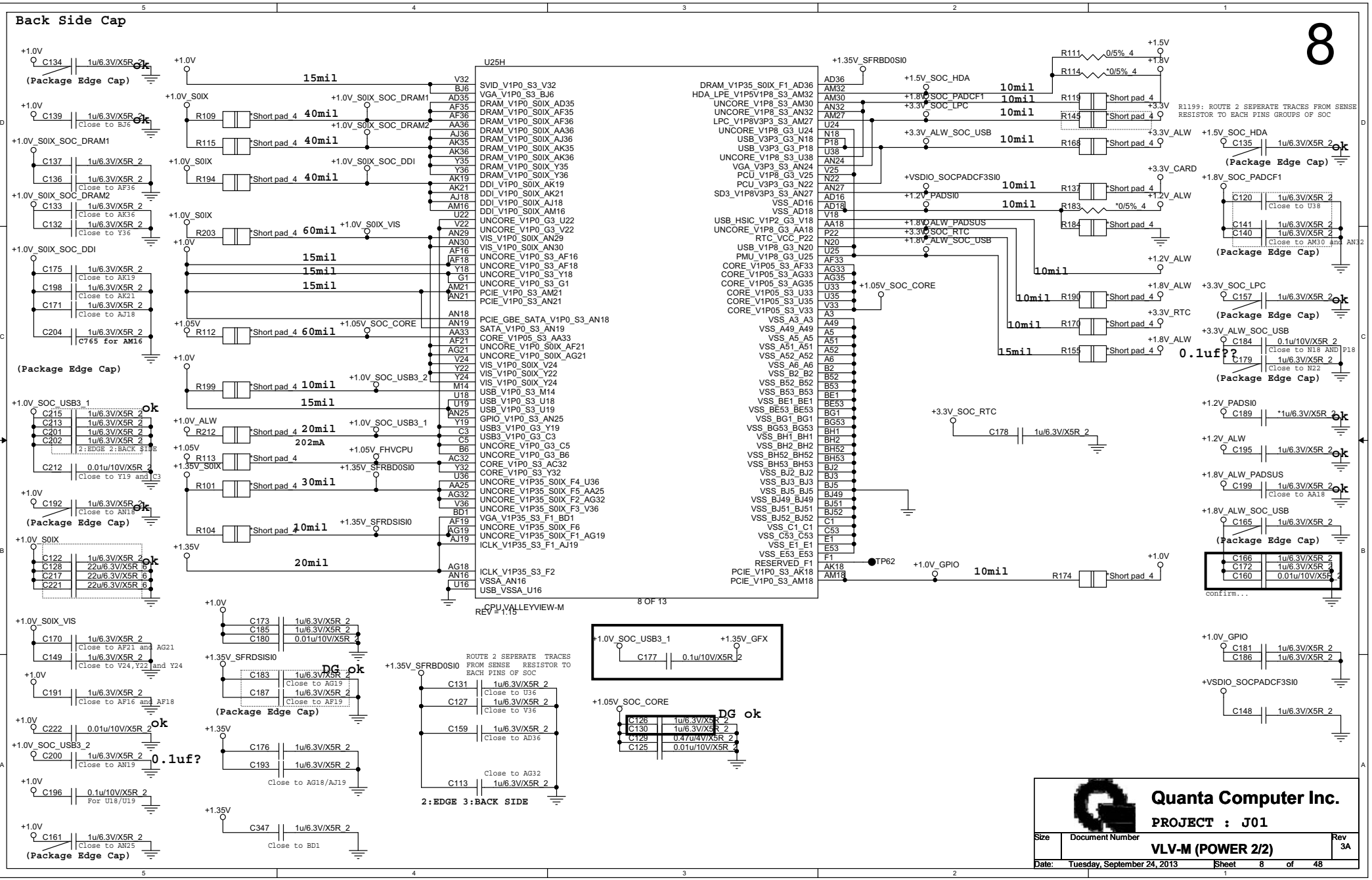


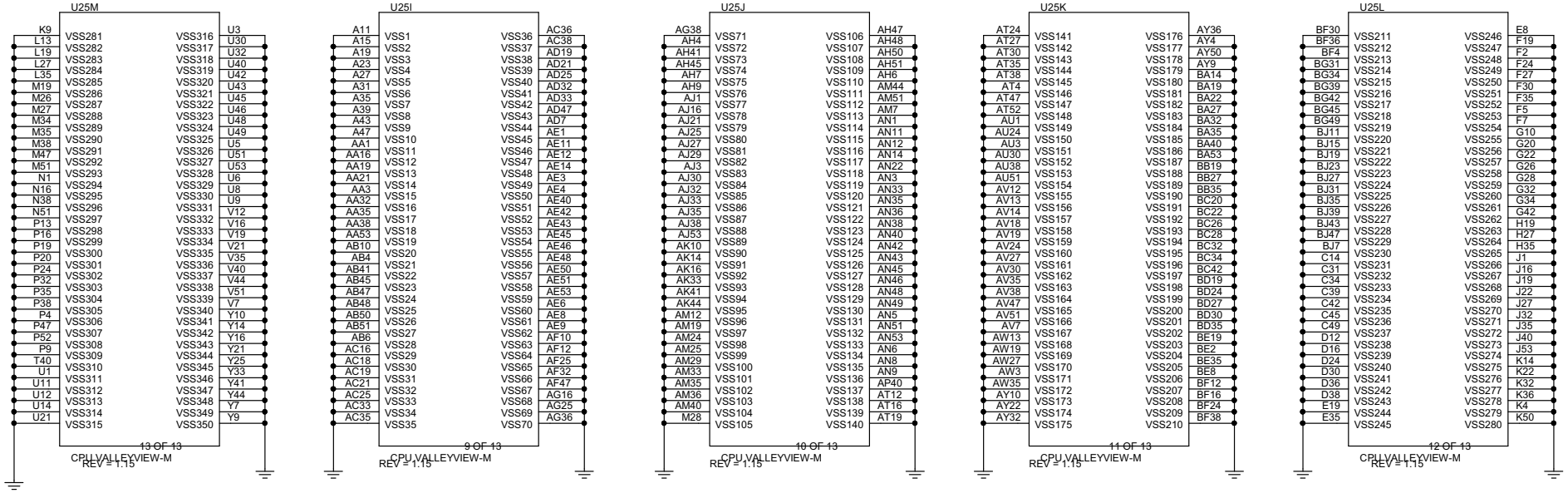
Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	VLV-M (POWER 1/2)	3A

Date: Tuesday, September 24, 2013 Sheet 7 of 48


Back Side Cap
8
U25H
CPU_VALLEYVIEW-M
REV = 1.15
8 OF 13
(Package Edge Cap)
ok
DG ok
0.1uf?
0.1uf??
2:EDGE 3:BACK SIDE
ROUTE 2 SEPERATE TRACES FROM SENSE RESISTOR TO EACH PINS OF SOC
R1199: ROUTE 2 SEPERATE TRACES FROM SENSE RESISTOR TO EACH PINS GROUPS OF SOC
Quanta Computer Inc.
PROJECT : J01
VLV-M (POWER 2/2)
Size
Document Number
Rev
3A
Date: Tuesday, September 24, 2013
Sheet 8 of 48



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	VLV-M (GND)	3A

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Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	VLV-M SOC (DEBUG)	3A

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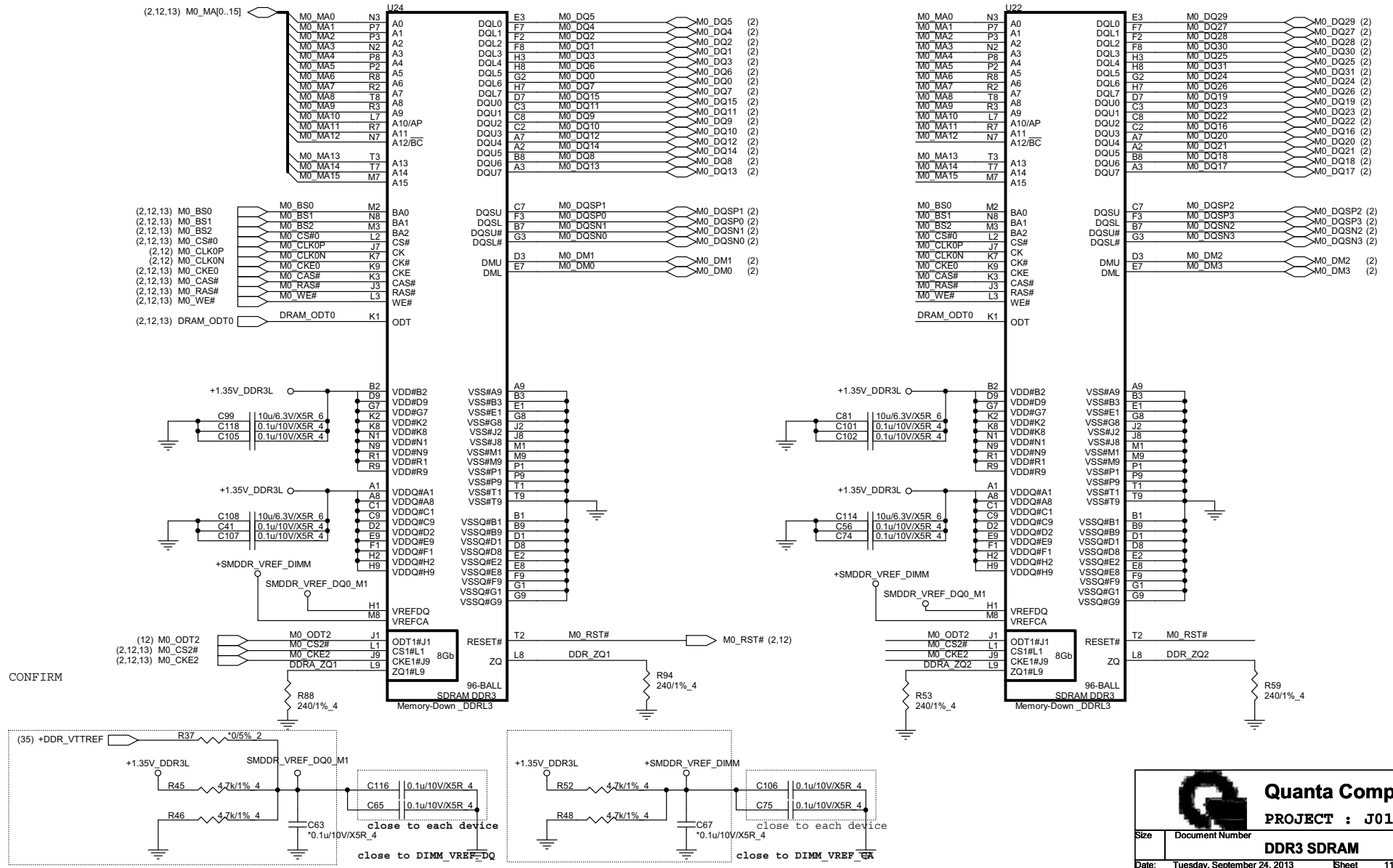
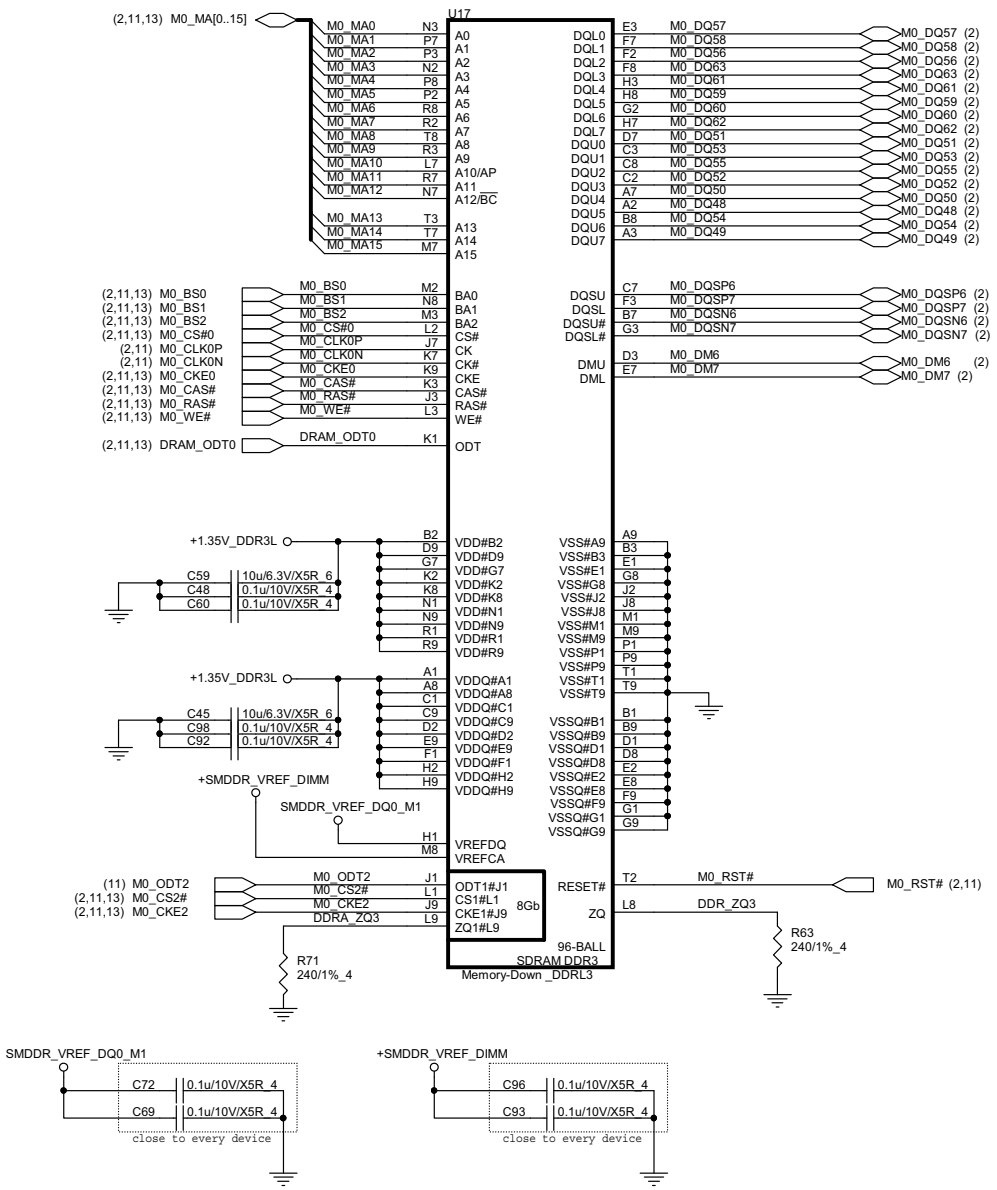


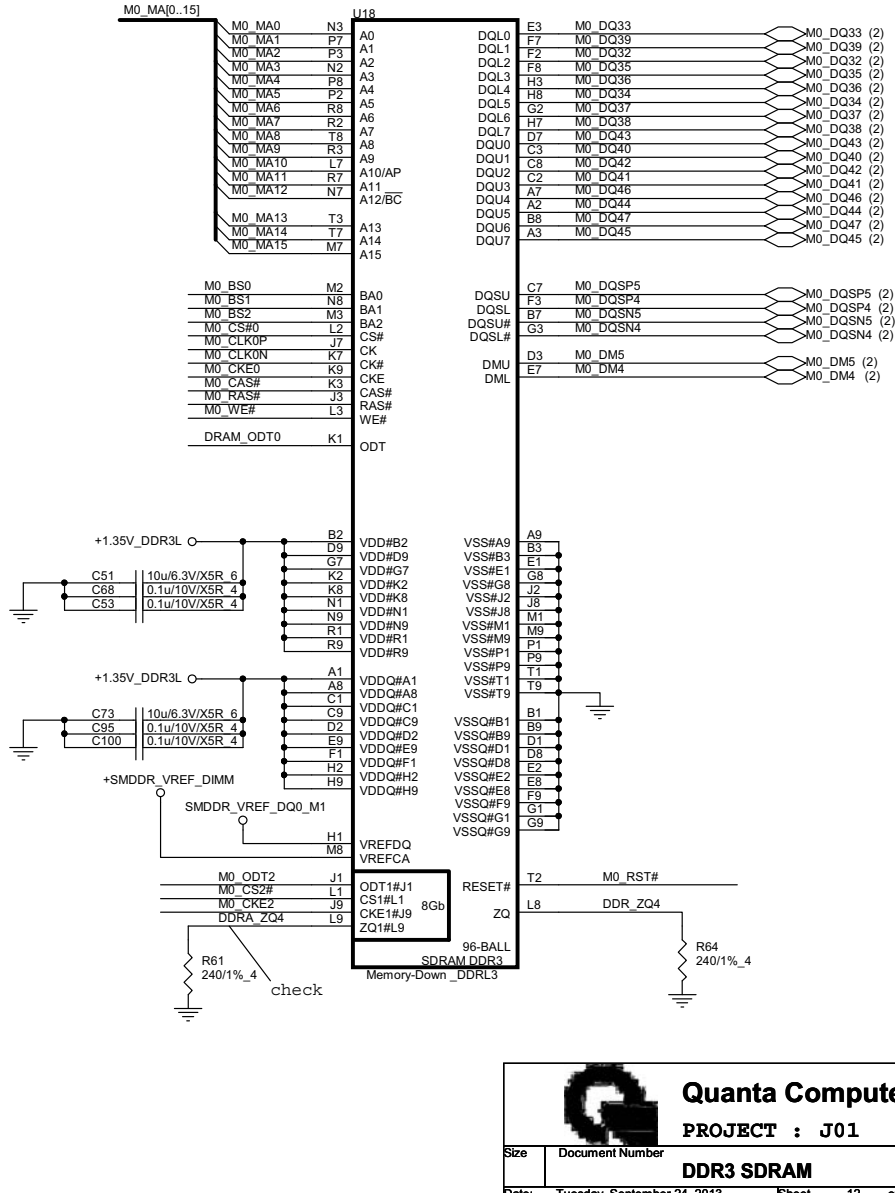
Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	DDR3 SDRAM	3A

Date: Tuesday, September 24, 2013 Sheet 11 of 48





Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	DDR3 SDRAM	3A

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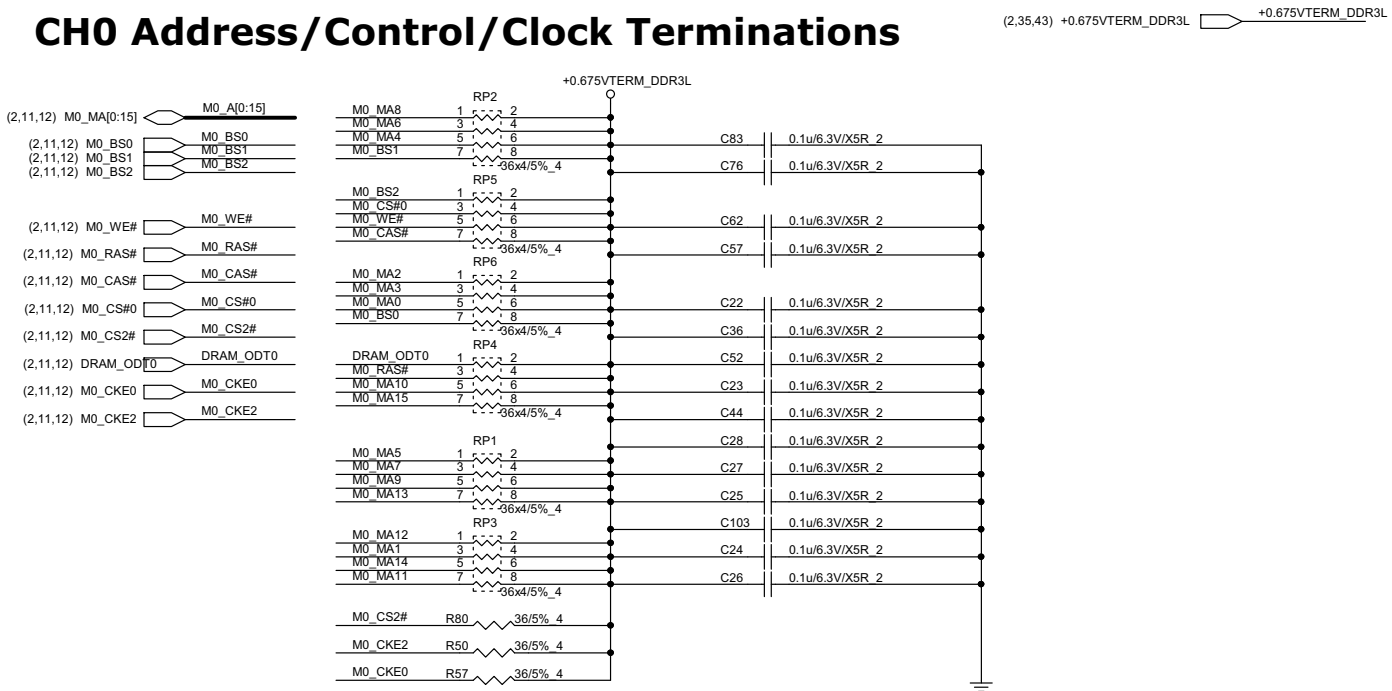
CH0 Address/Control/Clock Terminations

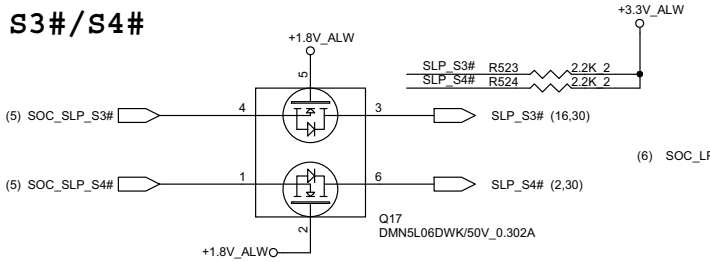


Quanta Computer Inc.		
PROJECT : J01		
Size	Document Number: DDR3 TERMINATION	Rev 3A
Date: Tuesday, September 24, 2013	Sheet 13 of 48	

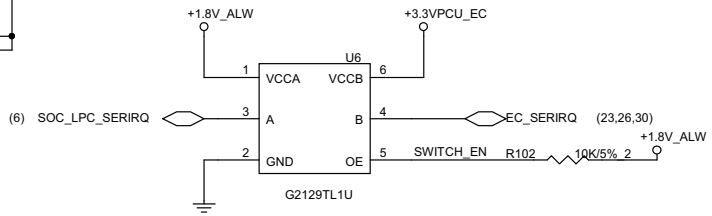
Level Shifter

14

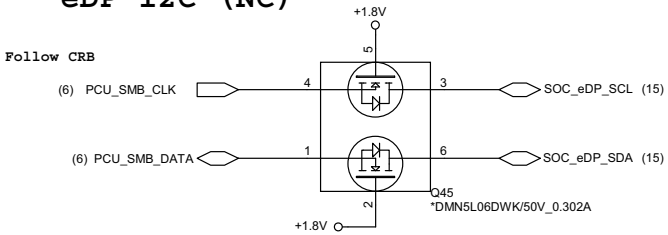
S3#/S4#



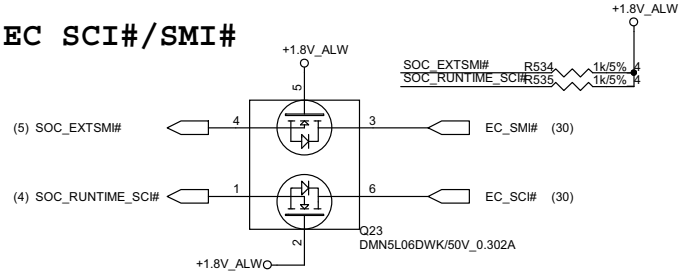
SERIRQ



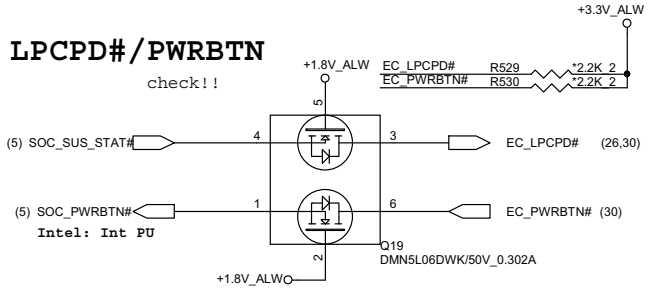
eDP I2C (NC)



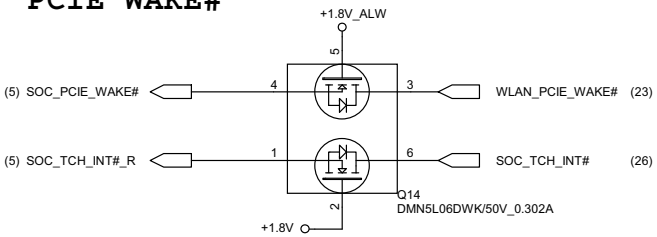
EC SCI#/SMI#



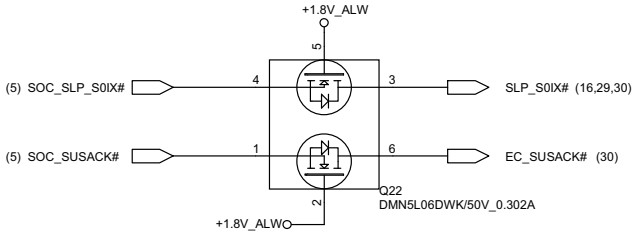
LPCPD#/PWRBTN



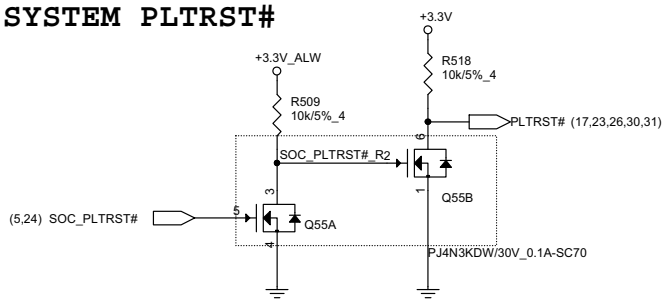
PCIE WAKE#



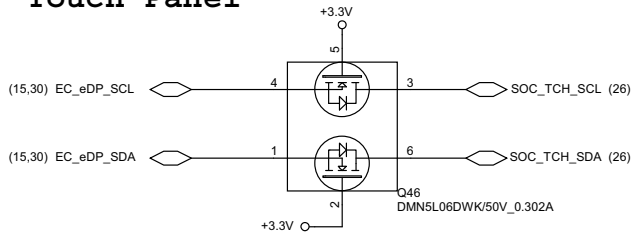
SLP_S0IX#/SOC_SUSACK#



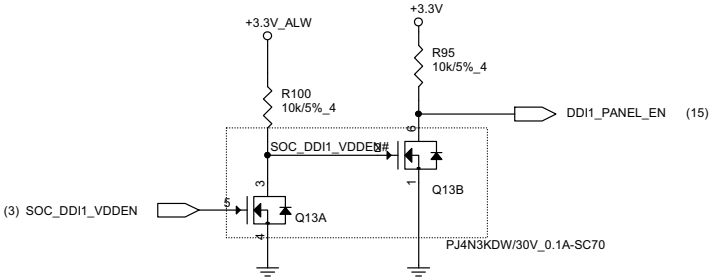
SYSTEM PLTRST#



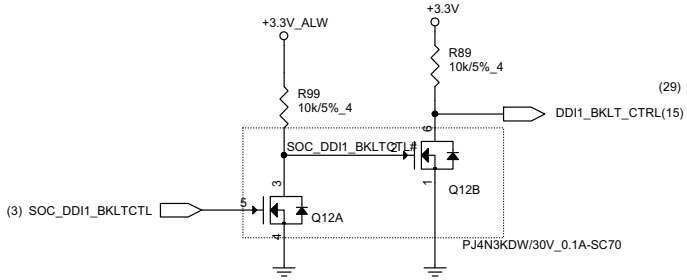
Touch Panel



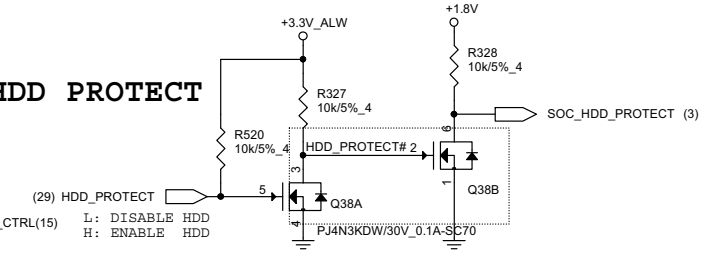
PANEL POWER ON



PANEL BKLT_CTRL



HDD PROTECT



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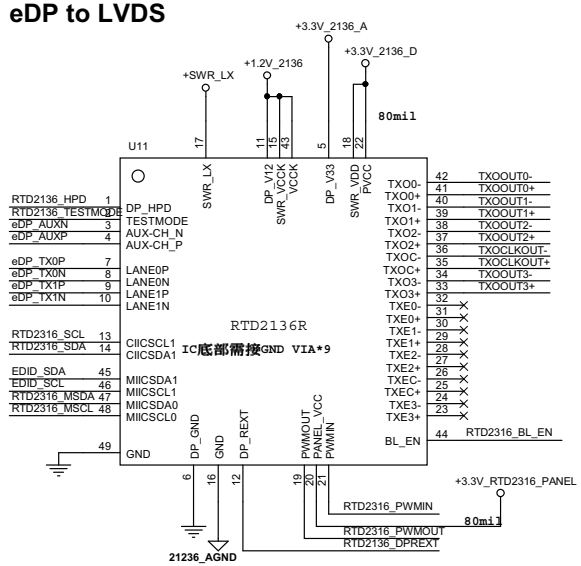
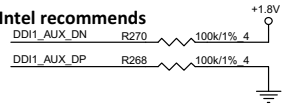
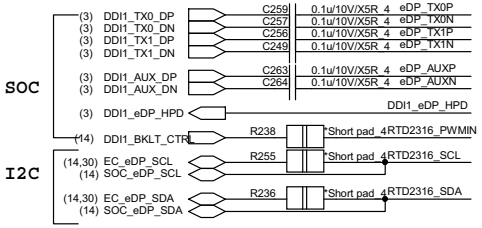
eDP to LVDS



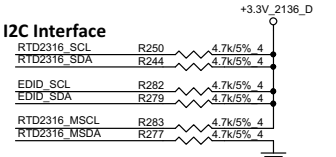
Intel recommends



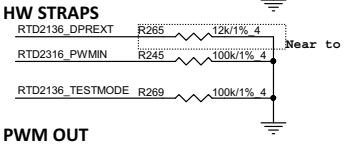
Interface



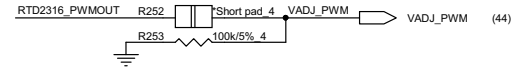
I2C Interface



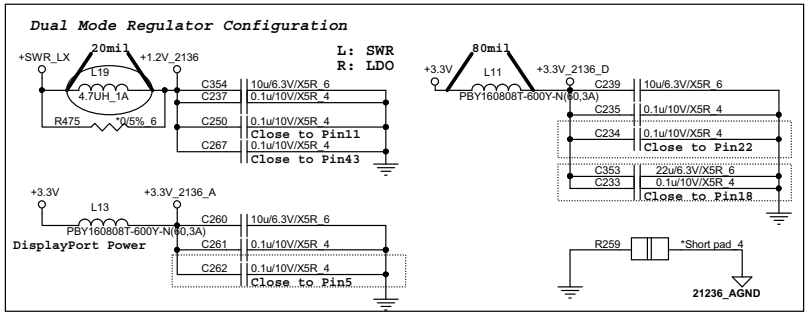
HW STRAPS

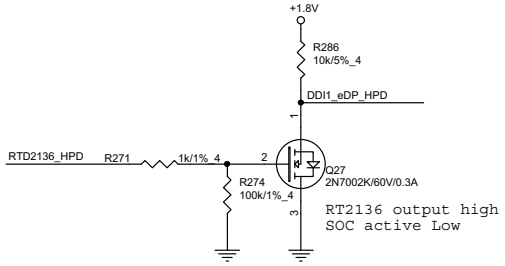


PWM OUT



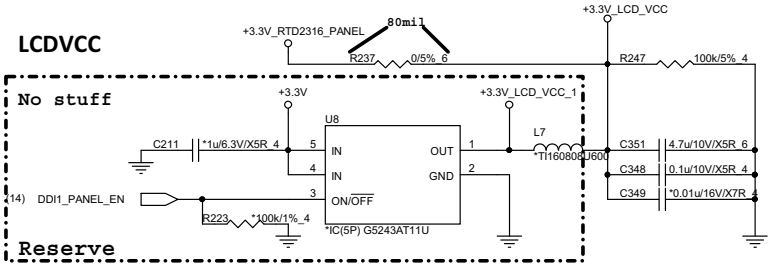
RTD2132R Power



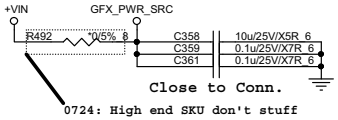


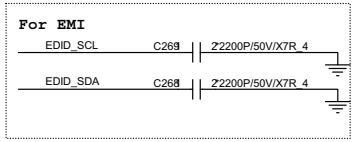
LED PANEL

LCDVCC

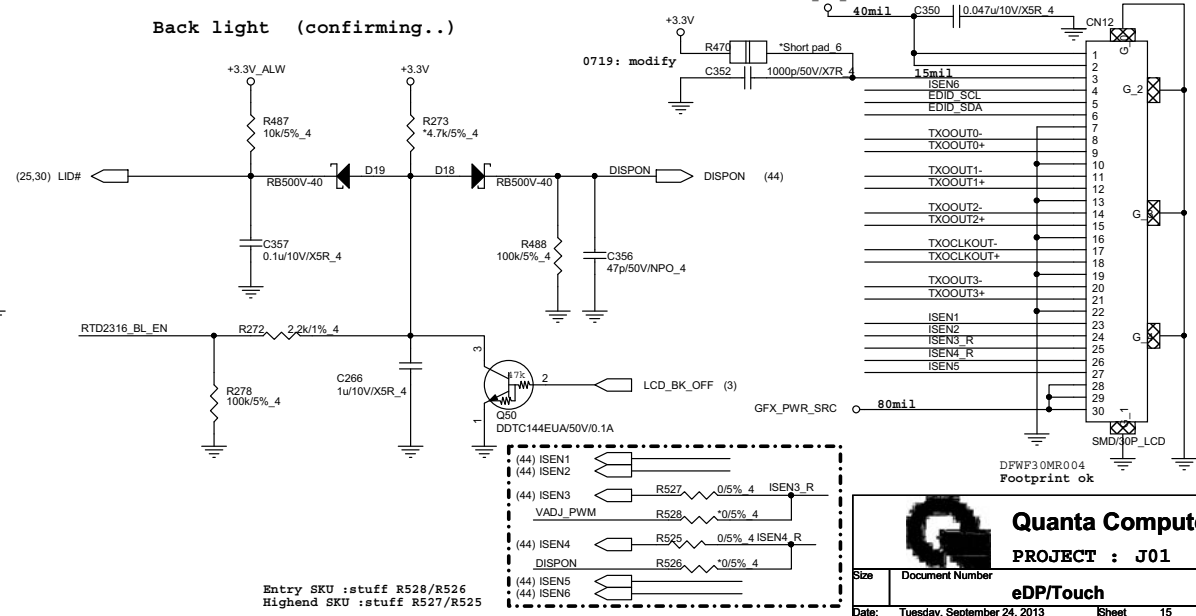


LED POWER





Back light (confirming..)



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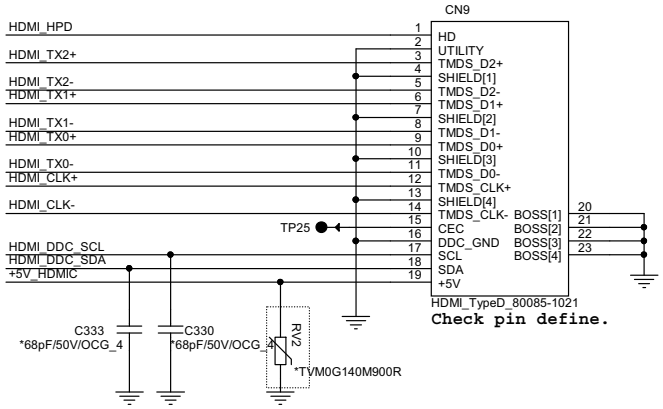
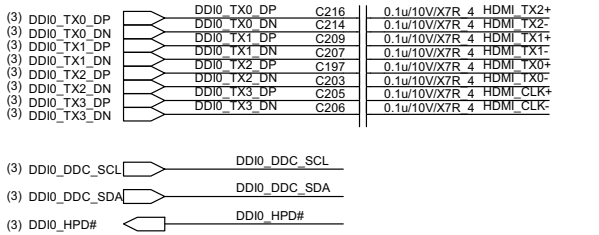
HDMI CONNECTOR (D TYPE)

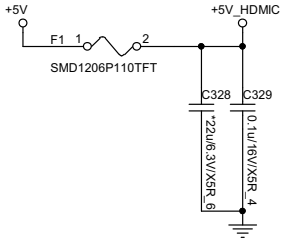


HDMI INTERFACE

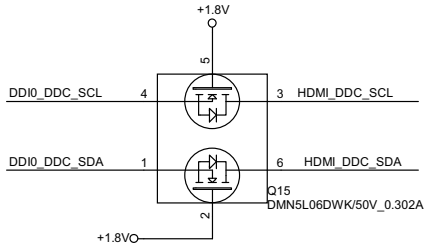
DG MAPPING OK



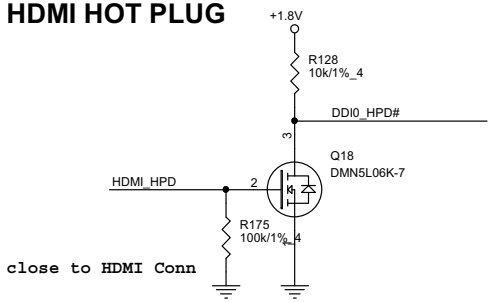
HDMI POWER SUPPLY



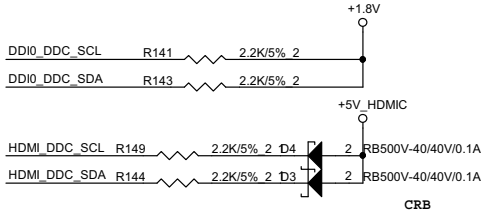
I2S BUS LEVEL SHIFT



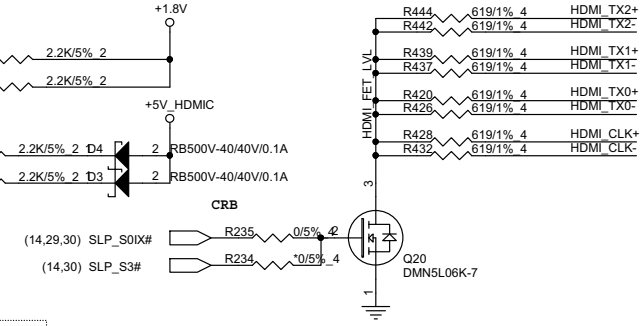
HDMI HOT PLUG



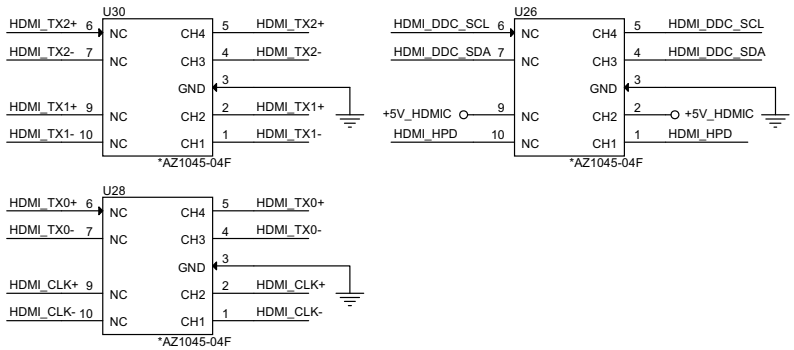
I2C Pull up



HDMI LEVEL SHIFT

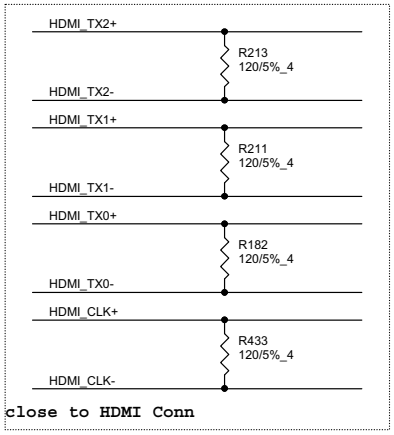


ESD reserve for HDMI



Layout note:Place close to HDMI Conn

EMI reserve for HDMI



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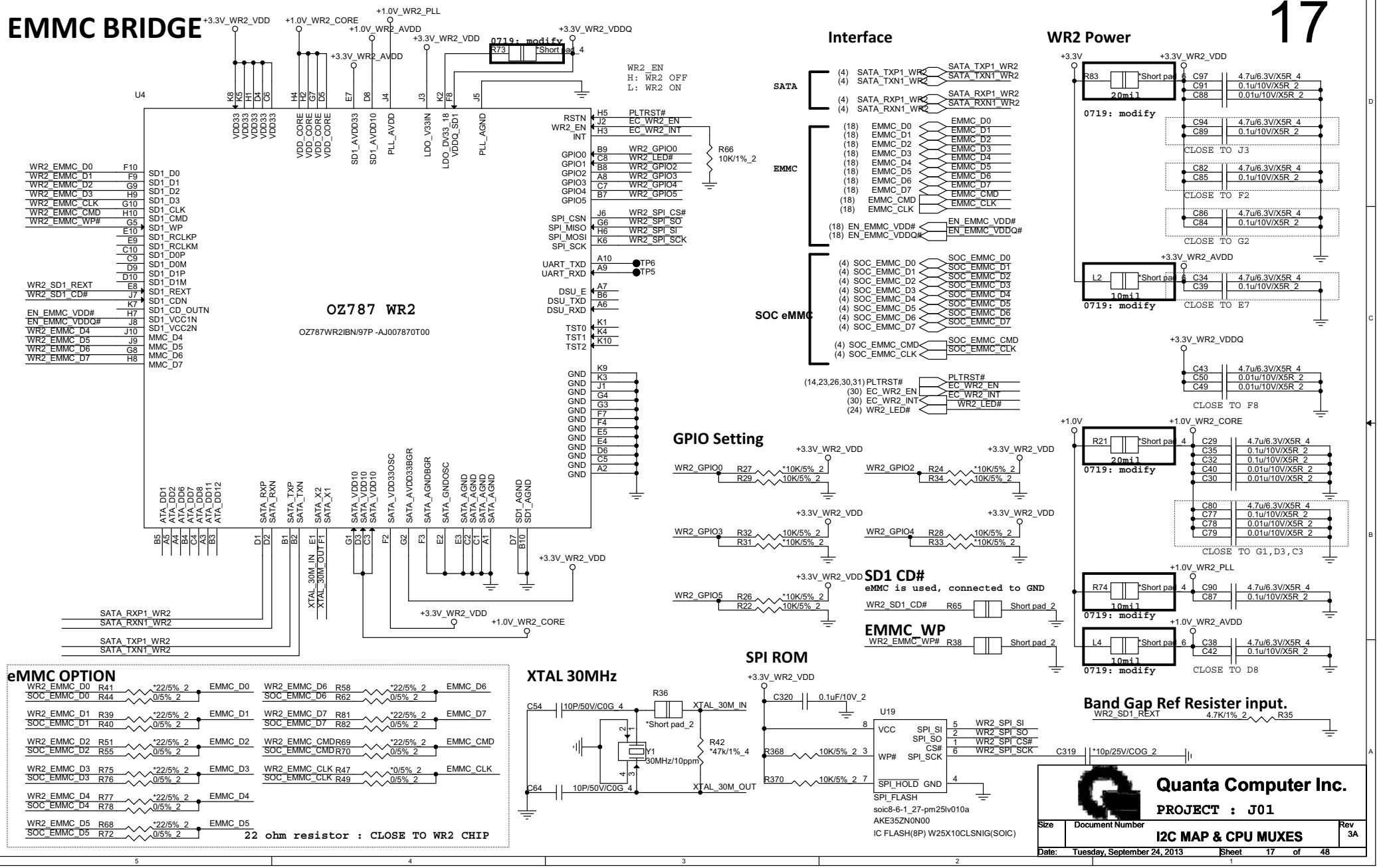
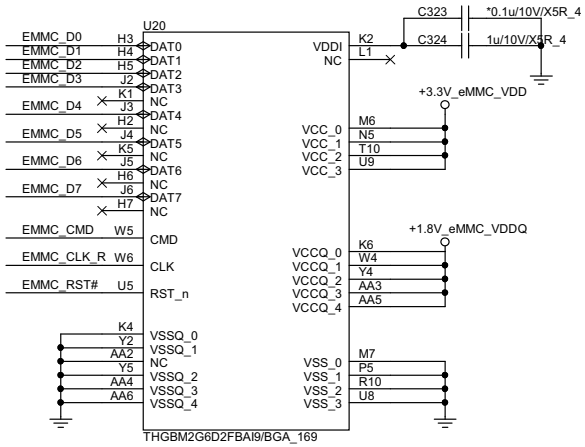
EMMC BRIDGE

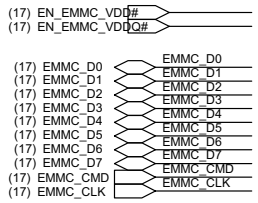
17



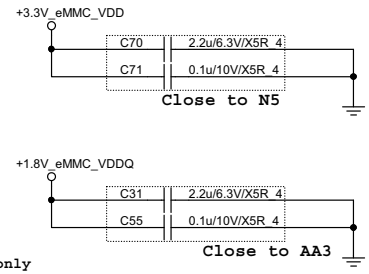
eMMC



Interface

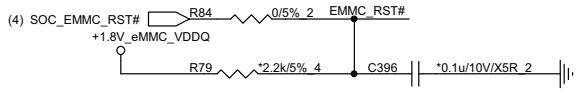


eMMC Power

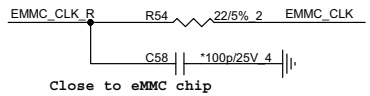


eMMC RST#

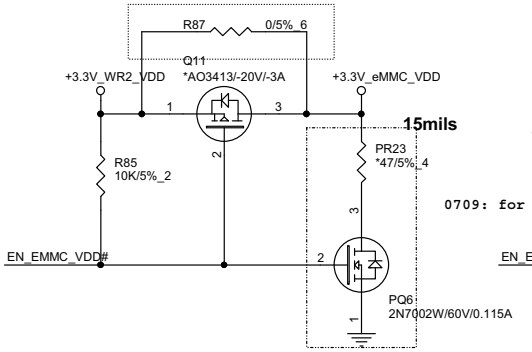
0709: for eMMC only



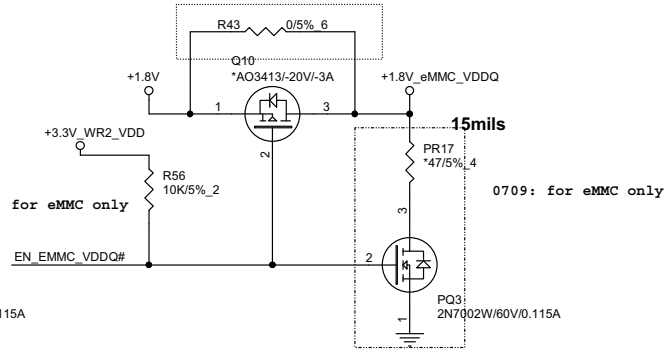
eMMC CLOCK



eMMC VDD POWER CONTROL



eMMC VDDQ POWER CONTROL



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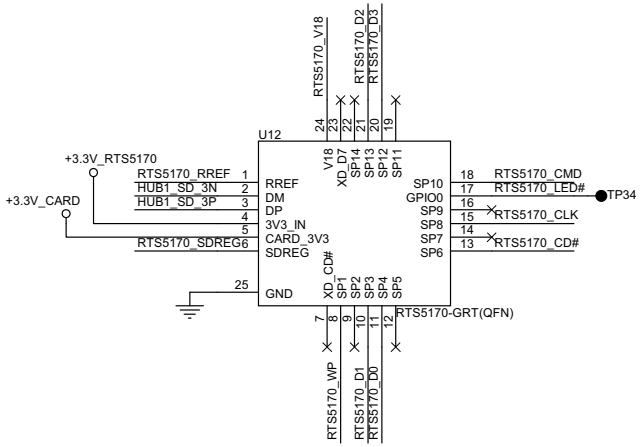
Mirco SD



CARD PCIE INTERFACE

CARD READER

(21) HUB1_SD_3N — HUB1_SD_3N
(21) HUB1_SD_3P — HUB1_SD_3P

CO-LAY with SoC

RTS5170_CD#	R319	0/5% 4	SD3_CD#_CONN
RTS5170_D0	R318	0/5% 4	SD3_D0_CONN
RTS5170_D1	R317	0/5% 4	SD3_D1_CONN
RTS5170_D3	R303	0/5% 4	SD3_D3_CONN
RTS5170_CMD	R305	0/5% 4	SD3_CMD_CONN
RTS5170_D2	R302	0/5% 4	SD3_D2_CONN
	C278	*0.1u/10V/X5R_4	
RTS5170_CLK	R310	0/5% 4	SD3_CLK_CONN
	C288	*0.1u/10V/X5R_4	

HW STRAPS

RTS5170_RREF — R301 — 6.2K/1%_4
CLOSE TO SD PIN9

RTS5170_WP — R316 — *Short pad_4

CARD POWER

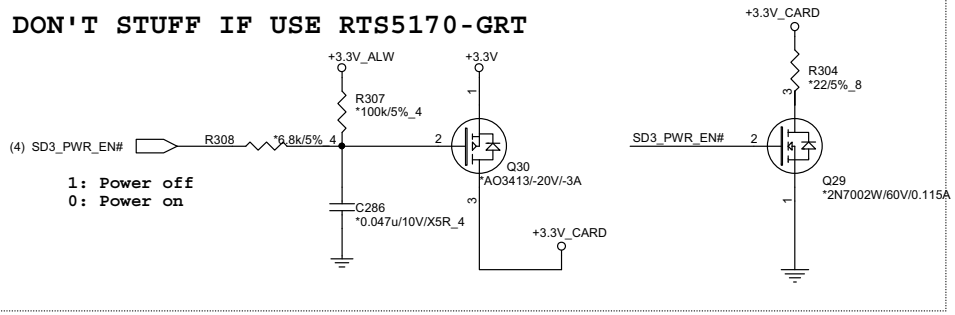
+3.3V — R309 — *Short pad_6 — +3.3V_RTS5170
400mA/ 30mil

C283 — 4.7u/6.3V/X5R_4
C282 — 0.1u/10V/X5R_4

RTS5170_V18 — C279 — 1u/10V/X5R_4

RTS5170_SDREG — C285 — 1u/10V/X5R_4

DON'T STUFF IF USE RTS5170-GRT



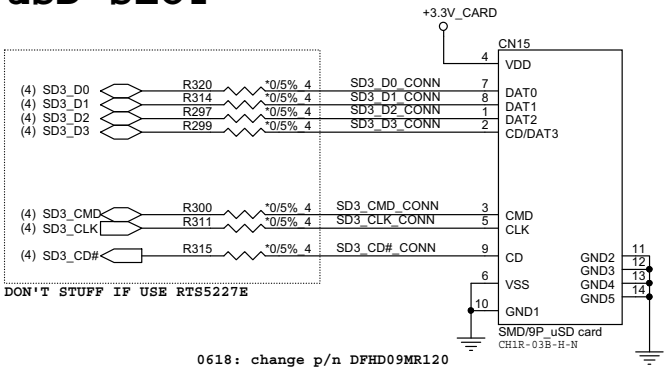
1: Power off
0: Power on

+3.3V_CARD — C280 — 0.1u/10V/X5R_4
CLOSE TO uSD SLOT

EMI

SD3_D0	EC9	*10p/50V/NPO_4
SD3_D1	EC8	*10p/50V/NPO_4
SD3_D2	EC6	*10p/50V/NPO_4
SD3_D3	EC5	*10p/50V/NPO_4
SD3_CLK_CONN	EC7	*10p/50V/NPO_4

uSD SLOT



DON'T STUFF IF USE RTS5227E

0618: change p/n DFHD09MR120

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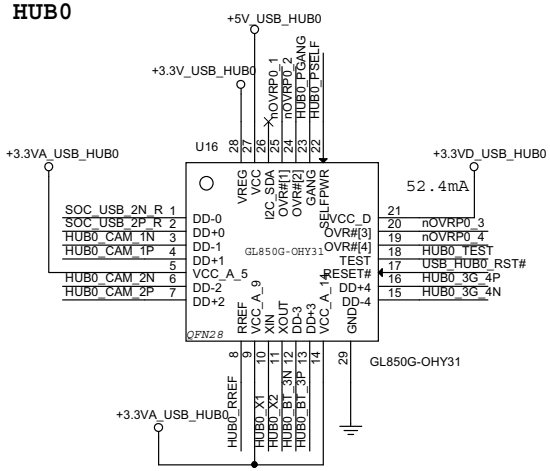
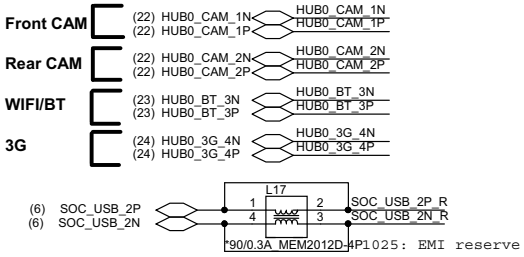
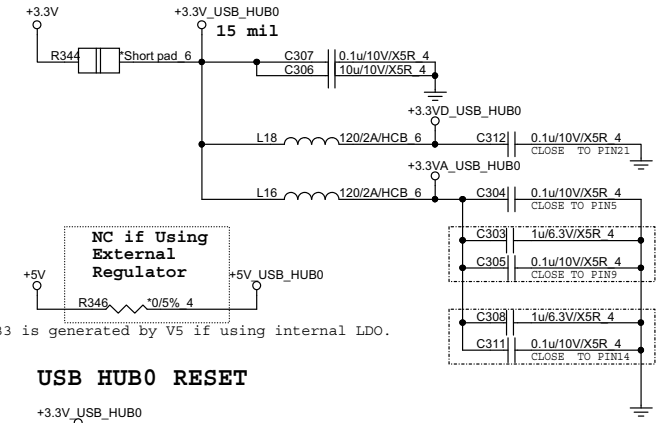
USB HUB0



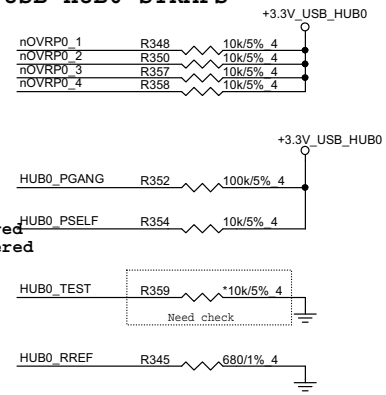
USB HUB0 Interface



USB HUB0 Power

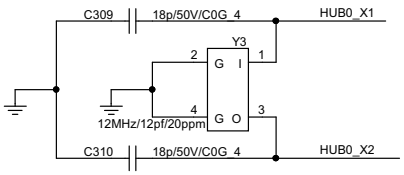


USB HUB0 STRAPS



On HUB IC, V33 is generated by V5 if using internal LDO.

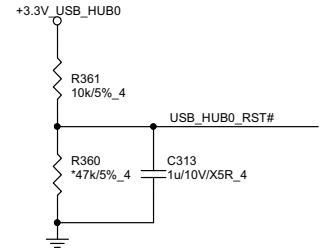
USB HUB0 XTAL



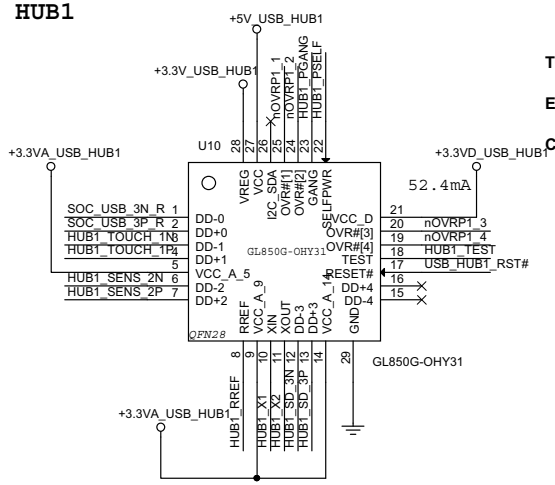
HUB_PSELF
0: GL850G is bus-powered
1: GL850G is self-powered

HUB_TEST
0: Normal Operation (Internal PD)
1: Test Mode

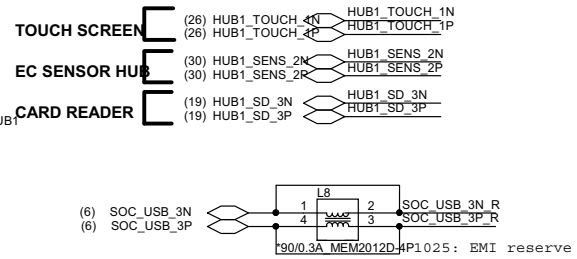
USB HUB0 RESET



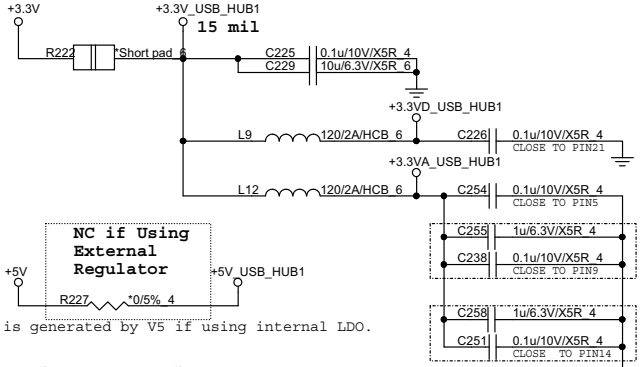
USB HUB1



USB HUB1 Interface

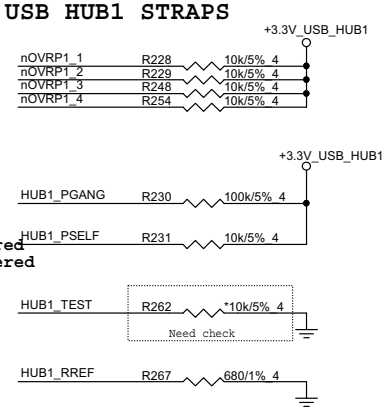


USB HUB1 Power

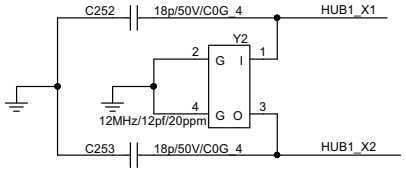


On HUB IC, V33 is generated by V5 if using internal LDO.

USB HUB1 STRAPS



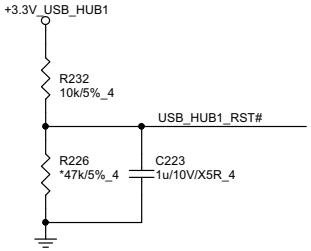
USB HUB1 XTAL



HUB_PSELF
0: GL850G is bus-powered
1: GL850G is self-powered

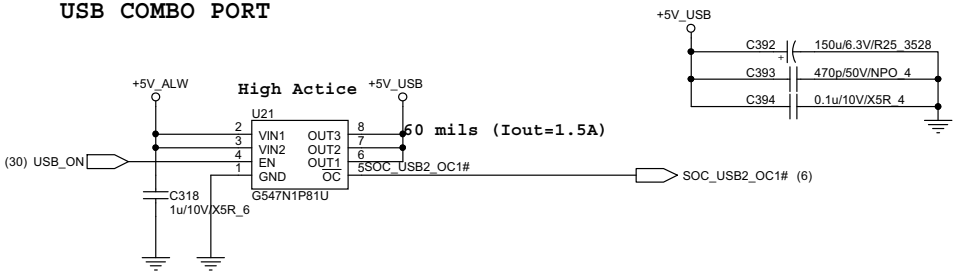
HUB_TEST
0: Normal Operation (Internal PD)
1: Test Mode

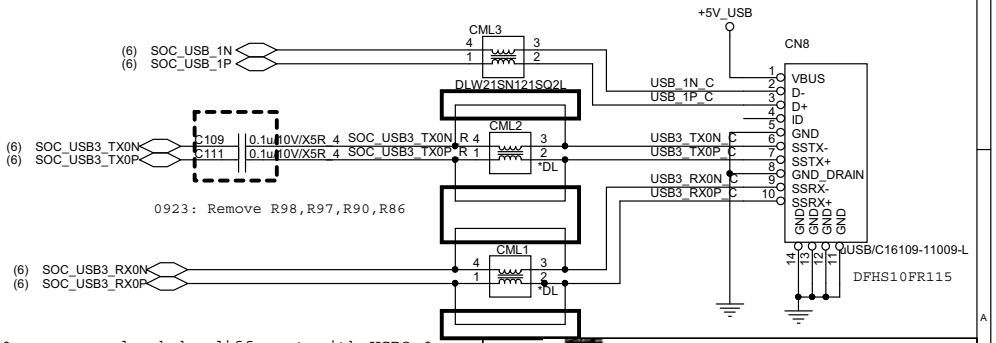
USB HUB RESET



0603: change footprint

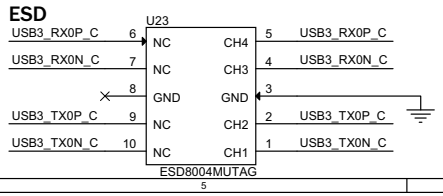
USB COMBO PORT

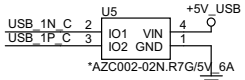




Use USB3.0 common mode choke different with USB2.0

ESD





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	USB HUB1 / COMBO 3.0	3A

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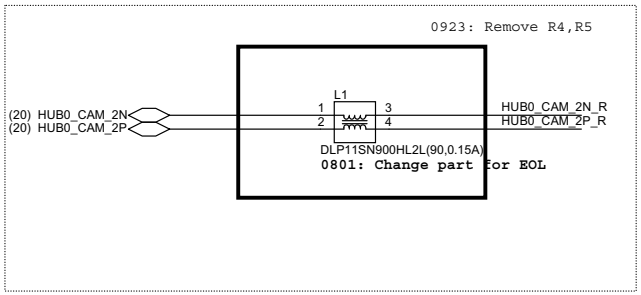
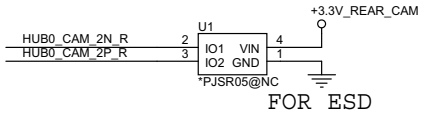
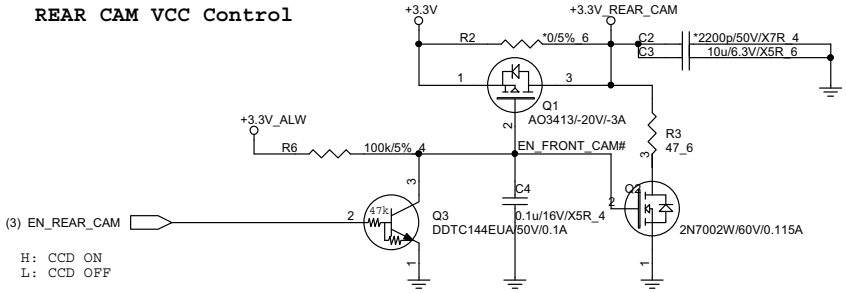
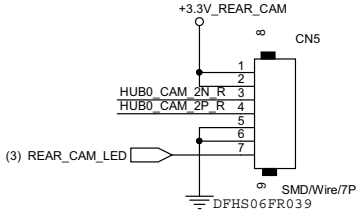
REAR CCD 8M



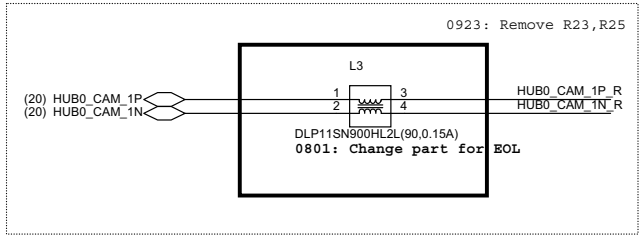


REAR CAM VCC Control

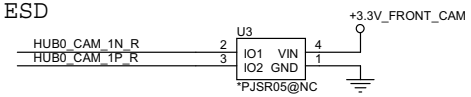




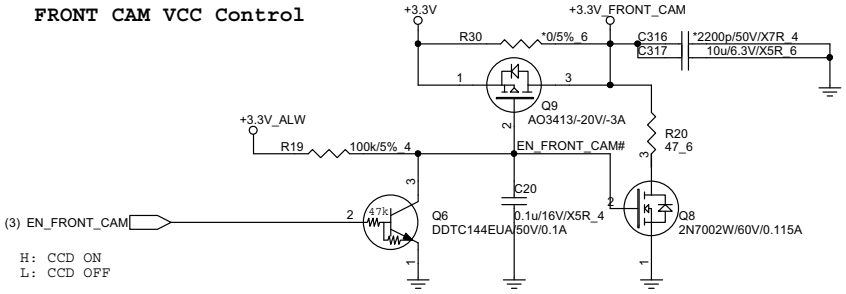
Front CCD 2M

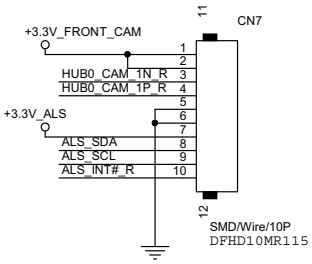


ESD

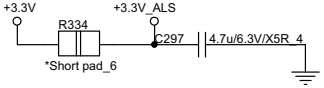


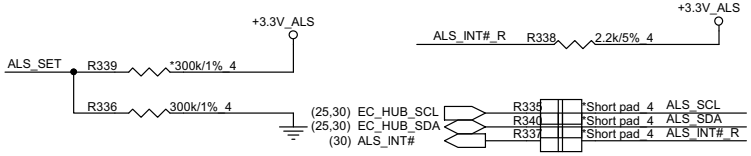
FRONT CAM VCC Control

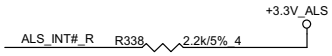




G-Sensor (0823)







I2C Address Setting :

R339	R336	I2C Address
asm		0x48
	asm	0x10

Quanta Computer Inc.

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	2M/8M CCD&Flash LED	3A

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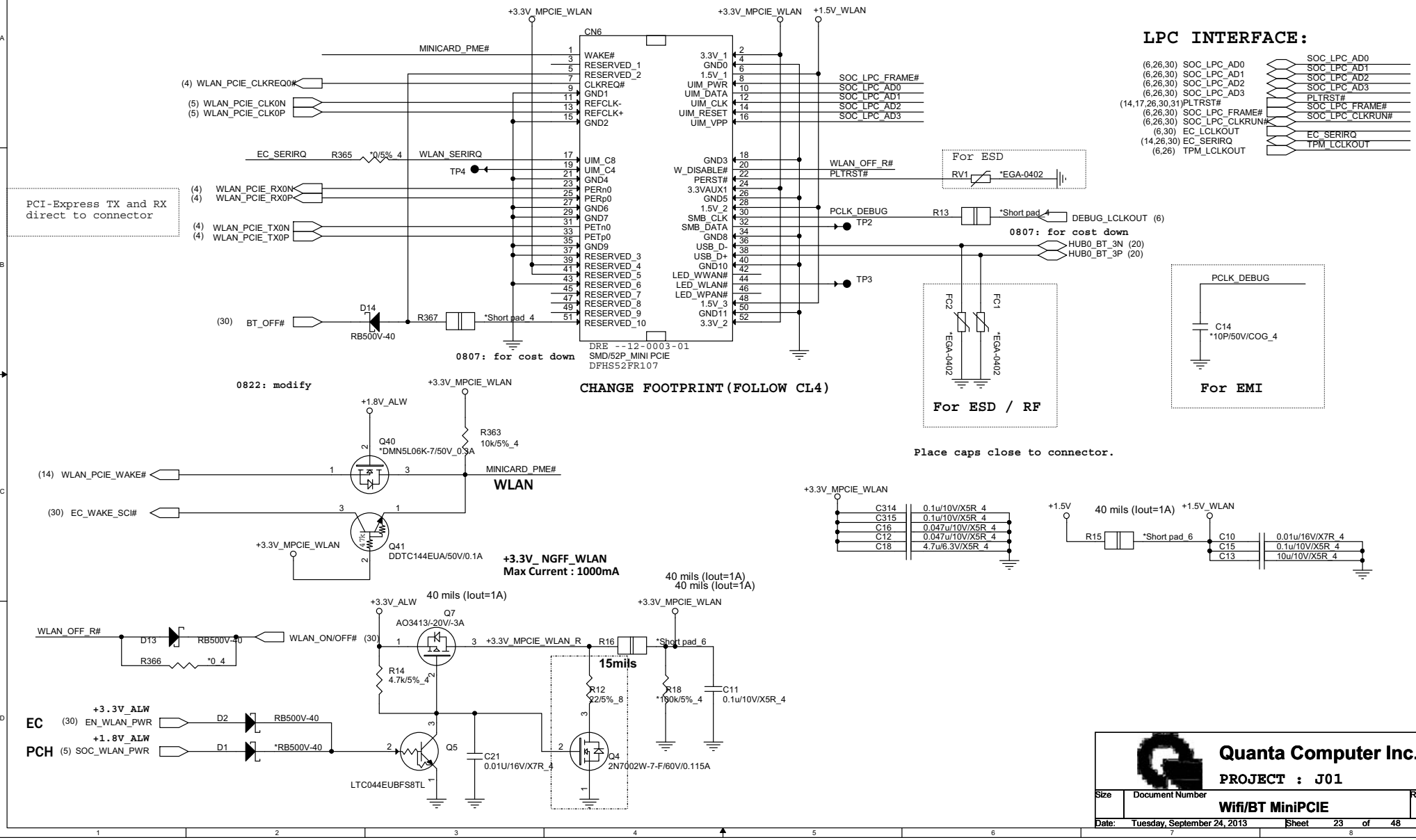
Mini PCIE Wifi/BT connector

+3.3V_ALW (2,8,14,15,19,22,26,29,30,31,34,35,36,37,38,39,40,41,42)
+1.5V (8,27,38,43)



LPC INTERFACE:

(6,26,30)	SOC_LPC_AD0	SOC_LPC_AD0
(6,26,30)	SOC_LPC_AD1	SOC_LPC_AD1
(6,26,30)	SOC_LPC_AD2	SOC_LPC_AD2
(6,26,30)	SOC_LPC_AD3	SOC_LPC_AD3
(14,17,26,30,31)	PLTRST#	PLTRST#
(6,26,30)	SOC_LPC_FRAME#	SOC_LPC_FRAME#
(6,26,30)	SOC_LPC_CLKRUN#	SOC_LPC_CLKRUN#
(6,30)	EC_LCLKOUT	EC_SERIRQ
(14,26,30)	EC_SERIRQ	TPM_LCLKOUT
(6,26)	TPM_LCLKOUT	

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	Wifi/BT MiniPCIE	3A

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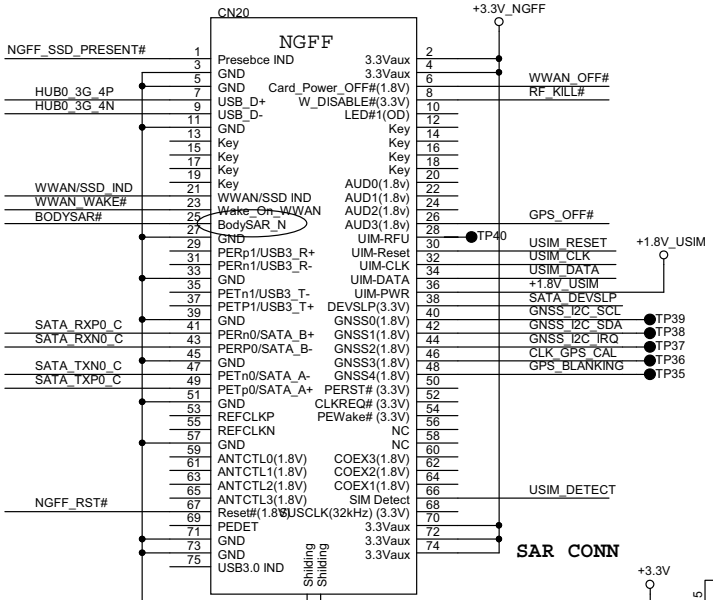
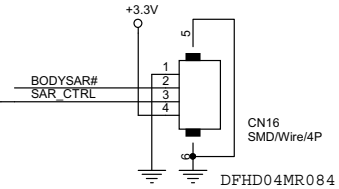
3G NGFF Conn (MU736)

23

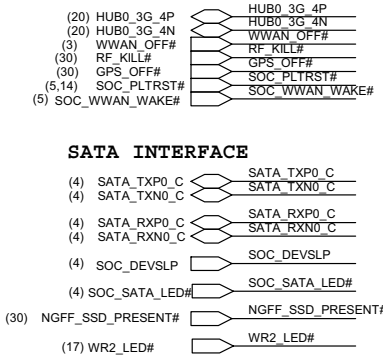
CHECK FOOTPRINT PART NUMBER



SAR CONN

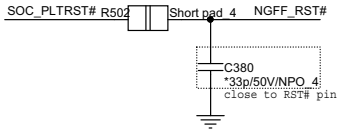


NGFF INTERFACE

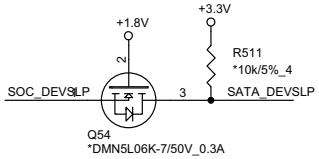


SATA INTERFACE

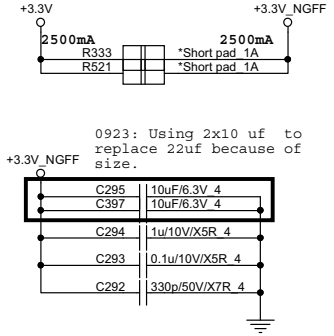
NGFF_RST# (1.8V)



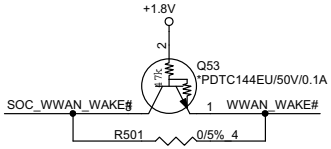
SATA DEVSLP



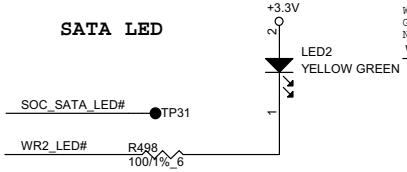
NGFF POWER



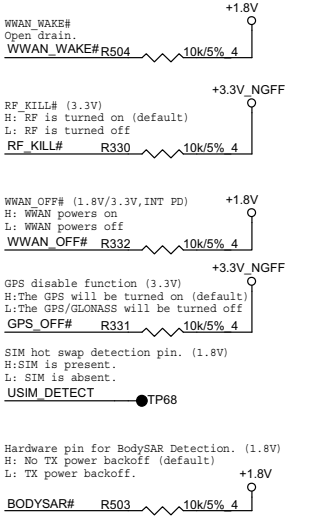
WWAN WAKE#



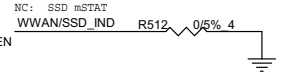
SATA LED



NGFF HW STRAPS

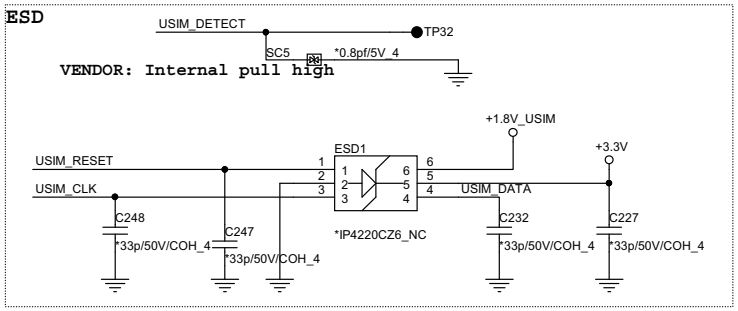


WWAN/SSD_IND, Slot B Indication Pin Definitions
GND: WWAN
NC: SSD mSTAT

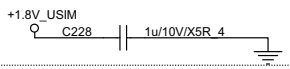


SIM Card

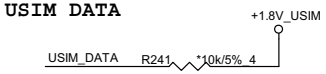
ESD



USIM POWER

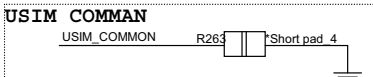


USIM DATA

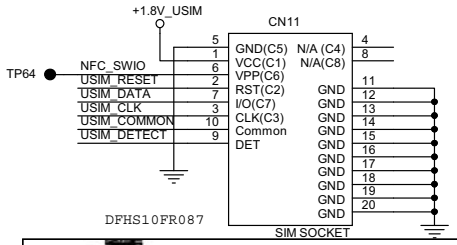


VENDOR: Internal pull high

USIM COMMAN



VENDOR: COMMON Shoule be connected to GND.



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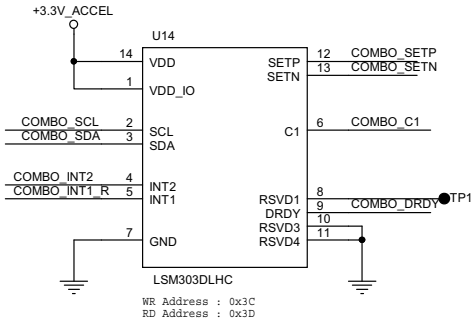
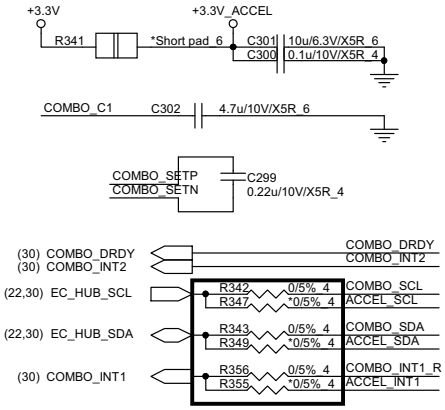
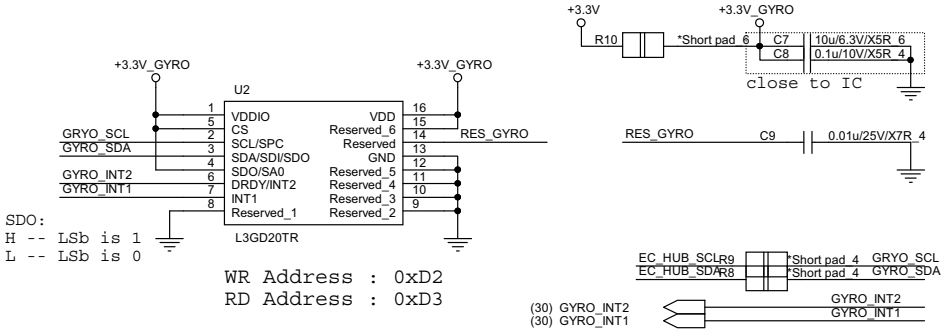
G-sensor/E-compass/Magnetometer (High-end SKU) Gyroscope (High-end SKU)



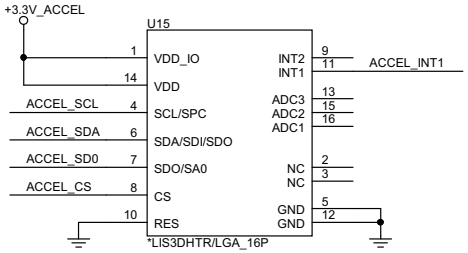
Checking ~~~



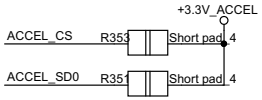


0924:
High-END: populate R342/R343/R356
Entry-SKU: populate R347/R349/R355

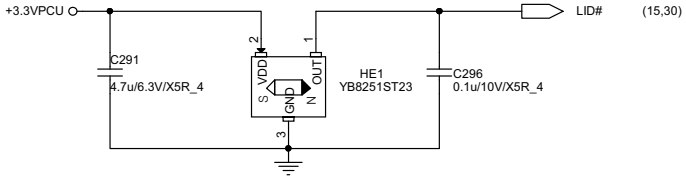
Accelerometer (Entry SKU)



G_SENSOR_CS
1: I2C mode
0: SPI enabled



Hall sensor



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	GPS SAR LED ALS POWER BUTTON	3A

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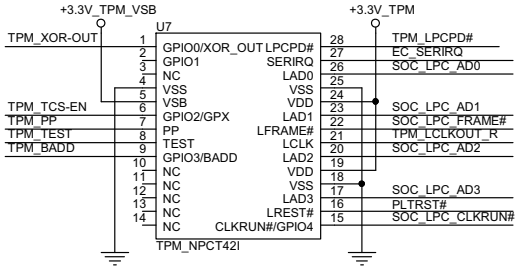
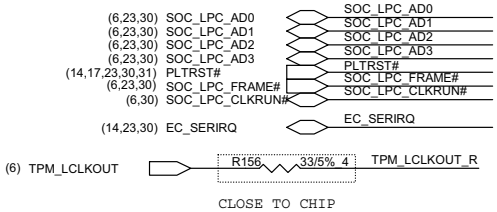
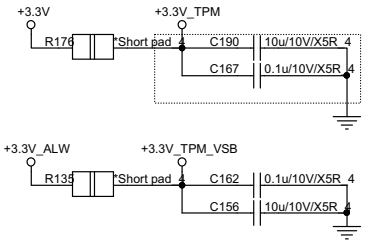
TPM



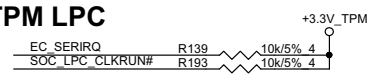
TPM interface



TPM power supplier



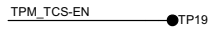
TPM LPC



TPM LPCPD#

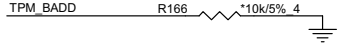
TPM PP

TPM TCS-EN

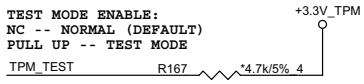


TPM HW STRAPS

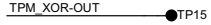
```
BASE ADRESS:
NC -- 7Eh-7Fh  , NORMAL (DEFAULT)
PULL DOWN -- EEh-EFh
```




```
TEST MODE ENABLE:
NC -- NORMAL (DEFAULT)
PULL UP -- TEST MODE
```




```
XOR TREE OUTPUT:
```



INTERNAL PU & PD RESISTORS.

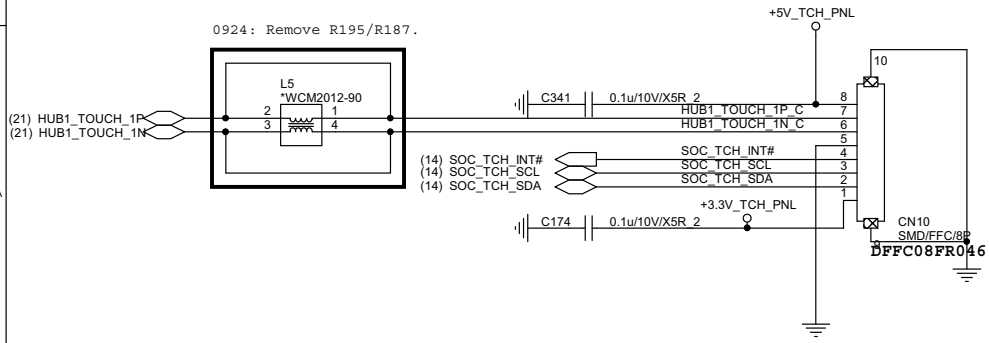
Table 2. Internal Pull-Up and Pull-Down Resistors

Signal	Pin(s)	Power Well	Type	Comments
LPCPD	28	V_{DD}	PU_{110}	
GPIO4-0	15, 9, 6, 2, 1	V_{DD}	PU_{110}	Programmable[1]
GPX	6	V_{DD}	PU_{110}	Note[2]
PP	7	V_{DD}	PU_{110}/PD_{110}	Programmable[3]
TEST	8	V_{DD}	PD_{110}	Strap

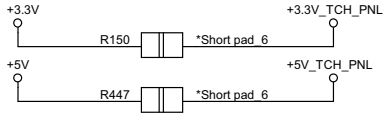
1. Default at reset: GPIO0,2,3 enabled, GPIO1,4 disabled.
2. When GPIO-Express-00 (GPX) is selected for pin 6, the pull-up is enabled by default.
3. Default at reset: pull-down enabled.

Touch Screen

0924: Remove R195/R187.

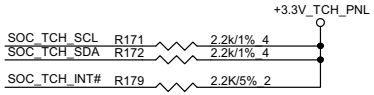


Touch Panel VCC Control

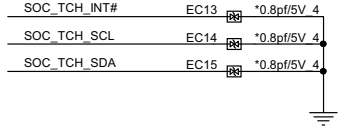


+5V_TOUCH_PANEL
Max Current : 800mA

Touch Panel I2C



Touch Panel ESD



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	TPM	3A

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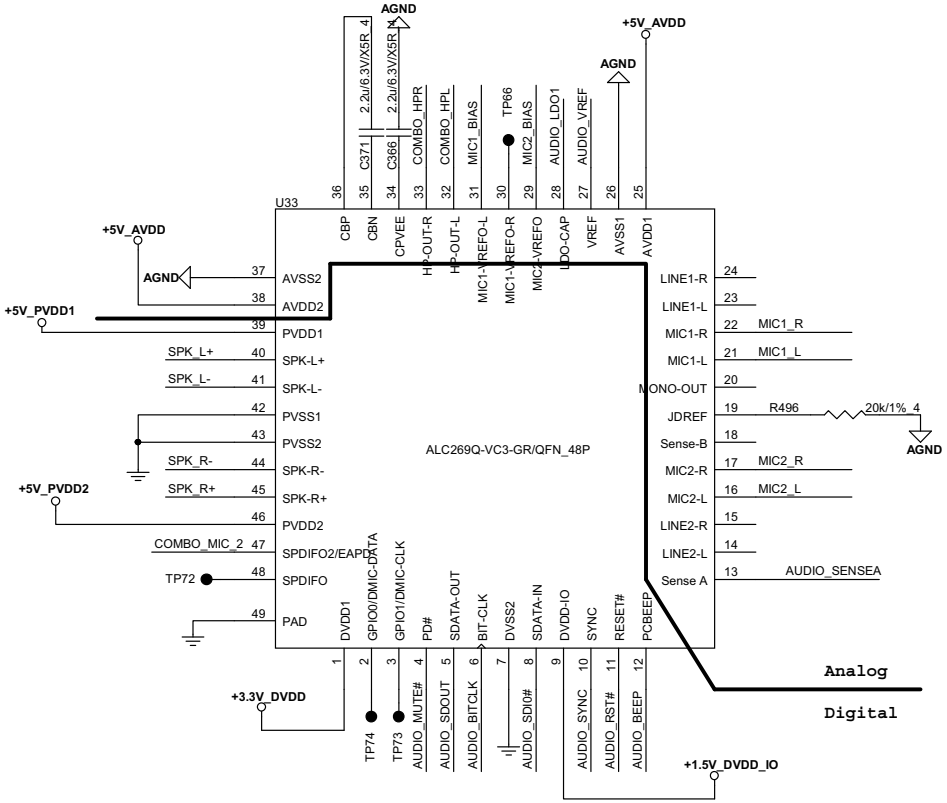
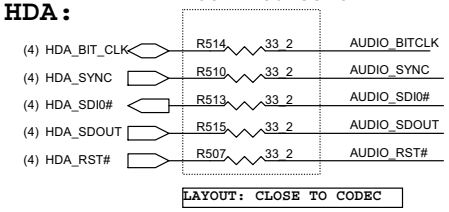
AUDIO CODEC

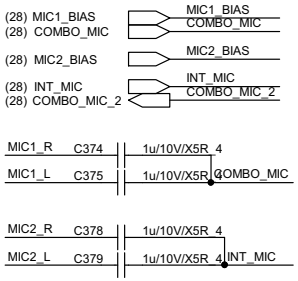


HDA:

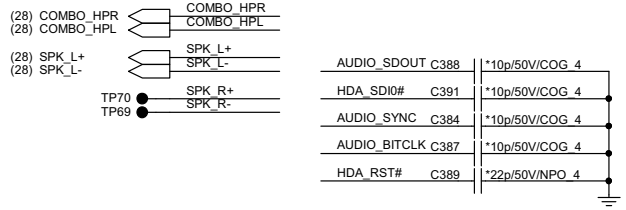
Intel DG: 33 ohm



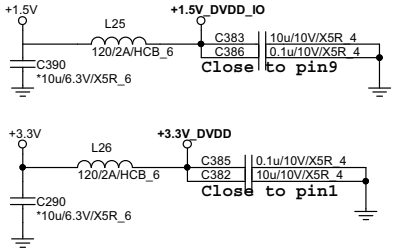
INT/EXT MIC:

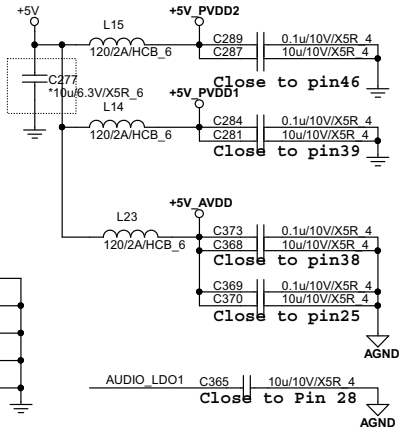


H/P OUT & SPK OUT:

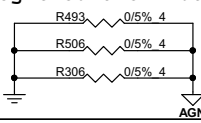


Audio Power

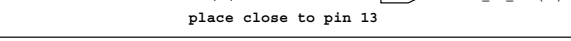




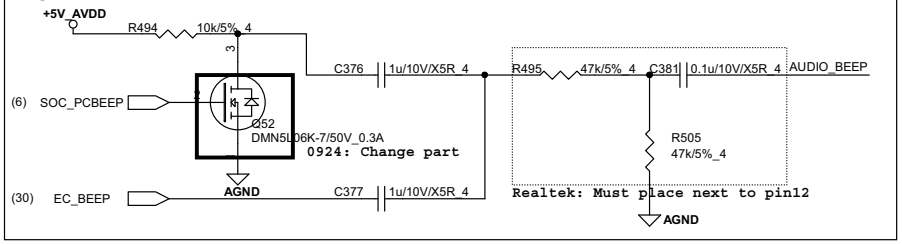
Analog Ground of Audio



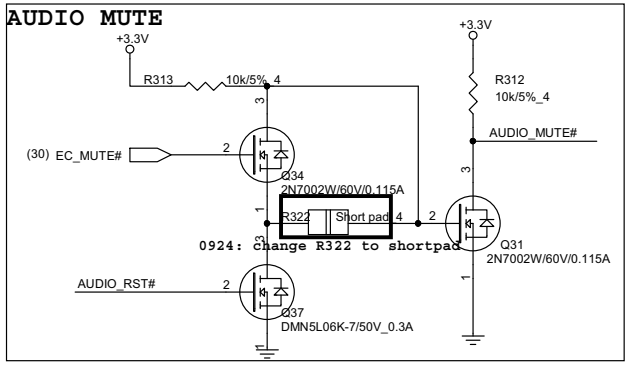
JACK SENSE



PC BEEP



AUDIO MUTE



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	HDA AUDIO CODEC ALC282	3A

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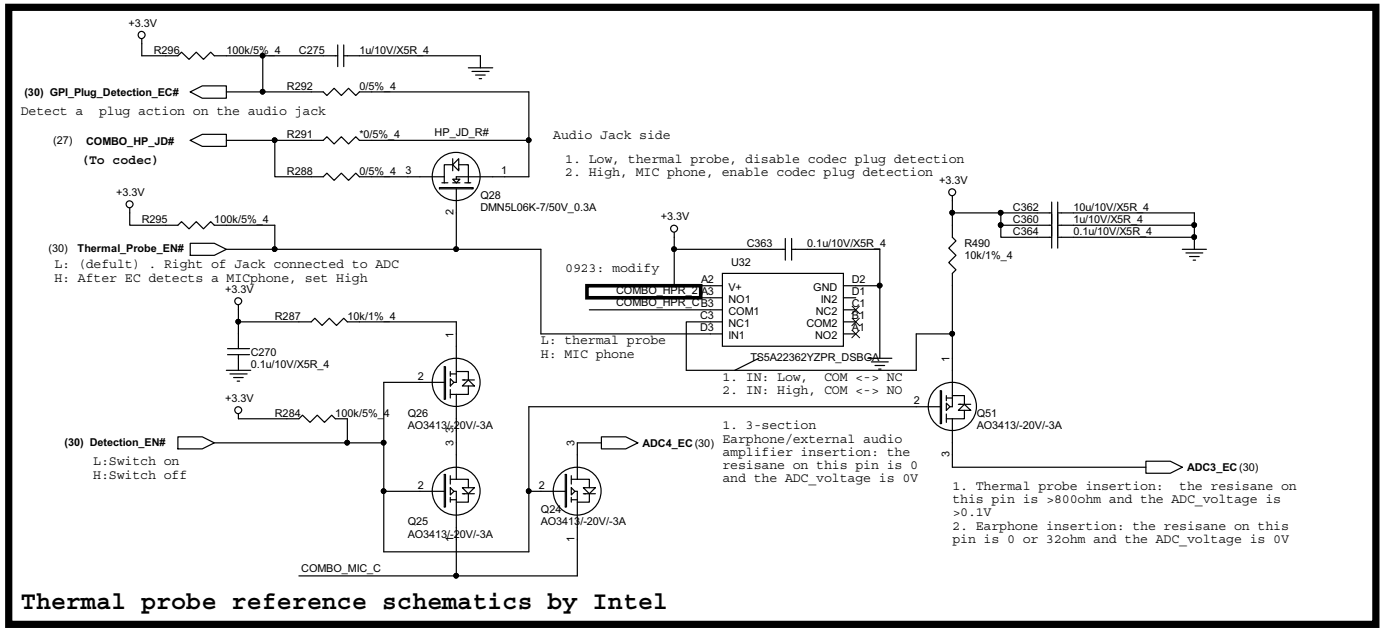
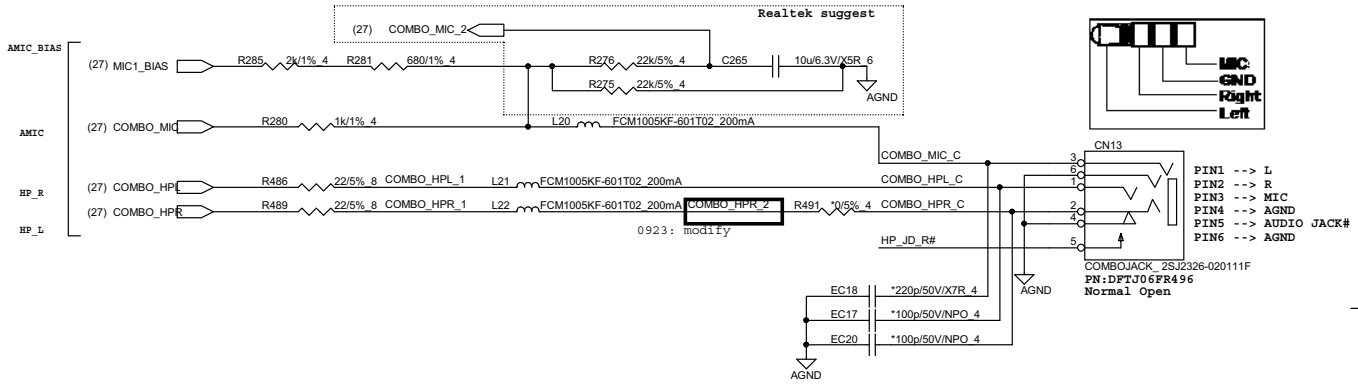
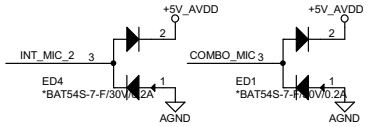
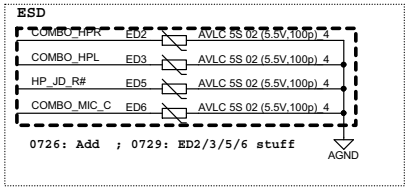
Headphone and Mic Jack



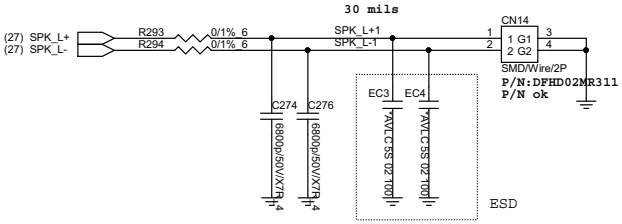
Thermal probe reference schematics by Intel



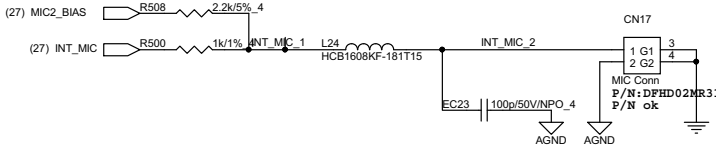




SPEAKERS



INTERNAL MIC



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	AUDIO/SPK/HP/MIC	3A

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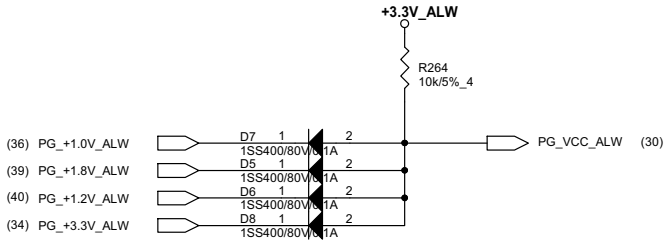
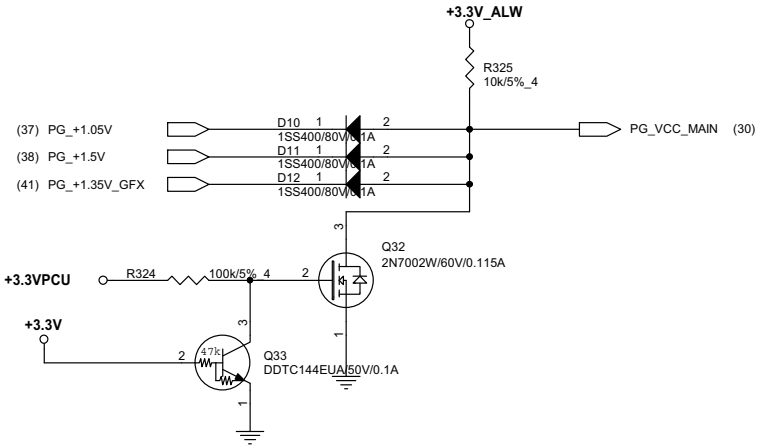
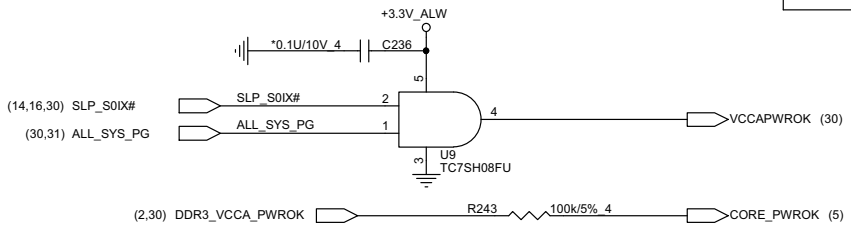
ALWAYS POWER GOOD



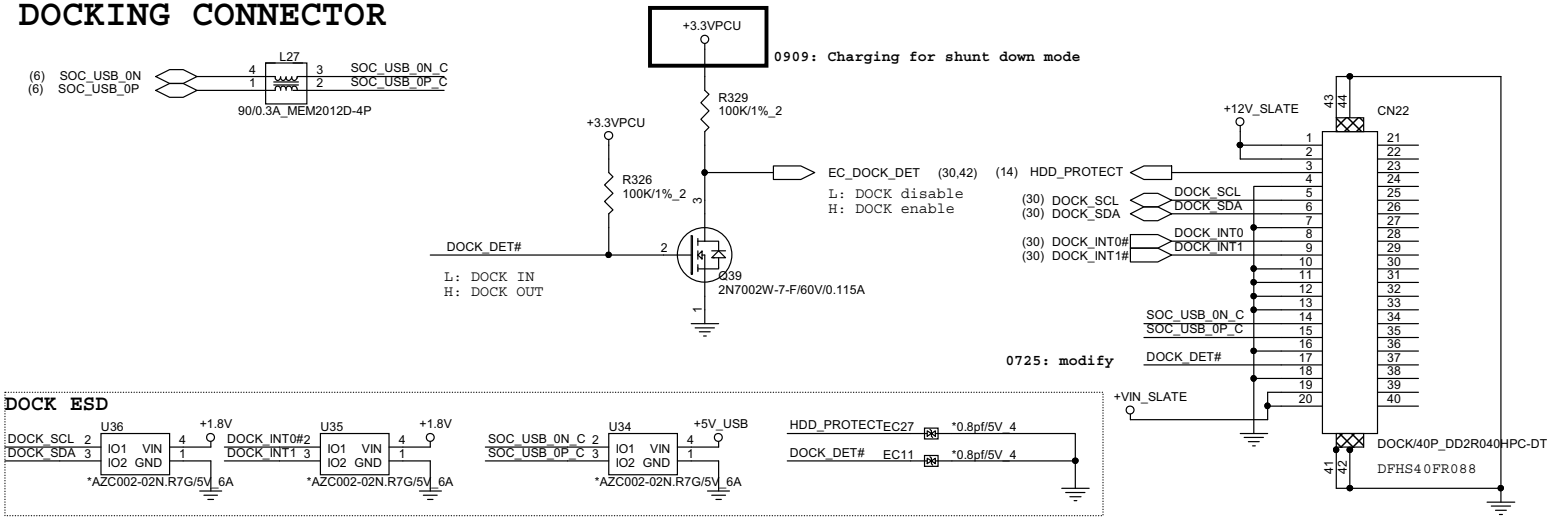
ALL SYSTEM POWER GOOD

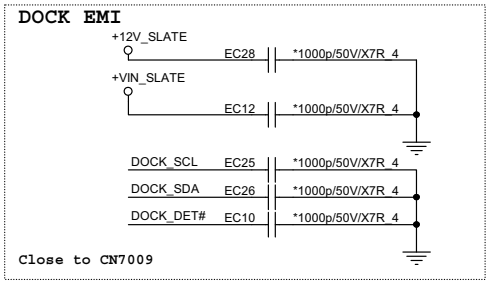


DRAM/CORE POWER OK



DOCKING CONNECTOR





Quanta Computer Inc.

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Size	Document Number	Rev
	TBD	3A

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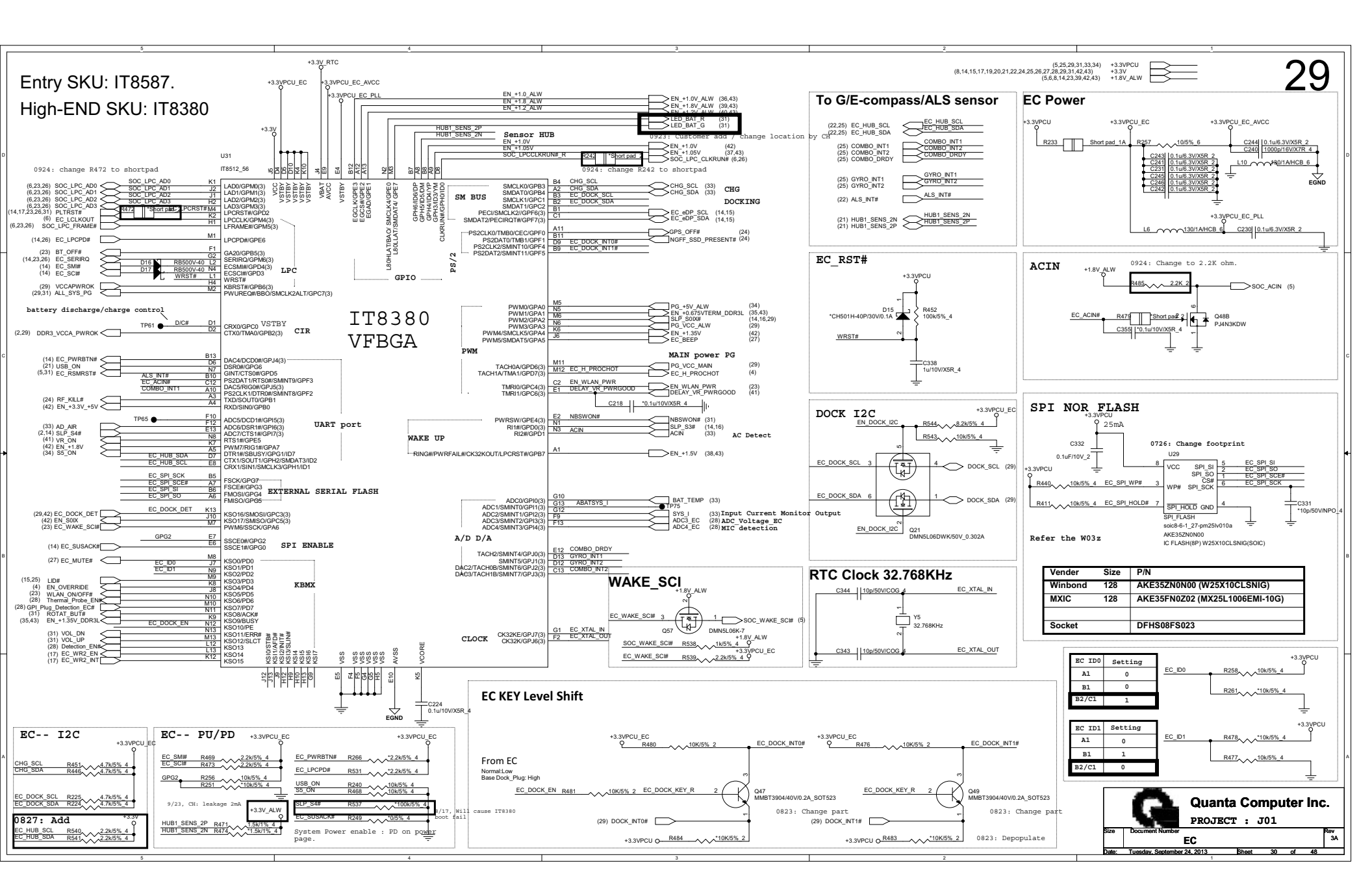


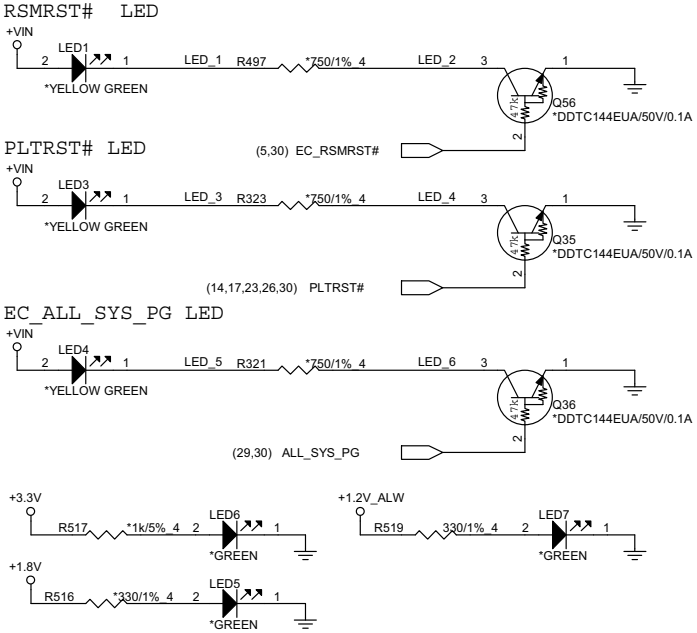
Vender	Size	P/N
Winbond	128	AKE35ZN0N00 (W25X10CLSNIG)
MXIC	128	AKE35FN0Z02 (MX25L1006EMI-10G)
Socket	DFHS08FS023	

EC ID0	Setting
A1	0
B1	0
B2/C1	1

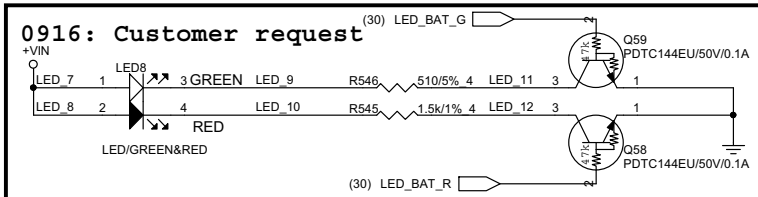
EC ID1	Setting
A1	0
B1	1
B2/C1	0

LED For bring-up

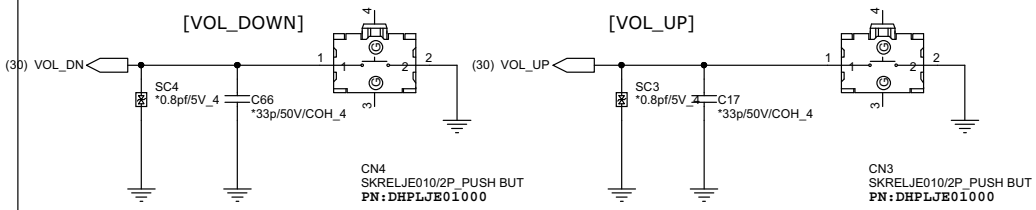
0914: Remove all from PVT2 stage



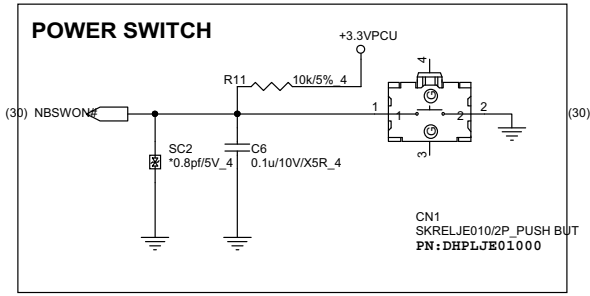
0916: Customer request



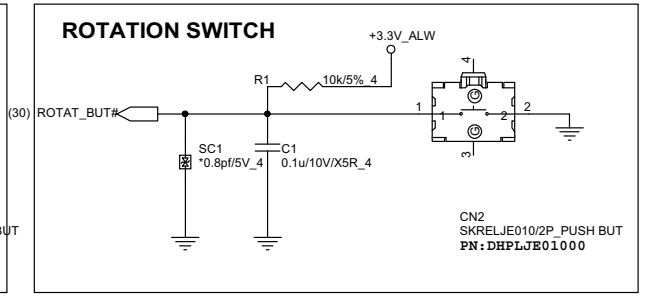
VOLUME CONTROL



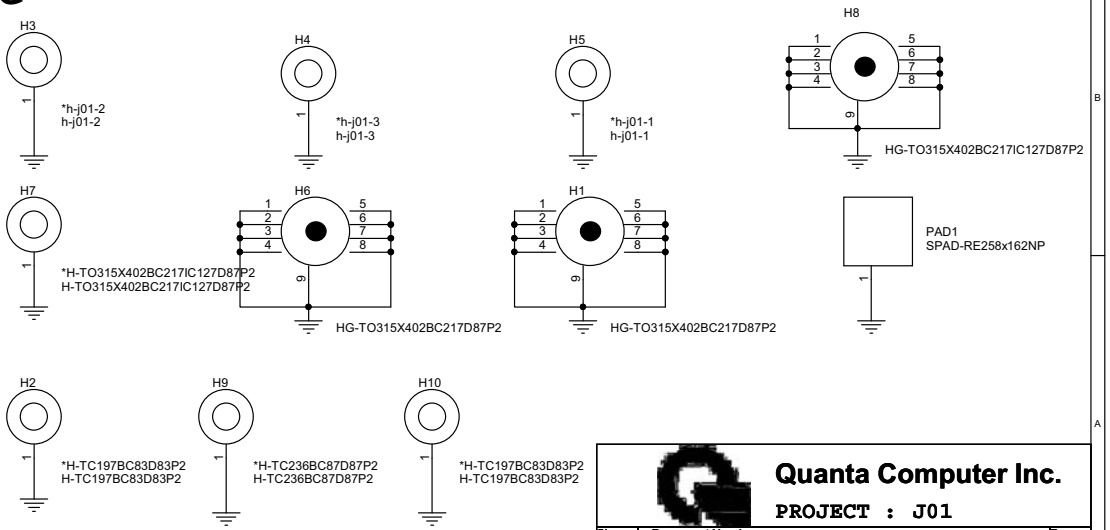
POWER SWITCH



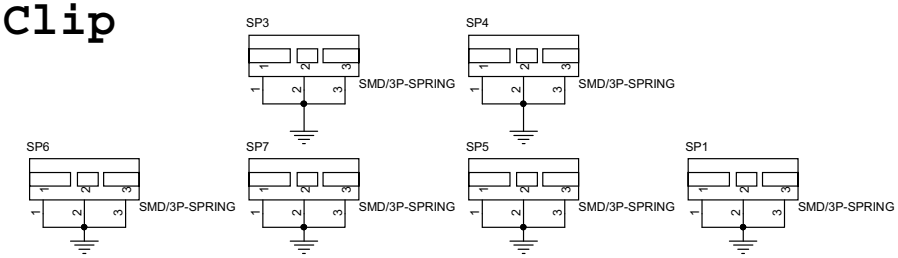
ROTATION SWITCH



Hole



Clip



Quanta Computer Inc.

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Size	Document Number	Rev
	ULPMC	3A

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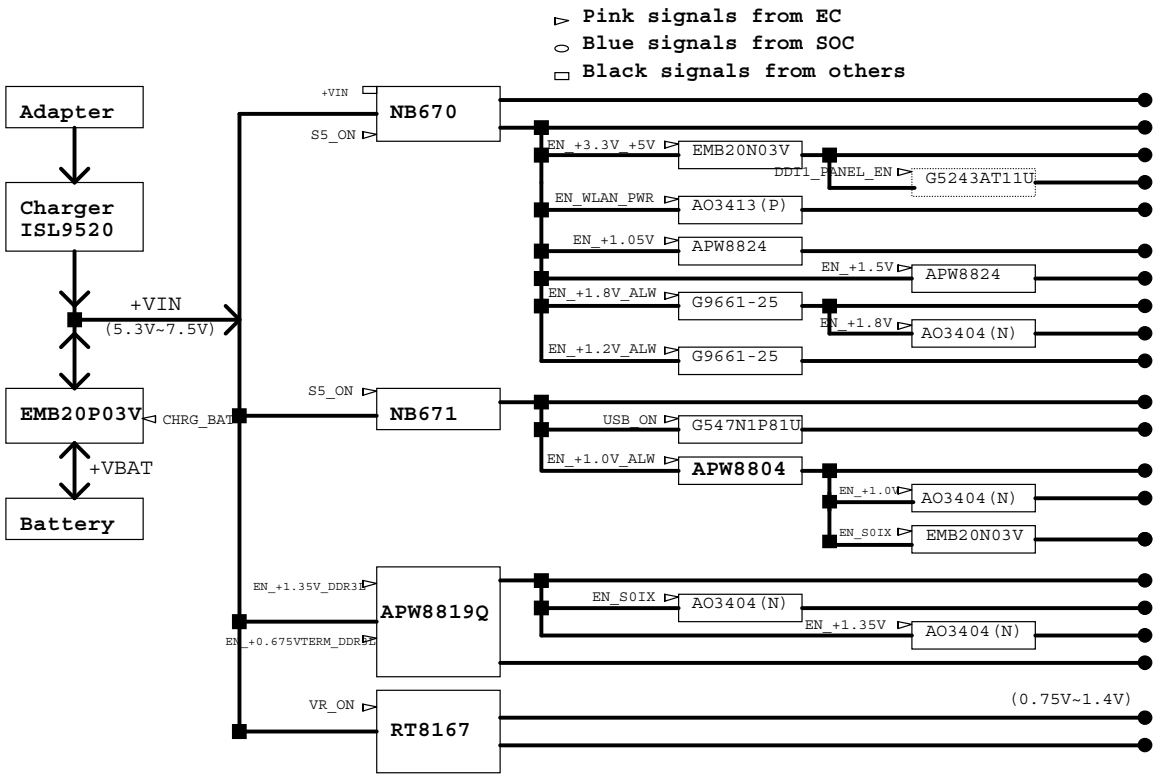

Power Rails	Rating	Succeed Power Rails
+3.3VPCU	(0.1A)	+3.3VPCU_EC, +3.3VPCU_EC_AVCC, +3.3VPCU_EC_PLL
+3.3V_ALW	(1.0A)	+3.3V_ALW_SOC_USB,+3.3V_TPM_VSB
+3.3V	(1.7A)	+3.3V_2136_D,+3.3V_2136_A,+3.3V_WR2_VDD,+3.3V_WR2_AVDD, +3.3V_USB_HUB0,+3.3V_USB_HUB1,+3.3V_REAR_CAM,+3.3V_NGFF, +3.3V_ACCEL,+3.3V_GYRO,+3.3V_ALS,+3.3V_RFRONT_CAM +3.3V_TPM,+3.3V_DVDD
+3.3V_LCD_VCC		
+3.3V_MPCIE_WLAN		
+1.05V		+1.05V_SOC_CORE
+1.5V		+1.5V_SOC_HDA,+1.5V_WLAN,+1.5V_DVDD_IO
+1.8V_ALW		+1.8V_ALW_PADSUS,+1.8V_ALW_SOC_USB
+1.8V		+1.8V_eMMC_VDDQ,+1.8V_SOC_PADCF1
+1.2V_ALW		
+5V_ALW	(1.5A)	
+5V_USB	(1.0A)	
+1.0V_ALW		+1.0V_SOC_USB3_1
+1.0V		+1.0V_WR2_AVDD,+1.0V_WR2_PLL,+1.0V_WR2_CORE +1.0V_SOC_USB3_2,+1.0V_GPIO
+1.0V_S0IX		+1.0V_S0IX_SOC_DRAM1,+1.0V_S0IX_SOC_DRAM2, +1.0V_S0IX_SOC_DDI
+1.35V_DDR3L		+0.675_SOC_DVREF,+1.35V_SOC_DDRCLK,+1.35V_SOC_DDRXXX
+1.35V_S0IX		+1.35V_SFRBD0SI0,+1.35V_SFRDSISI0
+1.35V		
+0.675VTERM_DDR3L		
+VCORE		
+1.35V_GFX		

Quanta Computer Inc.

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Size	Document Number	Rev
	POWER MAP	3A

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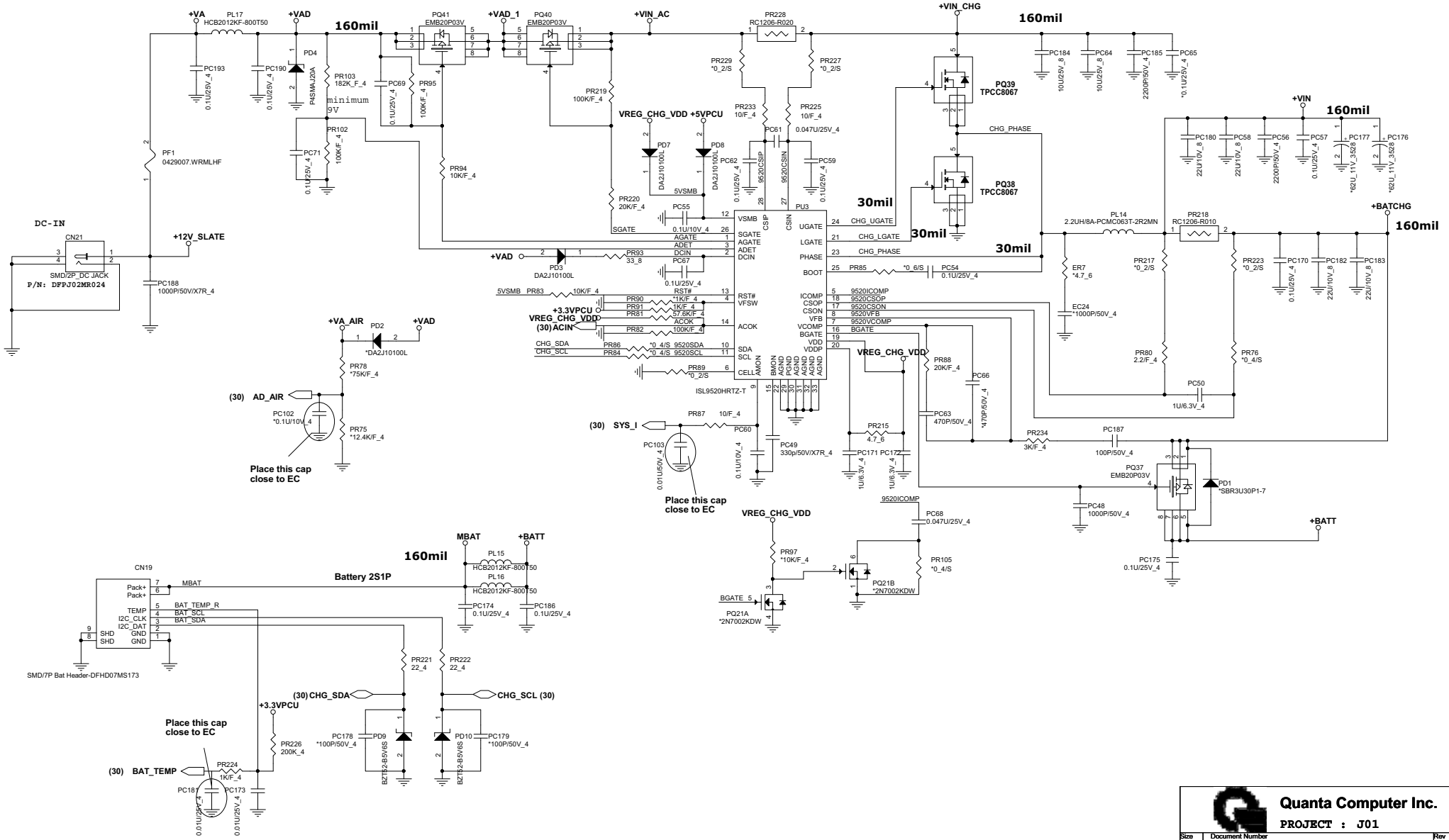
ADP Voltage=12V



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	CHARGER (ISL9520)	3A

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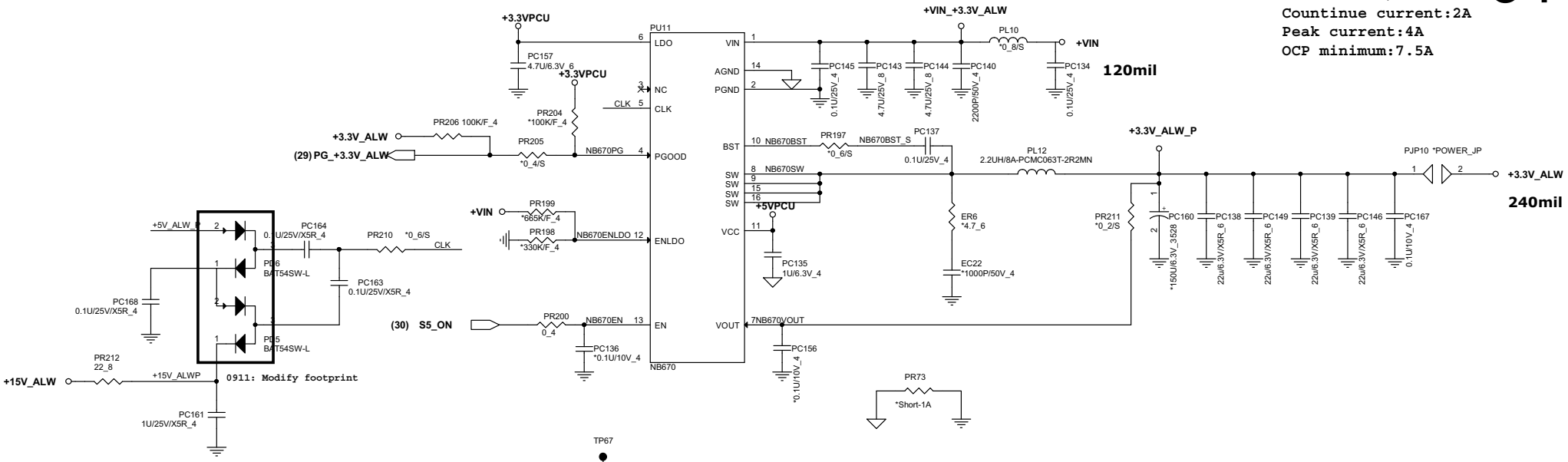
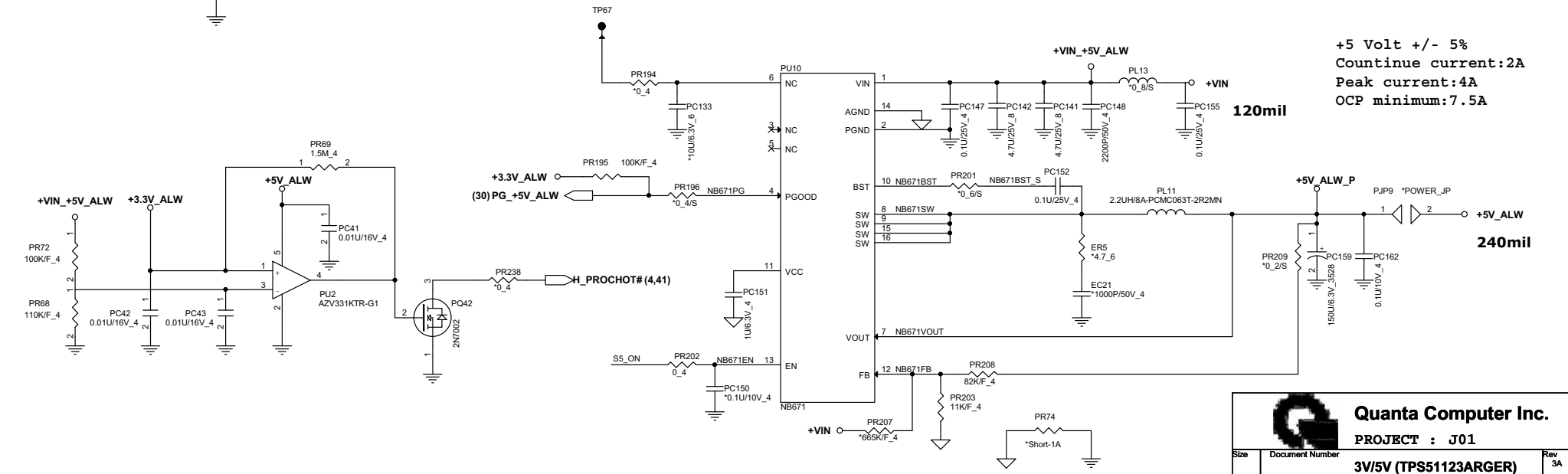
+3.3 Volt +/- 5%
Countinue current:2A
Peak current:4A
OCP minimum:7.5A



+5 Volt +/- 5%
Countinue current:2A
Peak current:4A
OCP minimum:7.5A



Quanta Computer Inc.

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Size	Document Number	Rev
	3V/5V (TPS51123ARGER)	3A

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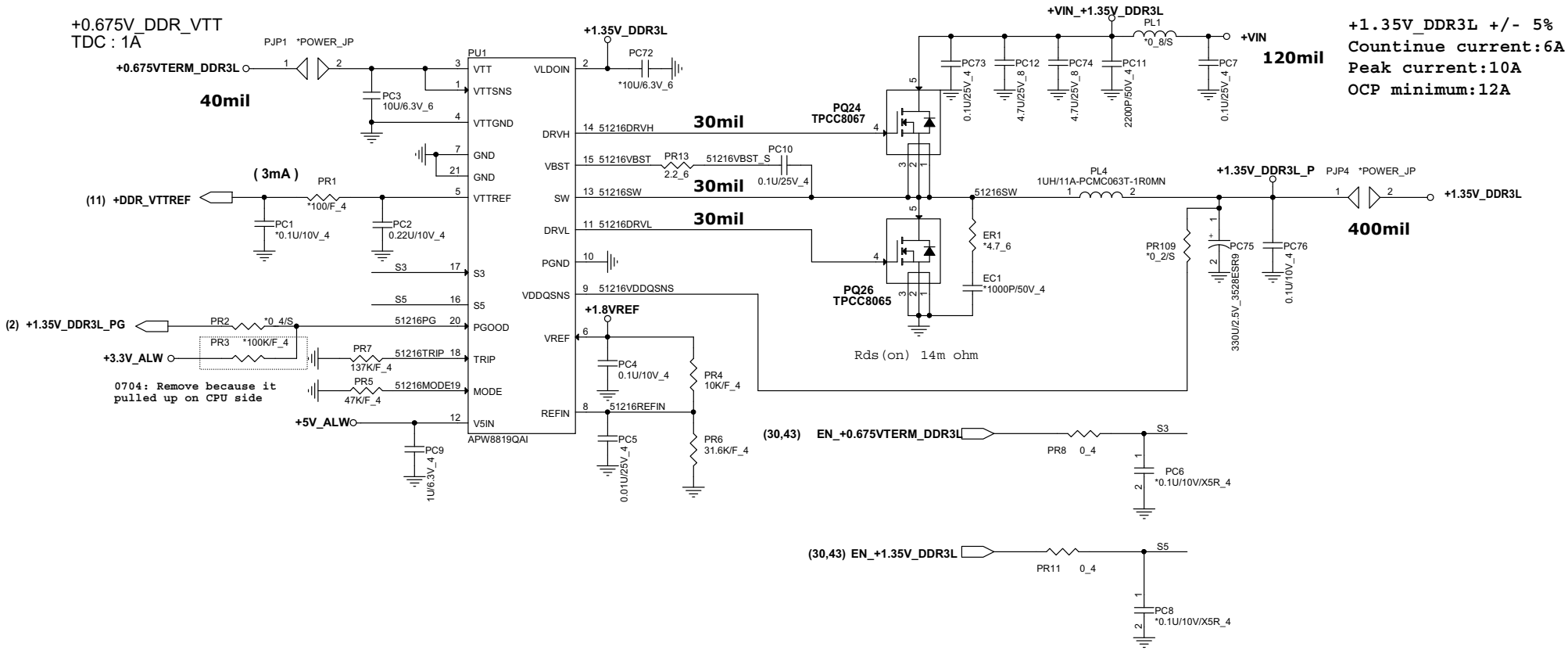

+1.35V_DDR3L +/- 5%
Countinue current:6A
Peak current:10A
OCP minimum:12A

Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	1.35/0.675V(TPS51216RUKR)	3A

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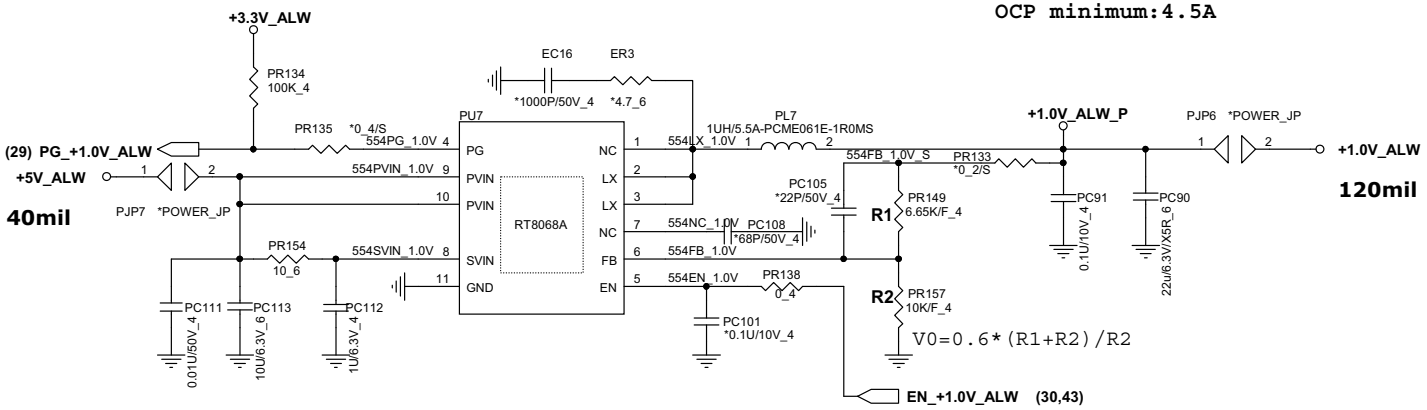
+1.0V_ALW Volt +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum:4.5A



Quanta Computer Inc.		
PROJECT : J01		
Size	Document Number	Rev
	+1.0V_ALW(RT8068A)	3A
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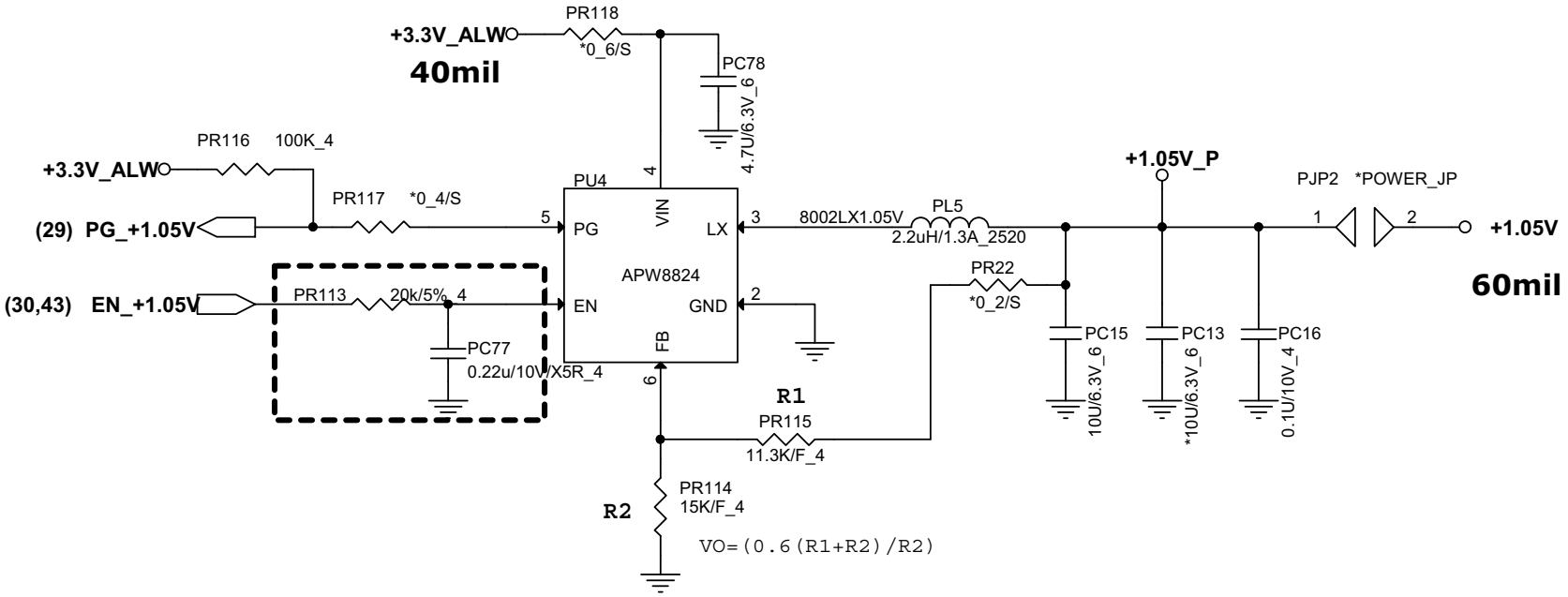
+1.05V Volt +/- 5%
Countinue current:1A
Peak current:1.3A
OCP minimum:2A



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	+1.05V (APW8824)	3A

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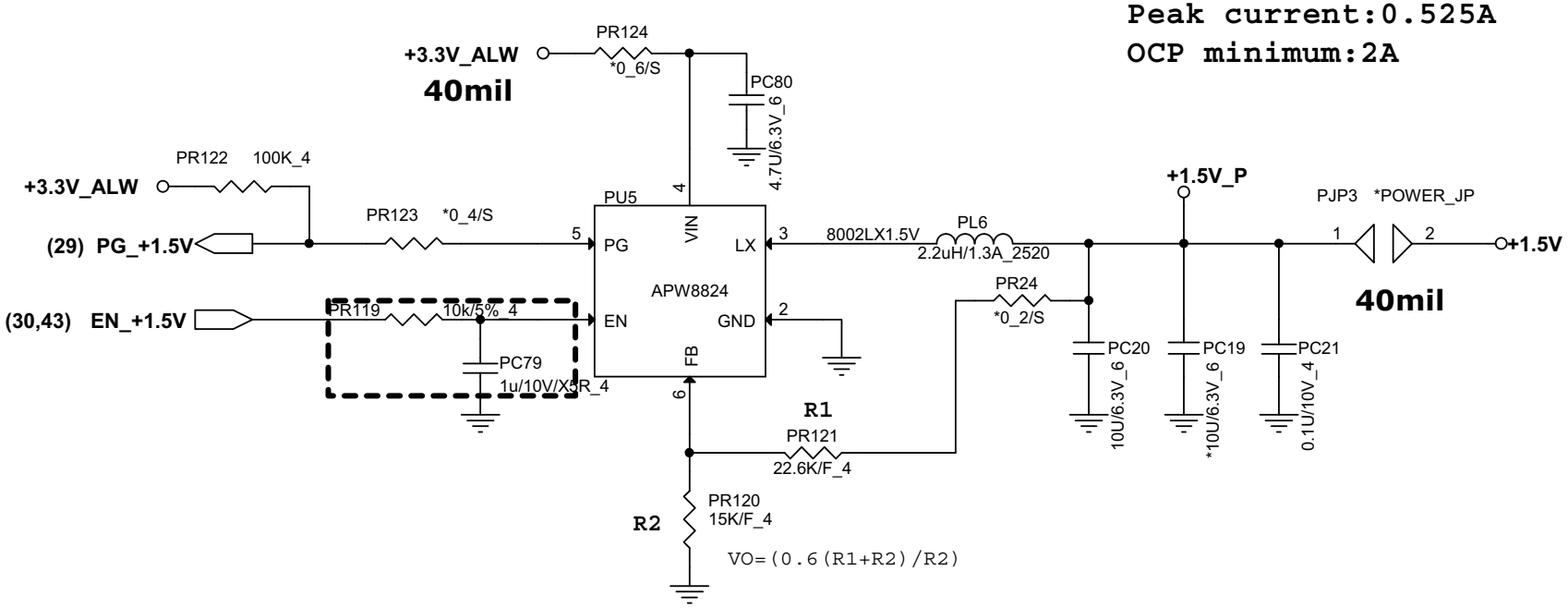
+1.5V +/- 5%
Countinue current:0.45A
Peak current:0.525A
OCP minimum:2A



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	+1.5V (APW8824)	3A

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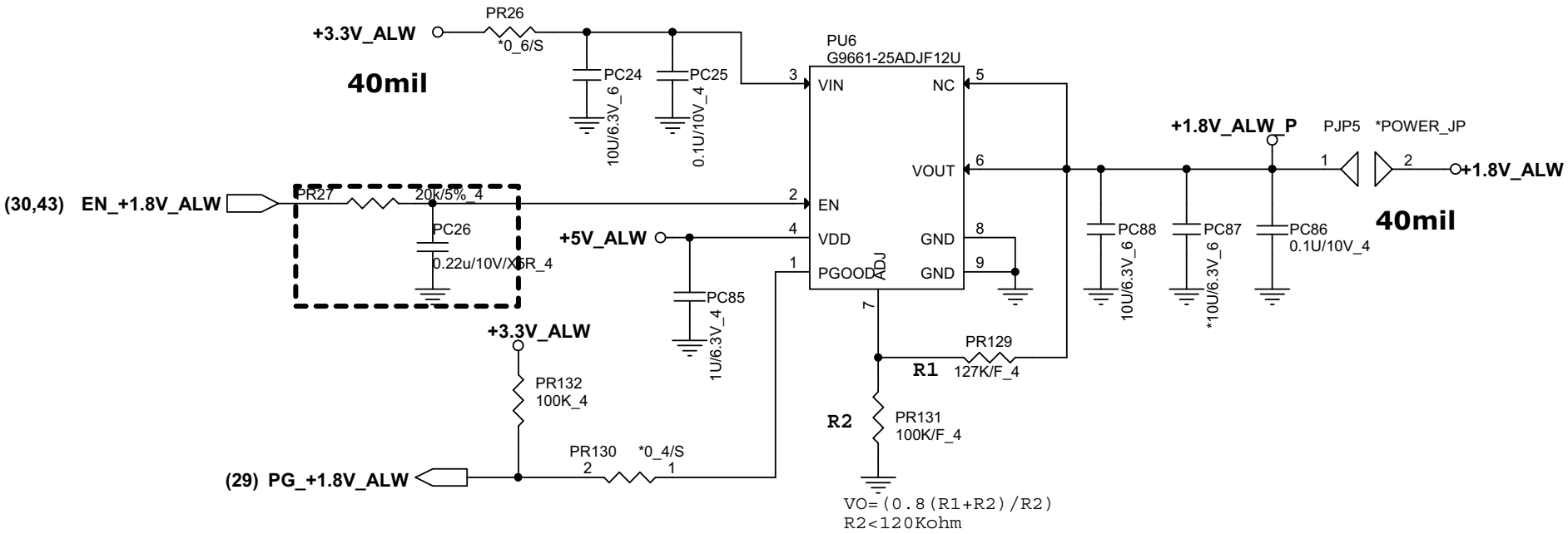
+1.8V Volt +/- 5%
Countinue current:0.105A
Peak current:0.3A



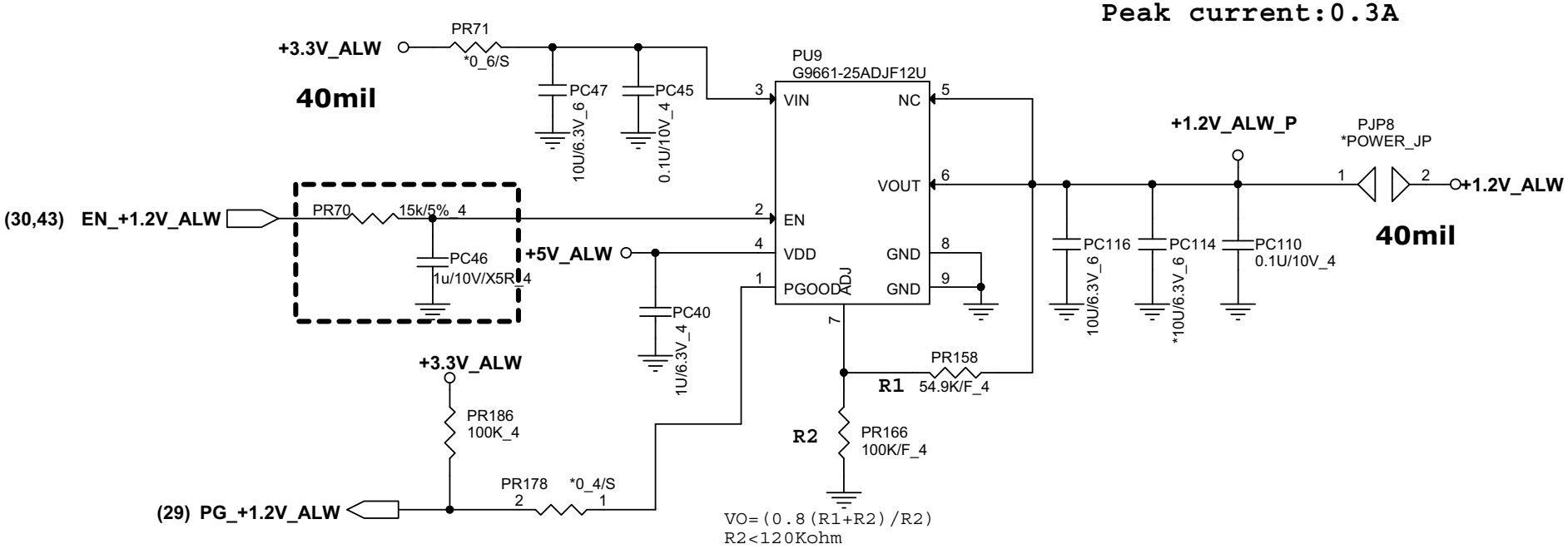
Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	+1.8V_ALW(G9661)	3A

Date: Tuesday, September 24, 2013 Sheet 39 of 48

+1.2V_ALW Volt +/- 5%
Countinue current:35mA
Peak current:0.3A



Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	+1.2V_ALW (G9661)	3A

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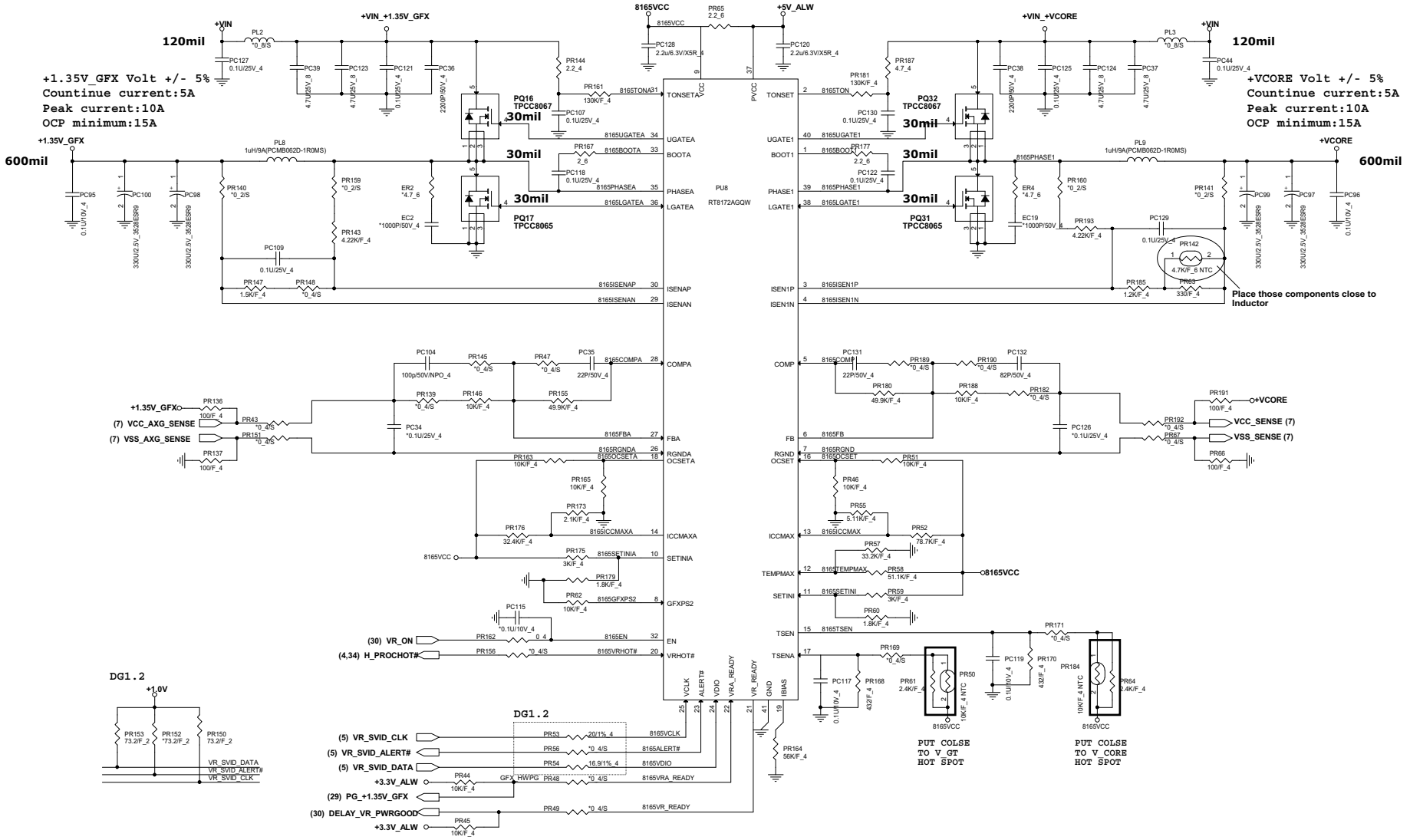

Quanta Computer Inc.

PROJECT : J01

Size	Document Number	Rev
	Vcore + Vgfx (TPS559641)	3A

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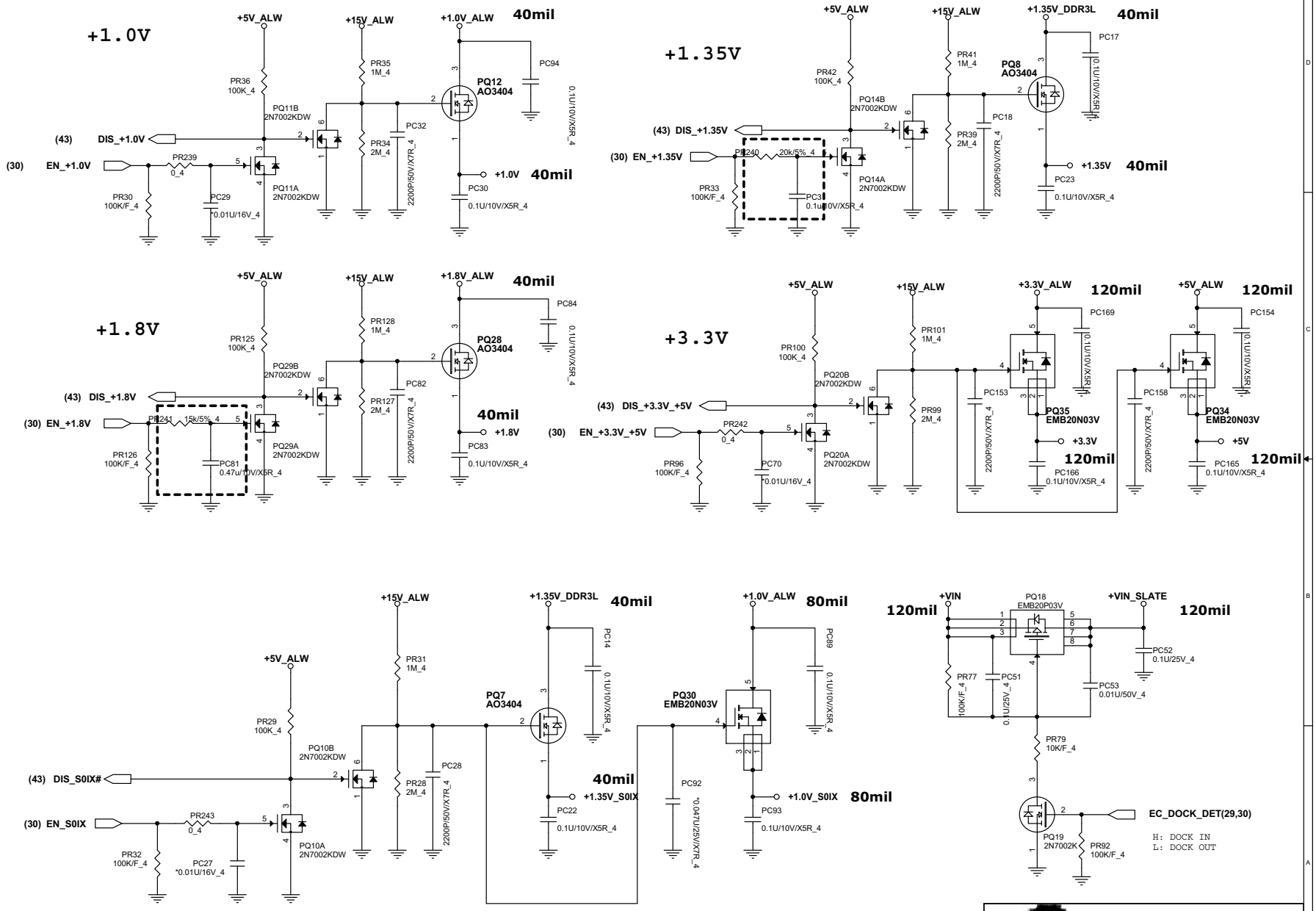
Load switch



Quanta Computer Inc.

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	Load Switch	3A

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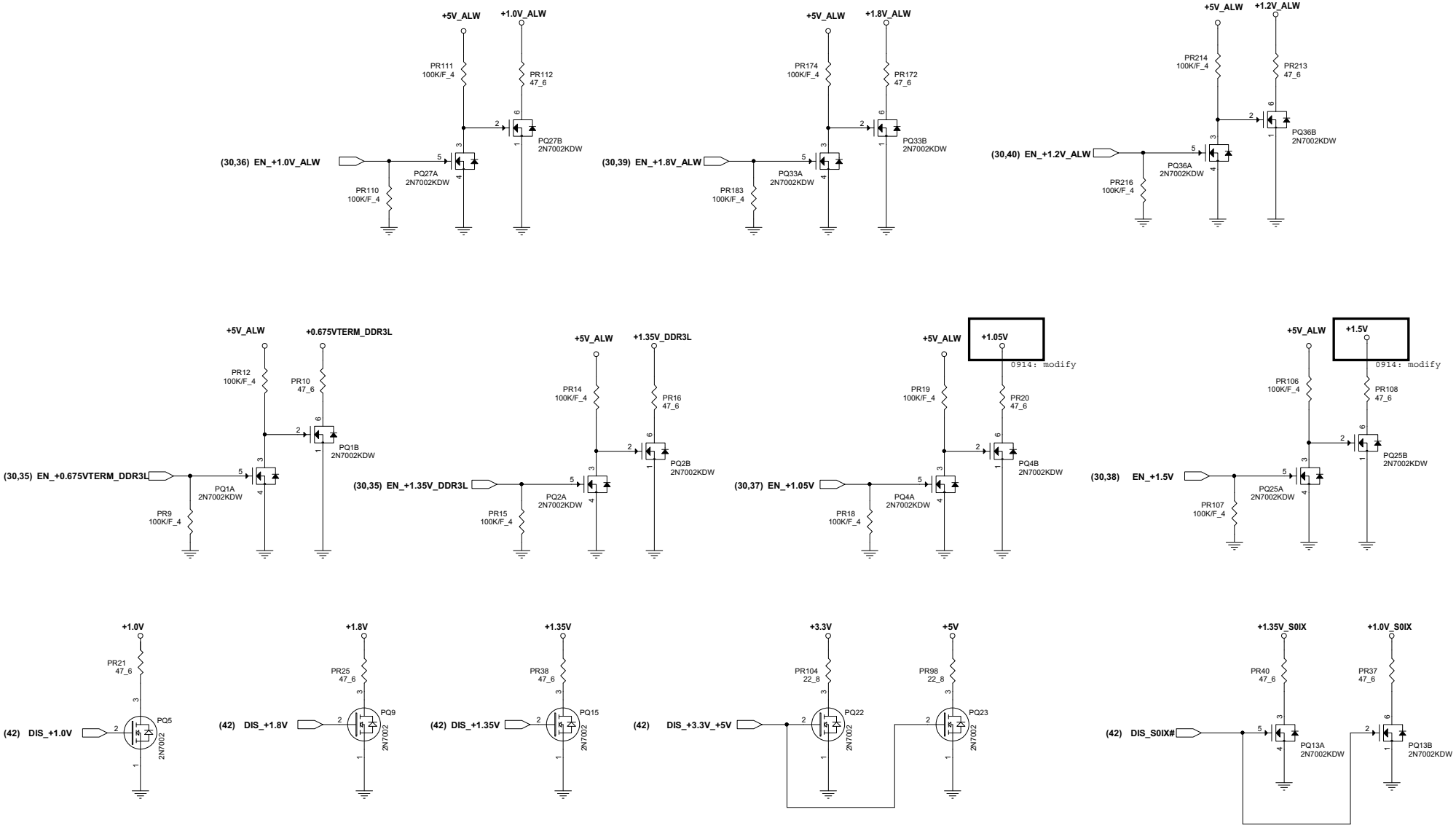
DISCHARGE

(8,14,15,17,19,20,21,22,24,25,26,27,28,29,30,31,42) +3.3V
(3,4,5,6,8,14,15,16,18,24,29,31,42) +1.8V
(16,20,21,26,27,42) +5V
(4,5,8,17,41,42) +1.0V
(8,42) +1.35V
(8,42) +1.35V_S0IX

+3.3V
+1.8V
+5V
+1.0V
+1.35V
+1.35V_S0IX

(8,31,40) +1.2V_ALW
(2,7,11,12,35,42) +1.35V_DDR3L
(2,8,14,15,19,22,23,26,29,30,31,34,35,36,37,38,39,40,41,42) +3.3V_ALW
(5,6,8,14,23,30,39,42) +1.8V_ALW
(21,34,35,36,39,40,41,42) +5V_ALW
(8,36,42) +1.0V_ALW
(8,23,27,38) +1.5V
(8,37) +1.05V
(2,13,35) +0.675VTERM_DDR3L
(8,42) +1.0V_S0IX

+1.2V_ALW
+1.35V_DDR3L
+3.3V_ALW
+1.8V_ALW
+5V_ALW
+1.0V_ALW
+1.5V
+1.05V
+0.675VTERM_DDR3L
+1.0V_S0IX



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	Discharge	3A

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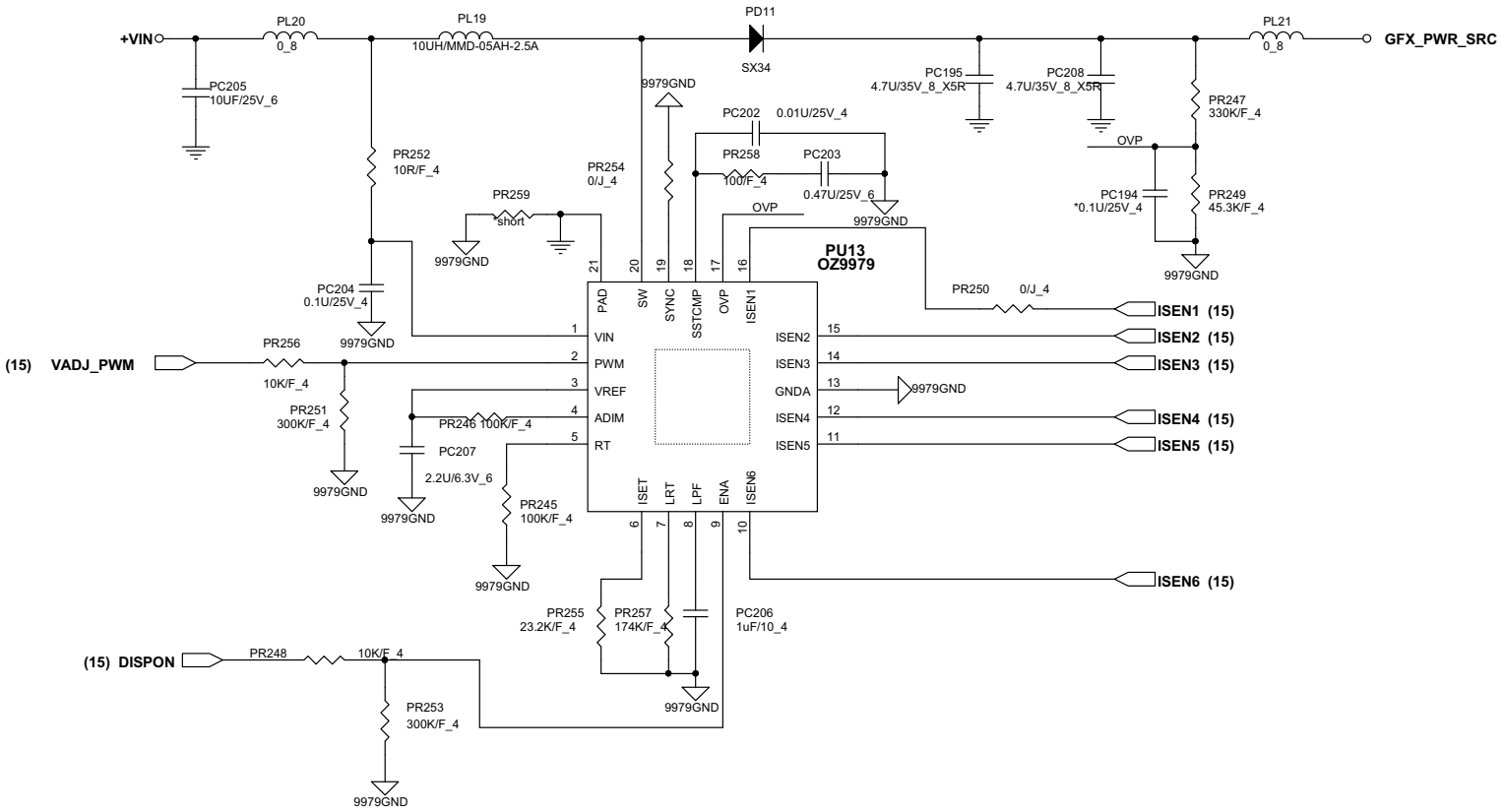
For AUO Panel



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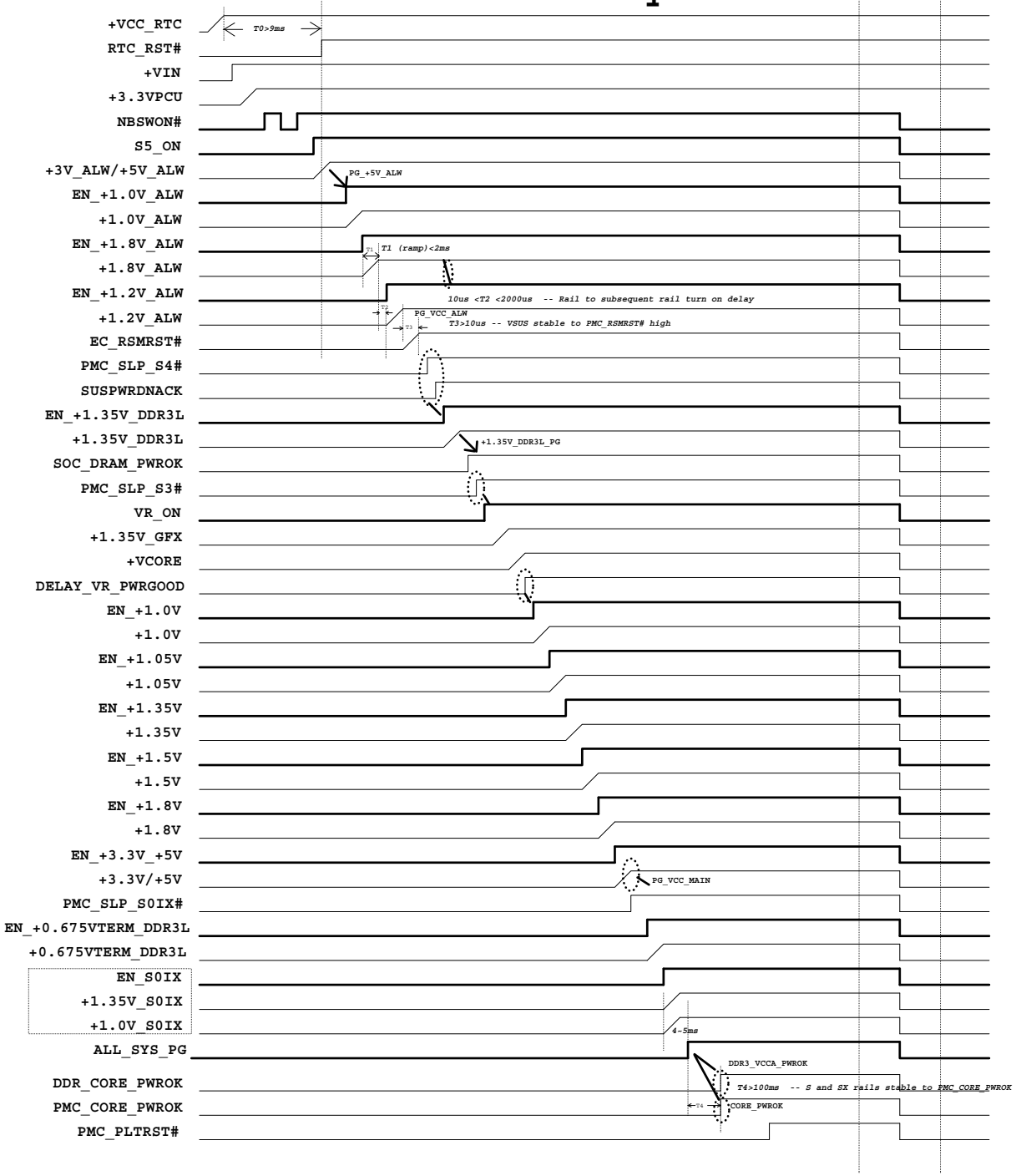
Power on sequence OFF



T0: +RTCVCC stable to RTCRST# high > 9ms
T1: VR ramp up time from 10% to 90% voltage level < 2ms
T2 :Rail to subsequent rail turn on delay < 2ms
T3 :+VALWAS stable to EC_RSMRST# high > 10us
T4 :+VS rails stable to PMC_CORE_PWROK > TBD

NOTE:
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

Green signals (PG) to EC
Blue timing -- Intel
Pink signals from EC

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Model	REV	CHANGE LIST	MODEL	FROM	To
	1A				

DOC NO.	PROJECT MODEL :	PD9	APPROVED BY:		DATE:	2012/12/13
	PART NUMBER:		DRAWING BY:		REVISON:	1A

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Size	Document Number	Rev
	ULPMC	3A

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Model	REV	CHANGE LIST	MODEL	FROM	To
	2A	B-->C *1. Modify CORE_PWROK in page 29*			

DOC NO.	PROJECT MODEL :	PD7	APPROVED BY:		DATE:	2011/10/28
	PART NUMBER:		DRAWING BY:		REVISON:	1A

Quanta Computer Inc.

PROJECT : J01

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Model	REV	CHANGE LIST	MODEL	FROM	To
	3A	B2-->C 1. Depopulate related components in the debug LED circuit. 2. Modify power name for discharging ciurcit 3. Modify PD5/PD6 footprint			

DOC NO.	PROJECT MODEL :	PD7	APPROVED BY:		DATE:	2011/10/28
	PART NUMBER:		DRAWING BY:		REVISON:	1A

Quanta Computer Inc.

PROJECT : J01

Size | Document Number: Change History2 | Rev 3A

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