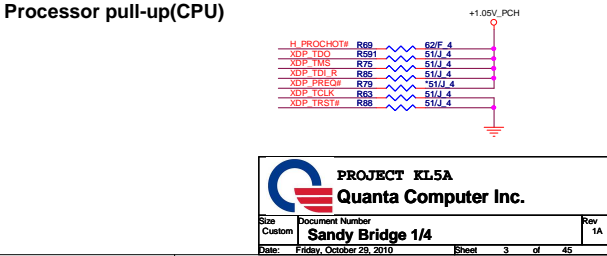
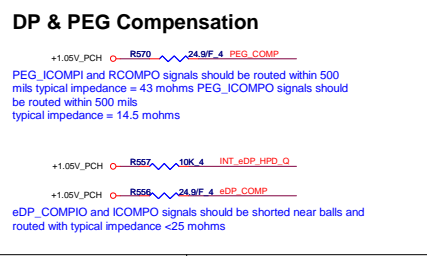
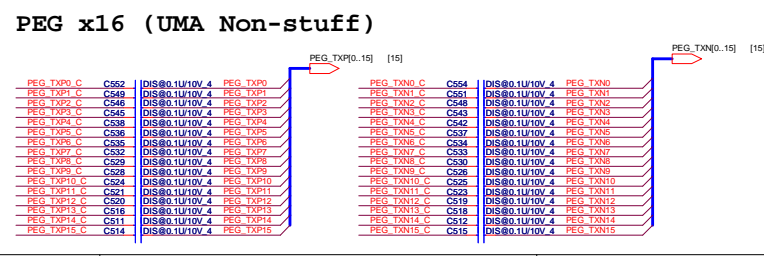
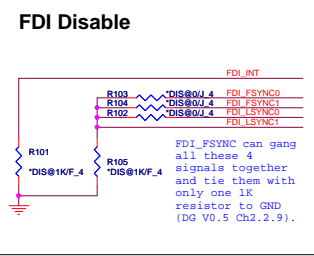
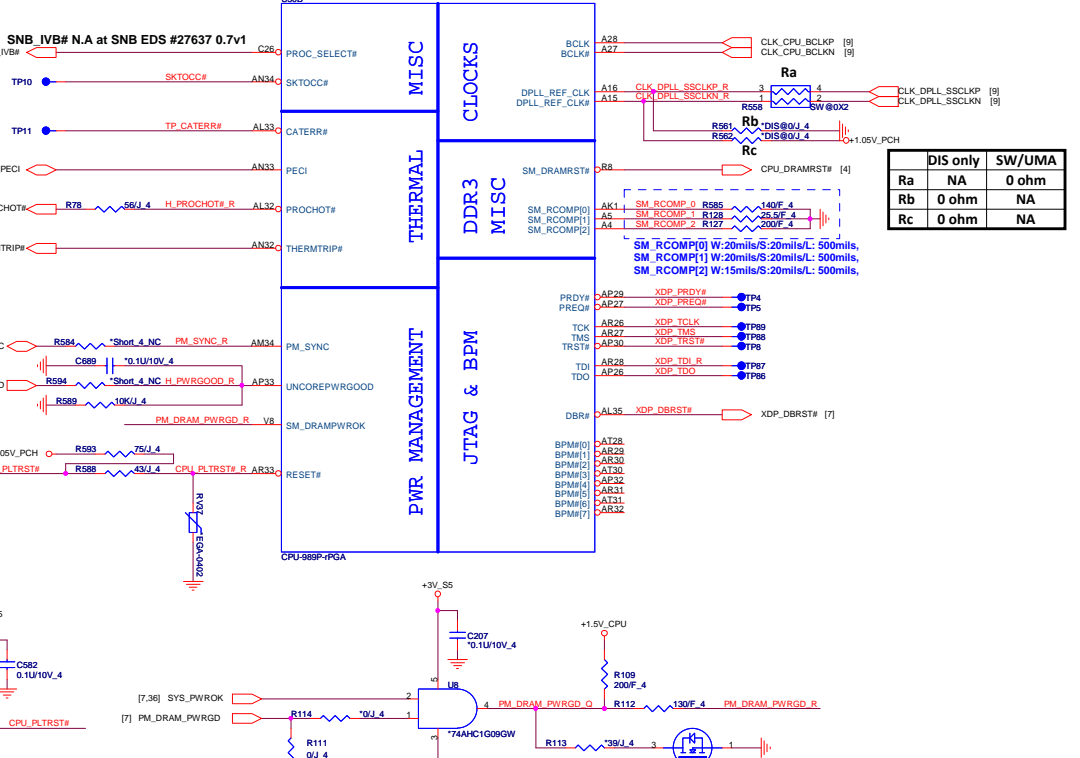
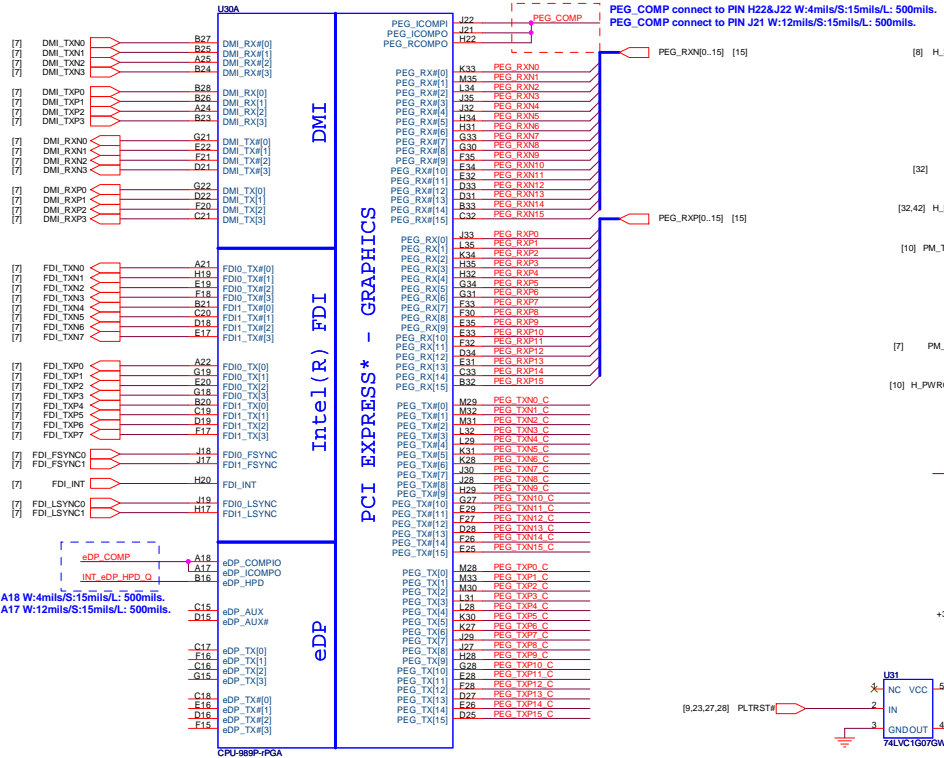


Table of Contents	
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7-12	CougarPoint (PCH)
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20	HDMI CONN
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22	LCD CONN
23	LAN(RTL8111E-VB-GR)
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25	SATA HDD/ESATA/CD-ROM
26	Card Reader (RTS5139)
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30	K/B, T/P
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32	KBC IT8518
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40	+0.85V (OZ8117)
41	+1.05_PCH (OZ8117)
42	IMVP7 2+1 (ISL95831)
43	KL5A Power On Sequence
44	EC Tracking Record A

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,33,35,36,37,39,40,41,42	MAIN POWER		S0-S5
+3V_RTC	+3.0V~+3.3V	07,08,11,12,32	RTC		S0-S5
+3VPCU	+3.3V	07,08,22,23,25,30,31,32,34,35,37,38	ITE8052 POWER	3V5V_EN	S0-S5
+5VPCU	+5V	25,34,35,36,37,38,39,40,41	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	22,25,27,34,36,37,38,41	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	23,34	LAN POWER	LAN_ON	
+5V_S5	+5V	11,22,25,27,28,34	PCH SUS POWER	S5_ON	S0-S3
+3V_S5	+3.3V	03,07,08,09,10,11,27,28,31,32,34	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WIMAX POWER	S5_ON	S0-S3
GFX_CORE	+0.9V~+1.2V	15,34,39	VGA CORE POWER	MAINON	S0
+0.75V_DDR_VTT	+0.75V	5,14,32	DDR3 SODIMM REFERENCE POWER	SYS_PWROK	S0
+5V	+5V	07,08,11,20,21,24,25,29,30,31,32,34,35,42	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	07,08,09,10,11,13,14,15,20,21,22,23,24,25,26,27,28,29,31,32,34,35,39,40,41,42	SLP_S3# CTRLD POWER	MAINON	S0
+1.8V	+1.8V	05,08,11,34,38	LVDS,NVM POWER	MAINON	S0
+1.5V	+1.5V	11,25,27,34	Mini PCIe,Express Card POWER	MAINON	S0
+1.05V_PCH	+1.05V	03,05,07,08,09,11,34,36,41	PCH CORE POWER	MAINON	S0
+VCC_CORE		05,34,42	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	22	LCD Power	INT_LVDS_VDDEN	S0
BAT-V	+10V~+17V	35	MAIN BATTERY	CHG_PBATT	S0-S5

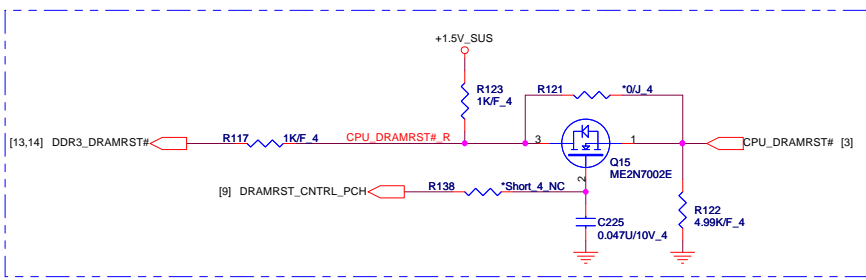
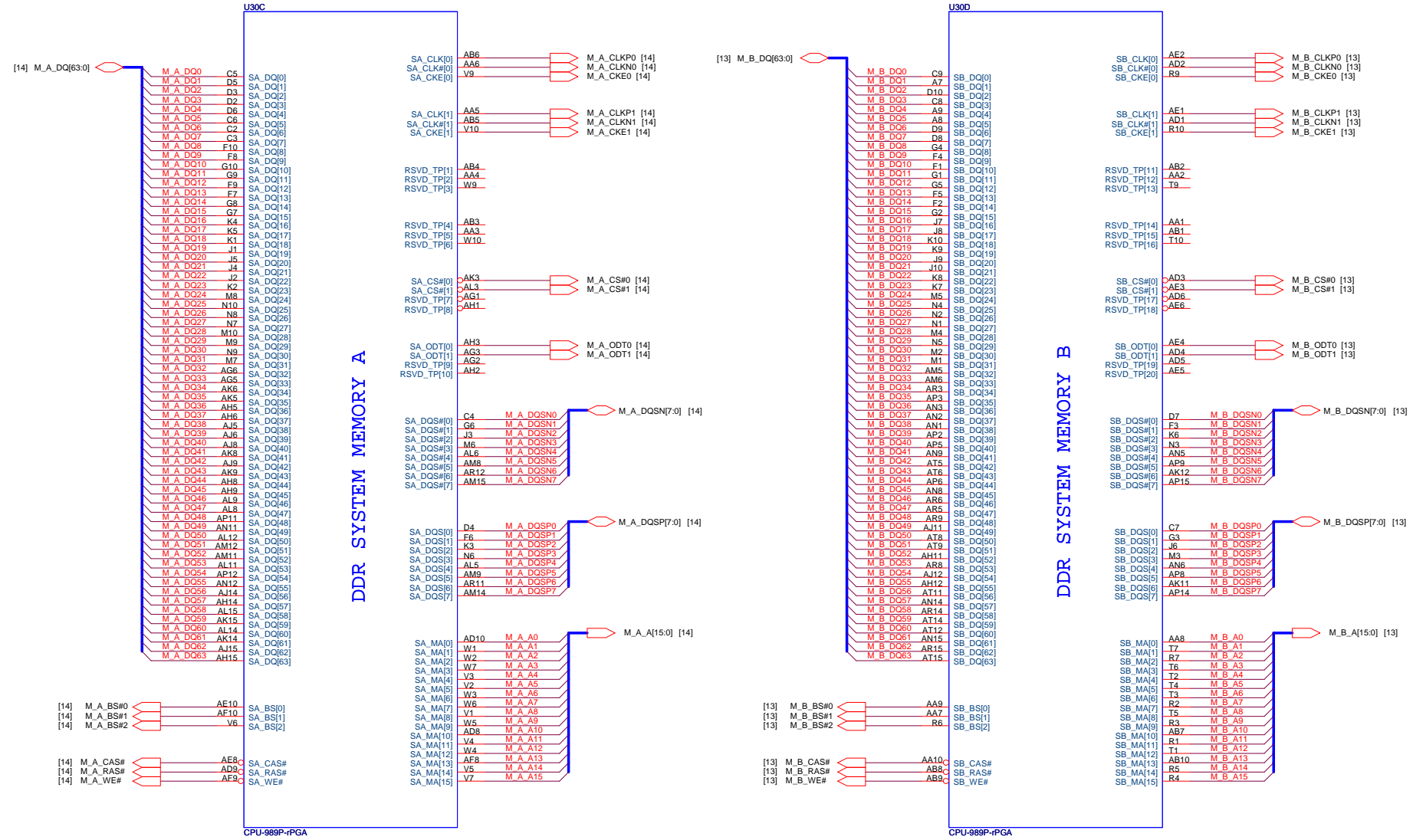
Sandy Bridge Processor (DMI,PEG,FDI)



PROJECT KL5A
Quanta Computer Inc.

Size: Custom Document Number: Sandy Bridge 1/4 Rev: 1A
Date: Friday, October 29, 2010 Sheet: 3 of 45

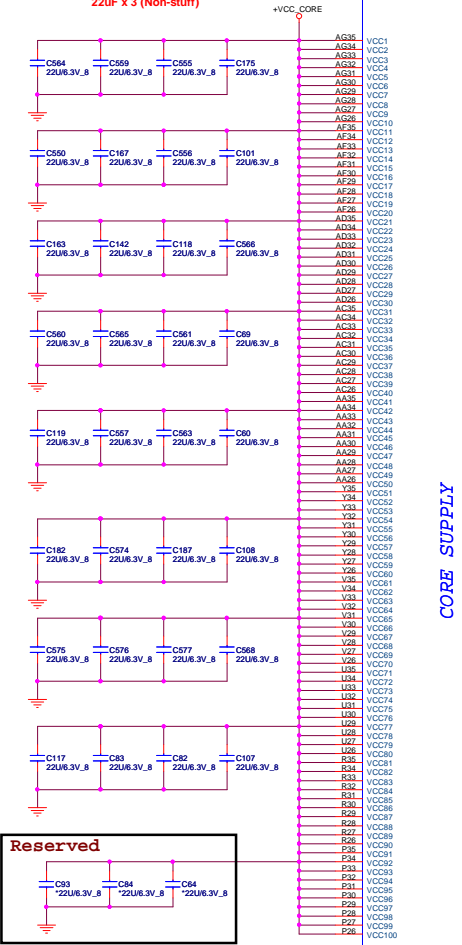
Sandy Bridge Processor (DDR3)



Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A,36A(TDP)
22uF x 32
22uF x 3 (Non-stuff)



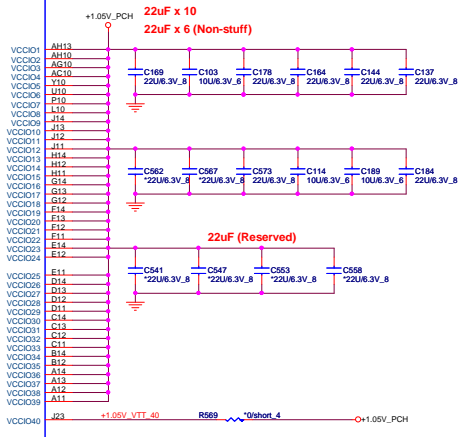
POWER

PEG AND DDR

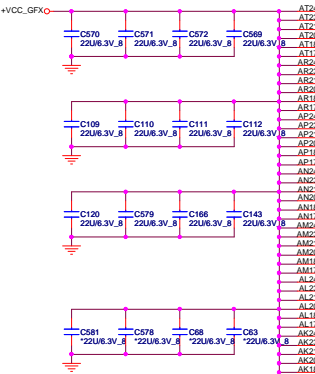
CORE SUPPLY

SENSE LINES

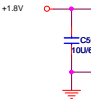
CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)



CPU VGT
SNB 45W:24A
22uF x 12
22uF x 4 (Reserved)



CPU VCCPL
SNB 45W:1.2A
330uF/7mohm x 1
10uF x 1
1uF x 2



POWER

GRAPHICS

1.8V RAIL

MISC

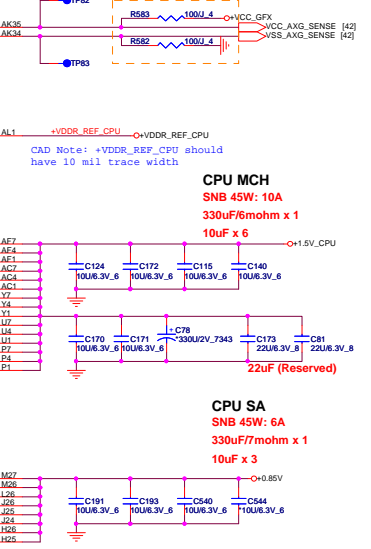
SENSE LINES

VREF

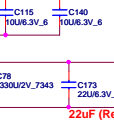
DDR3 - 1.5V RAILS

SA RAIL

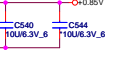
SENSE LINES



CPU MCH
SNB 45W: 10A
330uF/6mohm x 1
10uF x 6



CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

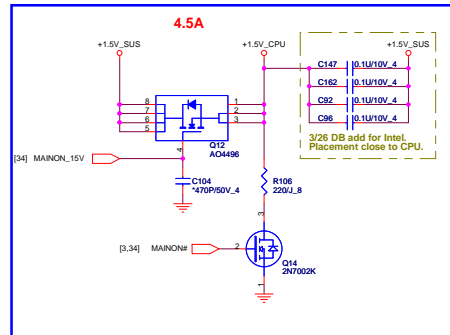


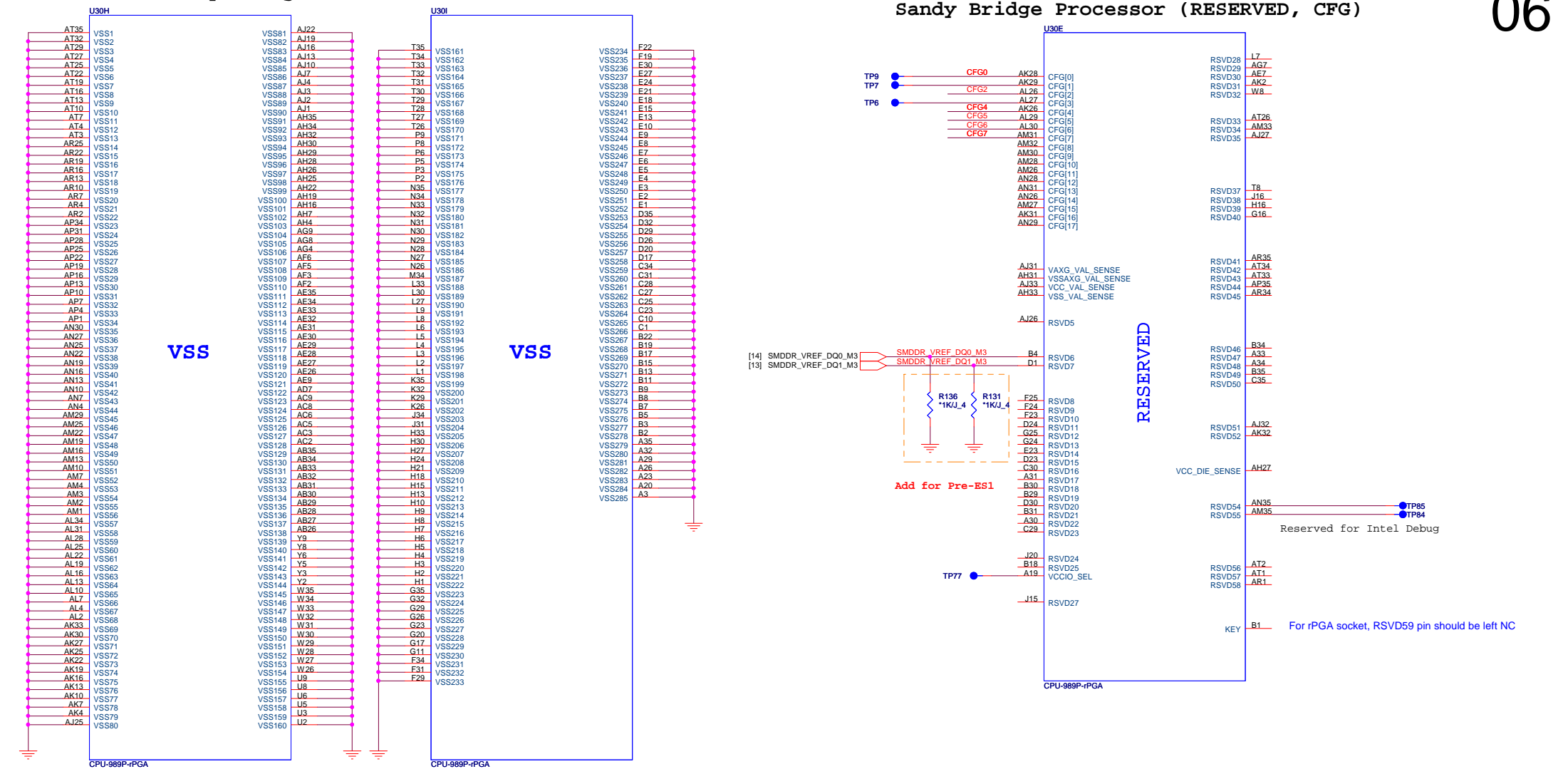
Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
H_CPU_SVIDCLK R83 *Short_4_NC

SVID DATA
Place PU resistor close to CPU
Close to VR
H_CPU_SVIDDATA R74 64.9F_4

SVID ALERT
Place PU resistor close to CPU
Close to VR
H_CPU_SVIDALRT# R80 43u_4





Processor Strapping

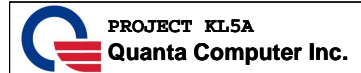
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



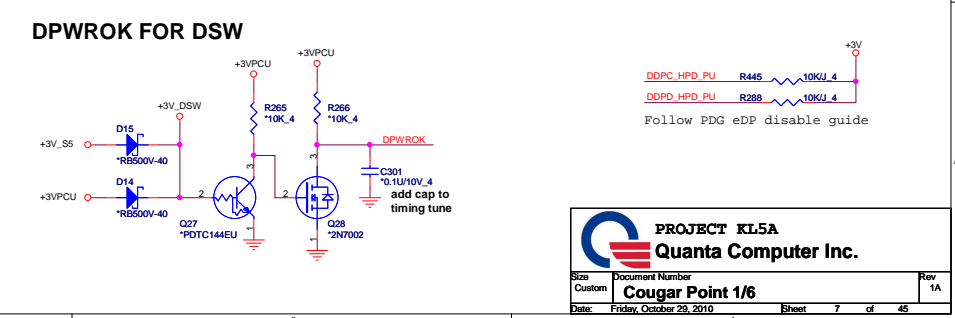
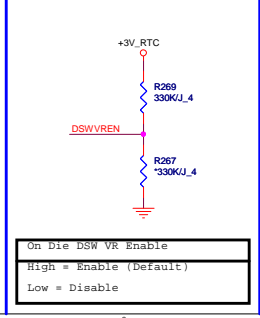
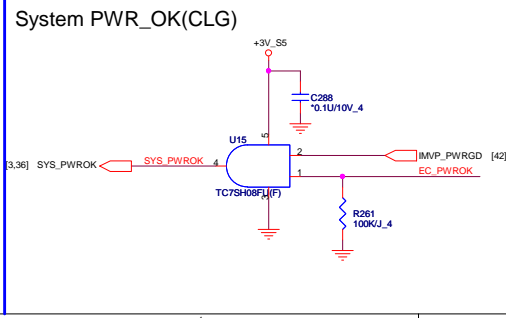
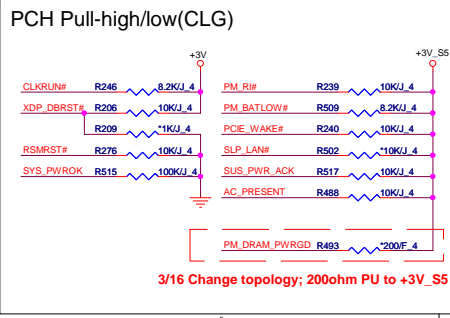
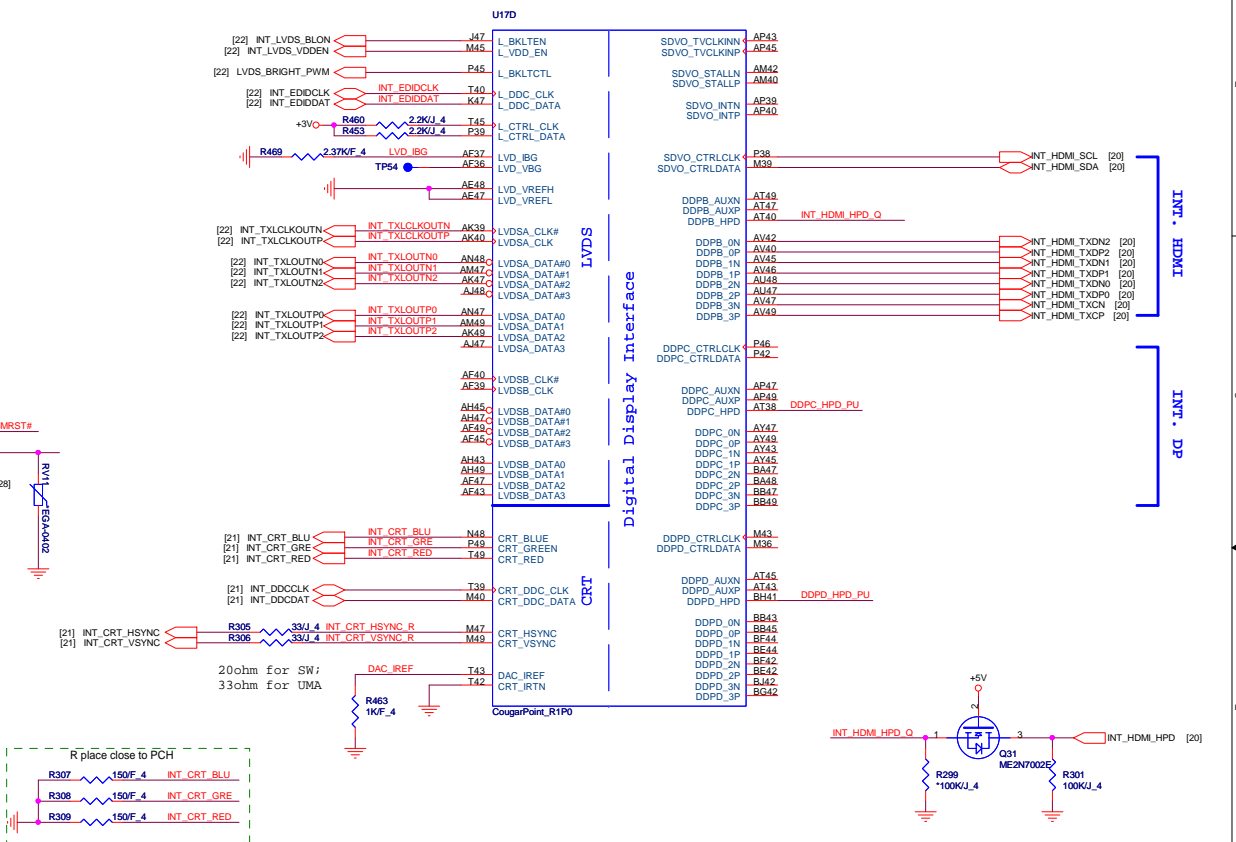
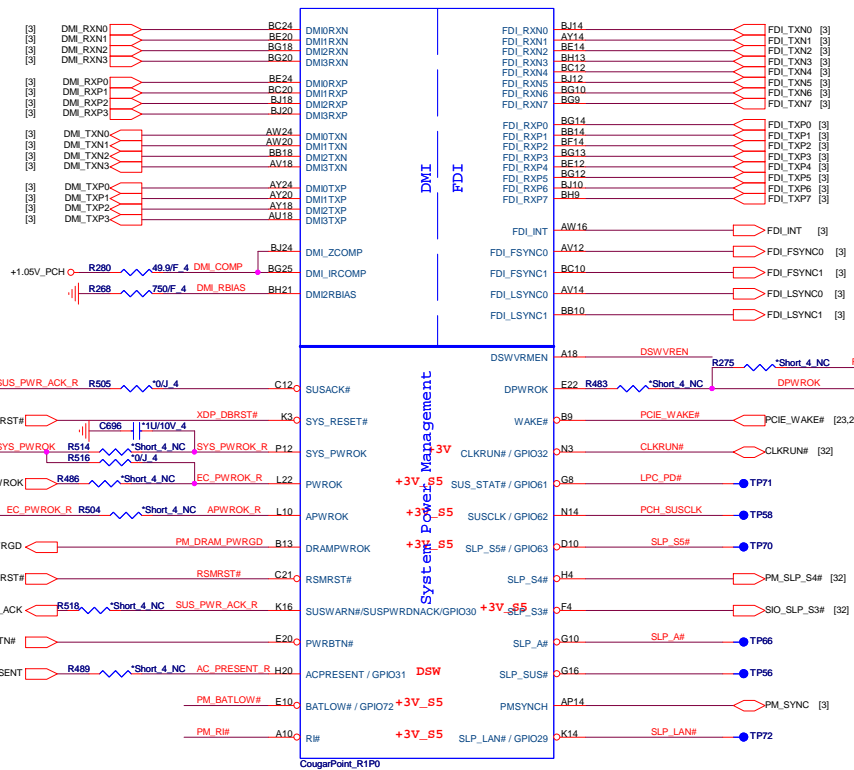
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

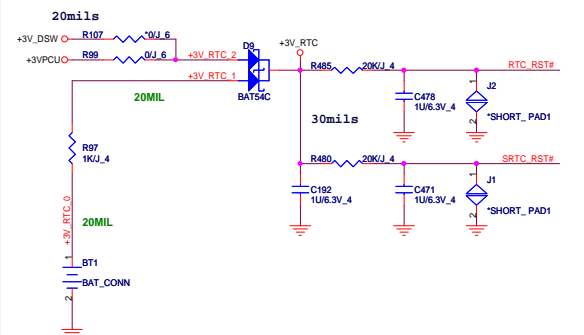


Cougar Point (LVDS,DDI)

Cougar Point (DMI,FDI,PM)

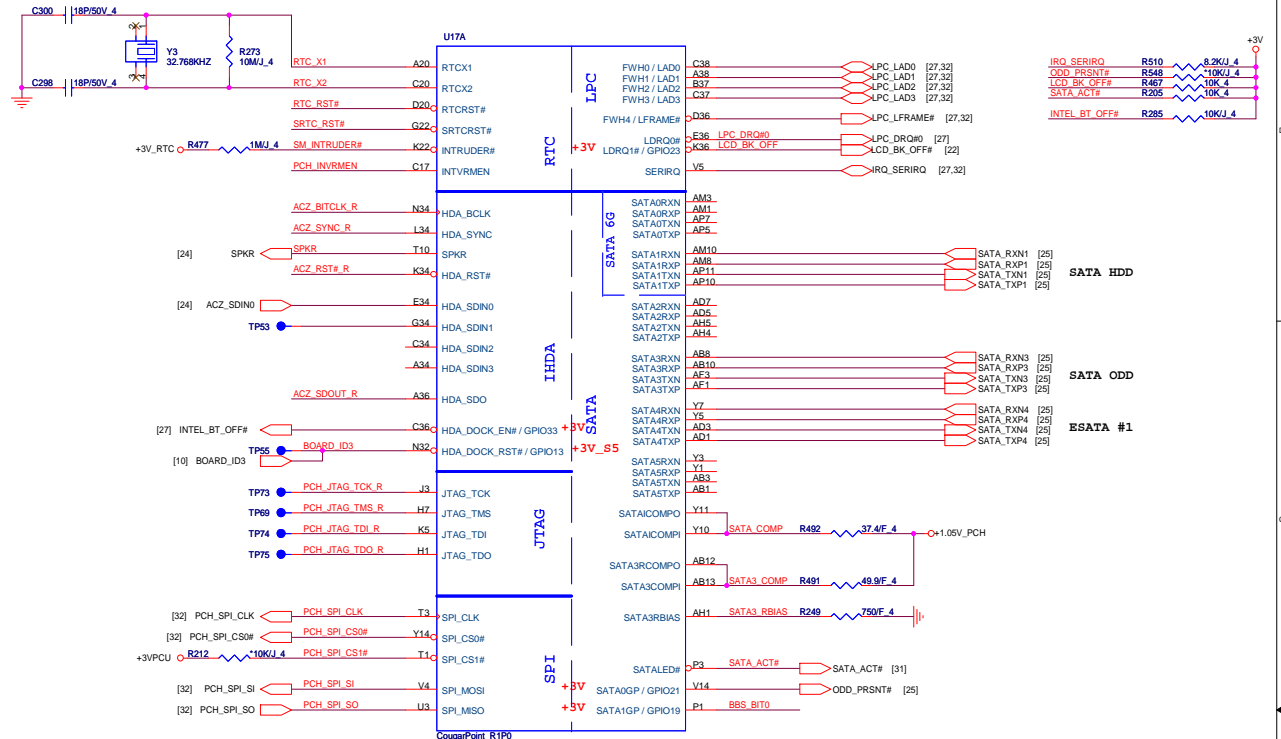


RTC Circuitry(RTC)

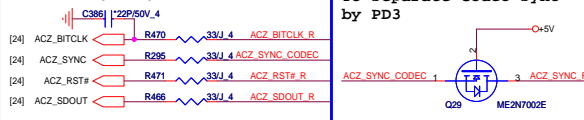


PCH2 (CLG)

Cougar Point (HDA, JTAG, SATA)

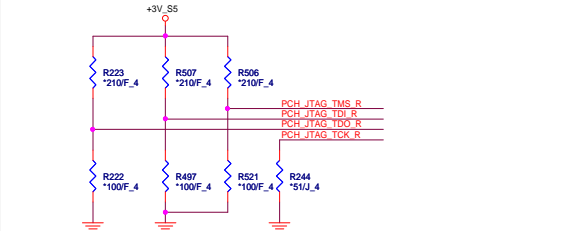


HDA Bus(CLG)



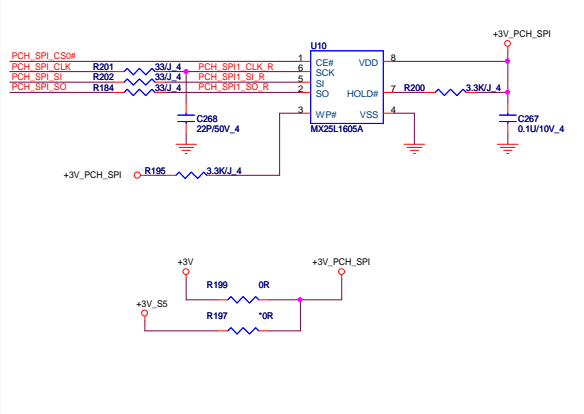
To Separate Codec Sync by PD3

PCH JTAG Debug (CLG)



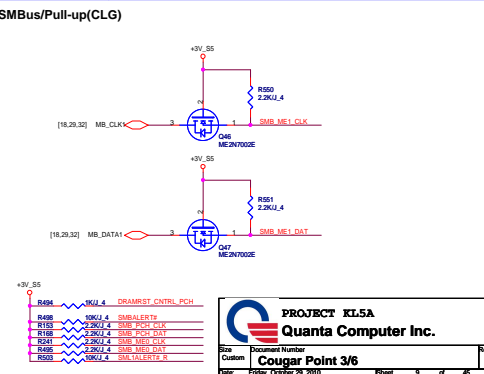
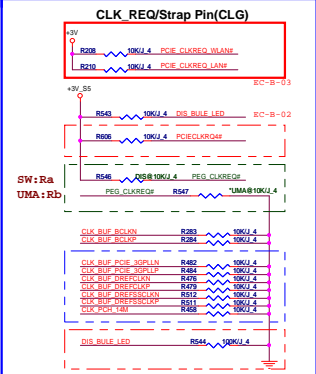
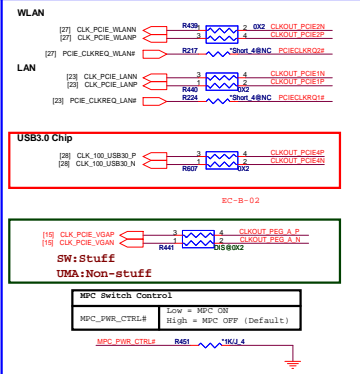
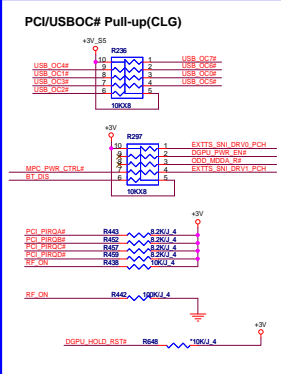
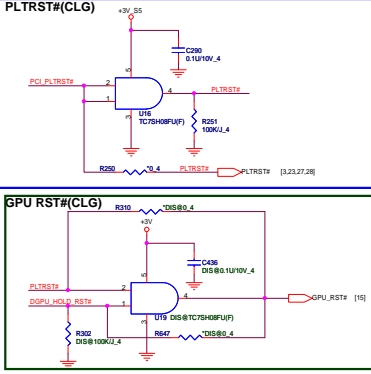
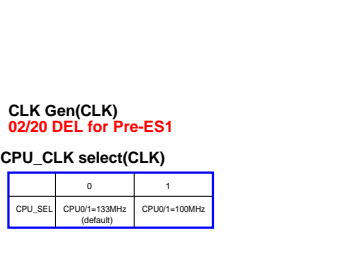
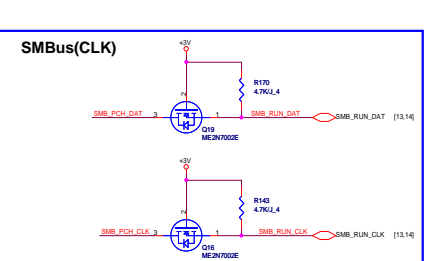
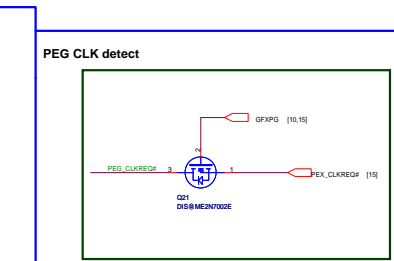
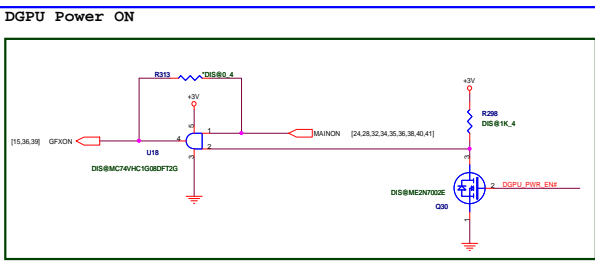
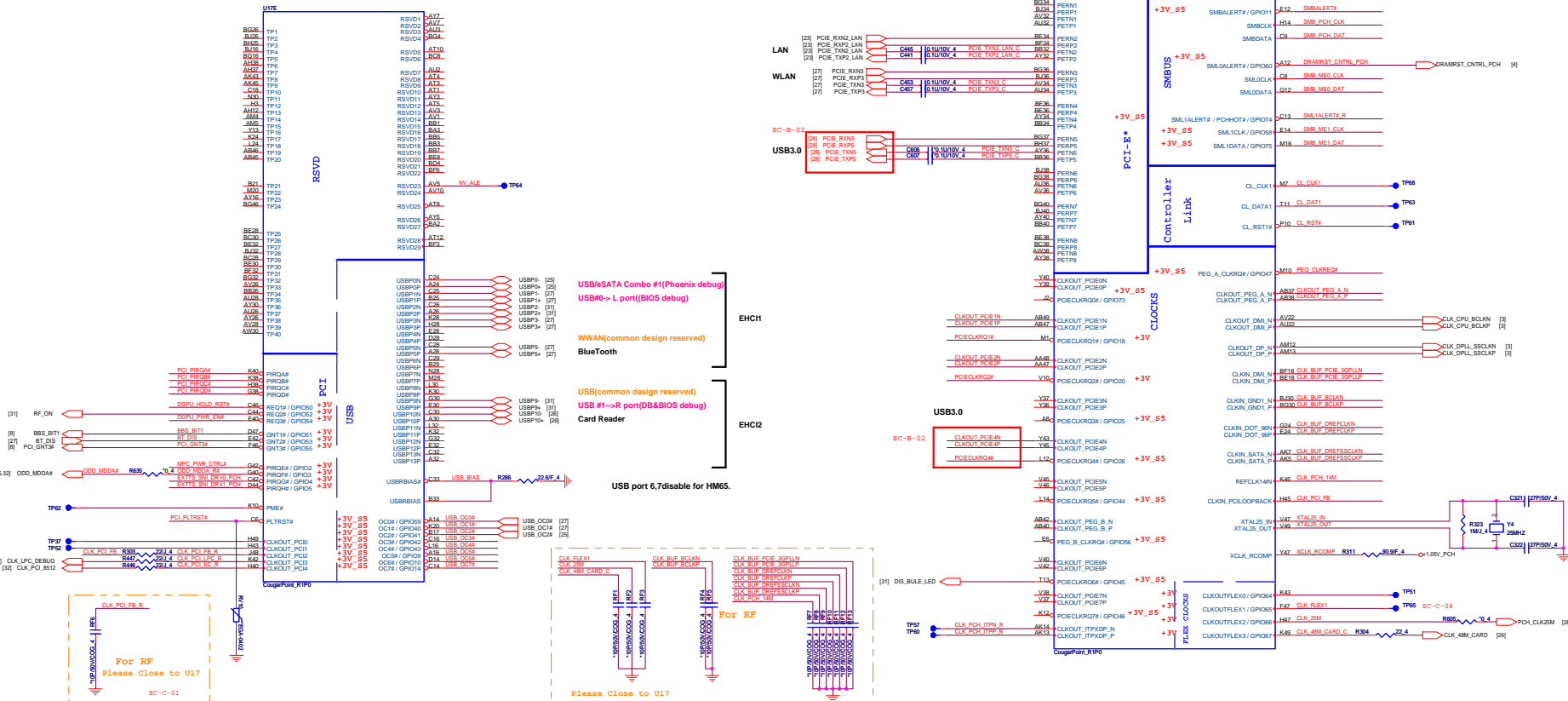
PCH Dual SPI (CLG)

MX25L3205DM2I-12G; AKE39FP0Z00
W25X32VSSIG; AKE39ZP0N00
Socket: DG008000031



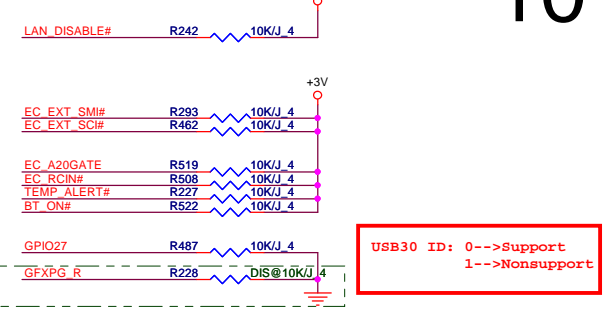
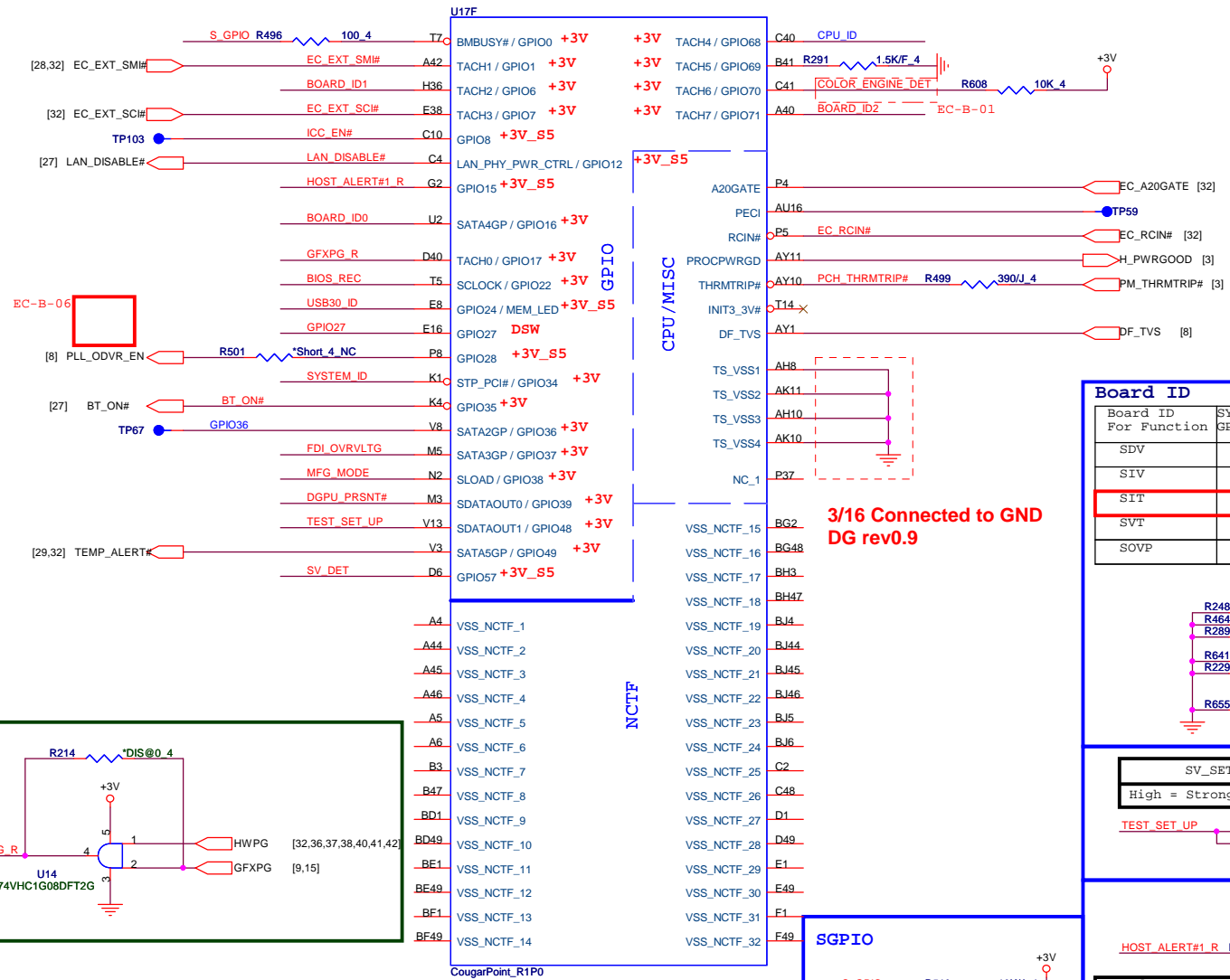
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_0 R529 *1KJ_4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R450 *1KJ_4 PCI_GNT3# [9]									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC_0 R272 330KJ_4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	<p>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</p> R448 *1KJ_4 BBS_BIT1 [9] R247 *1KJ_4 BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5_0 R468 *1KJ_4 ACZ_SDOOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWR0K	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R238 2.2KJ_4 DF_TVS [10] R252 4.7KJ_4 H_SNB_IVB# [9]									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R523 *1KJ_4 PLL_ODVR_EN [10]									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5_0 R296 *1KJ_4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable	+3V_0 R203 *1KJ_4 PCH_SPI_SI									
NV_ALE	Intel Anti-Theft HDD protection	PWR0K	0 = Disable (Internal pull-down 20kohm)										

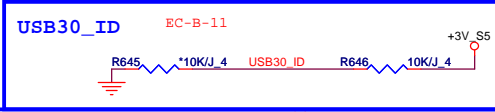


Cougar Point (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down(CLG)



USB30 ID: 0-->Support
1-->Nonsupport



Board ID (EC-B-04, EC-B-11)

Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID1 GPIO6	ID0 GPIO16	ID3 GPIO13
SDV	0	0	0	0	0
SIV	0	0	0	1	0
SIT	0	0	1	0	0
SVT	0	0	1	1	0
SOVP	0	0	0	0	1

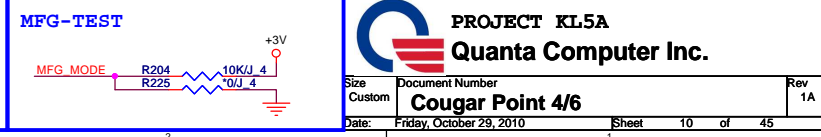
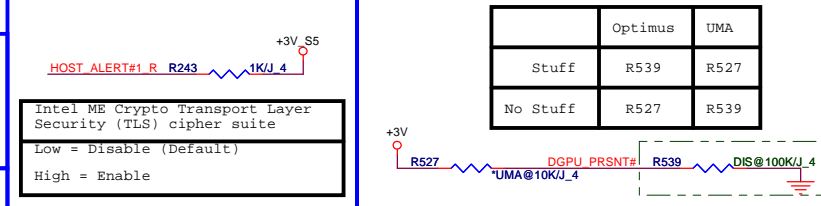
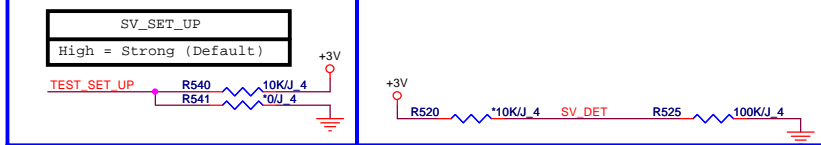
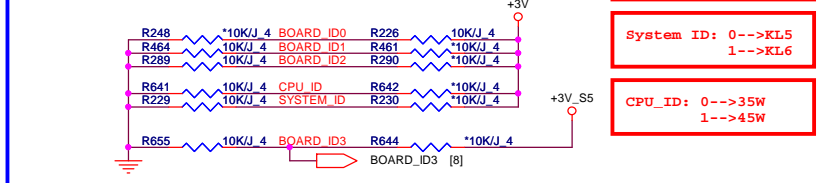
Board ID use below GPIO:

- BOARD_ID0
- BOARD_ID1
- BOARD_ID3

ID2: 0-->6 layer
1-->8 layer

System ID: 0-->KL5
1-->KL6

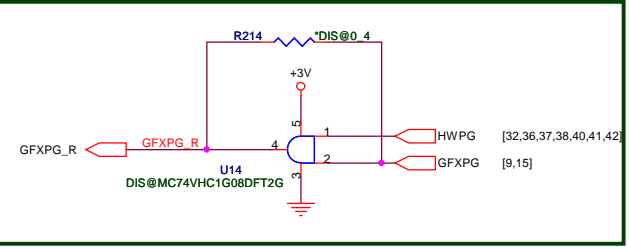
CPU_ID: 0-->35W
1-->45W



PROJECT KL5A
Quanta Computer Inc.

Size Custom Document Number
Cougar Point 4/6

Date: Friday, October 29, 2010 Sheet 10 of 45 Rev 1A



3/16 Connected to GND
DG rev0.9

FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

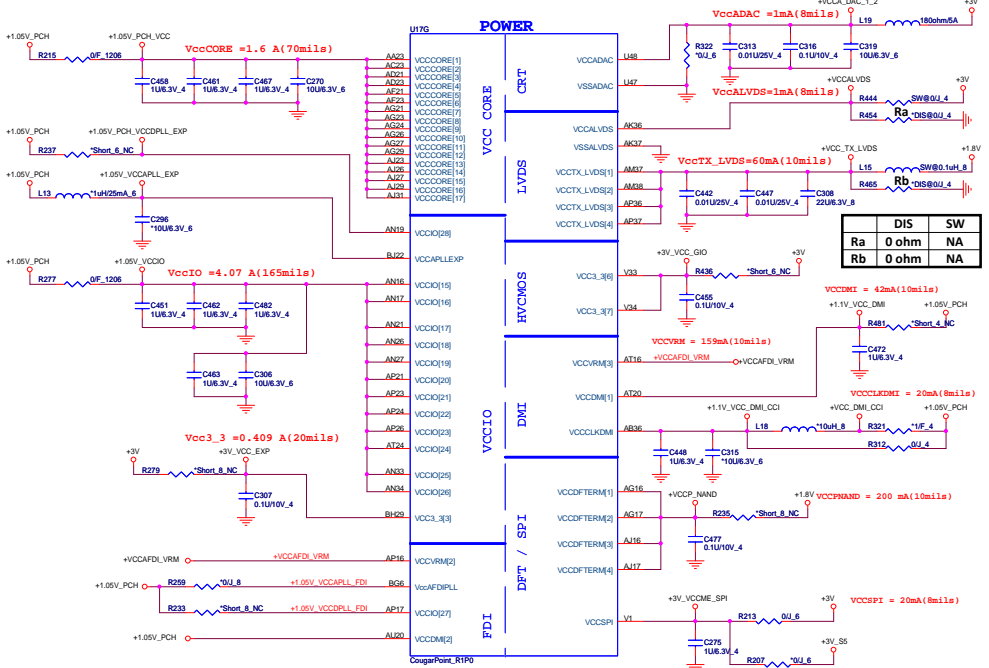
DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY

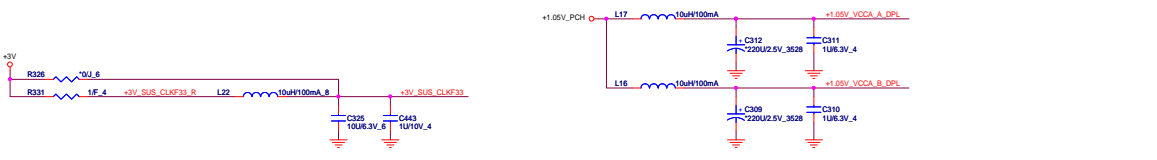
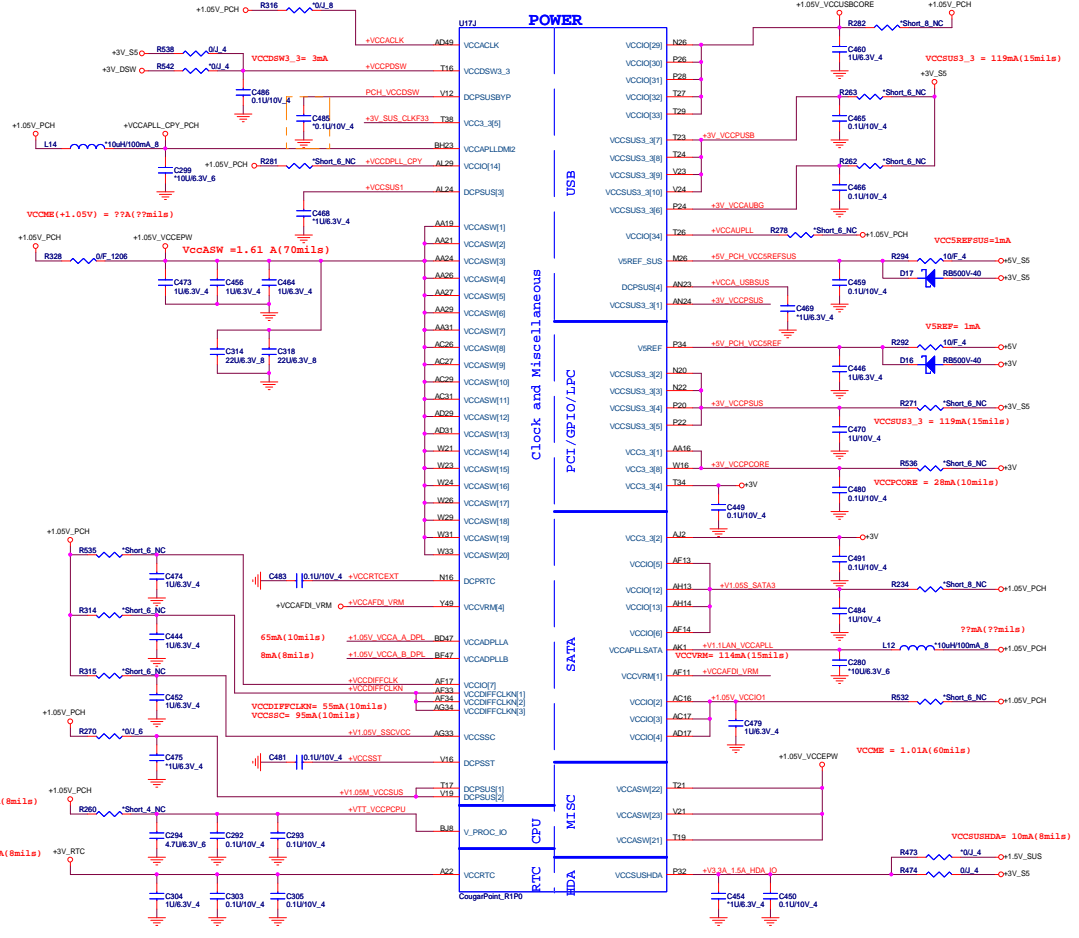
High = Disable (Default)
Low = Enable

COUGAR POINT (POWER)

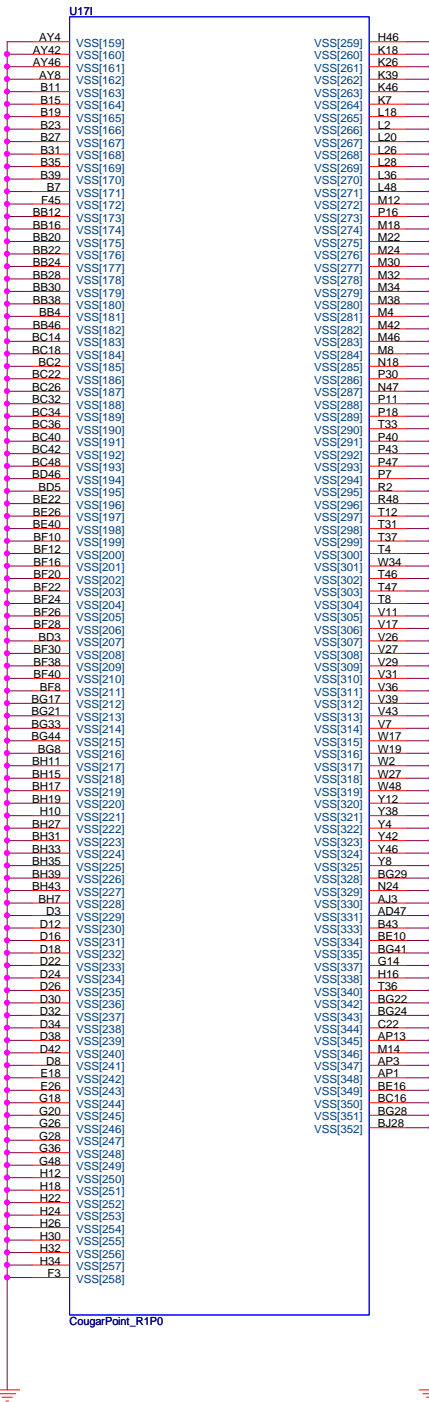
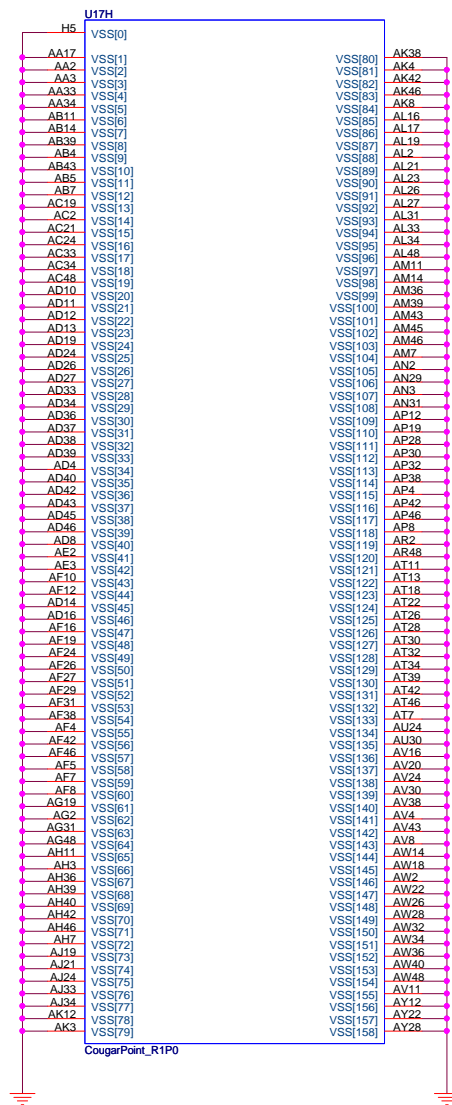


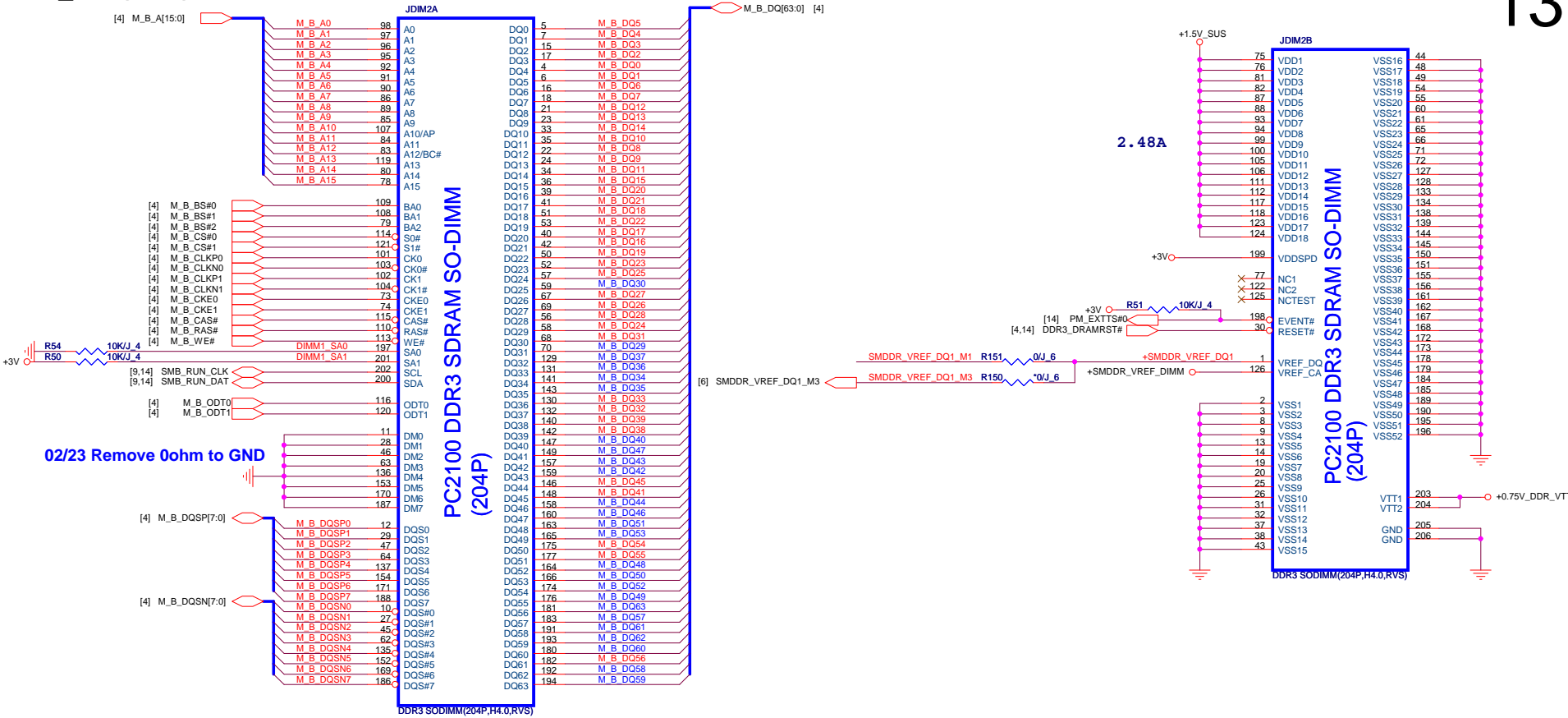
	DIS	SW
Ra	0 ohm	NA
Rb	0 ohm	NA

Cougar Point-M (POWER)



IBEX PEAK-M (GND)



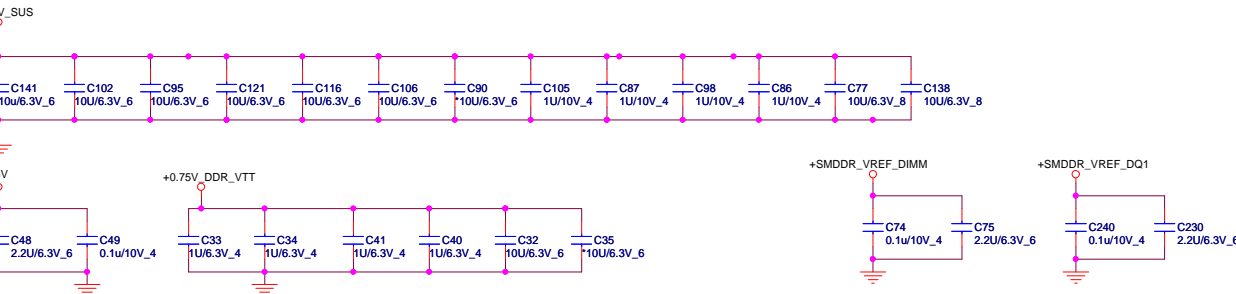


PC2100 DDR3 SDRAM SO-DIMM (204P)

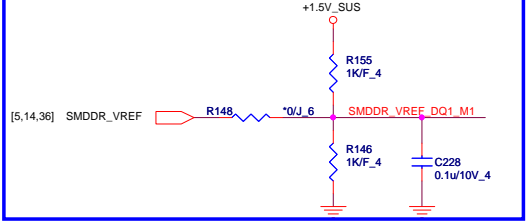
PC2100 DDR3 SDRAM SO-DIMM (204P)

02/23 Remove 0ohm to GND

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



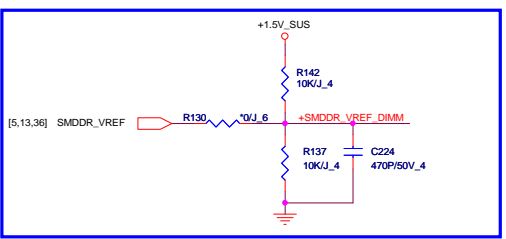
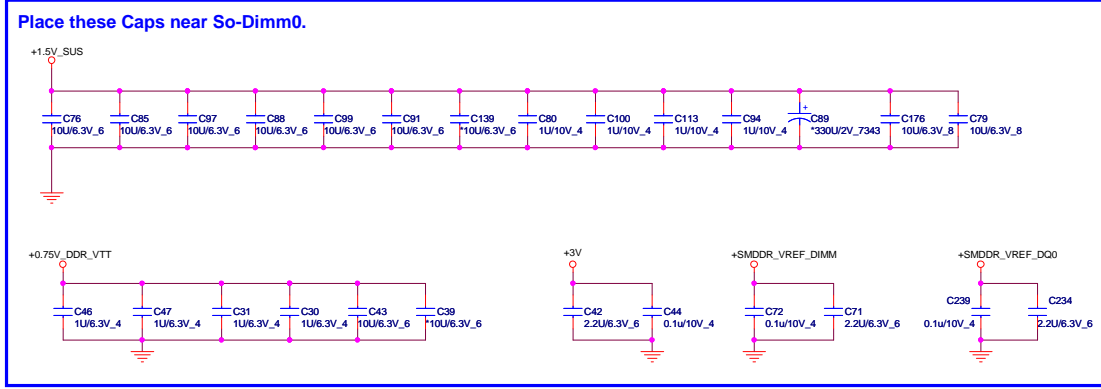
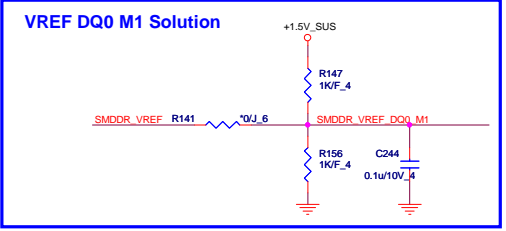
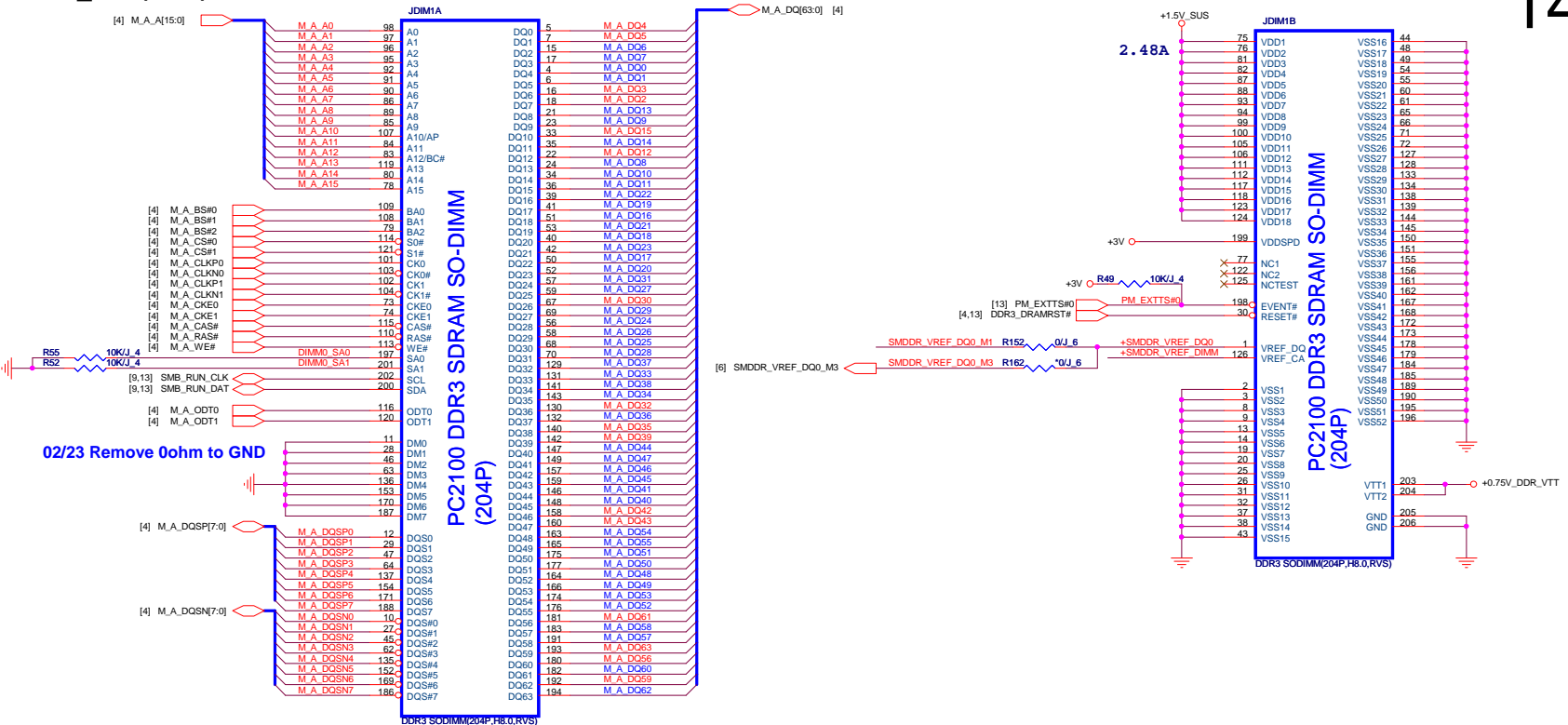
	STD 4H	STD 8H
FOX	DGMK4000090	DGMK4000122
LTK	DGMK4000005	DGMK4000087
SUY	DGMK4000181	DGMK4000182
SKT	DGMK0000120	DGMK4000139

Standard 8H type:DDR-C-2013310-204p-1

PROJECT KL5A
Quanta Computer Inc.

Size: Custom Document Number: **DDRIII SO-DIMM-0** Rev: 1A

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power up sequence

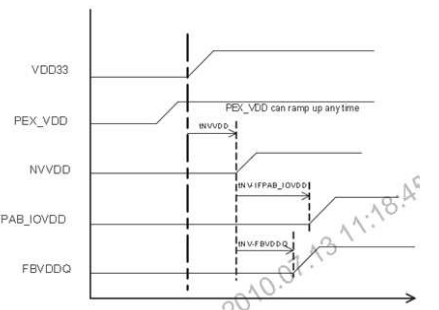
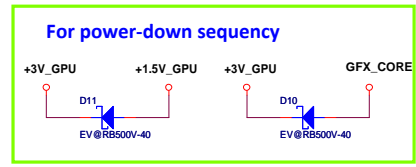
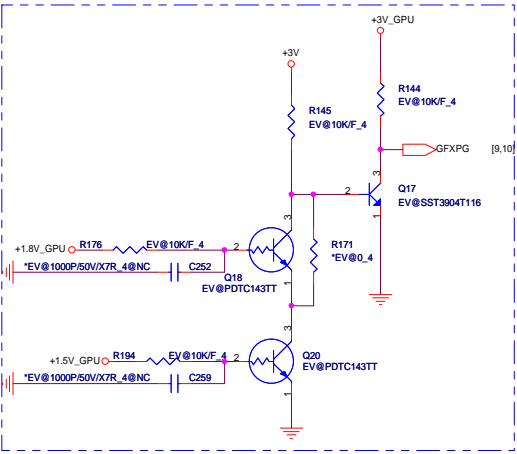
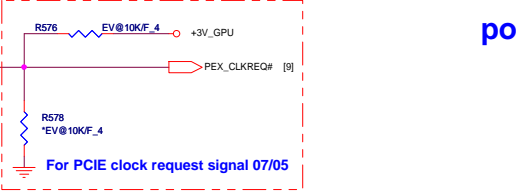
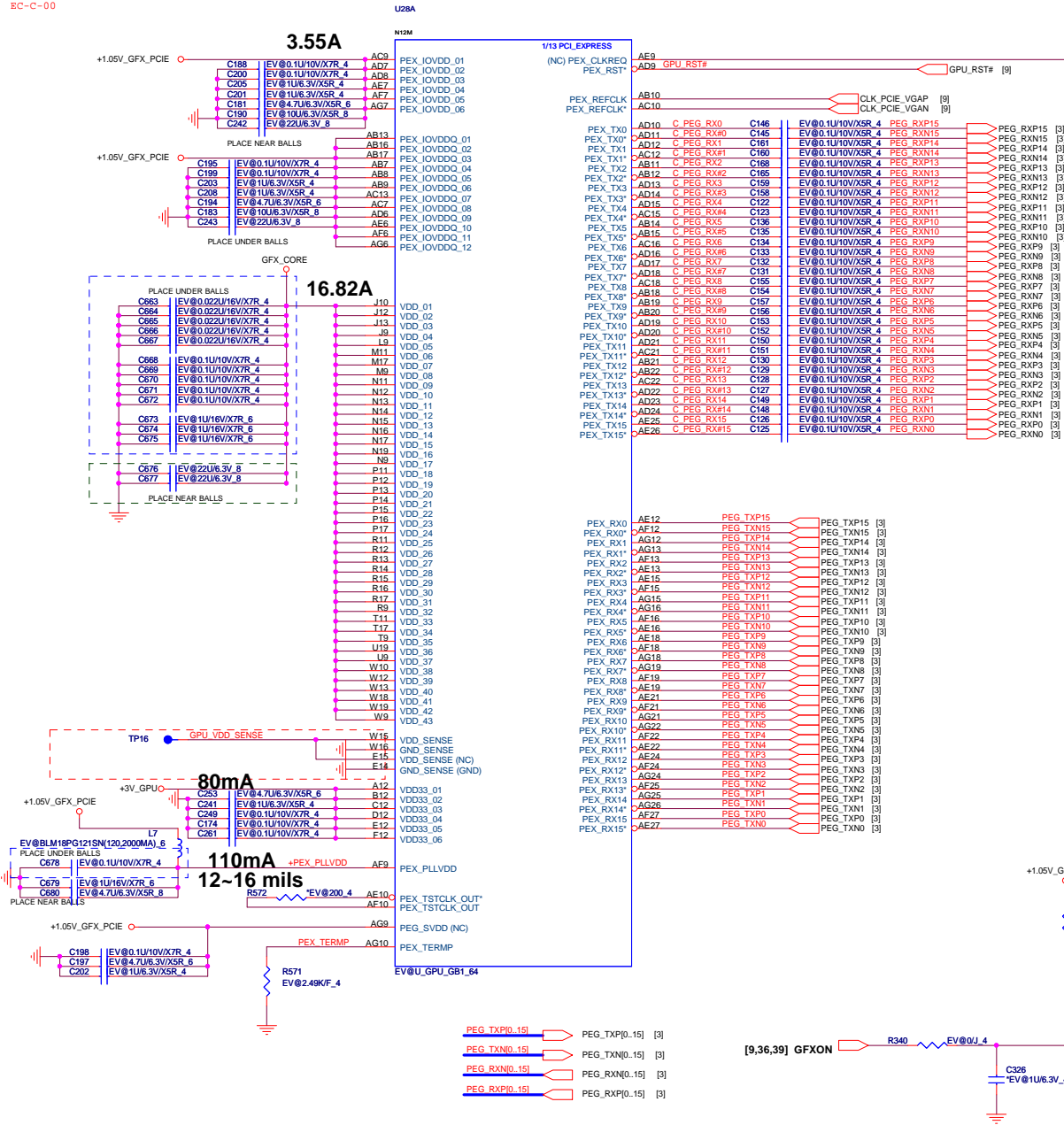
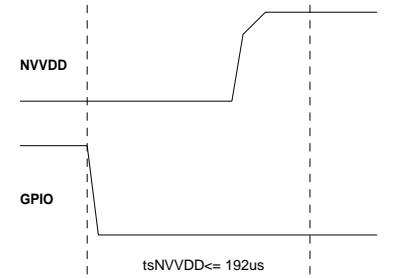


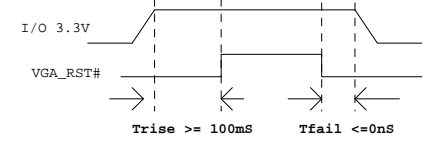
Figure 3.12 Recommended Power Sequencing Order

DGPU_PWR_EN# = GFXON >> +1.05_GFX_PCIE
 >> +3V_GPU_EN >> +3V_GPU
 >> NVVDD = NVVDD_PG
 >> +1.5_GPU >> +1.8V_GPU

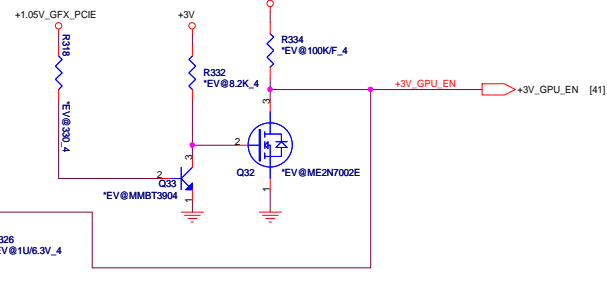
NVVDD Maximum Settling Time



PEX_RST timing



The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:
 ▶ NVVDD <= VDD33+0.5V
 ▶ FBVDDQ <= VDD33+0.5V



- PEG_TXP0[0..15] PEG_TXP0[0..15] [3]
- PEG_TXN0[0..15] PEG_TXN0[0..15] [3]
- PEG_RXN0[0..15] PEG_RXN0[0..15] [3]
- PEG_RXP0[0..15] PEG_RXP0[0..15] [3]

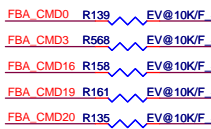
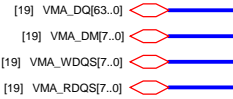
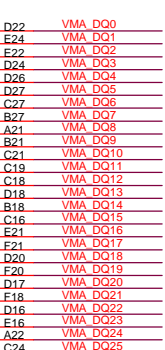
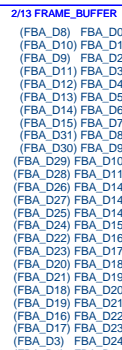
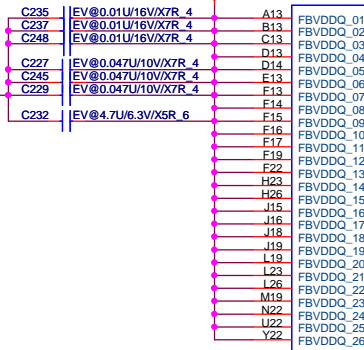
[9,36,39] GFXON

EC-C-00

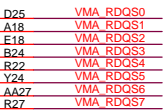
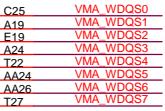
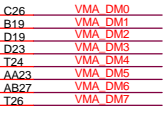
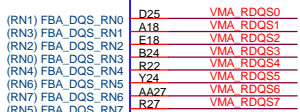
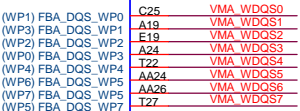
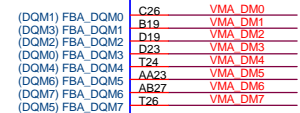
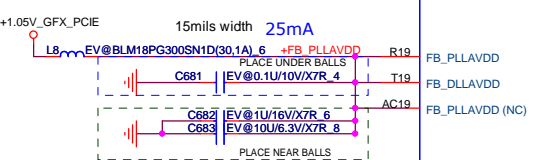
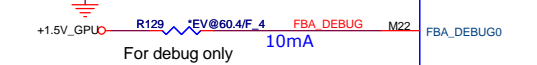
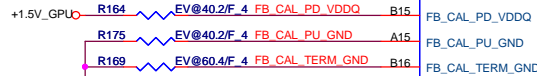
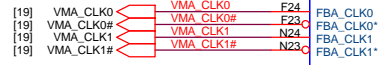
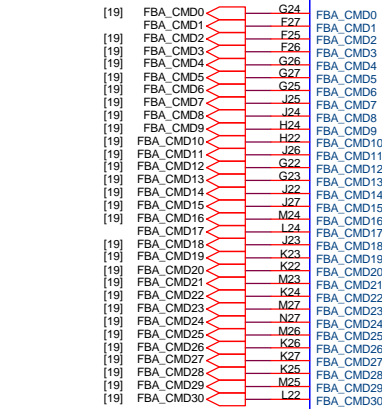
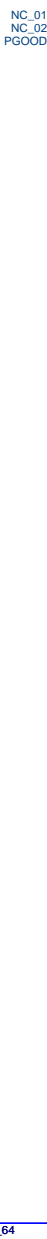
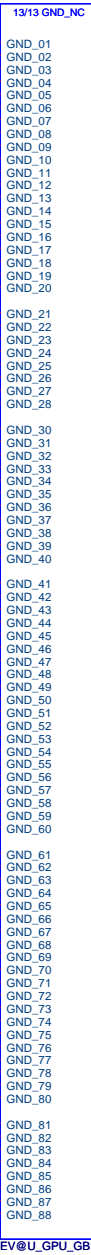
2.63A

+1.5V_GPU

U28B N12M



U28B N12M



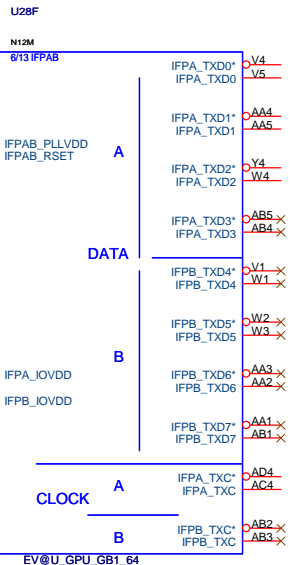
EV@U_GPU_GB1_64

EV@U_GPU_GB1_64

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Quanta Computer Inc.

Size: Custom Document Number: **N12M(MEMORY I/F & GND) 2/5** Rev: 1A

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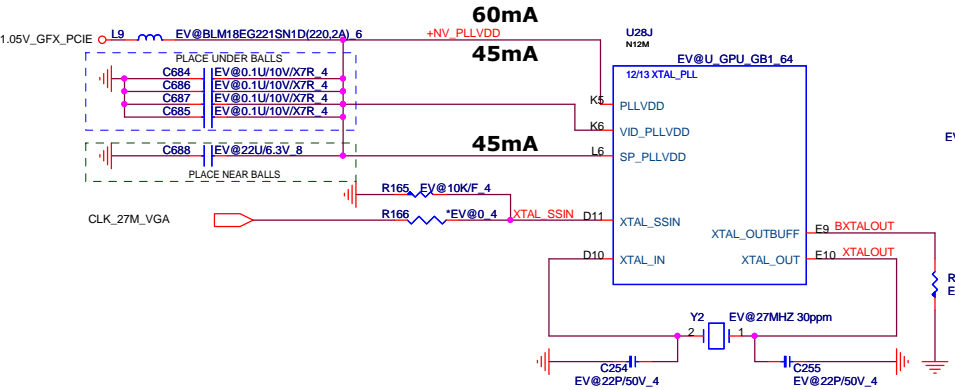
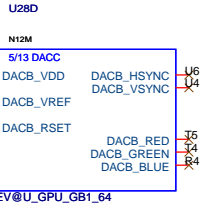
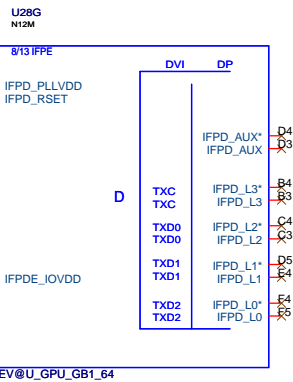
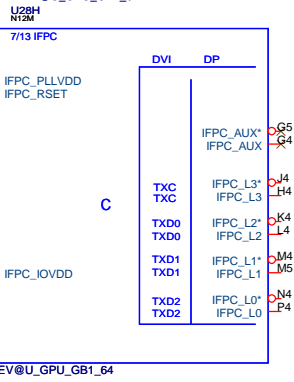


220 mA (1.05V +/- 3%)

220 mA (1.8V)

220 mA

285 mA (1.05V +/- 3%)



STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS Install it when not connected to Spread spectrum device

The following guidelines only apply to a fully unused IFP macro:

- ▶ Pull down IFPxy_IOVDD with 10 kΩ resistor
- ▶ Pull down IFPxy_PLLVDD with 10 kΩ resistor
- ▶ The other IO pins can be NC
- ▶ It is also recommended that footprints for both a 10 kΩ resistor to ground and a 10 kΩ resistor to power be implemented as stuffing options to allow for flexibility in design options

The circuit shown in Figure 6.12 shows the connection for an unused IFP macro.

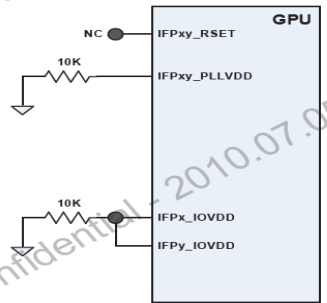
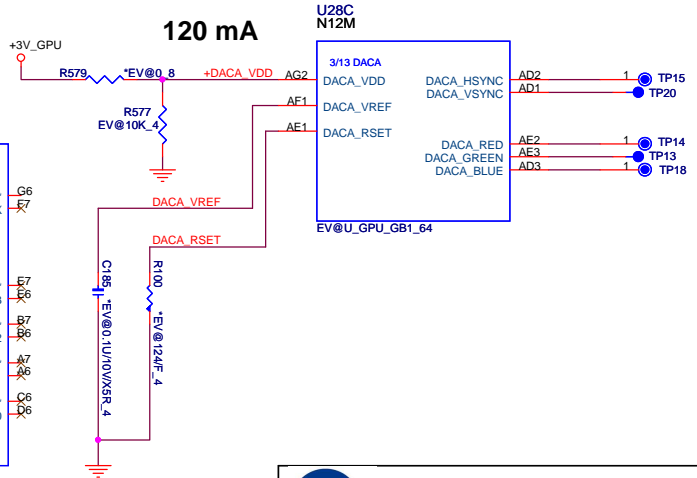


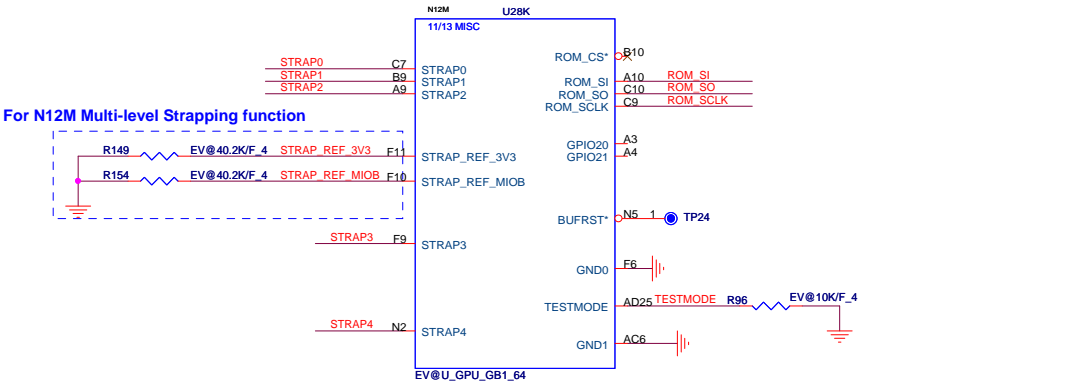
Figure 6.12 Unused IFP Interface

7.4 Unused DAC Interface

To disable a DAC interface:

- ▶ Pull down the DACx_VDD with a 10 kΩ resistor
- ▶ The other DAC IO pins (including DACx_VREF, DACx_RSET) can be NC

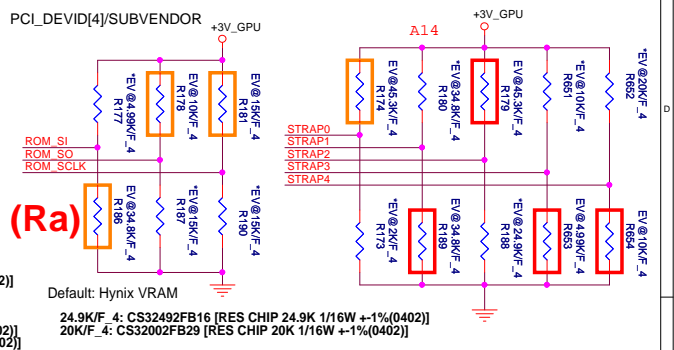




N12M-GS

Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

nV FAB suggest that the device ID for N12M-GS-S is 0x1054.-0909

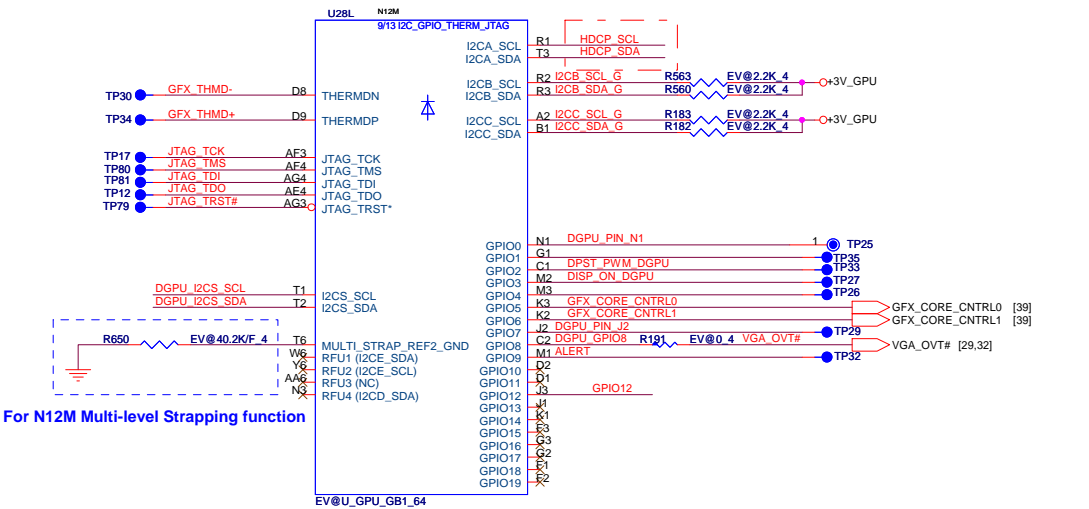


4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
 30K/F 4: CS33002FB13 [RES CHIP 30K 1/16W +1%(0402)]
 34.8K/F 4: CS33482FB22 [RES CHIP 34.8K 1/16W +1%(0402)]
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

Default: Hynix VRAM
 24.9K/F 4: CS32492FB16 [RES CHIP 24.9K 1/16W +1%(0402)]
 20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]

9.5 Unused I2C Pins

For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors, routing.



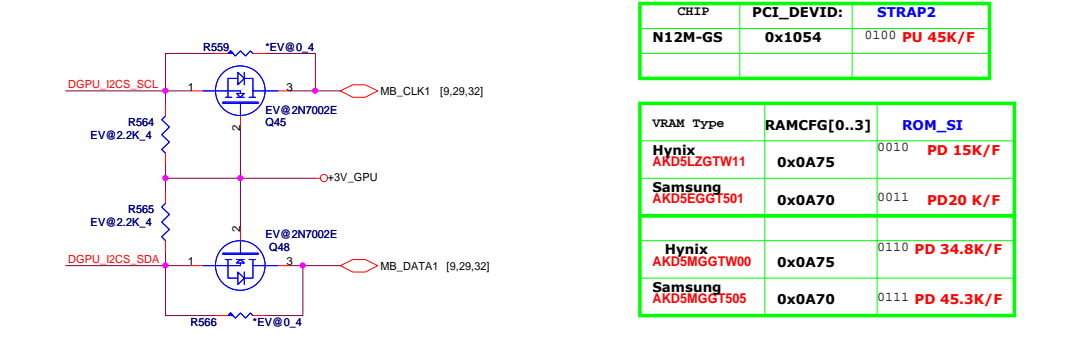
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	N12M-GS FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

(Ra)	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
	0001				
	0010	DDR3 64Mx16x4, 128bit, 512MB,800MHz	Hynix	H5TQ1G63DFR-12C	PD 15K/F
	0011	DDR3 64Mx16x4, 128bit, 512MB,800MHz	Samsung	K4W1G1646G-BC12	PD 20K/F
	0101		Reserved		
	0110				
	0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix	H5TQ2G63BFR-12C	PD 34.8K/F
	0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung	K4W2G1646G-HC12	PD 45.3K/F

GPIO ASSIGNMENTS

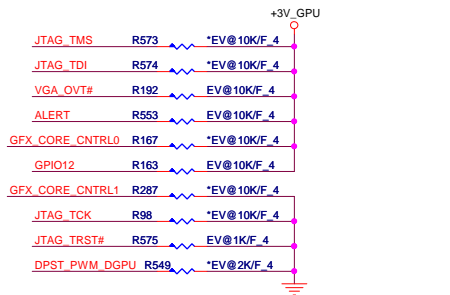
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP



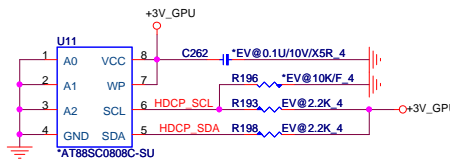
CHIP	PCI_DEVID:	STRAP2
N12M-GS	0x1054	0100 PU 45K/F

VRAM Type	RAMCFG[0..3]	ROM_SI
Hynix AKD5LZGTW11	0x0A75	0010 PD 15K/F
Samsung AKD5EGGT501	0x0A70	0011 PD 20 K/F
Hynix AKD5MGGTW00	0x0A75	0110 PD 34.8K/F
Samsung AKD5MGGT505	0x0A70	0111 PD 45.3K/F

GPU Type	STRAP0	STRAP1	STRAP3	STRAP4	ROM_SO	ROM_SCLK
N12M-GS	PU 45.3K/F	PD 34.8K/F	PD 4.99K/F	PD 20K/F	PU 10K/F	PU 15K/F



HDCP ROM

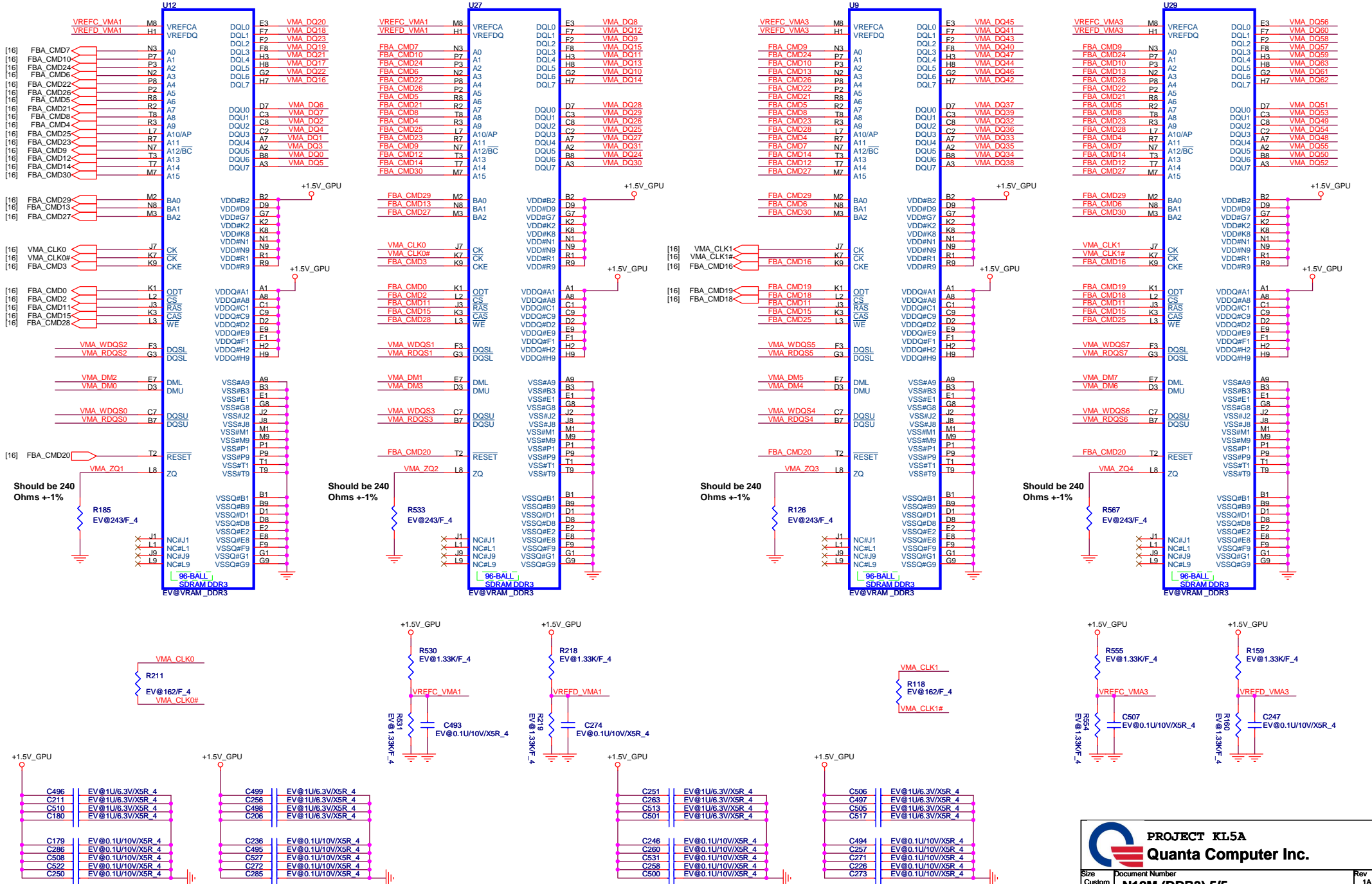


DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

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 Quanta Computer Inc.
 Size Custom Document Number
N12M(GPIO & STRAPS) 4/5
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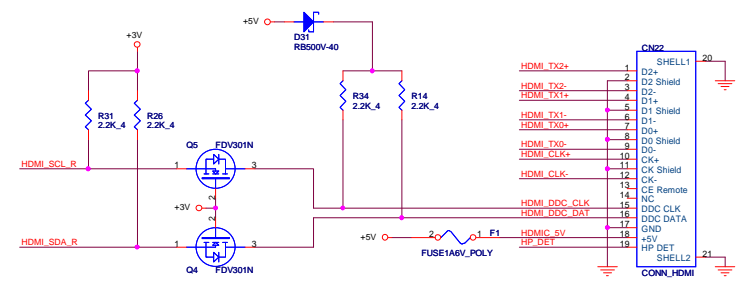
[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

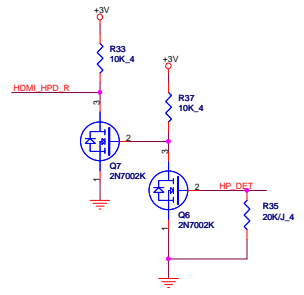


PROJECT KI.5A
Quanta Computer Inc.

Size: Custom Document Number: **N12M (DDR3) 5/5** Rev: 1A
 Date: Friday, October 29, 2010 Sheet: 19 of 45

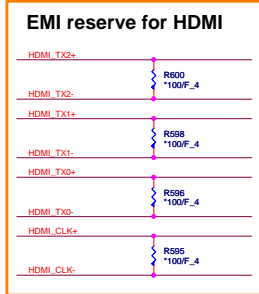
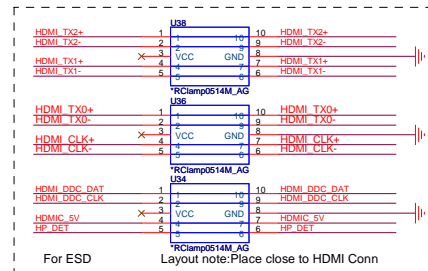
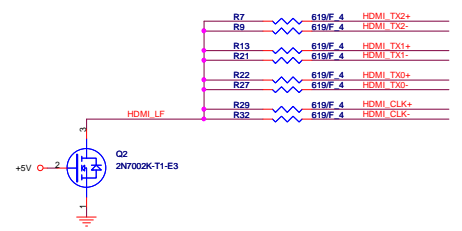
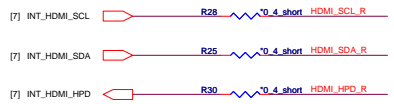


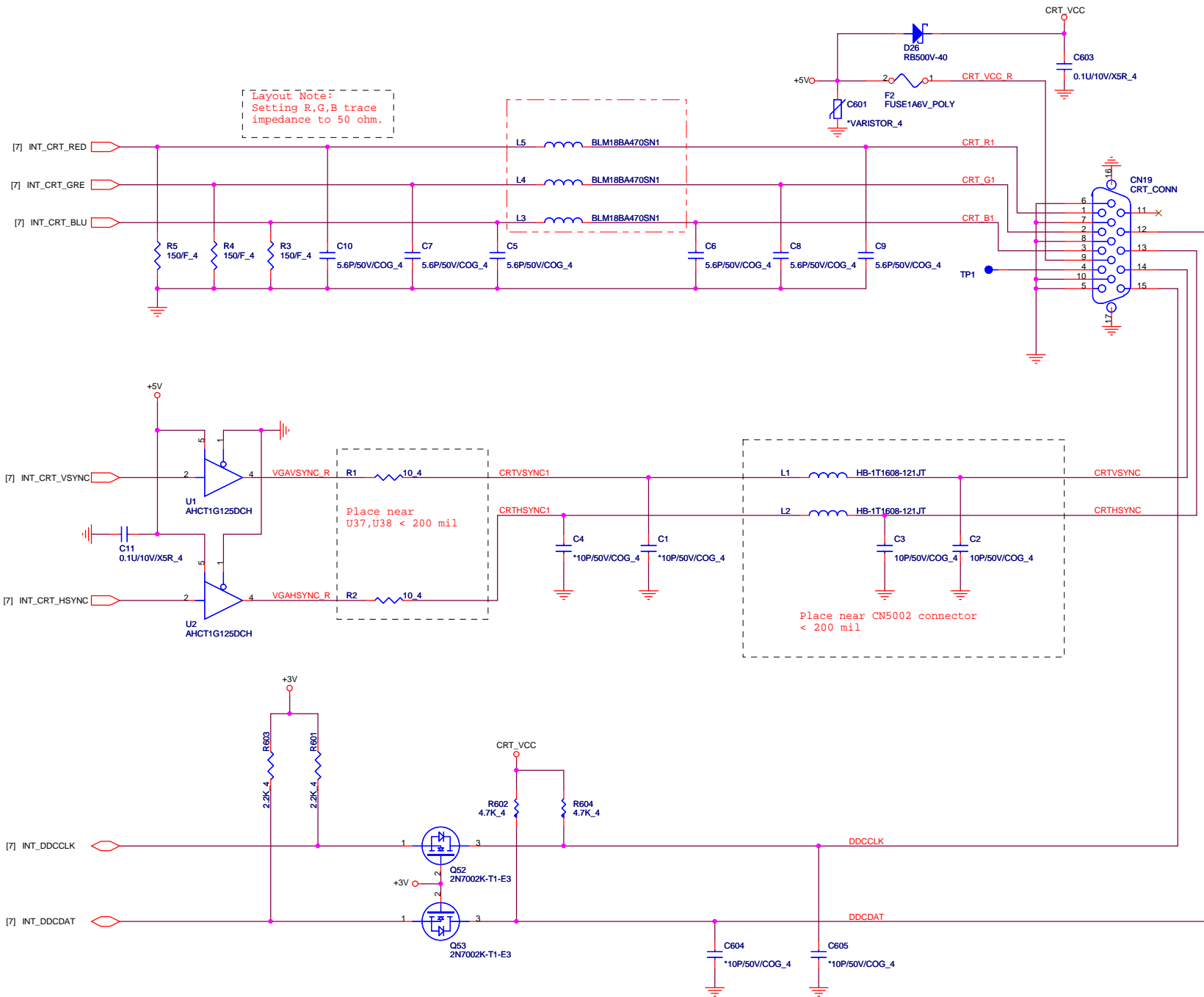
HDMI Hot-PLUG to EC and GPU



UMA Only / HDMI

[7] INT_HDMI_TXDP2	C502	0.1u/10V/X5R_4	HDMI_TX2+
[7] INT_HDMI_TXDN2	C598	0.1u/10V/X5R_4	HDMI_TX2-
[7] INT_HDMI_TXDP1	C597	0.1u/10V/X5R_4	HDMI_TX1+
[7] INT_HDMI_TXDN1	C594	0.1u/10V/X5R_4	HDMI_TX1-
[7] INT_HDMI_TXDP0	C590	0.1u/10V/X5R_4	HDMI_TX0+
[7] INT_HDMI_TXDN0	C588	0.1u/10V/X5R_4	HDMI_TX0-
[7] INT_HDMI_TXCP	C587	0.1u/10V/X5R_4	HDMI_CLK+
[7] INT_HDMI_TXCN	C586	0.1u/10V/X5R_4	HDMI_CLK-

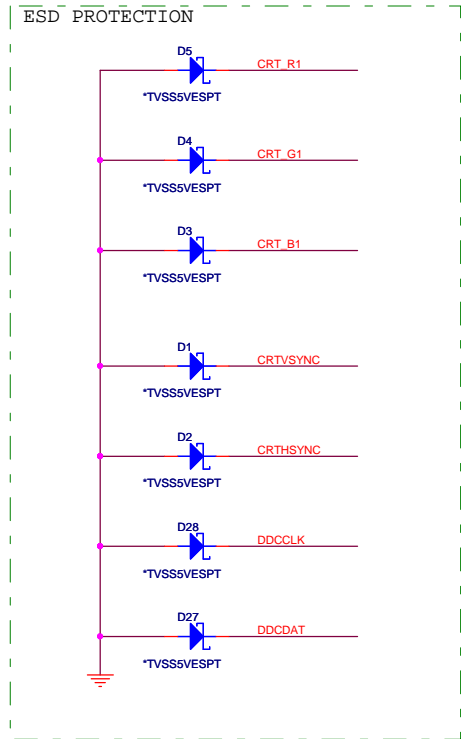


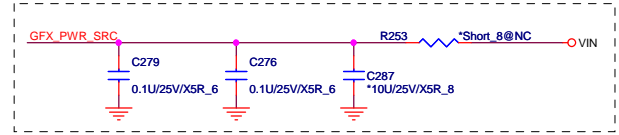
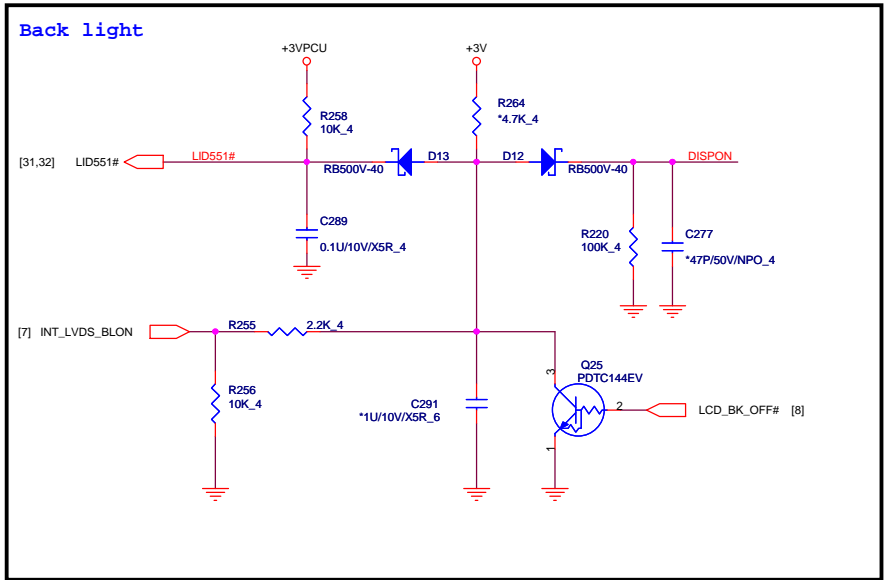
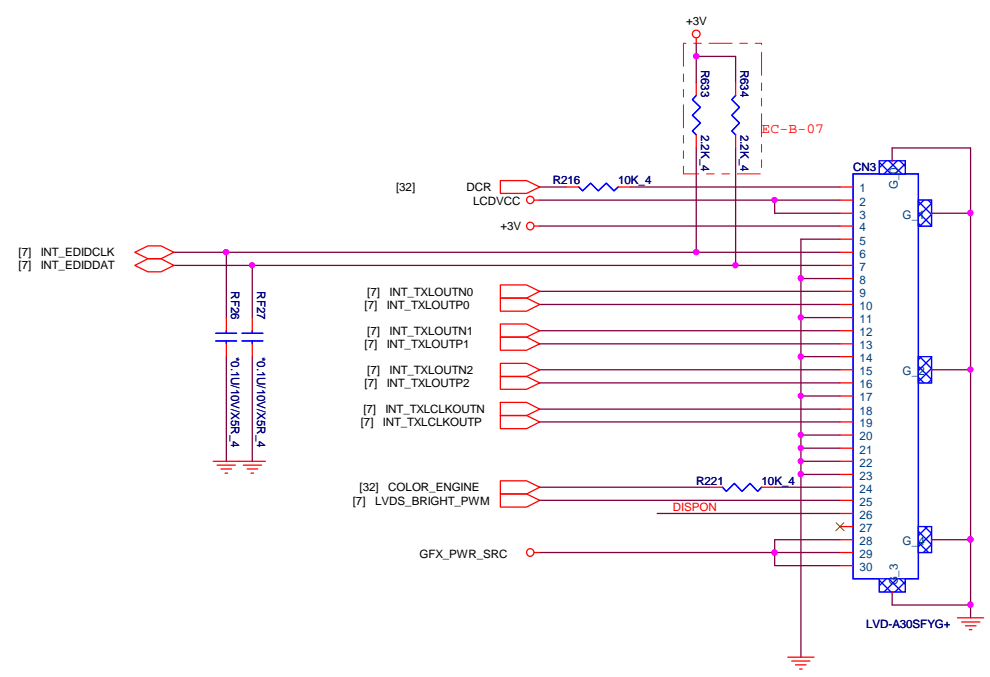
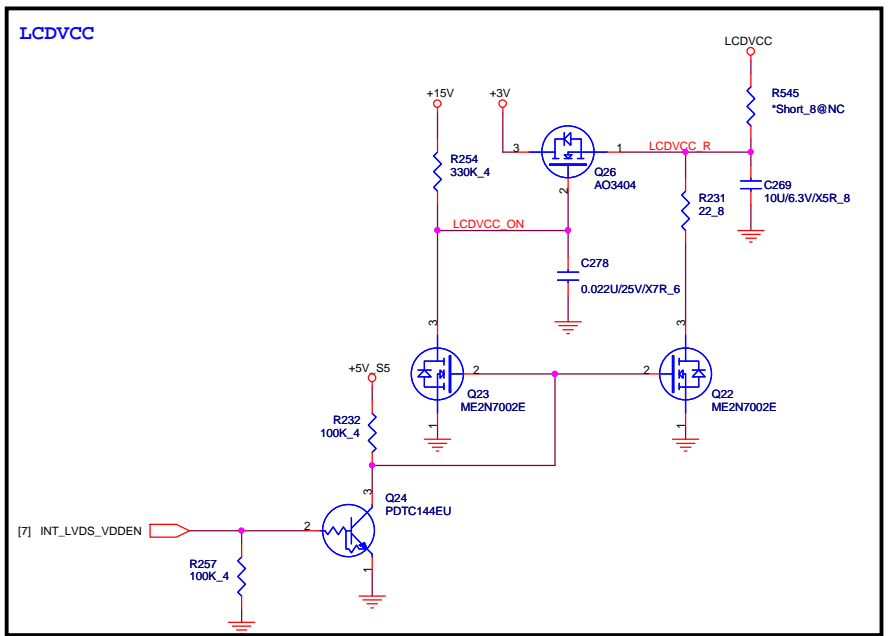


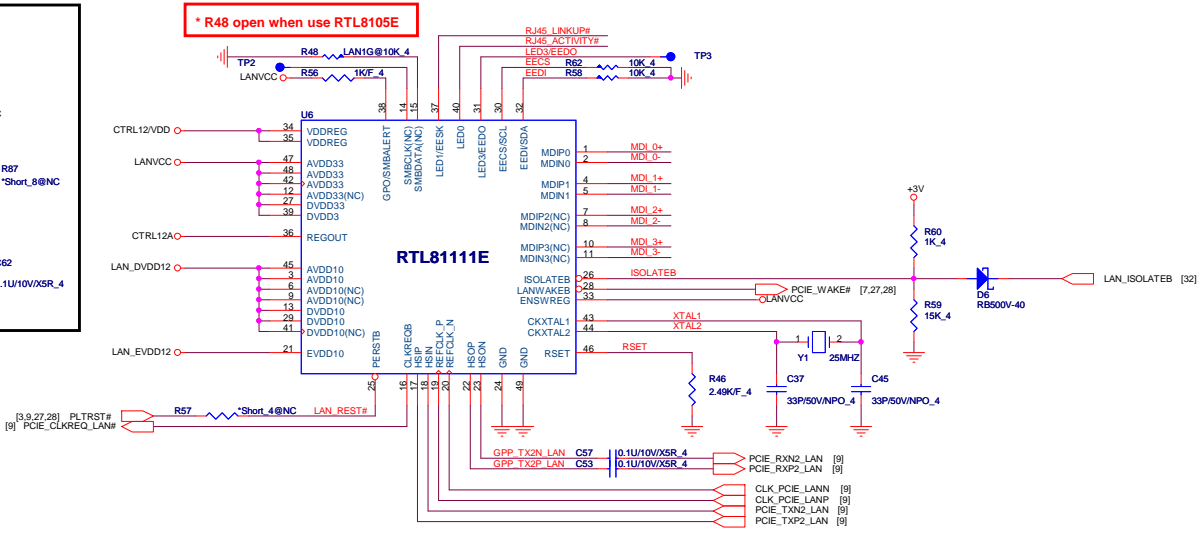
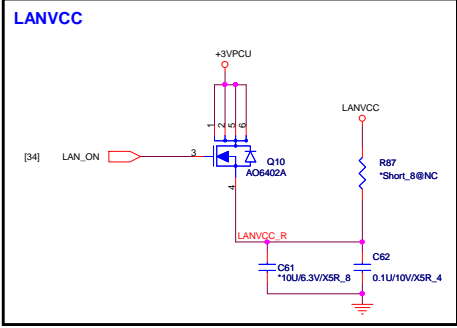
Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

Place near
U37,U38 < 200 mil

Place near
CN5002 connector
< 200 mil

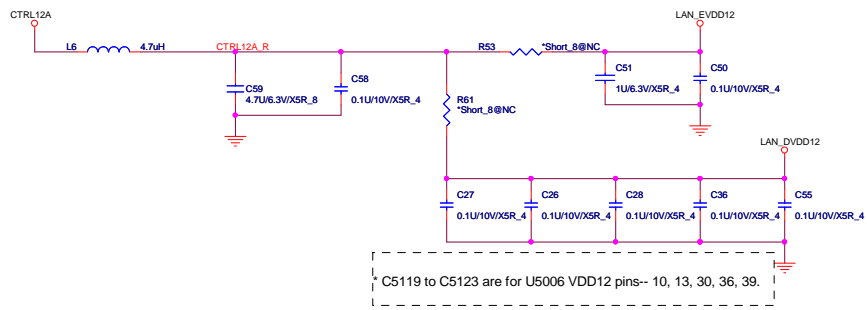
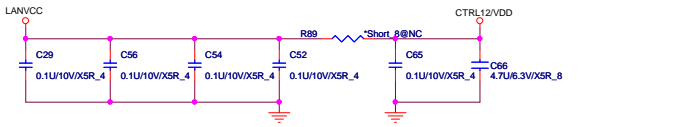






* R48 open when use RTL8105E

* C5116 and C5273 are for U5006 EVDD12 pin 19.

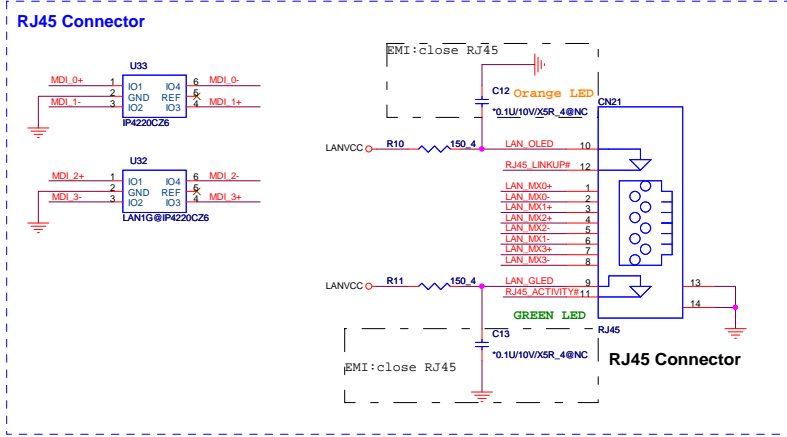
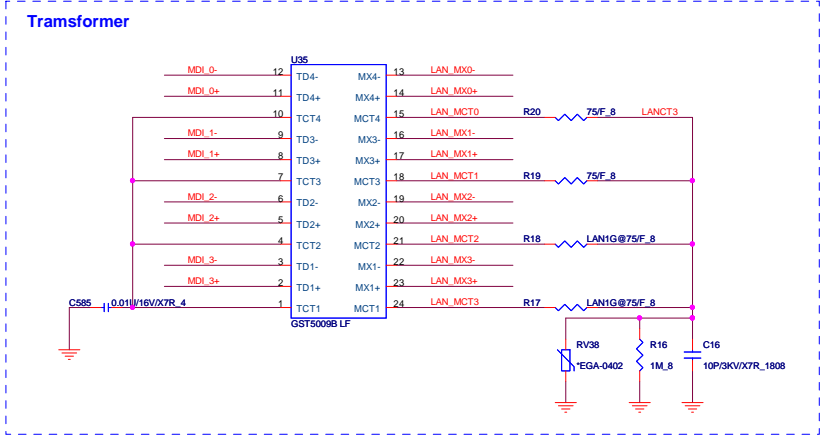


* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40. Place C5113, C5094 closed to U5006 pins 44, 45, and 40.

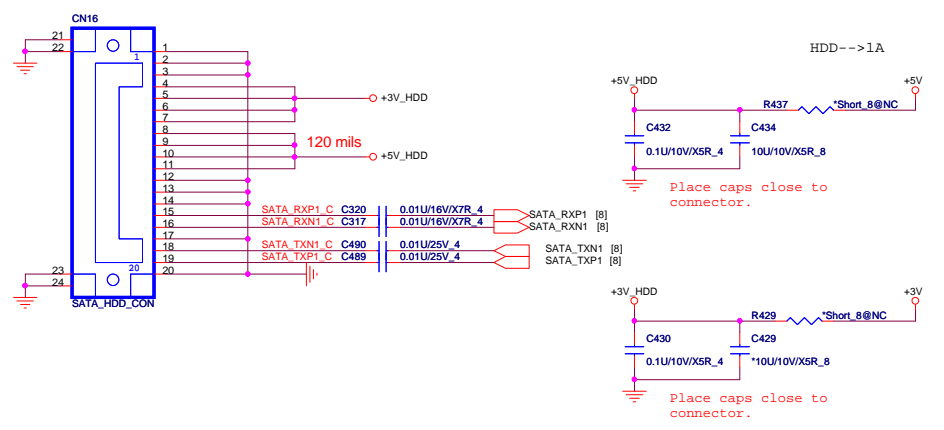
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

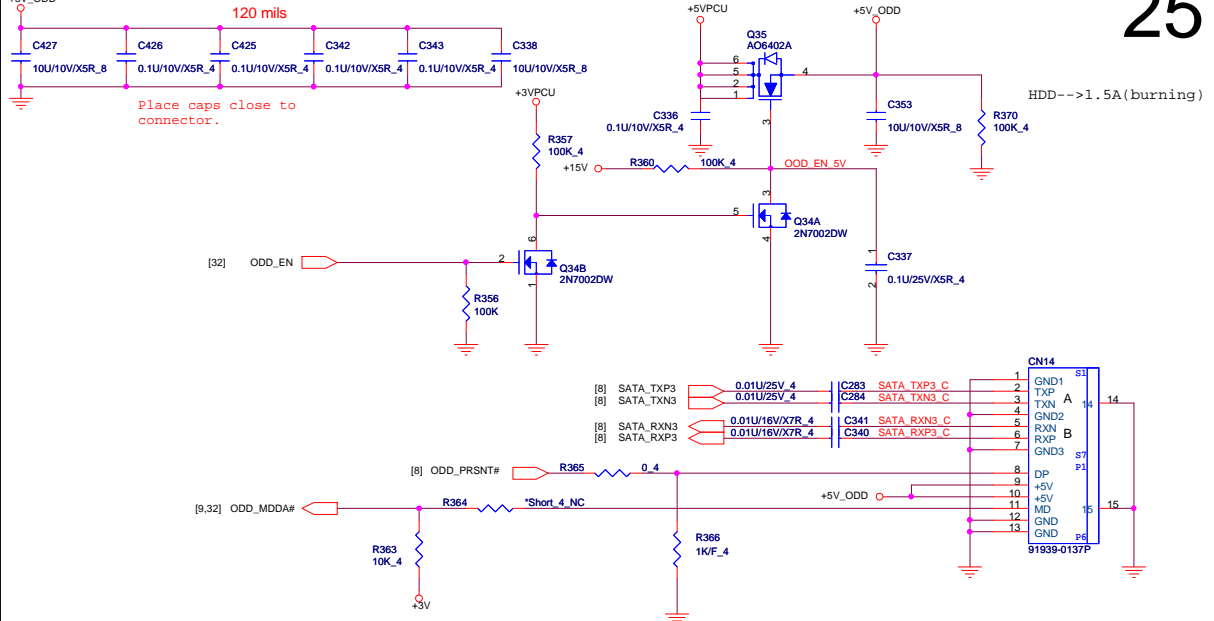
Layout: All termination signal should have 20 mil trace



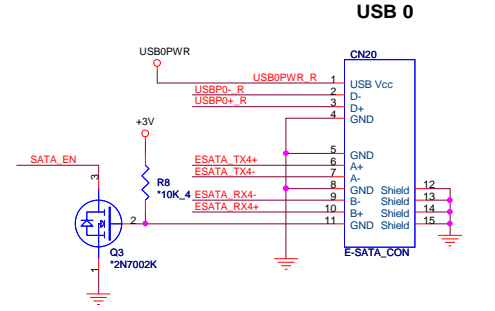
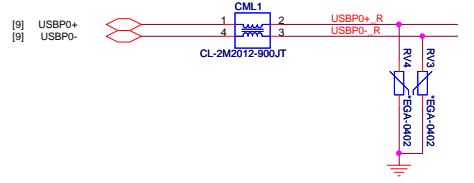
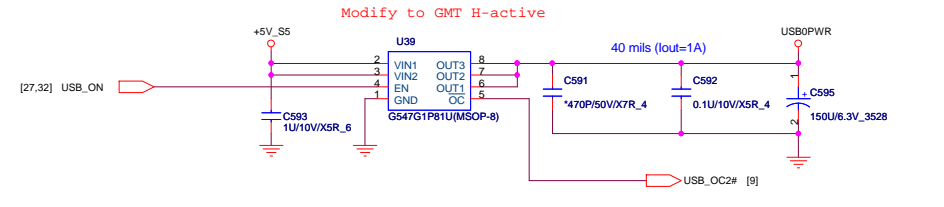
SATA HDD Connector.



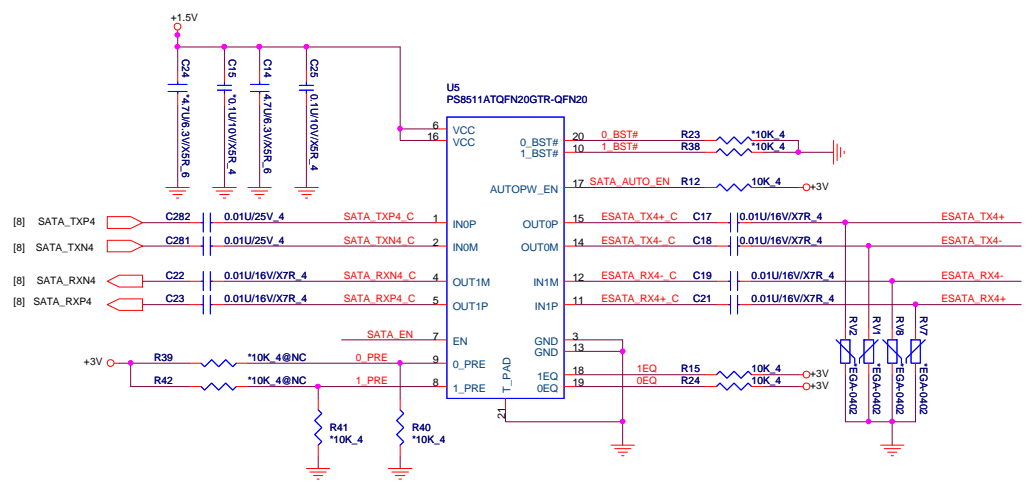
SATA ODD Connector.



USB + E-SATA



E-SATA RE-DRIVER

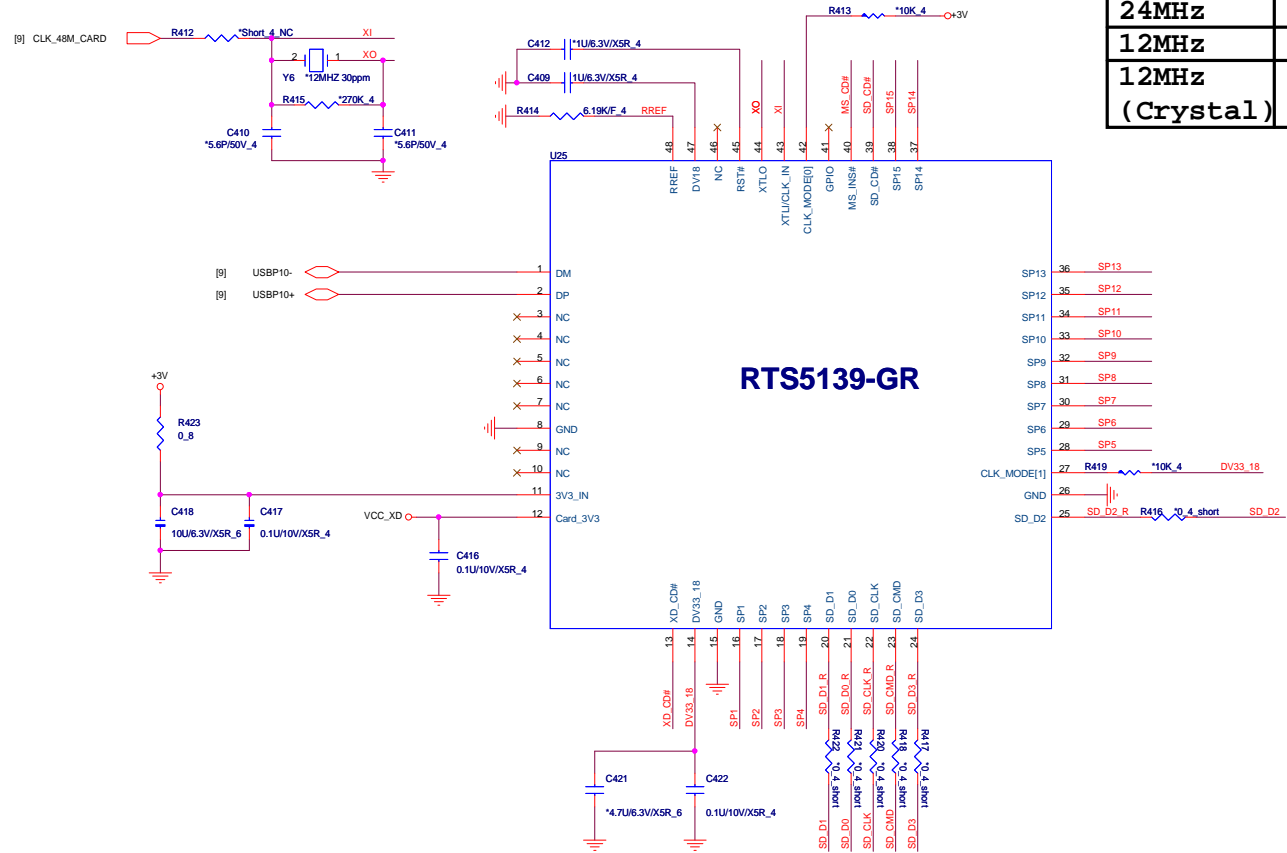


Layout: Locate this IC near to conn 2-3 inch, and it can away PCH above 10 inch.

- Straps notice:
- SATA 3G-->600mV ; 0/1 BST#-->H
 - If input length is over 7 inch ; 0/1EQ-->H

Int.PH(150Kohm) : EN, 0/1_BST#
Int.PL(150Kohm) : AUTO_EN, 0/1EQ, 0/1_PRE

EN	AUTO_EN	0/1EQ	D/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

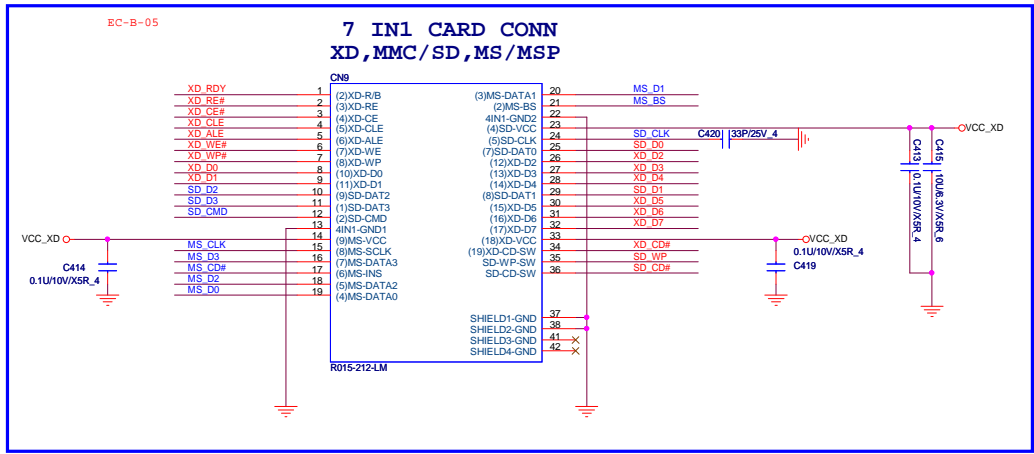


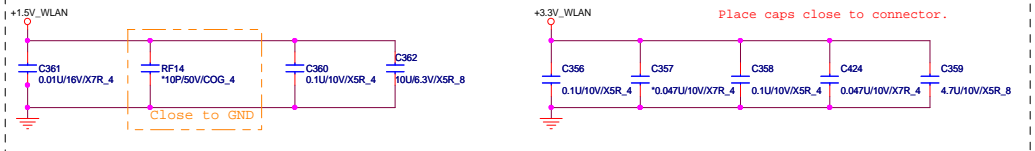
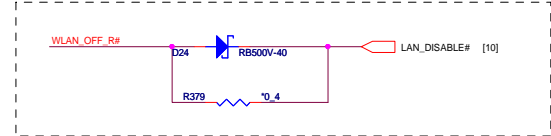
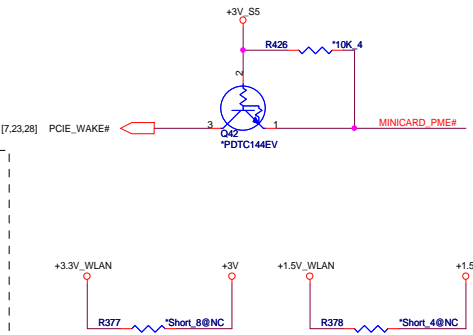
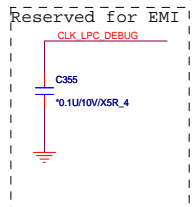
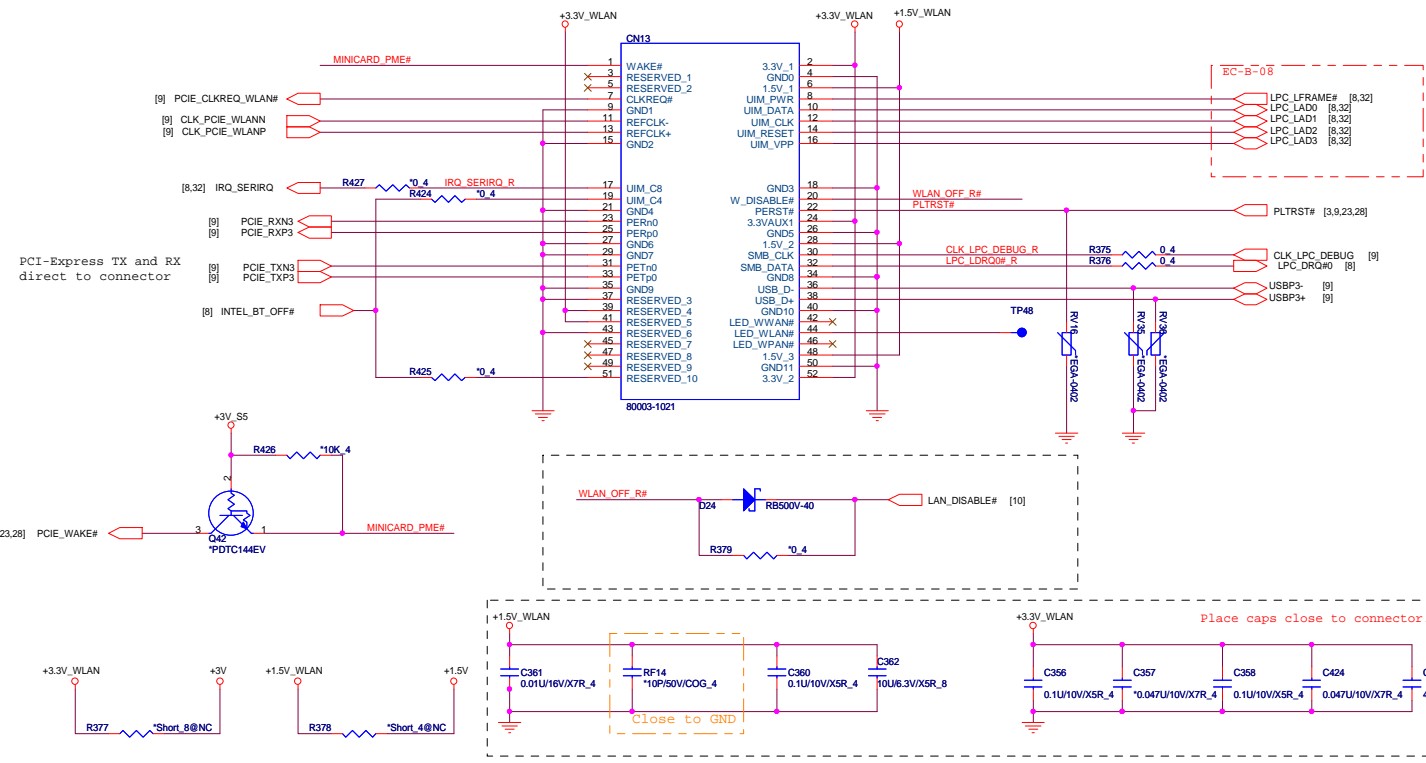
Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

Note:

SD/MMC	MS	XD
SP1	SD D7	XD RDY
SP2	SD D6	XD RE#
SP3	SD D5	XD CE#
SP4	SD D4	XD WE#
SP5	MS BS	XD CLE
SP6	MS D5	XD ALE
SP7	MS D1	XD WP#
SP8	MS D4	XD D0
SP9	MS D0	XD D1
SP10	MS D2	XD D2
SP11	MS D6	XD D3
SP12	MS D3	XD D4
SP13	MS D7	XD D5
SP14	MS CLK	XD D6
SP15	SD WP	XD D7

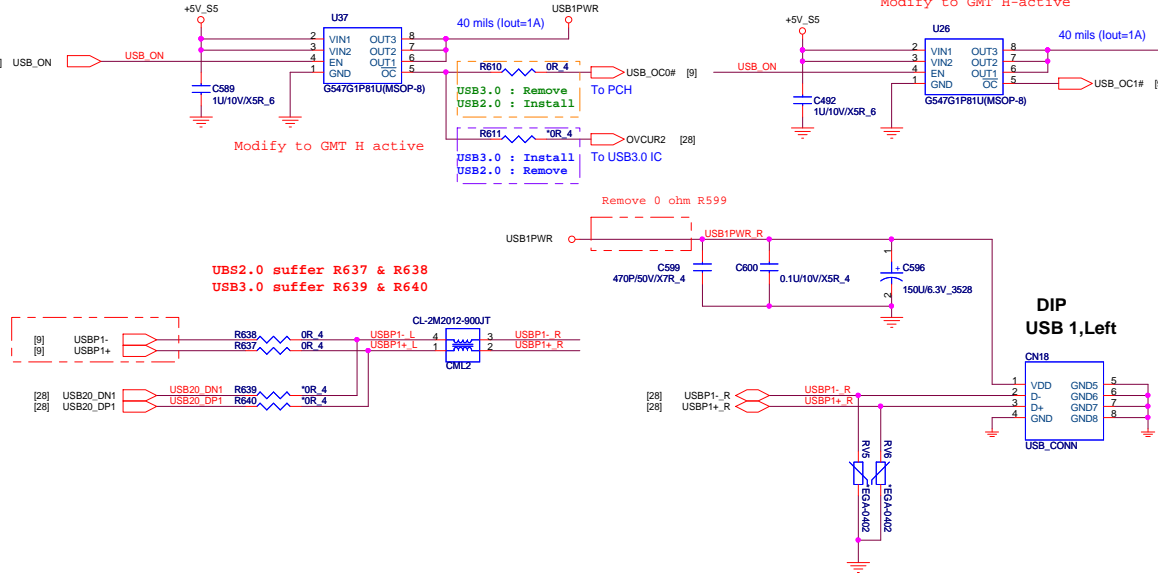
For RTS5139
SD,MS 4bit only



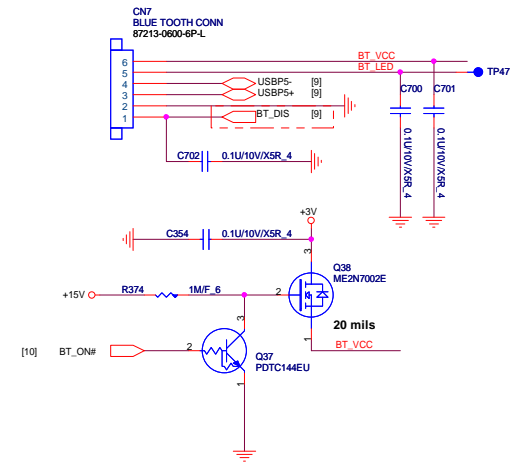


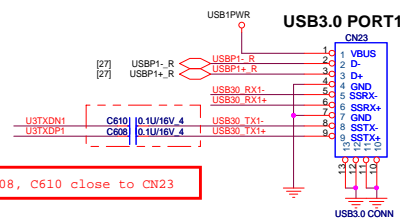
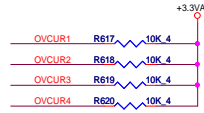
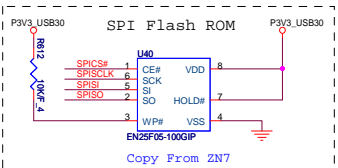
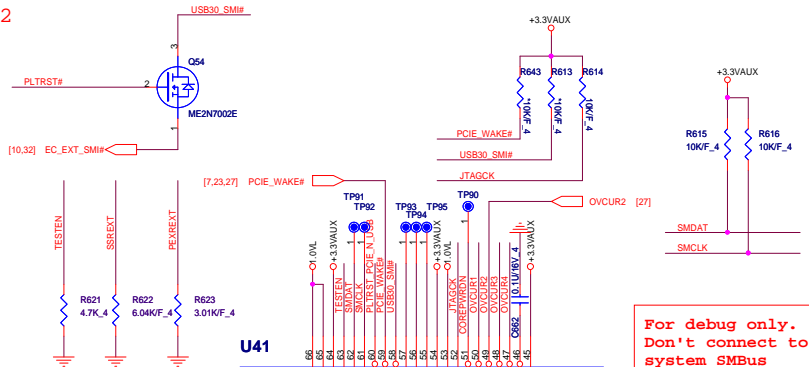
USB2.0*1

EC-B-02



BLUETOOTH

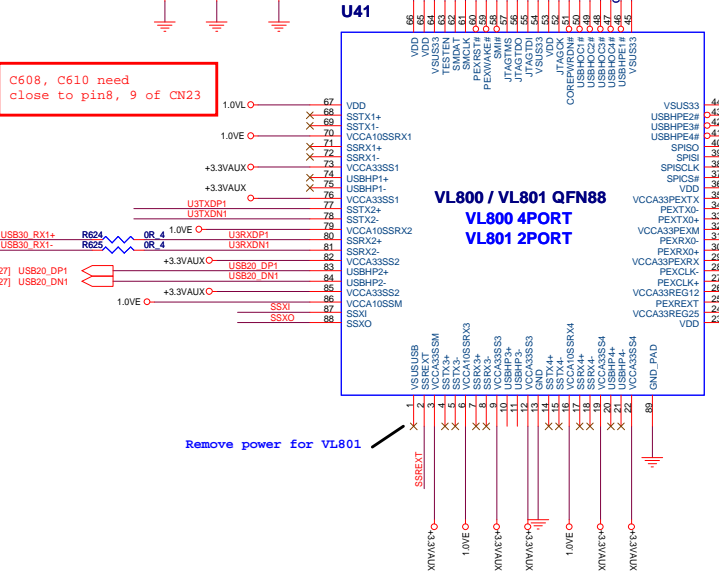




C608, C610 need close to pin8, 9 of CN23

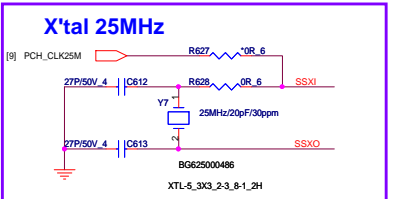
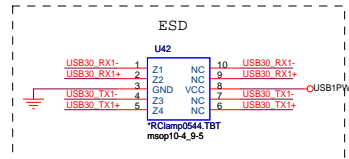
C608, C610 close to CN23

SUY USB3.0: DFHS09FR063
SUY USB2.0: DFHS04FR455



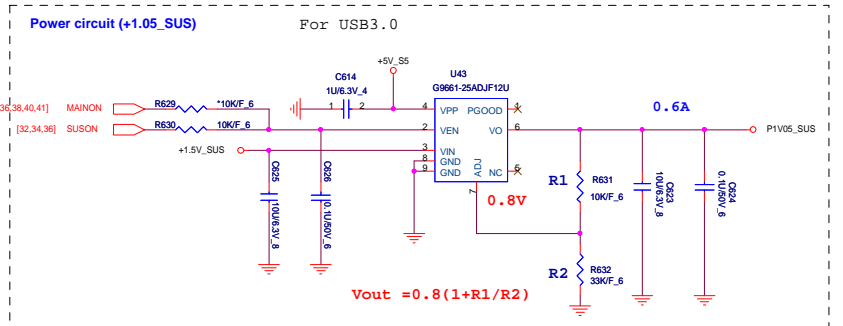
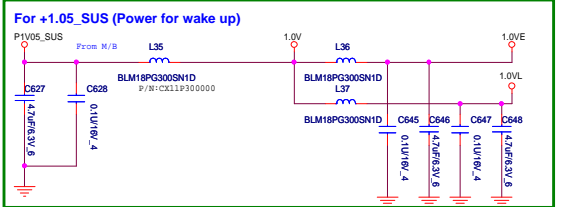
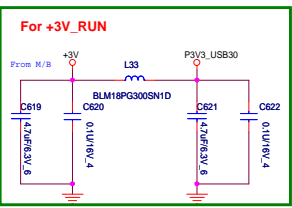
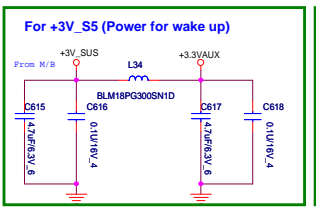
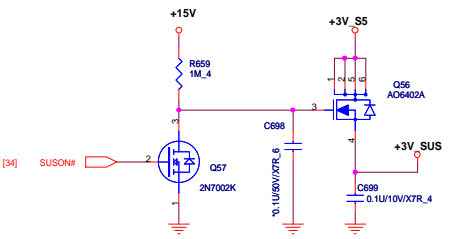
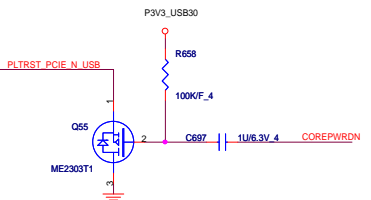
For debug only. Don't connect to system SMBus

Near PCIe Slot



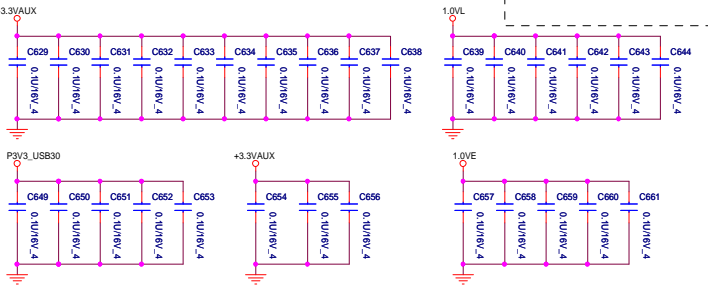
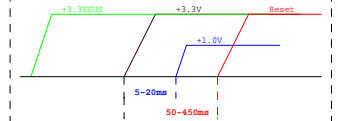
Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

For USB3.0
Remove SUSD turn on switch (From PCU to SUS) (Used +3V_S5 power plane)

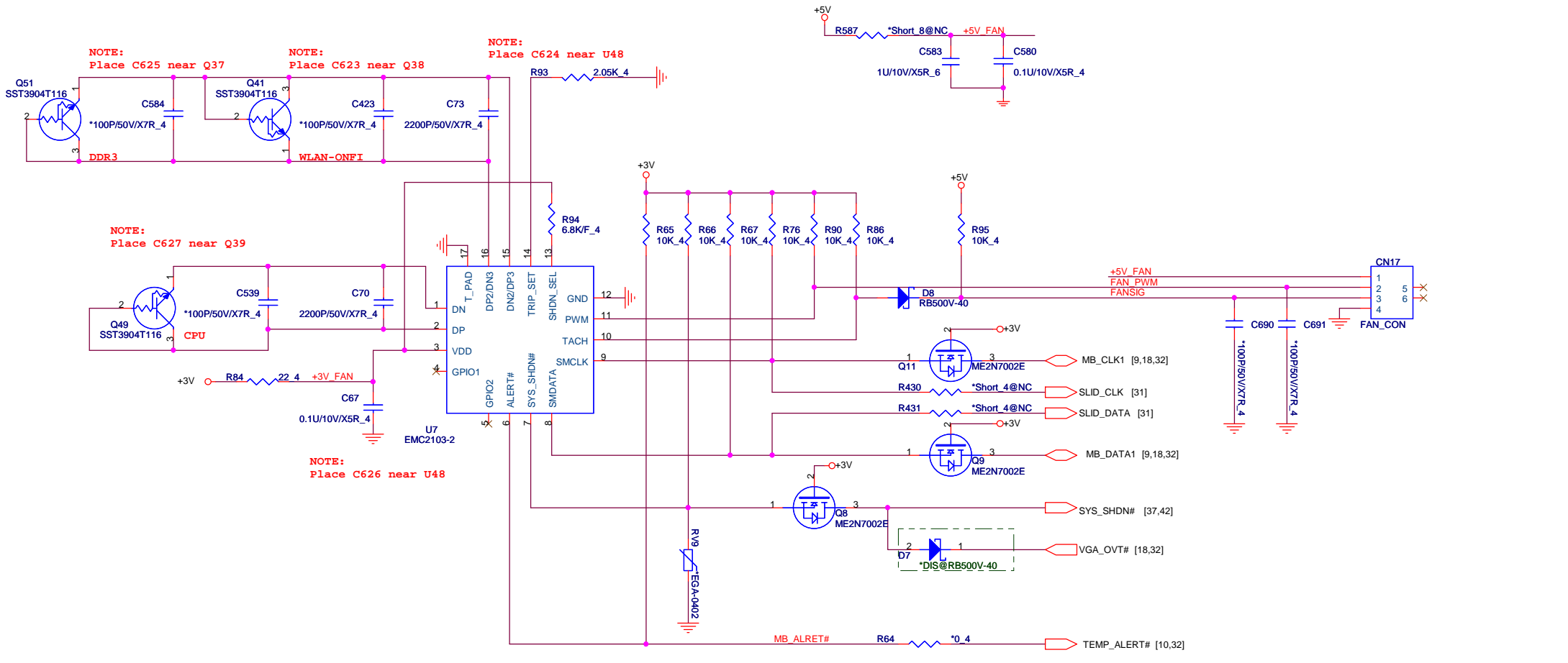


$$V_{out} = 0.8(1 + R1/R2)$$

Power sequence for Host.

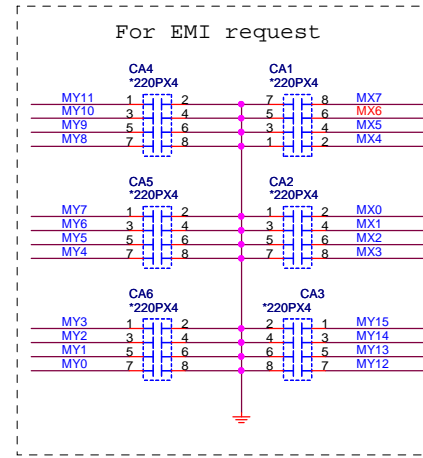
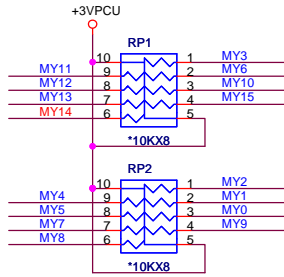
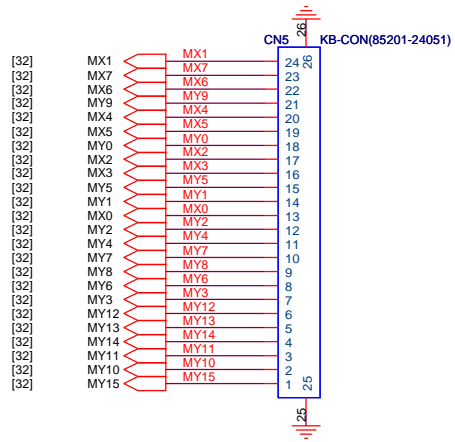


FAN CONTROL

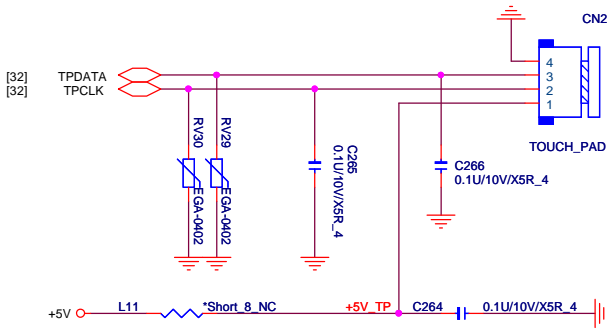


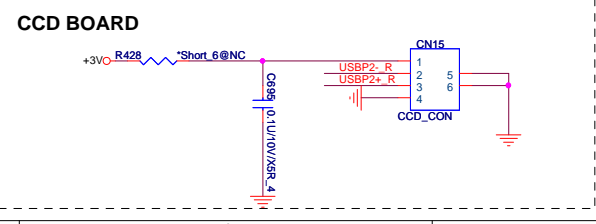
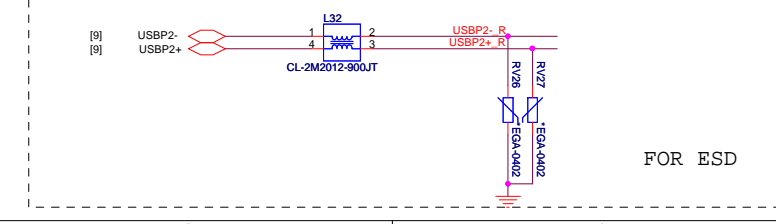
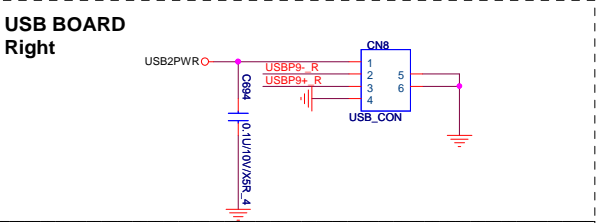
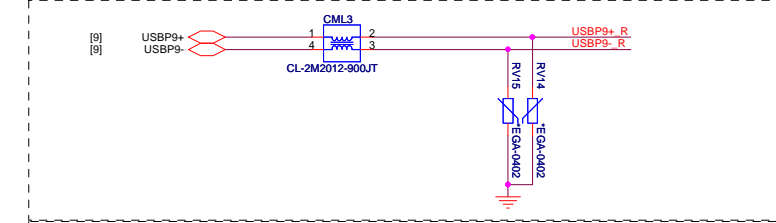
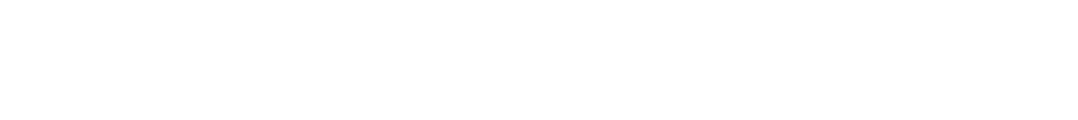
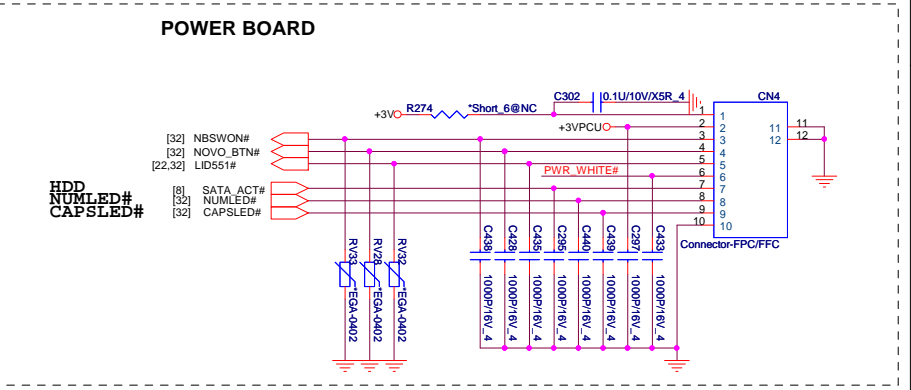
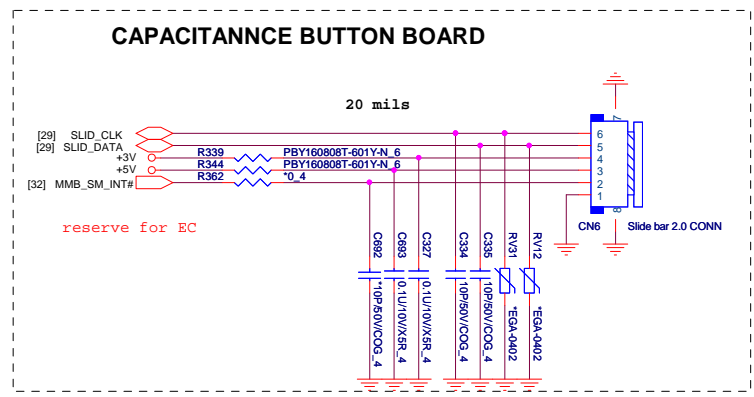
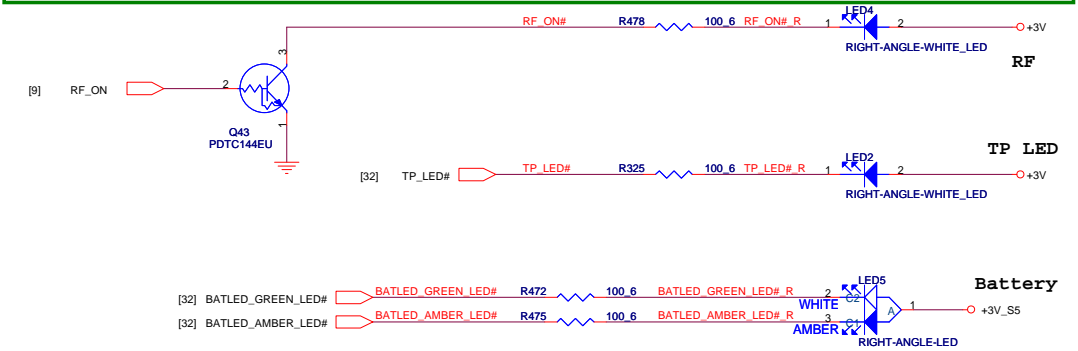
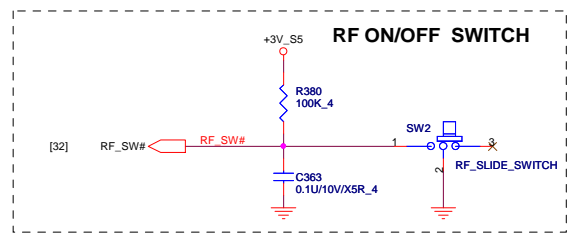
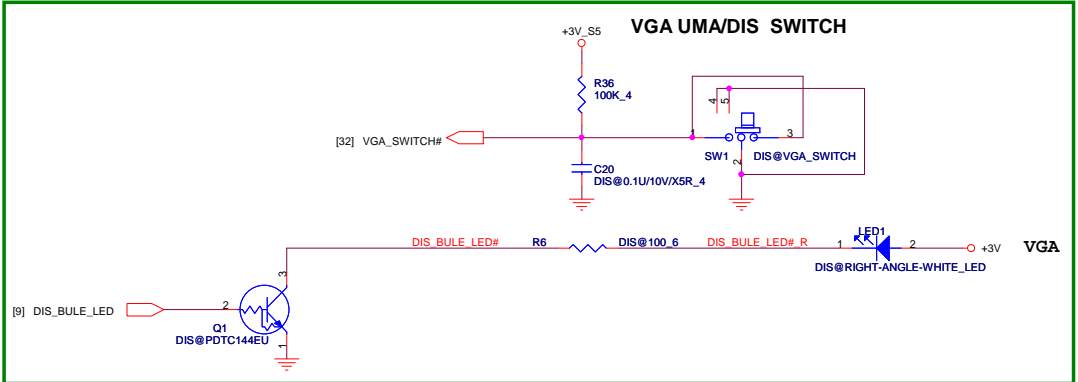
		PROJECT KL5A Quanta Computer Inc.	Size	Document Number	Rev
			B	FAN / THERMAL	1A
Date: Friday, October 29, 2010		Sheet	29	of	45

KEYBOARD

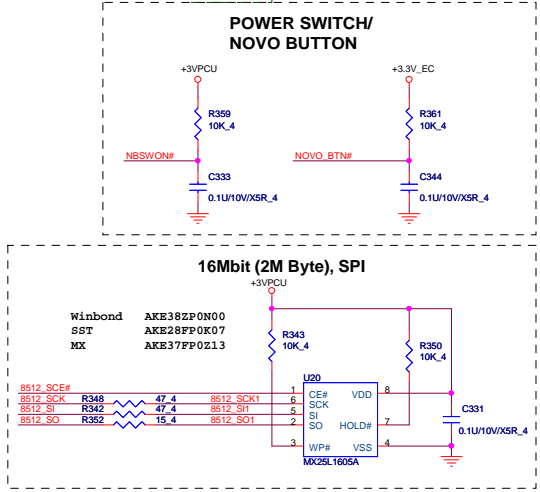
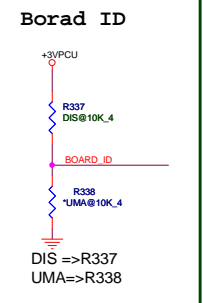
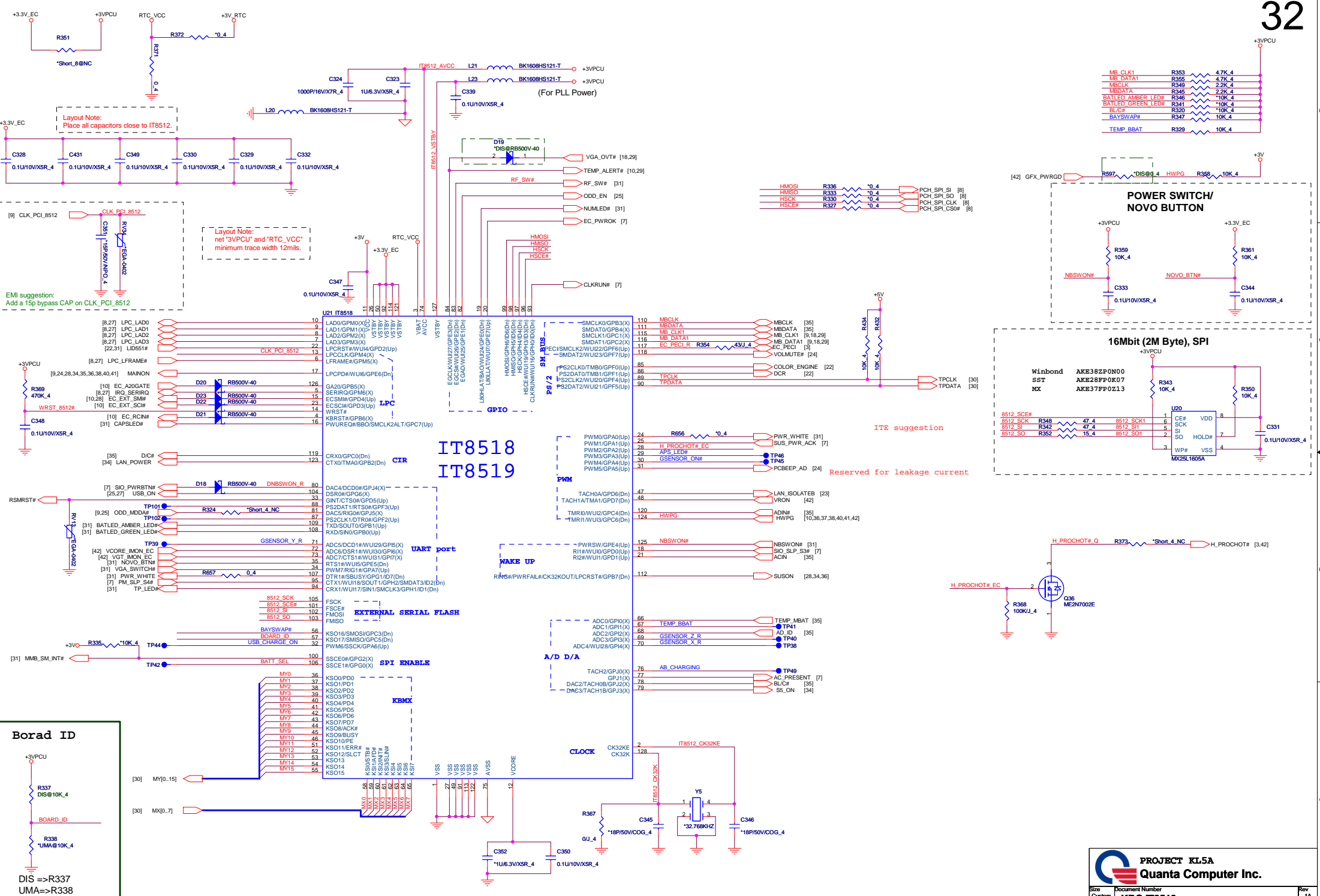


Touch pad

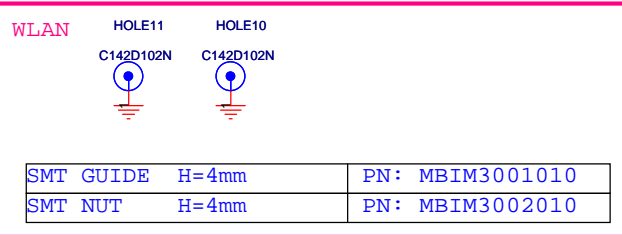




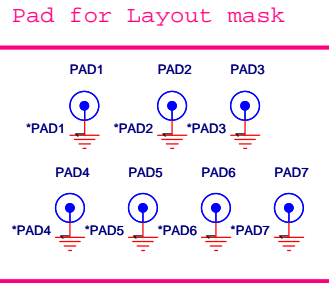
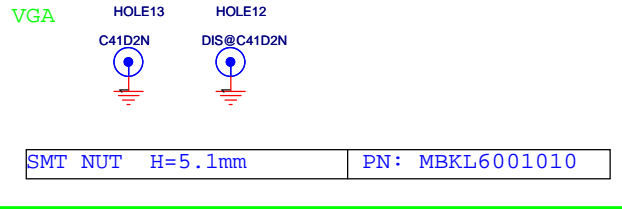
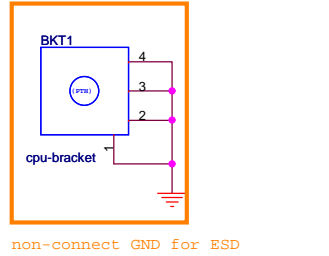
FOR ESD



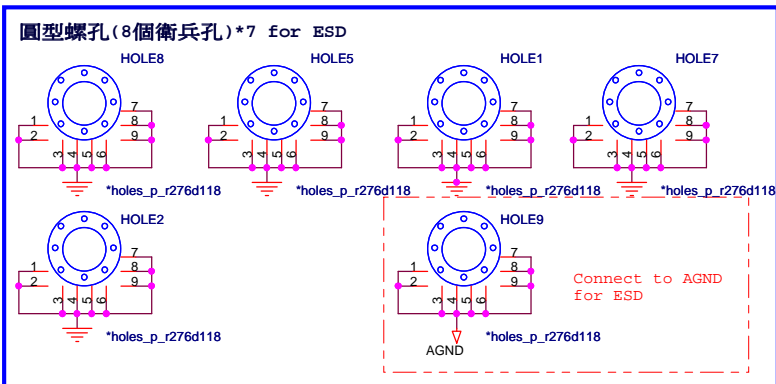
Screw for ME



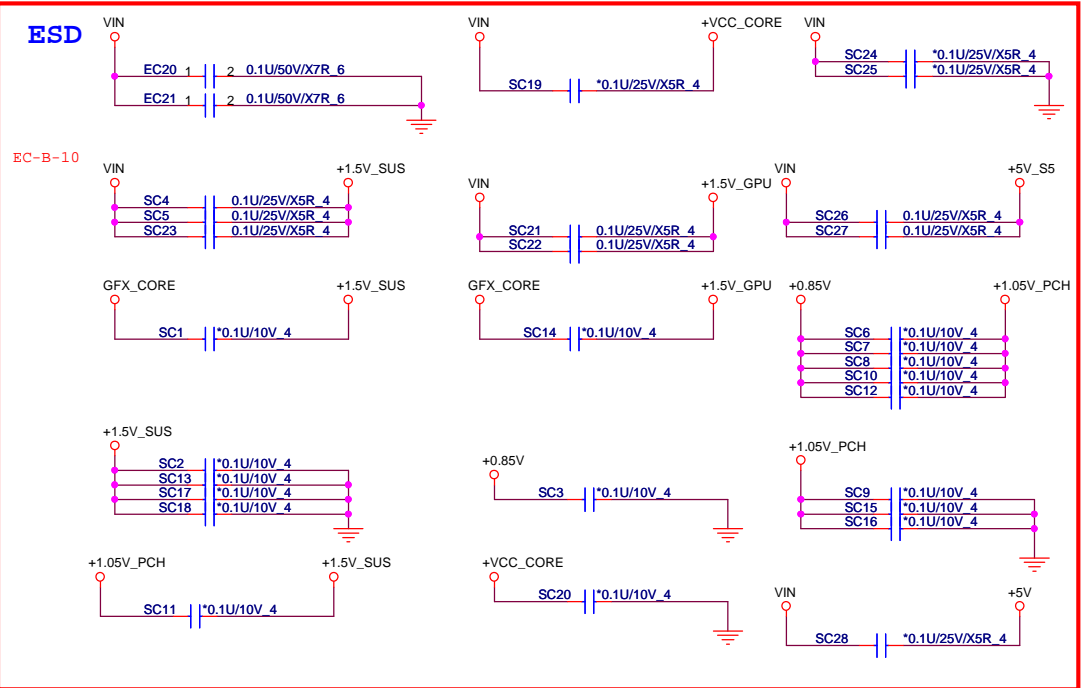
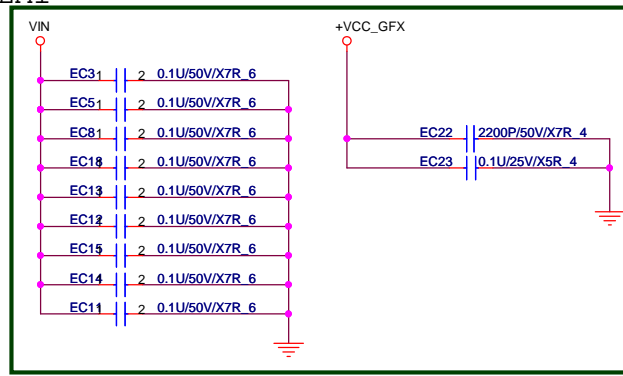
CPU BKT



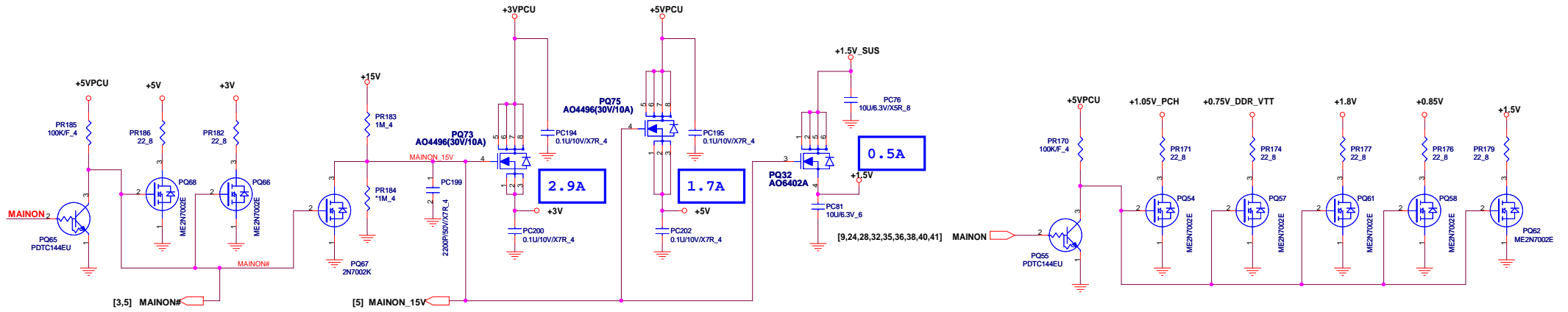
ME-other holes



EMI

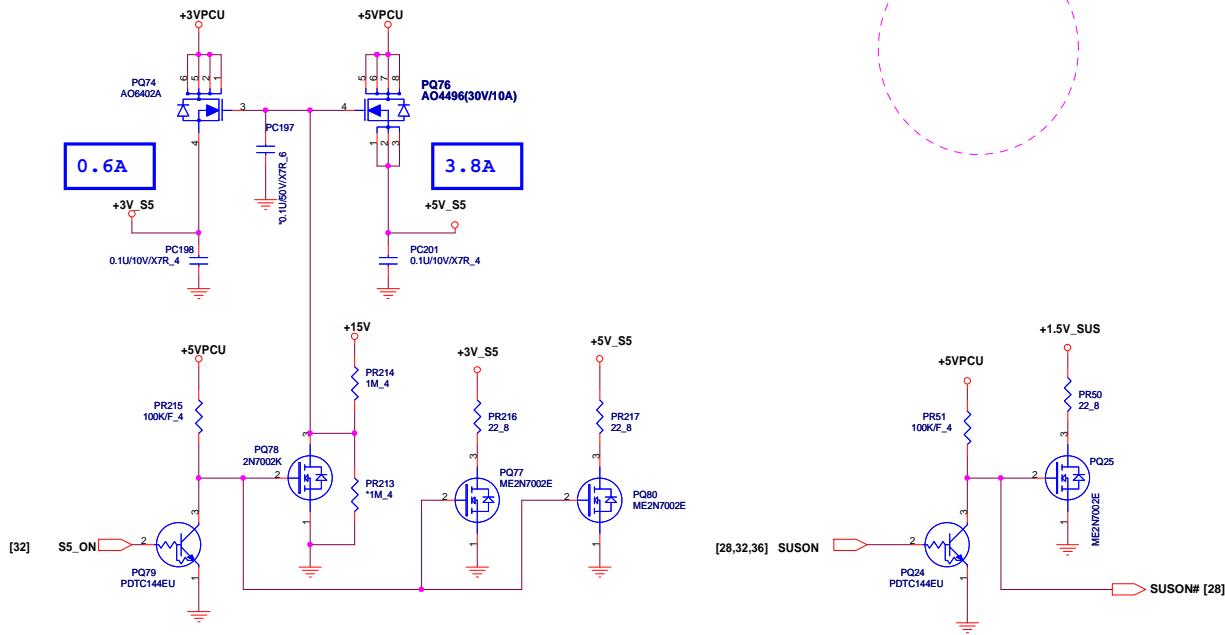


+3V, +5V, 1.5V

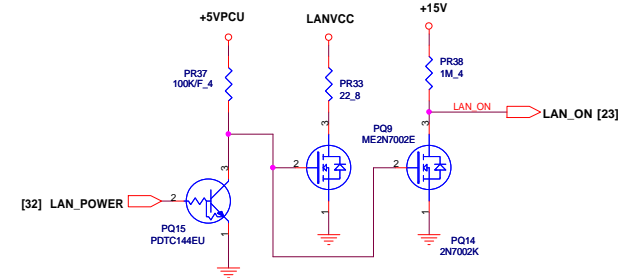


3V_S5, 5V_S5

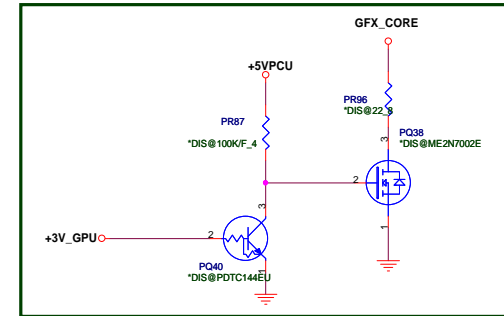
B-00

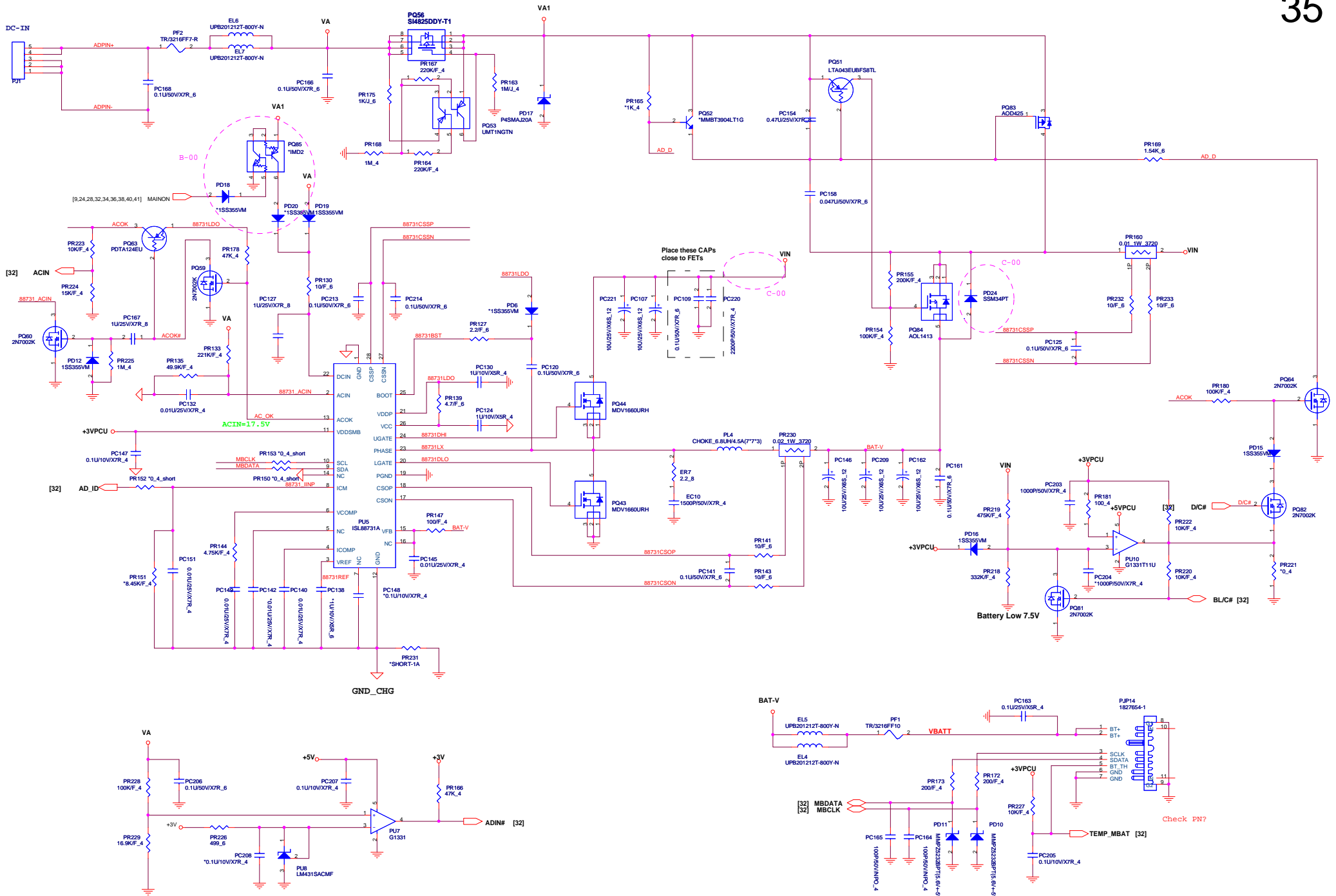


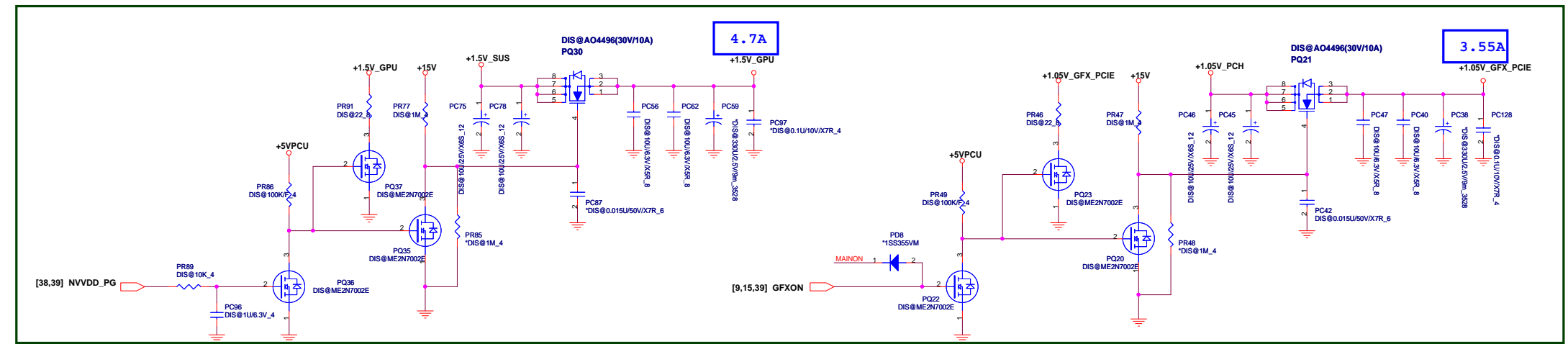
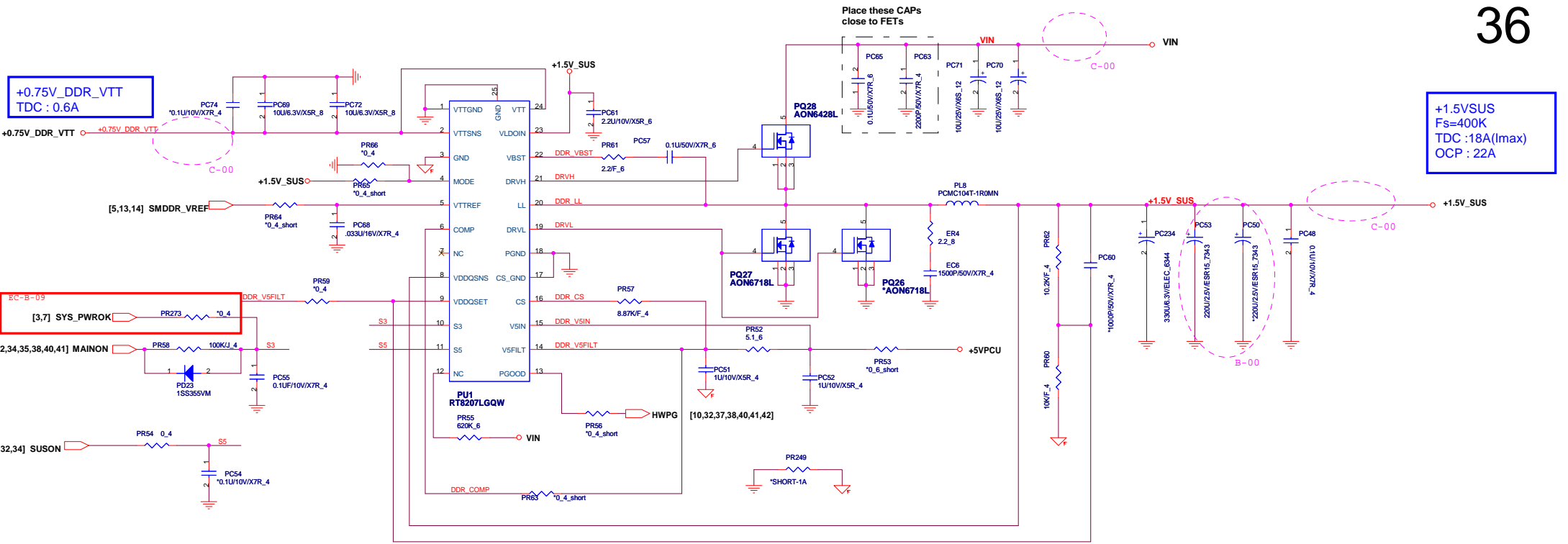
LANVCC

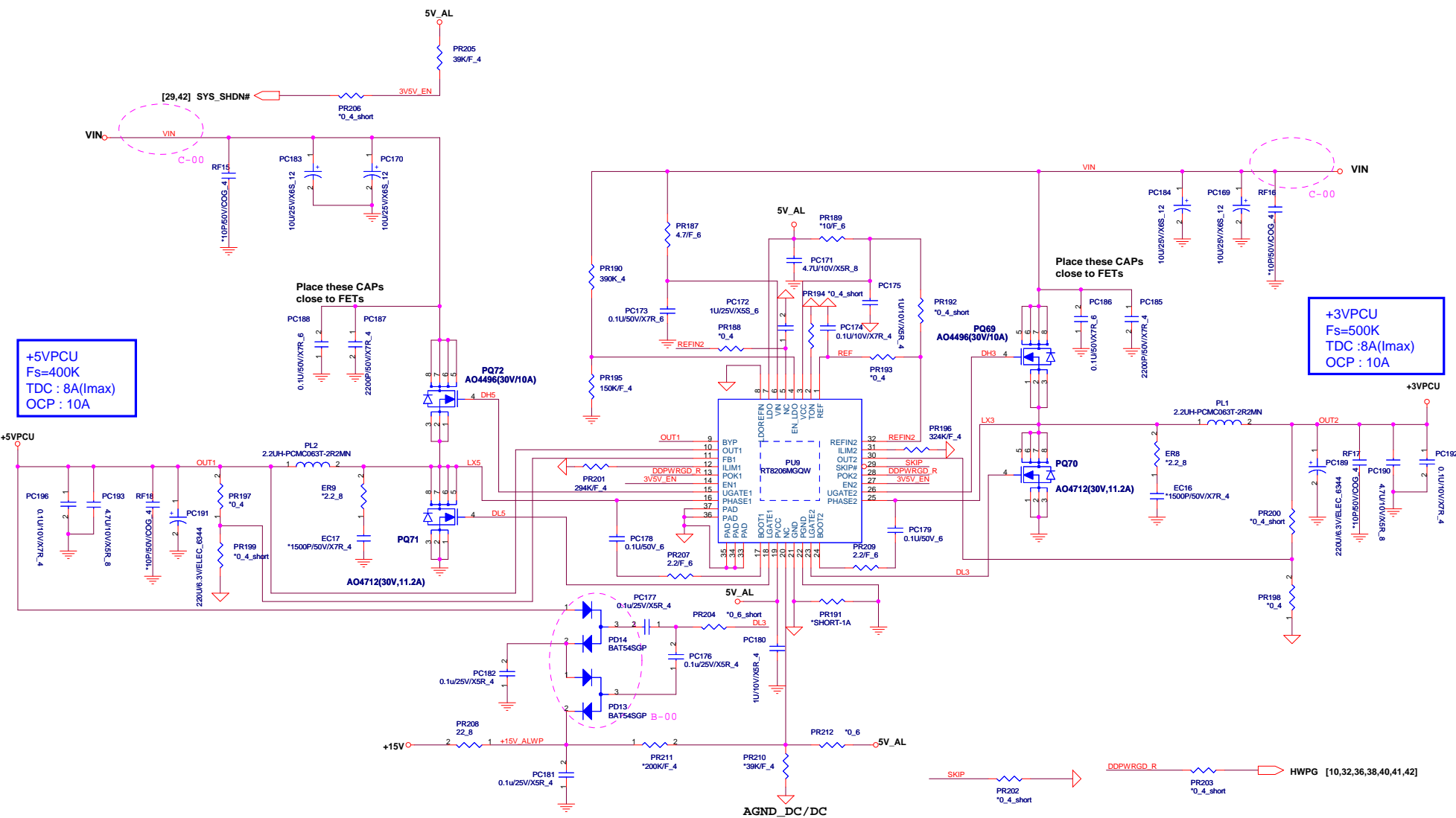


GFX_CORE







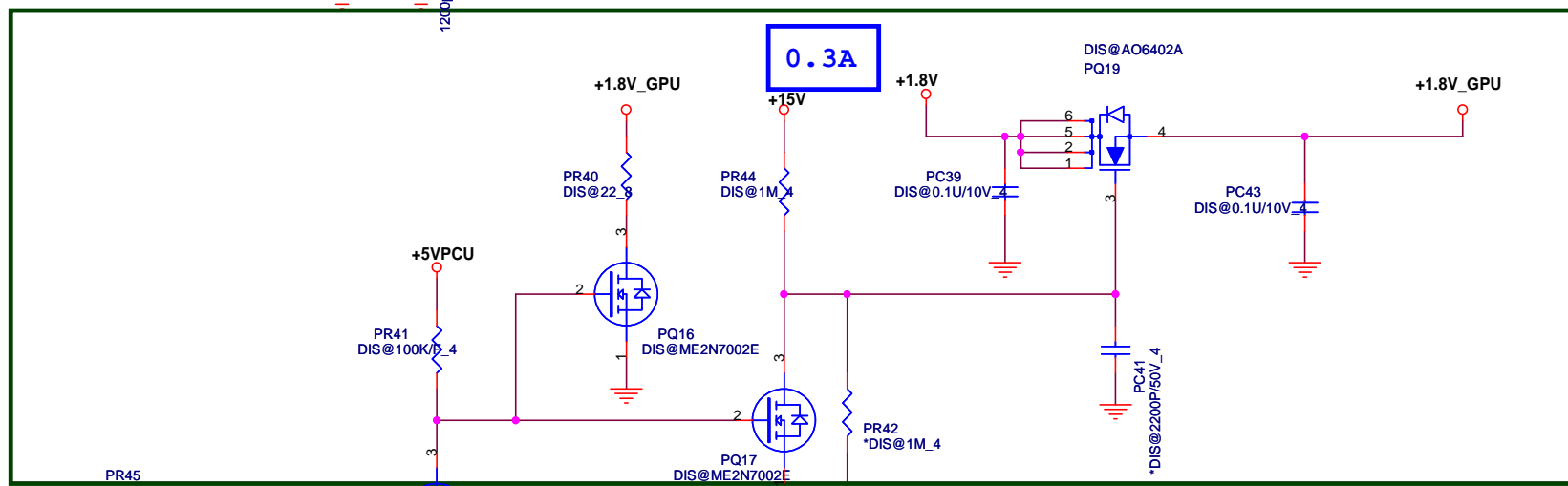
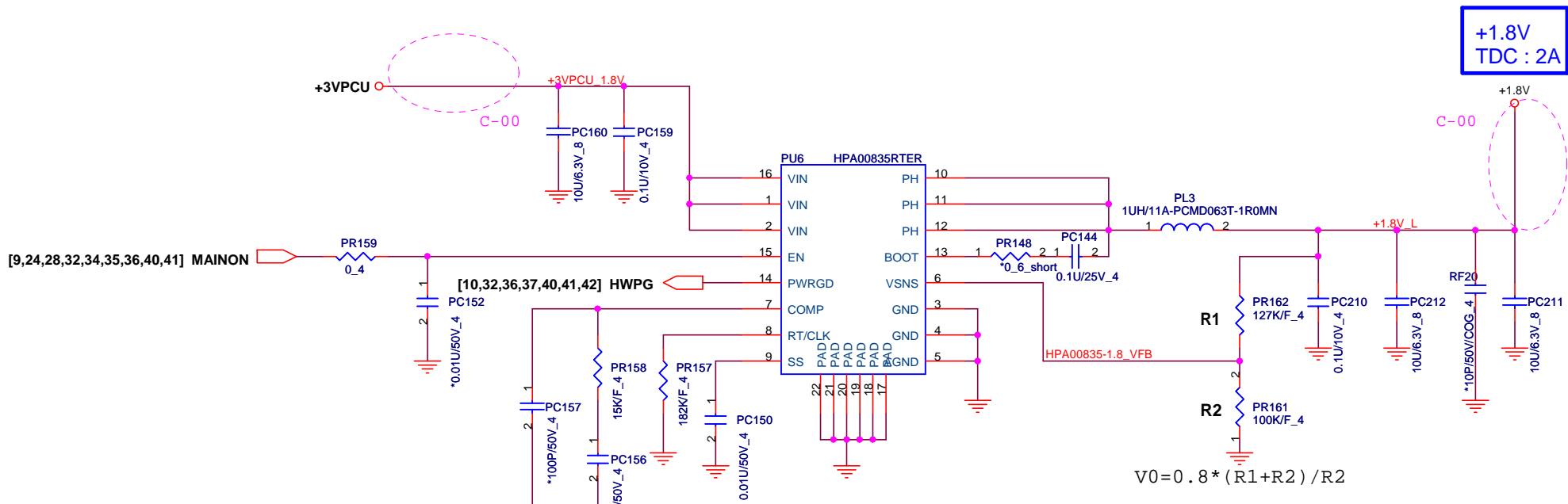


+5VPCU
 Fs=400K
 TDC : 8A(I_{max})
 OCP : 10A

+3VPCU
 Fs=500K
 TDC : 8A(I_{max})
 OCP : 10A

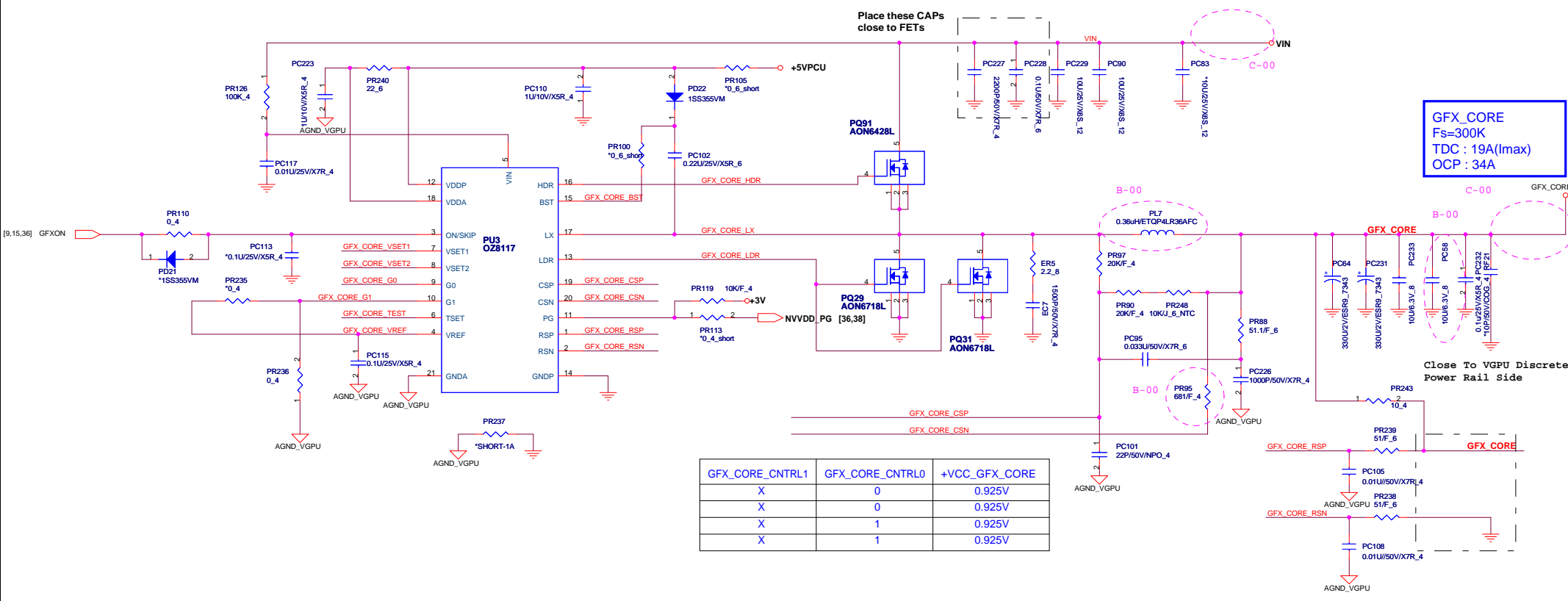
Place these CAPs close to FETs

Place these CAPs close to FETs

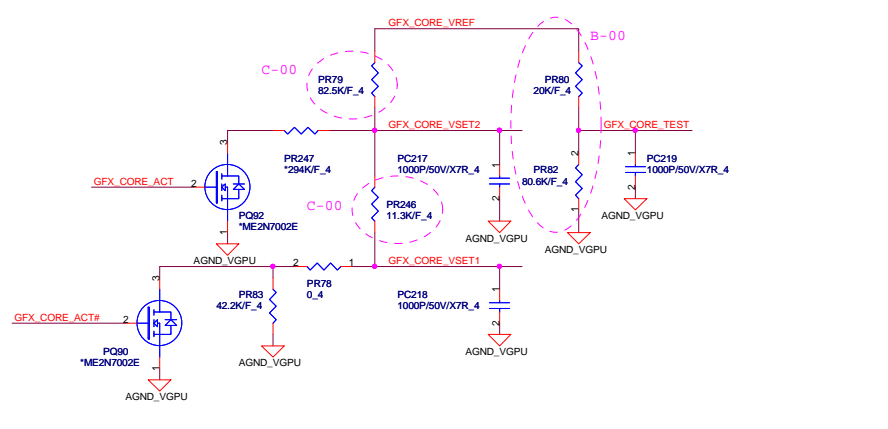
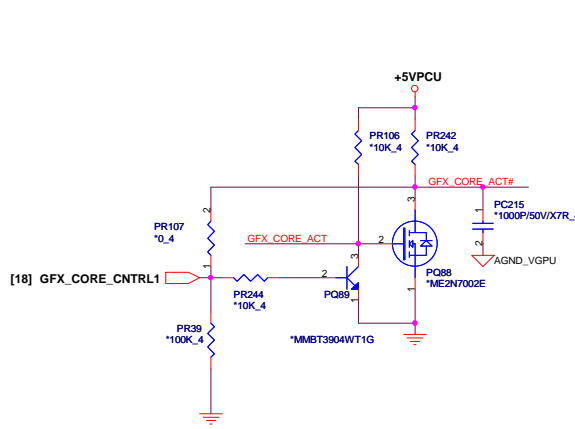
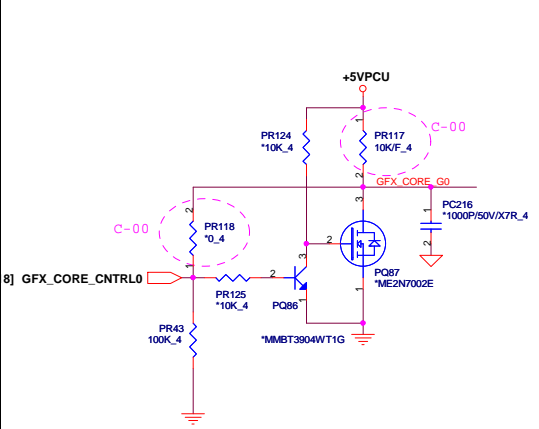


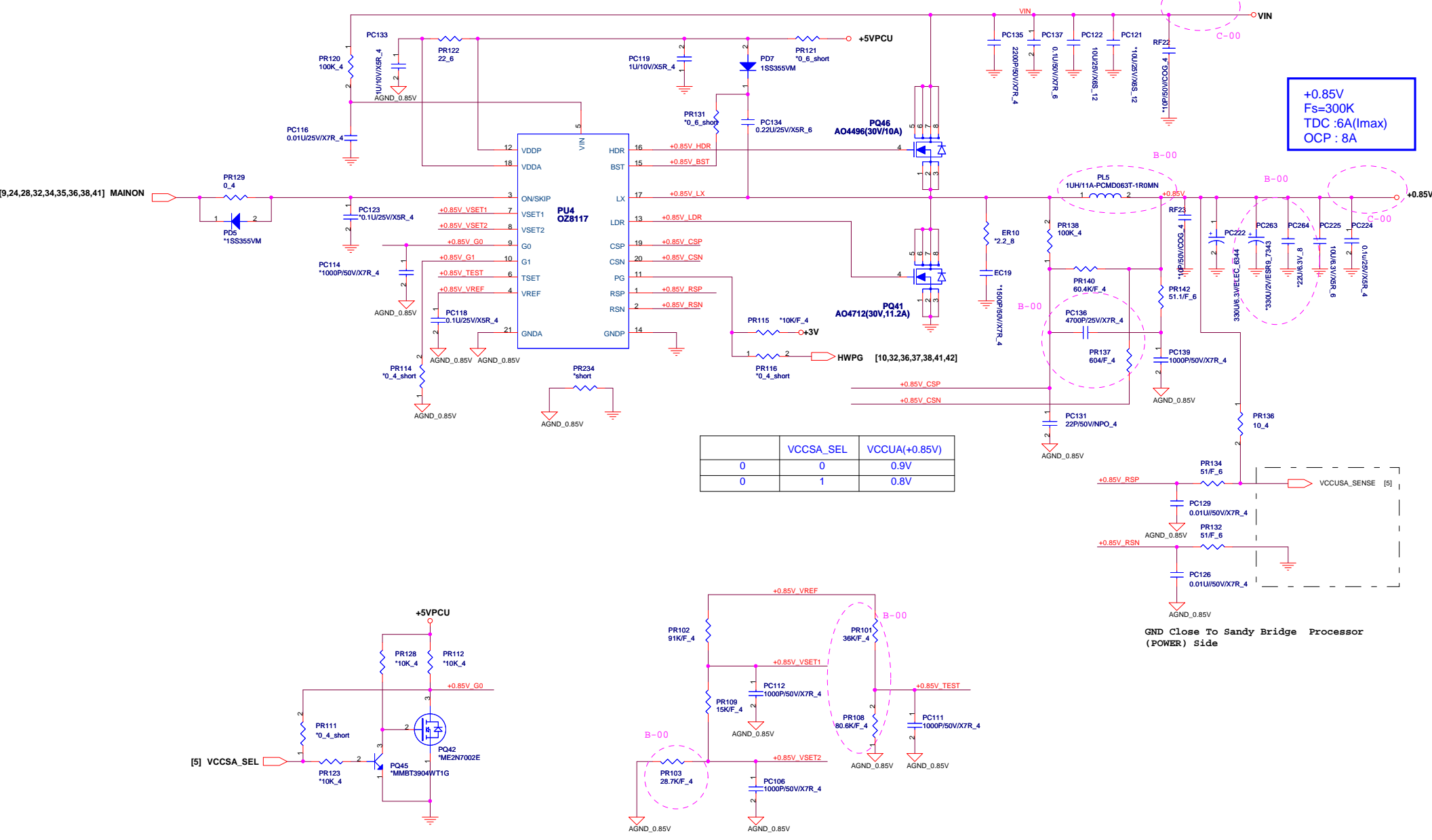
PROJECT KL5A
Quanta Computer Inc.

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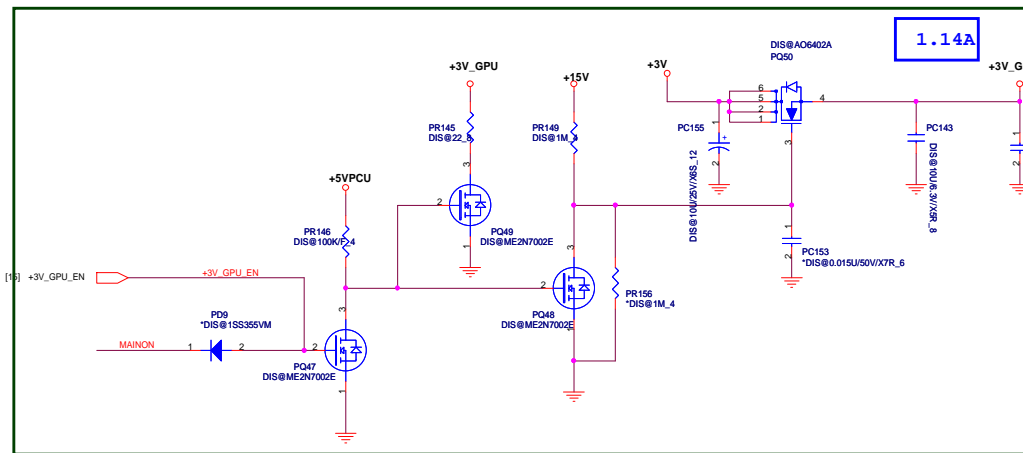
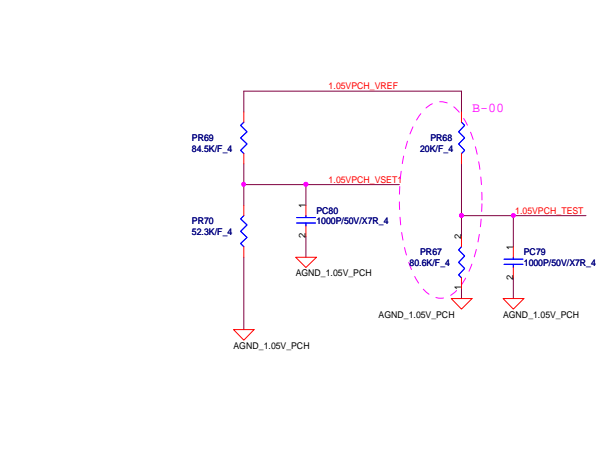
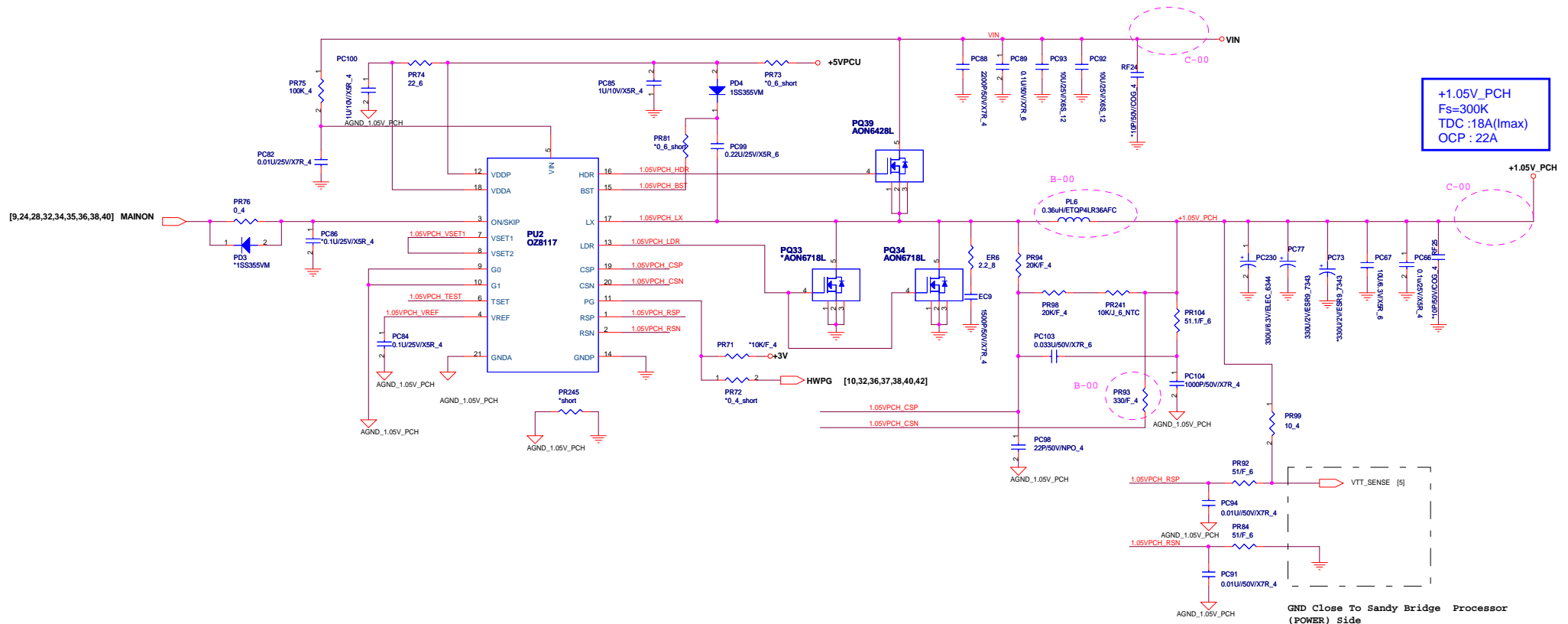
GFX_CORE
Fs=300K
TDC : 19A(I_{max})
OCP : 34A

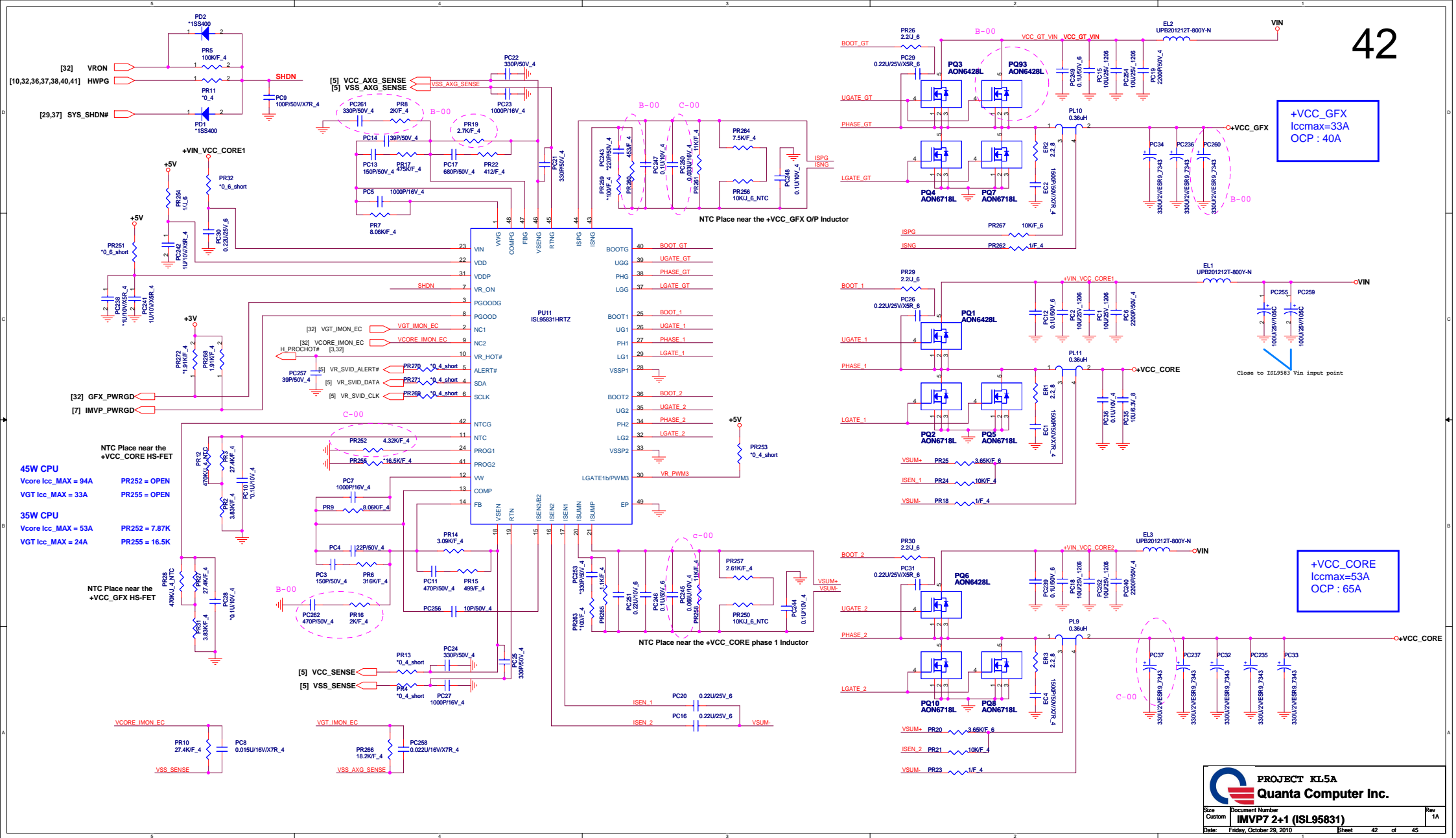




+0.85V
 Fs=300K
 TDC :6A(I_{max})
 OCP : 8A

	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V





+VCC_GFX
Iccmax=33A
OCP : 40A

+VCC_CORE
Iccmax=53A
OCP : 65A

45W CPU
Vcore Icc_MAX = 94A
VGT Icc_MAX = 33A

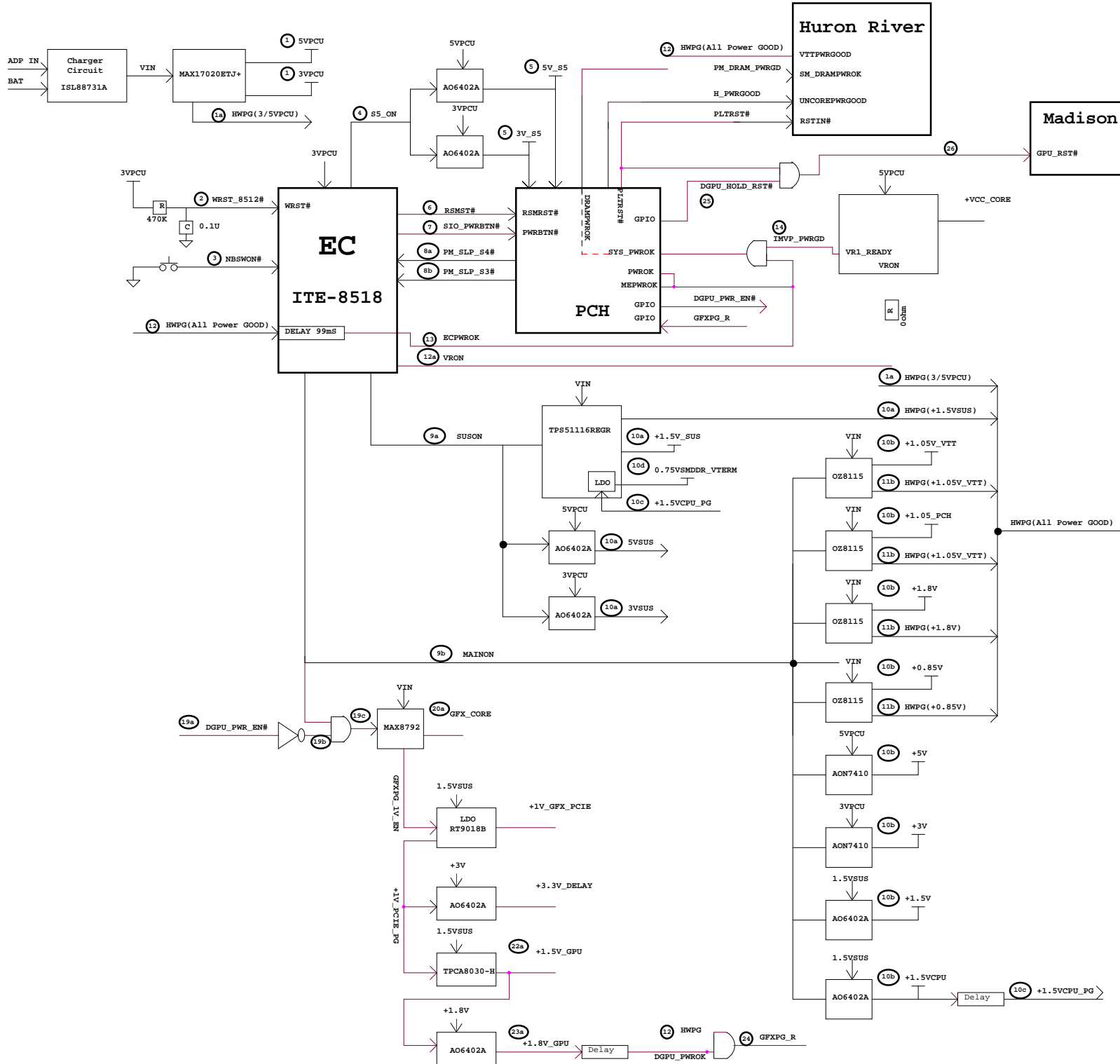
35W CPU
Vcore Icc_MAX = 53A
VGT Icc_MAX = 24A

Vcore_IMON_EC
VSS_SENSE

VGT_IMON_EC
VSS_AXG_SENSE


PROJECT KL5A
Quanta Computer Inc.

Size: Custom
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Date: Friday, October 26, 2010
Sheet: 42 of 45
Rev: 1A



KL5A / Z370 Huron River Schematic EC Tracking Record A (for SDV --> SIV,B) August 5, 2010

EC #	Page	CMVC#	Description	Date	Part Affected
B-00	24		Separate D25 to two single Diodes.	0816,1100	D25
B-01	10,22		Add Color Engine detect pin(PCH GPIO 70).	0816,1100	U17
B-02	9,27,28		Reserve USB3.0 solution for LC request.	0816,1500	U41
B-03	9		Modify PH of PCIE_CLKREQ_WLAN/LAN# to +3V for avoiding leakage current.	0816,1500	U17
B-04	10		Make Board ID table for BIOS control.	0816,1500	
B-05	26		Modify sch of card reader.	0818,1500	U25, CN9
B-06	10		NC R526 for boot issue.	0824,1500	R526
B-07	22		Add 2.2K PH for LVDS EDID used.	0824,1500	R633, R634
B-08	27		Correct the debug pin defition	0825,1400	CN13
B-09	36		Add SYS_PWROK connect to the net "S3" for S3 issue	0825,1400	PU1
B-10	33		Add some capacitors for ESD	0902,1900	SC1, SC2, , SC3, SC4, SC5, SC6, SC7, SC8, SC9, SC10, SC11, SC12, SC13, SC14, SC15, SC16, SC17, SC18, SC19, SC20, SC21, SC22, SC23, SC24, SC25, SC26, SC27, C28
B-11	10		add USB30_ID at GPIO24 & add GPIO13 for ID3	0907,1200	U17




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EC #	Page	CMVC#	Description	Date	Part Affected
C-00	15-19		GPU change to N12M-GS	0908,1000	U28
C-01	9,22,27, 37,38,39, 40,41		Add RF soultion	0913,1300	RF1,RF2,RF3,RF4,RF5, RF6,RF7,RF8,RF9,RF10, RF11,RF12,RF13,RF14,RF15, RF16,RF17,RF18,RF20,RF21, RF22,RF23,RF24,RF25,RF26, RF27
C-02	31		Change LED3 power from +3V_S5 to +3VPCU for Power LED always bright	0925,1100	LED3
C-03	3,4,7,8, 10,20,23 ,24,		Remove 0 ohm	1011,1700	R87,R253,R217,R224,R274, R339,R344,R351,R375,R376, R377,R378,R387,R397,R402, R409,R410,R423,R424,R425, R428,R429,R437,R430,R431, R545,R587
C-04	9		Remove U13 for delete 27Mhz clock signal form PCH	1015,1400	U13

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