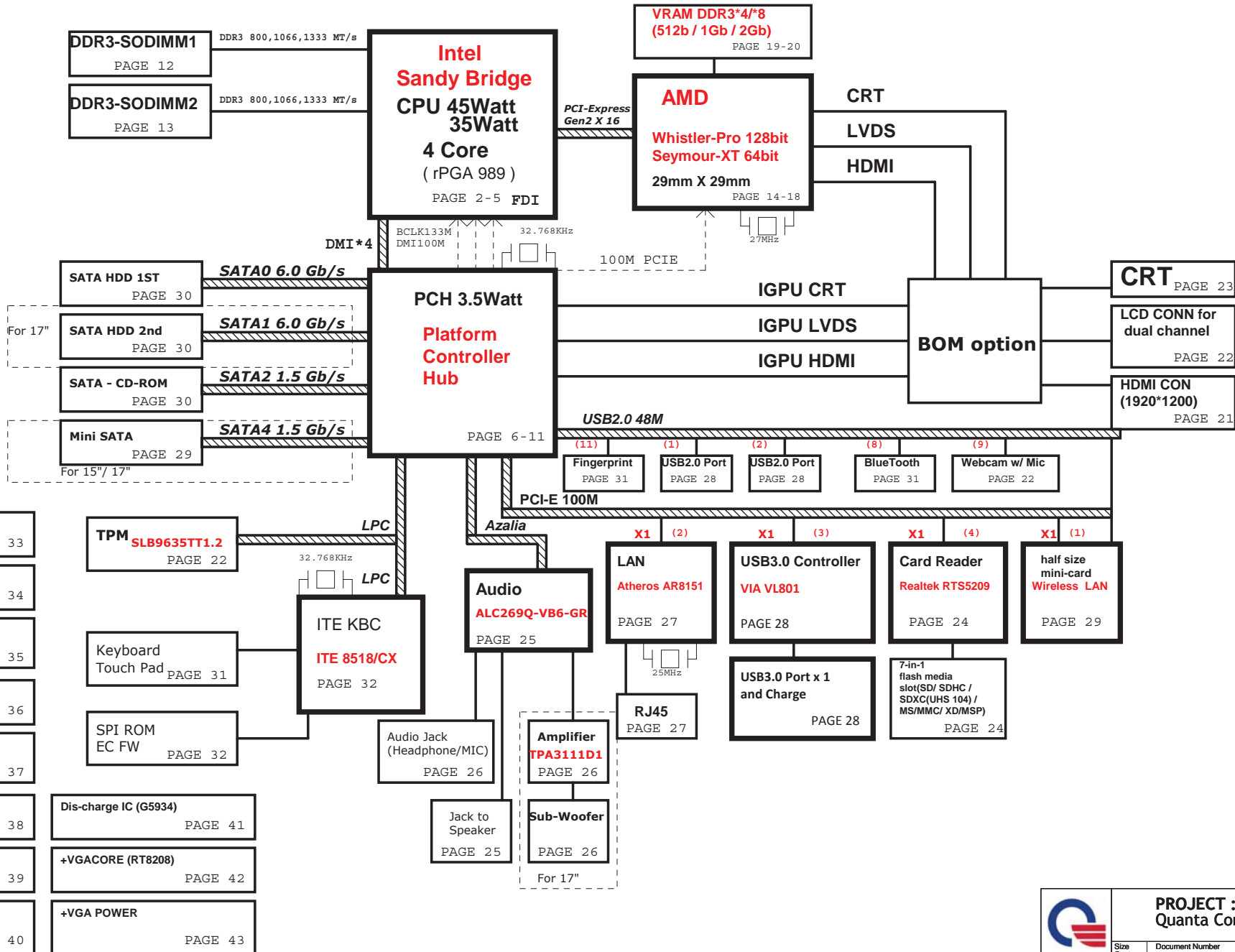


LG2/4 (14"/15.6") MUXLESS and Dis. BLOCK DIAGRAM

01

PCB 8L STACK UP

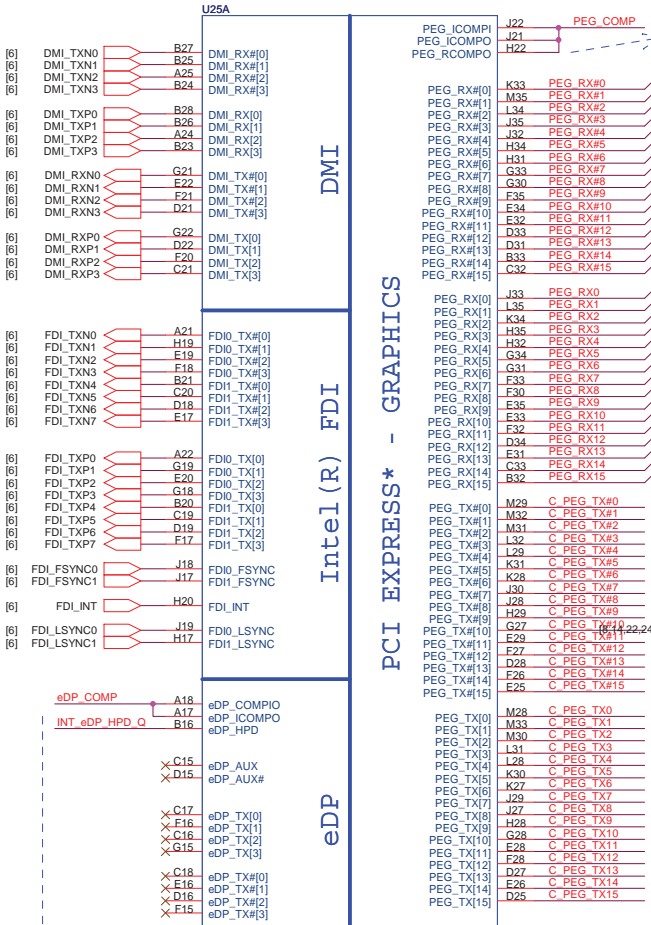
- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(Low)
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



- Charger (OZ8681) PAGE 33
- 3/5VS5 (RT8223M) PAGE 34
- DDR III (RT8207) PAGE 35
- VCCSA (RT8241A) PAGE 36
- +1.05V_VTT(RT8240B) PAGE 37
- +1.05V/+1.8V (G5173) PAGE 38
- CPU Core1 (NCP6132)QC PAGE 39
- CPU Core2 (NCP5911)QC PAGE 40

- TPM SLB9635TT1.2 PAGE 22
- Keyboard Touch Pad PAGE 31
- SPI ROM EC FW PAGE 32
- Dis-charge IC (G5934) PAGE 41
- +VGACORE (RT8208) PAGE 42
- +VGA POWER PAGE 43

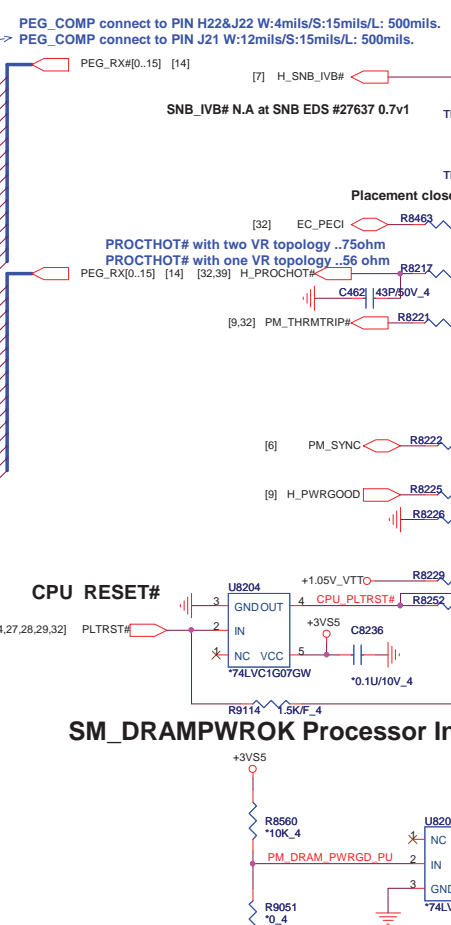
	PROJECT : LG2/4 DIS Quanta Computer Inc.		
	Size Custom	Document Number BLOCK DIAGRAM	Rev 3A
	Date: Wednesday, May 18, 2011	Sheet 1 of 47	



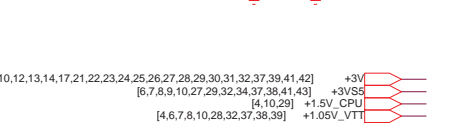
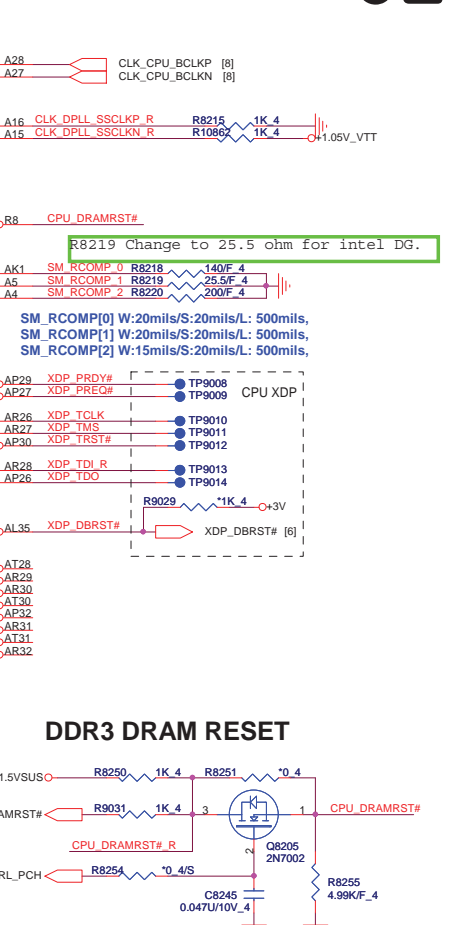
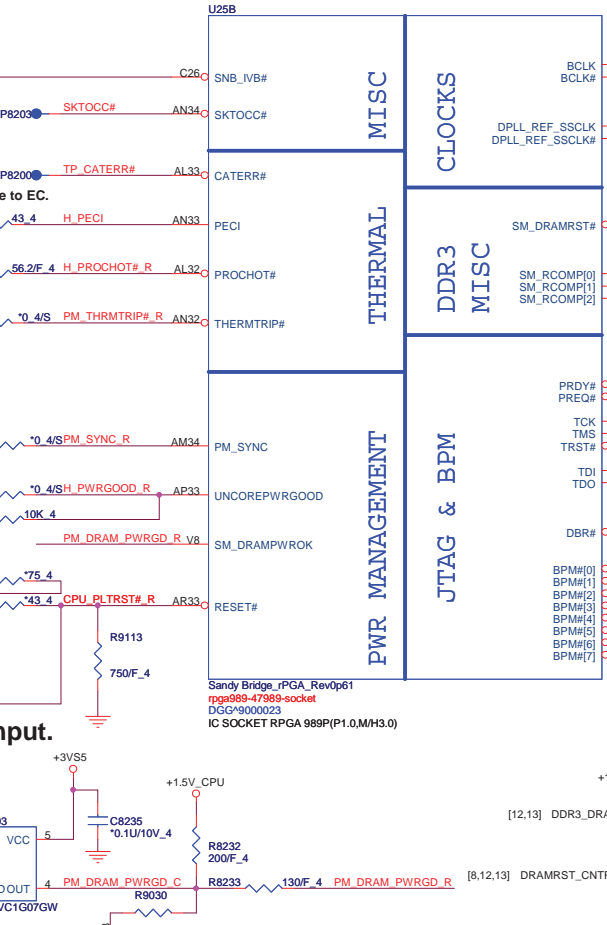
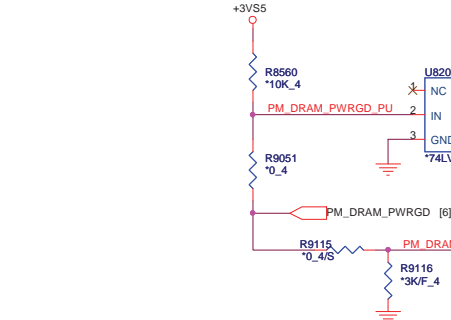
Intel (R) FDI
PCI EXPRESS* - GRAPHICS

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG#9000023
IC SOCKET RPGA 989P(P1.0,MH3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.



SM_DRAMPWROK Processor Input.



FDI disable (DIS only stuff)

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

C PEG TX0	C8227	0.1u/10V_4	PEG TX0	C PEG TX#0	C8212	0.1u/10V_4	PEG TX#0
C PEG TX1	C8228	0.1u/10V_4	PEG TX1	C PEG TX#1	C8213	0.1u/10V_4	PEG TX#1
C PEG TX2	C8229	0.1u/10V_4	PEG TX2	C PEG TX#2	C8214	0.1u/10V_4	PEG TX#2
C PEG TX3	C8230	0.1u/10V_4	PEG TX3	C PEG TX#3	C8215	0.1u/10V_4	PEG TX#3
C PEG TX4	C8231	0.1u/10V_4	PEG TX4	C PEG TX#4	C8216	0.1u/10V_4	PEG TX#4
C PEG TX5	C8232	0.1u/10V_4	PEG TX5	C PEG TX#5	C8217	0.1u/10V_4	PEG TX#5
C PEG TX6	C8233	0.1u/10V_4	PEG TX6	C PEG TX#6	C8218	0.1u/10V_4	PEG TX#6
C PEG TX7	C8234	0.1u/10V_4	PEG TX7	C PEG TX#7	C8219	0.1u/10V_4	PEG TX#7
C PEG TX8	C8235	0.1u/10V_4	PEG TX8	C PEG TX#8	C8220	0.1u/10V_4	PEG TX#8
C PEG TX9	C8236	0.1u/10V_4	PEG TX9	C PEG TX#9	C8221	0.1u/10V_4	PEG TX#9
C PEG TX10	C8237	0.1u/10V_4	PEG TX10	C PEG TX#10	C8222	0.1u/10V_4	PEG TX#10
C PEG TX11	C8238	0.1u/10V_4	PEG TX11	C PEG TX#11	C8223	0.1u/10V_4	PEG TX#11
C PEG TX12	C8239	0.1u/10V_4	PEG TX12	C PEG TX#12	C8224	0.1u/10V_4	PEG TX#12
C PEG TX13	C8240	0.1u/10V_4	PEG TX13	C PEG TX#13	C8225	0.1u/10V_4	PEG TX#13
C PEG TX14	C8241	0.1u/10V_4	PEG TX14	C PEG TX#14	C8226	0.1u/10V_4	PEG TX#14
C PEG TX15	C8242	0.1u/10V_4	PEG TX15	C PEG TX#15	C8227	0.1u/10V_4	PEG TX#15

0.22uF AC coupling Caps for PCIe GEN1/2/3

DP & PEG Compensation

+1.05V_VTT0 R9016 10K_4 INT_eDP_HPD_Q

+1.05V_VTT0 R8243 24.9F_4 eDP_COMP

+1.05V_VTT0 R8244 24.9F_4 PEG_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

PROCHOT# with two VR topology ..100ohm
PROCHOT# with one VR topology ..62 ohm

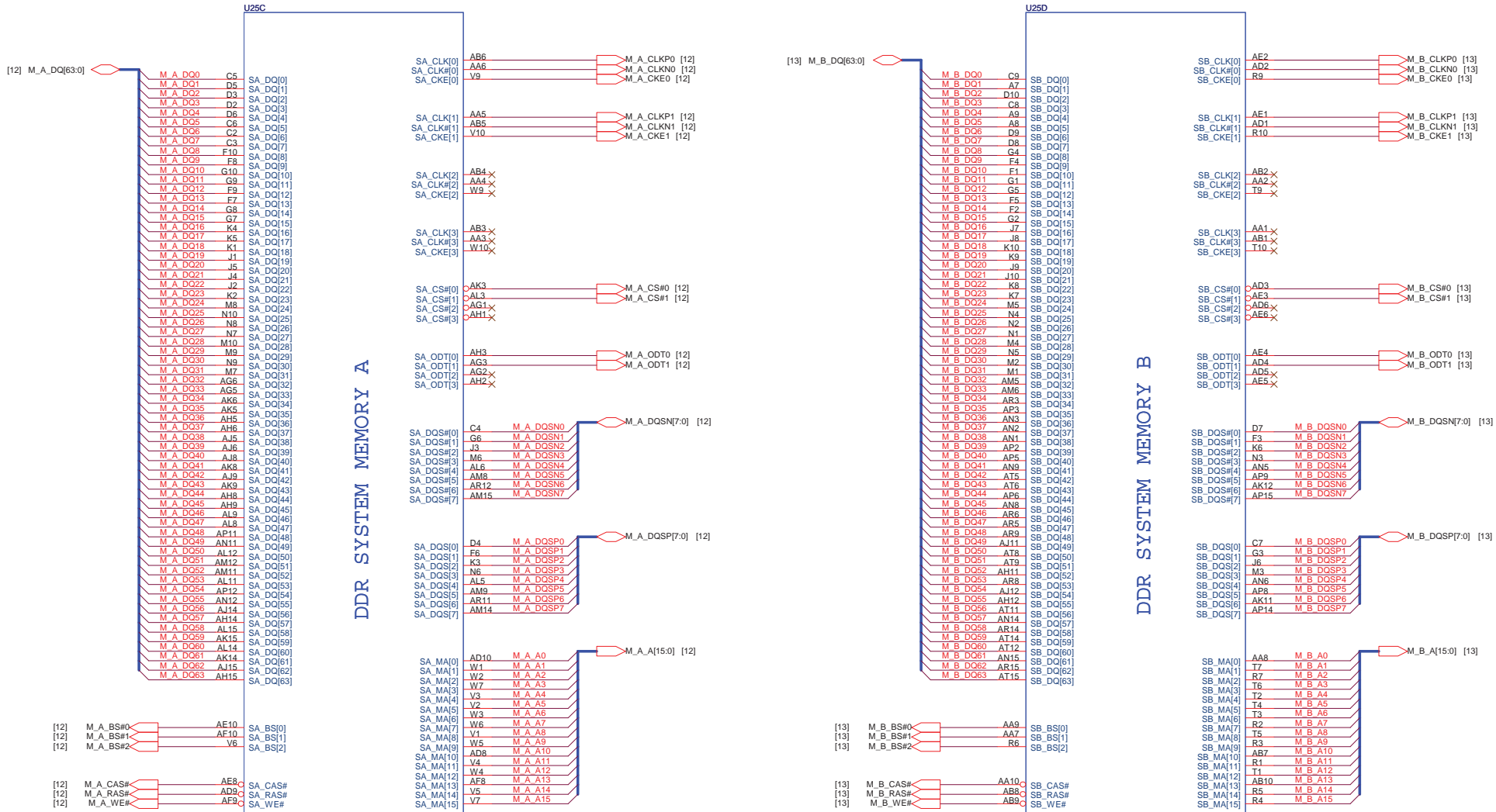
H PROCHOT#	R8238	62_4
XDP_TDO	R8239	51_4
XDP_TMS	R8240	51_4
XDP_TDI_R	R8241	51_4
XDP_PREQ#	R8242	51_4
XDP_TCLK	R8243	51_4
XDP_TRST#	R8244	51_4

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom Document Number **SNB 1/4 (PCIE&DMI&FDI)** Rev 3A

Date: Wednesday, May 18, 2011 Sheet 2 of 47

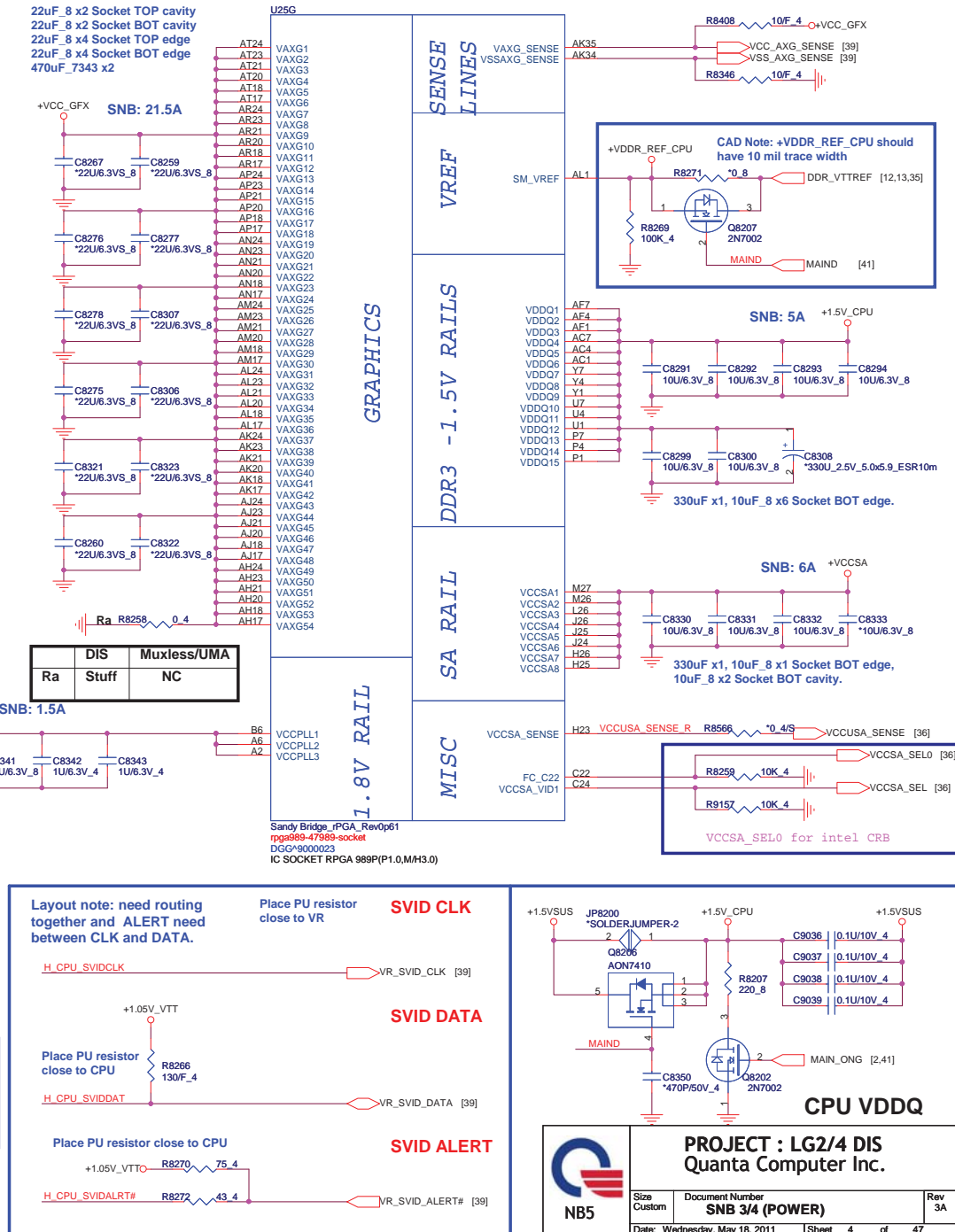
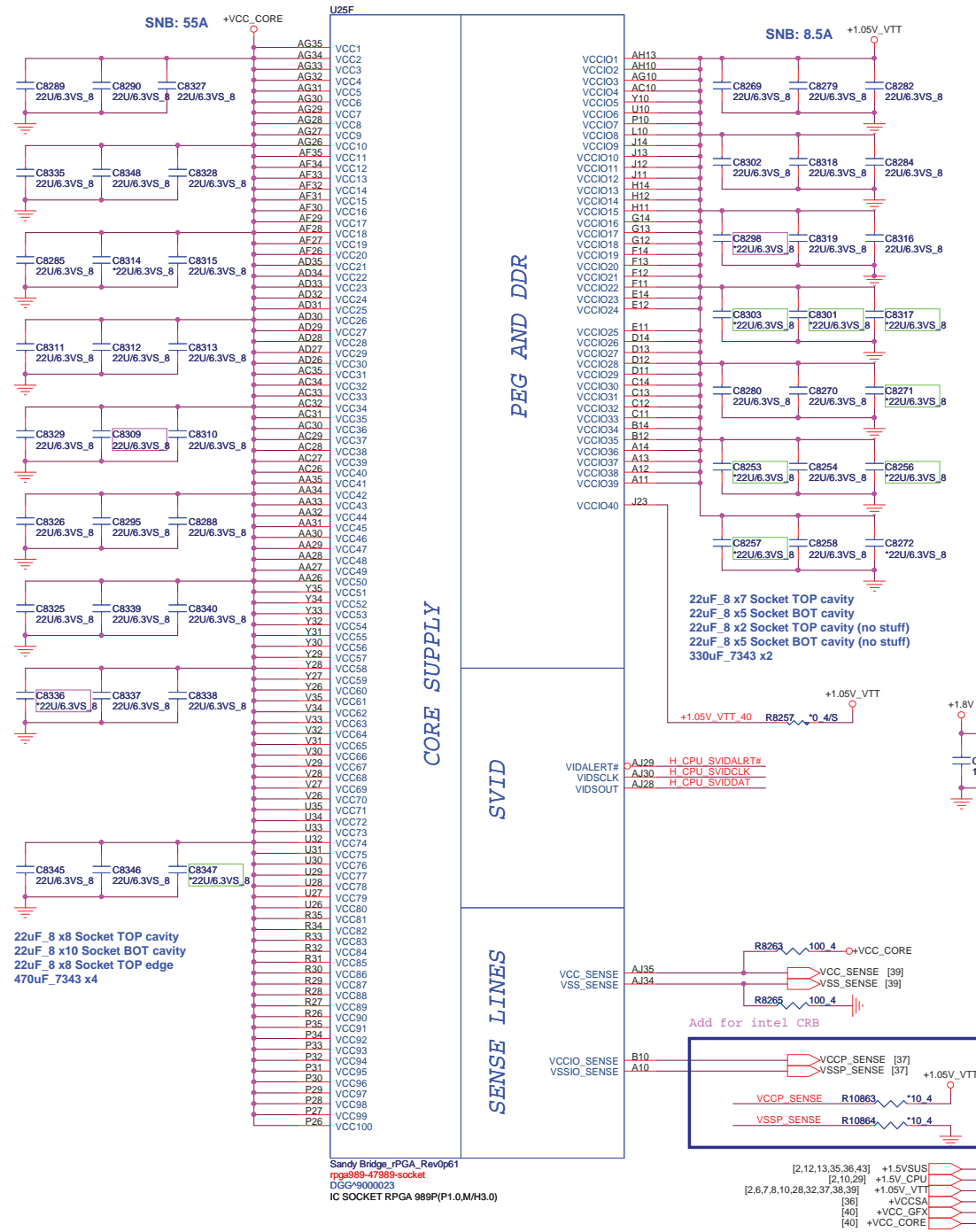
Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000023
 IC SOCKET RPGA 989P(P1.0,MH3.0)

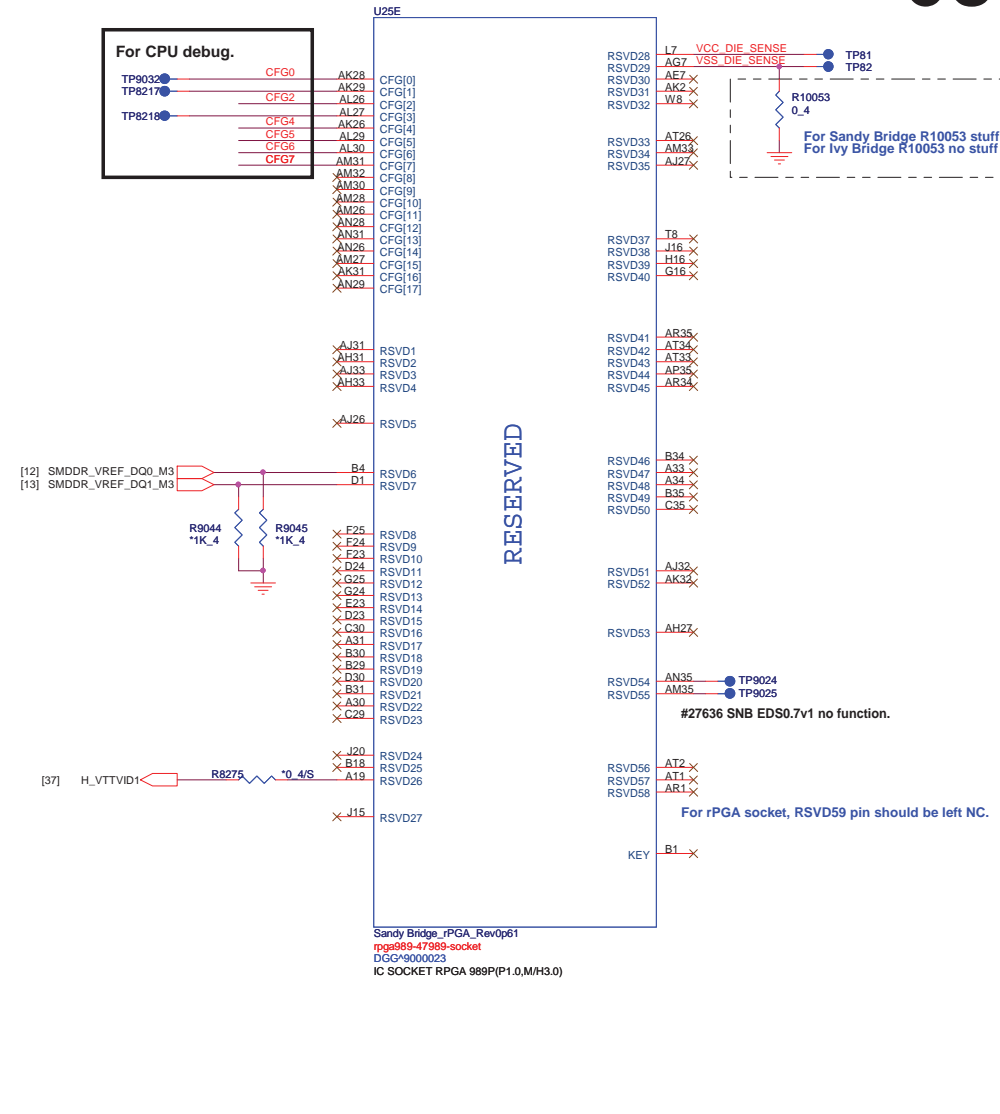
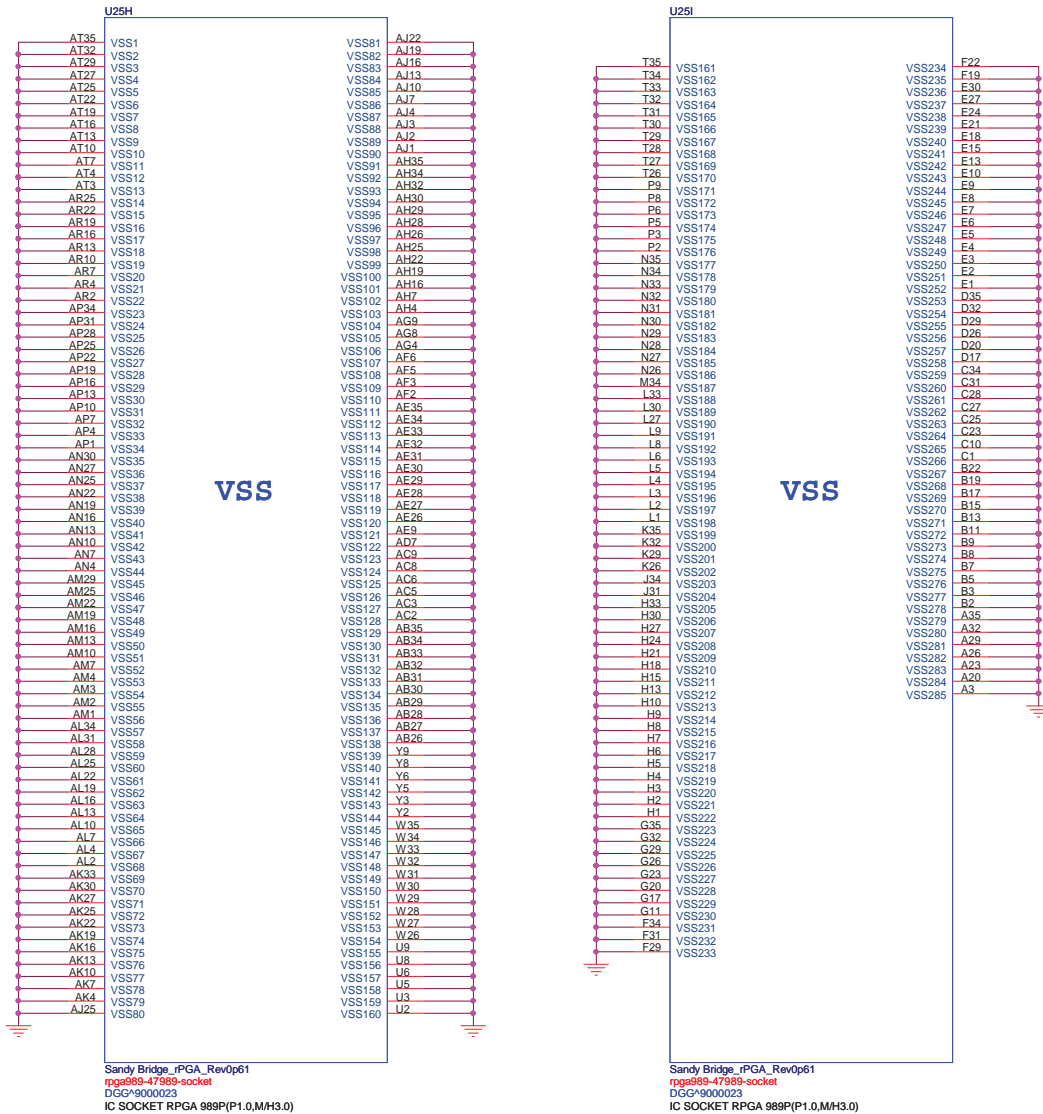
Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000023
 IC SOCKET RPGA 989P(P1.0,MH3.0)

	PROJECT : LG2/4 DIS		Rev 3A
	Quanta Computer Inc.		
	Size Custom	Document Number SNB 2/4 (DDR3 I/F)	
Date: Wednesday, May 18, 2011		Sheet 3 of 47	



Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

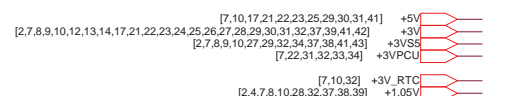
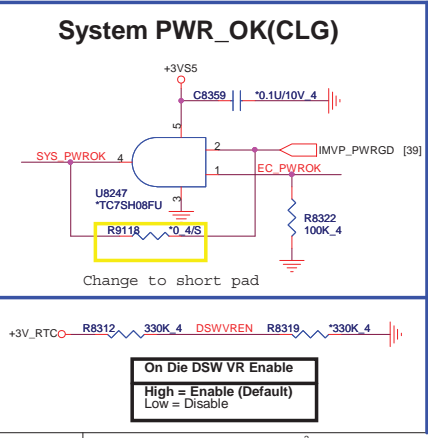
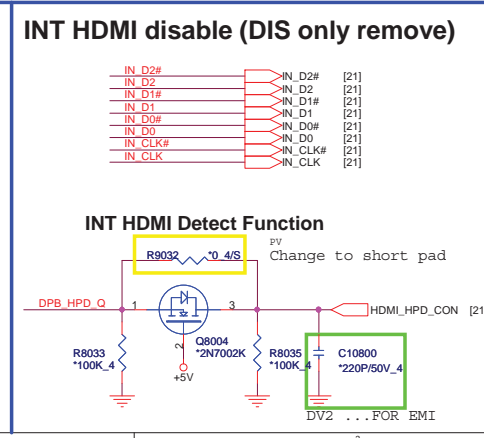
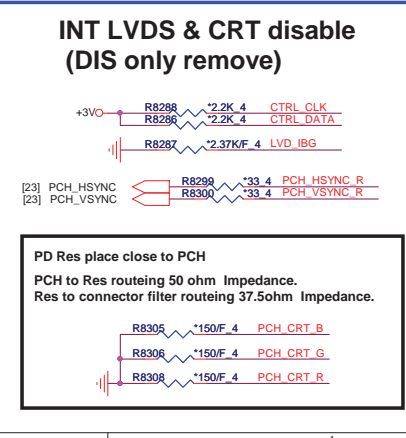
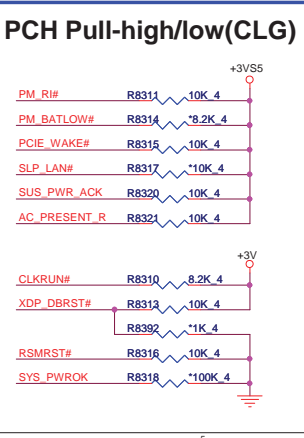
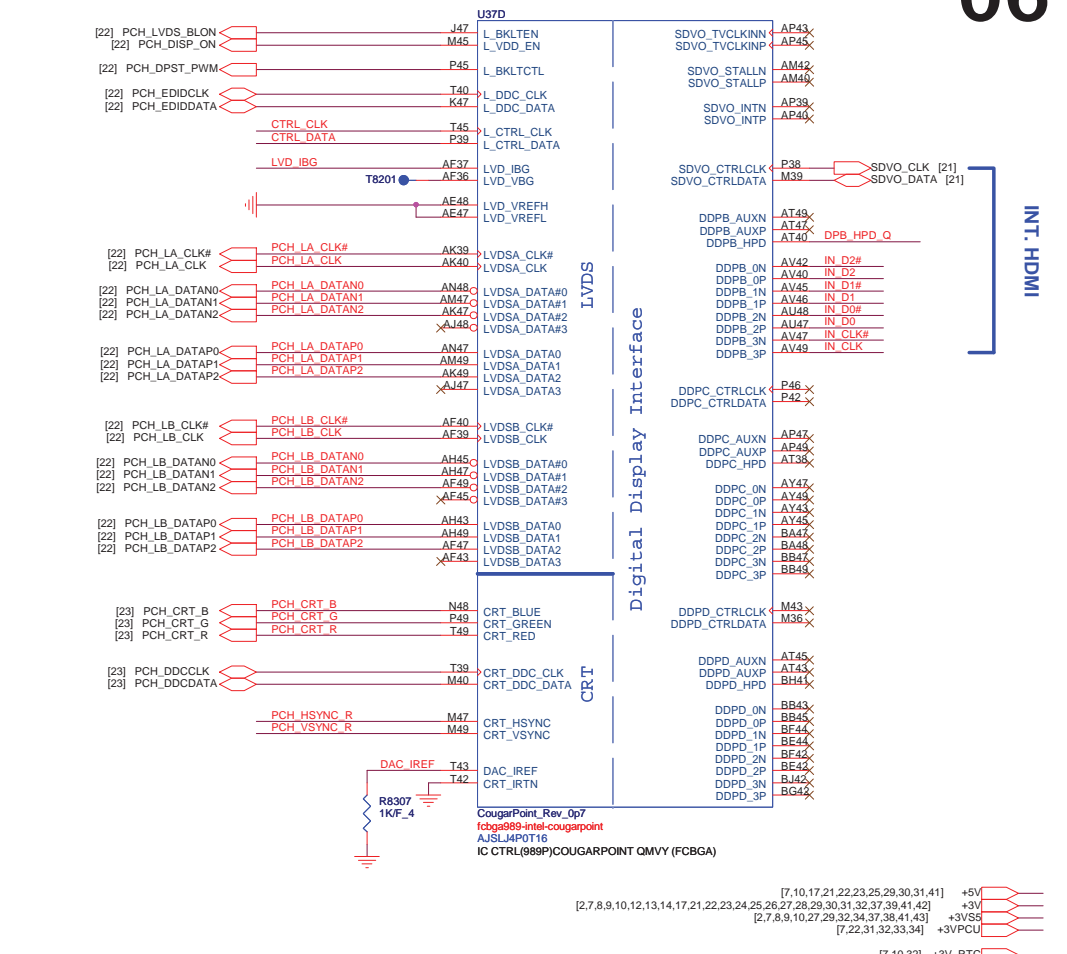
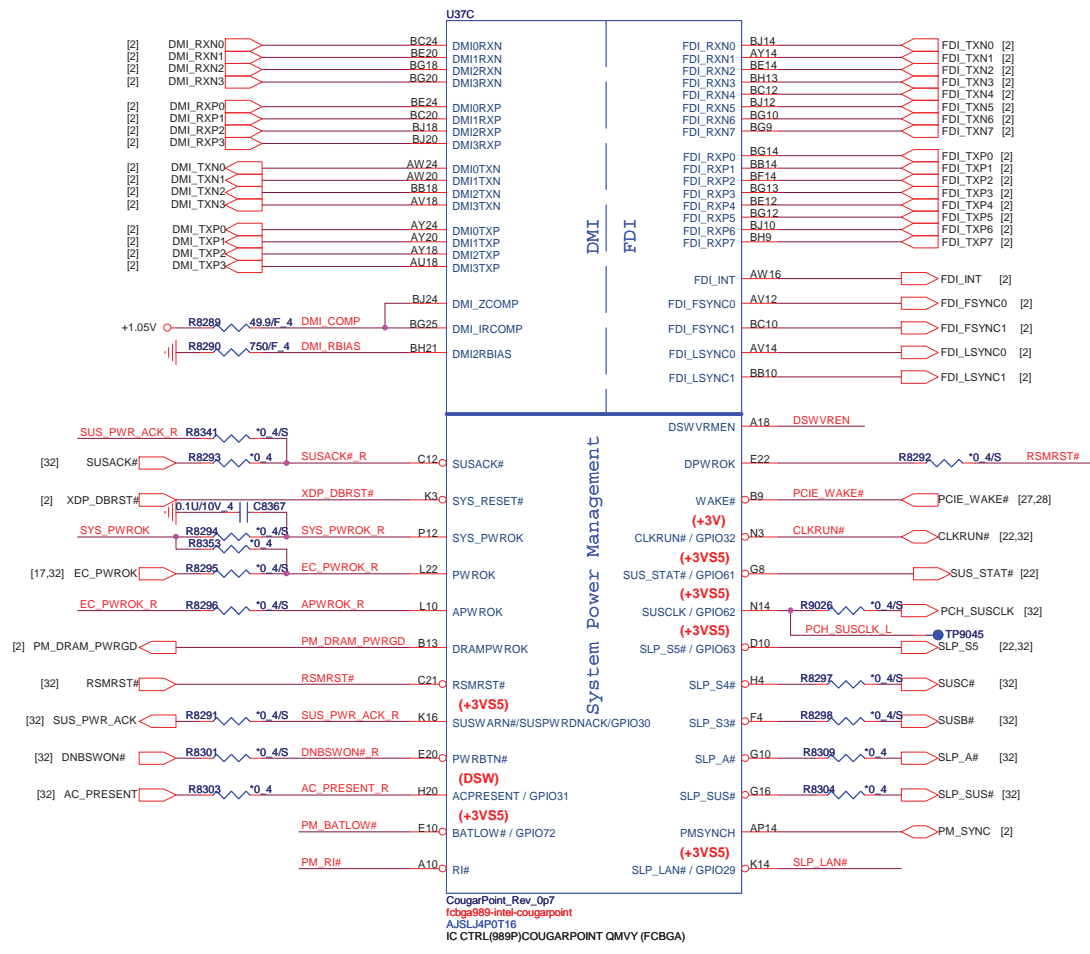
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom Document Number **SNB 4/4 (GND)** Rev 3A

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PROJECT : LG2/4 DIS Quanta Computer Inc.

Size Custom	Document Number	Rev
PCH 1/6 (DMI/FDI/VIDEO)		3A
Date: Wednesday, May 18, 2011		Sheet 6 of 47

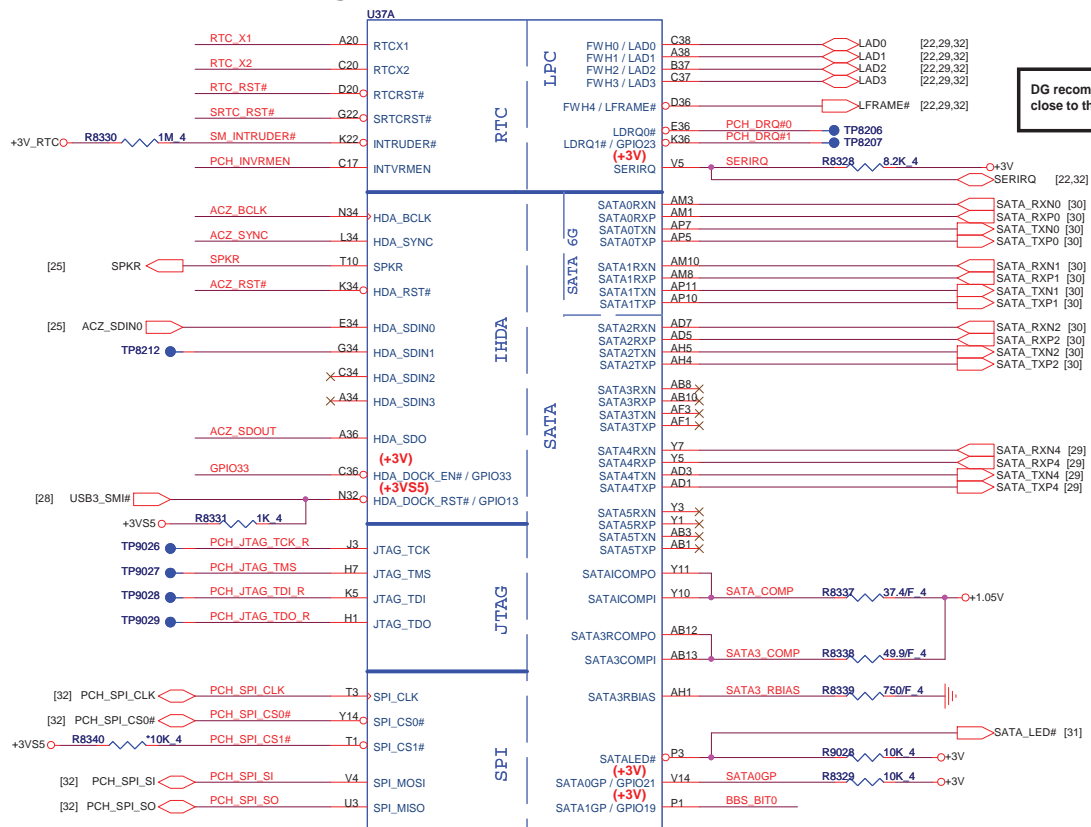
INT_HDMI

Digital Display Interface

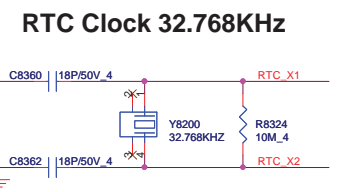
CRT

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

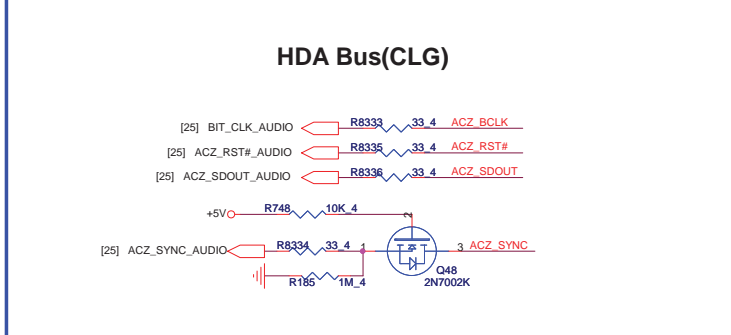
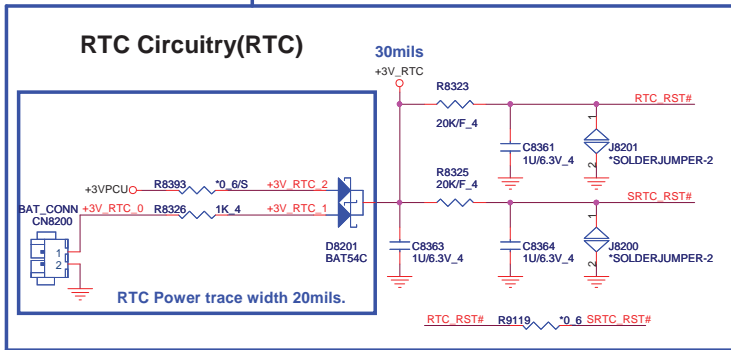
Cougar Point (HDA, JTAG, SATA)



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

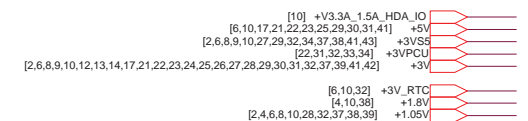


HDD0 (SATA3 6.0Gb/s)
 2nd HDD0 (SATA3 6.0Gb/s)
 ODD
 MINISATA (SATA1 1.5Gb/s)



PCH Strap Table

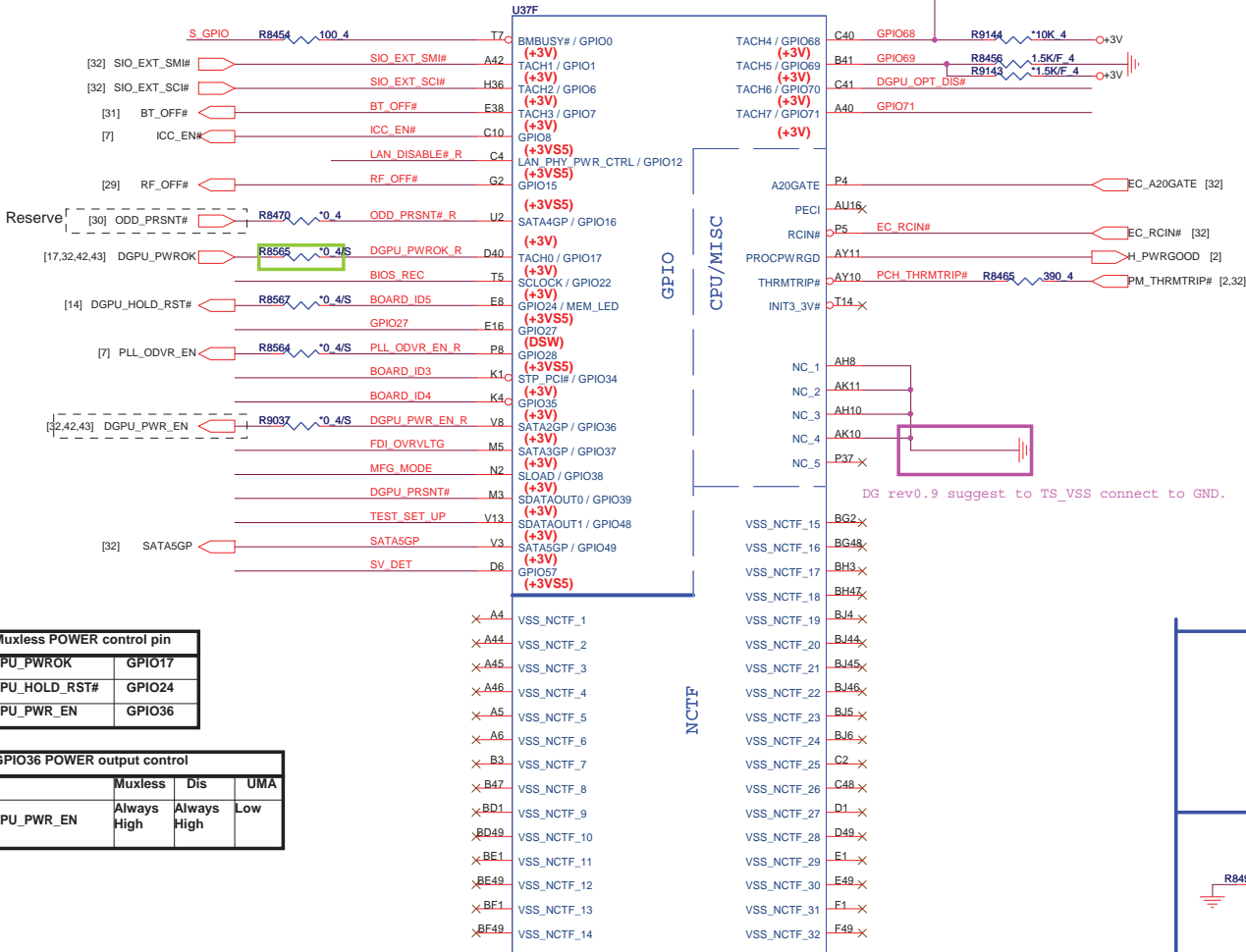
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWR0K		
GNT2# / GPIO53	ESI strap (Server only)	PWR0K	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWR0K	0 = Disable (Internal pull-down 20kohm)	
NV_CLE	DMI Termination voltage	PWR0K	weak pull-down 20kohm	
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	
HDA_SDO	Flash Descriptor Security	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable	



PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 3A
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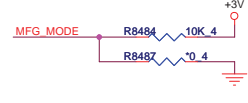
Cougar Point (GPIO,VSS_NCTF,RSVD)



	Ra	Rb
UMA/Muxless	NC	Stuff
DIS	Stuff	NC

DGPU_OPT_DIS#:
High : Muxless.
Low: Discrete.

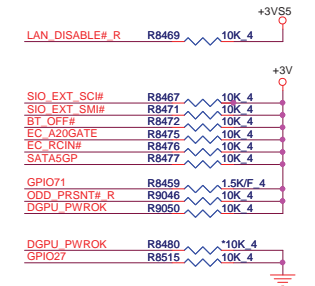
MFG-TEST



SGPIO



GPIO Pull-up/Pull-down(CLG)



Muxless POWER control pin

DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

GPIO36 POWER output control

	Muxless	Dis	UMA
DGPU_PWR_EN	Always High	Always High	Low

RF_OFF# R8468 1K 4 +3V55

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

TEST SET UP R8486 10K 4 +3V

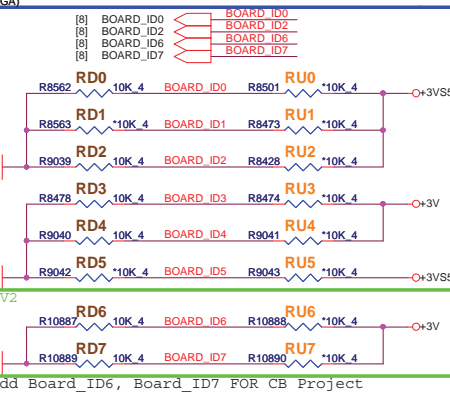
SV_SET_UP High = Strong (Default)

SV_DET R8482 10K 4 +3V

TEST DETECT Low = Default

BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID6	ID7	GPIO70	GPIO39
LG/CB	0=LG 1=CB								
15.6" / 14"			14" 15" 17" LG6						
			ID2	1 0 0 1					
17"			ID3	0 0 1 1					
doby								1=YES 0=NO	
DIS/Muxless								1= Muxless 0=DIS	
UMA/VGA								1= VGA 0=UMA	



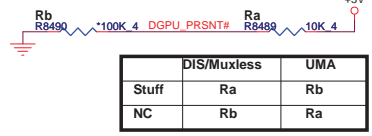
DGPU_PWR_EN R8492 200K/F 4 +3V

DMI TERMINATION VOLTAGE OVERRIDE Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI_OVRVLGT R8494 1K 4 +3V

FDI TERMINATION VOLTAGE OVERRIDE LOW - Tx, Rx terminated to same voltage

GFX Present



	DIS/Muxless	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : LG2/4 DIS
Quanta Computer Inc.

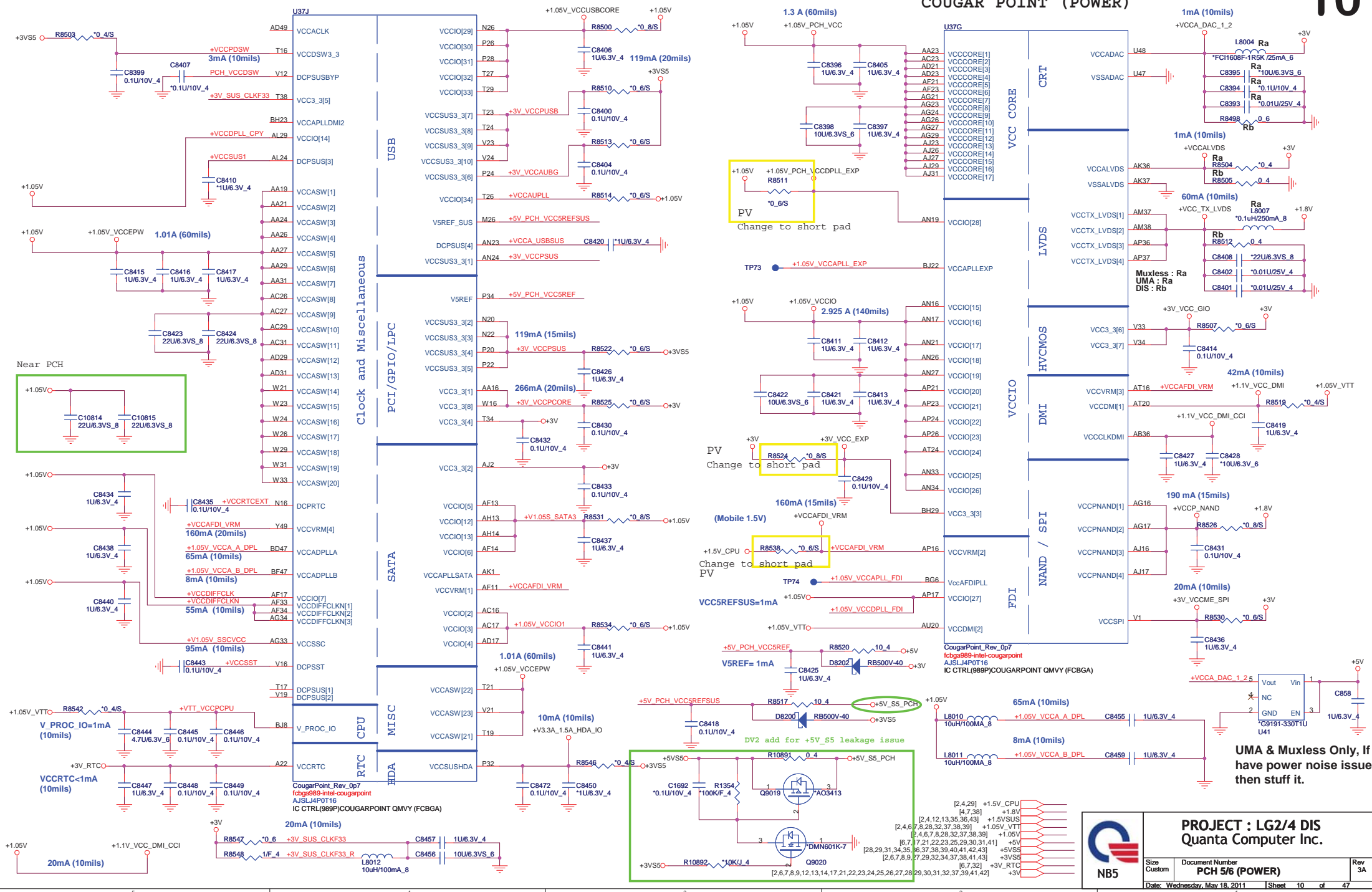
NBS

Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 3A

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Cougar Point-M (POWER)

COUGAR POINT (POWER)



UMA & Muxless Only, If have power noise issue then stuff it.

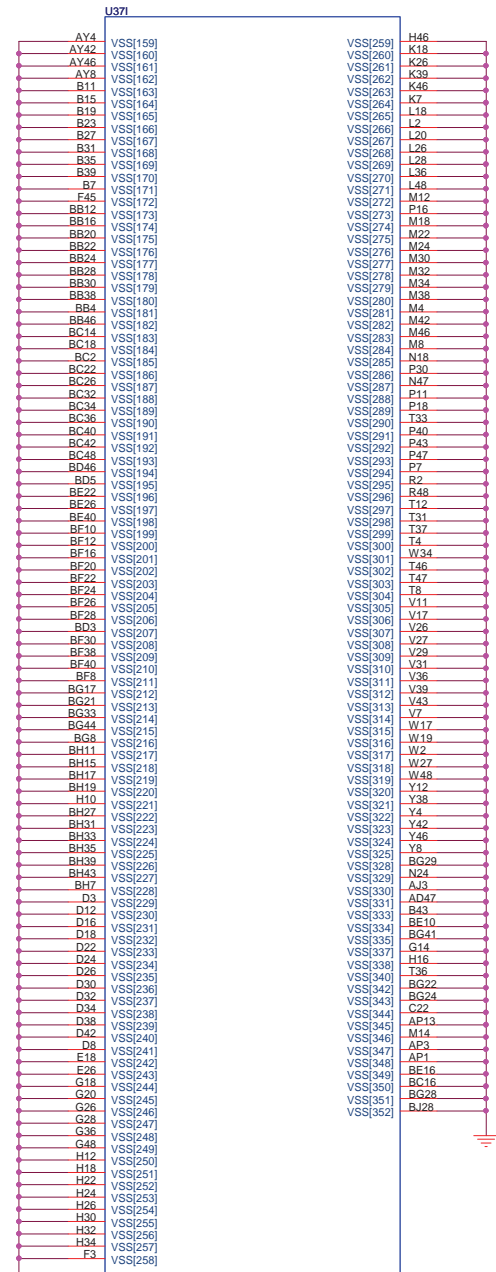
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	3A
Date: Wednesday, May 18, 2011		Sheet 10 of 47

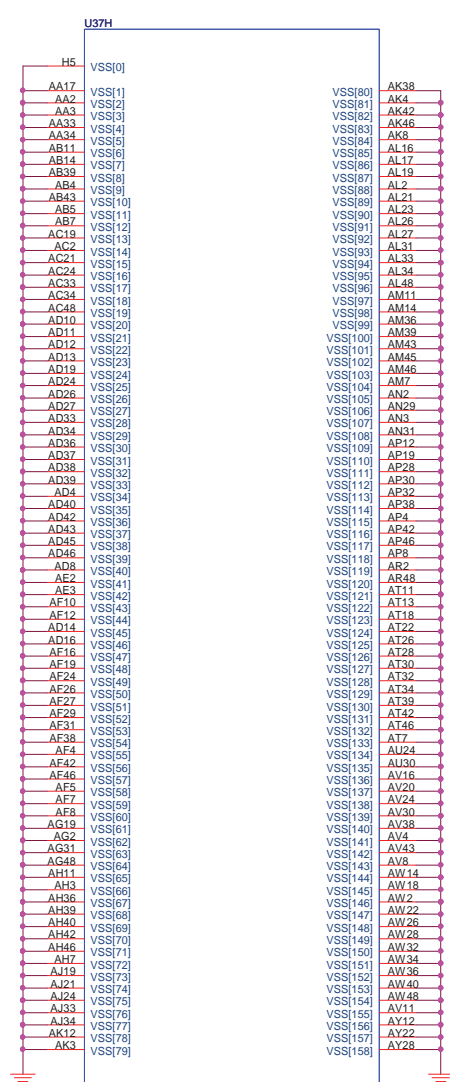
- [2,4,29] +1.5V_CPU
- [4,7,38] +1.8V
- [2,4,6,7,8,28,32,37,38,39] +1.5VSUS
- [4,6,7,8,28,32,37,38,39] +1.05V_VTT
- [6,7,21,22,23,25,29,30,31,41] +5V
- [28,29,31,34,35,36,37,38,39,40,41,42,43] +5VSS
- [2,6,7,8,9,27,29,32,34,37,38,41,43] +3VSUS
- [6,7,32] +3V_RTC
- [2,6,7,8,9,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

IBEX PEAK-M (GND)


IBEX PEAK-M (GND)

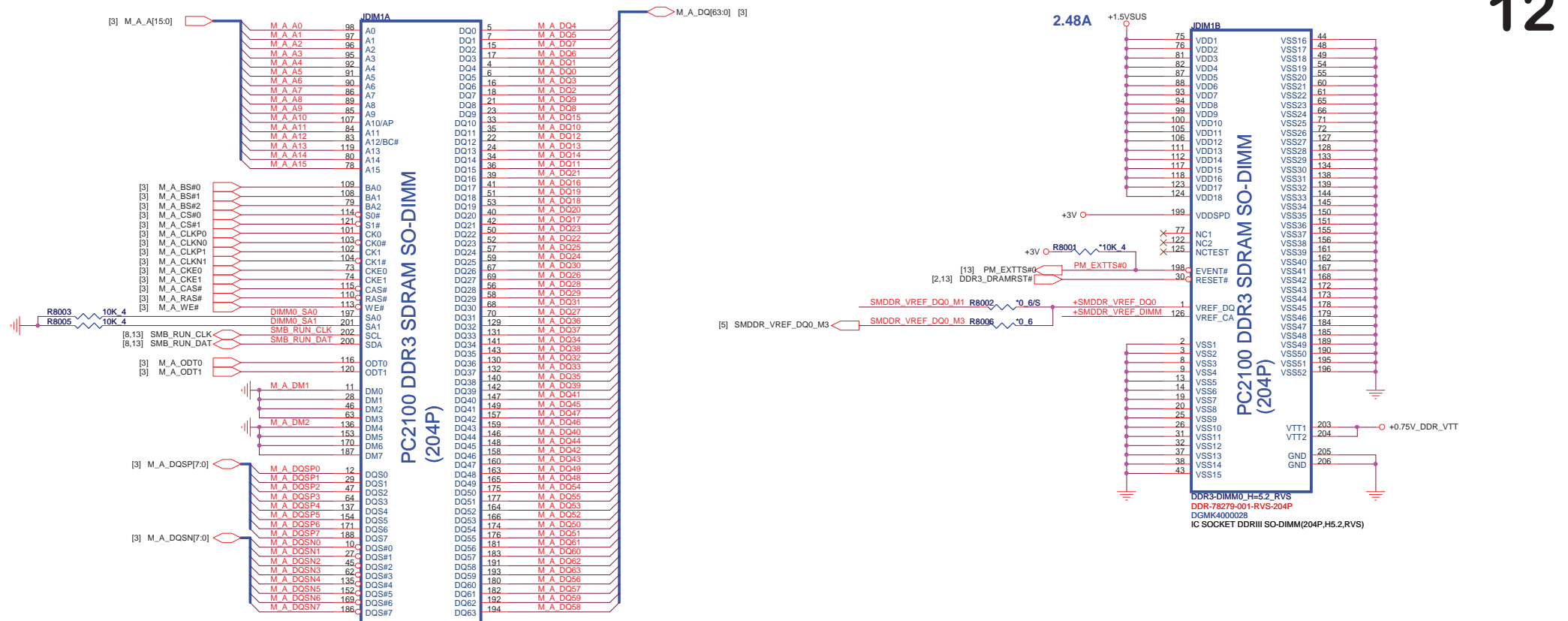


CougarPoint_Rev_0p7

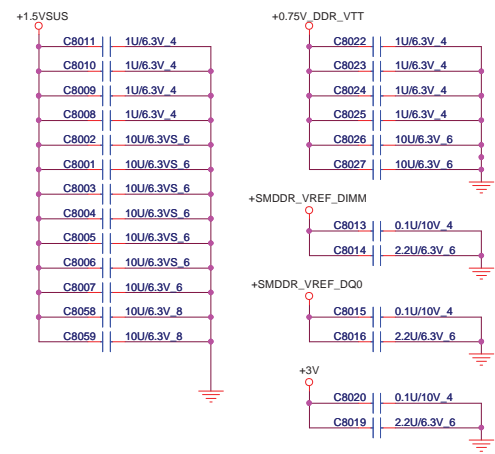


CougarPoint_Rev_0p7

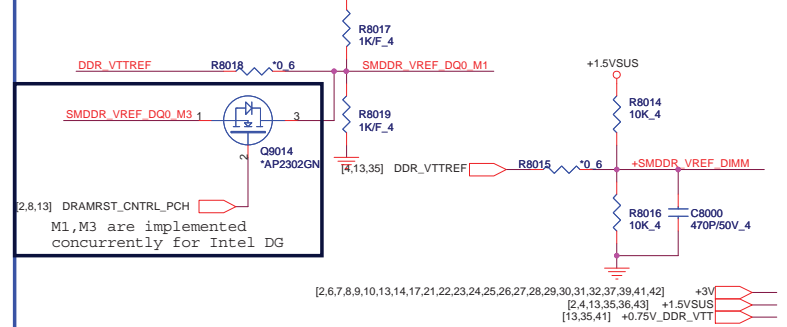
	PROJECT : LG2/4 DIS		Rev 3A
	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	
Date: Wednesday, May 18, 2011		Sheet 11 of 47	



Place these Caps near So-Dimm0.



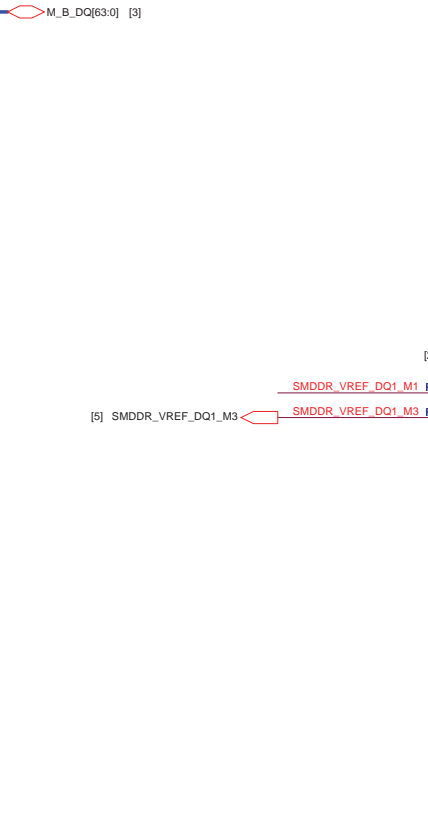
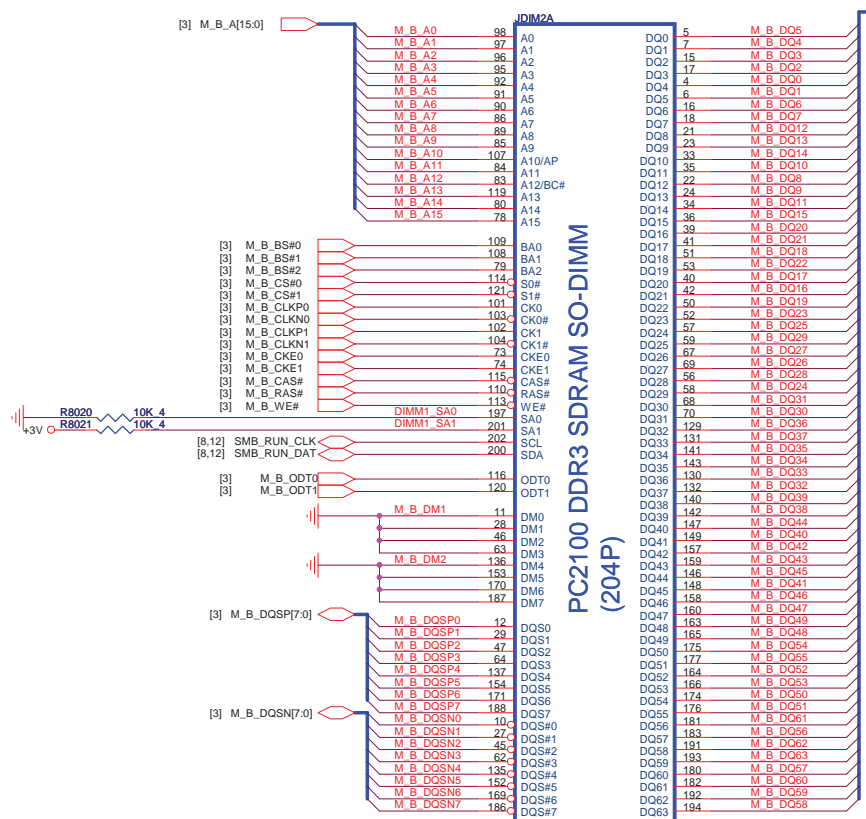
VREF DQ0 M1 Solution



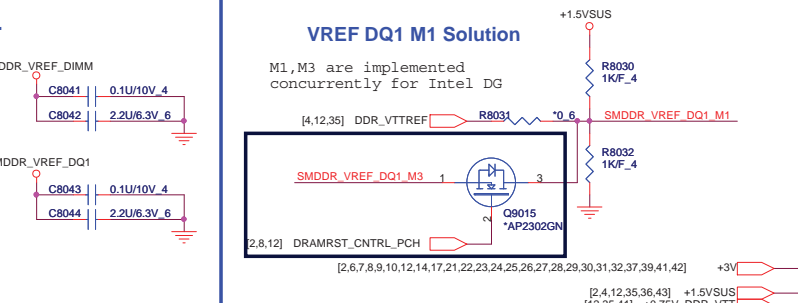
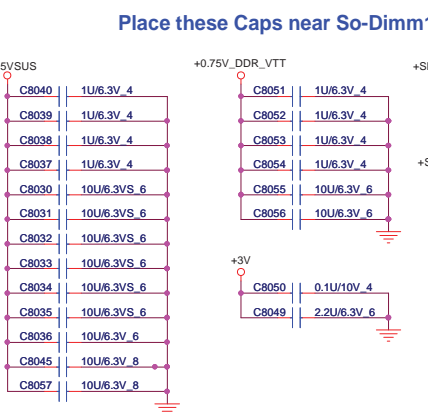
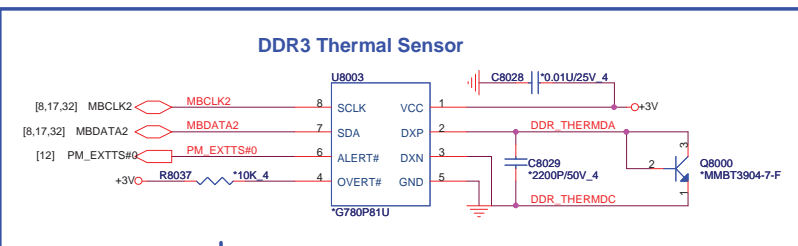
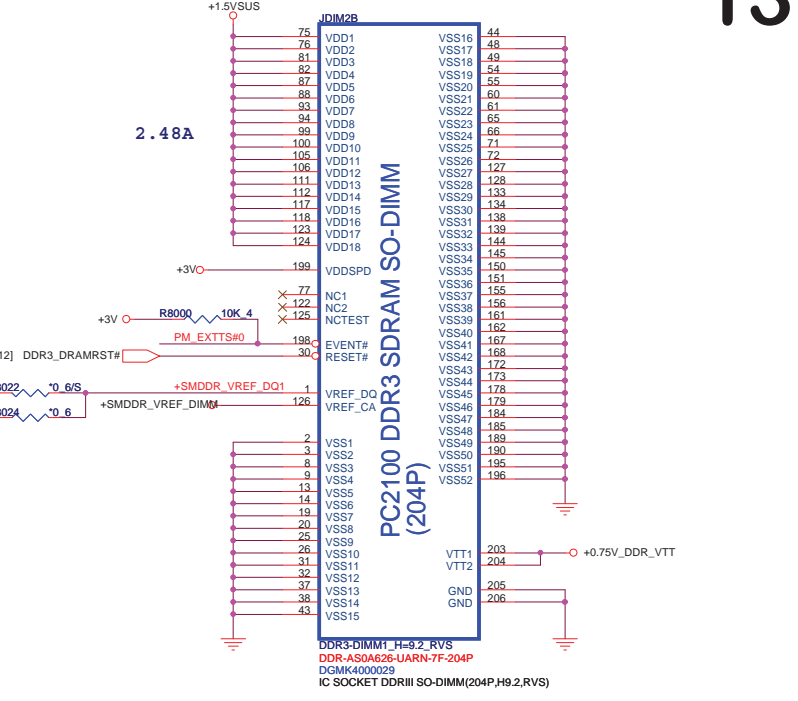
**PROJECT : LG2/4 DIS
Quanta Computer Inc.**

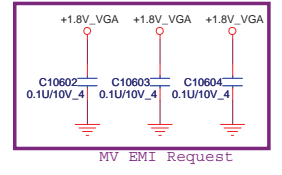
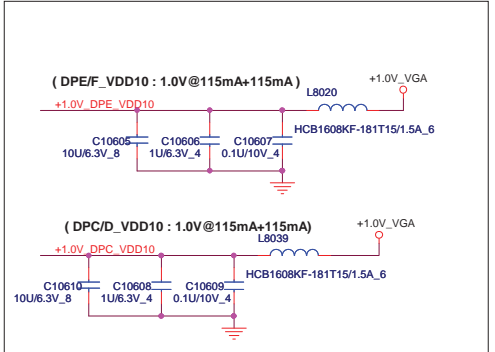
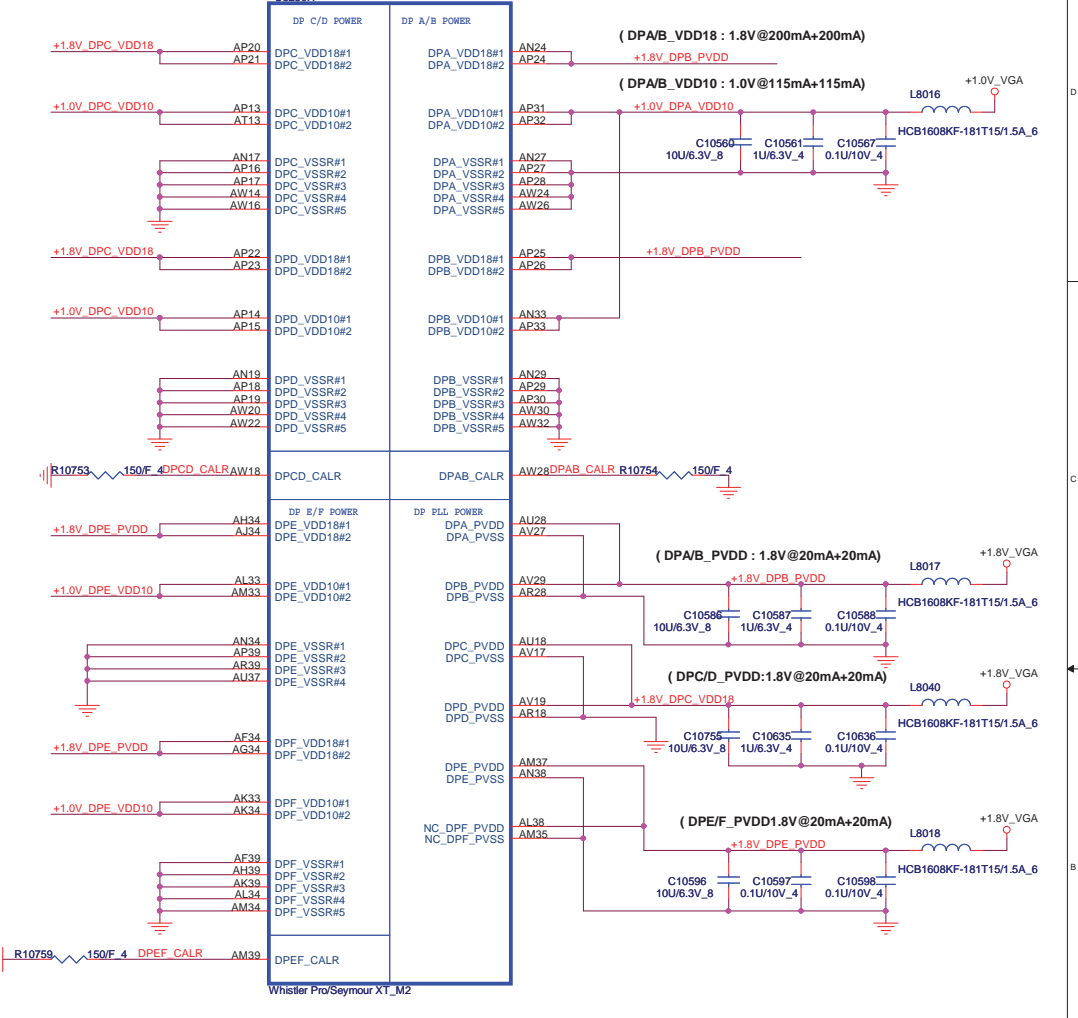
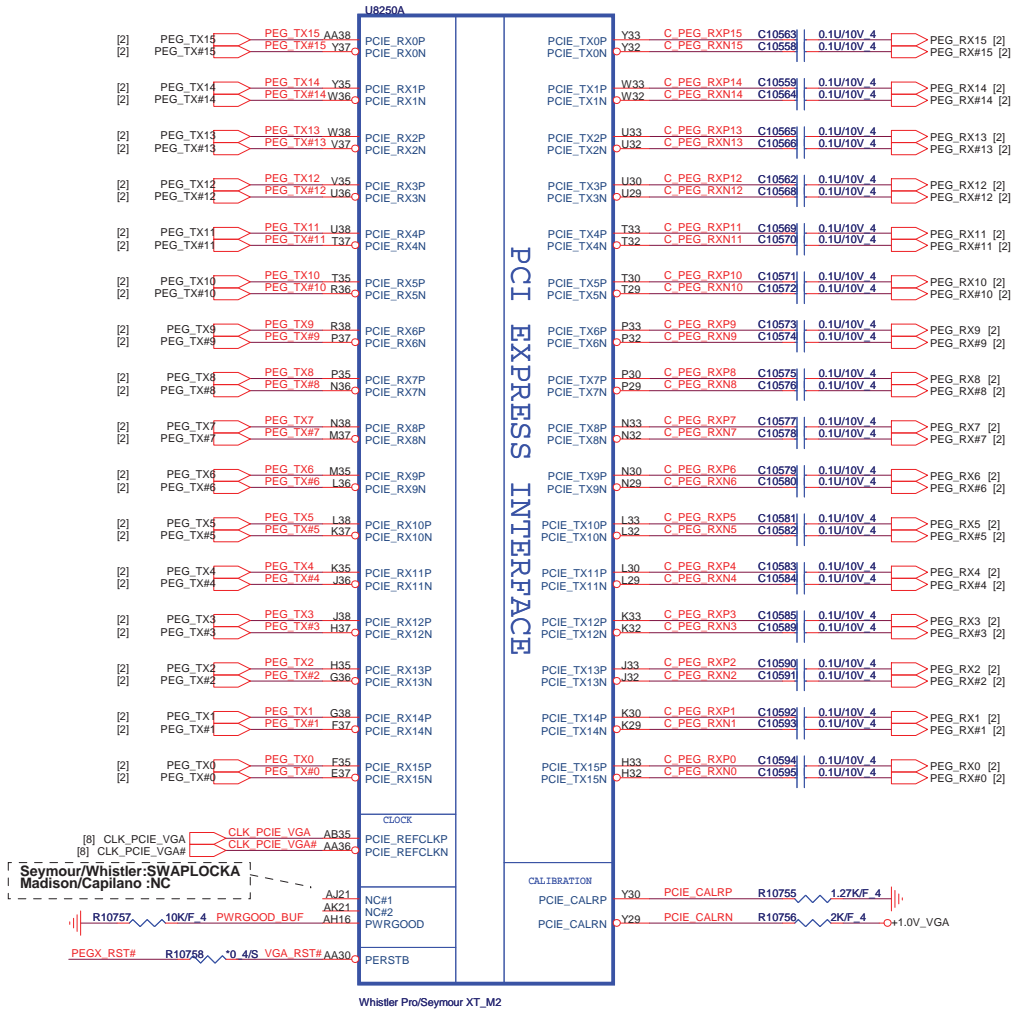
NBS

Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	Rev 3A
Date: Wednesday, May 18, 2011	Sheet 12	of 47



DDR3-DIMM1_H=9.2_RVS
 DDR-AS0A626-UARN-7F-204P
 DGMK4000029
 IC SOCKET DDRIII SO-DIMM(204P,H9.2,RVS)



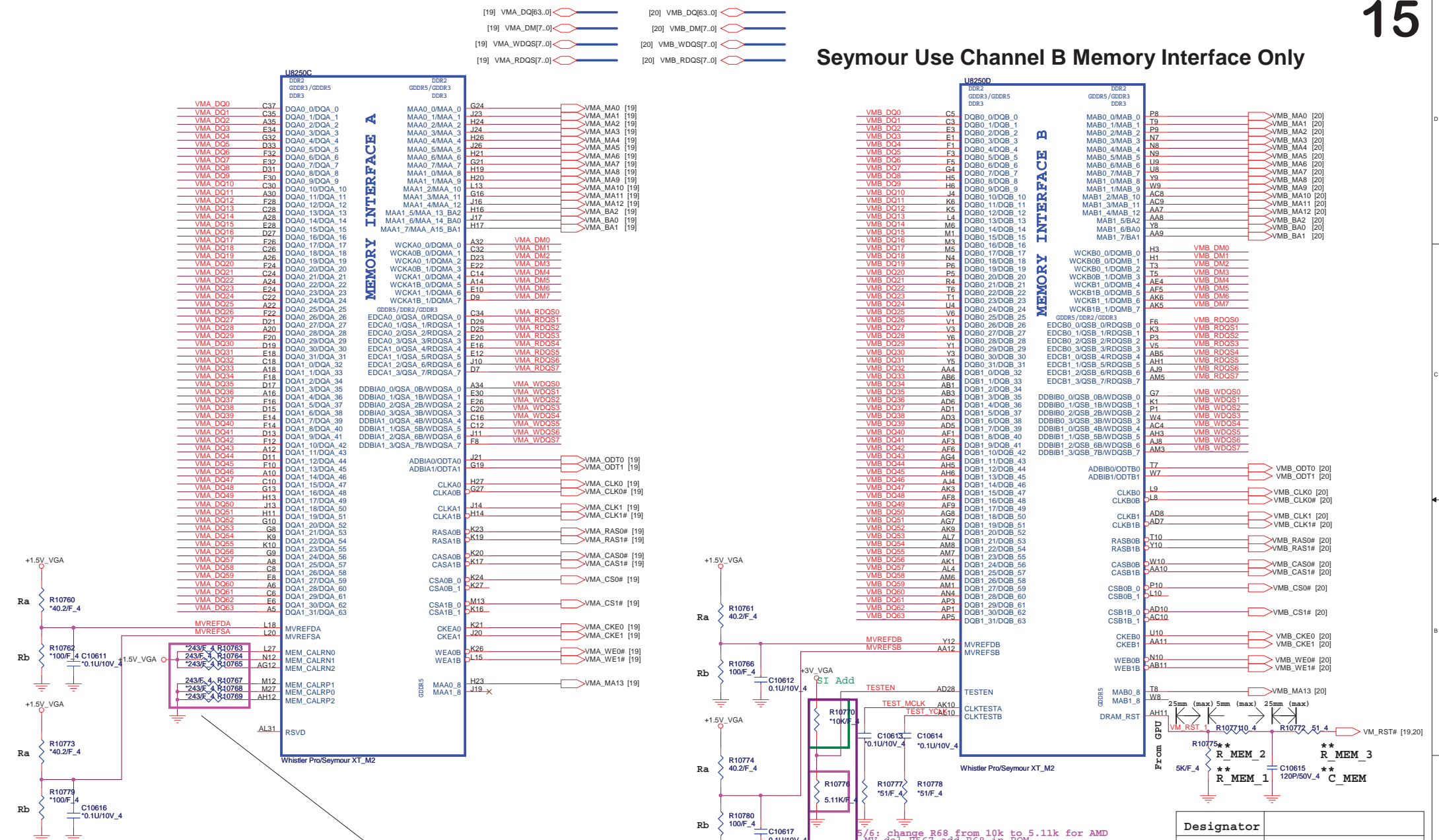


[2,6,7,8,9,10,12,13,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V
 [16,18,43] +1.8V_VGA
 [16,17,18,43] +1.0V_VGA

PROJECT : LG2/4 DIS Quanta Computer Inc.

NB5 Size Custom Document Number **AMD Whistler (MEM)1/5** Rev 3A
 Date: Wednesday, May 18, 2011 Sheet 14 of 47

Seymour Use Channel B Memory Interface Only



DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	For Whistler	For Seymour
MEM_CALRNP0	stuff	NC
MEM_CALRNP1	stuff	stuff
MEM_CALRNP2	stuff	NC
MVREFDA	stuff	NC
MVREFSA	stuff	NC

Place all these components very close to the GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

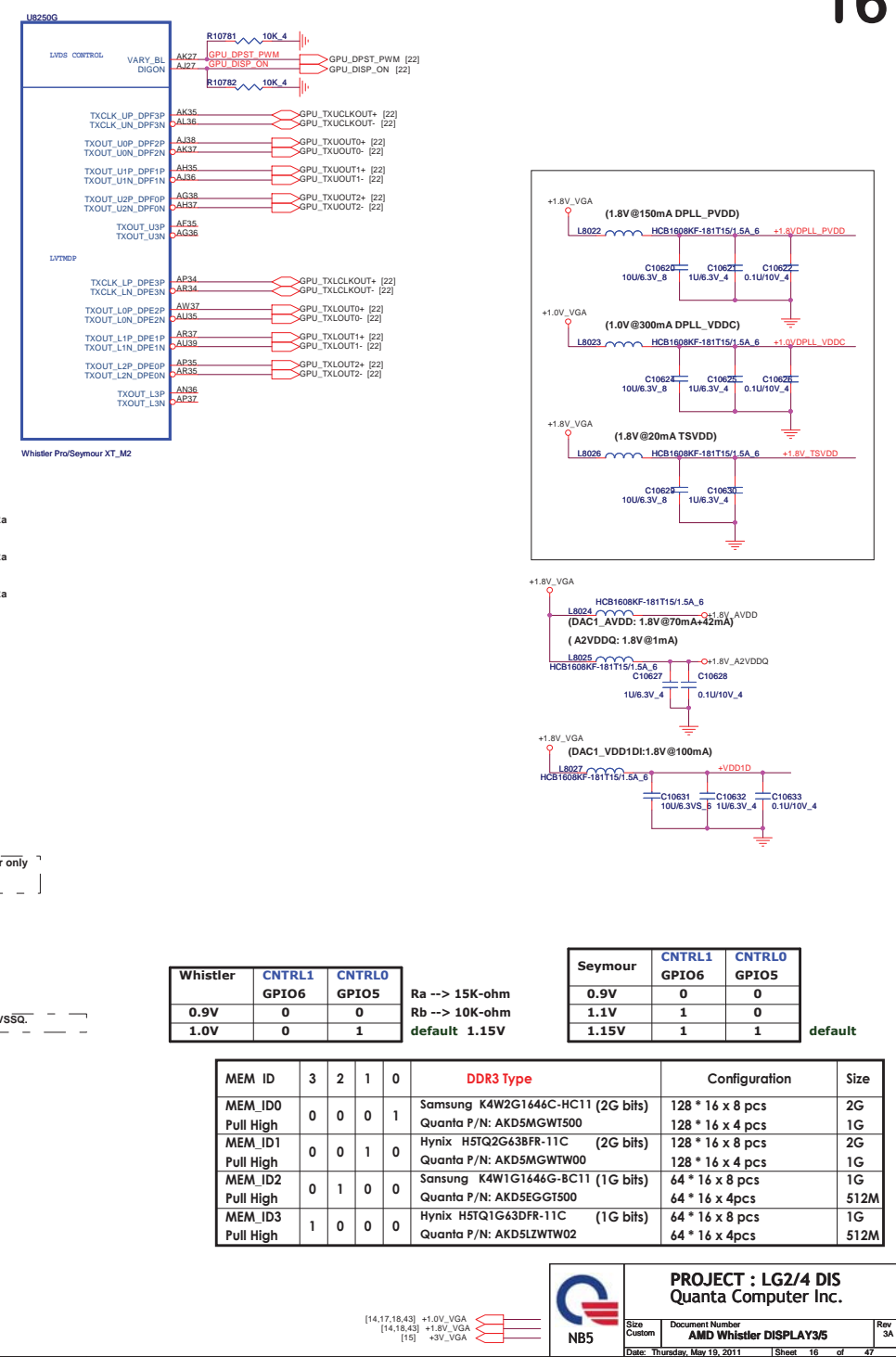
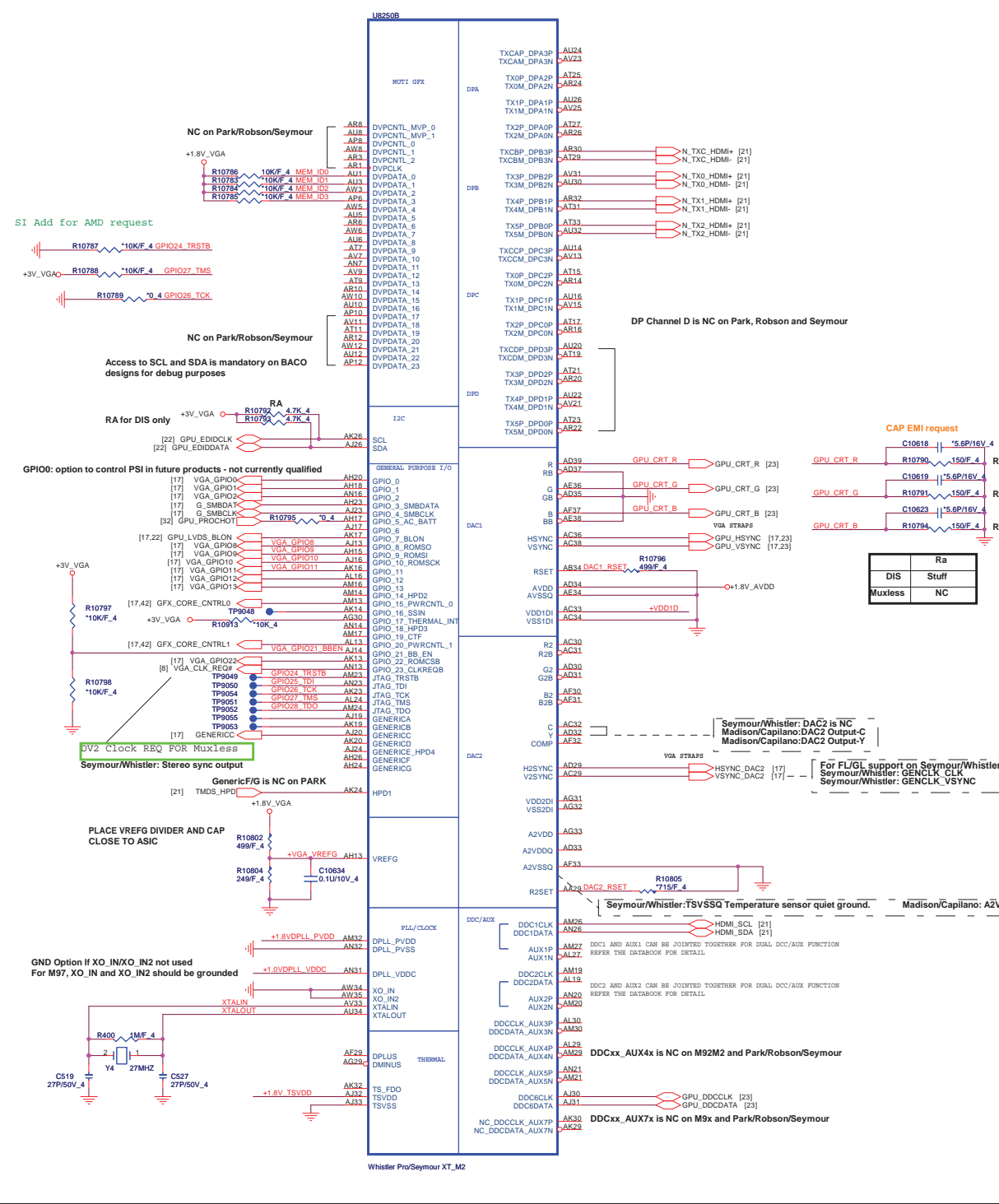
** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	Value
R_MEM_1	5K
R_MEM_2	10R
R_MEM_3	51R
C_MEM	120pF

PROJECT : LG2/4 DIS Quanta Computer Inc.

Size Custom Document Number **AMD Whistler (MEM)2/5** Rev 3A

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CAP EMI request

GPU_CRT_R	C10618	5.6P/16V_4	Ra
GPU_CRT_G	C10619	5.6P/16V_4	Ra
GPU_CRT_B	C10623	5.6P/16V_4	Ra
GPU_CRT_B	R10794	150F/4	Ra

	Ra
DIS	Stuff
Muxless	NC

Whistler	CNTRL1 GPIO6	CNTRLO GPIO5
0.9V	0	0
1.0V	0	1

Ra --> 15K-ohm
Rb --> 10K-ohm
default 1.15V

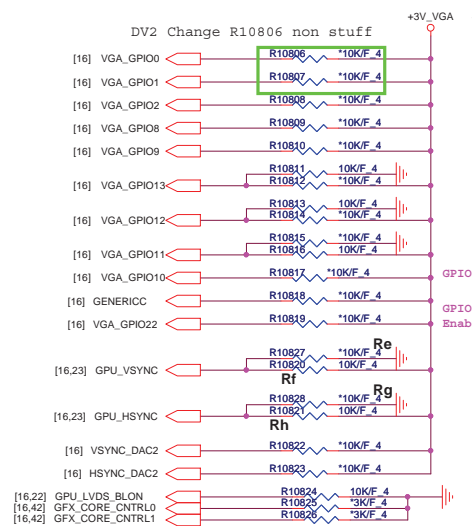
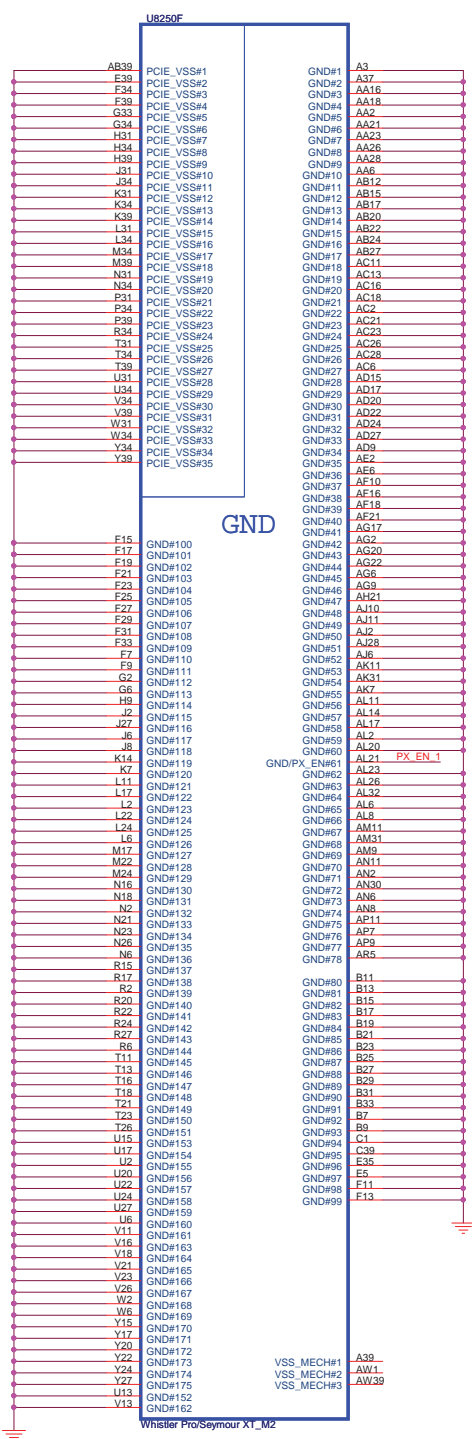
Seymour	CNTRL1 GPIO6	CNTRLO GPIO5	default
0.9V	0	0	
1.1V	1	0	
1.15V	1	1	default

MEM ID	3	2	1	0	DDR3 Type	Configuration	Size
MEM_ID0	0	0	0	1	Samsung K4W2G1646C-HC11 (2G bits)	128 * 16 x 8 pcs	2G
Pull High	0	0	0	1	Quanta P/N: AKD5MGWT500	128 * 16 x 4 pcs	1G
MEM_ID1	0	0	1	0	Hynix H5TQ2G63BFR-11C (2G bits)	128 * 16 x 8 pcs	2G
Pull High	0	0	1	0	Quanta P/N: AKD5MGWTW00	128 * 16 x 4 pcs	1G
MEM_ID2	0	1	0	0	Samsung K4W1G1646G-BC11 (1G bits)	64 * 16 x 8 pcs	1G
Pull High	0	1	0	0	Quanta P/N: AKD5EGGT500	64 * 16 x 4pcs	512M
MEM_ID3	1	0	0	0	Hynix H5TQ1G63DFR-11C (1G bits)	64 * 16 x 8 pcs	1G
Pull High	1	0	0	0	Quanta P/N: AKD5LZWTW02	64 * 16 x 4pcs	512M

PROJECT : LG2/4 DIS
Quanta Computer Inc.

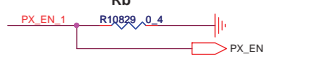
Size Custom Document Number **AMD Whistler DISPLAY/5** Rev 3A

Date: Thursday, May 19, 2011 Sheet 16 of 47



	Re	Rf	Rg	Rh
PX4.0	Stuff	NC	Stuff	NC
Discrete	NC	Stuff	NC	Stuff

Reserve for support BACO mode

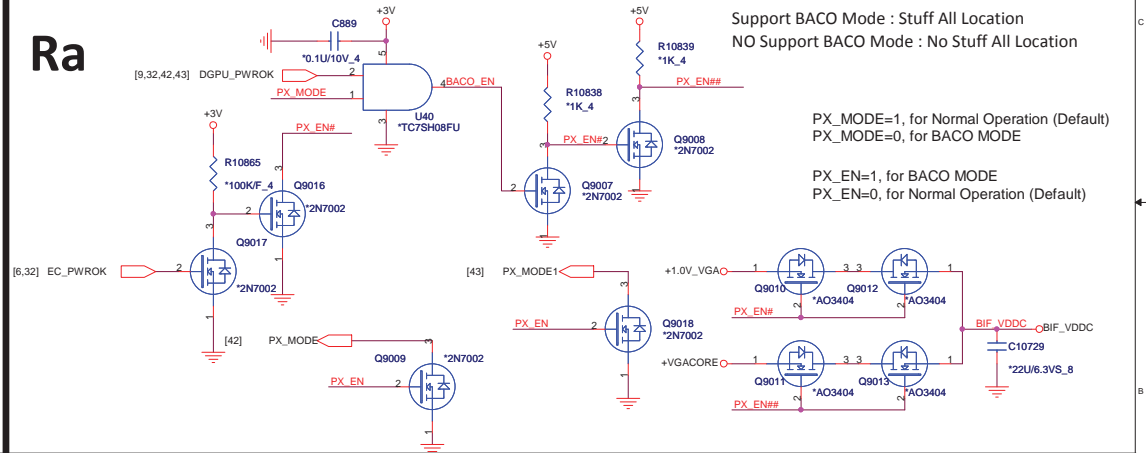


	Ra	Rb
BACO Functions	Stuff	Stuff 5.1k
NO BACO Functions	NC	Stuff 0 ohm

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

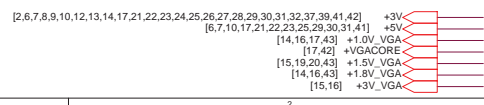
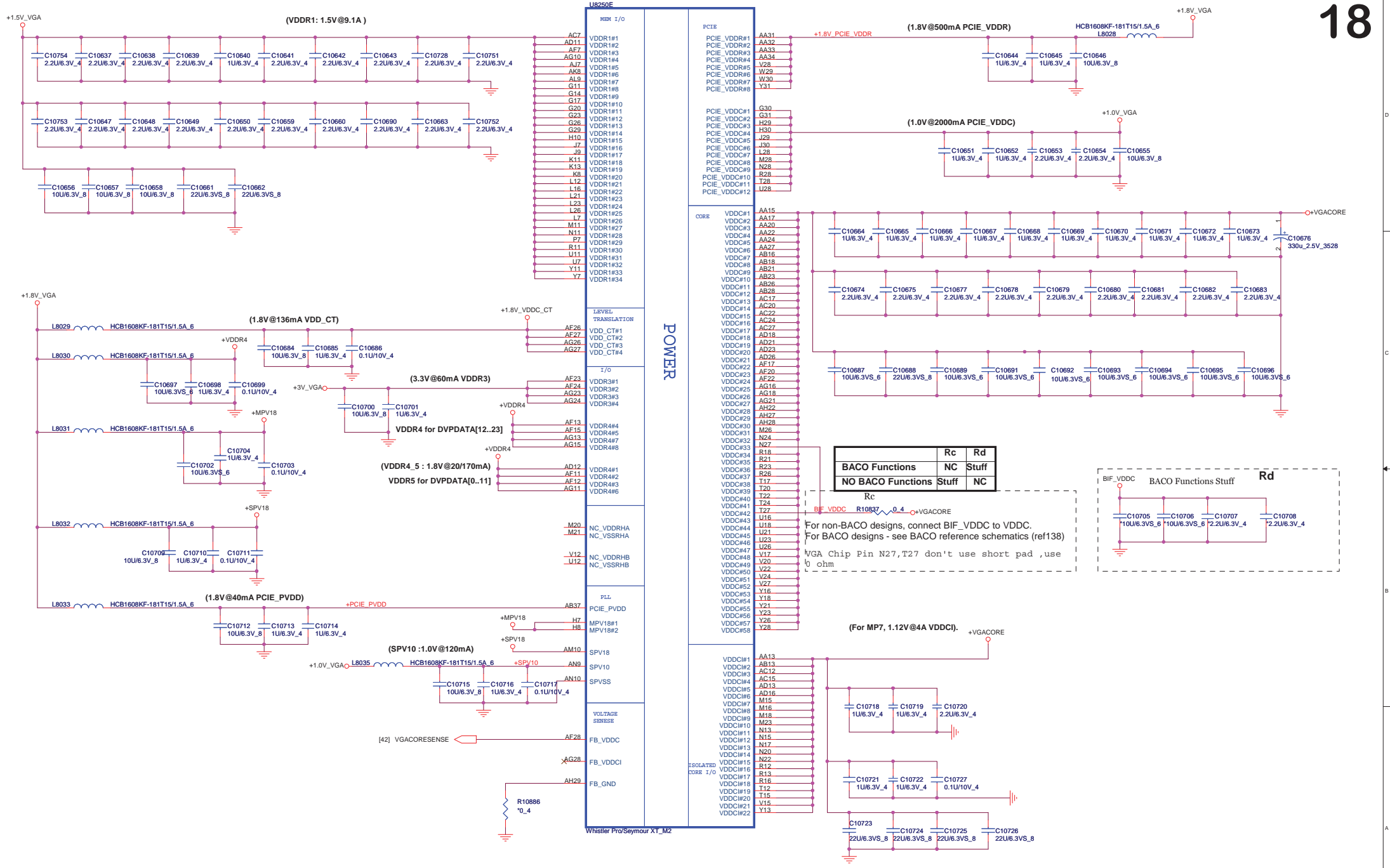
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRs_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 - Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 - Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2/0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11



PROJECT : LG2/4 DIS
Quanta Computer Inc.

NB5

Size Custom Document Number **AMD Whistler (GD&Str)/4/5** Rev 3A
Date: Wednesday, May 18, 2011 Sheet 17 of 47

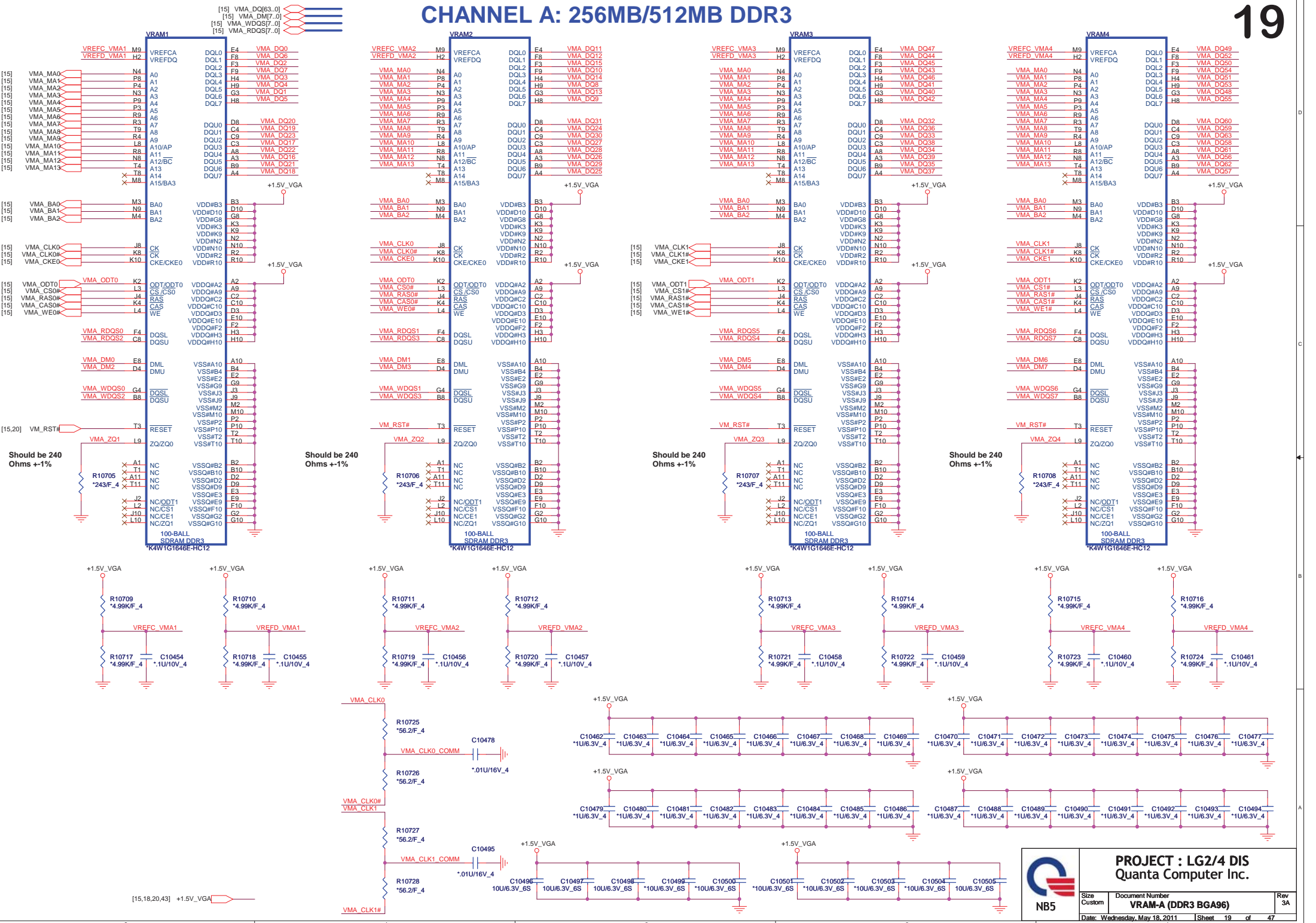


PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom Document Number **AMD Whistler (POWER) 5/5** Rev 3A

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CHANNEL A: 256MB/512MB DDR3

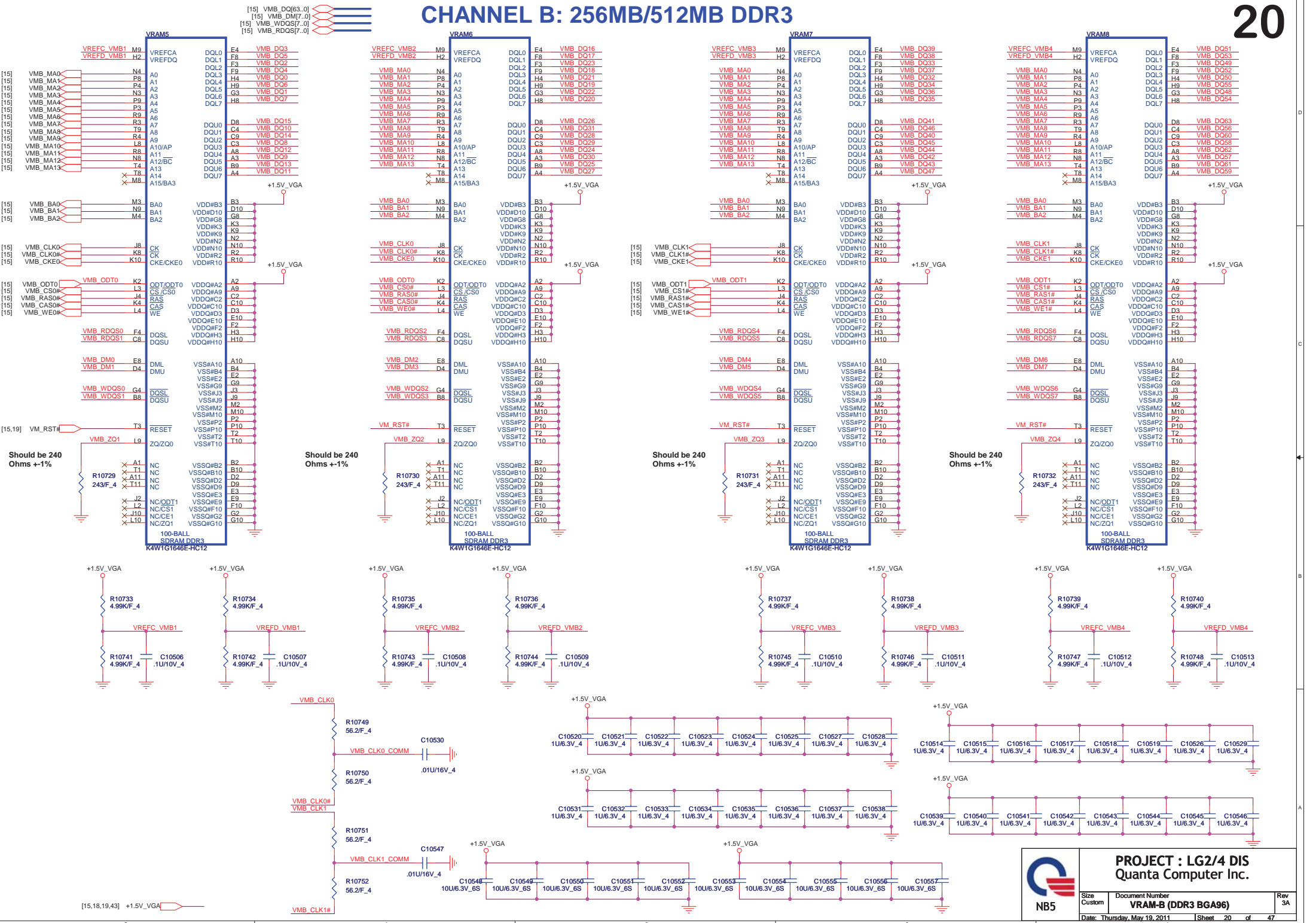


PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size: Custom
Document Number: **VRAM-A (DDR3 BG96)**
Date: Wednesday, May 18, 2011 | Sheet 19 of 47

Rev 3A

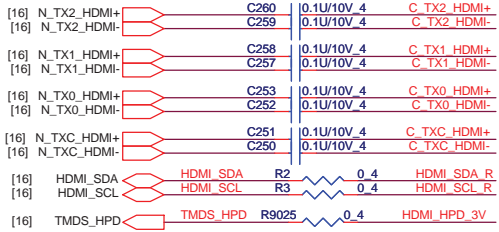
CHANNEL B: 256MB/512MB DDR3



PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number VRAM-B (DDR3 BGA96)	Rev 3A
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For DIS HDMI Only



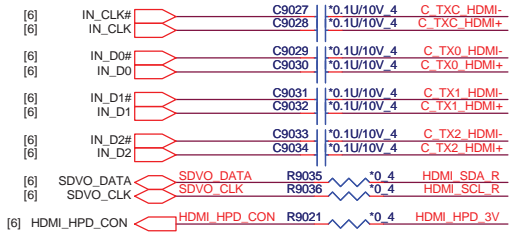
	Select
Dis	Ra
Muxless	Rb

Ra

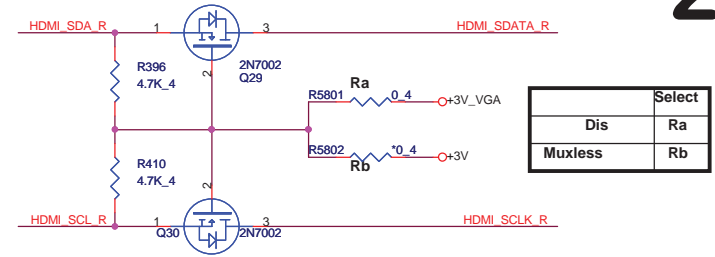
	Select
Dis	Ra
Muxless	Rb

Rb

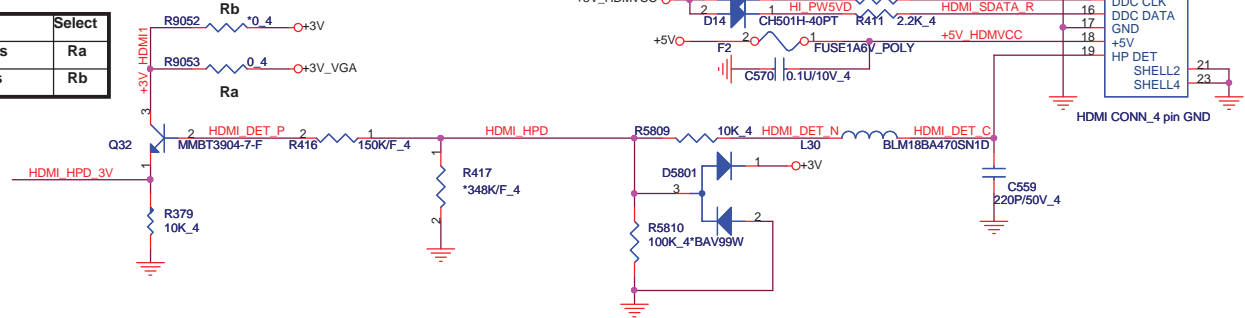
For Muxless/UMA HDMI function



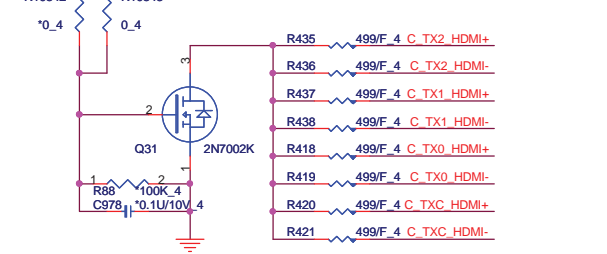
DIS: 4.7K
UMA/Muxless: 2.2K



	Select
Dis	Ra
Muxless	Rb



DIS 499 ohm ; UMA/Muxless 680 ohm
Close connector < 50 mil



Close connector < 50 mil
EMI

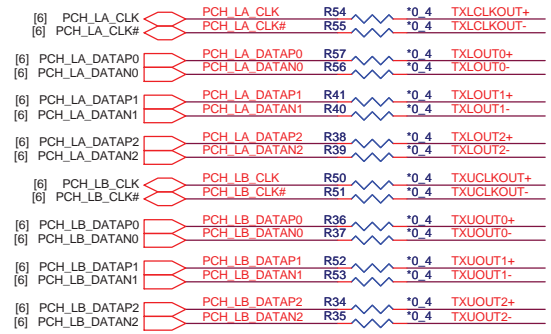
C_TXC_HDMI+	R135	150/F_4	C_TXC_HDMI-
C_TX0_HDMI+	R136	150/F_4	C_TX0_HDMI-
C_TX1_HDMI+	R141	150/F_4	C_TX1_HDMI-
C_TX2_HDMI+	R142	150/F_4	C_TX2_HDMI-

DV2 Change to 150 ohm

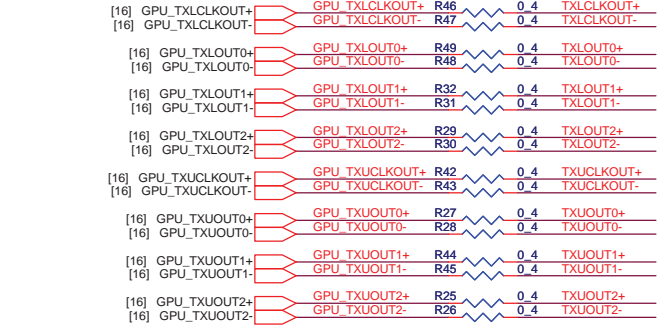
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number HDMI and connector	Rev 3A
Date: Friday, May 20, 2011 Sheet 21 of 47		

Rb MUXLESS



Ra DIS



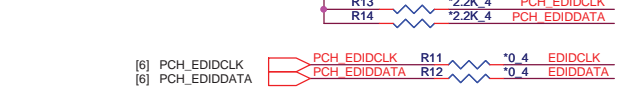
Rb MUXLESS



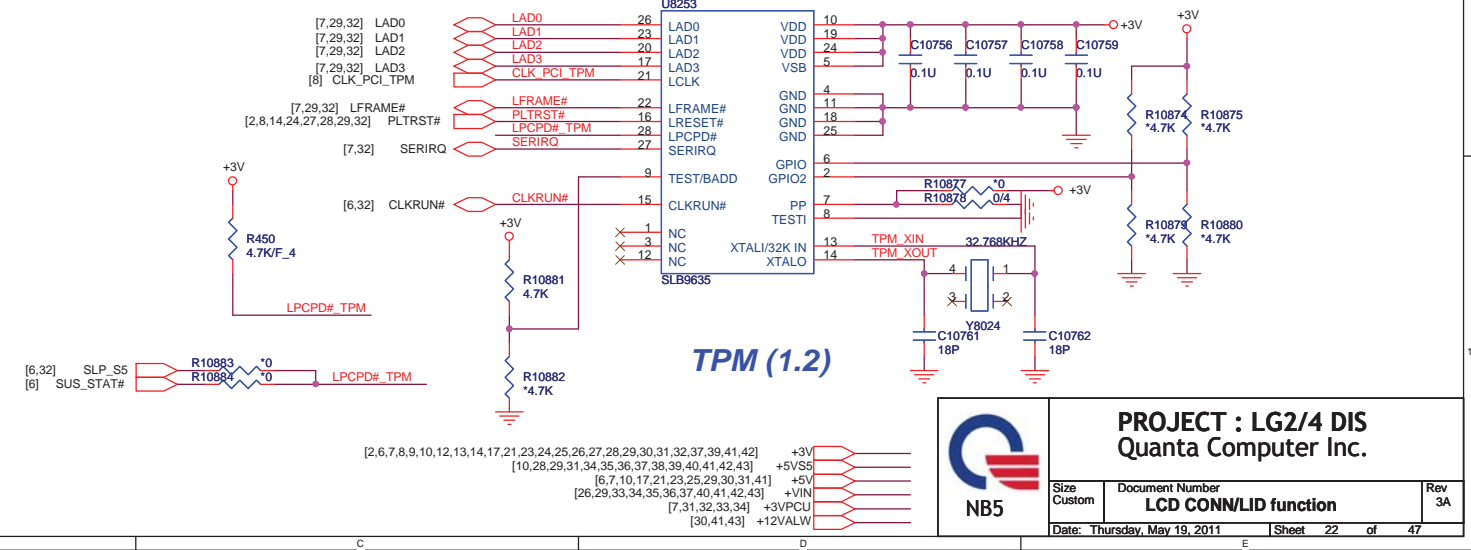
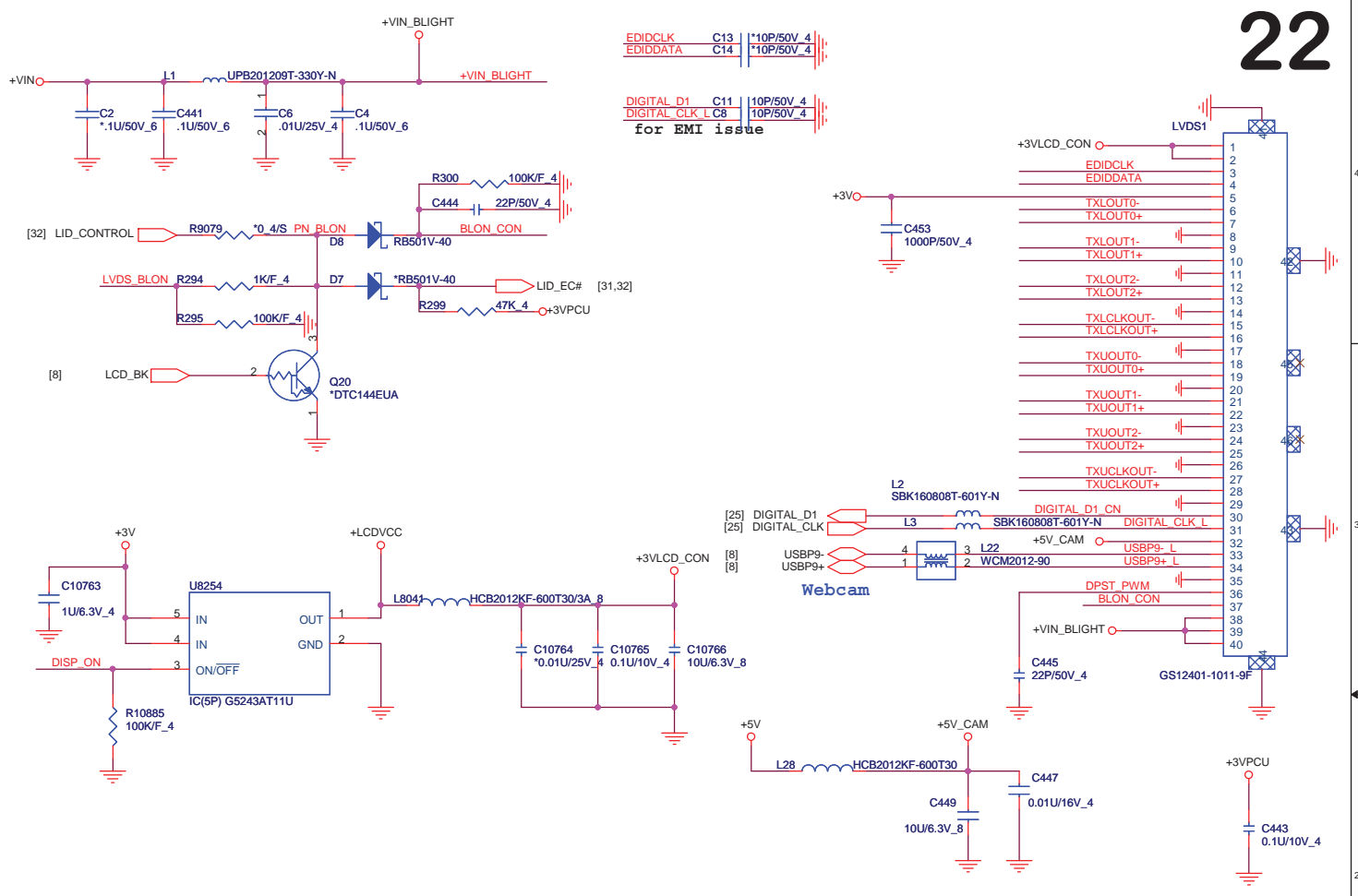
Ra DIS



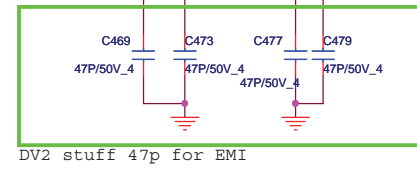
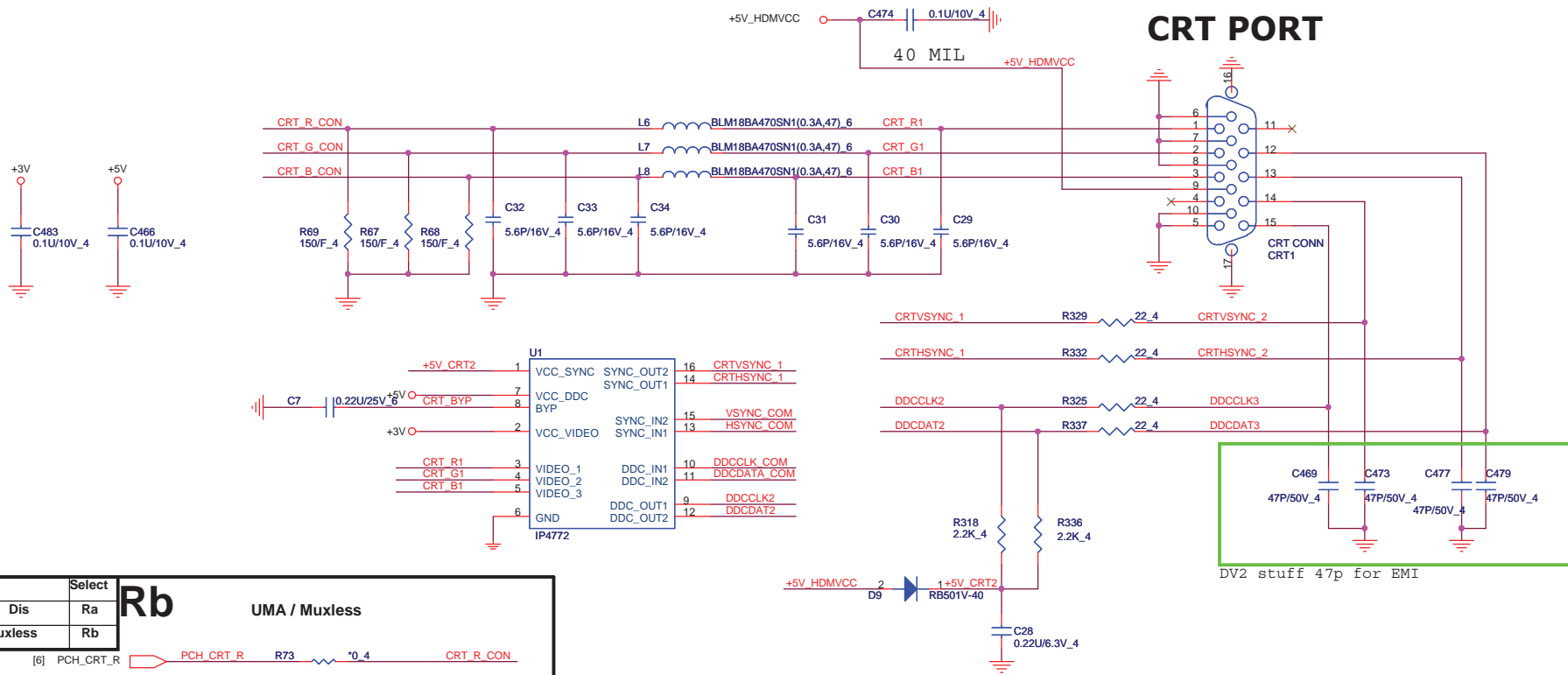
Rb MUXLESS



Ra DIS



	PROJECT : LG2/4 DIS	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 3A
LCD CONN/LID function		
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DV2 stuff 47p for EMI

Dis	Select	Ra	Rb
[6]	PCH_CRT_R	PCH_CRT_R	R73
[6]	PCH_CRT_G	PCH_CRT_G	R74
[6]	PCH_CRT_B	PCH_CRT_B	R75
[6]	PCH_HSYNC	PCH_HSYNC	R17
[6]	PCH_VSYNC	PCH_VSYNC	R23
[6]	PCH_DDCCLK	PCH_DDCCLK	R24
[6]	PCH_DDCDATA	PCH_DDCDATA	R16

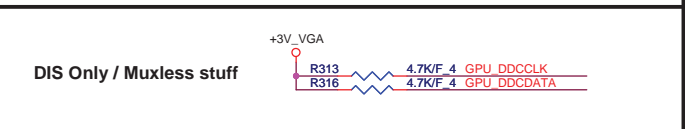
UMA / Muxless

+3V

R315 *4.7K/F_4 PCH_DDCCLK
R314 *4.7K/F_4 PCH_DDCDATA

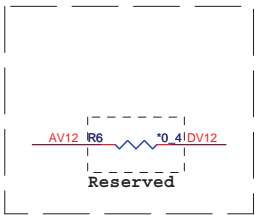
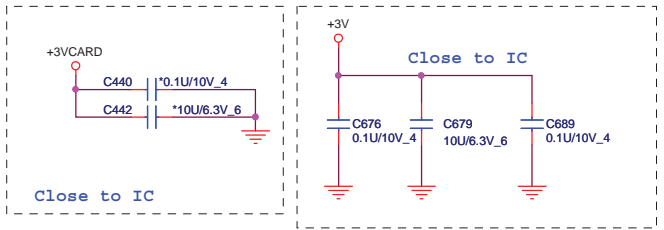
[16]	GPU_CRT_R	GPU_CRT_R	R70
[16]	GPU_CRT_G	GPU_CRT_G	R71
[16]	GPU_CRT_B	GPU_CRT_B	R72
[16,17]	GPU_HSYNC	GPU_HSYNC	R15
[16,17]	GPU_VSYNC	GPU_VSYNC	R20
[16]	GPU_DDCCLK	GPU_DDCCLK	R21
[16]	GPU_DDCDATA	GPU_DDCDATA	R18

DIS Only



[6,7,10,17,21,22,25,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,21,22,24,25,26,27,28,29,30,31,32,37,39,41,42] +3V

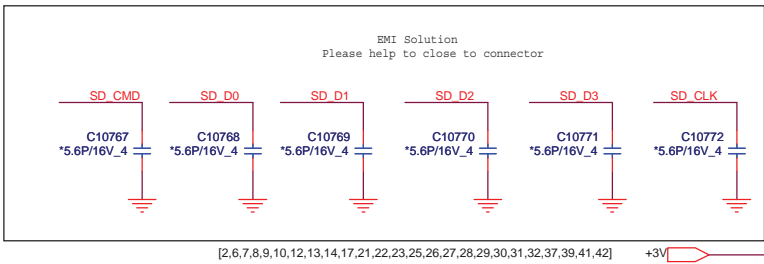
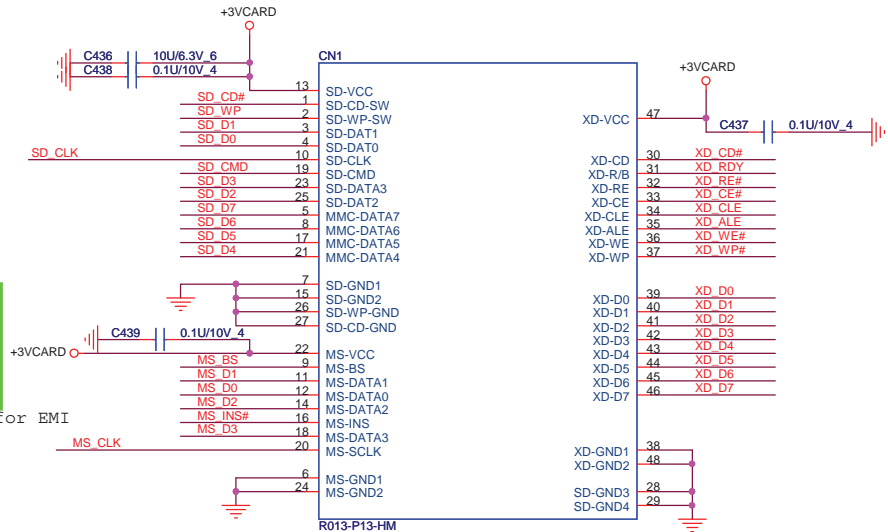
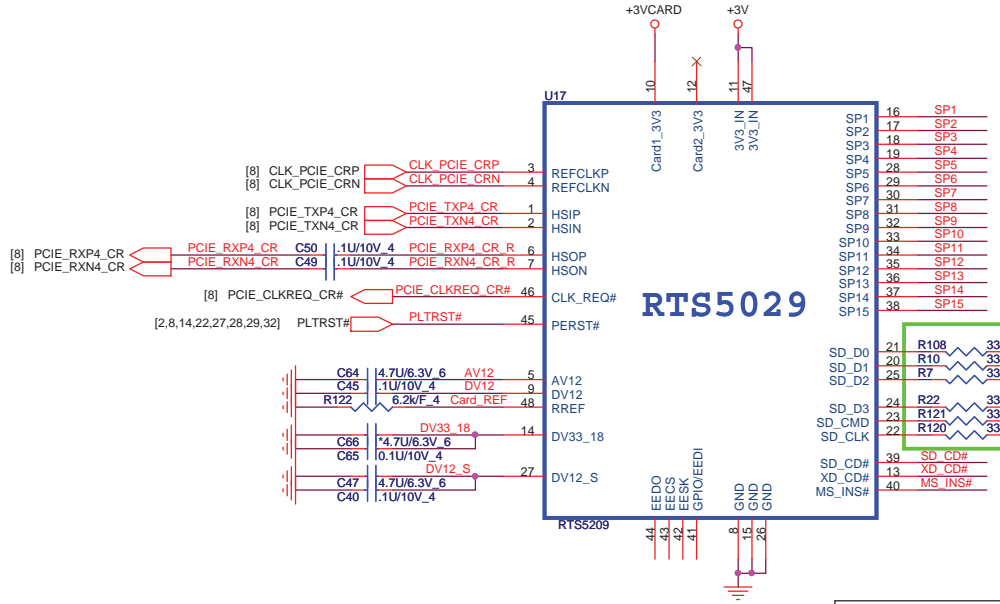
	PROJECT : LG2/4 DIS Quanta Computer Inc.		Rev 3A	
	Size Custom	Document Number CRT/HDMI Conn		Date: Wednesday, May 18, 2011 Sheet 23 of 47



SP1	SD D7	XD RDY
SP2	SD D6	XD RE#
SP3	SD D5	XD CE#
SP4	SD D4	XD WE#
SP5	MS BS	XD CLE
SP6	MS D5	XD ALE
SP7	MS D1	XD WP#
SP8	MS D4	XD D0
SP9	MS D0	XD D1
SP10	MS D2	XD D2
SP11	MS D6	XD D3
SP12	MS D3	XD D4
SP13	MS D7	XD D5
SP14	MS D7	XD D6
SP15	SD WP	XD D7

Share Pin

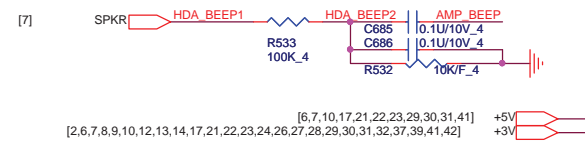
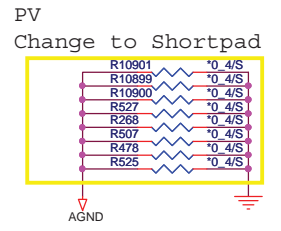
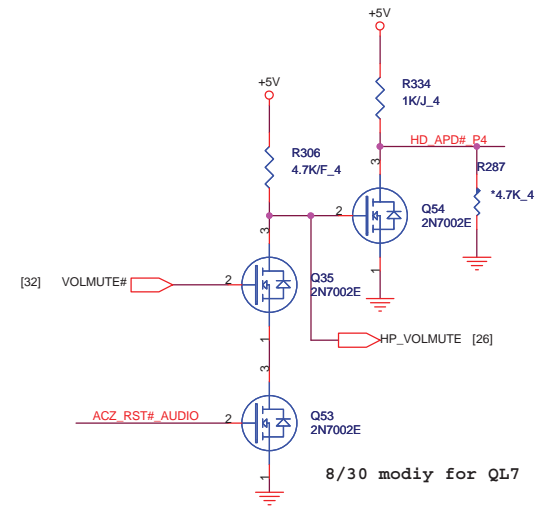
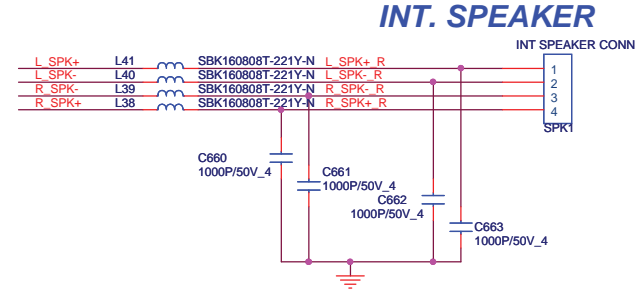
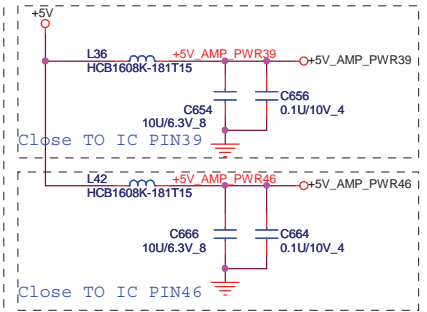
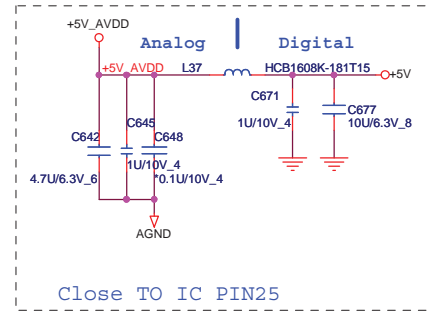
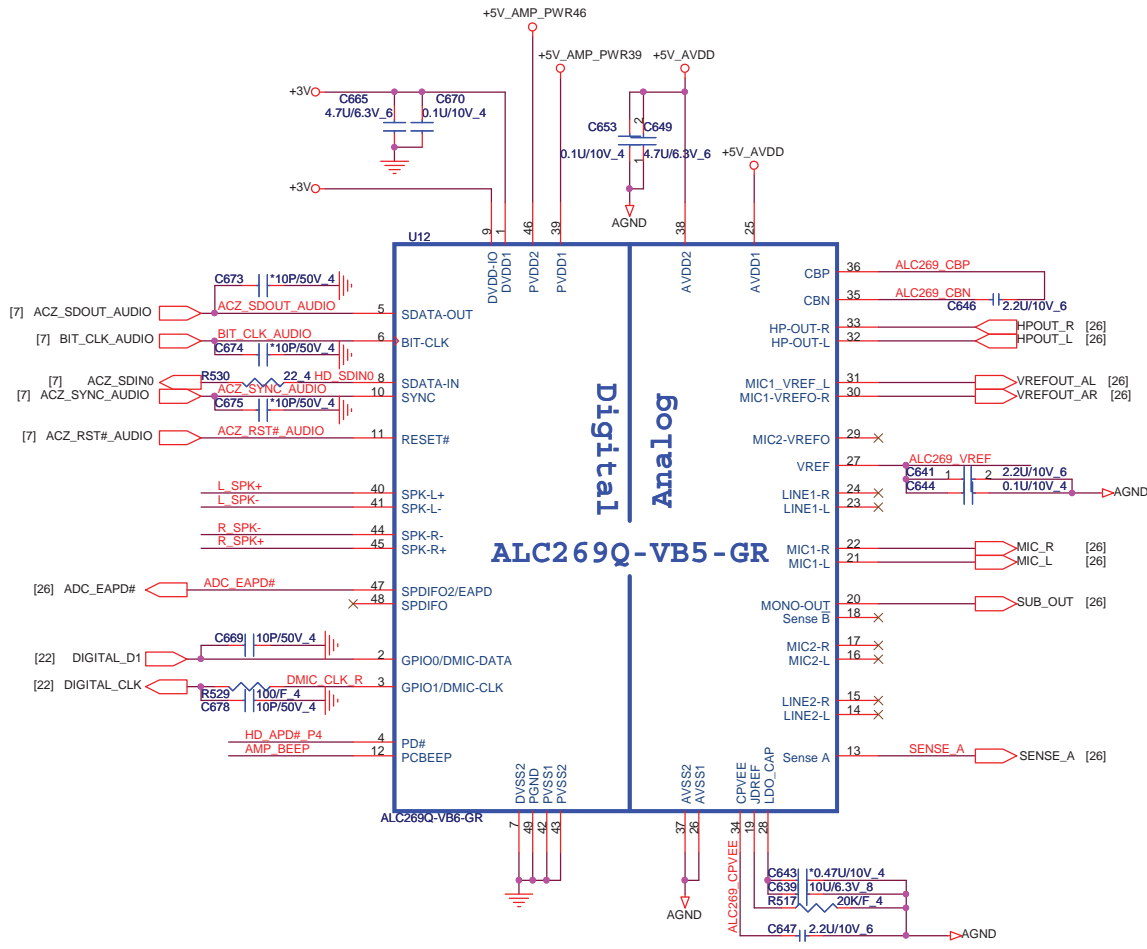
7-in-1 flash media slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)



PROJECT : LG2/4 DIS
Quanta Computer Inc.

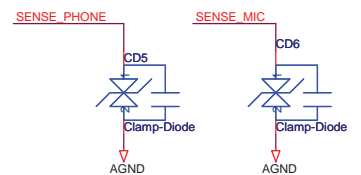
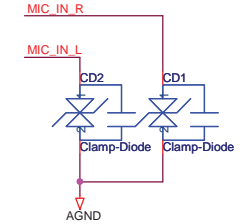
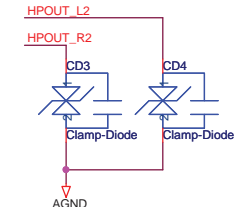
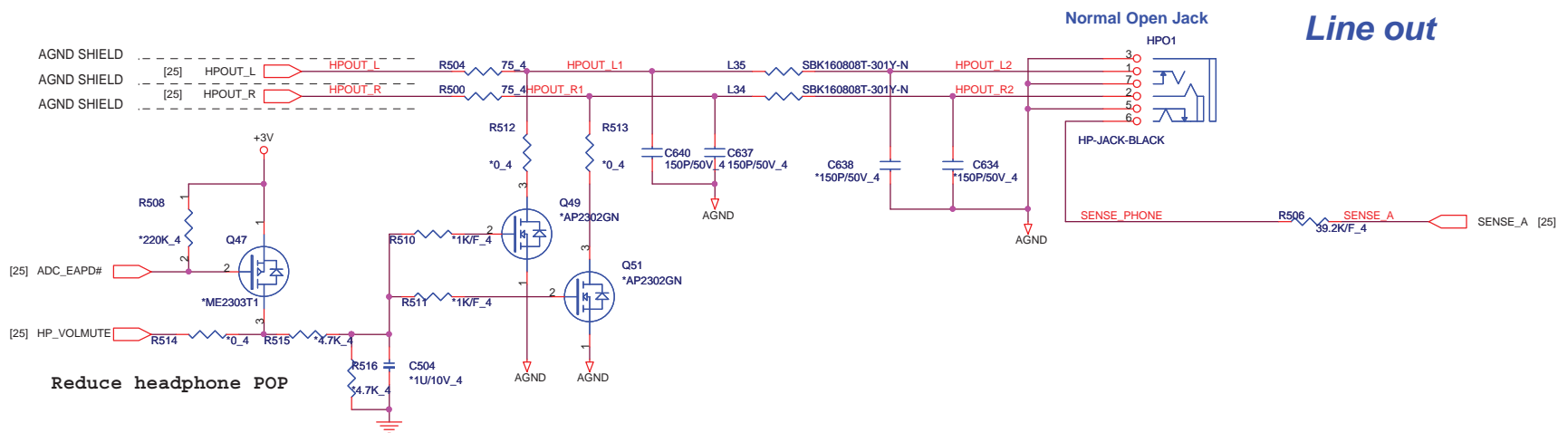
Size Custom Document Number **Card reder (RTS5029)** Rev 3A

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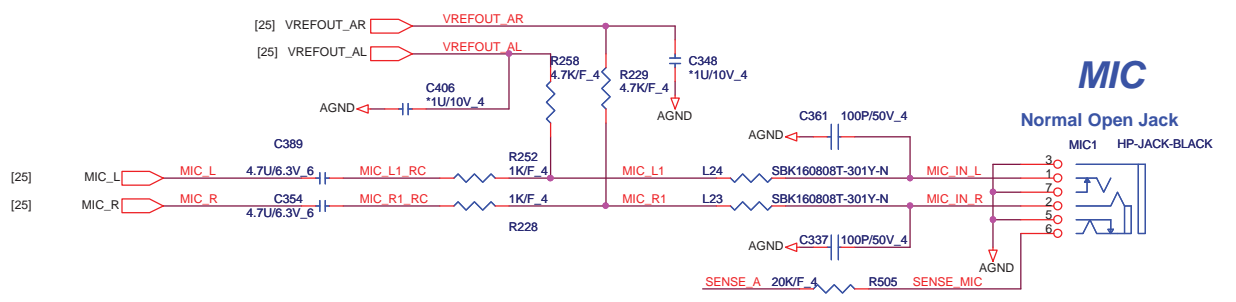
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number HDA Azalia ALC269	Rev 3A
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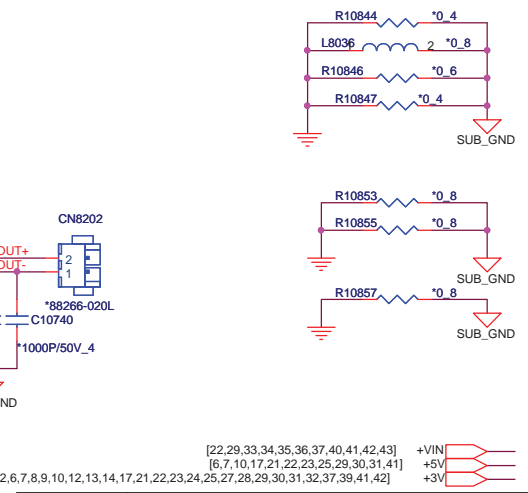
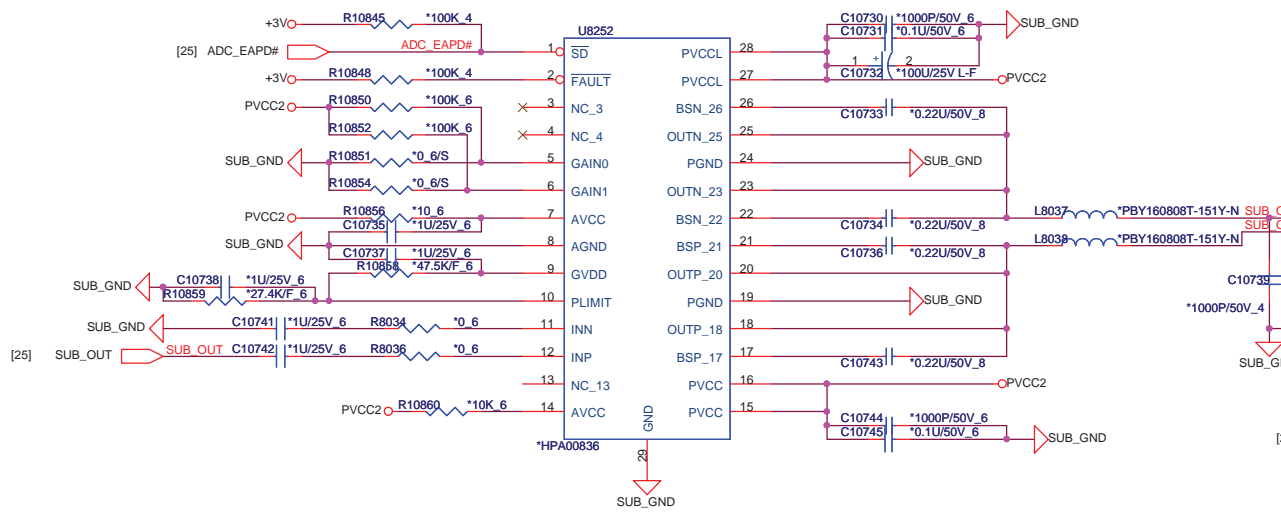
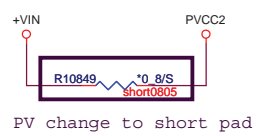


Reduce headphone POP

MIC



Sub-Woofer for 17"



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

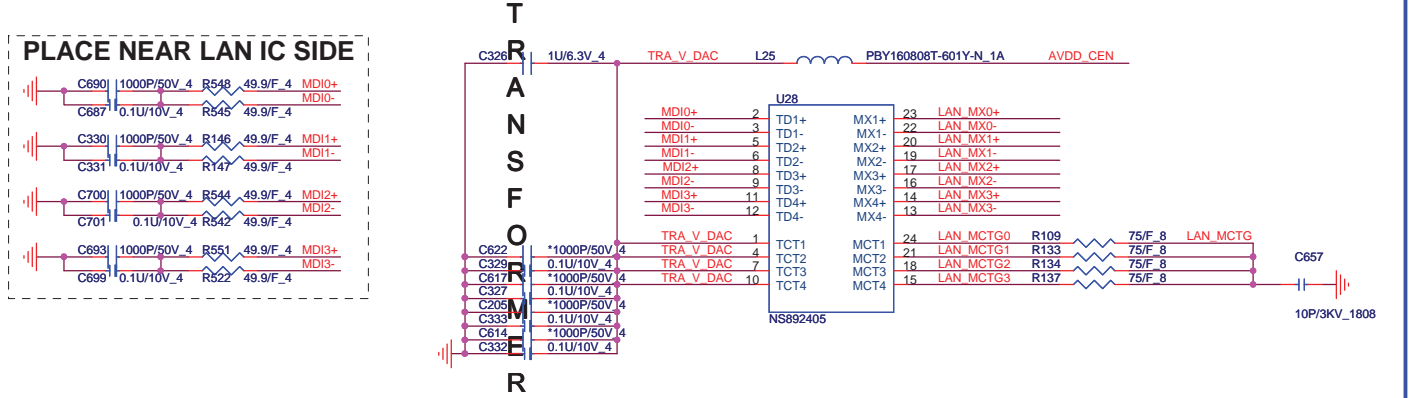
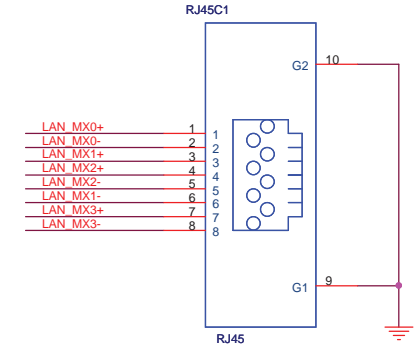
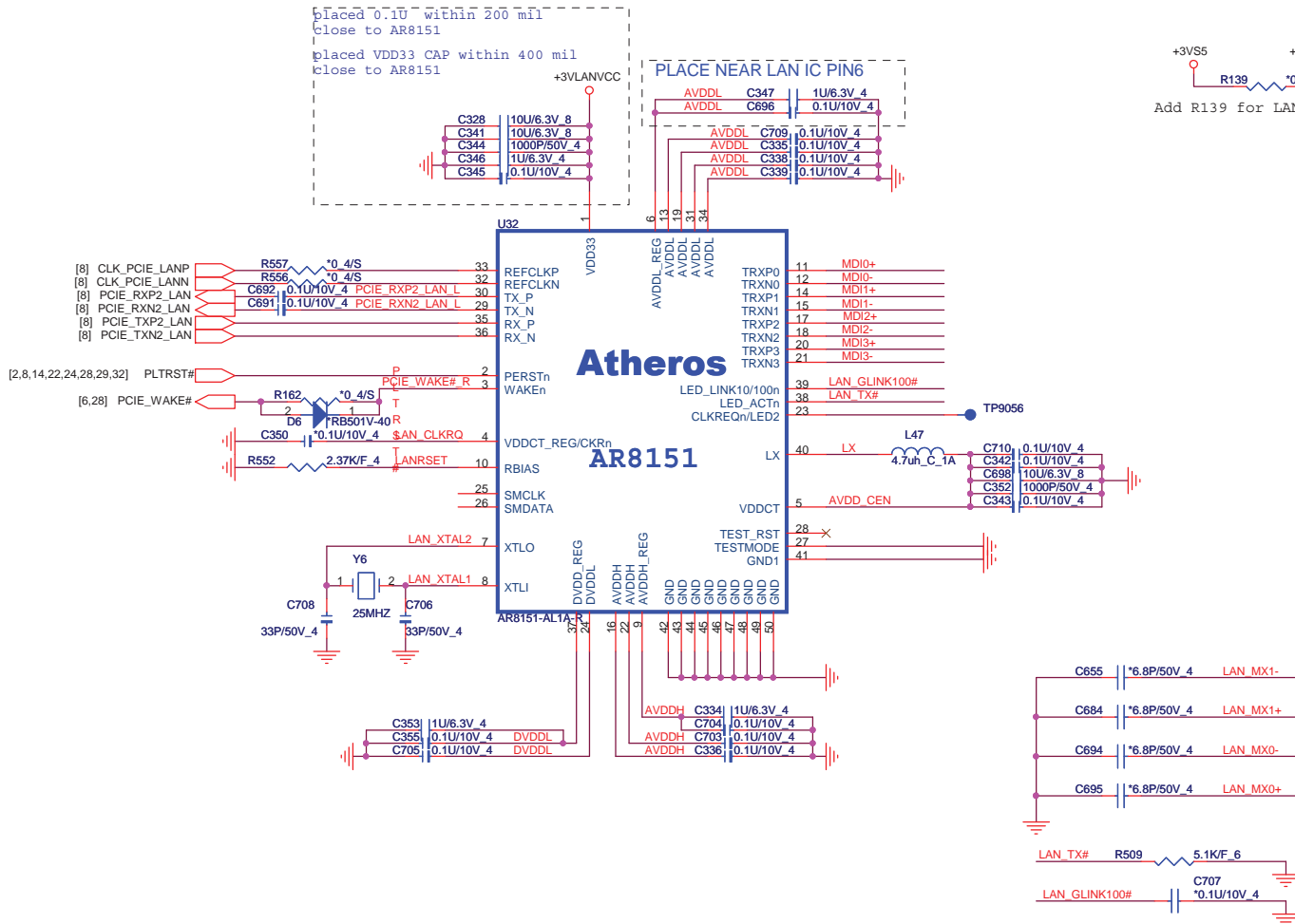
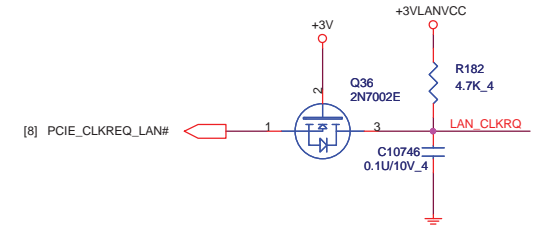
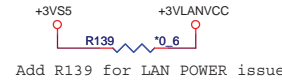
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,31,41] +VIN
 [6,7,10,17,21,22,23,25,29,30,31,41] +5V
 [2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,31,32,37,39,41,42] +3V

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom Document Number **Audio Jack/Accelerometer** Rev 3A

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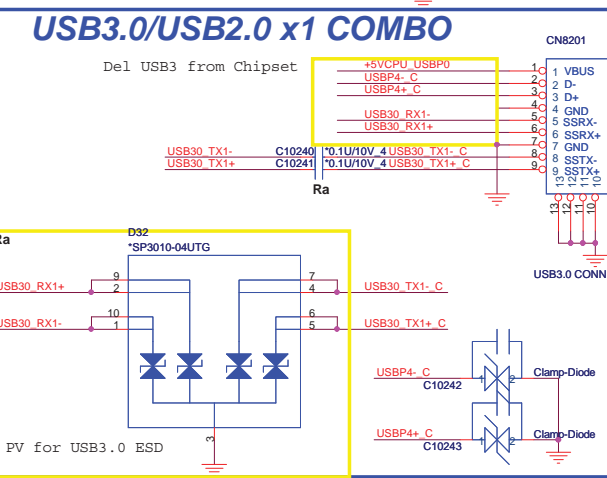
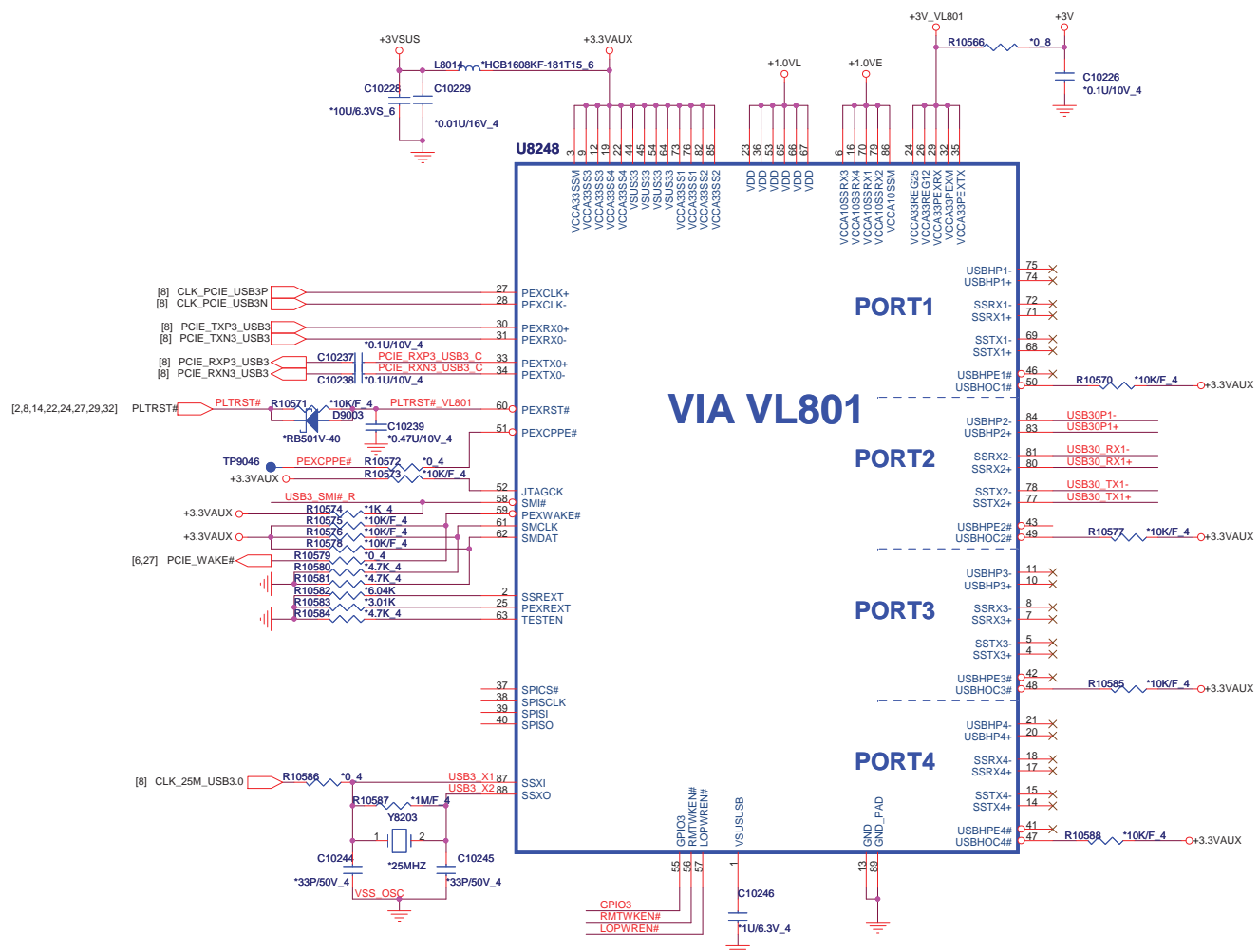
Atheros Lan



[2,6,7,8,9,10,29,32,34,37,38,41,43] +3V55
 [41] +3VLANVCC
 [2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,39,41,42] +3V

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number LAN AR8151/RJ45	Rev 3A
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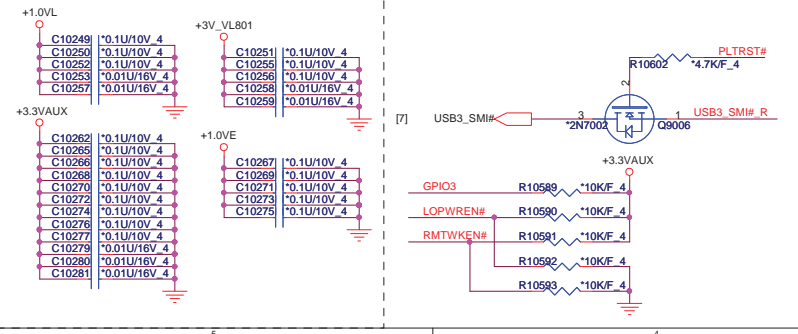


CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

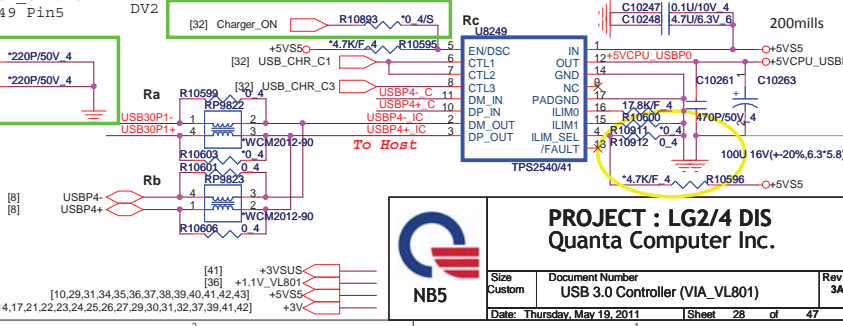
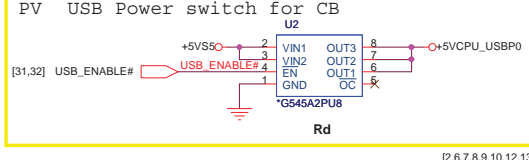
LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
user define Battery % and wake up from USB		SDP		OFF

	Select
USB3.0	Ra
USB2.0	Rb

Charger USB Add R10911,R10912,R10596 for TPS2543
 80 mils (Iout=2A) **high active** Ios = 48000/RILIMO default: Auto-detect



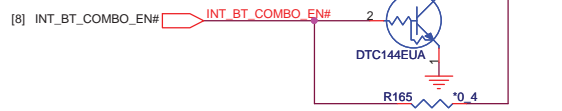
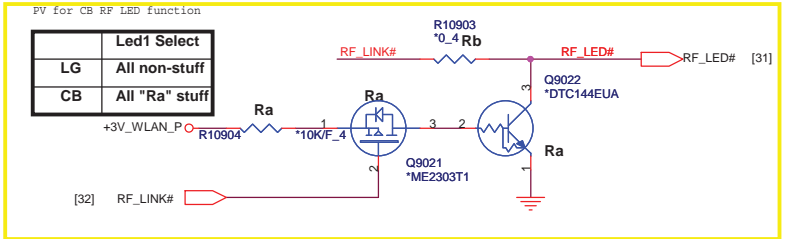
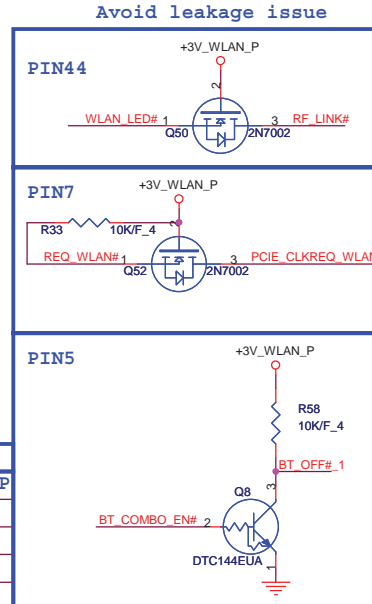
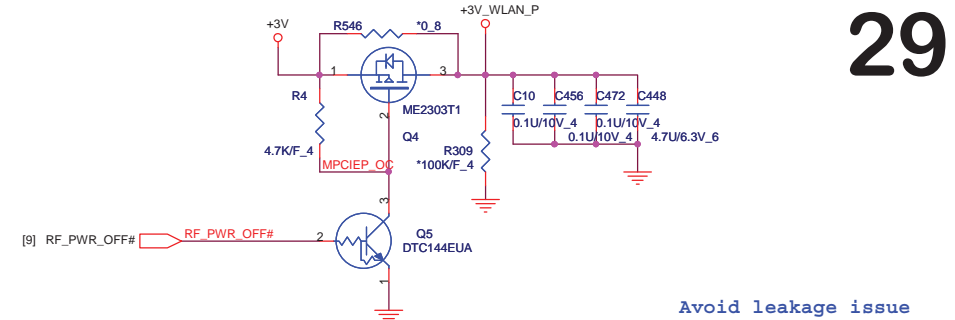
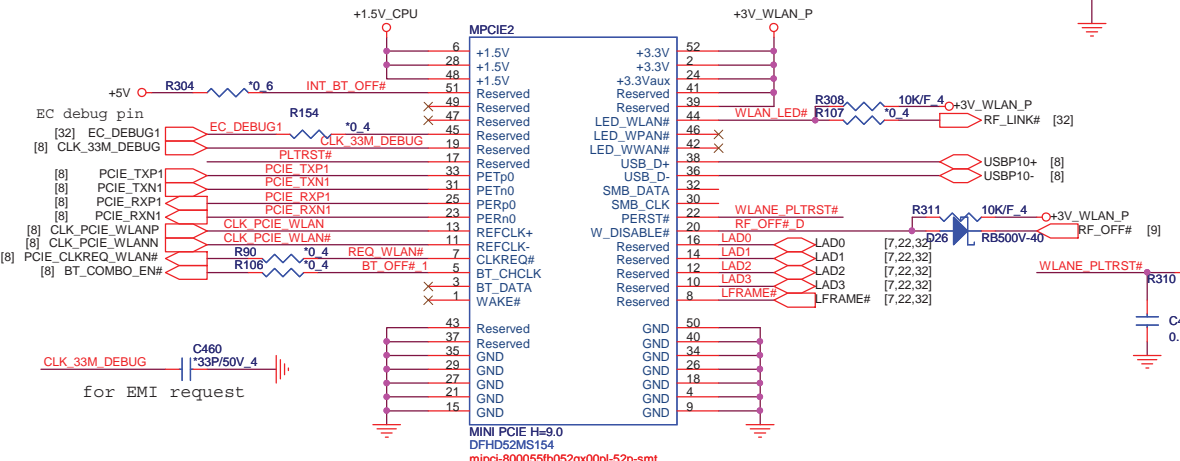
Power switch select	
LG	Rc
CB	Rd



PROJECT : LG2/4 DIS
 Quanta Computer Inc.

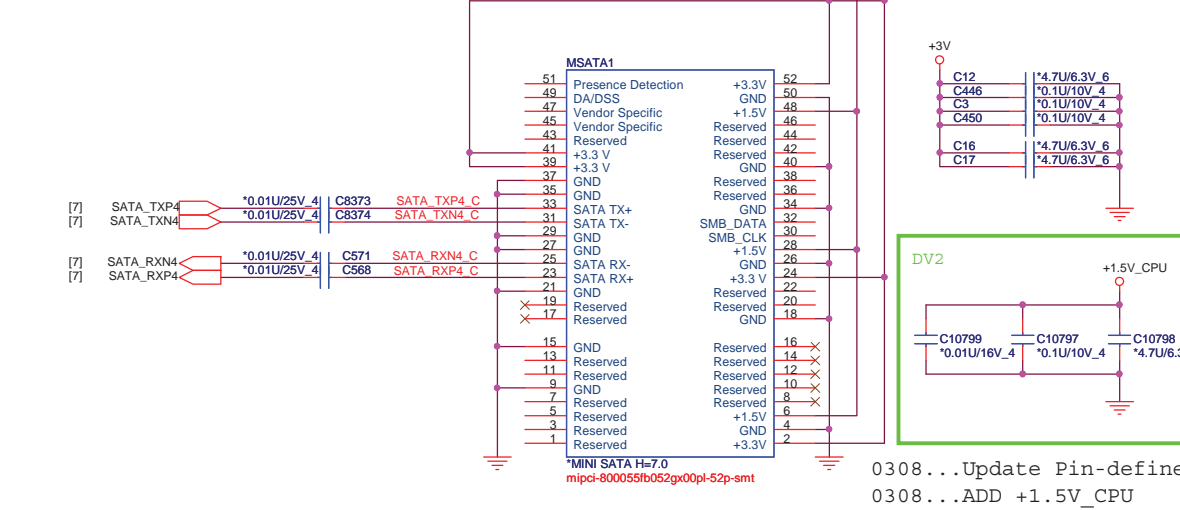
Size Custom	Document Number	Rev
	USB 3.0 Controller (VIA_VL801)	3A
Date: Thursday, May 19, 2011	Sheet 28 of 47	

Mini PCI-E Card 1 - Half WLAN

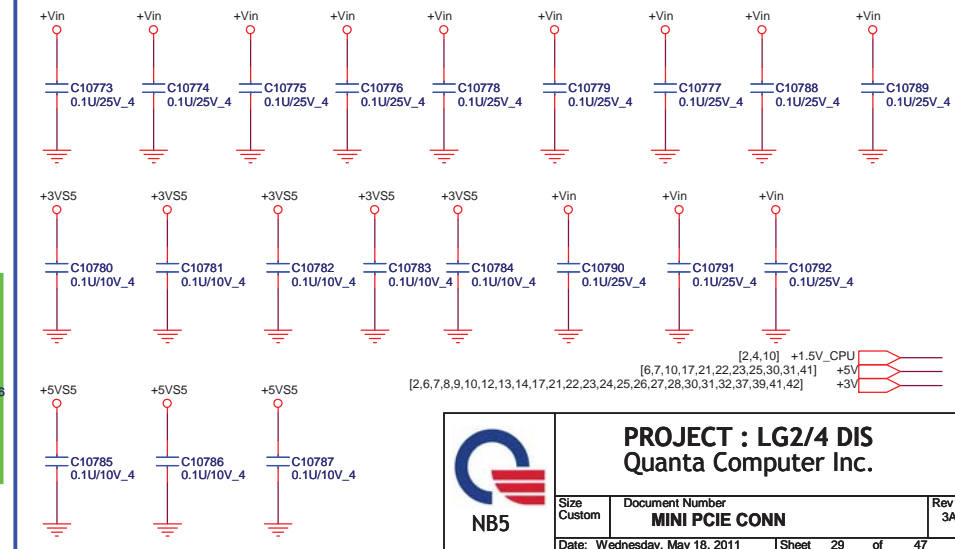


WLAN	Bluetooth	+3V WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

Mini PCI-E Card 2- Full size MINISATA



Power Plan Cap for EMI



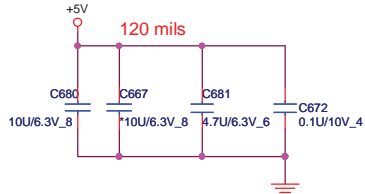
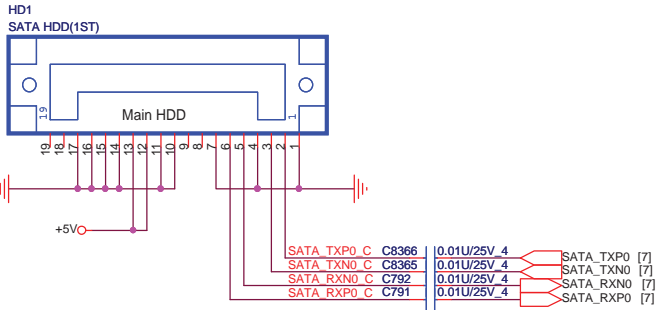
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN	Rev 3A
Date: Wednesday, May 18, 2011 Sheet 29 of 47		

0308...Update Pin-define
0308...ADD +1.5V_CPU

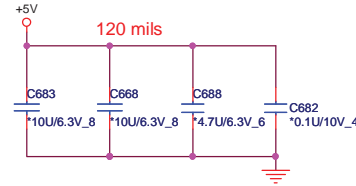
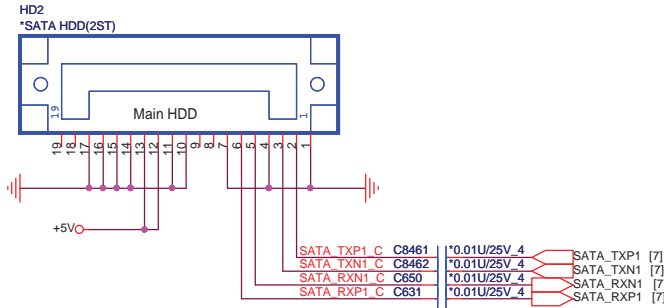
MAIN SATA HDD

DC Current rating: 0.5 A



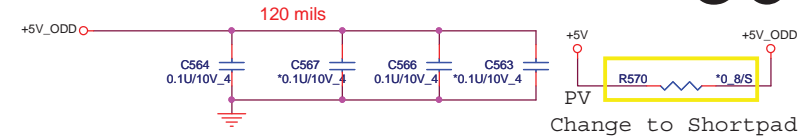
2nd SATA HDD for 17"

DC Current rating: 0.5 A



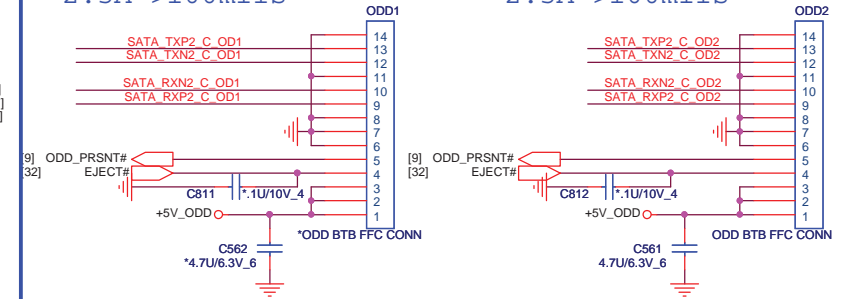
SATA CD-ROM To ODD Board

30

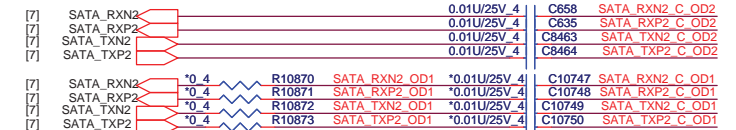


For 17" place
2.5A >100mils

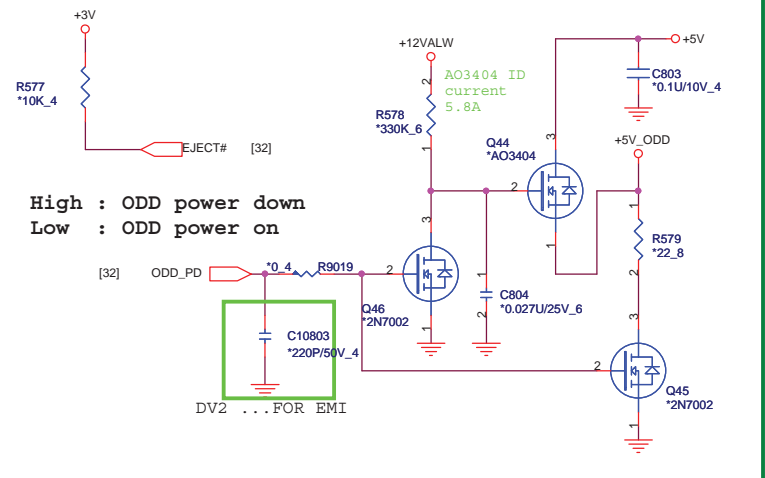
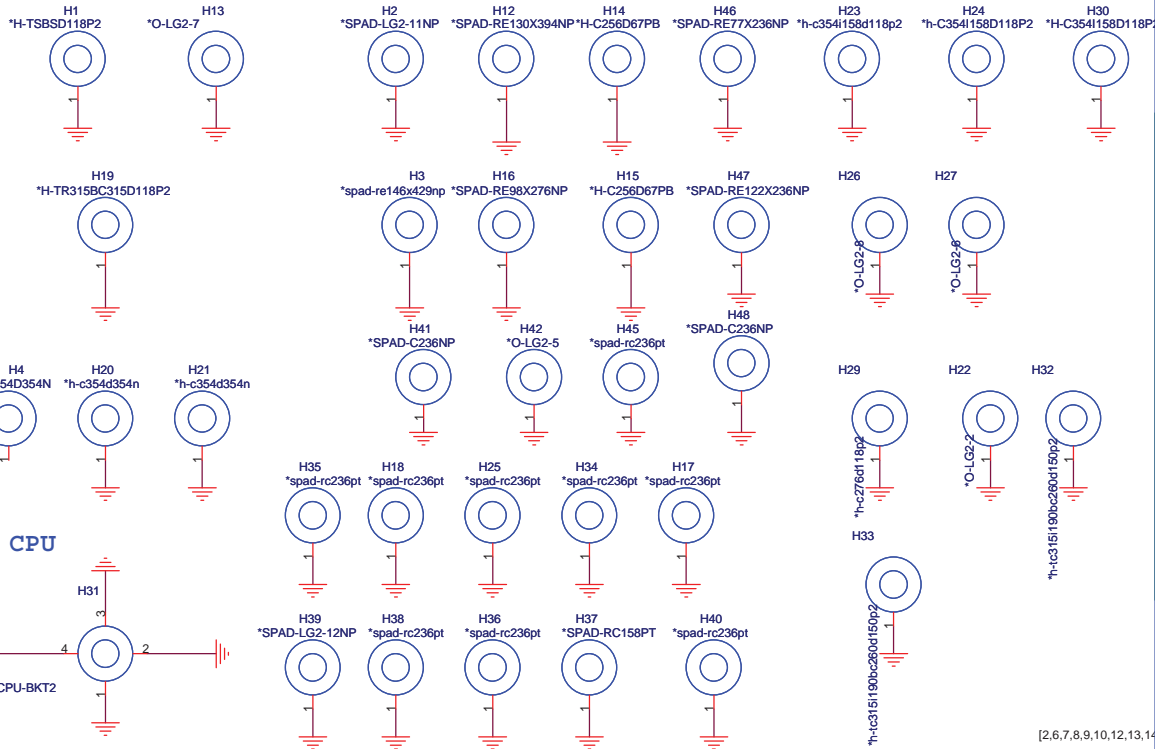
For 14"/15" place
2.5A >100mils



Ra FOR 14"/15"
Rb FOR 17"



Rb Ra



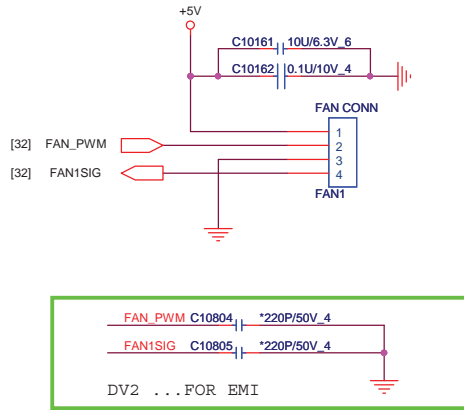
High : ODD power down
Low : ODD power on

PROJECT : LG2/4 DIS
Quanta Computer Inc.

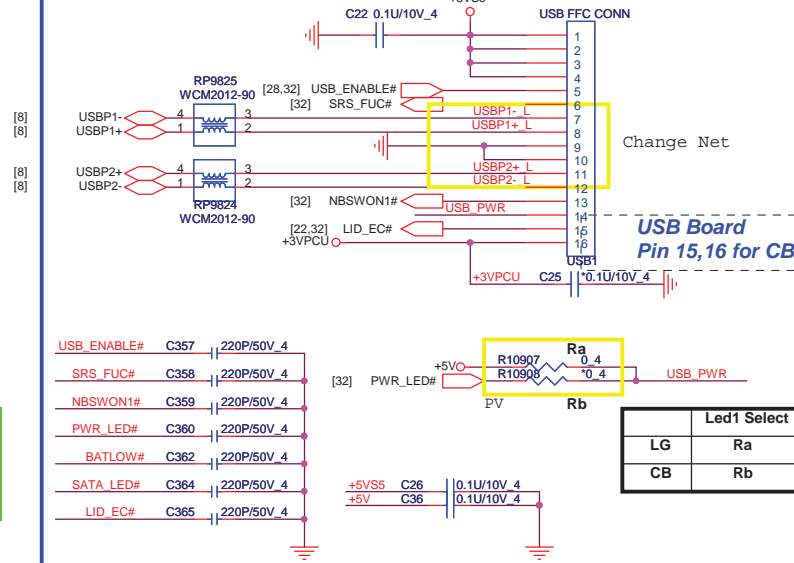
Size Custom	Document Number ODD/HDD/HOLES	Rev 3A
Date: Thursday, May 19, 2011 Sheet 30 of 47		

[6, 7, 10, 17, 21, 22, 23, 25, 28, 31, 41] +5V
[2, 6, 7, 8, 9, 10, 12, 13, 14, 17, 21, 22, 23, 24, 25, 26, 27, 28, 29, 31, 32, 37, 39, 41, 42] +3V

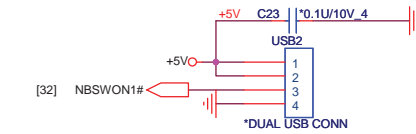
CPU FAN



USB / Power LED & SW for 14"/15"/17" To USB Board



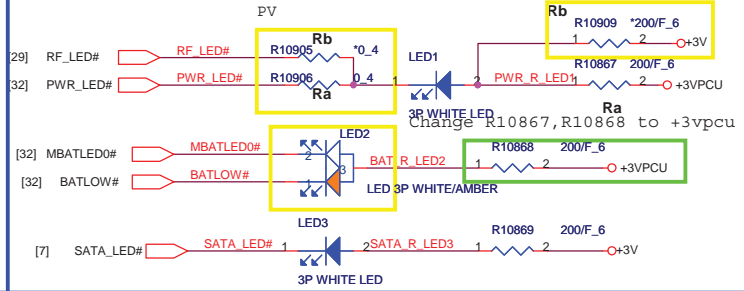
Power SW for 17"



LED Select Pin

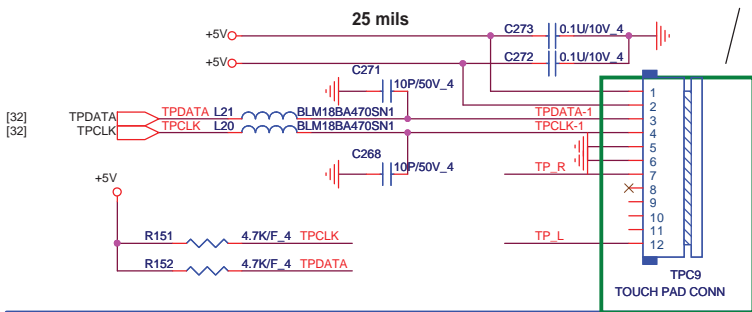
LG	Led1 Select	Led2 P/N
CB	Ra	BEWH0051Z00
CB	Rb	BEWY0007Z40

10 mils (250mA)

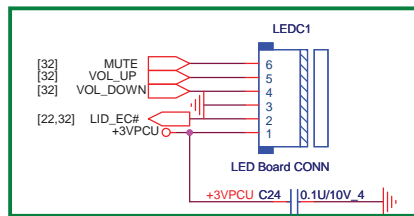


TOUCH PAD CONNECTOR To Click Board & FP

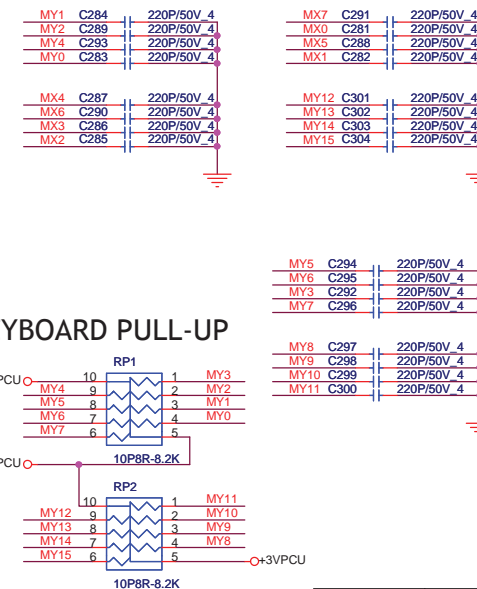
Update TPC9 footprint & P/N...0303



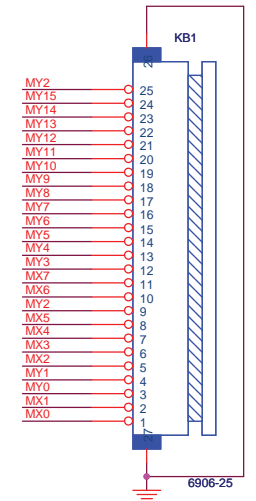
LID / MUTE / VU UP / VU DO To AD Function Board



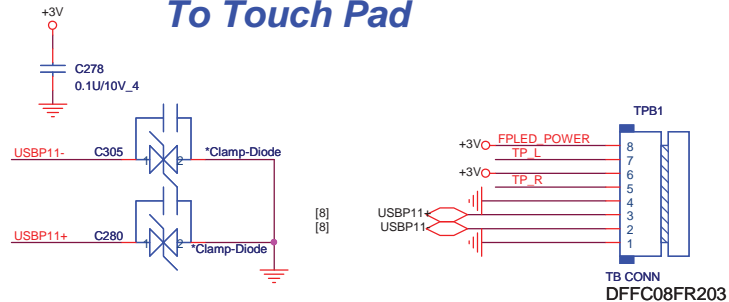
KEYBOARD PULL-UP



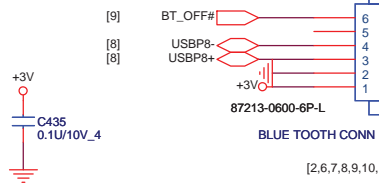
KEYBOARD Con.



TP Button CONNECTOR To Touch Pad



BLUETOOTH



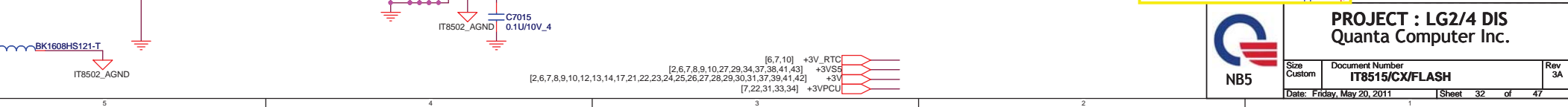
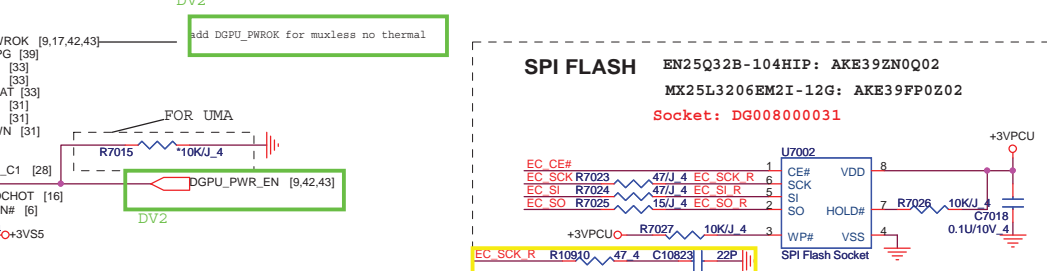
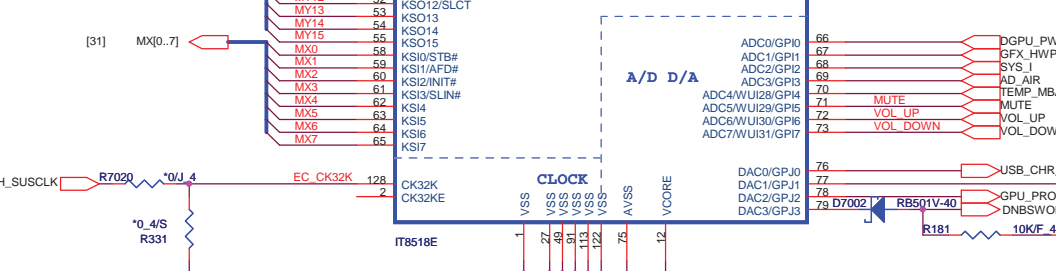
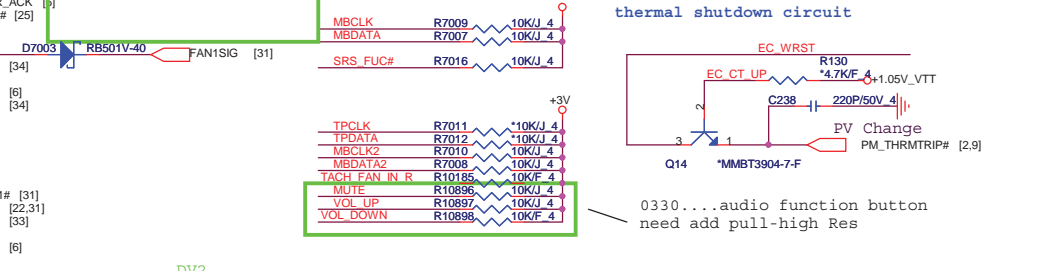
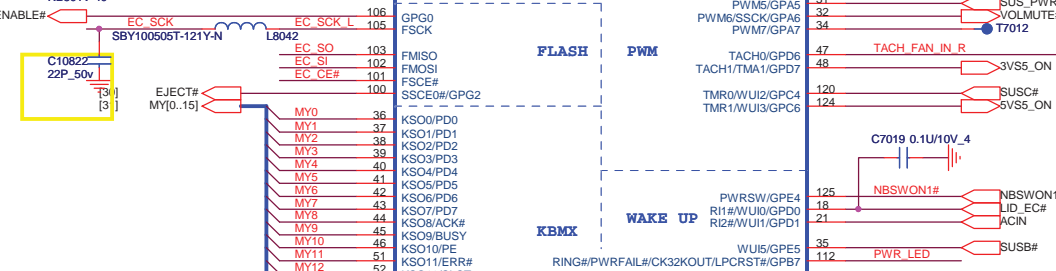
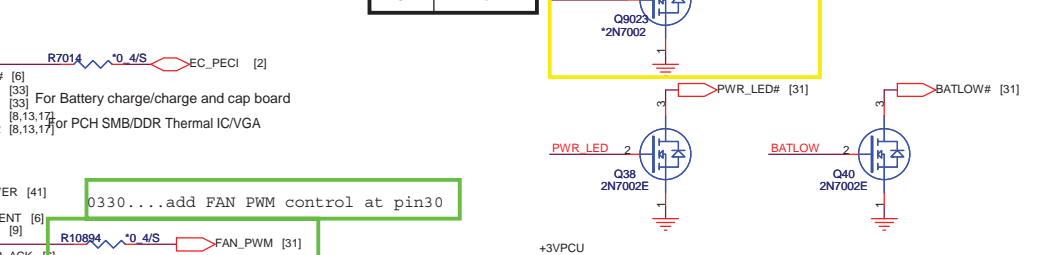
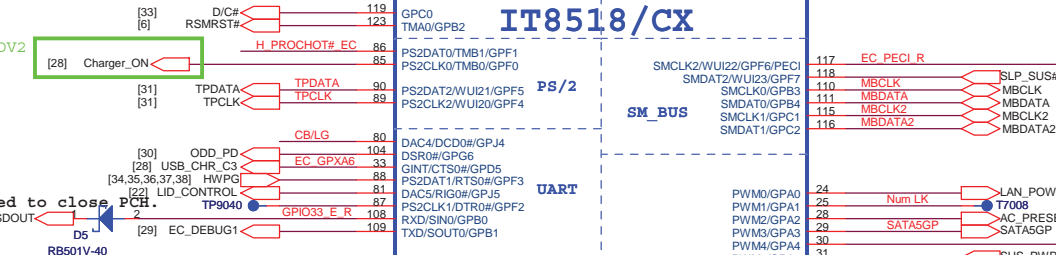
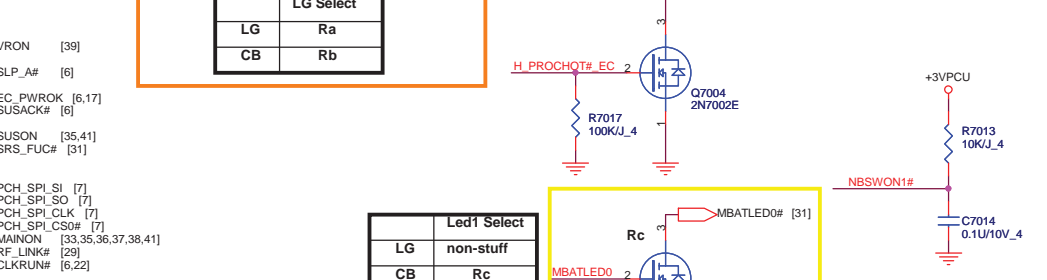
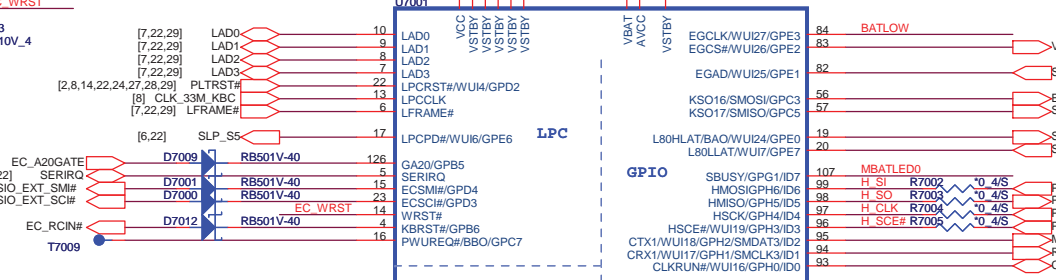
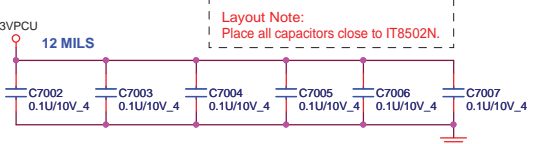
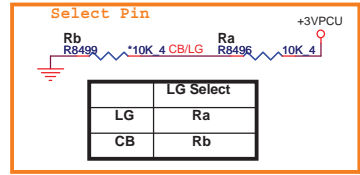
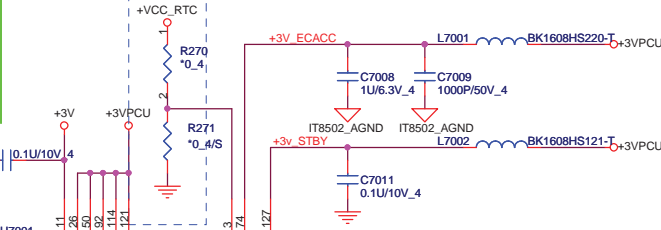
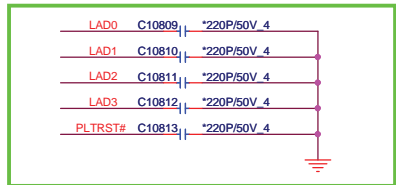
PROJECT : LG2/4 DIS
Quanta Computer Inc.

NBS

Size Custom	Document Number BT/USB/eSATA	Rev 3A
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DV2 ... POR EMI

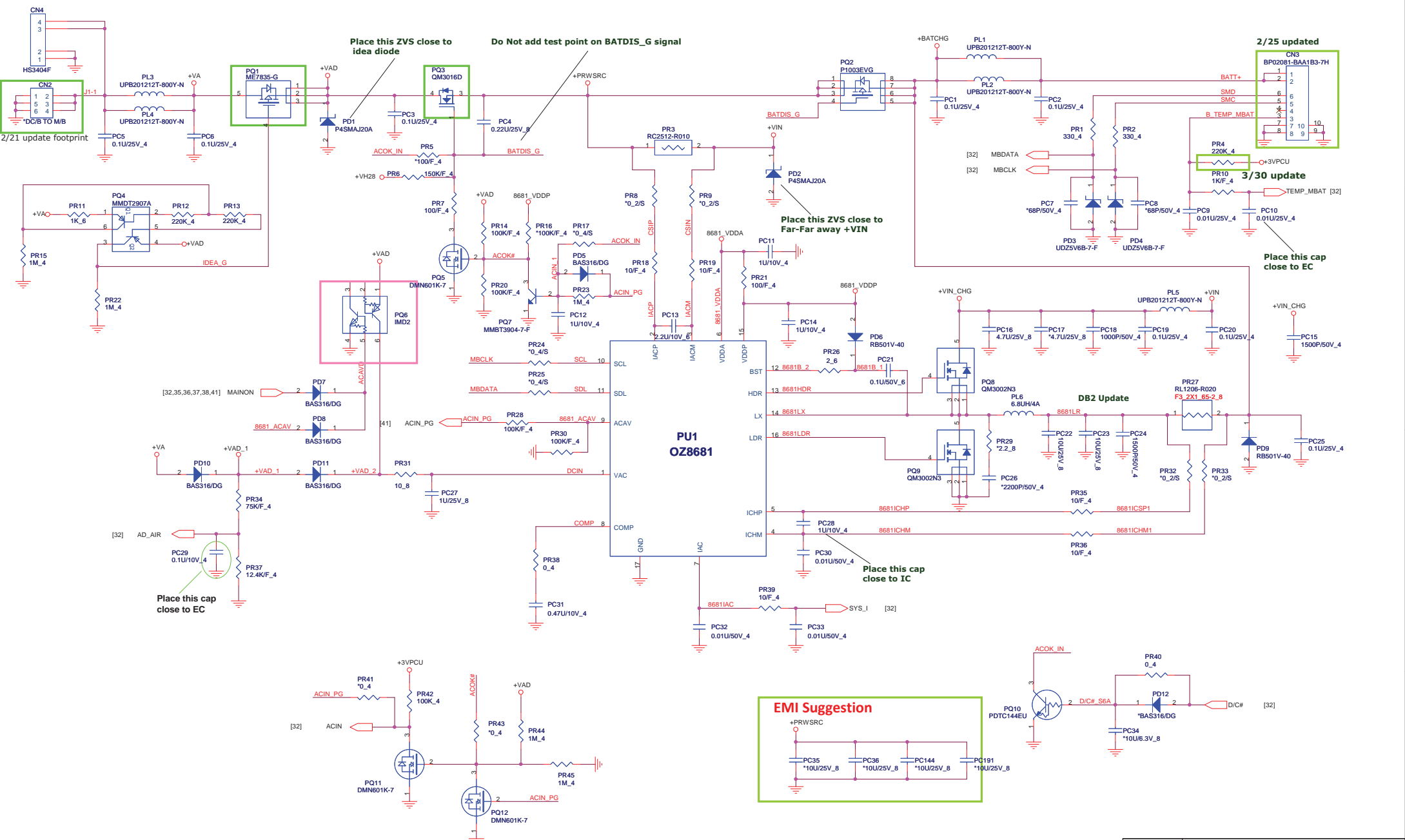


PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom Document Number **IT8515/CX/FLASH** Rev 3A
 Date: Friday, May 20, 2011 Sheet 32 of 47

TOP DC_JACK
90W/120W(QC)

LG2_DIS only



Place this ZVS close to idea diode

Do Not add test point on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

2/25 updated

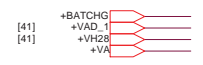
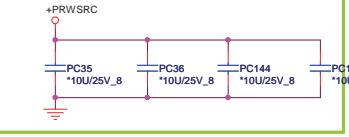
3/30 update

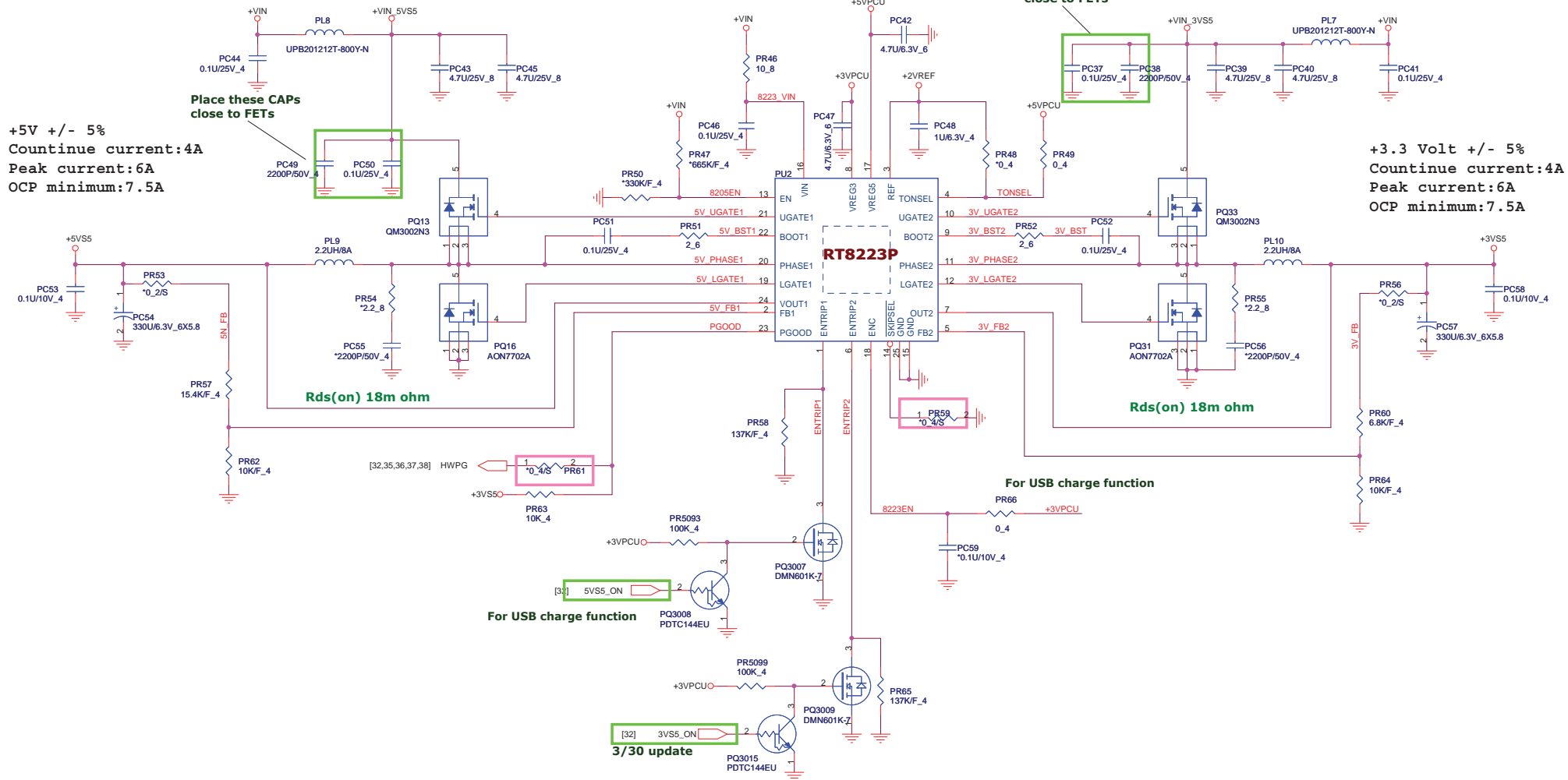
Place this cap close to EC


Place this cap close to EC

Place this cap close to IC

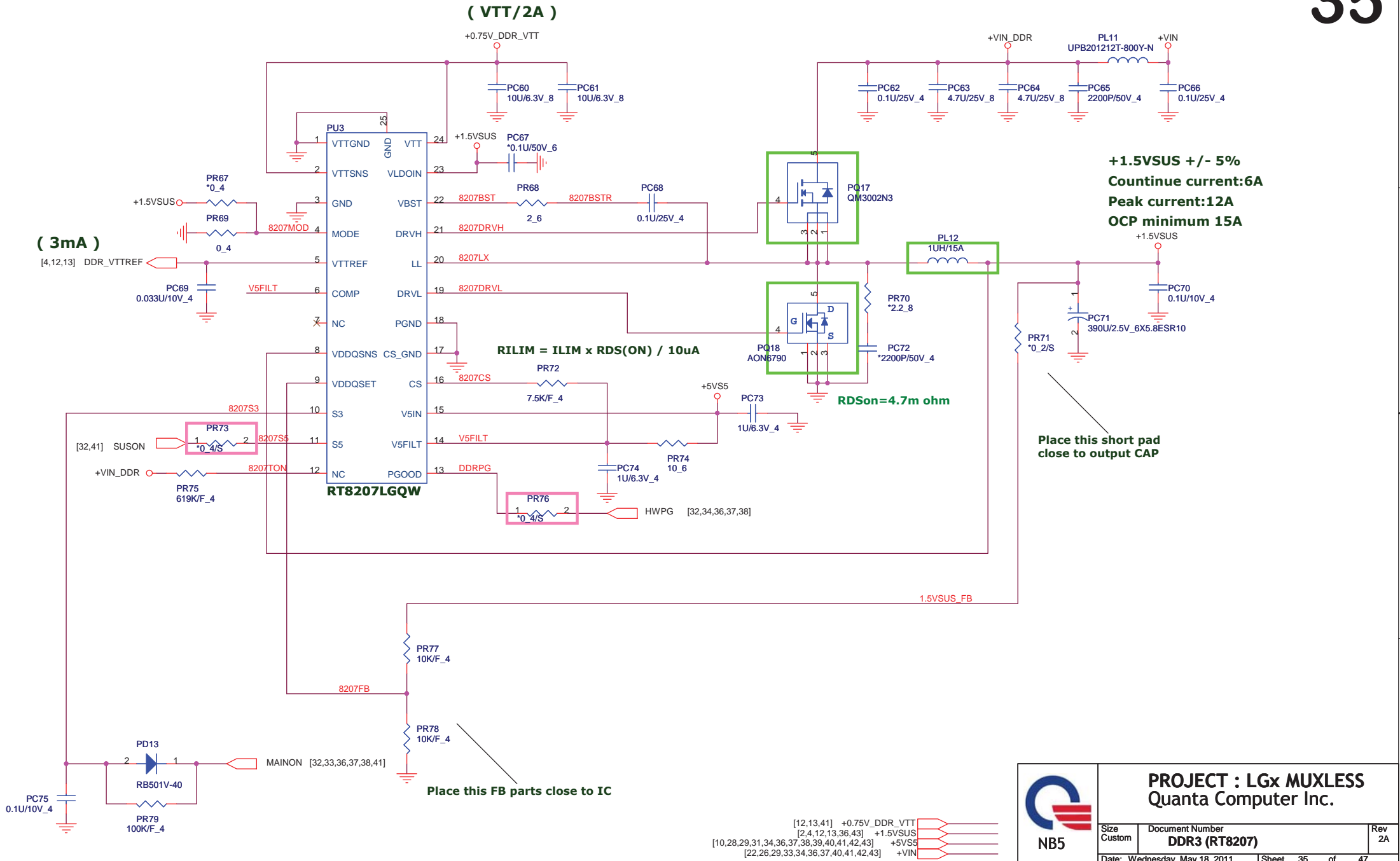
EMI Suggestion





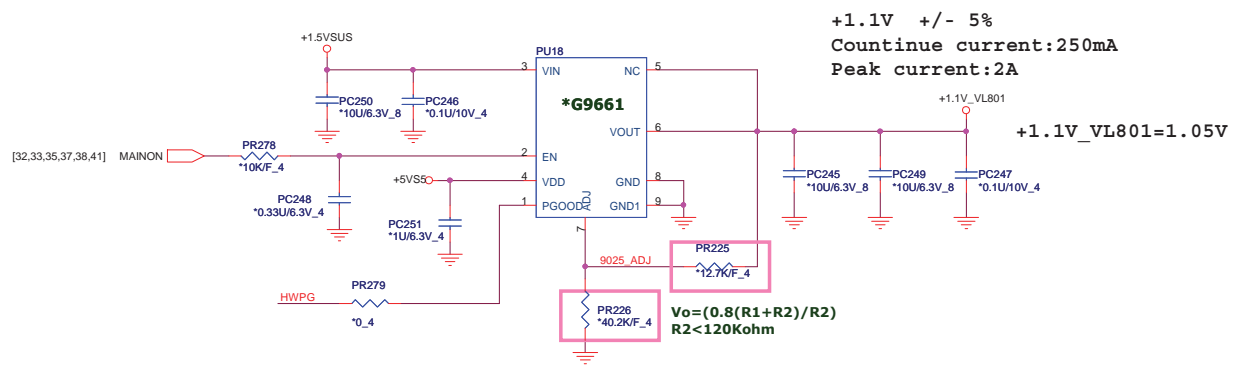
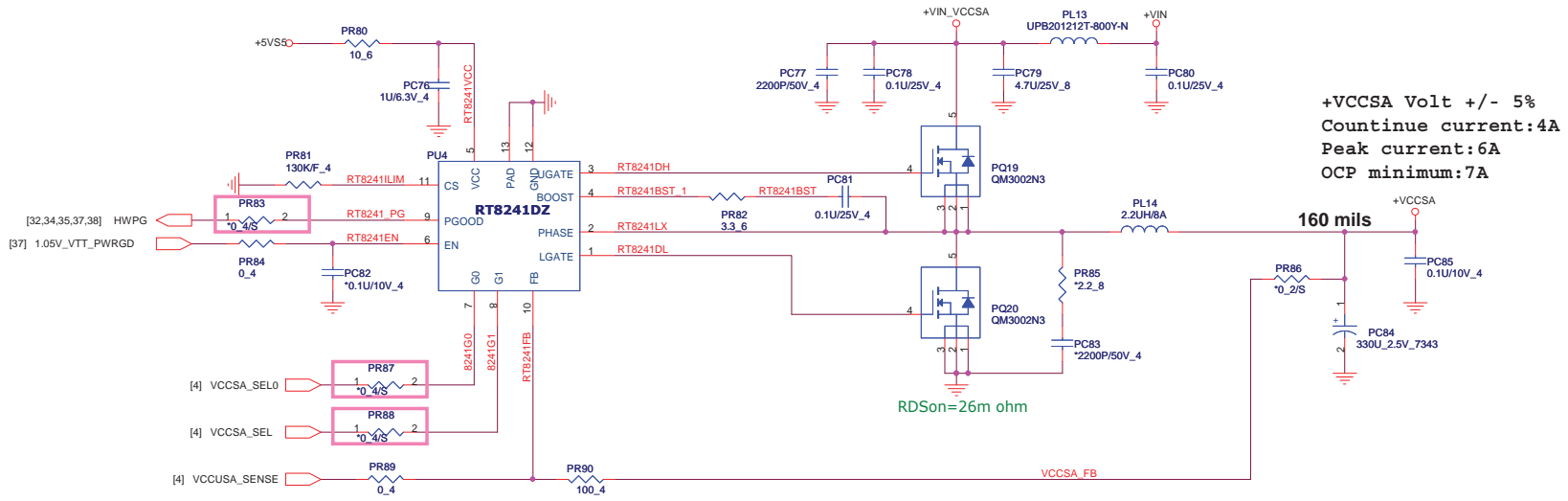
	PROJECT : LGx MUXLESS Quanta Computer Inc.		
	Size Custom	Document Number 3/5VSS (RT8223M)	Rev 2A
	Date: Wednesday, May 18, 2011		Sheet 34 of 47

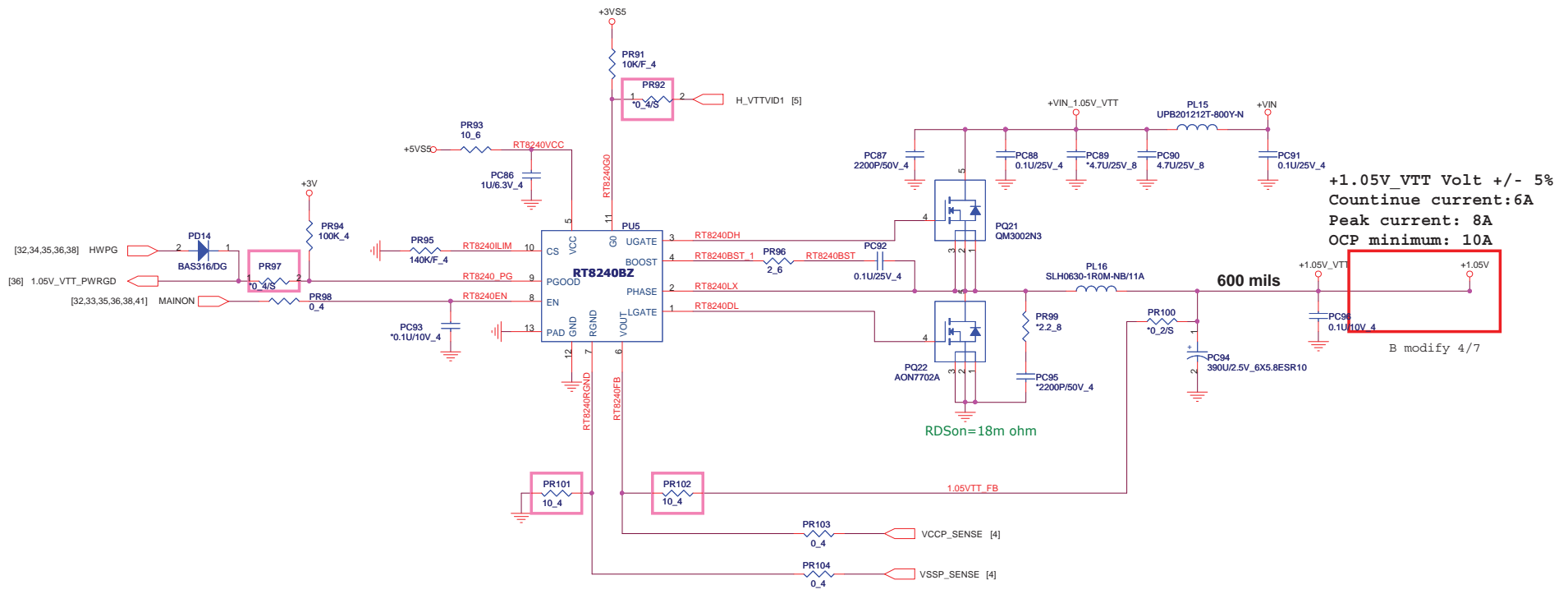
+5VPCU




PROJECT : LGx MUXLESS
Quanta Computer Inc.

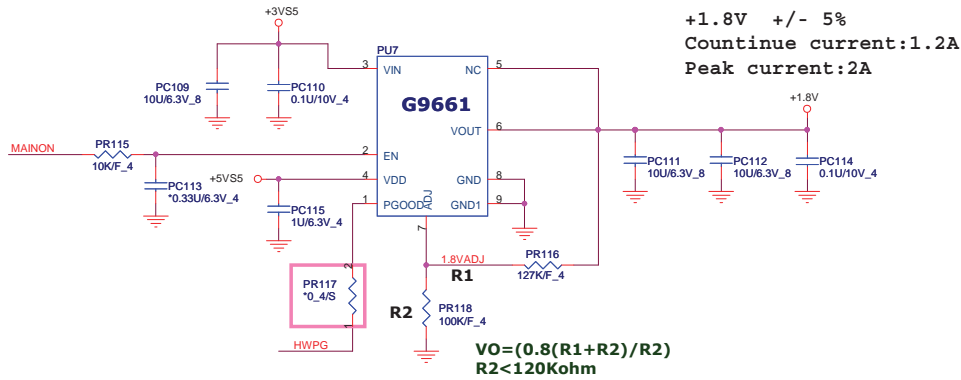
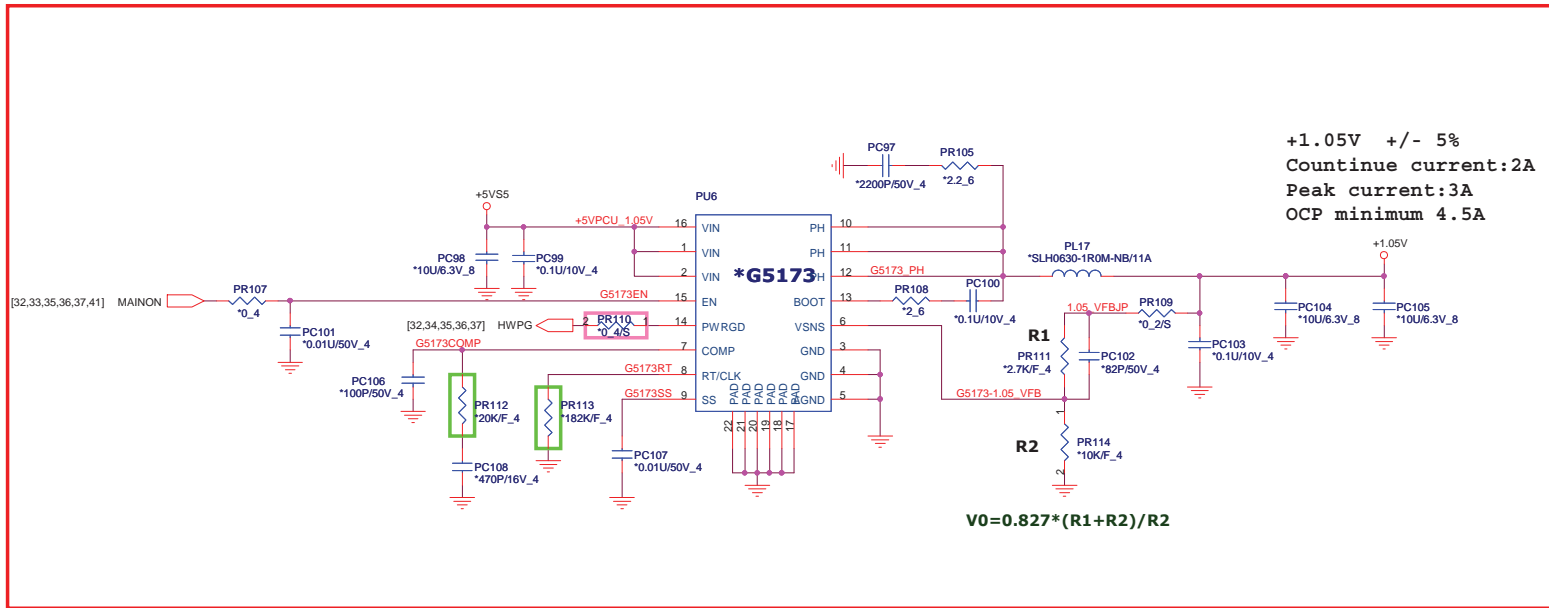
Size Custom	Document Number DDR3 (RT8207)	Rev 2A
Date: Wednesday, May 18, 2011 Sheet 35 of 47		



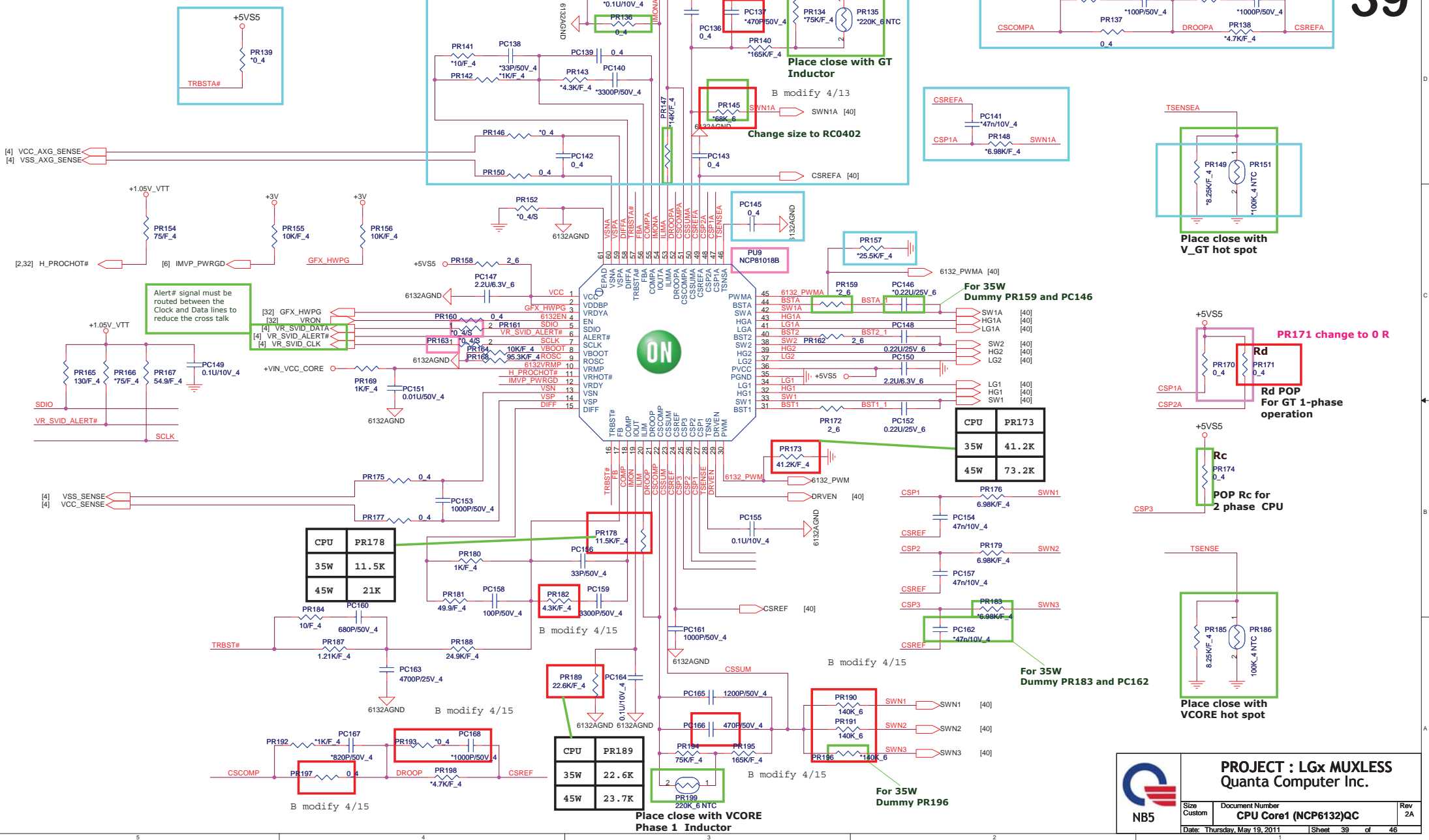


	PROJECT : LGx MUXLESS Quanta Computer Inc.		
	Size Custom	Document Number +1.05V_VTT(RT8240B)	Rev 2A
	Date: Wednesday, May 18, 2011	Sheet 37	of 46

B modify 4/7



LG2_DIS only sky blue color is disable GT setting



[4] VCC_AXG_SENSE
[4] VSS_AXG_SENSE

[2,32] H_PROCHOT#
[6] IMVP_PWRGD

[4] VSS_SENSE
[4] VCC_SENSE

B modify 4/15

B modify 4/15

B modify 4/15

B modify 4/15

B modify 4/15

B modify 4/15

B modify 4/15

B modify 4/15

For 35W Dummy PR159 and PC146

CPU	PR173
35W	41.2K
45W	73.2K

For 35W Dummy PR183 and PC162

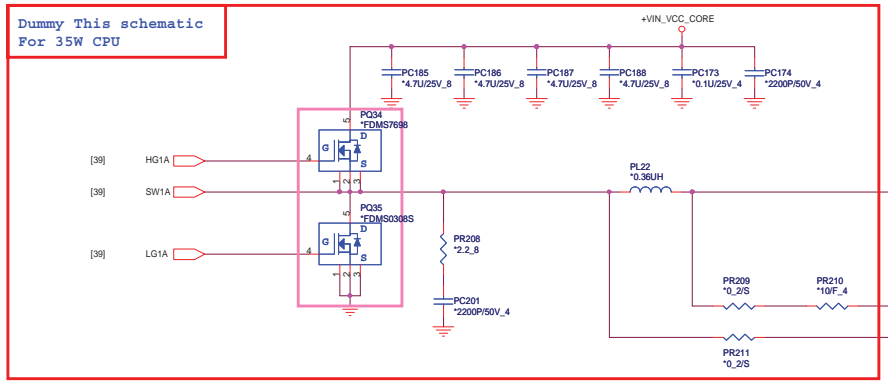
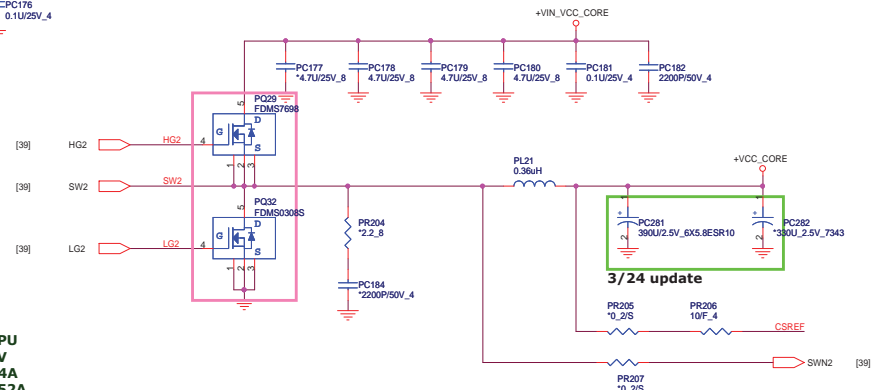
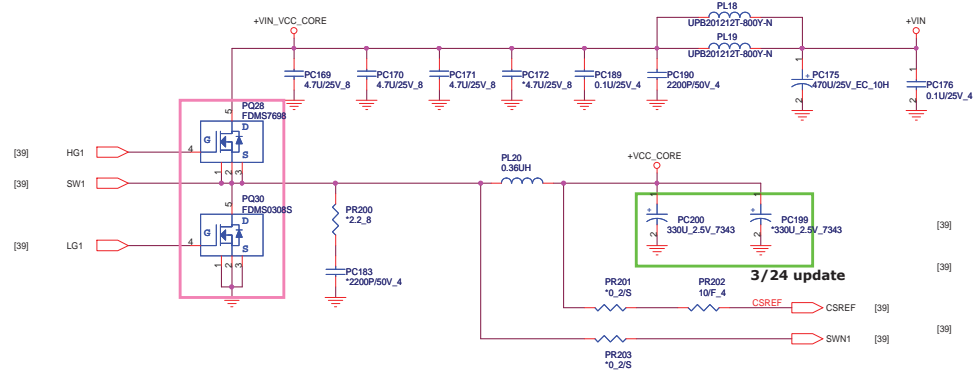
For 35W Dummy PR196



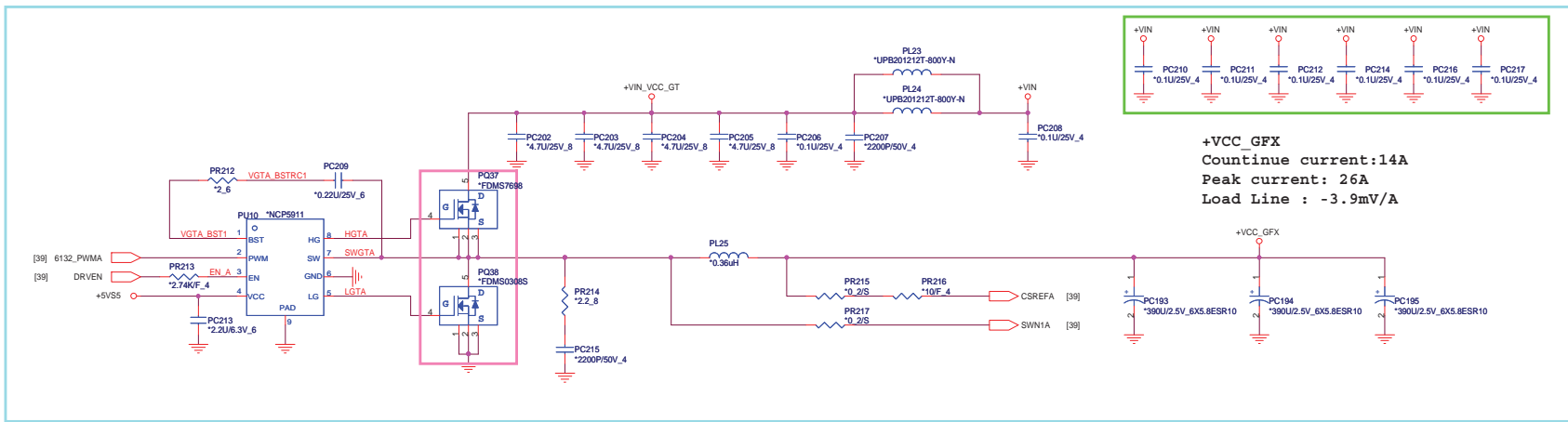
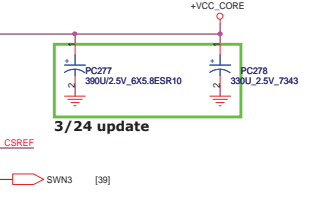
**PROJECT : LGx MUXLESS
Quanta Computer Inc.**

Size Custom	Document Number CPU Core1 (NCP6132)QC	Rev 2A
Date: Thursday, May 19, 2011	Sheet 39 of 46	

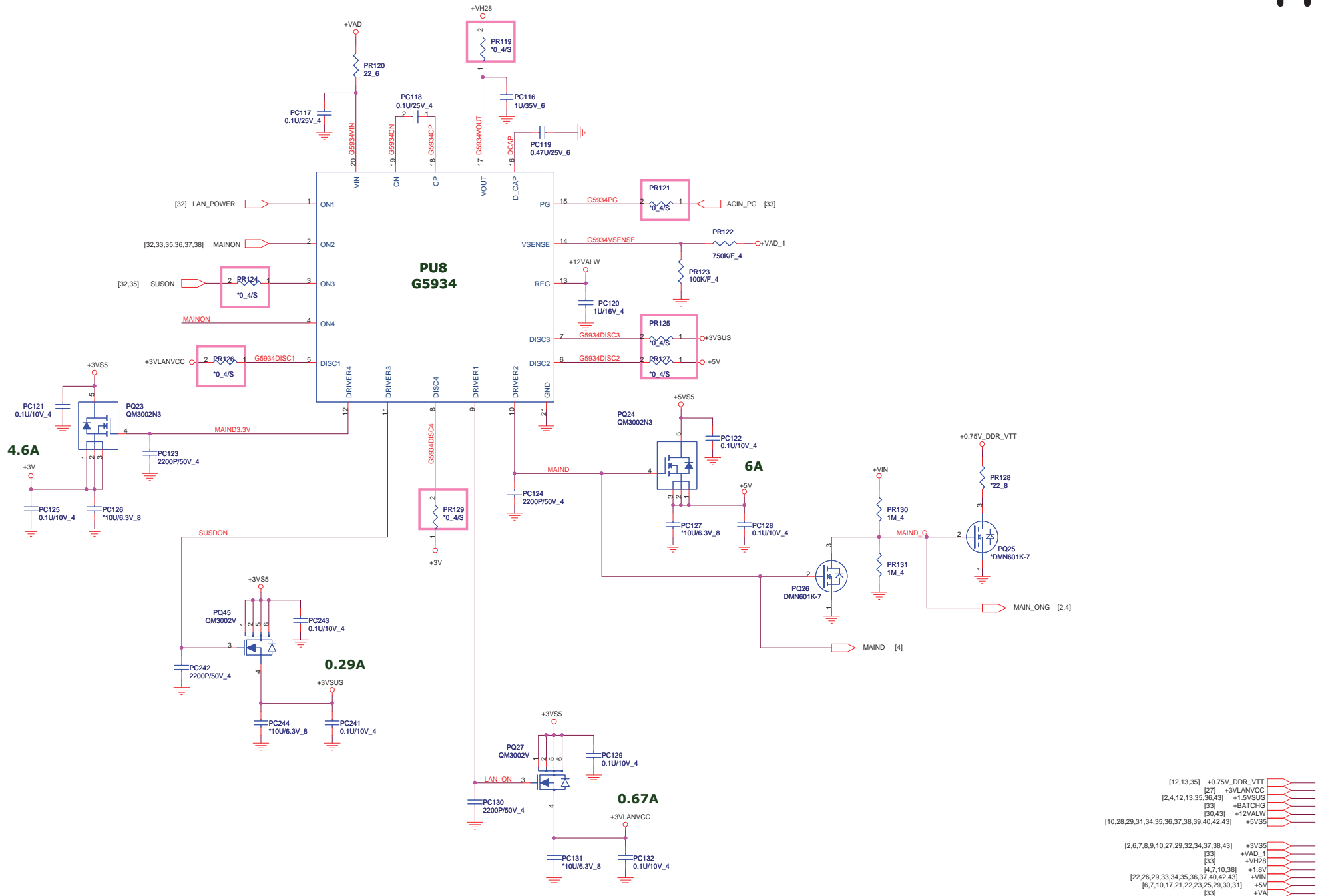
LG2_DIS only



QC 45W CPU
 VID1=0.9V
 IccMax=94A
 Icc_TDC=52A
 R_LL=1.9m ohm
 OCP~110A



sky blue color is disable GT setting



- [12,13,35] +0.75V_DDR_VTT
- [27] +3VLANVCC
- [2,4,12,13,35,36,43] +1.5VSUS
- [33] +BATVCC
- [30,43] +12VALW
- [10,28,29,31,34,35,36,37,38,39,40,42,43] +5VS5
- [2,6,7,8,9,10,27,29,32,34,37,38,43] +3VS5
- [33] +VAD_1
- [33] +VH28
- [4,7,10,38] +1.8V
- [22,26,29,33,34,35,36,37,40,42,43] +VIN
- [6,7,10,17,21,22,23,25,29,30,31] +5V
- [33] +VA

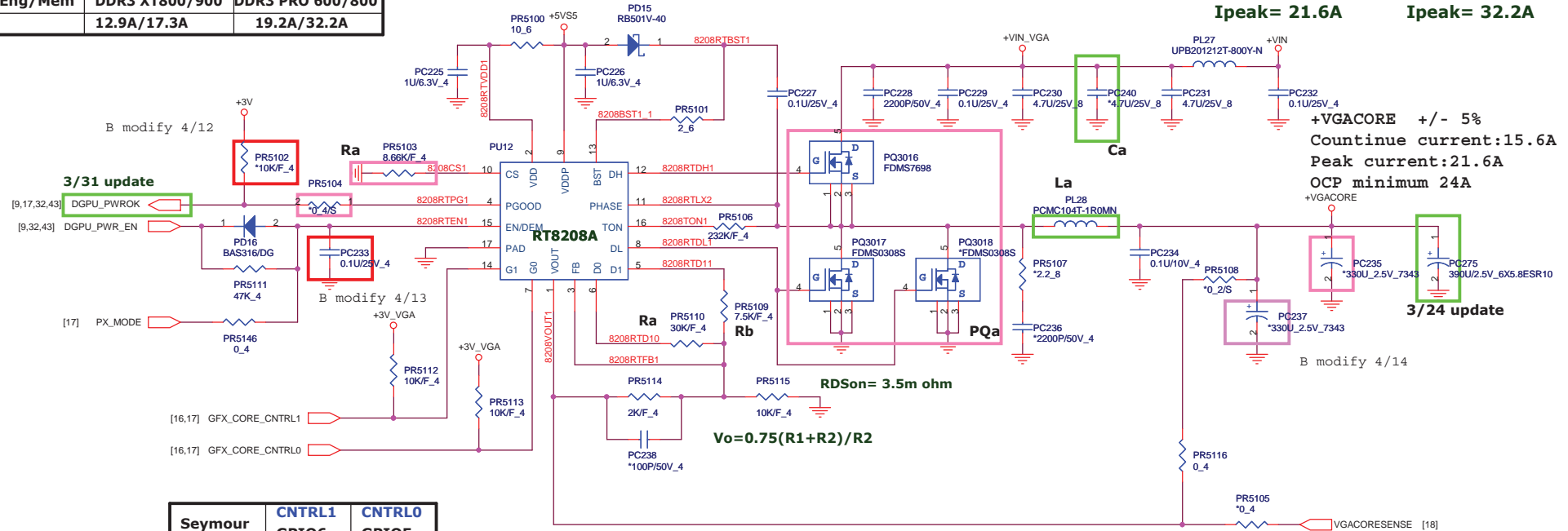
VGA Core

LG2_DIS only
VGA chip only Seymour

	Seymour (OCP 24A)	Whistler
Ca	PC240 X	V
Cb	PC235 PC237 X	V
PQa	PQ3018 X	V
La	1U/15A	0.45U25A
Ra	8.66K-ohm	8.66K-ohm
Eng/Mem	DDR3 XT800/900	DDR3 PRO 600/800
	12.9A/17.3A	19.2A/32.2A

Seymour-XT 64bit
Irms= 15.6A
Ipeak= 21.6A

Whistler
Irms= 19.2A
Ipeak= 32.2A



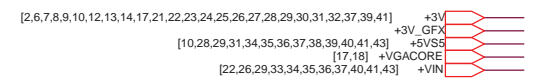
+VGACORE +/- 5%
Countinue current:15.6A
Peak current:21.6A
OCP minimum 24A

Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
0.95V	0	1
1.1V	1	0
1.15V	1	1

default

Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
1.0V	0	1
1.05V	1	0
1.15V	1	1

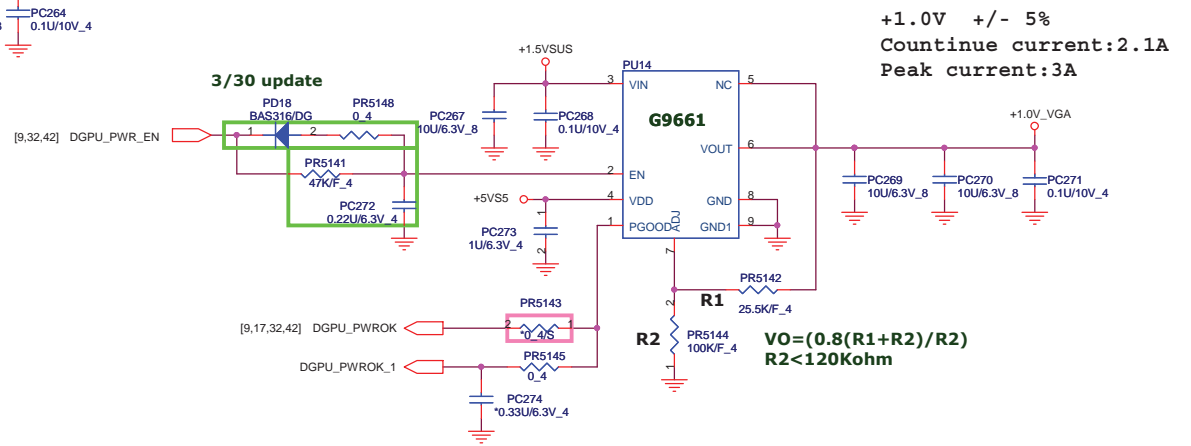
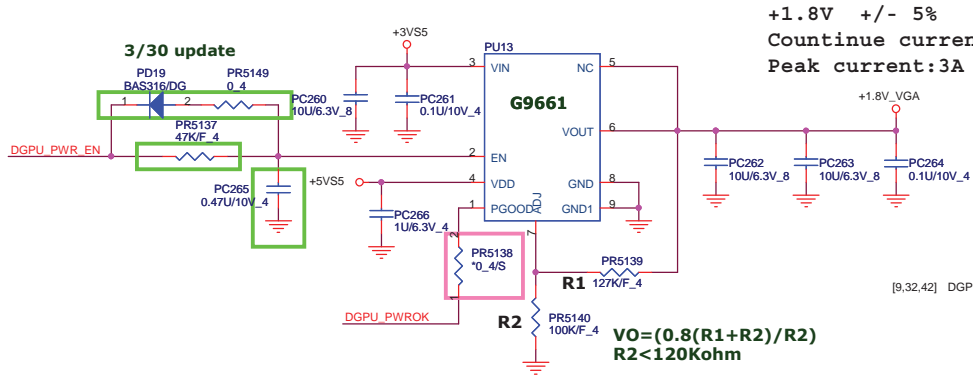
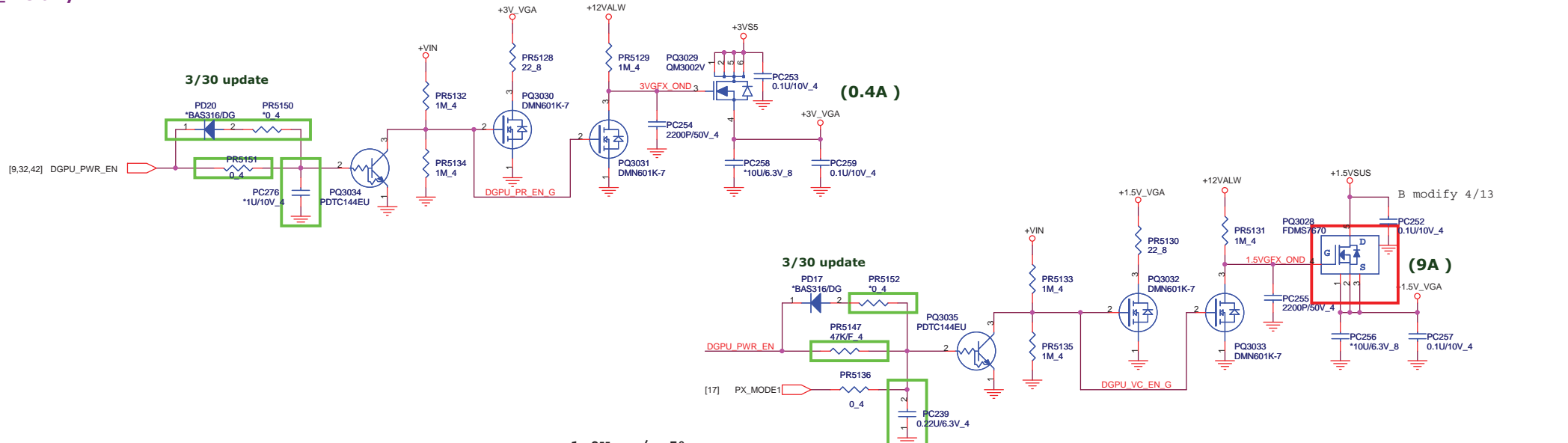
Ra --> 15K-ohm
Rb --> 10K-ohm



PROJECT : LGx MUXLESS
Quanta Computer Inc.

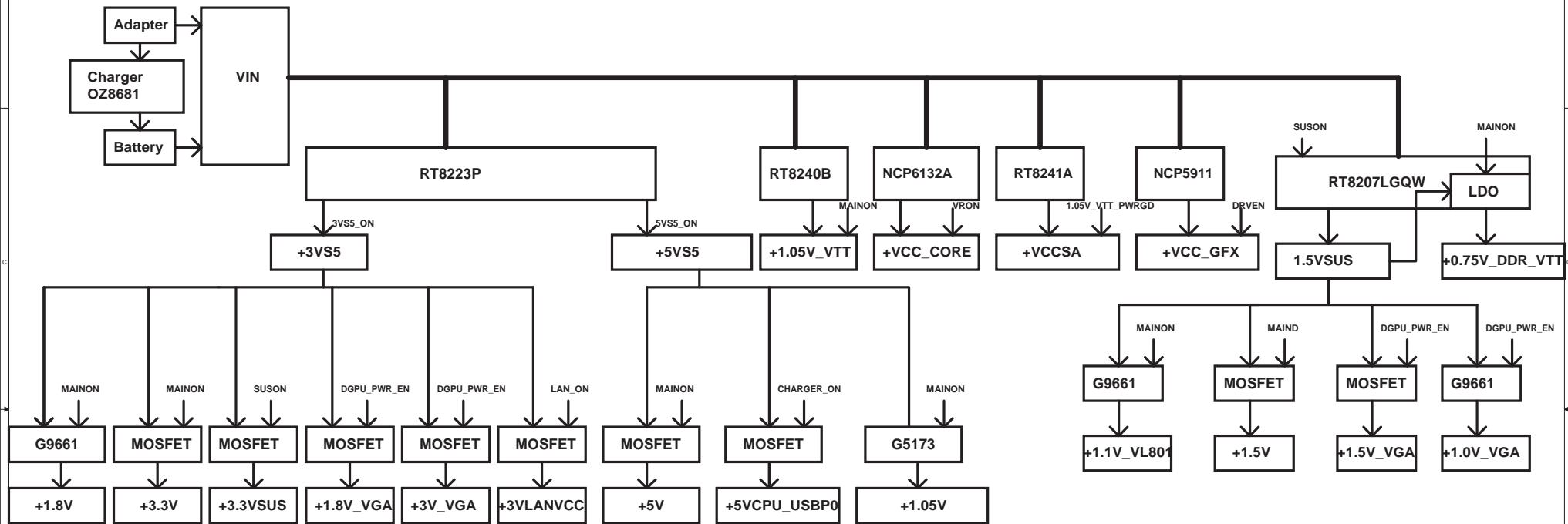
Size Custom	Document Number +VGACORE (RT8208)	Rev 2A
Date: Wednesday, May 18, 2011	Sheet 42 of 46	

LG2_DIS only

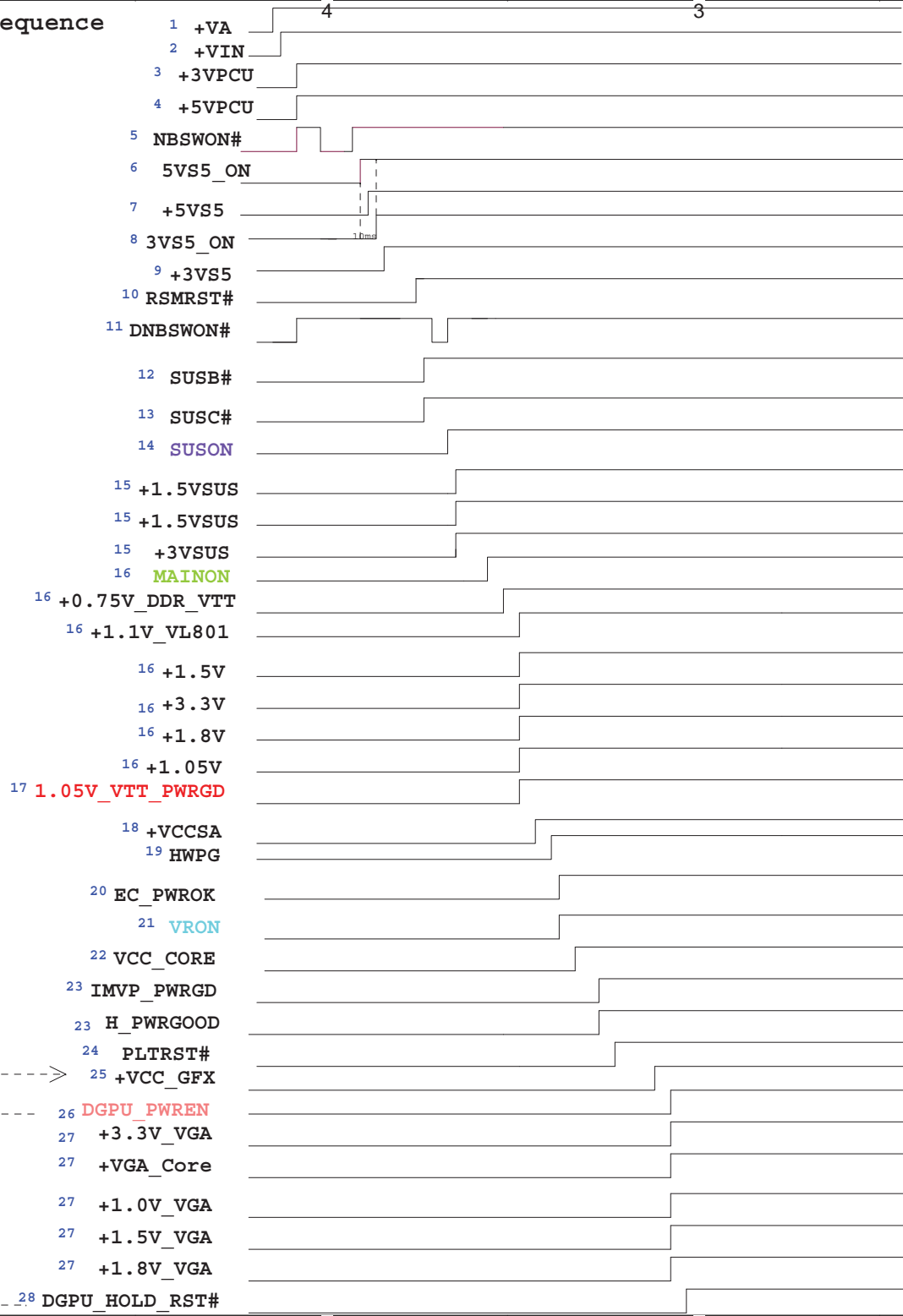


- [2,4,12,13,35,36] +1.5VSUS
- [2,6,7,8,9,10,27,29,32,34,37,38,41] +3VS5
- [15,16] +3V_VGA
- [14,16,18] +1.8V_VGA
- [15,18,19,20] +1.5V_VGA
- [14,16,17,18] +1.0V_VGA
- [30,41] +12VALW
- [22,26,29,33,34,35,36,37,40,41,42] +VIN

LG2/4 Power rail map




LG2/4/6 Power Sequence



UMA/Muxless internal GPU Sequence

DIS GPU Power Sequence

	PROJECT : LG2/4 DIS		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	Power Sequence	3A	
Date:	Sheet	of	47

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