

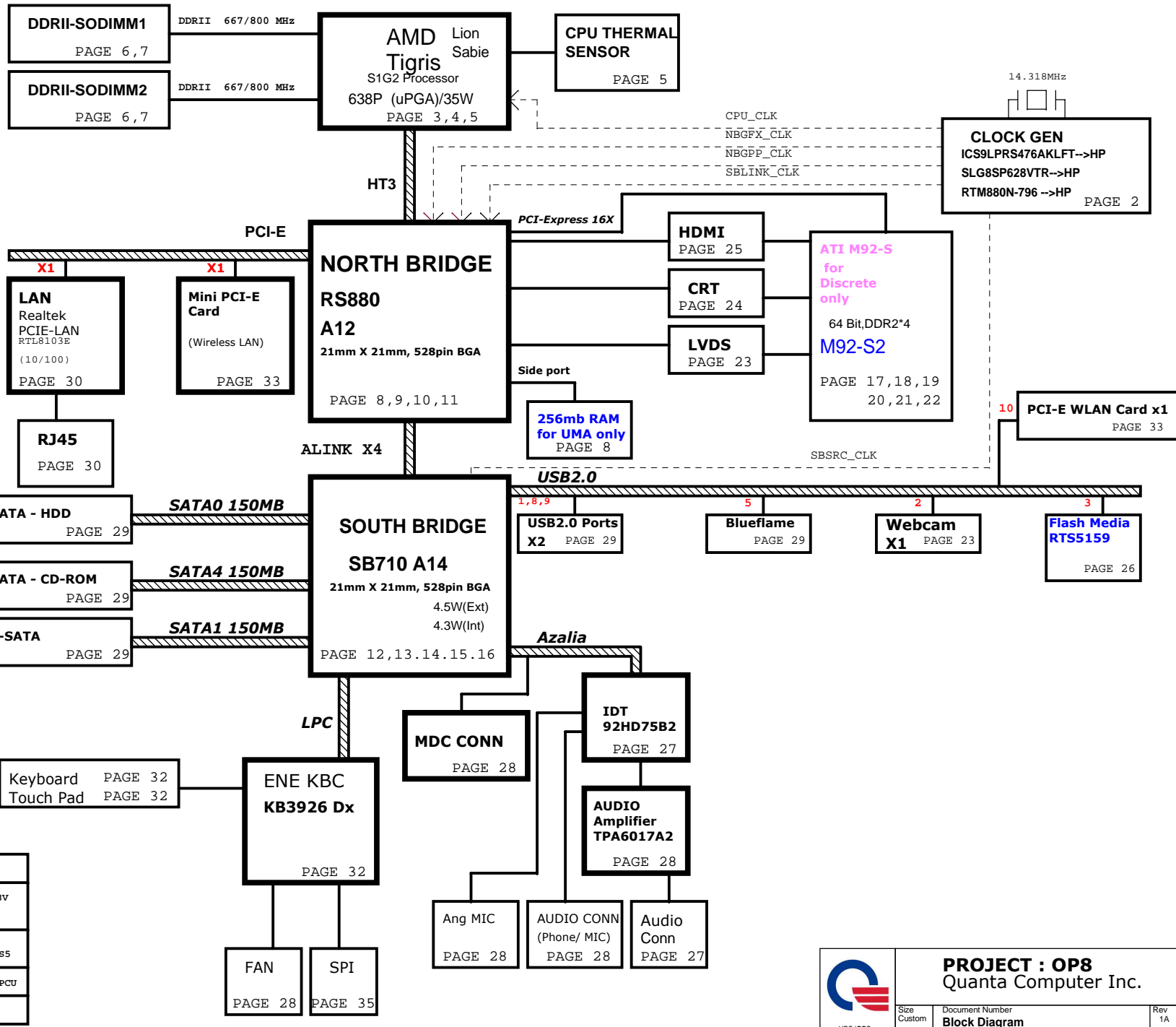
# OP8 SYSTEM DIAGRAM



01

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : IN1
- LAYER 3 : IN2
- LAYER 4 : VCC
- LAYER 5 : IN3
- LAYER 6 : BOT



- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR\_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V~1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

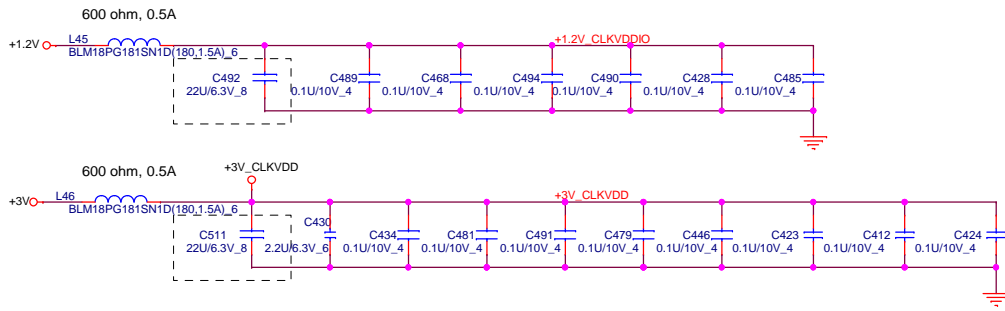
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

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Quanta Computer Inc.

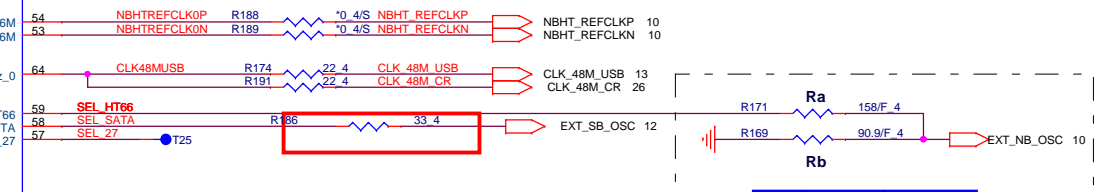
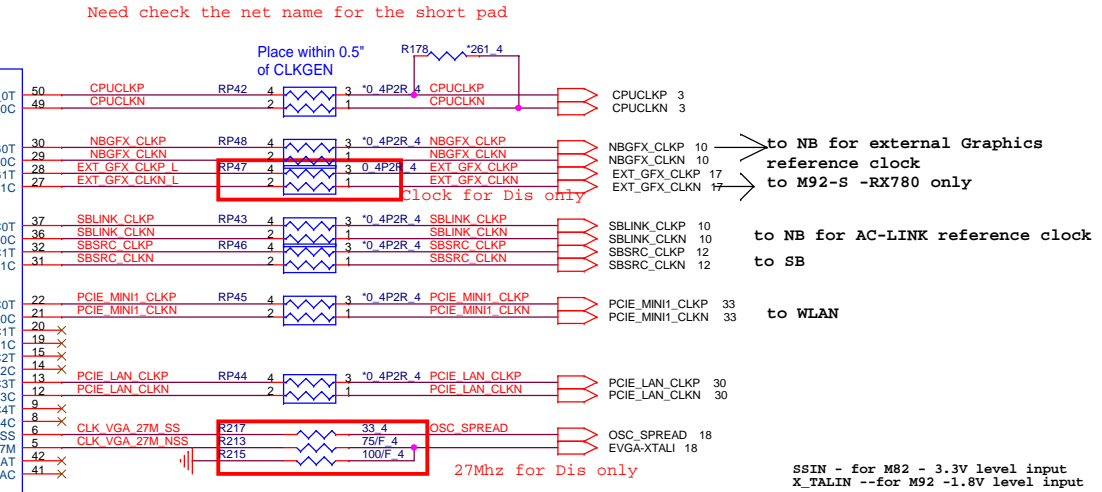
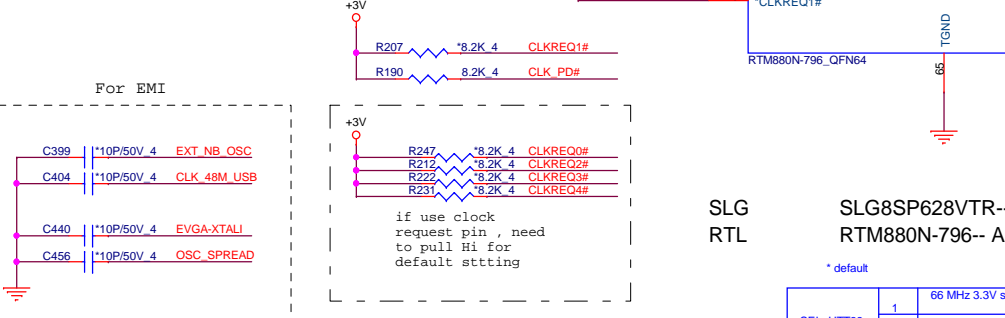
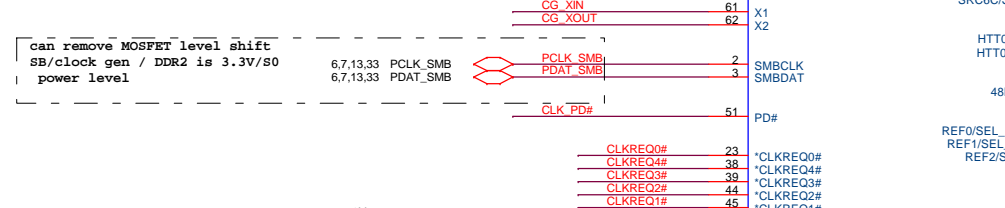
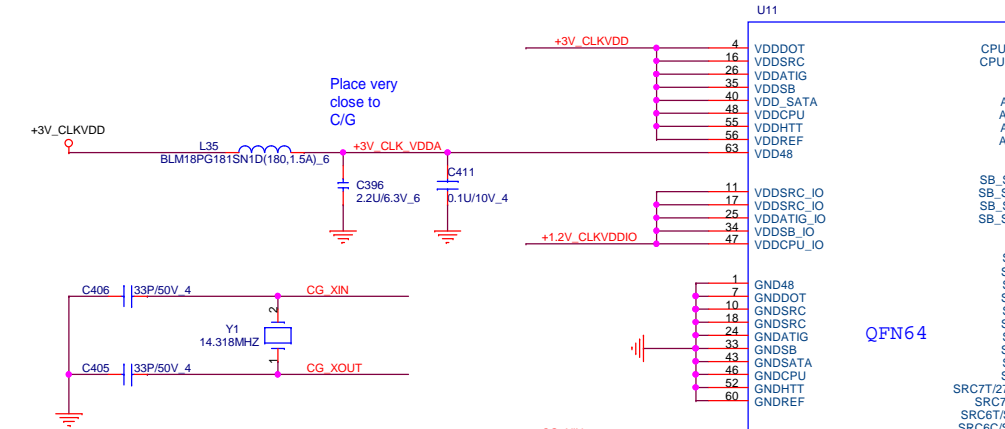
Size Custom Document Number  
**Block Diagram**

Date: Friday, March 20, 2009 Sheet 1 of 42

Rev 1A

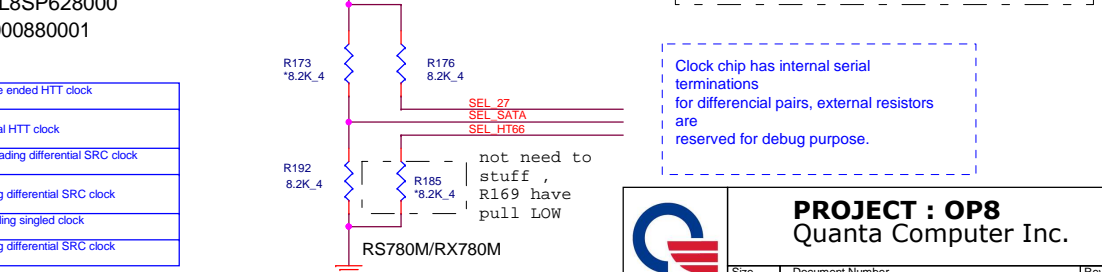


CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP48 STUFF	RP48 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP47 STUFF	RP47 NC	to M92-S external reference clock -RX780 only
SBLINK_CLKP SBLINK_CLKN	RP43 STUFF	RP43 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R213, R215 STUFF	R213, R215 NC	To M92-S 27Mhz - RX780 only



	RX880	RS880
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)-L-F -->CS11302FB15  
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00  
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15  
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11



SLG  
RTL  
SLG8SP628VTR--AL8SP628000  
RTM880N-796-- AL000880001

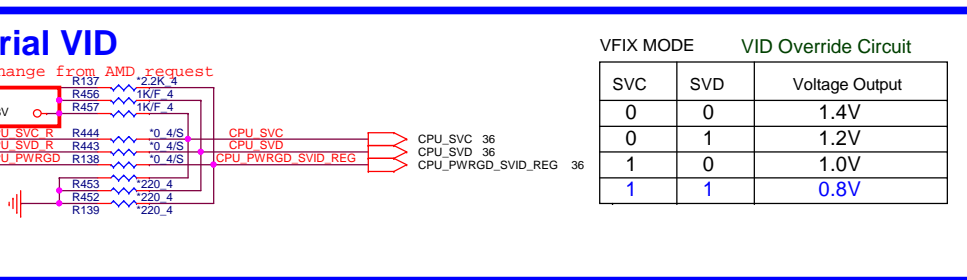
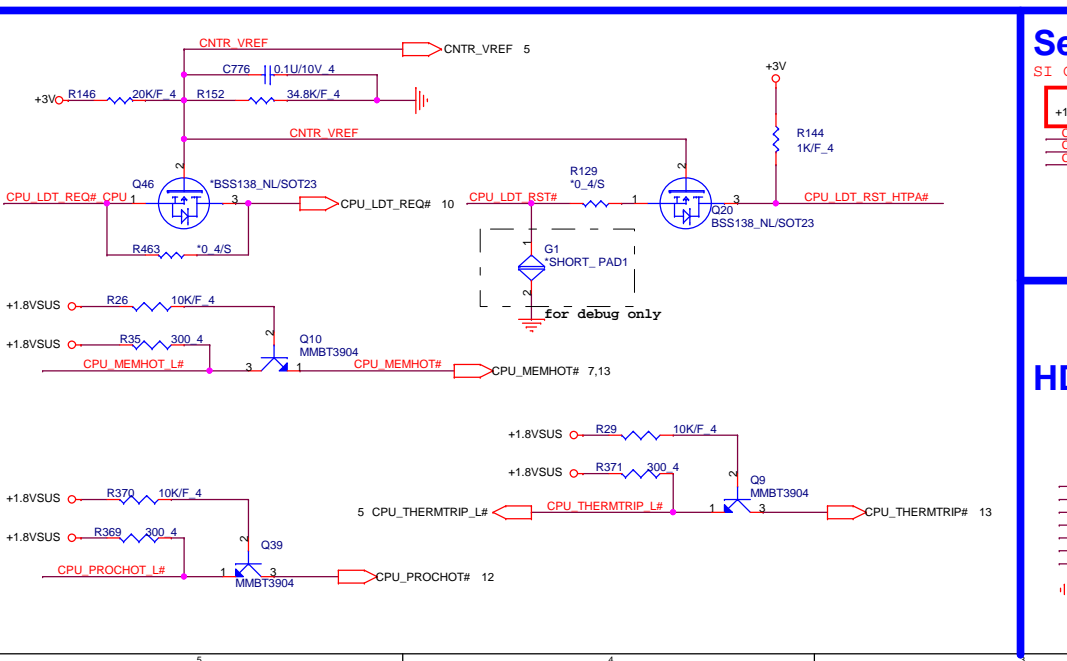
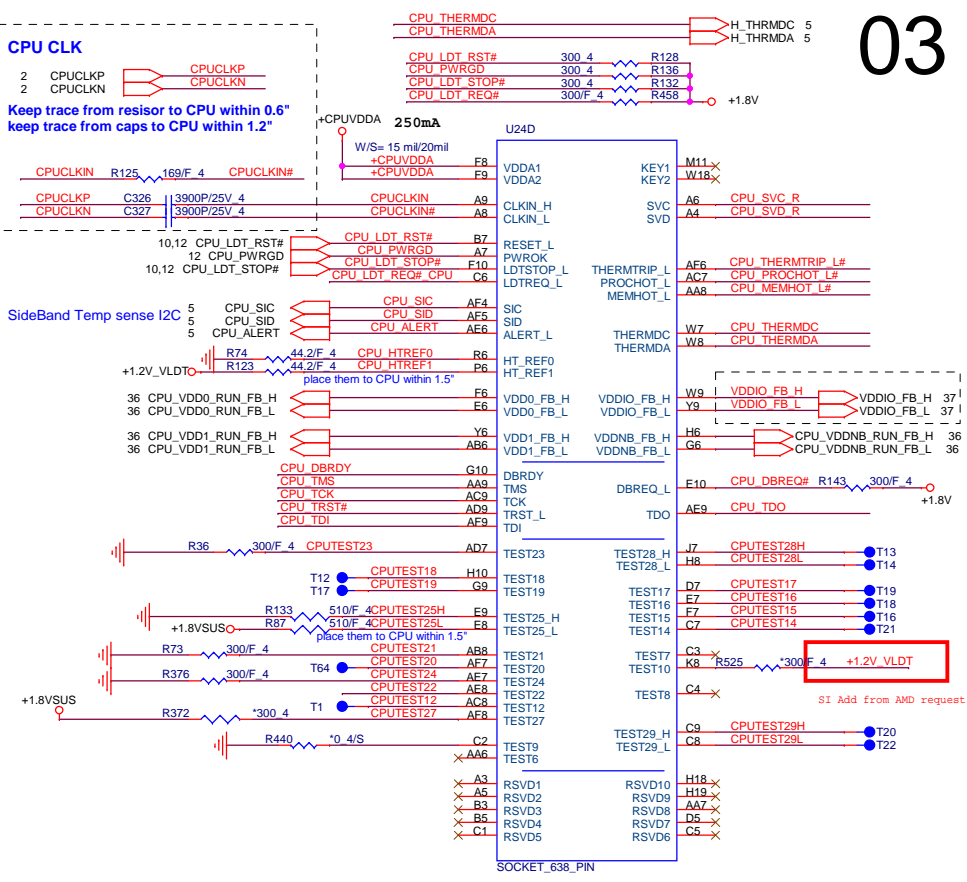
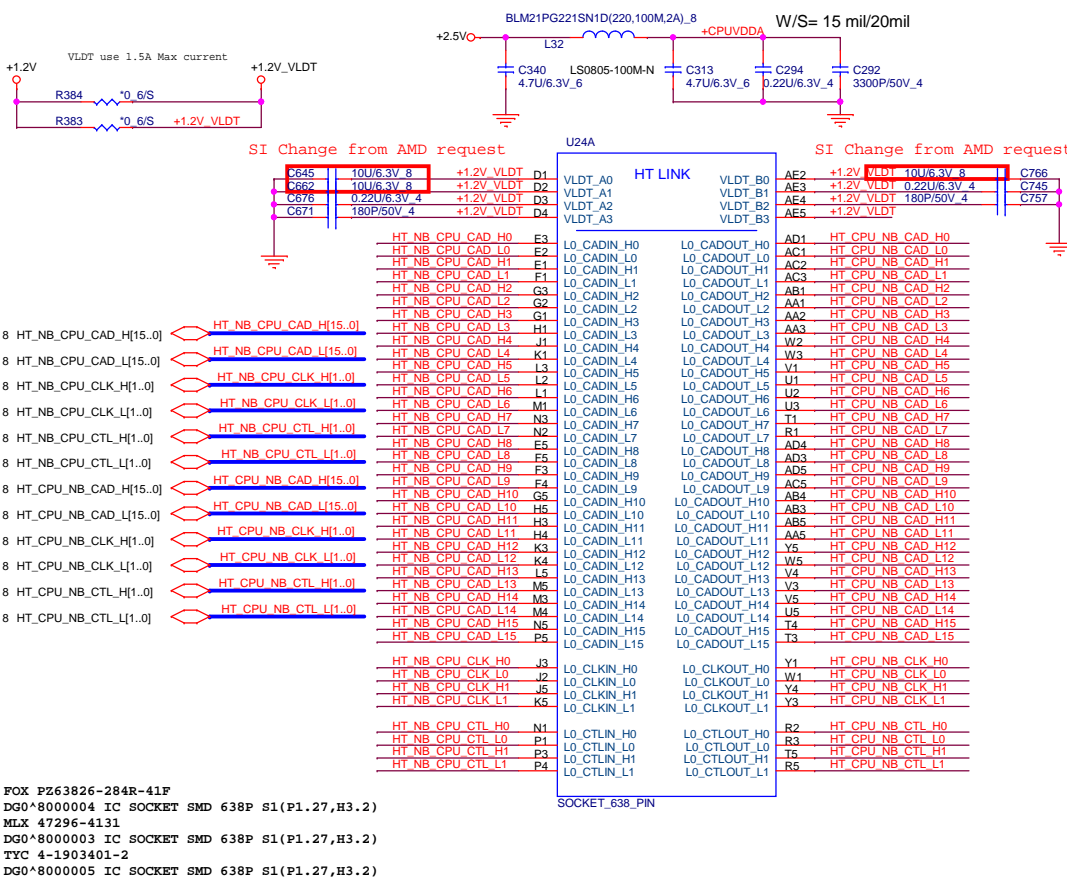
\* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

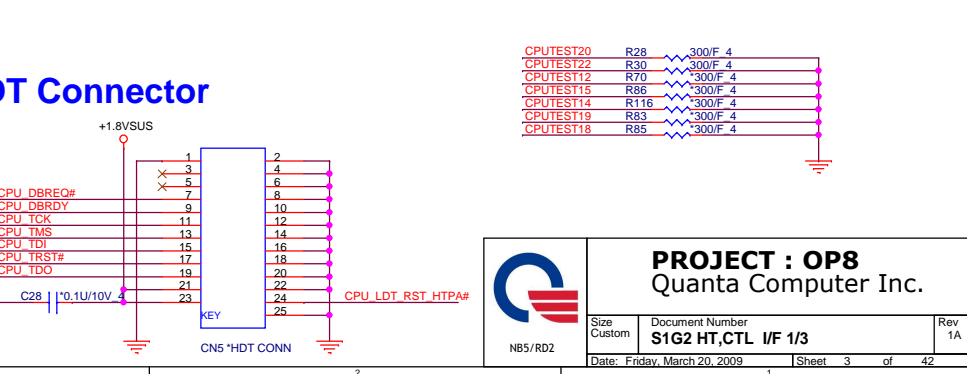
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom Document Number  
**Clock Generator** Rev 1A

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VFIX MODE		VID Override Circuit	
SVC	SVD	Voltage Output	
0	0	1.4V	
0	1	1.2V	
1	0	1.0V	
1	1	0.8V	

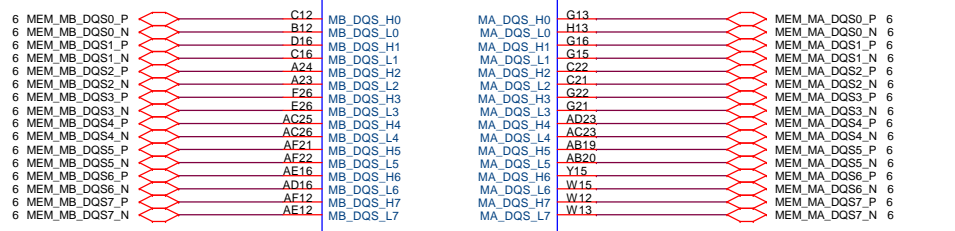
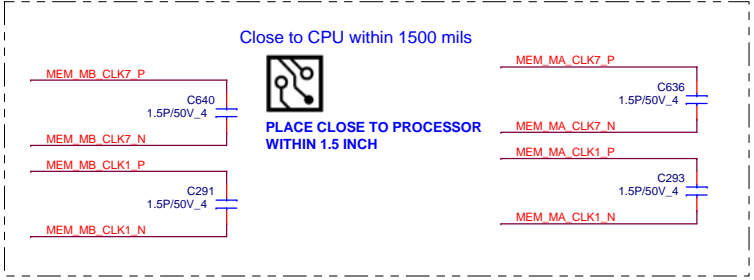
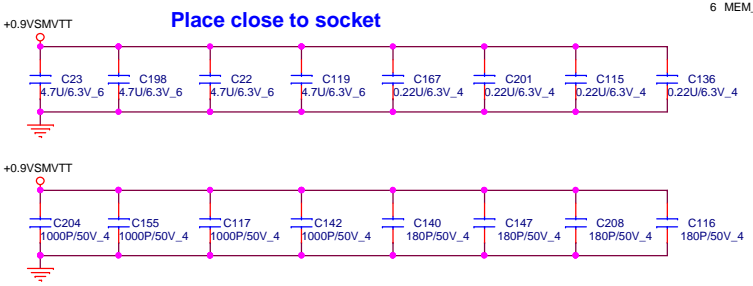
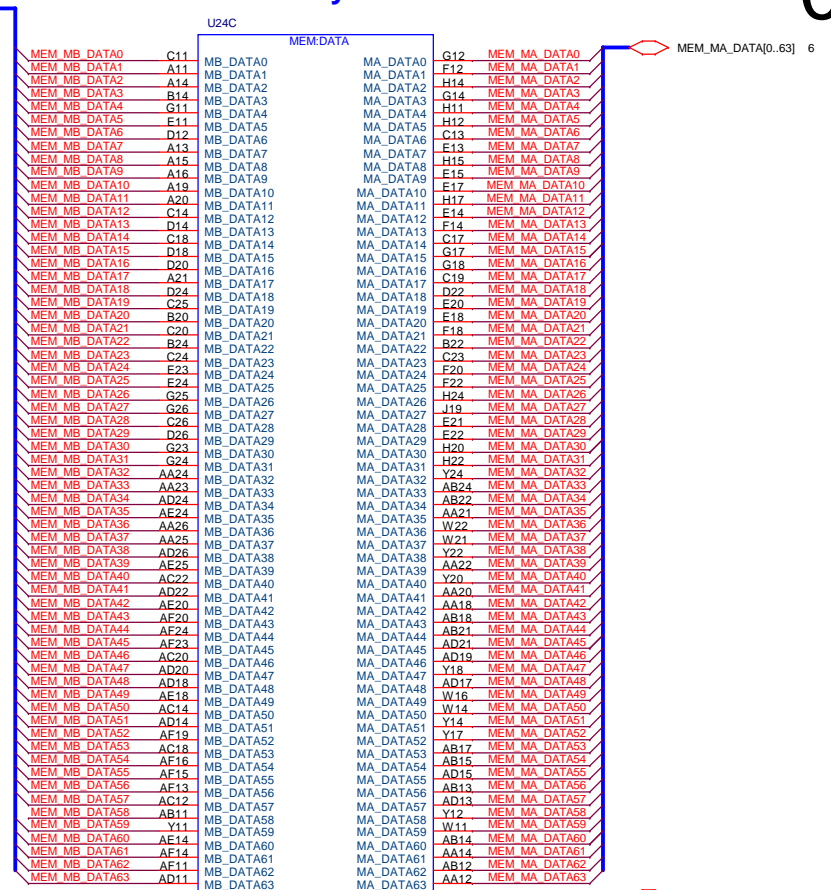
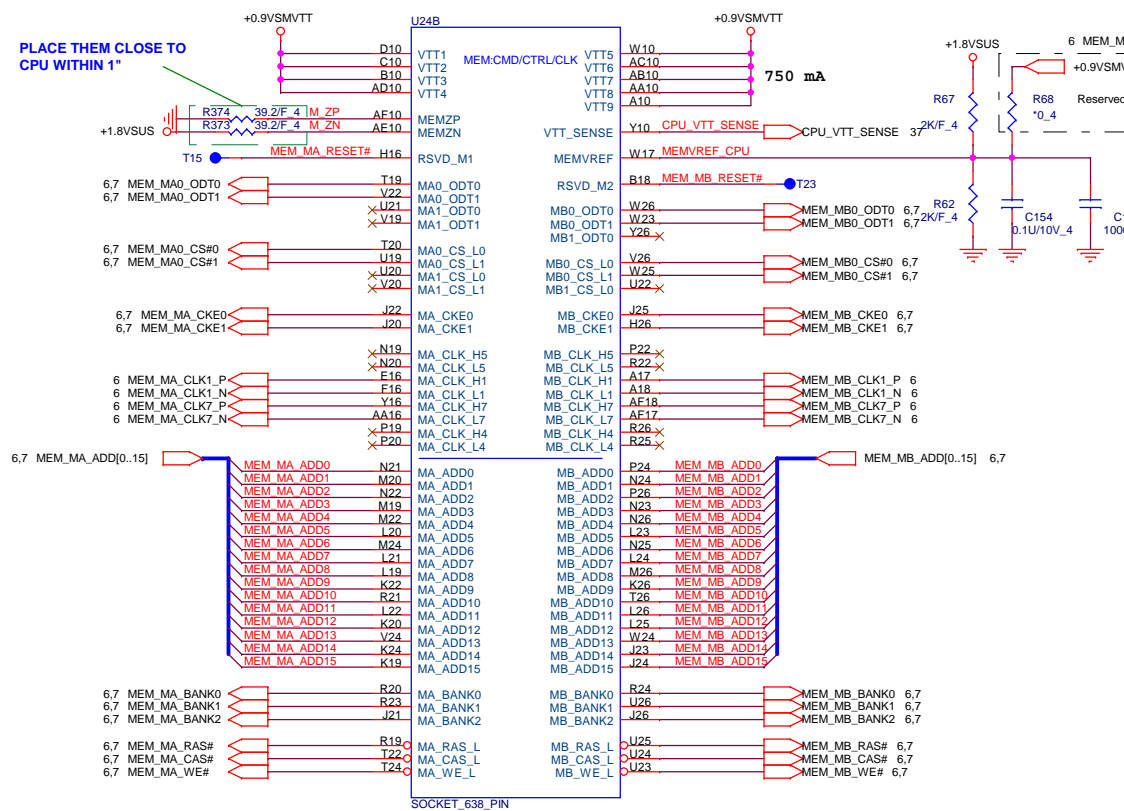


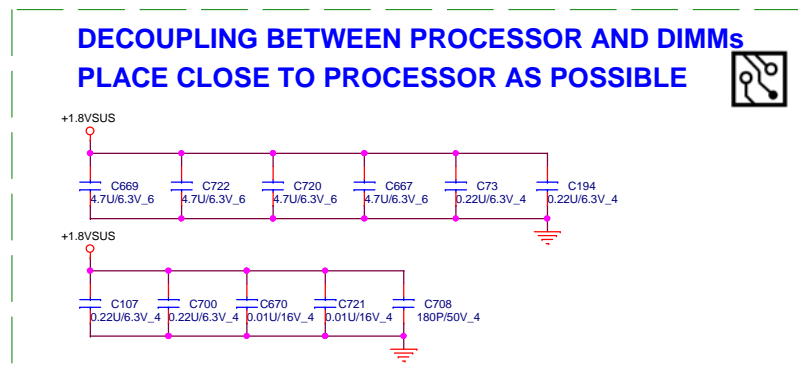
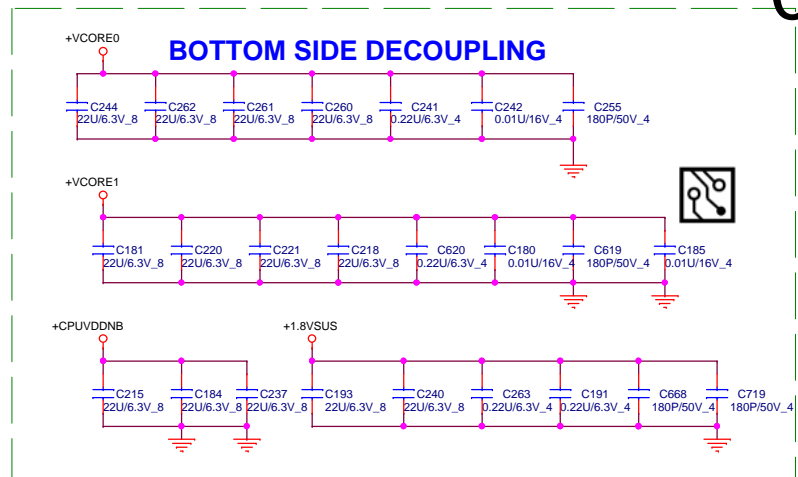
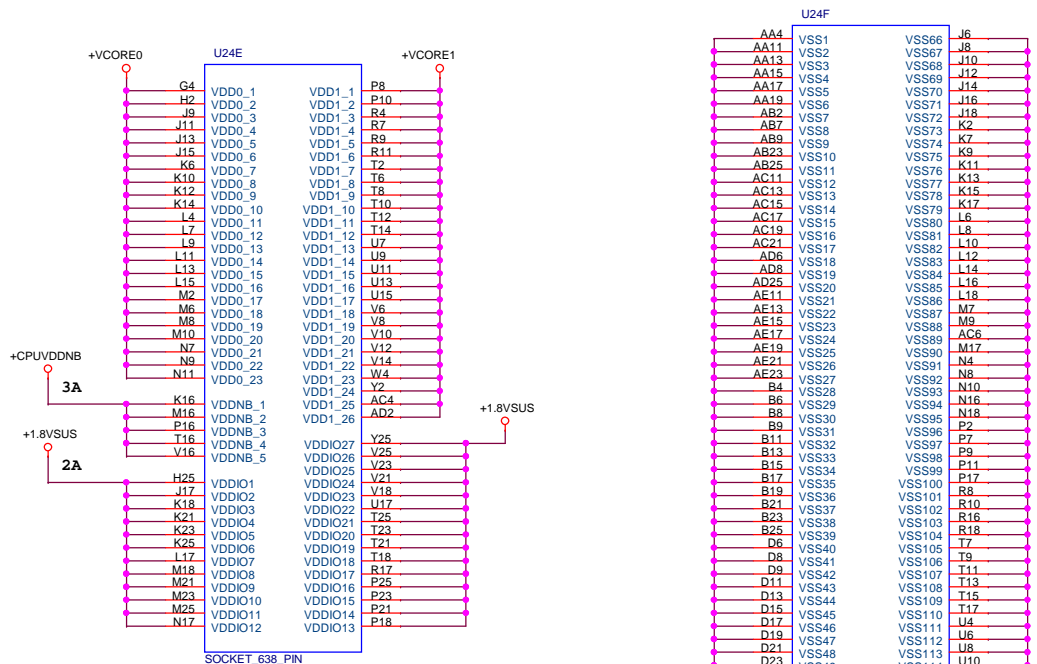
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom    Document Number **S1G2 HT,CTL I/F 1/3**    Rev 1A  
Date: Friday, March 20, 2009    Sheet 3 of 42

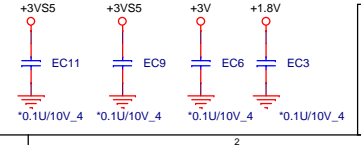
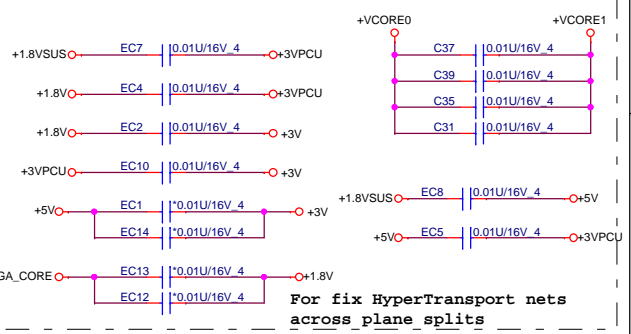
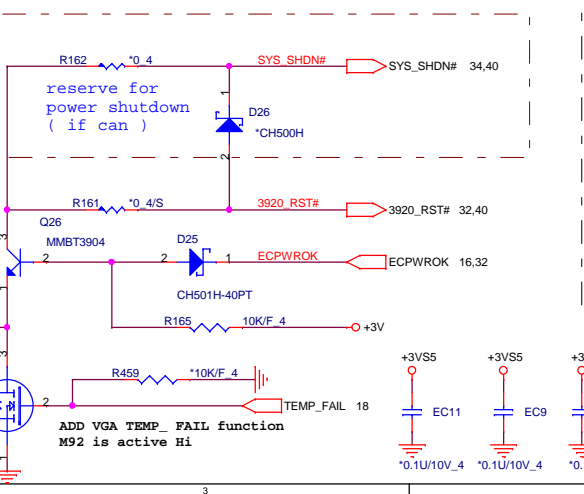
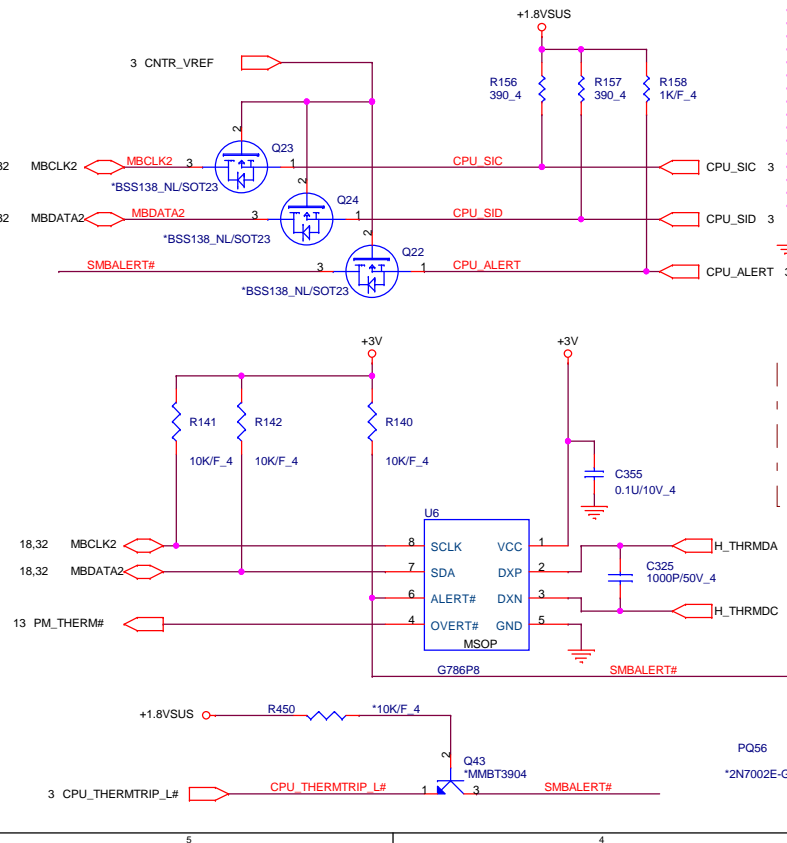
# Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"





# PROCESSOR POWER AND GROUND



**PROJECT : OP8**  
Quanta Computer Inc.

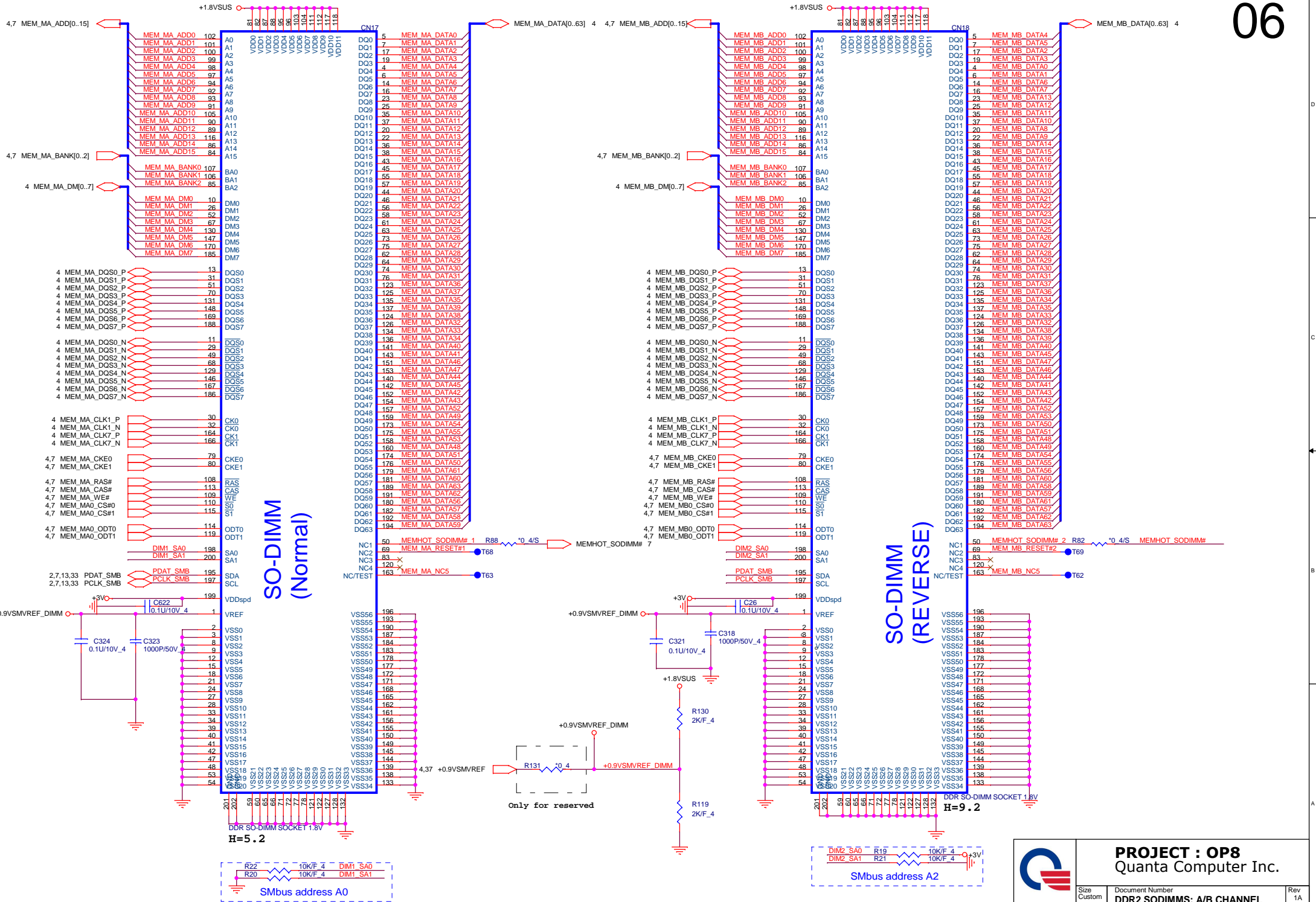
Date: Friday, March 20, 2009

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Rev 1A

Size Custom Document Number S1G2 PWR & GND 3/3

NB5/RD2

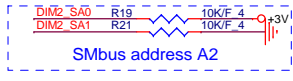
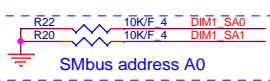


**SO-DIMM  
(Normal)**

**SO-DIMM  
(REVERSE)**

DDR SO-DIMM SOCKET 1.8V  
H=5.2

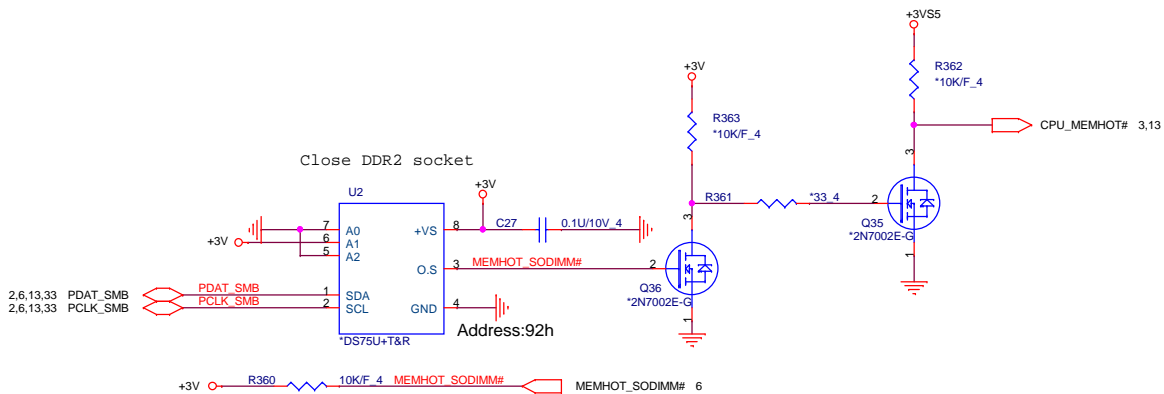
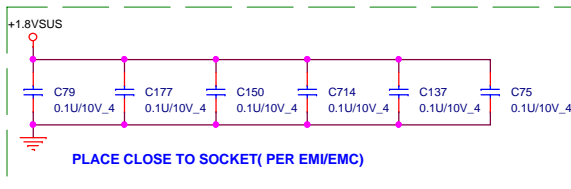
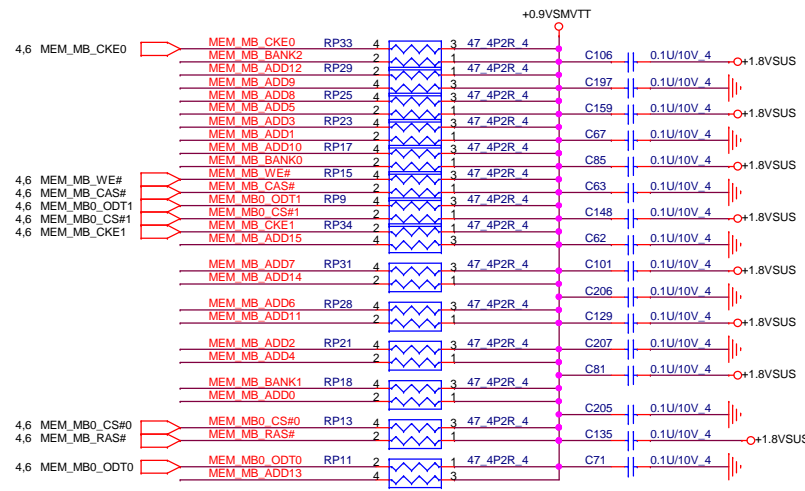
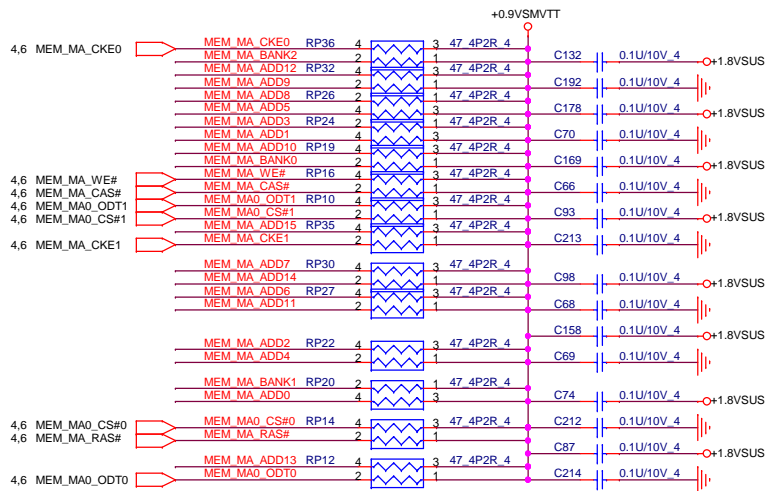
DDR SO-DIMM SOCKET 1.8V  
H=9.2



**PROJECT : OP8**  
Quanta Computer Inc.

4,6 MEM\_MA\_ADD[0..15] MEM\_MA\_ADD[0..15]  
4,6 MEM\_MA\_BANK[0..2] MEM\_MA\_BANK[0..2]

4,6 MEM\_MB\_ADD[0..15] MEM\_MB\_ADD[0..15]  
4,6 MEM\_MB\_BANK[0..2] MEM\_MB\_BANK[0..2]



**PROJECT : OP8**  
Quanta Computer Inc.

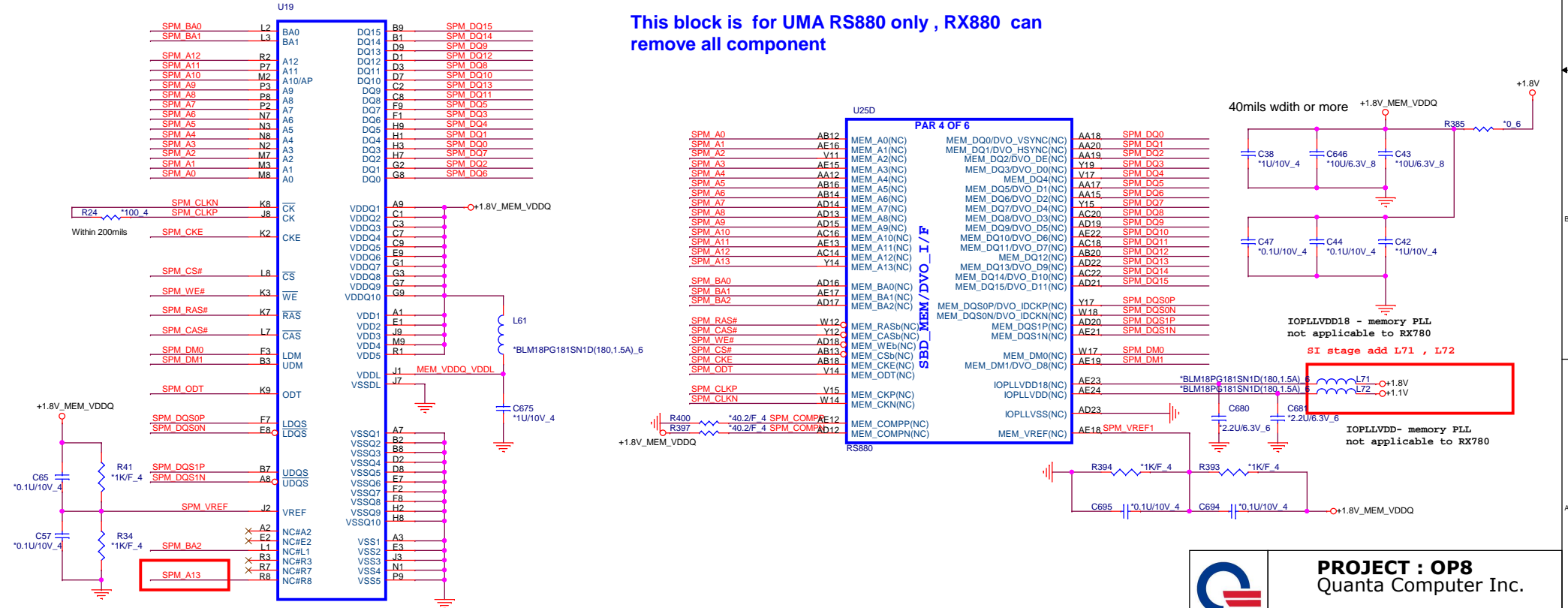


signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

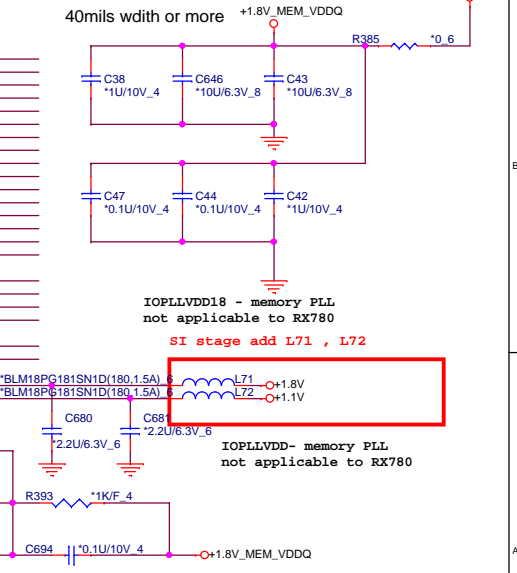
RES CHIP 1.21K 1/16W +-1%(0402)  
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)  
P/N : CS13012FB14

**This block is for UMA RS880 only, RX880 can remove all component**



SI add A13 for side port function \*HYB18T512161B2F-25

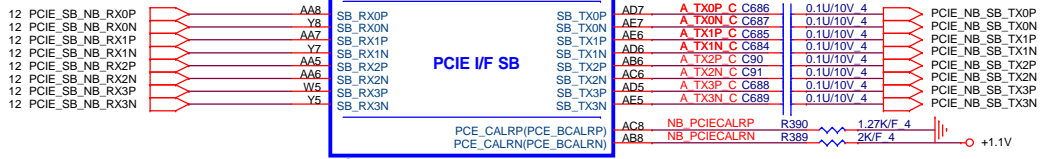
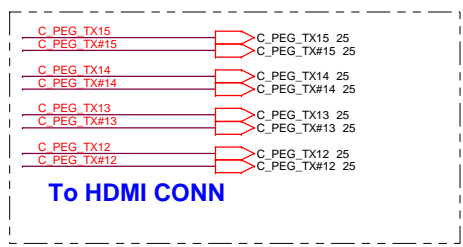
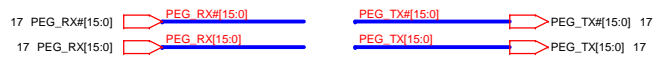
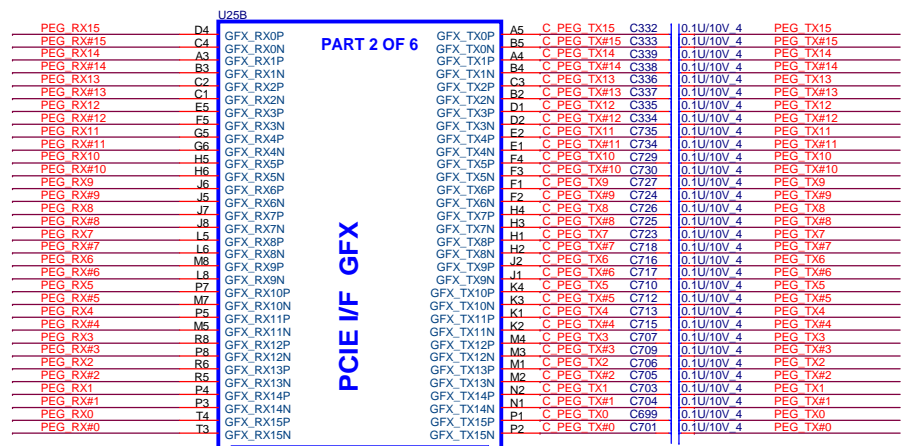


**PROJECT : OP8**  
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Size Custom Document Number NB5/RD2  
Date: Friday, March 20, 2009 Sheet 8 of 42

RS740/RS780-HT LINK I/F 1/5 Rev 1A





RS880

**RS880 Display Port Support (muxed on GFX)**

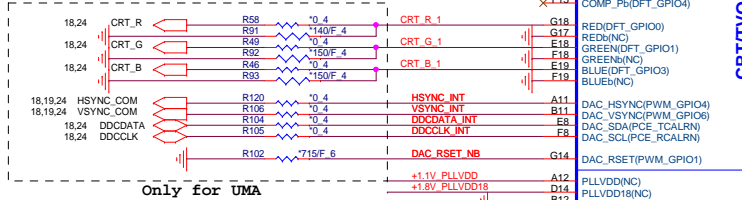
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



**PROJECT : OP8**  
Quanta Computer Inc.

R91 for UMA use 140 ohm for DIS use 150 ohm

140ohm CS11402FB19  
150ohm CS11502FB21



PART 3 OF 6

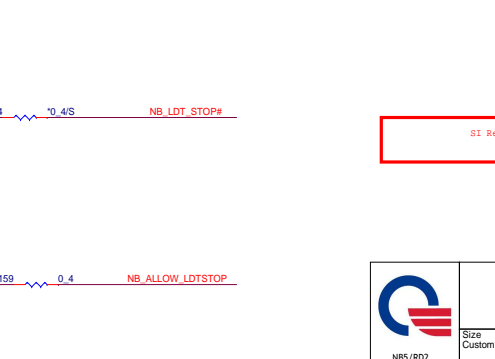
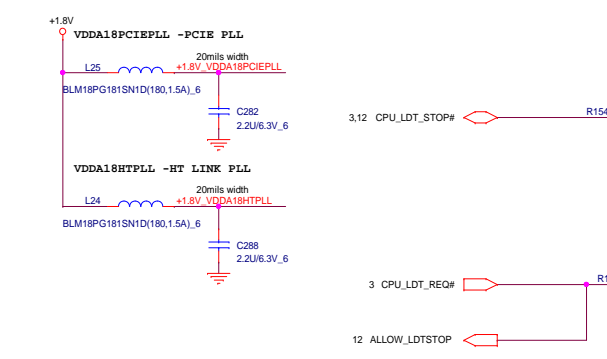
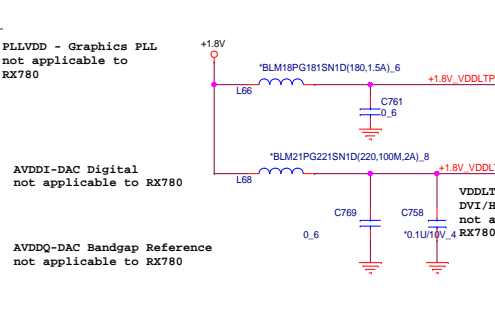
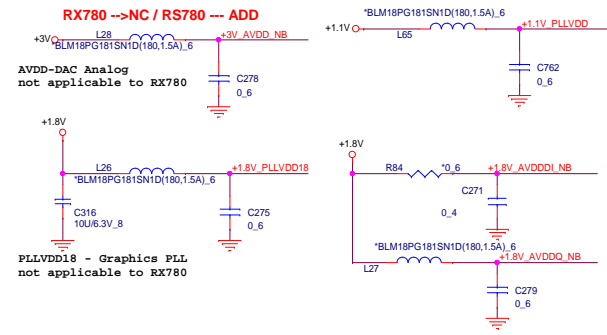
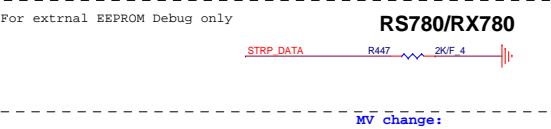
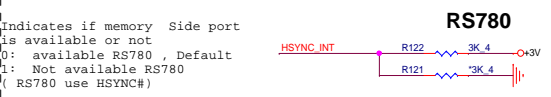
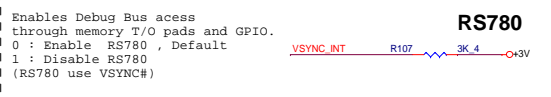
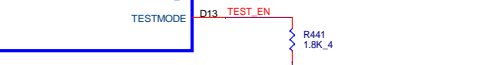
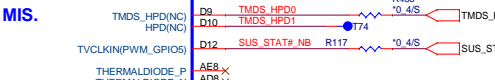
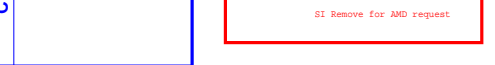
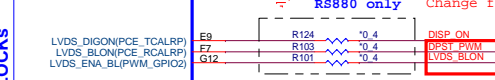
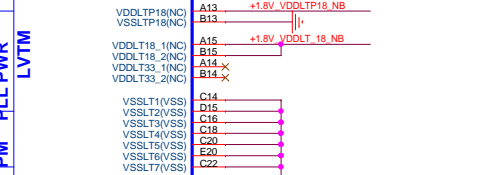
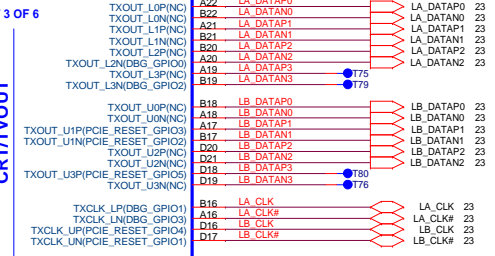
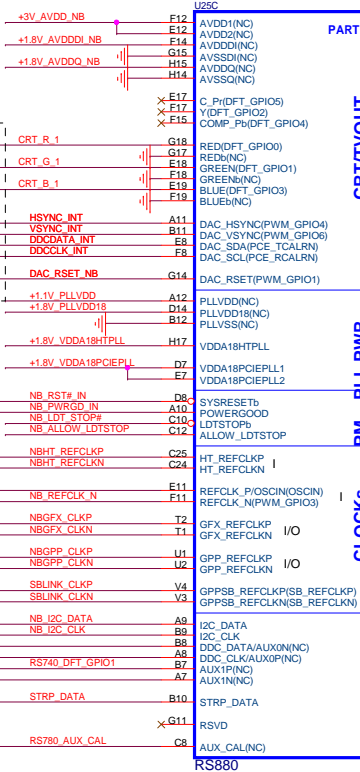
CRTRVOUT

PM PLL PWR

CLOCKS

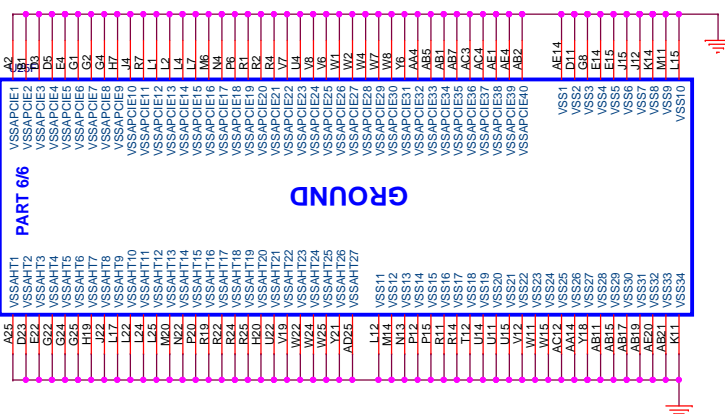
MIS.

TESTMODE



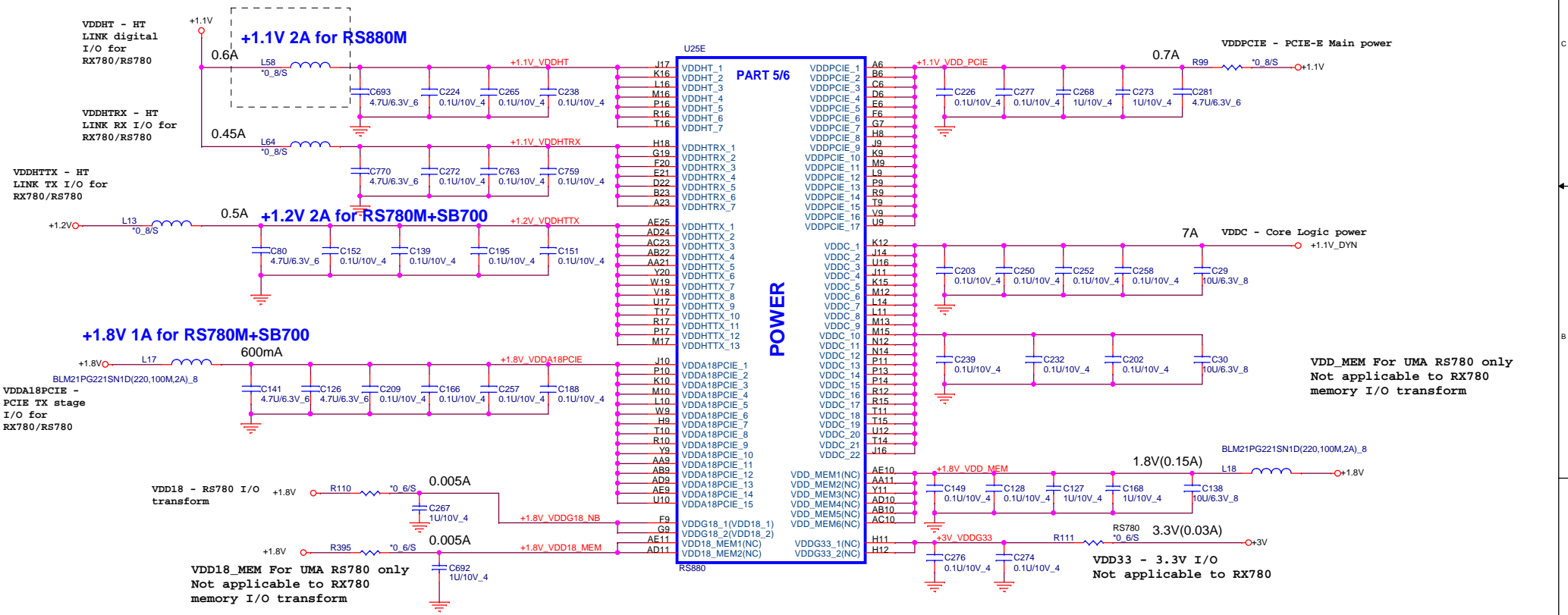
PROJECT : OP8  
Quanta Computer Inc.

Size Custom	Document Number RS740/RS780-SYSTEM I/F 3/5	Rev 1A
Date: Friday, March 20, 2009		



RX780/RS780 POWER DIFFERENCE TABLE

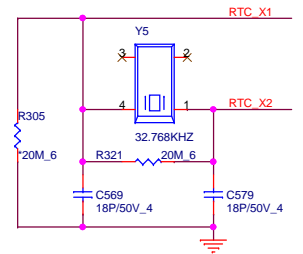
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC



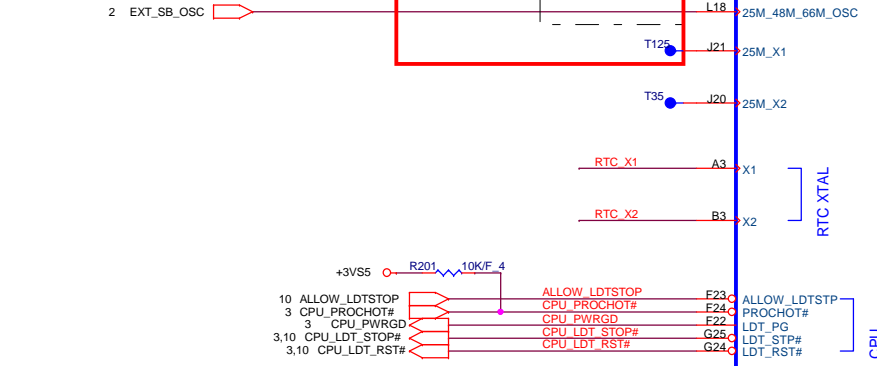
**PROJECT : OP8**  
Quantas Computer Inc.

PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U600

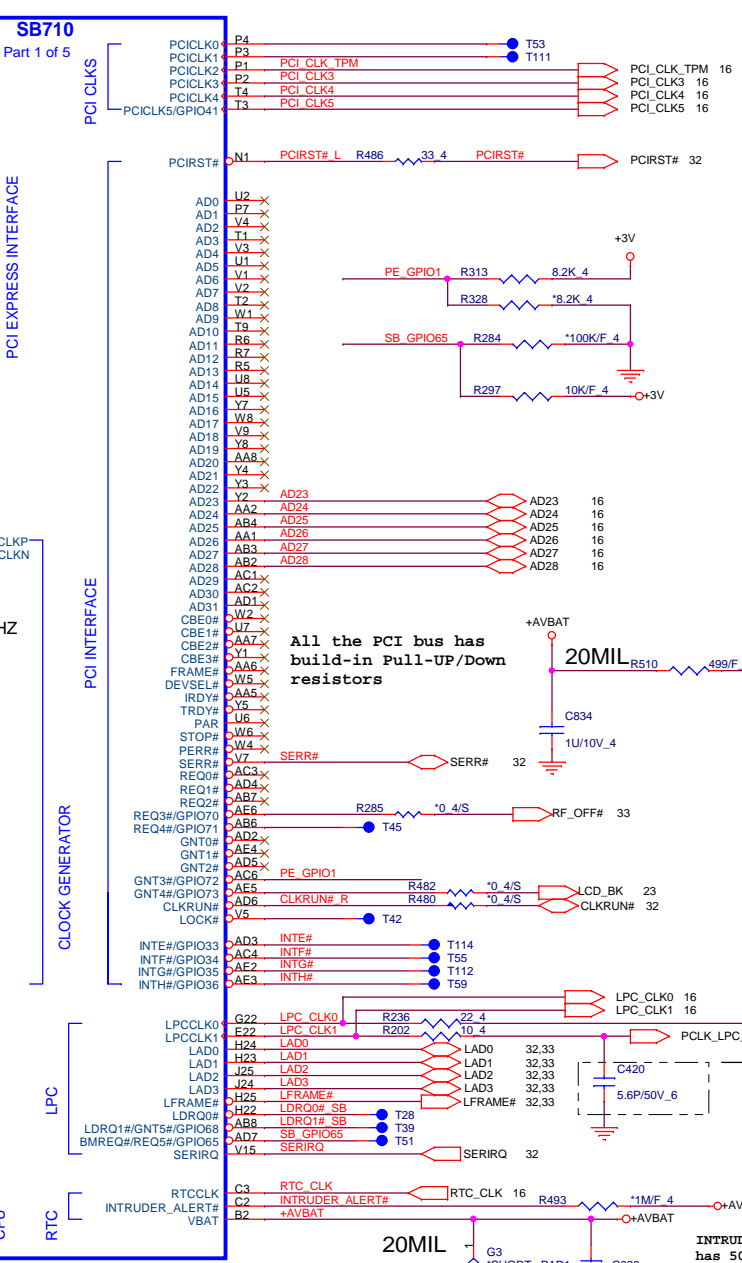
To RS780



Change for SB710 chip  
FOR A14 chip

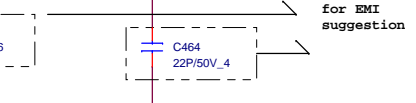


SB710  
IC CTRL(528P) SB710 A14(218-0660017)  
P/N : AJ066000T01



All the PCI bus has  
built-in Pull-UP/Down  
resistors

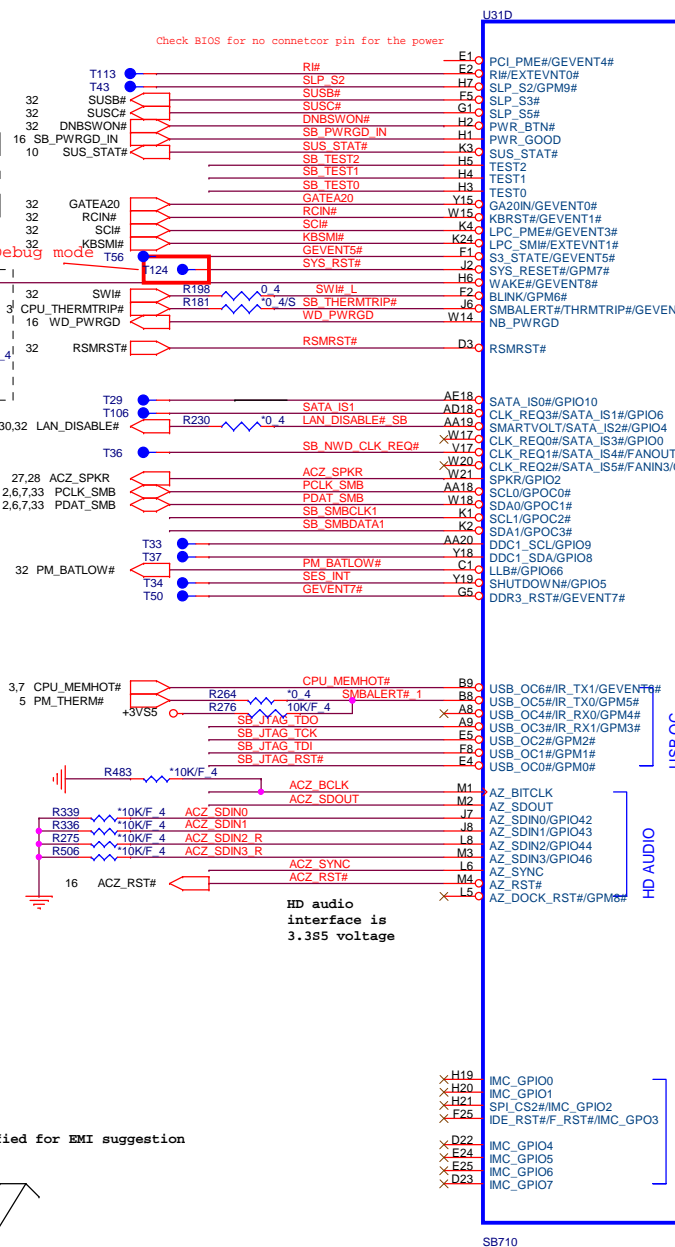
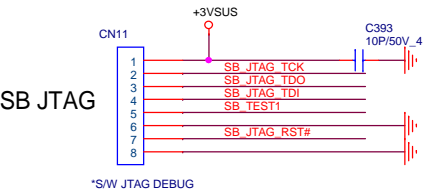
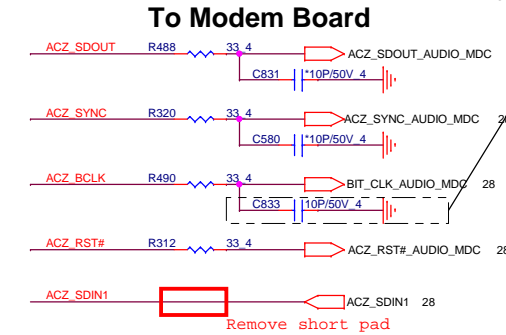
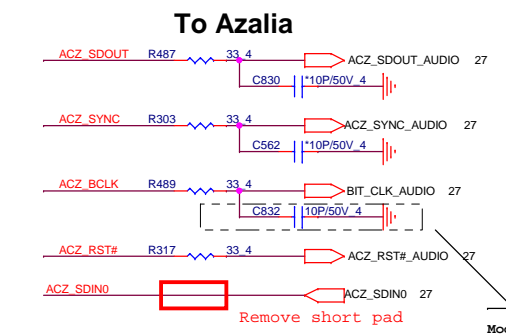
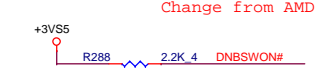
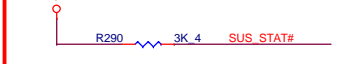
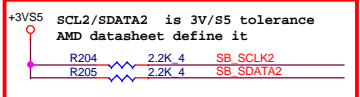
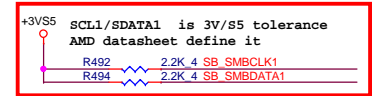
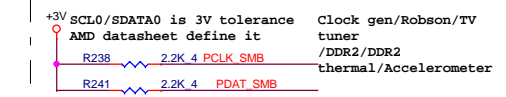
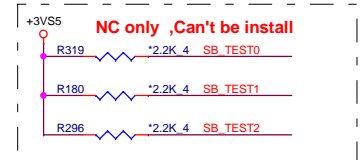
Change from  
0ohm to 1K  
for safety  
issue



INTRUDER\_ALERT# Left not connected (Southbridge  
has 50-kohm internal pull-up to VBAT).



PROJECT : OP8  
Quanta Computer Inc.



Check BIOS for no connector pin for the power

Change for test point for Debug mode

Change from AMD request

Modified for EMI suggestion

Remove short pad

Remove short pad

SB710 Part 4 of 5

for EMI

Si Change USB port reference Raven 2.0 design



**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>SB700-ACPI/GPIO/USB 2/4</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 13 of 42

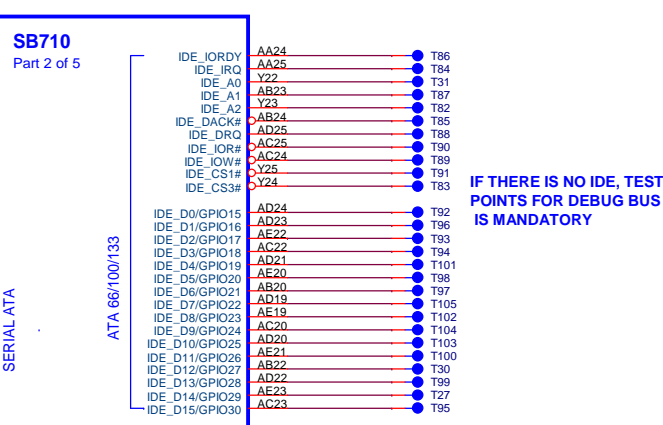
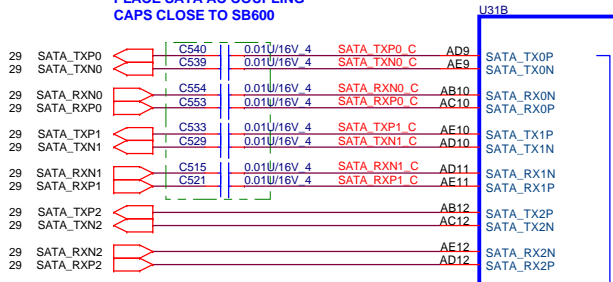
SATA PORT 0,1,2,3  
can support AHCI  
mode

PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600

SATA1

SATA ODD

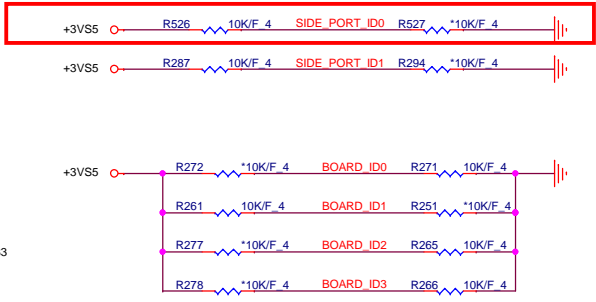
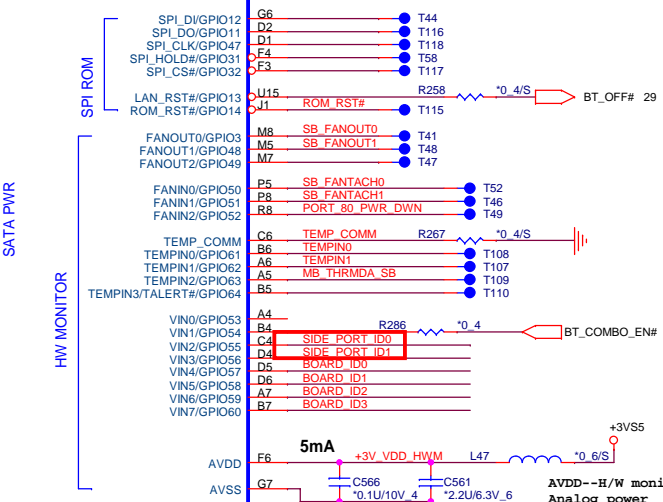
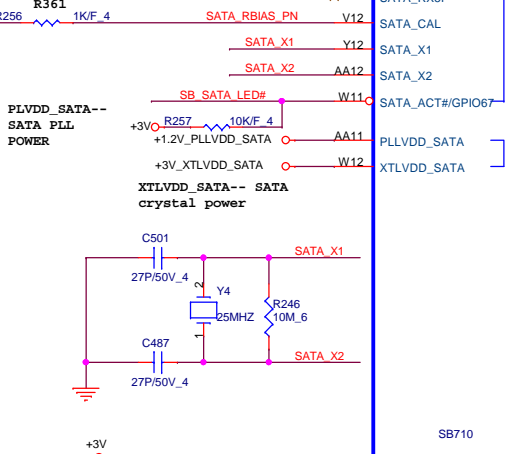
E-SATA



IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY

SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no support side port

**NOTE:**  
R361 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



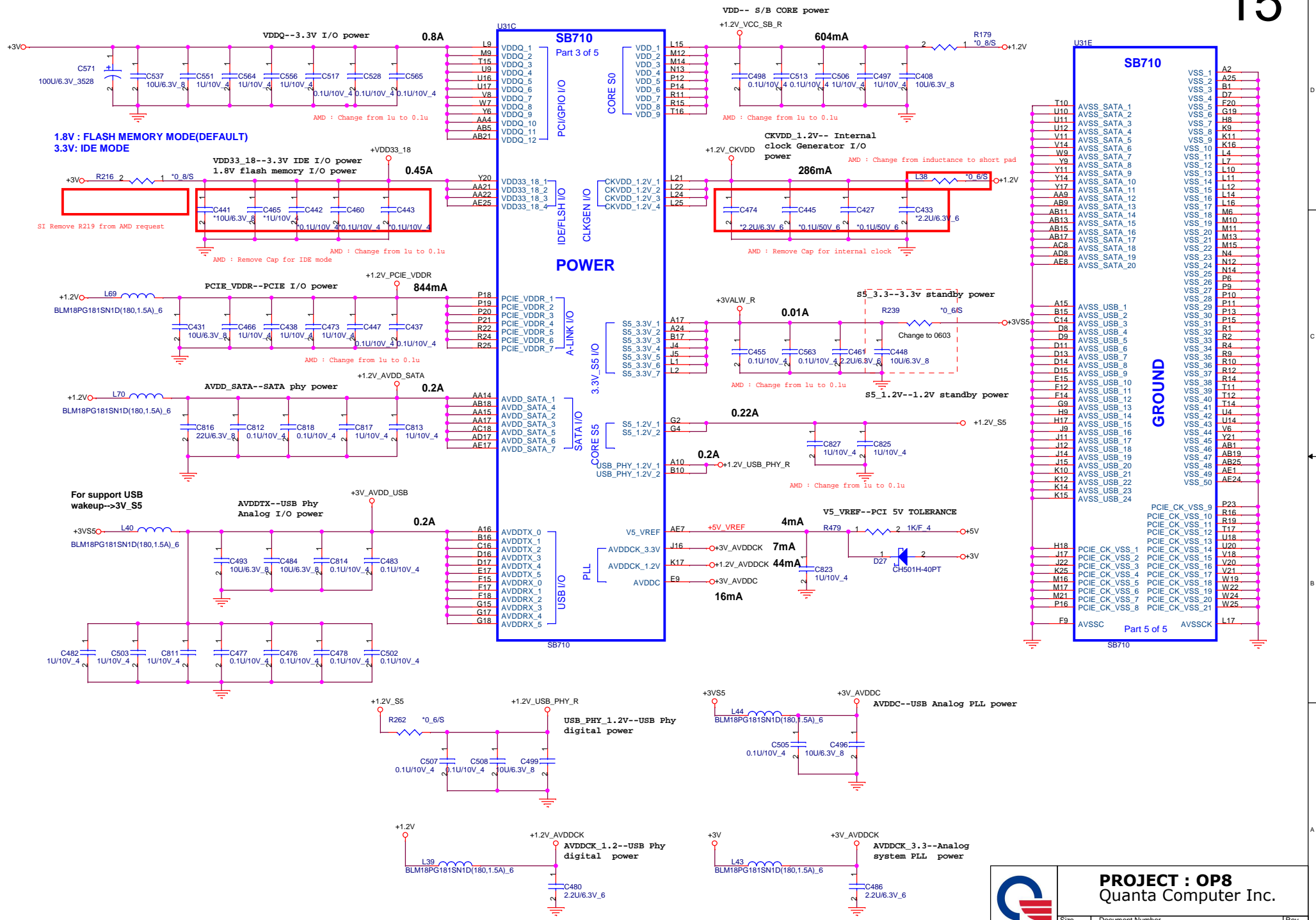
ID3	ID2	ID1	ID0	
0	0	0	0	OP8 UMA
0	0	0	1	OP9 UMA
0	0	1	0	OP8 Dis
0	0	1	1	OP9 Dis
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

Add for design



**PROJECT : OP8**  
Quanta Computer Inc.

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



**PROJECT : OP8**  
Quantas Computer Inc.

Size Custom	Document Number <b>SB700-PWR/DECOUPLING 4/4</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 15 of 42

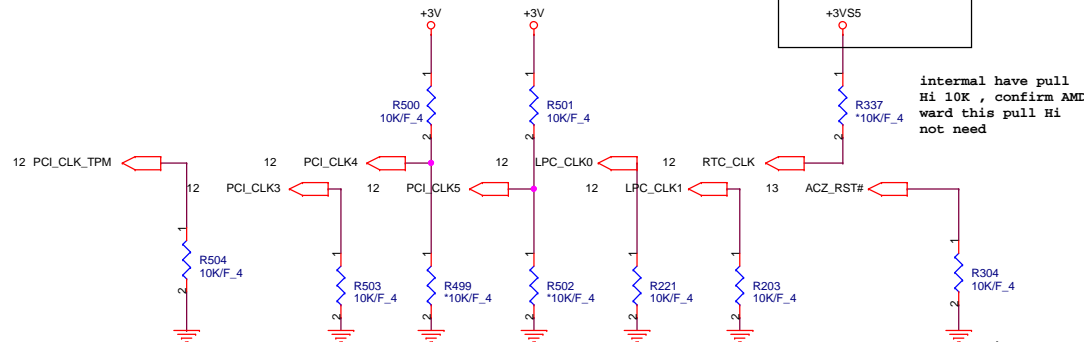
NB5/RD2



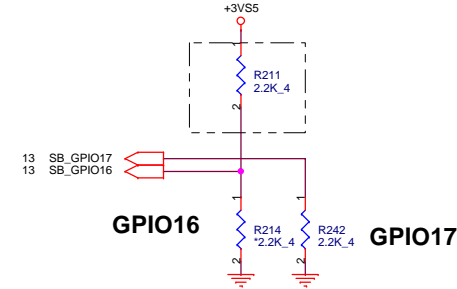
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

### REQUIRED STRAPS



internal have pull Hi 10K , confirm AMD ward this pull Hi not need

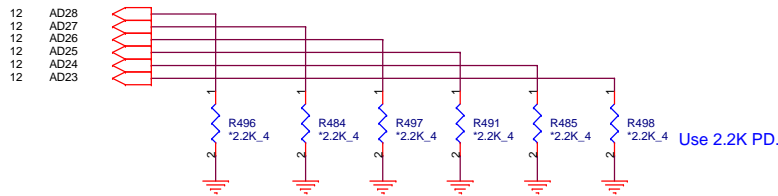


TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT

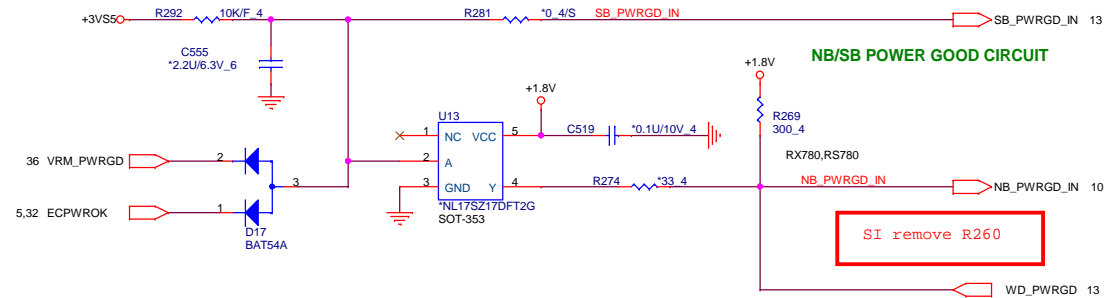
### DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB\_PWRGD\_IN: RS780/RX780 = 1.8V; RS740 = 3.3V Do NOT share it with SB\_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

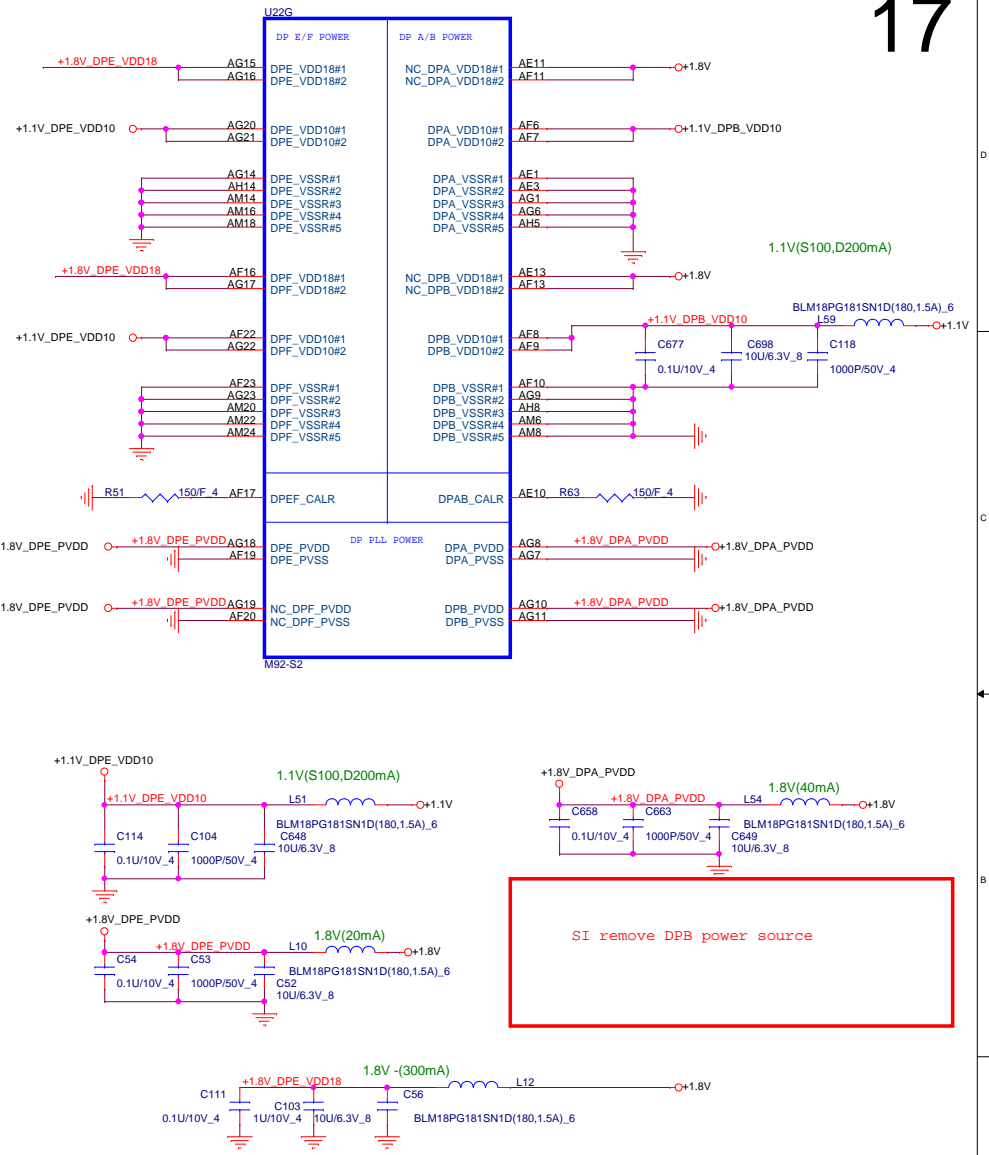
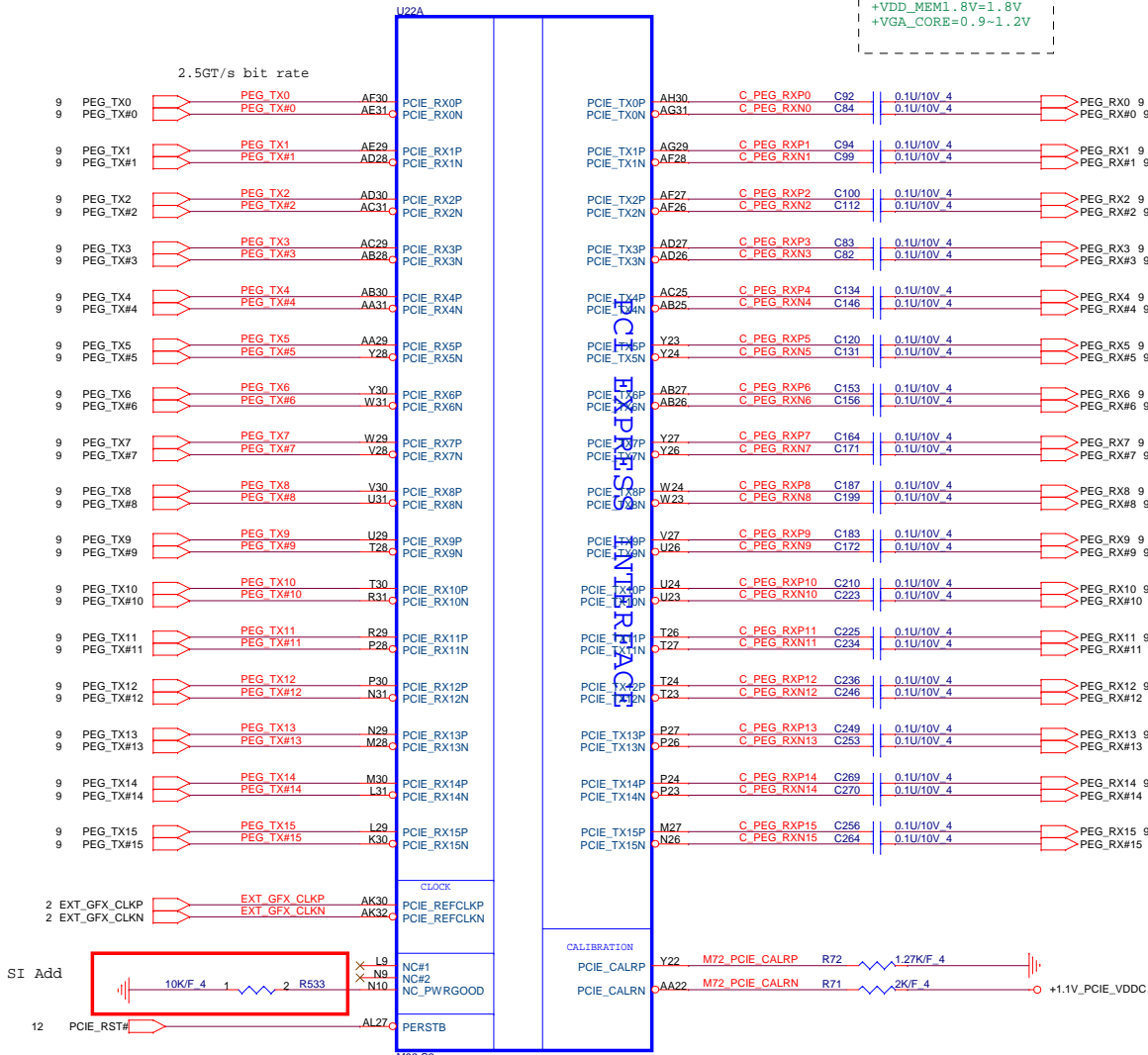


PROJECT : OP8  
Quanta Computer Inc.

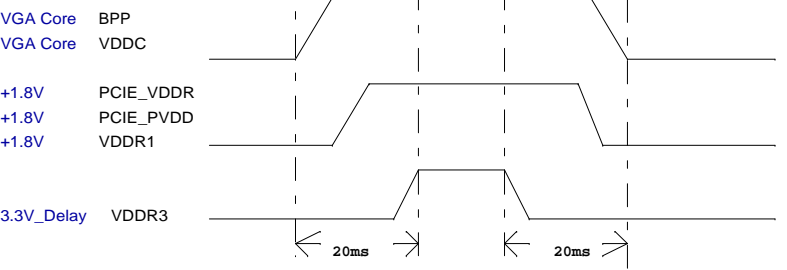
Size Custom Document Number SB700-STRAPS Rev 1A  
Date: Friday, March 20, 2009 Sheet 16 of 42



POWER  
 +PCIE\_VDDR=1.2V  
 +VDD\_MEM1.8V=1.8V  
 +VGA\_CORE=0.9-1.2V

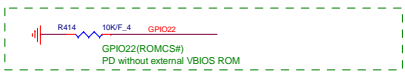


100MHz (+/-300ppm) input frequency,  
 0-0.7V single-ended swing



**PROJECT : OP8**  
 Quanta Computer Inc.

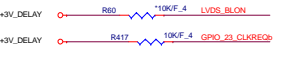
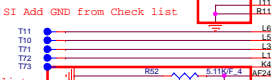
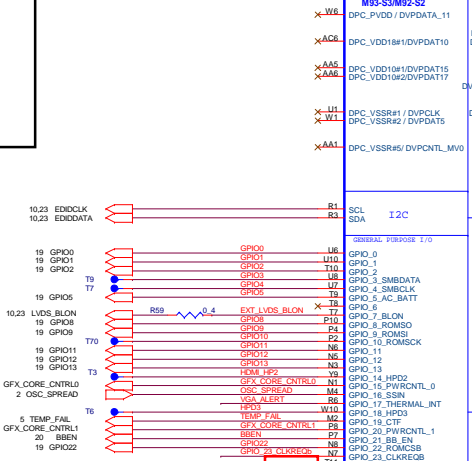
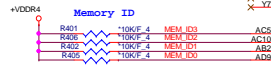
Size Custom Document Number M7X/M8X\_PCIE\_Interface Rev 1A  
 NBS/RD2 Date: Friday, March 20, 2009 Sheet 17 of 42



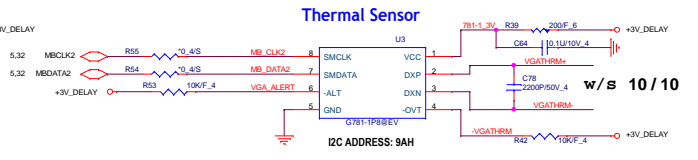
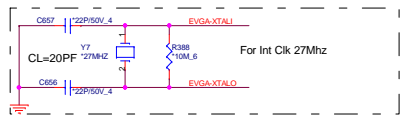
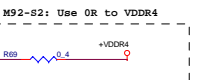
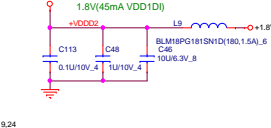
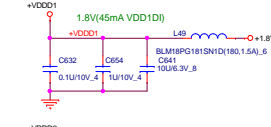
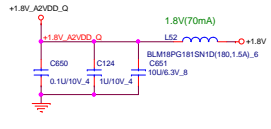
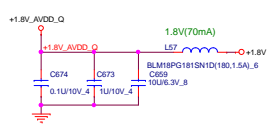
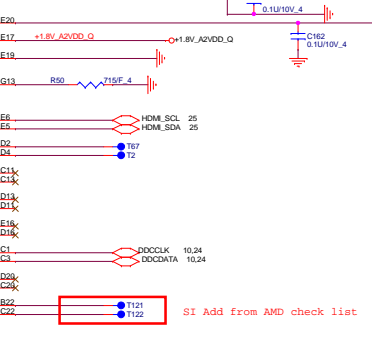
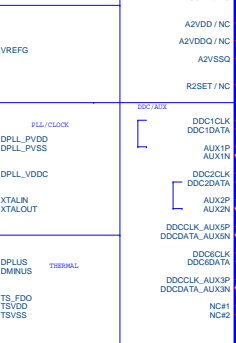
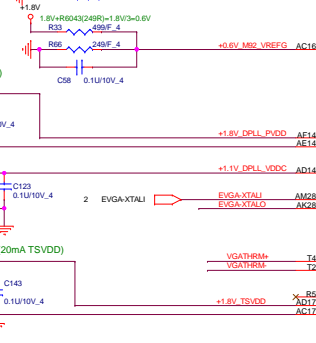
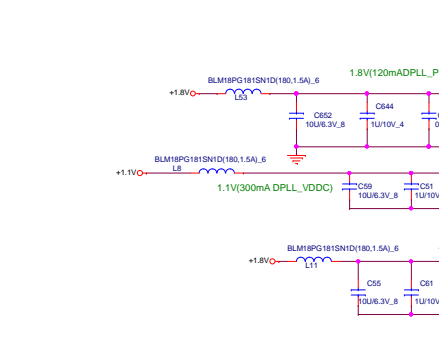
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix	4*16-500MHZ	HP16G135RW-20L
0001	Samsung (E die)	4*16-500MHZ	K9NIG164QE-HC20
0010	Qimonda (Infineon)	4*16-500MHZ	TD
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

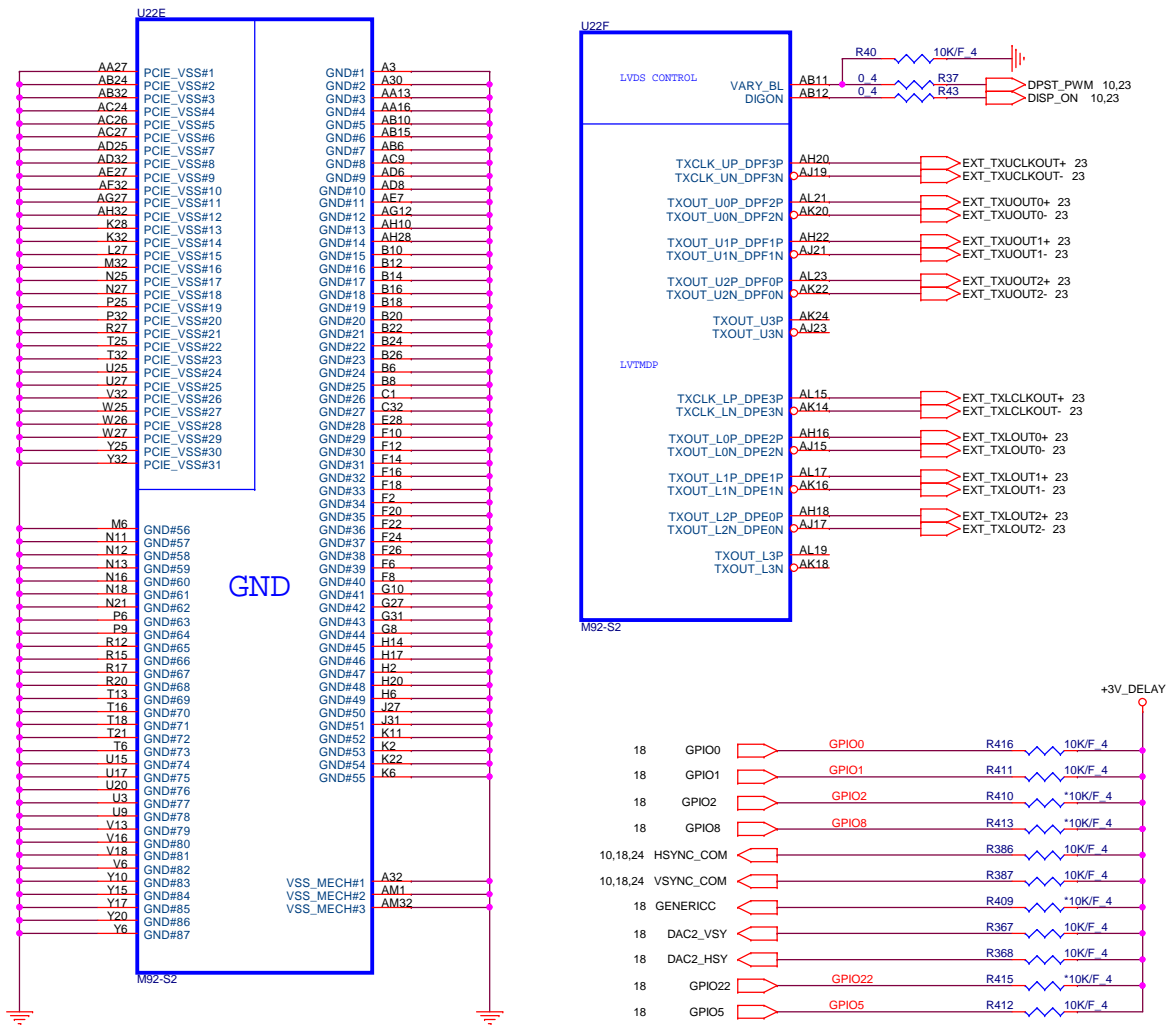
	BBEN	BBP
L	0	V-CORE
H	1	+1.8V



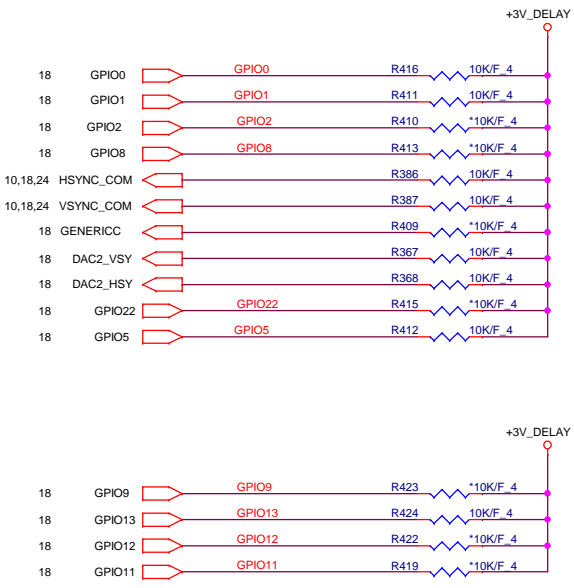
SI Add GND from Check list



SI Add from AMD check list



Strap Name	Pin Straps description	Default Value
<b>TX_PWRS_ENB</b>	<b>GPIO0</b> Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	<b>1</b>
<b>TX_DEEMPH_EN</b>	<b>GPIO1</b> PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	<b>1</b>
<b>BIF_GEN2_EN</b>	<b>GPIO2</b> 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	<b>0</b>
<b>STRAP_BIF_CLK_PM_EN</b>	<b>GPIO8</b> Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	<b>0</b>
<b>BIOS_ROM_EN</b>	<b>GPIO22</b> Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	<b>0</b>
<b>AUDIO[0]</b>	<b>VSYN</b>	<b>1</b>
<b>AUD(1)</b>	<b>HSYN</b> HSYN - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	<b>1</b>
<b>VIP_DEVICE_STRAP_DIS</b>	<b>DAC2_VSY</b> If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	<b>0</b>
<b>SMS_EN_HARD</b>	<b>DAC2_HSY</b>	<b>0</b>
<b>CCBYPASS</b>	<b>GENERICC</b>	<b>0</b>



### Memory Aperture size

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
<b>0</b>	<b>128M</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>256M</b>	<b>0</b>	<b>0</b>	<b>1</b>
<b>0</b>	<b>64M</b>	<b>0</b>	<b>1</b>	<b>0</b>
<b>0</b>	<b>32M</b>	<b>0</b>	<b>1</b>	<b>1</b>
<b>0</b>	<b>512M</b>	<b>1</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>1G</b>	<b>1</b>	<b>0</b>	<b>1</b>
<b>0</b>	<b>2G</b>	<b>1</b>	<b>1</b>	<b>0</b>
<b>0</b>	<b>4G</b>	<b>1</b>	<b>1</b>	<b>1</b>

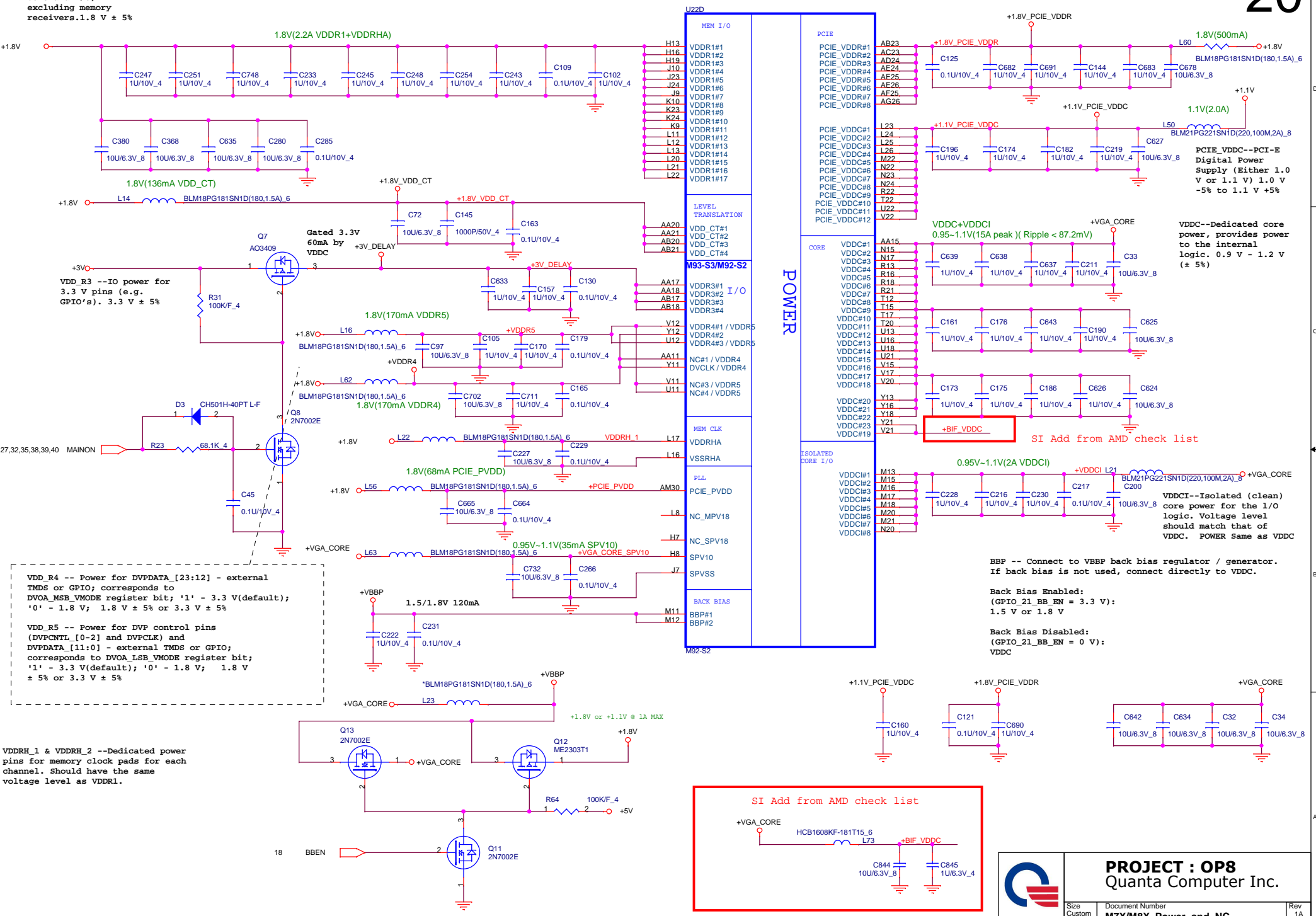
It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>M7X/M8X_GND / LVDS/ Straps</b>	Rev 1A
NB5/RD2	Date: Friday, March 20, 2009	Sheet 19 of 42

VDD\_CT -- Level translation between core and I/O, excluding memory receivers. 1.8 V ± 5%

PCIE\_VDDR--PCI-E I/O power. 1.8 V ± 5%



**VDD\_R4 -- Power for DVPDATA\_[23:12] - external TMS or GPIO; corresponds to DVOA\_MSB\_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%**

**VDD\_R5 -- Power for DVP control pins (DVPCNTL\_[0-2] and DVPCLK) and DVPDATA\_[11:0] - external TMS or GPIO; corresponds to DVOA\_LSB\_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%**

**VDDRH\_1 & VDDRH\_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.**

**PCIE\_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%**

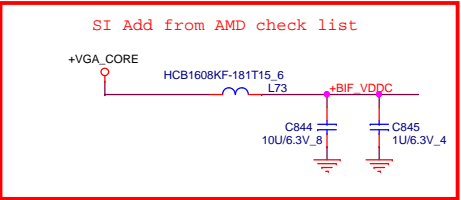
**VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)**

**VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC**

**BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.**

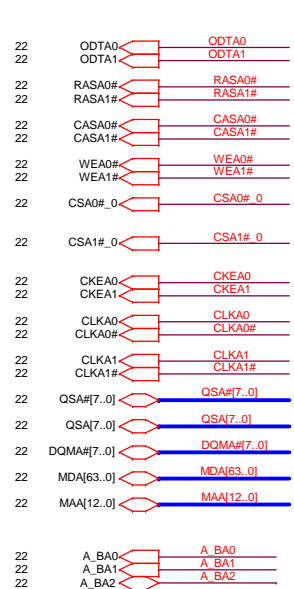
**Back Bias Enabled:**  
(GPIO\_21\_BB\_EN = 3.3 V):  
1.5 V or 1.8 V

**Back Bias Disabled:**  
(GPIO\_21\_BB\_EN = 0 V):  
VDDC

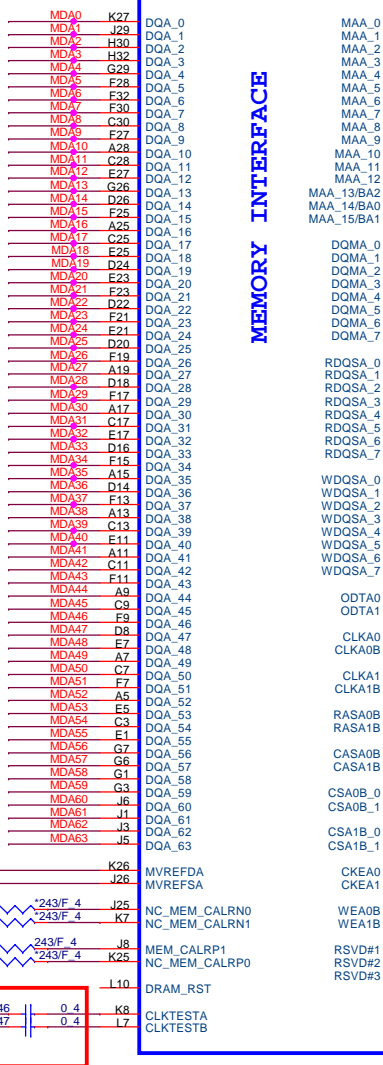


**PROJECT : OP8**  
Quanta Computer Inc.

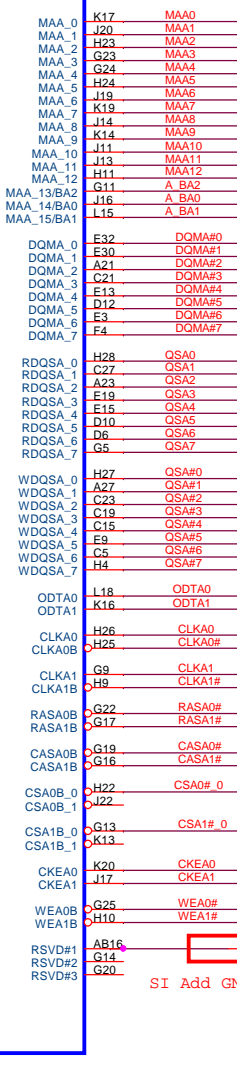
Size Custom	Document Number M7X/M8X_Power_and_NC	Rev 1A
Date: Friday, March 20, 2009		Sheet 20 of 42



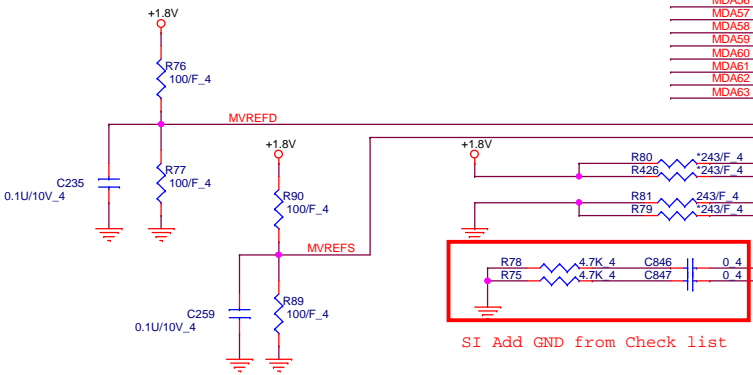
support 1Gbit  
VRAM ( 64M X 16 )



MEMORY INTERFACE



SI Add GND from Check list



SI Add GND from Check list

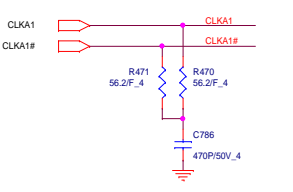
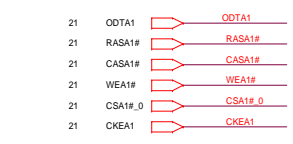
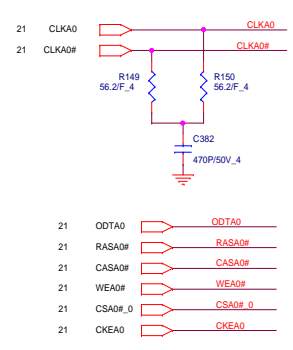
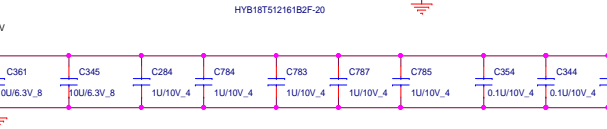
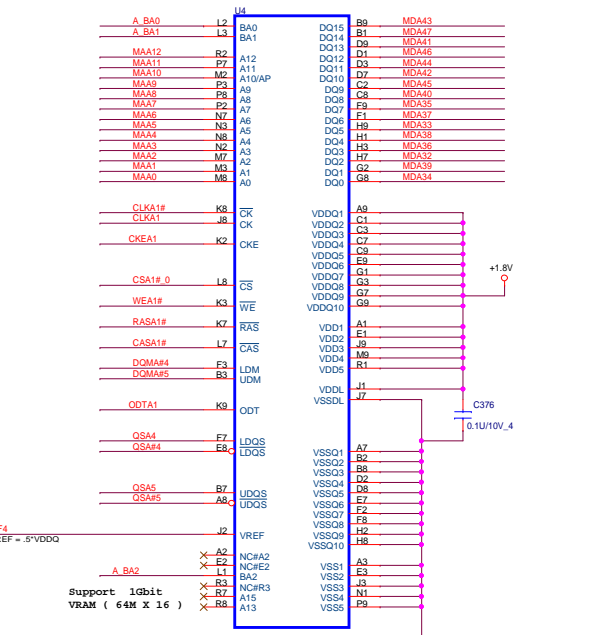
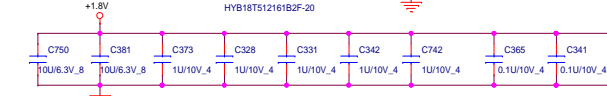
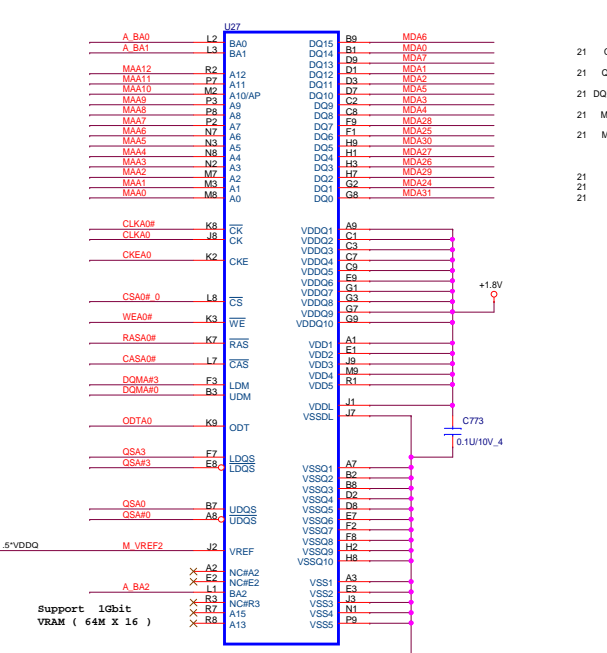
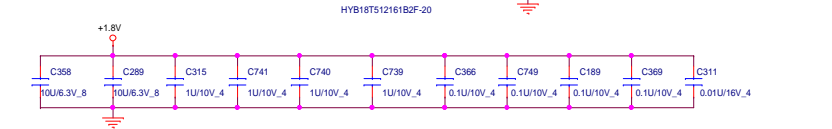
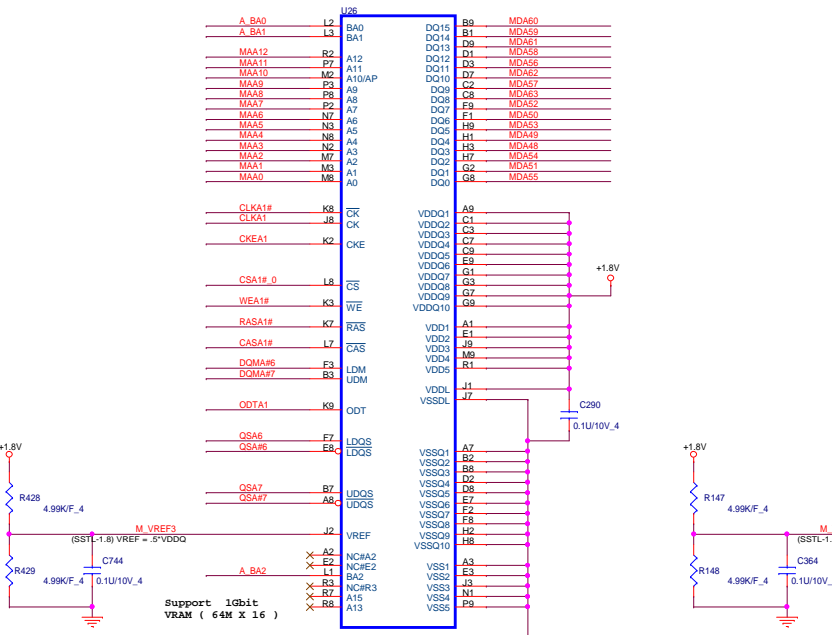
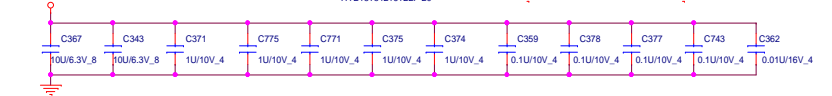
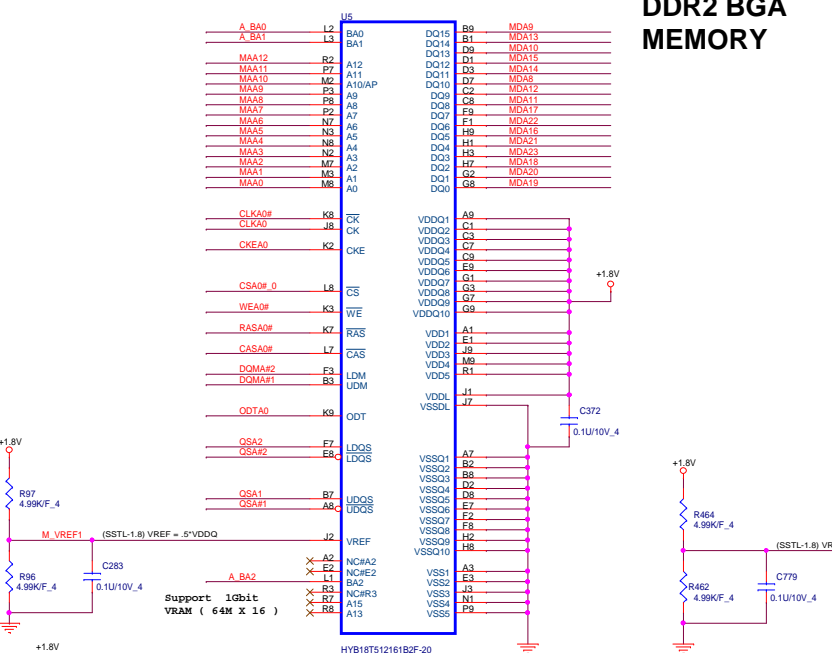
Change MEMTEST to 240 1% ohm to GND , AMD update



**PROJECT : OP8**  
Quantas Computer Inc.

Size Custom	Document Number <b>M7X/M8X/MEM_Interface</b>	Rev 1A
Date: Friday, March 20, 2009	Sheet 21 of 42	

# DDR2 BGA MEMORY

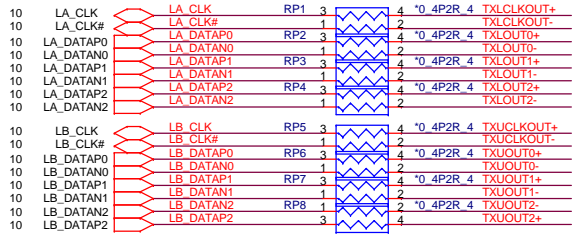


DDR2 BGA MEMORY

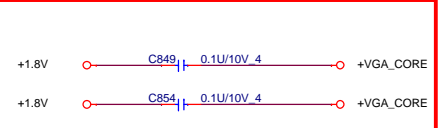
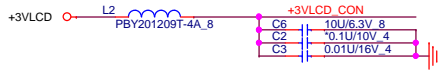
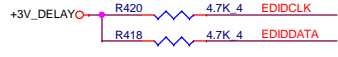
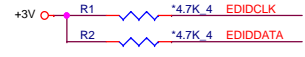
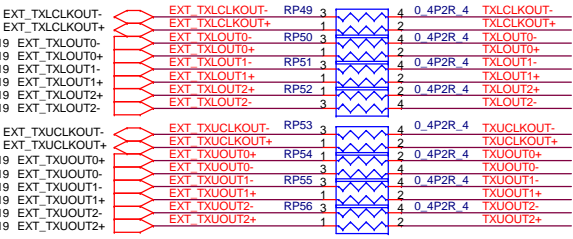
	<b>PROJECT : OP8</b>		Rev 1A
	Quanta Computer Inc.		
Size C	Document Number		
	<b>M92/VRAM_A0,A1</b>		
Date: Friday, March 20, 2009	Sheet 22	of 42	

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

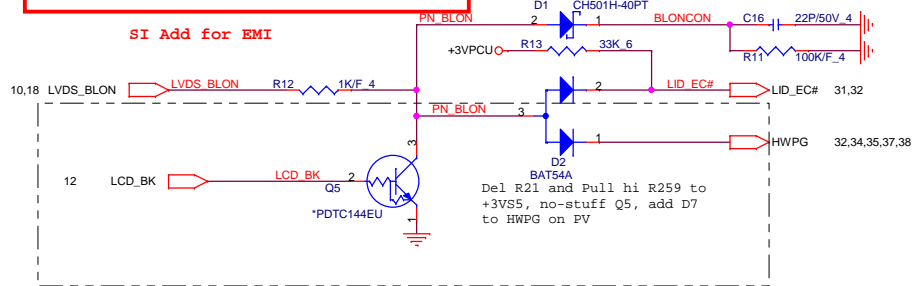
**OPTION SIGNAL FROM NB to LVDS for UMA**



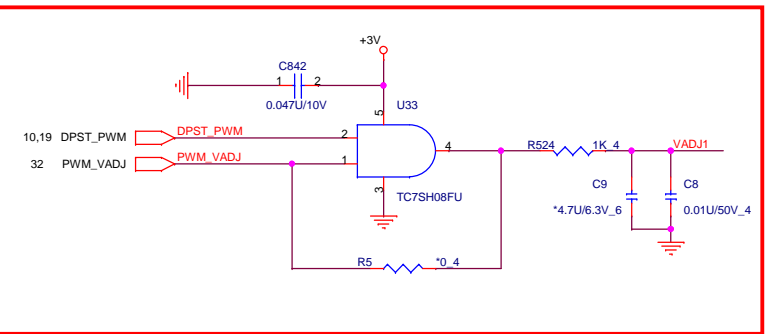
**OPTION SIGNAL FROM M92 to LVDS for discrete**



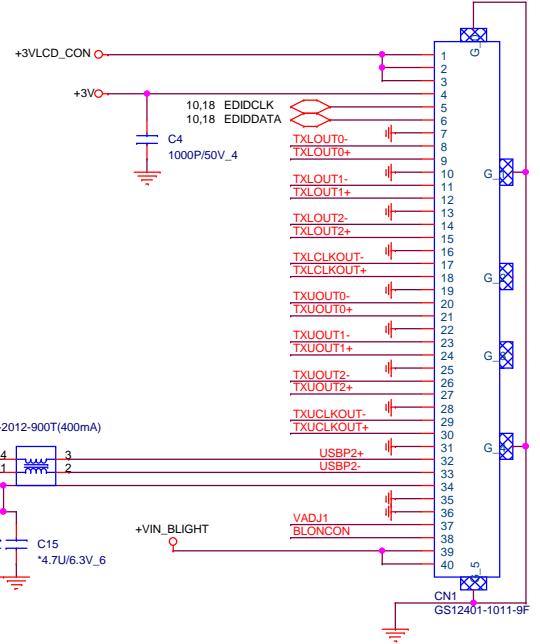
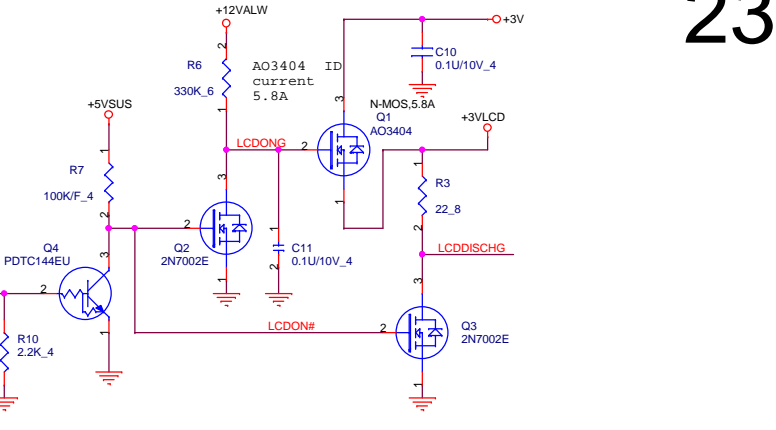
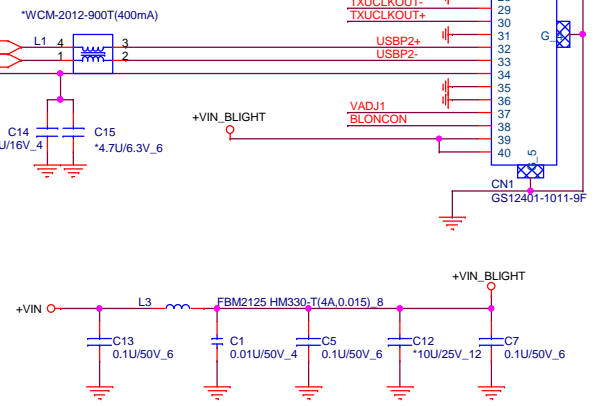
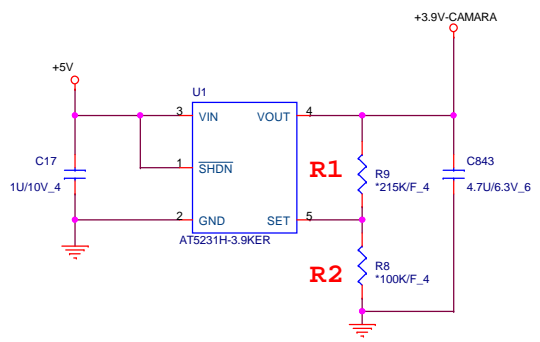
SI Add for EMI



Del R21 and Pull hi R259 to +3VS5, no-stuff Q5, add D7 to HWPG on PV



SI add U33,R524,C842 for Vari bright function

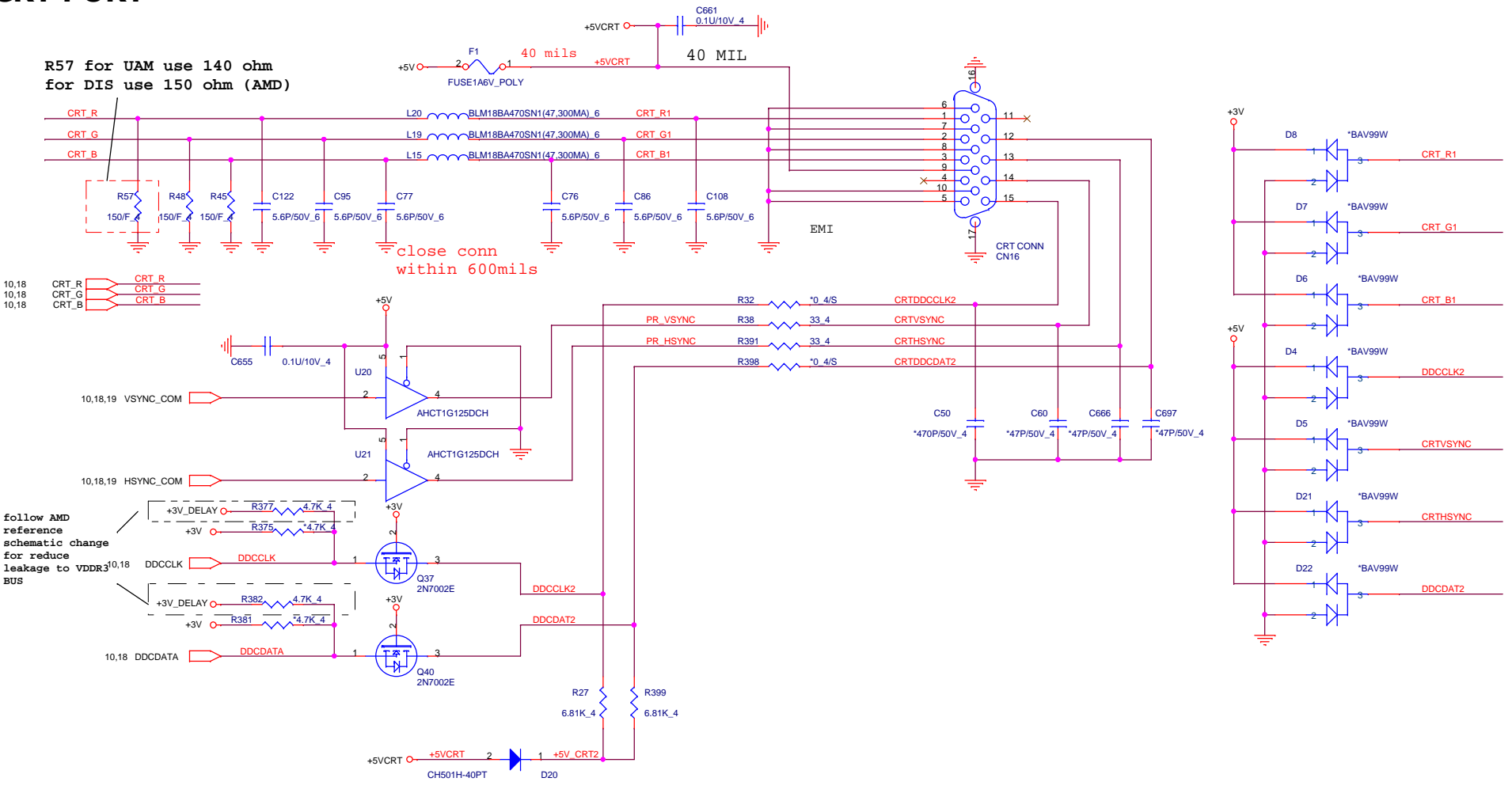


**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>LCD CONN</b>	Rev 1A
Date: Friday, March 20, 2009	Sheet 23 of 42	

CRT PORT

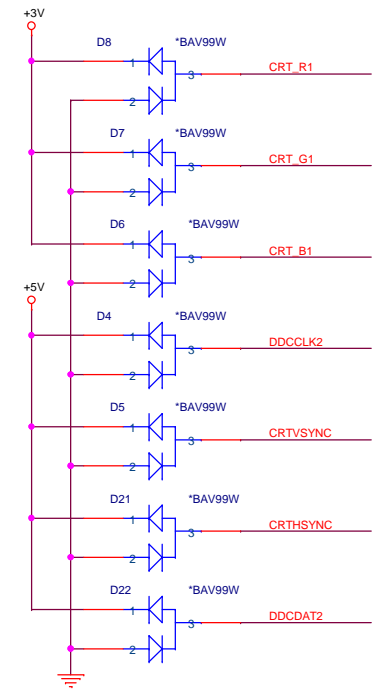
R57 for UAM use 140 ohm  
for DIS use 150 ohm (AMD)



close conn  
within 600mils



follow AMD  
reference  
schematic change  
for reduce  
leakage to VDDR3  
BUS



**PROJECT : OP8**  
Quantas Computer Inc.

Size Custom	Document Number <b>CRT</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 24 of 42

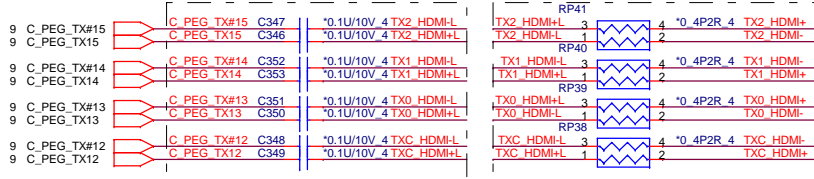


**UMA/DISCRETE select for HDMI**

**From RS780M**

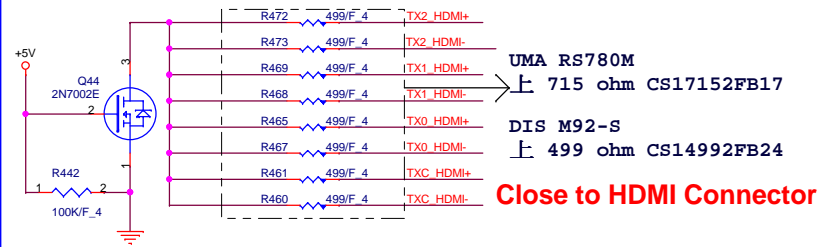
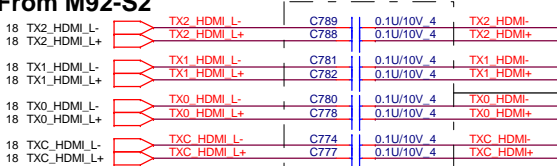
for Layout concern  
,placement close  
north bridge

for Layout concern  
,placement close  
HDMI conn

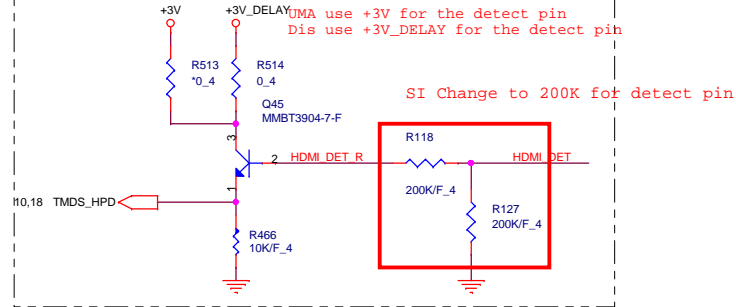


**From M92-S2**

for Layout concern  
,placement close  
HDMI conn

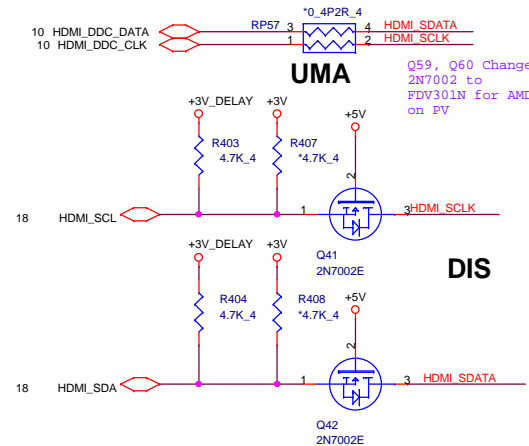


**HDMI HPD SENSE**

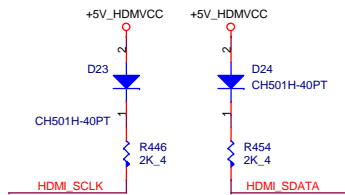
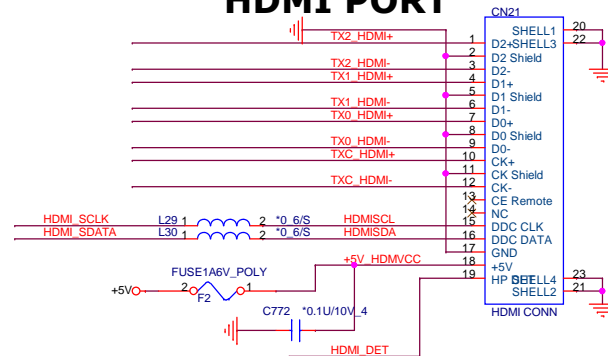


**UMA AND DISCRETE HDMI I2C SELECT**

**Close to HDMI Connector**

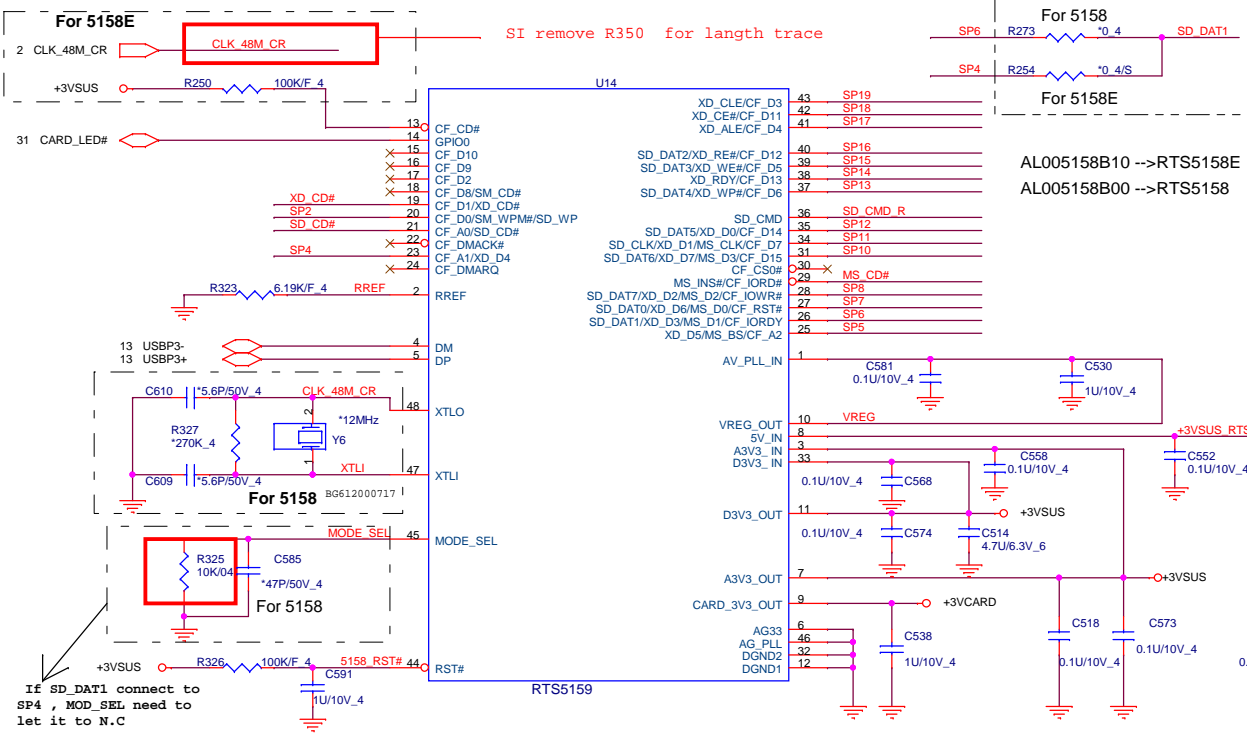


**HDMI PORT**



**PROJECT : OP8**  
Quanta Computer Inc.

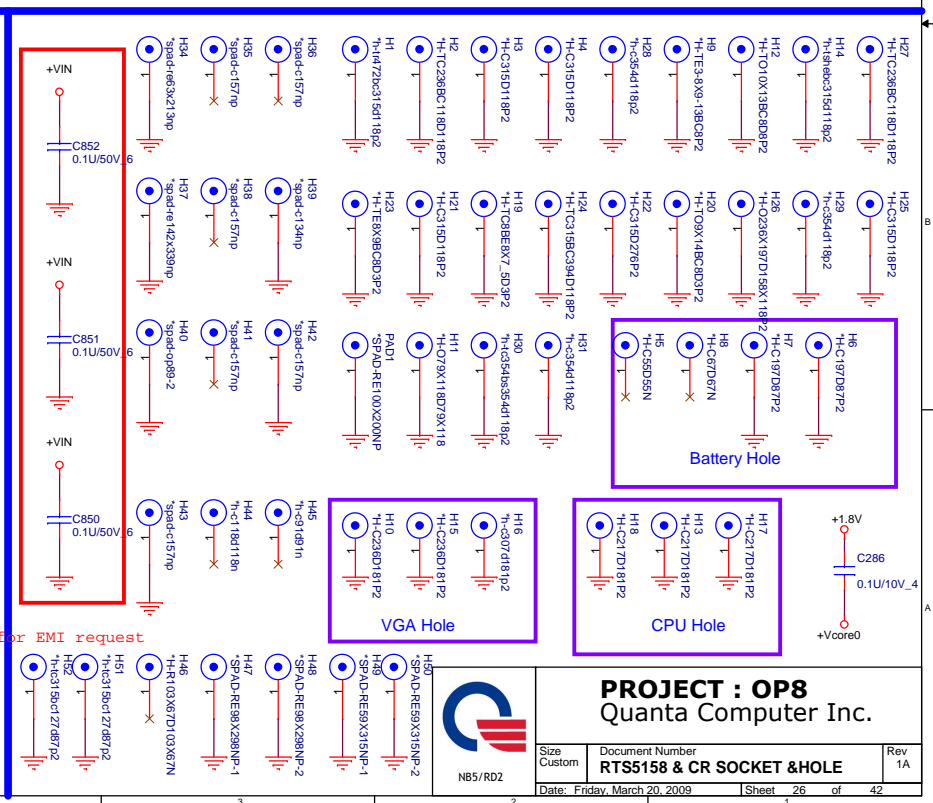
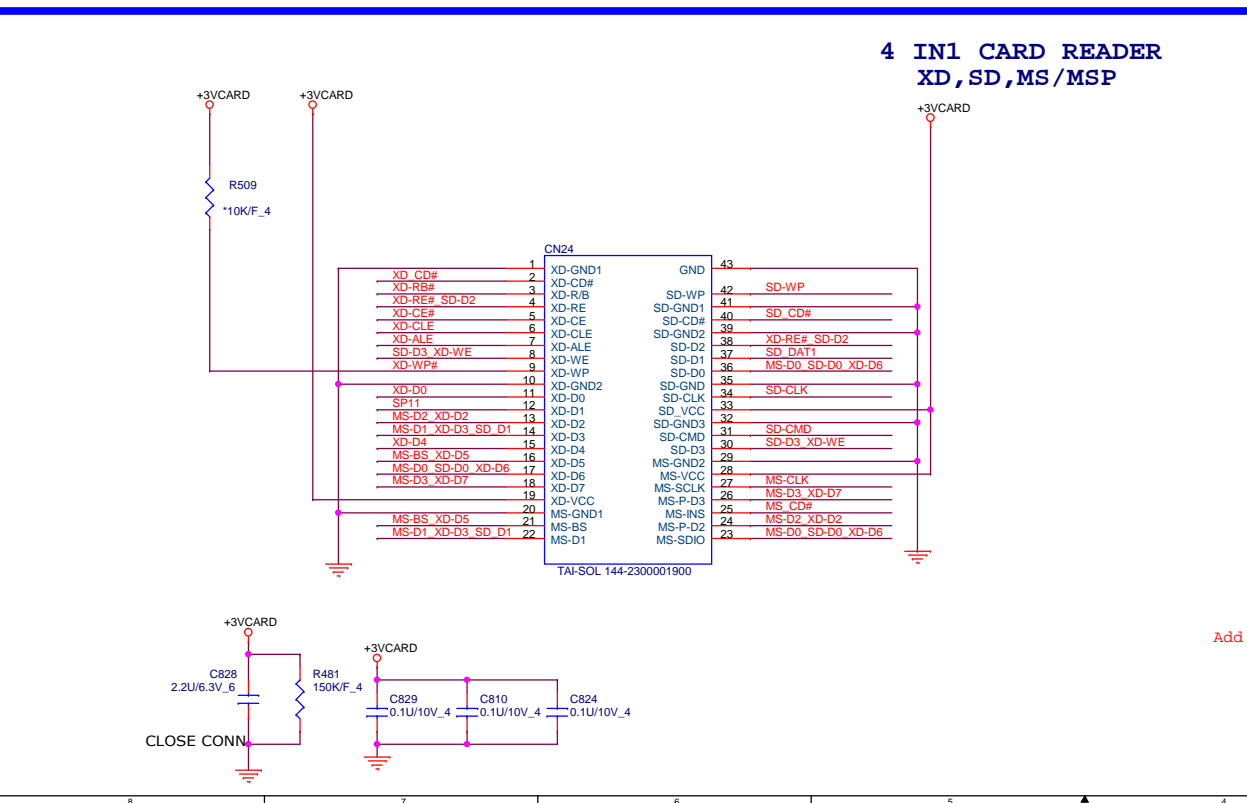
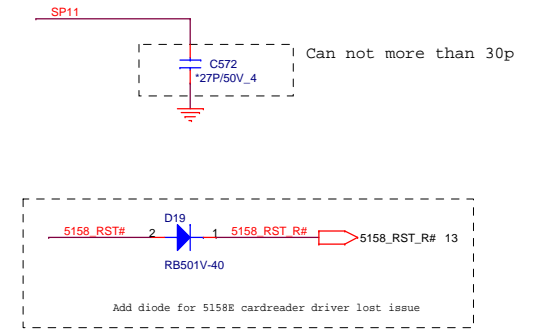
Size Custom	Document Number <b>HDMI</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 25 of 42

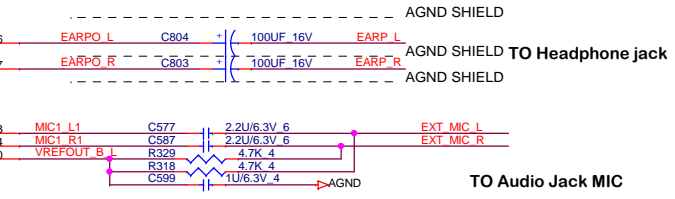
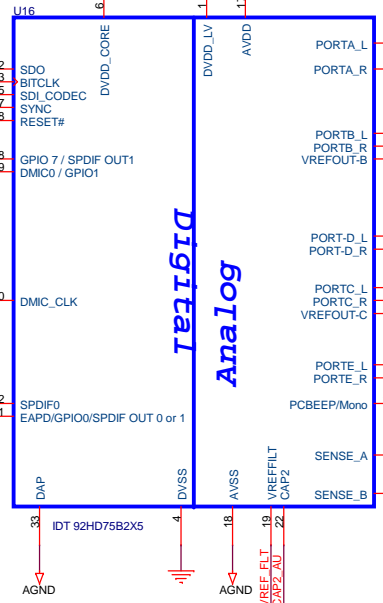
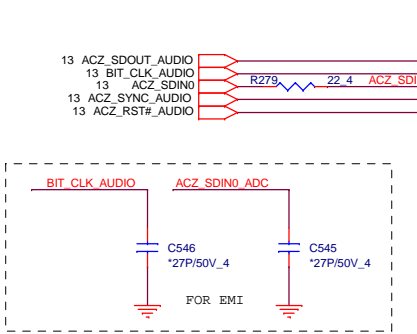
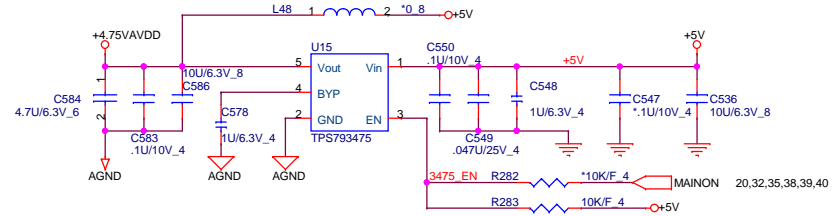
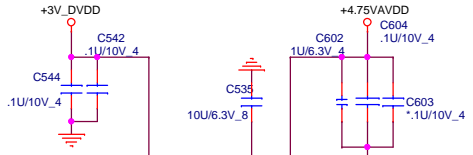
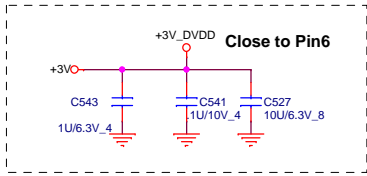


**Note:**

SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD_D4
SP5	MS_BS	XD_D5
SP6	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9	MS_INS#	XD_D2
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD_D1
SP13	SD_DAT4	XD_WP#
SP14		XD_R/#
SP15	SD_DAT3	XD_WE#
SP16	SD_DAT2	XD_RE#
SP17		XD_ALE
SP18		XD_CE#
SP19		XD_CLE

SP7	R280	*0.4/S	MS-D0	SD-D0	XD-D6
SP8	R268	*0.4/S	MS-D1	XD-D3	SD-D1
SP6	R252	*0.4/S	MS-D2	XD-D2	
SP16	R343	*0.4/S	XD-RE#	SD-D2	
SP6	R258	*0.4/S	MS-BS	XD-D5	
SP15	R342	*0.4/S	SD-D3	XD-WE	
SP11	R314	*0.4/S	SD-CLK		
SP2	R523	*0.4/S	MS-CLK		
SP3	R255	*0.4/S	SD_WP		
SP19	R345	*0.4/S	XD_WP#		
SP4	R253	*0.4/S	XD-D4		
SP10	R291	*0.4/S	MS-D3	XD-D7	
SP14	R353	*0.4/S	XD-R/#		
SP12	R322	*0.4/S	XD-D0		
SP17	R354	*0.4/S	XD-ALE		
SP18	R344	*0.4/S	XD-CE#		
SD_CMD_R	R331	*0.4/S	SD-CMD		



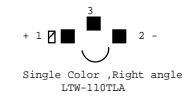
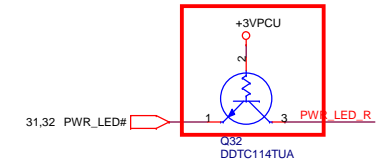
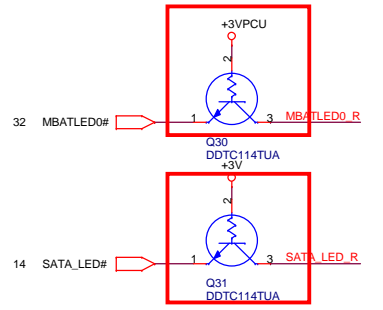
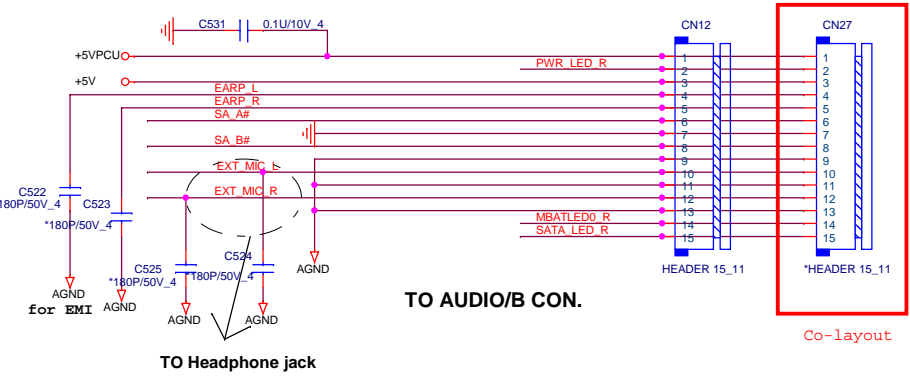
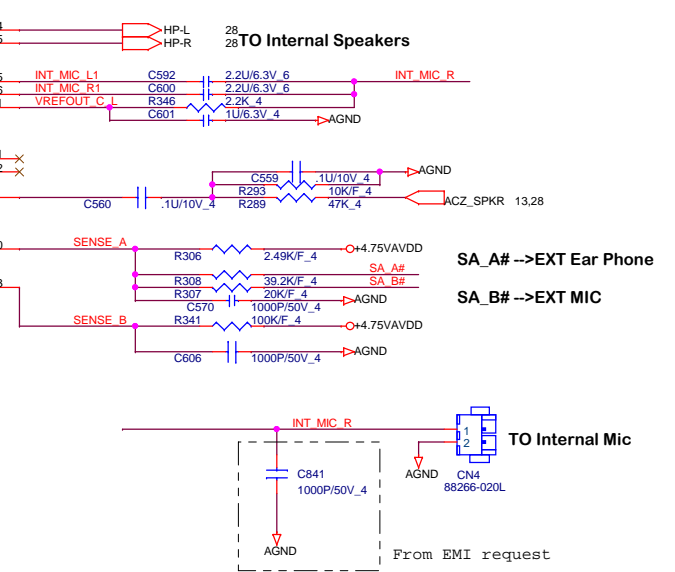
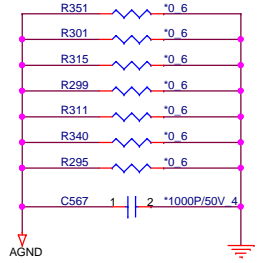


**Audio JACK: Normal Open**

SA\_A# -->EXT HP

SA\_B# -->EXT MIC

Sense\_B -->INT MIC



**PROJECT : OP8**  
Quanta Computer Inc.

NB5/RD2

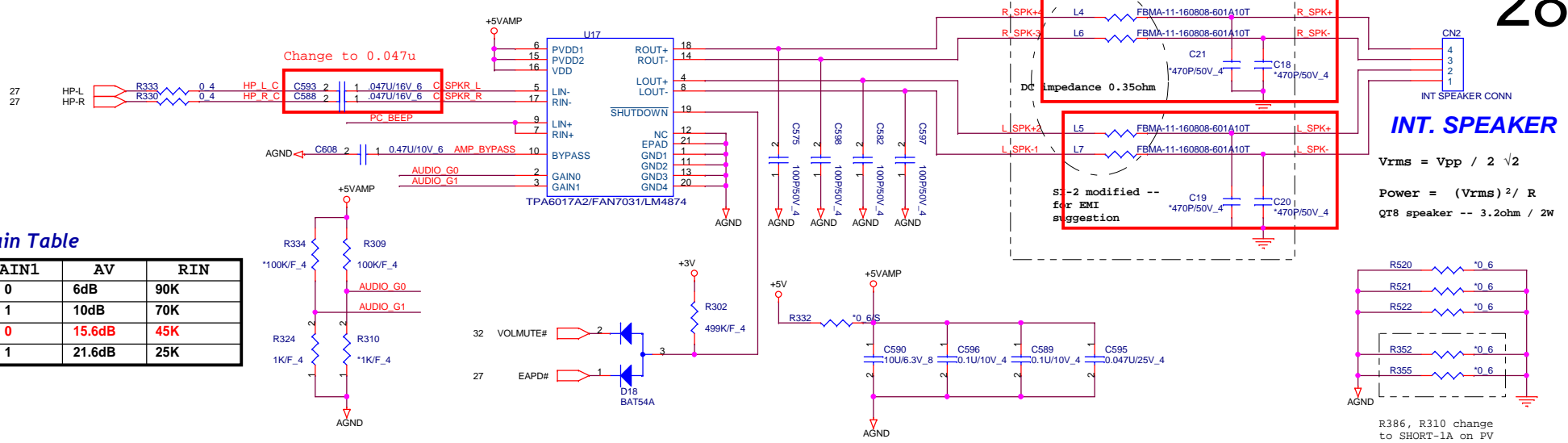
Size Custom

Document Number **Azalia 92HD75B2X5**

Date: Friday, March 20, 2009

Rev 1A

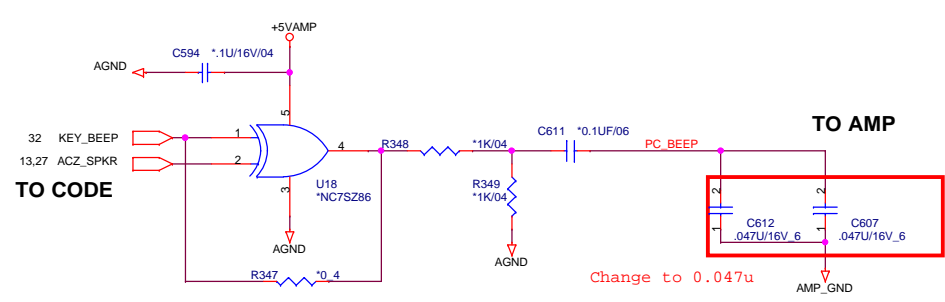
Sheet 27 of 42



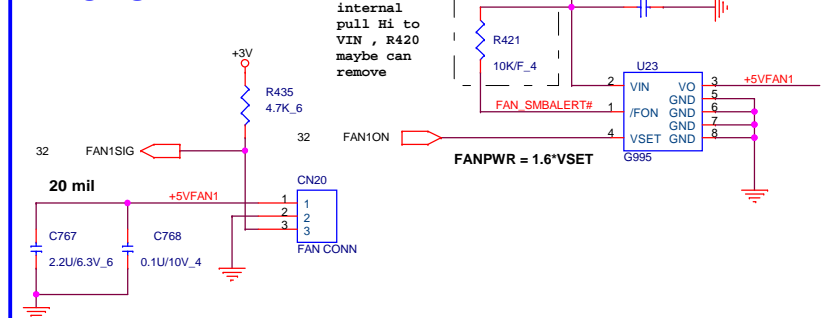
6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

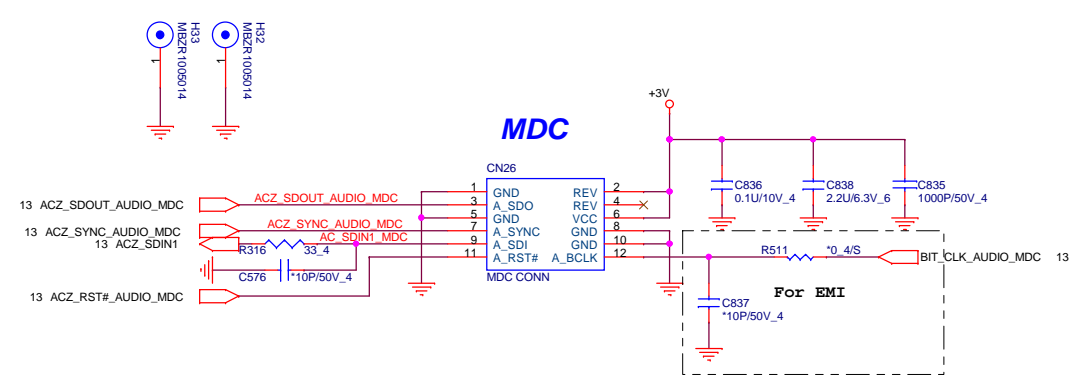
## PC-BEEP



## CPU FAN

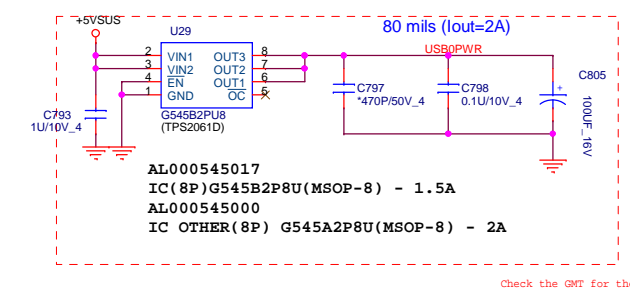
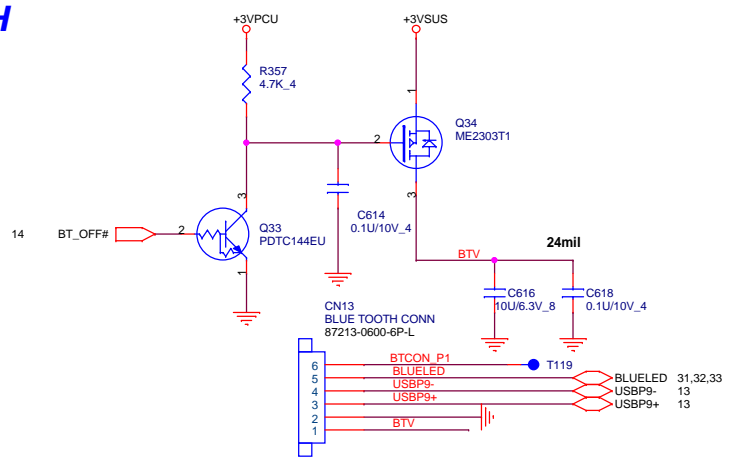


## Modem CONN



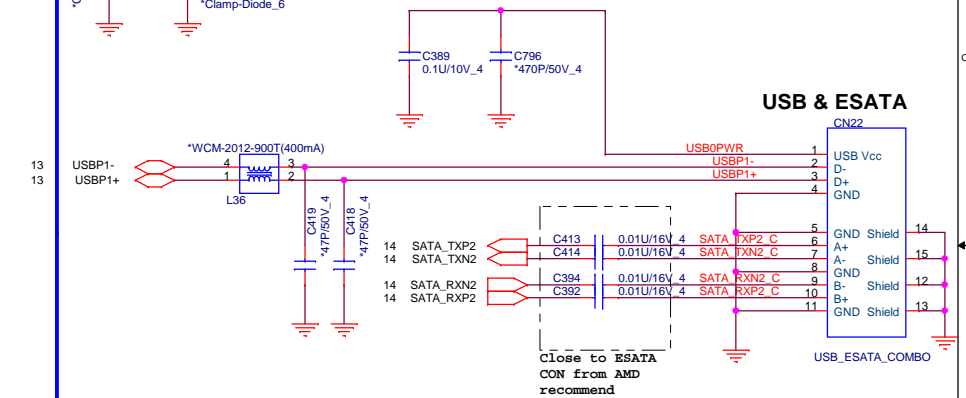
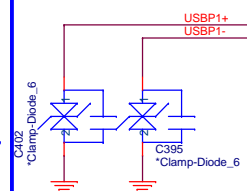
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>AMP_TPA6017/MDC1.5/CPU FAN</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 28 of 42



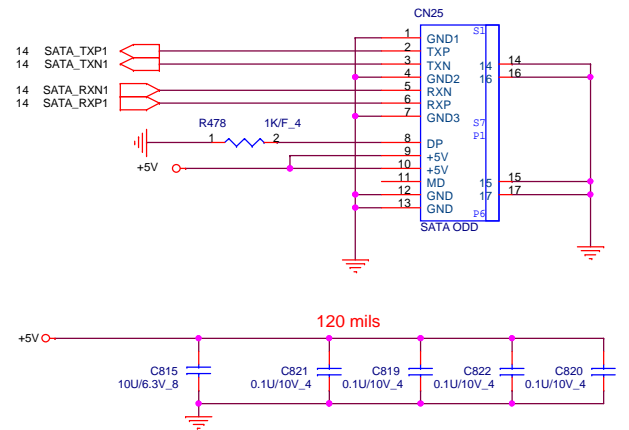
AL000545017  
 IC (8P) G545B2P8U (MSOP-8) - 1.5A  
 AL000545000  
 IC OTHER (8P) G545A2P8U (MSOP-8) - 2A

Check the GMT for the chip



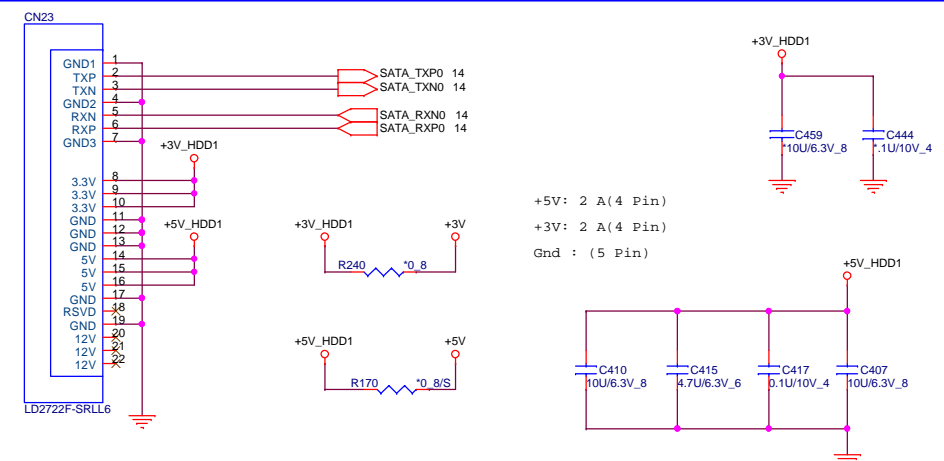
Close to ESATA  
 CON from AMD  
 recommend

SATA CD-ROM



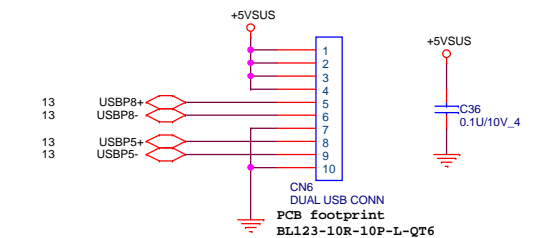
120 mils

SATA HDD



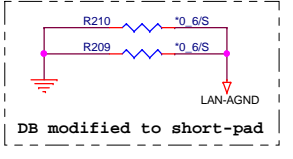
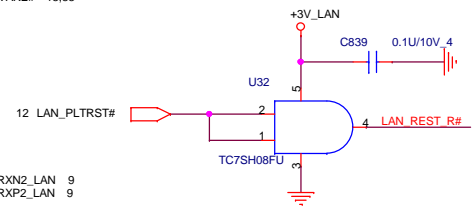
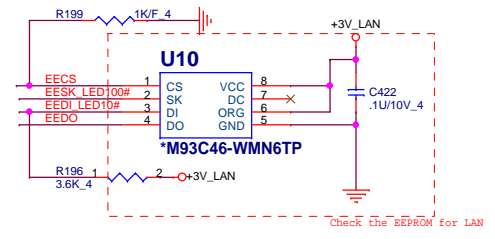
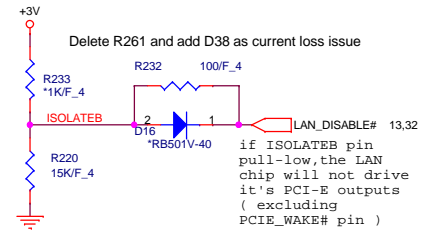
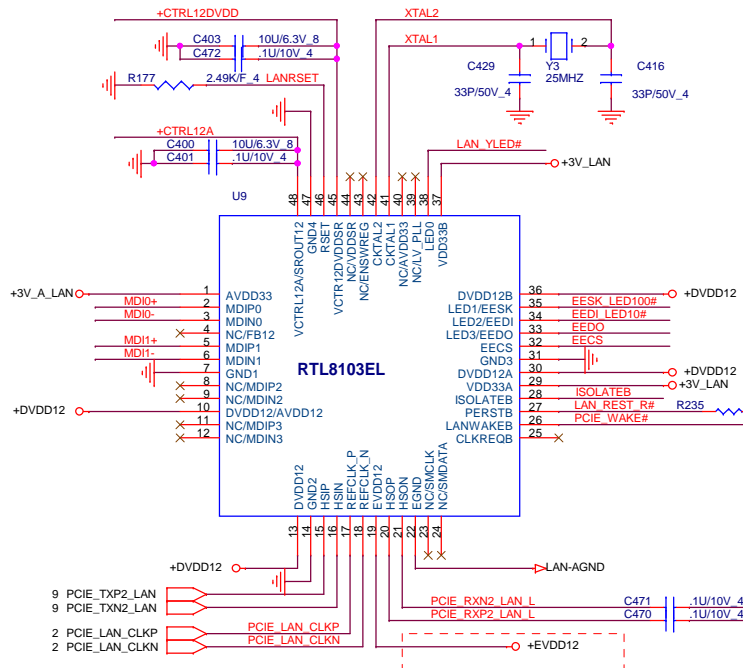
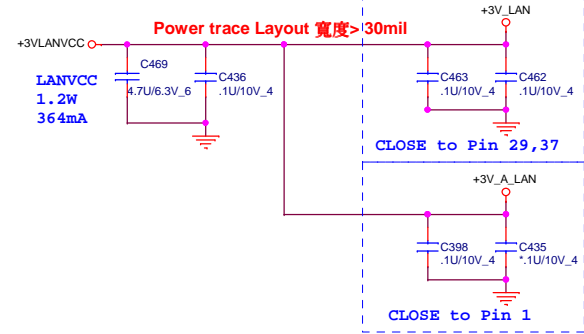
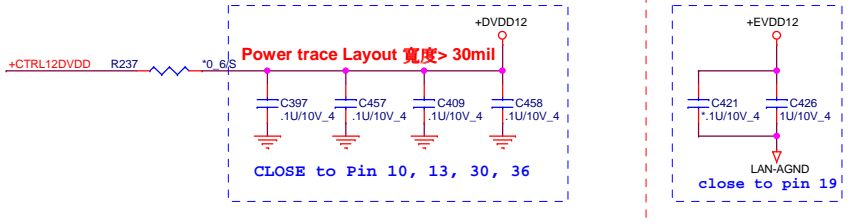
+5V: 2 A (4 Pin)  
 +3V: 2 A (4 Pin)  
 Gnd : (5 Pin)

RIGHT SIDE USBX2

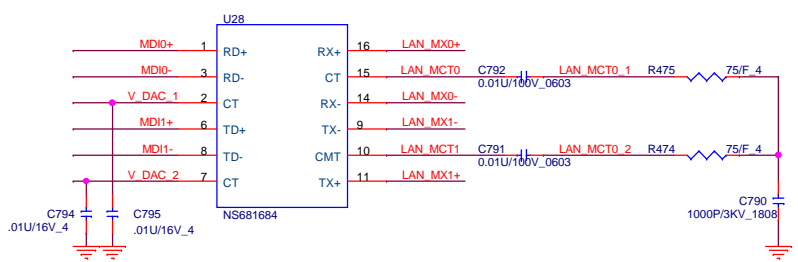


**PROJECT : OP8**  
 Quanta Computer Inc.

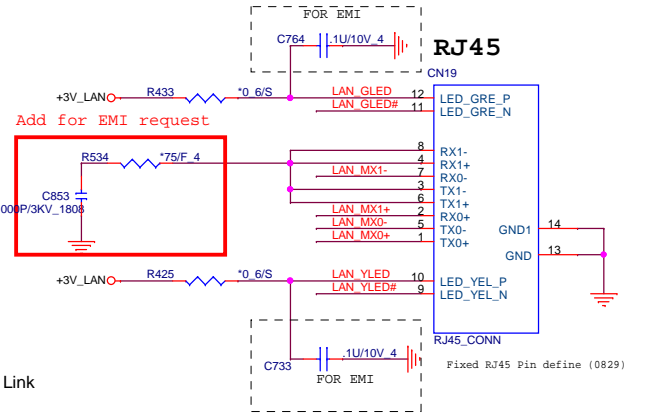
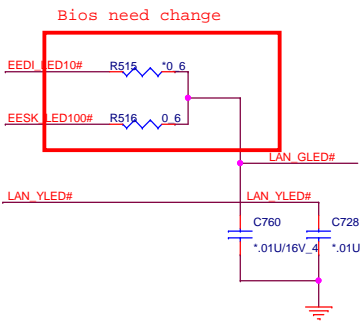
Size Custom	Document Number <b>BT/USBX3/ESATA/SATA ODD/HDD</b>	Rev 1A
Date: Friday, March 20, 2009		Sheet 29 of 42



### LAN\_Transformer



Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0 Tx/Rx
LED1	O	56	35	LED1 LNK100
LED2	O	55	34	LED2 LNK10
LED3	O	54	33	LED3 NA



NB5/RD2

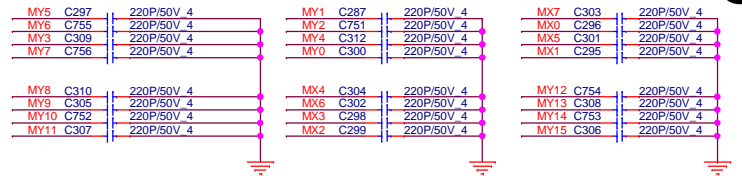
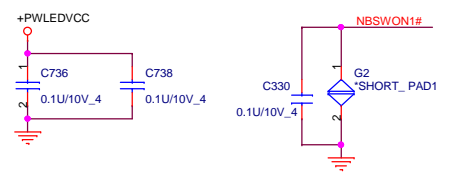
**PROJECT : OP8**  
Quanta Computer Inc.

Rev 1A

Size Custom	Document Number <b>RTL8102EL/RJ45</b>	Rev 1A
Date: Friday, March 20, 2009	Sheet 30 of 42	

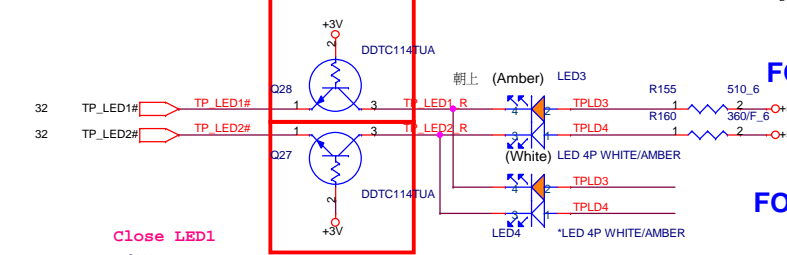
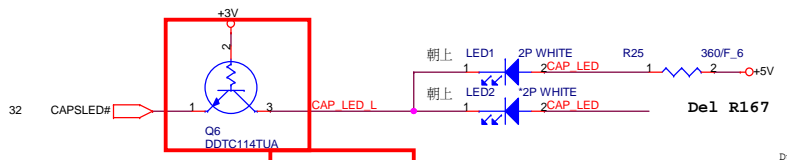
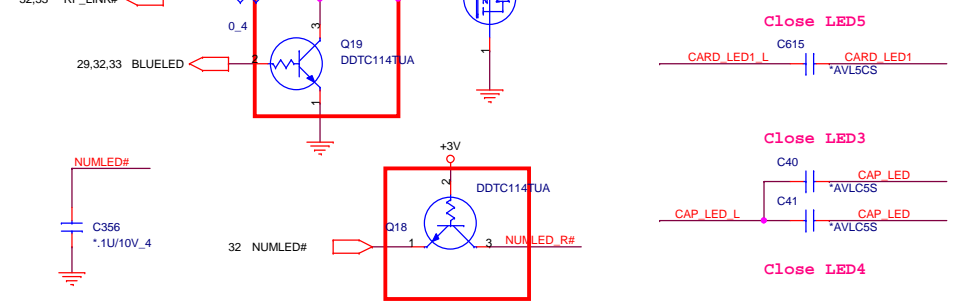
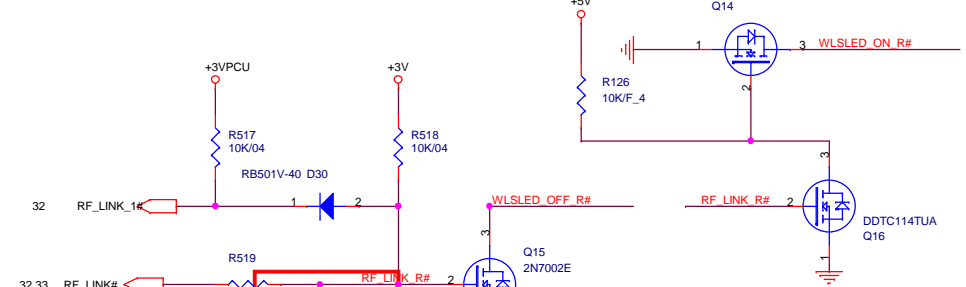
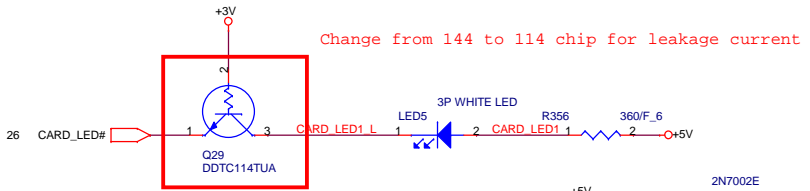
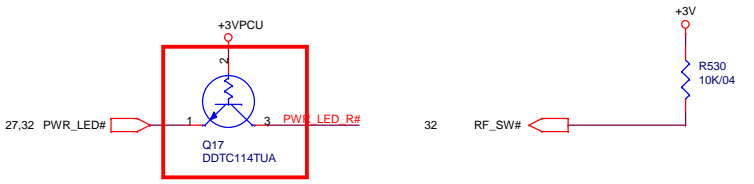
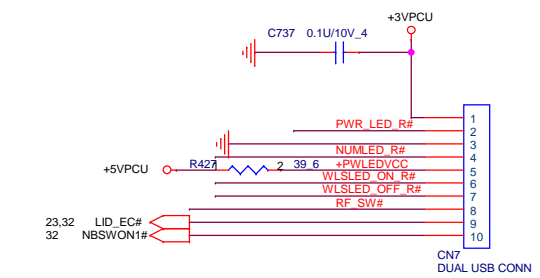
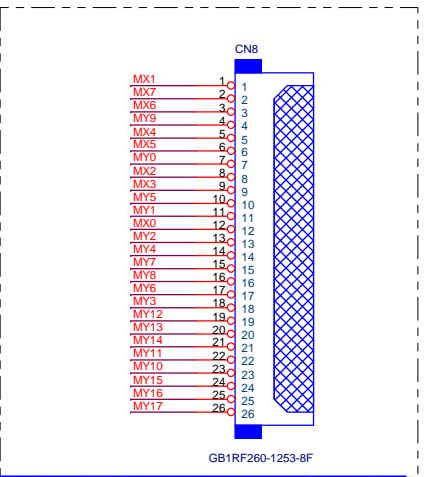
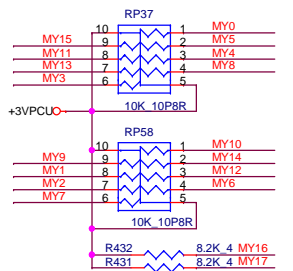
# POWER BUTTON CONNECT

31



1. +3VPCU(LIDSWITCH PWR)
2. PWR\_LED#
3. GND
4. NumLED
5. +5VPCU (PWRLED PWR)
6. WLSLED\_ON#
7. WLSLED\_OFF#
8. RF\_SW#
9. LIDSWITCH
10. POWERON#

## KEYBOARD PULL-UP

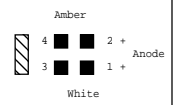


FOR 16"  
FOR 17.3"

Dual Color ,Right angle

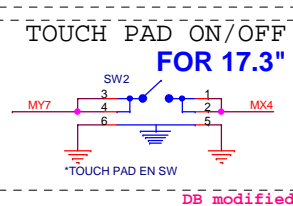
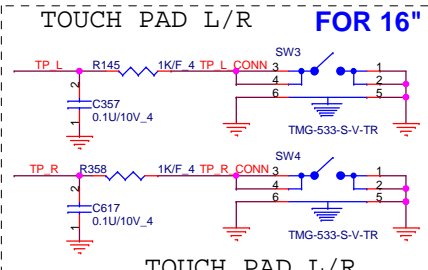
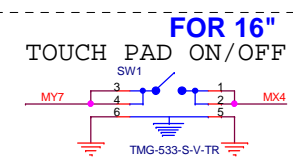
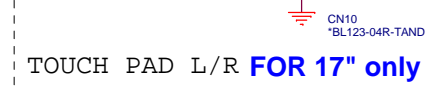
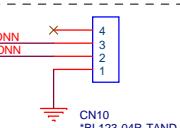
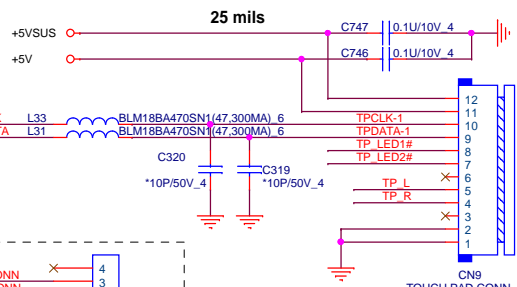
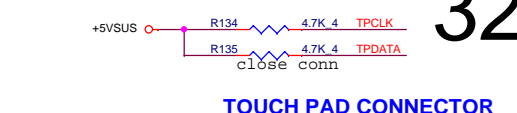
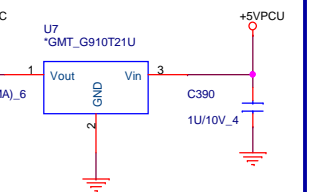
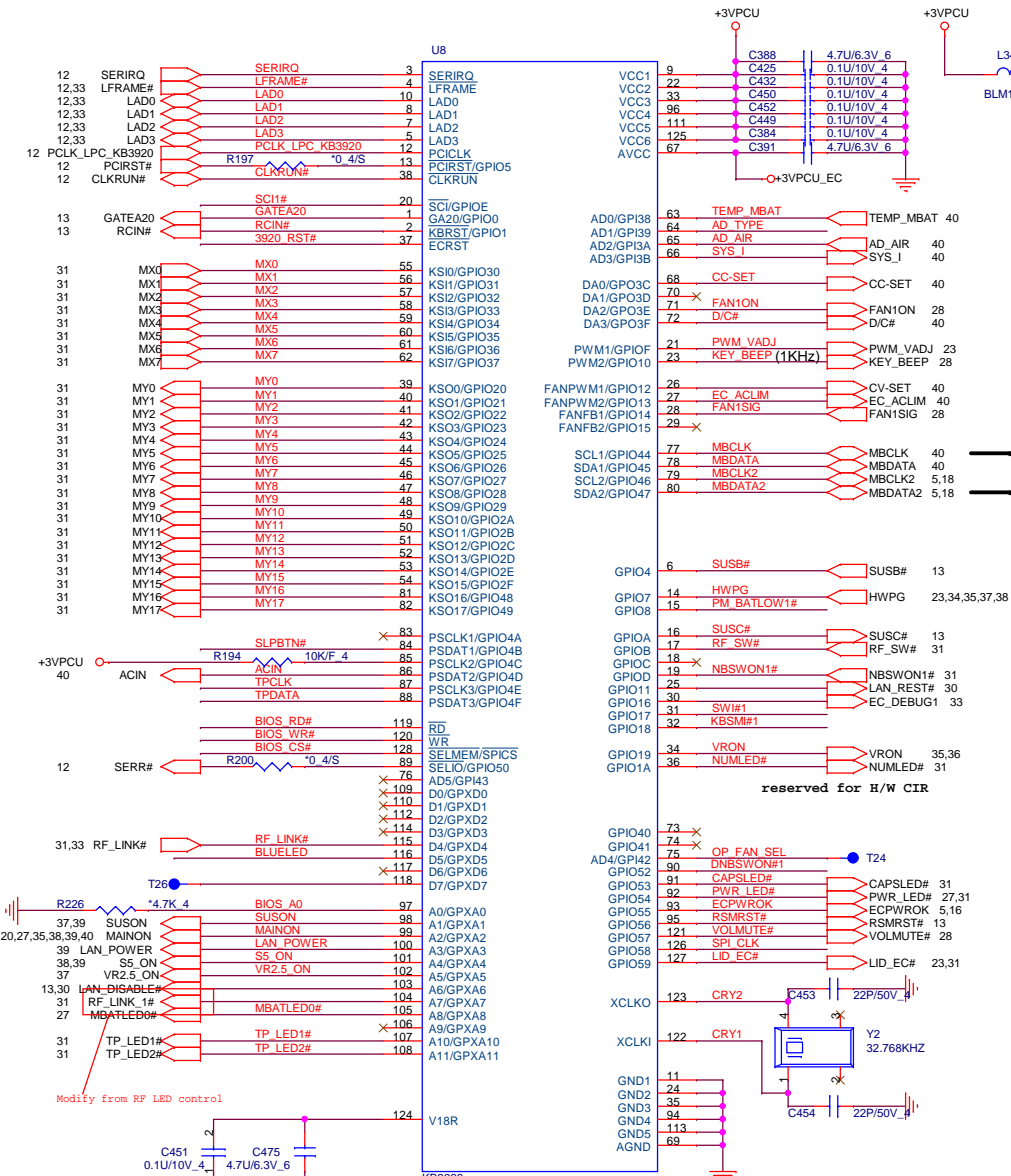
FOR 16"

FOR 17.3"



**PROJECT : OP8**  
Quanta Computer Inc.

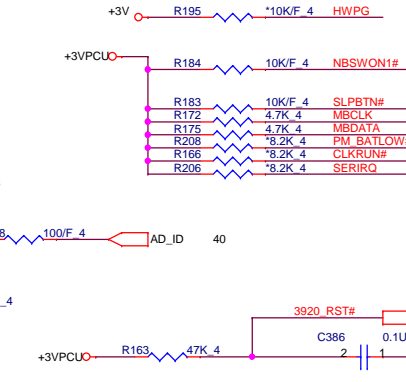
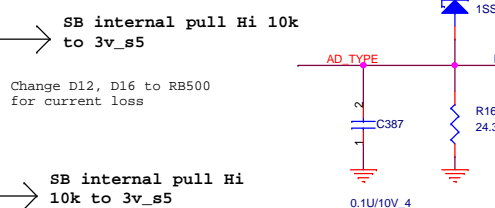
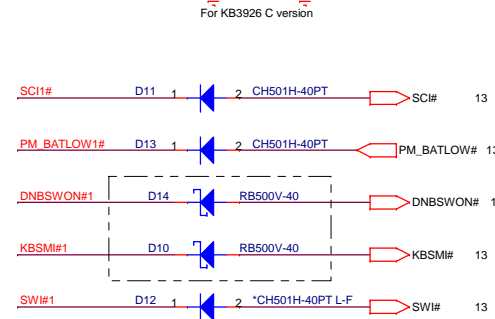
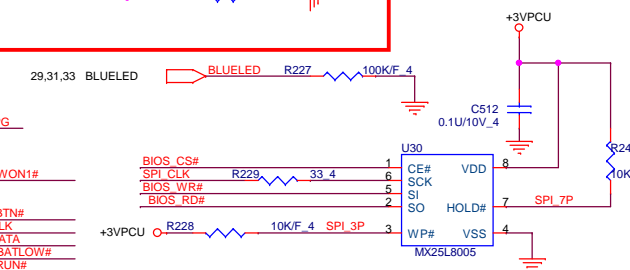
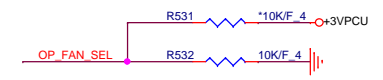
Size Custom	Document Number	Rev 1A
LED/KEYBOARD/SW_BOARD		
Date: Friday, March 20, 2009	Sheet 31 of 42	



→ Battery charge/discharge Cap button  
 → VGA thermal system thermal

Project Model	GPIO42
OPX 16"	Low
OPX 17.3"	High

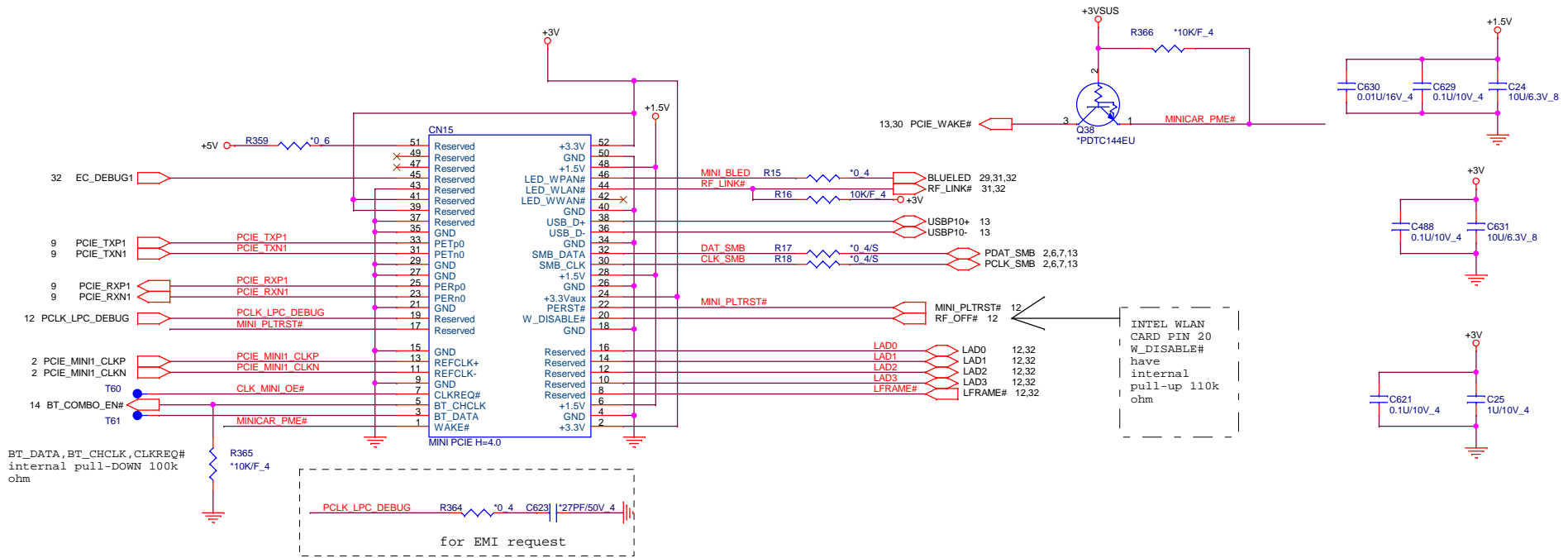
GPIO42 control fan table



**PROJECT : OP8**  
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# Mini PCI-E Card 1 WLAN



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Size Custom	Document Number <b>Mini CARD</b>	Rev 1A
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NBS/RD2

# DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,20,23,24,25,27,28,29,30,31,32,33,35,39

TON: 5V / 3.3V  
GND = 400 / 500KHz  
REF = 400 / 300KHz  
VCC = 200 / 300KHz

- +5VPCU 27,31,32,35,36,37,38
- +3VPCU 5,12,23,27,29,31,32,36,37,38,40
- +3VSUS 13,26,29,33,35,37,39
- +3VS5 5,7,12,13,14,15,16,39
- +5VSUS 23,29,32,39
- +5V 5,15,20,23,24,25,27,28,29,31,32,33,35,38,39
- +3VLANVCC 30,39

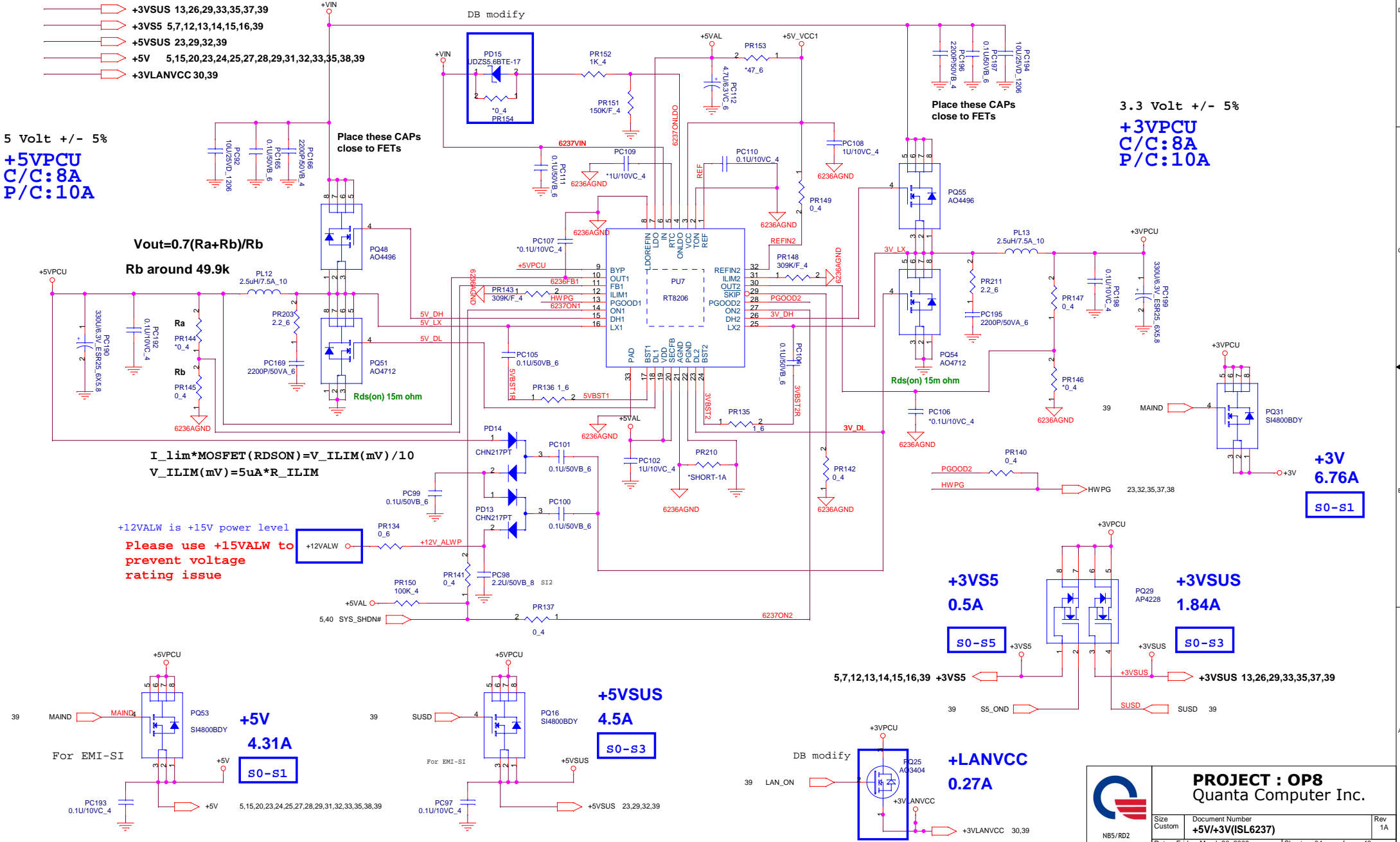
5 Volt +/- 5%  
**+5VPCU**  
C/C:8A  
P/C:10A

3.3 Volt +/- 5%  
**+3VPCU**  
C/C:8A  
P/C:10A

$V_{out} = 0.7(Ra + Rb) / Rb$   
Rb around 49.9k

$I_{lim} * MOSFET (RDSON) = V_{ILIM} (mV) / 10$   
 $V_{ILIM} (mV) = 5uA * R_{ILIM}$

+12VALW is +15V power level  
Please use +15VALW to prevent voltage rating issue



**+3V**  
6.76A  
S0-S1

**+3VS5**  
0.5A  
S0-S5

**+3VSUS**  
1.84A  
S0-S3

**+5VSUS**  
4.5A  
S0-S3

**+5V**  
4.31A  
S0-S1

**+LANVCC**  
0.27A

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Size: Custom	Document Number: +5V/+3V(ISL6237)	Rev: 1A
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$$T_{on} = 3.85p * R_{TON} * V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} * T_{ON})$$

reserved for pwr seq -- andrew

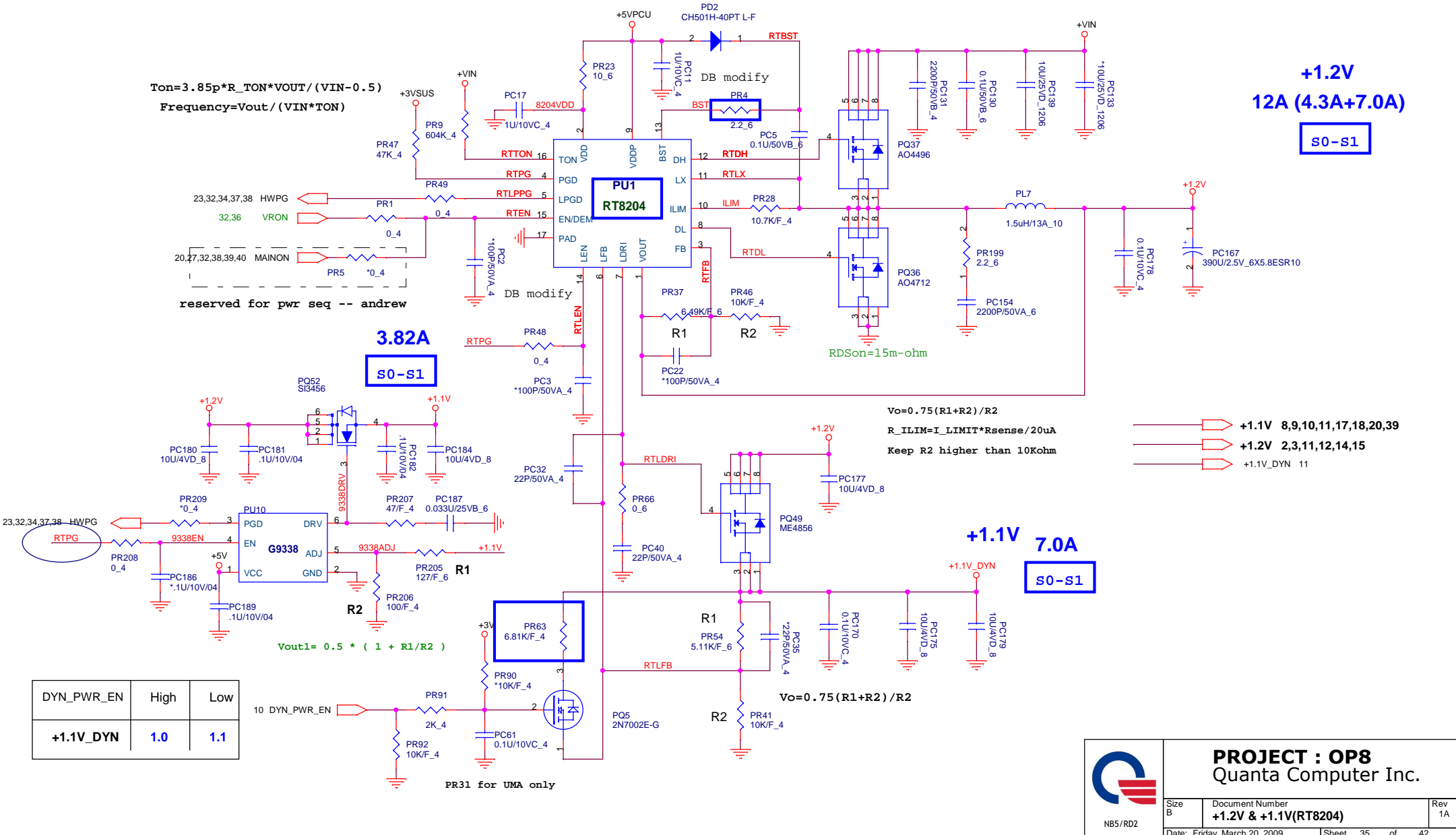
**3.82A**  
**S0-S1**

**+1.2V**  
**12A (4.3A+7.0A)**  
**S0-S1**

**+1.1V**  
**7.0A**  
**S0-S1**

- +1.1V 8,9,10,11,17,18,20,39
- +1.2V 2,3,11,12,14,15
- +1.1V\_DYN 11

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1



$$V_o = 0.75 (R1 + R2) / R2$$

$$R_{ILIM} = I_{LIMIT} * R_{sense} / 20\mu A$$

Keep R2 higher than 10Kohm

$$V_o = 0.75 (R1 + R2) / R2$$

PR31 for UMA only



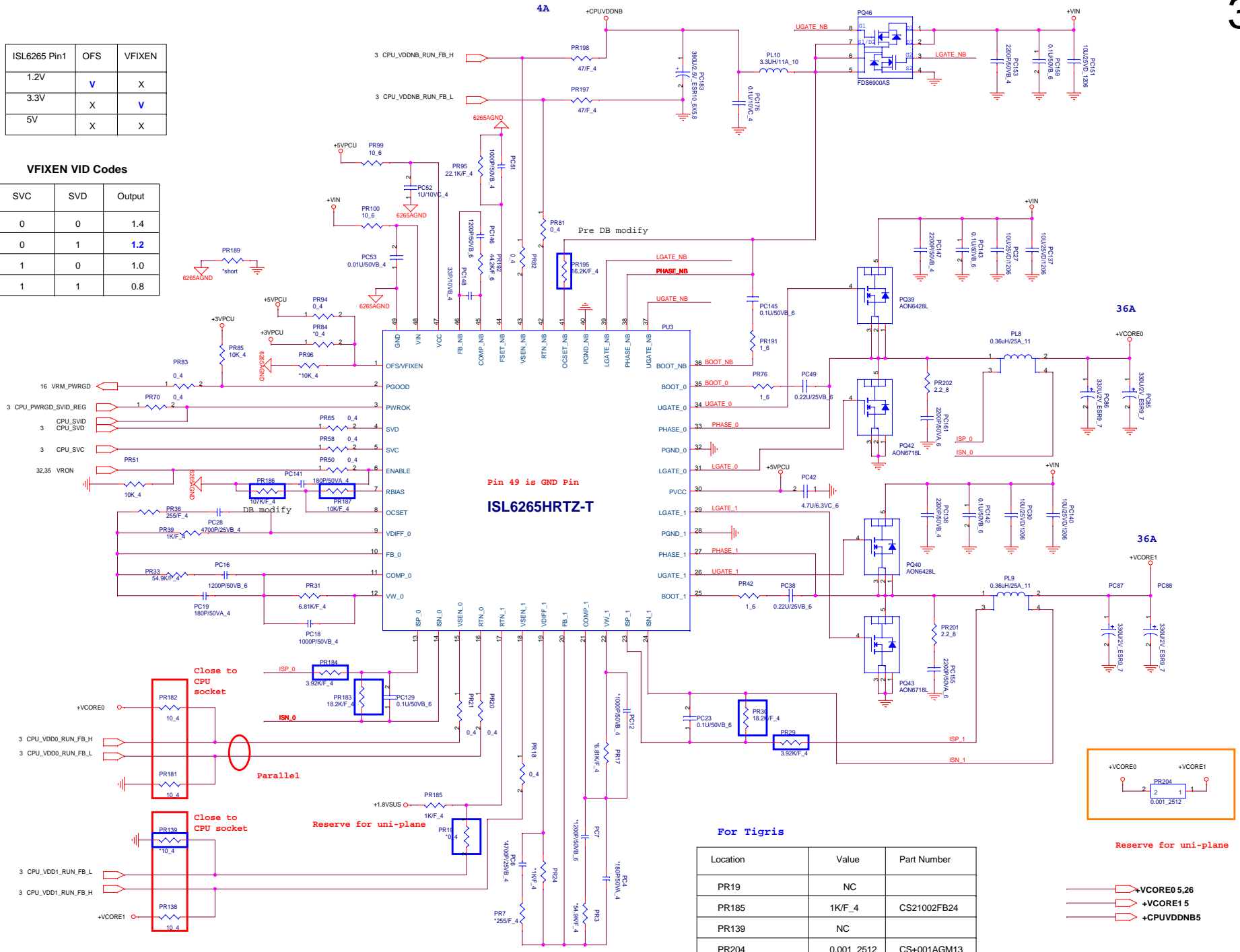
**PROJECT : OP8**  
**Quanta Computer Inc.**

Size B	Document Number <b>+1.2V &amp; +1.1V(RT8204)</b>	Rev 1A
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

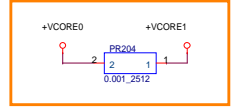
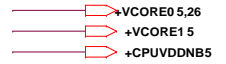
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

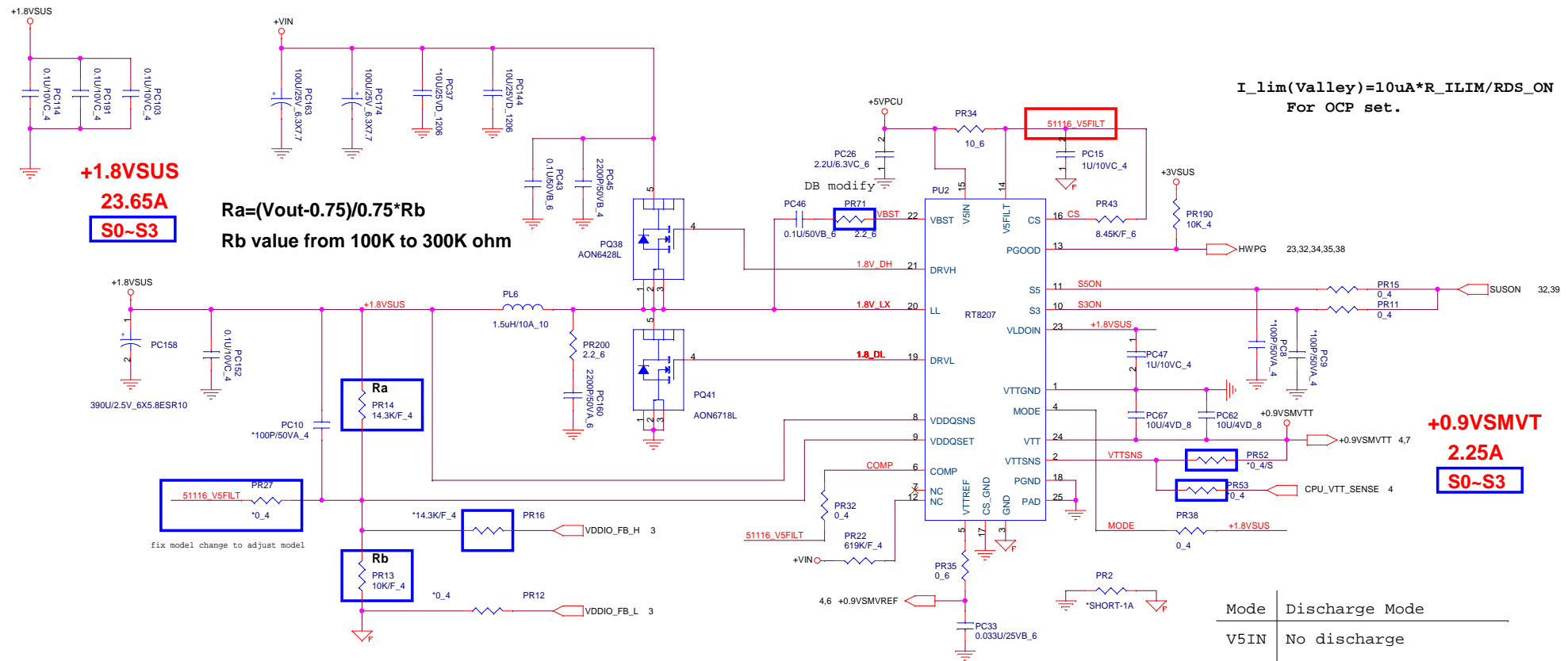


For Tigris

Location	Value	Part Number
PR19	NC	
PR185	1K/F_4	CS21002FB24
PR139	NC	
PR204	0.001_2512	CS+001AGM13
PC12,PR17,PC4,PC7, PR3,PR24,PC6,PR7	NC	



→ +2.5V 3  
→ +1.8VSUS 3,4,5,6,7,36,38



$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS\_ON}$   
For OCP set.

**+1.8VSUS**  
**23.65A**  
**S0~S3**

$R_a = (V_{out} - 0.75) / 0.75 * R_b$   
Rb value from 100K to 300K ohm

**+0.9VSMVT**  
**2.25A**  
**S0~S3**

**+2.5V**  
**0.25A**  
**S0~S1**

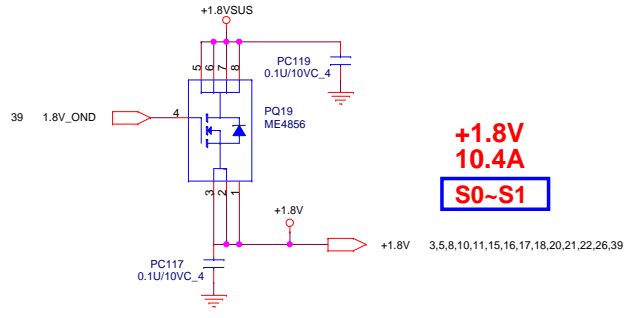
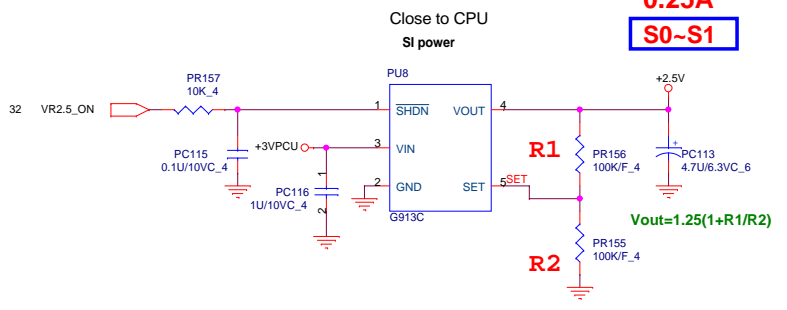
**+1.8V**  
**10.4A**  
**S0~S1**

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V\_TRIP(mV) = R\_TRIP(Kohm) * 10(uA)$

$I\_OCP = V\_trip / R_{ds\_on} + I\_Ripple / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V\_vddqsns / 2$	DDR
V5IN	1.8	$V\_vddqsns / 2$	DDR2
FB	adjustable	$V\_VDDQSN / 2$	$1.5V < VDDQ < 3V$



**Discrete: SI4856**  
**UMA: SI4800**

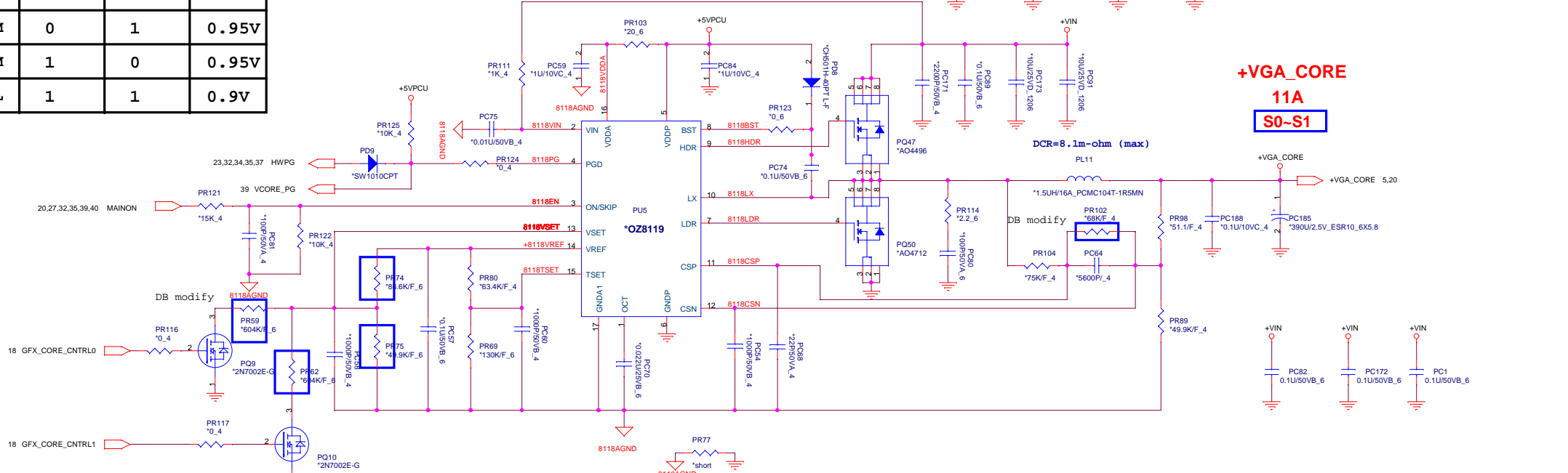
**PROJECT : OP8**  
Quanta Computer Inc.

Size Custom	Document Number <b>1.8VSUS/DDR_VTER/+1.8V/2.5V</b>	Rev 1A
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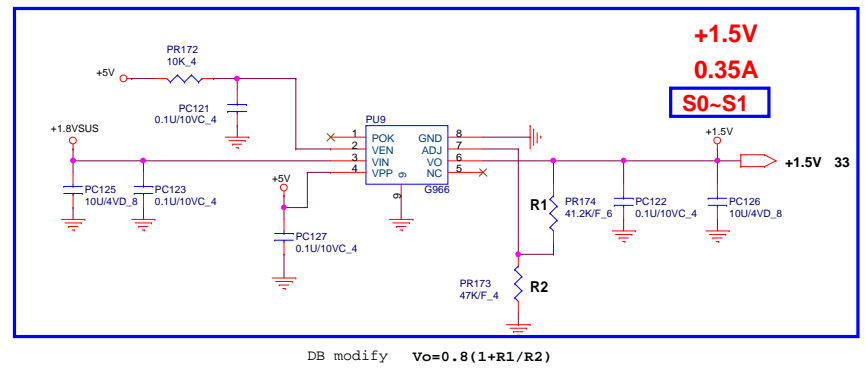
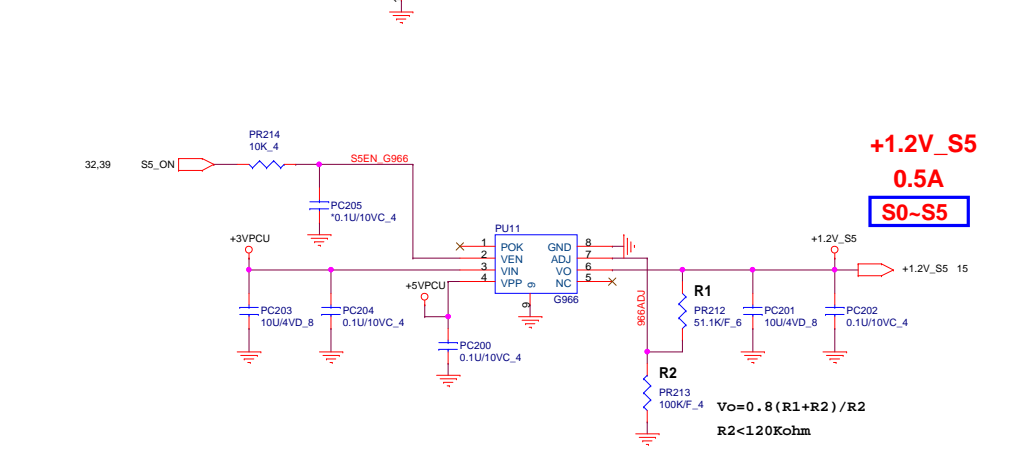
# ATI M92-S2

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.0V
M	0	1	0.95V
M	1	0	0.95V
L	1	1	0.9V

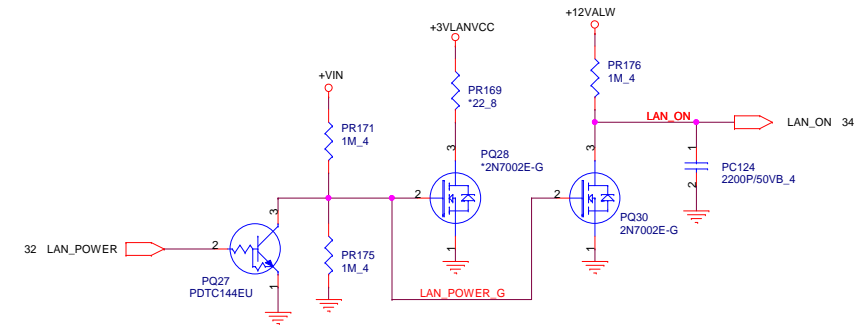
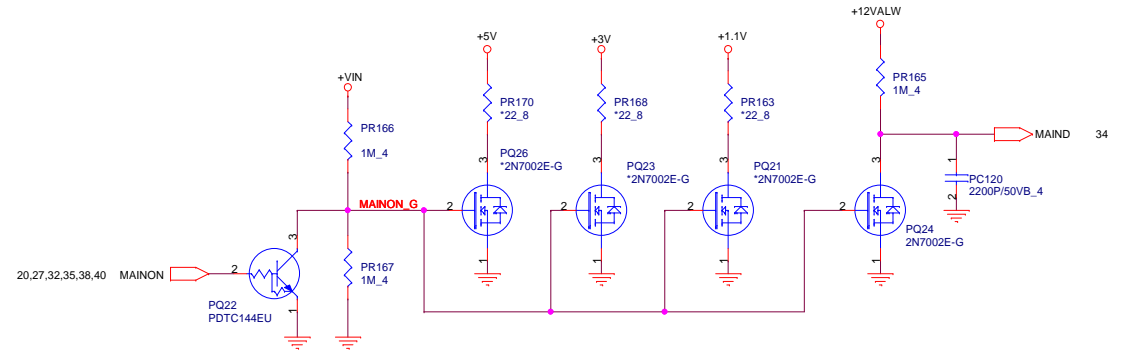
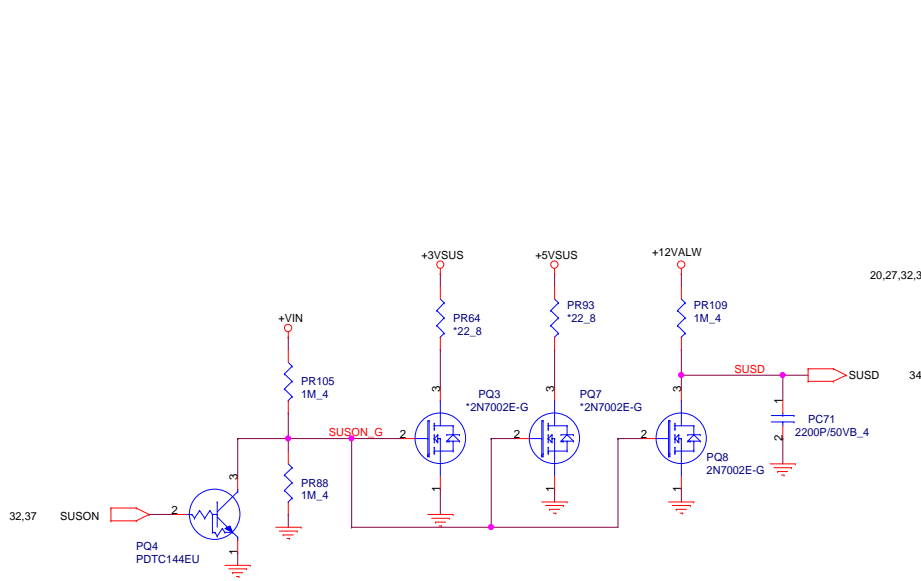
- +VGA\_CORE 5,20
- +1.2V\_S5 15
- +1.5V 33



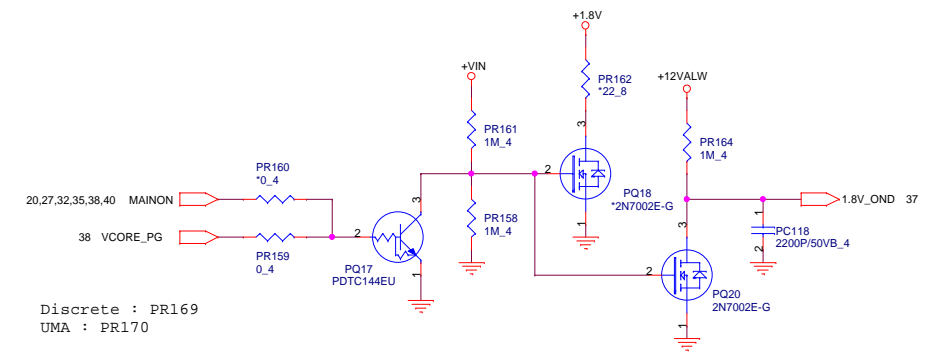
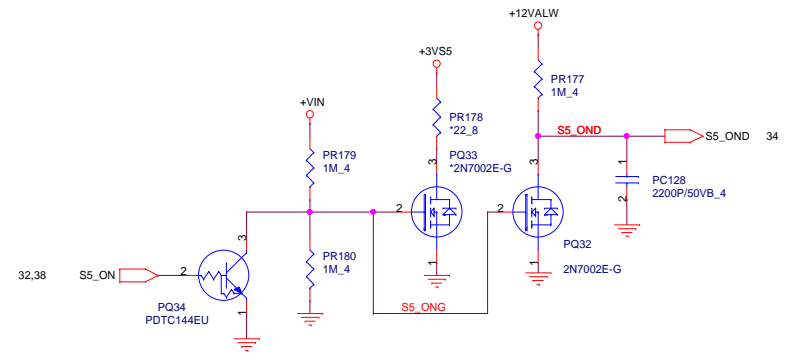
**+VGA\_CORE**  
**11A**  
**S0-S1**



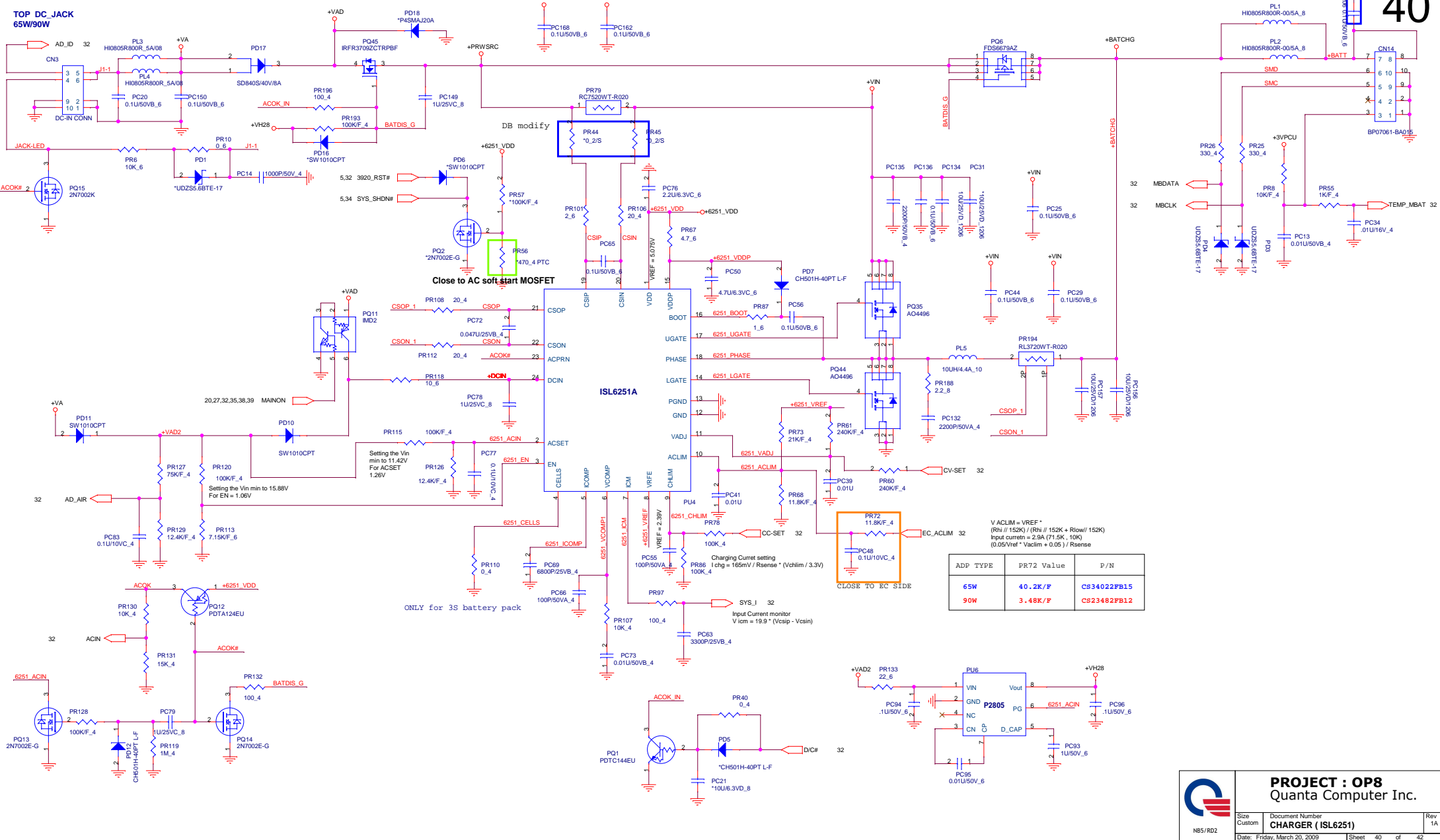
	<b>PROJECT : OP8</b>		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	VGA PWR OZ8118/1.2V_S5/+1.5	
NB5/RD2	Date:	Friday, March 20, 2009	Sheet 38 of 42



*For Discrete Only*



Discrete : PR169  
UMA : PR170



**PROJECT : OP8**  
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Size: Custom | Document Number: **CHARGER (ISL6251)** | Rev: 1A

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