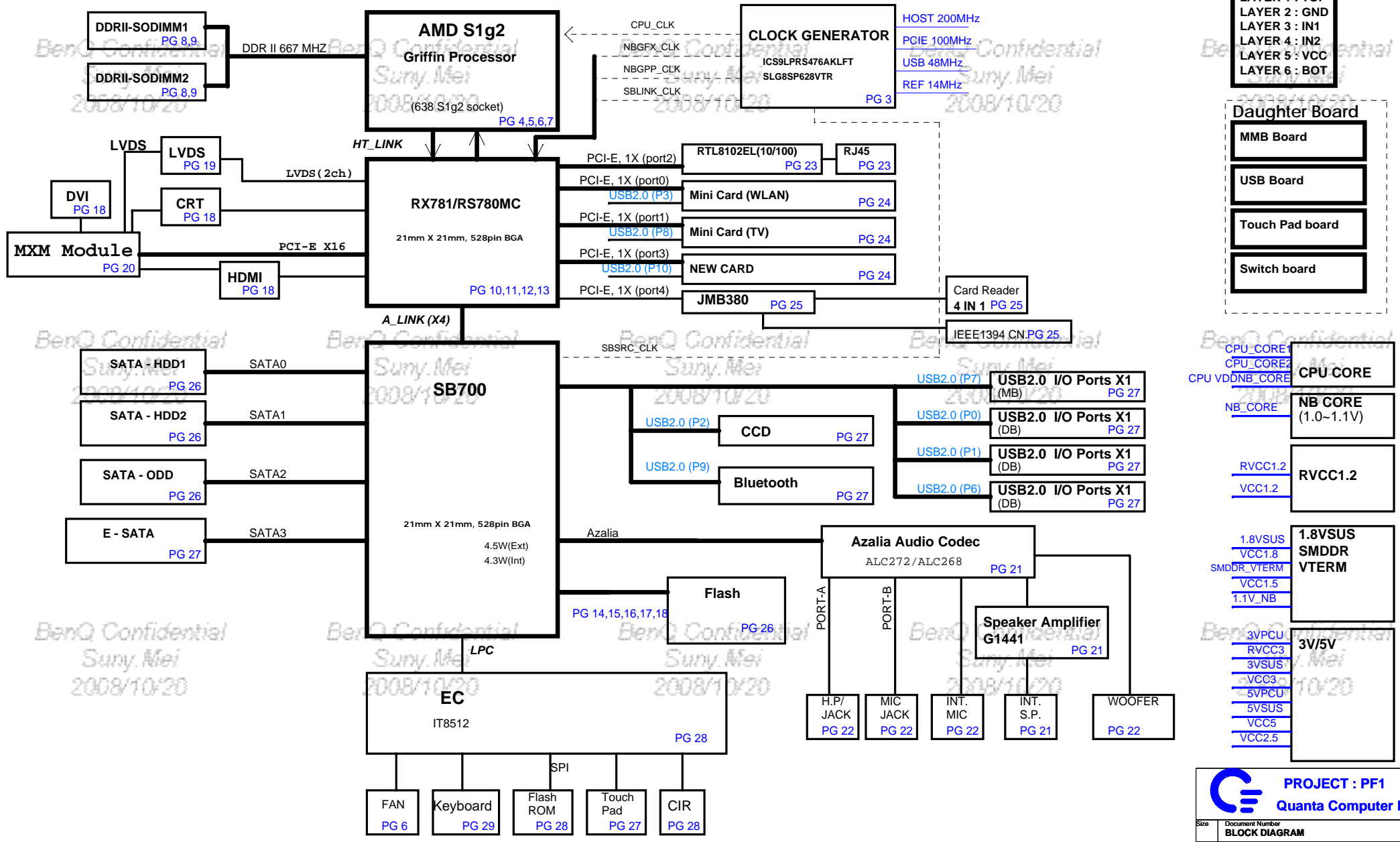


# PF1/2/PF1Q BLOCK DIAGRAM

01

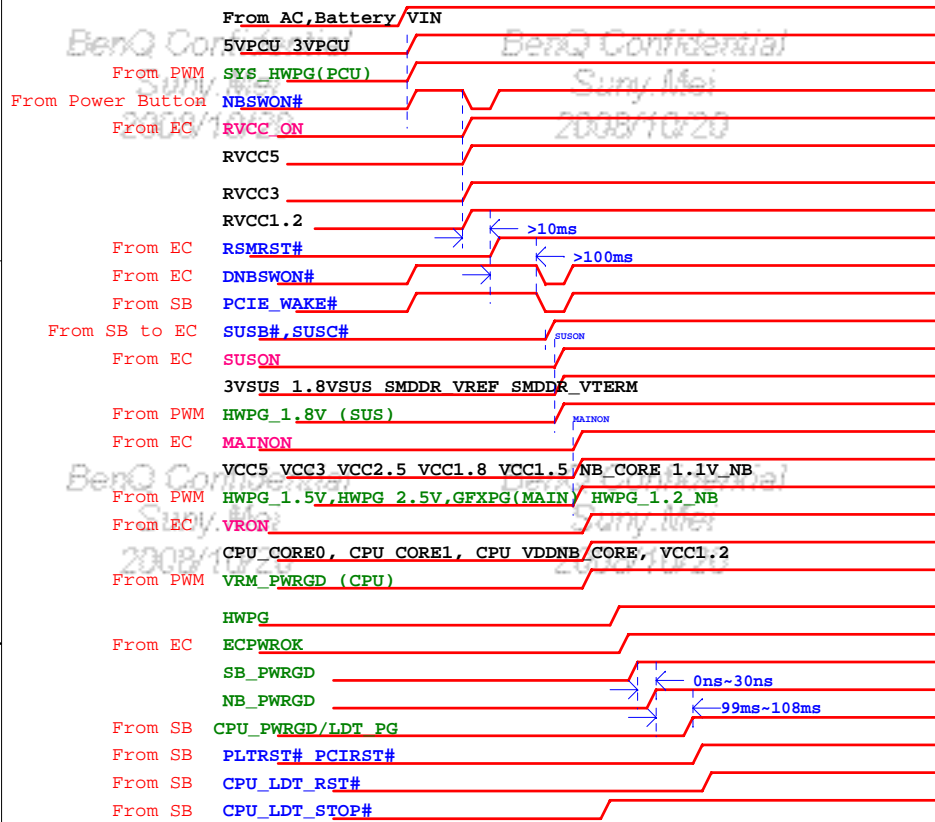


**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>BLOCK DIAGRAM</b>	2A
Date: Wednesday, June 11, 2008	Sheet	1 of 40

PF1 Power On Sequence

BOM naming rule



Items	Function	BTO	Name	Description
1	UMA	v	IV@	Internal VGA stuff
2	Discrete VGA	v	EV@	External VGA stuff
3	Subwoofer	v	WF@	Only for PF2P
4	IEEE 1394	v	EV@	External VGA model stuff
5	DVI-I	v	EV@	External VGA model stuff
6	D-SUB(CRT)	v	IV@	Internal VGA model stuff
7	HDMI	v	EV@	External VGA model stuff
8	CIR	v	CIR@	For PF1P and PF2P(M86)
9	TV		TV@	For PF1P and PF2P(M86)
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				

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\*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB700 SMBUS Table

	CLK GEN	RAM	Mini Card (TV)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(VCC3)	V	V	V	V	V	
SB700 SDATA1/SCLK1(3V_S5)						V
SB700 SDATA2/SCLK2(3V_S5)						
Power	VCC3	VCC3	VCC3	VCC3(Atheros)	VCC3	RVCC3
Reserve MOS ckt	V	V	V	V	V	V

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI	CEC
EC775 SDATA1/SCLK1(3VPCU)	V						
EC775 SDATA2/SCLK2(3VPCU)		V	V				
EC775 SDATA3/SCLK3(3VPCU)				V	V	V	
EC775 SDATA4/SCLK4(3VPCU)							
Power	3VPCU	VCC3	3VPCU	VCC3	3VPCU	5VPCU	
Reserve MOS ckt	X	V	X	V	X	V	

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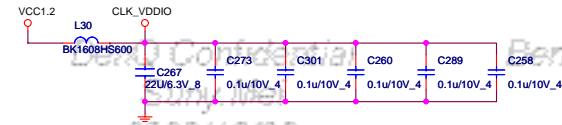
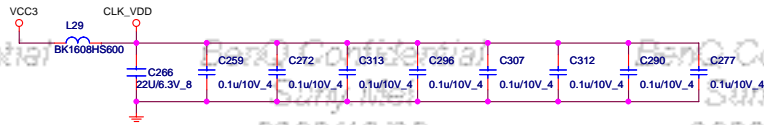
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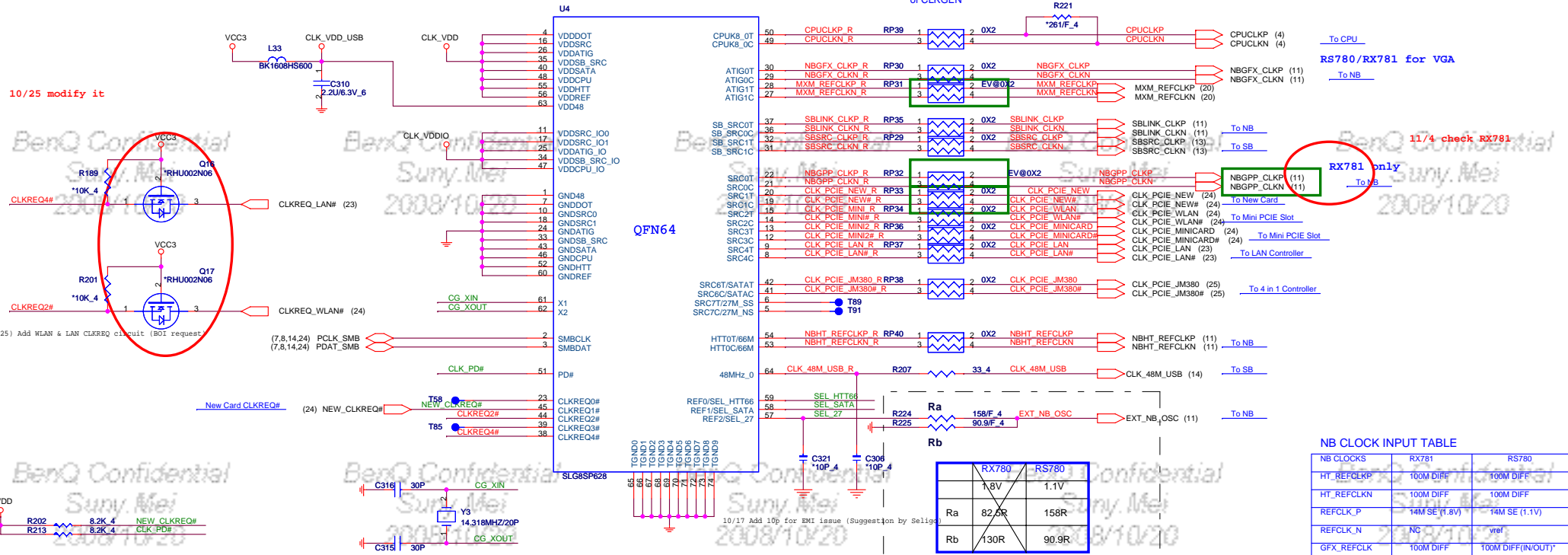
**PROJECT : PF1**  
**Quanta Computer Inc.**

Size: 5  
Document Number:  
**SYSTEM INFORMATION**  
Date: Wednesday, June 11, 2008 Sheet 2 of 40



ICS9LPRS480 P/N : ALPRS480000  
 SLG8SP628 P/N : AL8SP628000  
 RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



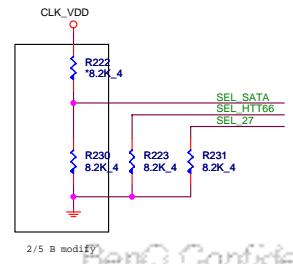
**NB CLOCK INPUT TABLE**

NB CLOCKS	RX781	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF (IN/OUT)
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

	RX780	RS780
Ra	82.0R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +1%(0402)LF -->CS11302FB15  
 RES CHIP 158 1/16W +1%(0402) -->CS11582FB00  
 RES CHIP 90.9 1/16W +1%(0402) -->CS08022FB15  
 RES CHIP 82.5 1/16W +1%(0402) -->CS08252FB11

CLOCKS name	RX781	RS780	Clock pin function
NBGFCLKP NBGFCLKN	RP30 STUFF	RP30 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP31 STUFF	RP31 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPCLKN	RP32 STUFF	RP32 NC	to NB for RX780 for PCIeX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP35 STUFF	RP35 STUFF	to NB for AC-LINK reference clock



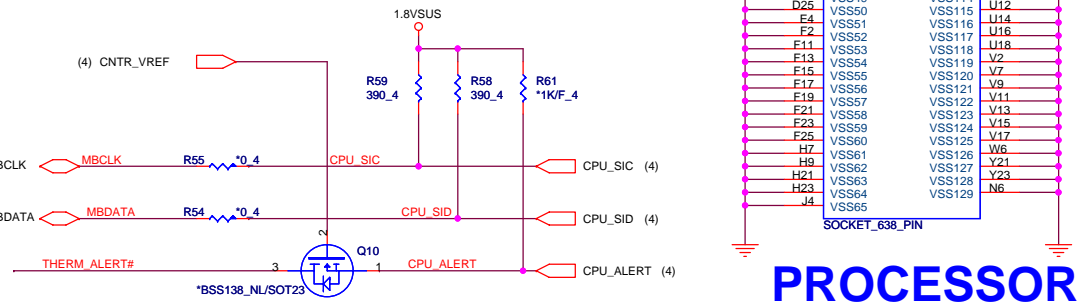
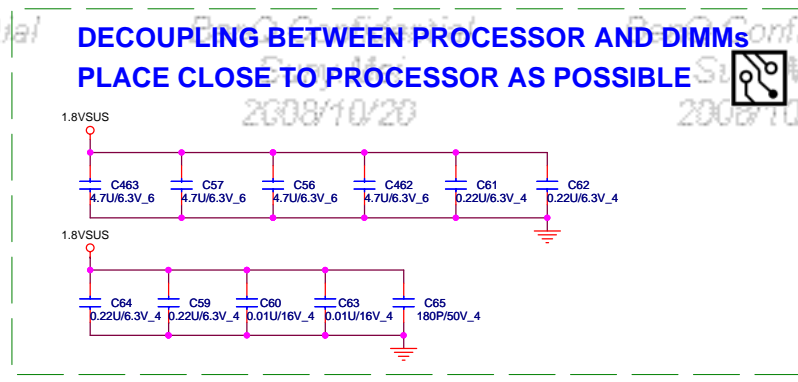
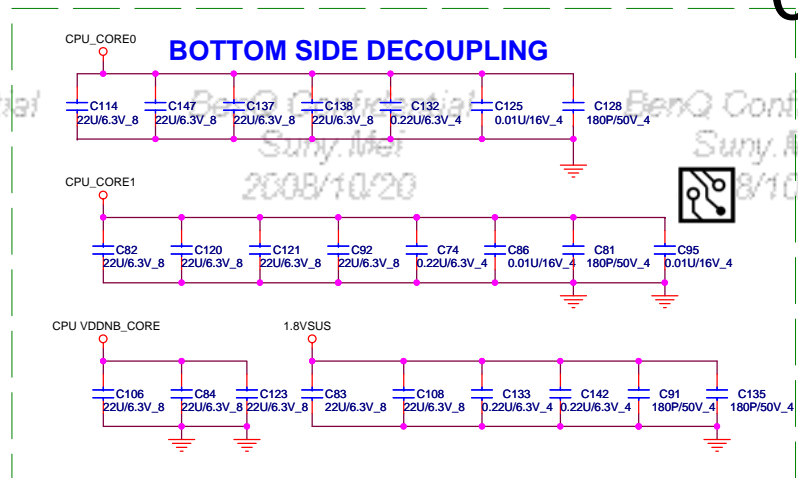
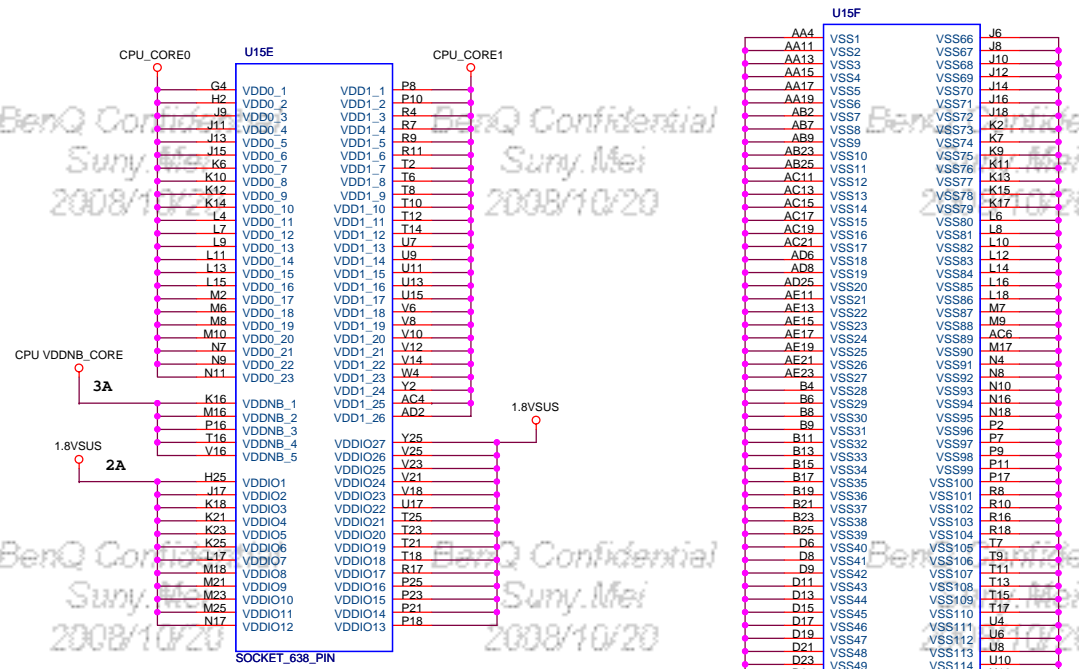
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_HTT66	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
SEL_SATA	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
SEL_27	0*	100 MHz SRC clock

**PROJECT : PF1**  
**Quanta Computer Inc.**

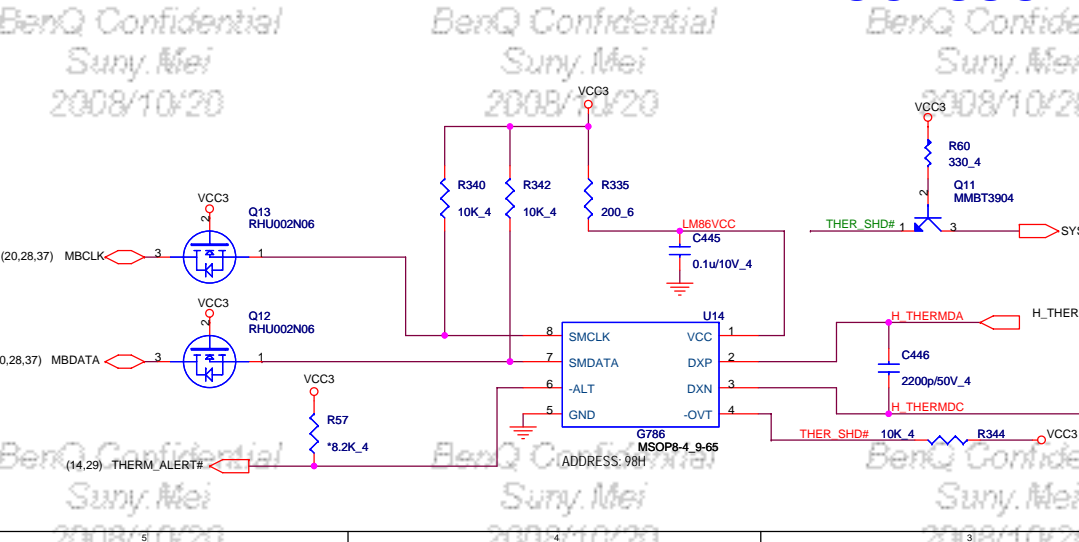
Size:  Document Number:   
**CLK\_GENERATOR\_SLG8SP628**  
 Date: Wednesday, June 11, 2008 Sheet 3 of 40 Rev 1A





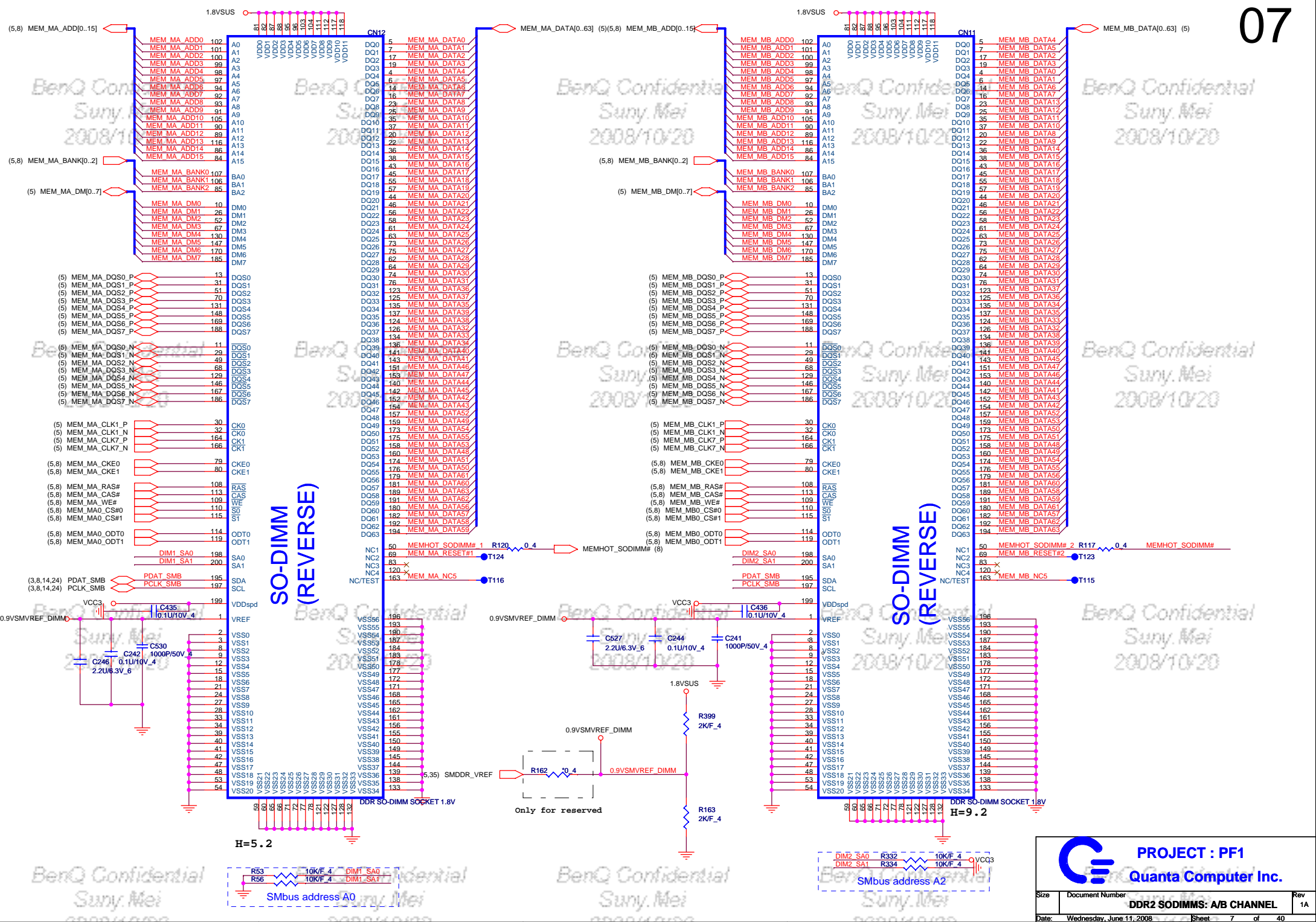


### PROCESSOR POWER AND GROUND



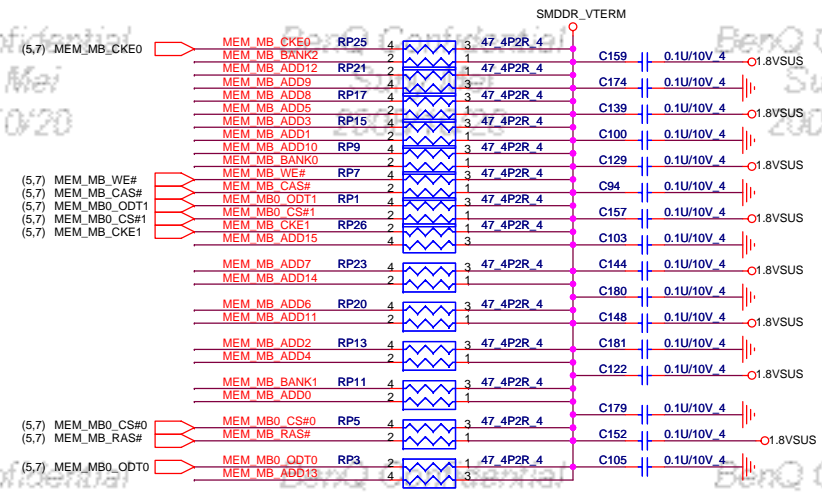
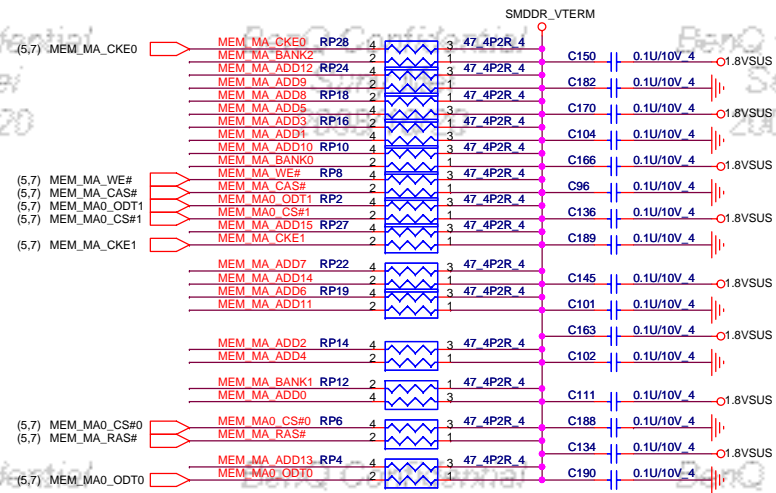
**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>S1G2 PWR &amp; GND 3/3</b>	1A
Date:	Wednesday, June 11, 2008	Sheet 6 of 40



(5,7) MEM\_MA\_ADD[0..15] → MEM\_MA\_ADD[0..15]  
(5,7) MEM\_MA\_BANK[0..2] → MEM\_MA\_BANK[0..2]

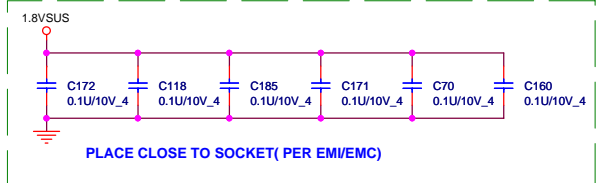
(5,7) MEM\_MB\_ADD[0..15] → MEM\_MB\_ADD[0..15]  
(5,7) MEM\_MB\_BANK[0..2] → MEM\_MB\_BANK[0..2]



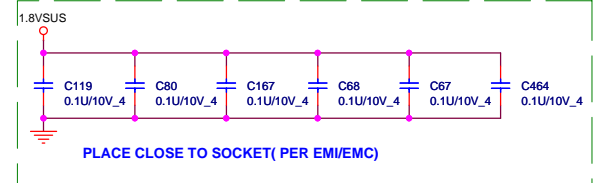
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



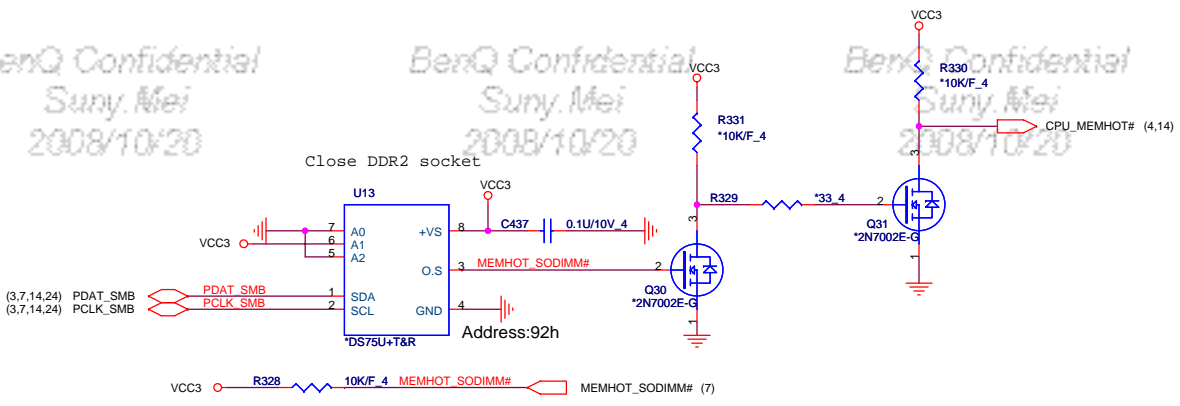
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



PLACE CLOSE TO SOCKET (PER EM/EMC)



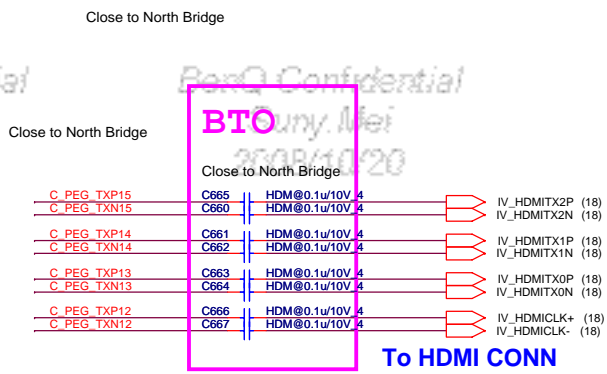
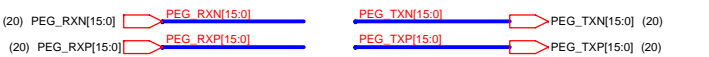
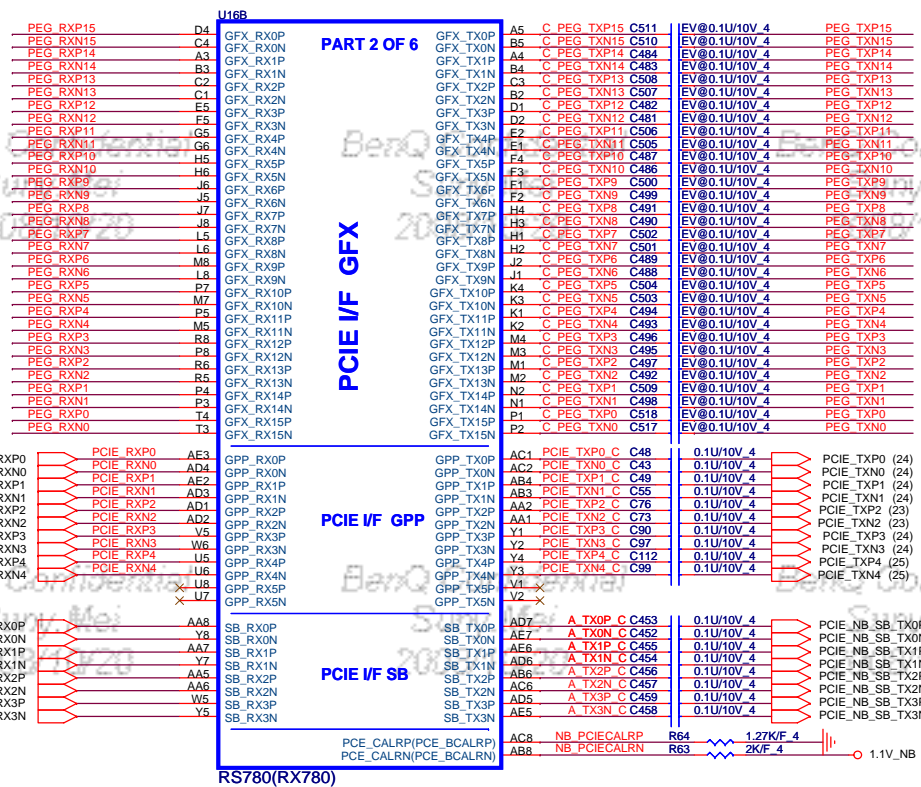
PLACE CLOSE TO SOCKET (PER EM/EMC)



**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR2 SODIMMS TERMINATIONS</b>	1A
Date:	Wednesday, June 11, 2008	Sheet 8 of 40





**RX780/RS740/RS780 difference table (PCIE LINK)**

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

**RS780 Display Port Support (muxed on GFX)**

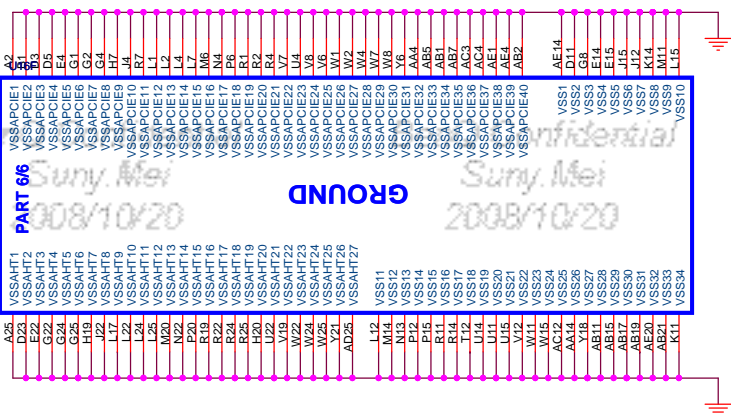
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

**PROJECT : PF1**  
**Quanta Computer Inc.**

Size: Document Number: **RS740/RS780-PCIE I/F 2/5** Rev: 1A

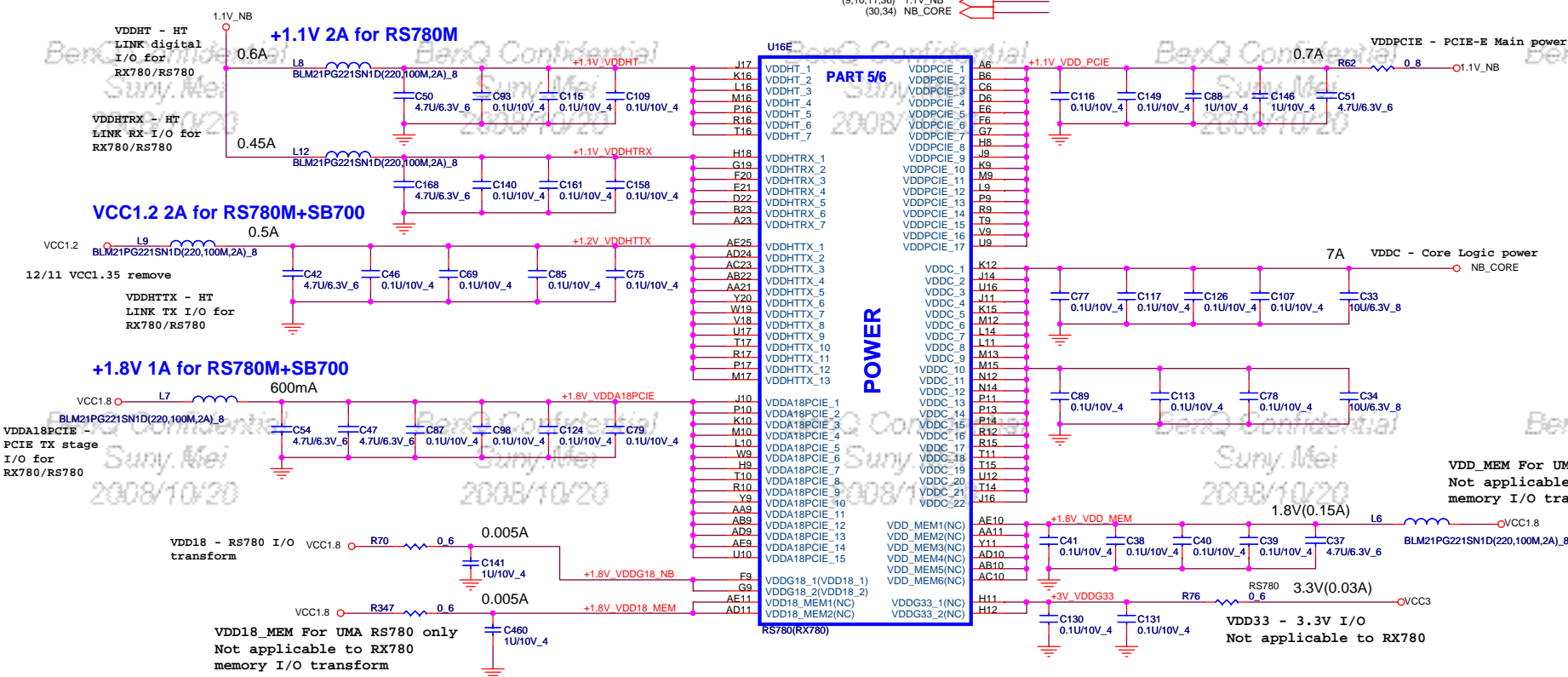
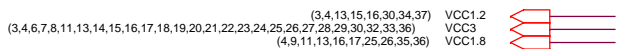
Date: Wednesday, June 11, 2008 Sheet: 10 of 40





RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD0	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD0	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD018	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC

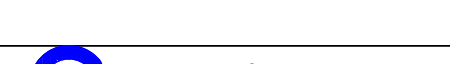
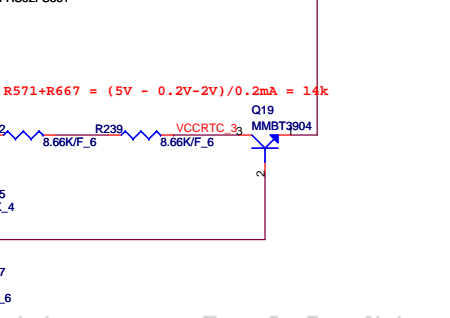
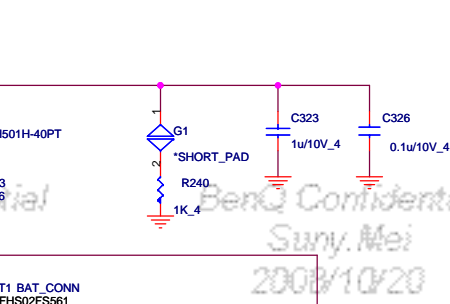
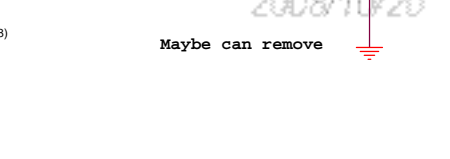
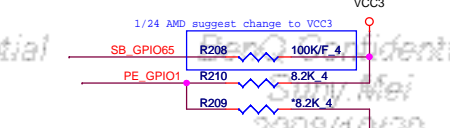
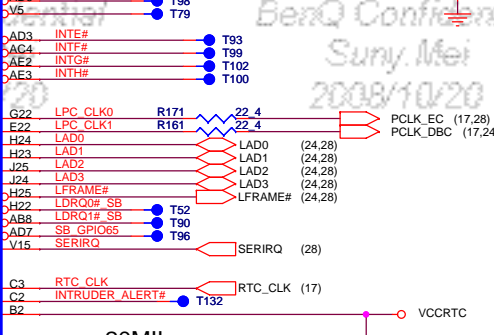
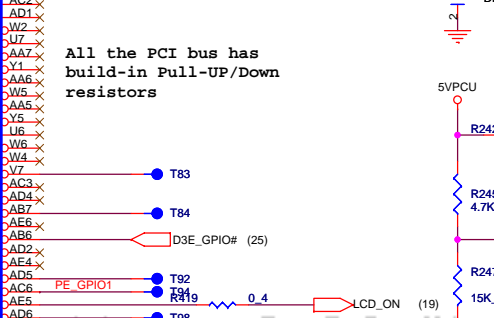
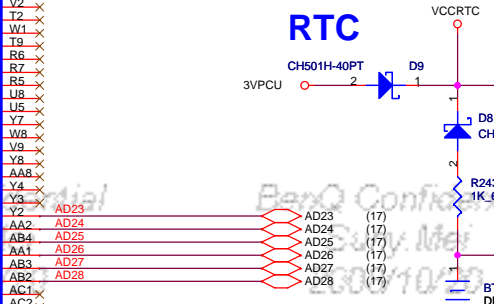
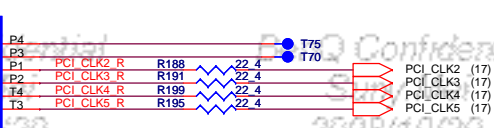
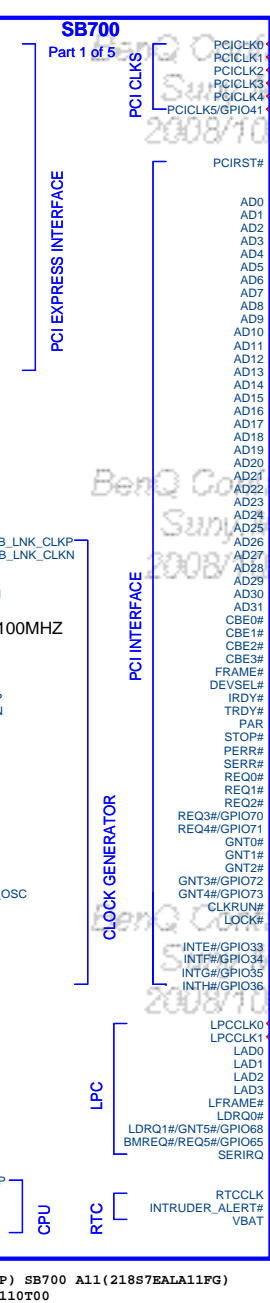
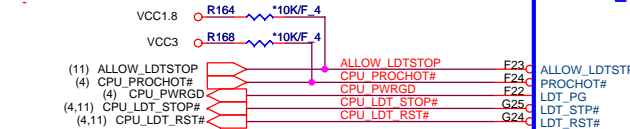
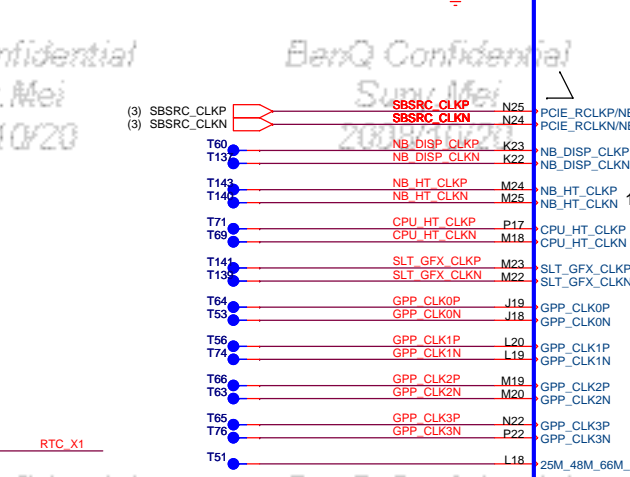
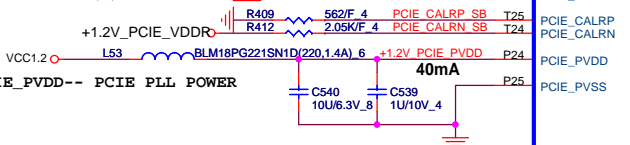
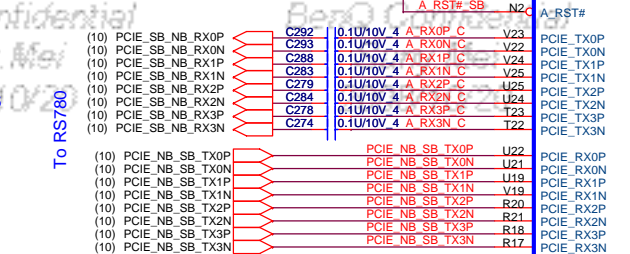


VDD\_MEM For UMA RS780 only  
Not applicable to RX780  
memory I/O transform

**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RS740/RS780-POWER5/5</b>	1A
Date:	Wednesday, June 11, 2008	Sheet 12 of 40

PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U19



All the PCI bus has  
build-in Pull-UP/Down  
resistors

$R571+R667 = (5V - 0.2V-2V)/0.2mA = 14k$

SB700  
IC CTRL(528P) SB700 A11(218S7EALA11FG)  
P/N : AJALA110T00

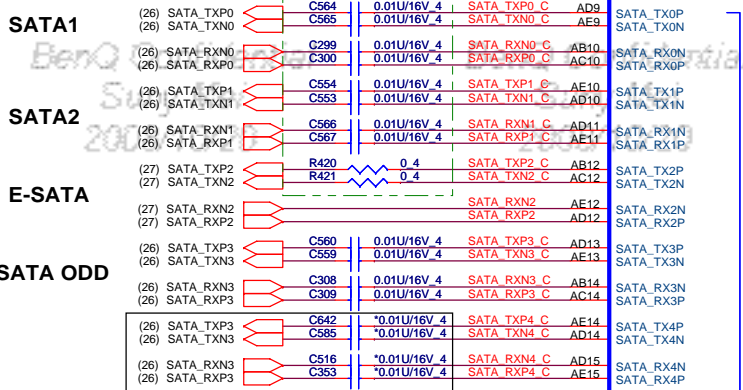
**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>SB700-PCIE/PCI/CPU/LPC 1/4</b>	1A
Date:	Wednesday, June 11, 2008	Sheet 13 of 40



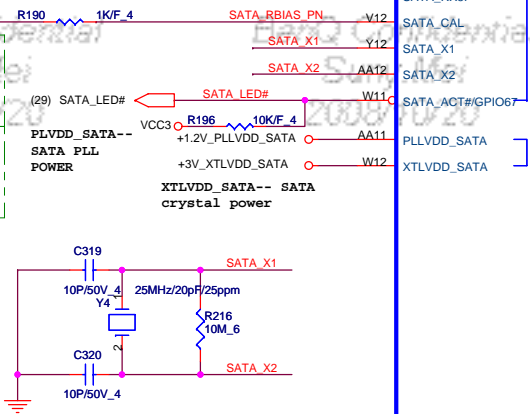
SATA PORT 0,1,2,3  
can support AHCI  
mode

PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600



SATA PORT 4,5 are  
only support IDE  
mode

NOTE:  
R190 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

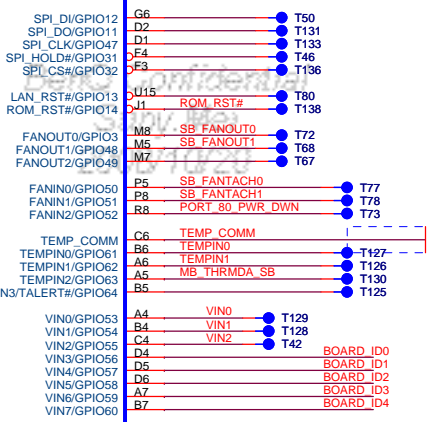
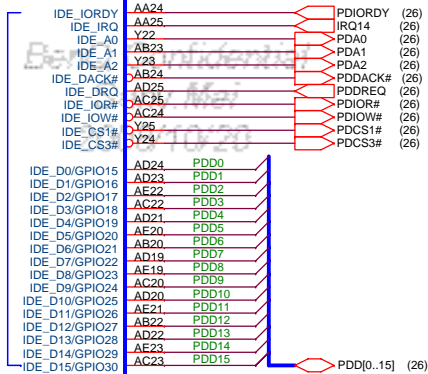


SB700  
Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR



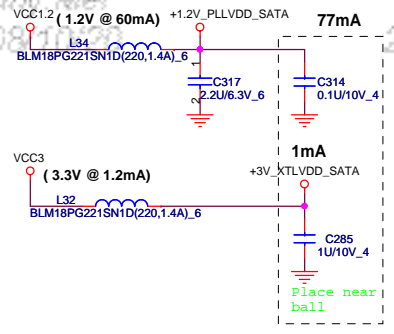
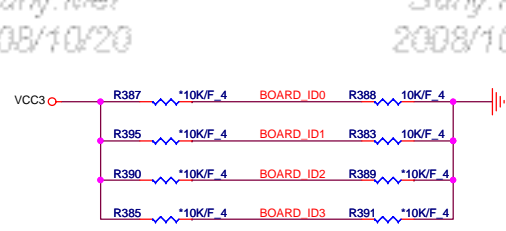
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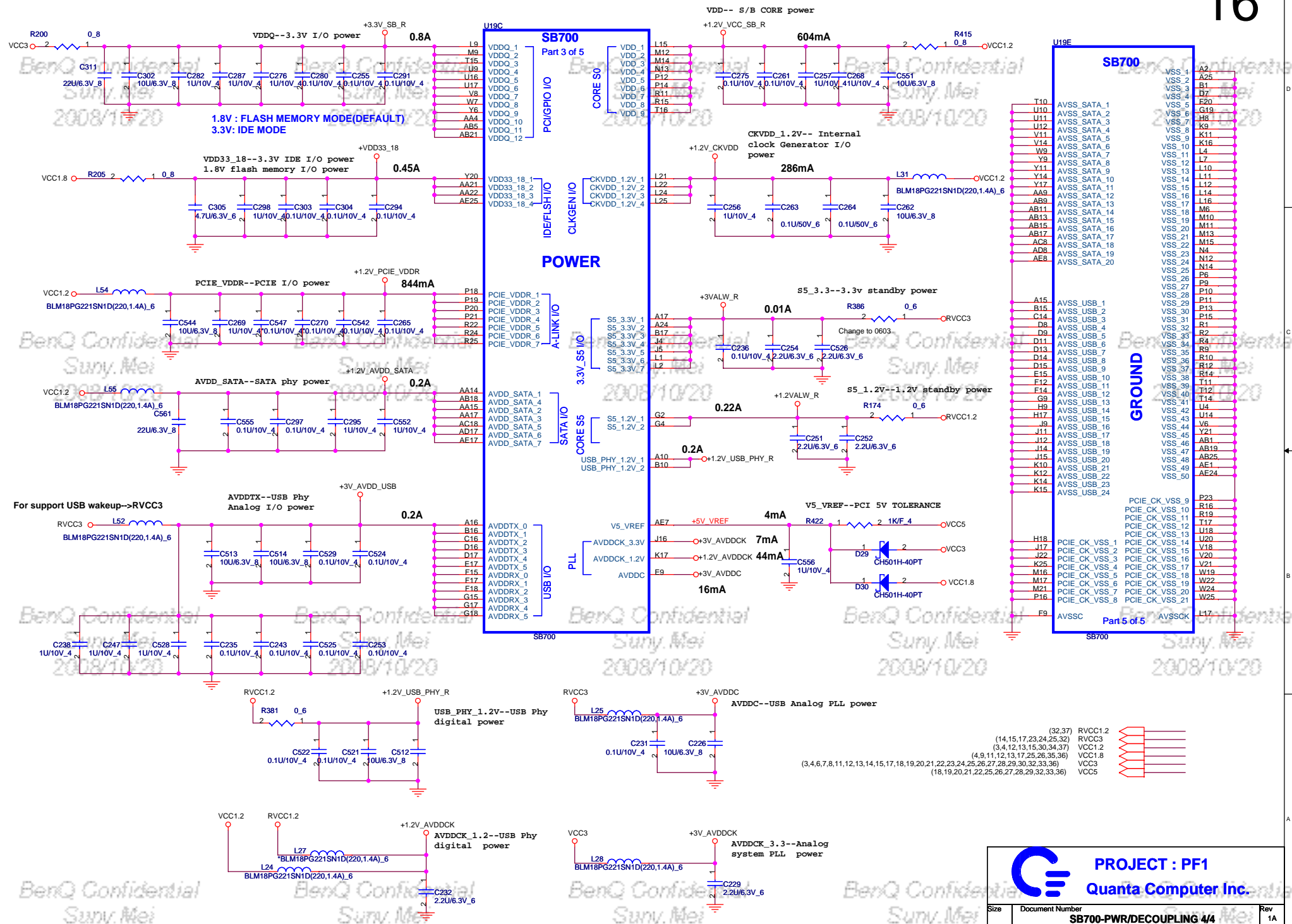
11/23 Board ID define MXM  
MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
15" UMA	x	x	0	0	0
15" M82	x	x	0	0	1
15" M86	x	x	0	1	1
17" UMA	x	x	1	0	0
17" M82	x	x	1	0	1
17" M86	x	x	1	1	1



**PROJECT : PF1**  
**Quanta Computer Inc.**

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

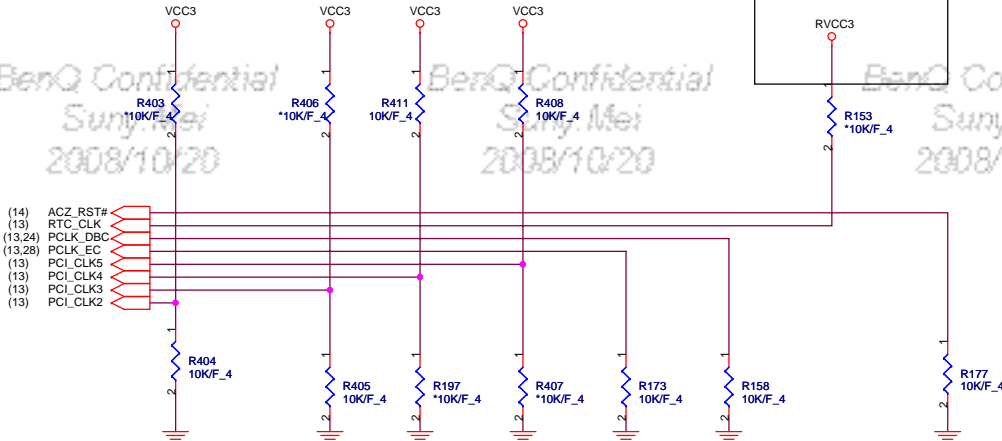


**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>SB700-PWR/DECOUPLING 4/4</b>	<b>1A</b>
Date:	Wednesday, June 11, 2008	Sheet 16 of 40

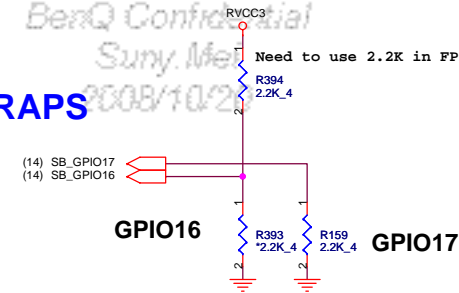


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



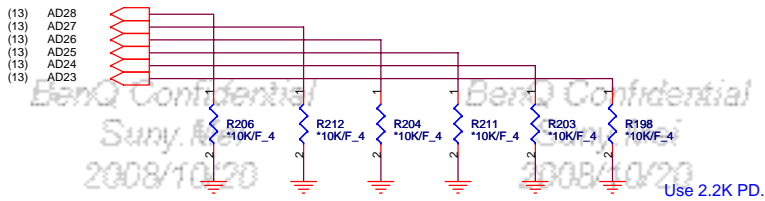
### REQUIRED STRAPS

	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

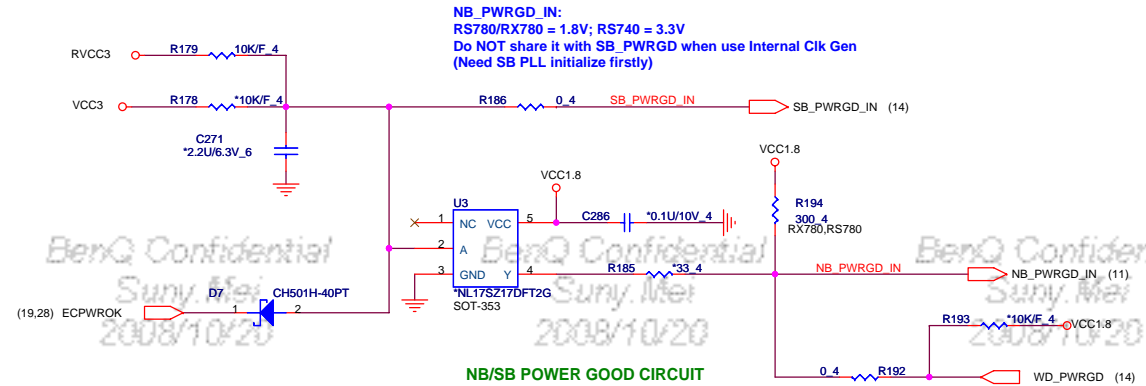


TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

### DEBUG STRAPS SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



NB\_PWRGD\_IN:  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen  
(Need SB PLL initialize firstly)

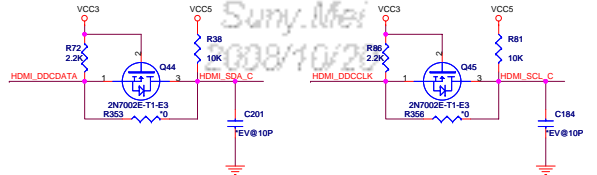
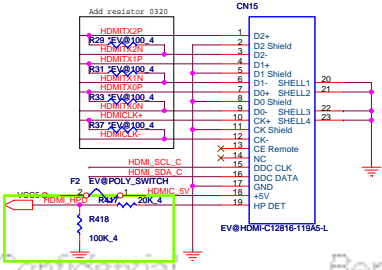
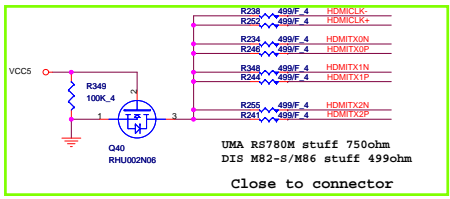
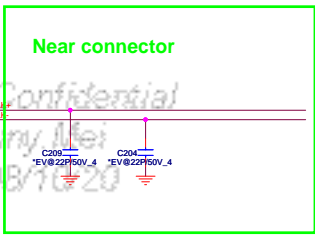
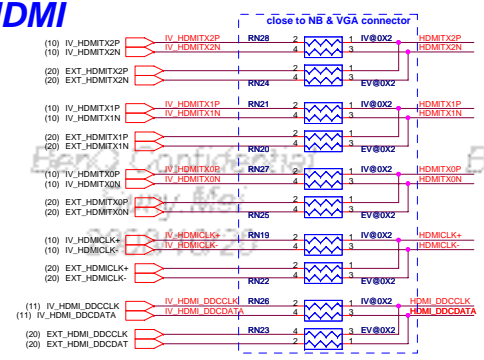
	U11	R230	R229	R245	R234
RX780	V	V	V	X	X
RS780M					

AL17SZ17000	IC (5P) NL175Z17DFT2G (SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR (SOT23-5)	SOT23-5

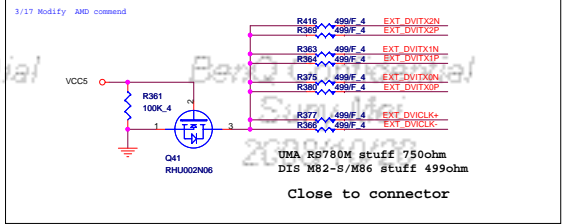
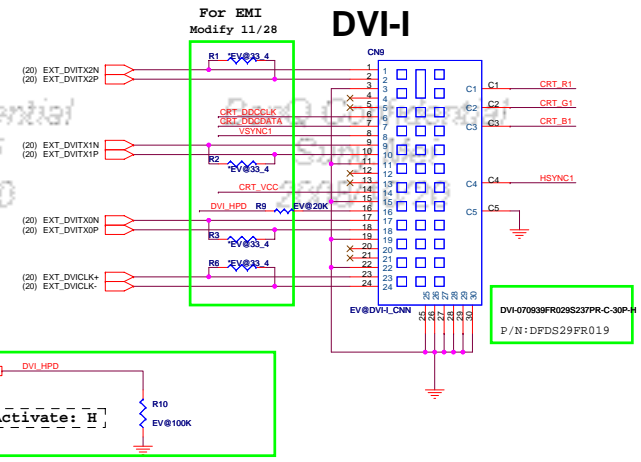


PROJECT : PF1  
Quanta Computer Inc.

HDMI

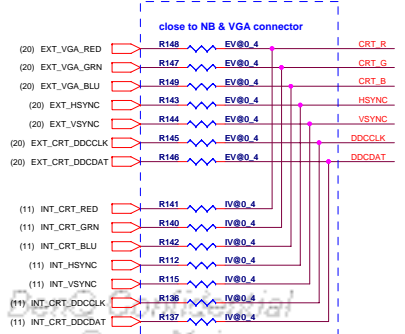
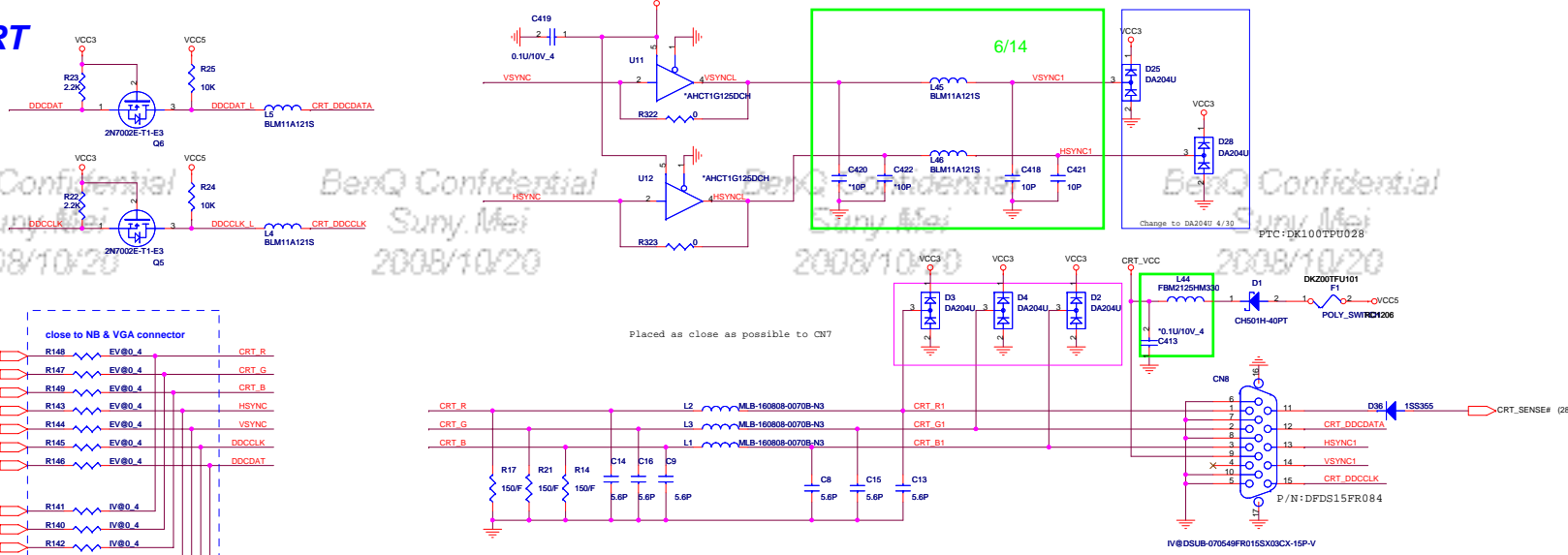


DVI



18

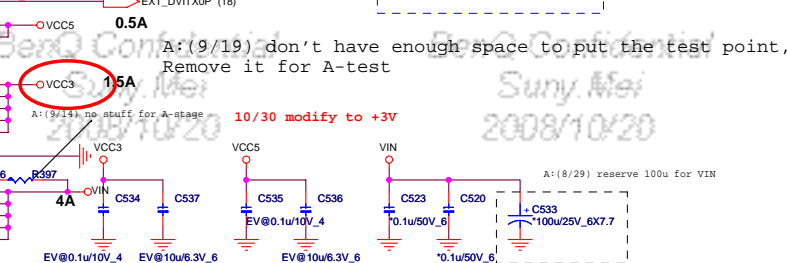
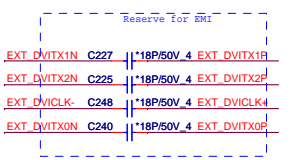
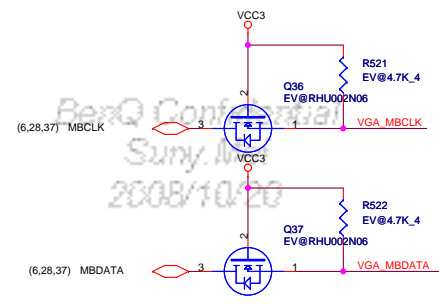
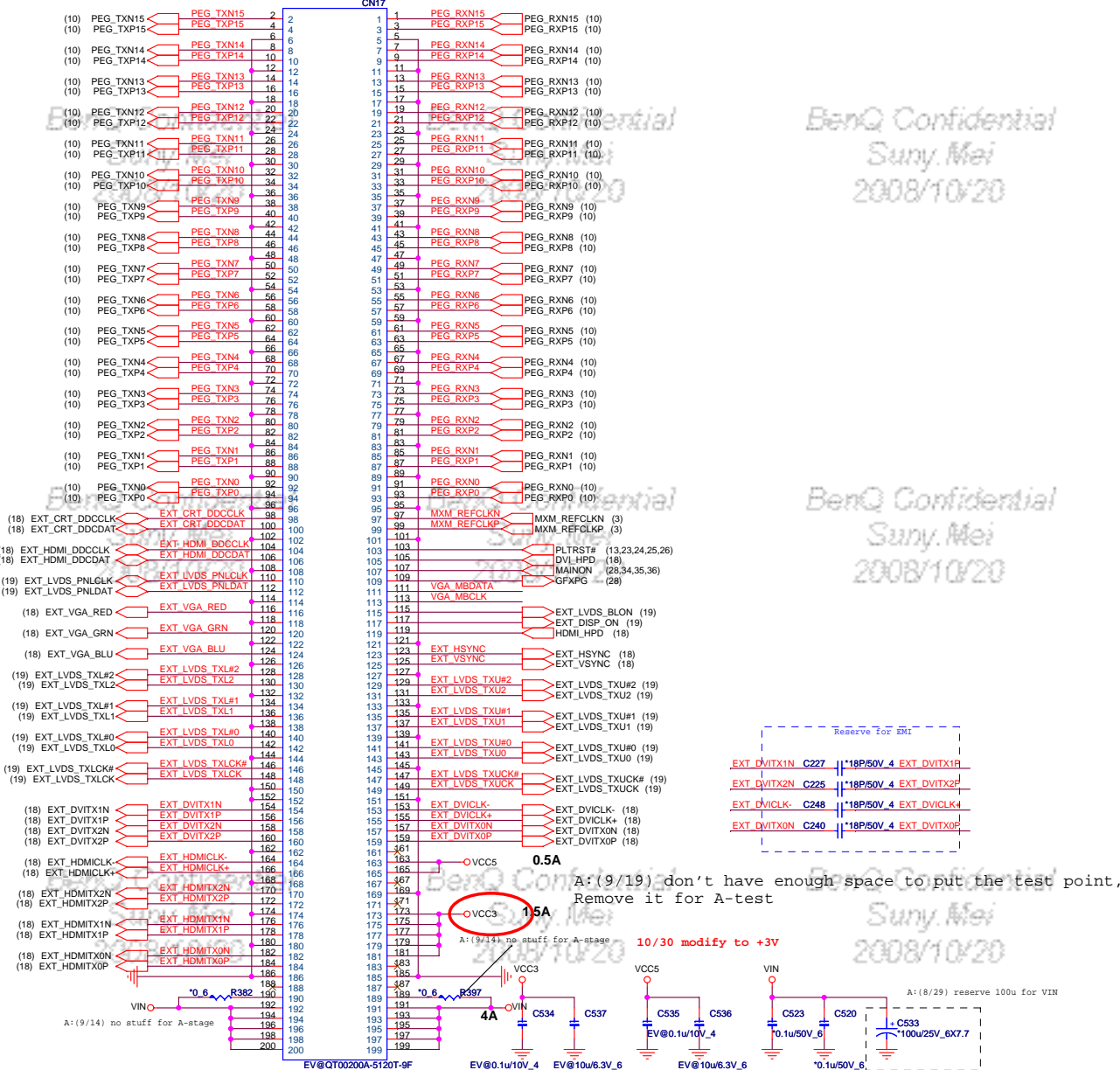
CRT PORT



PROJECT : PF1  
Quanta Computer Inc.  
Date: Wednesday, June 11, 2008 Sheet 18 of 40



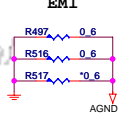
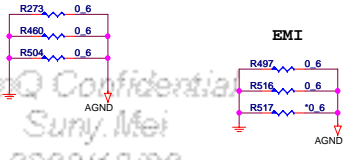
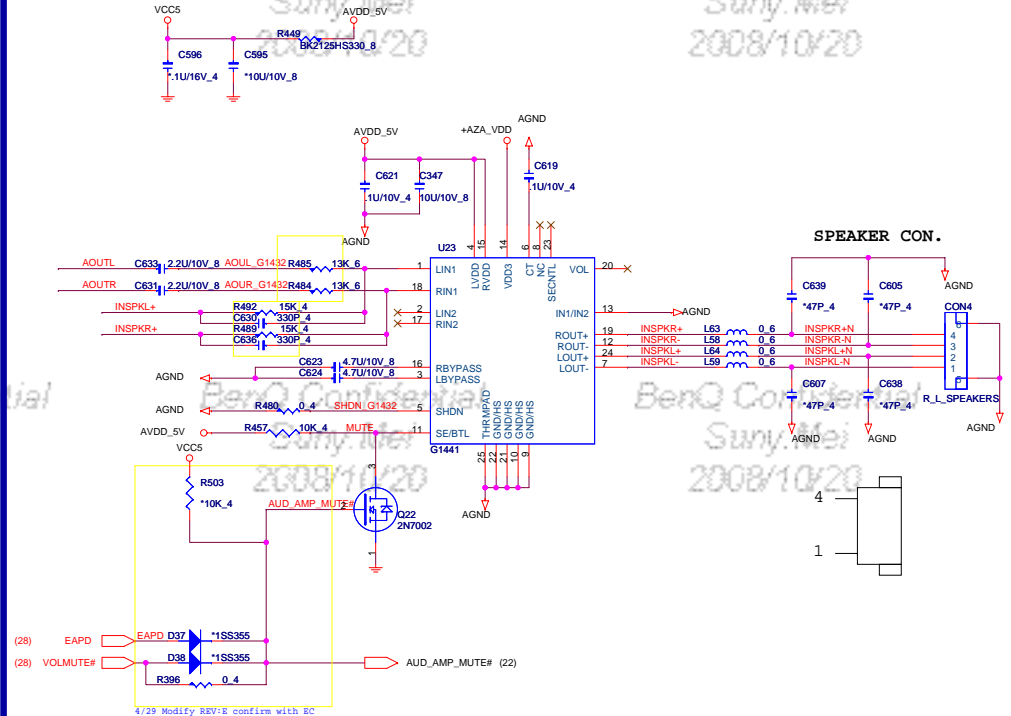
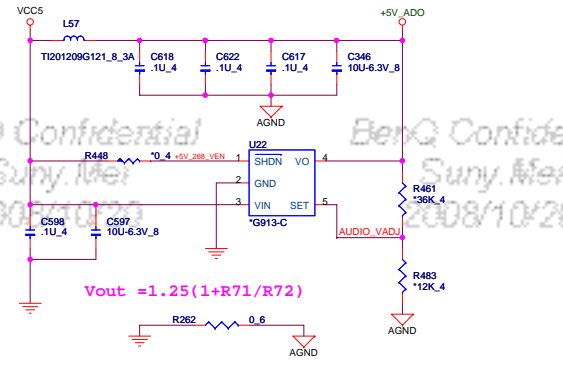
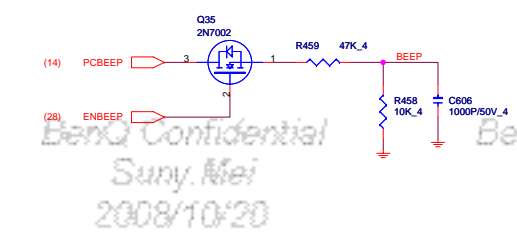
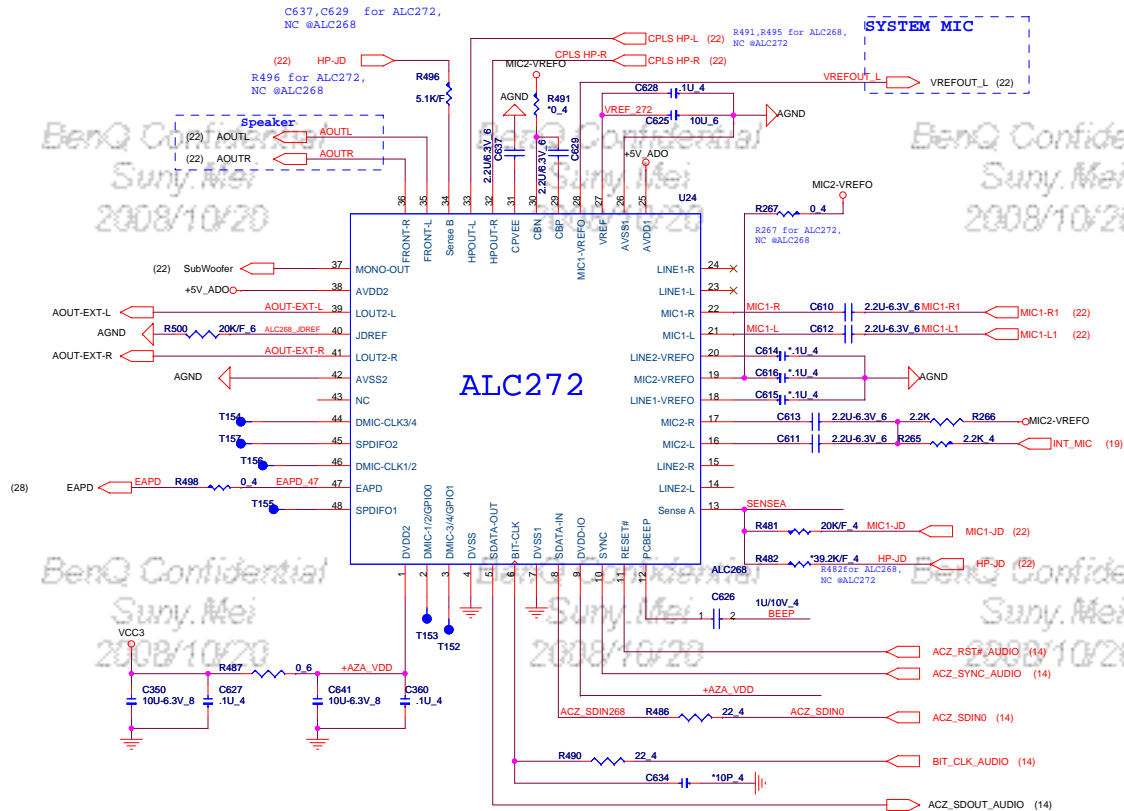
A:(8/18) update VGA conn footprint base on allan information  
A:(8/23) update vga conn pin-define (change pin 1 location)



**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>MXM CONNECTOR / TV</b>	2A
Date:	Wednesday, June 11, 2008	Sheet 20 of 40

Codec (ALC272)



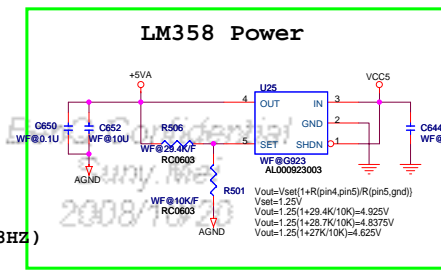
**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>ALC272/AMP</b>	<b>2A</b>
Date:	Wednesday, June 11, 2008	Sheet 21 of 40

Subwoofer

BenQ Confidential  
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Sunny Mei  
2008/10/20

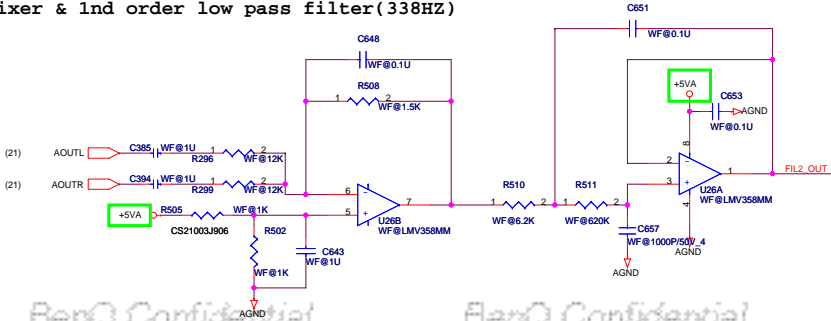


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Sunny Mei  
2008/10/20

Mixer & 1nd order low pass filter(338Hz)

2nd order low pass filter(338Hz)



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2008/10/20

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Sunny Mei  
2008/10/20

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Sunny Mei  
2008/10/20

BenQ Confidential  
Sunny Mei  
2008/10/20

HP

BenQ Confidential  
Sunny Mei  
2008/10/20

BenQ Confidential  
Sunny Mei  
2008/10/20

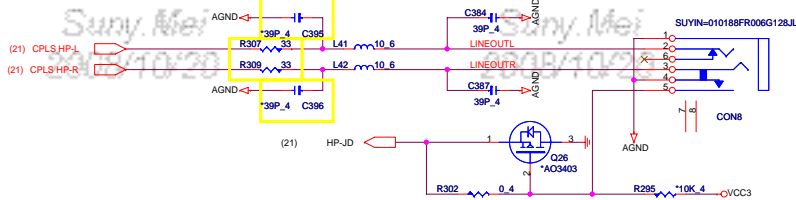
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2008/10/20

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Sunny Mei  
2008/10/20

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2008/10/20

Normal Open Jack

HEADPHONE



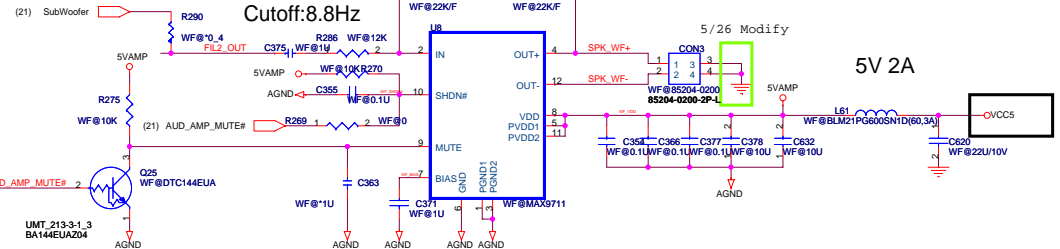
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Sunny Mei  
2008/10/20

BenQ Confidential  
Sunny Mei  
2008/10/20

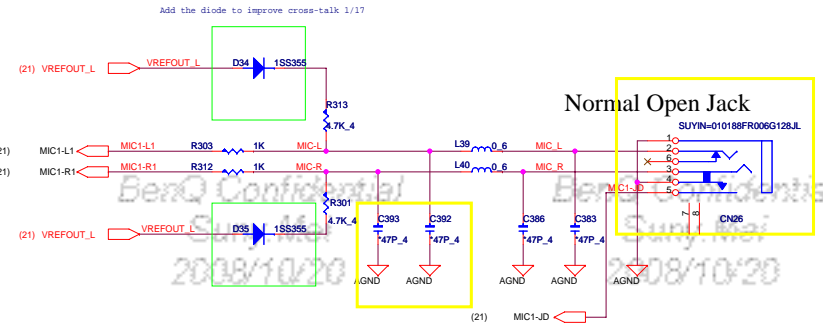
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2008/10/20

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Sunny Mei  
2008/10/20

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Sunny Mei  
2008/10/20



SYSTEM MIC



LAN\_REALTEK\_RTL8102E

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Sunny.Mei  
2008/10/20

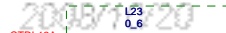
BenQ Confidential  
Sunny.Mei  
2008/10/20

BenQ Confidential  
Sunny.Mei  
2008/10/20

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Sunny.Mei  
2008/10/20

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For RTL8102EL, use this block.



Change L51 to 0 ohm in RTL8102EL application.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



Remove R1 & R2 in RTL8102EL application.

\* C469 and C192 are for U2 EVDD12 pin 19.



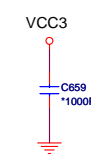
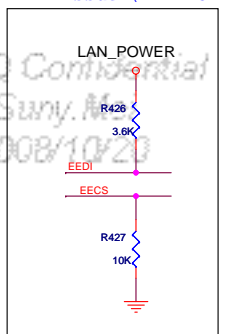
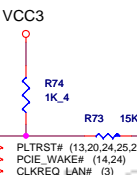
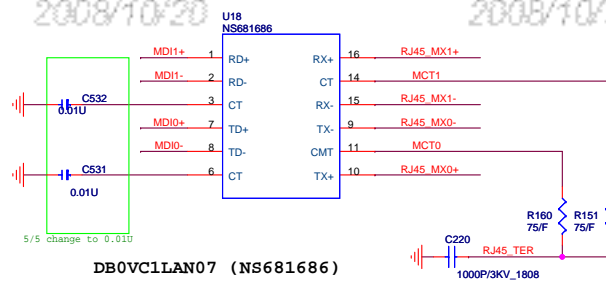
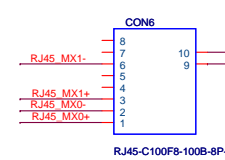
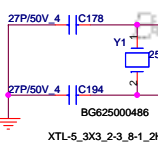
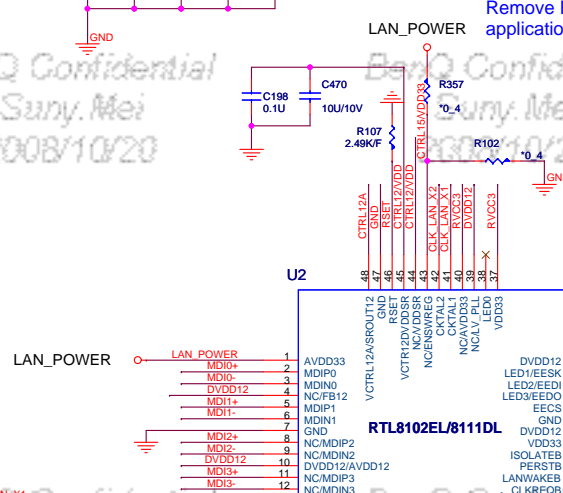
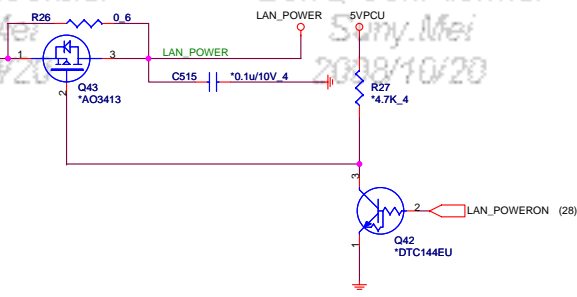
Charge to 1U



Remove R357 and R102 in RTL8102EL application.

Fix PXE issue (ADD for B+)

LAN POWER CONTROL



PROJECT : PF1  
Quanta Computer Inc.  
Size: Document Number  
LAN\_REALTEK\_RTL8102EL  
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Rev 2A

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2008/10/20

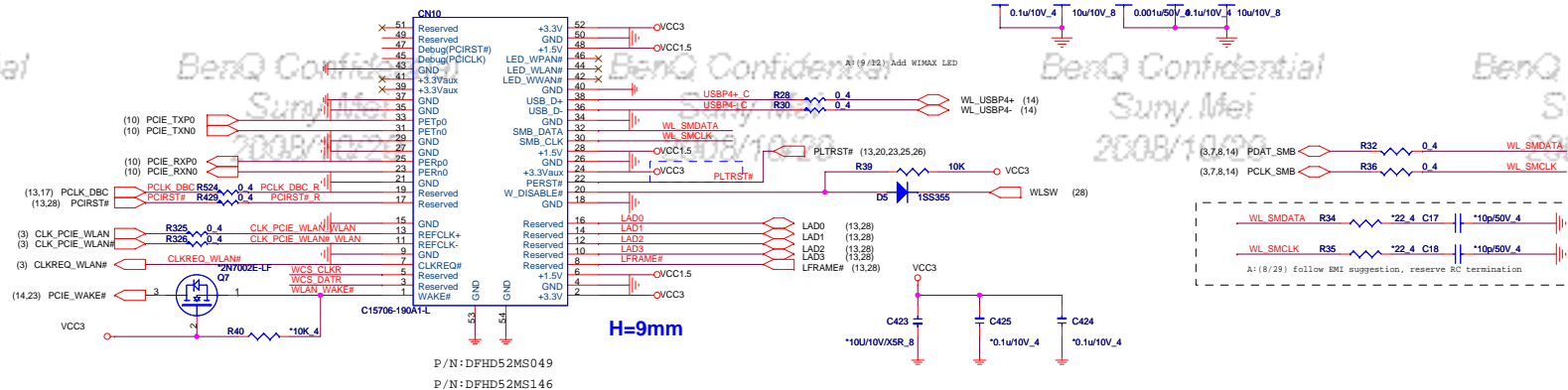
BenQ Confidential  
Sunny.Mei  
2008/10/20

BenQ Confidential  
Sunny.Mei  
2008/10/20

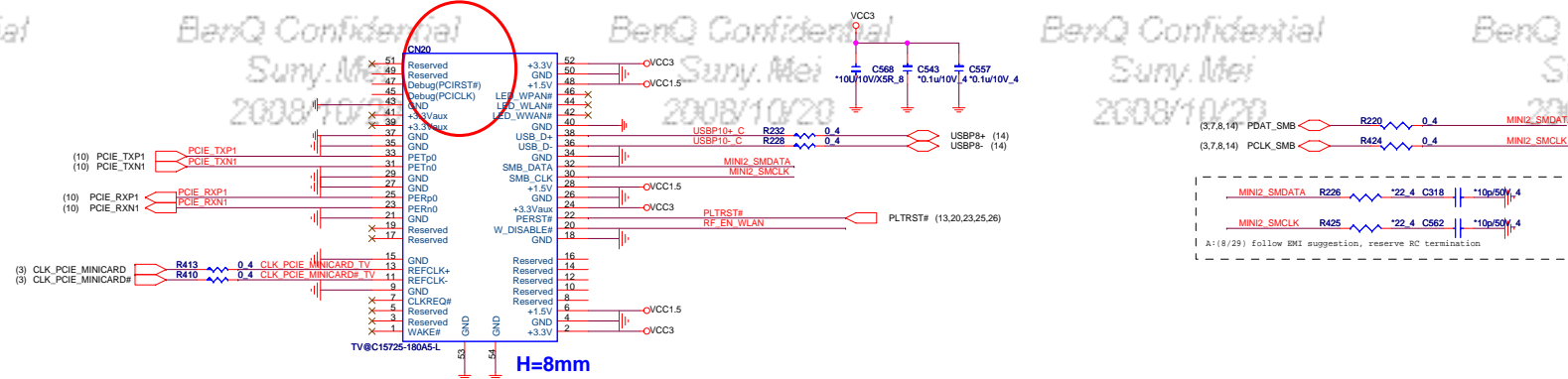
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2008/10/20

MINI-Card I (WLAN)



MINI-Card II (TV)



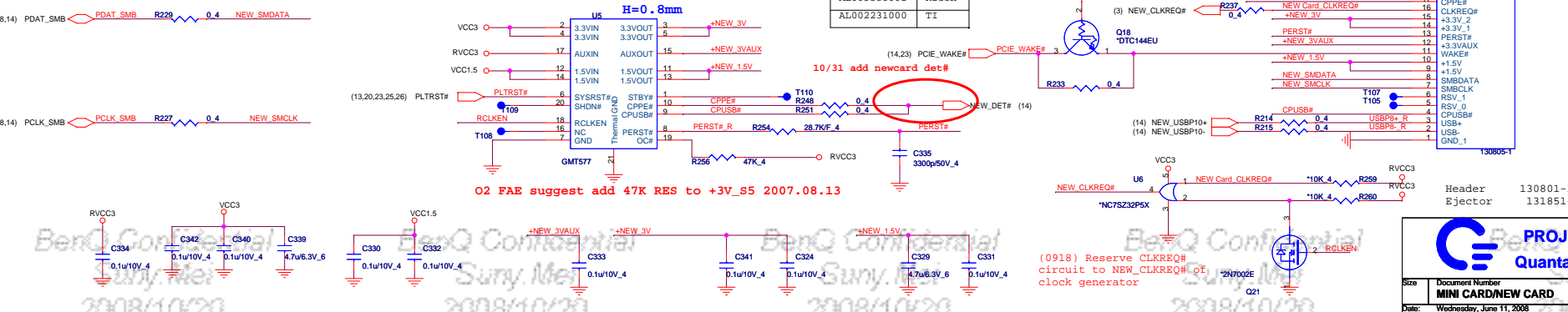
A: (9/7) per TI FAE suggestion:  
 (1) Please keep all Input and Output capacitor value > 4.8uF (0.1uF +4.7uF)  
 (2) Please put these caps closed to IC  
 (3) R4101(pin 19,OCN) value should change to 2k ohm.

**NEW CARD'S POWER SWITCH**

CPPE# : (Internal Pull Up, active low when card support PCIE)  
 CPUSB# : (Internal Pull Up, active low when card support USB)  
 SHDN# : (Internal Pull Up)

New Card's Power Switch

OCII_PN	Vendor
AL000577001	GMT
AL027C10003	OMC
AL005538001	Ricoh
AL002231000	TI



**PROJECT: PF1**  
**Quanta Computer Inc.**

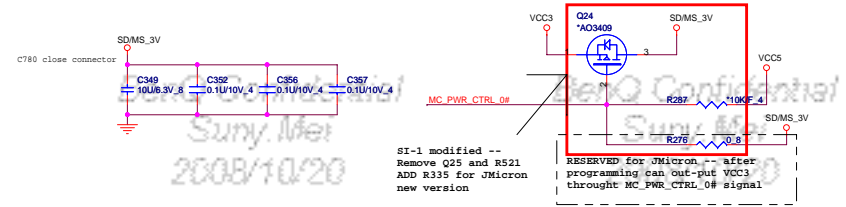
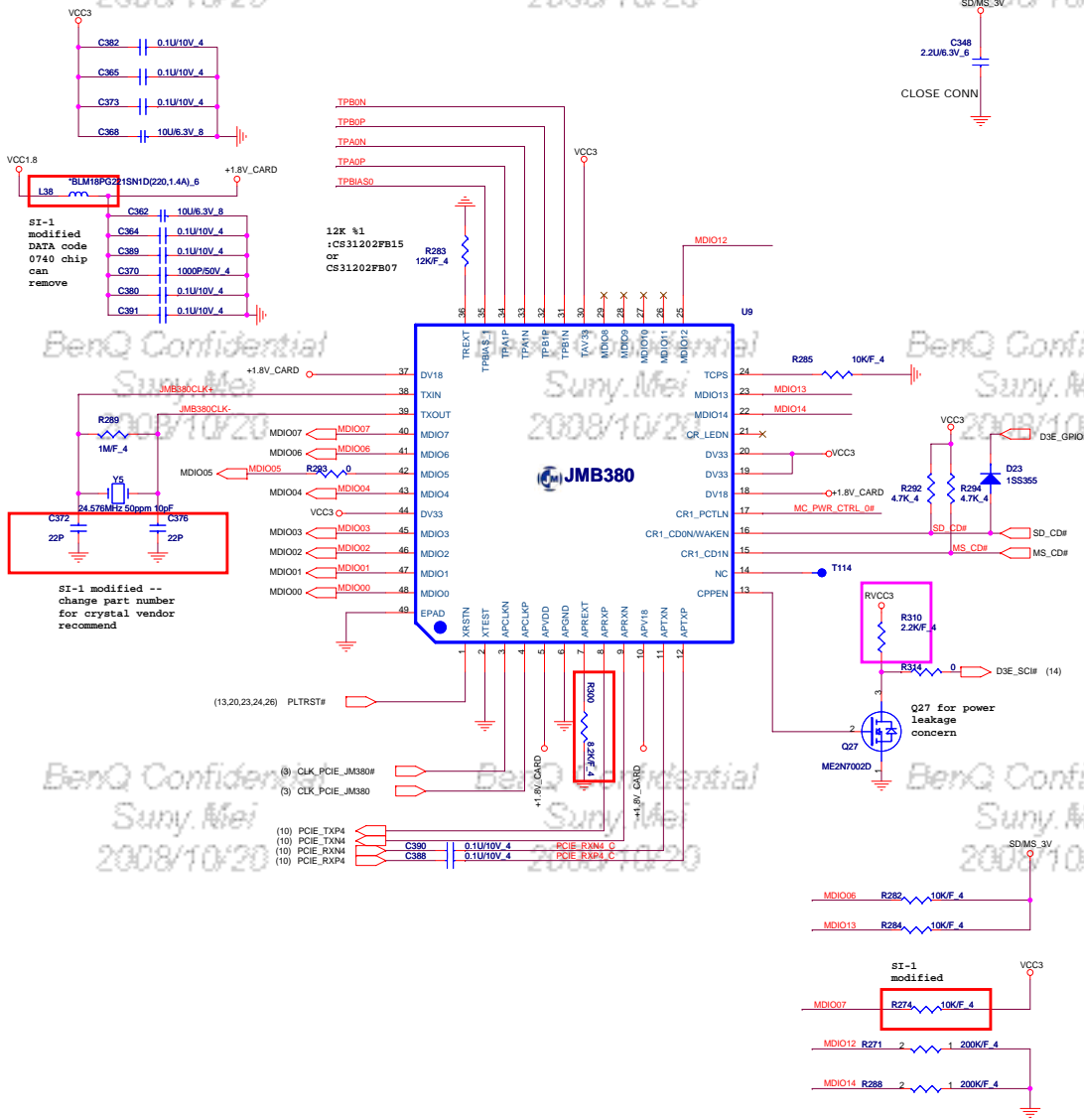
Header: 130801-1, DFHD26MR074  
 Ejector: 131851-V, FBBL5001010

Size: Document Number: MINI CARD/NEW CARD, Rev: 2A  
 Date: Wednesday, June 11, 2008, Sheet: 24 of 40

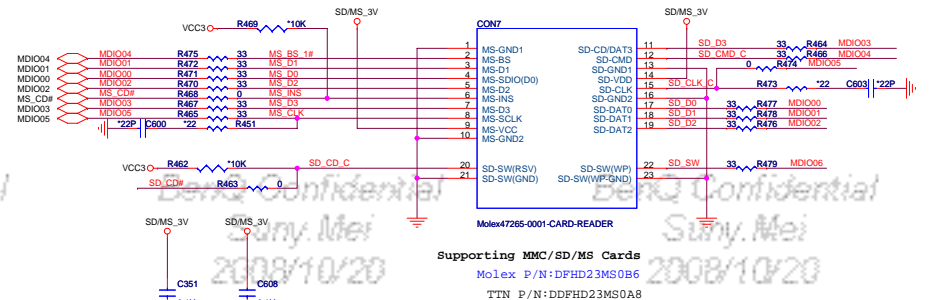
BenQ Confidential  
Sunny Mei  
2008/10/20

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Sunny Mei  
2008/10/20

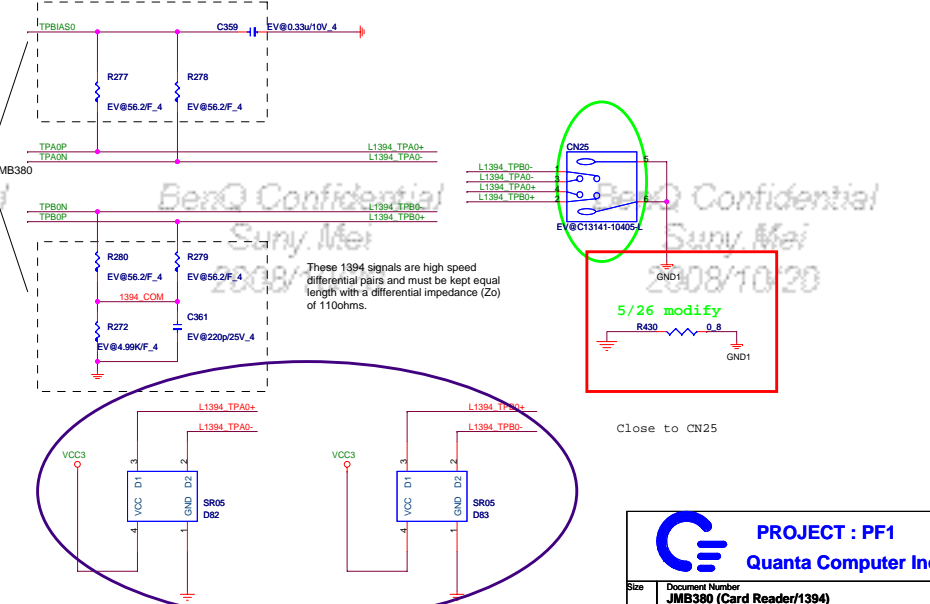
BenQ Confidential  
Sunny Mei  
2008/10/20

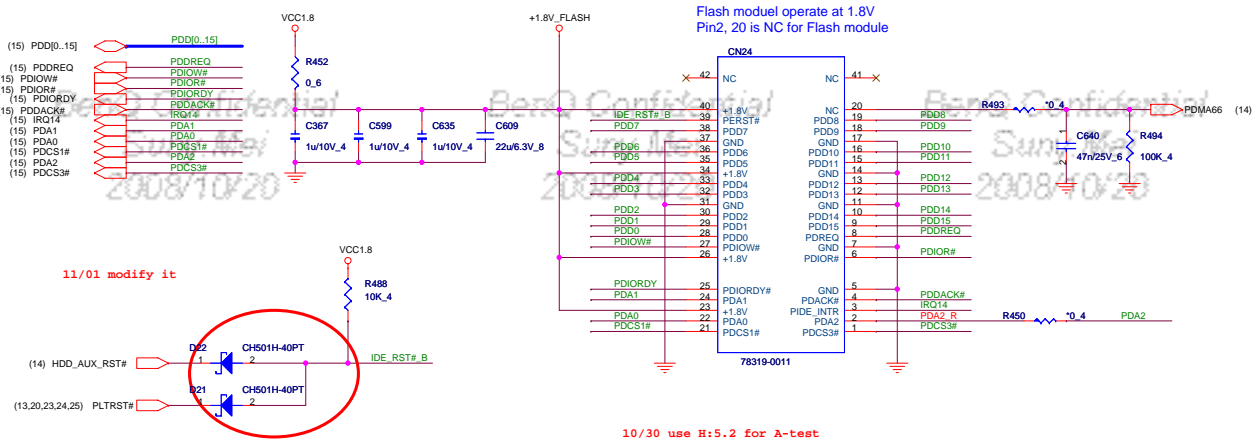


4 IN 1 CONN



1394



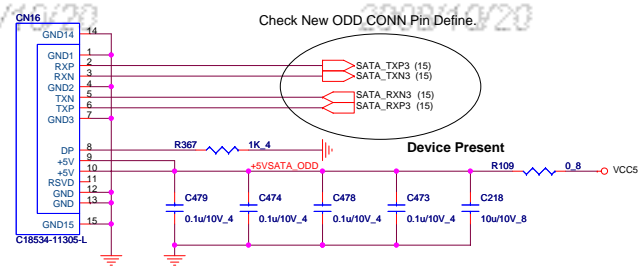


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SATA ODD

9/28 change to SATA ODD conn to BD3G use



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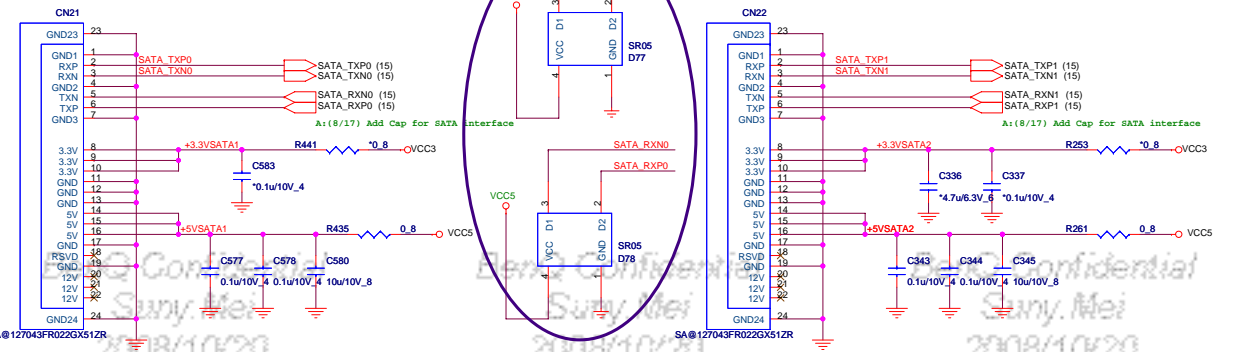
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SATA HDD

2'nd SATA HDD



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**Quanta Computer Inc.**

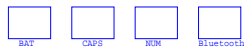
Size	Document Number	Rev
	SATA / HyberFLASH	2A
Date:	Wednesday, June 11, 2008	Sheet 26 of 40

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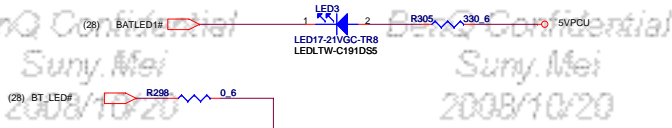




LED



BATTERY CHARGE LED



ODD/HDD LED



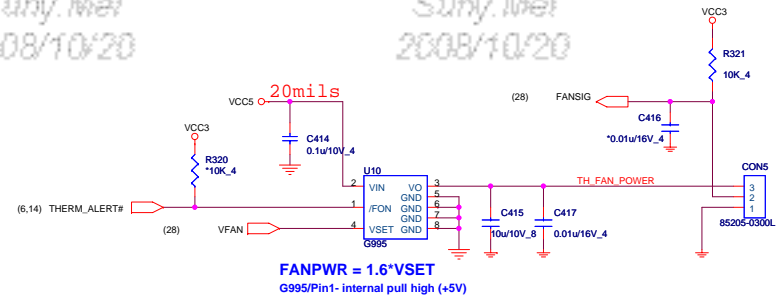
CAPS LED



Number Lock LED



CPU FAN



FANPWR = 1.6\*VSET  
G995/Pin1- internal pull high (+5V)

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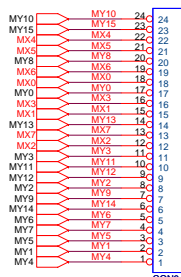
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Keyboard CONN



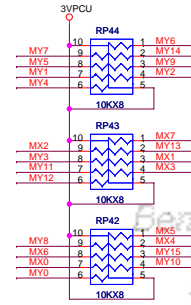
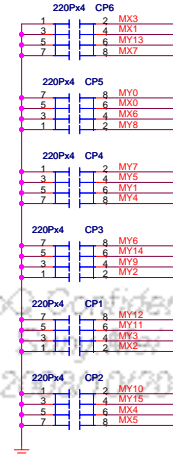
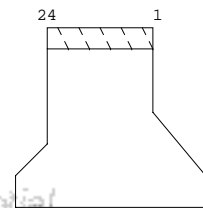
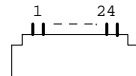
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2008/10/20



P/N:DFFC24FR181

Bot contact



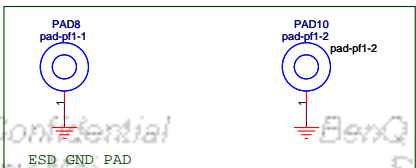
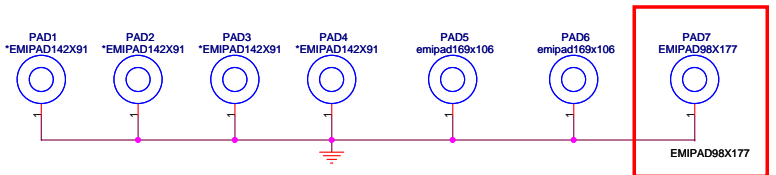
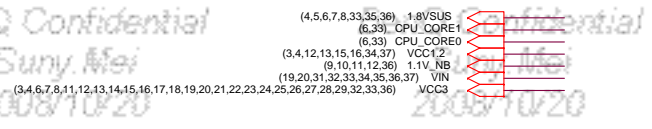
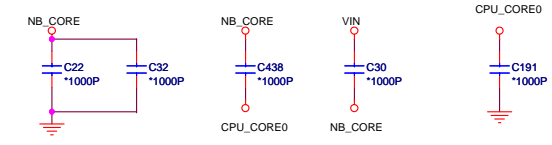
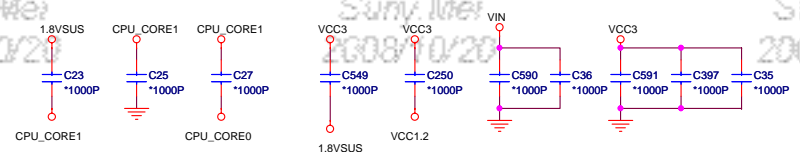
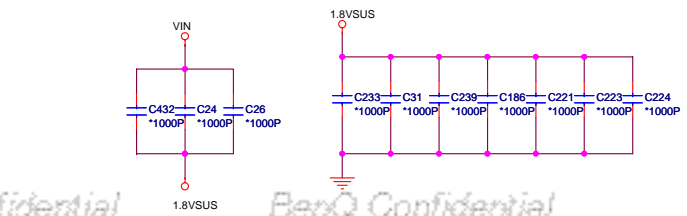
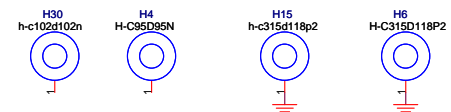
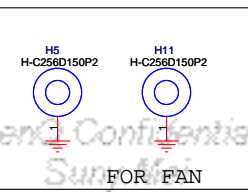
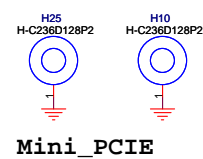
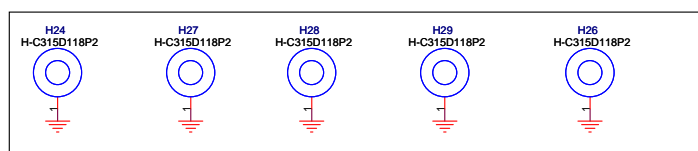
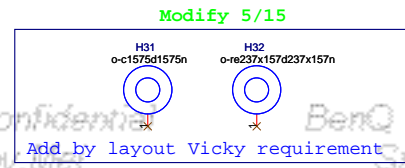
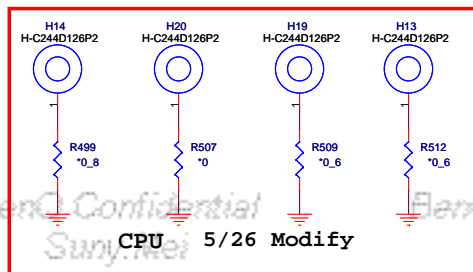
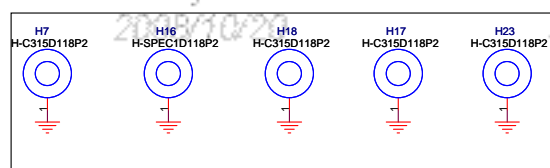
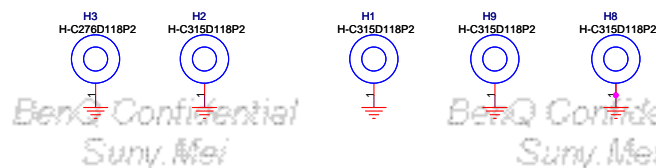
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2008/10/20

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Sunny Mei  
2008/10/20

BenQ Confidential  
Sunny Mei  
2008/10/20

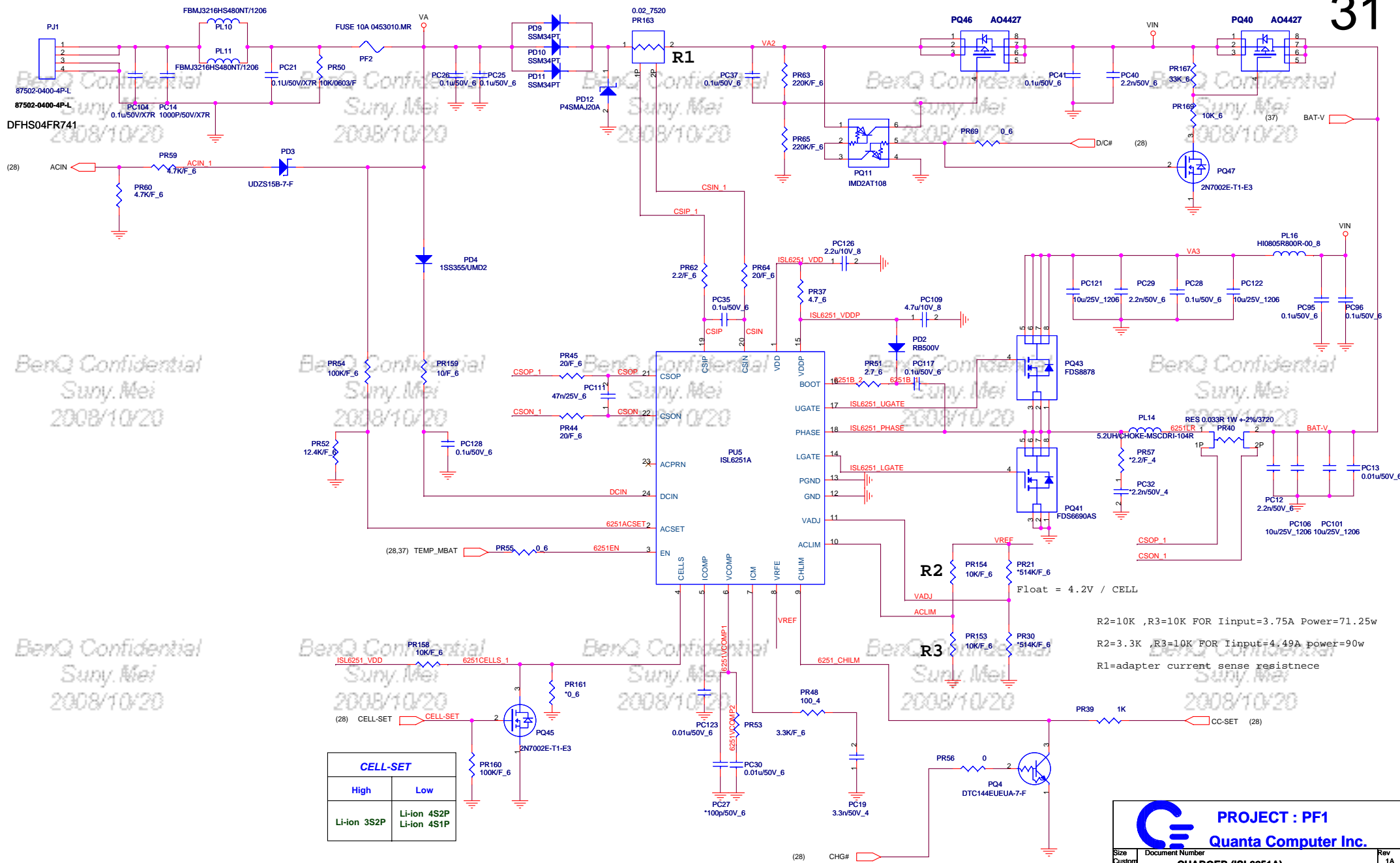
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Sunny Mei  
2008/10/20

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Sunny Mei  
2008/10/20



PROJECT : PF1  
Quanta Computer Inc.

Size	Document Number	Rev
	HOLE/EMI CAP/ESD PAD	2A
Date:	Wednesday, June 11, 2008	Sheet 30 of 40

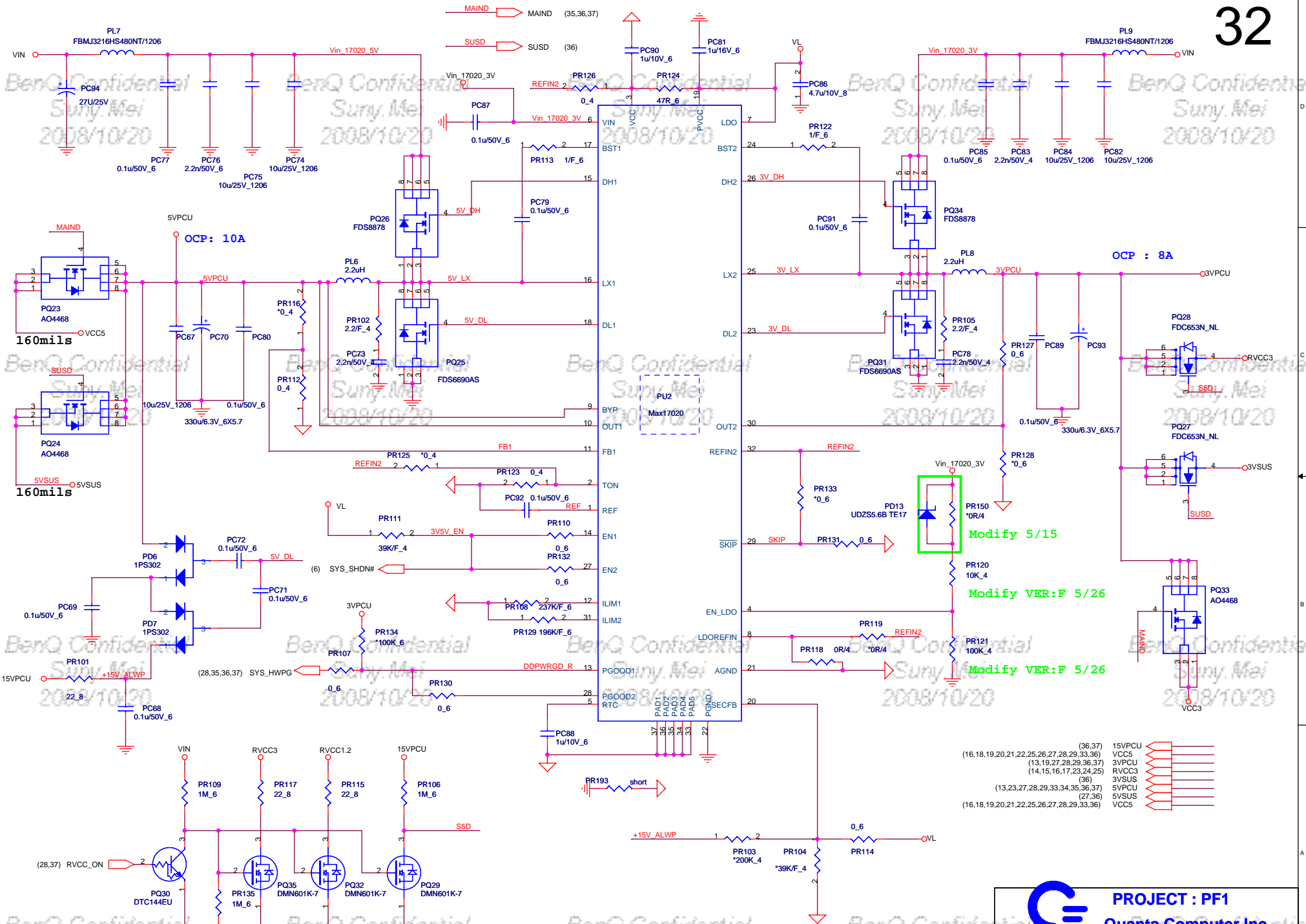


CELL-SET	
High	Low
Li-Ion 3S2P	Li-ion 4S2P Li-ion 4S1P

Float = 4.2V / CELL  
 R2=10K ,R3=10K FOR Iinput=3.75A Power=71.25w  
 R2=3.3K ,R3=10K FOR Iinput=4.49A power=90w  
 R1=adapter current sense resistence

**PROJECT : PF1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>CHARGER (ISL6251A)</b>	1A
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- (36,37) 15VPCU
- (16,18,19,20,21,22,25,26,27,28,29,33,36) VCC5
- (13,19,27,28,29,36,37) 3VPCU
- (14,15,16,17,23,24,25) RVCC3
- (36) 3VSUS
- (13,23,27,28,29,33,34,35,36,37) 5VPCU
- (27,36) 5VSUS
- (16,18,19,20,21,22,25,26,27,28,29,33,36) VCC5

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Size	Document Number	Rev
	<b>SYSTEM 5V/3V (ISL6237)</b>	<b>1A</b>
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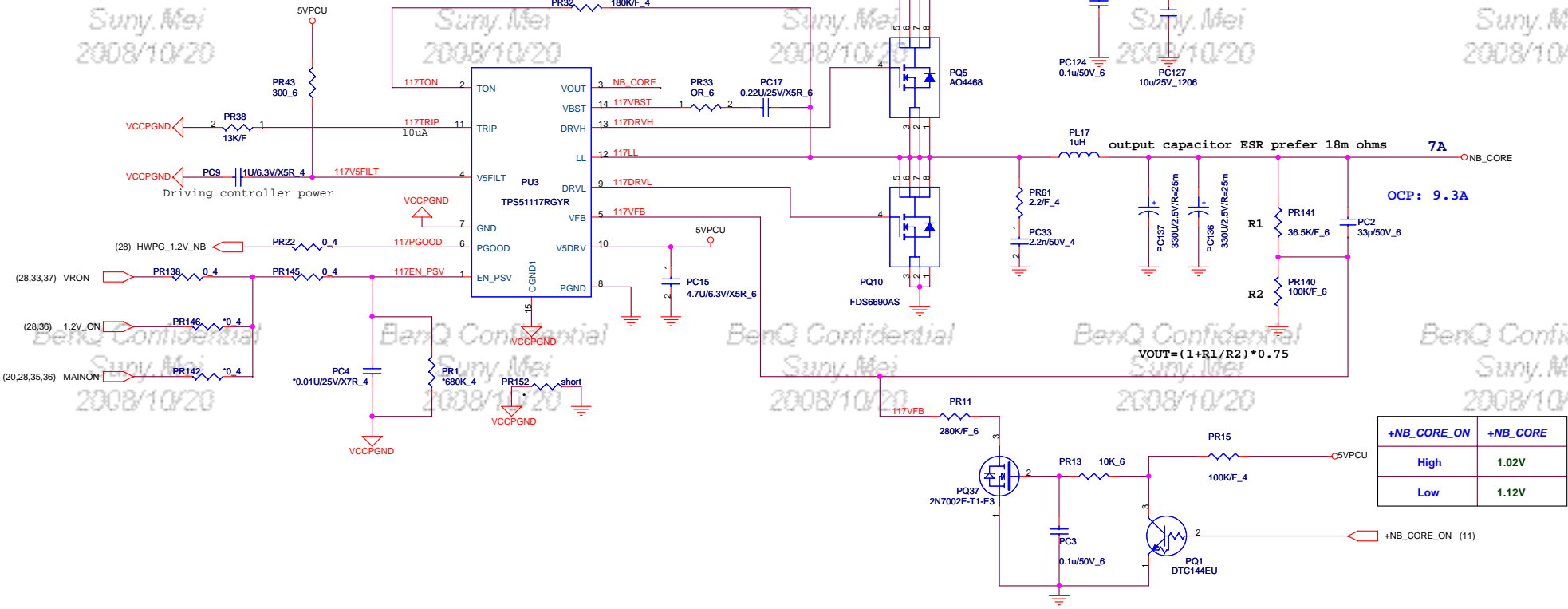
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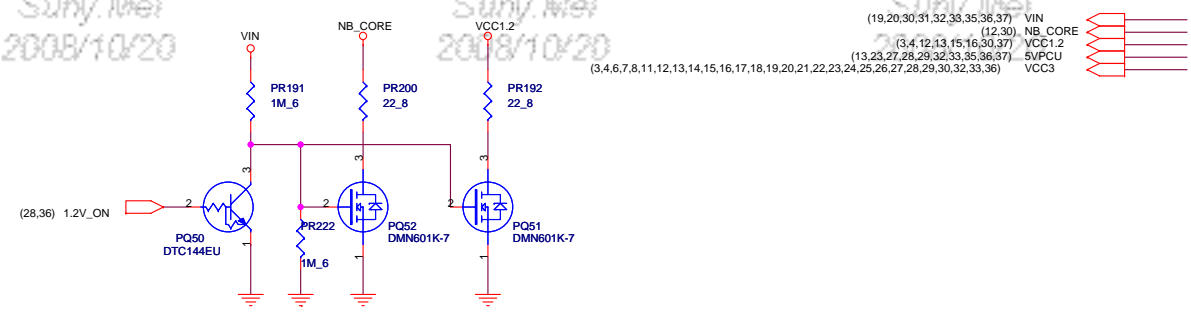
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	<b>NB_VCC (RT8202)</b>	1A
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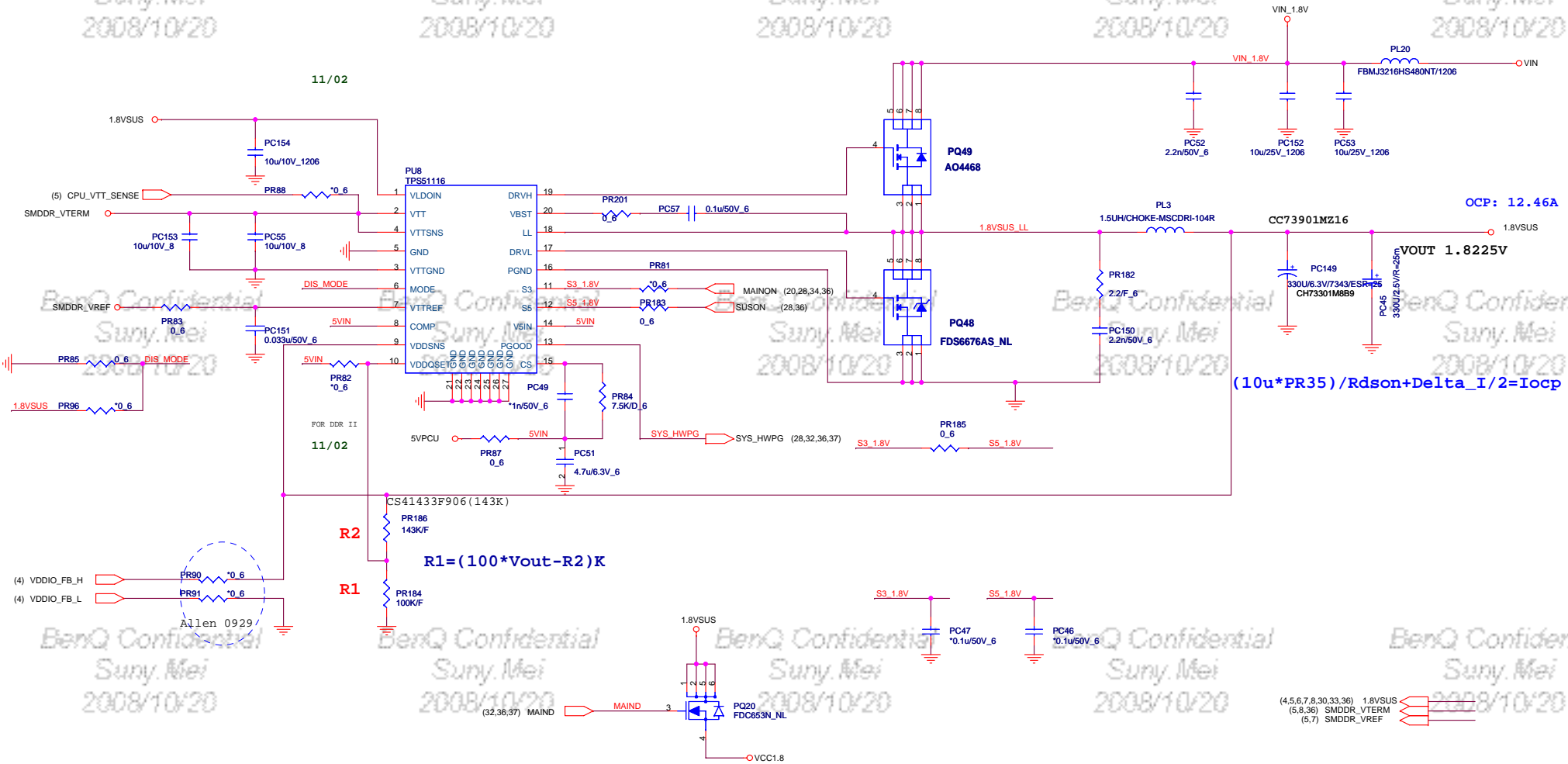
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11/02



$R1 = (100 * V_{out} - R2) K$

$(10u * PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$

(4,5,6,7,8,30,33,36) 1.8VSUS  
(5,8,36) SMDDR\_VTERM  
(5,7) SMDDR\_VREF

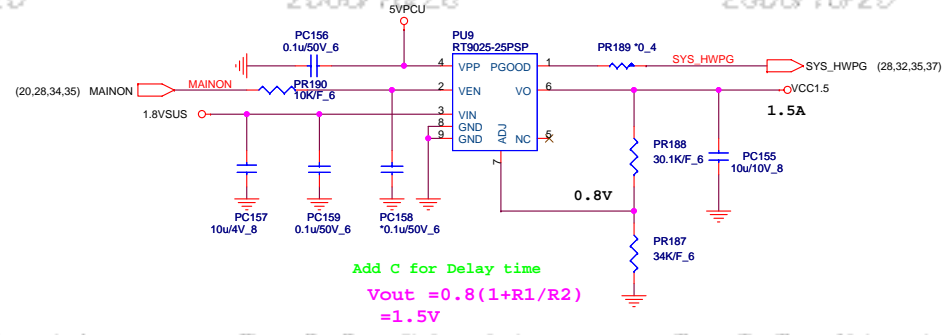
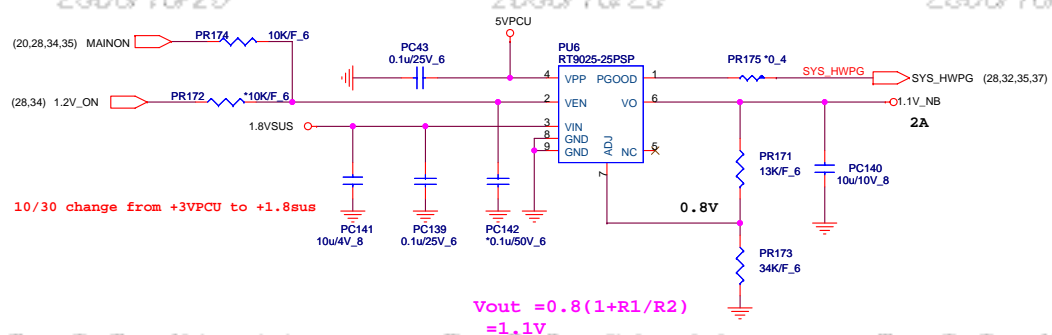
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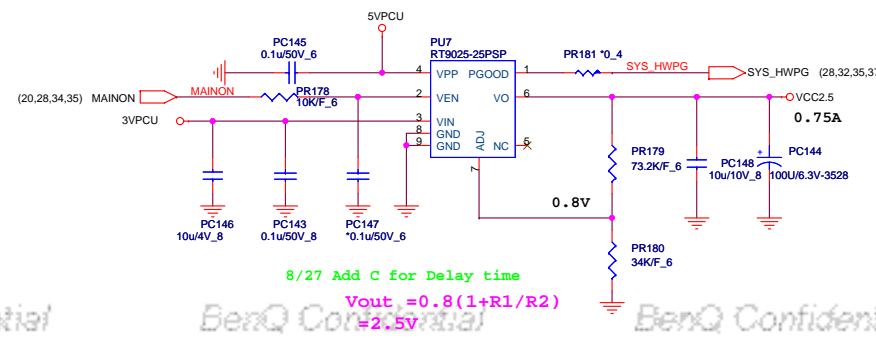
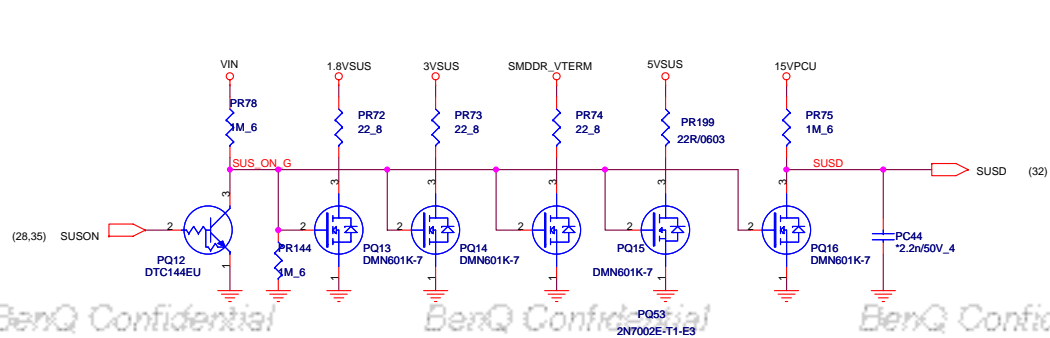
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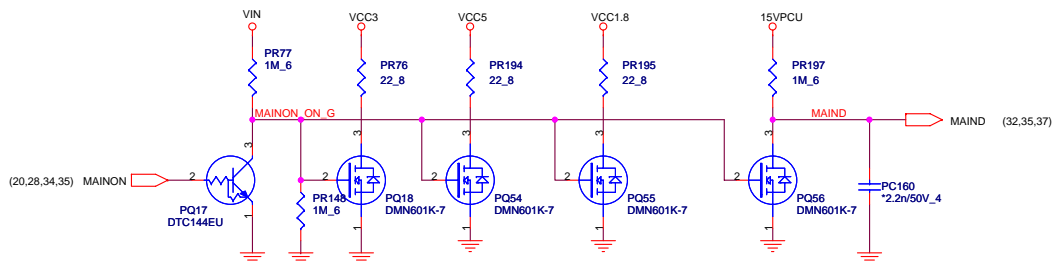
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- (24) VCC1.5
- (4) VCC2.5
- (9,10,11,12) 1.1V\_NB

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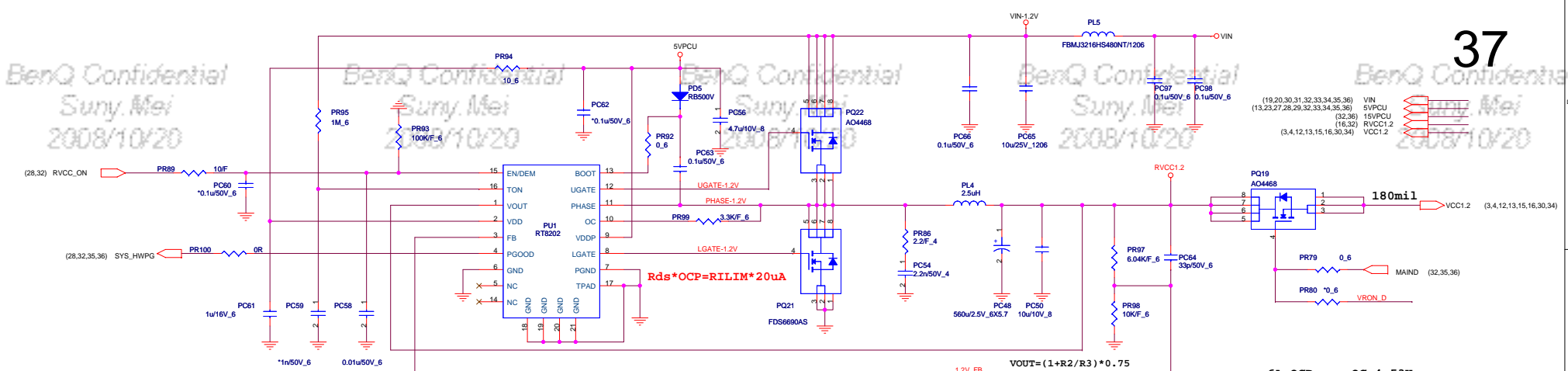
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**Discharge (1.25V/1.5V)**

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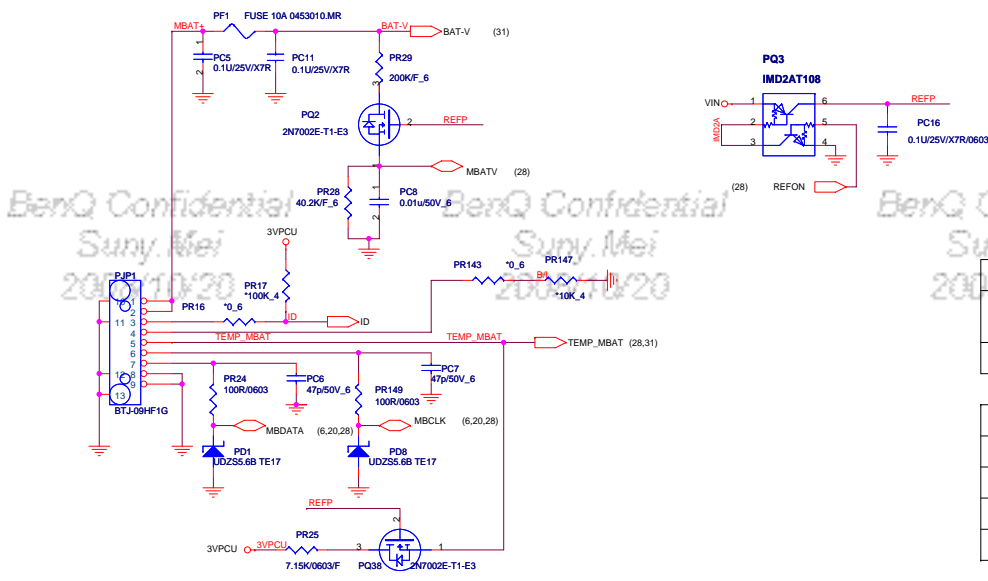
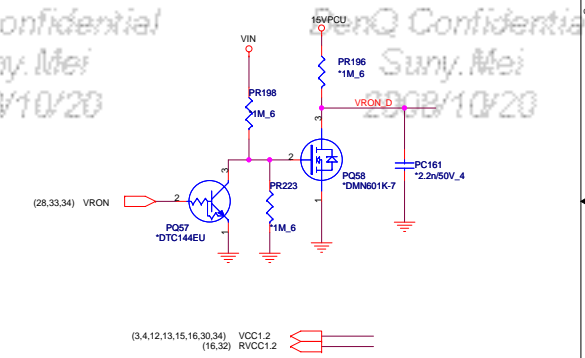
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TON=3.85p\*R<sub>TON</sub>\*V<sub>out</sub> / (V<sub>in</sub>-0.5)  
 Frequency=V<sub>out</sub> / (V<sub>in</sub>\*TON)

VOUT=(1+R2/R3)\*0.75

6A OCP --- OC=4.53K  
 FDS6690AS R<sub>ds</sub>=15mOhm



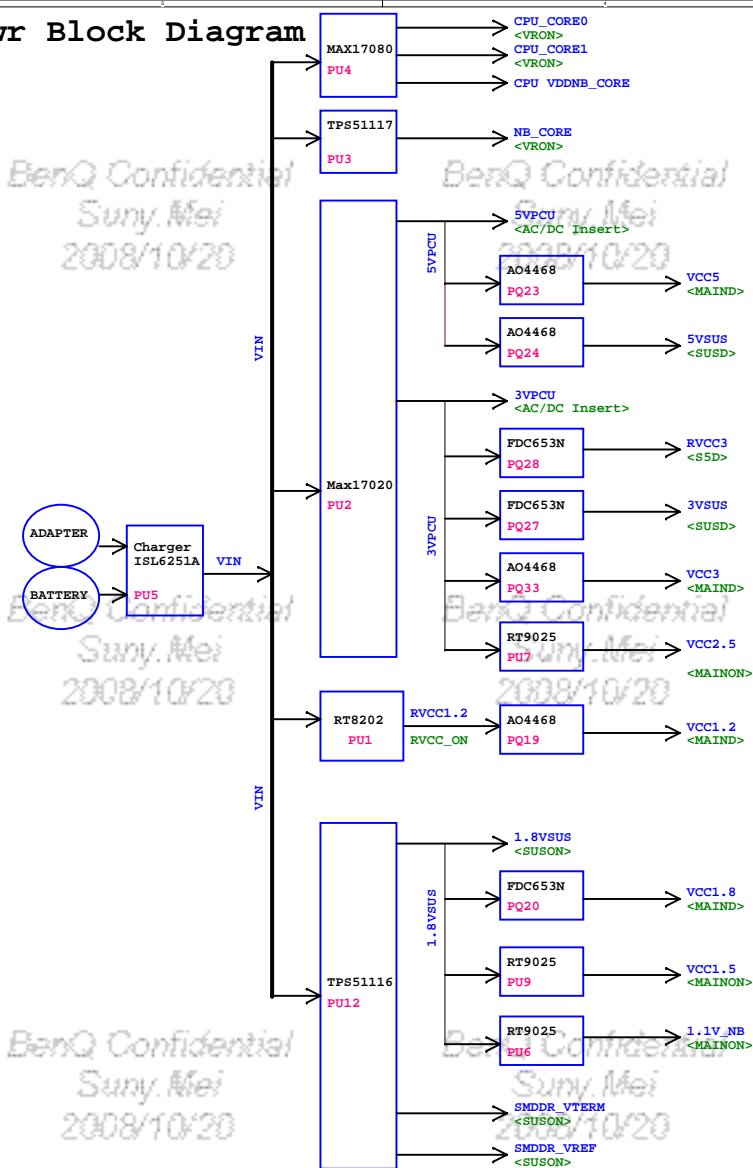
MBATV voltage :

Li-ion 4S*P	16.8V*40.2/(200+40.2) = 2.812V
	12.0V*40.2/(200+40.2) = 2.008V
Ni-MH 8S1P	8.0V*40.2/(200+40.2) = 1.34V

TEMP\_MBAT voltage :

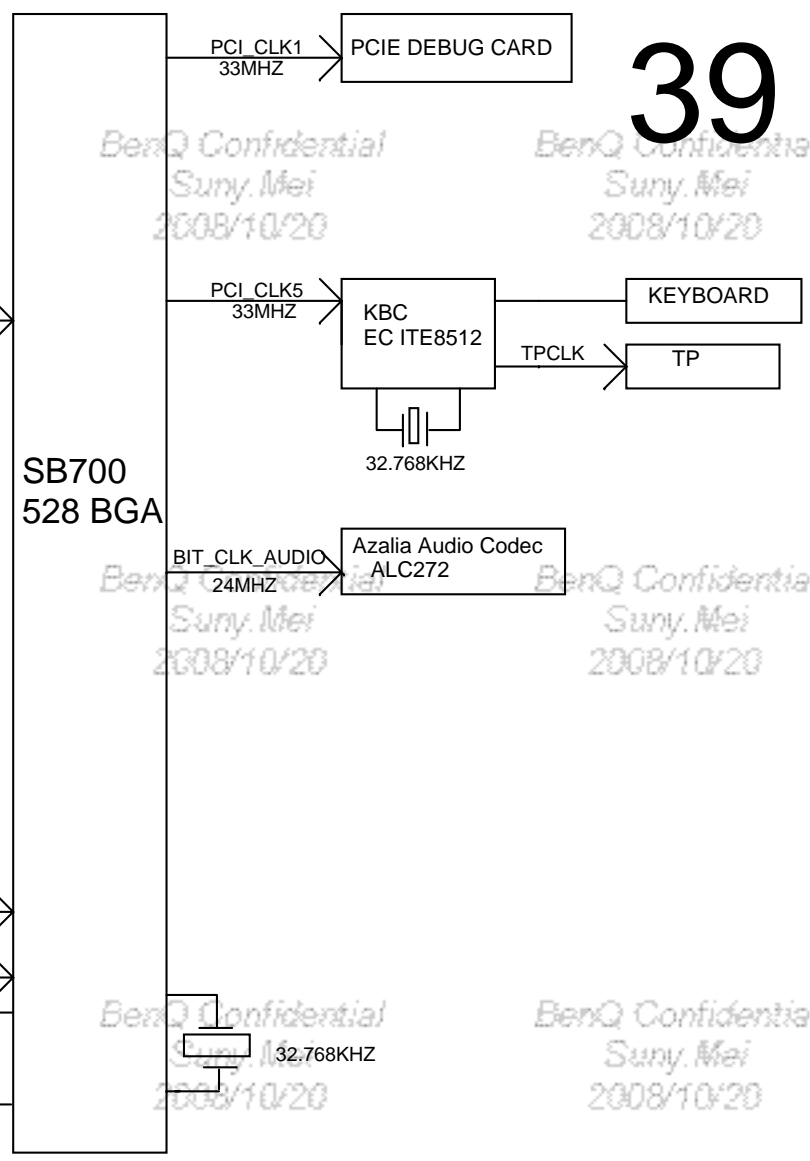
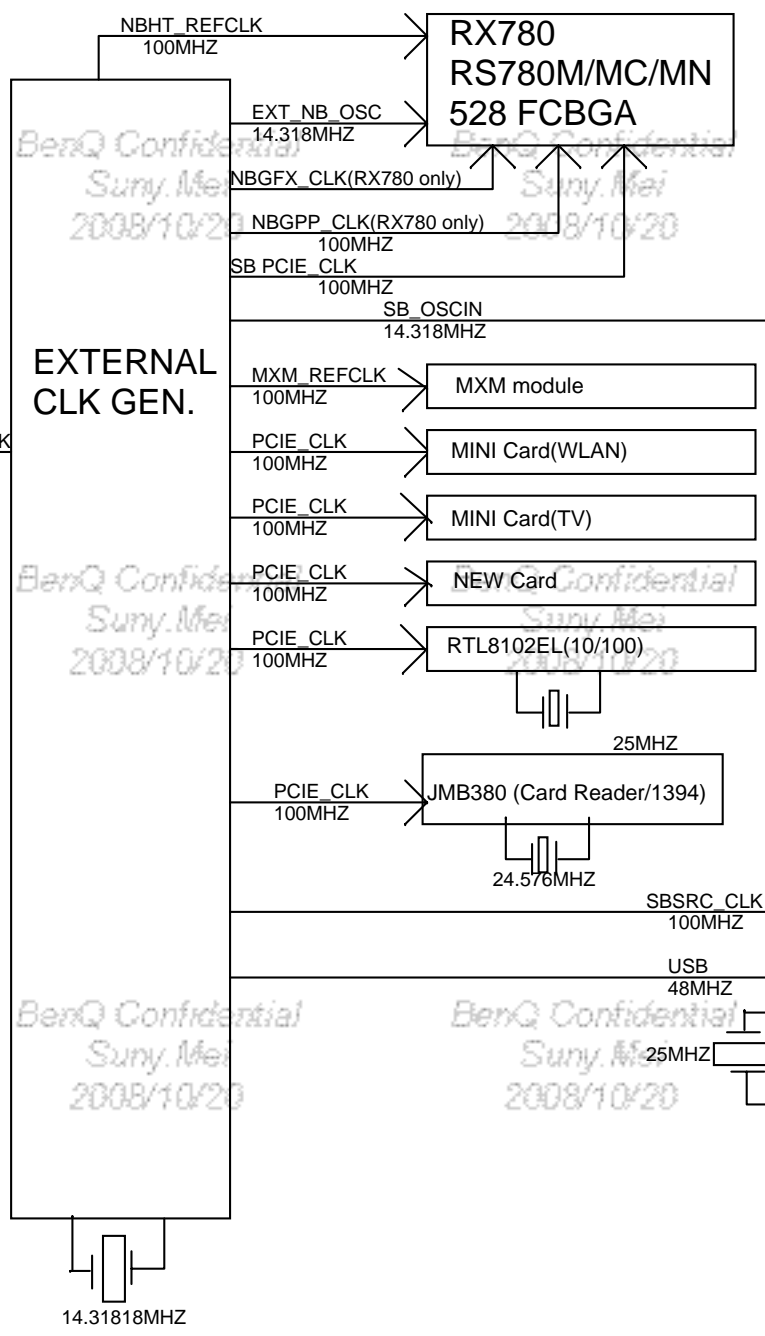
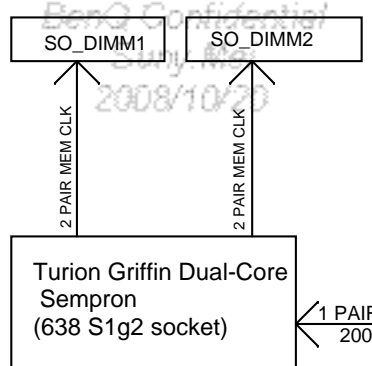
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

Power Block Diagram



Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
5VPCU	Battery LED , Power LED , CIR , RTC
3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
NB_CORE	RS780MC/RX781/RS780MN
VCC5	CAMERA , Card Reader LED , ODD/HDD LED , T/P , T/sensor , CRT , HDMI , SB700 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
VCC3	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , DVI , REQUIRED STRAPS , DEBUG STRAPS , SB700 , RS780MC , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , Headphone , EC , LAN , Audio Codec
RVCC3	WLAN , NEW CARD , SB700 , MXM , LAN
3VSUS	SB700
VCC2.5	CPU
RVCC1.2	SB700
1.8VSUS	SB700 , DDR , CPU , HDT
VCC1.8	SB700 , LCD , LVDS , RS780MC
VCC1.2	SB700 , RS780MC , CPU , WLAN , TV , NEW CARD
SMDDR_VTERM	DDR , CPU
SMDDR_VREF	DDR
5VSUS	USB



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# Reset & Power Good Diagram

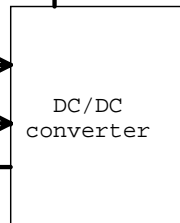
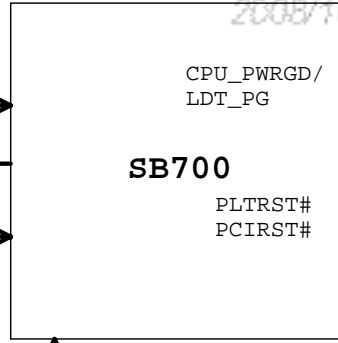
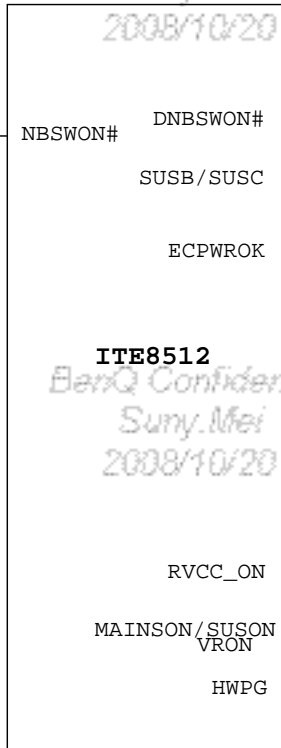
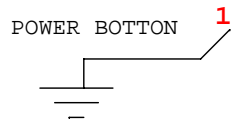
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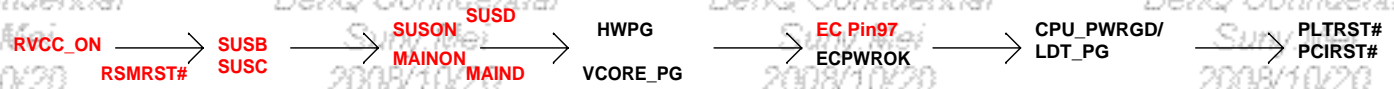
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	<b>Clock distribution diagram</b>	2A
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