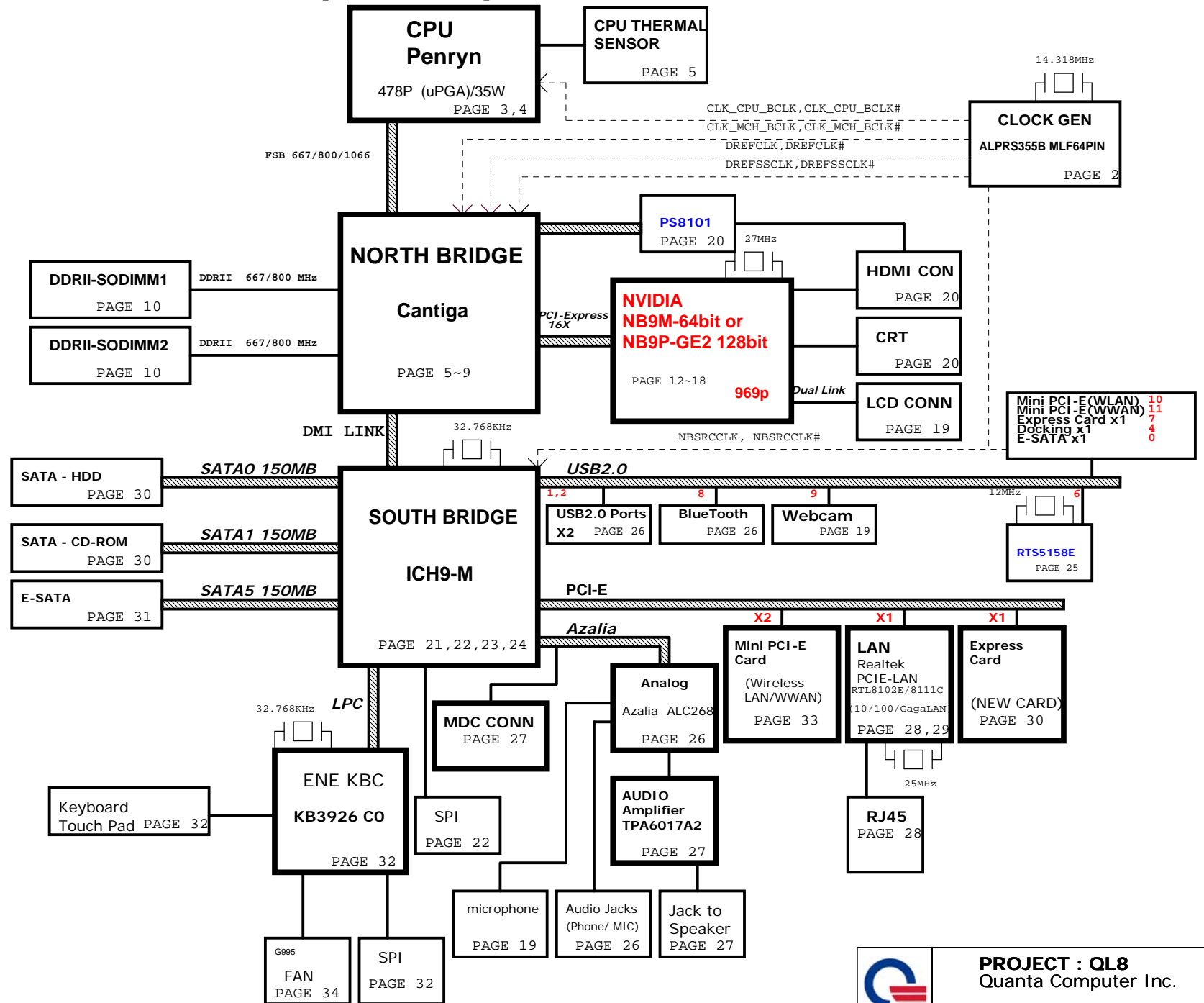


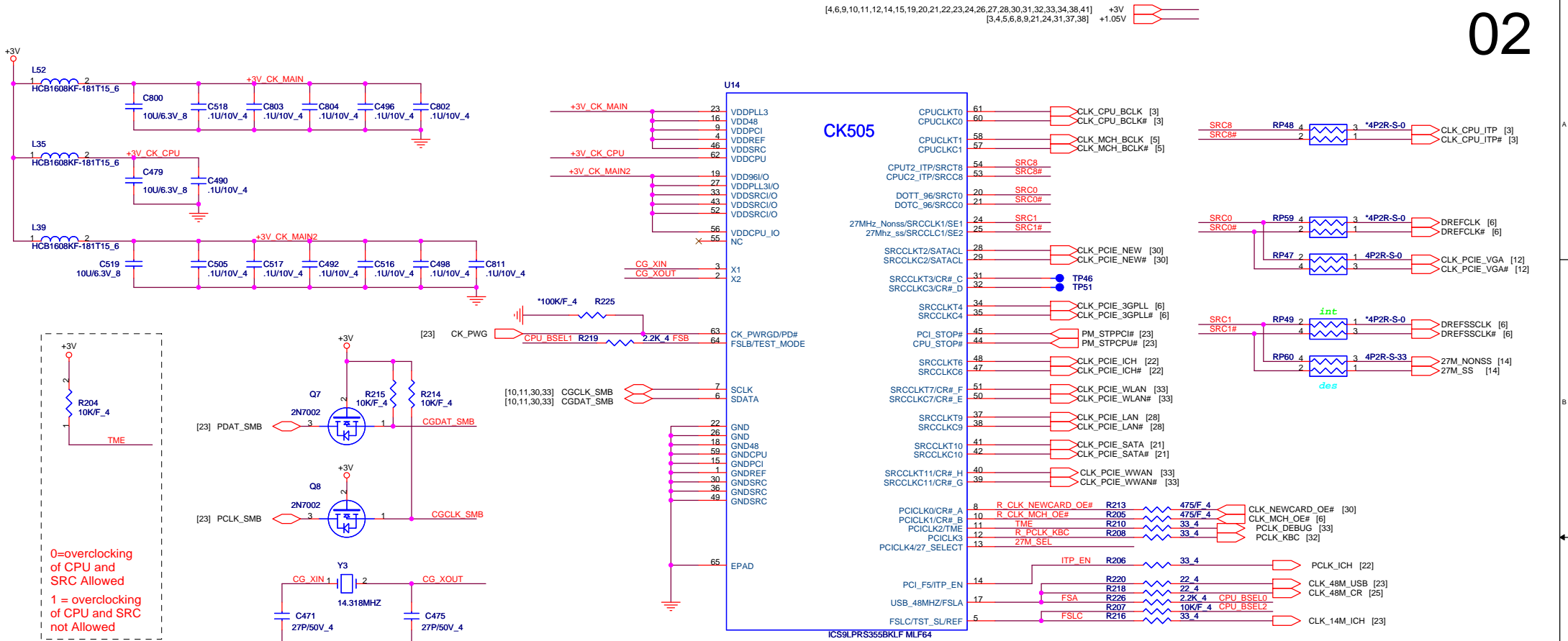
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SGND1
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : SGND2
LAYER 8 : BOT

Docking
CRT
LAN/RJ-45
Headphone Jack
USB Port
PAGE 34

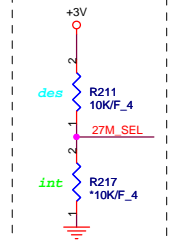
SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 35
SYSTEM POWER ISL6237IRZ-T PAGE 36
VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 37
CPU CORE ISL6266A PAGE 38
VGACORE(1.025V)Oz8118 PAGE 39
DDR II SMDRR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 40



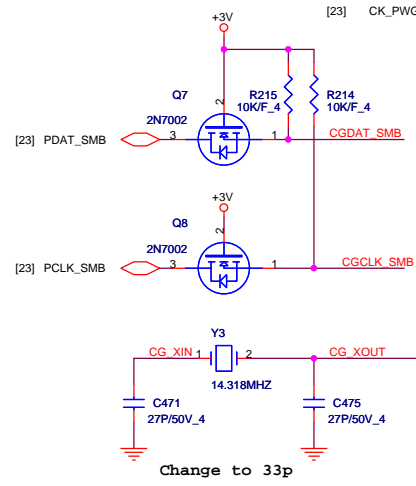
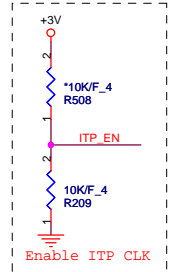
	PROJECT : QL8 Quanta Computer Inc.		Rev 3A
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	Date: Wednesday, April 02, 2008		Sheet 1 of 45



0=overclocking of CPU and SRC Allowed
 1 = overclocking of CPU and SRC not Allowed



0=UMA
 1 = External VGA

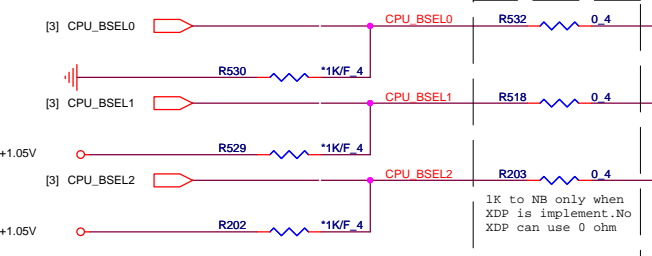


27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

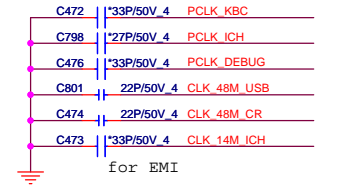
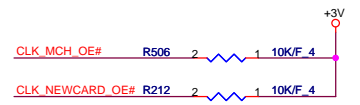
CK505 QFN64

ICS ICS9LPRS355BKLF ALPRS355000
 Silego SLG8SP513VTR AL8SP513000
 Realtek RTM875N-606-VD-GR AL000875000

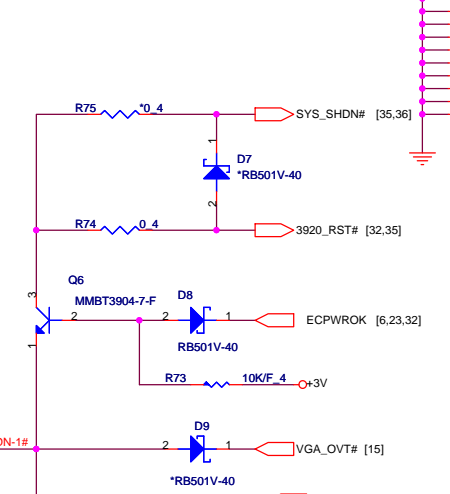
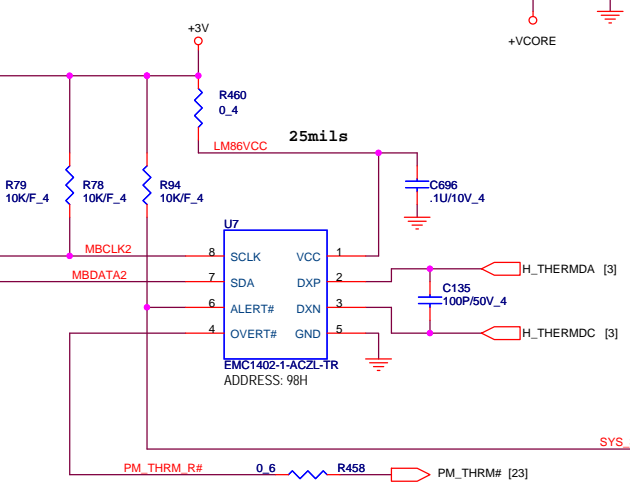
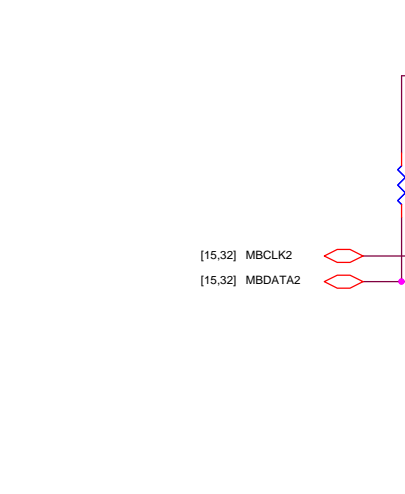
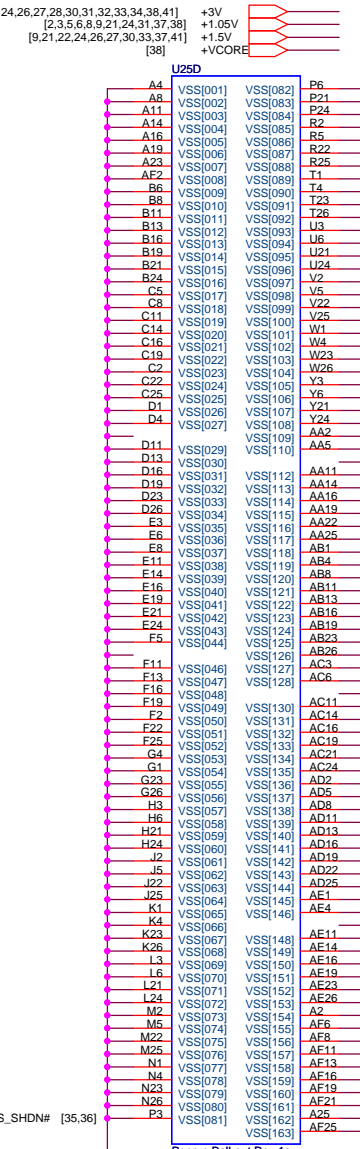
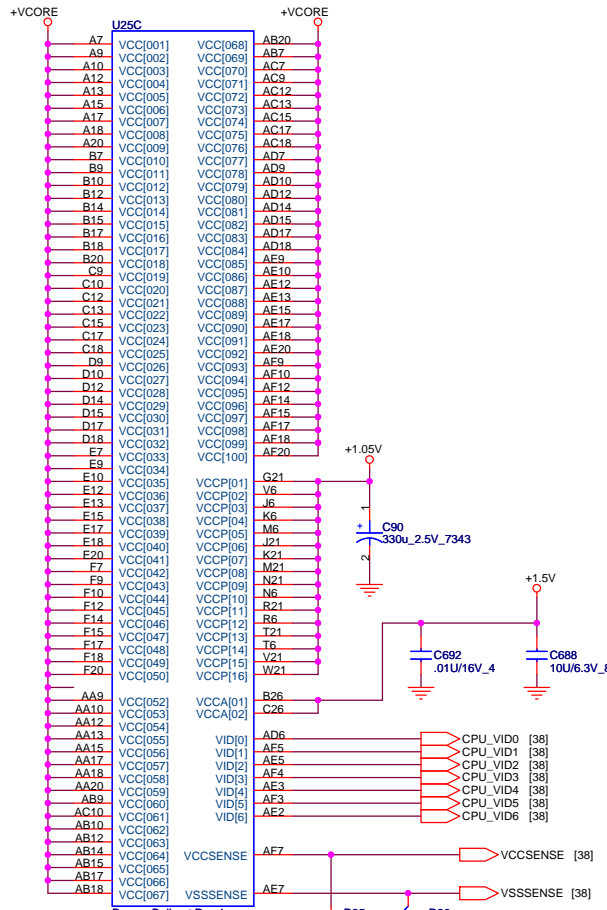
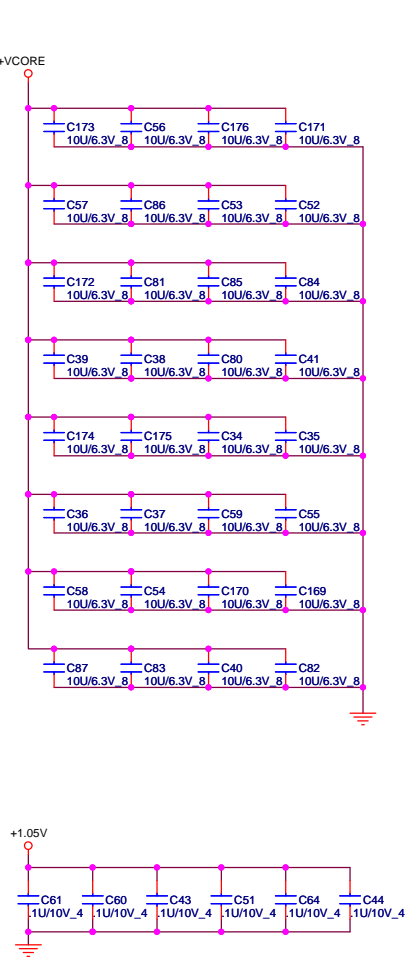
CPU Clock select



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



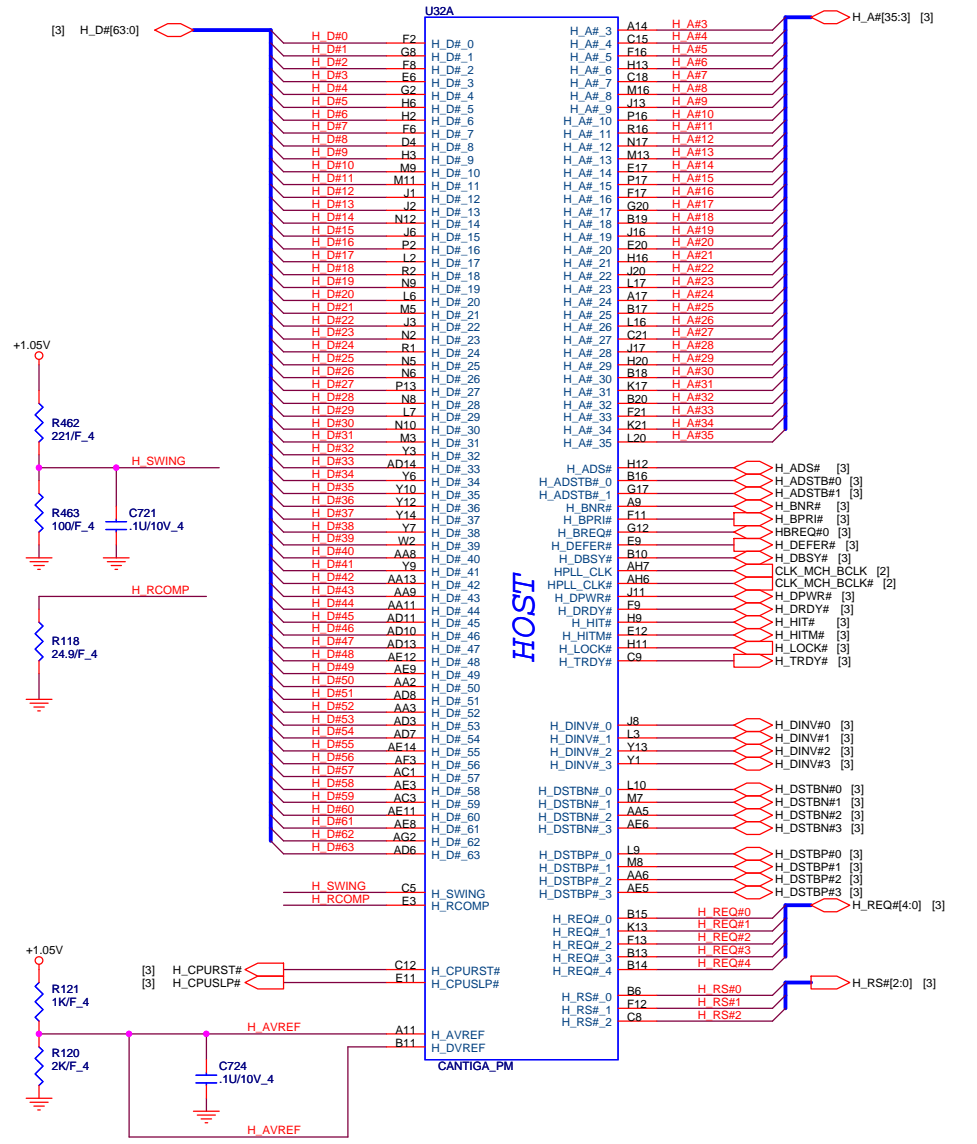
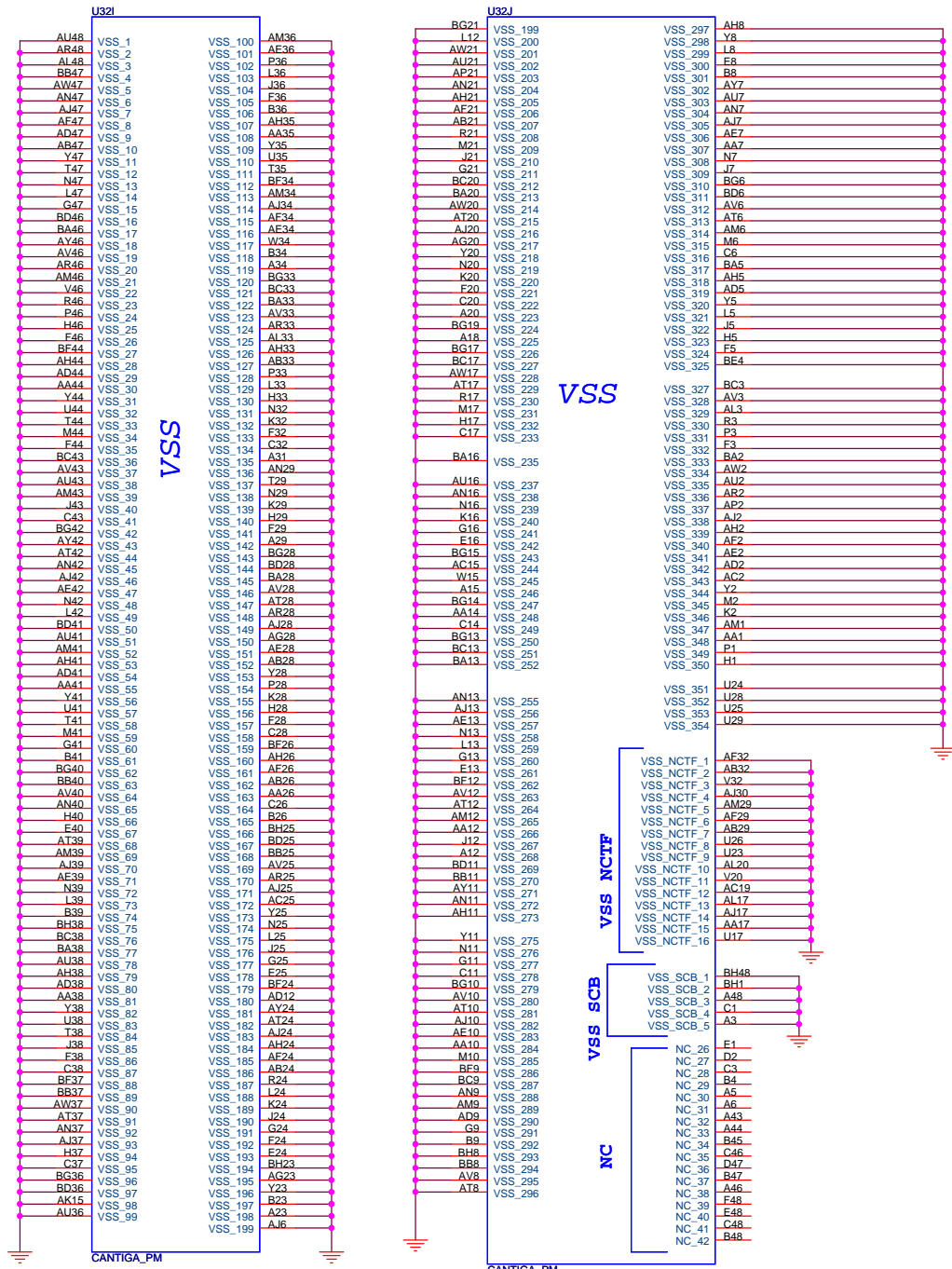
PROJECT : QL8
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PROJECT : QL8
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NB5

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[2,3,4,6,8,9,21,24,31,37,38] +1.05V

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NB5

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Cantiga Host & VSS 1/5

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Rev 3A

[2,4,9,10,11,12,14,15,19,20,21,22,23,24,26,27,28,30,31,32,33,34,36,41] +3V
 [8,9,10,31,37,40] +1.8VSUS
 [2,3,4,5,8,9,21,24,31,37,38] +1.05V
 [2,3,4,5,8,9,21,24,31,37,38] +1.05V_PEG

06

MCH_CFG_5 DMi2 selection

Low: DMi2
 High: DMi4 (Default)
 MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
 High: Normal operation(Default)
 MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
 High: Lane Reserved
 MCH_CFG_6 ITPM Host Interface

Low: ITPM Host Interface enabled
 High: ITPM Host Interface disabled (Default)
 MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality
 High: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
 High: Disabled (Default)
 MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration

0 0 Reserved
 1 0 XOR Mode enabled
 0 1 All-Z Mode enabled
 1 1 Normal operation (Default)

ME_JTAG_TCK TP35 AL34
 ME_JTAG_TDI TP29 AK34
 ME_JTAG_TDO TP28 AN35
 ME_JTAG_TMS TP27 AM35

MCH_BSEL0 [2] MCH_BSEL1 [2] MCH_BSEL2 [2]
 MCH_CFG_3 TP8
 MCH_CFG_4 TP21
 MCH_CFG_5 TP79
 MCH_CFG_6 TP20
 MCH_CFG_7 TP21
 MCH_CFG_8 TP21
 MCH_CFG_9 TP21
 MCH_CFG_10 TP11
 MCH_CFG_11 TP11
 MCH_CFG_12 TP18
 MCH_CFG_13 TP16
 MCH_CFG_14 TP18
 MCH_CFG_15 TP9
 MCH_CFG_16 TP14
 MCH_CFG_17 TP24
 MCH_CFG_18 TP24
 MCH_CFG_19 TP23
 MCH_CFG_20 TP25

DV2-FOR ITPM R168 *2.2K_4

[23] PM_SYNC# [3,21,38] H_DPRSTP# [10,11] PM_EXTTS#0 [11] PM_EXTTS#1 [12,22] PLT_RST-R# [3,21] PM_THRMTrip# [23,38] DPRSLPVR

PM_SYNC# R29
 PM_DPRSTP# B7
 PM_EXT_TS#_0 N33
 PM_EXT_TS#_1 P32
 PM_WROK A140
 RST_IN# MCH A111
 PM_WROK R123 *100K_4

PM_THRMTrip# R32
 DPRSLPVR R159 *10K/4_4 PM_EXTTS#0
 R155 *10K/4_4 PM_EXTTS#1

ACZ_BITCLK_MCH R483 *33_4
 C757 *33P/50V_4

NC.1 BG48
 NC.2 BF48
 NC.3 BC48
 NC.4 BH47
 NC.5 BH47
 NC.6 BG47
 NC.7 BE47
 NC.8 BH46
 NC.9 BE46
 NC.10 BH44
 NC.11 BH43
 NC.12 BH6
 NC.13 BH6
 NC.14 BG4
 NC.15 BH5
 NC.16 BH2
 NC.17 BH2
 NC.18 BH2
 NC.19 BG2
 NC.20 BE2
 NC.21 BF2
 NC.22 BF1
 NC.23 BD1
 NC.24 BC1
 NC.25 E1
 NC.26 A47

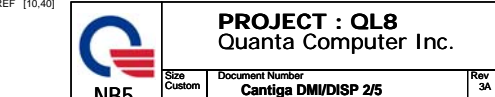
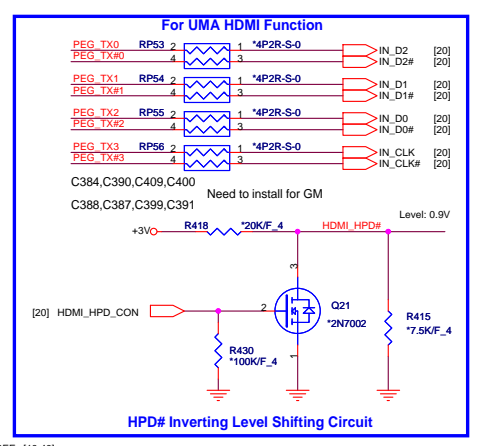
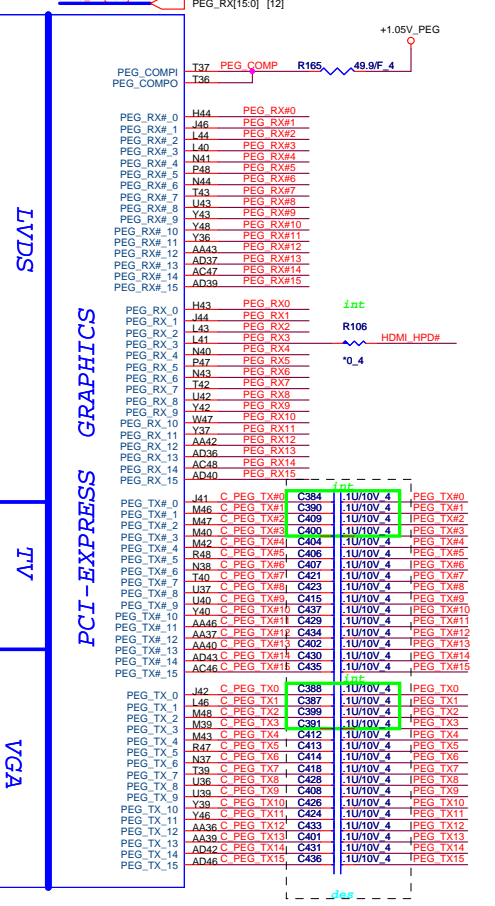
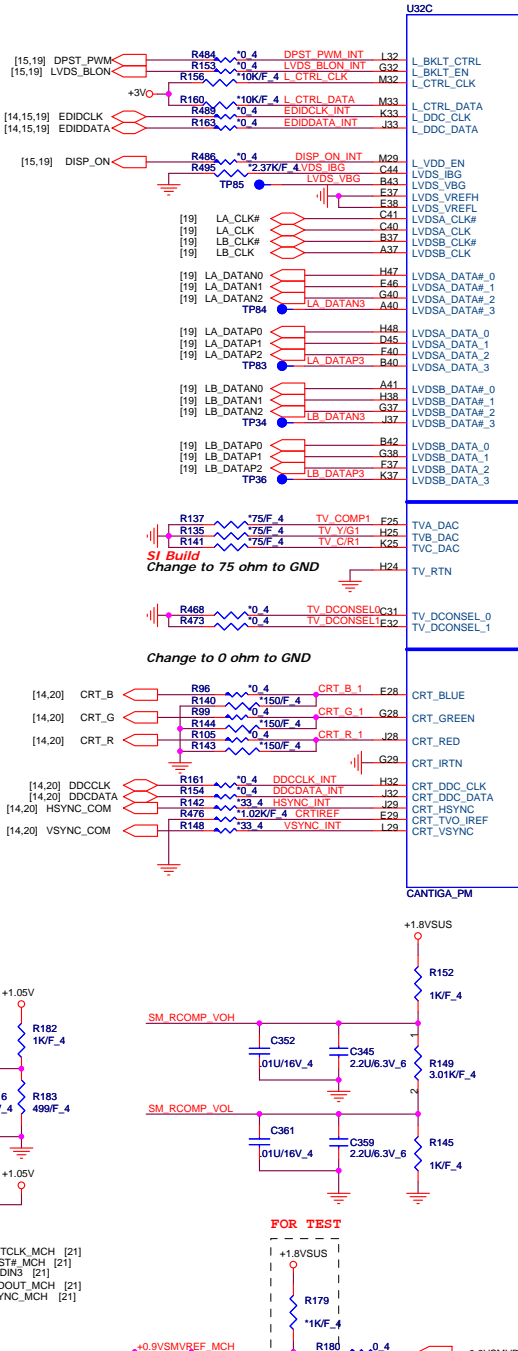
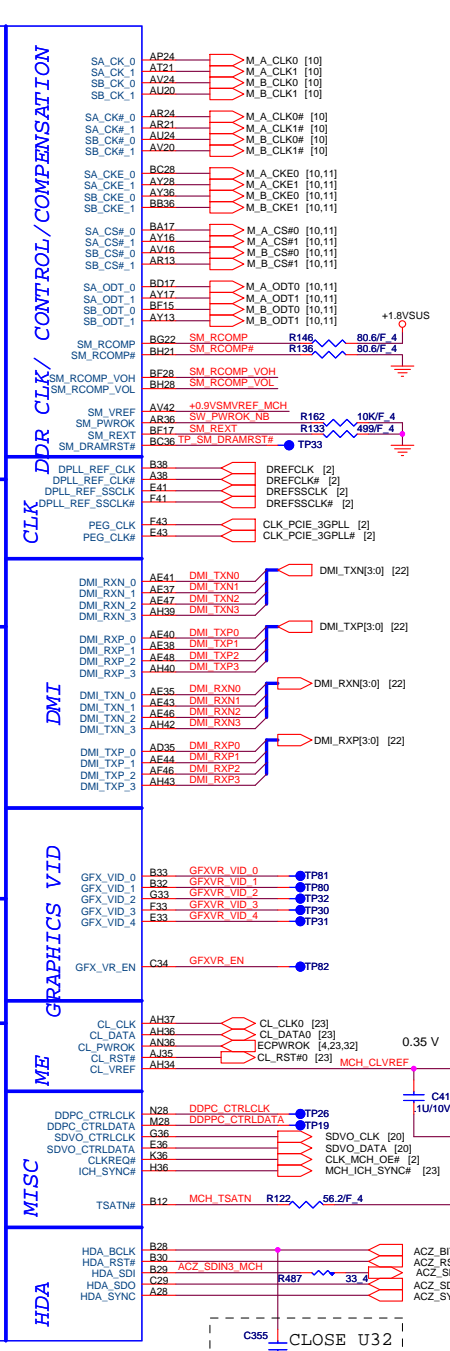
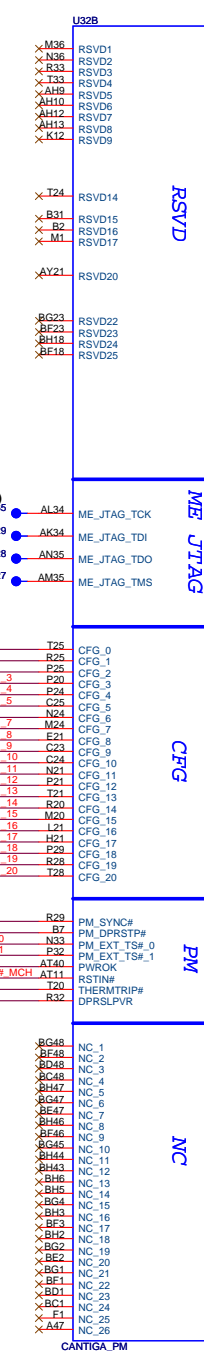
CL_CLK AH37
 CL_DATA AH38
 CL_PWROK AH36
 CL_RST# AH35
 CL_VREF AH34

DDPC_CTRLCLK N28
 DDPC_CTRLDATA M28
 SDVO_CLK G36
 SDVO_DATA E36
 CLK_MCH_OEP K36
 MCH_I2C_SYNC# H36

TSATN# B12
 MCH_TSATN R122 *56.2F_4

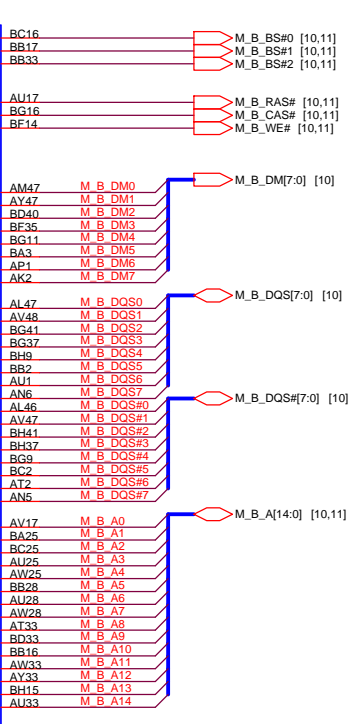
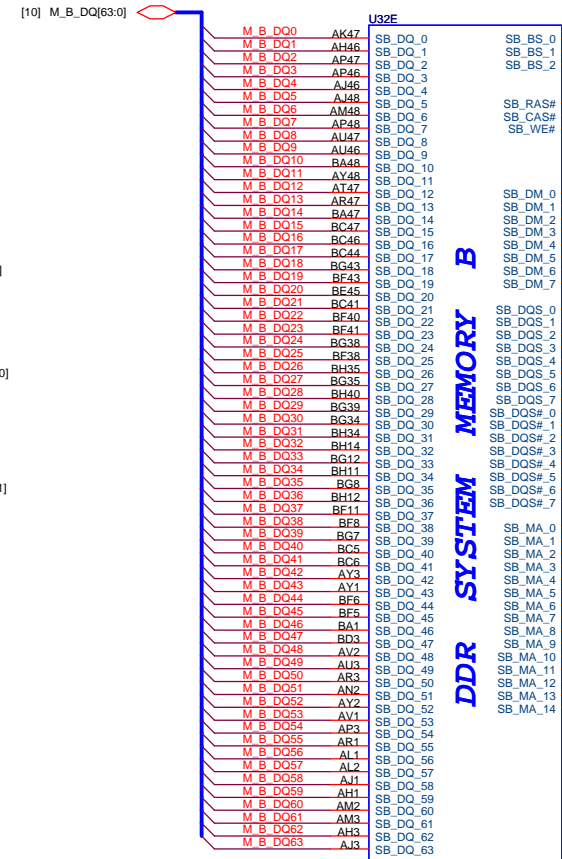
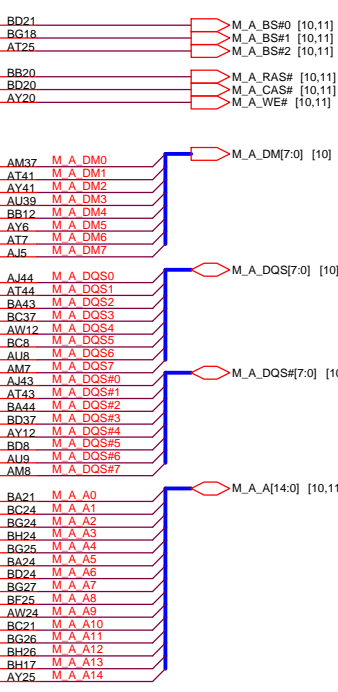
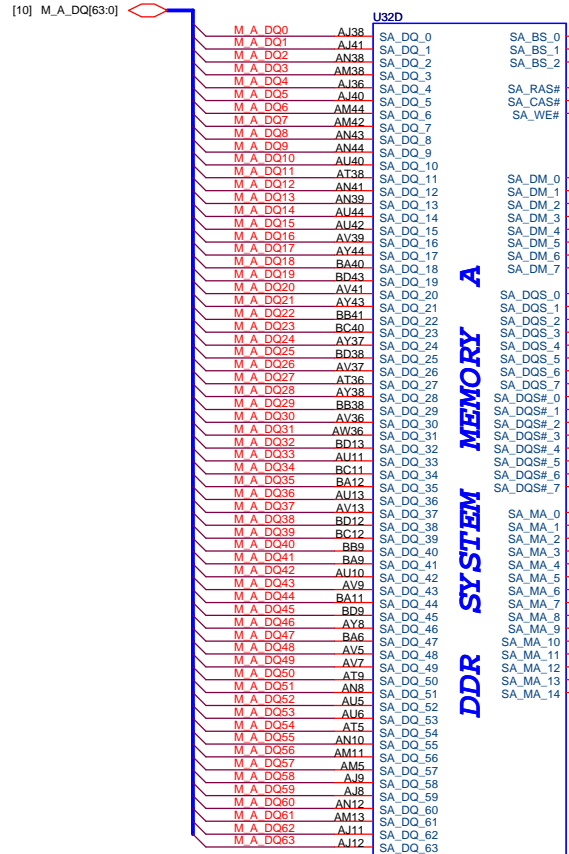
HDA_BCLK B28
 HDA_RST# B30
 HDA_SDI B29
 HDA_SDO C29
 HDA_SYNC BD1
 ACZ_BITCLK_MCH [21]
 ACZ_RST#_MCH [21]
 ACZ_SDI# [21]
 ACZ_SDO#_MCH [21]
 ACZ_SYNC_MCH [21]

CANTIGA_PM C355
 CLOSE U32
 EMI 10P/50V_4



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U32G

AP33	VCC_SM_1
AN33	VCC_SM_2
BH32	VCC_SM_3
BG32	VCC_SM_4
BF32	VCC_SM_5
BD32	VCC_SM_6
BC32	VCC_SM_7
BA32	VCC_SM_8
AY32	VCC_SM_9
AW32	VCC_SM_10
AV32	VCC_SM_11
AT32	VCC_SM_12
AM32	VCC_SM_13
AL32	VCC_SM_14
AK32	VCC_SM_15
AJ32	VCC_SM_16
AI32	VCC_SM_17
AH31	VCC_SM_18
AG31	VCC_SM_19
AF31	VCC_SM_20
AE31	VCC_SM_21
AD32	VCC_SM_22
AC32	VCC_SM_23
AB32	VCC_SM_24
AA32	VCC_SM_25
Y32	VCC_SM_26
Y31	VCC_SM_27
Y30	VCC_SM_28
Y29	VCC_SM_29
Y28	VCC_SM_30
Y27	VCC_SM_31
Y26	VCC_SM_32
Y25	VCC_SM_33
Y24	VCC_SM_34
Y23	VCC_SM_35

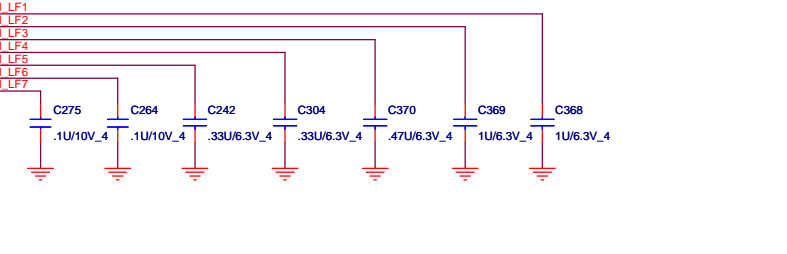
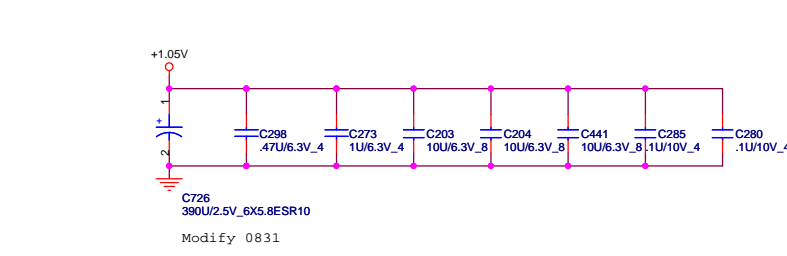
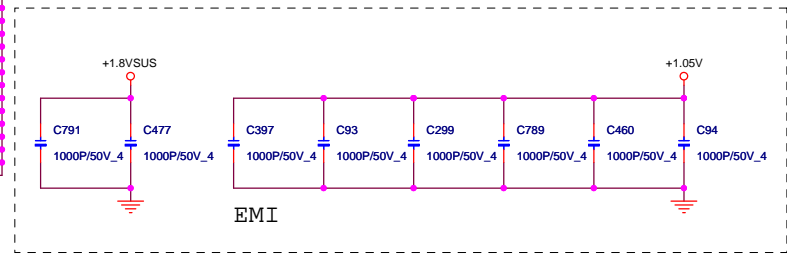
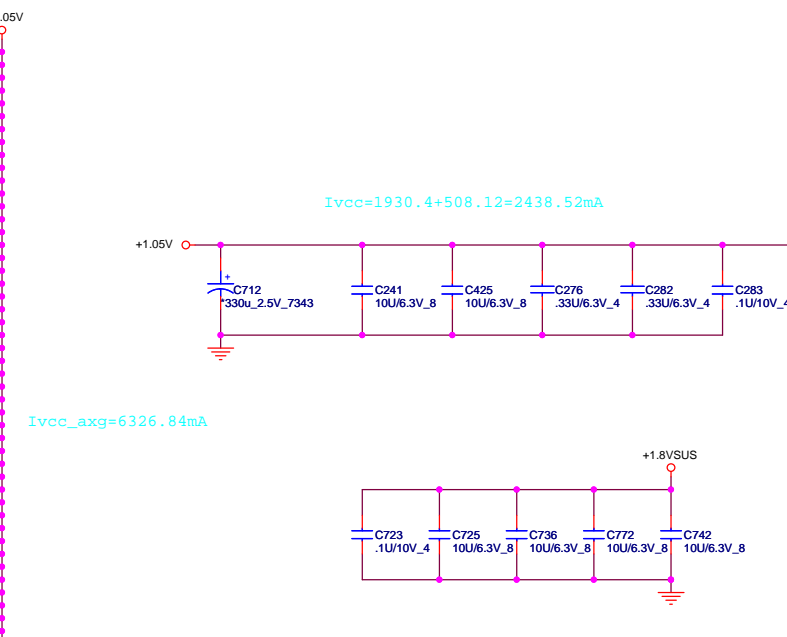
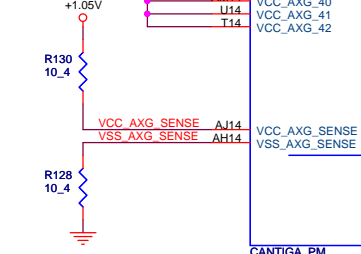
W28	VCC_AXG_NCTF_1
V28	VCC_AXG_NCTF_2
W26	VCC_AXG_NCTF_3
V26	VCC_AXG_NCTF_4
W25	VCC_AXG_NCTF_5
V25	VCC_AXG_NCTF_6
W24	VCC_AXG_NCTF_7
V24	VCC_AXG_NCTF_8
W23	VCC_AXG_NCTF_9
V23	VCC_AXG_NCTF_10
AM21	VCC_AXG_NCTF_11
AL21	VCC_AXG_NCTF_12
W21	VCC_AXG_NCTF_13
V21	VCC_AXG_NCTF_14
U21	VCC_AXG_NCTF_15
AM20	VCC_AXG_NCTF_16
AK20	VCC_AXG_NCTF_17
W20	VCC_AXG_NCTF_18
U20	VCC_AXG_NCTF_19
AM19	VCC_AXG_NCTF_20
AL19	VCC_AXG_NCTF_21
AK19	VCC_AXG_NCTF_22
AJ19	VCC_AXG_NCTF_23
AH19	VCC_AXG_NCTF_24
AG19	VCC_AXG_NCTF_25
AF19	VCC_AXG_NCTF_26
AE19	VCC_AXG_NCTF_27
AD19	VCC_AXG_NCTF_28
AC19	VCC_AXG_NCTF_29
AB19	VCC_AXG_NCTF_30
AA19	VCC_AXG_NCTF_31
Y19	VCC_AXG_NCTF_32
W19	VCC_AXG_NCTF_33
V19	VCC_AXG_NCTF_34
U19	VCC_AXG_NCTF_35
AM17	VCC_AXG_NCTF_36
AL17	VCC_AXG_NCTF_37
AK17	VCC_AXG_NCTF_38
AJ17	VCC_AXG_NCTF_39
AH17	VCC_AXG_NCTF_40
AG17	VCC_AXG_NCTF_41
AF17	VCC_AXG_NCTF_42
AE17	VCC_AXG_NCTF_43
AD17	VCC_AXG_NCTF_44
AC17	VCC_AXG_NCTF_45
AB17	VCC_AXG_NCTF_46
Y17	VCC_AXG_NCTF_47
W17	VCC_AXG_NCTF_48
V17	VCC_AXG_NCTF_49
U17	VCC_AXG_NCTF_50
AM16	VCC_AXG_NCTF_51
AL16	VCC_AXG_NCTF_52
AK16	VCC_AXG_NCTF_53
AJ16	VCC_AXG_NCTF_54
AH16	VCC_AXG_NCTF_55
AG16	VCC_AXG_NCTF_56
AF16	VCC_AXG_NCTF_57
AE16	VCC_AXG_NCTF_58
AD16	VCC_AXG_NCTF_59
AC16	VCC_AXG_NCTF_60
AB16	VCC_AXG_NCTF_61
Y16	VCC_AXG_NCTF_62
W16	VCC_AXG_NCTF_63
V16	VCC_AXG_NCTF_64
U16	VCC_AXG_NCTF_65

VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desigs.

U32F

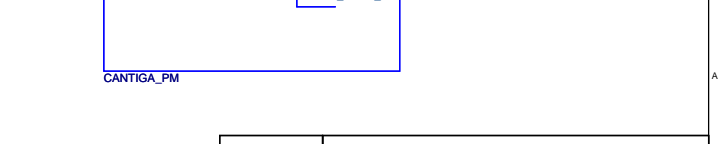
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AE25	VCC_AXG_2
AB25	VCC_AXG_3
AA25	VCC_AXG_4
AE24	VCC_AXG_5
AC24	VCC_AXG_6
AA24	VCC_AXG_7
Y24	VCC_AXG_8
AE23	VCC_AXG_9
AC23	VCC_AXG_10
AB23	VCC_AXG_11
AA23	VCC_AXG_12
AJ21	VCC_AXG_13
AG21	VCC_AXG_14
AF21	VCC_AXG_15
AD21	VCC_AXG_16
AA21	VCC_AXG_17
Y21	VCC_AXG_18
AH20	VCC_AXG_19
AF20	VCC_AXG_20
AE20	VCC_AXG_21
AC20	VCC_AXG_22
AB20	VCC_AXG_23
AA20	VCC_AXG_24
T17	VCC_AXG_25
T16	VCC_AXG_26
AM15	VCC_AXG_27
AL15	VCC_AXG_28
AK15	VCC_AXG_29
AJ15	VCC_AXG_30
AH15	VCC_AXG_31
AG15	VCC_AXG_32
AF15	VCC_AXG_33
AE15	VCC_AXG_34
AD15	VCC_AXG_35
Y15	VCC_AXG_36
V15	VCC_AXG_37
U15	VCC_AXG_38
AM14	VCC_AXG_39
AL14	VCC_AXG_40
AK14	VCC_AXG_41
AJ14	VCC_AXG_42

VCC_SM_LF1	AV44 +VCCSM_LF1
VCC_SM_LF2	BA37 +VCCSM_LF2
VCC_SM_LF3	AM40 +VCCSM_LF3
VCC_SM_LF4	AV21 +VCCSM_LF4
VCC_SM_LF5	AY5 +VCCSM_LF5
VCC_SM_LF6	AM10 +VCCSM_LF6
VCC_SM_LF7	BB13 +VCCSM_LF7



AG34	VCC_1
AC34	VCC_2
AB34	VCC_3
AA34	VCC_4
Y34	VCC_5
U34	VCC_6
AM33	VCC_7
AK33	VCC_8
AJ33	VCC_9
AG33	VCC_10
AF33	VCC_11
AE33	VCC_12
AC33	VCC_13
AA33	VCC_14
Y33	VCC_15
W33	VCC_16
U33	VCC_17
U33	VCC_18
U33	VCC_19
AH28	VCC_20
AF28	VCC_21
AC28	VCC_22
AA28	VCC_23
AJ26	VCC_24
AG26	VCC_25
AE26	VCC_26
AC26	VCC_27
AH25	VCC_28
AG25	VCC_29
AG24	VCC_30
AJ23	VCC_31
AH23	VCC_32
AF23	VCC_33
T32	VCC_34

VCC_NCTF_1	AM32
VCC_NCTF_2	AL32
VCC_NCTF_3	AK32
VCC_NCTF_4	AJ32
VCC_NCTF_5	AH32
VCC_NCTF_6	AG32
VCC_NCTF_7	AF32
VCC_NCTF_8	AE32
VCC_NCTF_9	AD32
VCC_NCTF_10	Y32
VCC_NCTF_11	U32
VCC_NCTF_12	U32
VCC_NCTF_13	AM30
VCC_NCTF_14	AL30
VCC_NCTF_15	AK30
VCC_NCTF_16	AH30
VCC_NCTF_17	AG30
VCC_NCTF_18	AF30
VCC_NCTF_19	AE30
VCC_NCTF_20	AC30
VCC_NCTF_21	AB30
VCC_NCTF_22	AA30
VCC_NCTF_23	Y30
VCC_NCTF_24	W30
VCC_NCTF_25	V30
VCC_NCTF_26	U30
VCC_NCTF_27	U30
VCC_NCTF_28	U30
VCC_NCTF_29	AK29
VCC_NCTF_30	AJ29
VCC_NCTF_31	AH29
VCC_NCTF_32	AG29
VCC_NCTF_33	AE29
VCC_NCTF_34	AD29
VCC_NCTF_35	AA29
VCC_NCTF_36	Y29
VCC_NCTF_37	W29
VCC_NCTF_38	V29
VCC_NCTF_39	U29
VCC_NCTF_40	U29
VCC_NCTF_41	AK28
VCC_NCTF_42	AL28
VCC_NCTF_43	AK26
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VCC_NCTF_44	AK24
VCC_NCTF_44	AK23



CANTIGA_PM

CANTIGA_PM

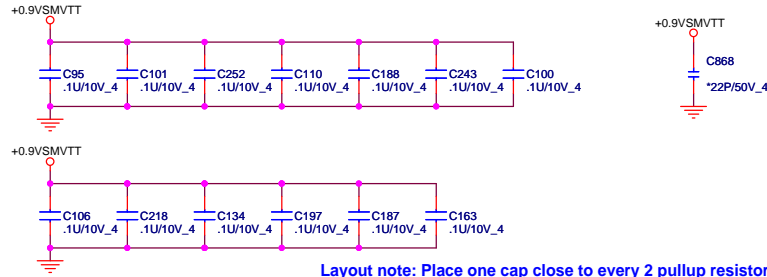
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Quanta Computer Inc.

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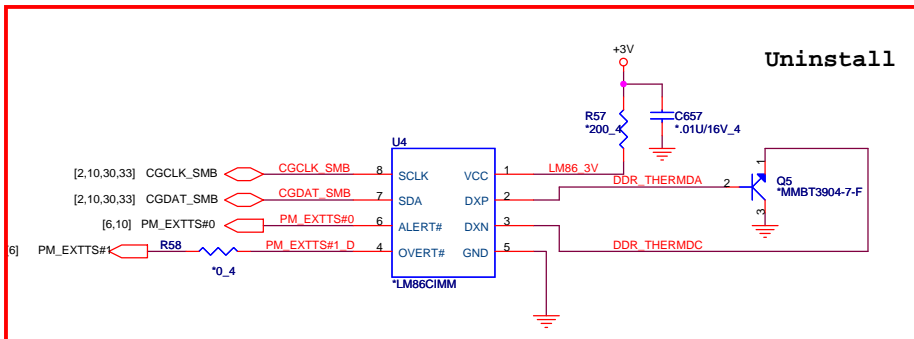
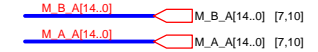
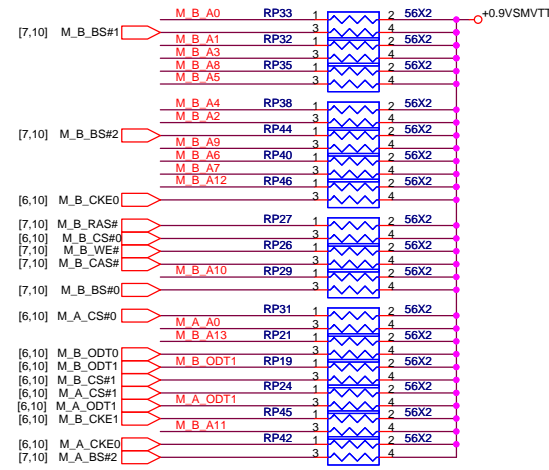
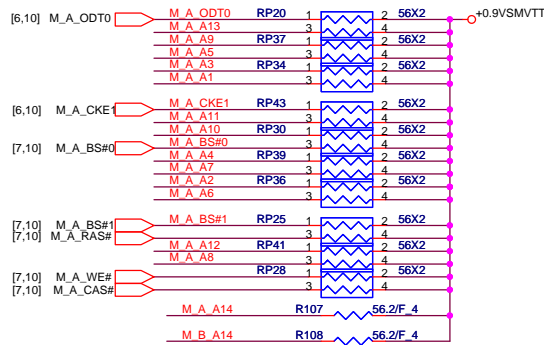
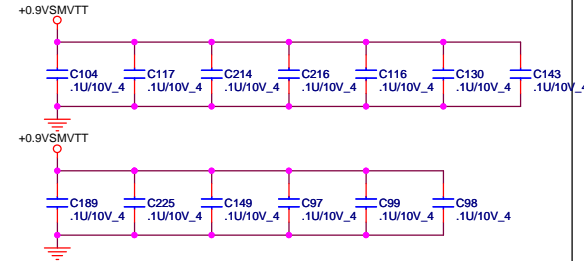
DDRII DUAL CHANNEL A,B.

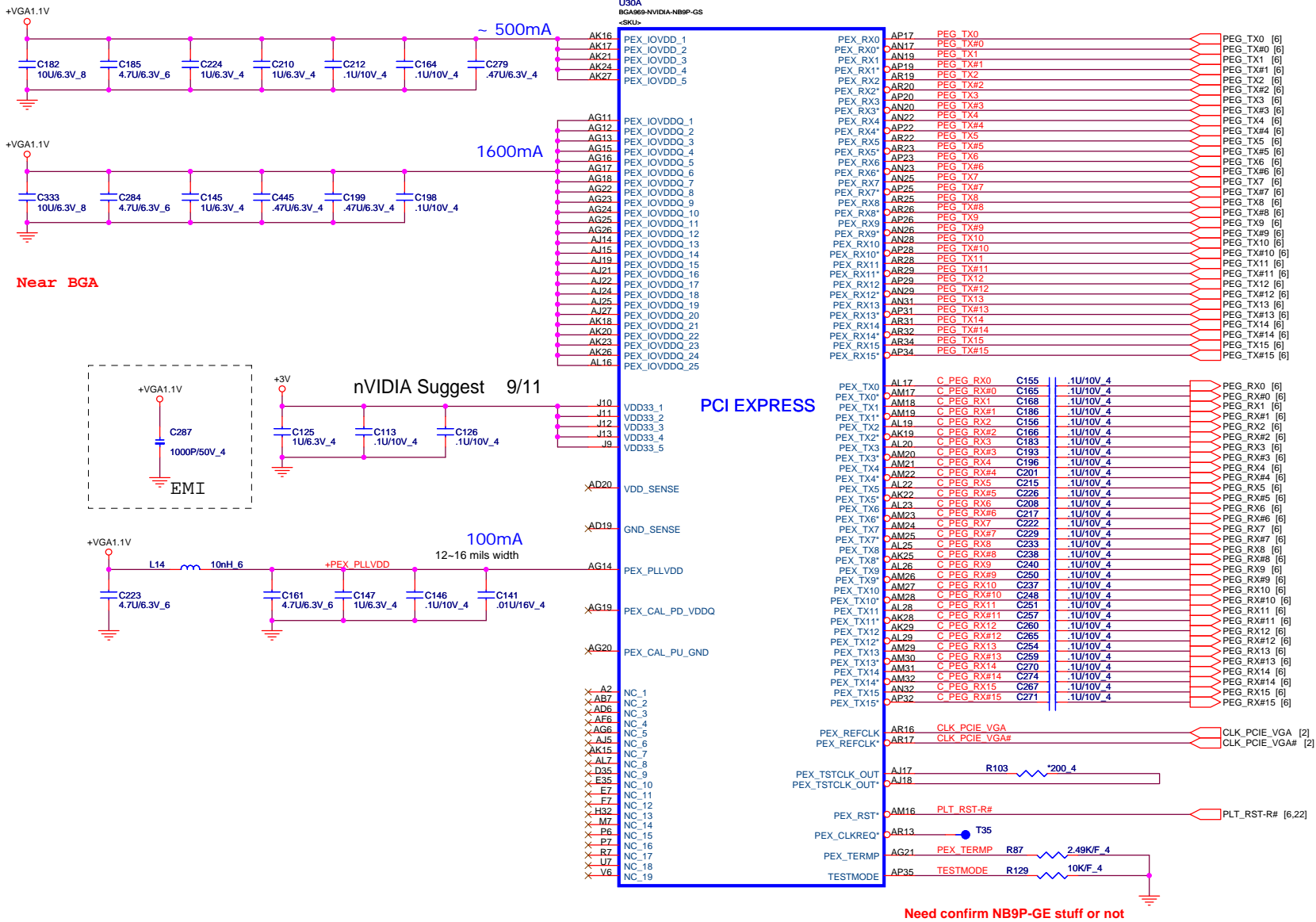
DDRII A CHANNEL

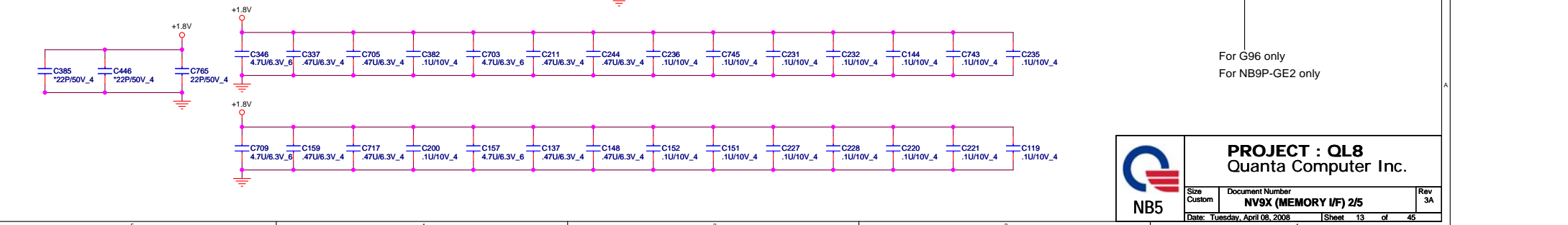
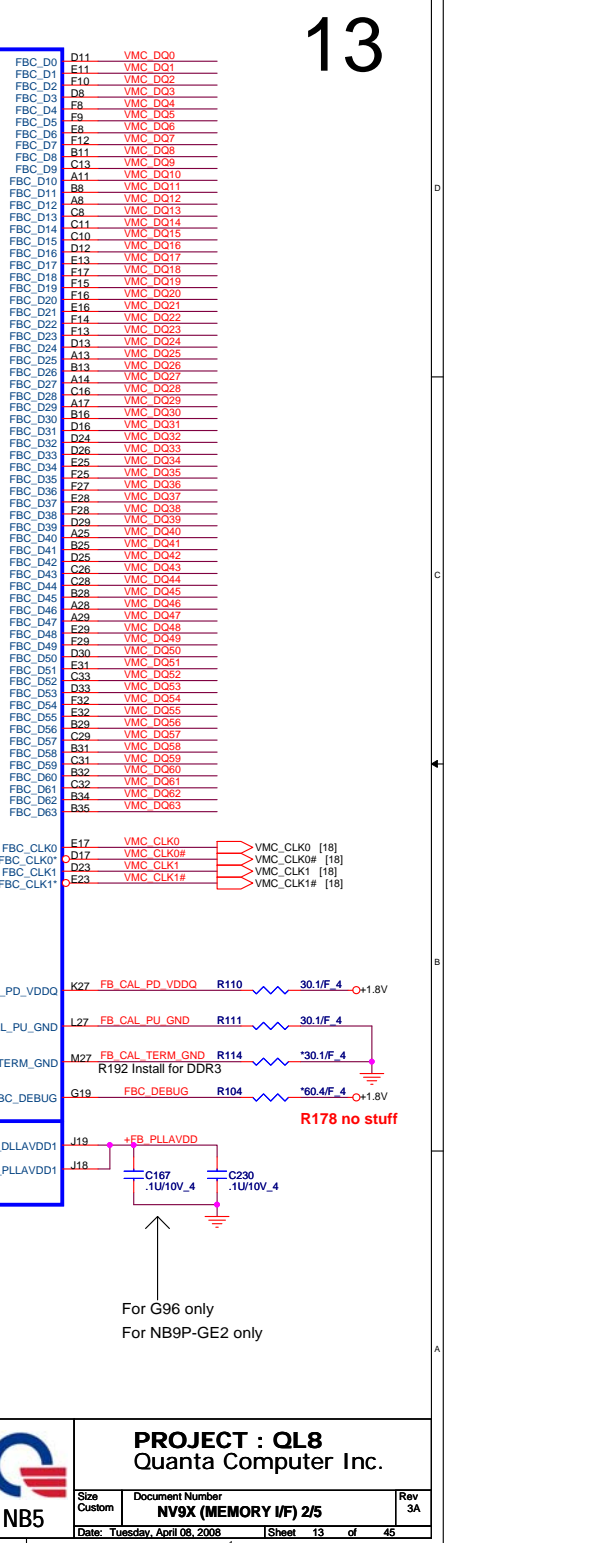
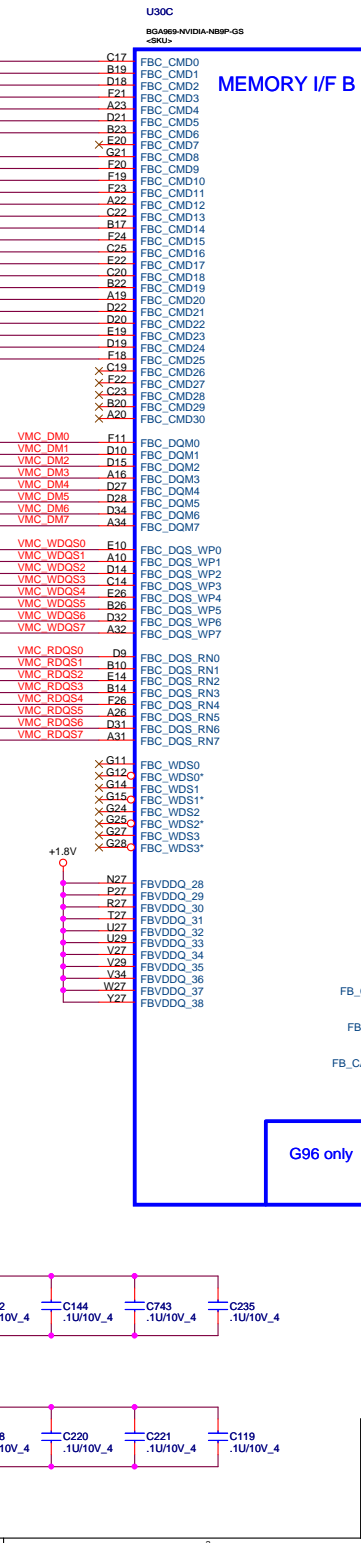
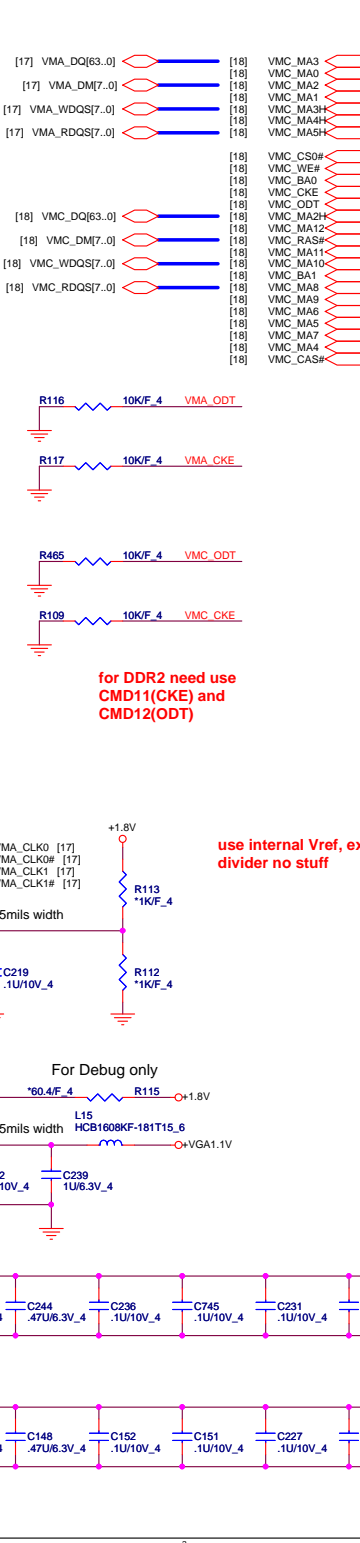
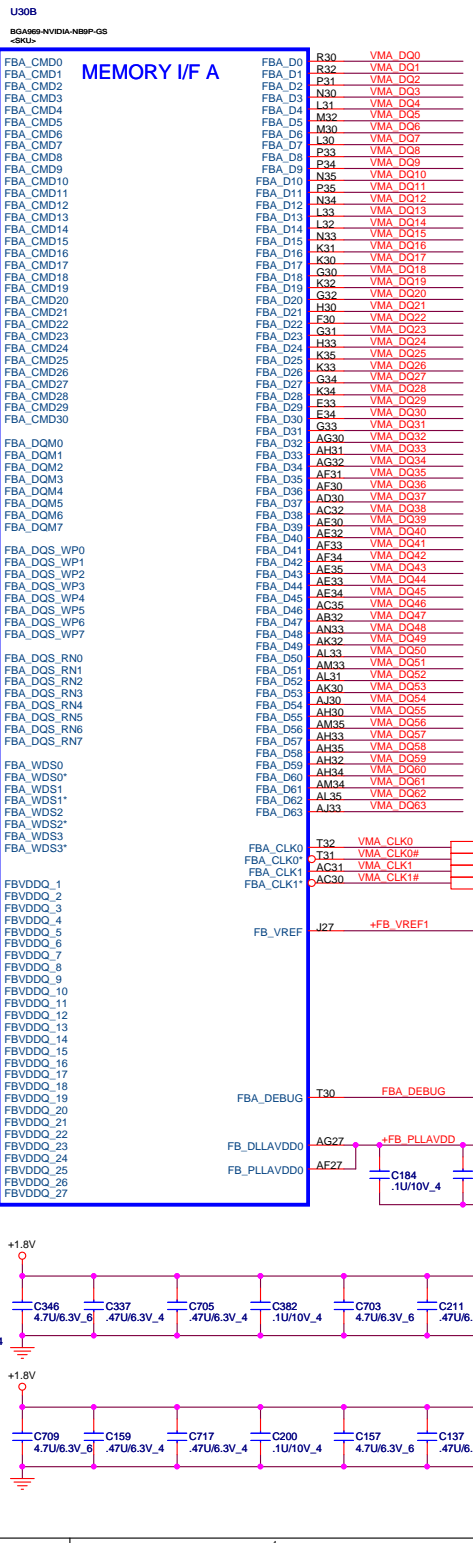
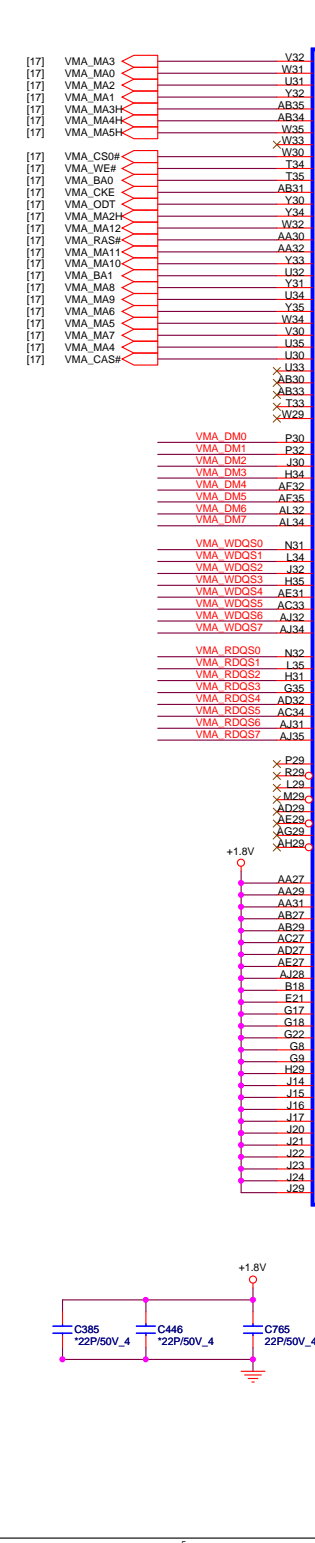


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

DDRII B CHANNEL







for DDR2 need use CMD11(CKE) and CMD12(ODT)

use internal Vref, ext divider no stuff

G96 only

R178 no stuff

For G96 only
For NB9P-GE2 only

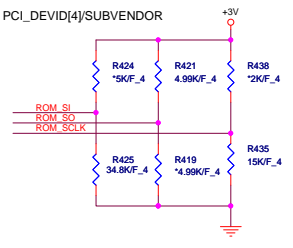
PROJECT : QL8

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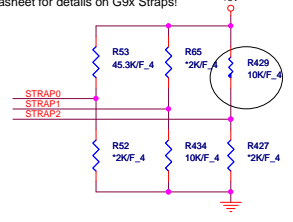
Size Custom	Document Number NV9X (MEMORY I/F) 2/5	Rev 3A
Date: Tuesday, April 08, 2008		
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NB9P-GE2 (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NV_VDD VID0
6	OUT	N/A	NV_VDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

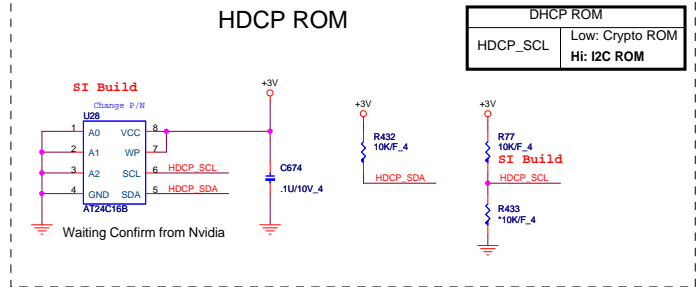
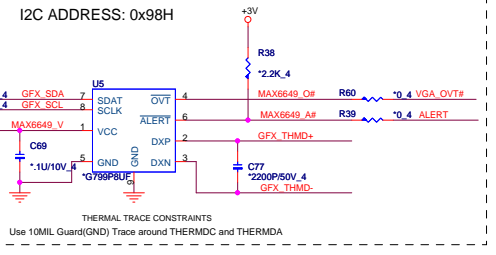
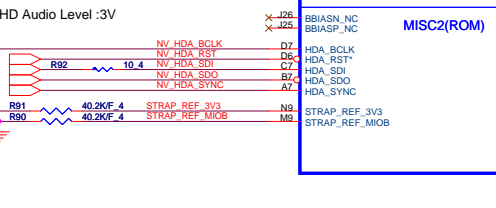
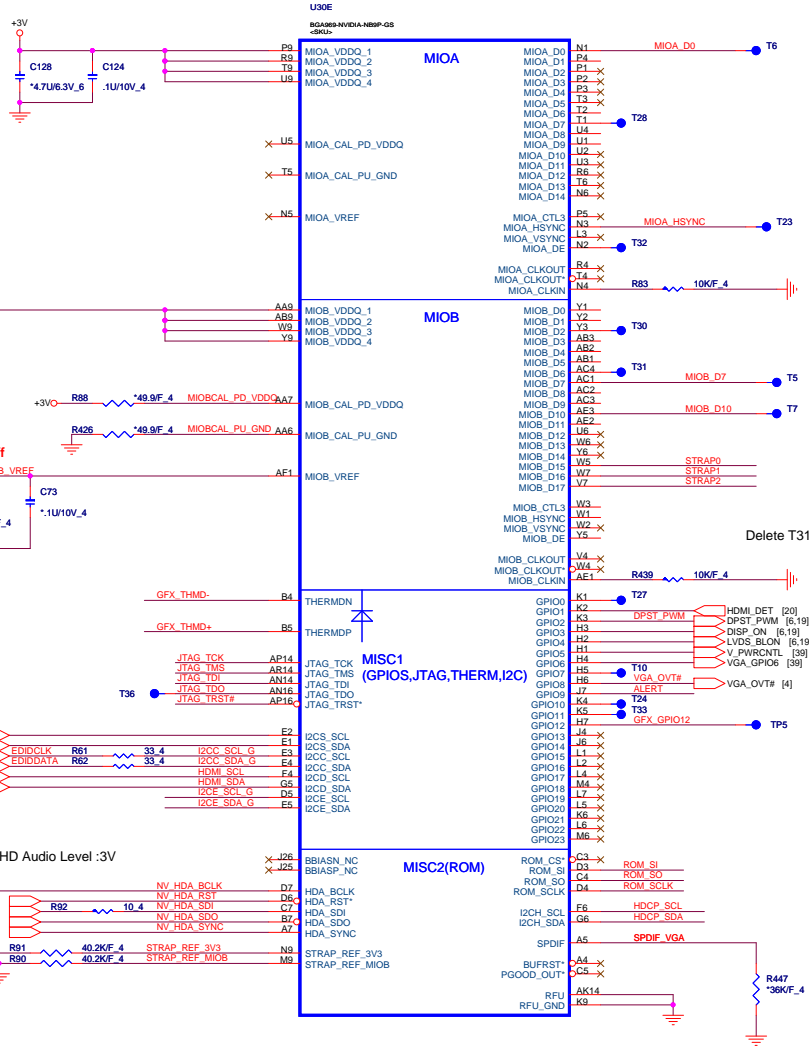
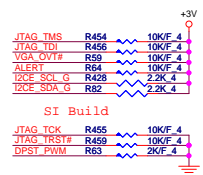


SEE Datasheet for details on G9x Straps!



Logical Strap Bit Mapping

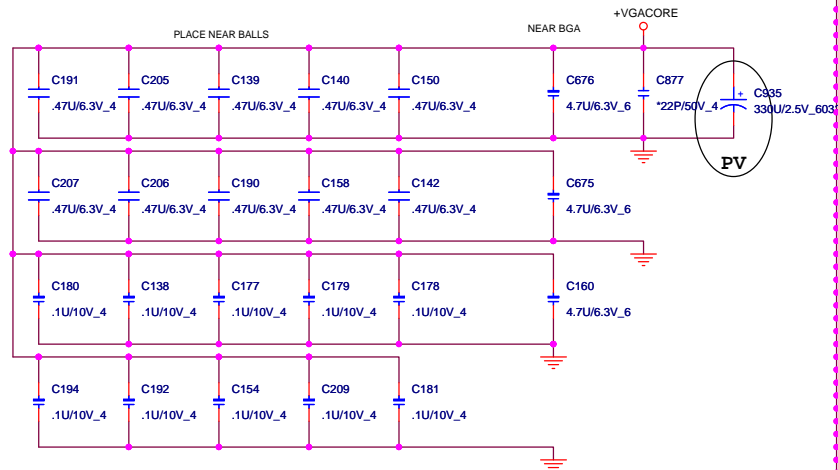
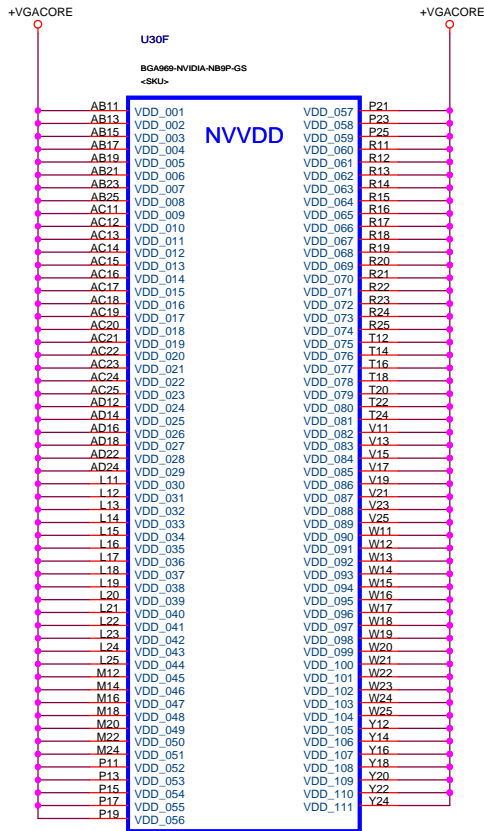
DB	9P-GE2 Qimonda	9M-GS-Hynix	5K	1000	0000
R425	CS33482FB22 35K	CS34532FB18 45K	10K	1001	0001
			15K	1010	0010
			20K	1011	0011
R429	CS24992FB26 4.99K	CS24992FB26 10K	25K	1100	0100
			30K	1101	0101
			35K	1110	0110
			45K	1111	0111



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

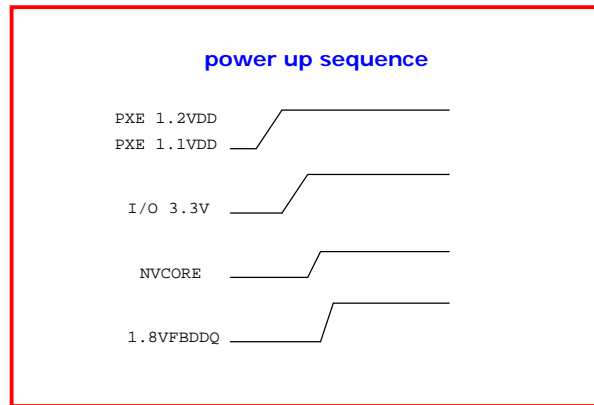
Waiting Confirm from Nvidia

NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

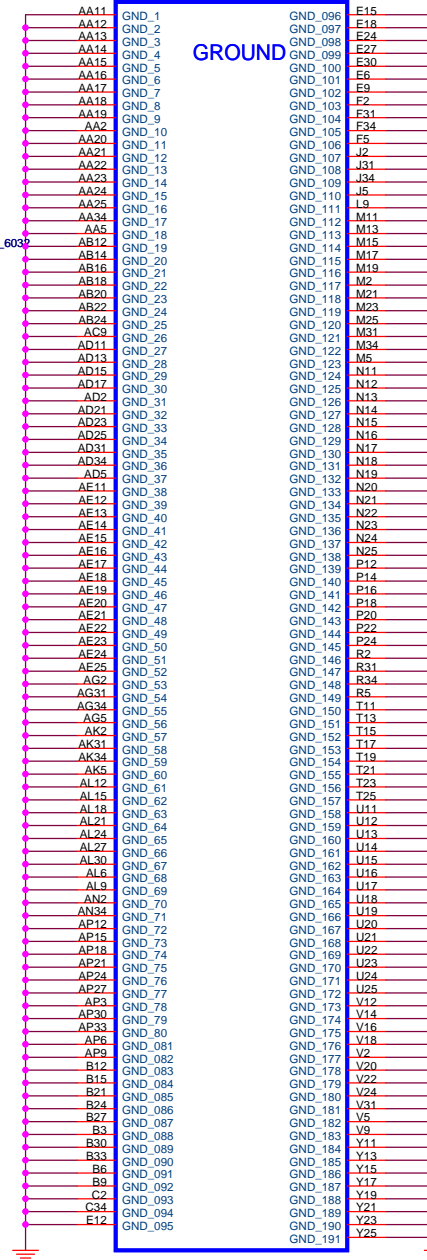
NB9M: VGACORE +0.90V (Normal) , +1.09V



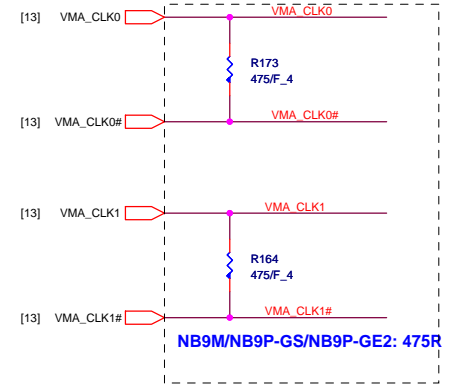
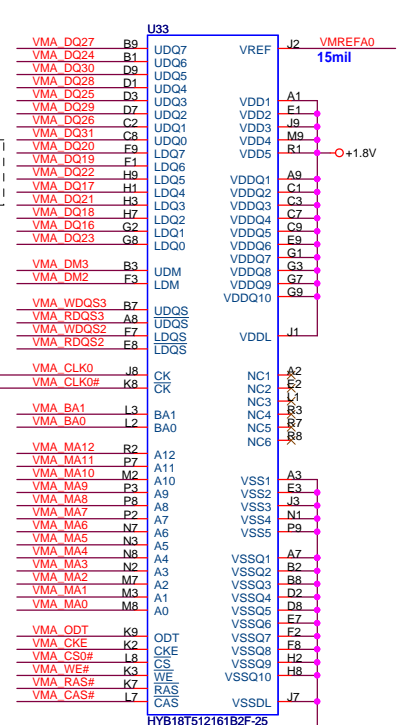
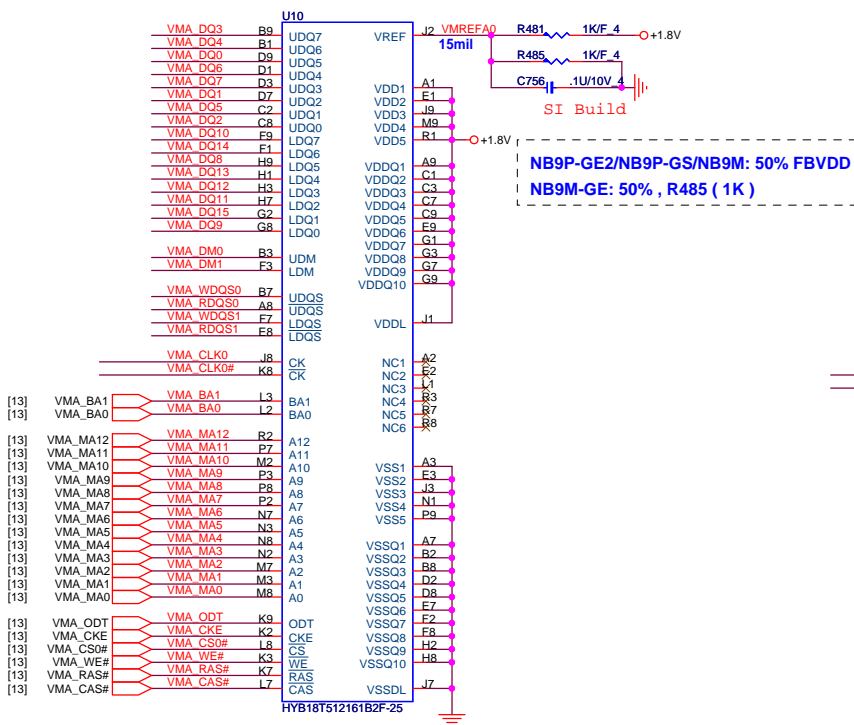
U30G

BGA969-NVIDIA-NB9P-GS

<SKU>

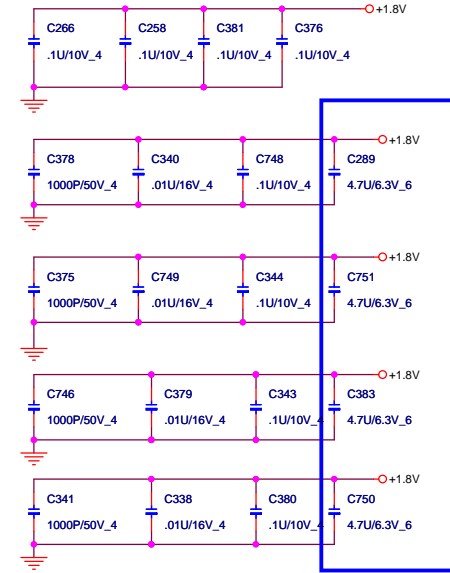


GROUND



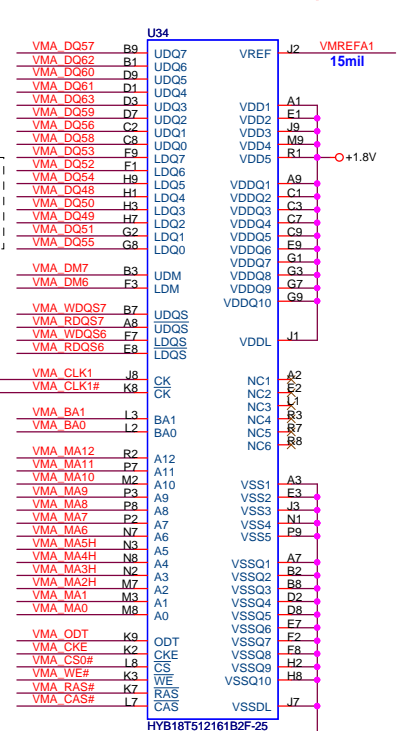
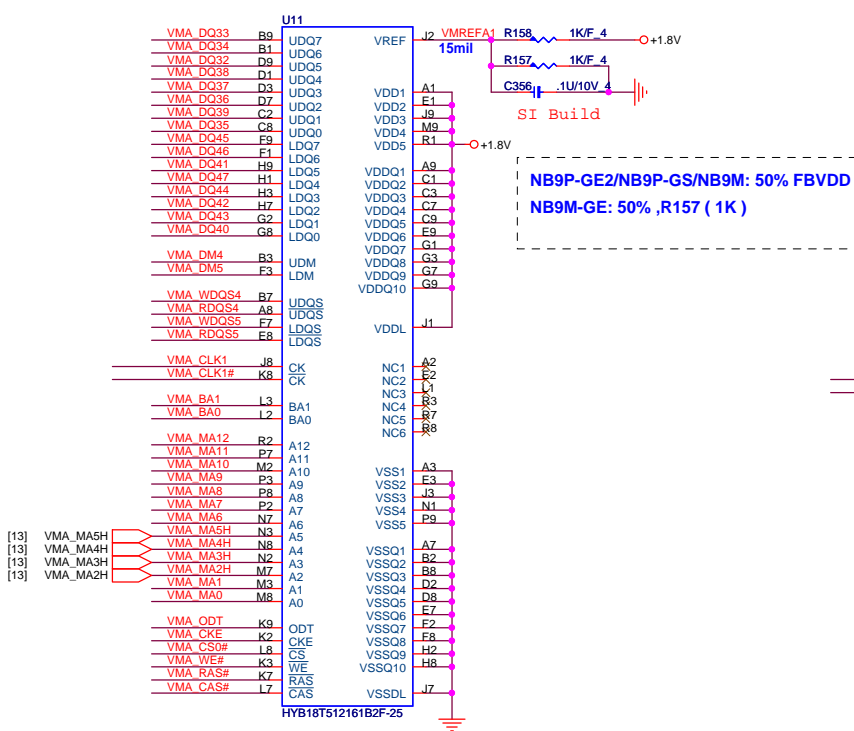
CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)



For DB:
 NB9P : AKD59G-T502(Samsung,32M*16)
 NB9M : AKD5FG-TW31(Hynix,32M*16)
 AKD5FG-T*03(Qimonda 32M*16)

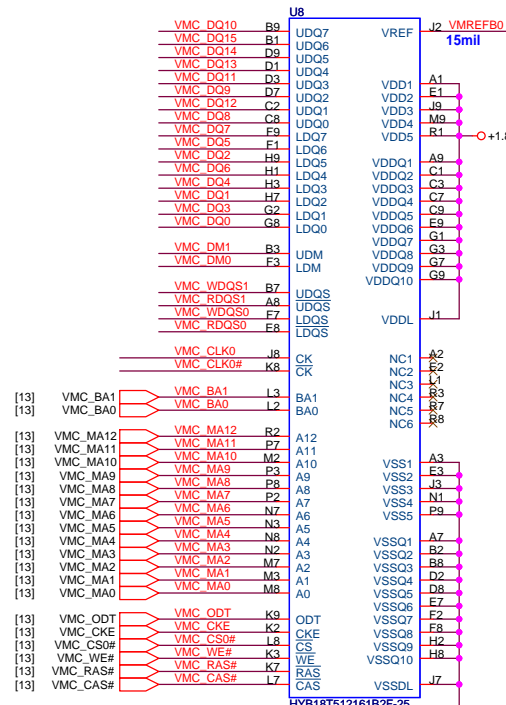
- [13] VMA_DQ[63..0]
 - [13] VMA_DM[7..0]
 - [13] VMA_WDQS[7..0]
 - [13] VMA_RDQS[7..0]
- 256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01



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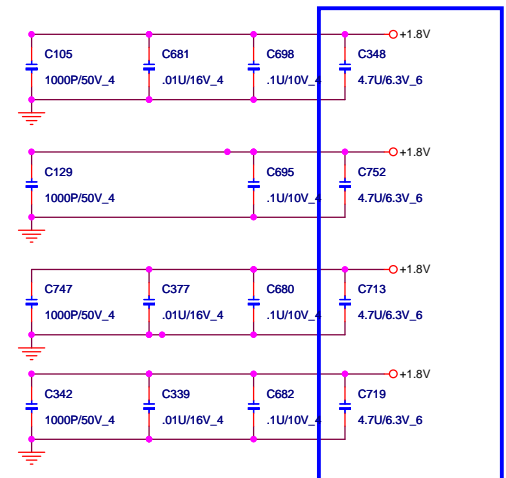
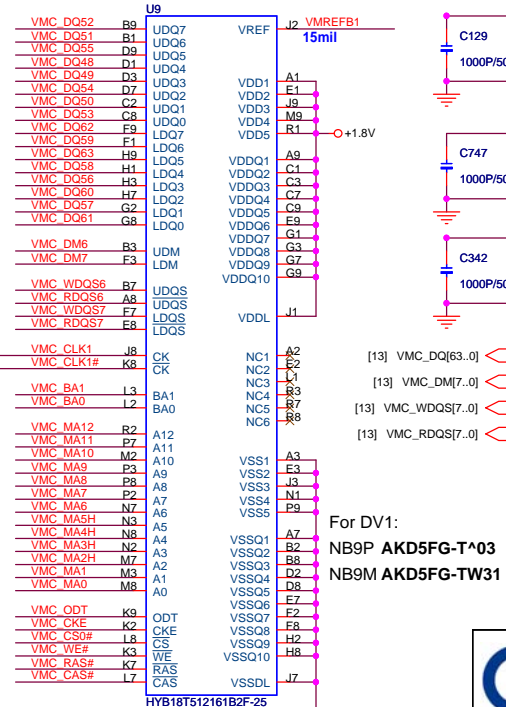
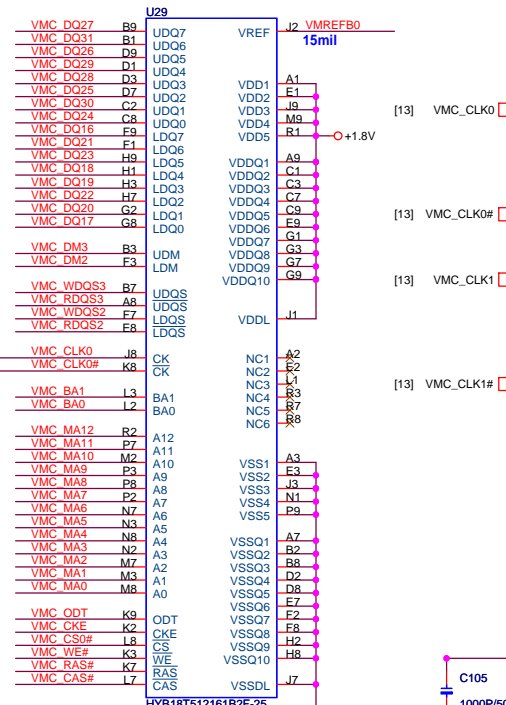
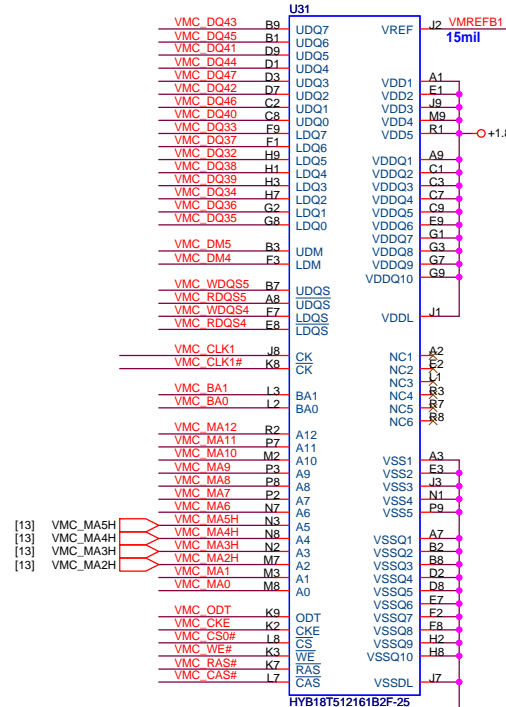
NB5

Size Custom	Document Number NV9X VRAM-1(GDDR2 BGA84)	Rev 3A
Date: Tuesday, April 08, 2008	Sheet 17 of 45	



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE:50% , R80 (1K)

NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50% ,R480 (1K)



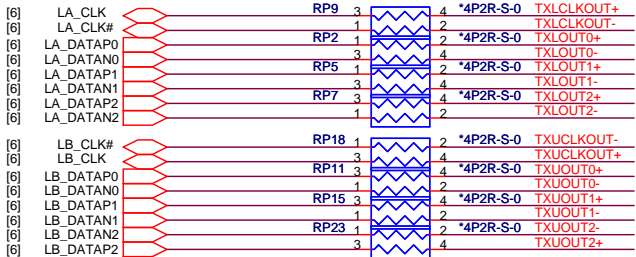
For DV1:
NB9P AKD5FG-T*03 IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) Qimonda
NB9M AKD5FG-TW31 IC SDRAM(84P) HY5PS121621CFP-25(FBGA) Hynix

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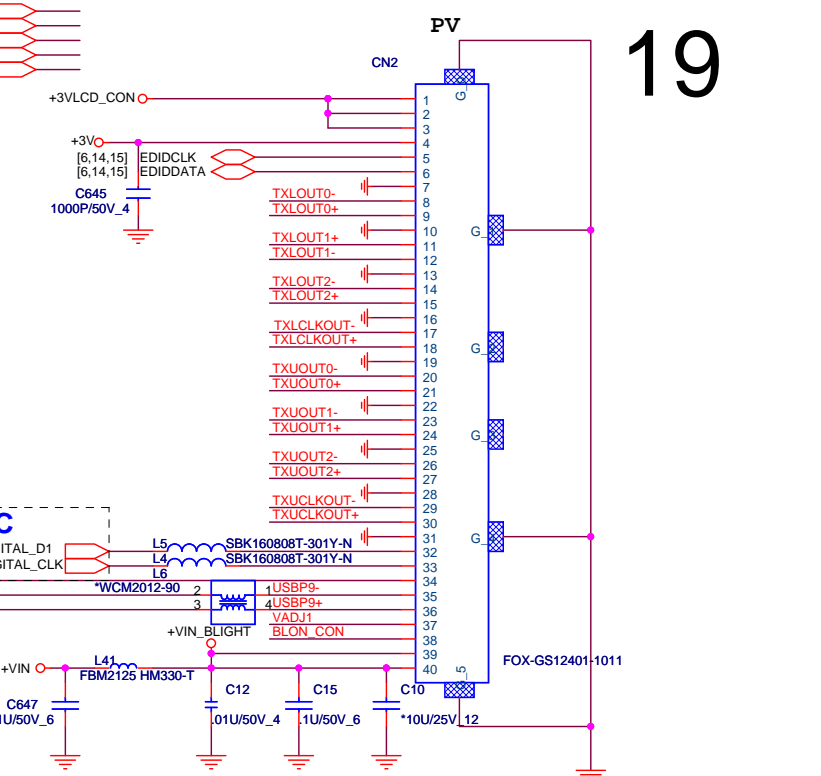
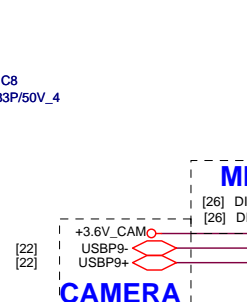
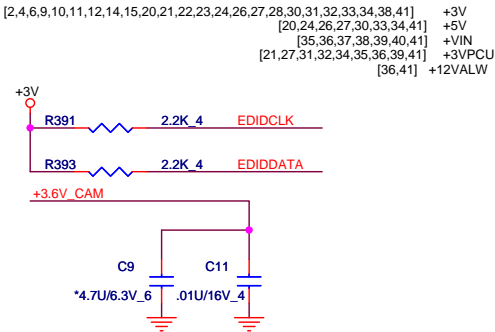
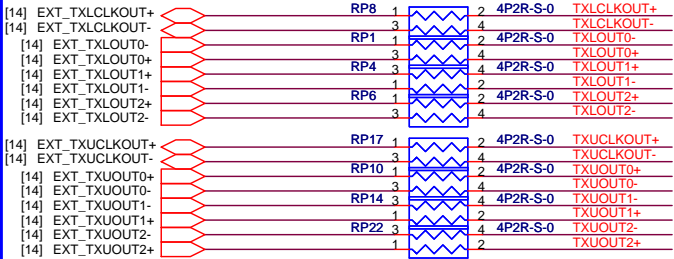
NB5	Size Custom	Document Number	Rev 3A
		NV9X VRAM-2(GDDR2 BGA84)	
Date: Tuesday, April 08, 2008		Sheet 18 of 45	

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

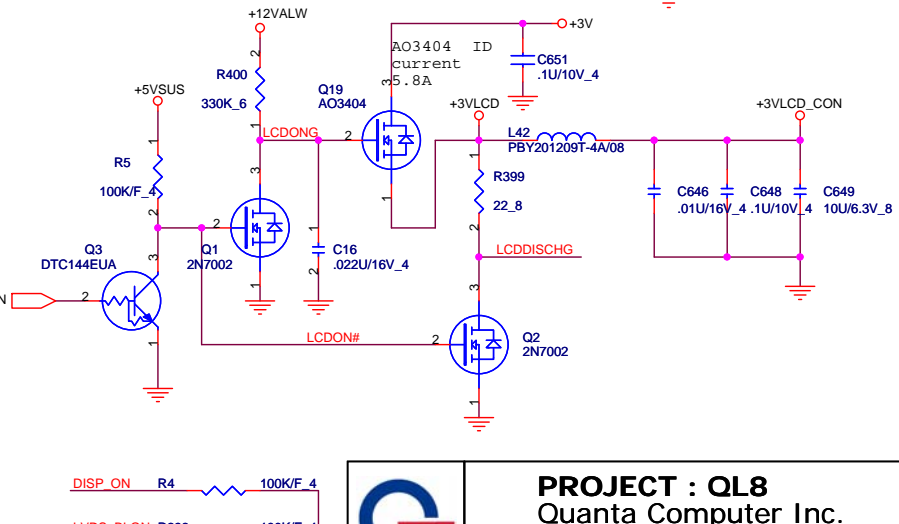
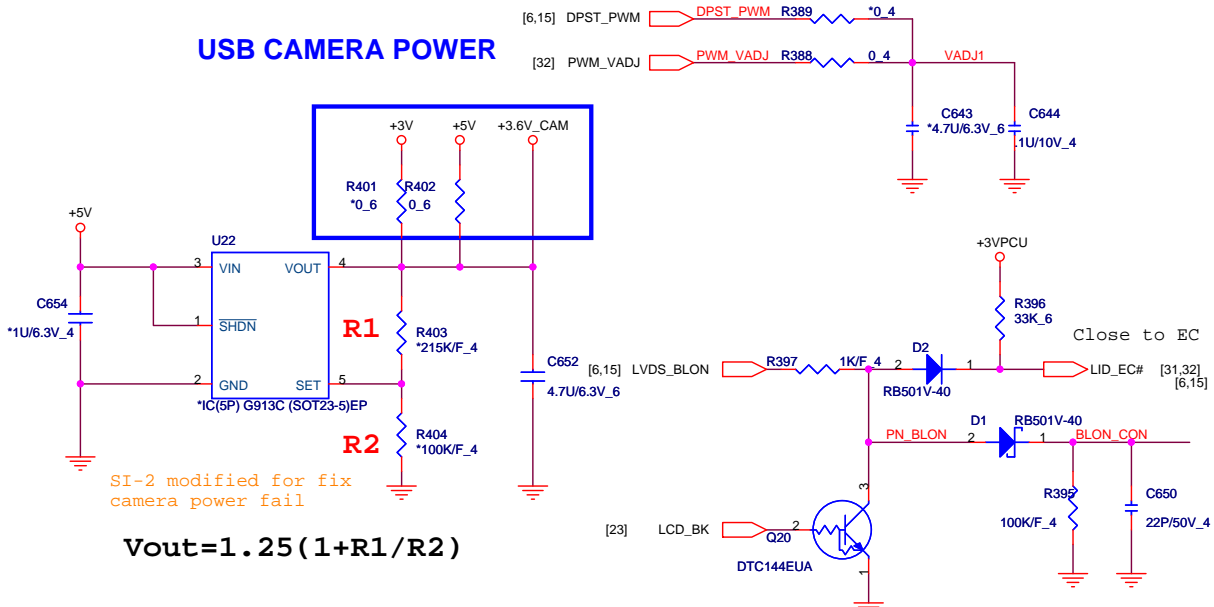
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

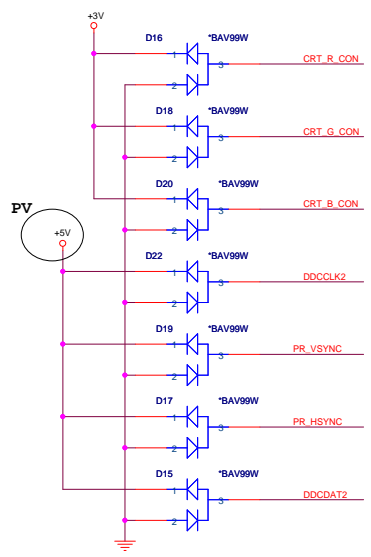
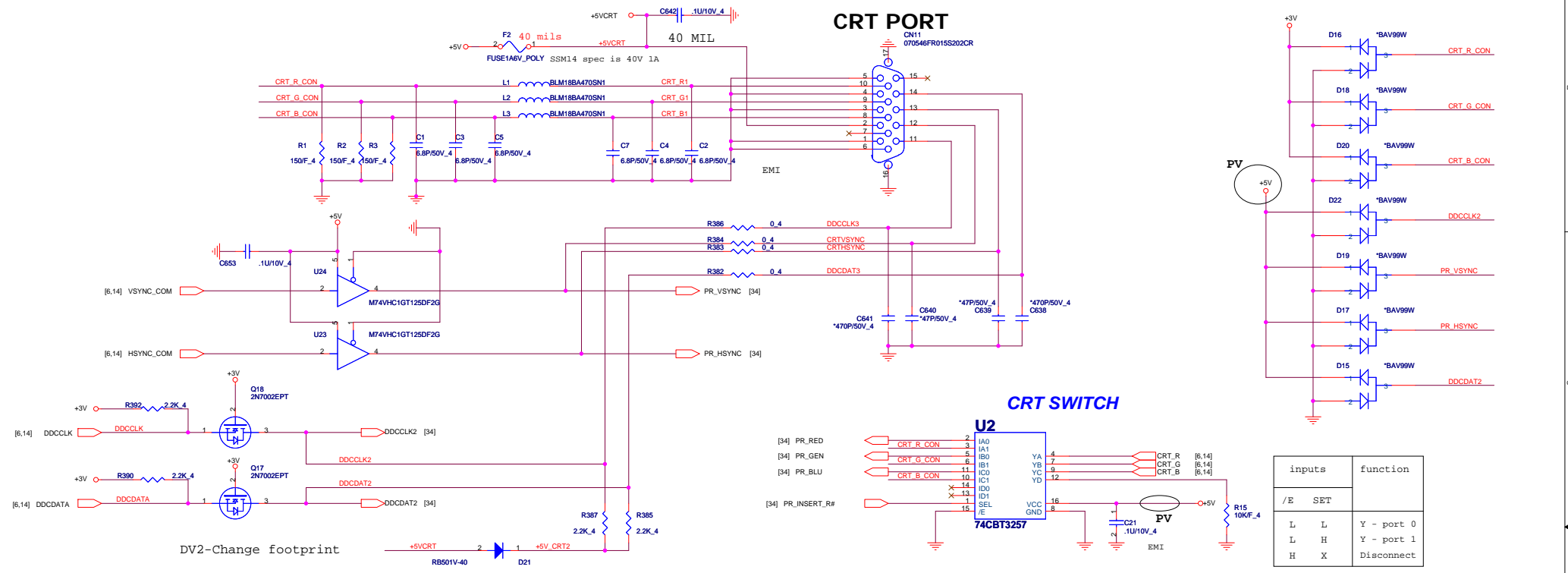


USB CAMERA POWER

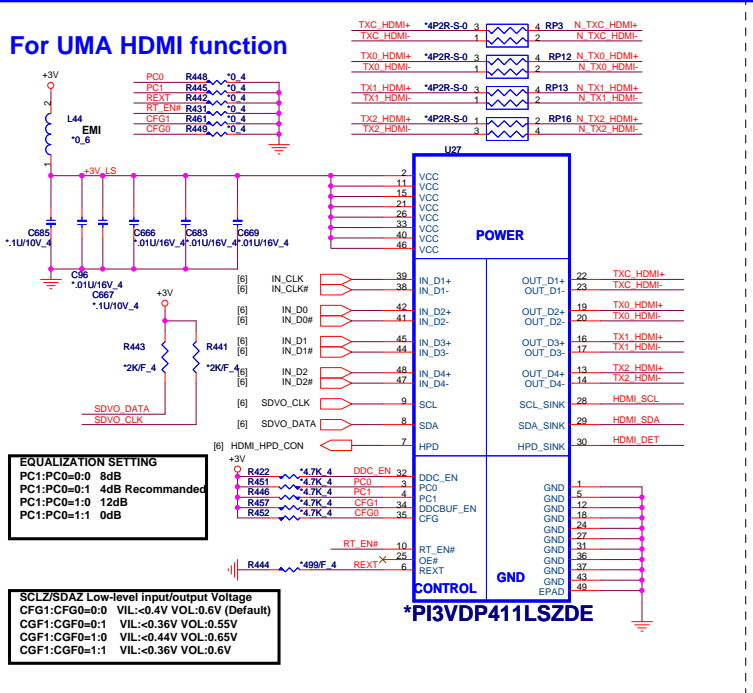


PROJECT : QL8
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Size B	Document Number LCD CONN/Lid function	Rev 3A
Date: Tuesday, April 08, 2008 Sheet 19 of 45		



inputs	function
/E SET	Y - port 0
L L	Y - port 1
L H	Y - port 1
H X	Disconnect

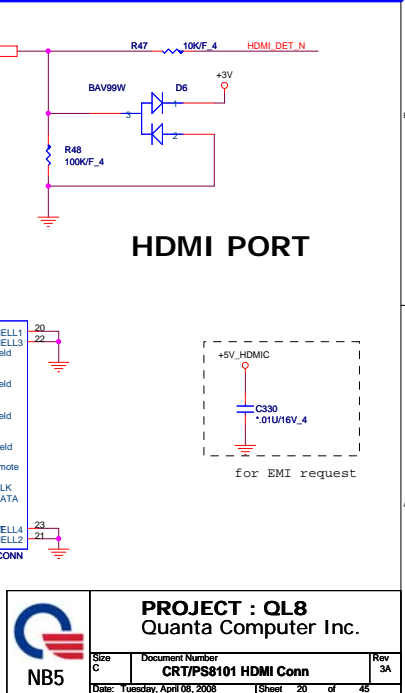
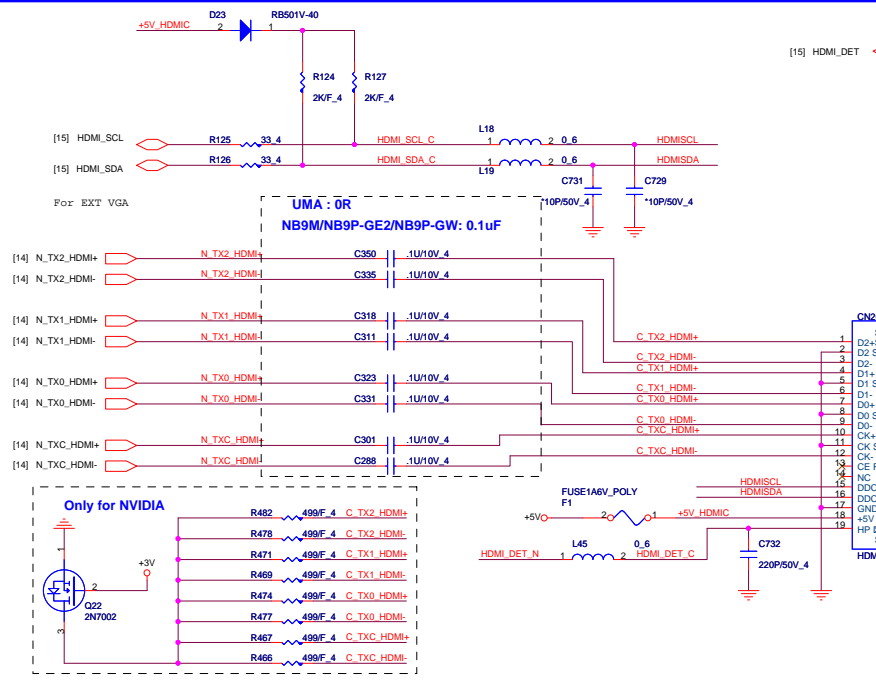


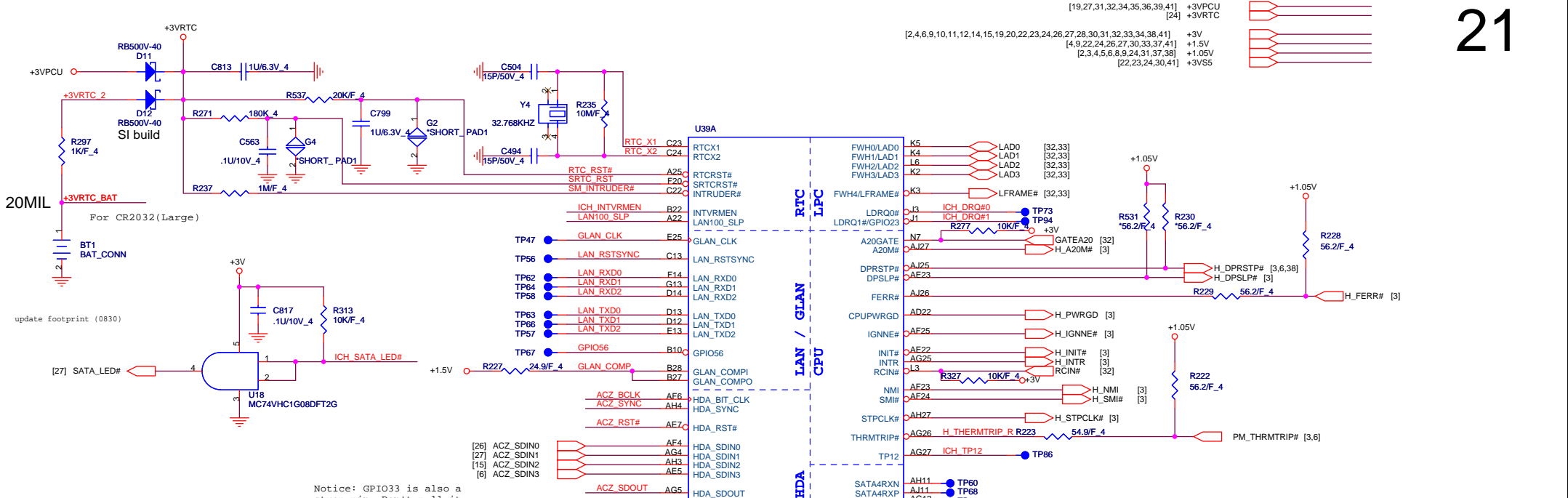
EQUALIZATION SETTING

PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage

CFG1:CFG0=0:0 VIL<-0.4V VOL:0.6V (Default)
 CFG1:CFG0=0:1 VIL<-0.36V VOL:0.55V
 CFG1:CFG0=1:0 VIL<-0.44V VOL:0.65V
 CFG1:CFG0=1:1 VIL<-0.36V VOL:0.5V





20MIL
For CR2032(Large)

update footprint (0830)

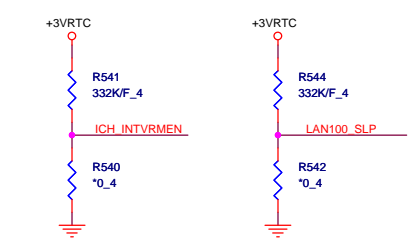
HP Request

SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for Vccsus1_05, Vccsus1_5 and VccCL1_5)

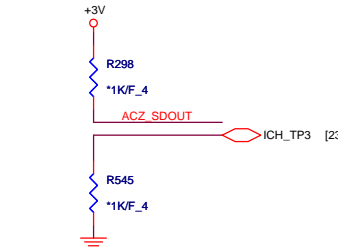
ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)	LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
----------	---	------------	---



XOR Chain Entrance Strap

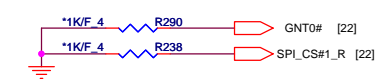
ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1



ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

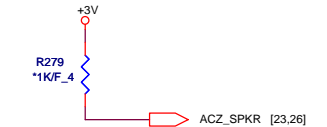


A16 swap override strap

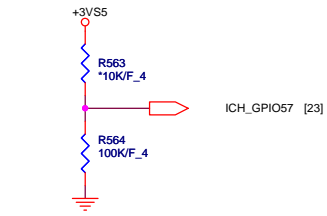
PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



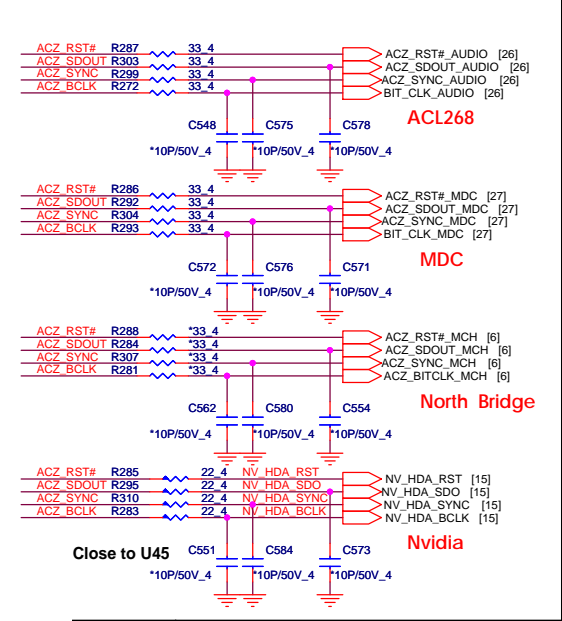
ACZ_SPKR	Low: Default Hi: No reboot
----------	-------------------------------



TPM physical presence	Low: Default
-----------------------	--------------



E-SATA CONNECT

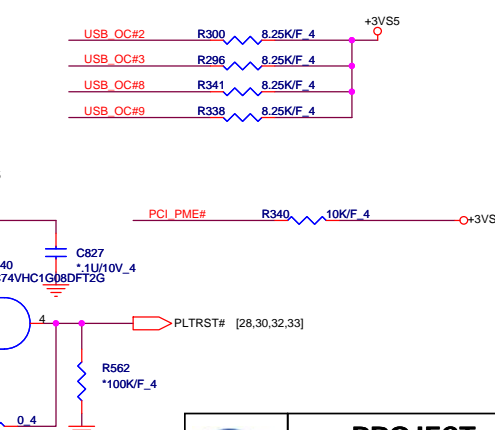
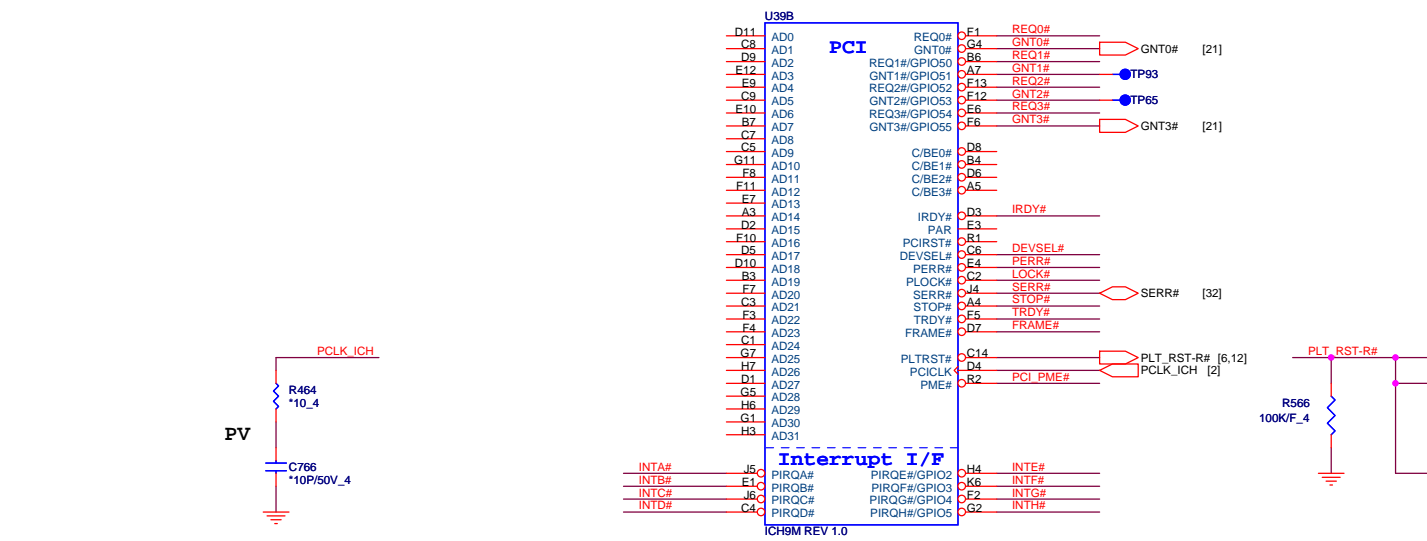
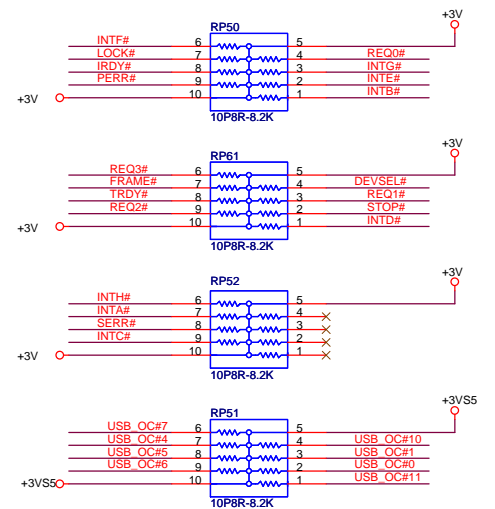
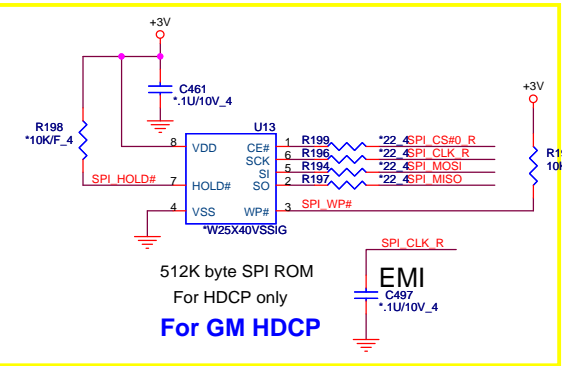
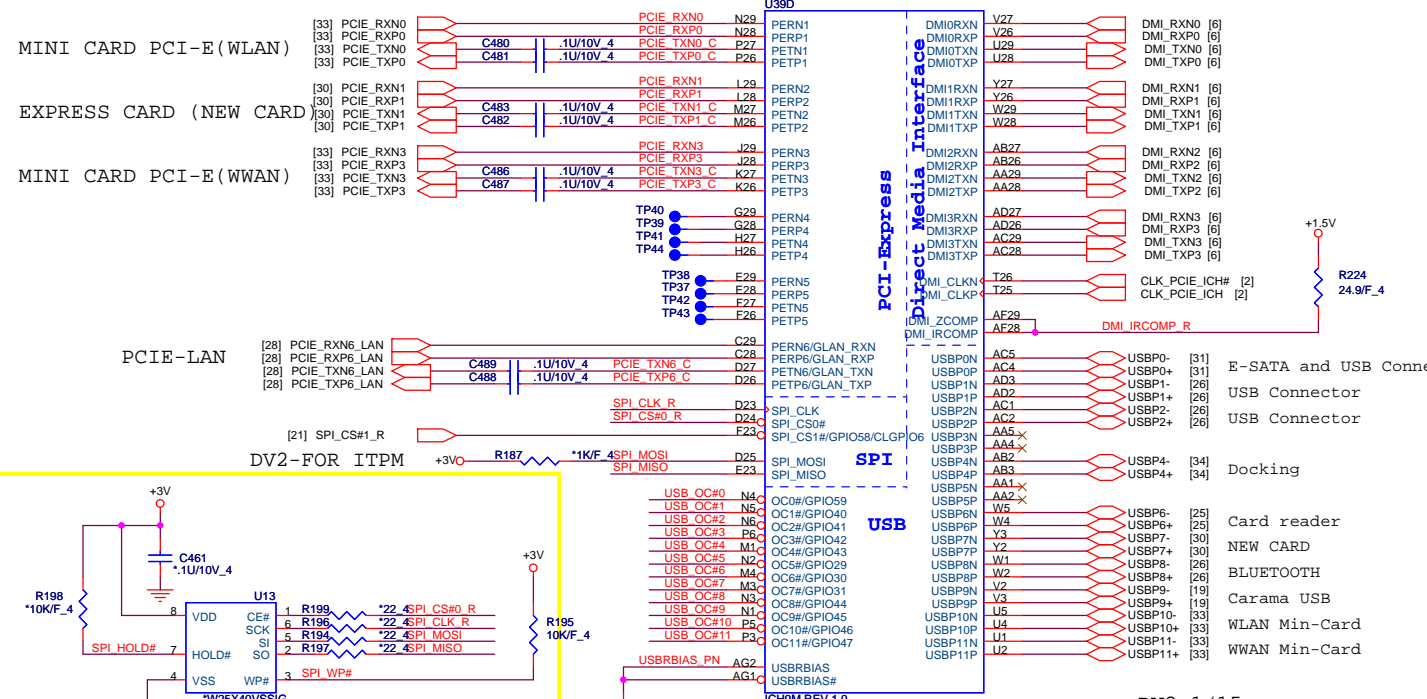


PROJECT : QL8
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Size Custom Document Number ICH9-M Host 1/4 Rev 3A

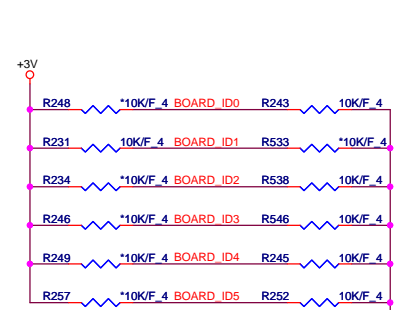
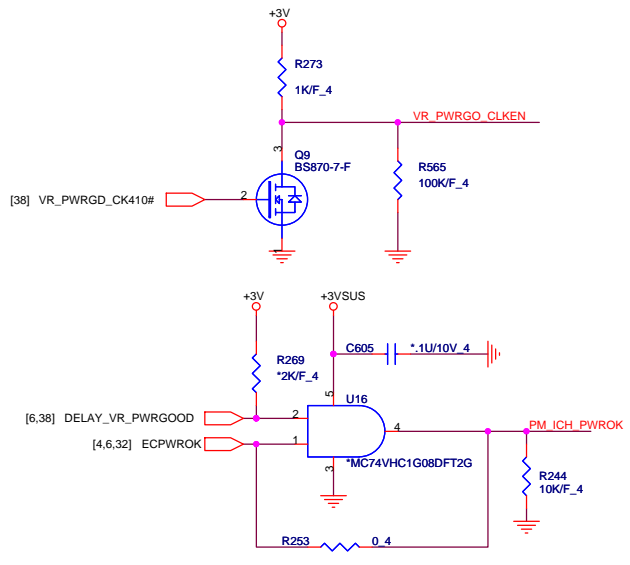
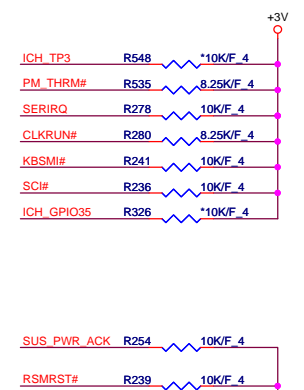
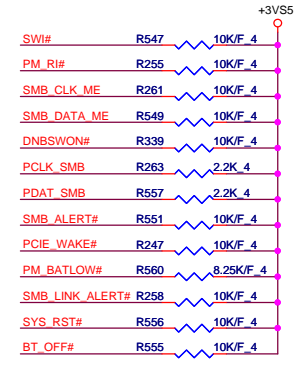
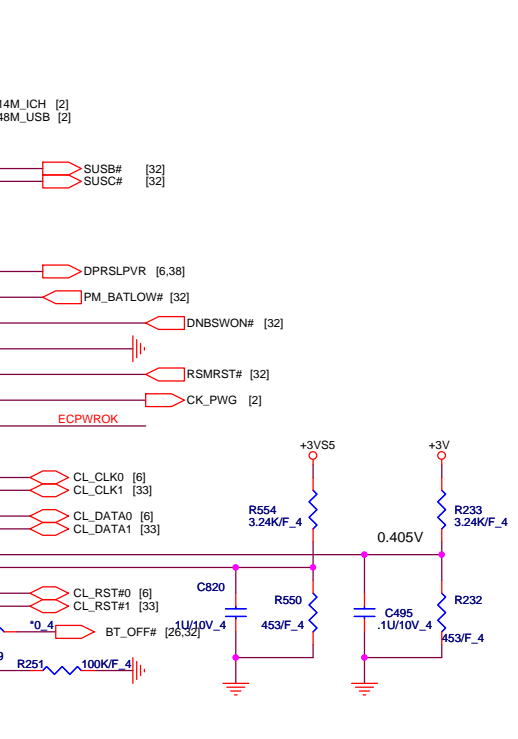
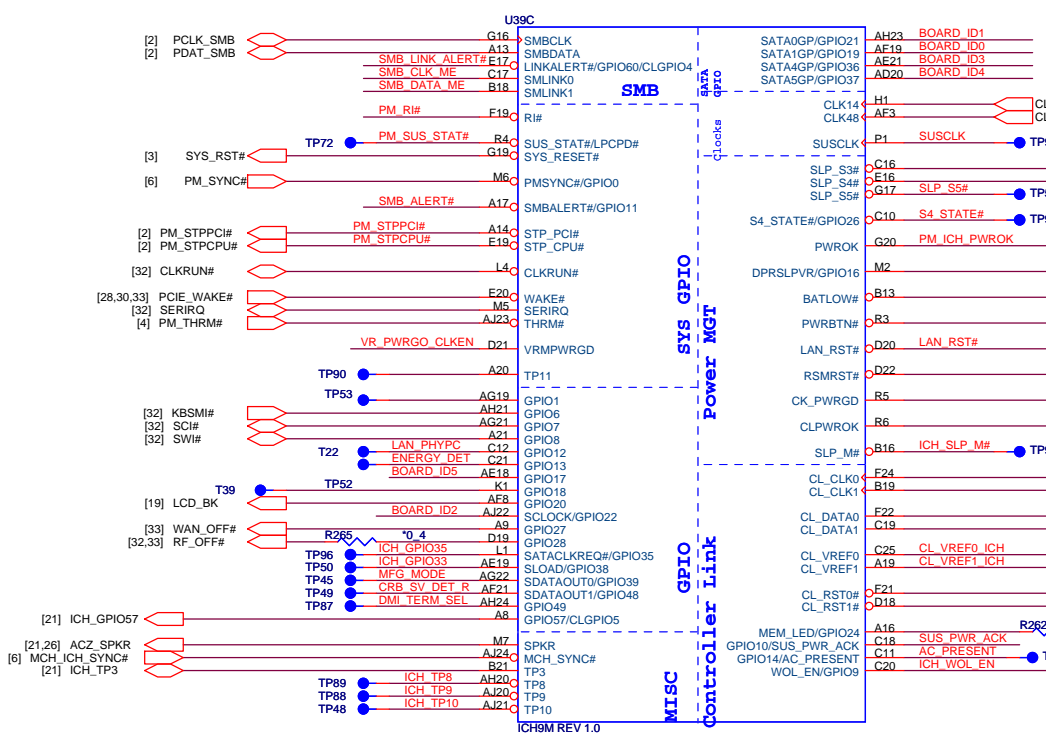
Date: Tuesday, April 08, 2008 Sheet 21 of 45

[2,4,6,9,10,11,12,14,15,19,20,21,23,24,26,27,28,30,31,32,33,34,38,41] +1.5V
[4,9,21,24,26,27,30,33,37,41] +3V
[23,25,26,33,37,39,41] +3VSUS



PROJECT : QL8
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NB5
Size Custom Document Number ICH9-M PCIE 2/4 Rev 3A
Date: Tuesday, April 08, 2008 Sheet 22 of 45

[4,9,21,22,24,26,27,30,33,37,41] +1.5V
 [2,4,6,9,10,11,12,14,15,19,20,21,22,24,26,27,28,30,31,32,33,34,38,41] +3V
 [21,22,24,30,41] +3VS5
 [25,26,33,37,39,41] +3VSUS



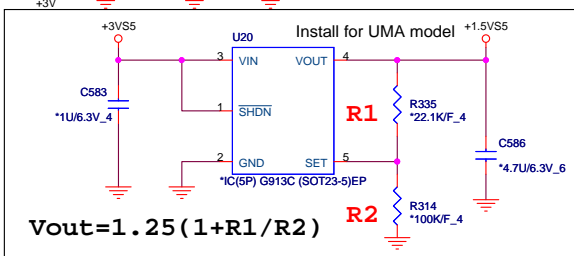
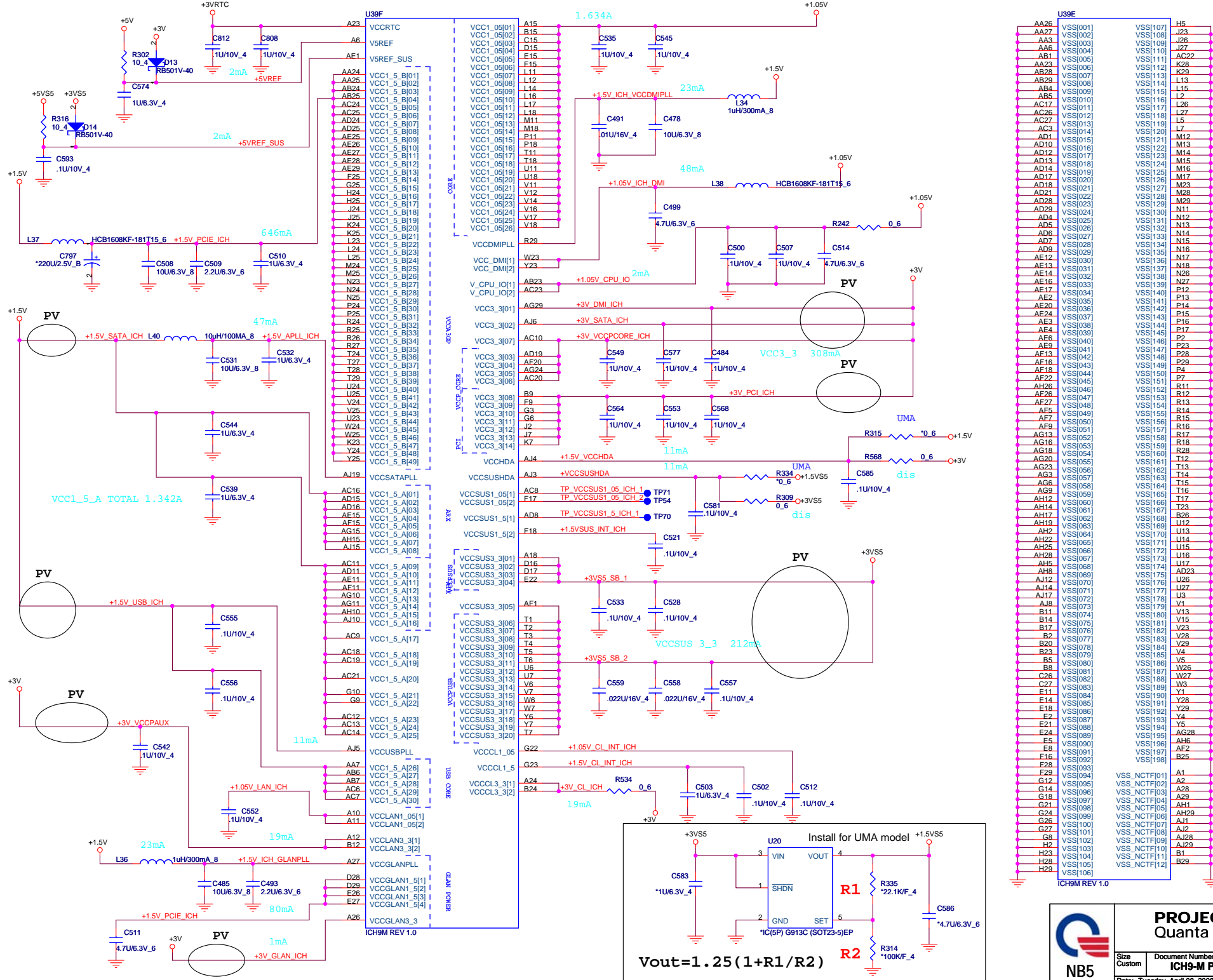
DV2 change Board ID

	Board ID 3	ID 2	ID 1	ID 0
QL8 UMA	0	0	0	0
9M	0	0	0	1
9P	0	0	1	0

	Board ID 3	ID 2	ID 1	ID 0
TW8 UMA	0	1	0	1
9M	0	1	1	0
9P	0	1	1	1

PROJECT : QL8
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Size Custom	Document Number ICH9-M GPIO 3/4	Rev 3A
Date: Tuesday, April 08, 2008		
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U93E

AA26	VSS1001	VSS1077	H5
AA27	VSS1002	VSS1088	J23
AA3	VSS1003	VSS1099	J26
AA6	VSS1004	VSS1100	K22
AA11	VSS1005	VSS1111	K28
AA23	VSS1006	VSS1122	L13
AB28	VSS1007	VSS1133	L13
AB29	VSS1008	VSS1144	L12
AB4	VSS1009	VSS1155	L26
AB16	VSS1010	VSS1166	L26
AC17	VSS1011	VSS1177	L27
AC26	VSS1012	VSS1188	L5
AC27	VSS1013	VSS1199	L7
AC3	VSS1014	VSS1200	M12
AD10	VSS1015	VSS1211	M13
AD11	VSS1016	VSS1222	M14
AD12	VSS1017	VSS1233	M15
AD13	VSS1018	VSS1244	M16
AD14	VSS1019	VSS1255	M17
AD17	VSS1020	VSS1266	M23
AD18	VSS1021	VSS1277	M28
AD21	VSS1022	VSS1288	M29
AD28	VSS1023	VSS1299	M30
AD29	VSS1024	VSS1300	N12
AD5	VSS1025	VSS1311	N13
AD6	VSS1026	VSS1322	N14
AD7	VSS1027	VSS1333	N15
AD9	VSS1028	VSS1344	N16
AE12	VSS1029	VSS1355	N17
AE13	VSS1030	VSS1366	N18
AE14	VSS1031	VSS1377	N19
AE16	VSS1032	VSS1388	N26
AE17	VSS1033	VSS1399	N27
AE2	VSS1034	VSS1400	P12
AE20	VSS1035	VSS1411	P13
AE21	VSS1036	VSS1422	P14
AE24	VSS1037	VSS1433	P15
AE3	VSS1038	VSS1444	P16
AE4	VSS1039	VSS1455	P17
AE9	VSS1040	VSS1466	P2
AF13	VSS1041	VSS1477	P23
AF16	VSS1042	VSS1488	P28
AF18	VSS1043	VSS1499	P29
AF22	VSS1044	VSS1500	P4
AF26	VSS1045	VSS1511	P11
AF27	VSS1046	VSS1522	P12
AF7	VSS1047	VSS1533	P13
AF9	VSS1048	VSS1544	P14
AG13	VSS1049	VSS1555	P15
AG16	VSS1050	VSS1566	P16
AG18	VSS1051	VSS1577	P17
AG23	VSS1052	VSS1588	P18
AG3	VSS1053	VSS1599	P2
AG6	VSS1054	VSS1600	P23
AH12	VSS1055	VSS1611	P28
AH14	VSS1056	VSS1622	P29
AH17	VSS1057	VSS1633	P4
AH19	VSS1058	VSS1644	P11
AH22	VSS1059	VSS1655	P12
AH25	VSS1060	VSS1666	P13
AH28	VSS1061	VSS1677	P14
AH5	VSS1062	VSS1688	P15
AH8	VSS1063	VSS1699	P16
AH11	VSS1064	VSS1700	P17
AH13	VSS1065	VSS1711	P18
AH14	VSS1066	VSS1722	P19
AH17	VSS1067	VSS1733	T12
AH19	VSS1068	VSS1744	T13
AH22	VSS1069	VSS1755	T14
AH24	VSS1070	VSS1766	T15
AH27	VSS1071	VSS1777	T16
AH8	VSS1072	VSS1788	T17
B1	VSS1073	VSS1799	T18
B14	VSS1074	VSS1800	T2
B17	VSS1075	VSS1811	T23
B23	VSS1076	VSS1822	V23
B2	VSS1077	VSS1833	V28
B20	VSS1078	VSS1844	V29
B23	VSS1079	VSS1855	V4
B5	VSS1080	VSS1866	V5
B8	VSS1081	VSS1877	W26
C26	VSS1082	VSS1888	W27
C27	VSS1083	VSS1899	W3
E11	VSS1084	VSS1900	Y1
E14	VSS1085	VSS1911	Y28
E18	VSS1086	VSS1922	Y4
E2	VSS1087	VSS1933	Y5
E21	VSS1088	VSS1944	AC28
E5	VSS1089	VSS1955	AH6
E8	VSS1090	VSS1966	AF2
F16	VSS1091	VSS1977	B25
F28	VSS1092	VSS1988	
F29	VSS1093	VSS1999	A1
G12	VSS1094	VSS2000	A2
G14	VSS1095	VSS2001	A28
G18	VSS1096	VSS2002	A29
G21	VSS1097	VSS2003	AH1
G24	VSS1098	VSS2004	AH29
G26	VSS1099	VSS2005	AJ1
G27	VSS1100	VSS2006	AJ2
H2	VSS1101	VSS2007	AJ28
H23	VSS1102	VSS2008	AJ29
H28	VSS1103	VSS2009	B1
H29	VSS1104	VSS2010	B29
H29	VSS1105	VSS2011	
H29	VSS1106	VSS2012	

ICH9M REV 1.0



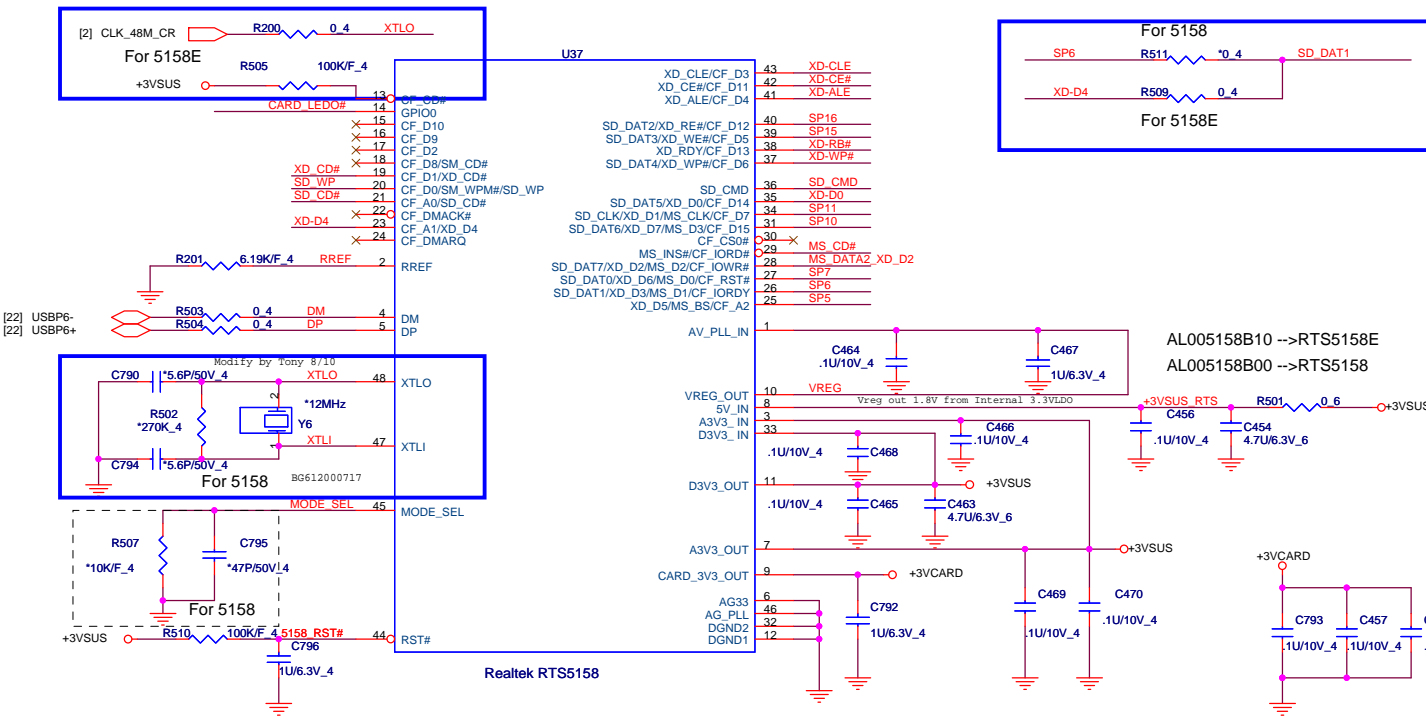
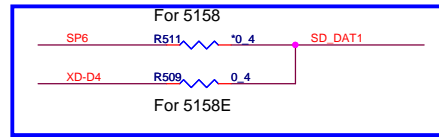
PROJECT : QL8
Quanta Computer Inc.

Note:

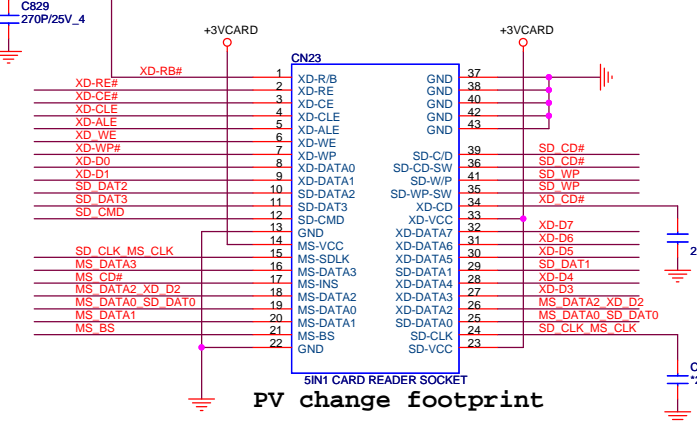
SD/MMMC	MS	XD
SP0		XD CD#
SP1	SD WP	XD CD#
SP2	SD CD#	
SP3	SD CD#	
SP4	SD DAT1	XD D4
SP5	MS BS	XD D5
SP6	SD DAT1	MS D1
SP7	SD DAT0	MS D0
SP8	SD DAT7	MS D2
SP9	MS INS#	
SP10	SD DAT6	MS D3
SP11	SD CLK	MS SCLK
SP12	SD DAT5	XD D0
SP13	SD DAT4	XD WP#
SP14		XD R/B#
SP15	SD DAT3	XD WE#
SP16	SD DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

For RTS5158

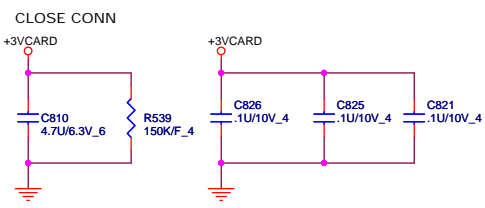
SP7	R525	0.4	MS DATA0	XD DAT0
	R526	0.4		XD D6
SP6	R527	0.4	MS DATA1	XD D3
	R528	0.4		XD D3
SP16	R514	0.4	SD DAT2	
	R513	0.4		XD RE#
SP5	R515	0.4	MS BS	
	R516	0.4		XD D5
SP15	R520	0.4	SD DAT3	
	R517	0.4		XD WE
SP11	R522	0.4	SD CLK	MS CLK
	R521	0.4		XD D1
SP10	R523	0.4	MS DATA3	
	R524	0.4		XD D7



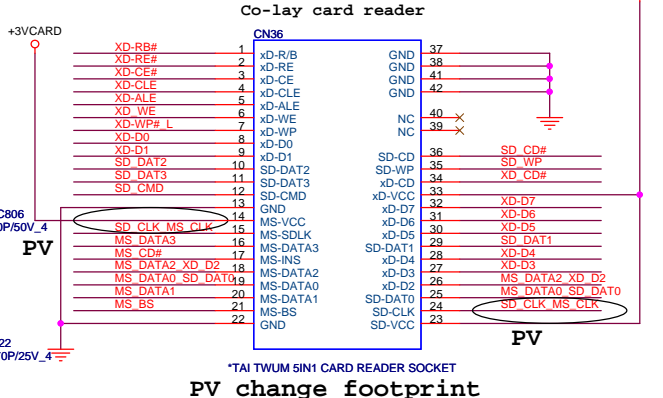
5 IN1 CARD READER
XD, MMC/SD, MS/MSP



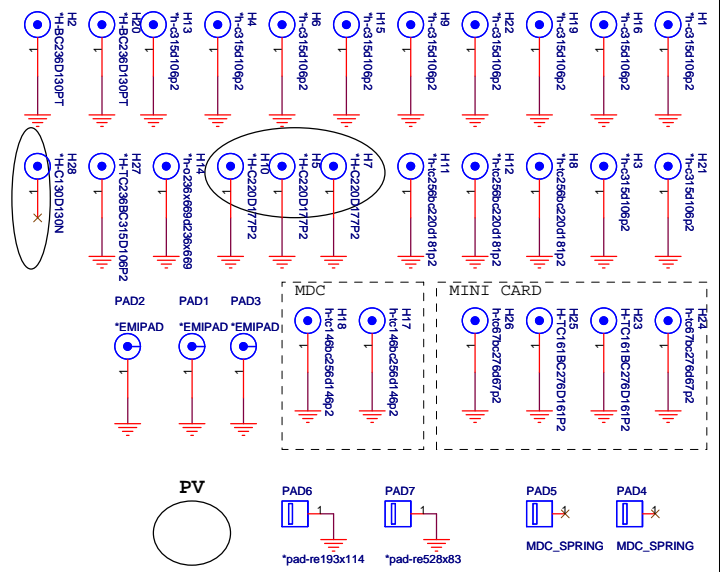
PV change footprint



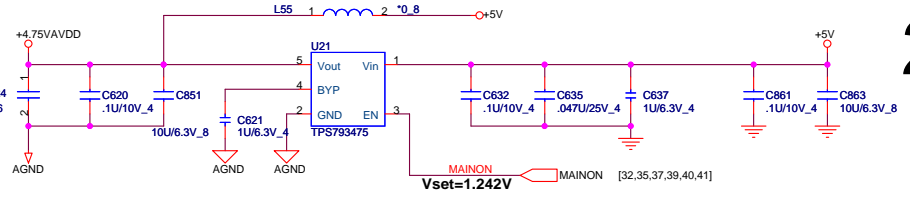
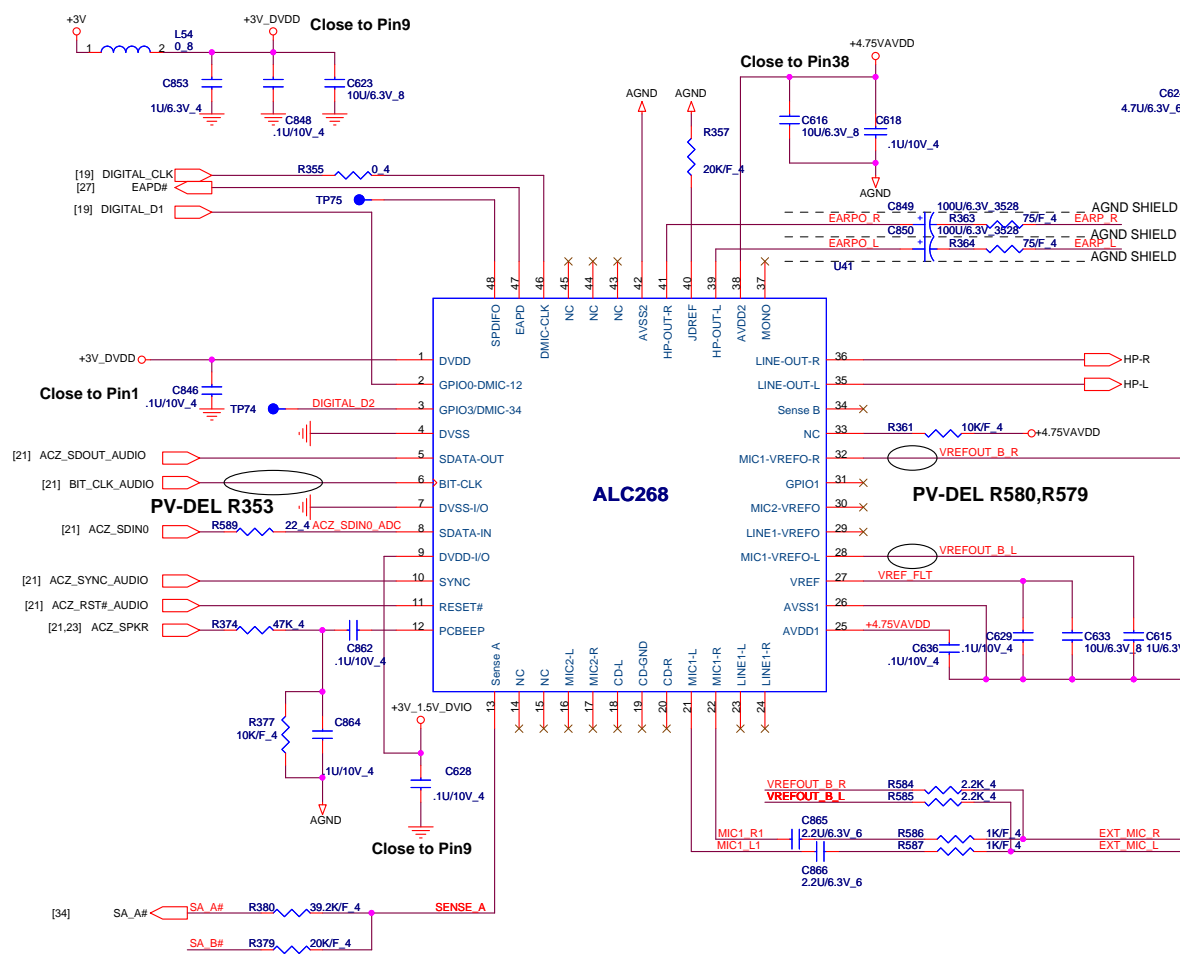
5 IN1 CARD READER
XD, MMC/SD, MS/MSP



PV change footprint

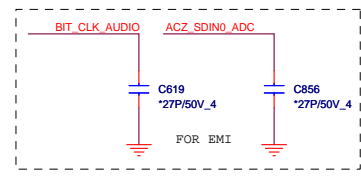


PROJECT : QL8
Quanta Computer Inc.

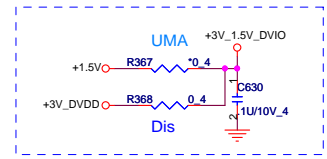


TO Headphone jack

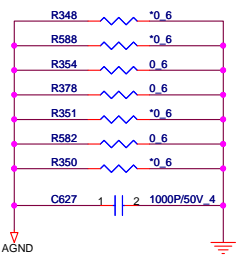
TO Internal Speakers



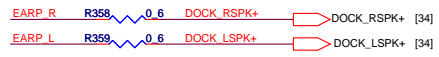
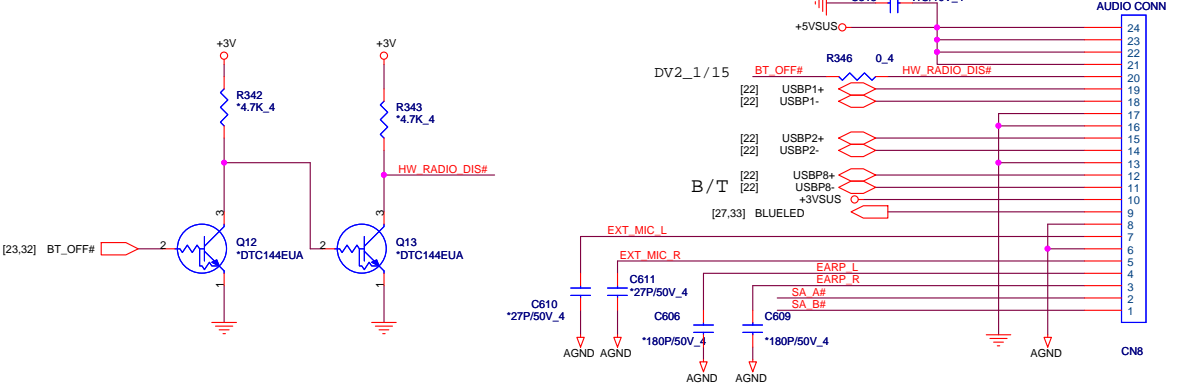
PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	X
PORT F	X
DM	DIGITAL MIC



TO Audio Jack MIC

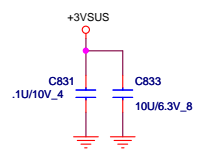


TO AUDIO/B CON.



BLUETOOTH

Audio

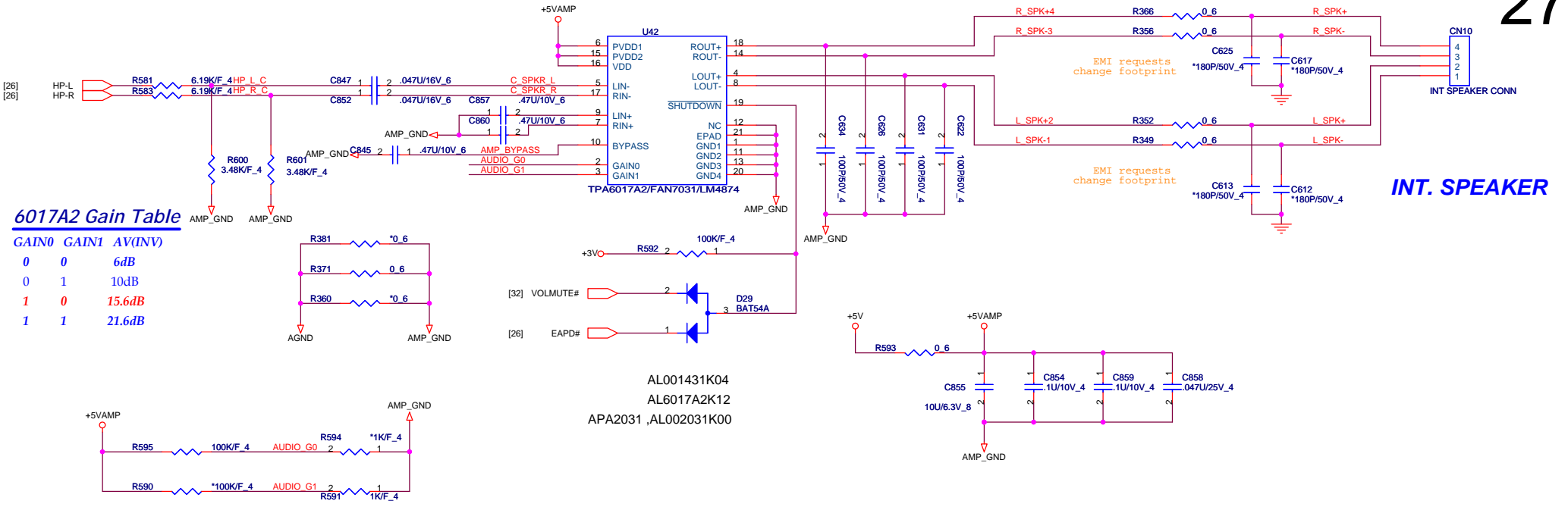


SA_A# -->EXT HP
SA_B# -->EXT MIC
Audio JACK: Normal Open

PROJECT : QL8
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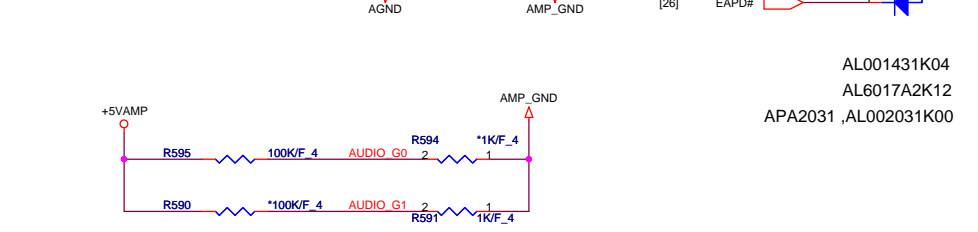
Size Custom	Document Number Azalia ALC268	Rev 3A
Date: Tuesday, April 08, 2008		
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AUDIO AMPLIFIER

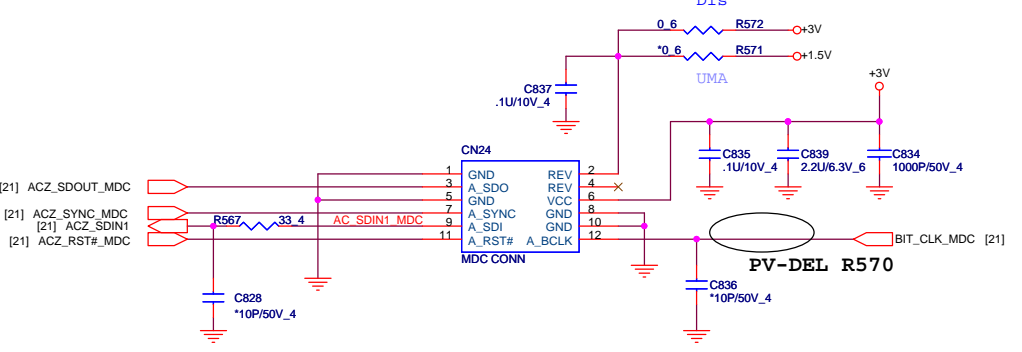


6017A2 Gain Table

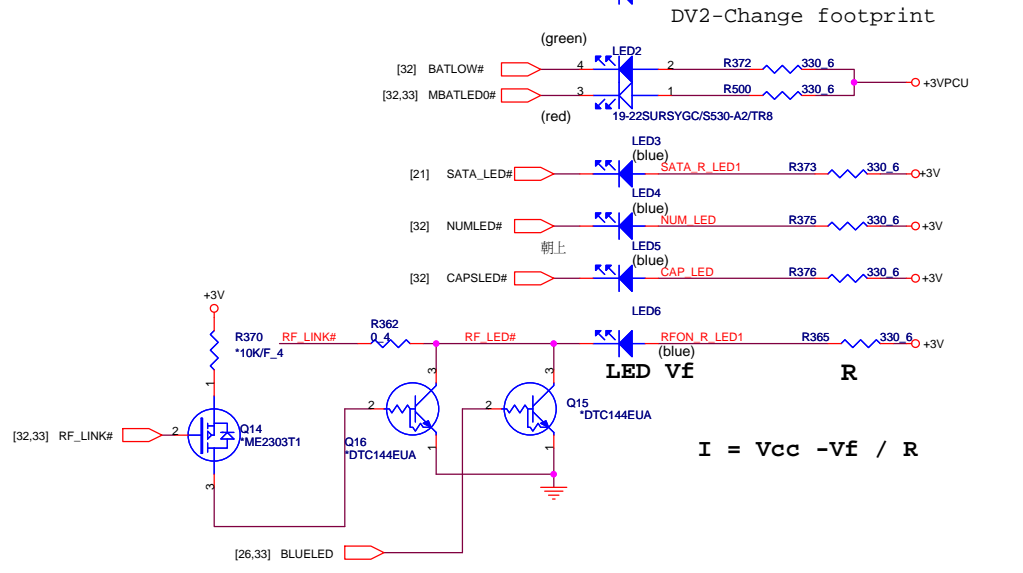
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



MDC CONNECTOR



LED

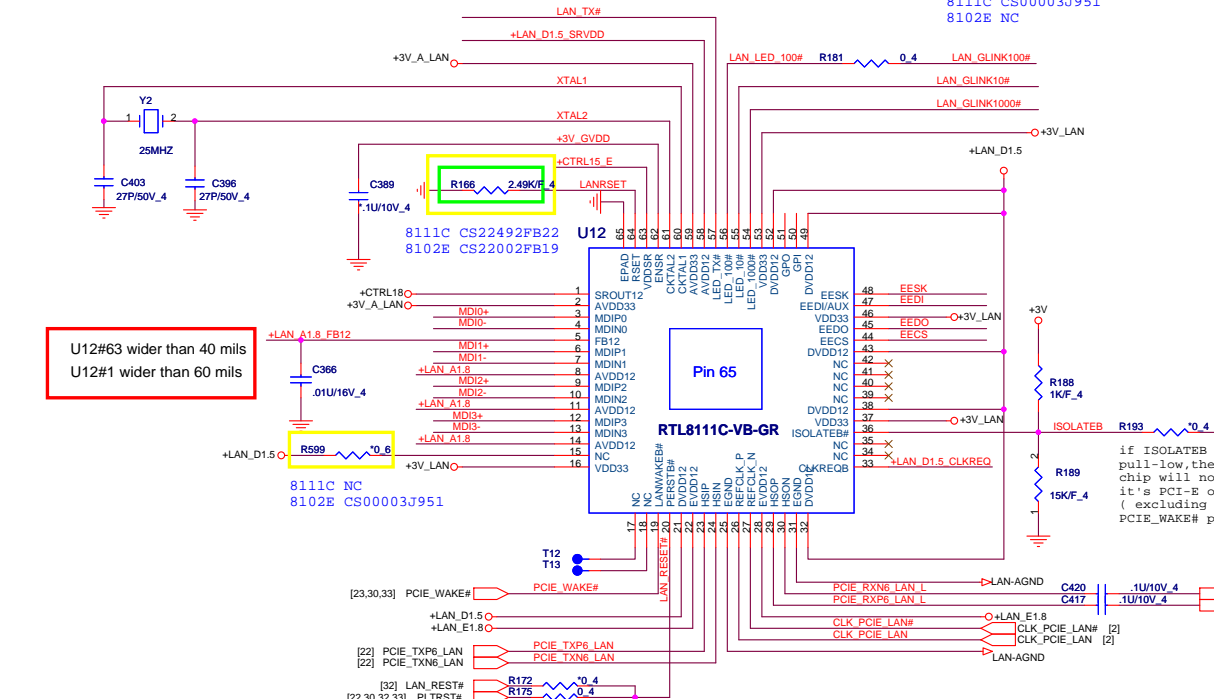
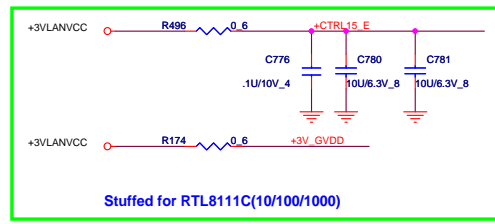


PROJECT : QL8
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA6017/Accelerometer	Rev 3A
Date: Tuesday, April 08, 2008		Sheet 27 of 45

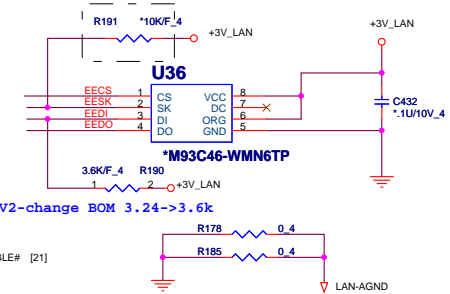
T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8102E(10/100)

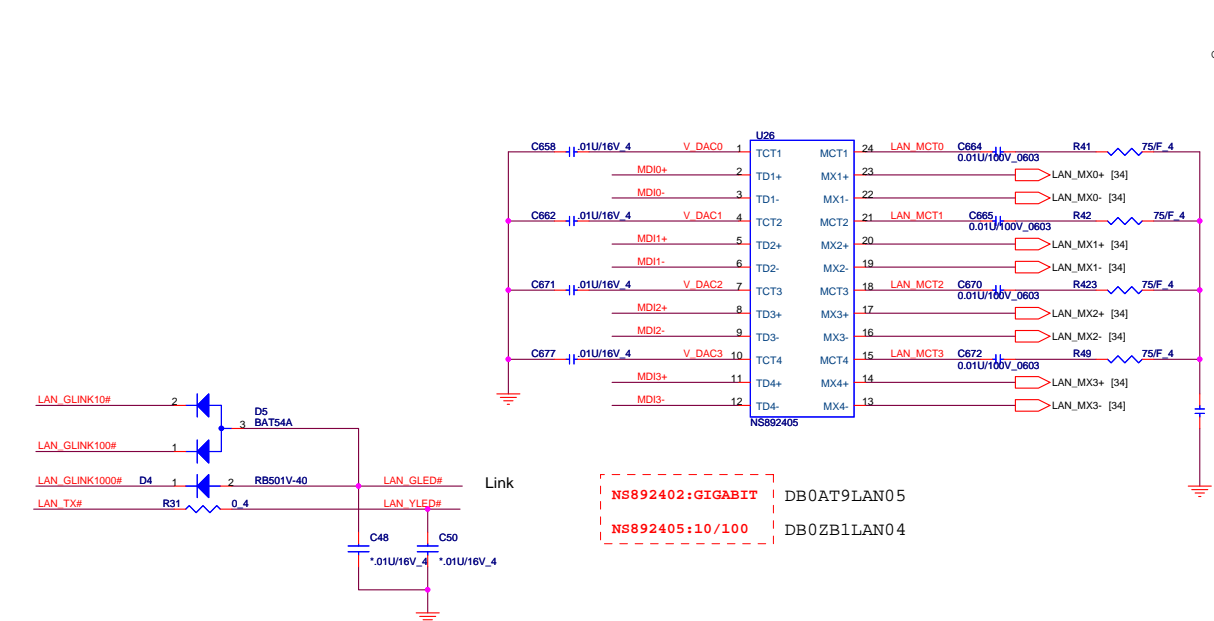


U12#63 wider than 40 mils
U12#1 wider than 60 mils

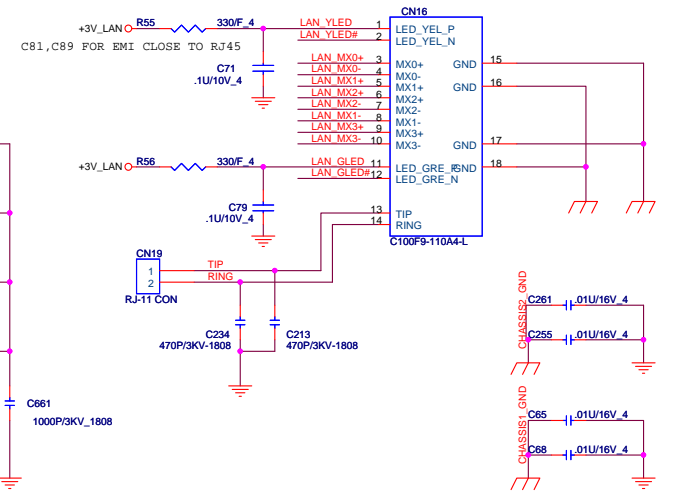
for 93C56 used. NC if 93C46 is used.



GIGABIT	AL08111C001	RTL8111C-VB-GR (QFN)
10/100	AL08102E001	RTL8102E-VB-GR
	AL08101E005	TL8101E-GR (QFN)



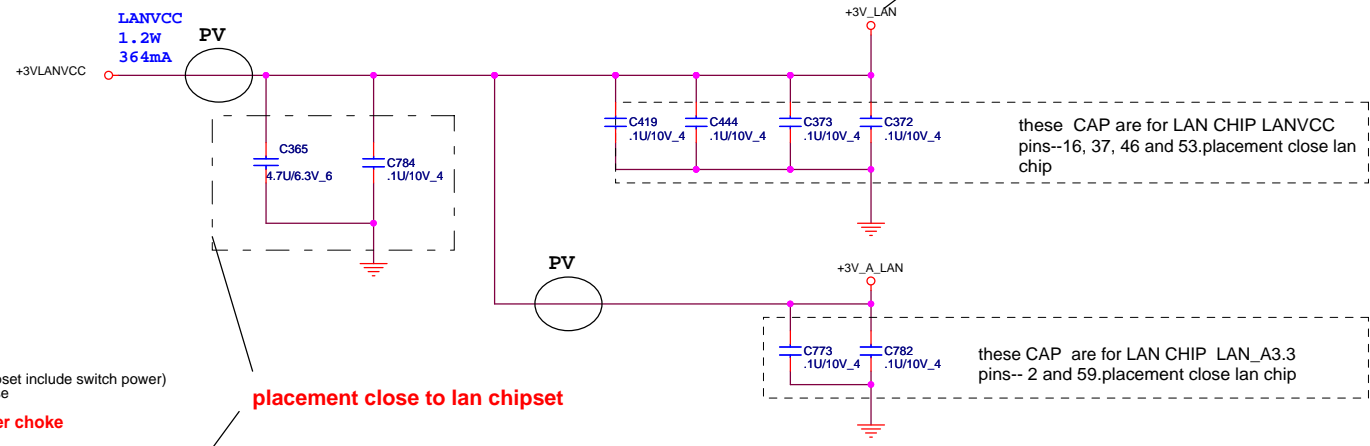
RJ45



	PROJECT : QL8	
	Quanta Computer Inc.	
Size Custom	Document Number RTL8111C/8102E/RJ45	Rev 3A
Date: Tuesday, April 08, 2008	Sheet 28 of 45	

T : Stuffed for RTL8111C(10/100/1000)

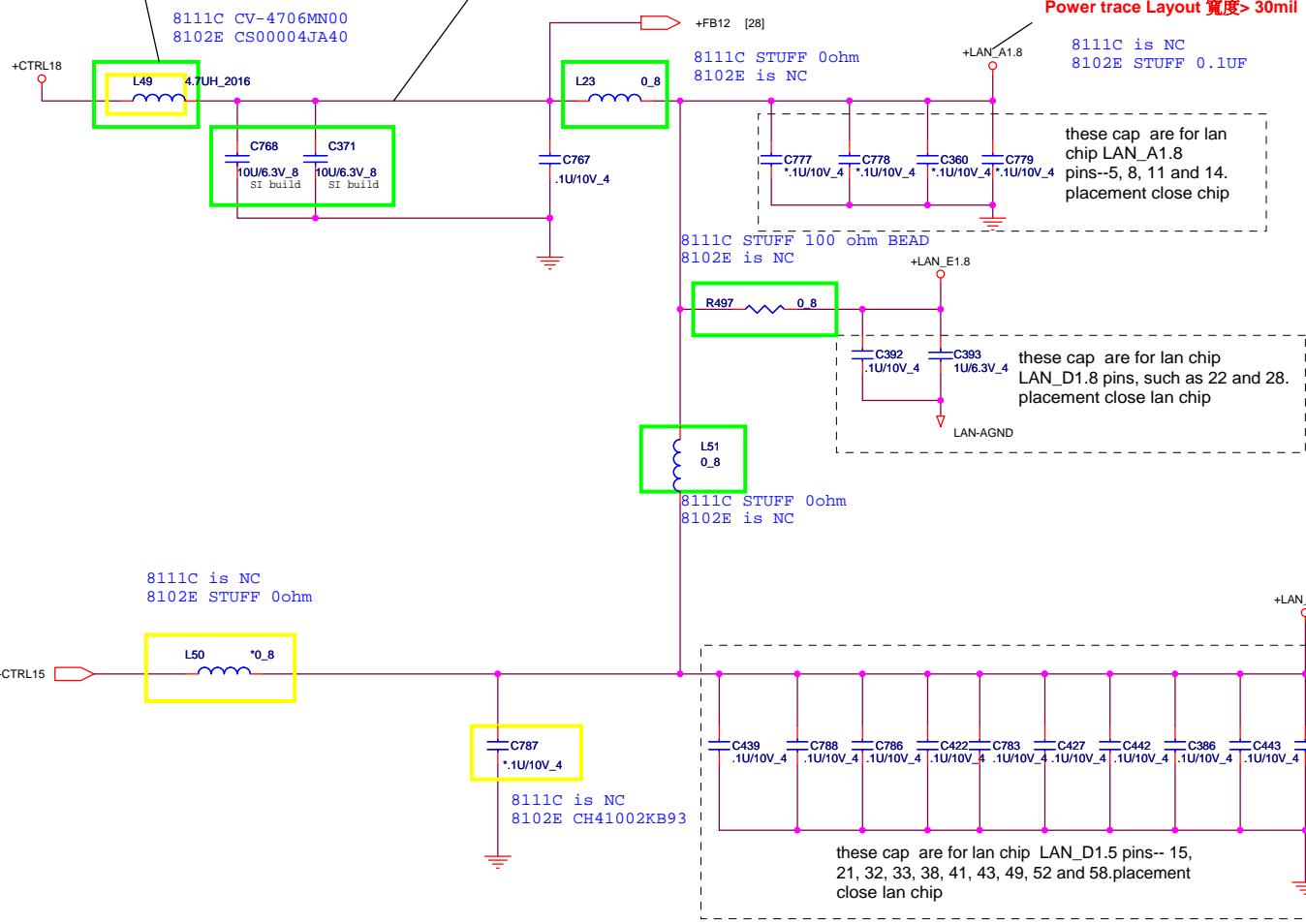
E : Stuffed for 8102E(10/100)



For Giga must change L65 to Inductor (Chipset include switch power)
+CTRL18 will become to switch power phase

L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%

placement close to lan chipset



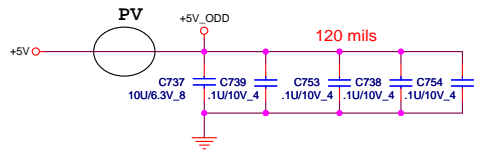
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

Power trace Layout 寬度> 30mil

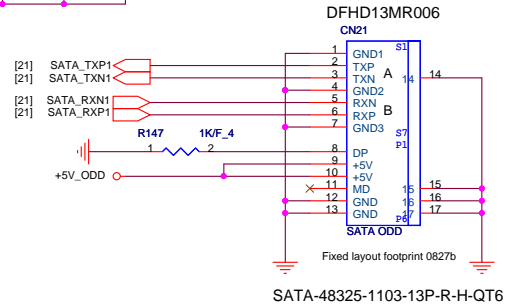
PROJECT : QL8
Quanta Computer Inc.

Size A3	Document Number	Rev 3A
LAN Power		
Date: Tuesday, April 08, 2008	Sheet 29 of 45	



SATA CD-ROM

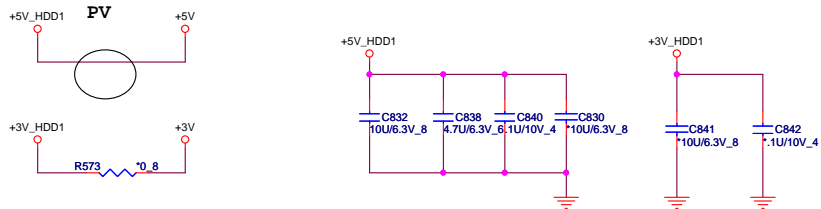
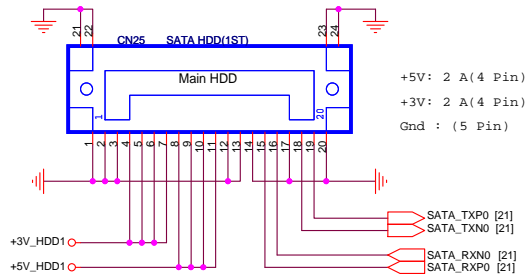
DV2 Change footprint



SATA-48325-1103-13P-R-H-QT6

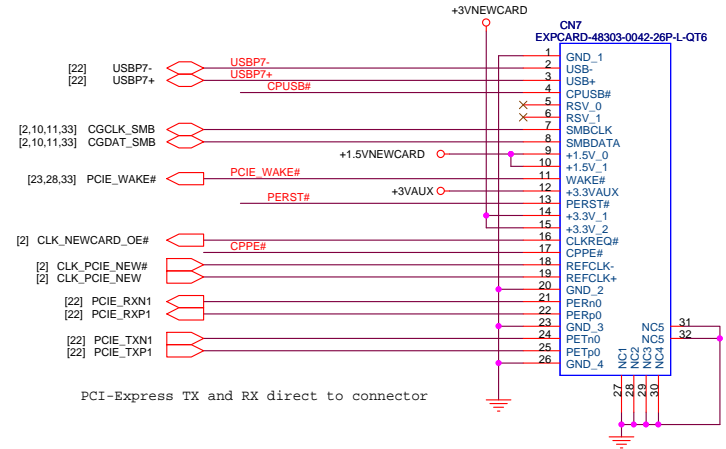
SATA_1 CONNECTOR

DC Current rating: 0.5 A



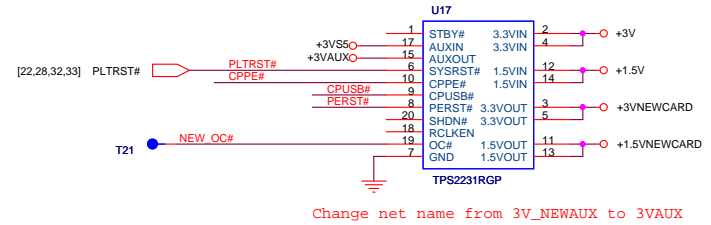
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

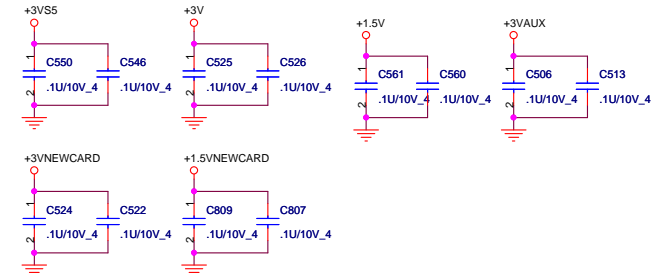


PCI-Express TX and RX direct to connector

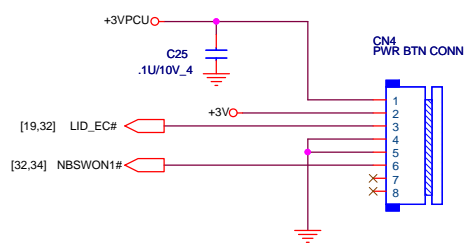
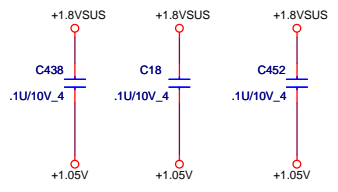
Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-1-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



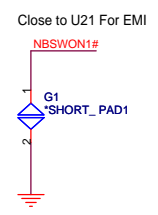
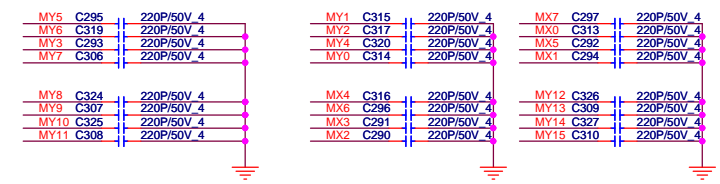
Change net name from 3V_NEWAUX to 3VAUX



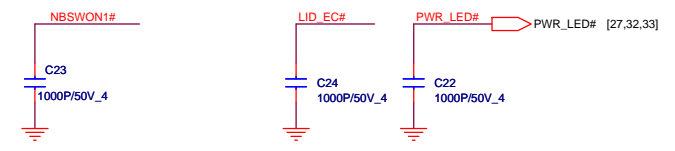
	PROJECT : QL8 Quanta Computer Inc.	
	Size Custom Document Number ODD/HDD/NEW CARD	Rev 3A
Date: Tuesday, April 08, 2008		Sheet 30 of 45



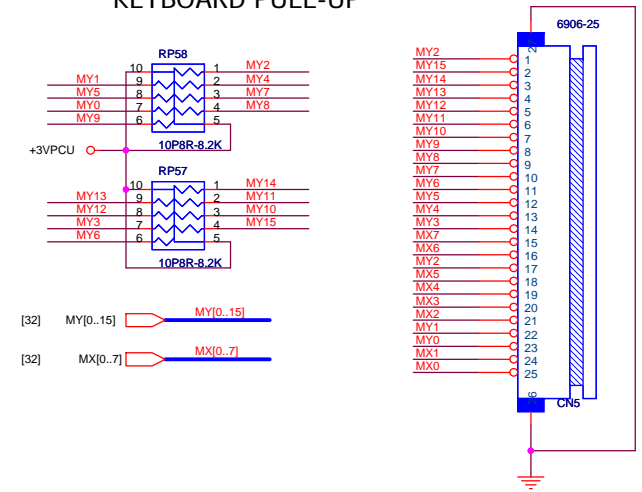
1. +3VPCU(LIDSWITCH PWR)
2. +3V
3. LIDSWITCH
4. GND
5. GND
6. POWERON#
7. NC
8. NC



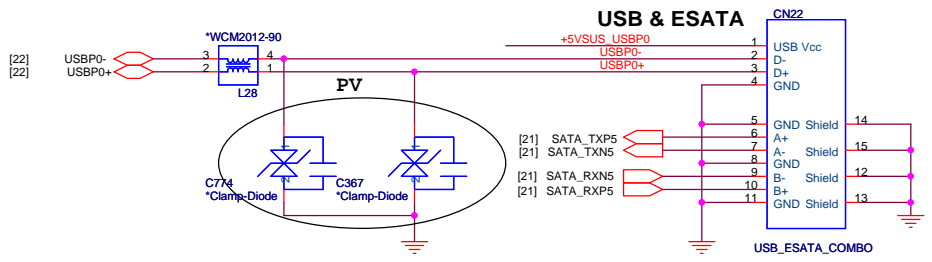
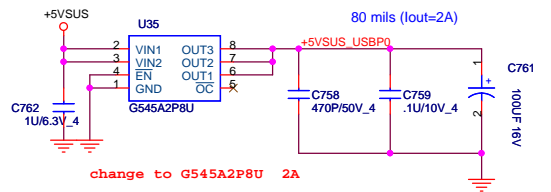
POWER BOTTON CONNECT



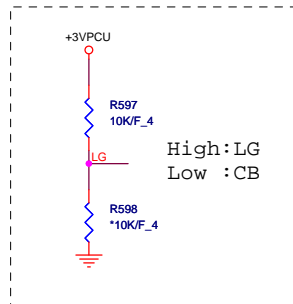
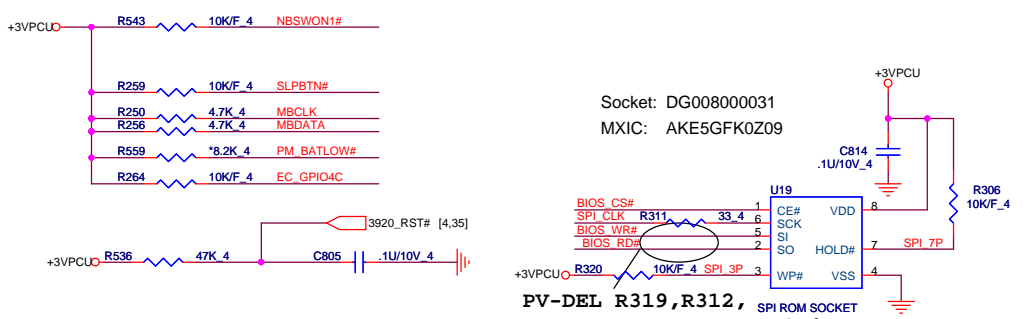
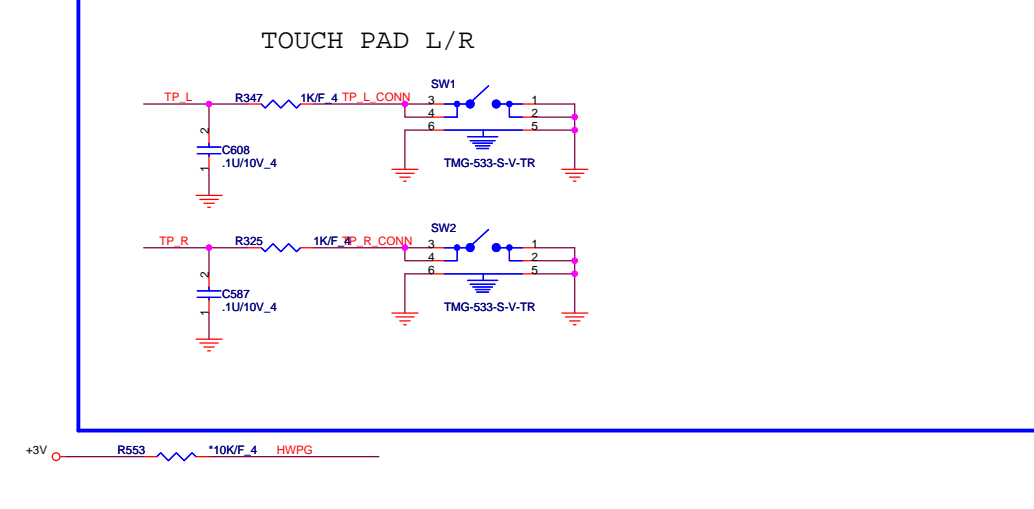
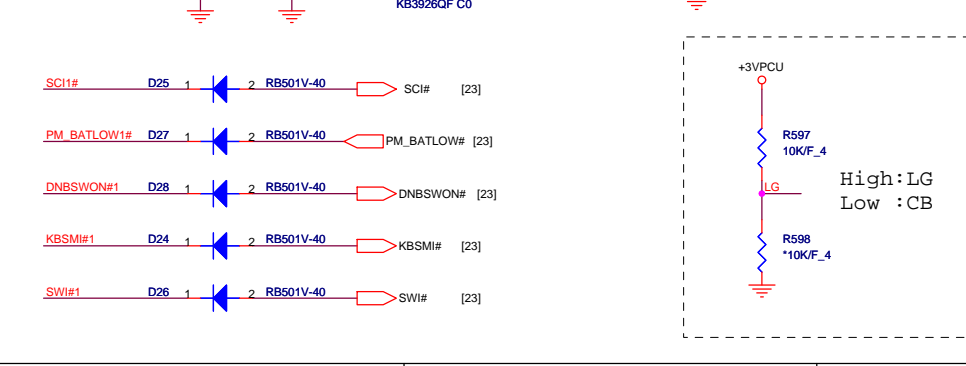
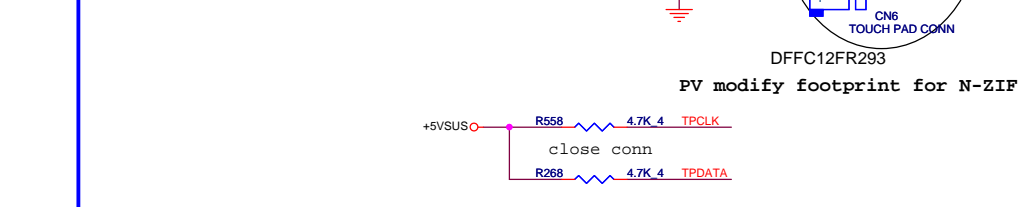
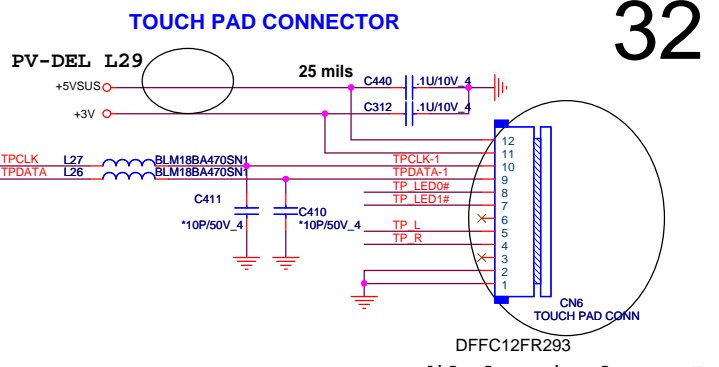
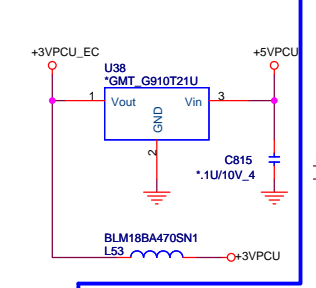
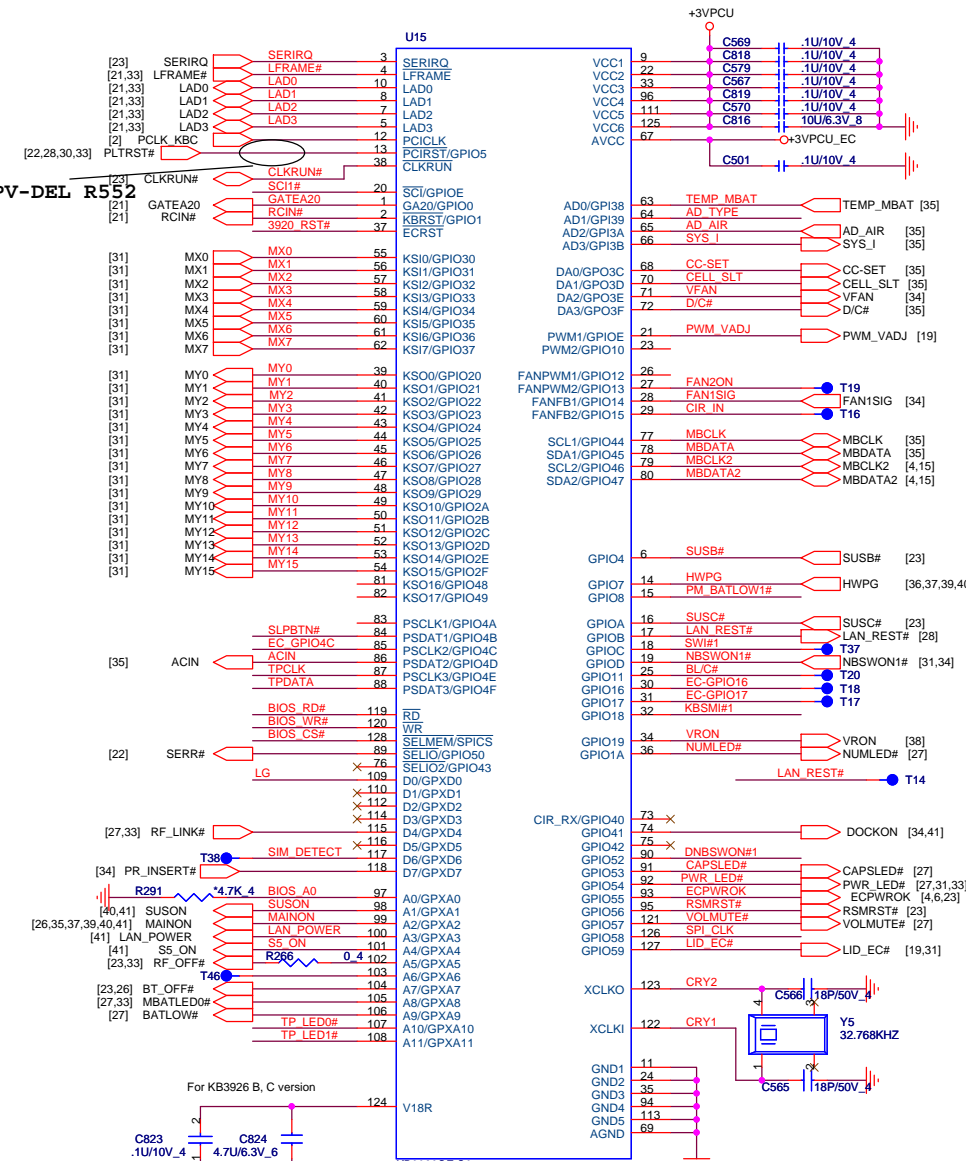
KEYBOARD PULL-UP



E-SATA/USB COMBO



	PROJECT : QL8 Quanta Computer Inc.	
	Size Custom	Document Number KB/CAP/POWER CONN
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Quanta Computer Inc.

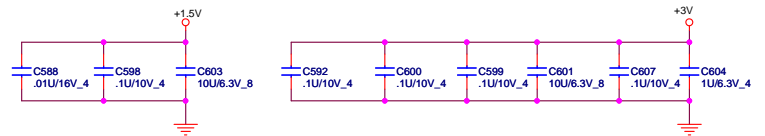
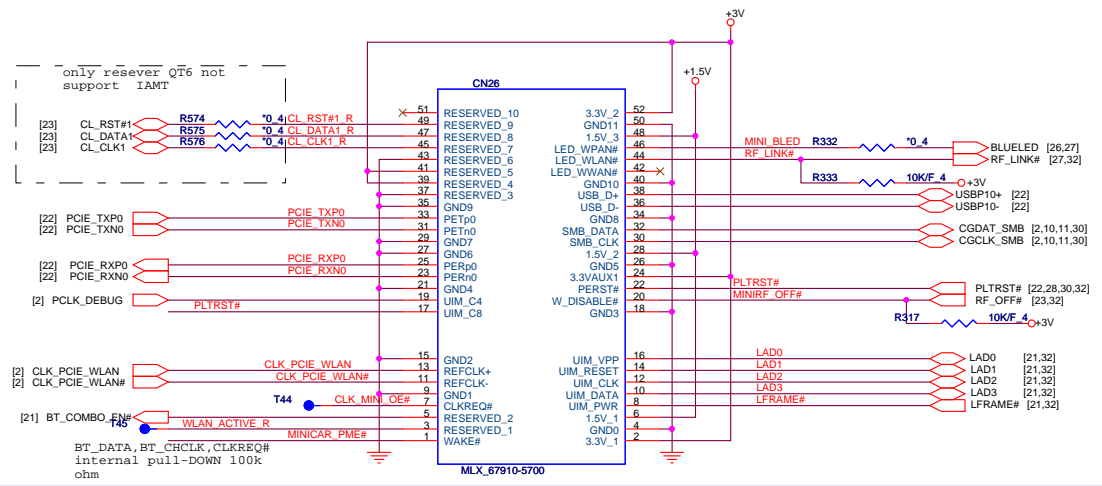
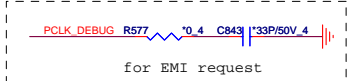
Socket: DG008000031
MXIC: AKE5GFK0Z09

PV-DEL R319, R312, SPI ROM SOCKET
1M byte
SPI
BIOS

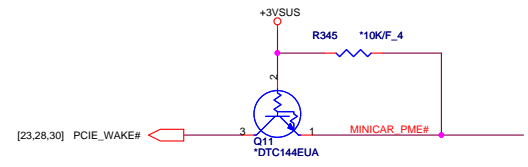
NB5

Size Custom	Document Number KB3926/ROM/TP	Rev 3A
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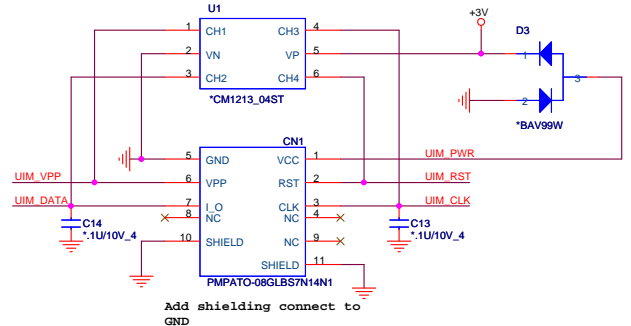
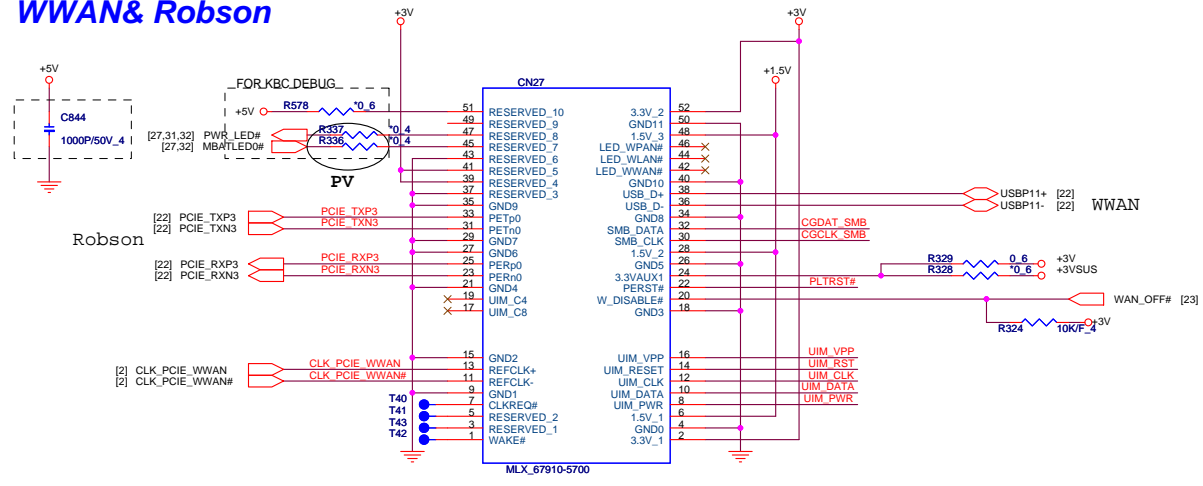
Mini PCI-E Card 1 WLAN

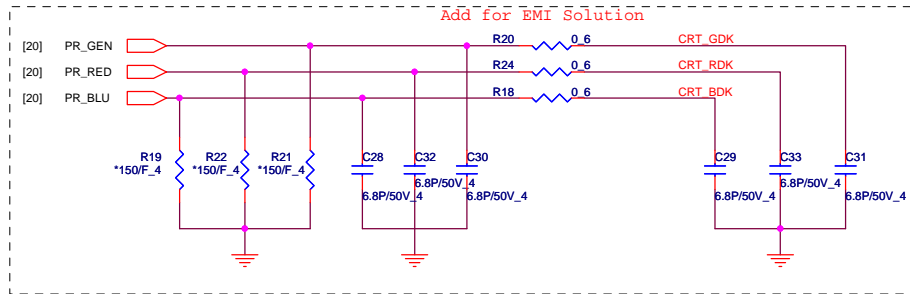
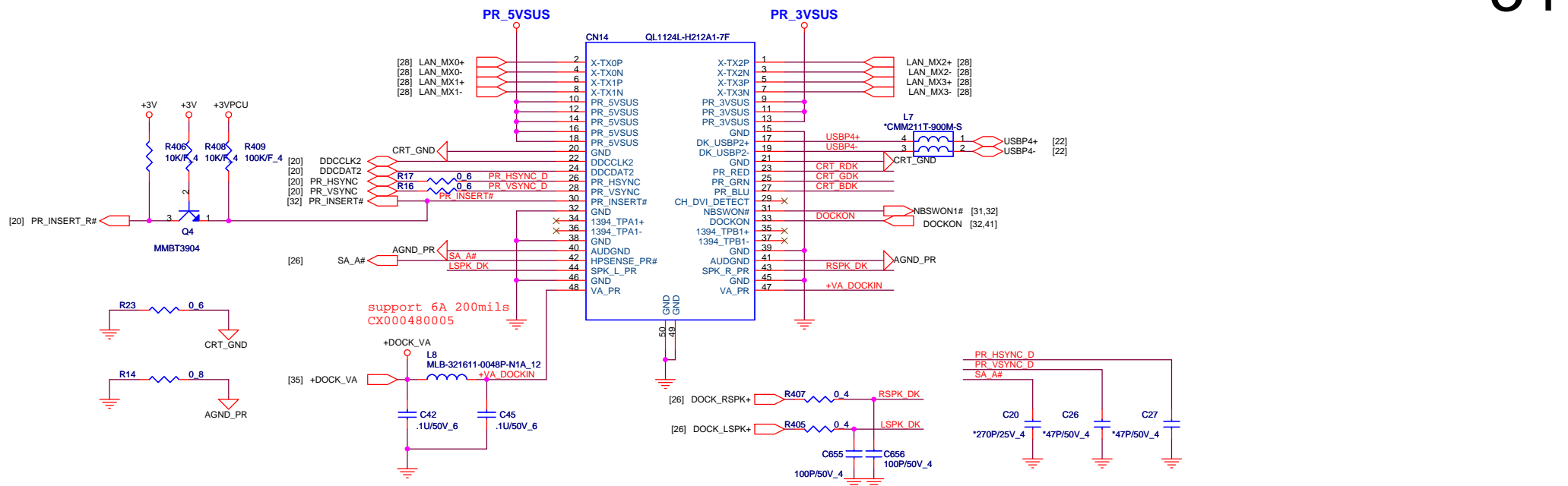


INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

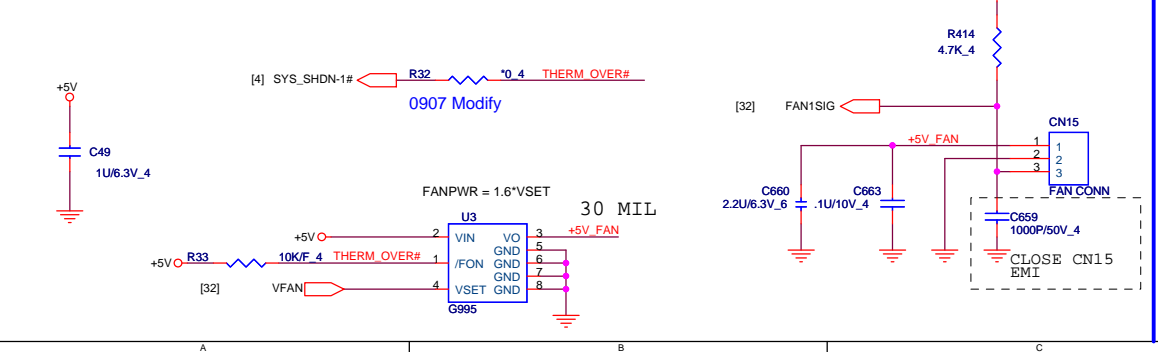


Mini PCI-E Card 2 WWAN& Robson





CPU FAN

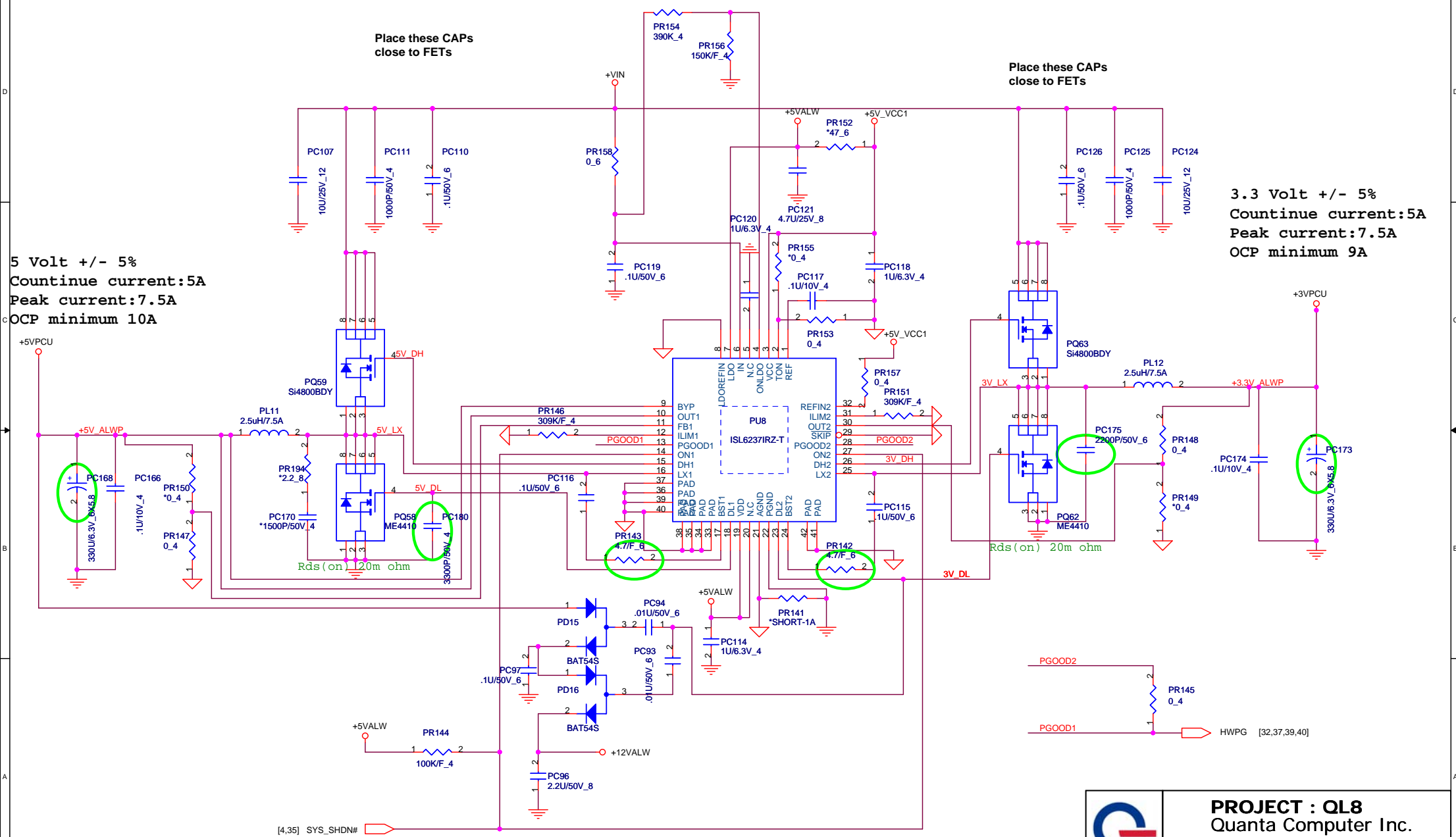



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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A

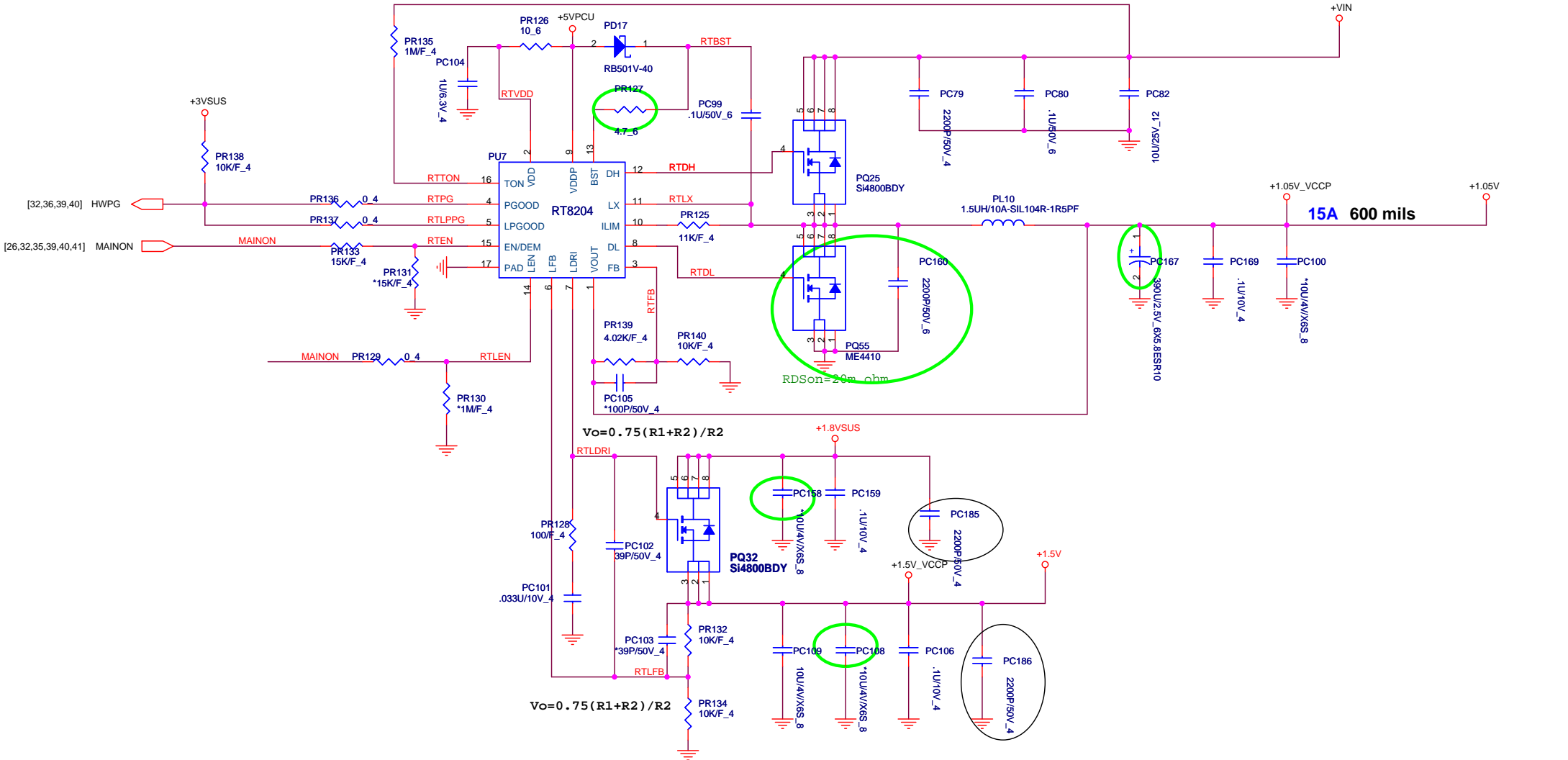



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	Size B	Document Number +5V/+3V (ISL6237)
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[4,35] SYS_SHDN#

VCCP1.05V & +1.5V

+1.05V Volt +/- 5%
 Continunue current 6A
 Peak current:8A
 OCP minimum 12A



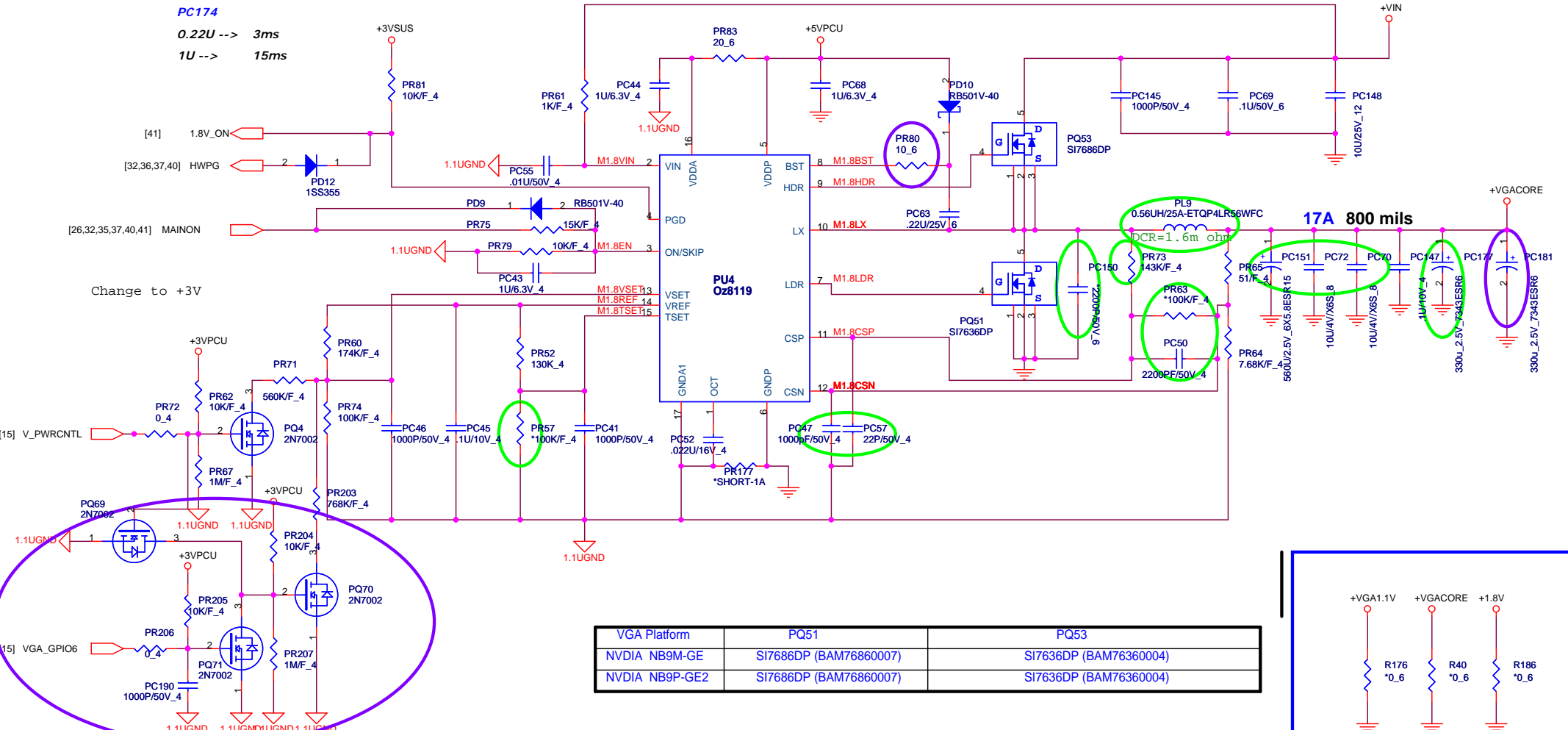
	PROJECT : QL8 Quanta Computer Inc.	
	Size B	Document Number +1.05V/+1.5V (RT8204)
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VGA Core & VCC1.1

+1.1Volt +/- 5%
 Countinue current:8A
 Peak current:9A
 OCP minimum 12A

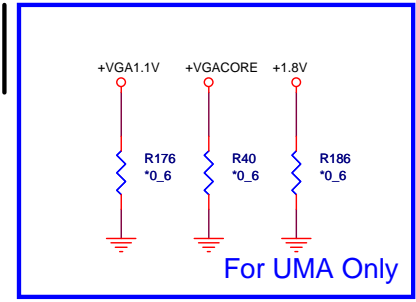
PC174

0.22U --> 3ms
 1U --> 15ms



Change to +3V

VGA Platform	PQ51	PQ53
NVIDIA NB9M-GE	SI7686DP (BAM76860007)	SI7636DP (BAM76360004)
NVIDIA NB9P-GE2	SI7686DP (BAM76860007)	SI7636DP (BAM76360004)



V_PWRCNTL	VGA_GPIO6	nVIDIA NB9M-GS	Resistor Value
LO	LO	1.09V	PR203_768K_CS47682FB10
LO	HI	1.17V	PR60_133K_CS41332FB06
HI	LO	0.90V	PR71_196K_CS41962FB01
HI	HI	0.90V	

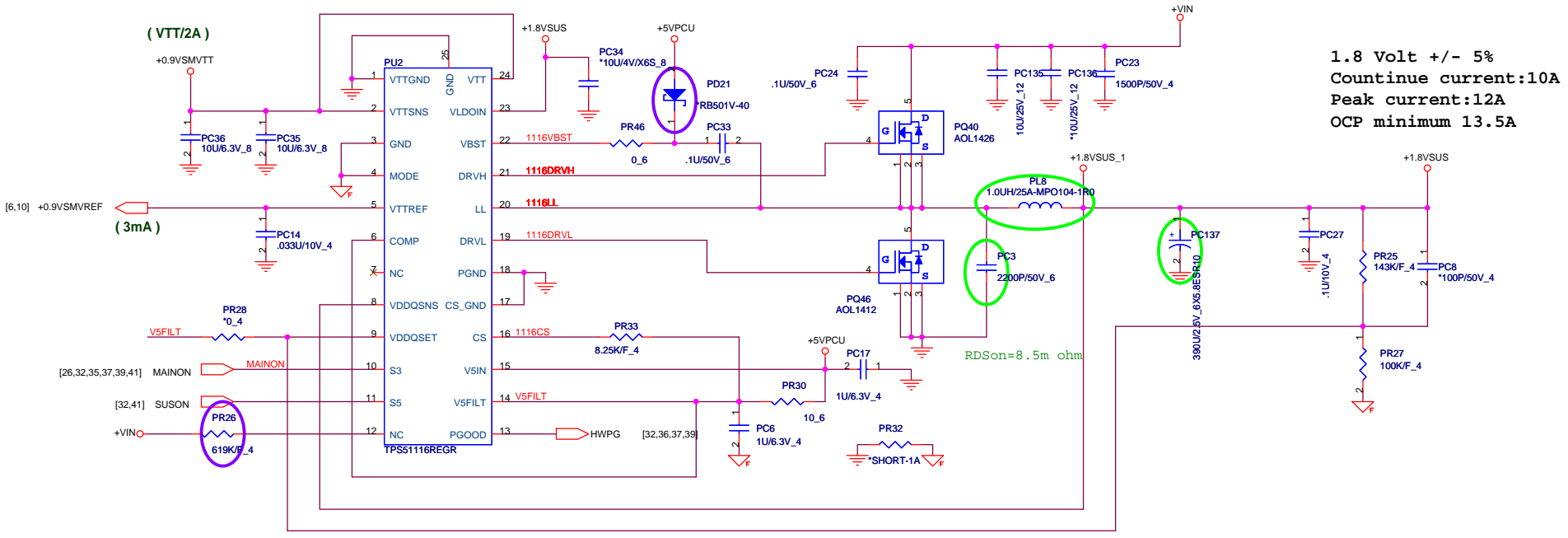
V_PWRCNTL	nVIDIA NB9M-GE	Resistor Value
HI	0.90V	PR71_392K_CS43922FB17
LO	1.09V	PR60_150K_CS41502FB18

V_PWRCNTL	nVIDIA NB9P-GE2	Resistor Value
HI	0.9V	PR71_560K_CS45602FB04
LO	1.0V	PR60_174K_CS41182FB10



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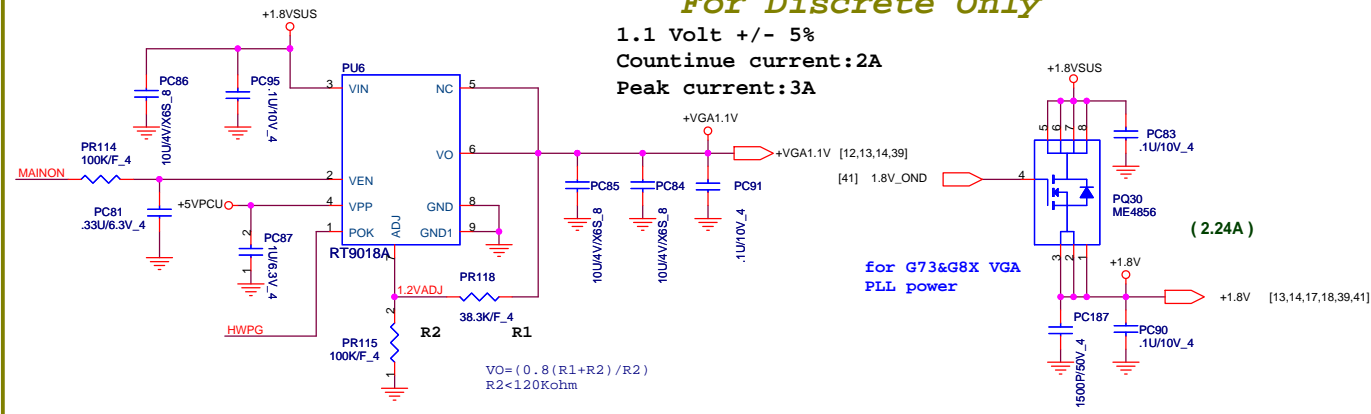
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1.8 Volt +/- 5%
 Countinue current:10A
 Peak current:12A
 OCP minimum 13.5A

For Discrete Only

1.1 Volt +/- 5%
 Countinue current:2A
 Peak current:3A



(2.24A)

for G73&G8X VGA
 PLL power

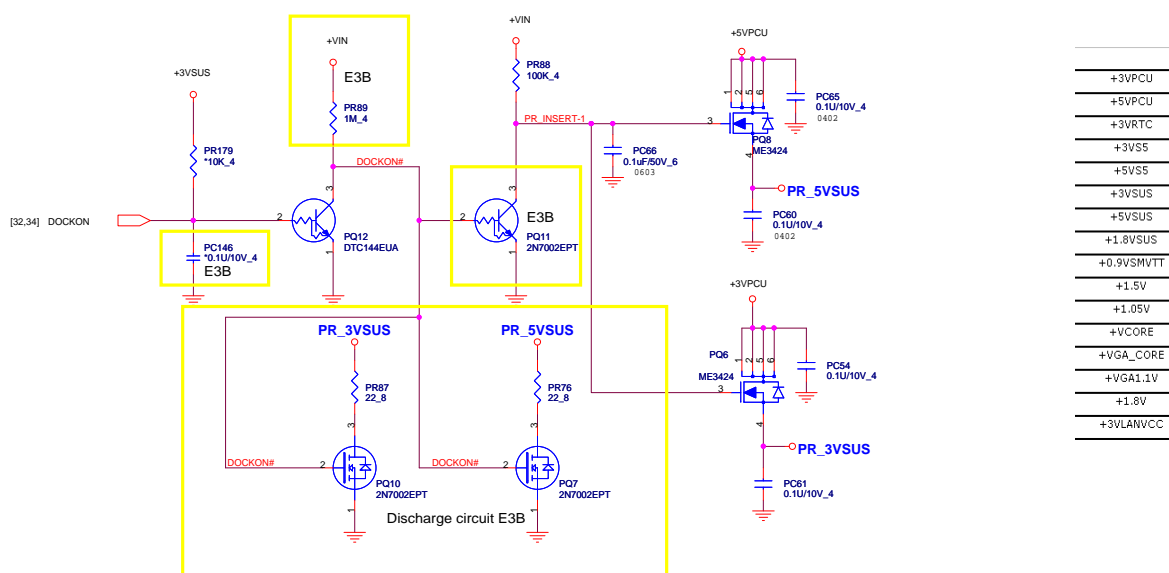
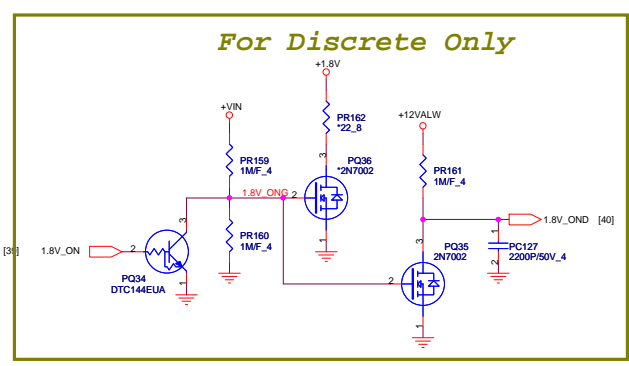
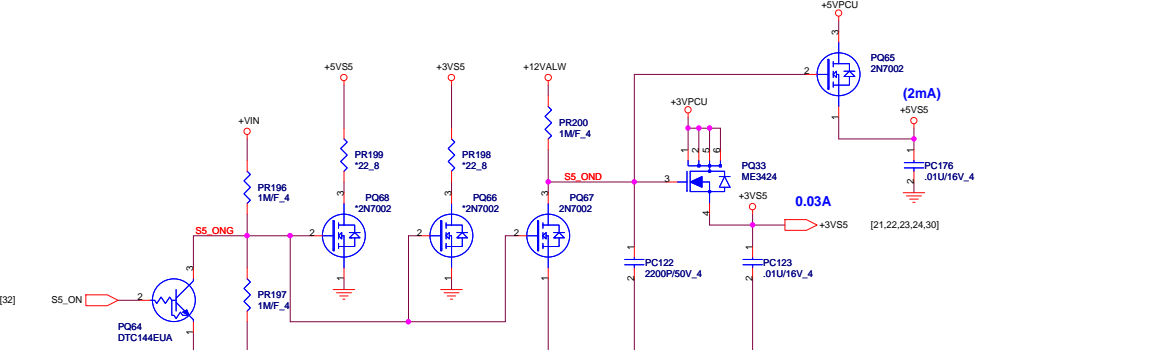
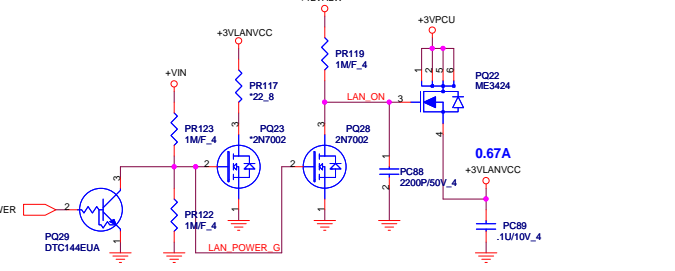
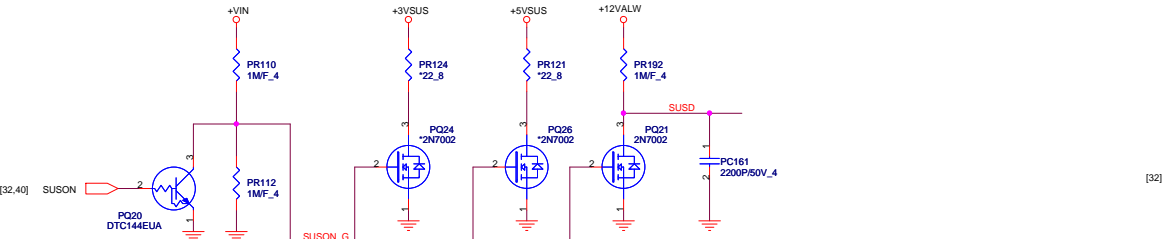
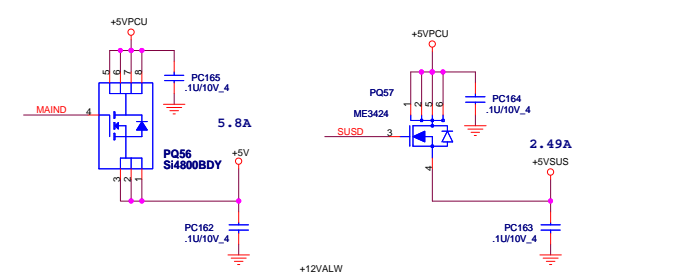
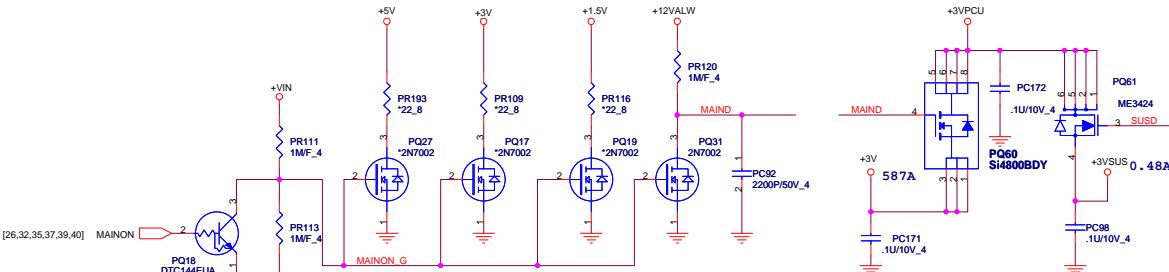
$$VO = (0.8 (R1 + R2) / R2)$$

$$R2 < 120Kohm$$



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	Voltage level	AC MODE					DC MODE				
		S0	S3	S4	S5	S0	S3	S4	S5		
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V	V	
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V	V	
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V	V	
+3VS5	3.3V +/- 5%	V	V	V	V	V	V	V	V	V	
+5VS5	5V +/- 5%	V	V	V	V	V	V	V	V	V	
+3VSUS	3.3V +/- 5%	V	V	V	V	V	V	V	V	V	
+5VSUS	5V +/- 5%	V	V	V	V	V	V	V	V	V	
+1.8VSUS	1.8V +/- 5%	V	V	V	V	V	V	V	V	V	
+0.9VSMVTT	0.9V +/- 5%	V	V	V	V	V	V	V	V	V	
+1.5V	1.5V +/- 5%	V	V	V	V	V	V	V	V	V	
+1.05V	1.05V +/- 5%	V	V	V	V	V	V	V	V	V	
+VCORE	0.9~1.15V	V	V	V	V	V	V	V	V	V	
+VGA_CORE	0.9~1.2V	V	V	V	V	V	V	V	V	V	
+VGA1.1V	1.1V +/- 5%	V	V	V	V	V	V	V	V	V	
+1.8V	1.8V +/- 5%	V	V	V	V	V	V	V	V	V	
+3VLANVCC	3.3V +/- 5%	V	V	V	V	V	V	V	V	V	

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