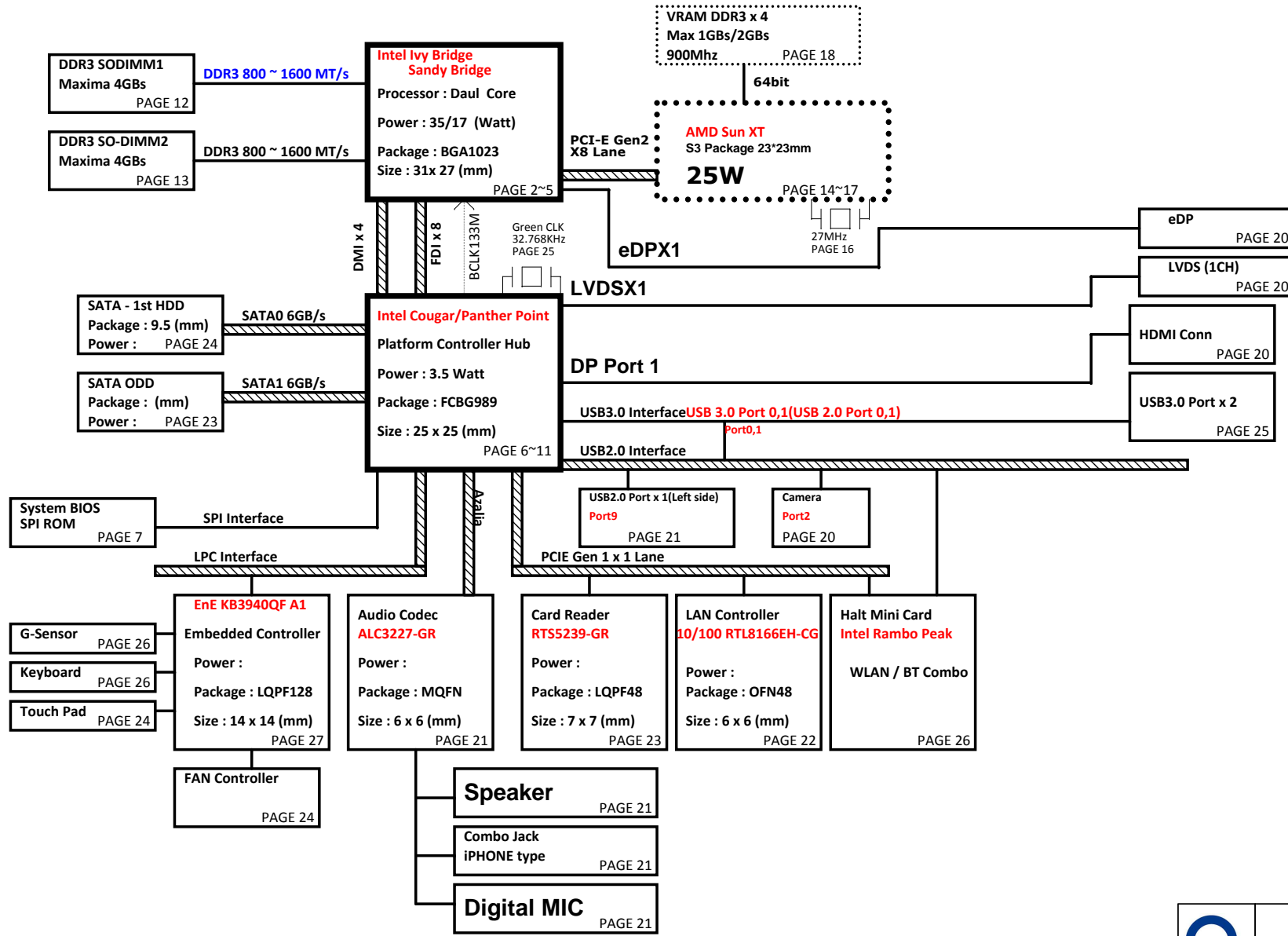


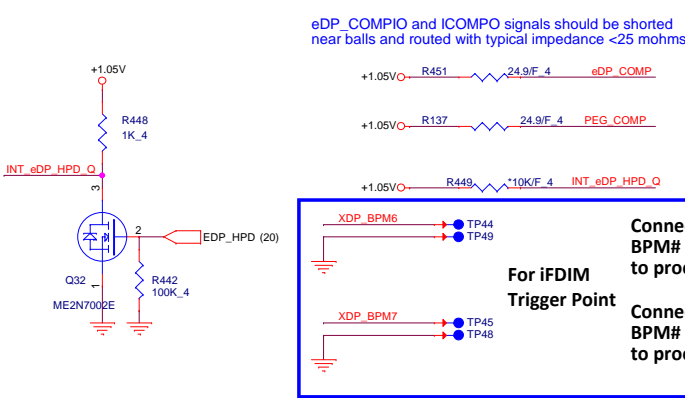
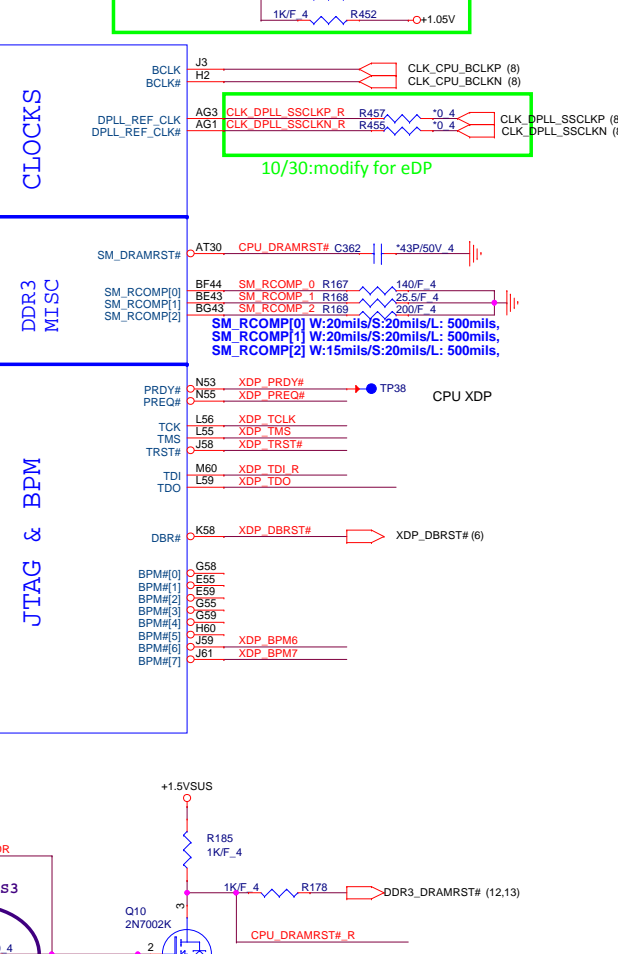
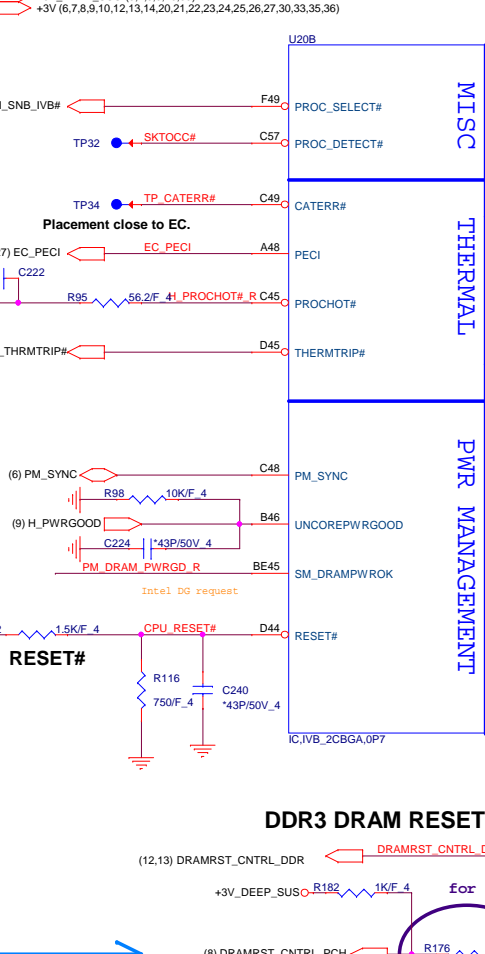
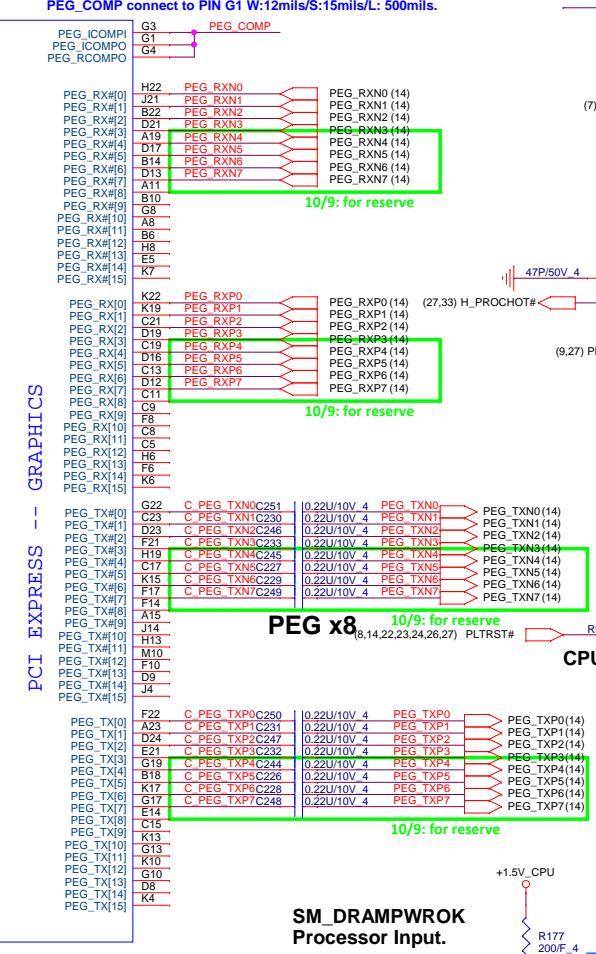
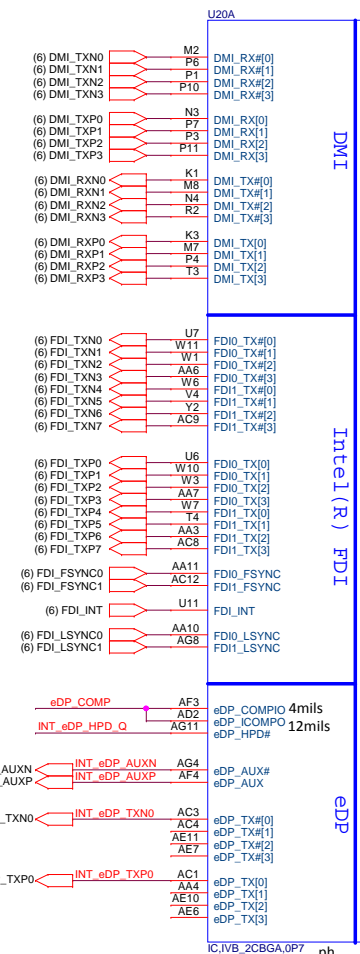
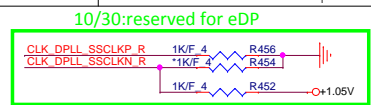
# U81 DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram

**PCB 6L STACK UP**  
 LAYER 1 : TOP  
 LAYER 2 : SGND  
 LAYER 3 : IN1(High)  
 LAYER 4 : IN2(Low)  
 LAYER 5 : SVCC  
 LAYER 6 : BOT

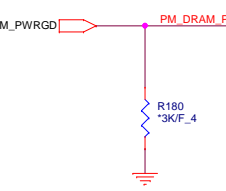


# Ivy Bridge Processor (DMI, PEG, FDI)

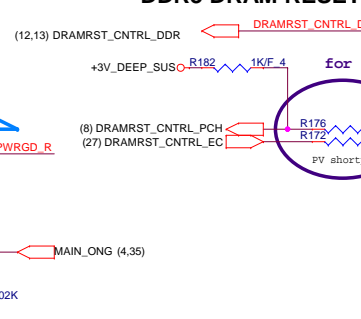
PEG\_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.  
 PEG\_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.



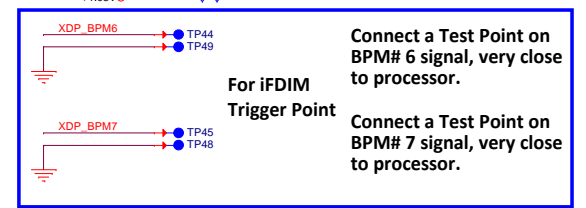
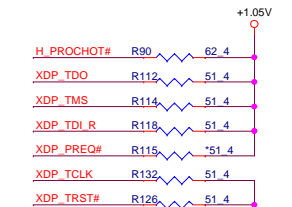
SM\_DRAMPWROK Processor Input.



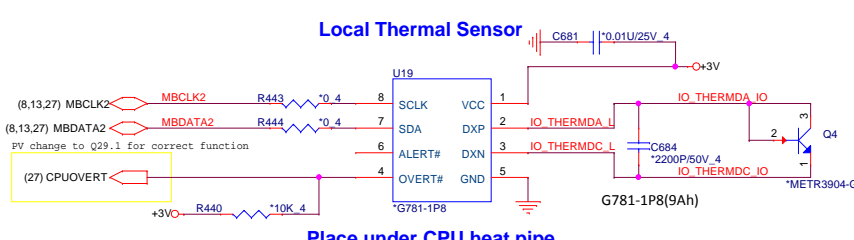
DDR3 DRAM RESET



Processor pull-up (CPU)



Connect a Test Point on BPM# 6 signal, very close to processor.  
 For iFIDM Trigger Point  
 Connect a Test Point on BPM# 7 signal, very close to processor.



Place under CPU heat pipe

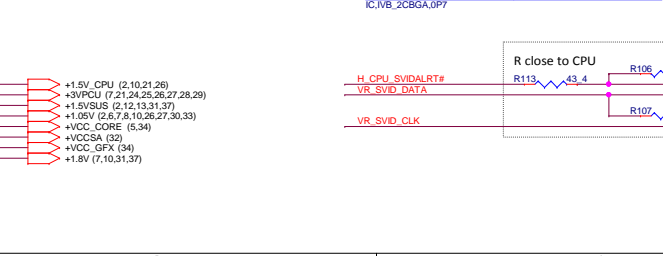
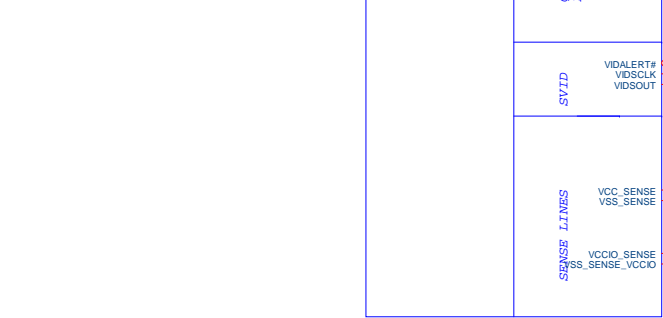
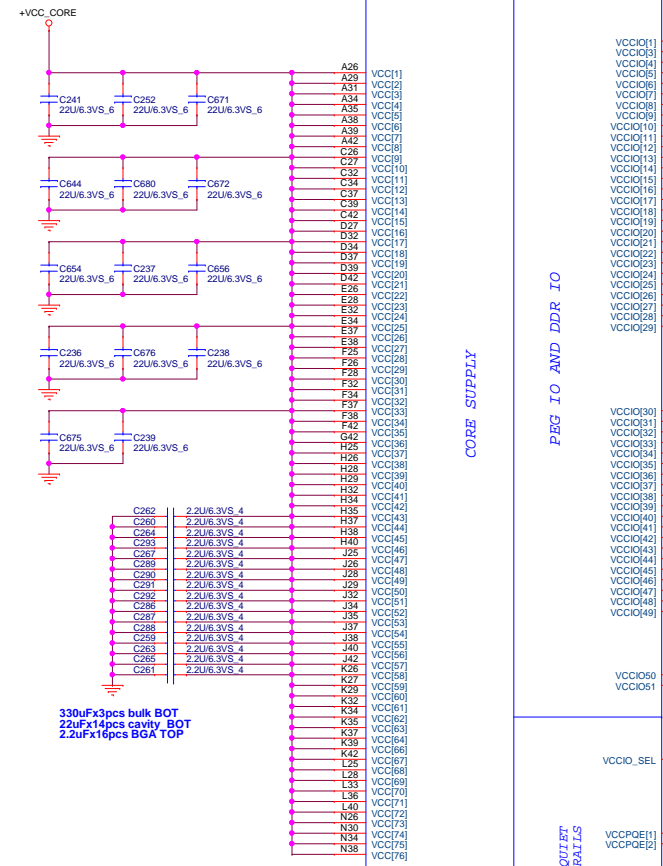
**PROJECT :U81**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>IVB 1/4 (DMI/PEG/FDI)</b>	Rev <b>1A</b>
Date: Friday, May 24, 2013	Sheet	2 of 37

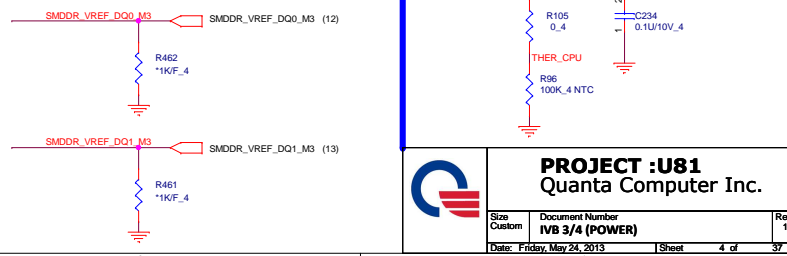
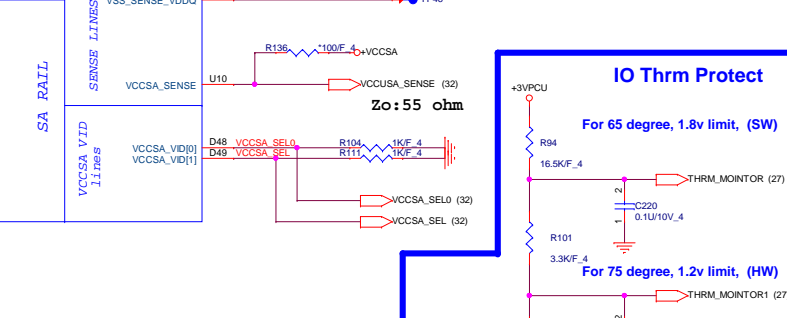
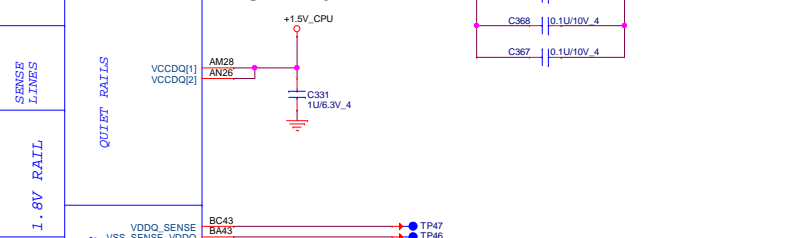
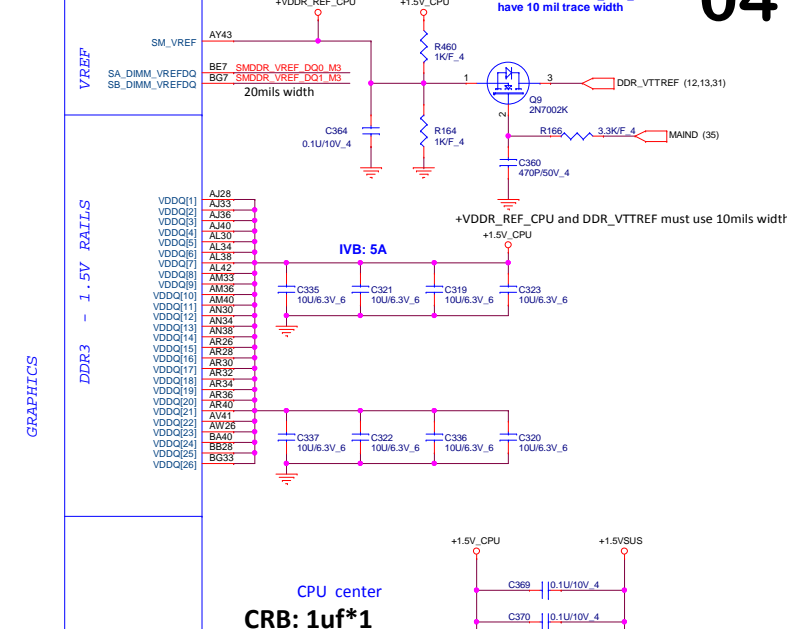
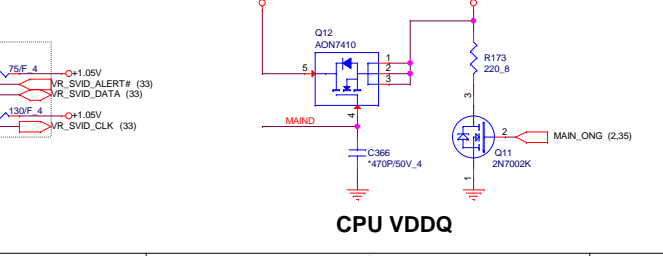
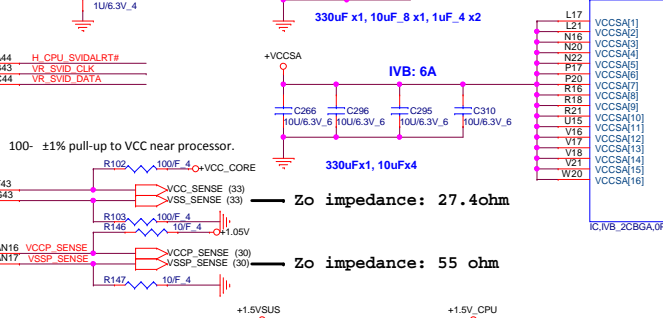
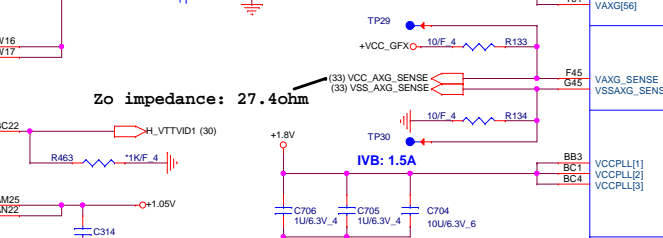
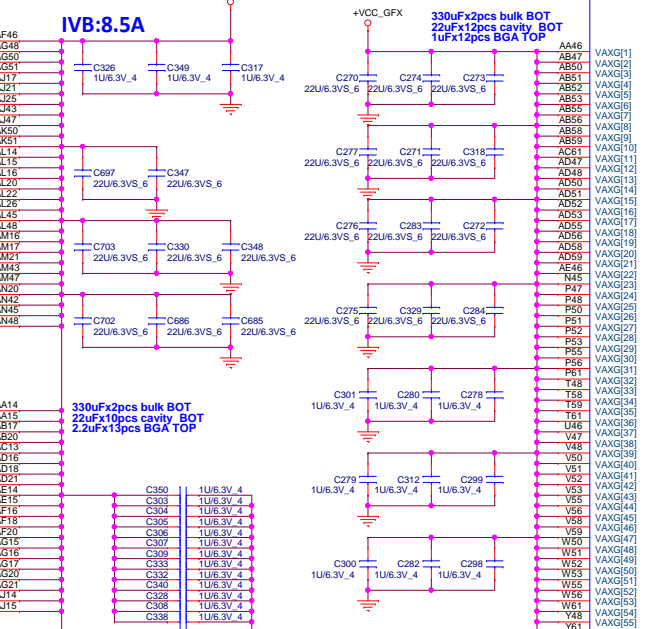


POWER

POWER

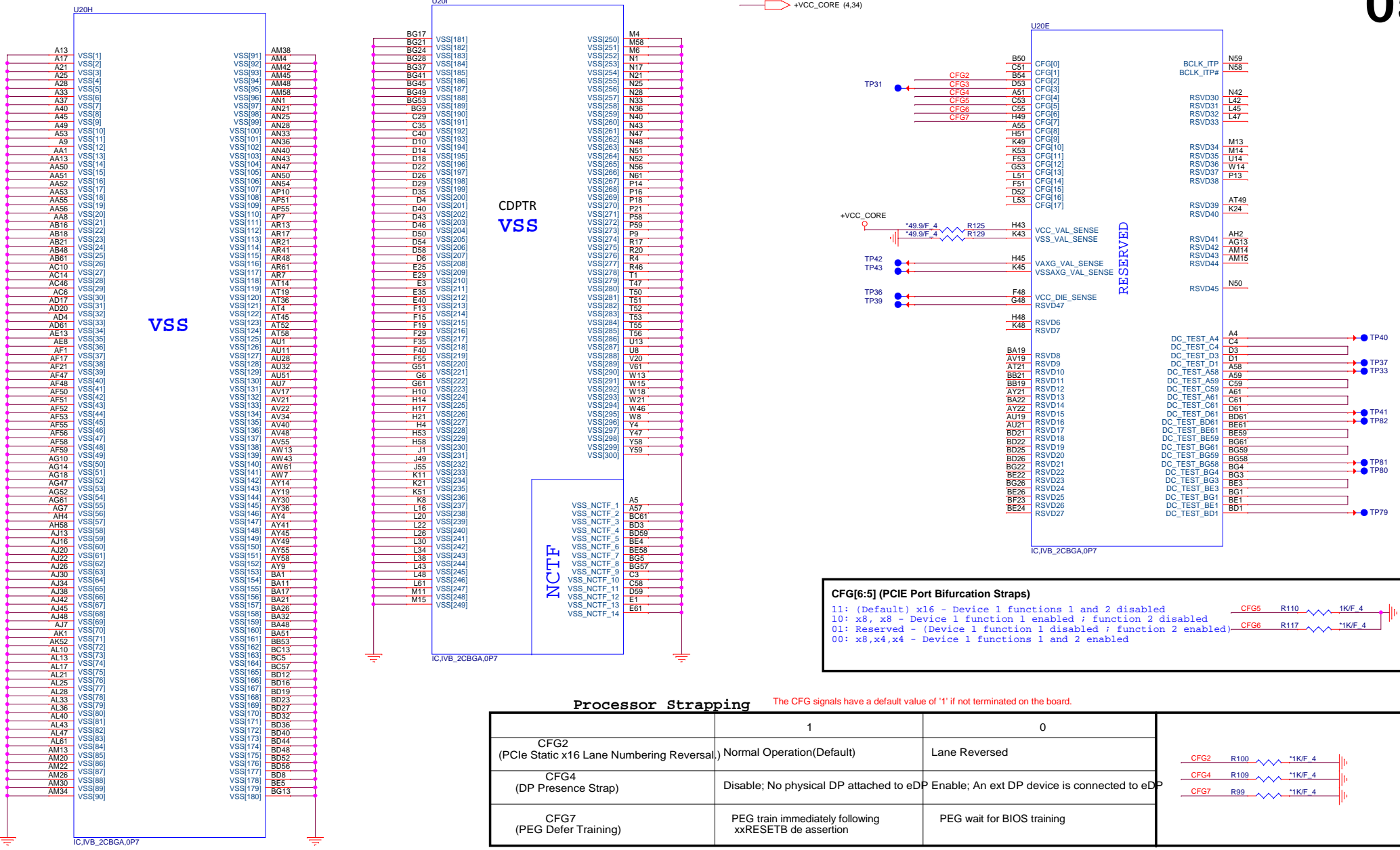


- +1.5V\_CPU (2,10,21,26)
- +3VPCU (7,21,24,25,26,27,28,29)
- +1.5VSUS (2,12,13,31,37)
- +1.05V (2,6,7,8,10,26,27,30,33)
- +VCC\_CORE (5,34)
- +VCCSA (32)
- +VCC\_GFX (34)
- +1.8V (7,10,31,37)



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Quanta Computer Inc.

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	<b>IVB 3/4 (POWER)</b>	
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**CFG[6:5] (PCIe Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

**Processor Strapping** The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

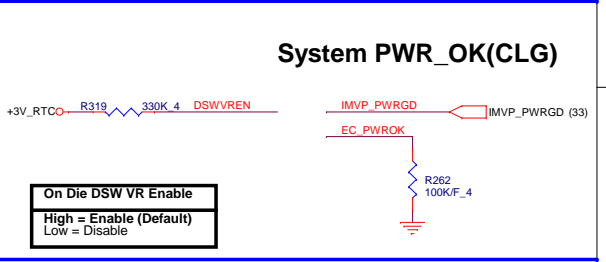
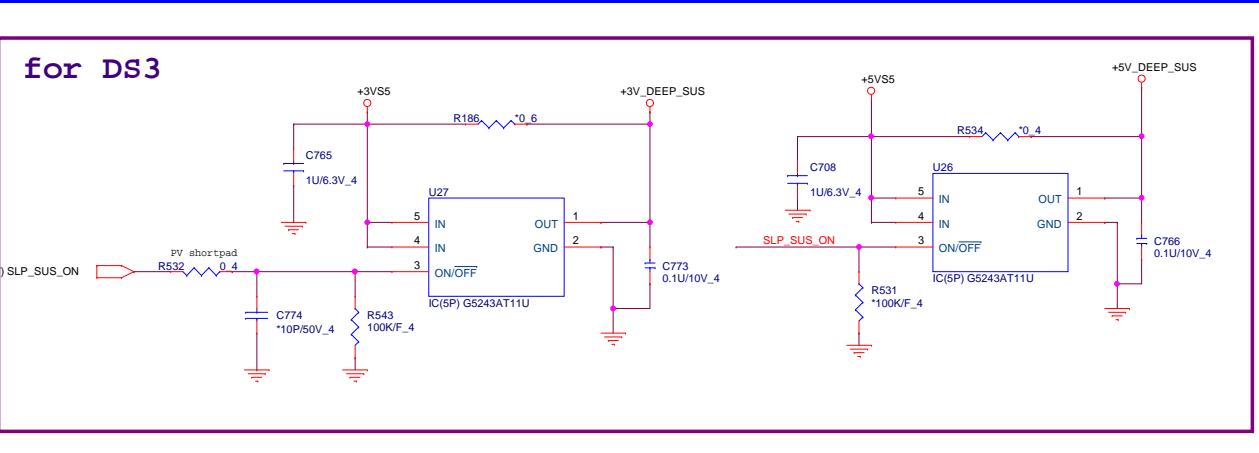
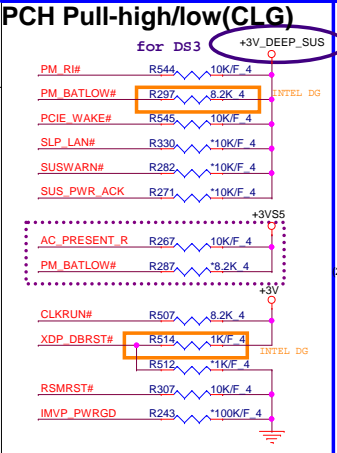
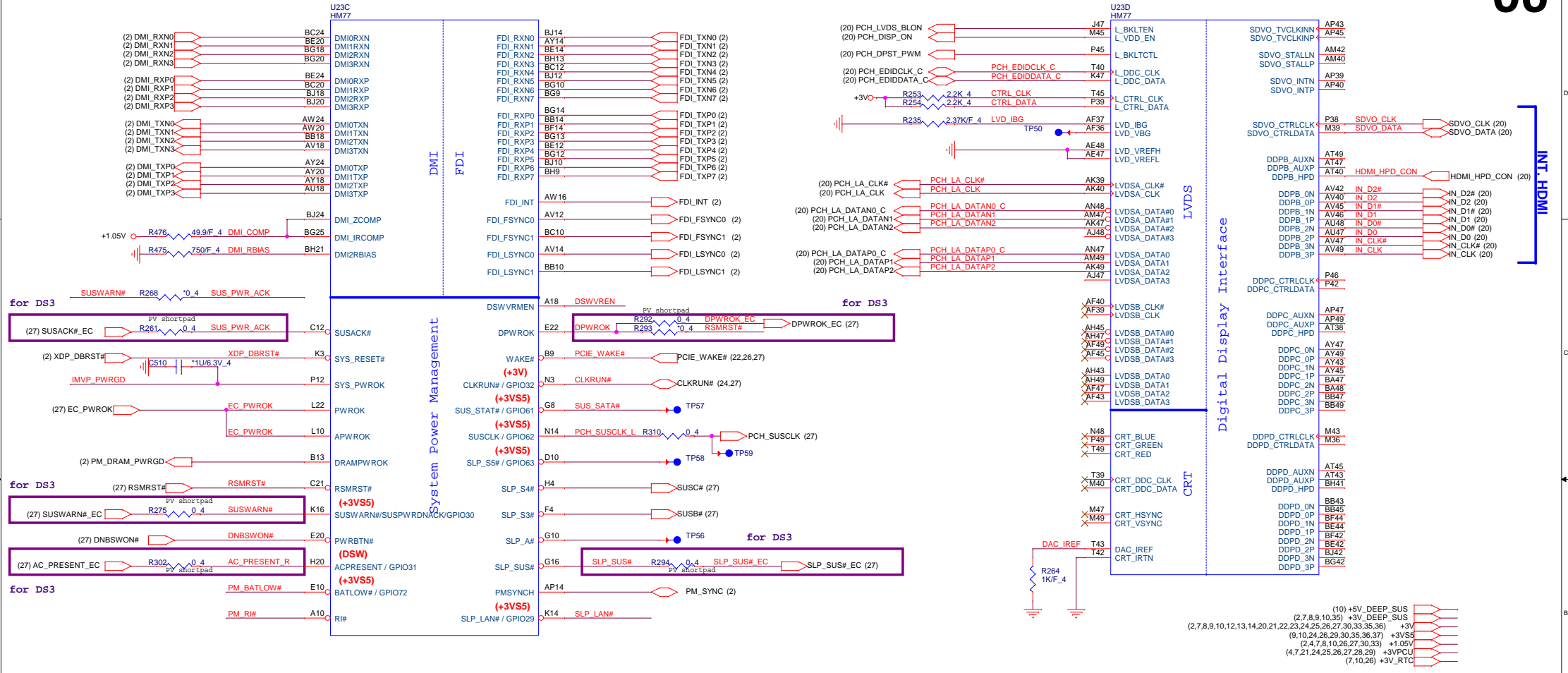
**PROJECT :U81**  
 Quanta Computer Inc.

Size Custom	Document Number IVB 4/4 (RSV,GND)	Rev 1A
Date: Monday, May 27, 2013	Sheet 5 of	37



### Cougar Point/Panther Point (DMI,FDI,PM)

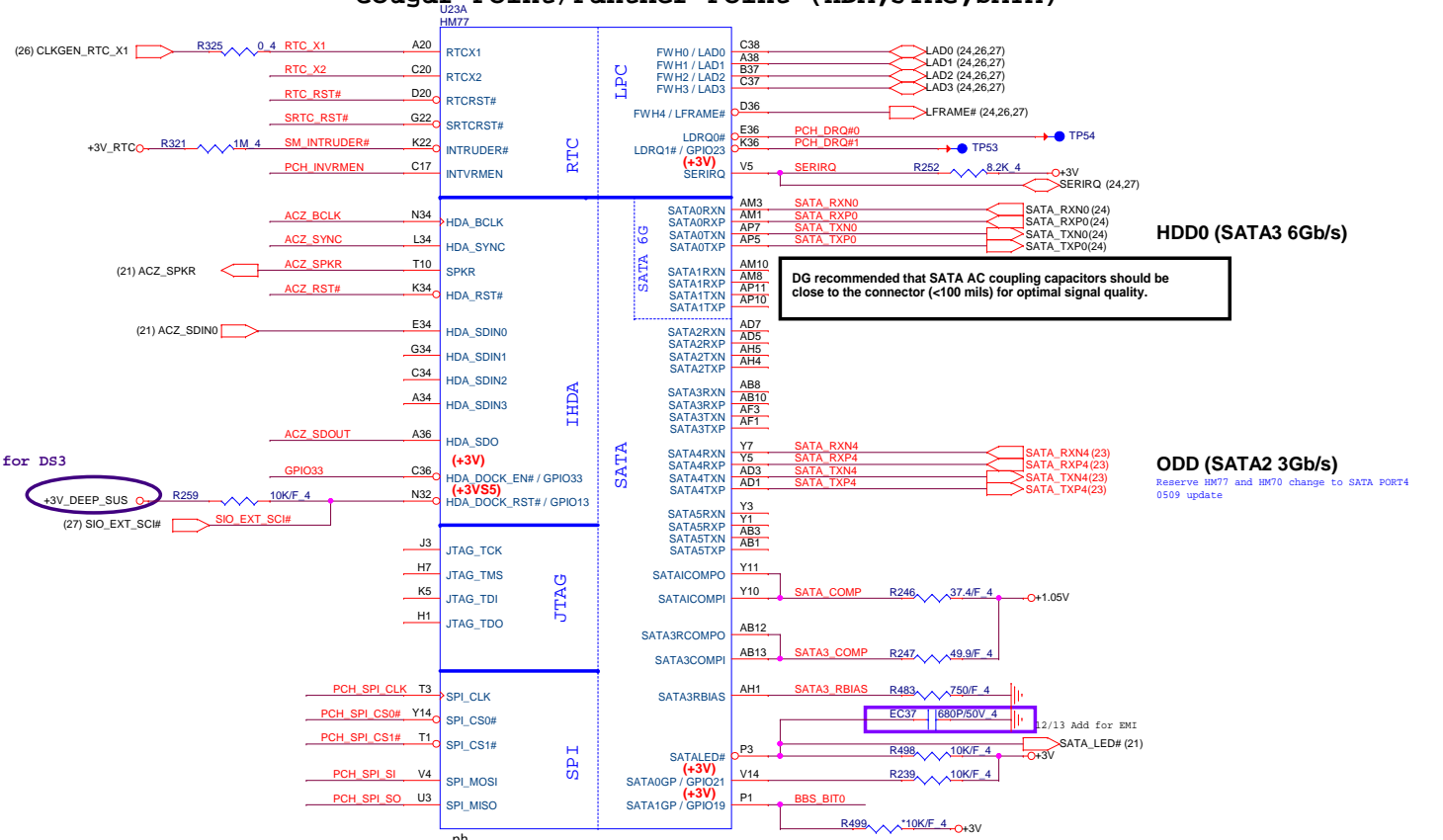
### Cougar Point/Panther Point (LVDS,DDI)



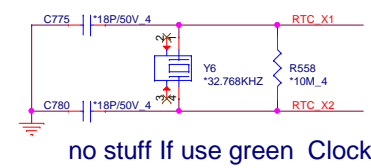
**PROJECT :U81**  
Quanta Computer Inc.

Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)	Rev 1A
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# Cougar Point/Panther Point (HDA, JTAG, SATA)

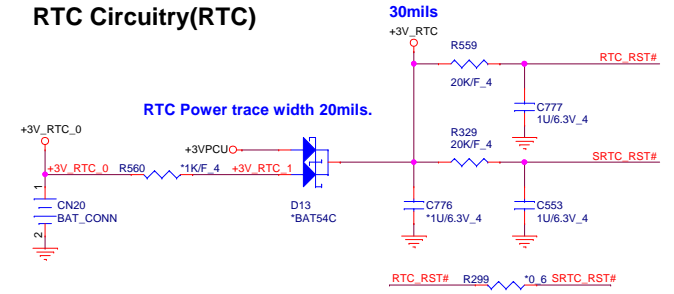


## RTC Clock 32.768KHz



no stuff if use green Clock

## RTC Circuitry(RTC)



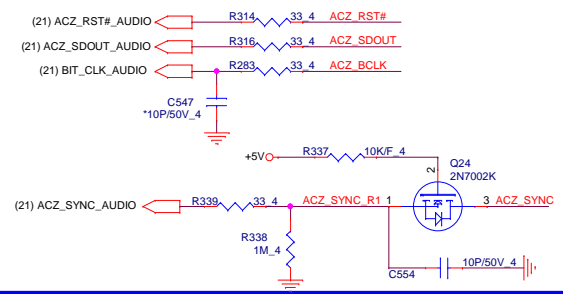
## HDD0 (SATA3 6Gb/s)

DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

## ODD (SATA2 3Gb/s)

Reserve HM77 and HM70 change to SATA PORT4 0509 update

## HDA Bus(CLG)

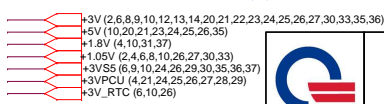
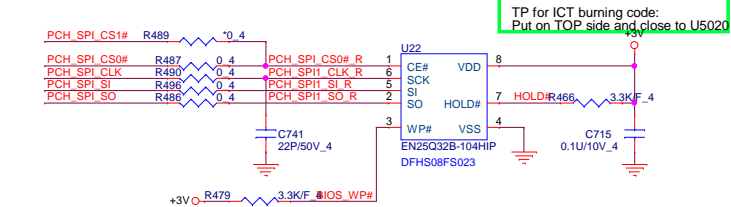
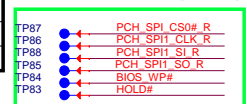


## PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V <sub>0</sub> R237 *1K/F 4 ACZ_SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V <sub>0</sub> R529 *1K/F 4 R527 *10K/F 4 PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V <sub>0</sub> RTC <sub>0</sub> R320 *330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	BIOS_WP# R471 *0.4 GPIO33
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Table with columns: GNT1#, GNT0#, Boot Location]	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R502 *1K/F 4 BBS_BIT0 R517 *1K/F 4 BBS_BIT1 (8)
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V <sub>0</sub> R472 *1K/F 4 INV_ALE (8)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V <sub>0</sub> R473 *2.2K 4 R474 *1K/F 4 INV_CLE (9) H_SNB_IVB# (2)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	for DS3 +3V <sub>0</sub> DEEP_SUS <sub>0</sub> R335 *1K/F 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V <sub>0</sub> DEEP_SUS <sub>0</sub> R322 *1K/F 4 ACZ_SDOUT R313 *0.4 GPIO33_EC (27)
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

Vender	Size	P/N
EON	4MB	AKE392N0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08F5023(91960-0084L-8P-SOCKET)

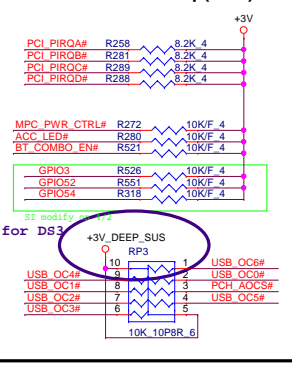
## PCH SPI ROM(CLG)



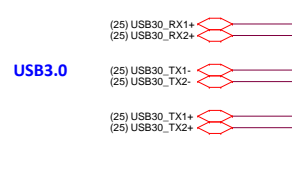
**PROJECT :U81**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
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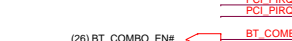
PCI/USBOC# Pull-up(CLG)



USB3.0



BT COMBO EN#



ACC\_LED#



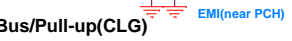
MPC\_PWR\_CTRL#



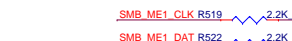
BOARD\_ID#



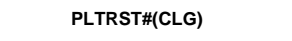
CLK\_PCI\_TPM



CLK\_33M\_DEBUG



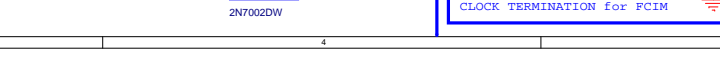
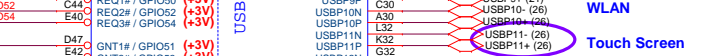
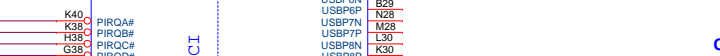
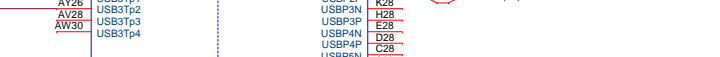
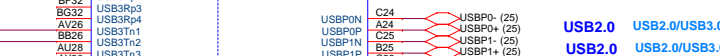
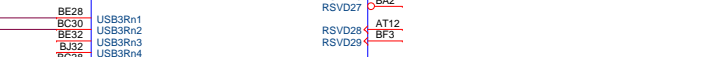
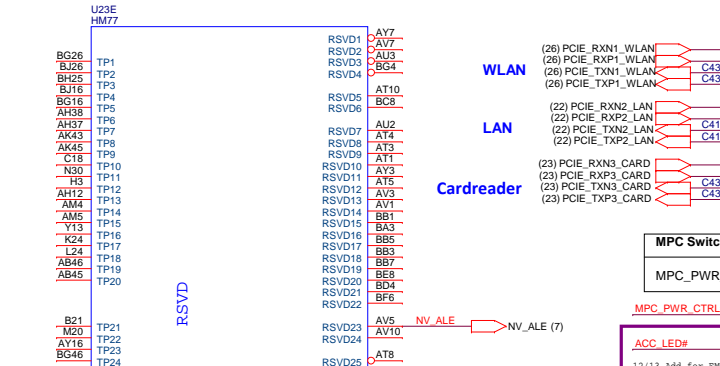
CLK\_33M\_KBC



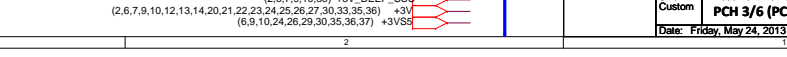
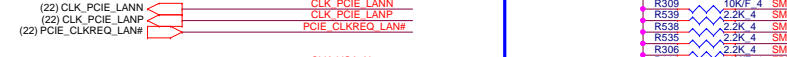
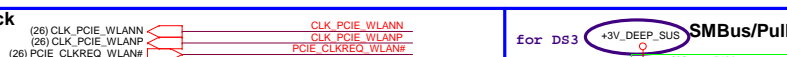
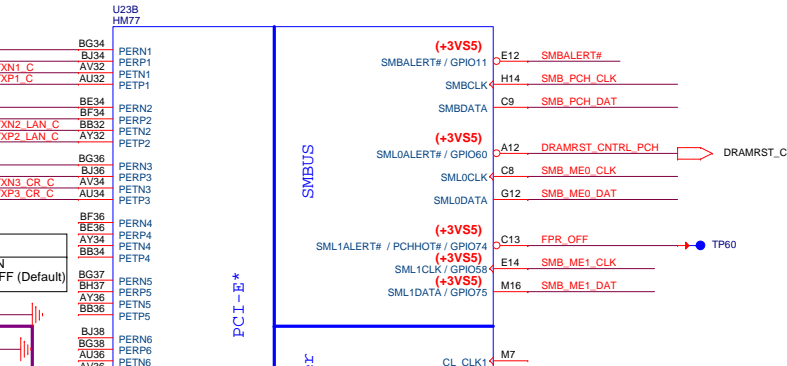
PLTRST#(CLG)



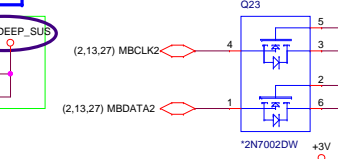
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



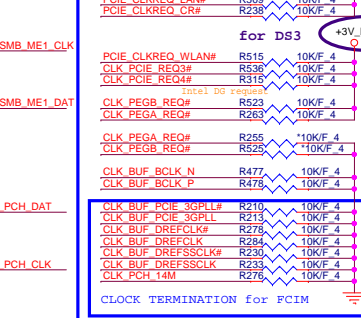
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



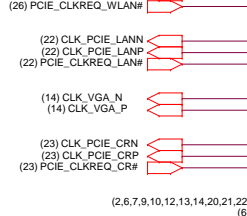
SMBus/Pull-up(CLG)



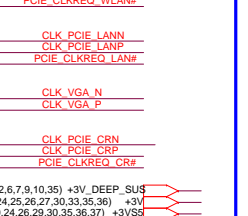
CLK\_REQ/Strap Pin(CLG)



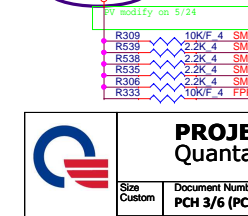
PCIe Clock



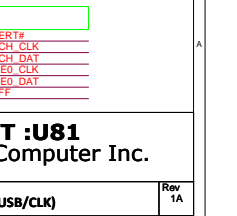
LAN



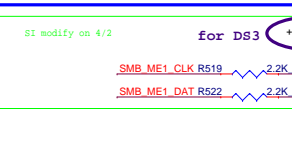
GPU



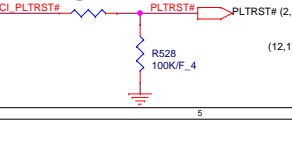
Cardreader



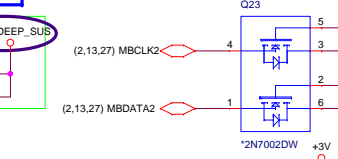
SMBus/Pull-up(CLG)



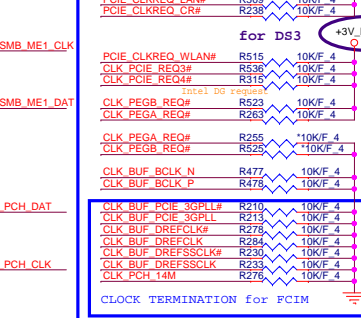
CLK\_REQ/Strap Pin(CLG)



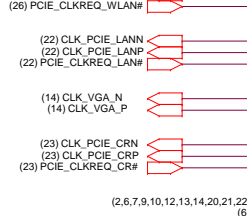
SMBus/Pull-up(CLG)



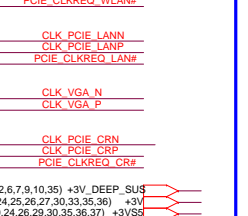
CLK\_REQ/Strap Pin(CLG)



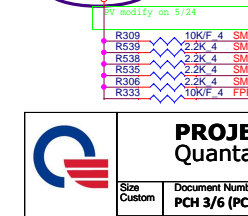
PCIe Clock



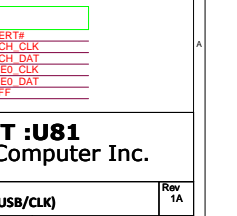
LAN



GPU



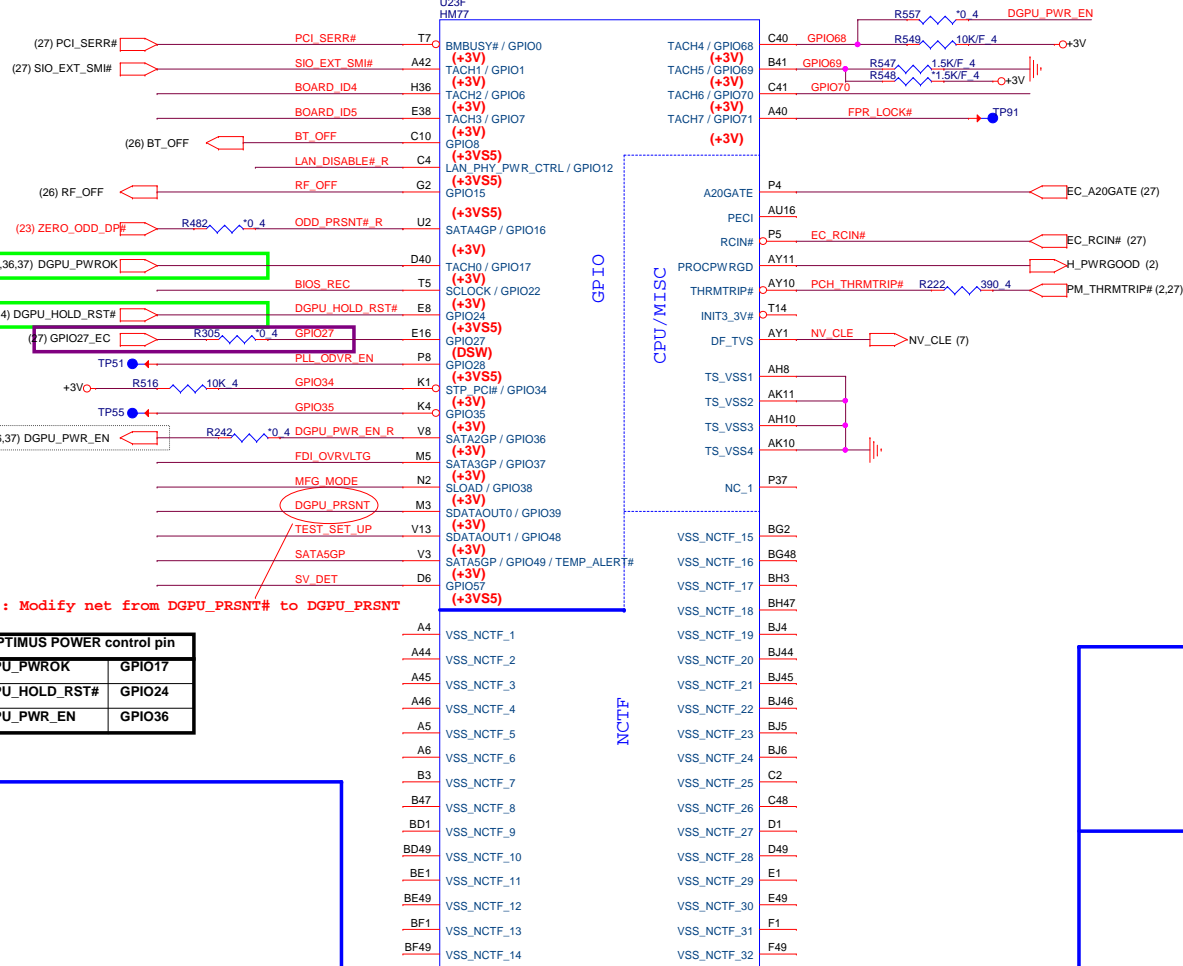
Cardreader



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Revision 1A
Date: Friday, May 24, 2013

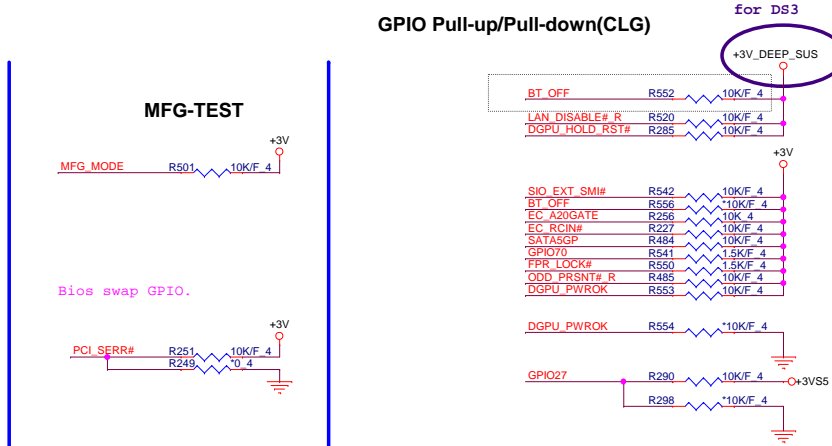


Cougar Point/Panther Point (GPIO,VSS\_NCTF,RSVD)



2011 12 01 : Modify net from DGPU\_PRSNT# to DGPU\_PRSNT

OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36



for DS3 +3V\_DEEP\_SUS

RF OFF R518 10K/F 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite  
 Low = Disable (Default)  
 High = Enable

BIOS RECOVERY High = Disable (Default)  
 Low = Enable

TEST SET UP R248 10K/F 4

SV\_SET\_UP High = Strong (Default)

R286 100K/F 4 SV\_DET

TEST DETECT Low = Default

SATA2GP/GPIO36 Reserved only

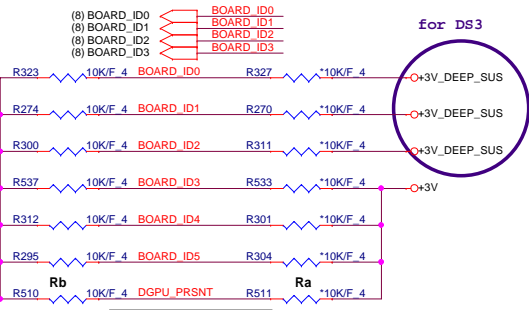
R231 100K/F 4 FDI\_OVRVLTG

FDI TERMINATION VOLTAGE OVERRIDE Reserved only

(2,6,7,8,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36) +3V  
 (6,10,24,26,29,30,35,36,37) +3VSS

Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14":0 15":1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0 UMA:0 DIS:1
U81 UMA	0	0	0	0	0	0
U81 SWG	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



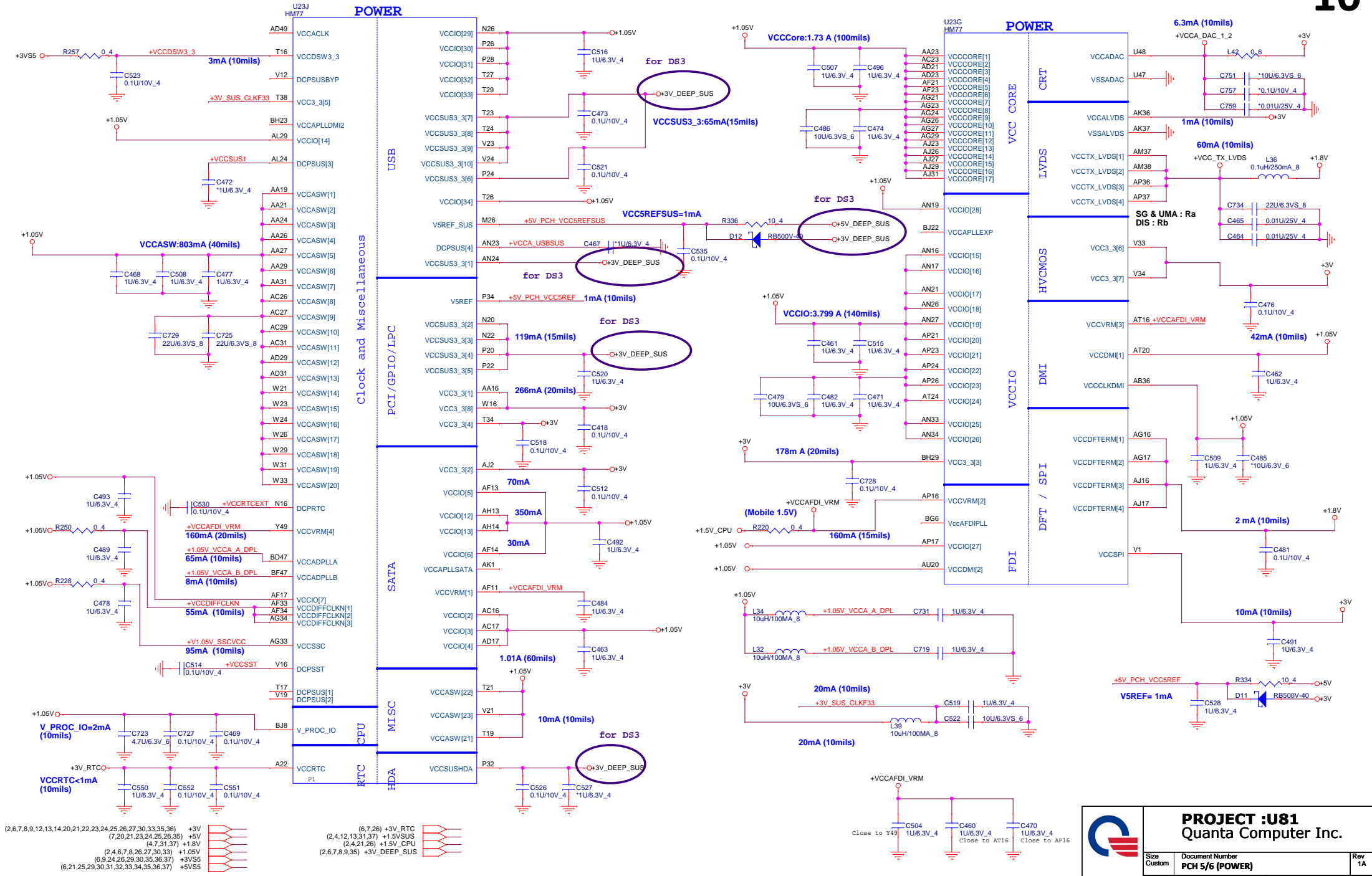
Stuff	SG	UMA
	Ra	Rb
NC	Rb	Ra

**PROJECT :U81**  
 Quanta Computer Inc.

Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 1A  
 Date: Friday, May 24, 2013 Sheet 9 of 37

Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)



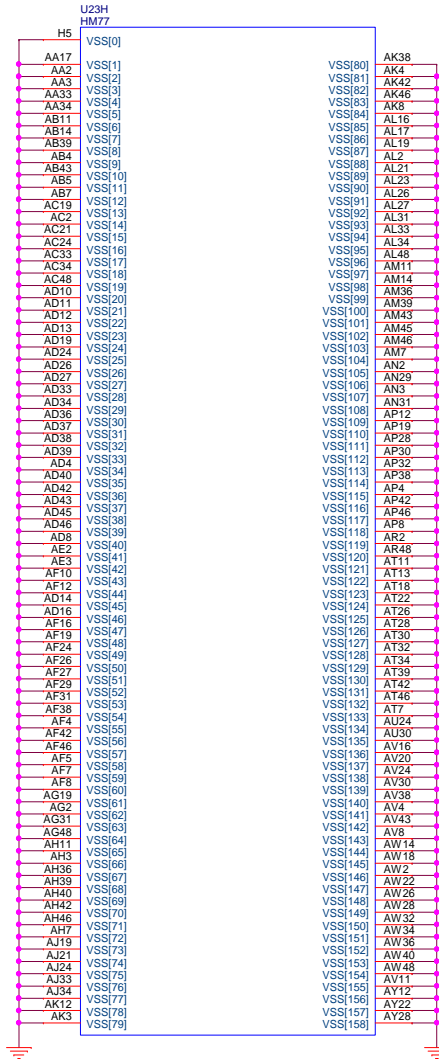
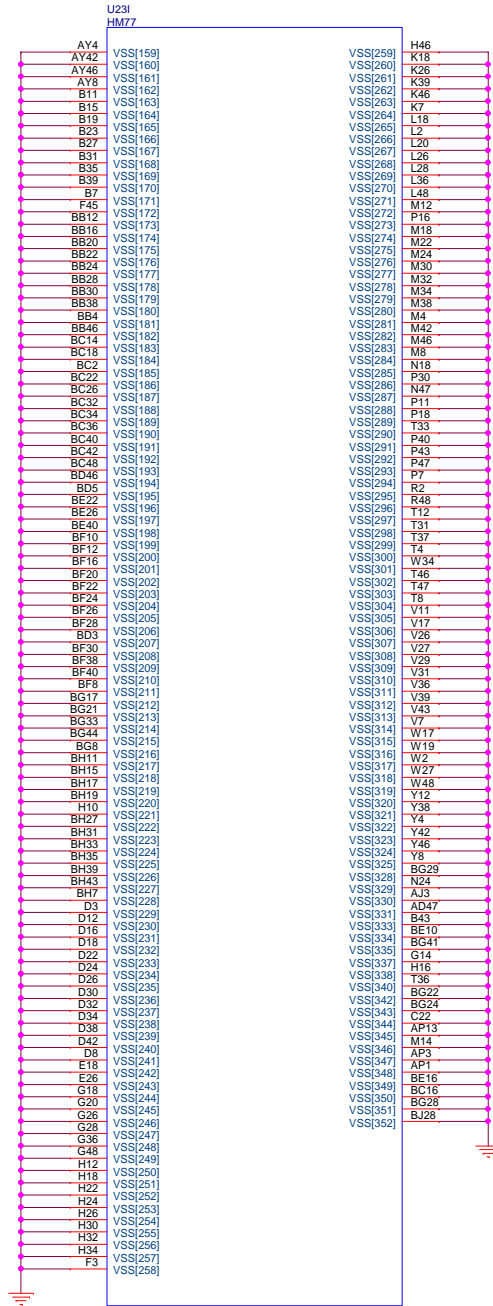
(2,6,7,8,9,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36)	+3V	(6,7,26)	+3V_RTC
(7,20,21,23,24,25,26,35)	+5V	(2,4,12,13,31,37)	+1.5VSUS
(4,7,31,37)	+1.8V	(2,4,21,26)	+1.5V_CPU
(2,4,6,7,8,26,27,30,33)	+1.05V	(2,6,7,8,9,35)	+3V_DEEP_SUS
(6,9,24,26,29,30,35,36,37)	+3VS5		
(6,21,25,29,30,31,32,33,34,35,36,37)	+5VS5		

**PROJECT :U81**  
**Quanta Computer Inc.**

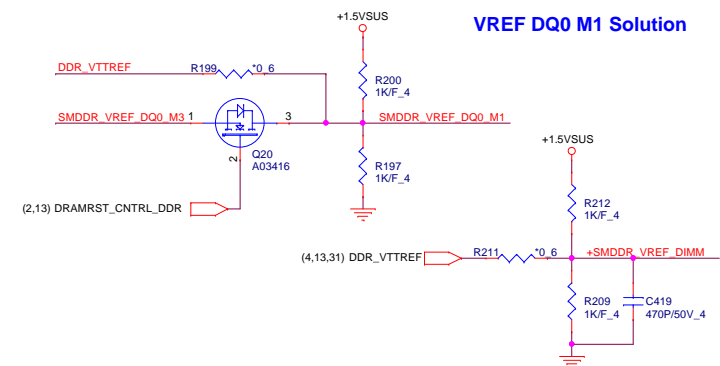
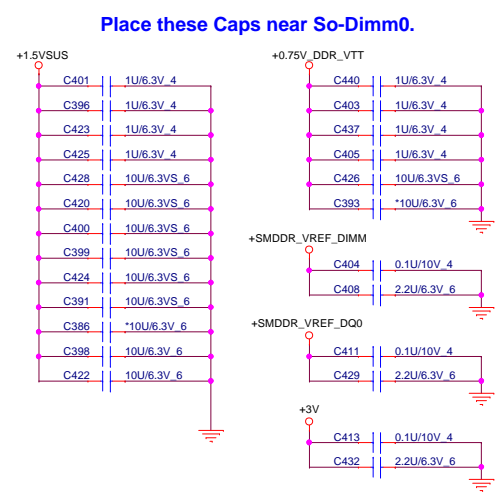
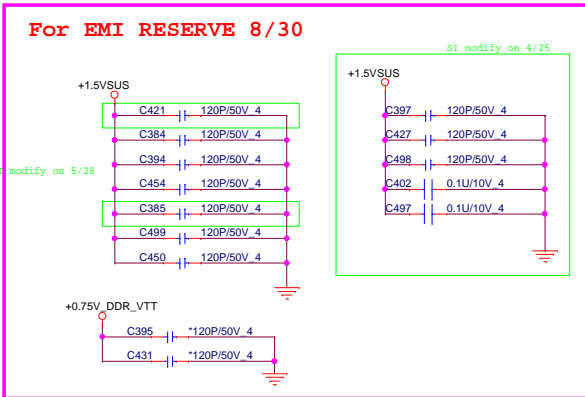
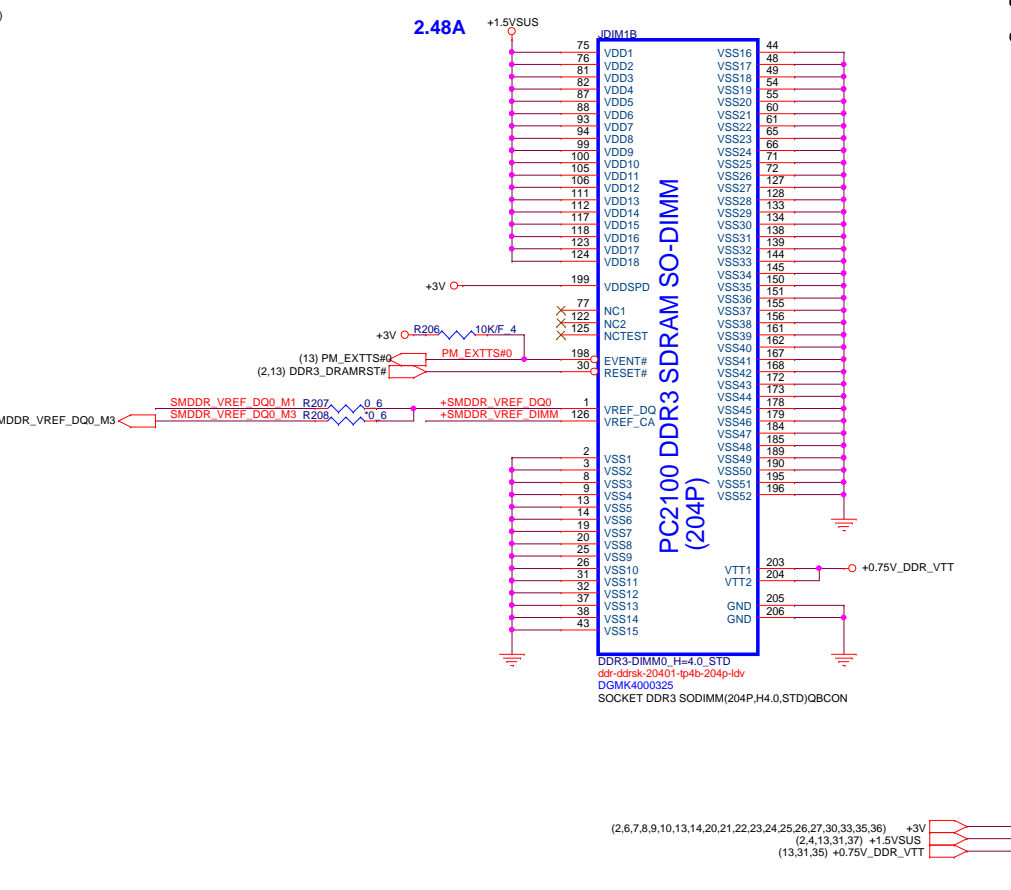
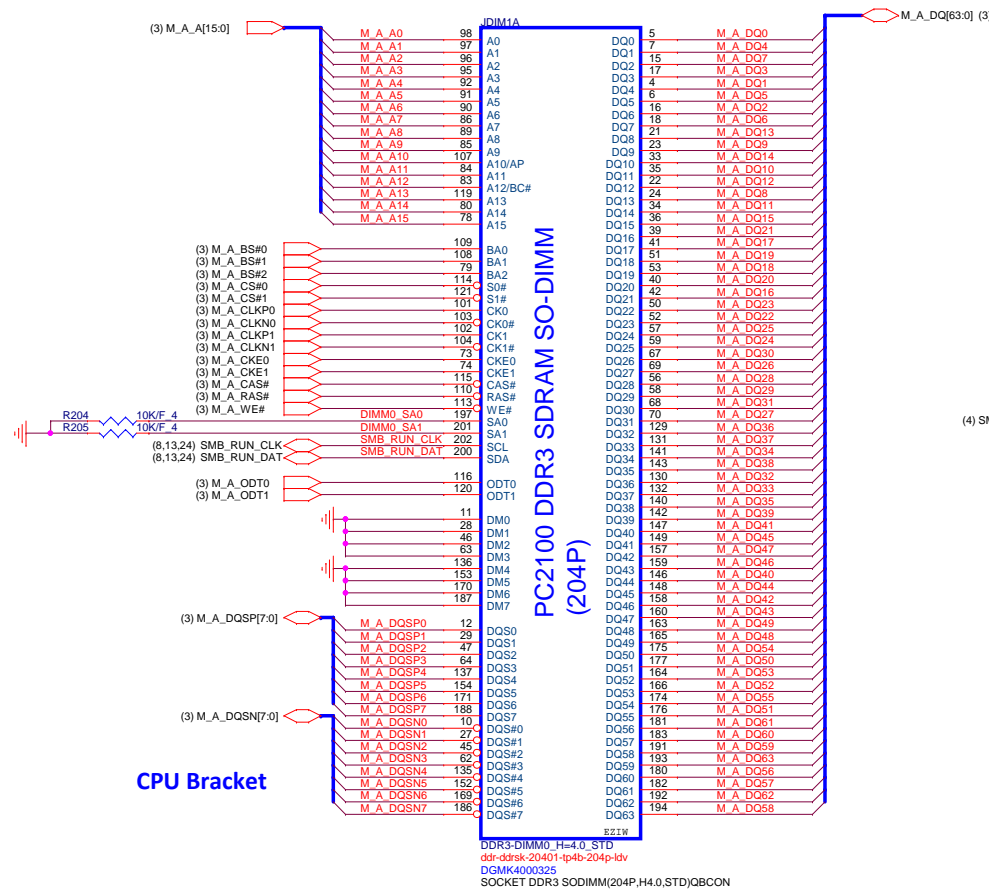
Size	Document Number	Rev
Custom	<b>PCH 5/6 (POWER)</b>	1A
Date:	Monday, May 27, 2013	Sheet
	10 of	37

Cougar Point/Panther Point (GND)

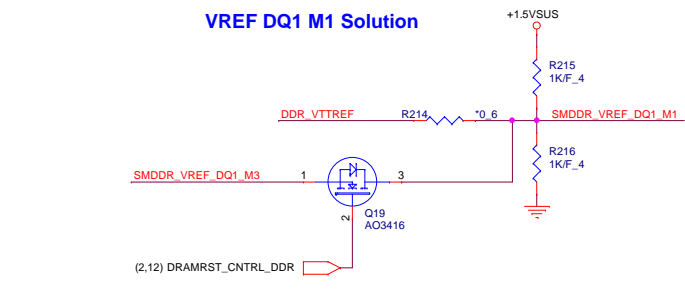
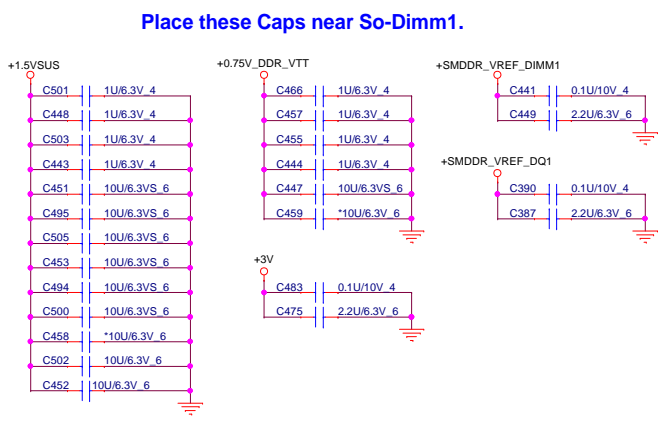
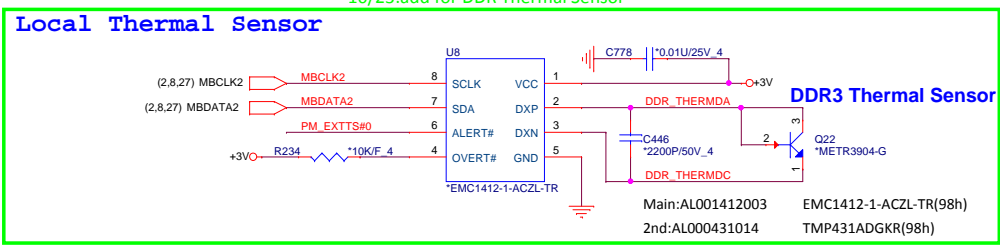
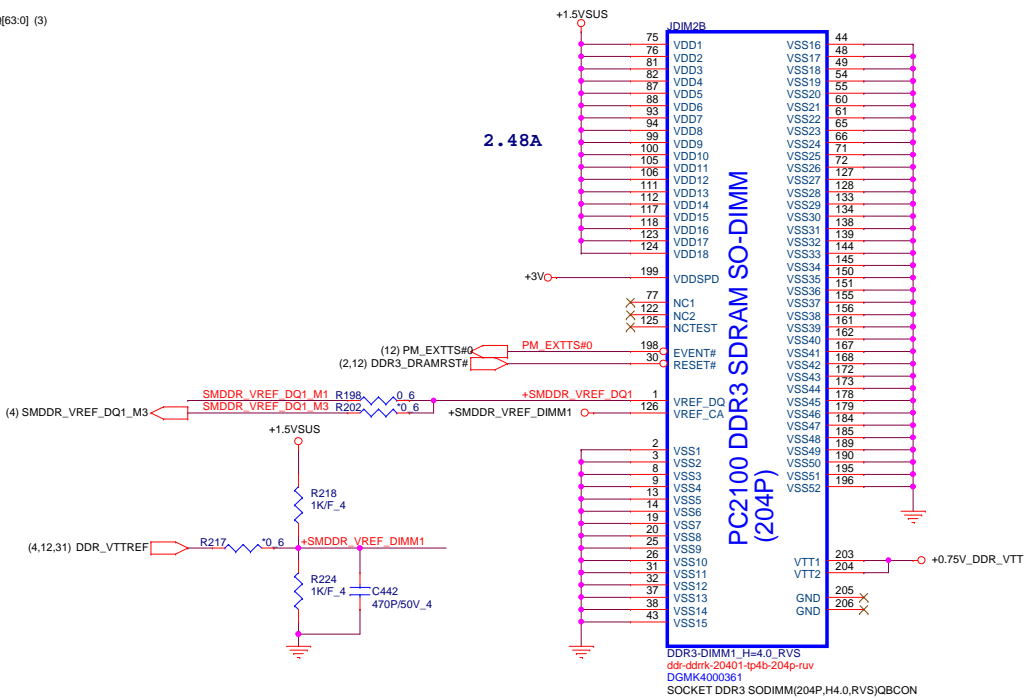
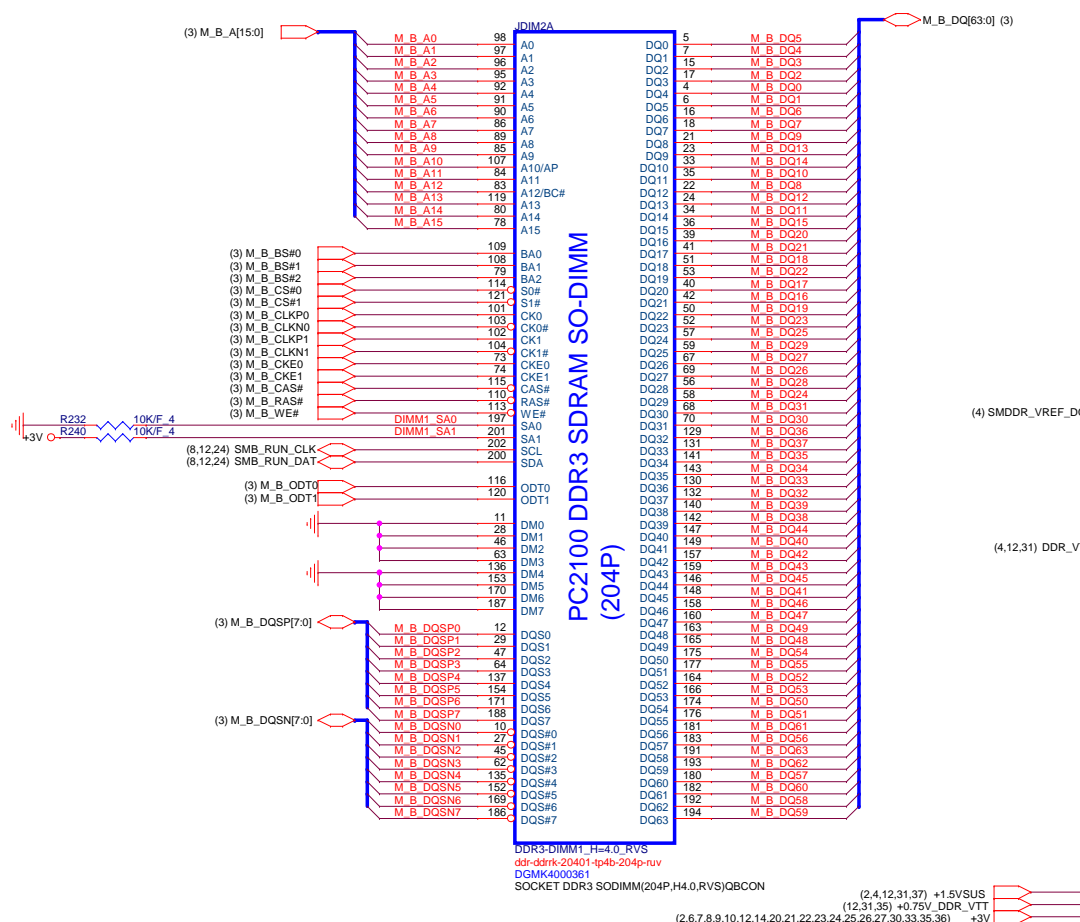
Cougar Point/Panther Point (GND)



	<b>PROJECT :U81</b>		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number PCH 6/6 (GND)		
Date: Friday, May 24, 2013	Sheet 11 of 37		



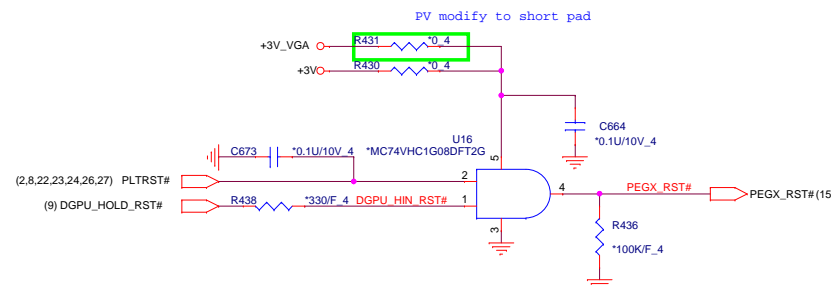
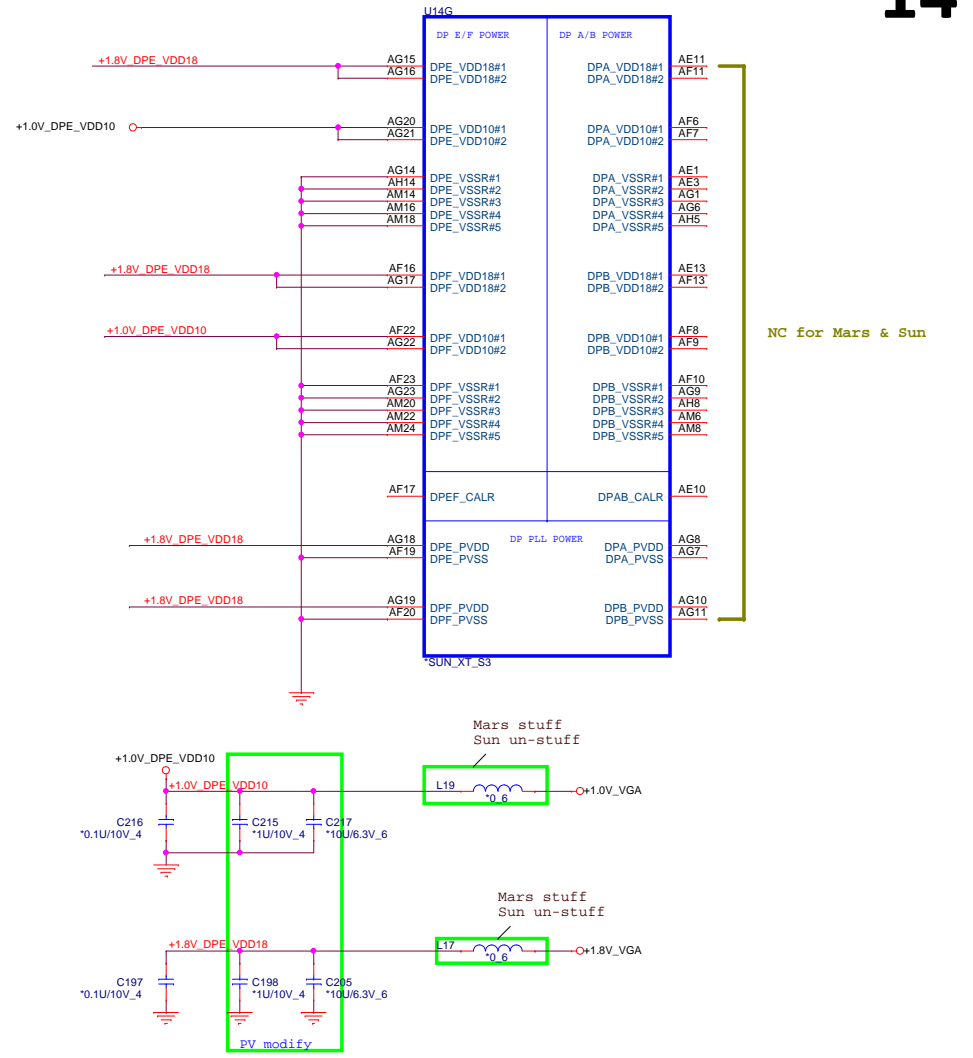
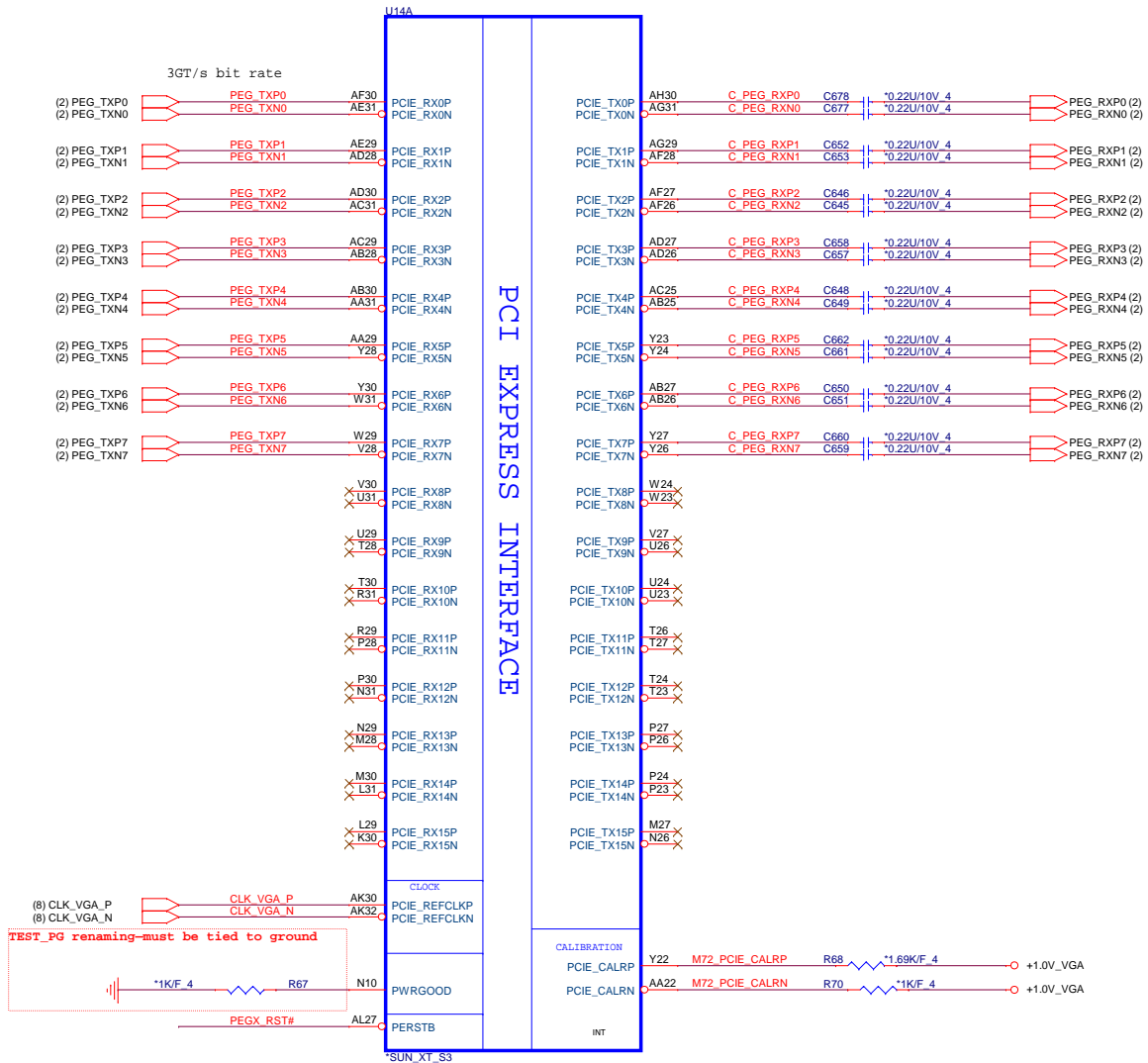
Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
Date: Friday, May 24, 2013	Sheet	12 of 37



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 Quanta Computer Inc.

Size Custom	Document Number <b>DDR3 DIMM1-RVS(4.0H)</b>	Rev 1A
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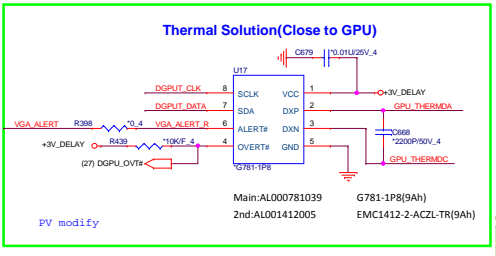
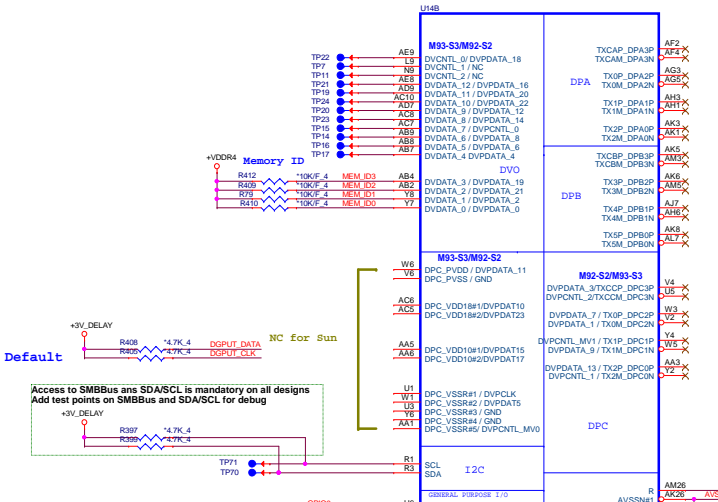




**PROJECT :U81**  
**Quanta Computer Inc.**

Size Custom	Document Number Sun S3 PCIE_Interface	Rev 1A
Date: Friday, May 24, 2013   Sheet 14 of 37		

GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWR_CNTL1	PWR_CNTL4	PWR_CNTL3	PWR_CNTL2	PWR_CNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	1	0	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V



**MLPS Implementation**

- Connect GPIO\_28 to 10K pulldown to enable MLPS
- If any of PS\_0/1/2/3 is not used, leave "no connect"
- R<sub>pu</sub>, R<sub>pd</sub> and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

**Capacitor Lookup Table**

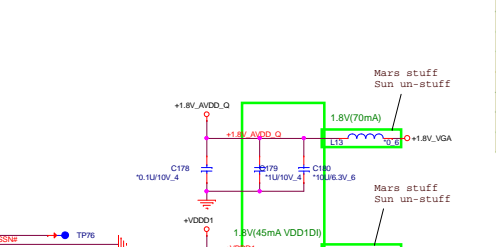
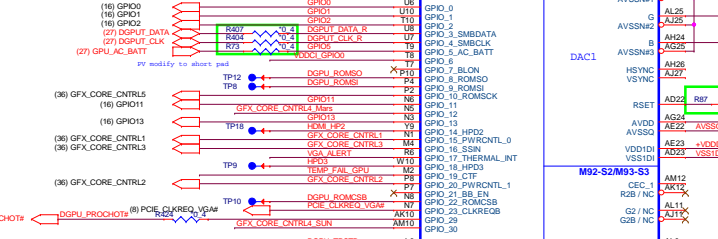
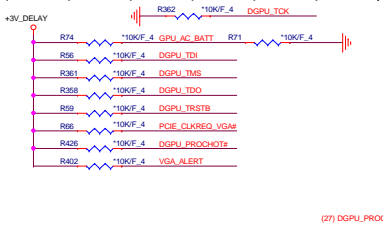
C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

**Resistor Divider Lookup Table**

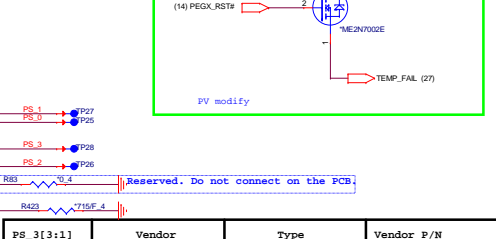
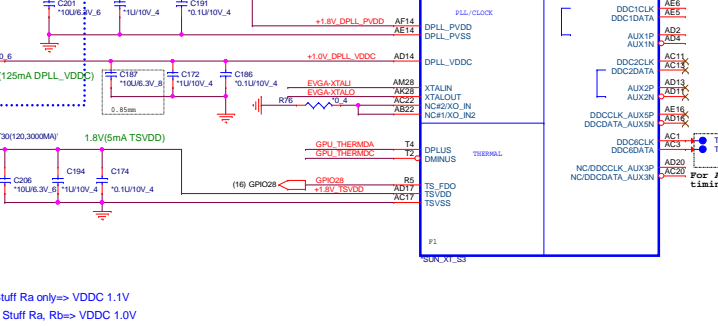
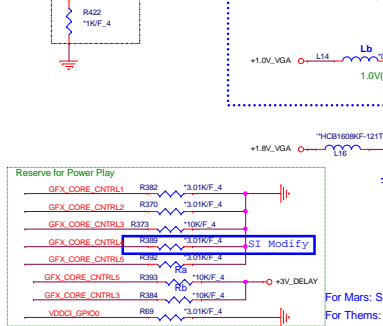
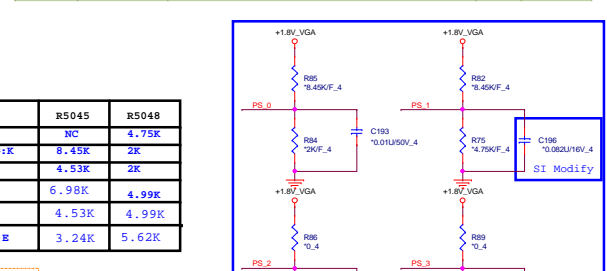
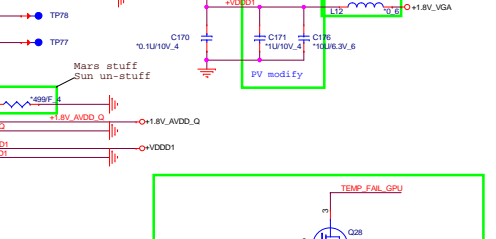
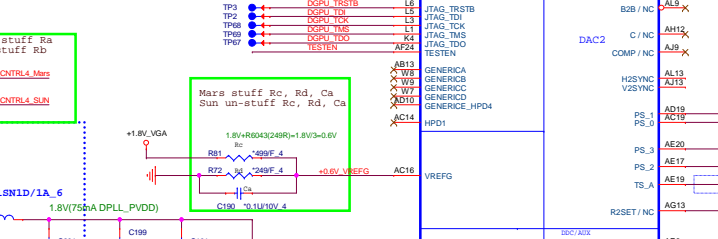
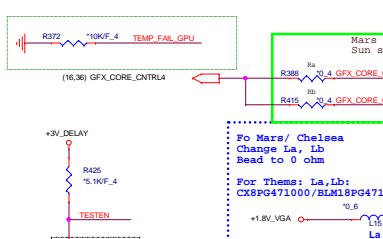
R <sub>pu</sub> (Ohm)	R <sub>pd</sub> (Ohm)	Bits(3,2,1)
4750	2000	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

**MLPS Circuit**

PS\_0, PS\_1, PS\_2, PS\_3



Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13, gpio_12, gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwrsv_erb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM_Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM_Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM_Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[0]	aud_port_cp[0]			



**PS\_3[3:1]**

Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix- F(Ruma)	128Mx16 *4, 900Mhz	H5TC2663FPR-11C	NC
001	Micron- V89C/K	128Mx16 *4, 900Mhz	MT41J128M16J7-093G:K	8.45K 2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646E-BC1A	4.53K 2K
011	Hynix- Huma die	256Mx16 *4, 900Mhz	H5TC463FAPR-11C	6.98K 4.99K
100	Samsung- E die	256Mx16 *4, 900Mhz	K4W4G1646B-HC1A	4.53K 4.99K
101	Micron- E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K 5.62K

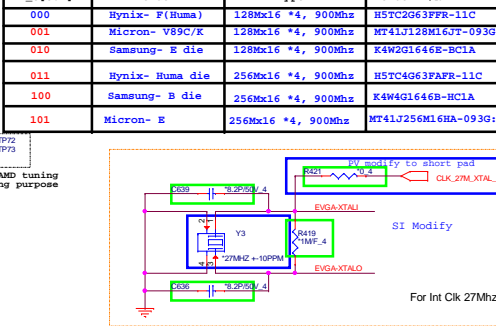
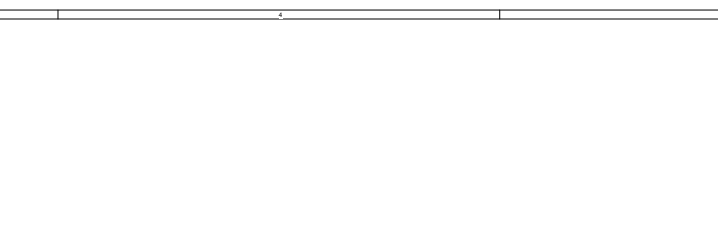
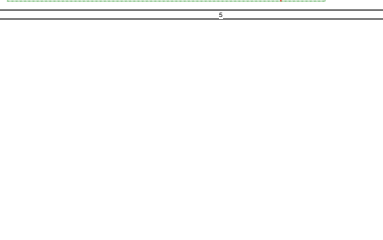
**BIT5 => BIT0**

PS0 => 11001

PS1 => 01000

PS2 => 00000

PS3 => 11000



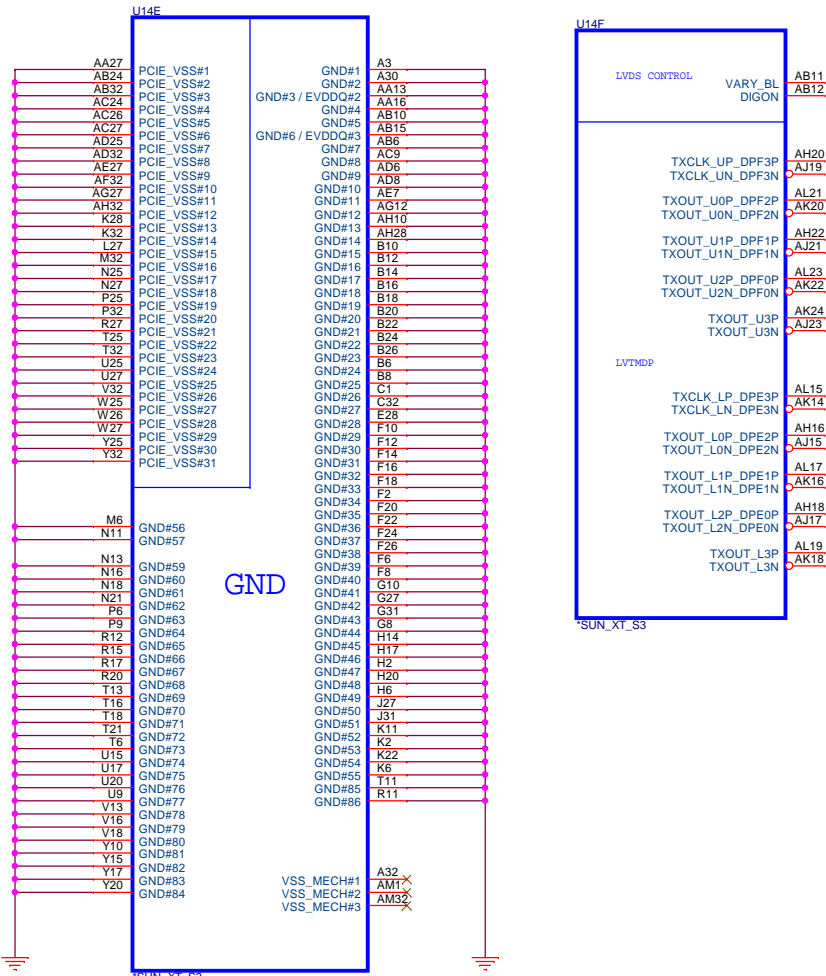
**PROJECT :U81**

**Quanta Computer Inc.**

Doc Number: Sun S3 Main

Date: Monday, May 27, 2013

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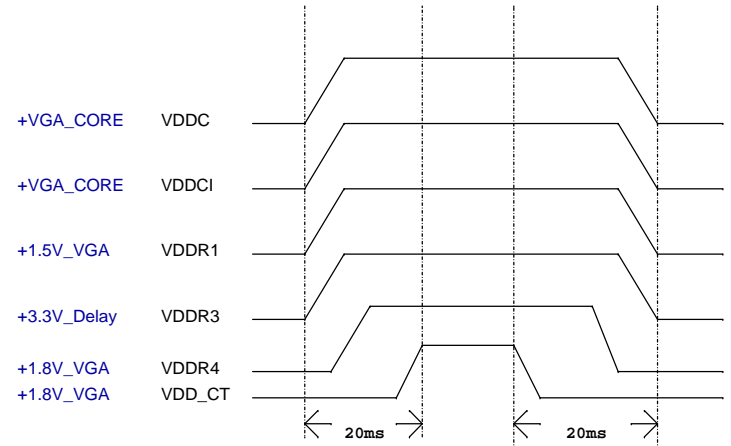
**CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS**  
**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRs_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	RESERVED	X
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

**NOTE1: AMD RESERVED CONFIGURATION STRAPS**  
**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.**

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

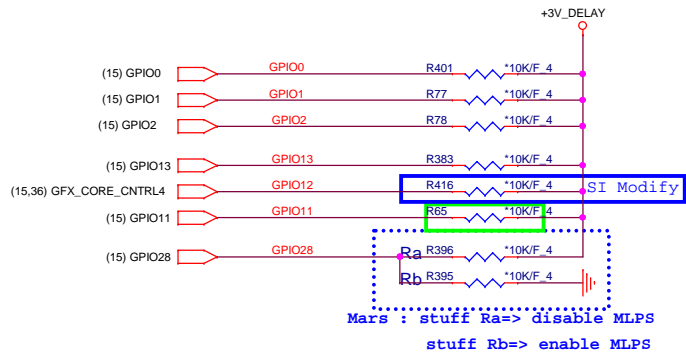
**Power Up/Down Sequence**



**Memory Aperture size(Seymour)**

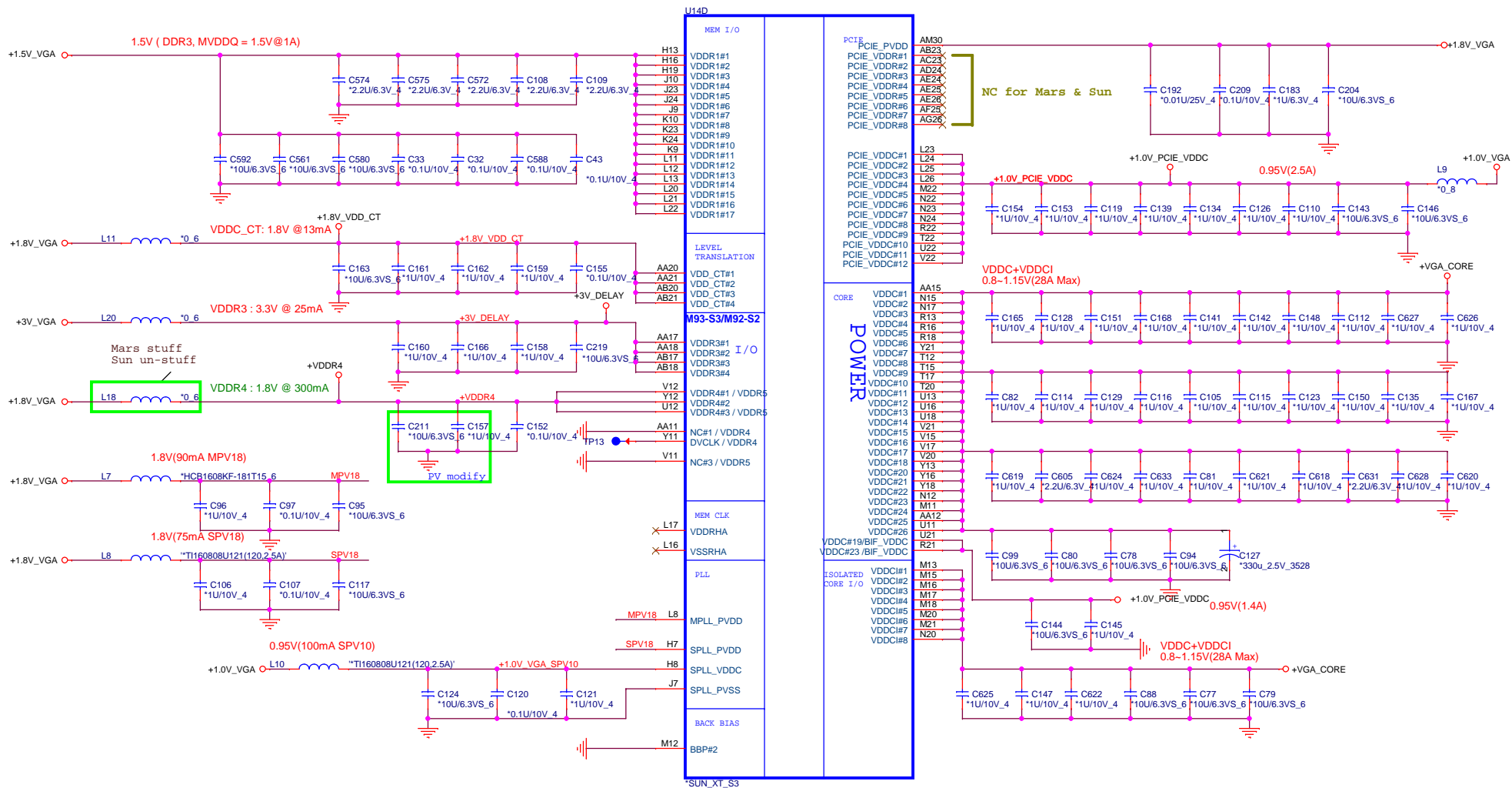
GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.




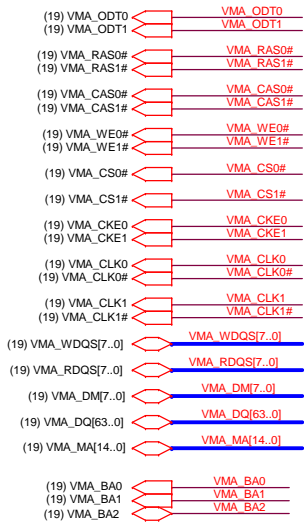
**PROJECT :U81**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>Sun S3 GND / LVDS/ Straps</b>	Rev 1A
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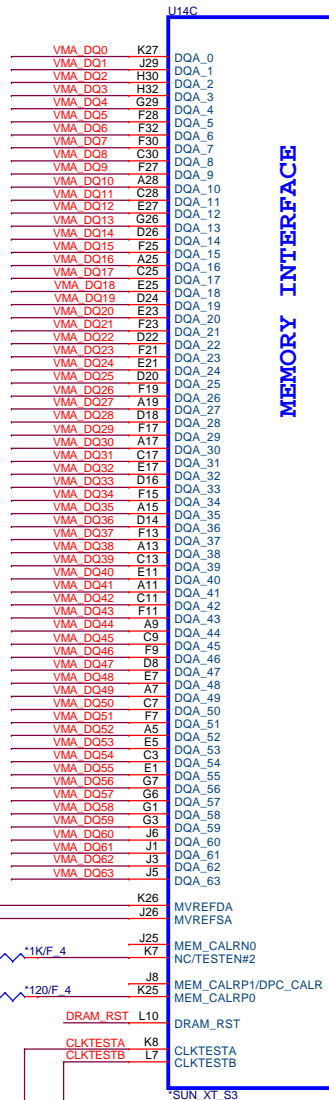


- ➔ +1.5V\_VGA (18.19.24.37)
- ➔ +1.8V\_VGA (14.15.37)
- ➔ +1.0V\_VGA (14.15.24.37)
- ➔ +VGA\_CORE (24.36.37)
- ➔ +3V\_DELAY (15.16)

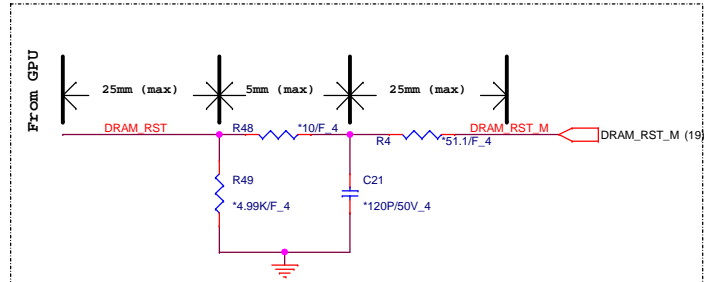
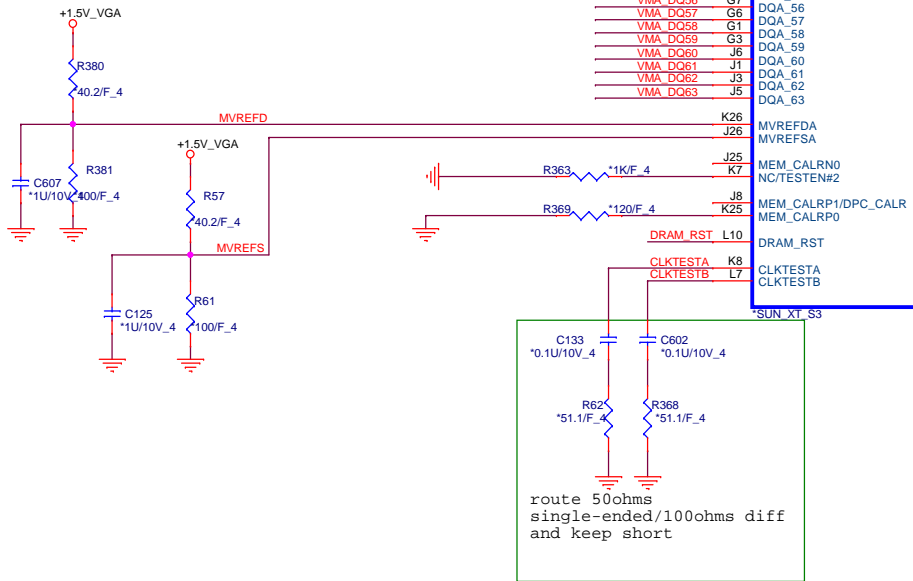
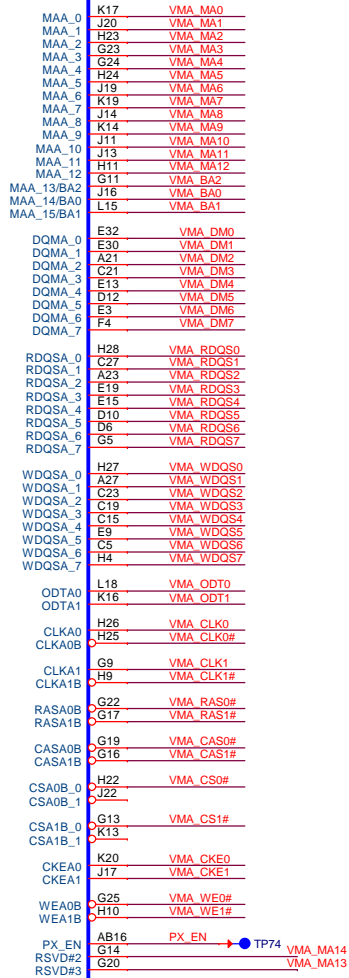
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		Quanta Computer Inc.	
Size Custom	Document Number	<b>Sun S3 Power_and_NC</b>	
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		Rev 1A	



support 1gbt  
VRAM ( 64M X 16 )



MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

+1.5V\_VGA (17.19.24.37)

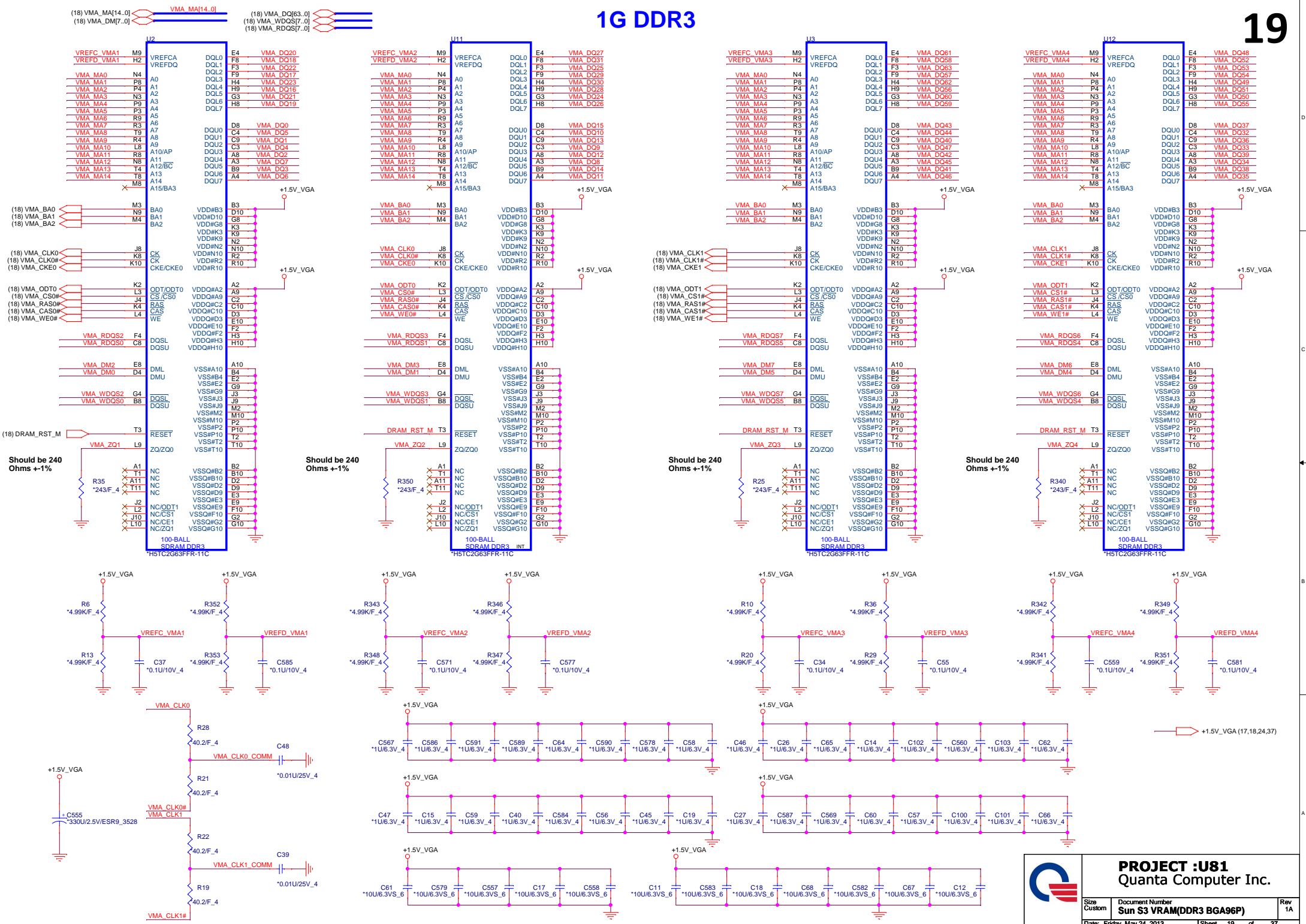


**PROJECT :U81**  
Quanta Computer Inc.

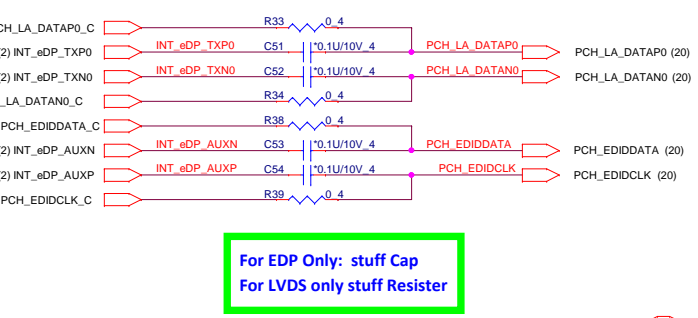
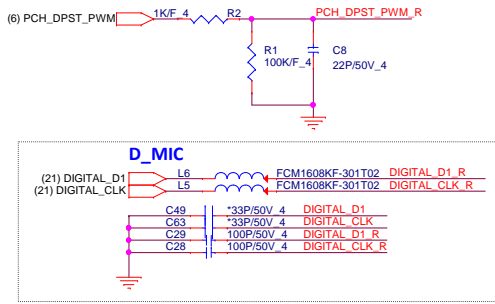
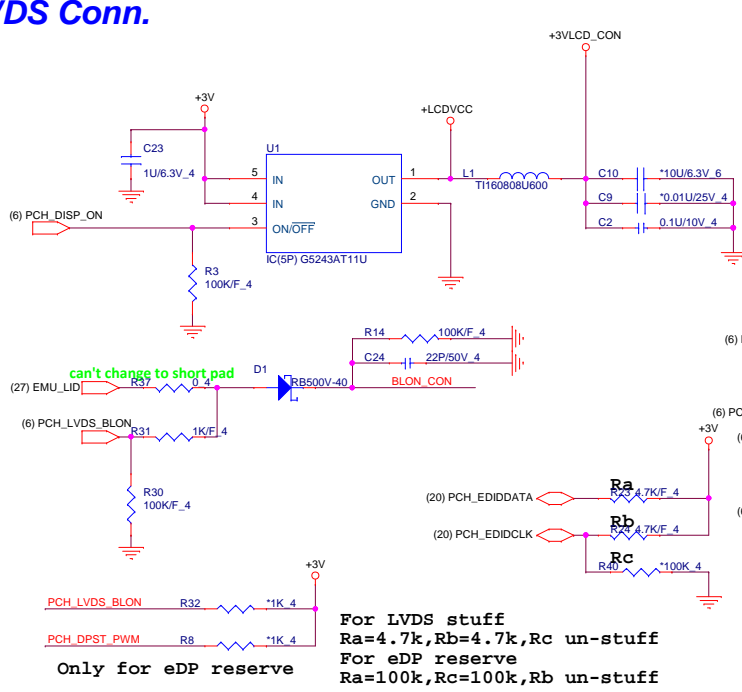
Size Custom	Document Number <b>Sun S3 MEM Interface</b>	Rev 1A
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1G DDR3



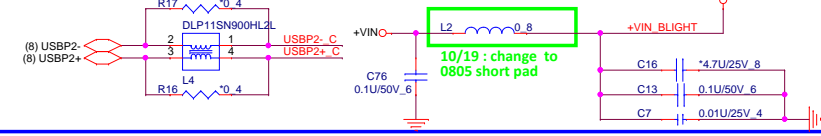
# LVDS Conn.



**For EDP Only: stuff Cap**  
**For LVDS only stuff Resistor**

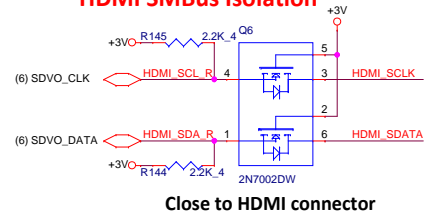
**For EDP Only: Stuff Rd**  
**For LVDS Only: Stuff Rc**

### USB CAMERA

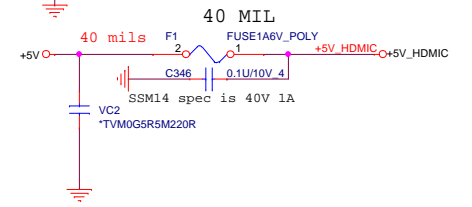
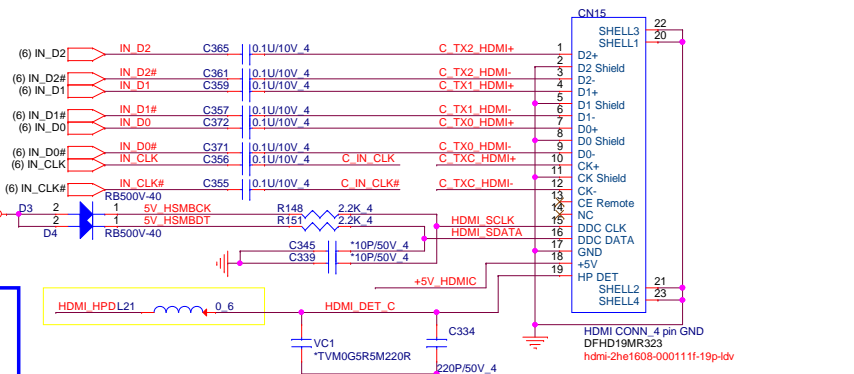
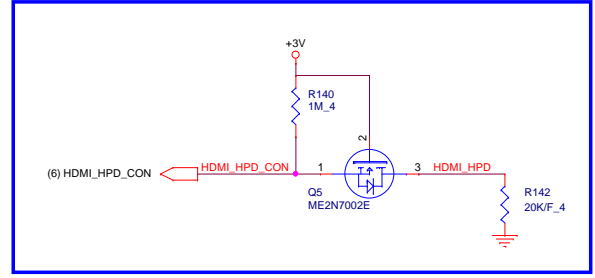
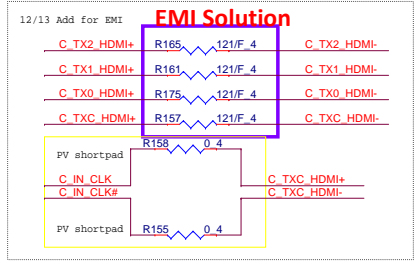


# HDMI Conn.

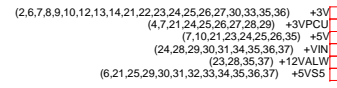
## HDMI SMBus Isolation



Close to HDMI connector

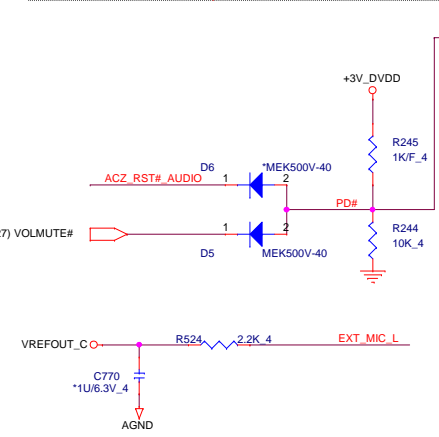
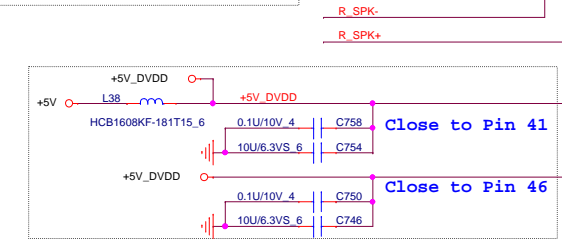
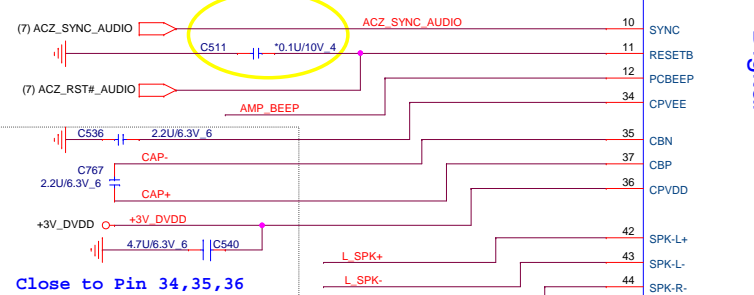
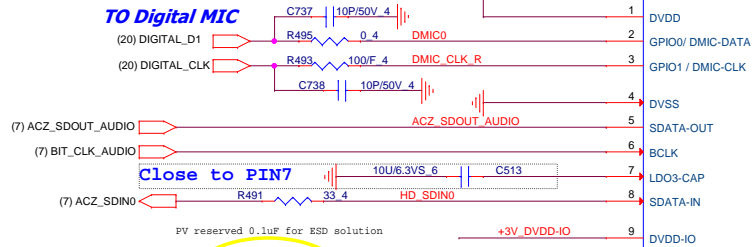
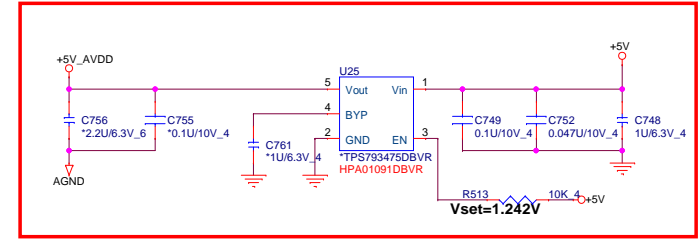
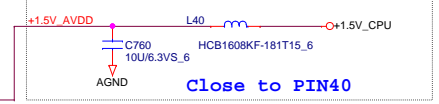
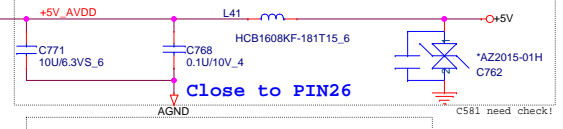
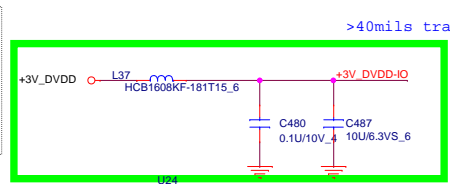
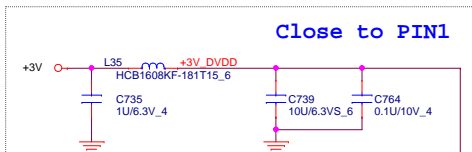


for EMI request



**PROJECT :U81**  
**Quanta Computer Inc.**

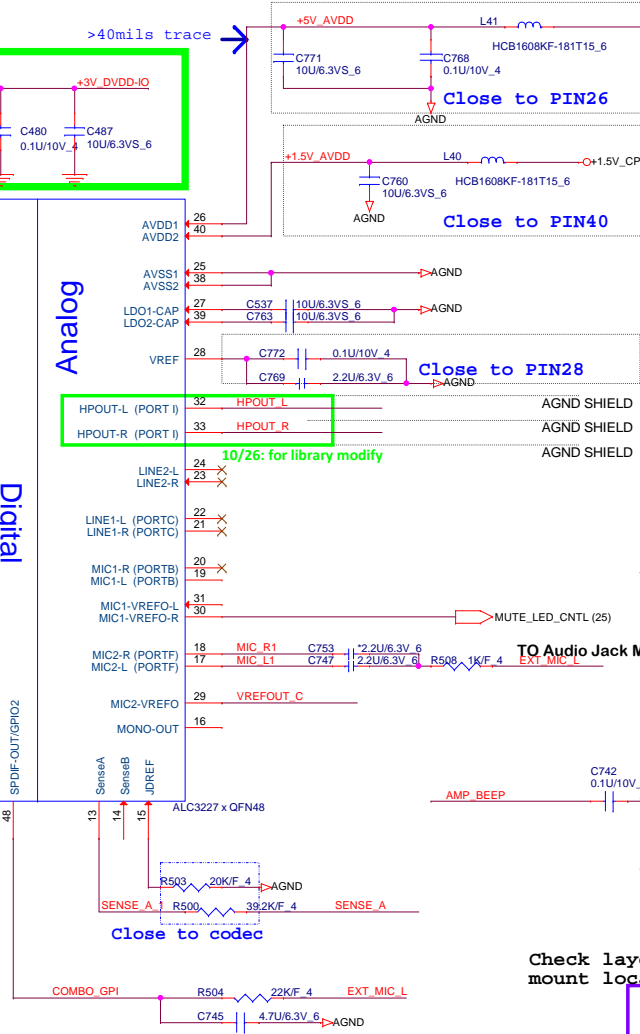
Size Custom	Document Number <b>LCD/HDMI/Camera</b>	Rev 1A
Date: Monday, May 27, 2013		Sheet 20 of 37



**Close to CODEC**

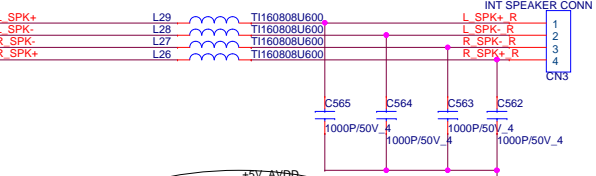
L_SPK+	EC27	1	21000P/50V_4
L_SPK-	EC25	1	21000P/50V_4
R_SPK+	EC23	1	21000P/50V_4
R_SPK-	EC24	1	21000P/50V_4
ACZ_SDIN0	EC33	1	*33P/50V_4
ACZ_SDOUT_AUDIO	EC22	1	*10P/50V_4
ACZ_SYNC_AUDIO	EC35	1	*10P/50V_4
BIT_CLK_AUDIO	EC34	1	*33P/50V_4

FOR EMI

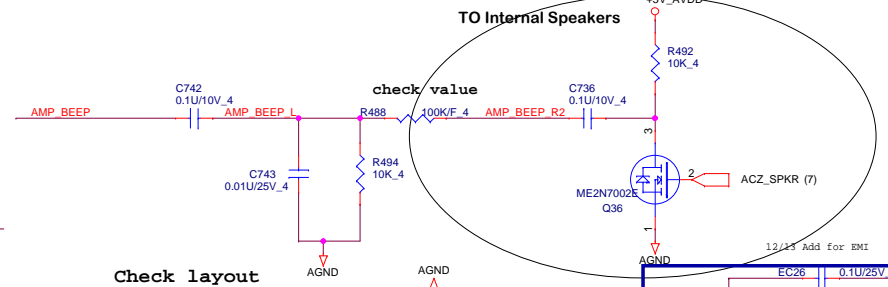


TO Headphone jack

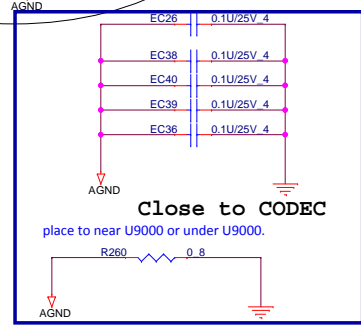
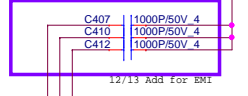
Close to Speaker  
Speaker 4 ohm: 40mils



TO Internal Speakers



Check layout  
mount location



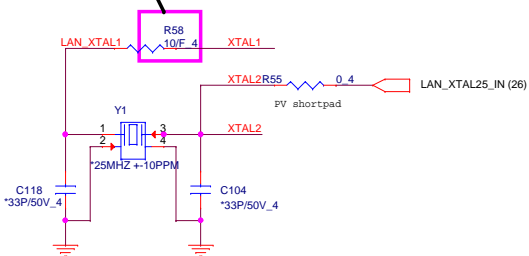
Close to CODEC  
place to near U9000 or under U9000.



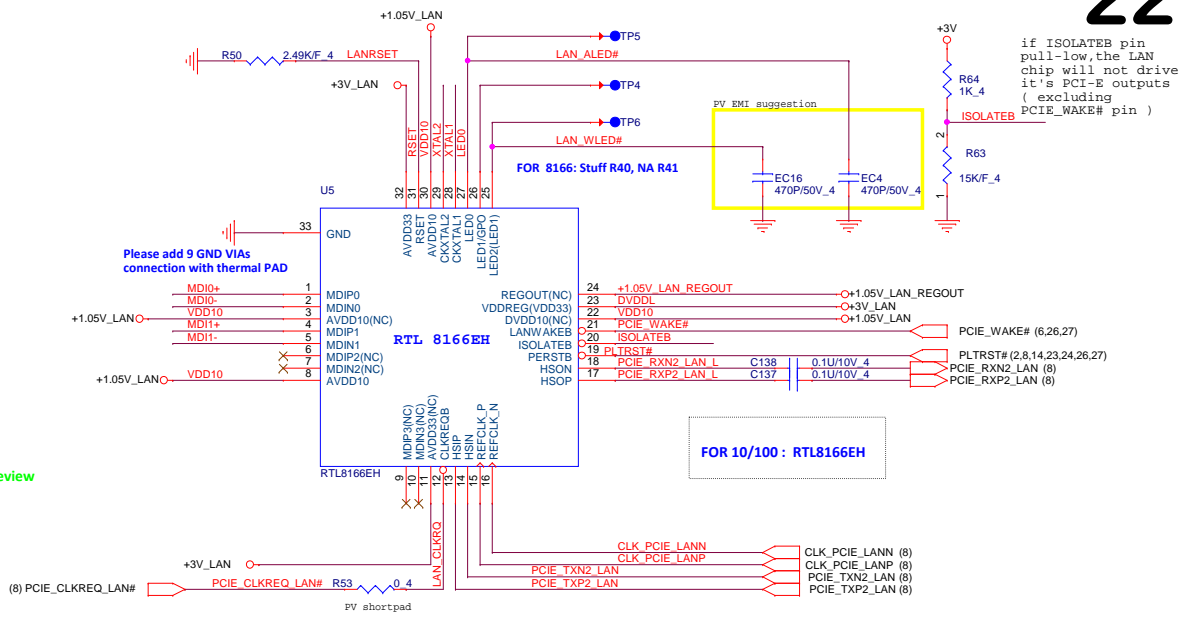
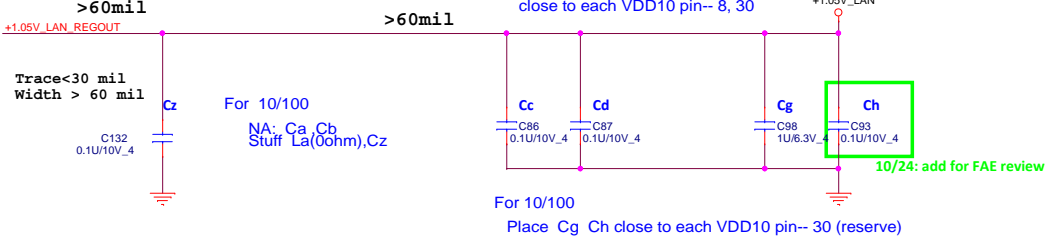
**PROJECT :U81**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC 3227/D-MIC	1A
Date: Friday, May 24, 2013	Sheet	21 of 37

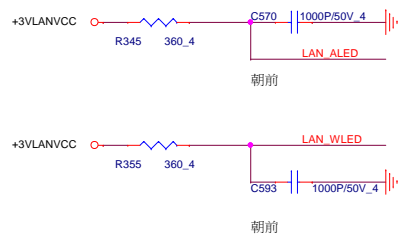
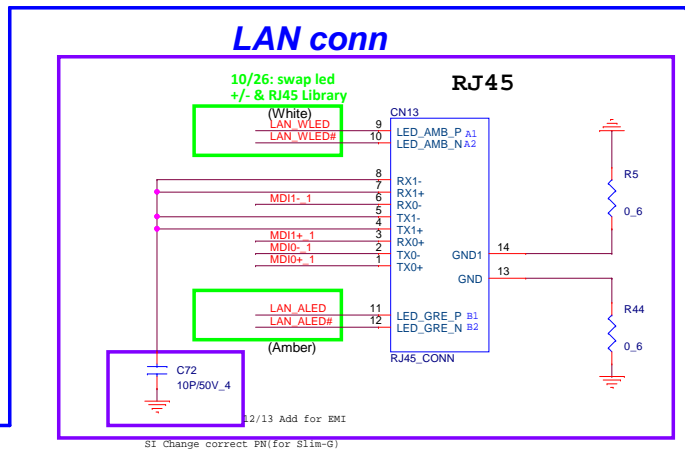
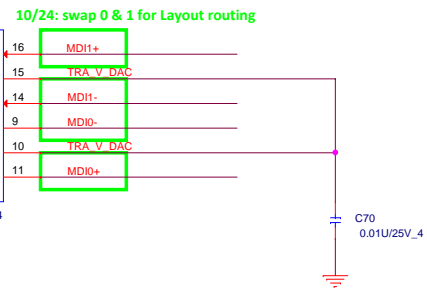
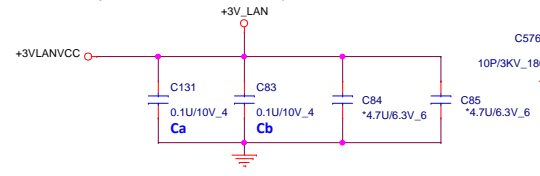
For EMI 0 ~ 22 ohm



Power trace Layout 宽度 > 60mil



For 10/100 Stuff Ca and Cb only, close to each VDD33 pin-- 23, 32

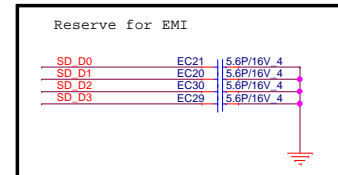
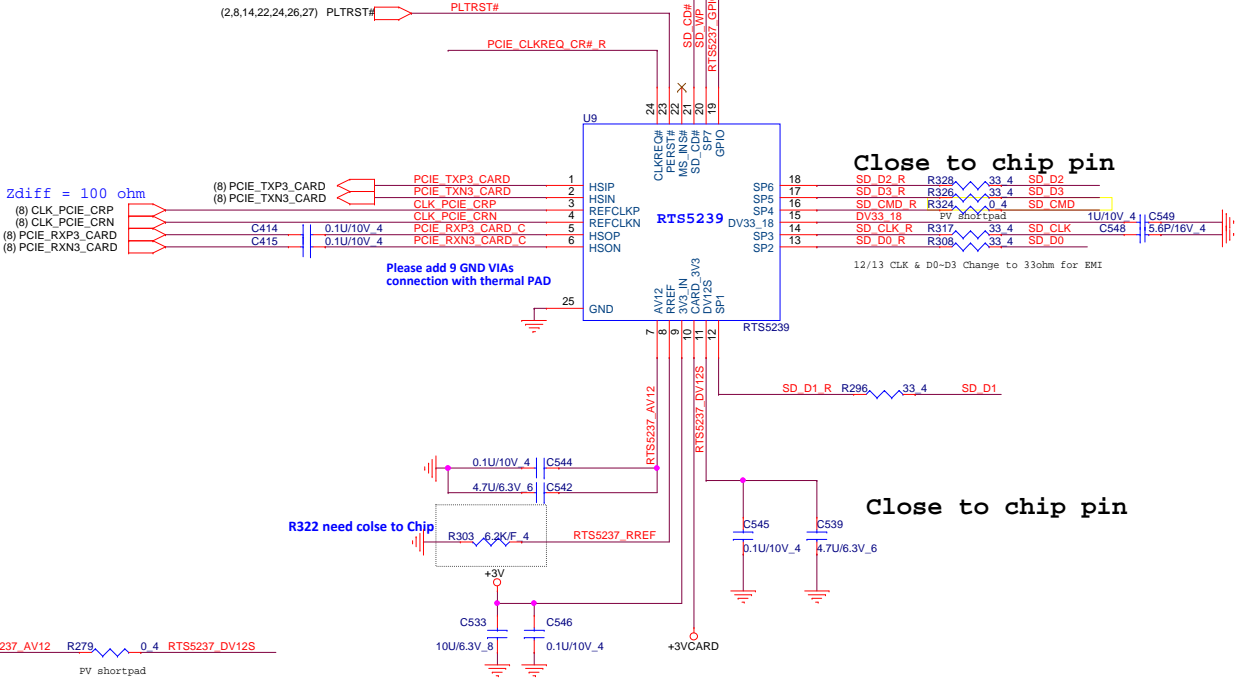


(2,6,7,8,9,10,12,13,14,20,21,23,24,25,26,27,30,33,35,36) +3V (26,35) +3VLANVCC

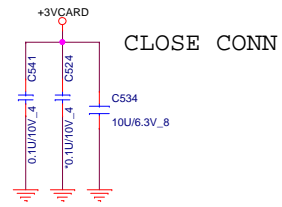
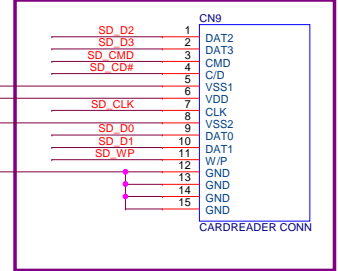
(8) PCIE\_CLKREQ\_CR# R331 0.4 PCIE\_CLKREQ\_CR#\_R

SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin



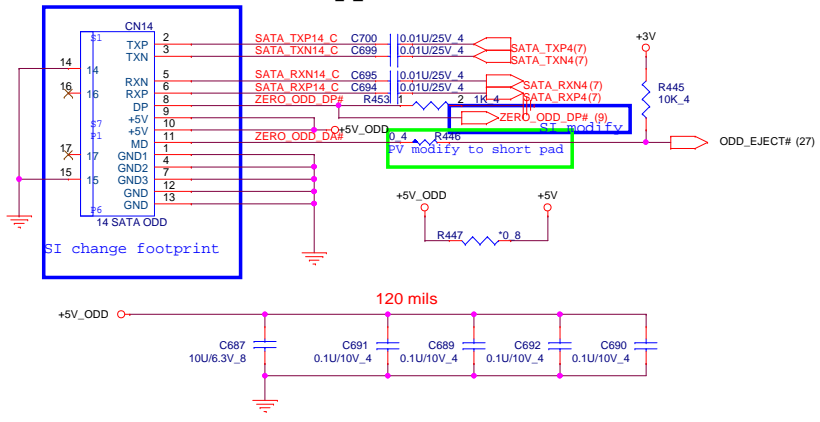
SD / MMC CARD READER



SATA ODD CONNECTOR

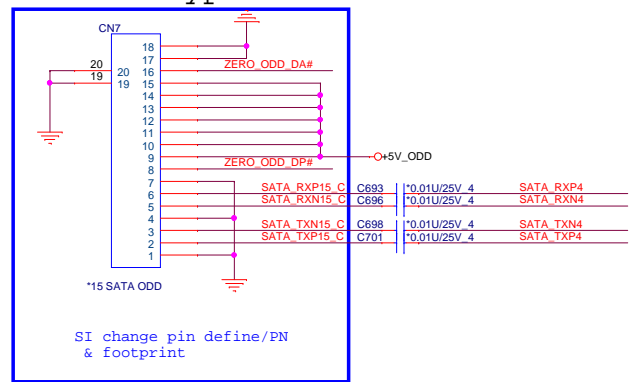
14" SATA ODD

Bypass CAP close conn



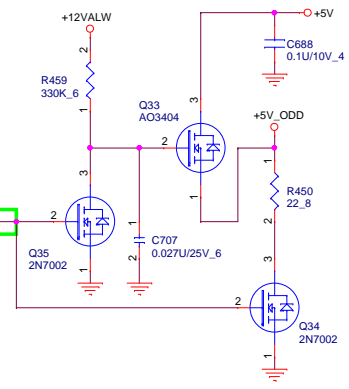
15" SATA ODD

New Type

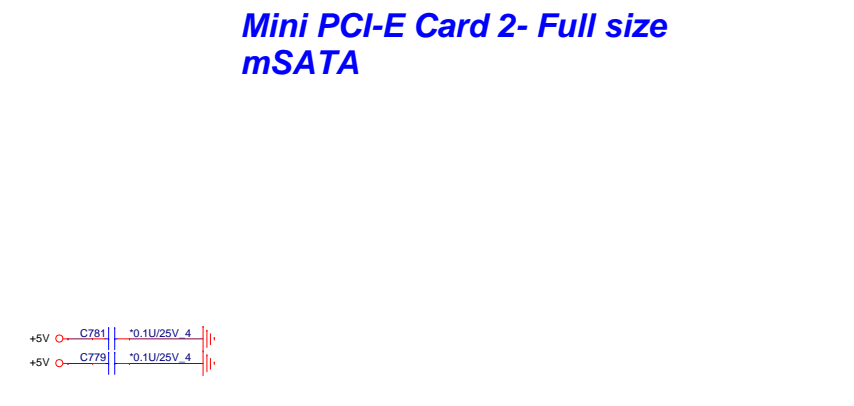
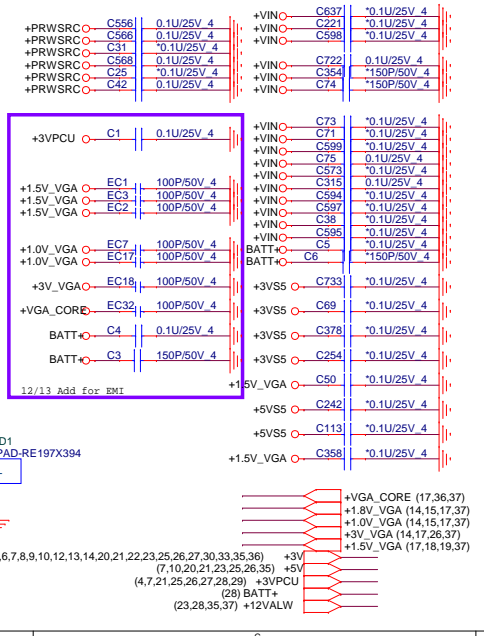
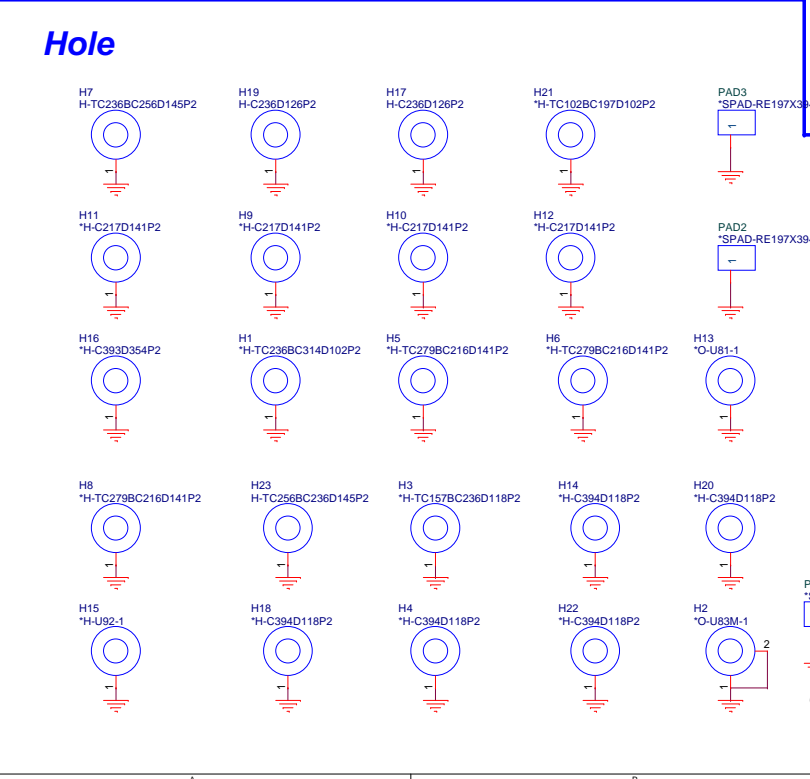
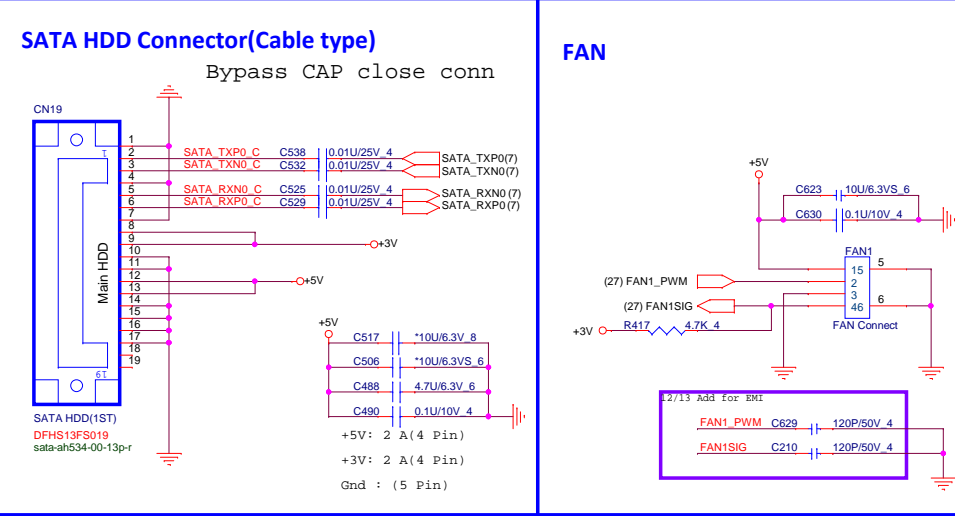
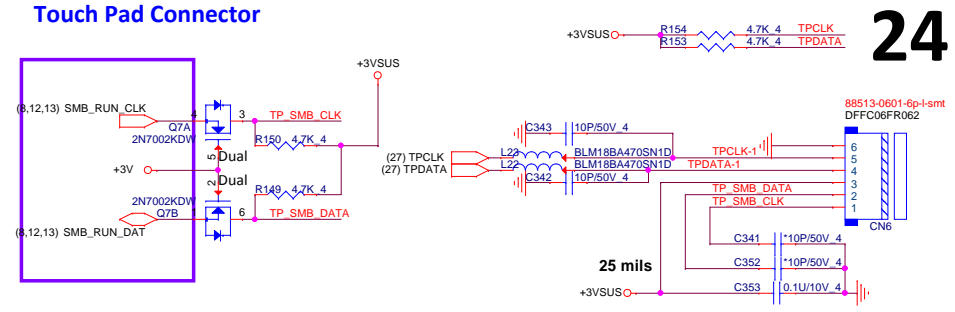
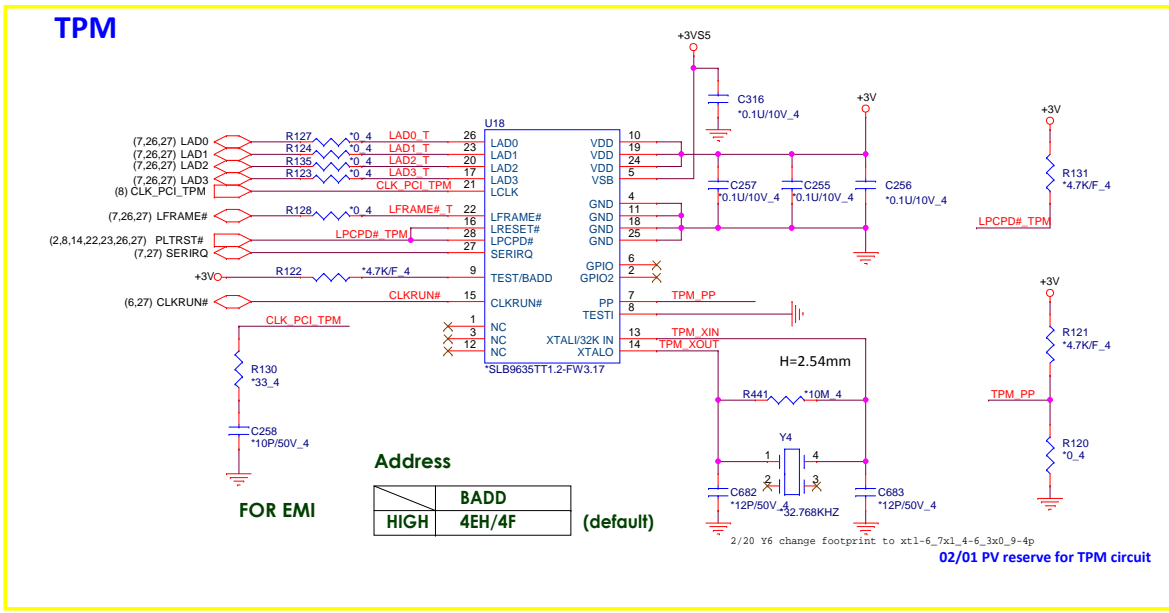


PV modify to short pad  
(27) ZERO\_PWR\_ODD

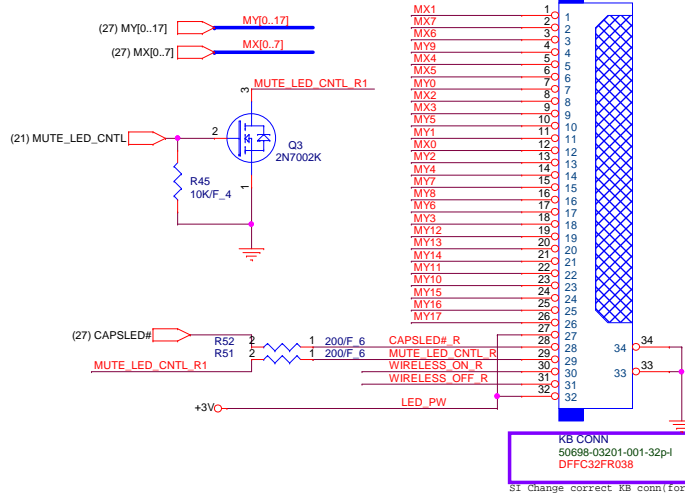
High : ODD power down  
Low : ODD power on



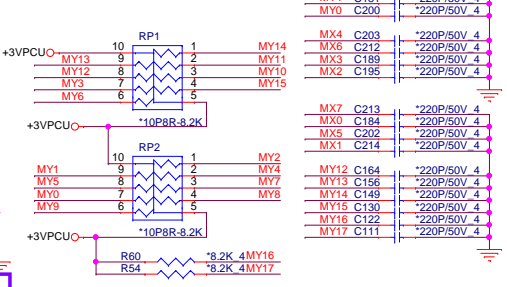




# KEYBOARD Con.

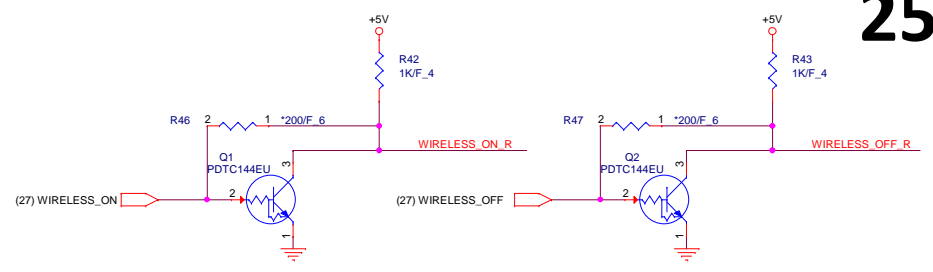


## KEYBOARD PULL-UP

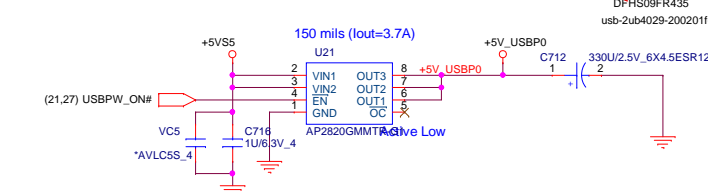
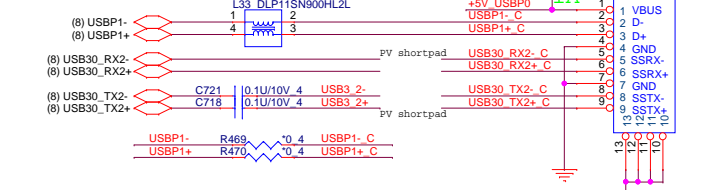
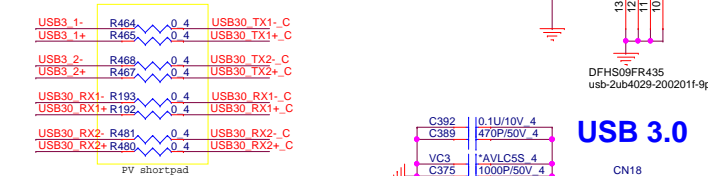
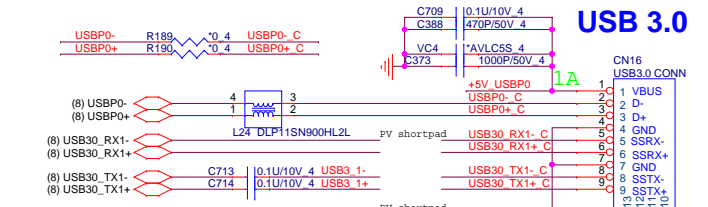
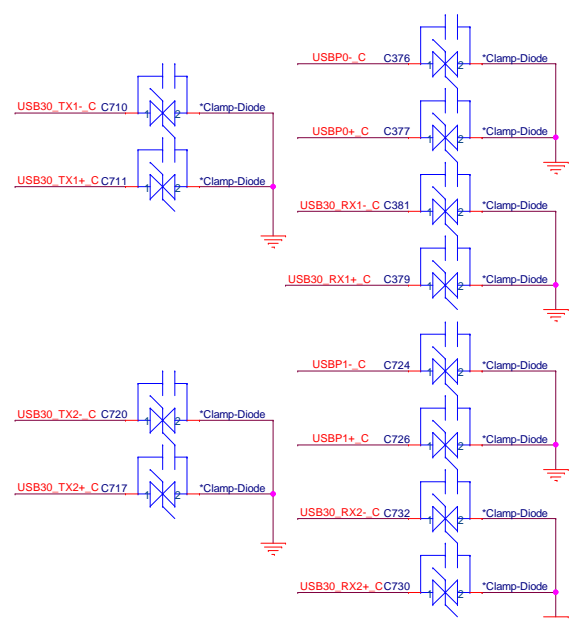


MY5	C188	*220P/50V_4
MY6	C173	*220P/50V_4
MY3	C169	*220P/50V_4
MY7	C177	*220P/50V_4
MY8	C175	*220P/50V_4
MY9	C208	*220P/50V_4
MY10	C136	*220P/50V_4
MY11	C140	*220P/50V_4
MY1	C185	*220P/50V_4
MY2	C182	*220P/50V_4
MY4	C181	*220P/50V_4
MY0	C200	*220P/50V_4
MX4	C203	*220P/50V_4
MX6	C212	*220P/50V_4
MX3	C189	*220P/50V_4
MX2	C195	*220P/50V_4
MX7	C213	*220P/50V_4
MX0	C184	*220P/50V_4
MX5	C202	*220P/50V_4
MX1	C214	*220P/50V_4
MY12	C164	*220P/50V_4
MY13	C156	*220P/50V_4
MY14	C149	*220P/50V_4
MY15	C130	*220P/50V_4
MY16	C122	*220P/50V_4
MY17	C111	*220P/50V_4

KB CONN  
50698-03201-001-32p-I  
DFFC32FR038  
S1 Change correct KB conn(for S1im-G)

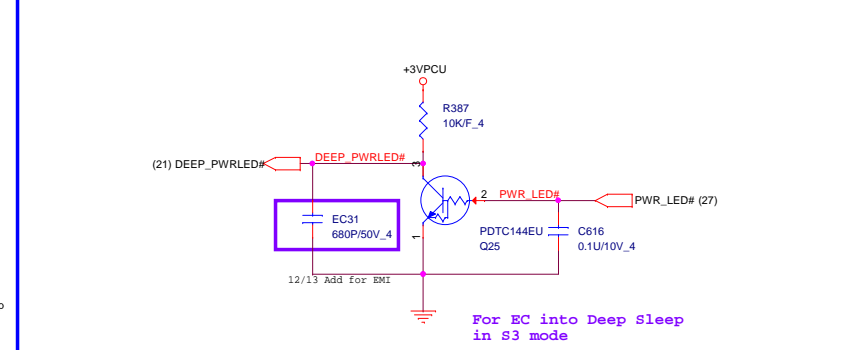
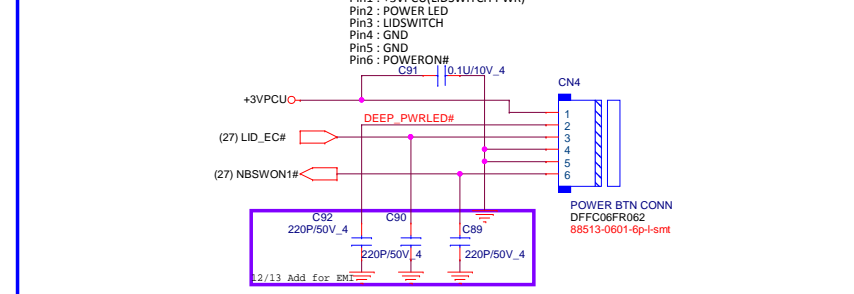


# USB 2.0/3.0 Combo



(6,21,29,30,31,32,33,34,35,36,37) +5V5S  
(4,7,21,24,26,27,28,29) +3VPCU

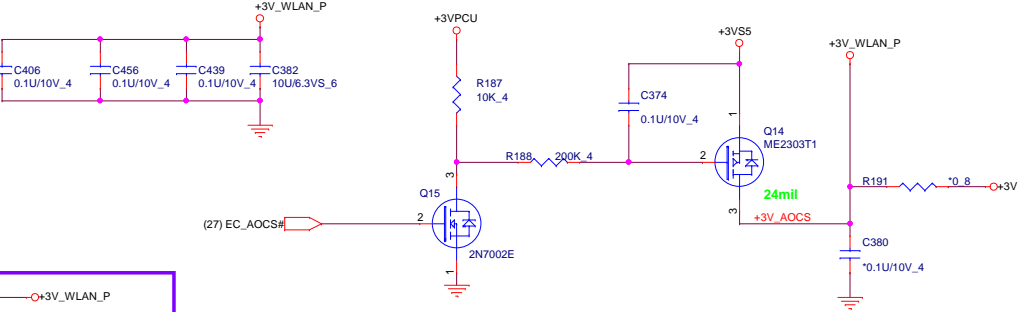
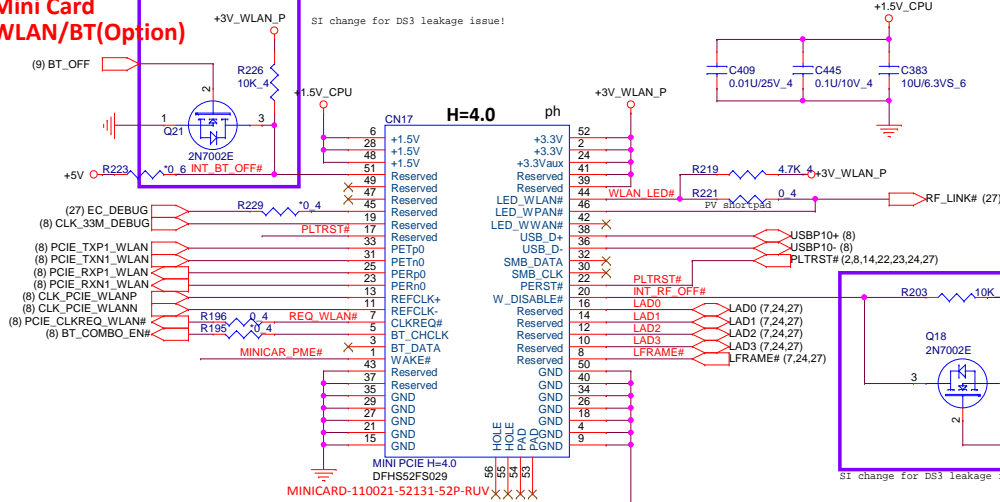
# Power Button Connector



For EC into Deep Sleep in S3 mode

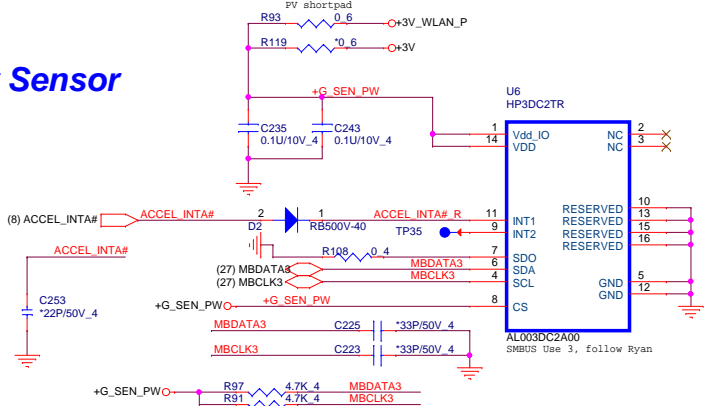
<b>PROJECT :U81</b> Quanta Computer Inc.		
Size Custom	Document Number <b>USB 3.0/KB</b>	Rev 1A
Date: Monday, May 27, 2013	Sheet 25 of 37	

### Mini Card WLAN/BT(Optional)

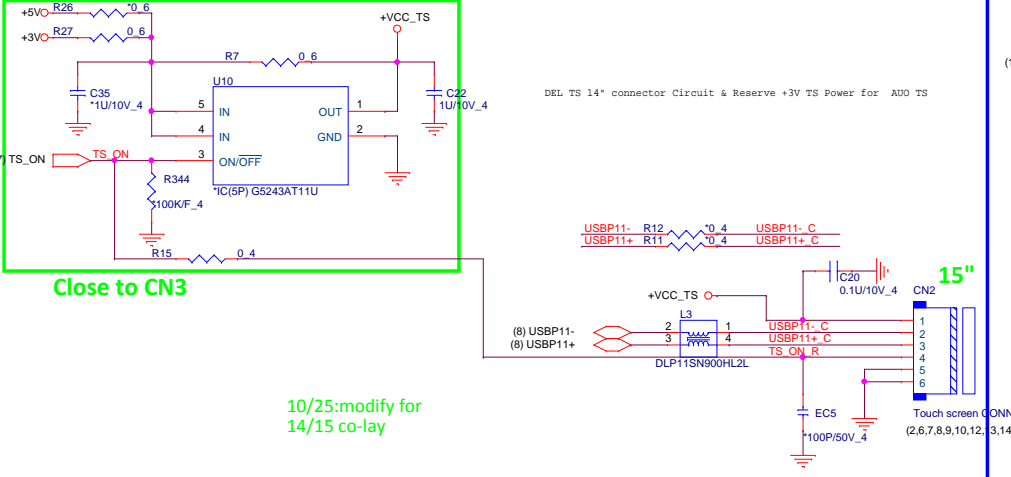


**For EMI Suggestion**  
 CLK\_33M\_DEBUG EC19 \*33P/50V\_4

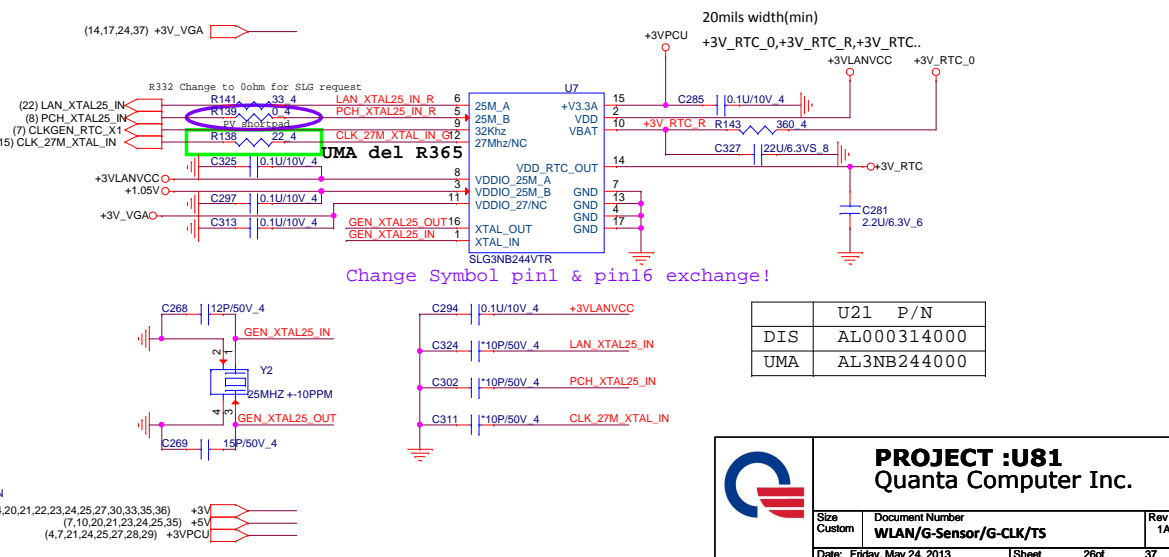
### Accelerometer Sensor



### Touch screen



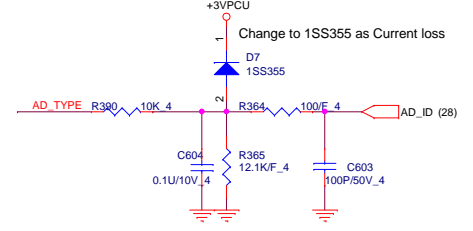
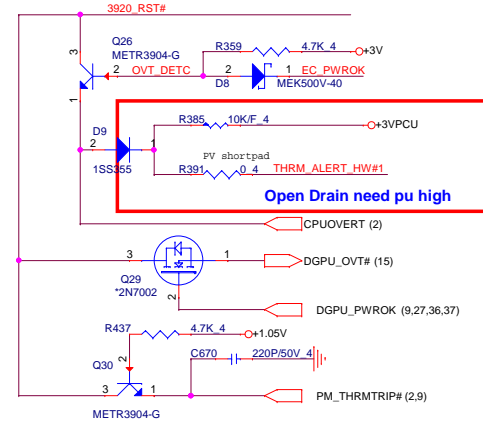
### Green CLK Circuitry



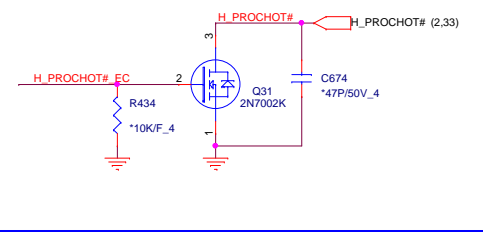
**PROJECT :U81**  
 Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	WLAN/G-Sensor/G-CLK/TS	
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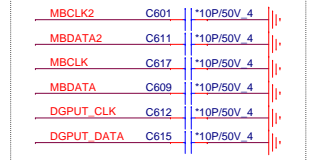
adapter Type check



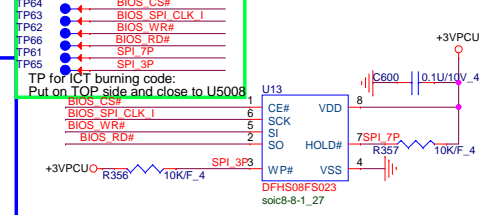
DGPU Thermal protect



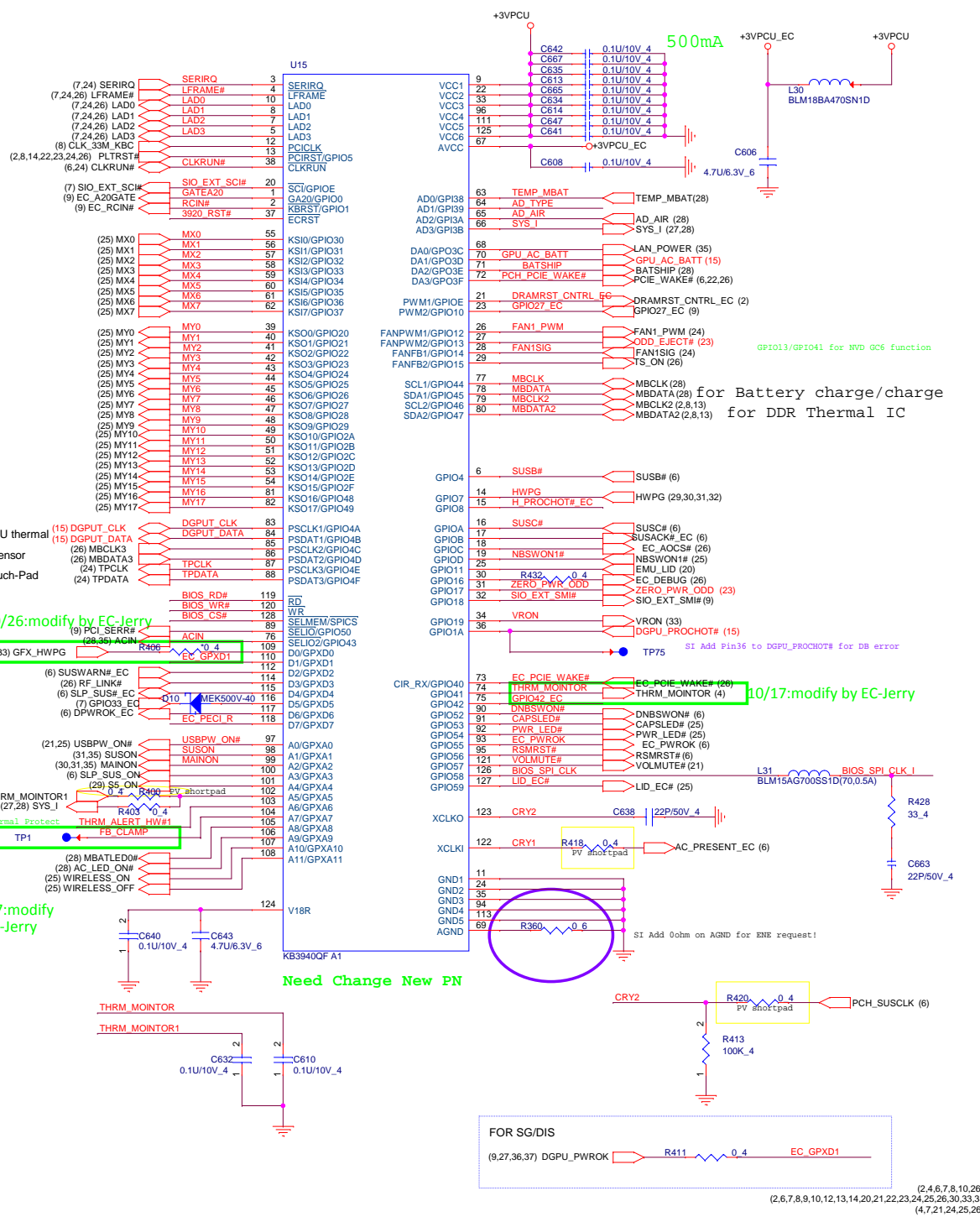
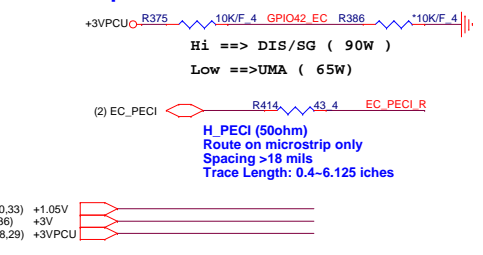
Reserve for ENE Hold time issue



Vender	Size	P/N
EON	1MB	AKE3GZNOQ01 (EON EN25Q80A-100HIP)
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

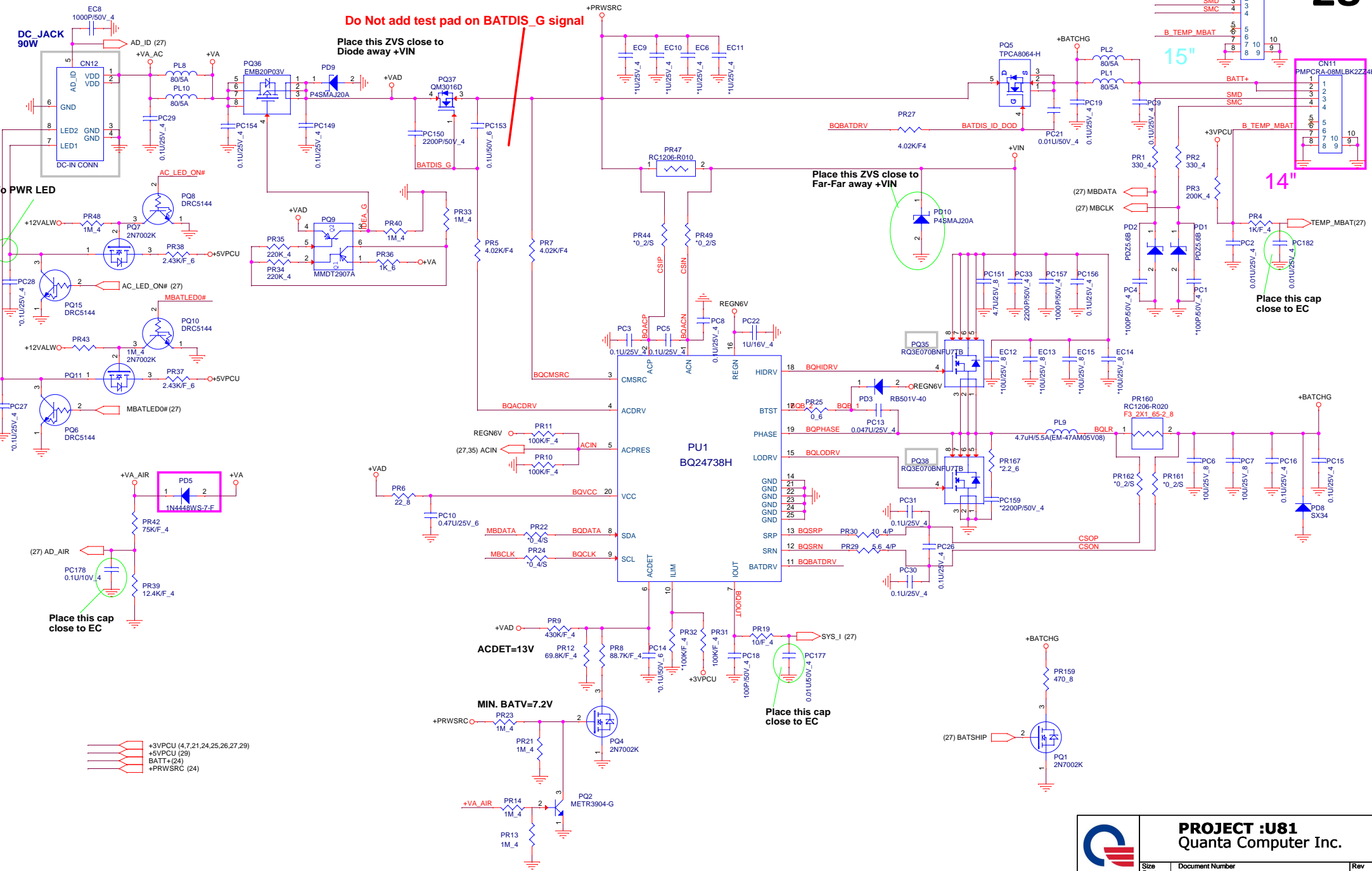


Adapter select for EC



**PROJECT :U81**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3940QF)/ROM	1A
Date: Friday, May 24, 2013	Sheet 27 of 37	



Do Not add test pad on BATDIS\_G signal

Place this ZVS close to Diode away +VIN


Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

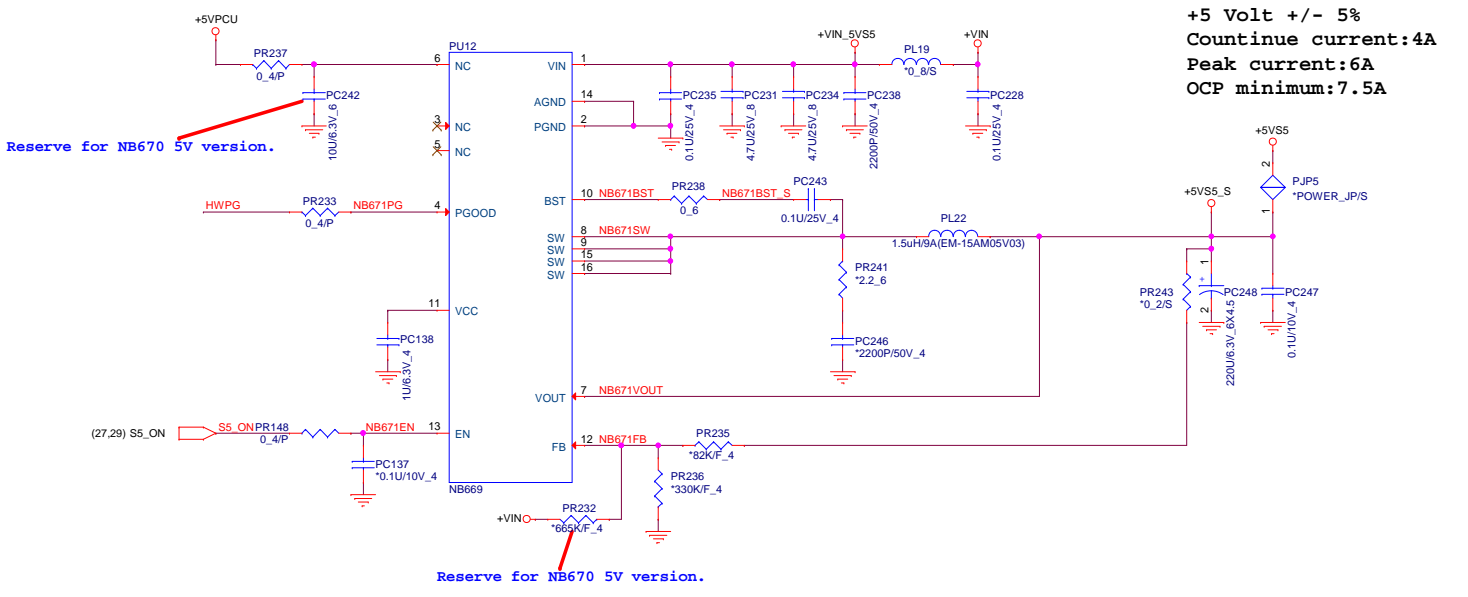
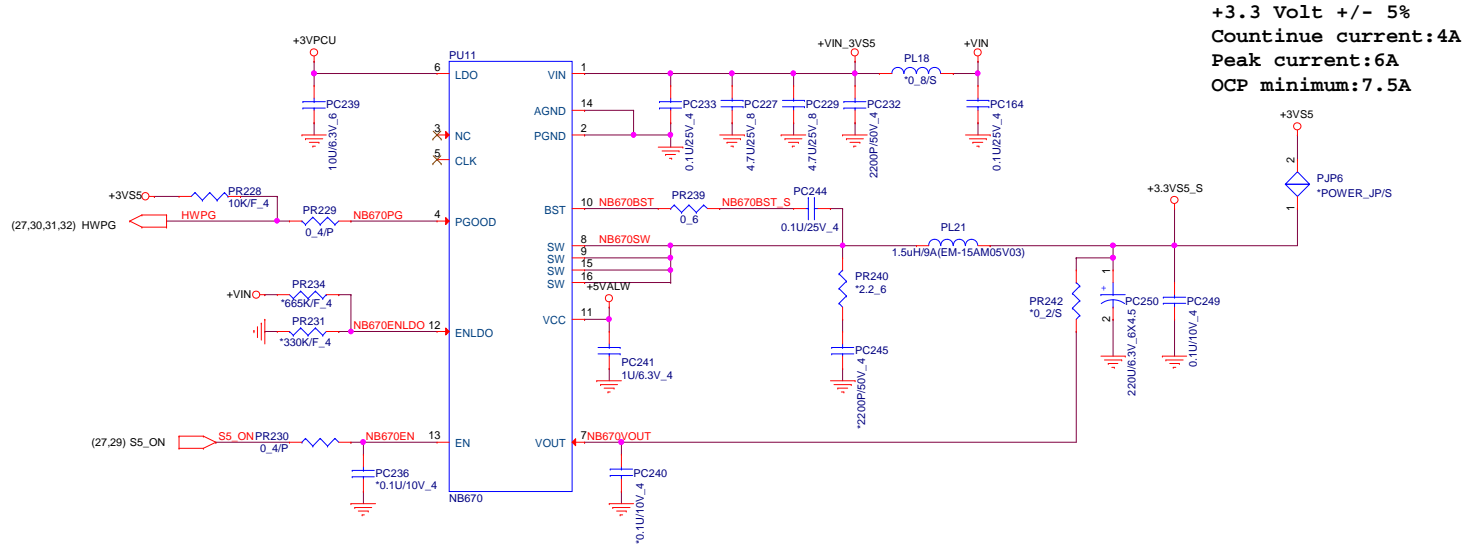
Place this cap close to EC


Place this cap close to EC

- +3VPCU (4,7,21,24,25,26,27,29)
- +5VPCU (29)
- BATT+(24)
- +PRWSRC (24)

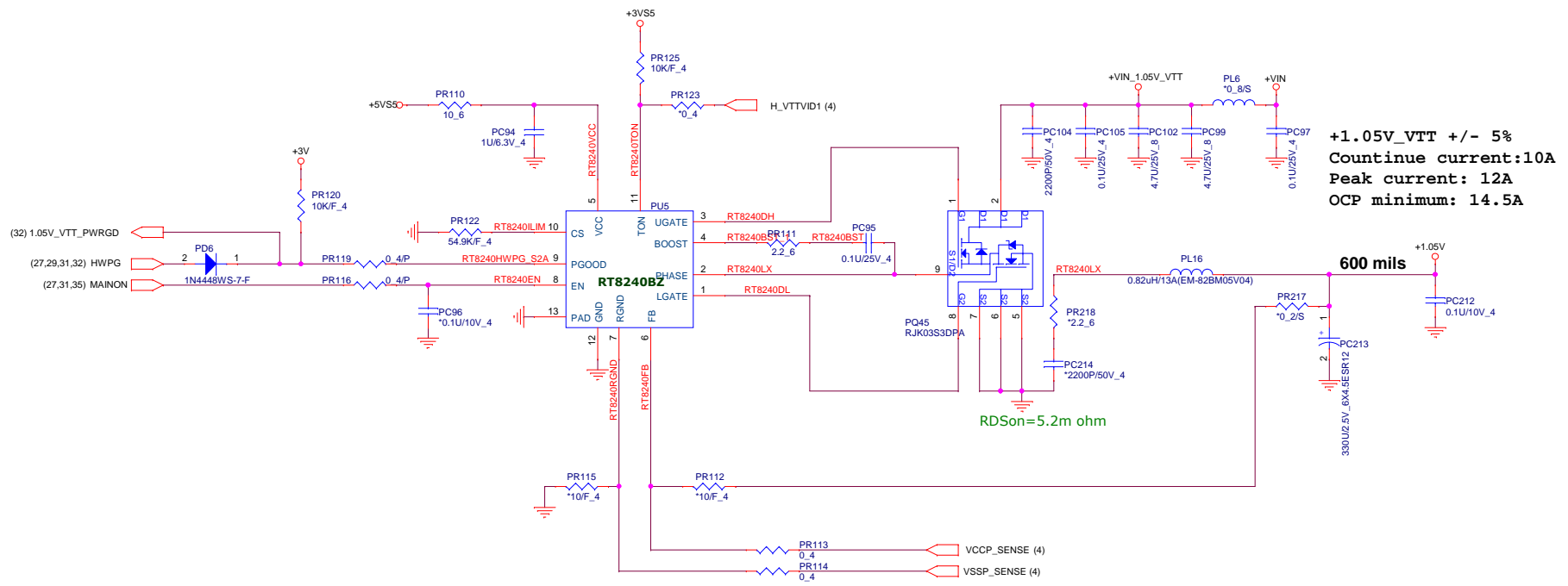
 <b>PROJECT :U81</b> Quanta Computer Inc.		
Size Custom	Date: Friday, May 24, 2013	Sheet 28 of 37

DC/DC +3VS5/+5VS5




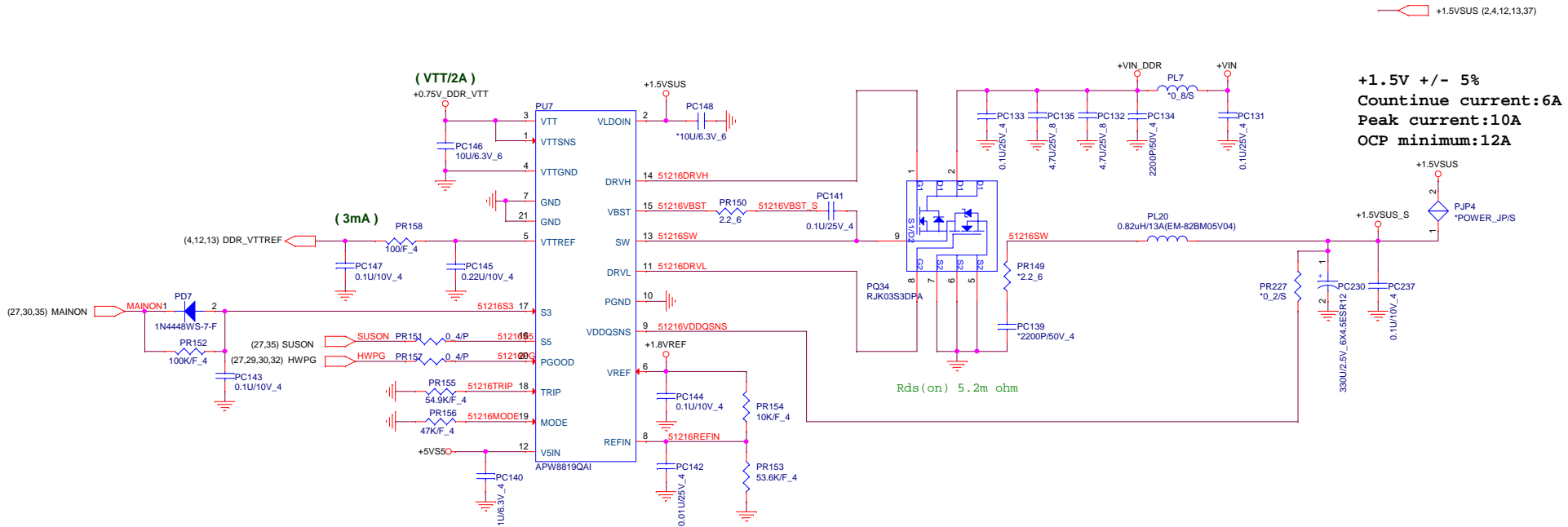
	<b>PROJECT :U81</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number <b>3/5VPCU(NB669/NB670)</b>	
Date: Friday, May 24, 2013	Sheet 29	of 37	



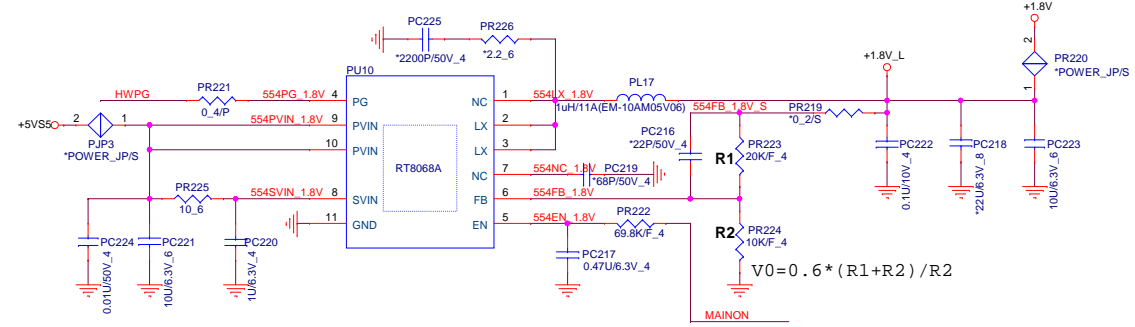


+1.05V (2,4,6,7,8,10,26,27,33)

	<b>PROJECT :U81</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number <b>1.05V(RT8240BZ)</b>	
Date: Friday, May 24, 2013		Sheet 30 of 37	



**1.8V +/- 3%**  
**Continuous current: 2A**  
**Peak current: 3A**  
**OCP minimum: 4A**



+1.5VSUS (2.4,12,13,37)

**+1.5V +/- 5%**  
**Continuous current: 6A**  
**Peak current: 10A**  
**OCP minimum: 1.2A**

+1.5VSUS  
 PJP4  
 \*POWER\_IP/S



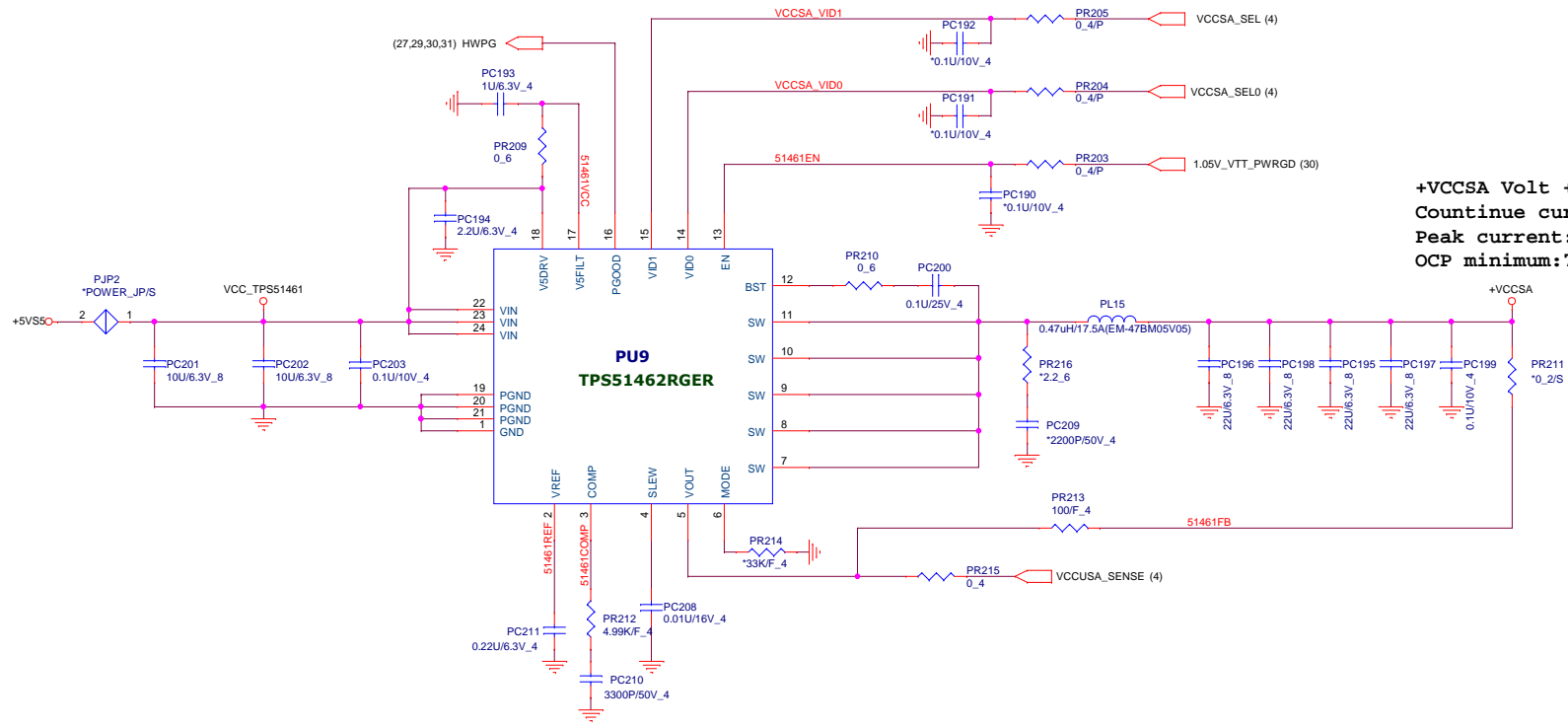
**PROJECT :U81**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>DDR3 (APW8819)</b>	Rev 1A
Date: Friday, May 24, 2013	Sheet 31	of 37

**TPSS1462RGER/AL051462000**

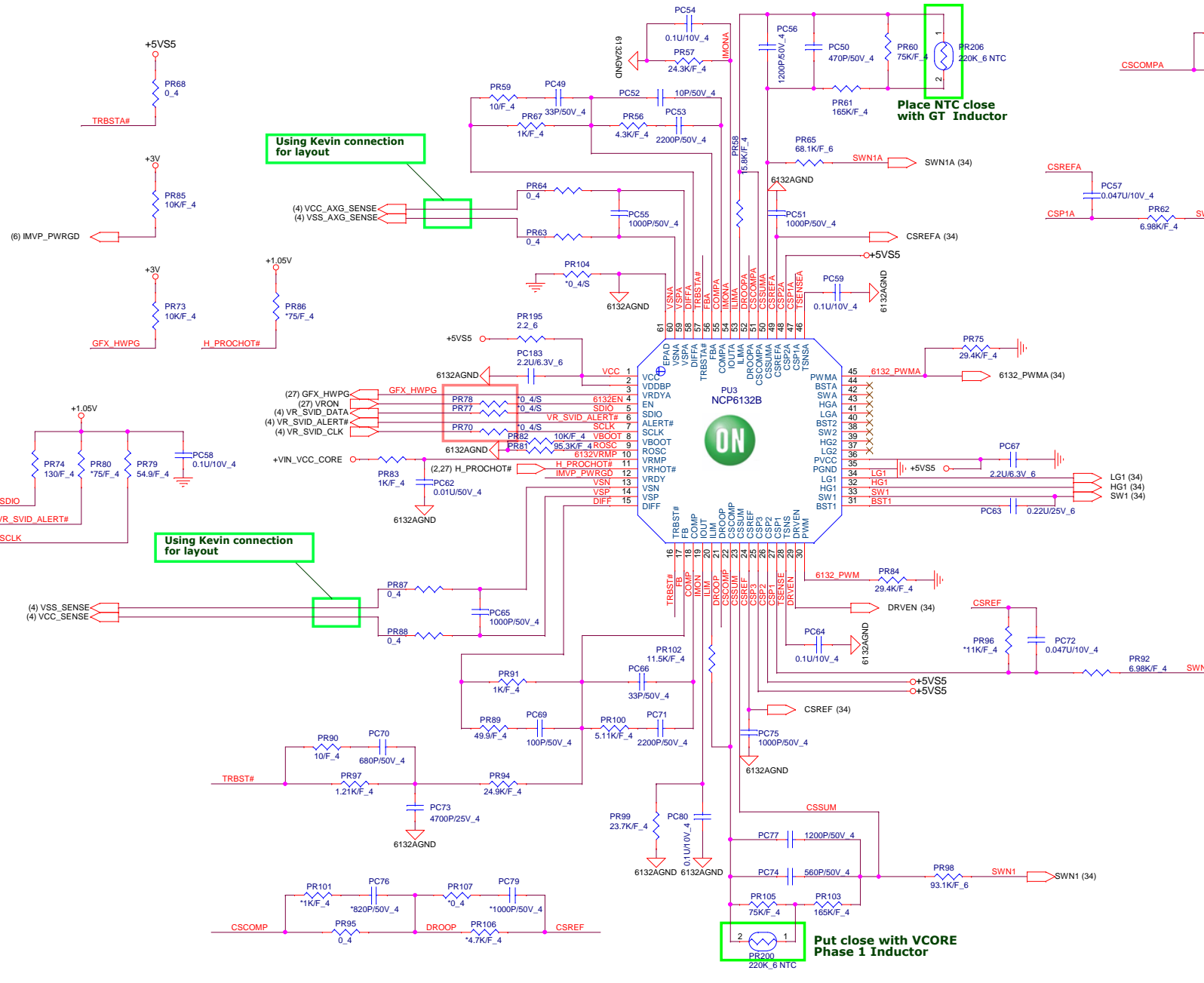
For CPU SV system agent  
voltage slew rate of 0.5 -10 mV/μs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



**+VCCSA Volt +/- 5%**  
**Countinue current:4A**  
**Peak current:6A**  
**OCp minimum:7A**

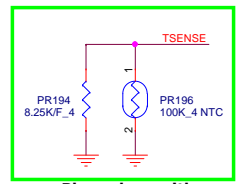
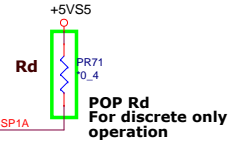
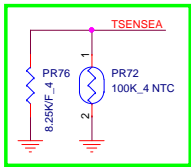
	<b>PROJECT :U81</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>VCCSA(TPSS1462RGER)</b>	Rev 1A
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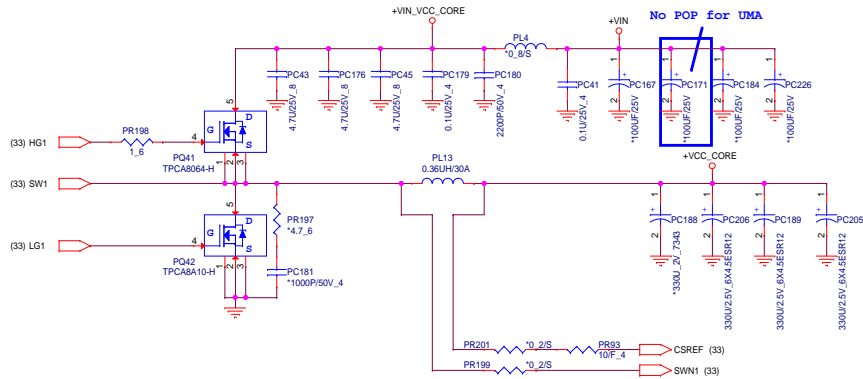
Using Kevin connection for layout

Using Kevin connection for layout

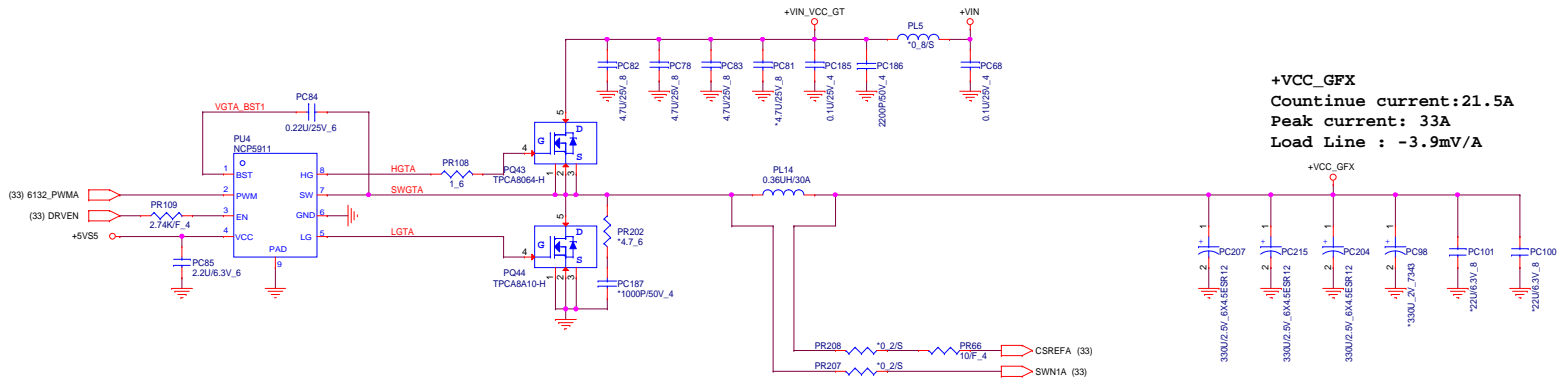
Place NTC close with GT Inductor



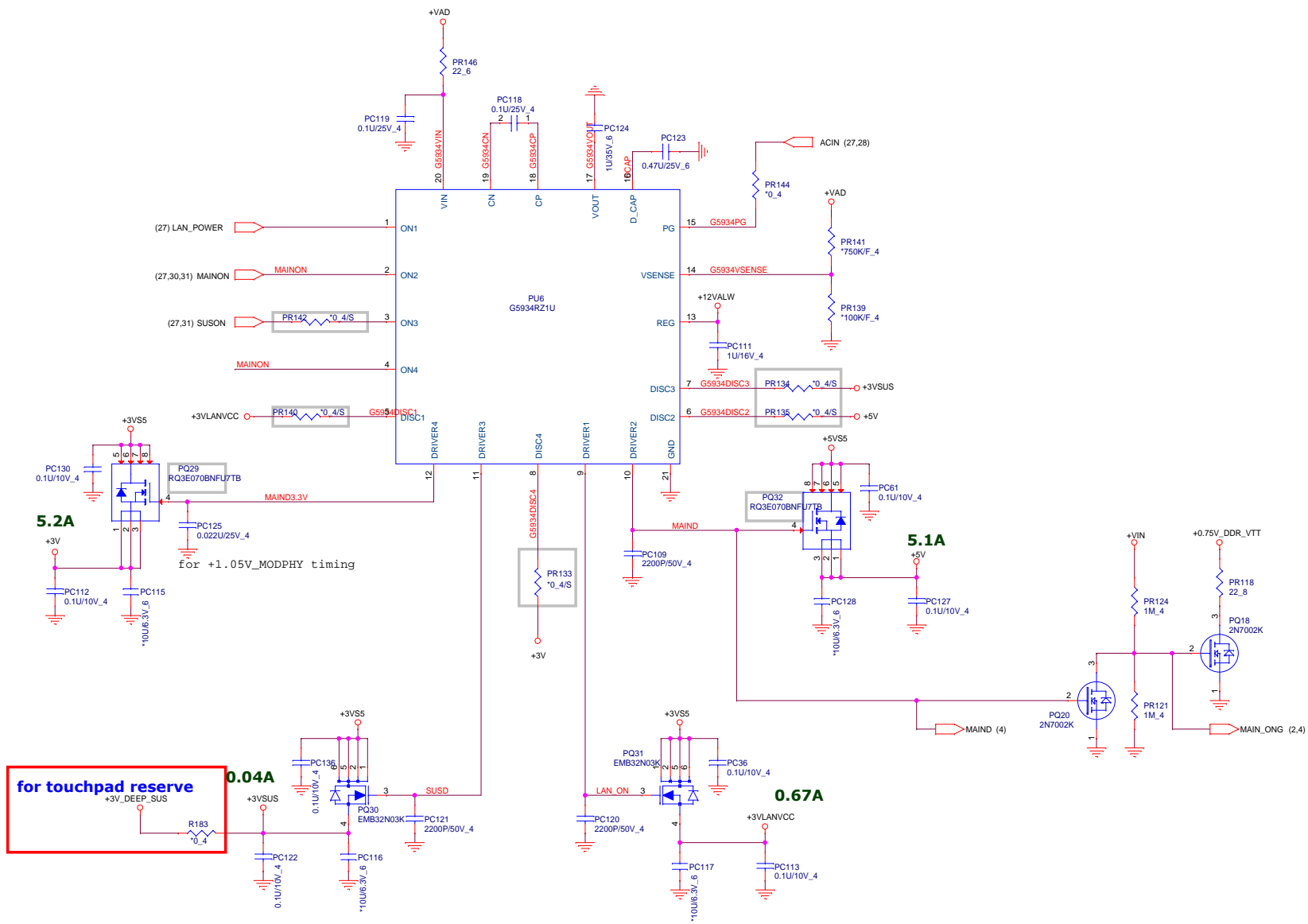
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**+VCC\_CORE (ULV 17W)**  
 Continue current:16A  
 Peak current: 33A  
 Load Line : -2.9mV/A



**+VCC\_GFX**  
 Continue current:21.5A  
 Peak current: 33A  
 Load Line : -3.9mV/A

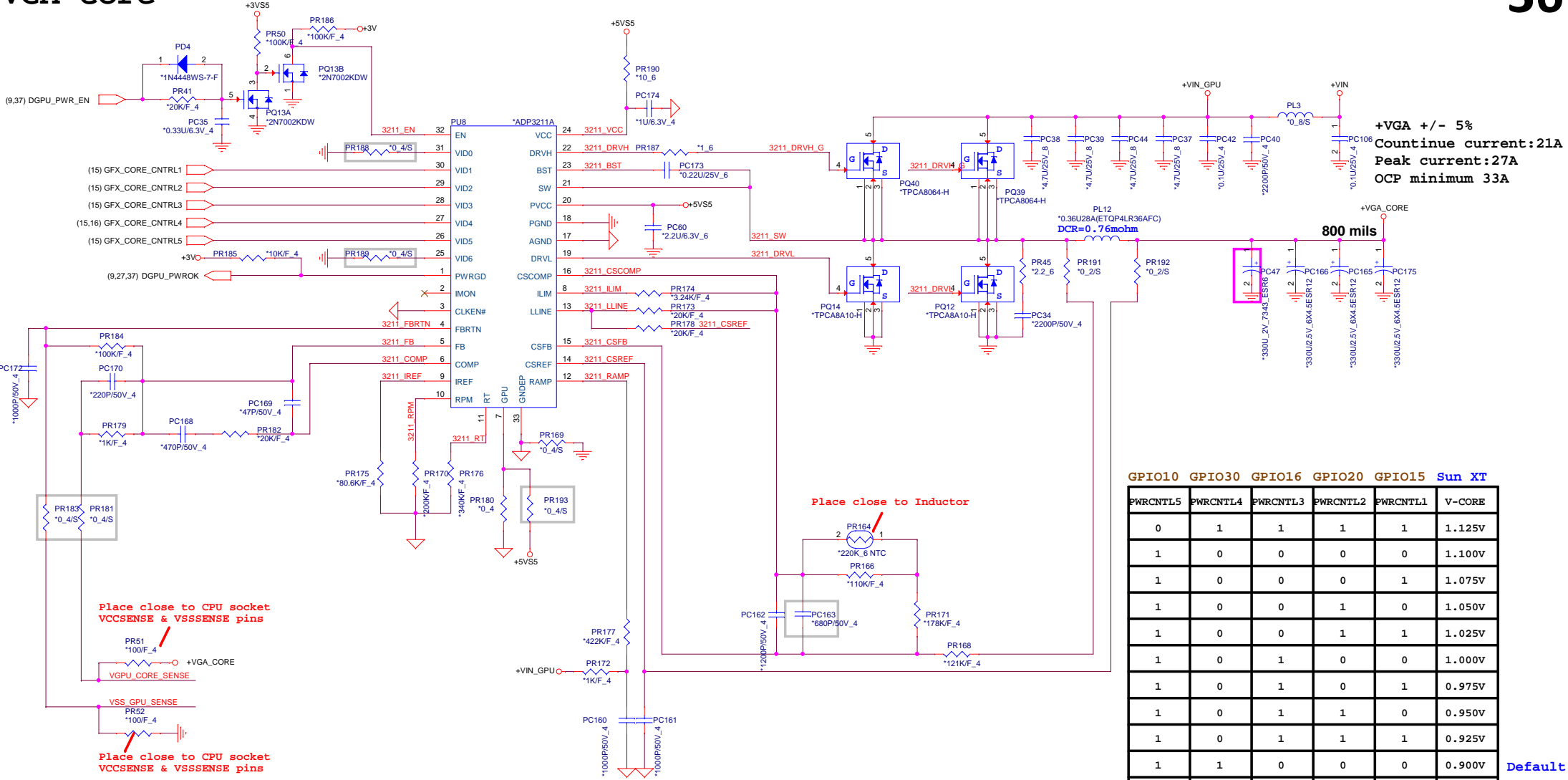


(2,6,7,8,9,10,12,13,14,20,21,22,23,24,25,26,27,30,33,36)	+3V
(7,10,20,21,23,24,25,26)	+5V
(20,24,28,29,30,31,34,36,37)	+VIN
(6,9,10,24,26,29,30,36,37)	+3VS5
(6,21,25,29,30,31,32,33,34,36,37)	+5VS5
(23,28,37)	+12VALW
(22,26)	+3VLANVCC
(12,13,31)	+0.75V_DDR_VTT

**for touchpad reserve**



VGA Core



**+VGA +/- 5%**  
**Countinue current:21A**  
**Peak current:27A**  
**OCP minimum 33A**

GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

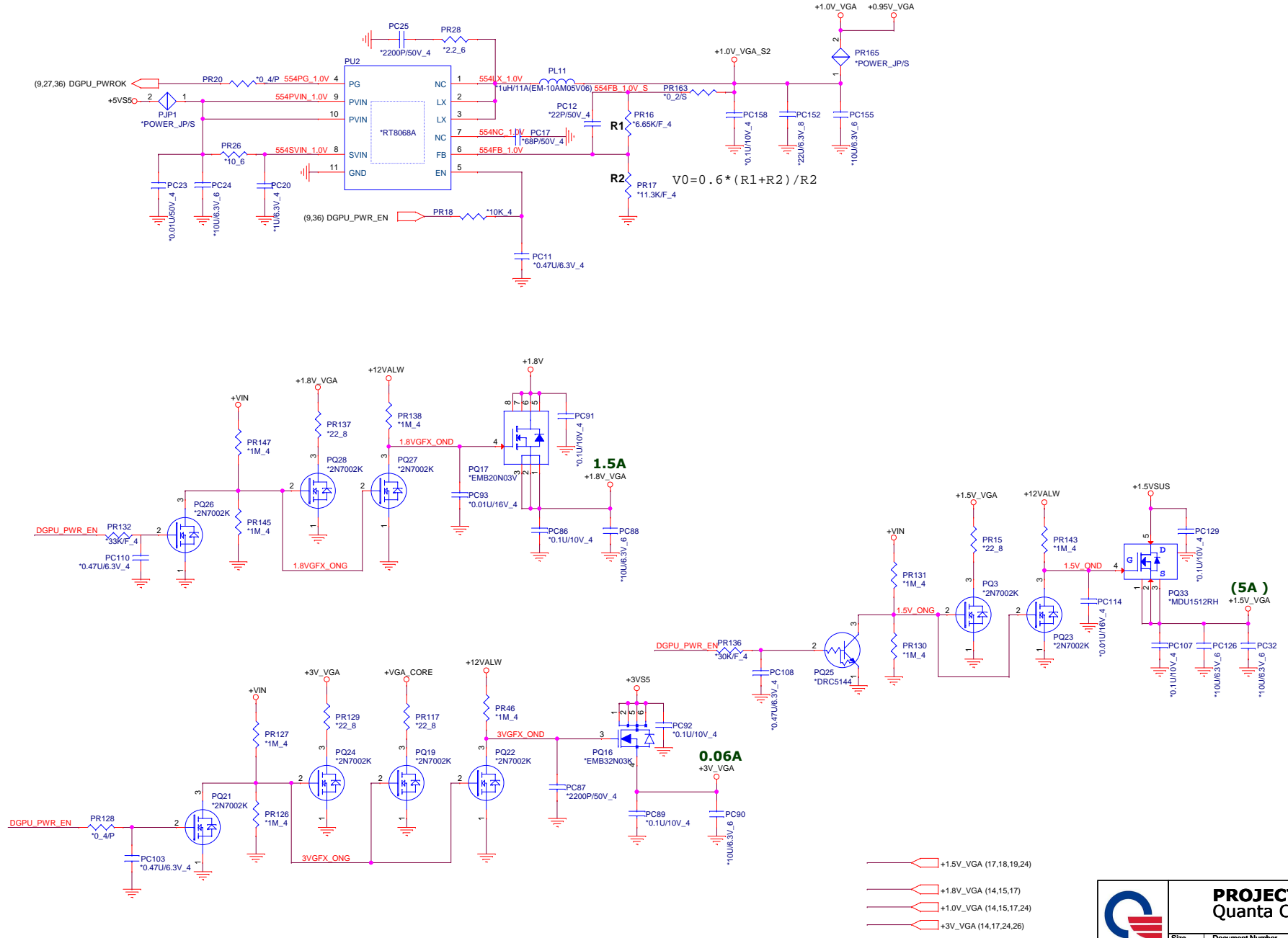
Default

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**Quanta Computer Inc.**


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VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%  
 Countinue current:2A  
 Peak current:3A  
 OCP minimum:4A



$$V0 = 0.6 * (R1 + R2) / R2$$

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