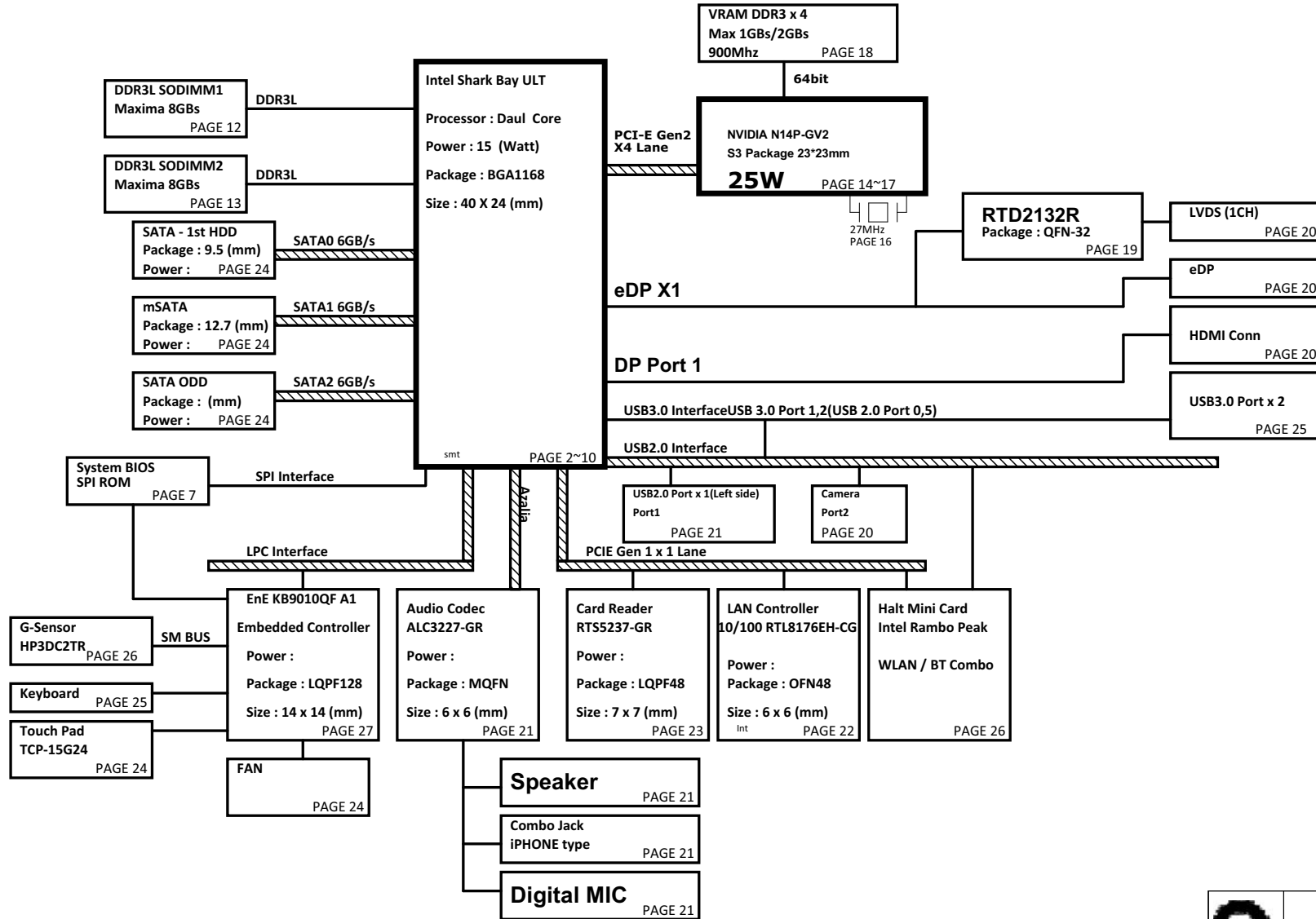
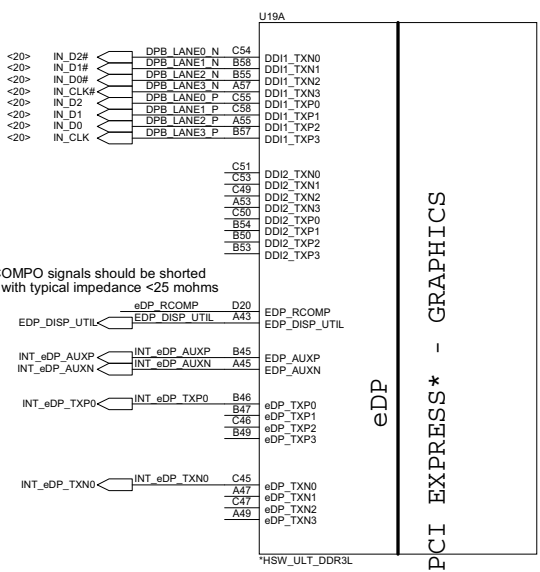


U82 DIS (14"/15.6") Ultra/Slim Intel Shark Bay ULT Platform Block Diagram

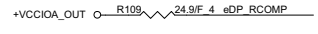
PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT

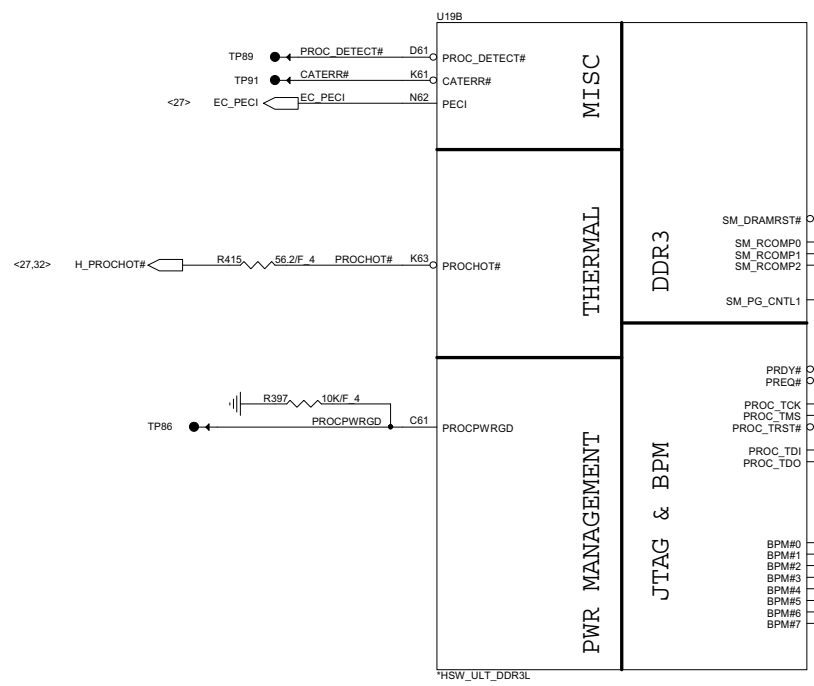




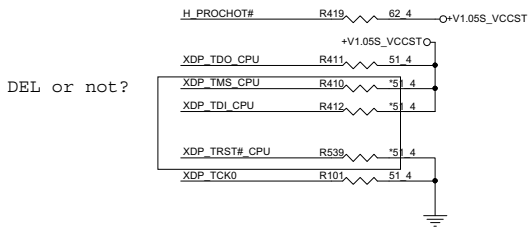
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



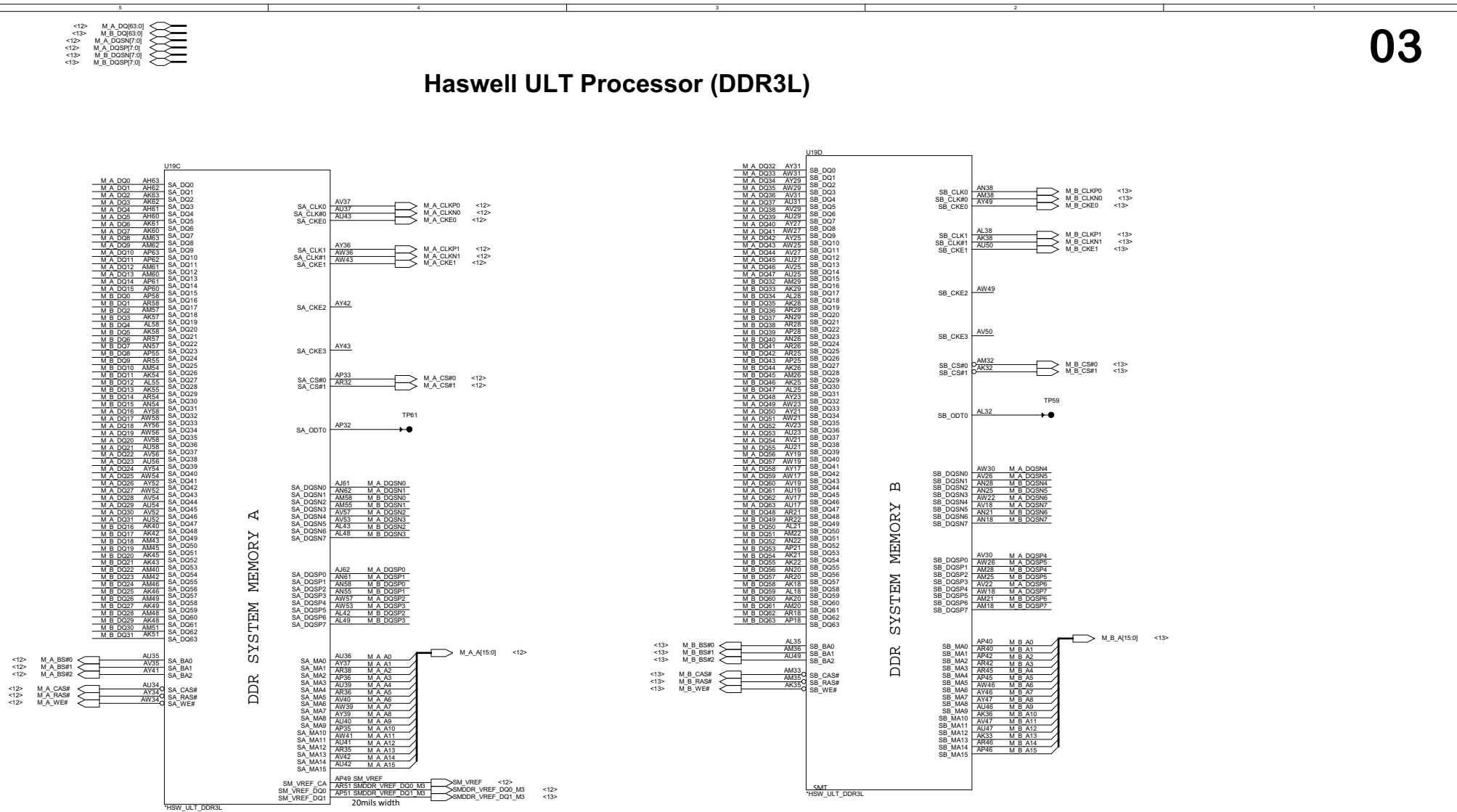
Processor pull-up (CPU)

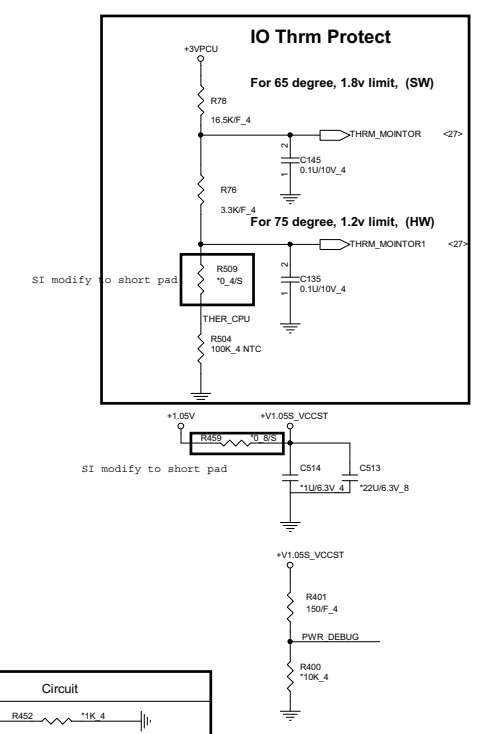
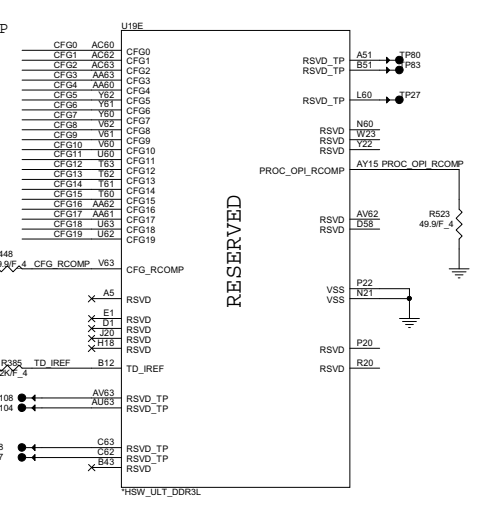
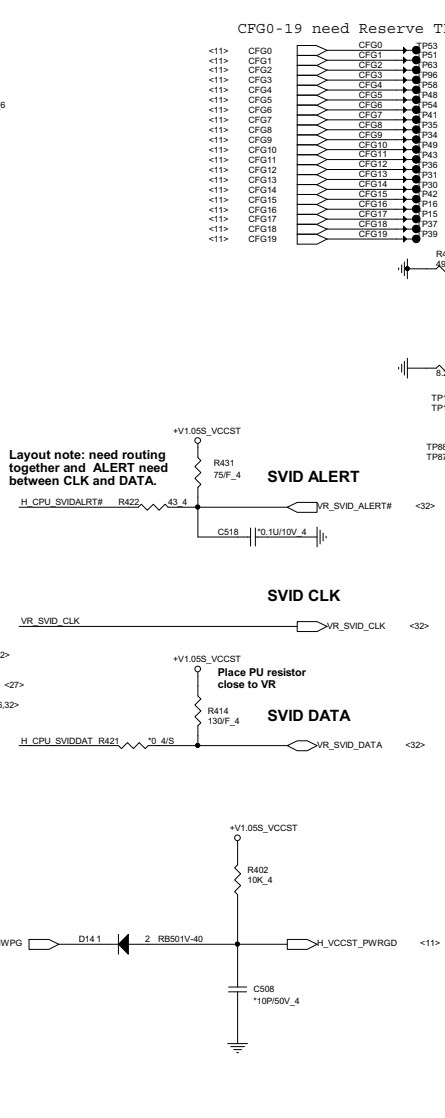
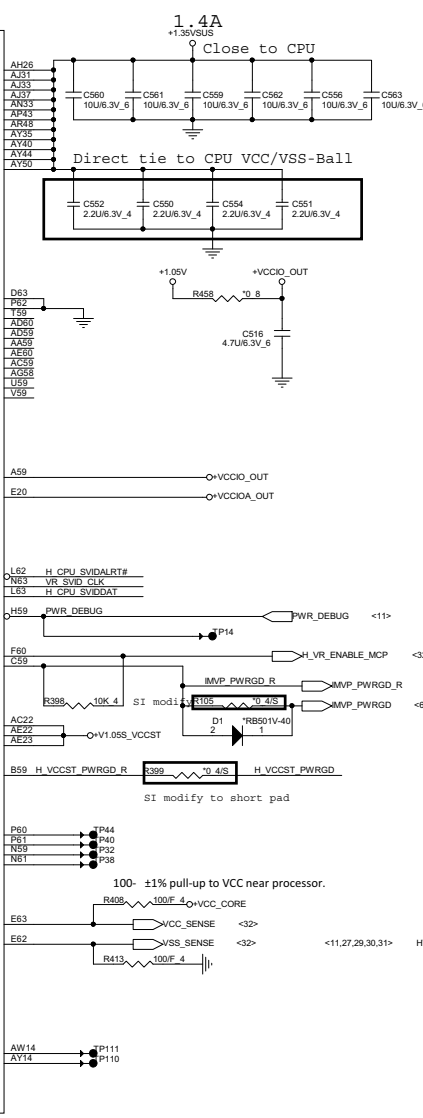
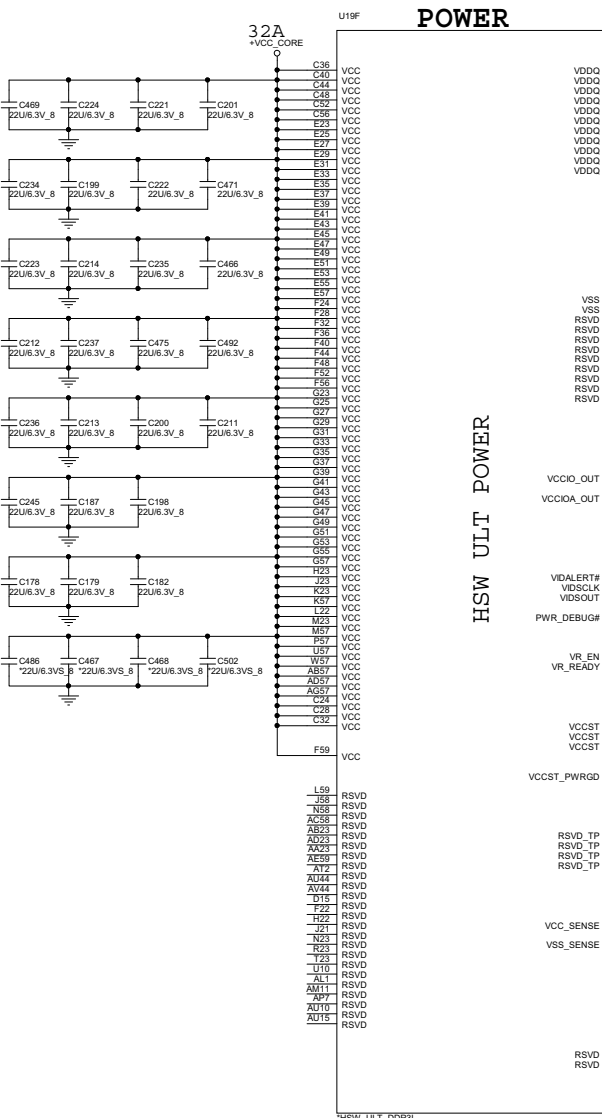


PROJECT :U82
 Quanta Computer Inc.

Size Custom Document Number ULT 1/9(eDP/DDI) Rev 1A
 Date: Friday, April 26, 2013 Sheet 2 of 40

Haswell ULT Processor (DDR3L)

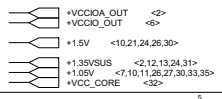




Processor Strapping

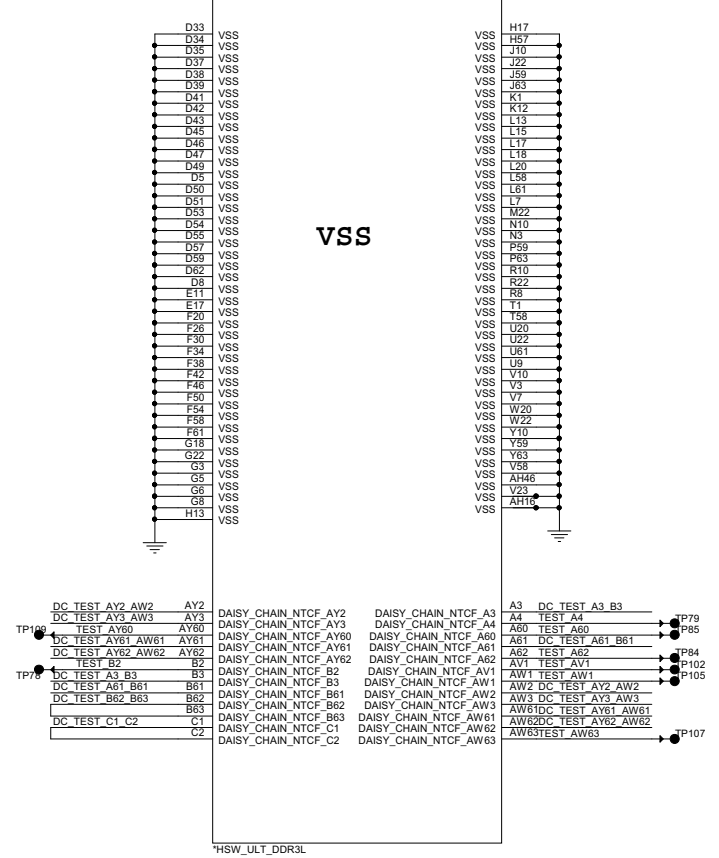
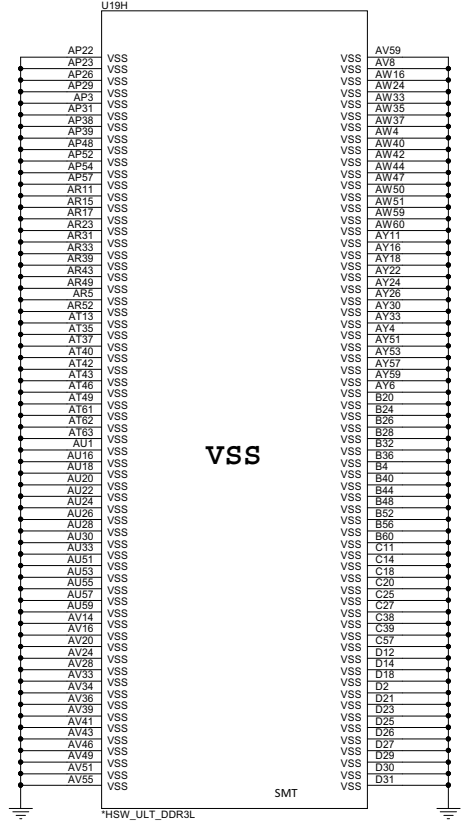
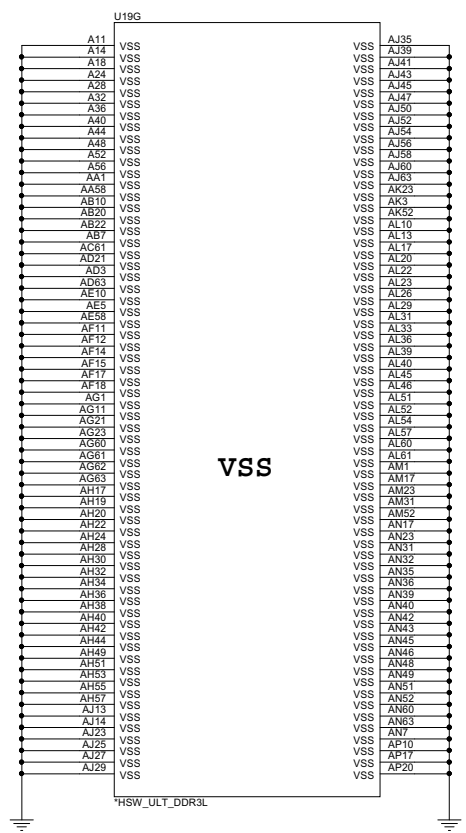
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R452 10K 4
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	CFG4 R143 10K 4



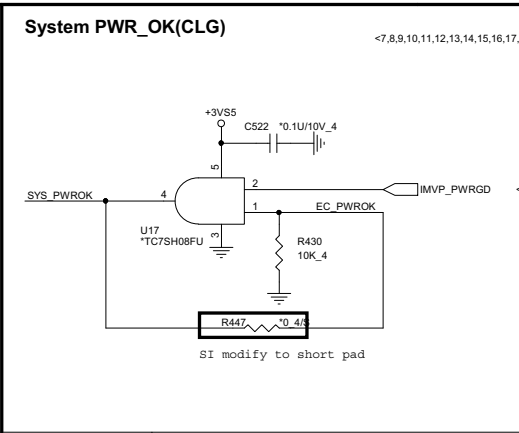
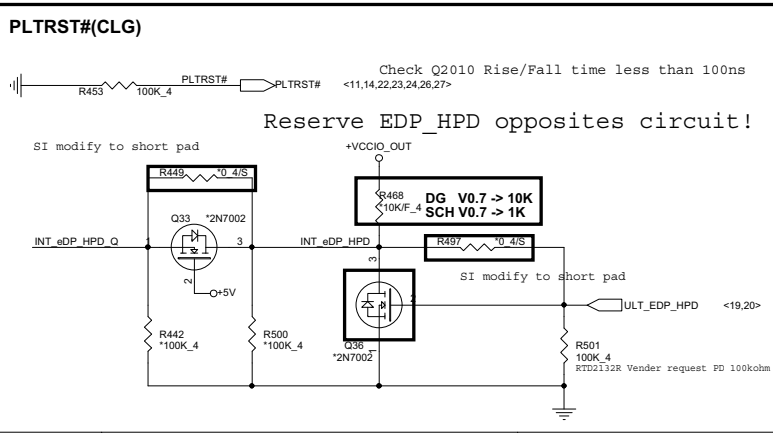
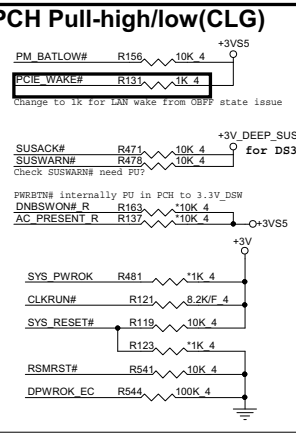
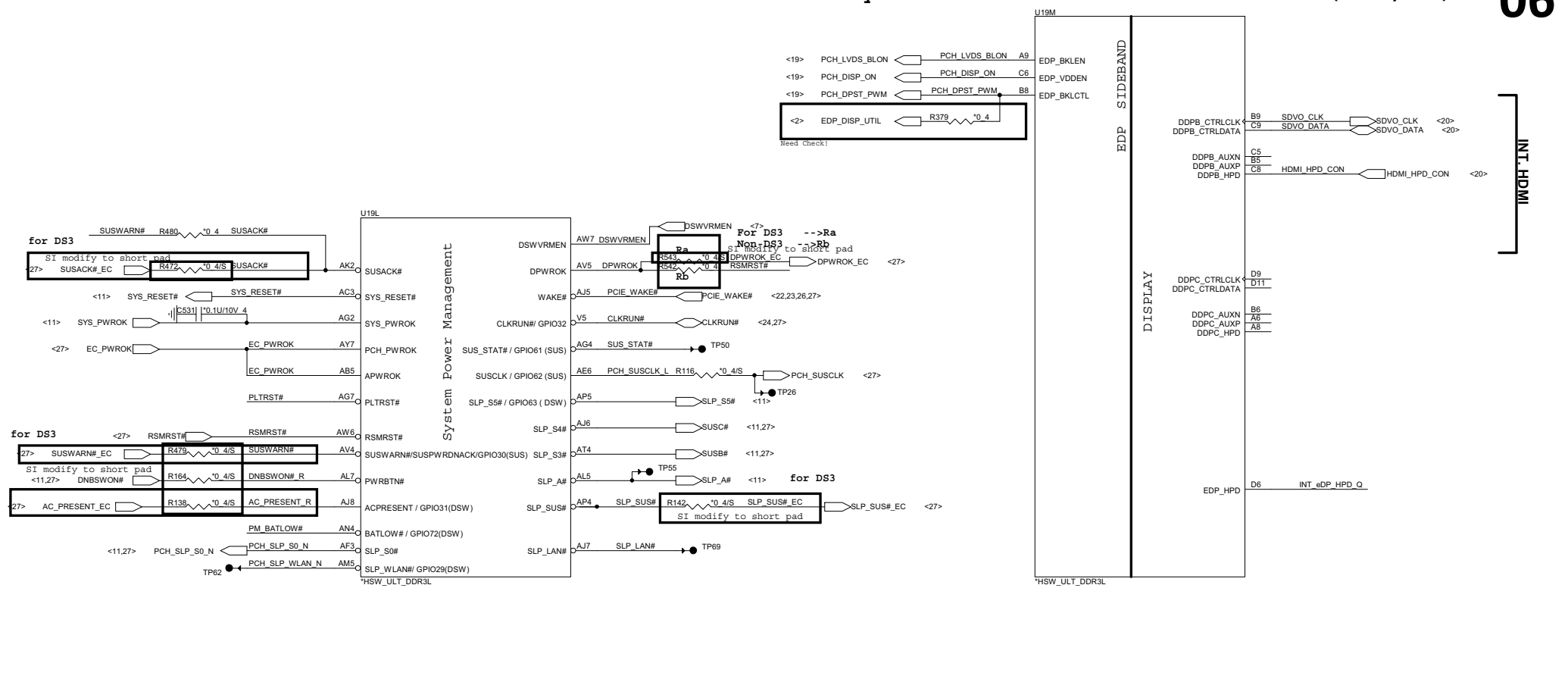
PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number 04 - ULT 3/9 (POWER-1)	Rev 1A
Date: Friday, April 26, 2013	Sheet 4 of	40



PROJECT :U82
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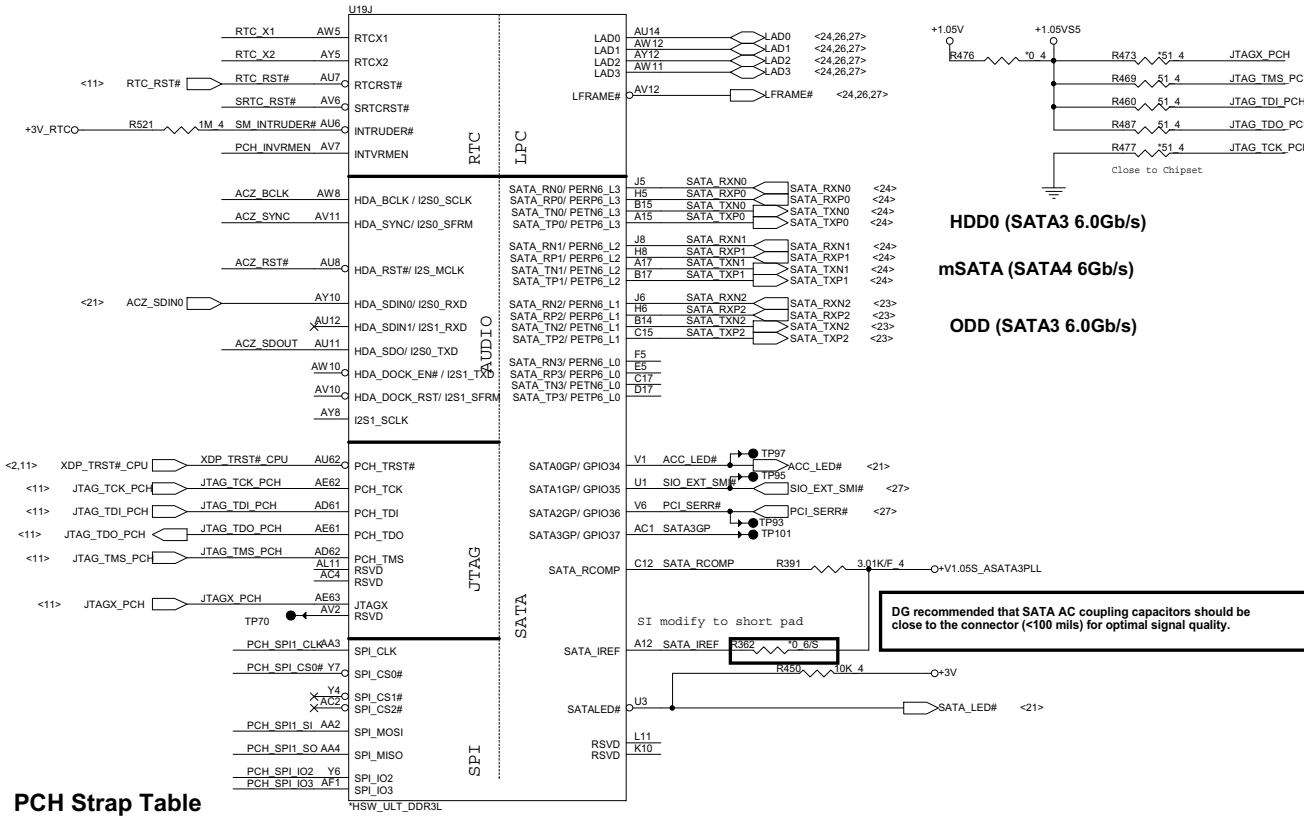
Size Custom Document Number **ULT 4/9 (RSV,GND)** Rev 1A
 Date: Monday, May 06, 2013 Sheet 5 of 40



PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number ULT 5/9(Power Manger)	Rev 1A
Date: Friday, April 26, 2013	Sheet 6 of	40

Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

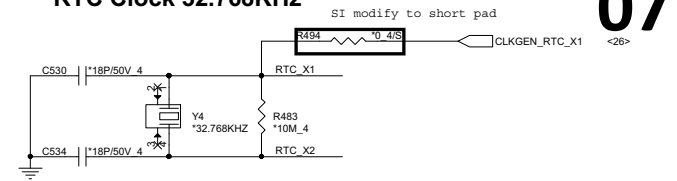


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 --- R455 1K 4 --- SPKR <9>												
SDIO_D0 / GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V0 --- R376 1K 4 --- R375 1K 4 --- GPIO66_ULT <9>												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC0 --- R519 330K 4 --- PCH_INVRMEN												
HDA_SDO / I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	<27> GPIO33_EC --- R182 1K 4 --- ACZ_SDOULT												
GSPI0_MOSI / GPIO86	Boot BIOS Selection	PWROK	<table border="1"> <tr> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>LPC</td> </tr> <tr> <td>0</td> <td>SPI(Default)</td> </tr> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)							
GNT0#	Boot Location															
1	LPC															
0	SPI(Default)															
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	+3V_DEEP_SUS --- R125 1K 4 --- GPIO15_ULT <9>												
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC0 --- R520 330K 4 --- DSWVRMEN <6>												
				<table border="1"> <tr> <td><27></td> <td>PCH_SPI_CS0#_R</td> <td>PCH_SPI_CS0#_R</td> </tr> <tr> <td><27></td> <td>PCH_SPI_CLK_R</td> <td>PCH_SPI_CLK_R</td> </tr> <tr> <td><27></td> <td>PCH_SPI_SI_R</td> <td>PCH_SPI_SI_R</td> </tr> <tr> <td><27></td> <td>PCH_SPI_SO_R</td> <td>PCH_SPI_SO_R</td> </tr> </table>	<27>	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R	<27>	PCH_SPI_CLK_R	PCH_SPI_CLK_R	<27>	PCH_SPI_SI_R	PCH_SPI_SI_R	<27>	PCH_SPI_SO_R	PCH_SPI_SO_R
<27>	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R														
<27>	PCH_SPI_CLK_R	PCH_SPI_CLK_R														
<27>	PCH_SPI_SI_R	PCH_SPI_SI_R														
<27>	PCH_SPI_SO_R	PCH_SPI_SO_R														

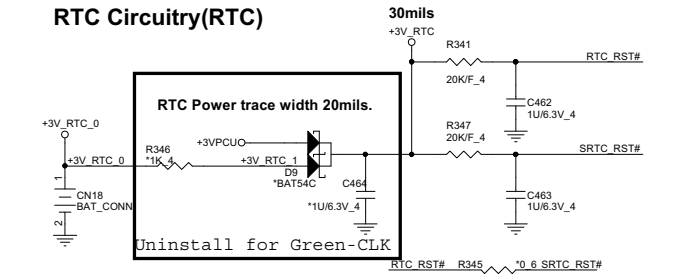
RTC Clock 32.768KHz

07

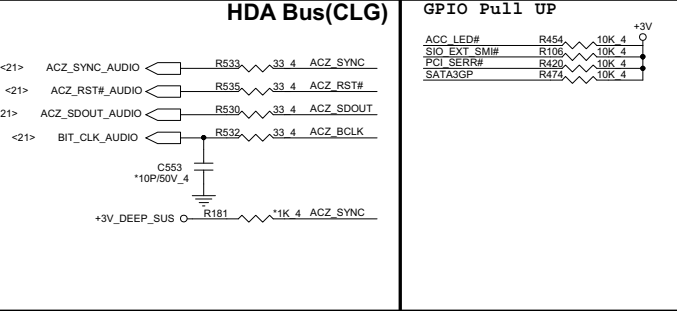


no stuff if use green clock

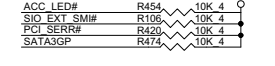
RTC Circuitry(RTC)



HDA Bus(CLG)



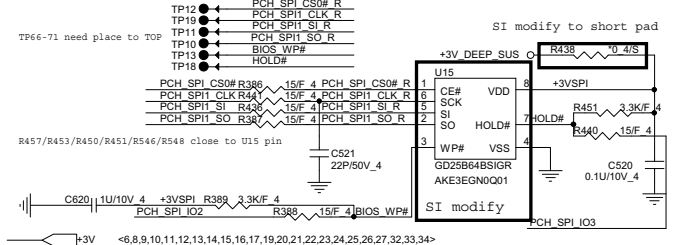
GPIO Pull UP



DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

Vender	Size	P/N
MXIC	8MB	AKE3EZ00Z00 (MX25L6473EM2I-10G)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFH08FS023

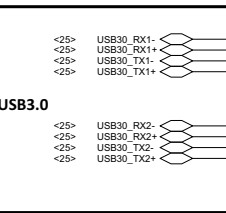
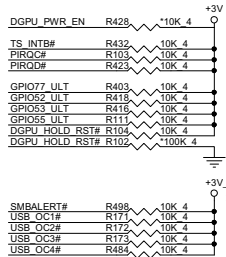
PCH SPI ROM(CLG)



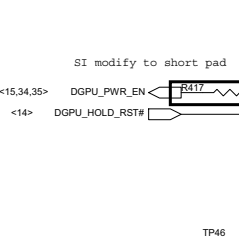
PROJECT :U82
Quanta Computer Inc.

Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

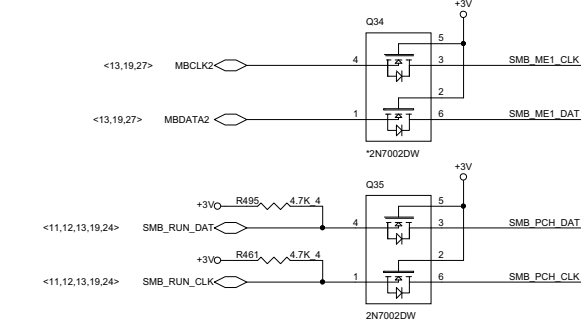
PCI/USB0# Pull-up(CLG)



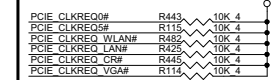
20111130 Modify USB3.0 for HM70



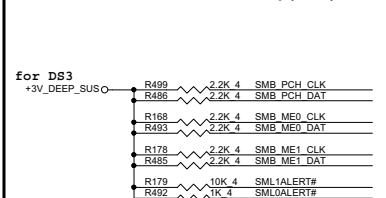
SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



Cardreader

WLAN

LAN

USB2.0(MB-1) (USBP0)

USB2.0/USB3.0 COMBO 1st

USB2.0 Small board (USBP1)

USB2.0/USB3.0 COMBO 2nd

USB2.0 Small board (USBP2)

Camera (USBP2)

USB2.0(MB-2) (USBP5)

WLAN

Touch Screen

Cardreader

WLAN

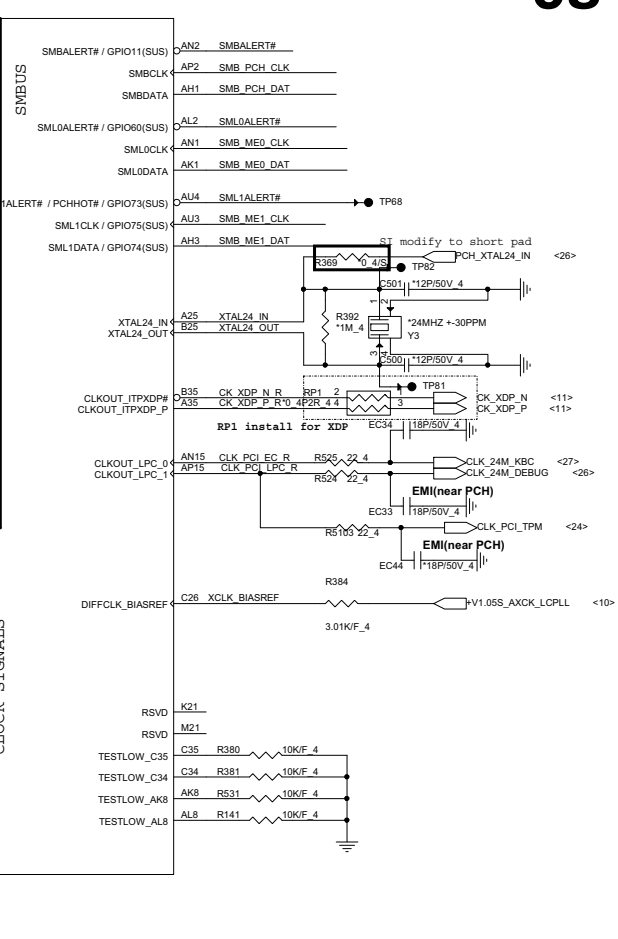
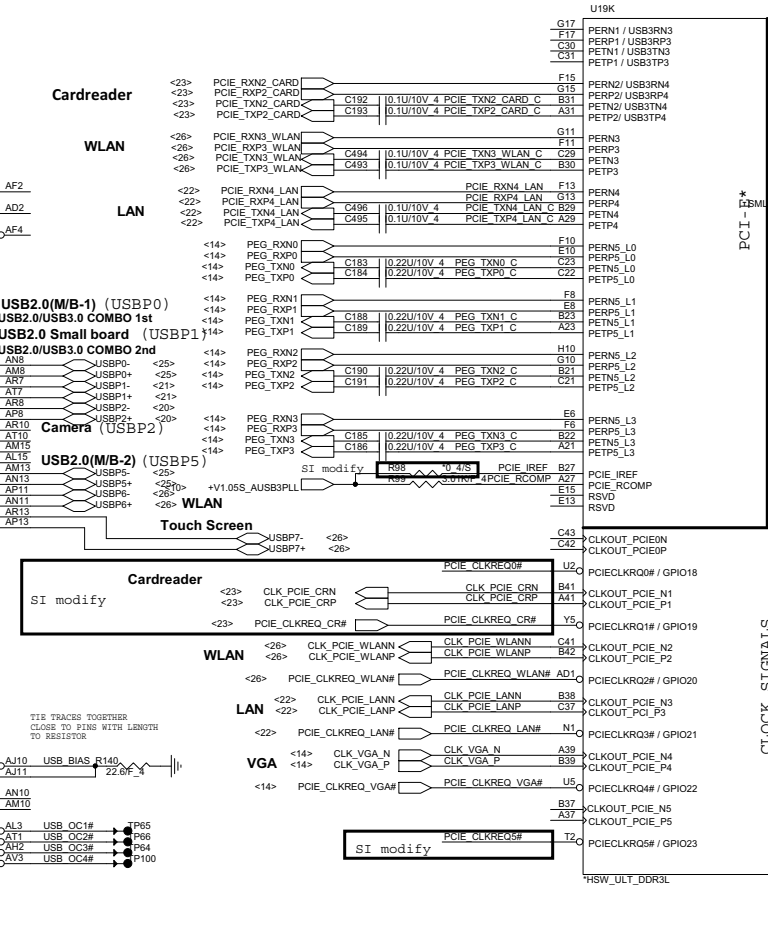
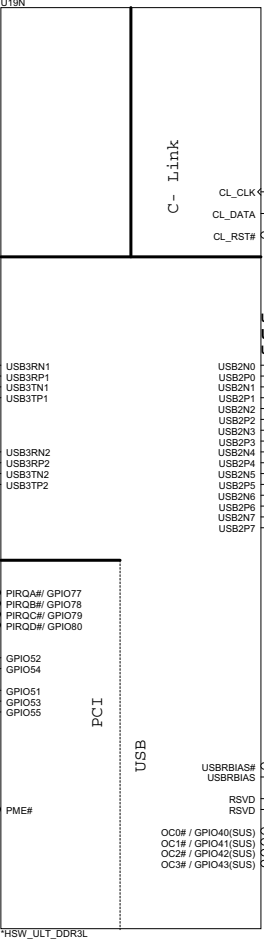
LAN

VGA

SWBUS

PCI - * GLB

CLOCK SIGNALS

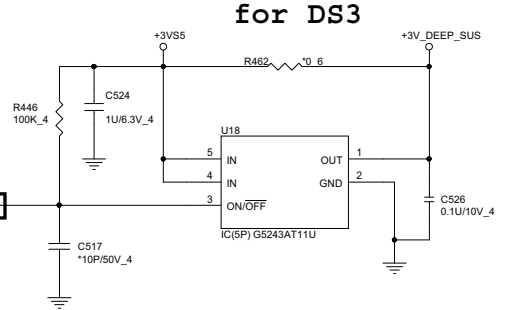
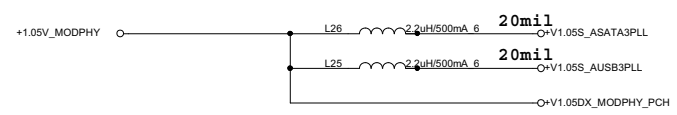
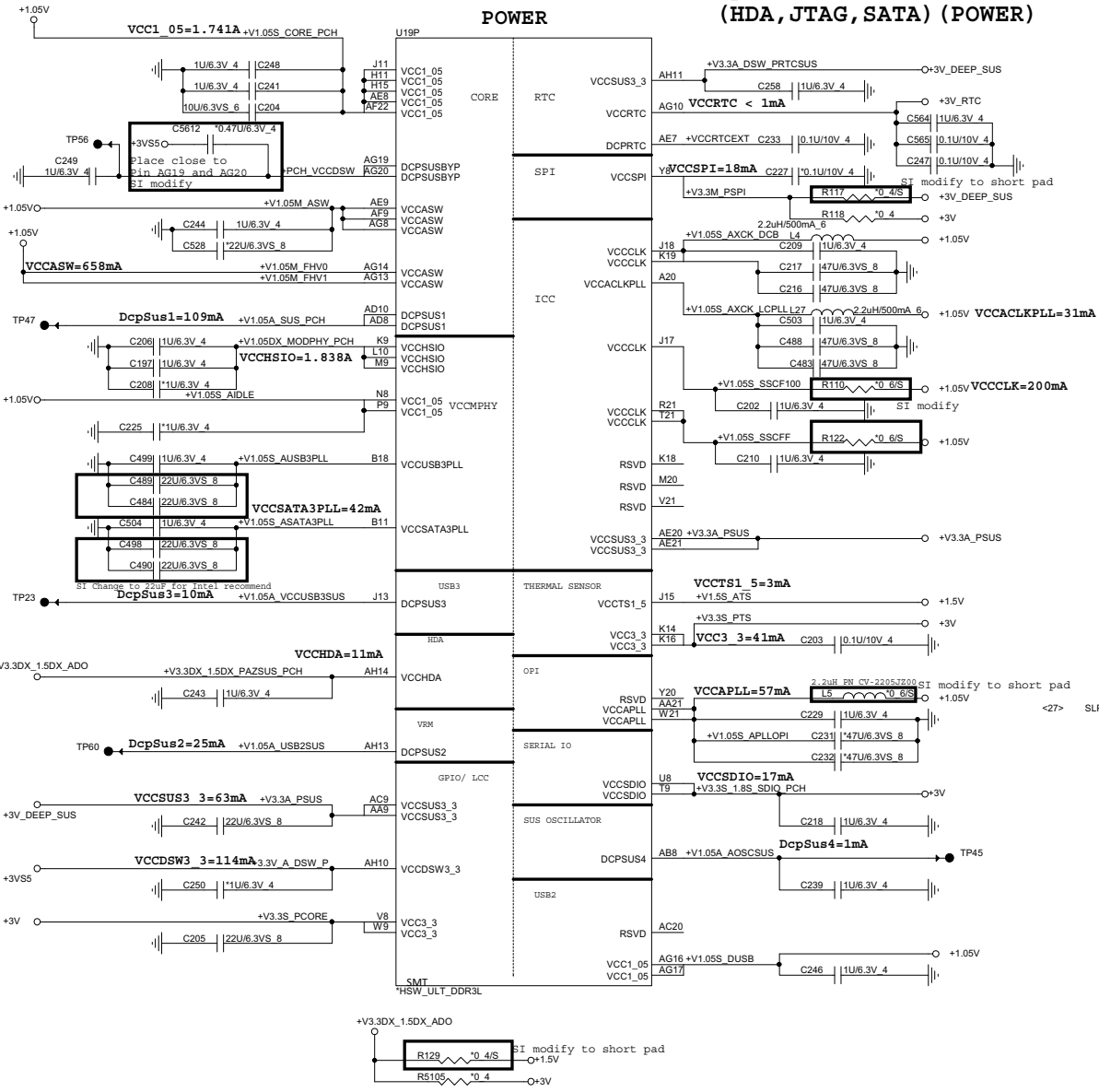


PROJECT :U82
Quanta Computer Inc.

Size Custom Document Number **ULT 7/9 (PCIE/USB/CLK)** Rev 1A
Date: Friday, April 26, 2013 Sheet 8 of 40

<6,7,9,10,11,12,13,14,15,16,17,19,20,21,22,23,24,25,26,27,32,33,34>
<6,7,9,10,11> +3V +3V_DEEP_SUS

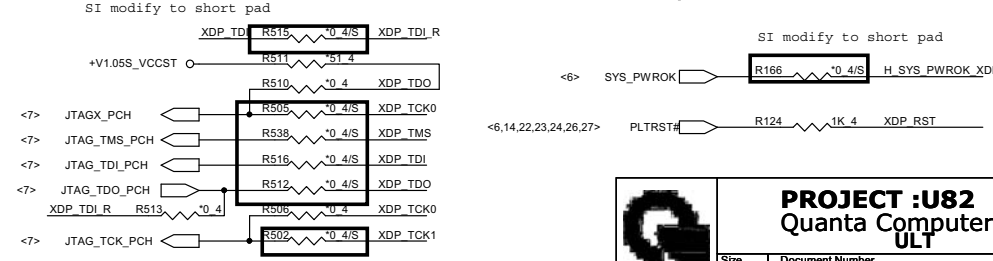
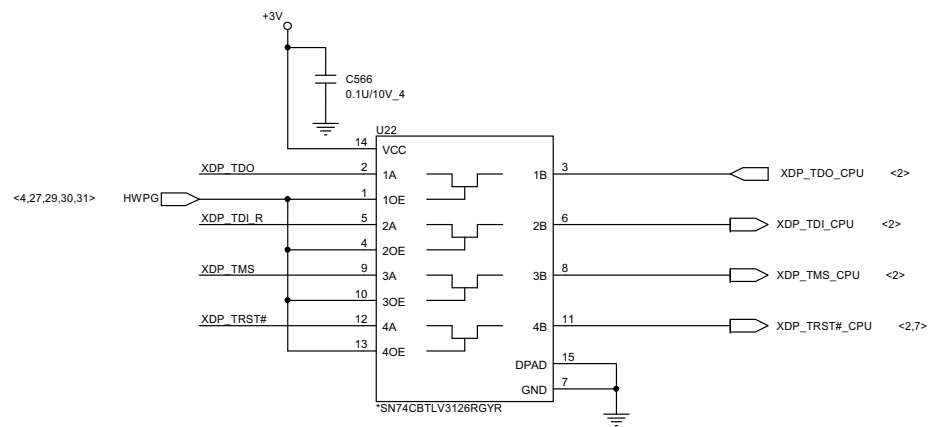
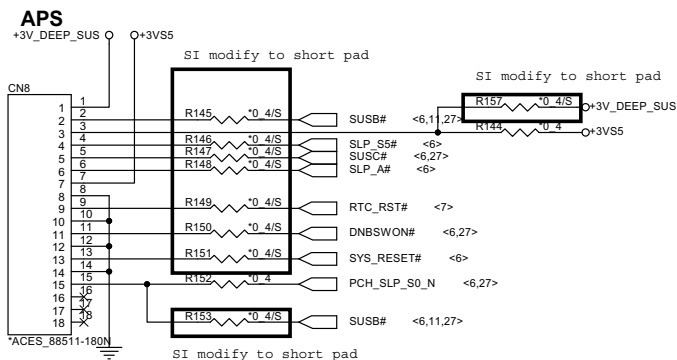
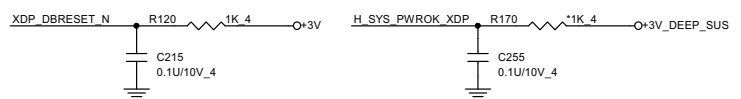
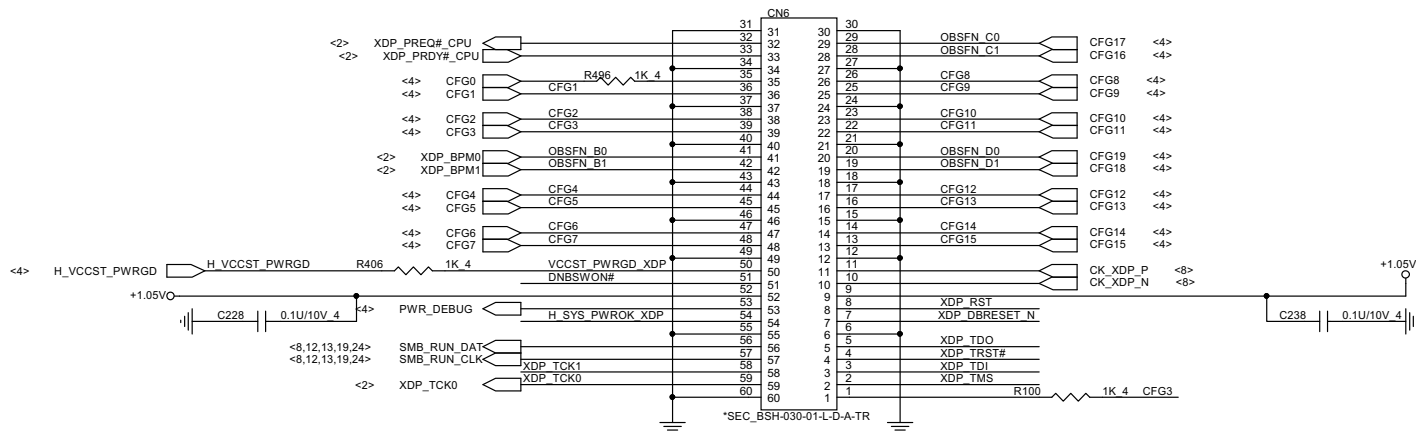
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA) (POWER)



<6,7,8,9,11,12,13,14,15,16,17,19,20,21,22,23,24,25,26,27,32,33,34>	+3V	<8>	+1.05S_AUSB3PLL
<6,20,21,23,24,25,26,33>	+5V	<7>	+1.05S_ASATA3PLL
<4,7,11,26,27,30,33,35>	+1.05V	<8>	+1.05S_AXCK_LCPPLL
<6,9,11,24,26,29,30,33,35>	+3V5S	<7,26>	+3V_RTC
<13,21,24,25,29,31,32,33,34,36>	+5V5S	<2,4,12,13,24,31>	+1.35VSUS

PROJECT :U82
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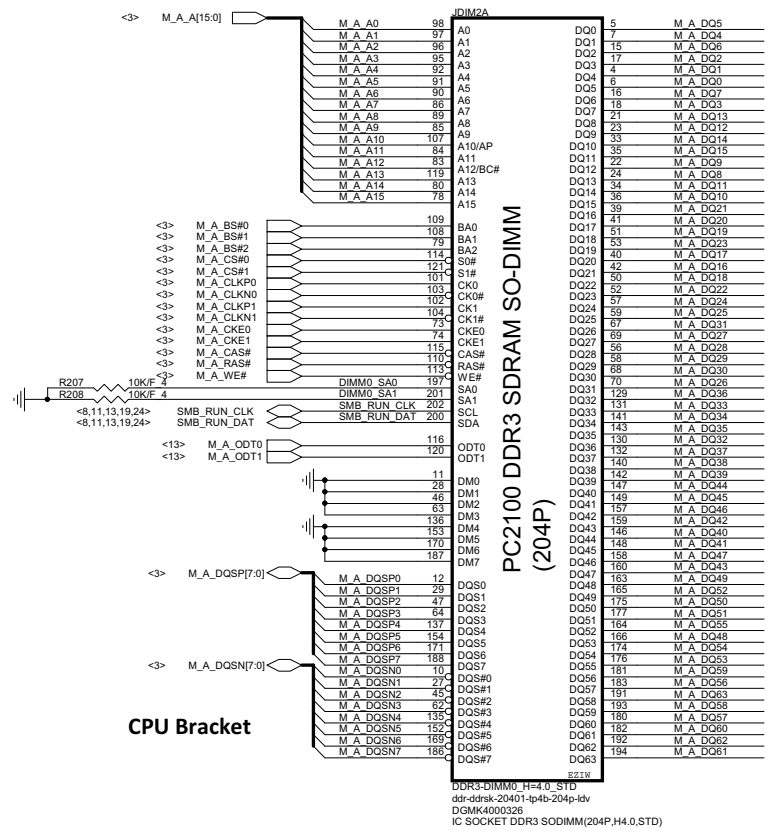
Size Custom	Document Number ULT 9/9(Power-2)	Rev 1A
Date: Monday, May 06, 2013	Sheet 10 of 40	



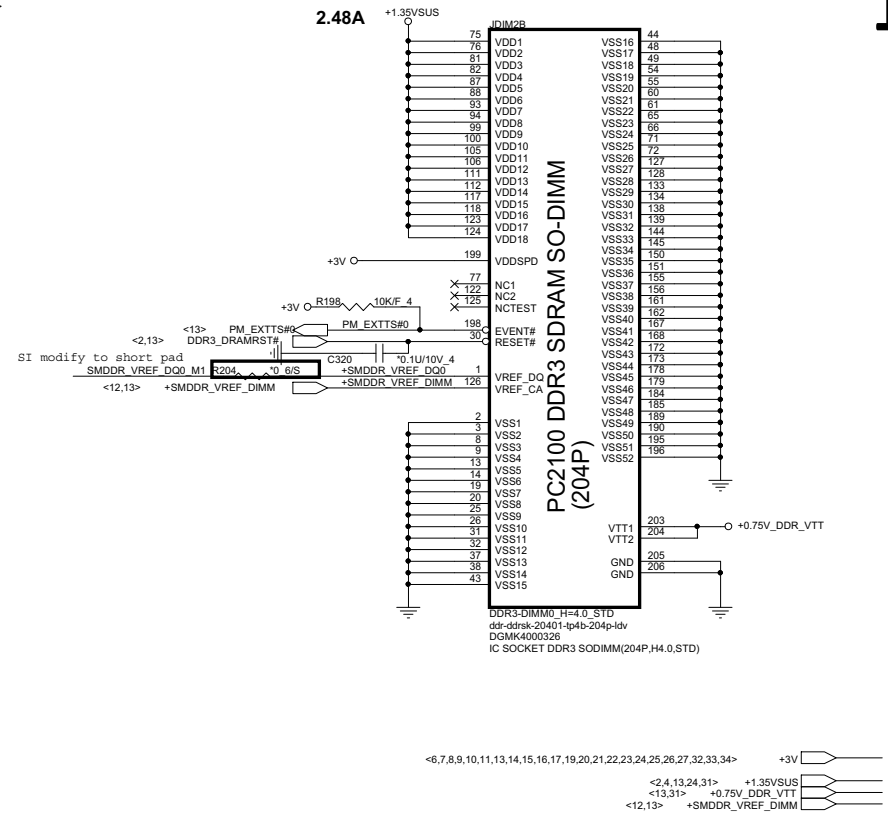
PROJECT :U82
Quanta Computer Inc.
ULT

Size Document Number Rev
HSW XDP & APS 1A

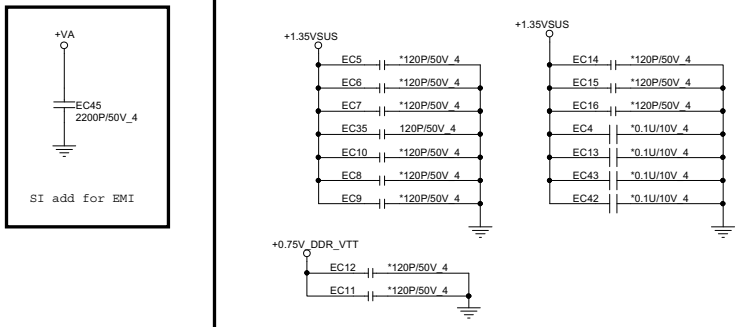
Friday, April 27, 2013 11:54:41 AM



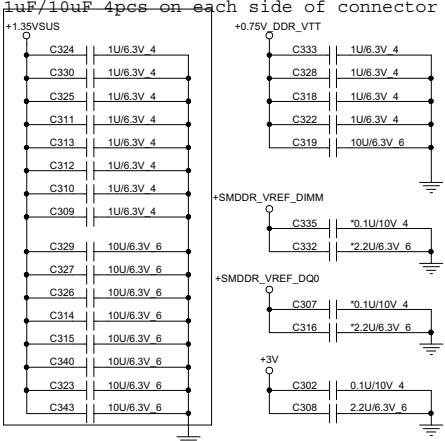
M_A_DQ[63:0]



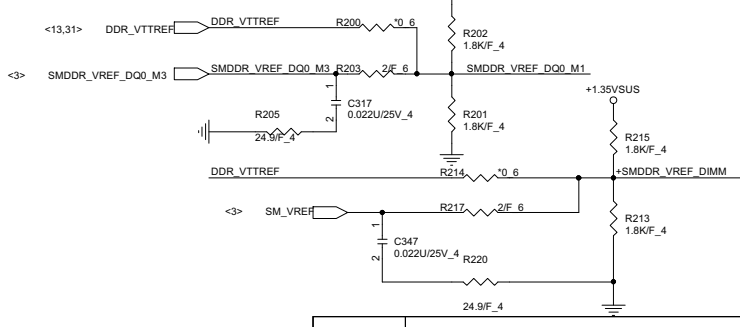
For EMI RESERVE



Place these Caps near So-Dimm0.



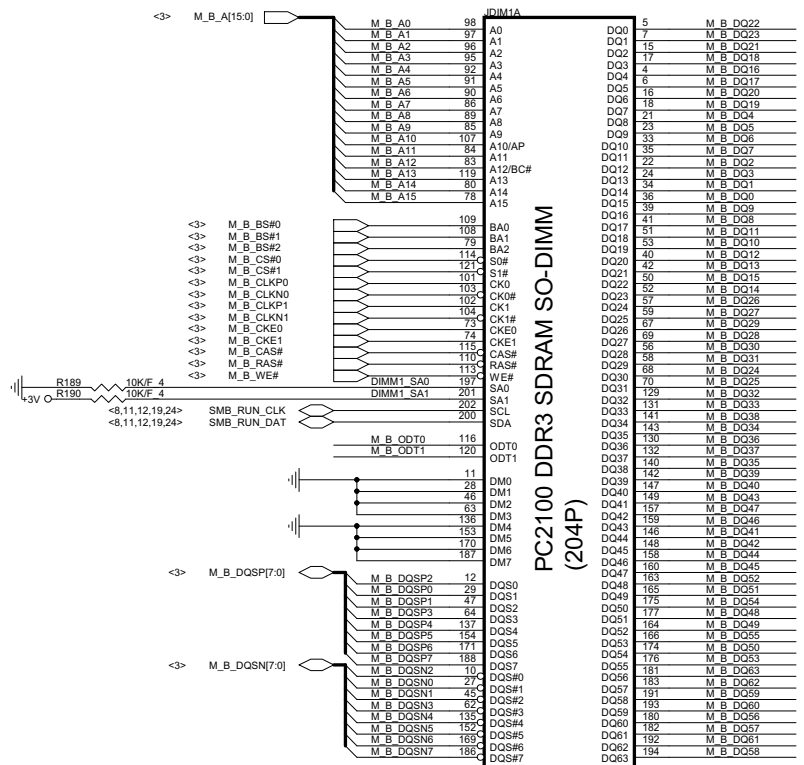
VREF DQ0 M1 Solution



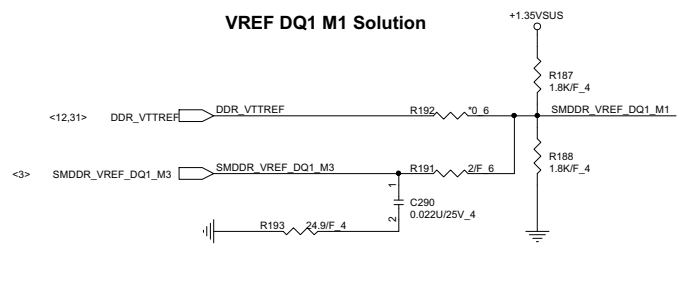
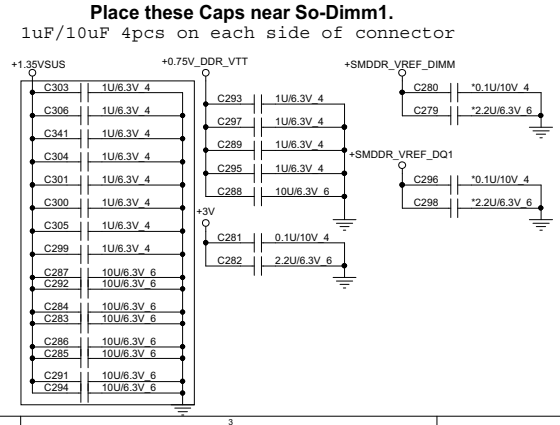
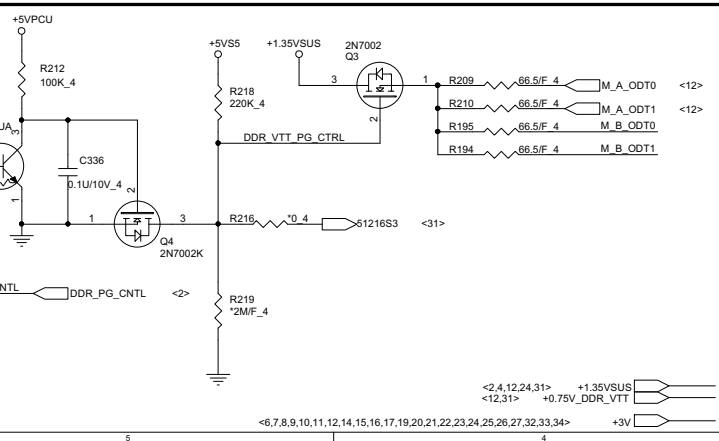
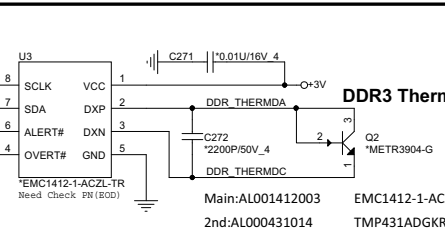
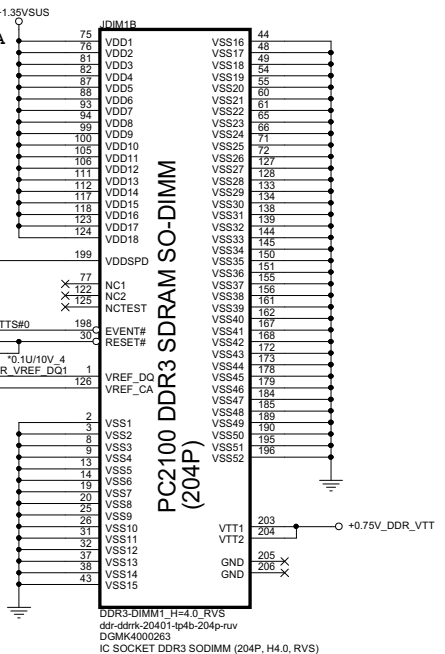
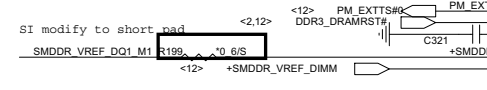
PROJECT :U82
Quanta Computer Inc.

Size Custom Document Number **DDR3 DIMM0-STD(4.0H)** Rev 1A
Date: Friday, April 26, 2013 Sheet 12of 40

M_B_DQ[63:0] <-3>

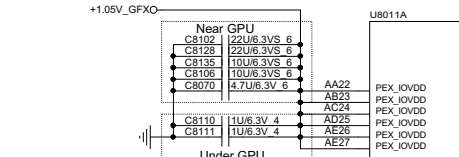


DDR3-DIMM1_H=4.0_RVS
 ddr-ddrk-20401-4p4b-204p-ruv
 DGMK4000263
 IC SOCKET DDR3 SODIMM (204P, H4.0, RVS)

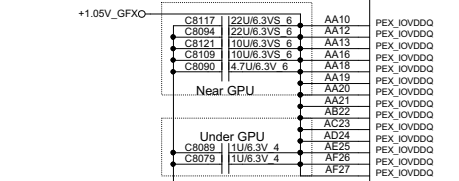


PROJECT :U82
 Quanta Computer Inc.

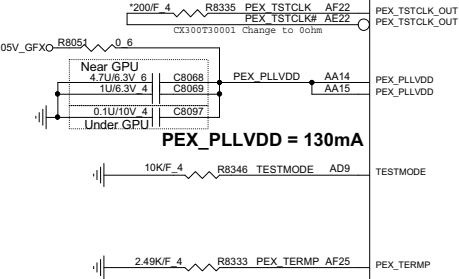
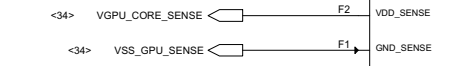
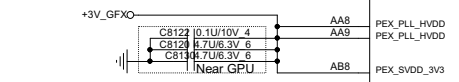
Size Custom Document Number **DDR3 DIMM1-RVS(4.0H)** Rev 1A
 Date: Friday, April 26, 2013 Sheet 13 of 40



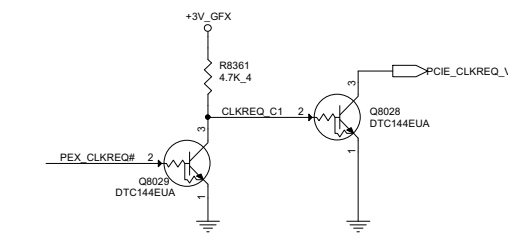
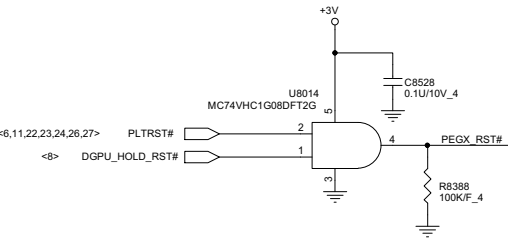
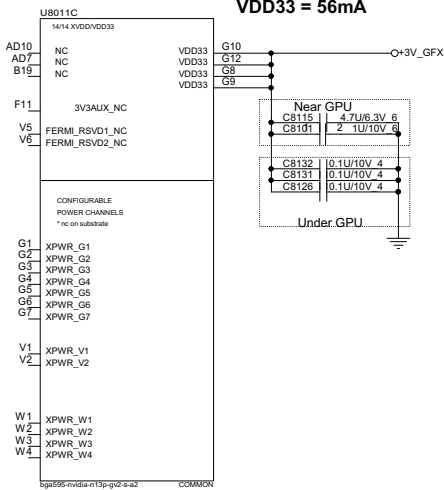
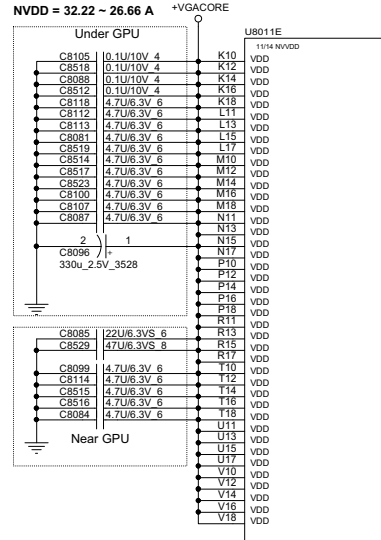
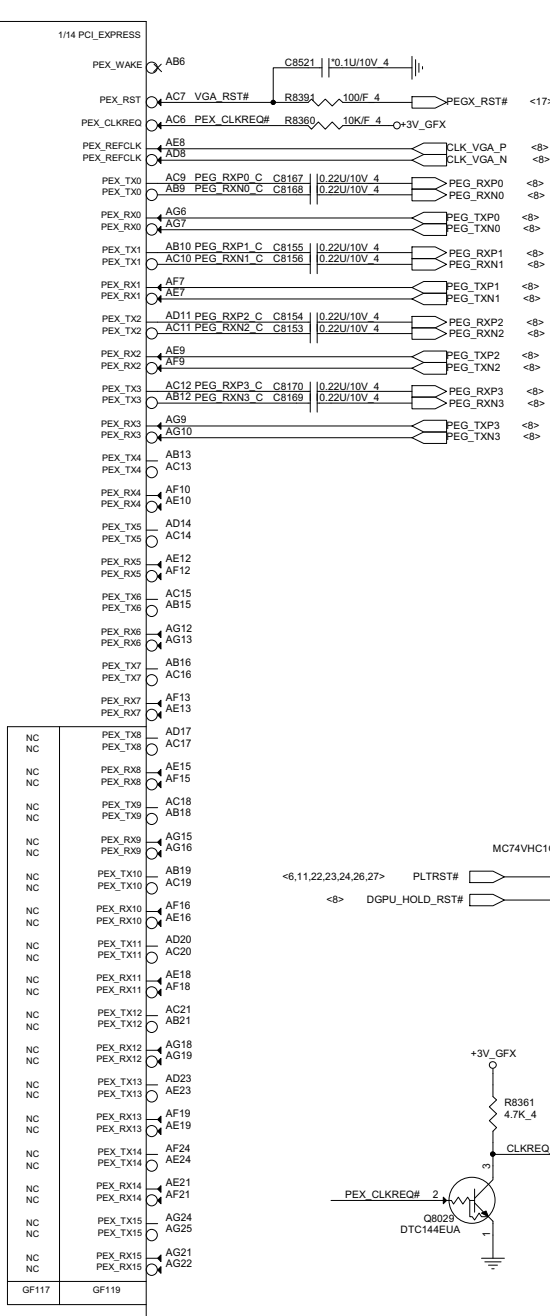
PEX_IOVDD + PEX_IOVDDQ = 1.042A



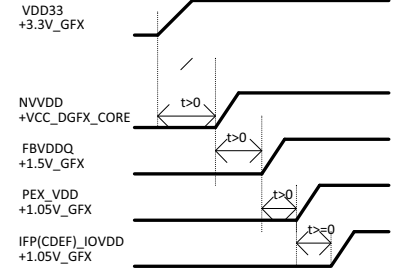
PEX_PLL HVDD + PEX_SVDD_3V3 = 143mA



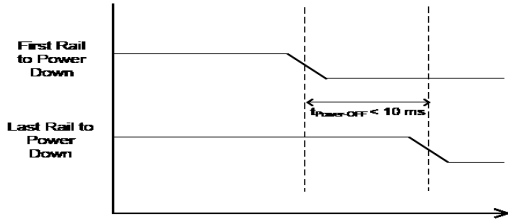
PEX_PLLVDD = 130mA



Power up sequence

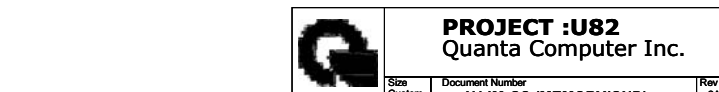
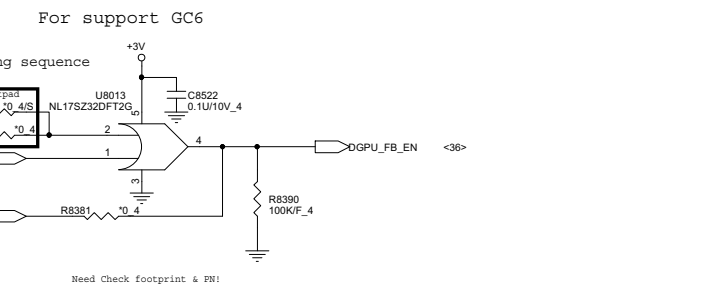
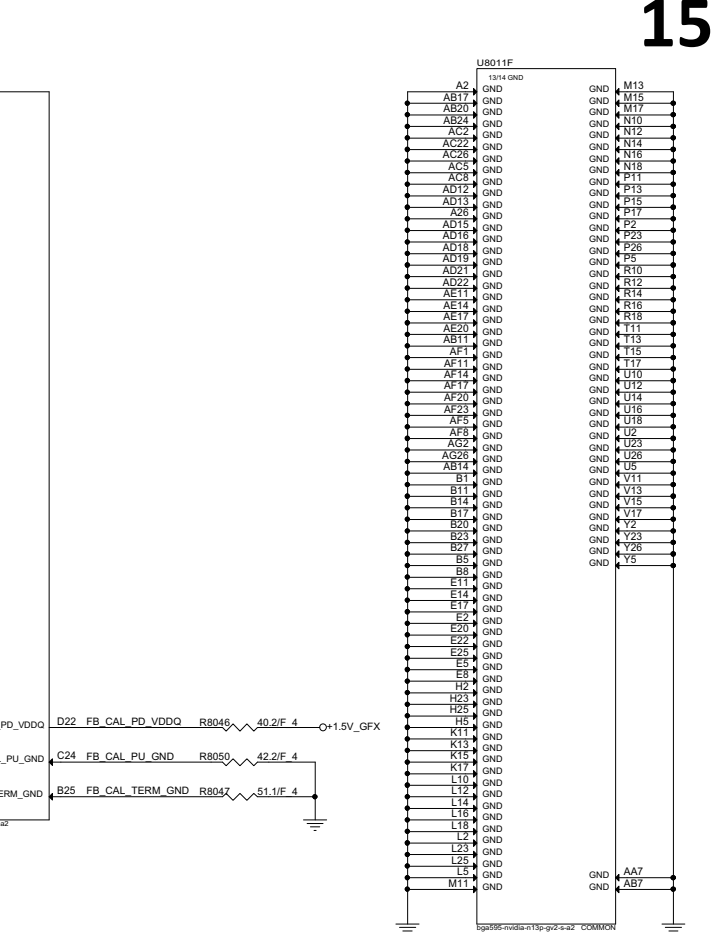
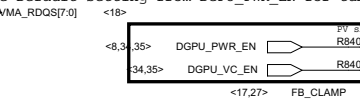
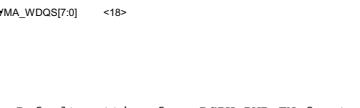
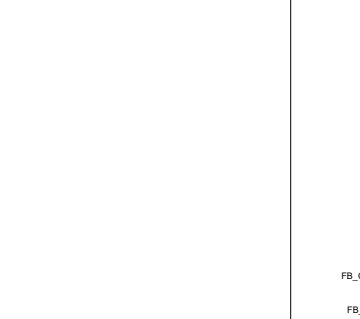
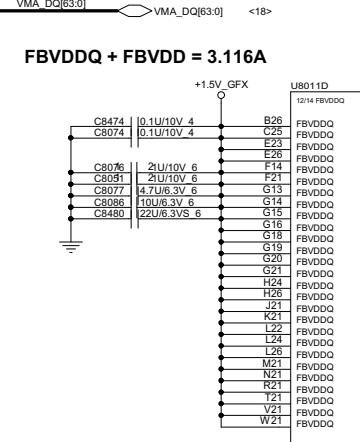
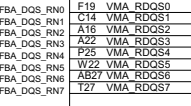
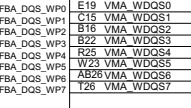
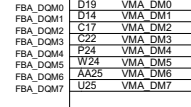
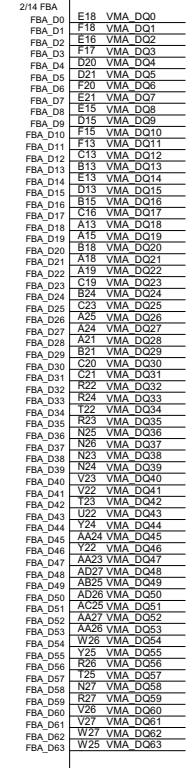
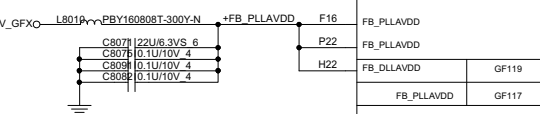
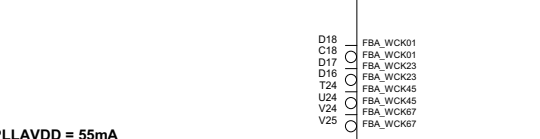
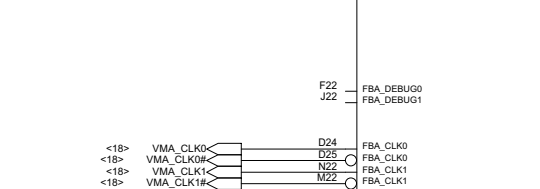
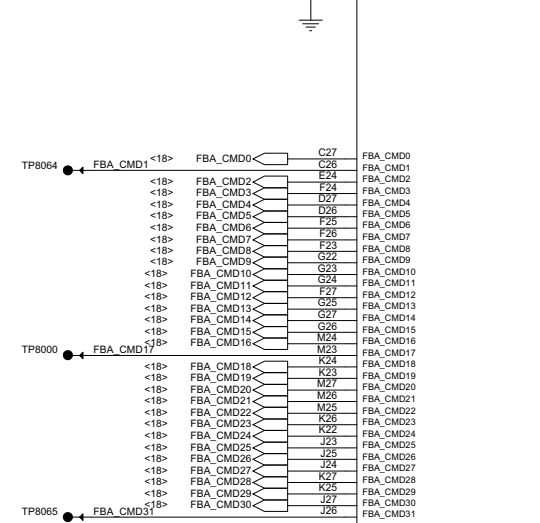
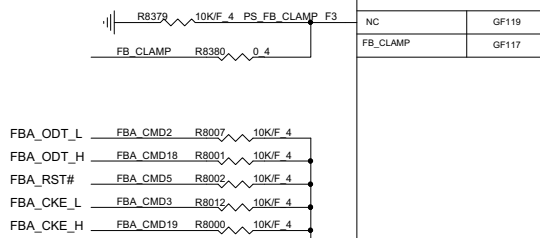


Power down sequence



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GS (PCIe I/F) /NVDD	2A
Date: Friday, April 26, 2013	Sheet 14 of 40	



FB_PLLAVDD = 55mA

FB_DLLAVDD = 15mA

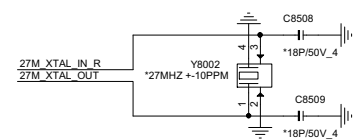
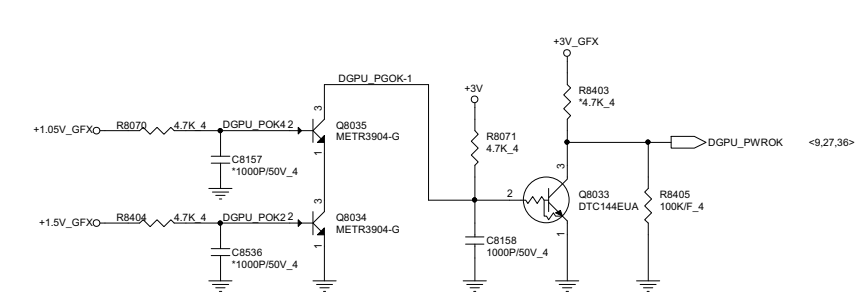
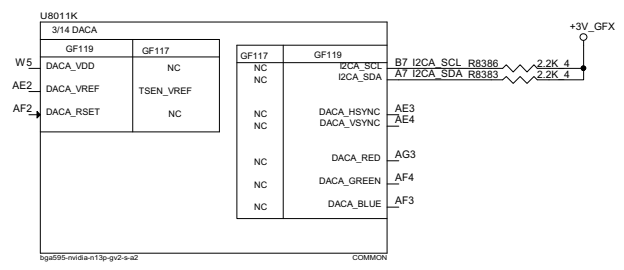
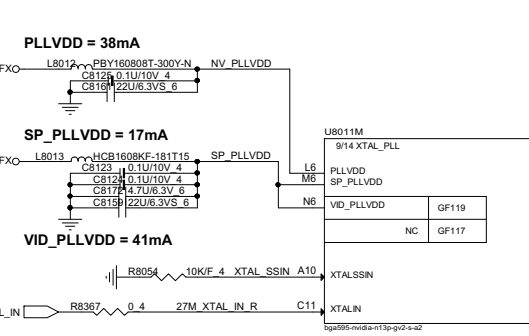
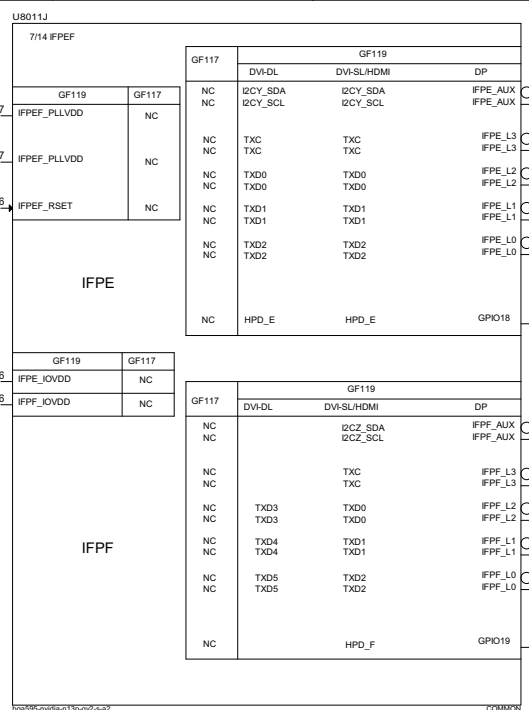
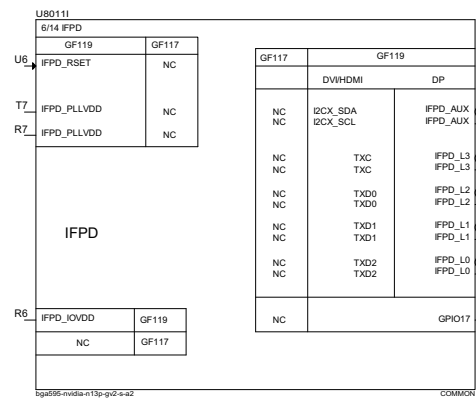
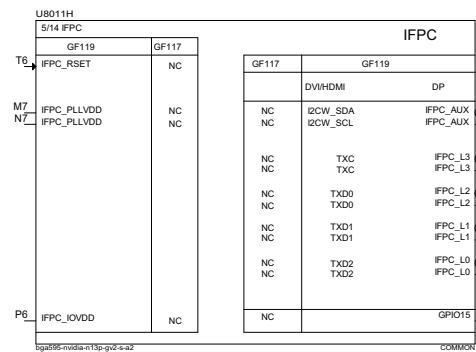
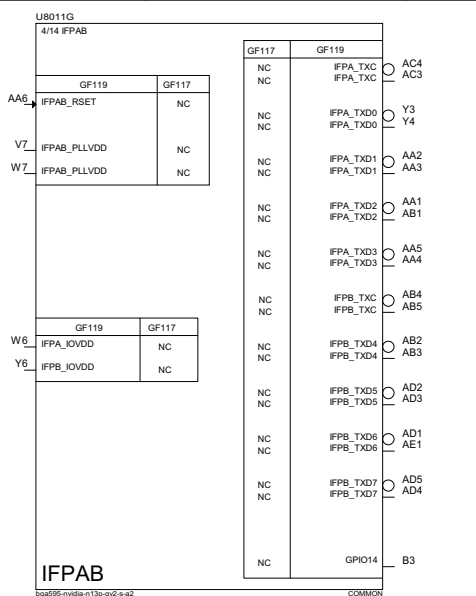
Change Default setting from DGPU_PWR_EN for tuning sequence

For support GC6

Need Check footprint & FN!



PROJECT :U82
Quanta Computer Inc.



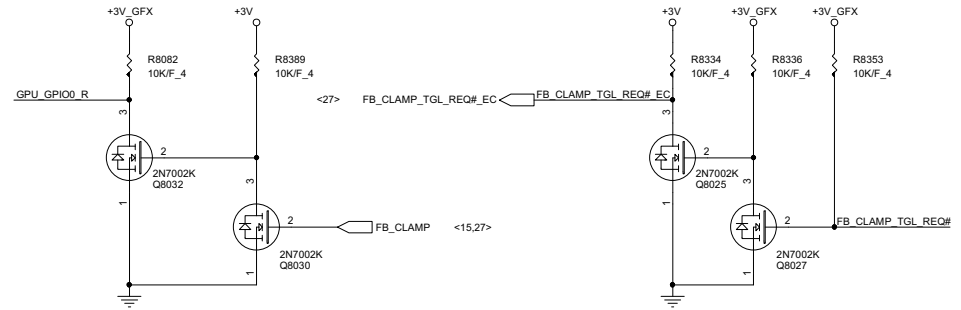
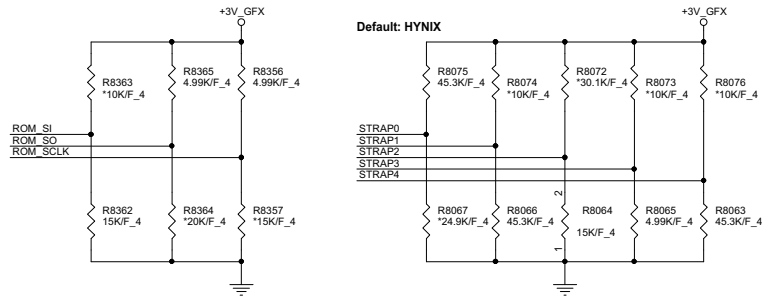
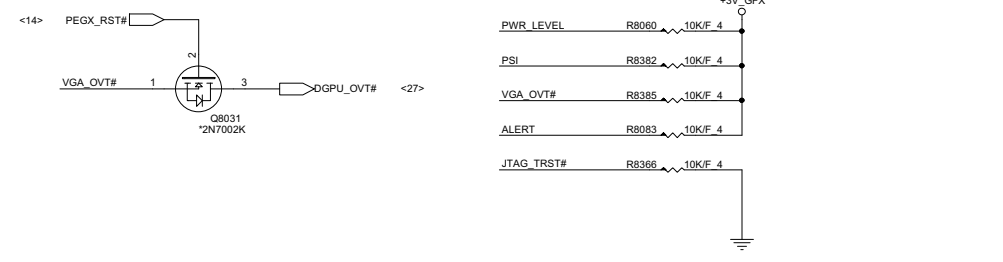
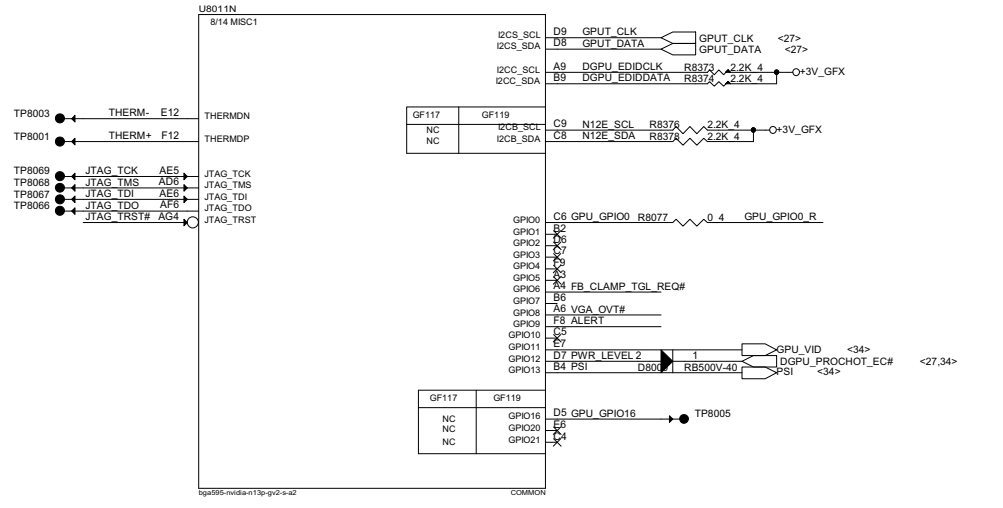
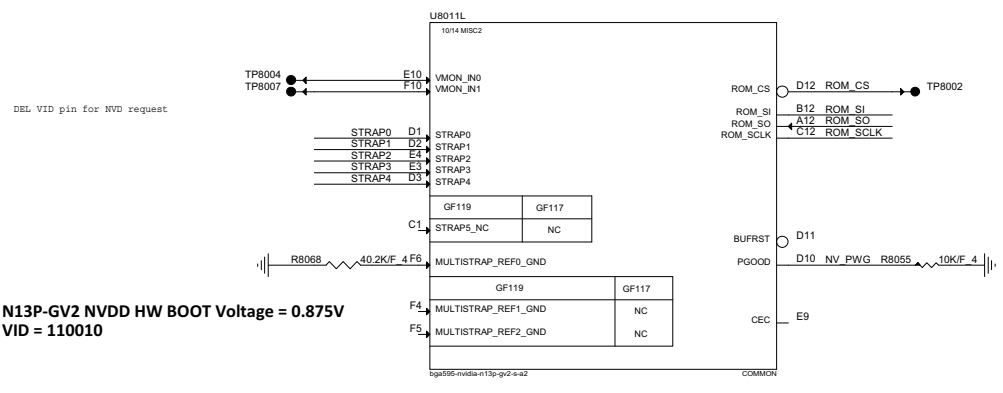
PROJECT :U82
Quanta Computer Inc.

Size Custom Document Number N14M-GS (DISPLAY) Rev 2A

Date: Friday, April 26, 2013 Sheet 16 of 40

DEL VID pin for NVD request

N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010



VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	QCI P/N
0000	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	Micron	MT41J128M16JT-107G:K	AKD5MGSTL06	AKD5MGSTL08
0000	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	HYNIX	H5TQ2G63DFR-11C	AKD5MGWTW16	AKD5MGWTW13
0111	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	SAMSUNG	K4W2G1646E-BC11	AKD5MGGT520	AKD5MGGT522

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

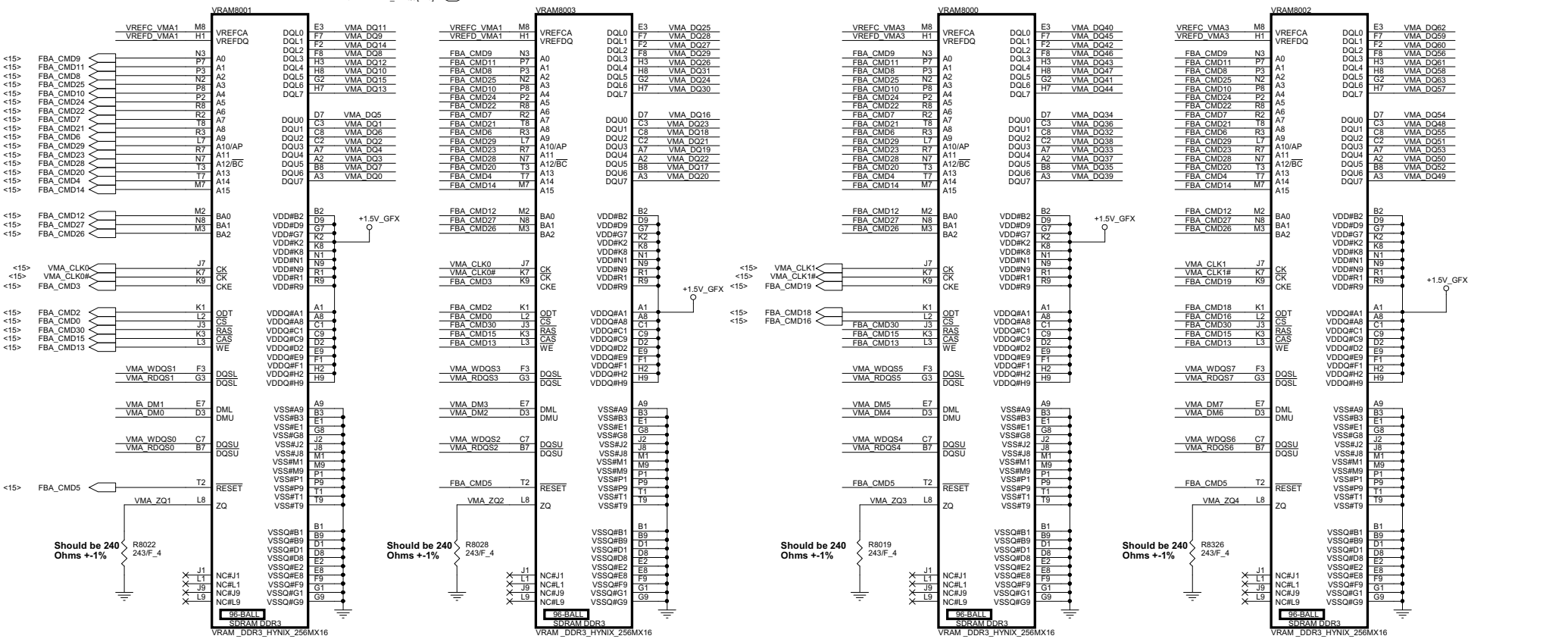
PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number N14M-GS (GPIO/STRAPS)	Rev 2A
Date: Friday, April 26, 2013	Sheet 17 of 40	

CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWTW08 --- AKD5PGWTW07
 Y12 Mx16, PN : AKD5MZDTW03 --- AKD5MZDTW02
 SAM 256Mx16, PN : AKD5PZDT501 --- AKD5PZDT500
 SAM 128Mx16, PN : AKD5MGT535 --- AKD5MGT534

<15> VMA_DQ[63..0]
 <15> VMA_DM[7..0]
 <15> VMA_WDQS[7..0]
 <15> VMA_RDQS[7..0]

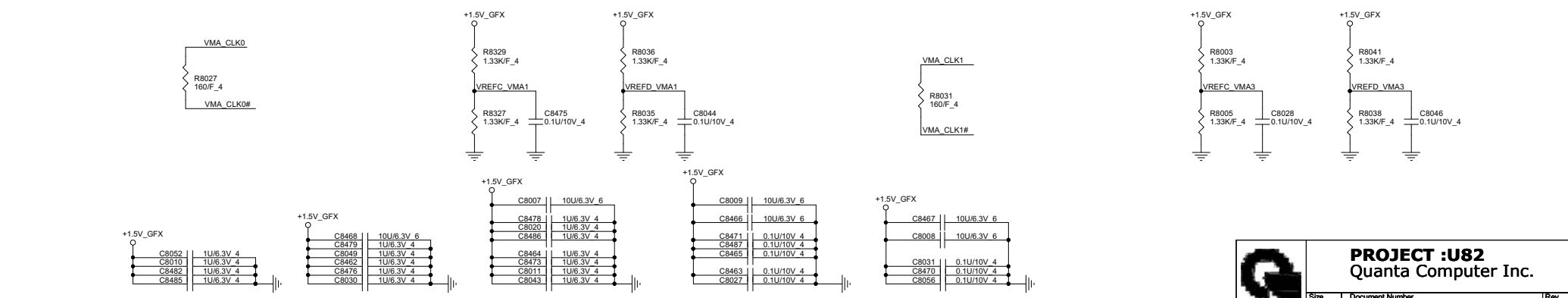


Should be 240 Ohms +/-1%

Should be 240 Ohms +/-1%

Should be 240 Ohms +/-1%

Should be 240 Ohms +/-1%

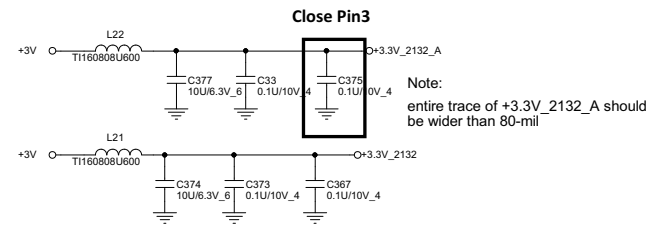
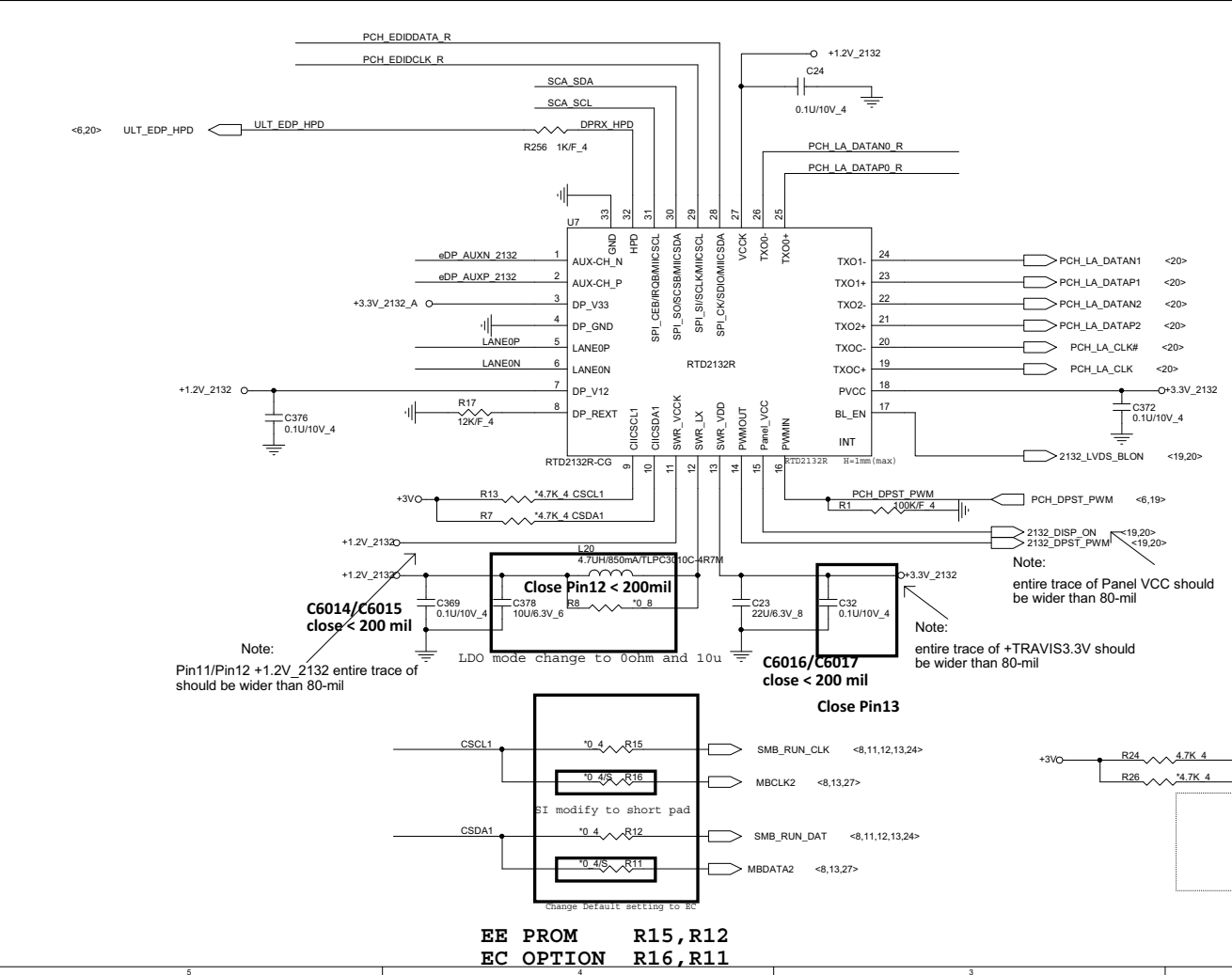
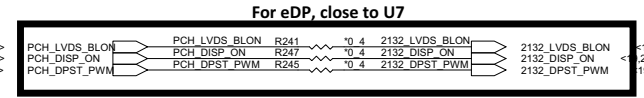
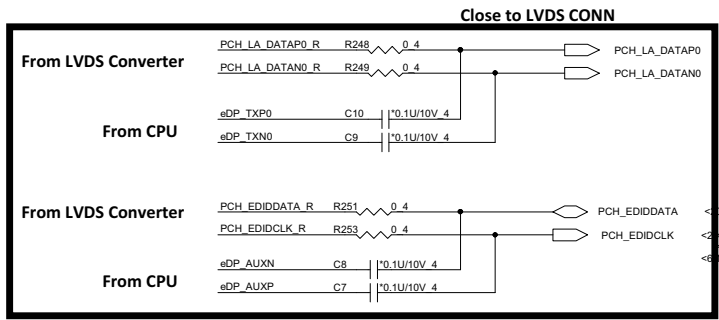
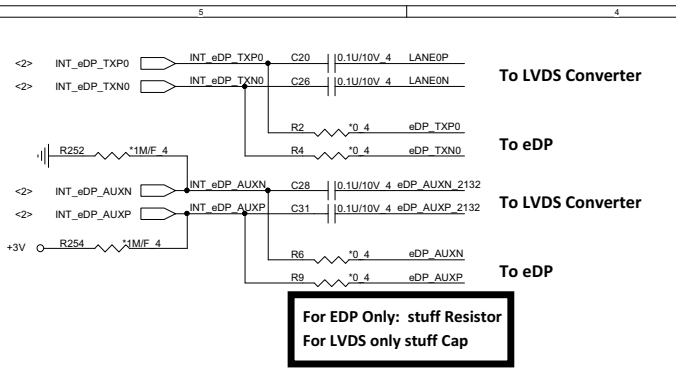


PROJECT :U82
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Size Custom Document Number
GPU Memory (DDR3)

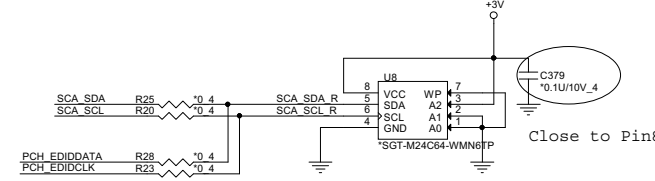
Date: Friday, April 26, 2013 Sheet 18 of 40

Rev 2A



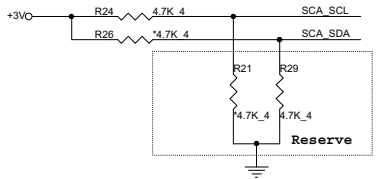
SCA_SCL pull high => EEPROM mode
 SCA_SDA pull low => EEPROM Free mode

Address=0xA8



RTD2132S => R25, R20
 RTD2132R => R28, R23

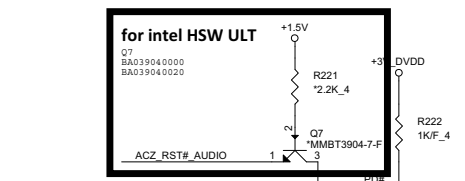
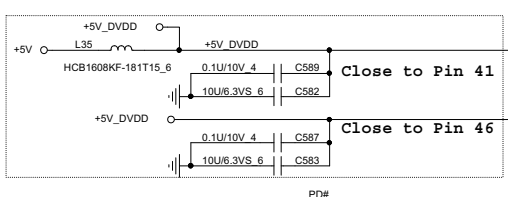
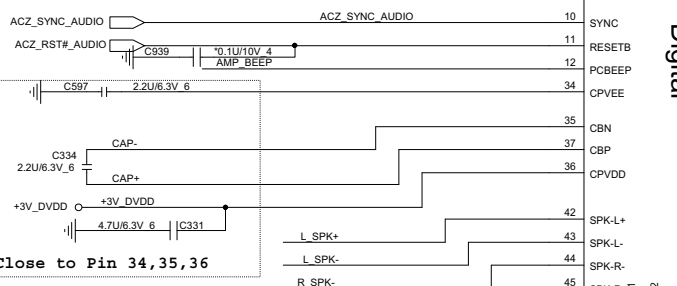
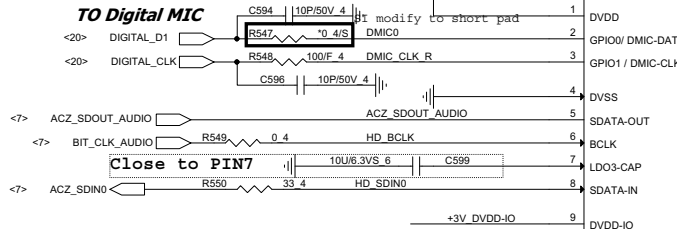
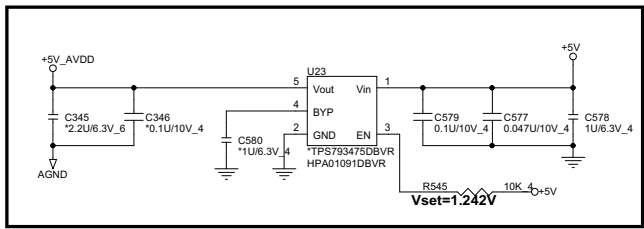
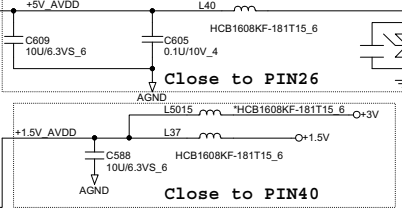
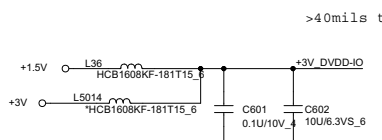
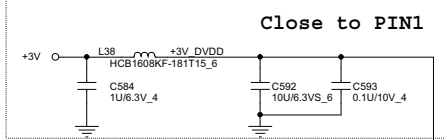
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



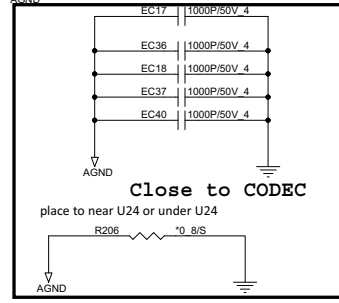
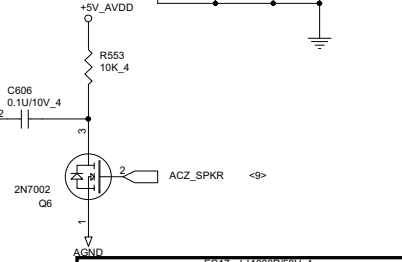
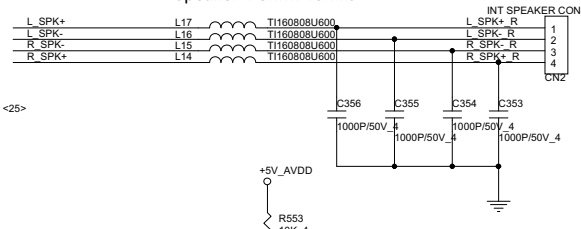
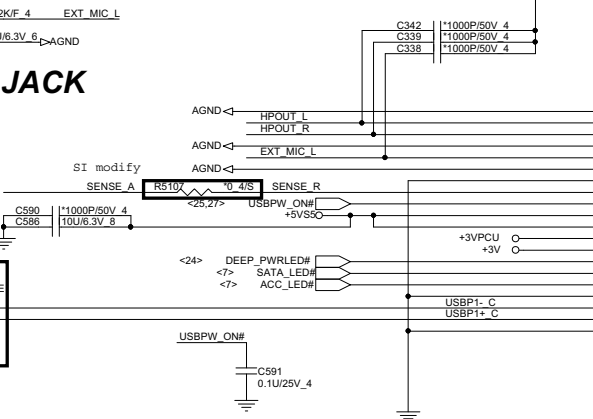
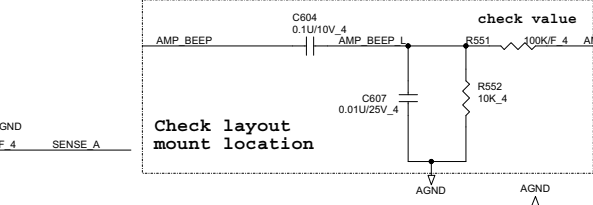
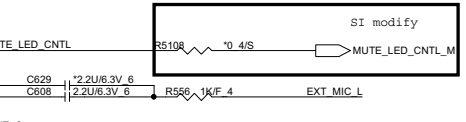
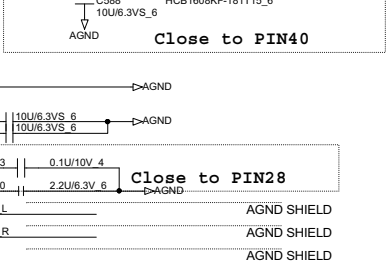
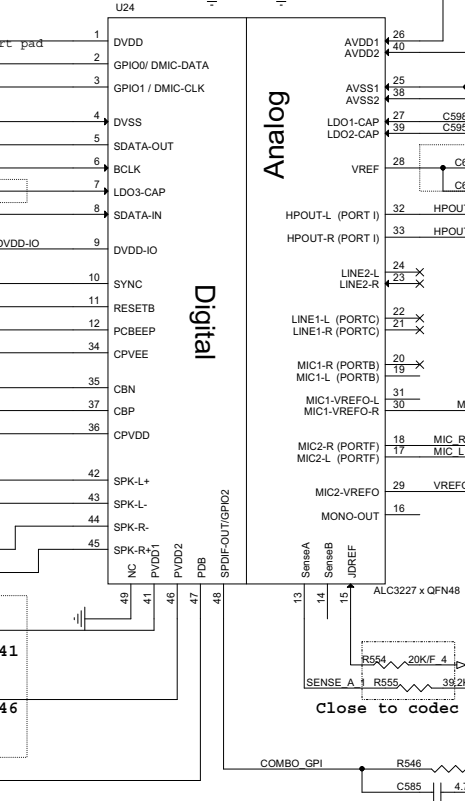
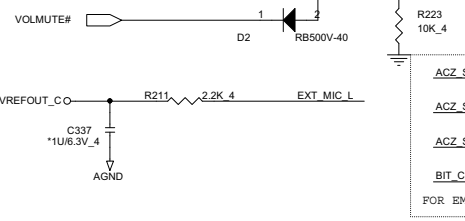
EE PROM R15, R12
 EC OPTION R16, R11

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 Quanta Computer Inc.

Size Custom	Document Number LVDS converter RTD2132R	Rev 1A
Date: Friday, April 26, 2013	Sheet 19	of 40

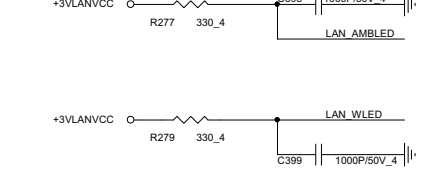
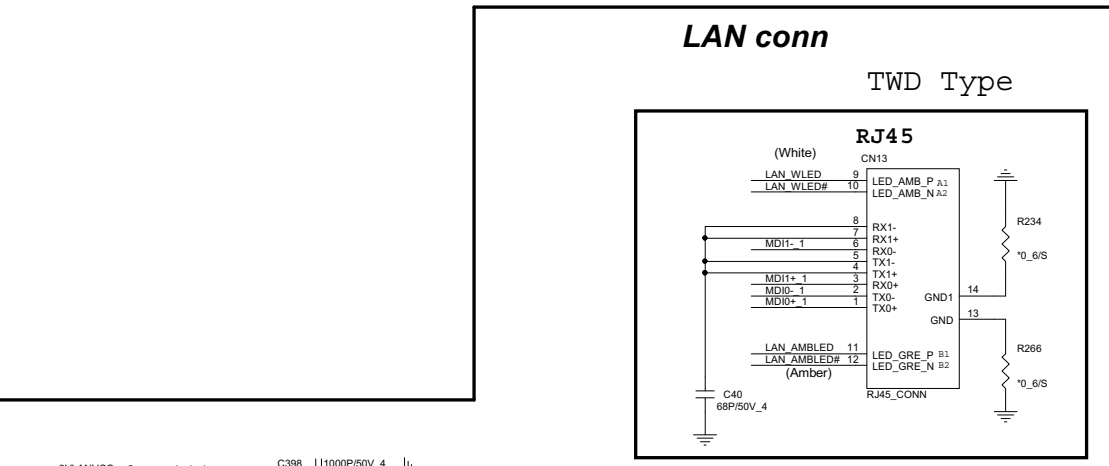
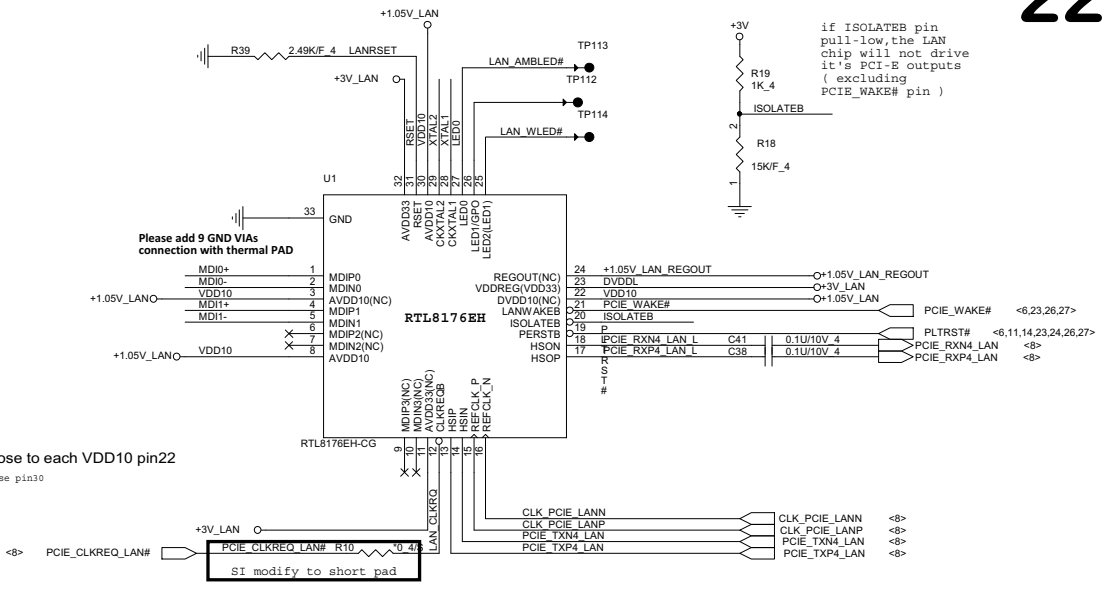
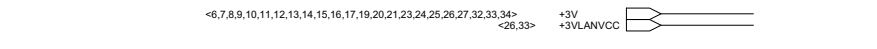
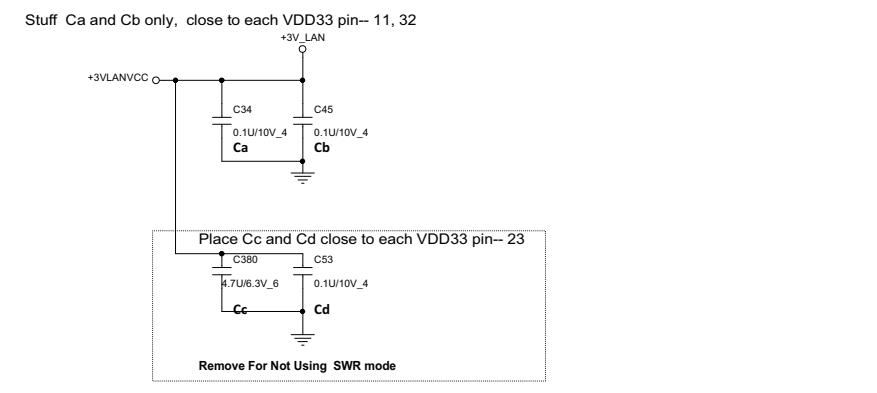
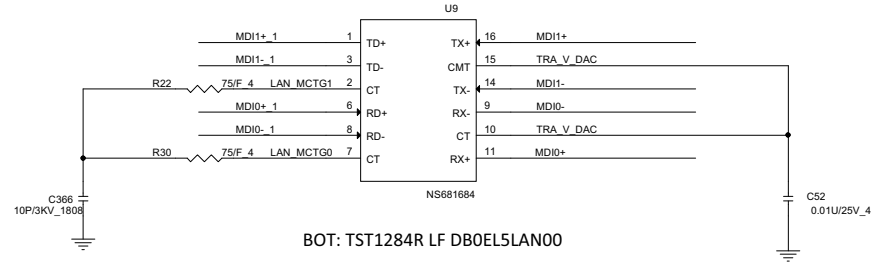
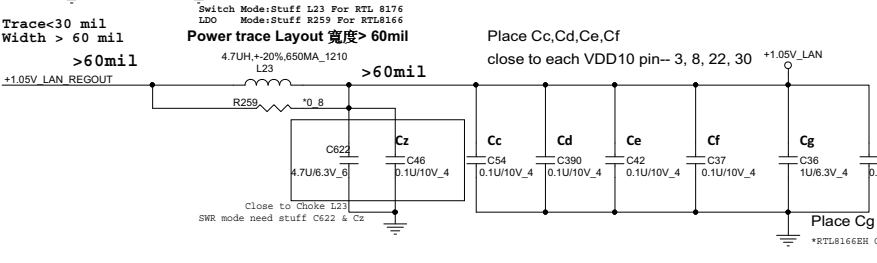
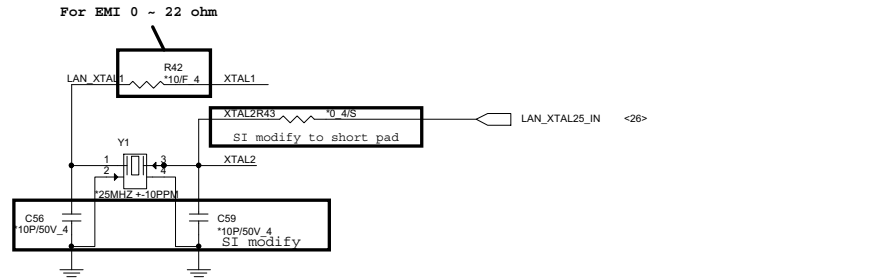


USB 2.0 AND AUDIO COMBO JACK



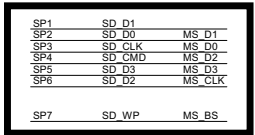
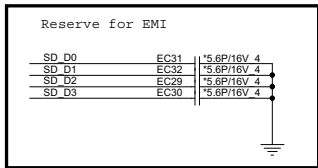
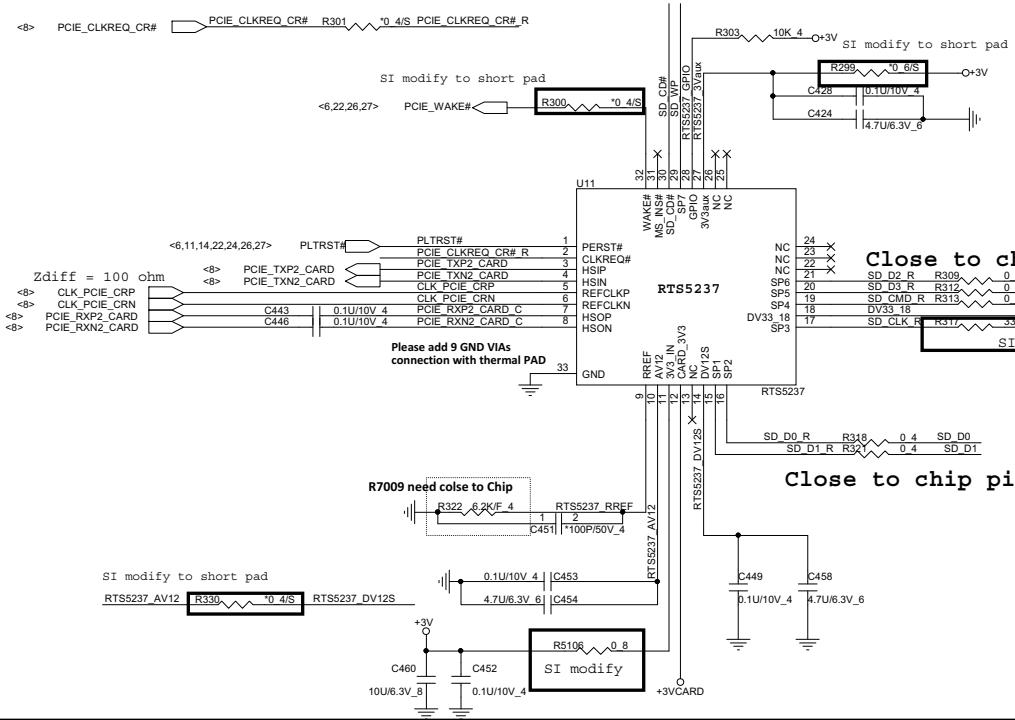
PROJECT :U82
Quanta Computer Inc.

Size Custom Document Number Azalla ALC 3227 Rev 1A
Date: Friday, April 26, 2013 Sheet 21 of 40



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Quanta Computer Inc.

Size Custom Document Number LAN RTL8176EH/RJ45 Rev 1A
Date: Friday, April 26, 2013 Sheet 22 of 40



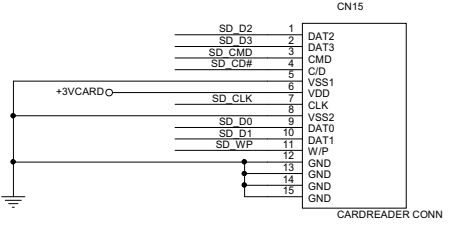
Share Pin
SD / MMC

Close to chip pin

Close to chip pin

CLOSE CONN

CARD READER

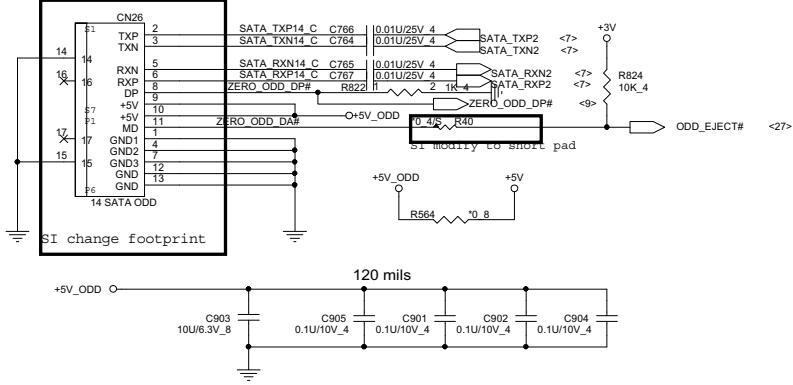


R3X Type

SATA ODD CONNECTOR

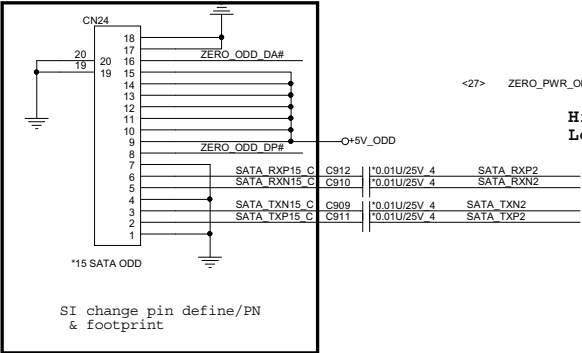
14" SATA ODD

Bypass CAP close conn



15" SATA ODD

New Type



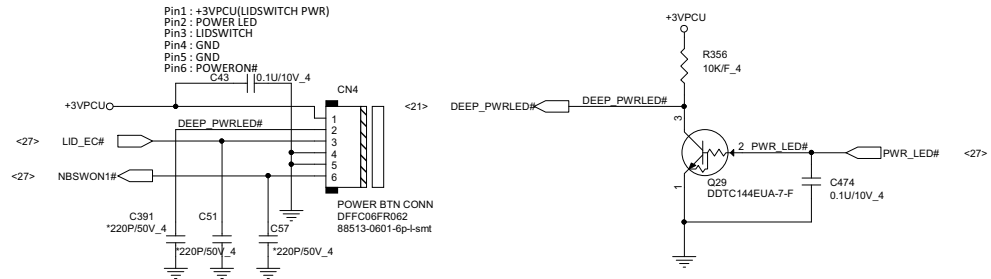
High : ODD power down
Low : ODD power on



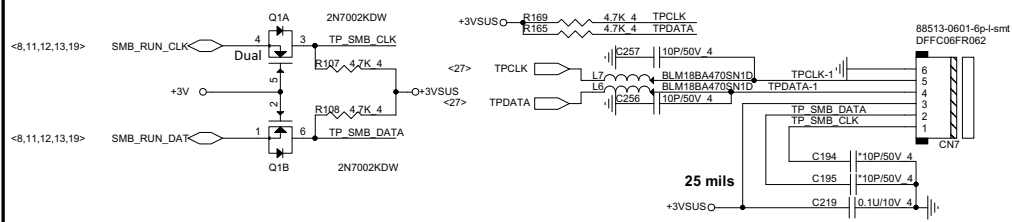
PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number CR RTS5237 & CR SOCKET	Rev 1A
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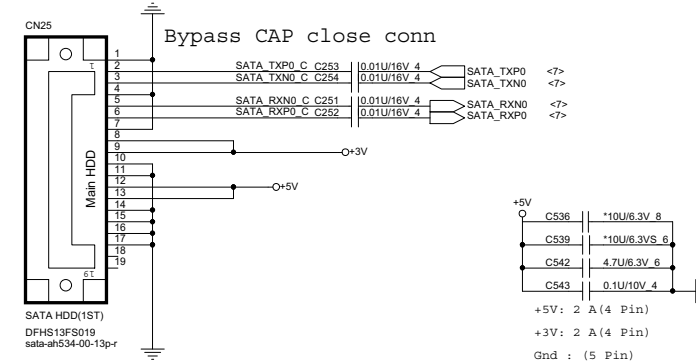
Power Button Connector



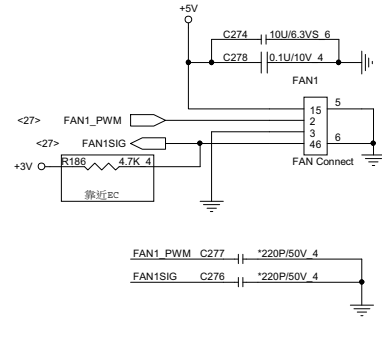
Touch Pad Connector



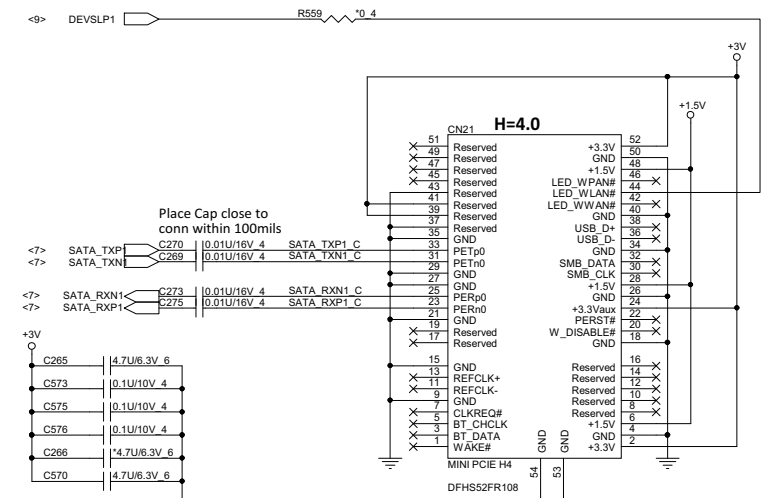
SATA HDD Connector(Cable type)



FAN

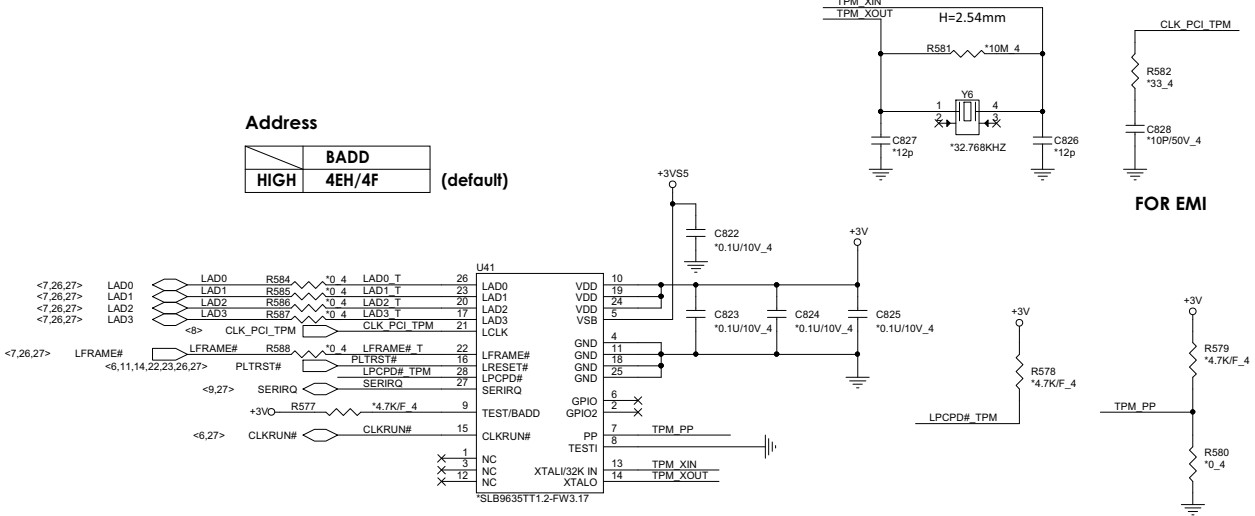


Mini PCI-E Card 2- Full size mSATA



TPM (1.2)

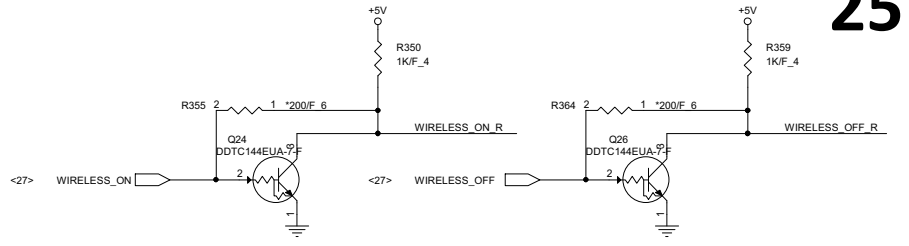
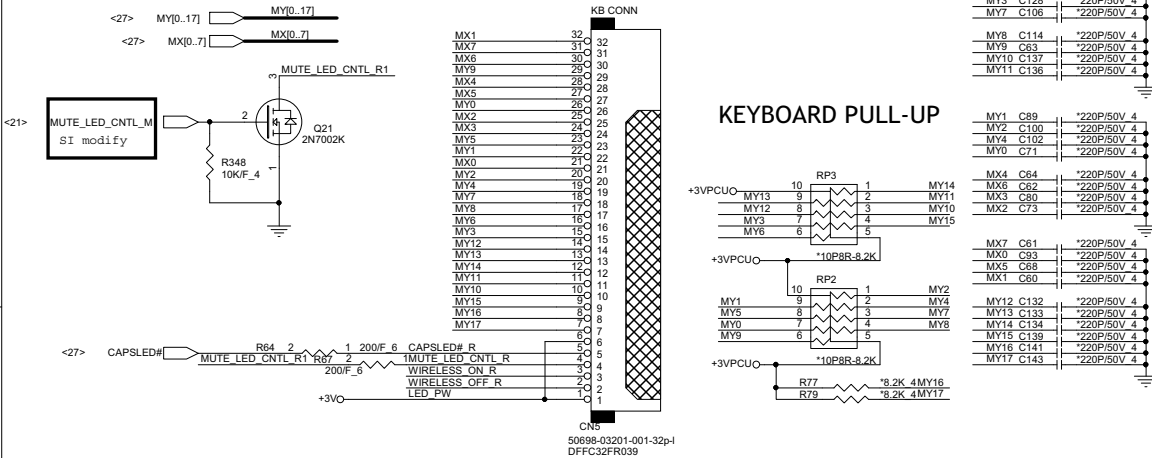
Address	
BADD	(default)
HIGH	4EH/4F



+VINO	C361	0.1u/25V 4
+VINO	C264	0.1u/25V 4
+VINO	C610	0.1u/25V 4
+VINO	C611	0.1u/25V 4
+VINO	C612	0.1u/25V 4
+VINO	C613	0.1u/25V 4
+VINO	C615	0.1u/25V 4
+VINO	C614	0.1u/25V 4
+VINO	C616	0.1u/25V 4
+VINO	C618	0.1u/25V 4
+VINO	C617	0.1u/25V 4
+VINO	C619	0.1u/25V 4
+VINO	C29	0.1u/25V 4
+VINO	C69	0.1u/25V 4
+VINO	C196	0.1u/25V 4
+VINO	C240	0.1u/25V 4
+VINO	C259	0.1u/25V 4
+VINO	C3	0.1u/25V 4
+VINO	C11	0.1u/25V 4
+VINO	C371	0.1u/25V 4
+VINO	C370	0.1u/25V 4
+VINO	C447	0.1u/25V 4
+VINO	C395	0.1u/25V 4
+VINO	C261	0.1u/25V 4
+VINO	C268	0.1u/25V 4
+PRWSRCO	C19	0.1u/25V 4
+PRWSRCO	C12	0.1u/25V 4
+PRWSRCO	C44	0.1u/25V 4
+PRWSRCO	C110	0.1u/25V 4

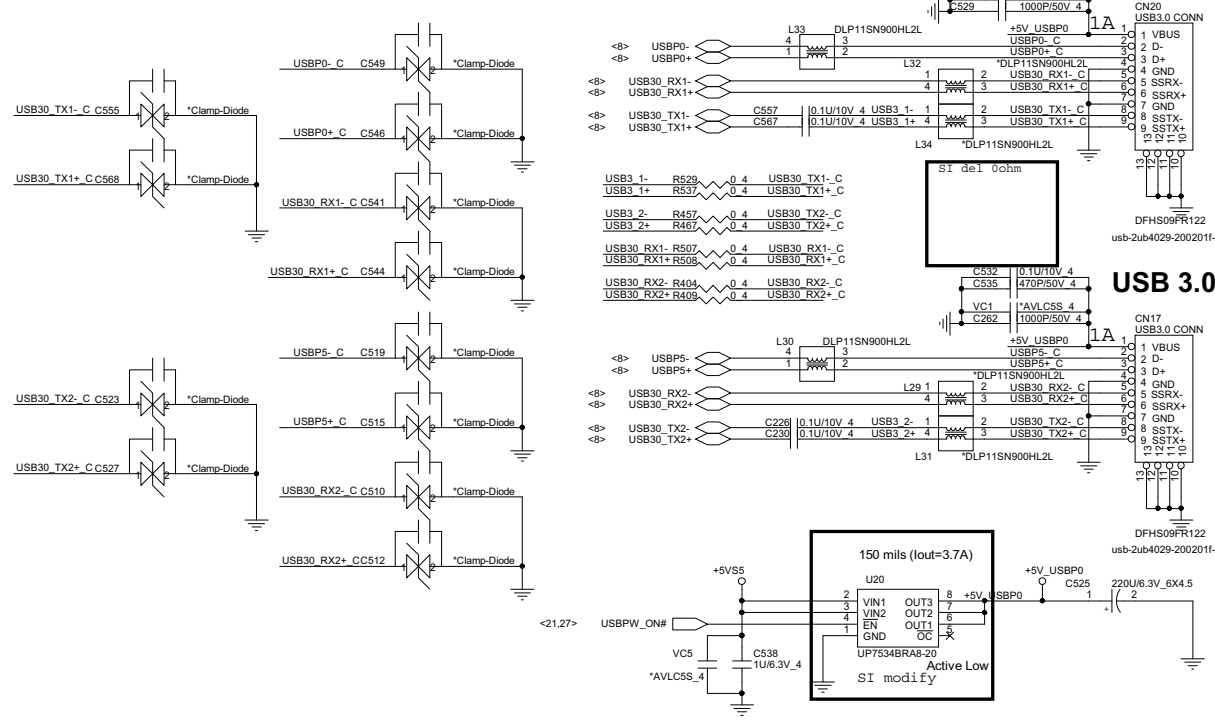
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KEYBOARD Con.

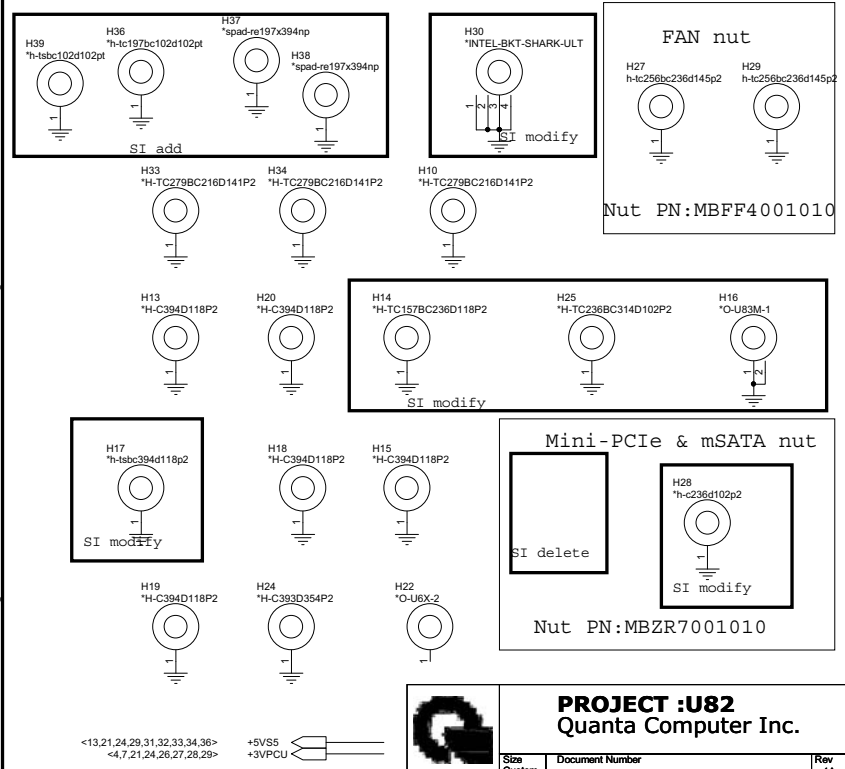


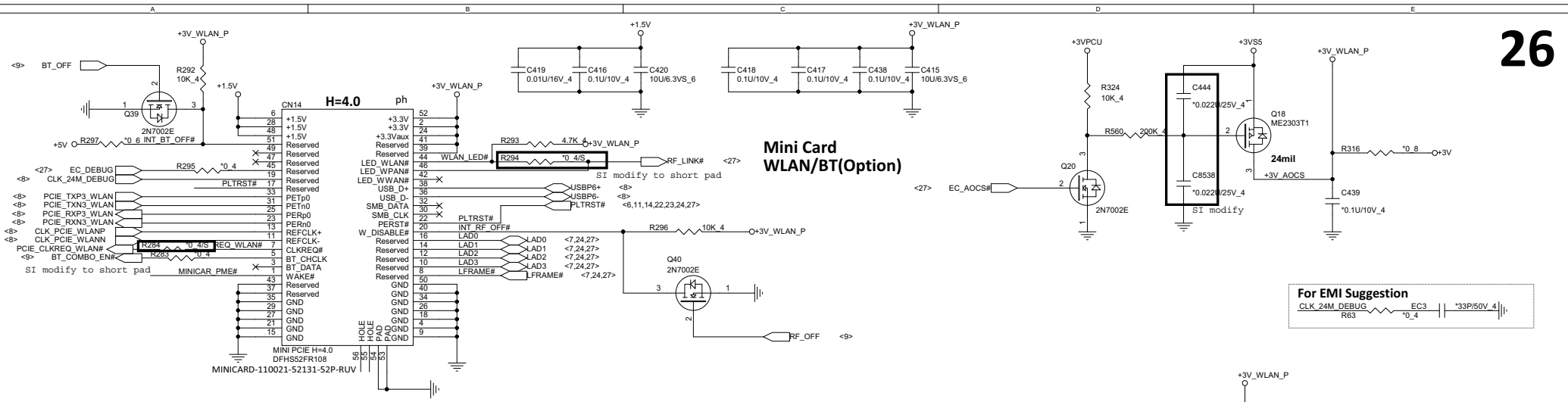
R6X Type

USB 2.0/3.0 Combo

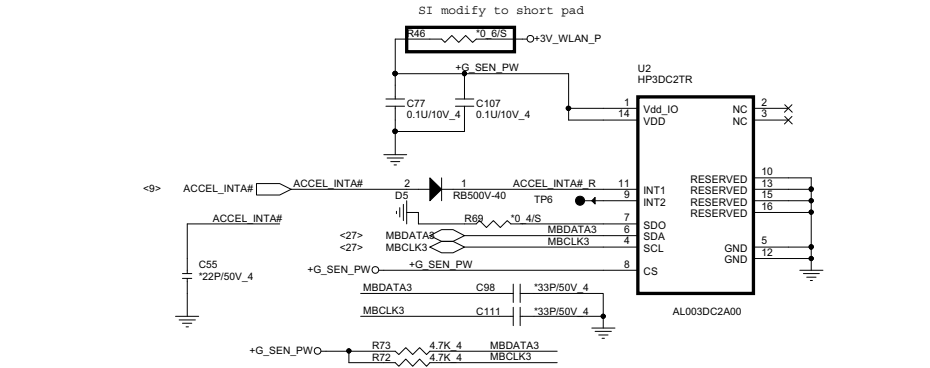


Hole

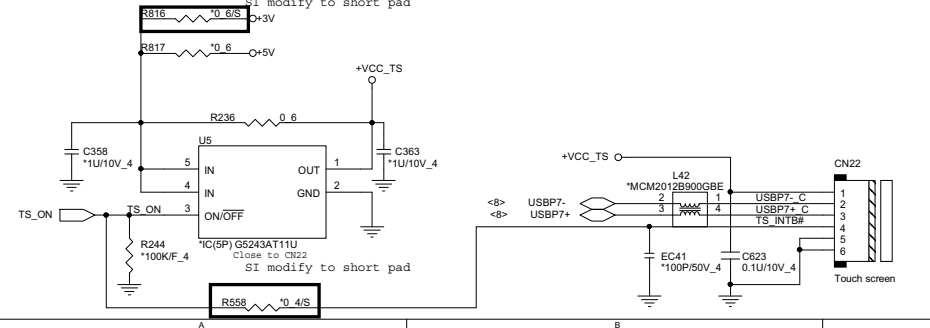




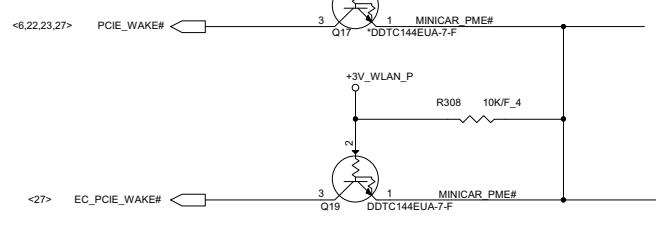
Accelerometer Sensor



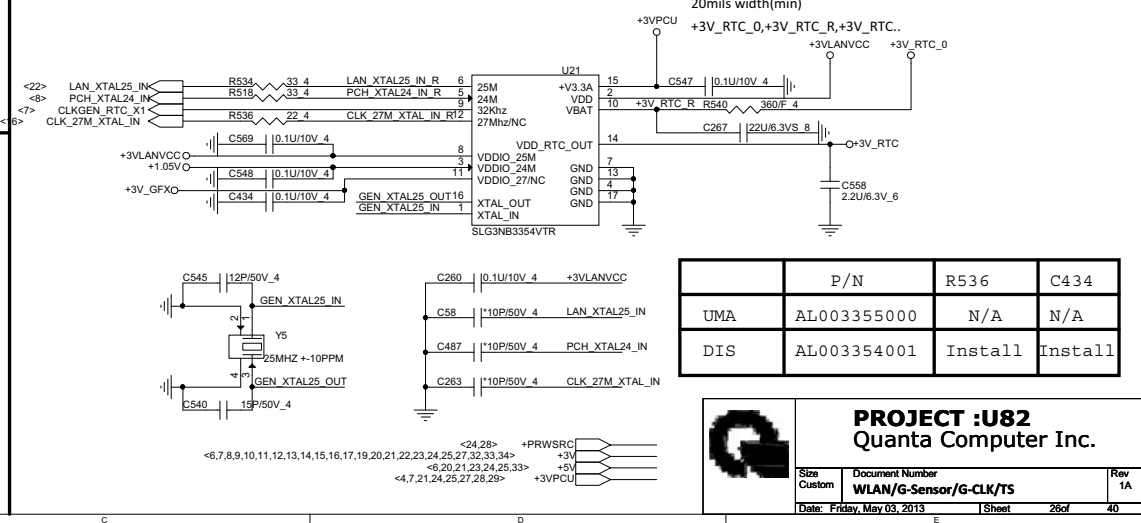
Touch screen



Support Wake Function(Reserve)



Green CLK Circuitry

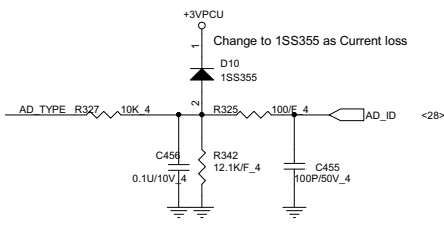
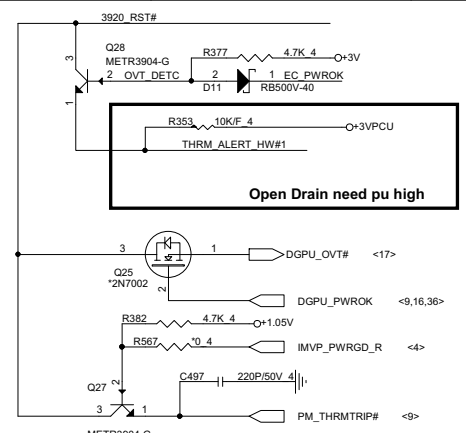


	P/N	R536	C434
UMA	AL003355000	N/A	N/A
DIS	AL003354001	Install	Install

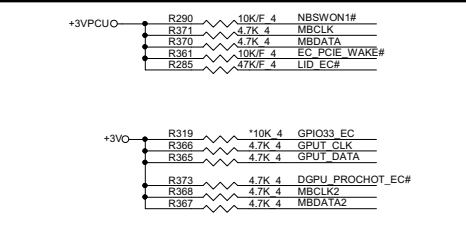
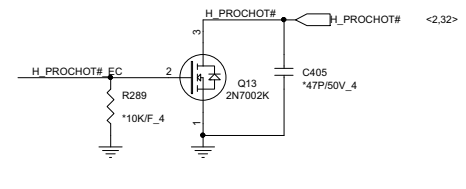
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Size Custom Document Number **WLAN/G-Sensor/G-CLK/TS** Rev 1A
Date: Friday, May 03, 2013 Sheet 26 of 40

adapter Type check

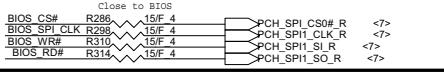


for Battery charge, charge for DDR Thermal IC

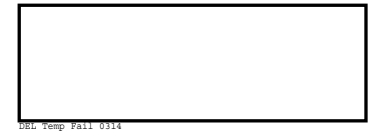


Reserve for ENB Hold time issue

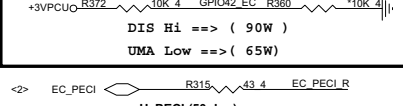
MBCLK2	C479	*10P/50V 4
MBDATA2	C478	*10P/50V 4
MBCLK	C481	*10P/50V 4
MBDATA	C480	*10P/50V 4
GPURT_CLK	C477	*10P/50V 4
GPURT_DATA	C476	*10P/50V 4



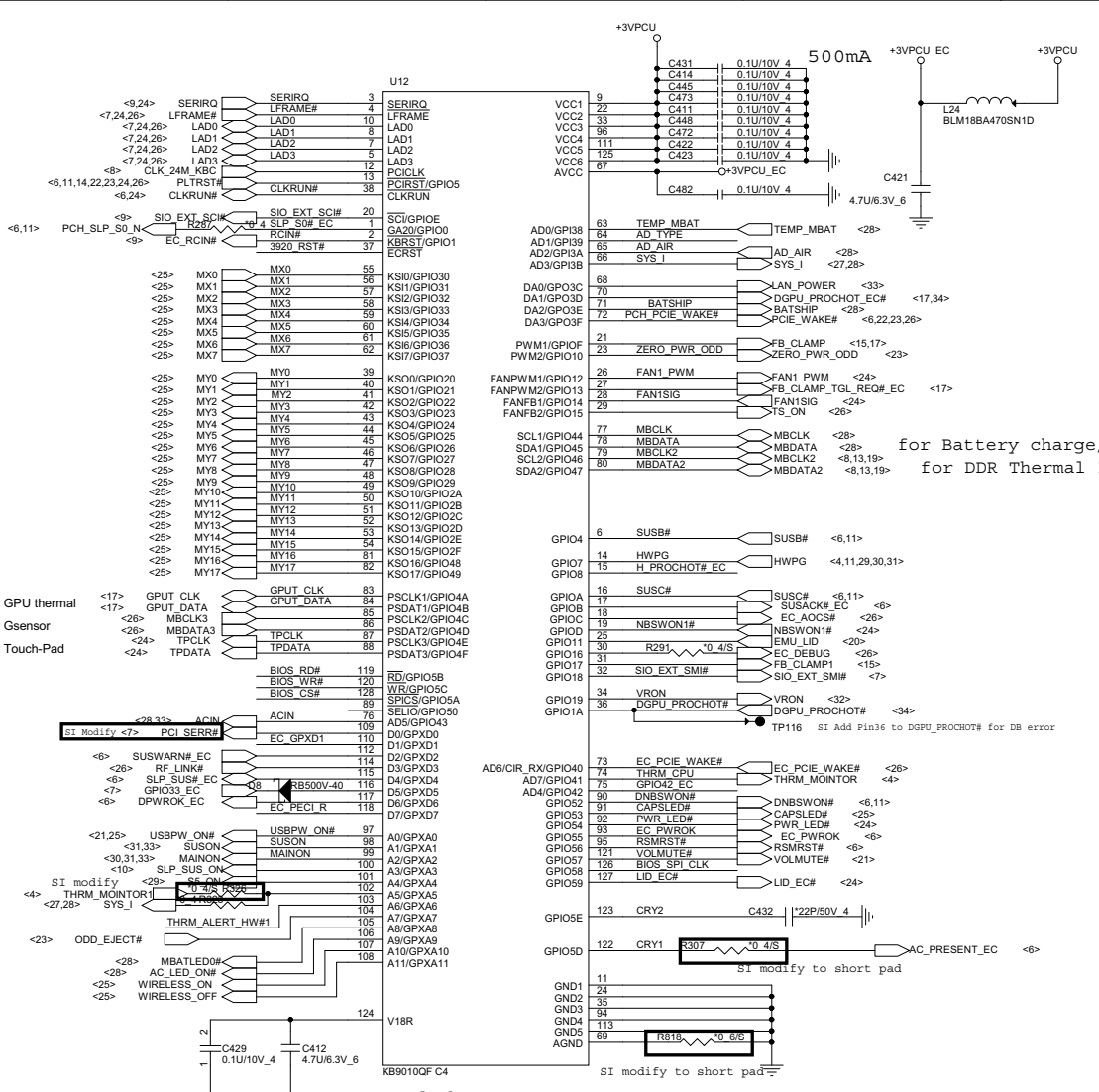
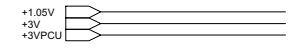
DGPU Thermal protect



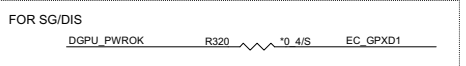
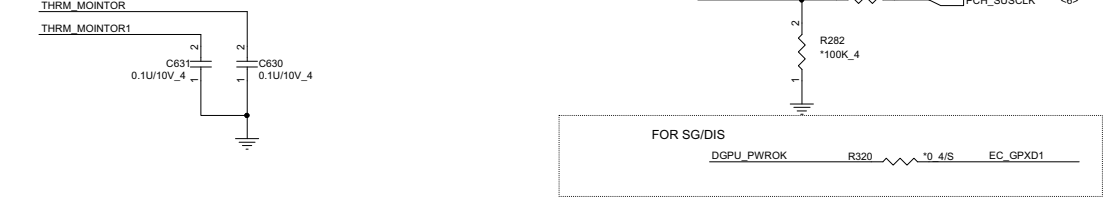
Adapter select for EC



H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4-6.125 inches

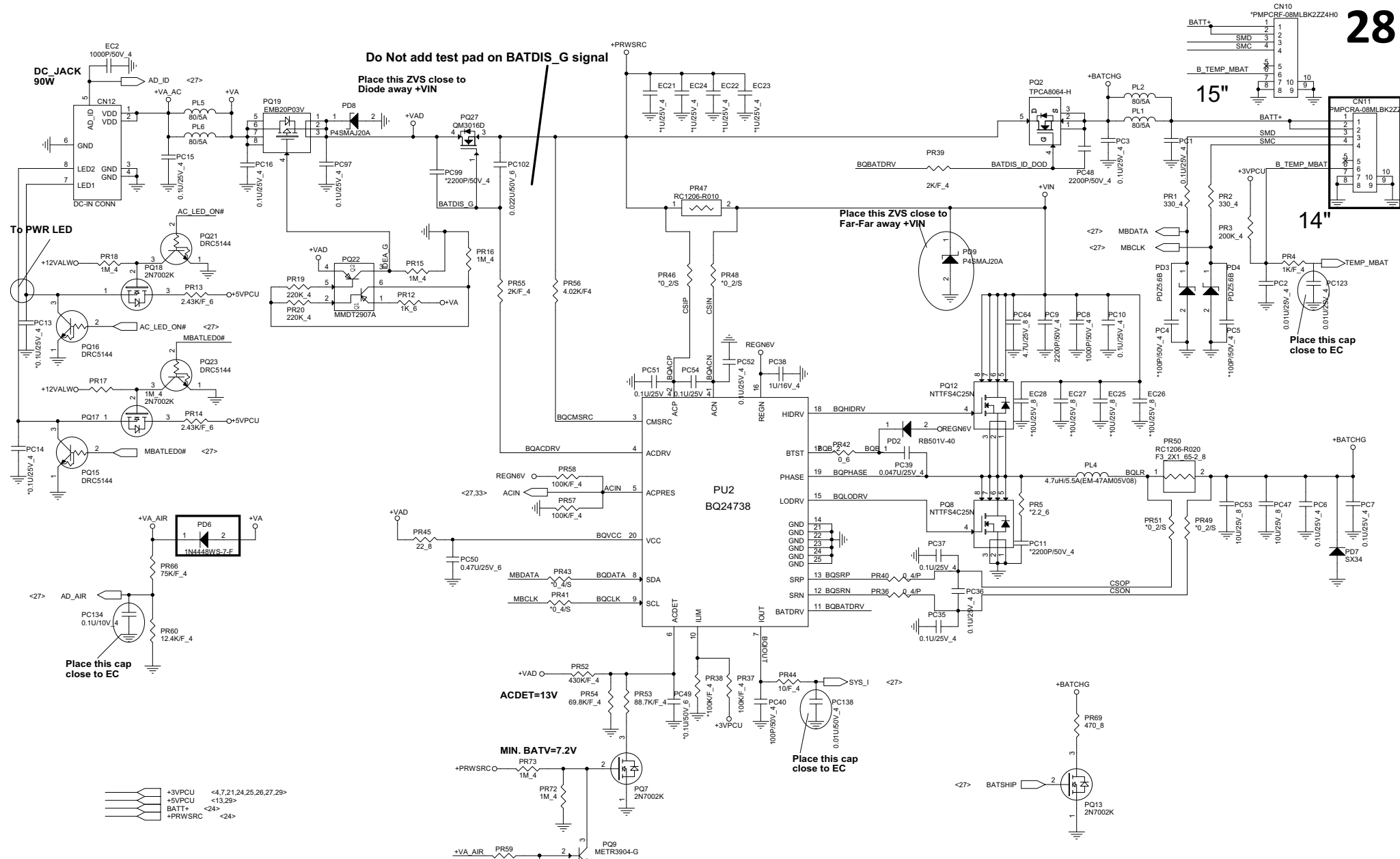


Need Change New PN



<6,7,8,9,10,11,12,13,14,15,16,17,19,20,21,22,23,24,25,26,32,33,34>
<4,7,21,24,25,26,28,29>

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15"

14"

Place this cap close to EC

Place this cap close to EC

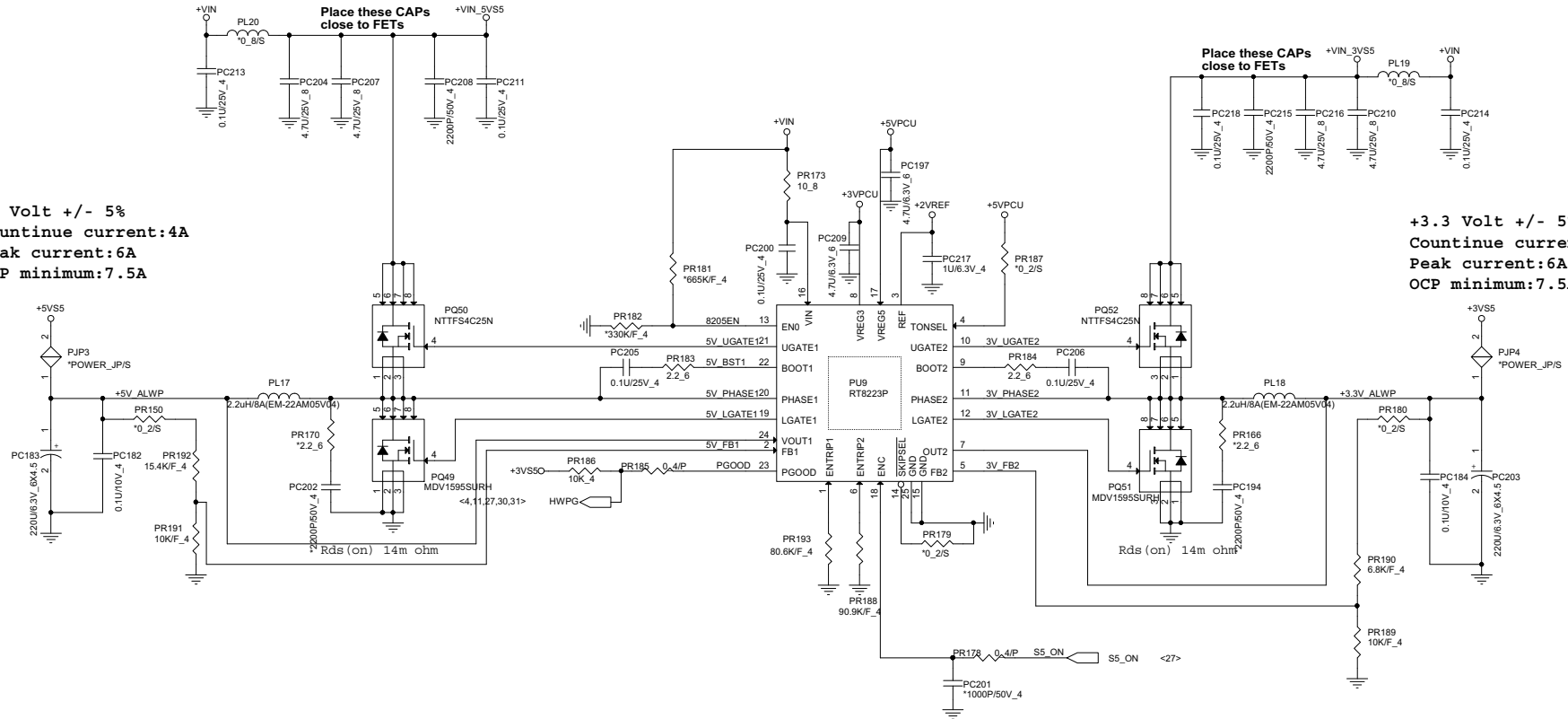
PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number Charger (BQ24738)	Rev 1A
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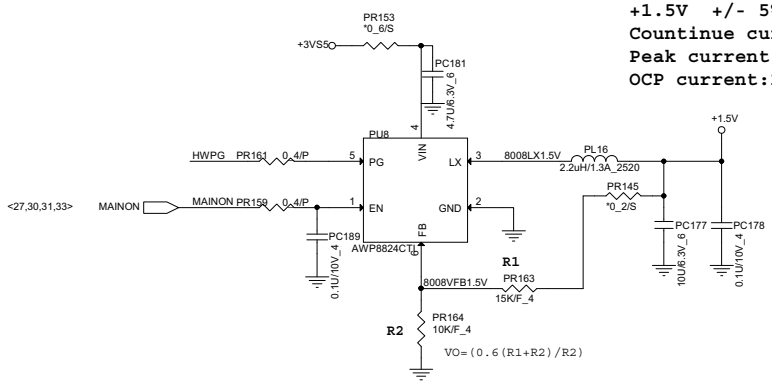
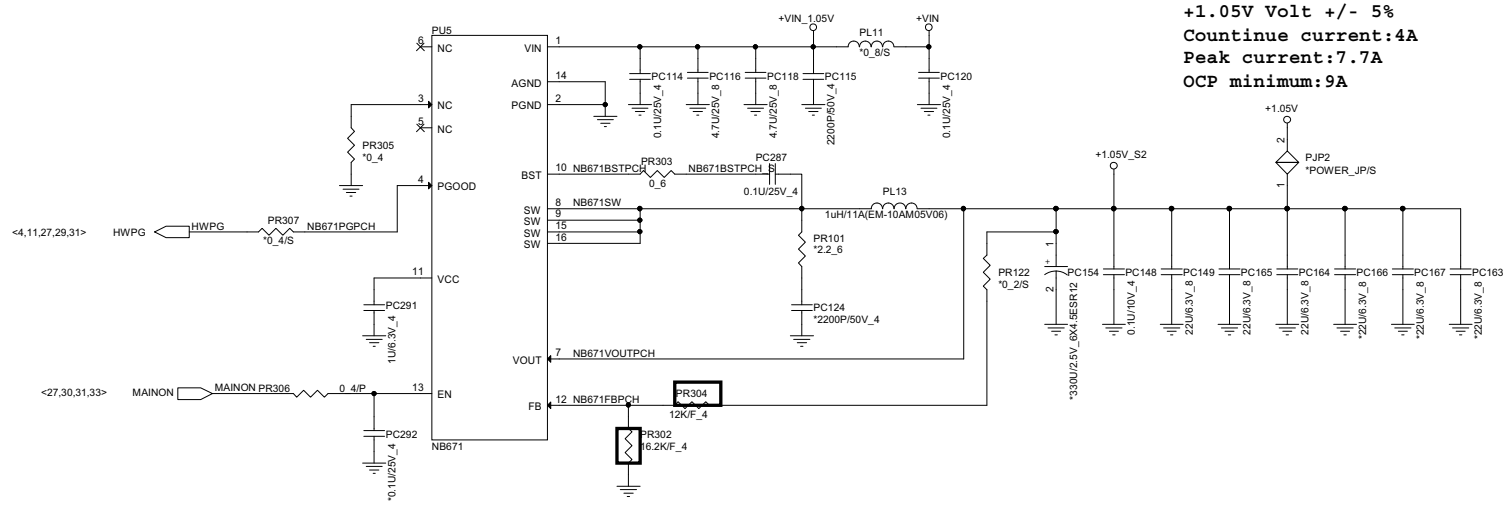
DC/DC +3VS5/+5VS5

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

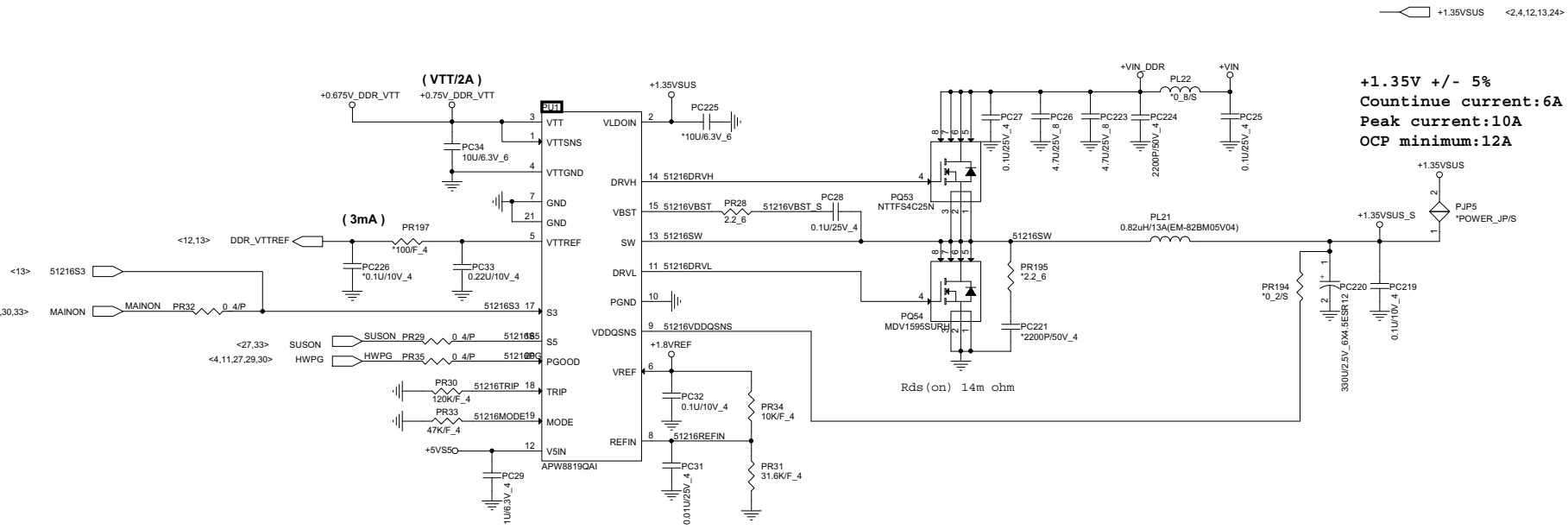


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	Size Custom	Document Number 3/5VPCU(RT8223P)
Date: Friday, April 26, 2013		Sheet 29 of 40



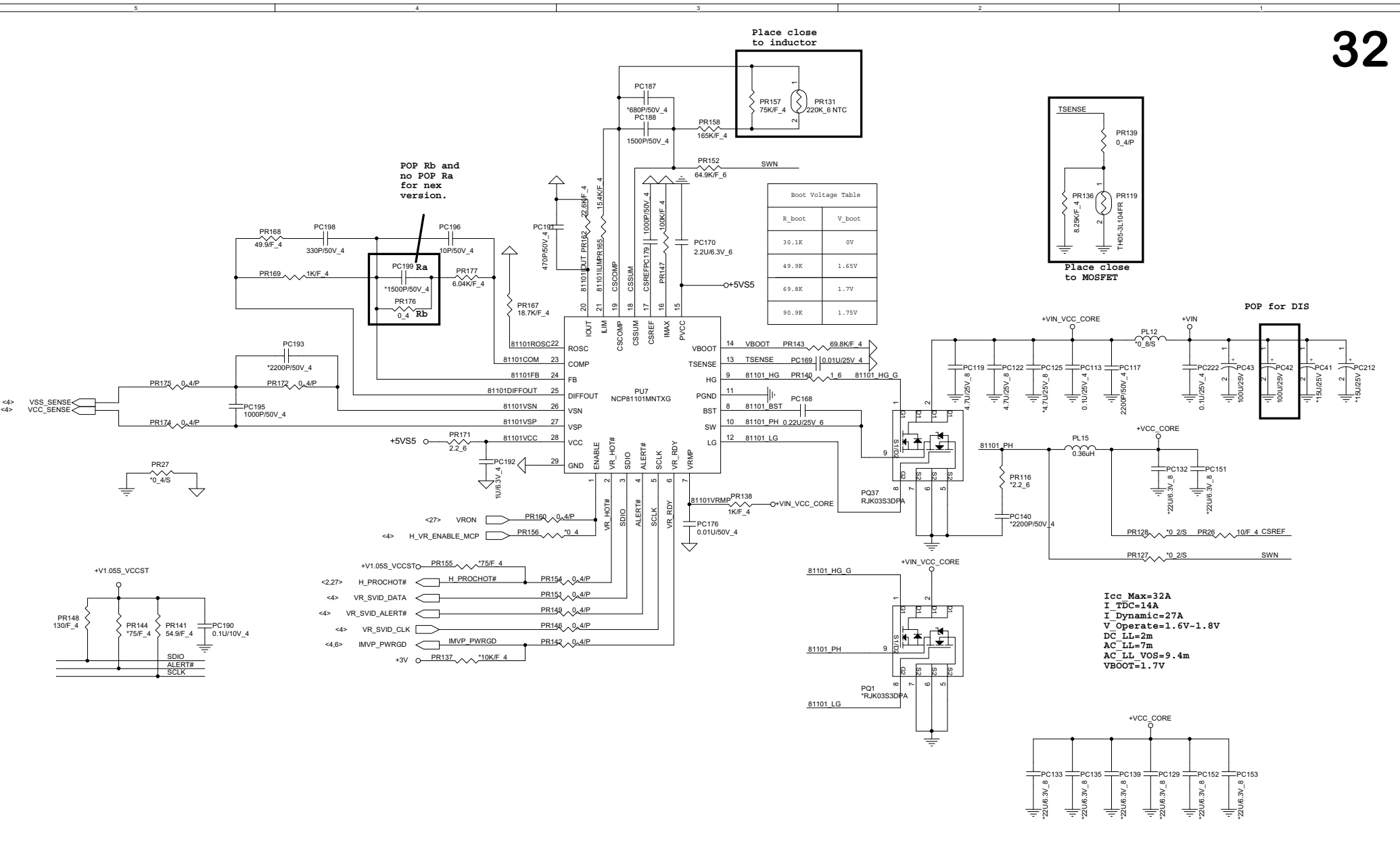
- +VIN <20,24,28,29,31,32,33,34,35,36>
- +3VS5 <6,9,10,11,24,26,29,33,35>
- +5VS5 <13,21,24,25,29,31,32,33,34,36>
- +5VPCU <13,28,29>


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	Quanta Computer Inc.		
Size Custom	Document Number +1.05V (NB671)/1.5V		
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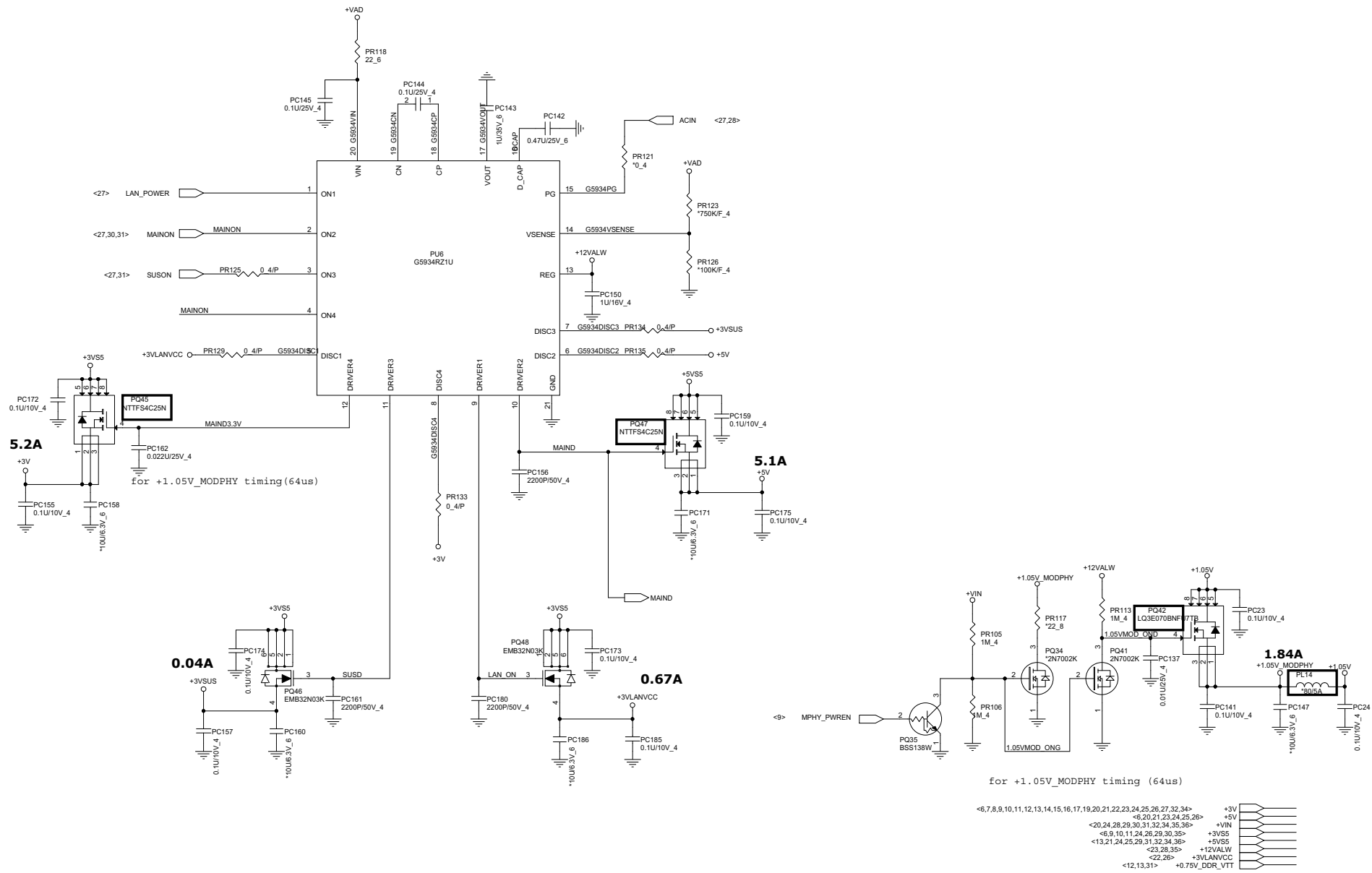
Size Custom	Document Number DDR3 (APW8819)	Rev 1A
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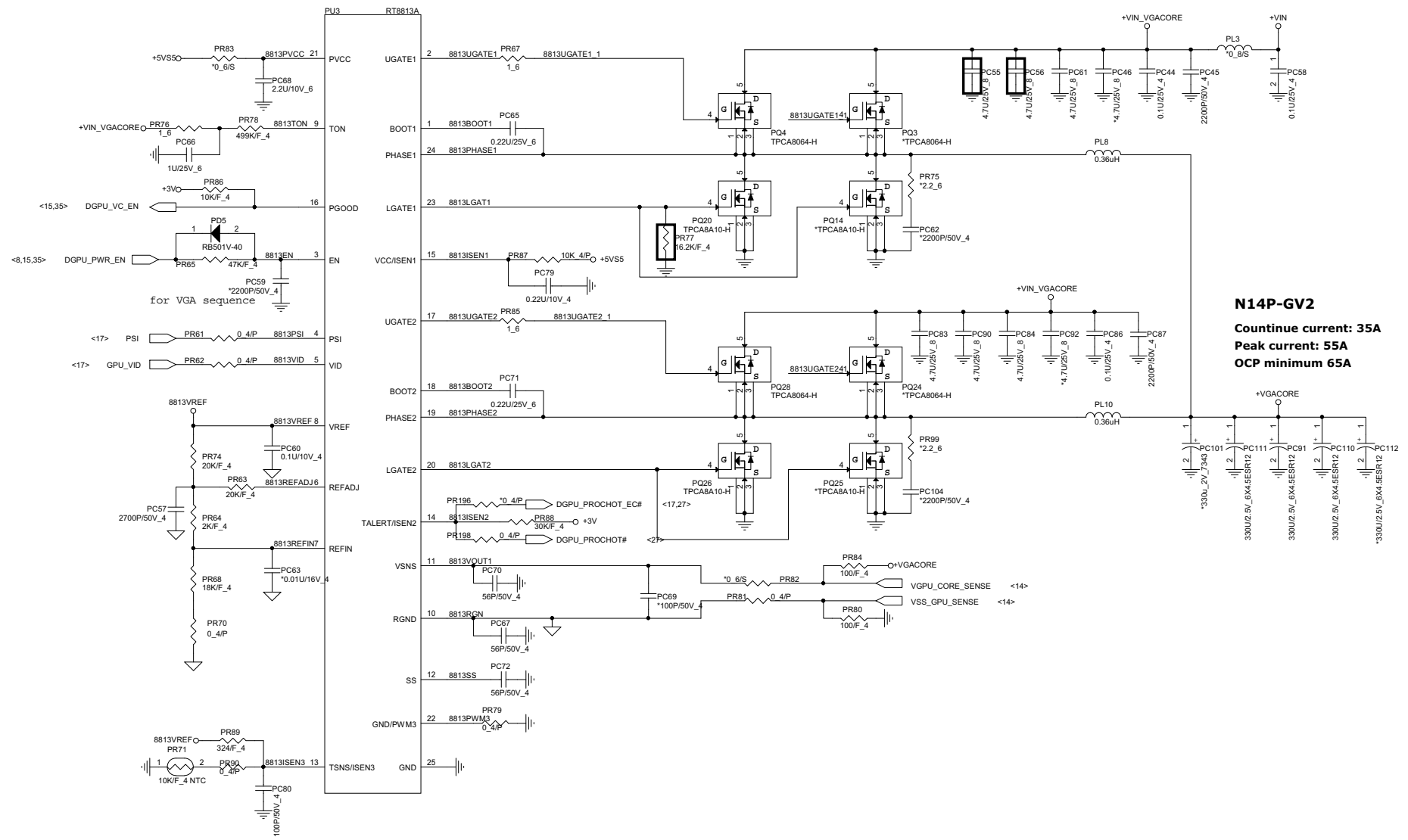
Size Custom Document Number CPU Core (NCP81101)JULT Rev 1A
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Quanta Computer Inc.

Size Custom	Document Number Dis-charge IC (SLG55448)	Rev 1A
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VGA Core

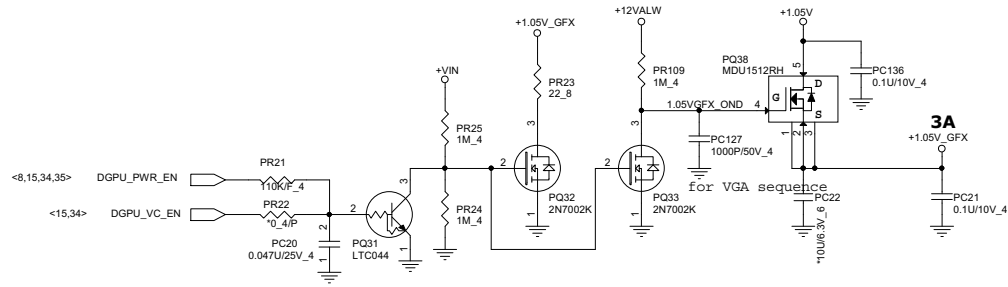
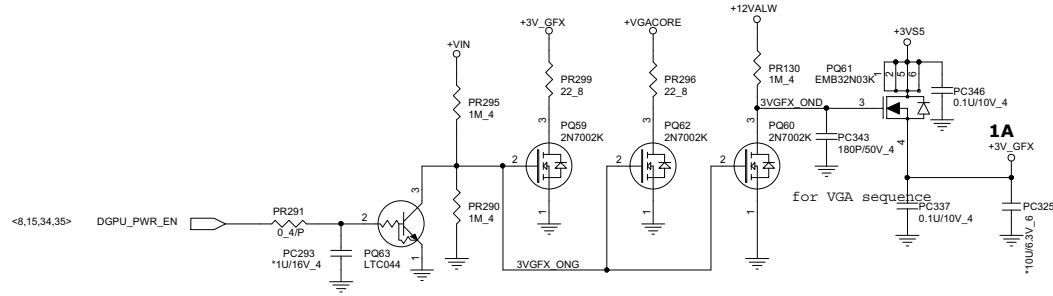



N14P-GV2
 Countinue current: 35A
 Peak current: 55A
 OCP minimum 65A

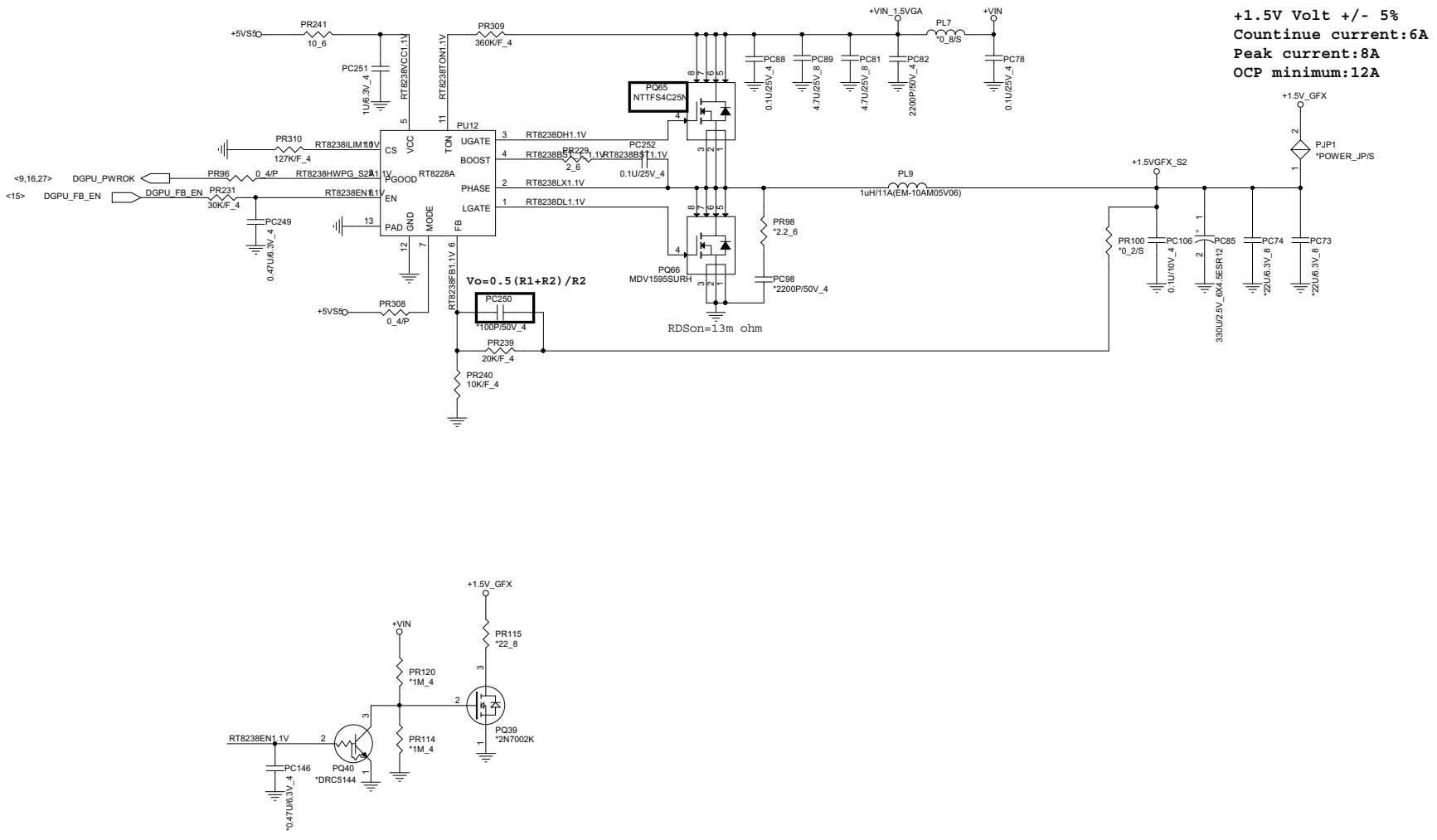



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Size Custom	Document Number +VGACORE (RT8813A)	Rev 1A
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	Size Custom	Document Number 1.05V_VGA/3V_VGA
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	Document Number +1.5V_VGA(RT8228)	Rev 1A
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USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON# (from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON# (from EC)
PORT3	NC	N/A
PORT4	NC	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON# (from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON# (from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON# (from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON (from EC)

SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	

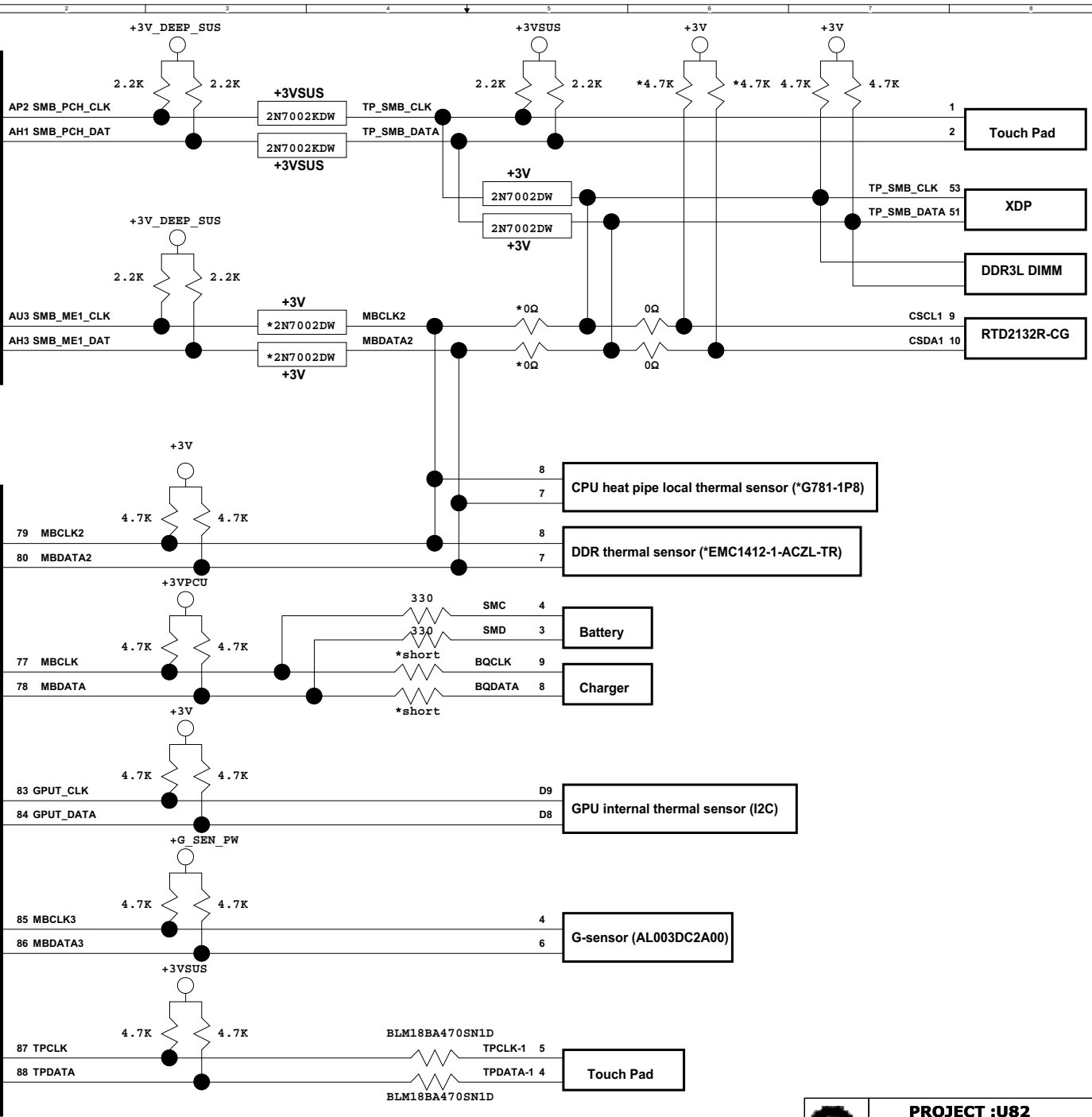


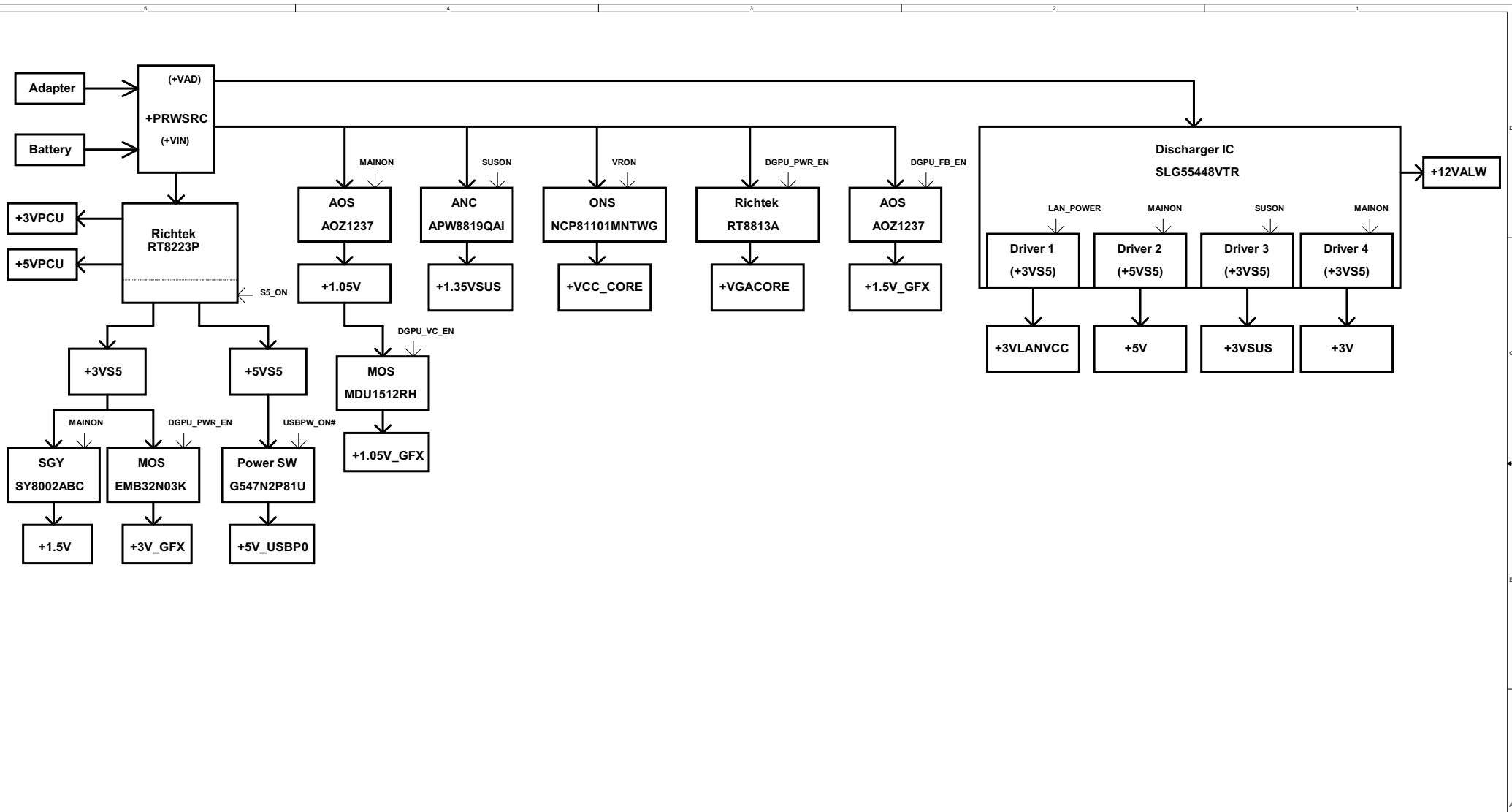
PROJECT :U82
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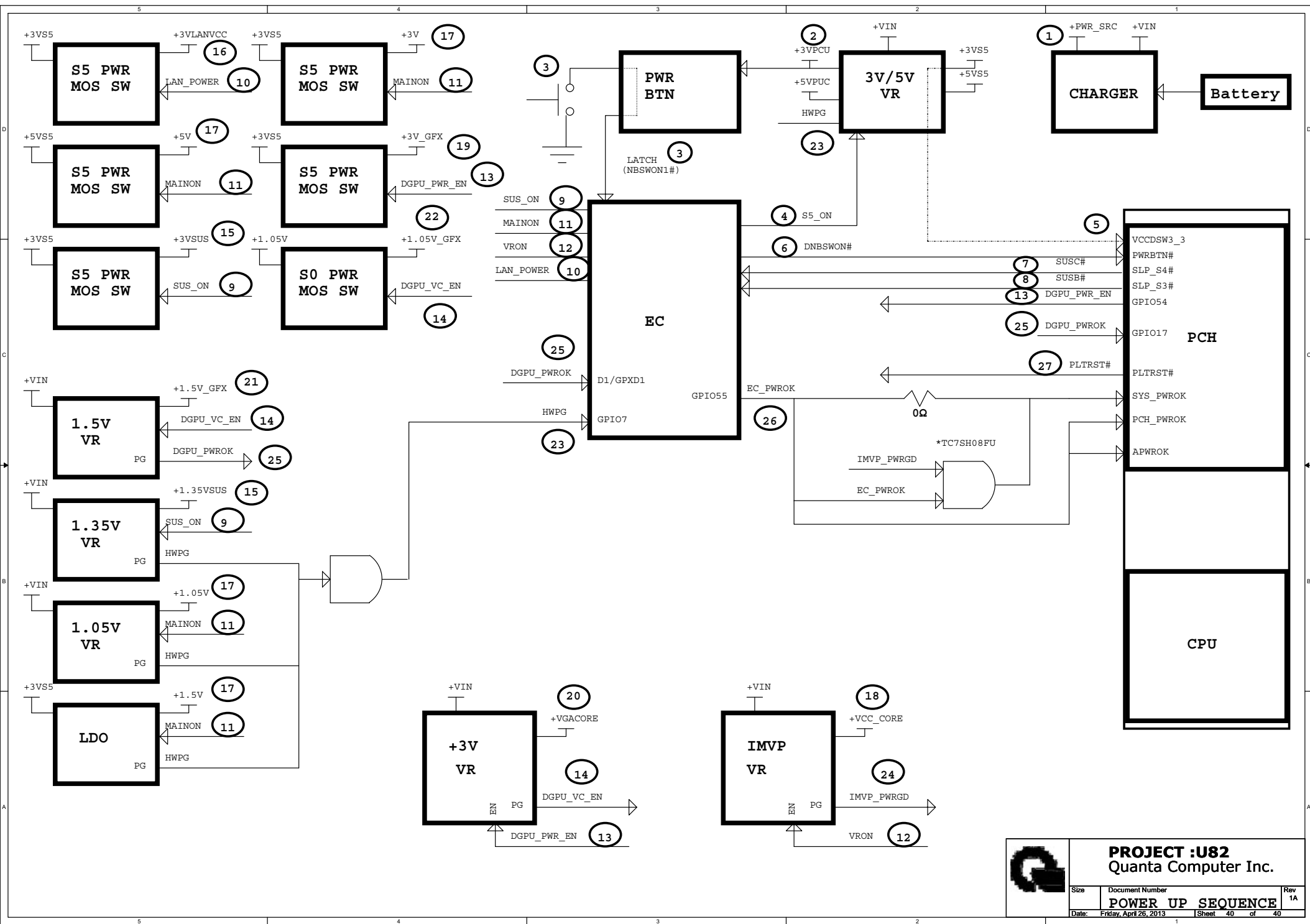
Size	Document Number	Rev 1A
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**Haswell
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