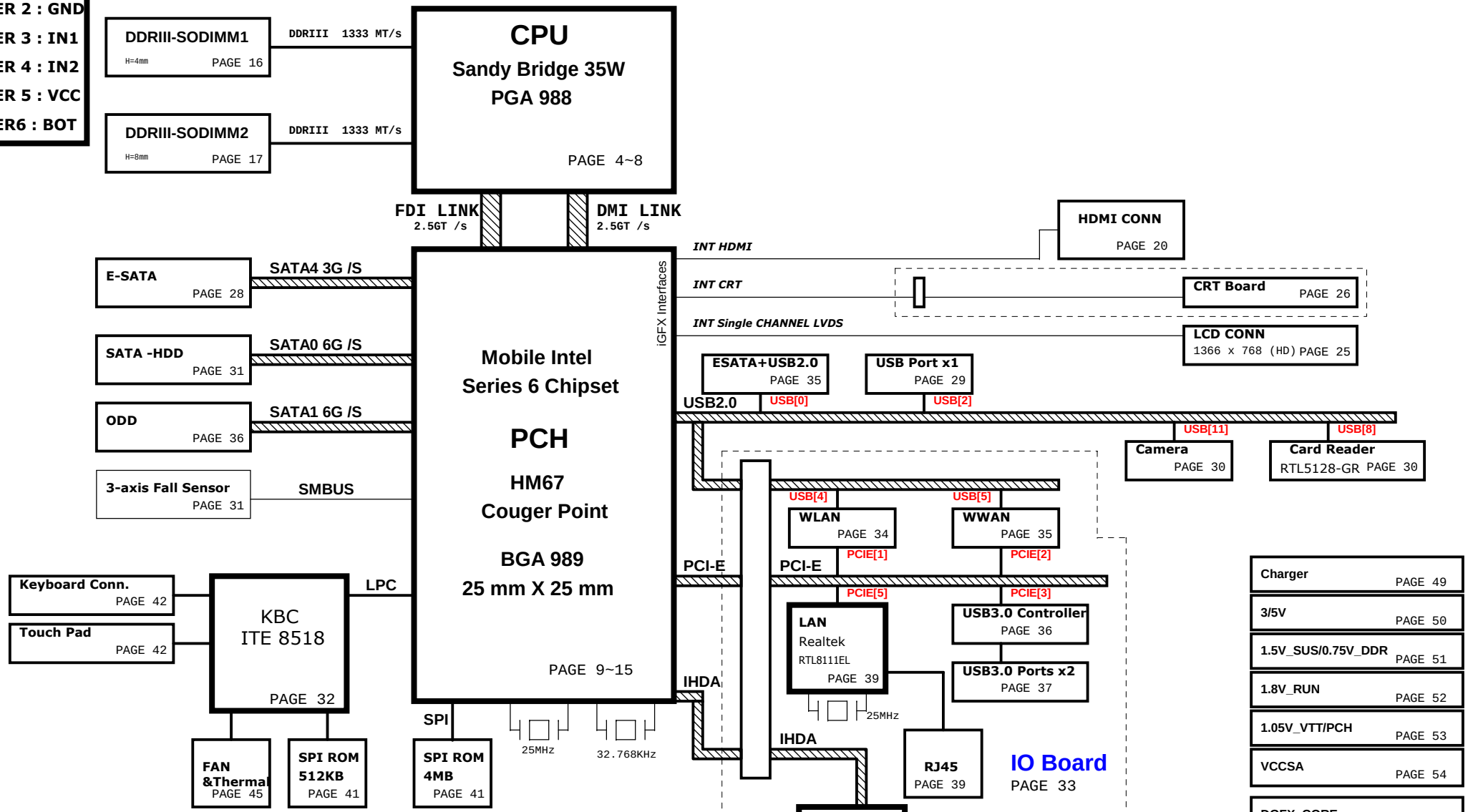
PCB STACK UP

6L UMA

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER6 : BOT

V02/R01 UMA BLOCK DIAGRAM



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PROJECT : V02/R01

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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power / State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

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Size	Document Number	Rev
	Power Rails	1A

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PROJECT : V02/R01

Size	Document Number	Rev
	BLANK	1A

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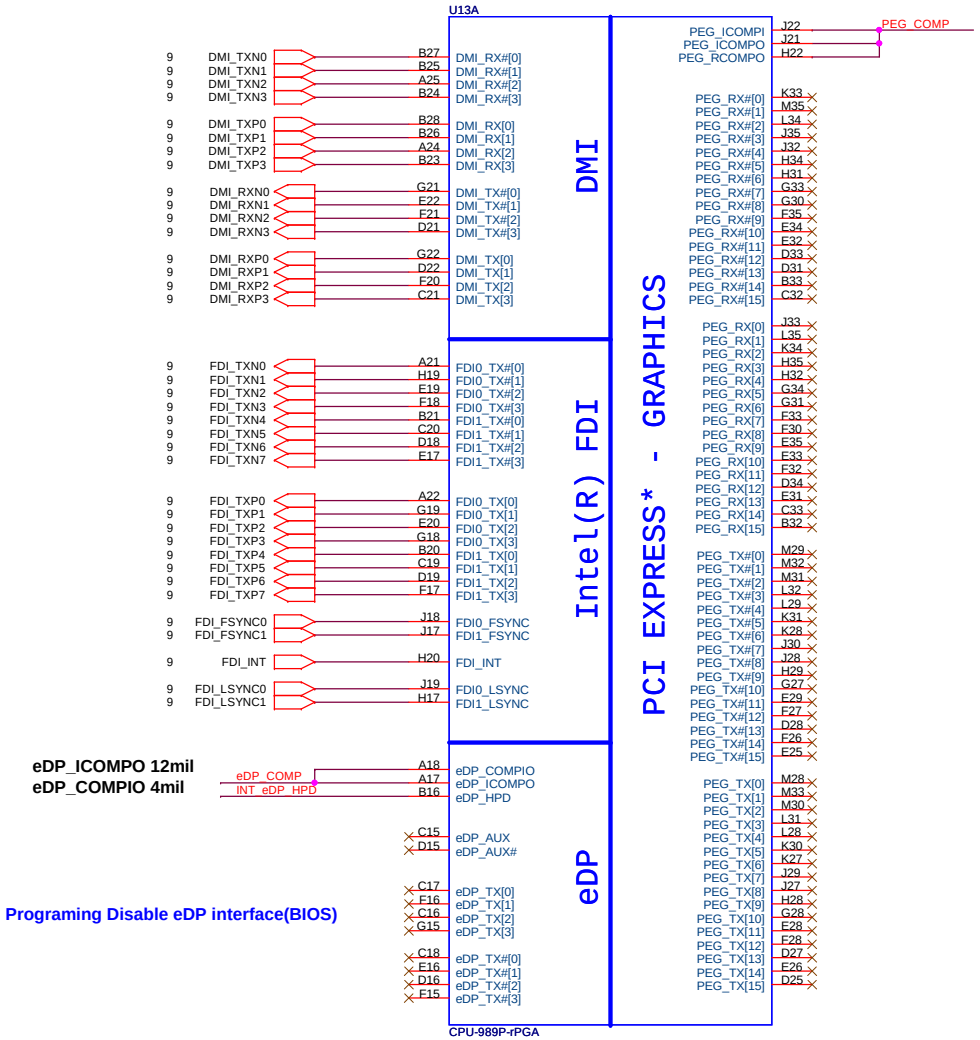
Sandy Bridge Processor (DMI,PEG,FDI)

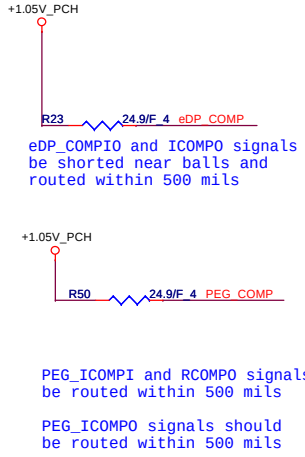


PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

eDP_ICOMPO 12mil
eDP_COMPIO 4mil

Programing Disable eDP interface(BIOS)

DP & PEG Compensation

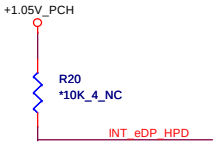


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

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	Sandy Bridge 1/5	1A
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Sandy Bridge Processor (CLK,MISC,JTAG)

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Over 130 degree C will drive low

Schematic C/L_v1.0, P56 (PU,PD 1k/J) (Intel and PD3)
Reserve (Intel confirm now)

SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

When MP, JTAG PU/PD resistor can be removed?
Need to confirm with Intel

CPU_PLTRST	R497,R228	U14,C314,R303,R302
Option1	POP	NC
Option2	NC	POP

IN	OUT
L	L
H	High-Z

Change OD part same with PDC

Copy from PDC

R8239, R8241 change to 5%

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

Follow #DG1.0 436735 P105
DDR Power Gating Topology

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration

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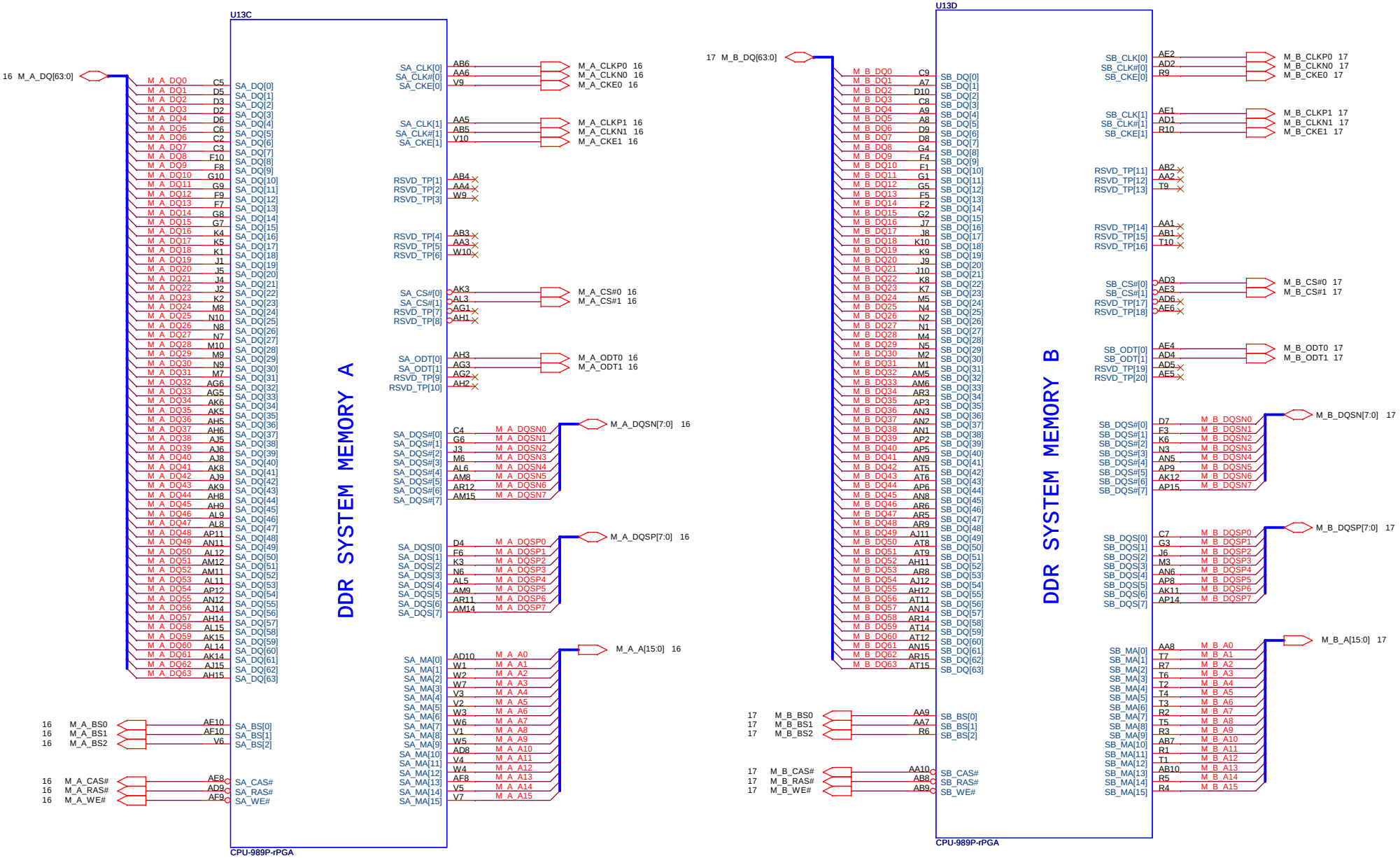
Sandy Bridge Processor (DDR3)



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	Sandy Bridge 3/5	1A

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 35W:55A
10uF x 24

CPU VTT
SNB 35W:8.5A
10F x12

CPU VGT
SNB 35W:22A
10uF x 12

CPU MCH
SNB 35W: 5A
10uF x 6

CPU SA
SNB35W: 6A
10uF x 3

CPU VCCPL
SNB 35W:3A
10uF x 1
1uF x 2

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
VREF
MISC
SENSE LINES
CPU-989P-rPGA

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

S3 Power reduce

Q3 FDMS7670 10A
Q4 *2N7002W-7-F_NC
Q5 2N7002W-7-F
Q7 2N7002W-7-F
Q6 *2N7002W-7-F_NC

Take care Q3509 Vgs(MAX)=2.5

Change R8281,R8285, R8704,R8329 to +/-5%
54.9 ohm has no 5%

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK — Close to VR — R299 54.9/F_4 — VR_SVID_CLK 40

Place PU resistor close to CPU — R293 130_4 — R297

SVID DATA — Close to VR — R295 130_4 — VR_SVID_DATA 40

Place PU resistor close to CPU — R300 75_4 — R298 43_4 — VR_SVID_ALERT# 40

SVID ALERT

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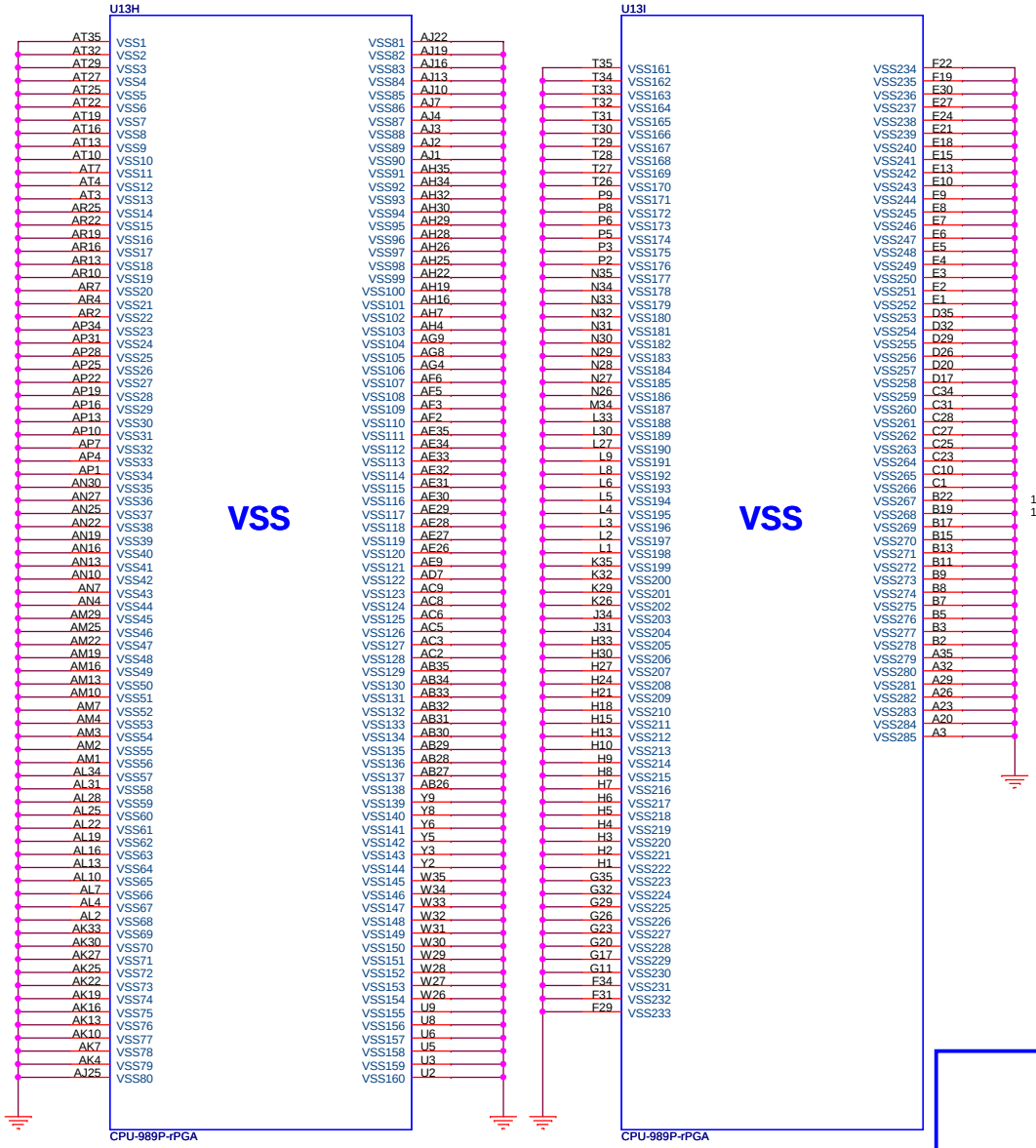
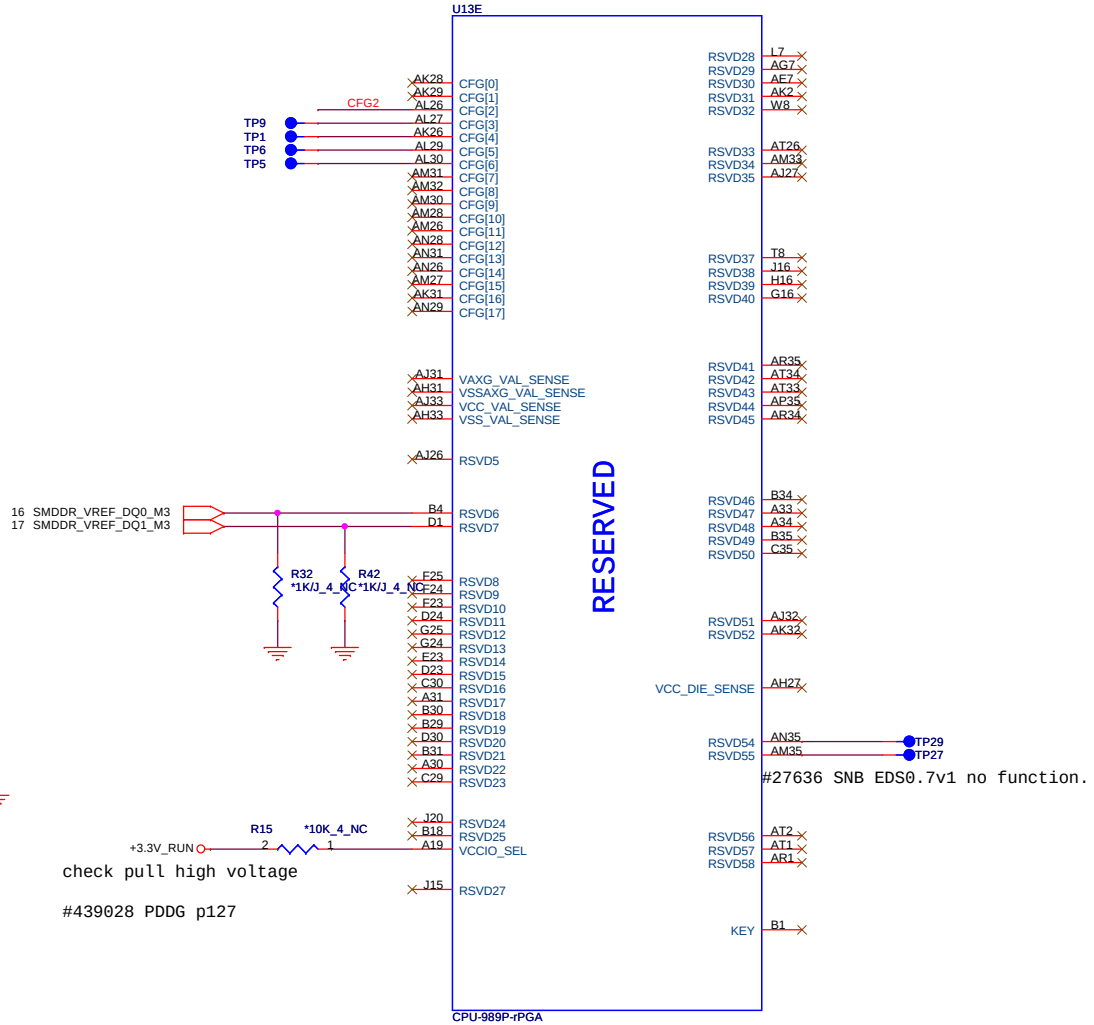
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



For rPGA socket, RSVD59 pin should be left NC

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R92 1K/F_4

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PROJECT : V02/R01

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	Sandy Bridge 5/5	1A
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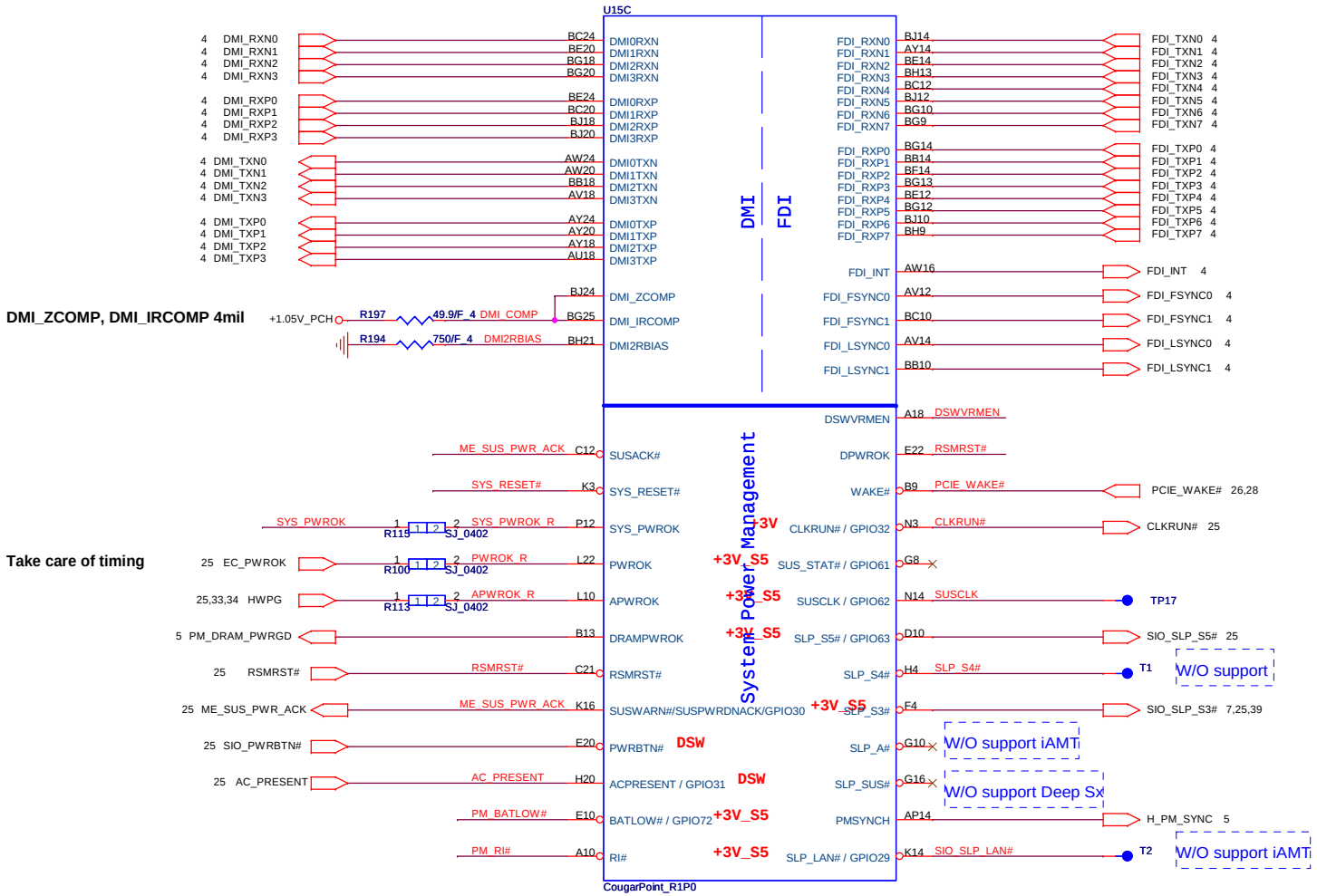
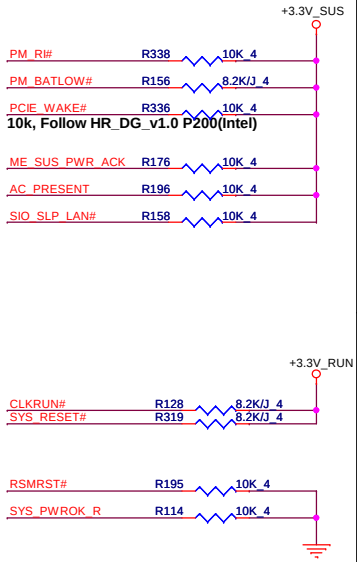
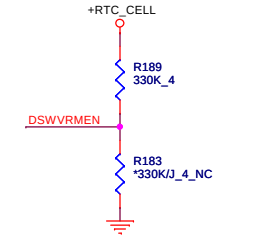
Cougar Point (DMI,FDI,PM)

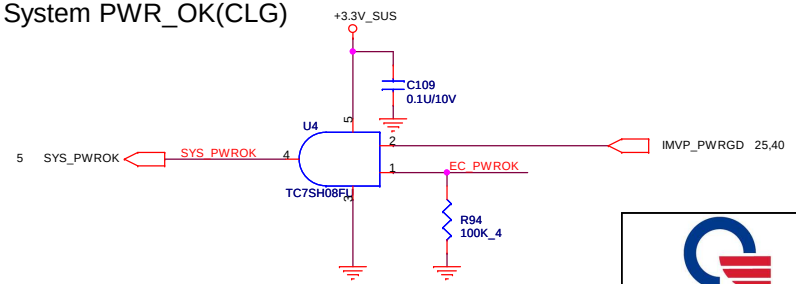


PCH Pull-high/low(CLG)





System PWR_OK(CLG)



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PROJECT : V02/R01		
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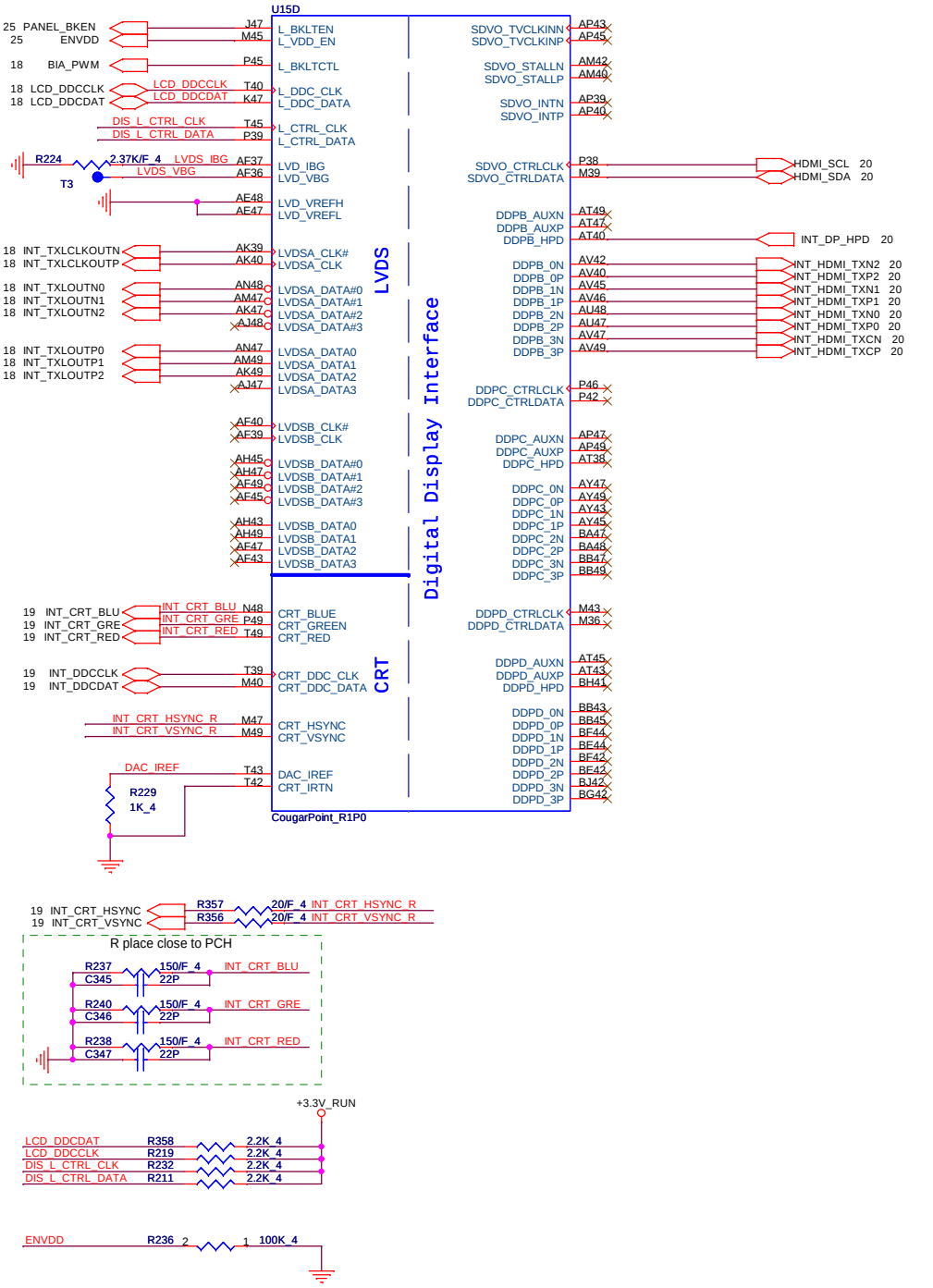
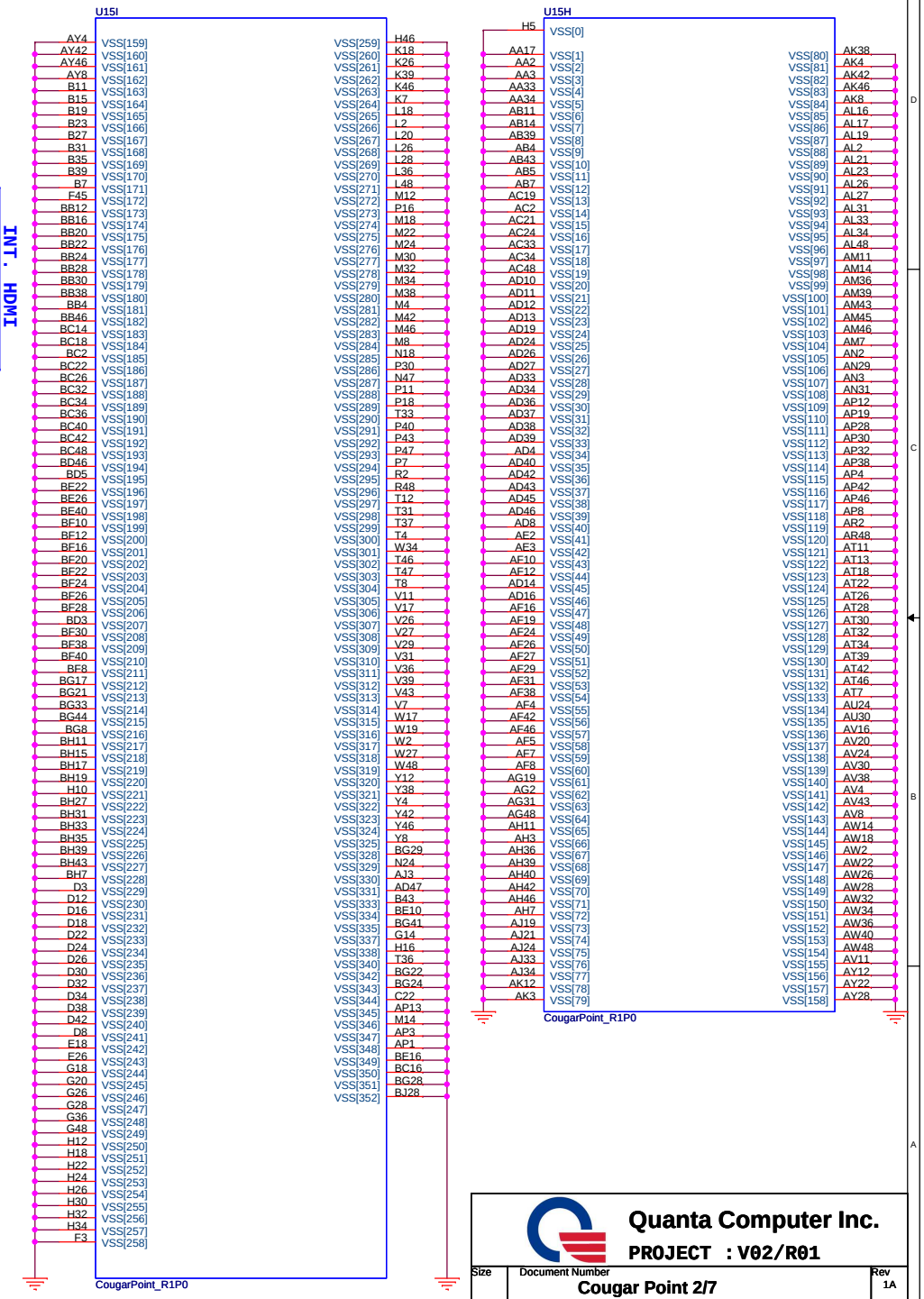
Cougar Point (LVDS,DDI)



Cougar Point (GND)



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PROJECT : V02/R01

Size	Document Number	Rev
	Cougar Point 2/7	1A

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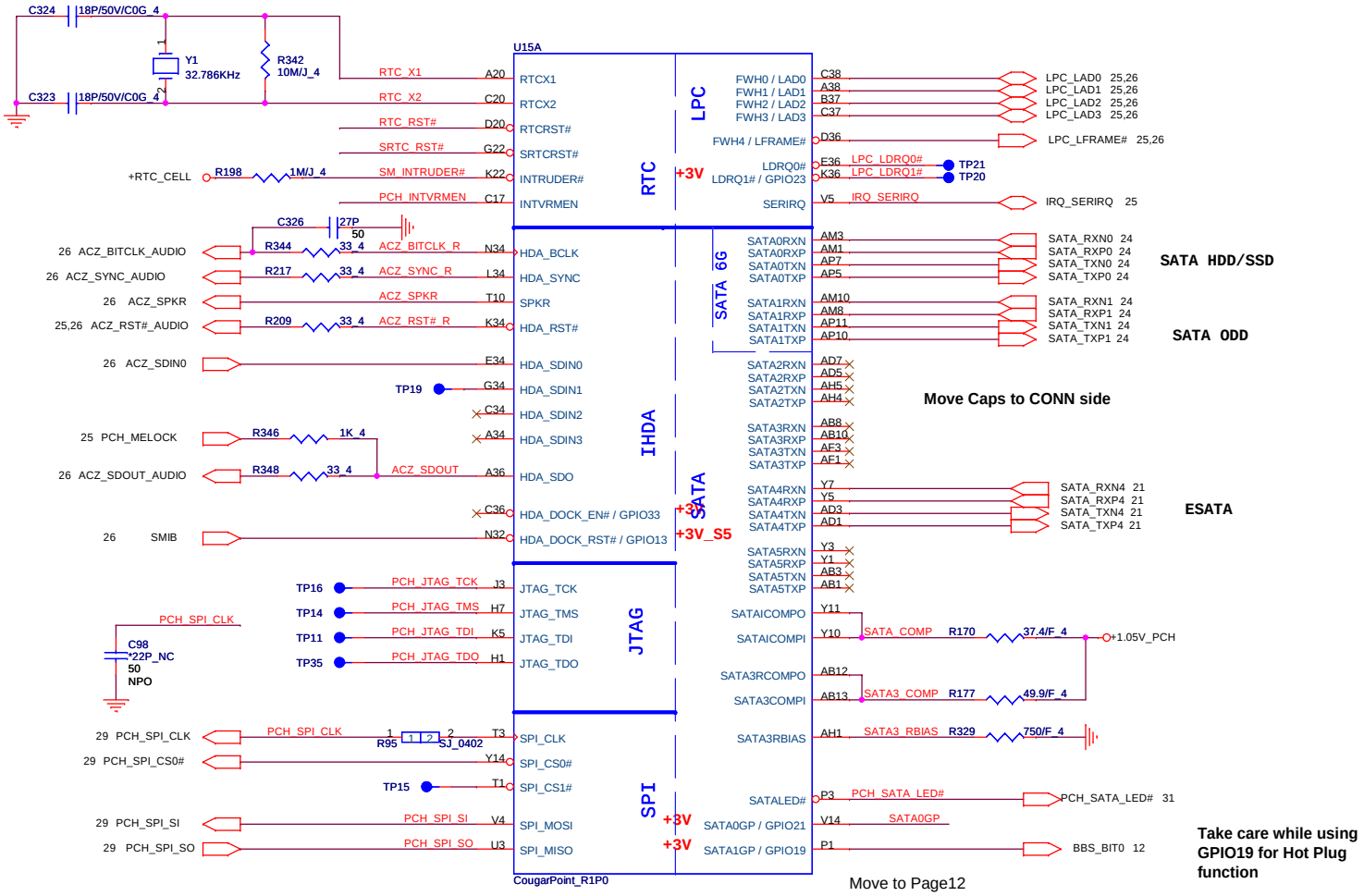
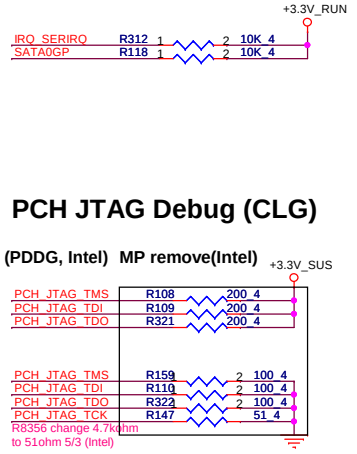
Cougar Point (HDA,JTAG,SATA)



PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R146 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R349 *1K_4_NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R181 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R212 1K_4 ACZ_SYNC_R

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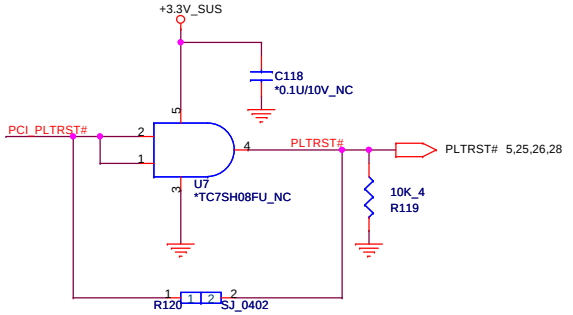
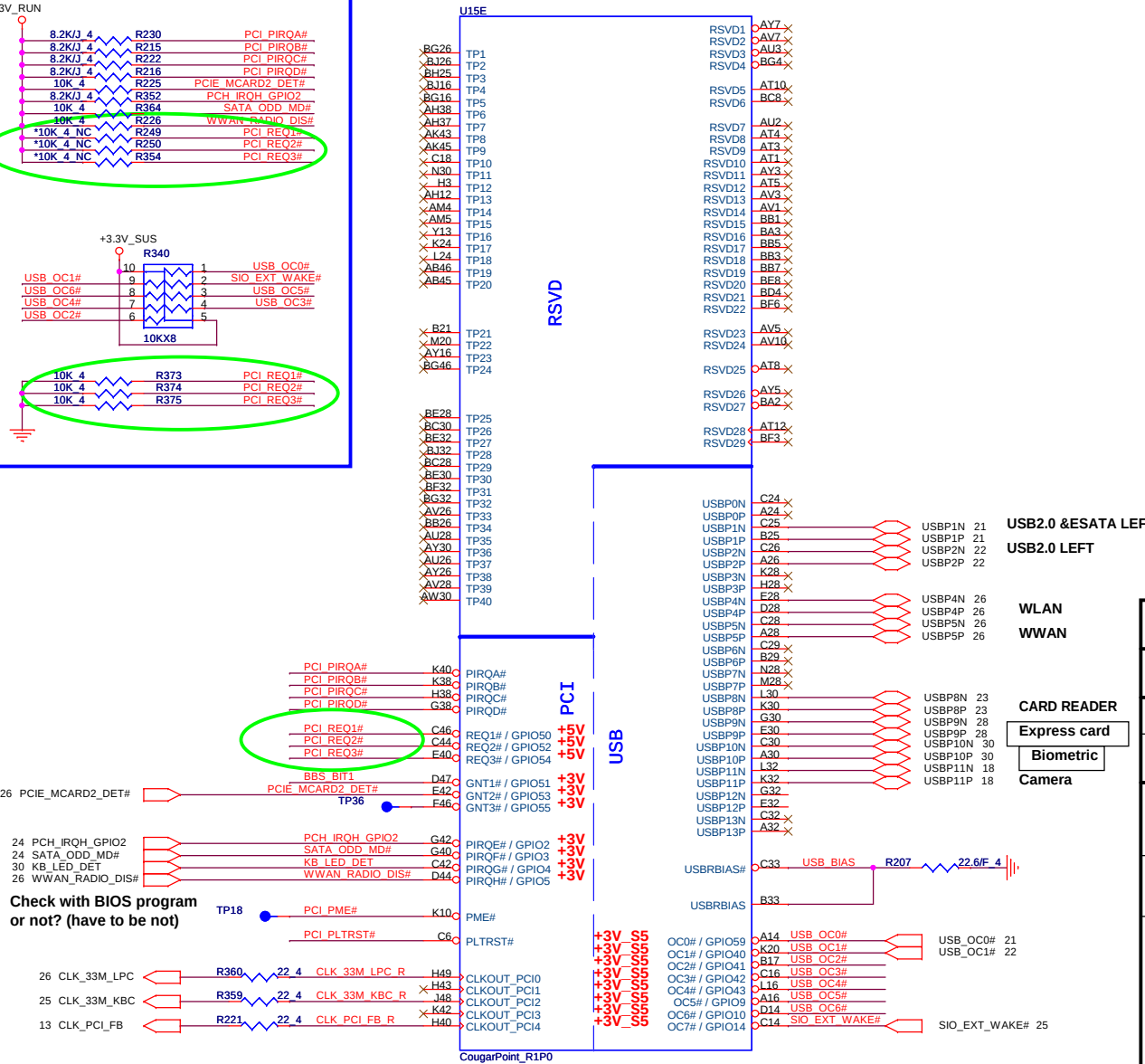
Cougar Point-M (PCI,USB,NVRAM)

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)





Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm

Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]

CheckList_1.0 p58; HR_v1.0 p450

Quanta Computer Inc.
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	Cougar Point 4/7	1A
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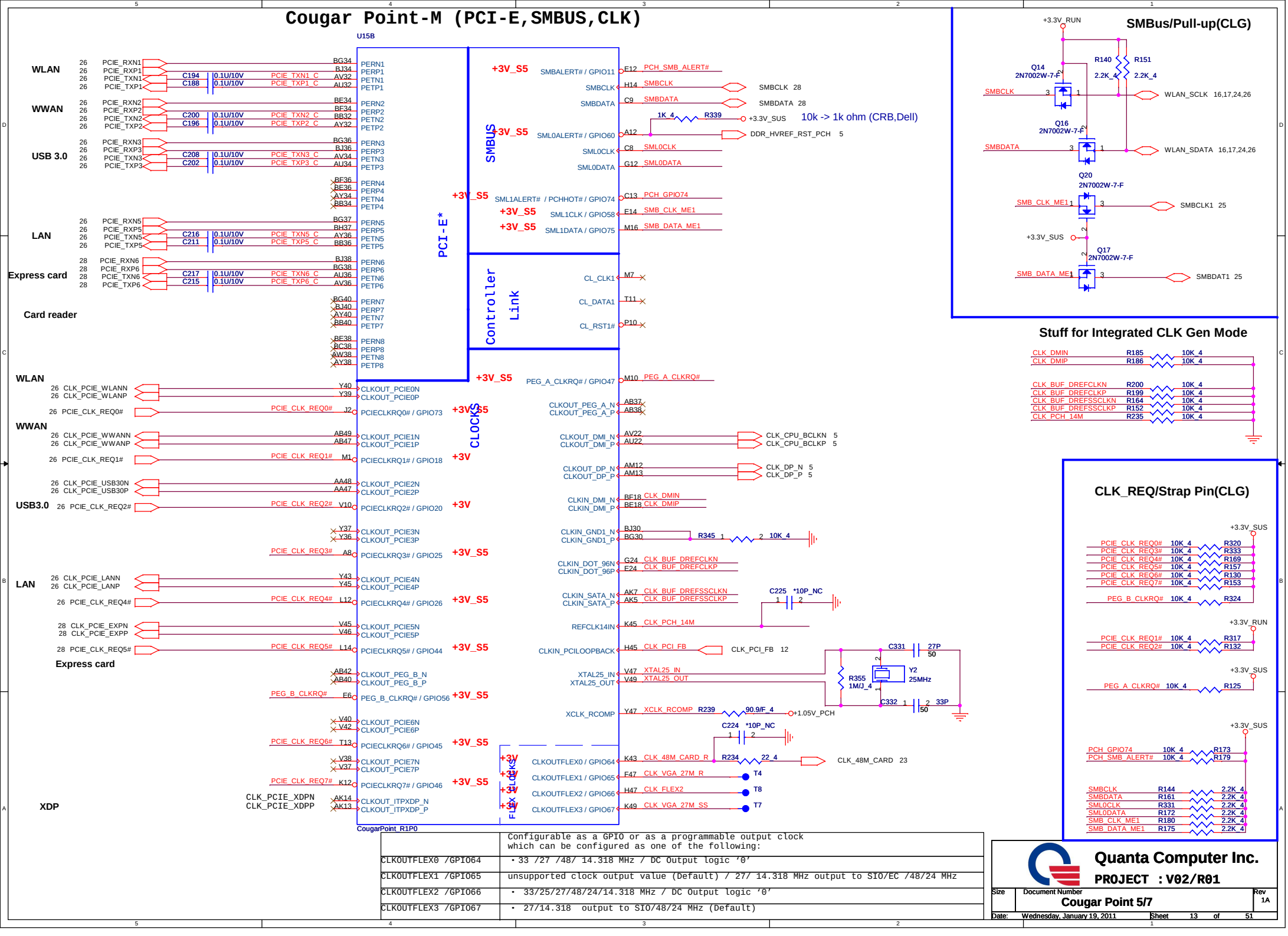
Cougar Point-M (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

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Size	Document Number	Rev
	Cougar Point 5/7	1A
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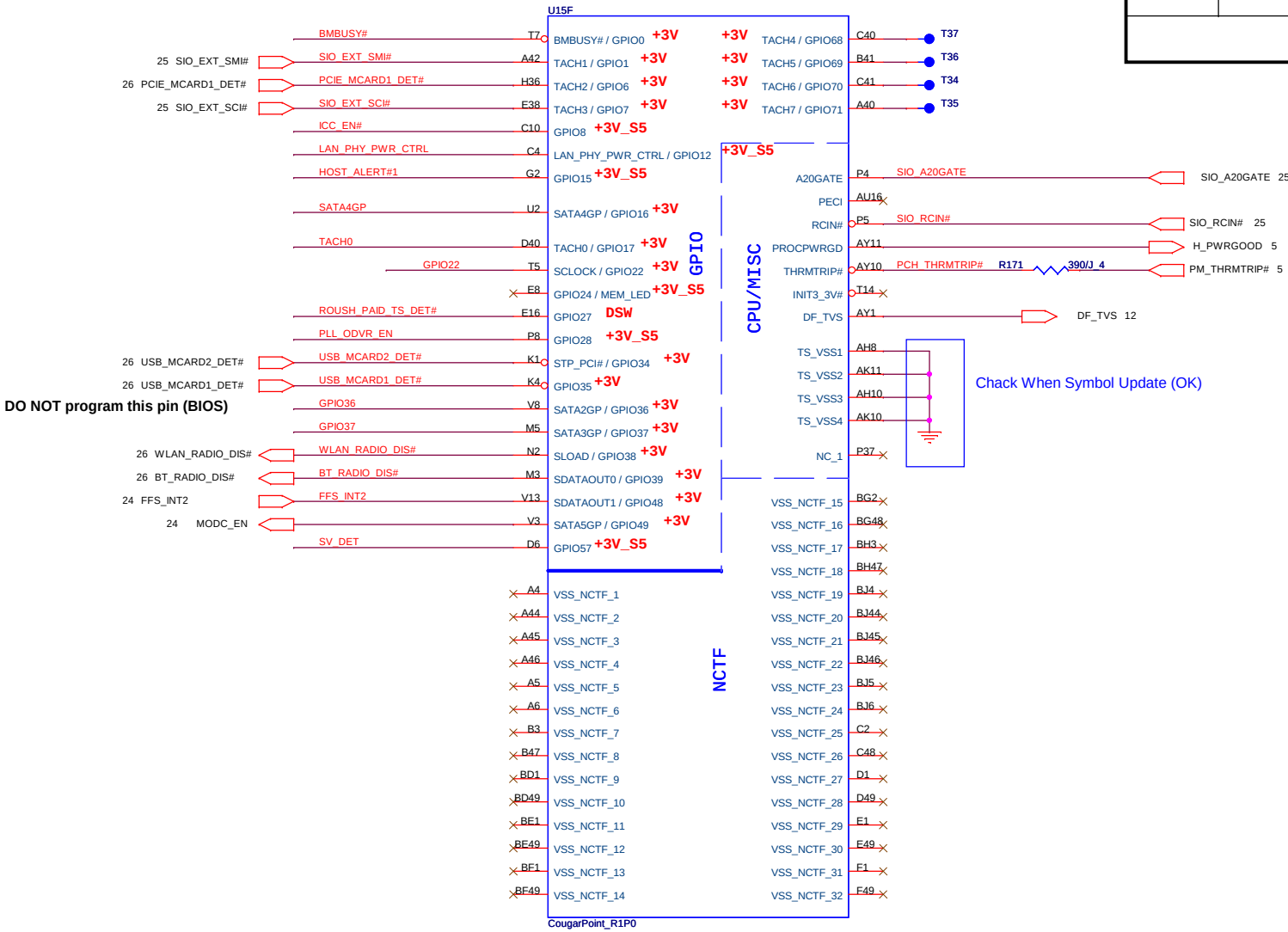
Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R174 *1K_4_NC PLL_ODVR_EN



DO NOT program this pin (BIOS)

Chack When Symbol Update (OK)

Ask Intel, what's the function?

Add Description in EC GPIO table (keyboard controller reset)

GPIO Pull-up/Pull-down(CLG)

+3.3V_SUS
ICC_EN# R337 10K_4
LAN_PHY_PWR_CTRL R325 10K_4
FFS_INT2 R131 *10K_4_NC

+3.3V_RUN
SIO_EXT_SMI# R227 10K_4
SIO_EXT_SCI# R218 10K_4
SIO_A20GATE R129 10K_4
SIO_RCIN# R148 10K_4
USB_MCARD2_DET# R318 10K_4
USB_MCARD1_DET# R112 10K_4
BT_RADIO_DIS# R127 10K_4
GPIO22 R143 10K_4
SATA4GP R116 10K_4
PCIE_MCARD1_DET# R347 10K_4
GPIO37 R111 *10K_4_NC
TACH0 R220 10K_4
FFS_INT2 R244 *10K_4_NC

ROUSH_PAID_TS_DET# R187 10K_4

Can be del

+3.3V_SUS
R149 *10K_4_NC SV_DET R150 100K_4

Have to Reserve

+3.3V_SUS
HOST_ALERT#1 R323 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite	
Low = Disable (Default)	
High = Enable	

GPIO36 R133 200K +3.3V_RUN

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY# R117 10K_4 +3.3V_RUN

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

MFG-TEST

WLAN_RADIO_DIS# R316 10K_4 +3.3V_RUN

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	Cougar Point 6/7	1A
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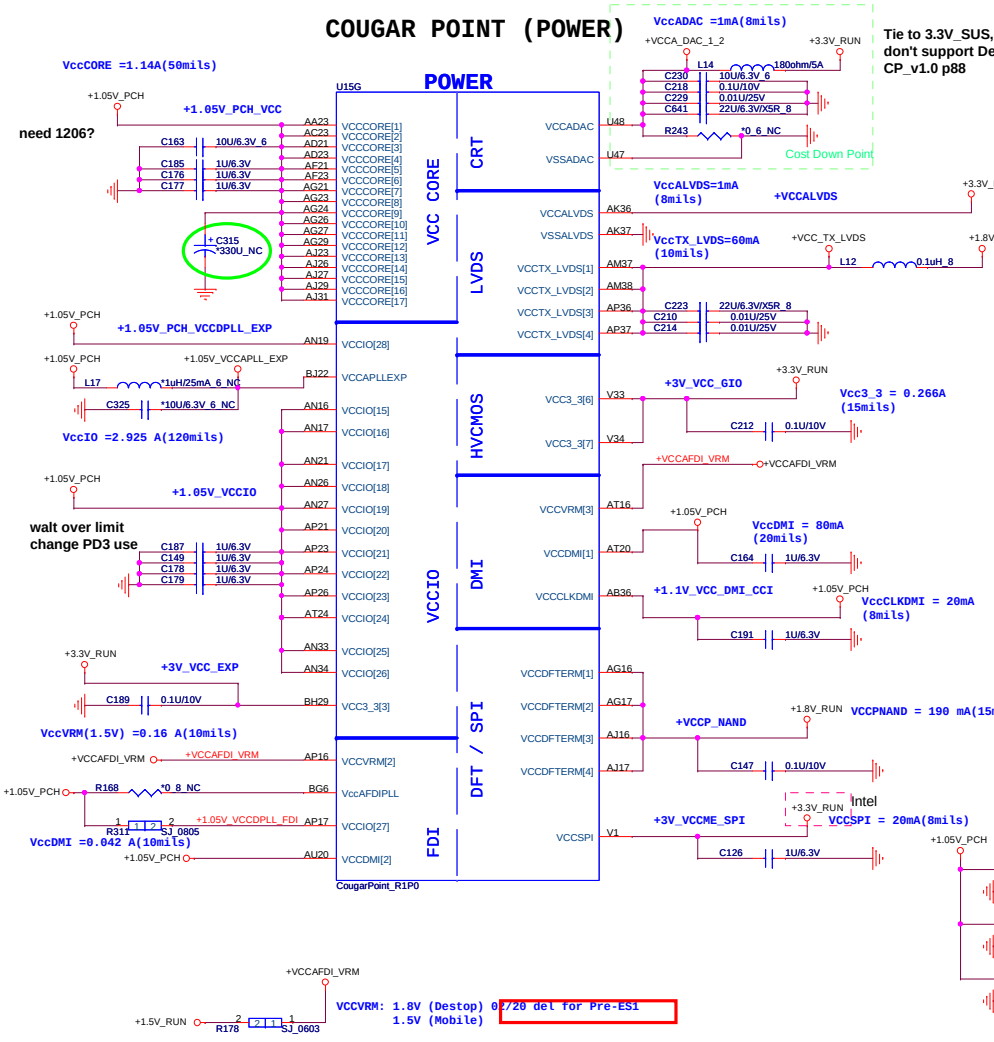
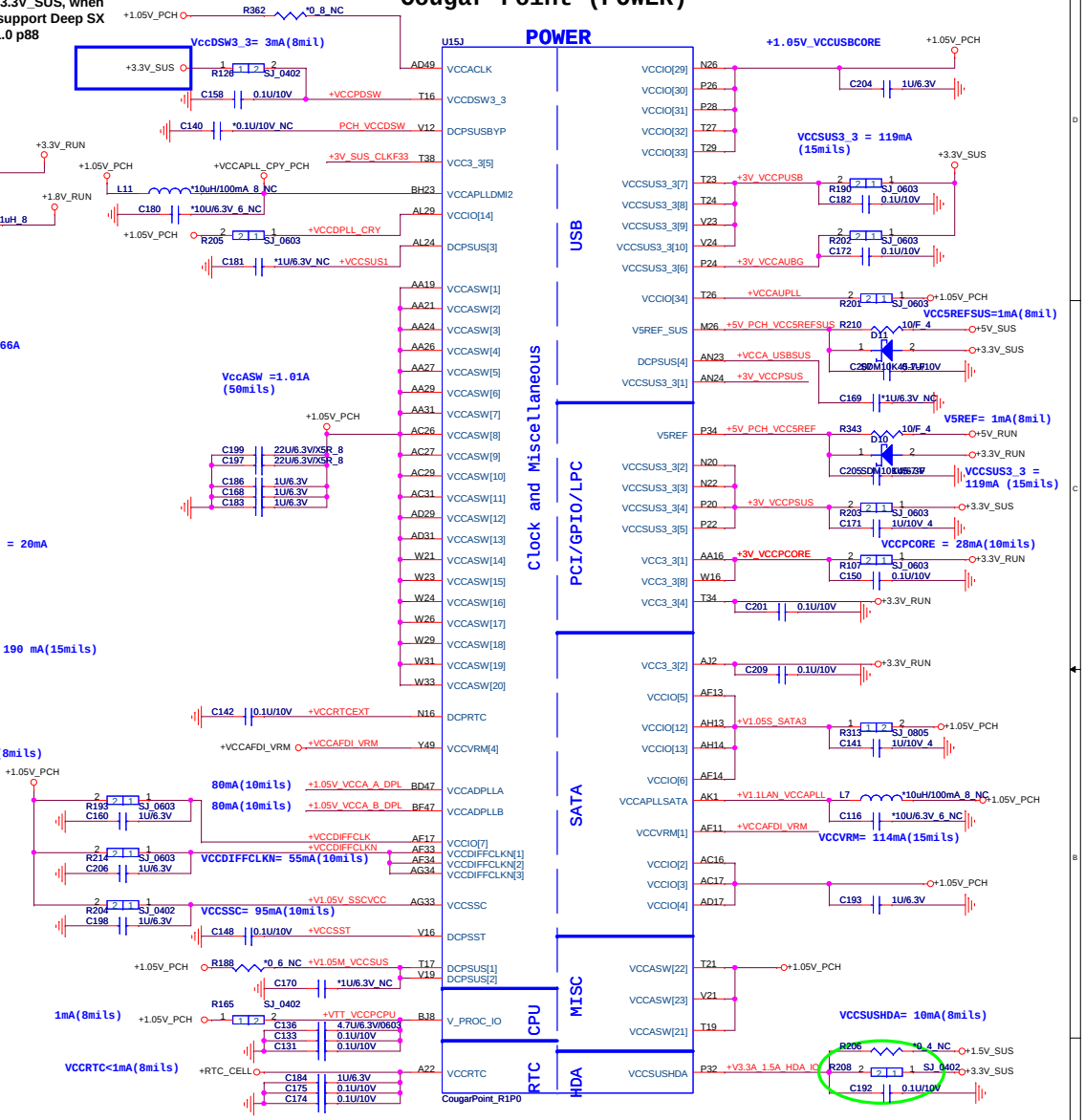
COUGAR POINT (POWER)



Cougar Point (POWER)



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H=8mm,RVS

SO-DIMMA_SPD Address is 0XA0
SO-DIMMA_TS Address is 0X30
Still Support?

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

S3 Power reduce

M1 VREF

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603 11/6
It can cost down 30%

For RF noise

For RF noise

Quanta Computer Inc.	PROJECT : V02/R01
Size	Document Number: DDR3 DIMM-0 — Rev: 1A
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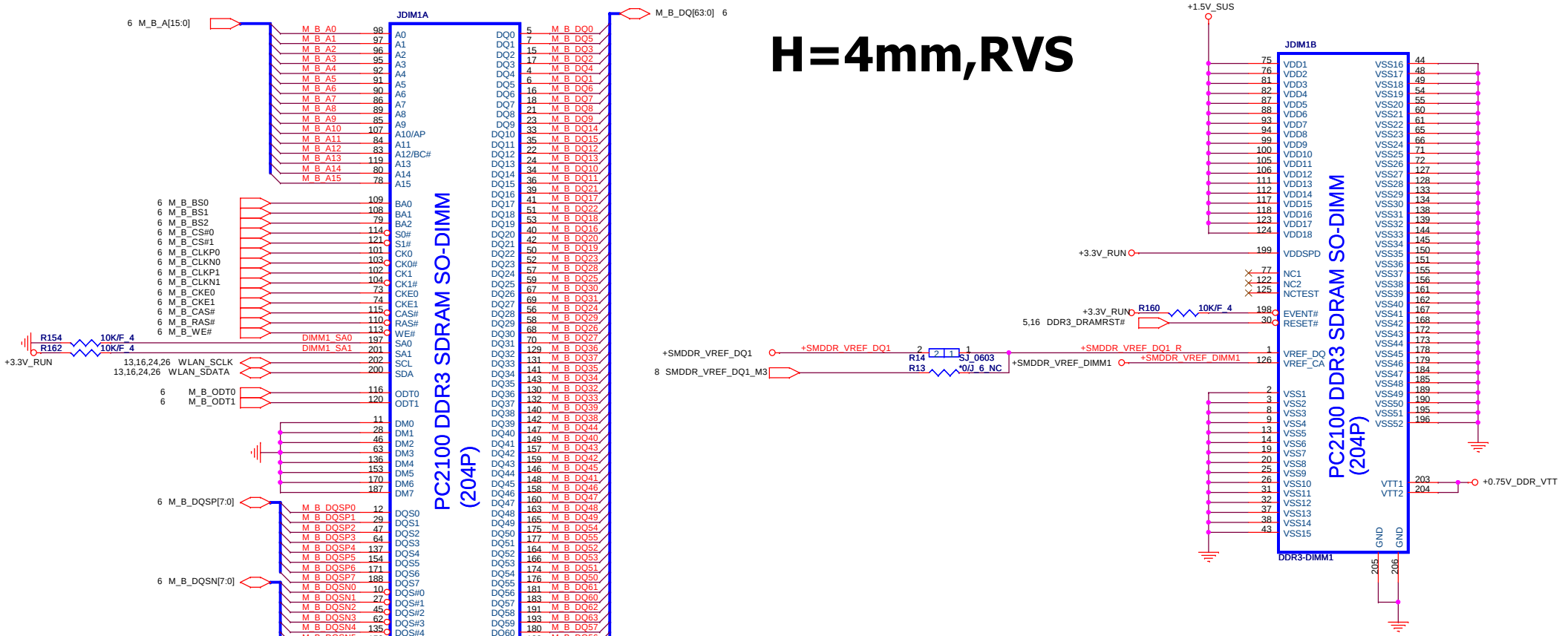
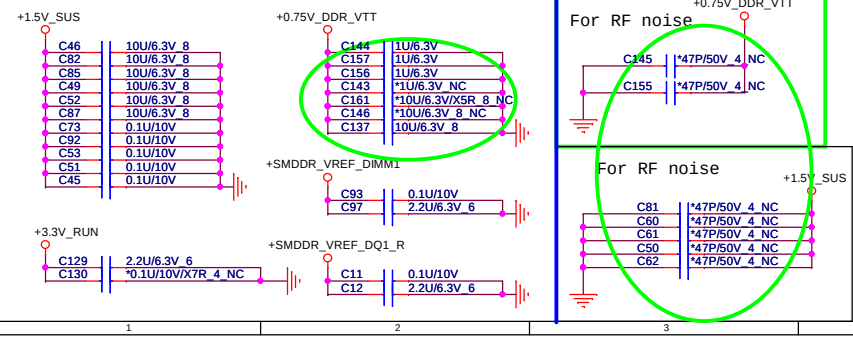
H=4mm,RVS

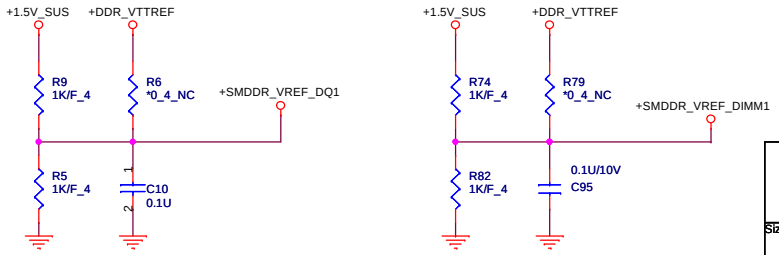


Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



M1 VREF



Quanta Computer Inc.
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Size	Document Number	Rev
	DDR3 DIMM-1	1A
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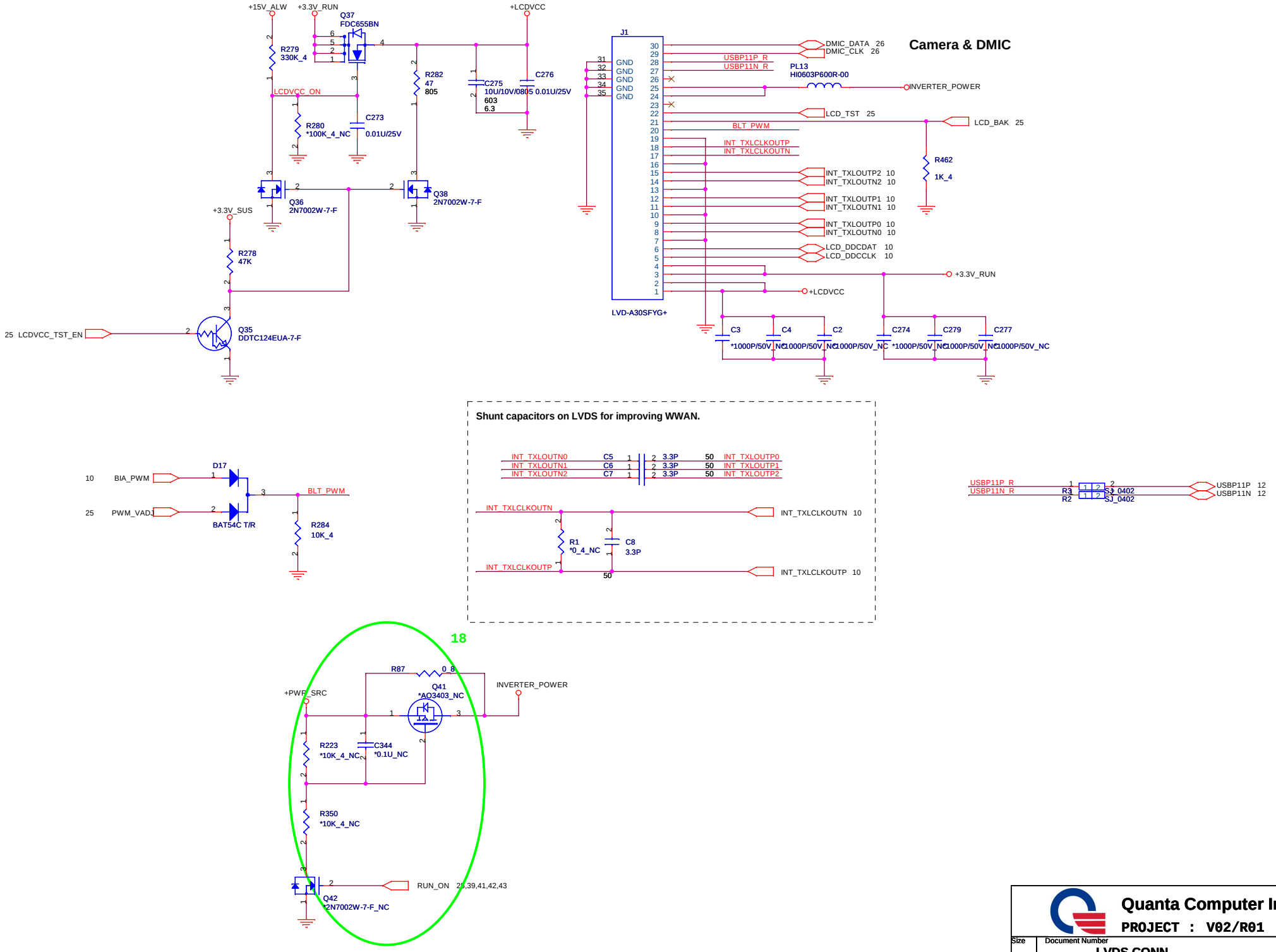

Quanta Computer Inc.

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Size	Document Number	Rev
	LVDS CONN	1A
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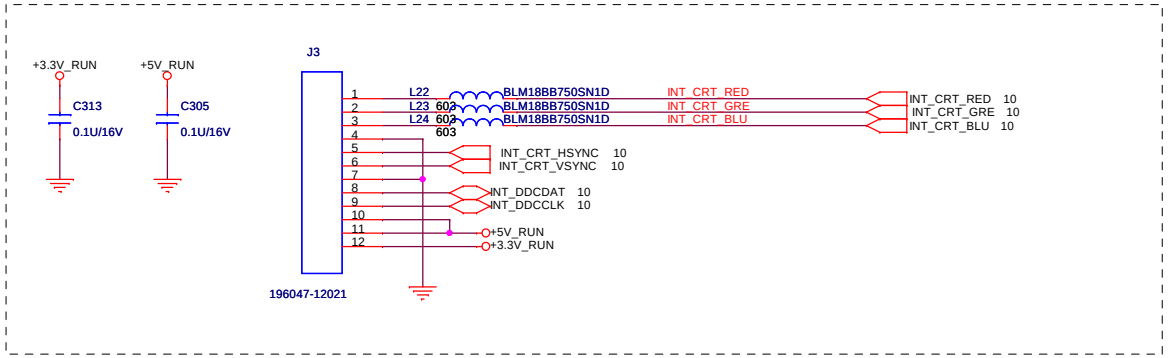

Quanta Computer Inc.		
PROJECT : V02/R01		
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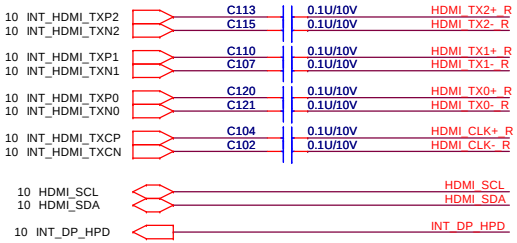
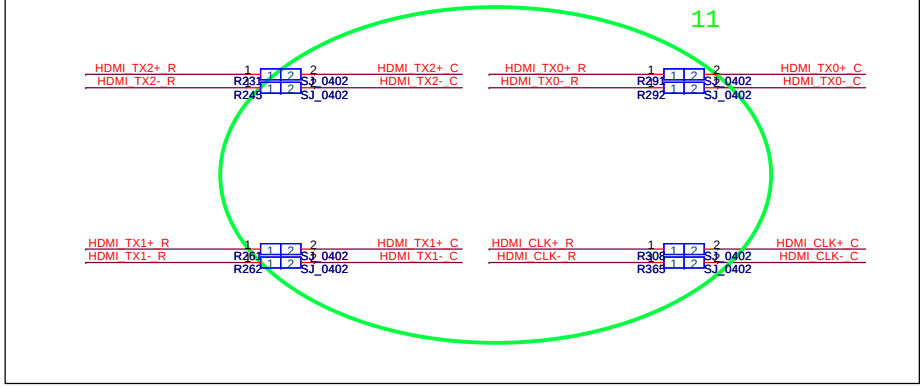
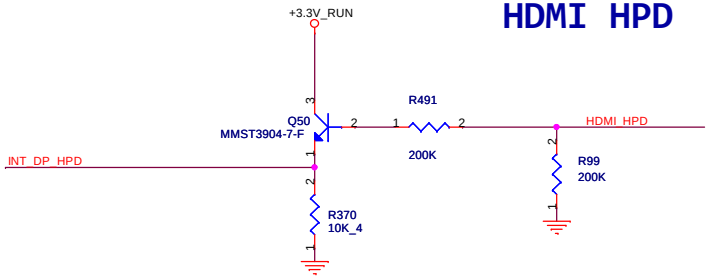
UMA HDMI

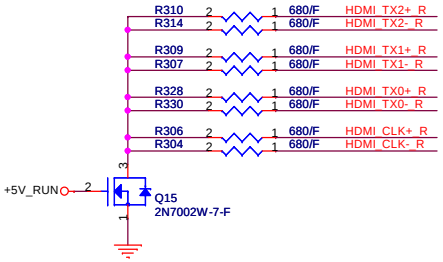


Reserve for EMI and close to HDMI CONN

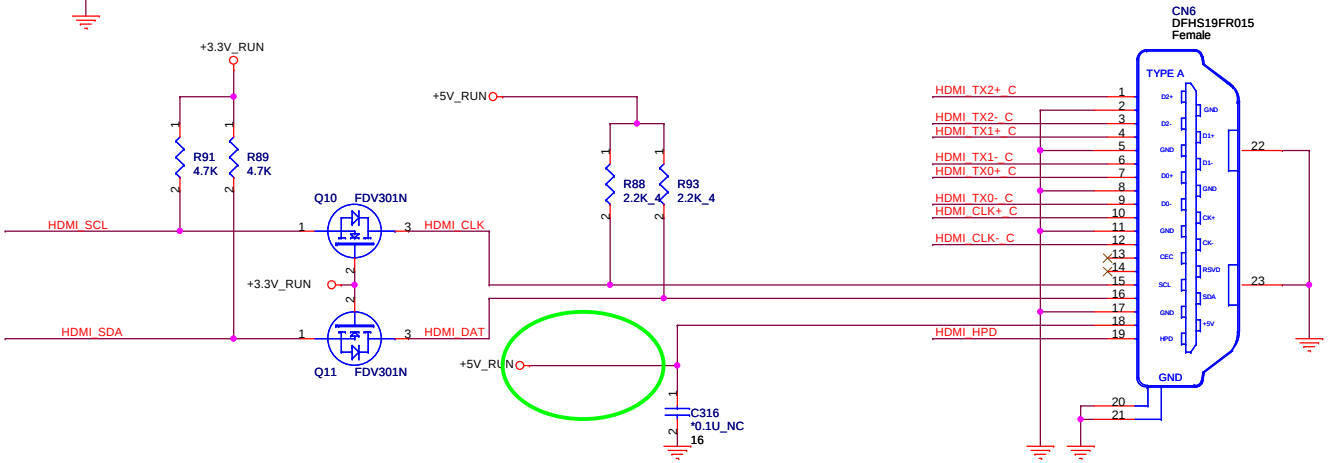


HDMI HPD





HDMI Conn.



Quanta Computer Inc.		
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Size	Document Number: HDMI CONN	Rev: 1A
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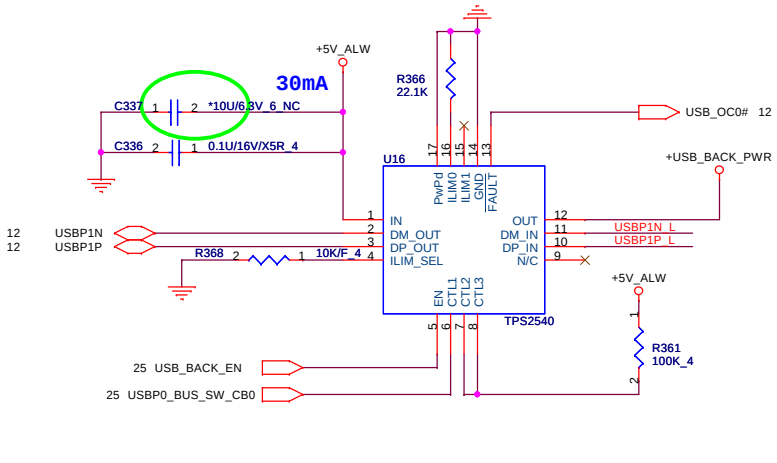
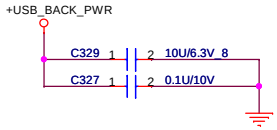
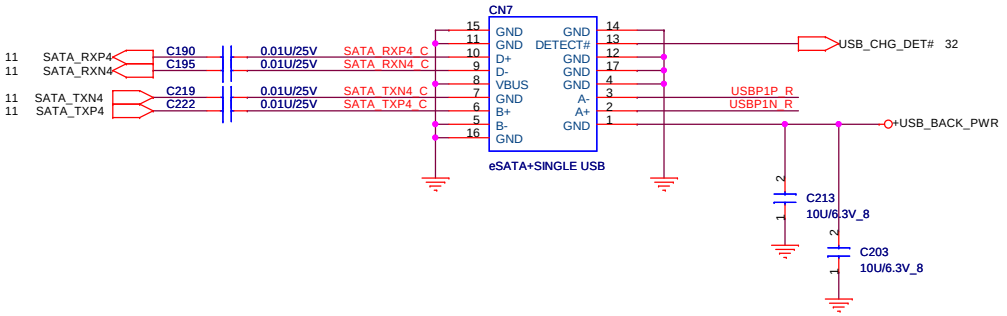
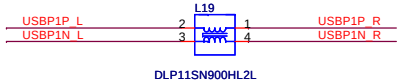
ESATA + USB Conn + Power share

S3/S5 USB charging circuit









USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

Quanta Computer Inc.

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Size	Document Number	Rev
	PUSB / ESATA	1A

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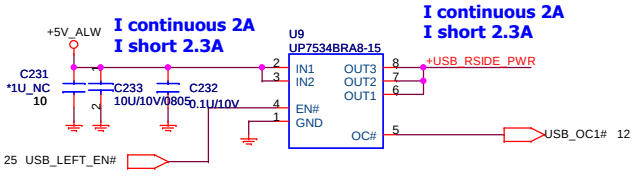
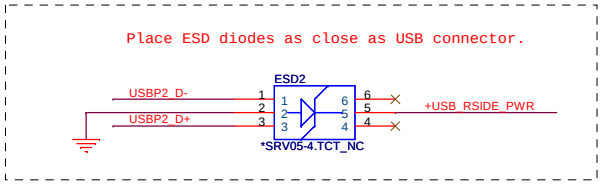
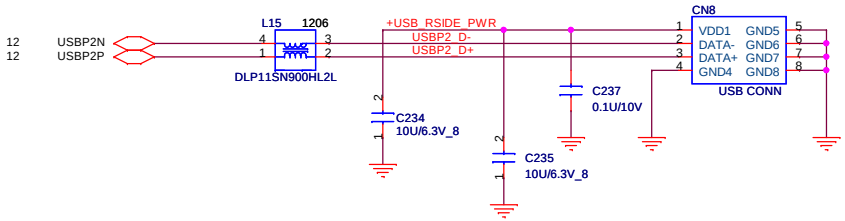
UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.





Quanta Computer Inc.		
PROJECT : V02/R01		
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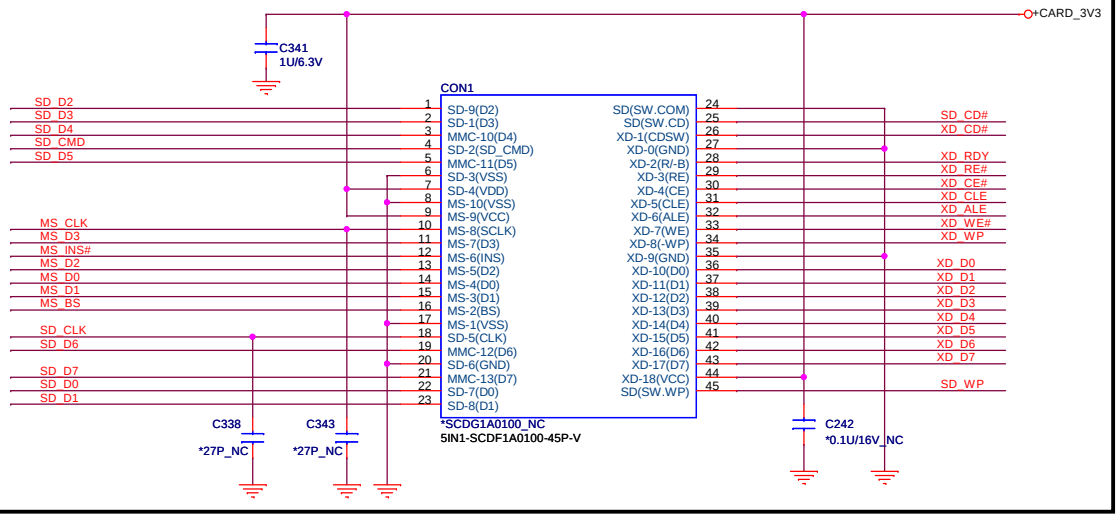
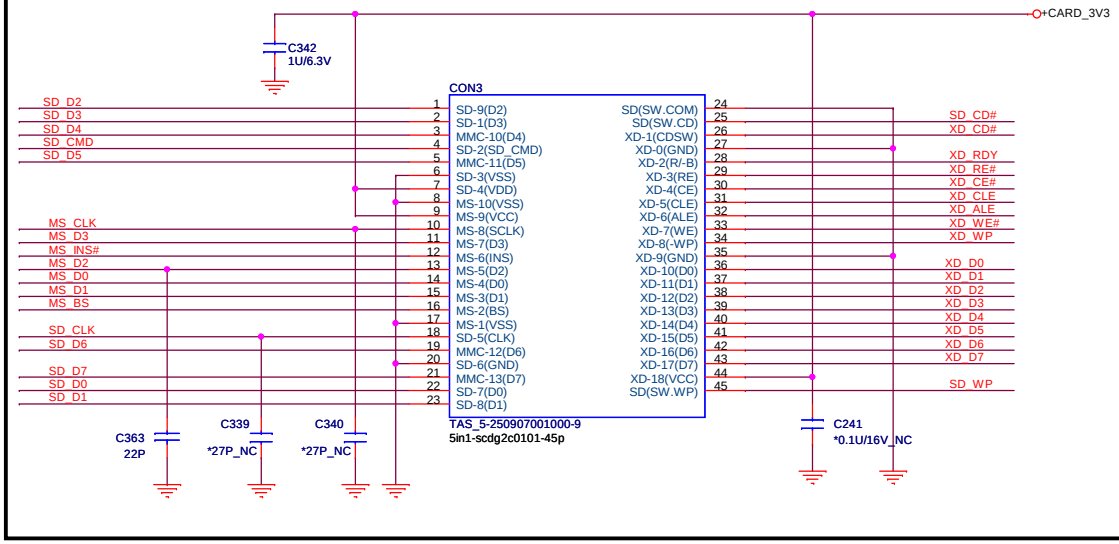
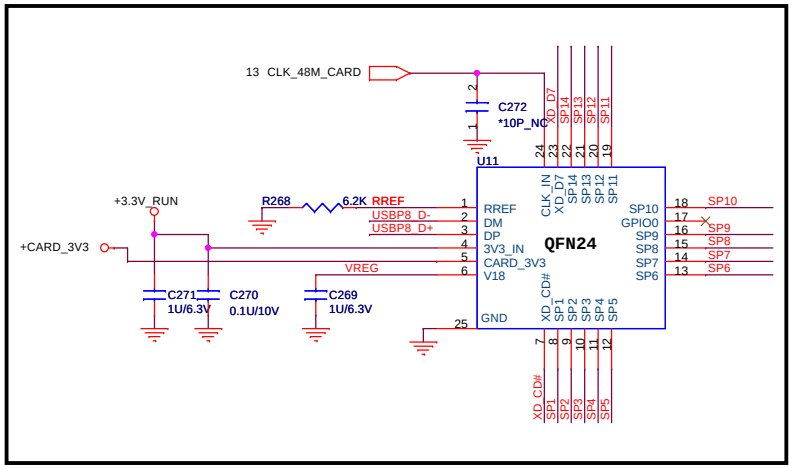
Inspiron



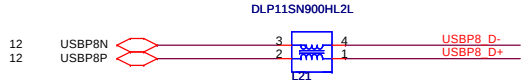
VOSTOR





SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

Quanta Computer Inc.

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	Cardreader (RTS5128)	1A

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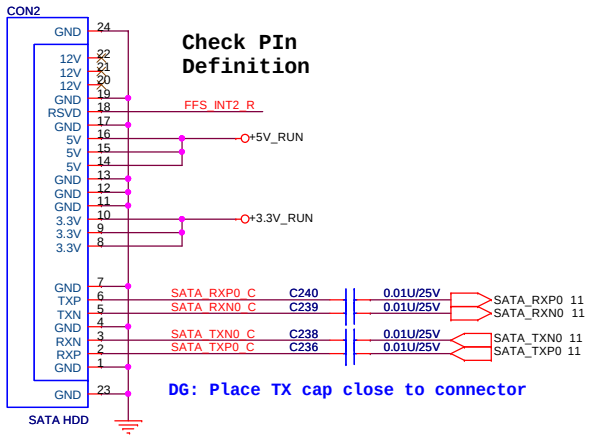
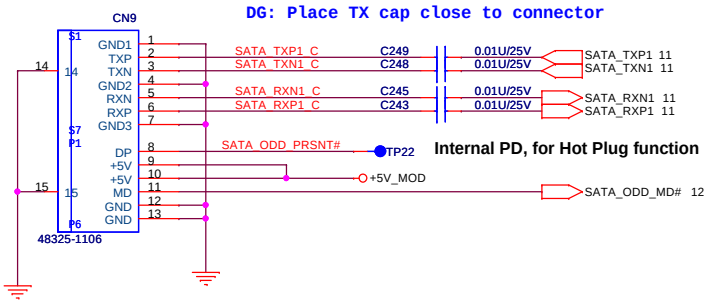
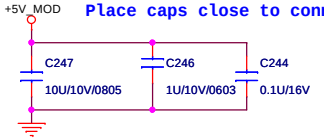
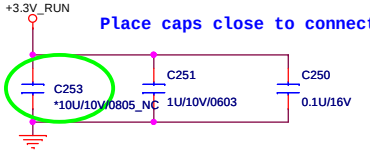
SATA Connector UM8

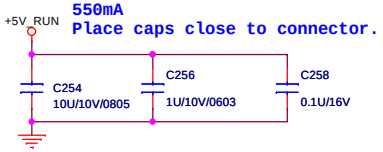


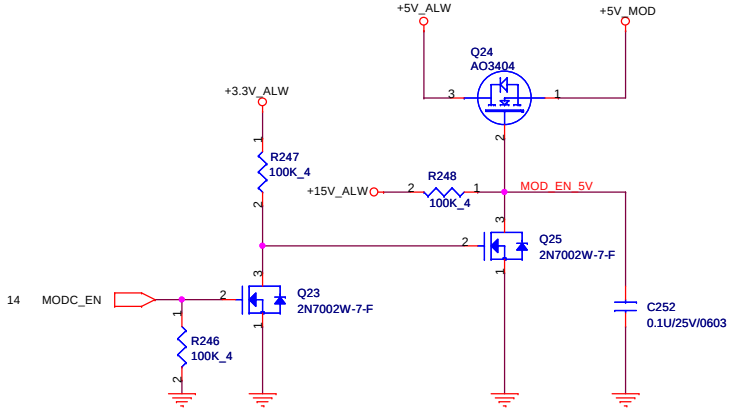
ODD Connector

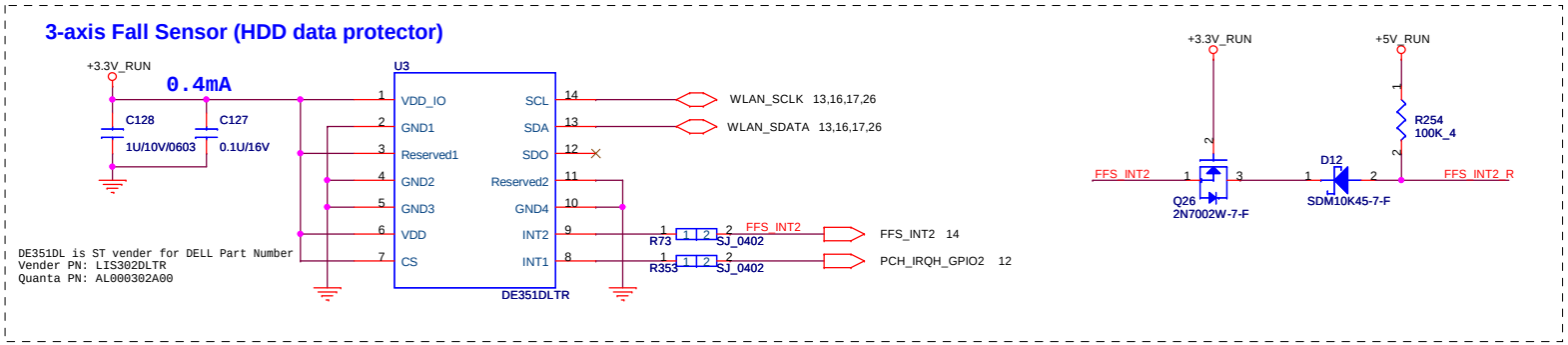












3-axis Fall Sensor	VOSTOR	Inspiron
U3,Q26,D12 R73,R254,R353 C127,C128	POP	NC

Quanta Computer Inc.
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	SATA HDD/ODD	1A

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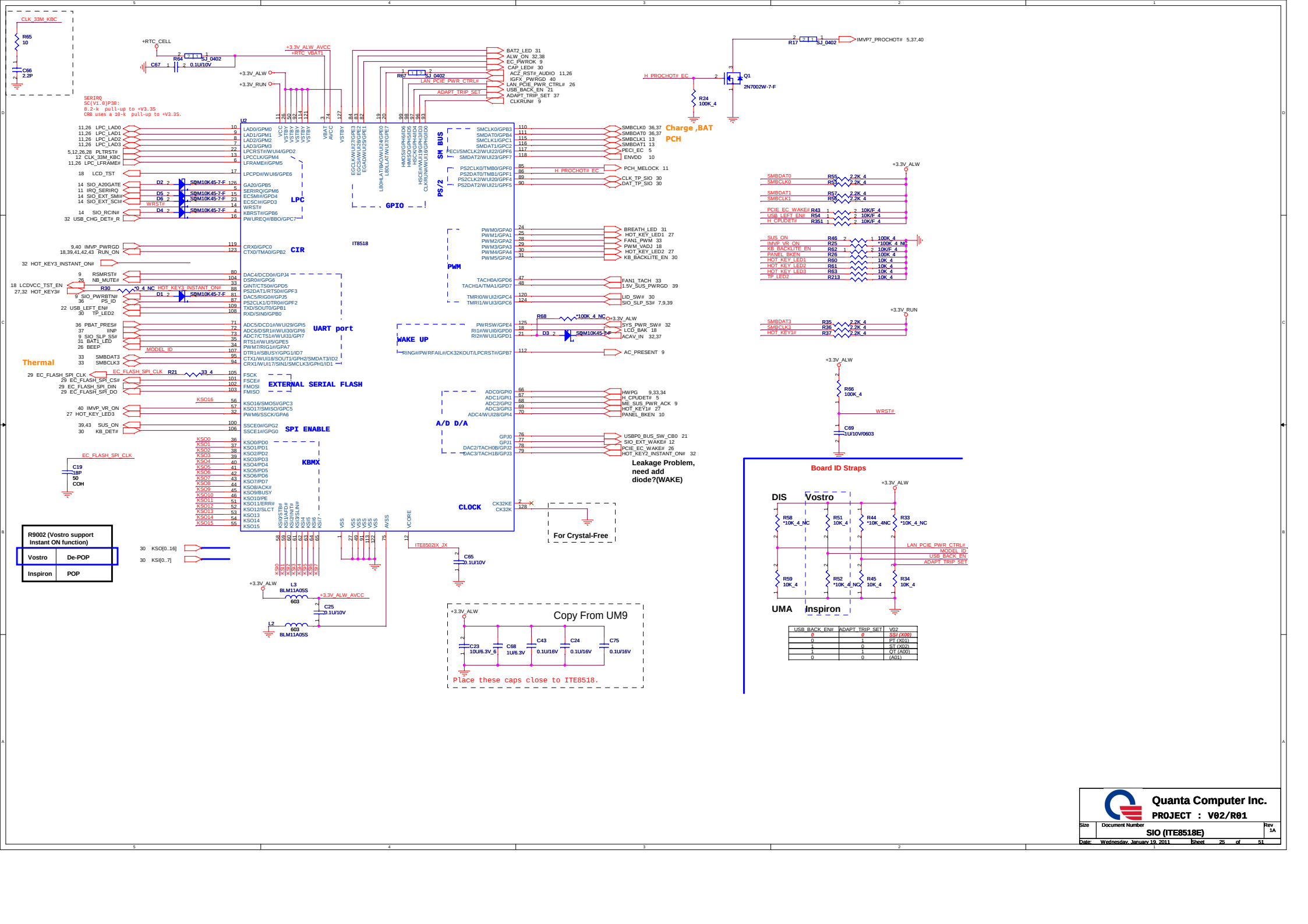
CLK_33M_KBC
R65 10
C66 2.2P
+RTC_CELL
R64 SJ_0402
C67 0.1U/10V
+3.3V_ALW_AVCC
+RTC_VBAT1
+3.3V_ALW
+3.3V_RUN
R67 SJ_0402
LAN_PCIE_PWR_CTRL#
ADAPT_TRIP_SET
BAT2_LED 31
ALW_ON 32,38
EC_PWROK 9
CAP_LED# 30
ACZ_RST# AUDIO 11,26
IGFX_PWRGD 40
LAN_PCIE_PWR_CTRL# 26
USB_BACK_EN 21
ADAPT_TRIP_SET 37
CLKRUN# 9
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.
U2
IT8518
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Thermal
Leakage Problem, need add diode?(WAKE)
For Crystal-Free
ITE8502IX_JX
C65 0.1U/10V
L3 BLM11A05S 603
L2 603 BLM11A05S
C25 0.1U/10V
Charge ,BAT PCH
H_PROCHOT# EC
Q1 2N7002W-7-F
R24 100K_4
R17 SJ_0402
IMVP7_PROCHOT# 5,37,40
SMBDAT0
SMBCLK0
SMBDAT1
SMBCLK1
PCIE_EC_WAKE#
USB_LEFT_EN#
H_CPUDET#
SUS_ON
IMVP_VR_ON
KB_BACKLITE_EN
PANEL_BKEN
HOT_KEY_LED1
HOT_KEY_LED2
HOT_KEY_LED3
TP_LED2
SMBDAT3
SMBCLK3
HOT_KEY1#
R66 100K_4
C69 1U/10V/0603
WRST#
Board ID Straps
DIS Vostro
UMA Inspiron
R58 *10K_4_NC
R51 10K_4
R44 *10K_4NC
R33 *10K_4_NC
R59 10K_4
R52 *10K_4_NC
R45 10K_4
R34 10K_4
Copy From UM9
C23 10U/6.3V_6
C68 1U/6.3V
C43 0.1U/16V
C24 0.1U/16V
C75 0.1U/16V
Place these caps close to ITE8518.
R9002 (Vostro support Instant ON function)
Vostro De-POP
Inspiron POP
USB_BACK_EN# ADAPT_TRIP_SET V02
0 0 SSI (X00)
0 1 PT (X01)
1 0 ST (X02)
1 1 QT (A00)
0 0 (A01)
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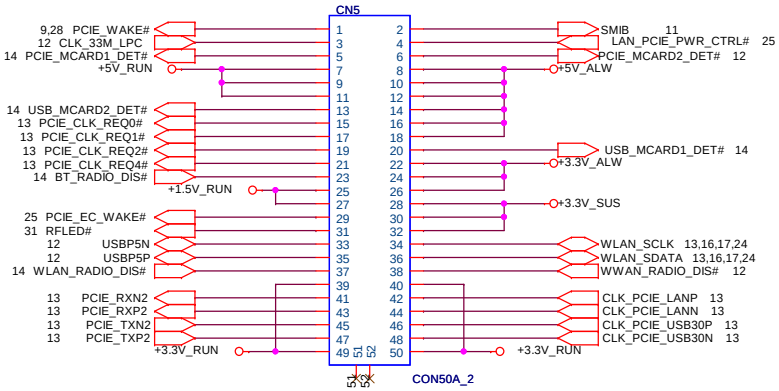

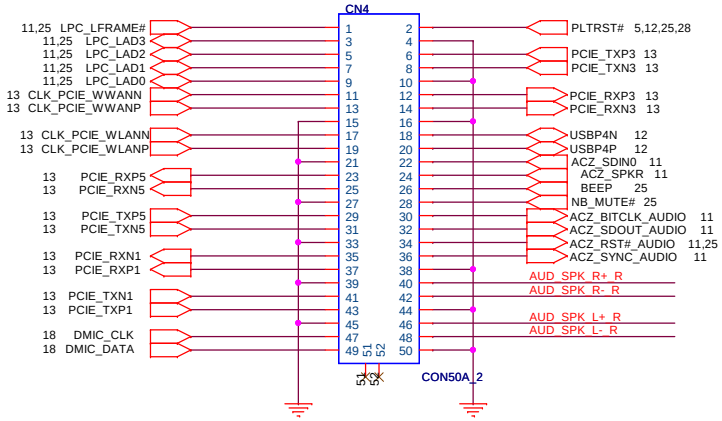

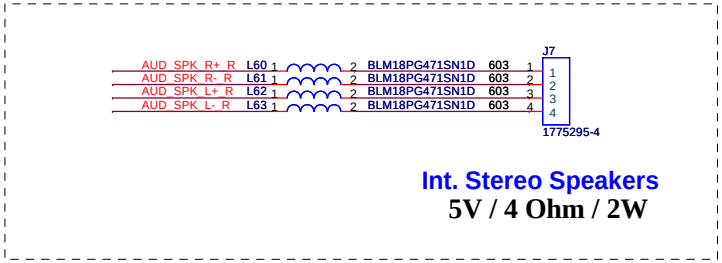

Quanta Computer Inc.

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	SIO (ITE8518E)	1A

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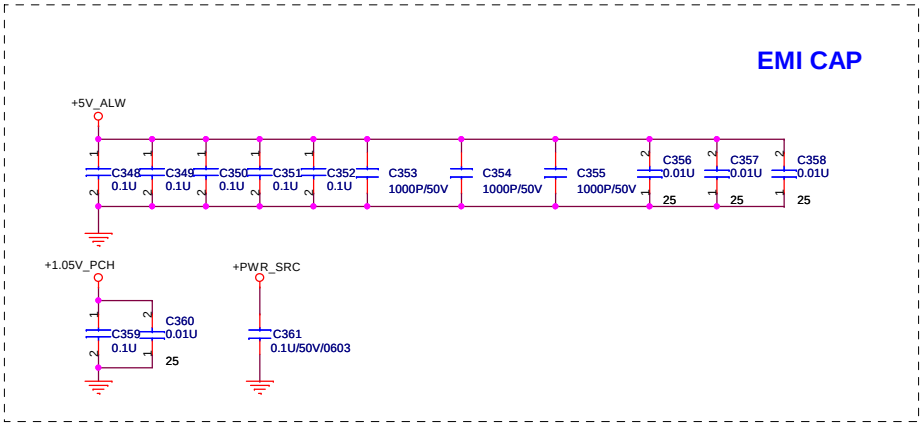
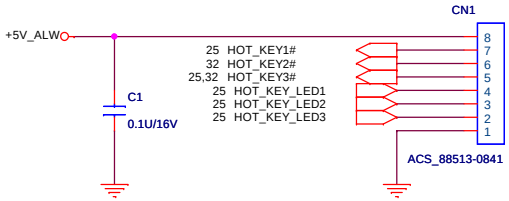
EMI CAP



HOTKEY CON



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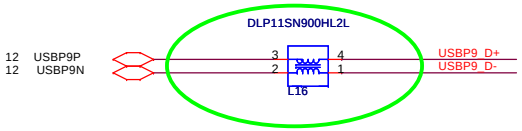
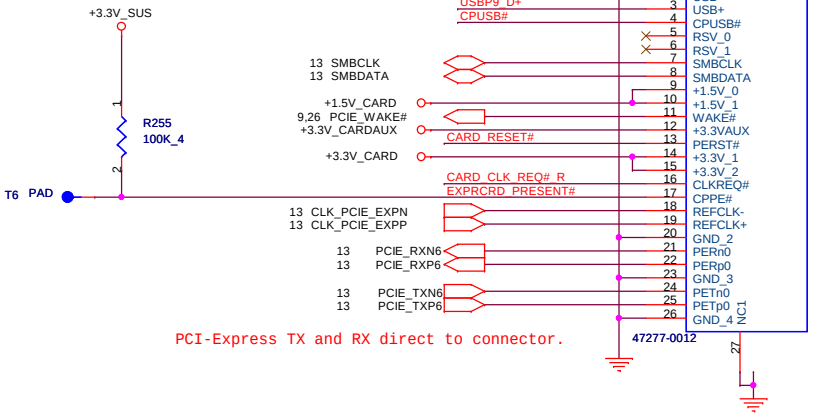
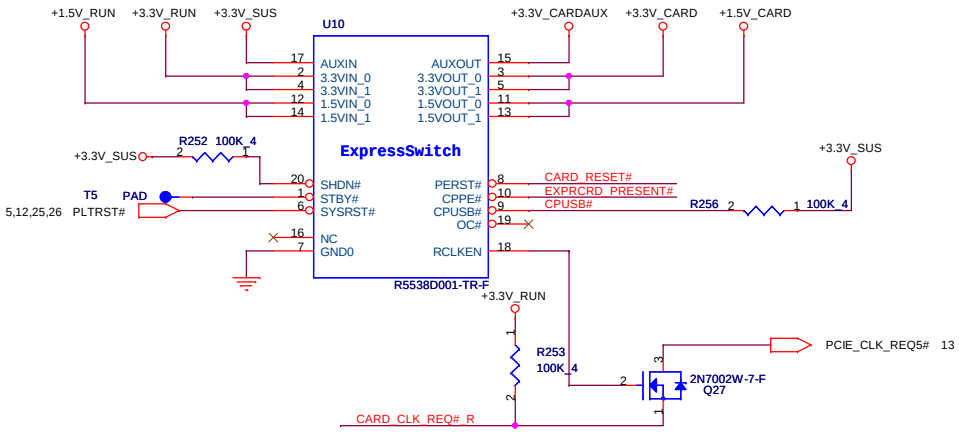
Express Card

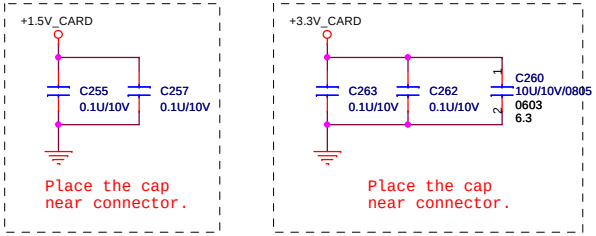




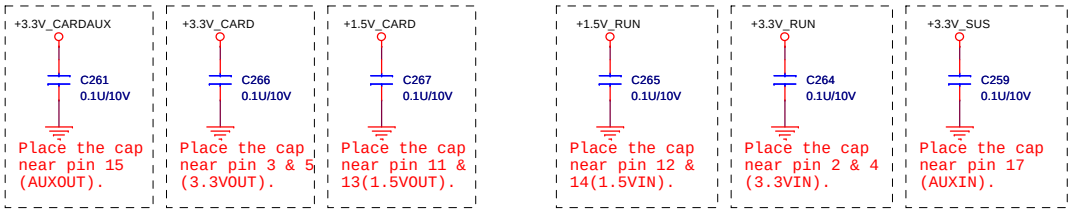
PCI-Express TX and RX direct to connector.

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.





If close enough, could combine



Quanta Computer Inc.
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Size	Document Number	Rev
	LAN (RTL8111EL)	1A
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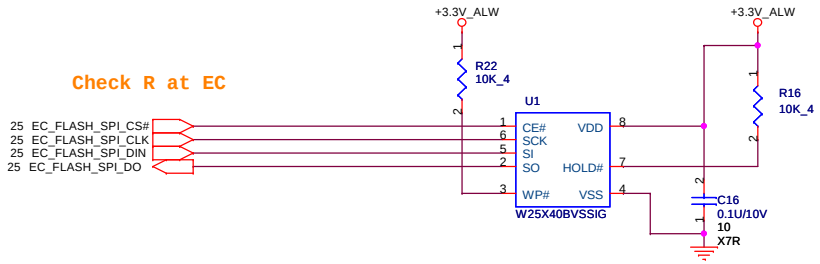
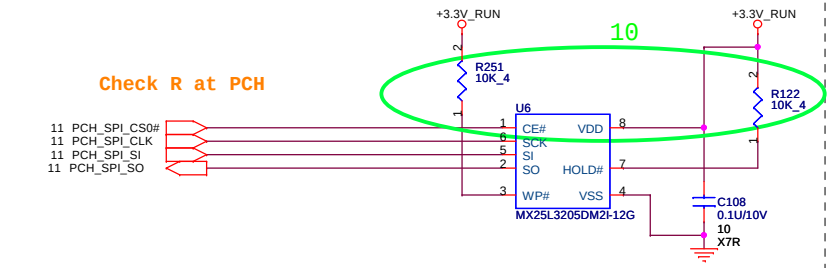
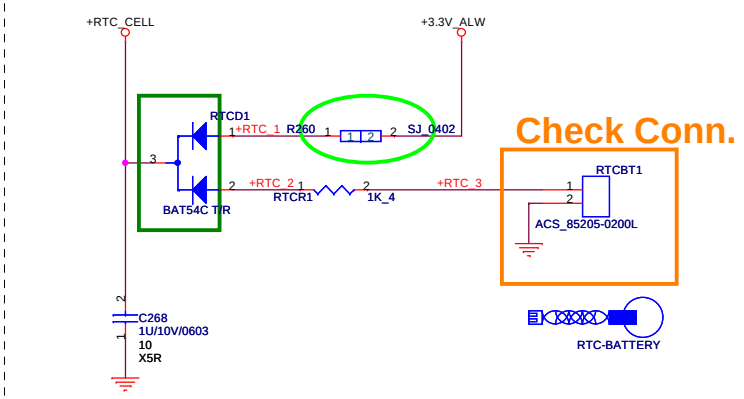
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC



Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

Quanta Computer Inc.		
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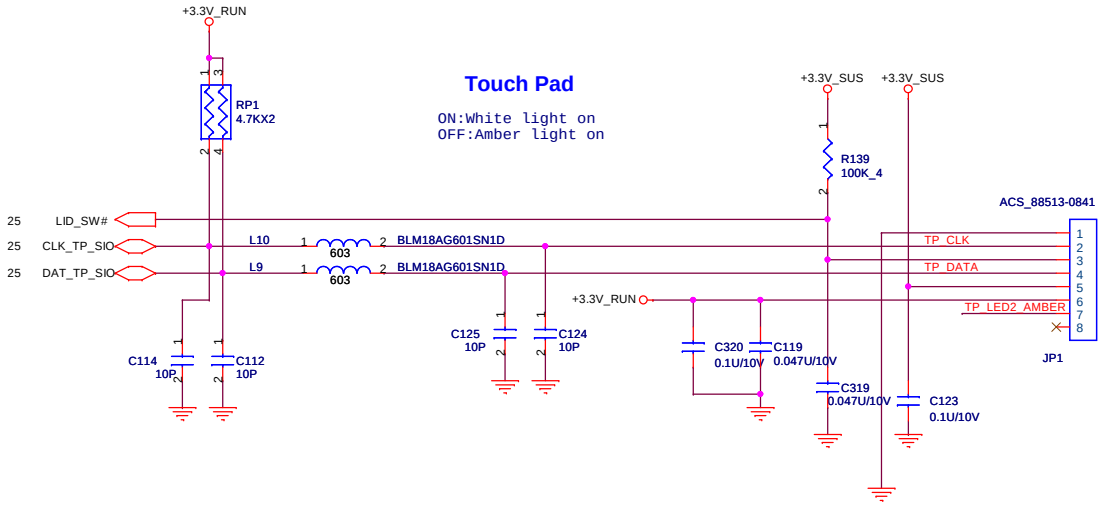
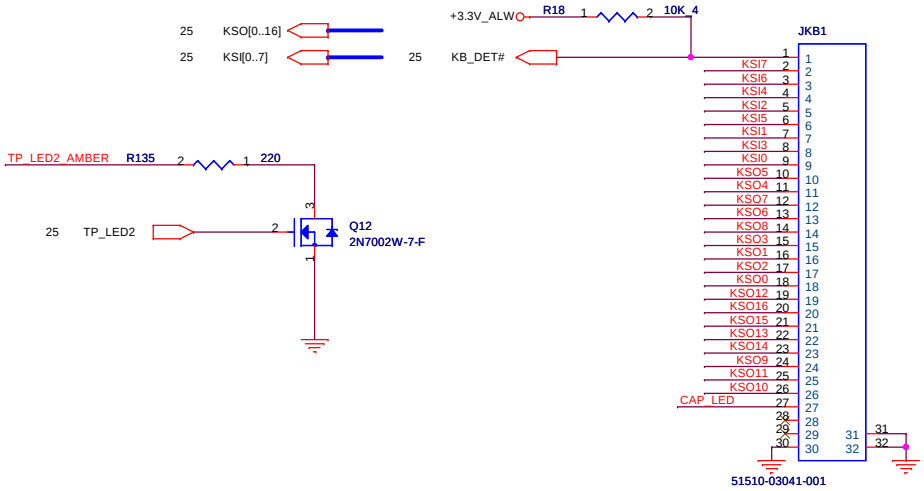
Touch Pad

ON:White light on
OFF:Amber light on

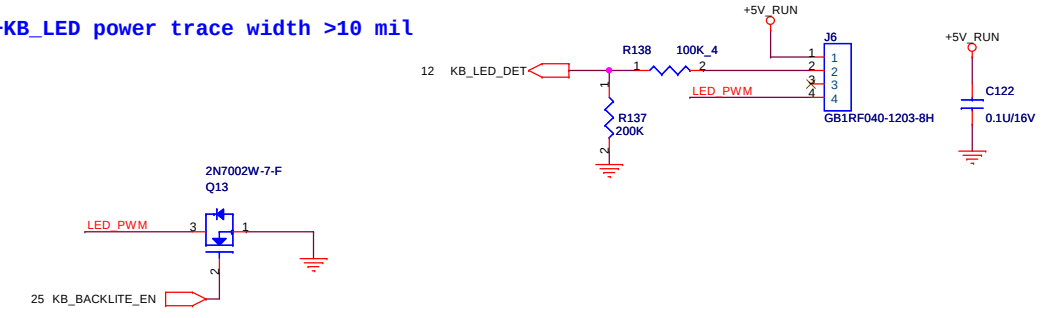


KEYBOARD CONNECTOR



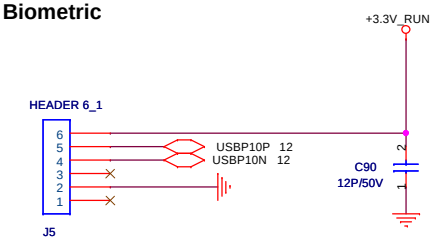
Key board illumination

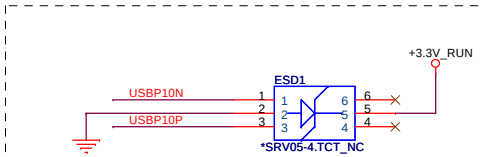
+KB_LED power trace width >10 mil

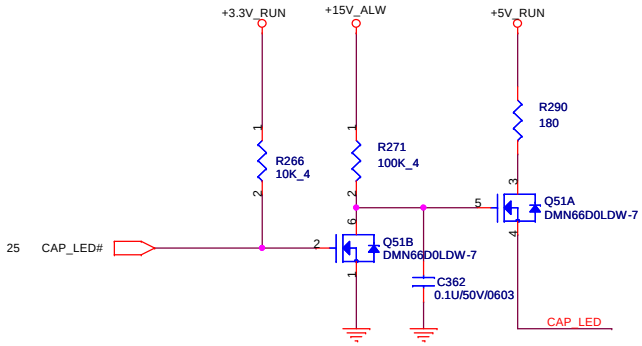


15

Biometric







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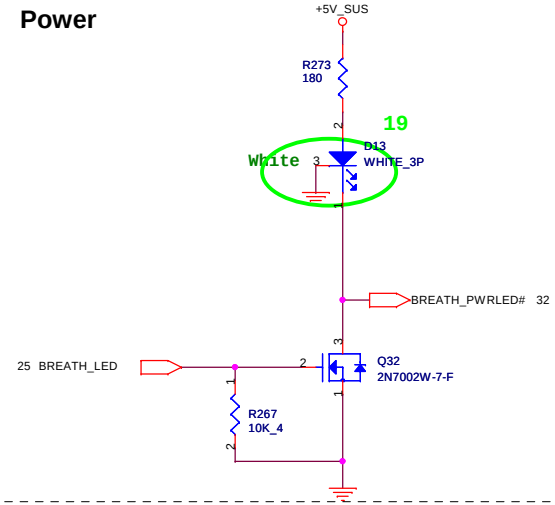
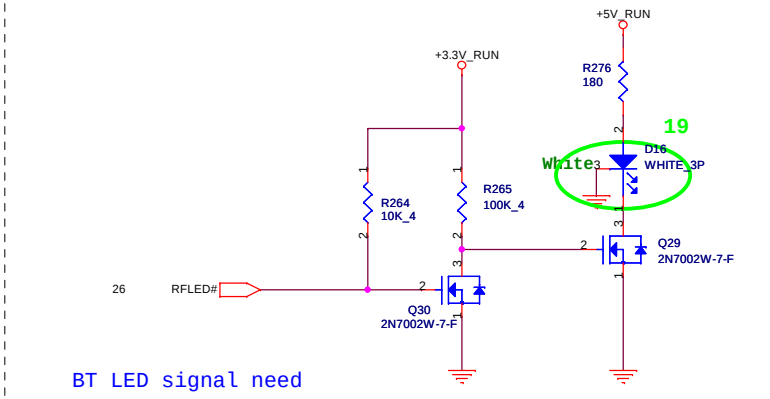
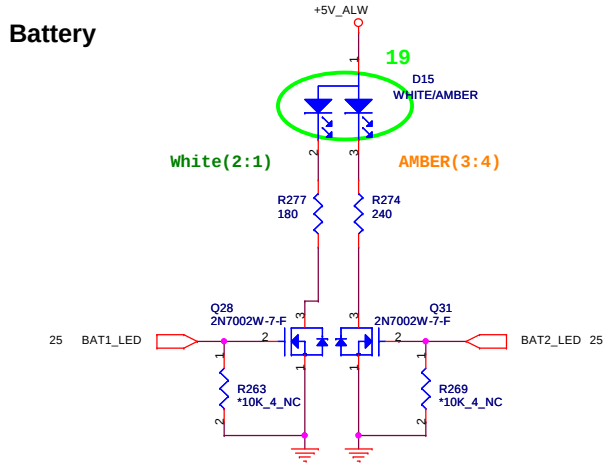
Power



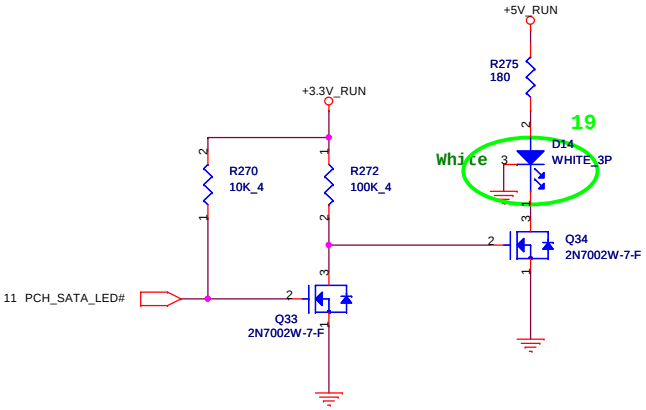
Bluetooth / WLAN on/off LED



Battery



HDD activity LED.



VOSTOR	R273,R276,R277,R275	R274
	180 ohm PN:CS11802JB15	240ohm PN:CS12402JB13
Inspiron	R273,R276,R277,R275	R274
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

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	LED	1A
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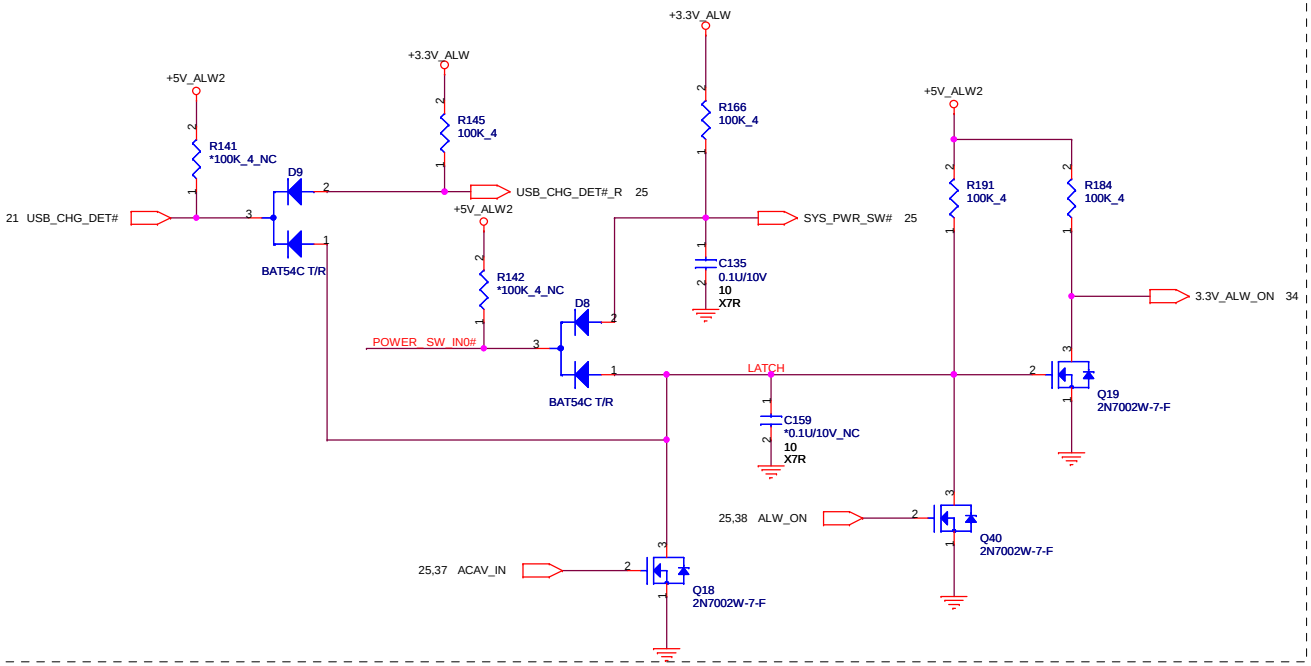
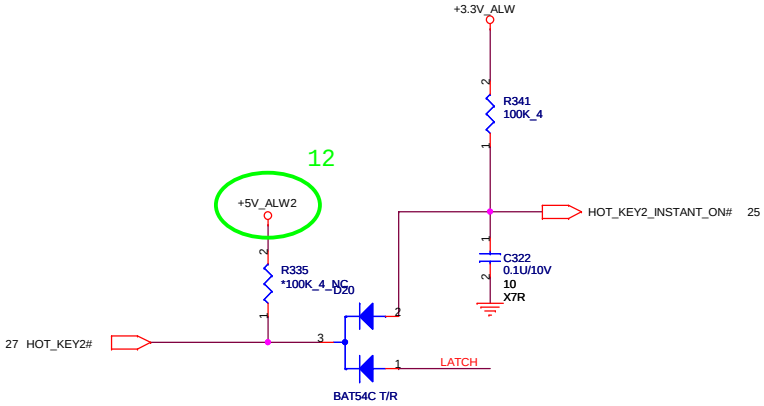
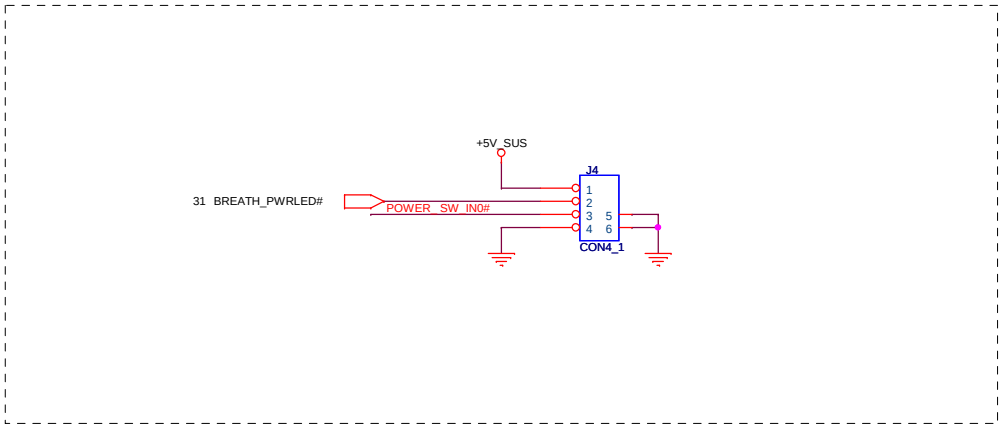
3VALW ON POWER LOGIC

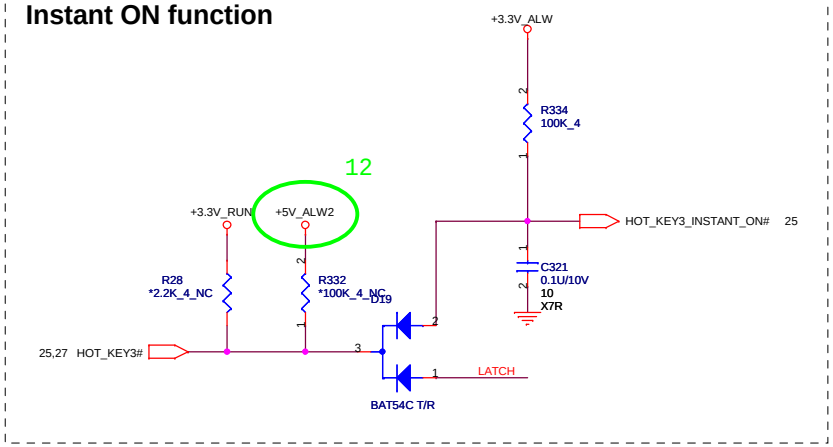




Vostro pop D19,C321,R334 depop R28,R30
Inspiron depop D19,C321,R334 pop R28,R30



Instant ON function



Quanta Computer Inc.
PROJECT : V02/R01

Size	Document Number	Rev
	PWR SW/LED	1A
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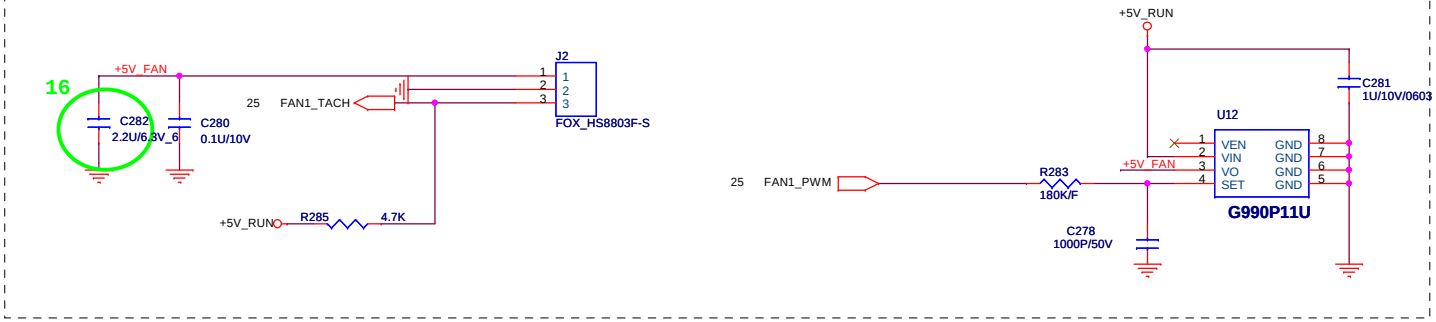
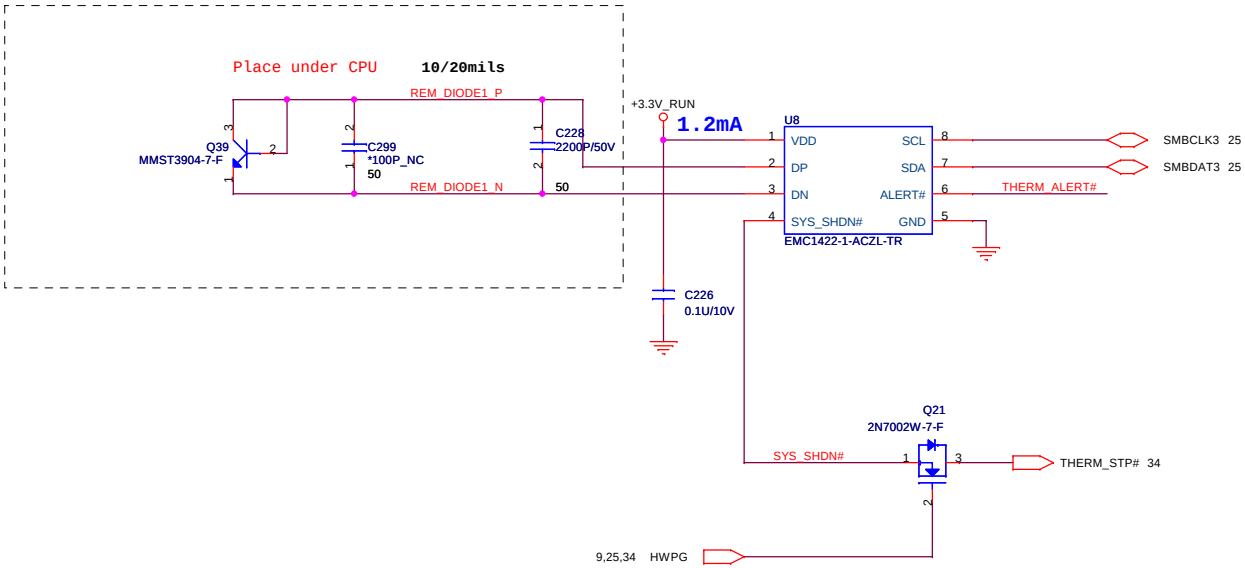
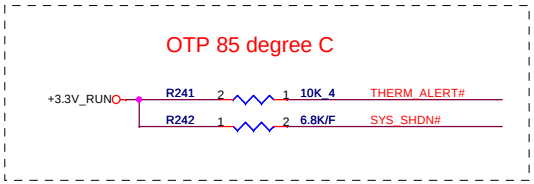
FAN CONTROL







SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

Quanta Computer Inc.

PROJECT : V02/R01

Size	Document Number	Rev
	FAN & THERMAL	1A

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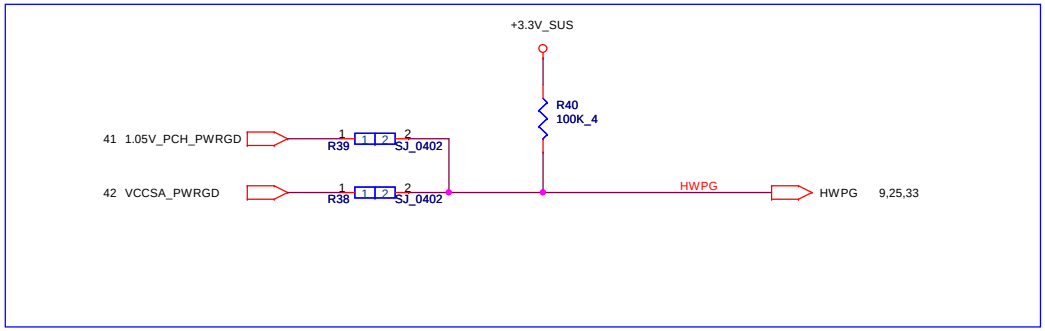
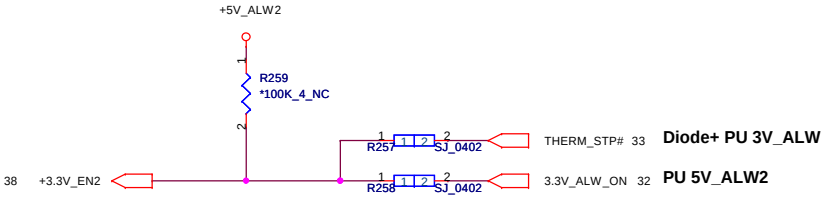
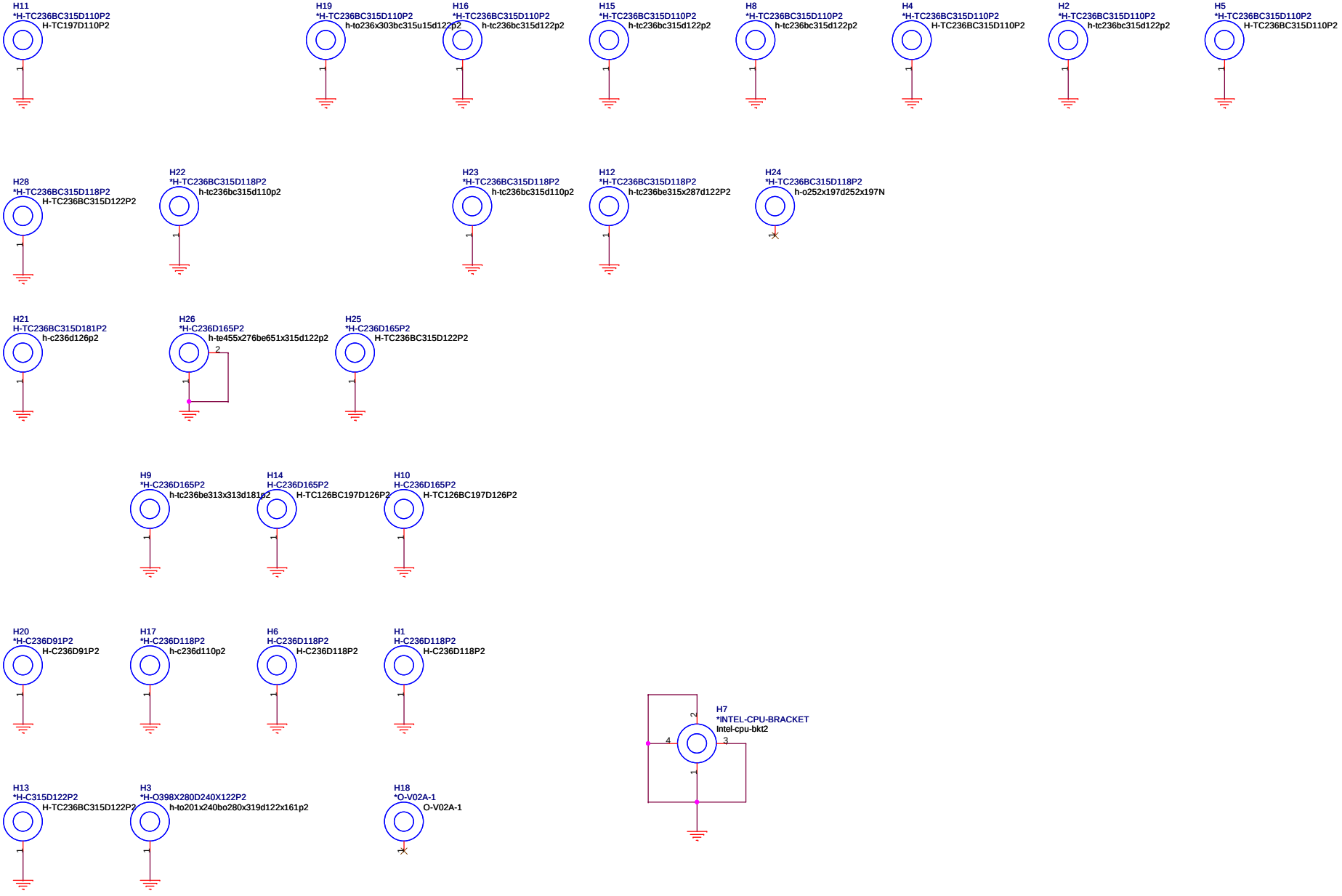
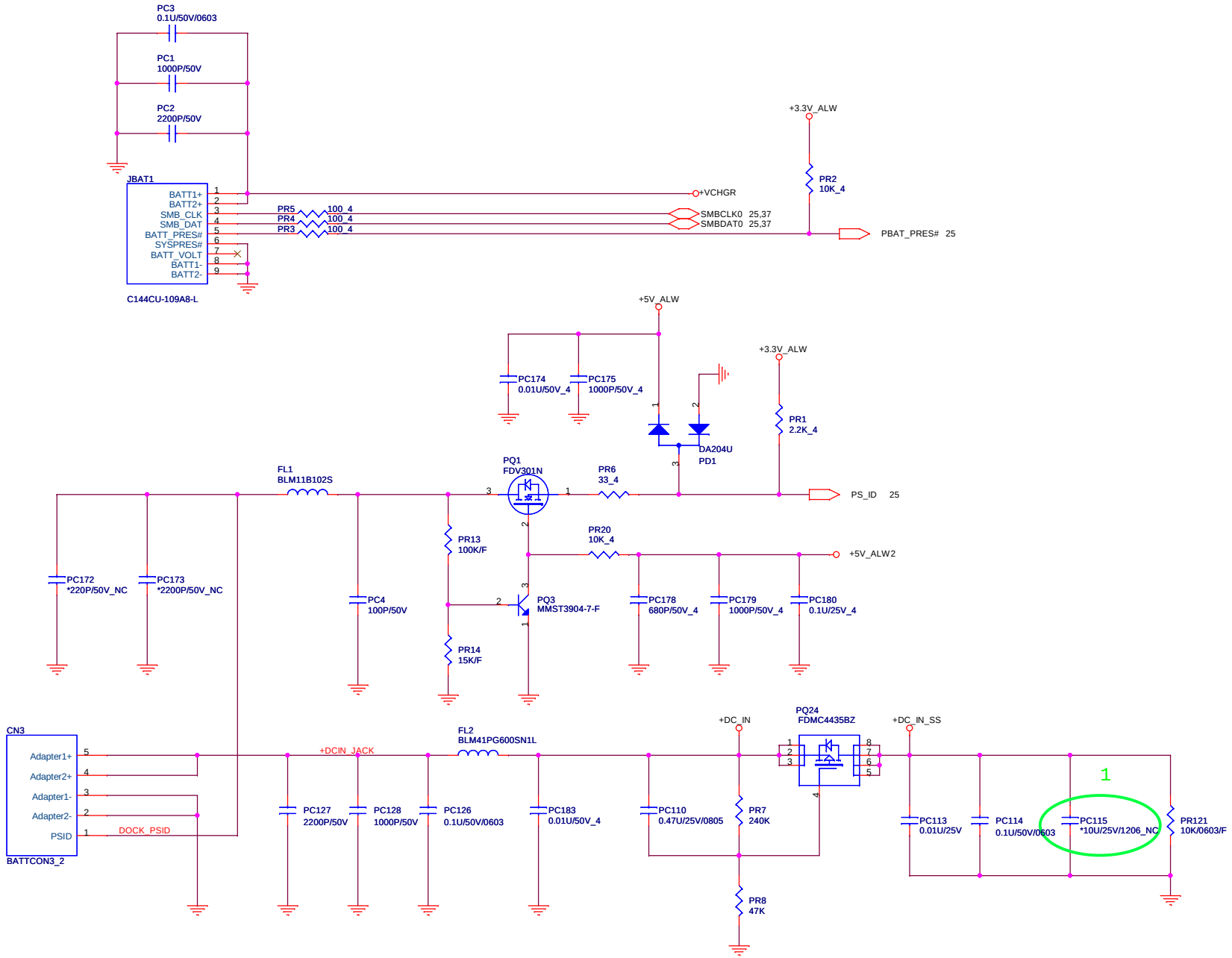




Quanta Computer Inc.		
PROJECT : V02/R01		
Size	Document Number: System Reset Circuit	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 34 of 51	



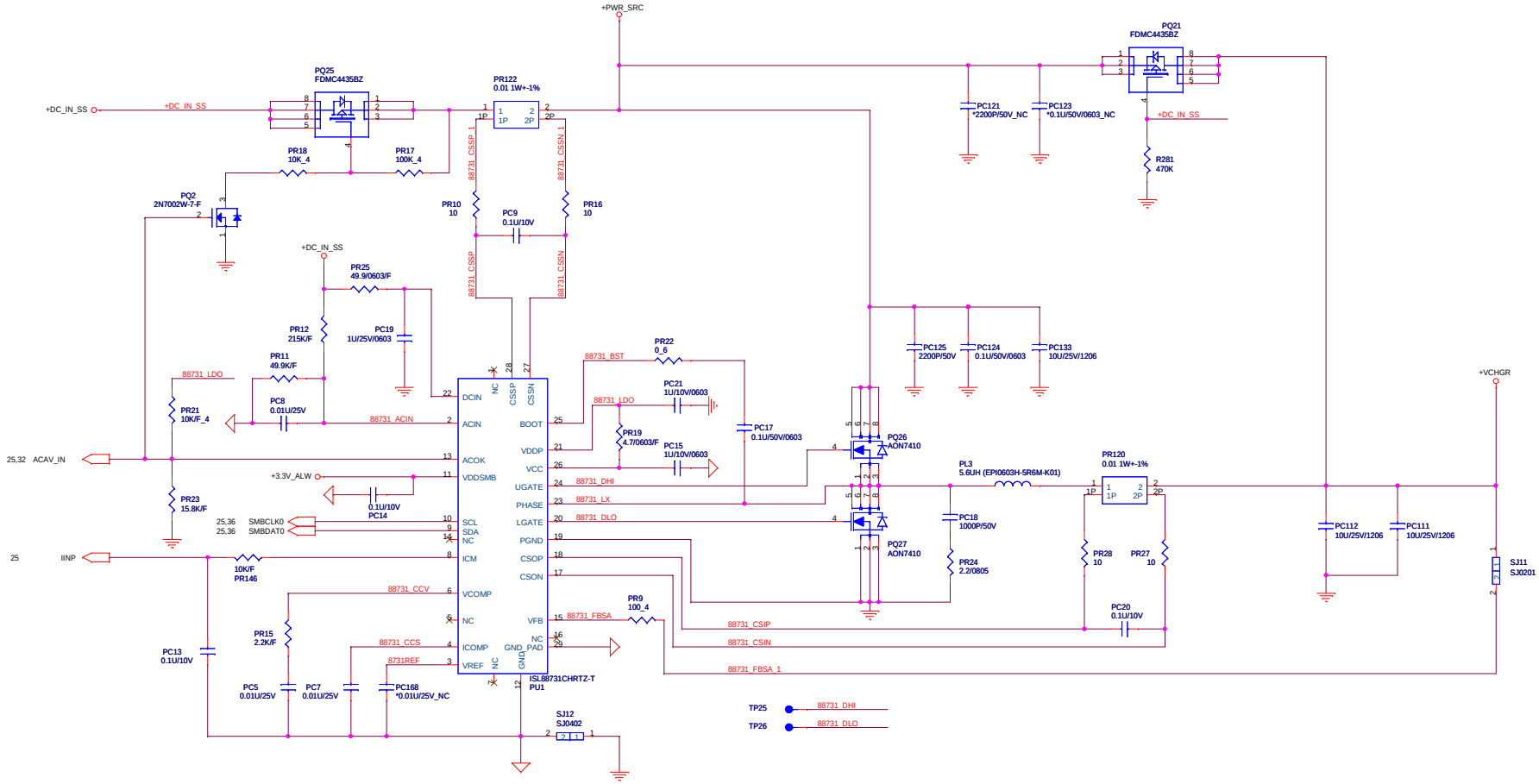
Quanta Computer Inc.		
PROJECT : V02/R01		
Size	Document Number: SCREW PAD	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 35 of 51	

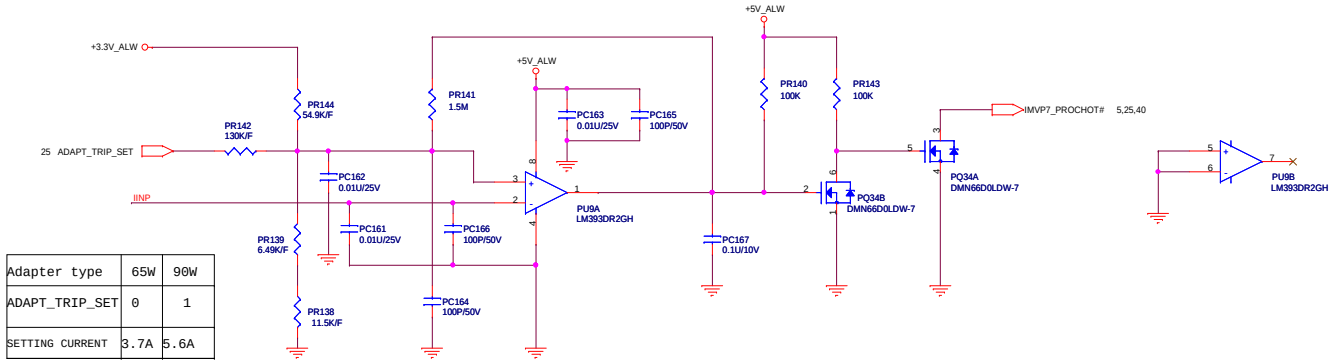


Quanta Computer Inc.

PROJECT : V02/R01

Size	Document Number	Rev
	DC IN / BATT	1A
Date: Wednesday, January 19, 2011	Sheet 36 of 51	





Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Quanta Computer Inc.
PROJECT : V02/R01

Size	Document Number	Rev
	Charger (BQ24765RUVR)	1A

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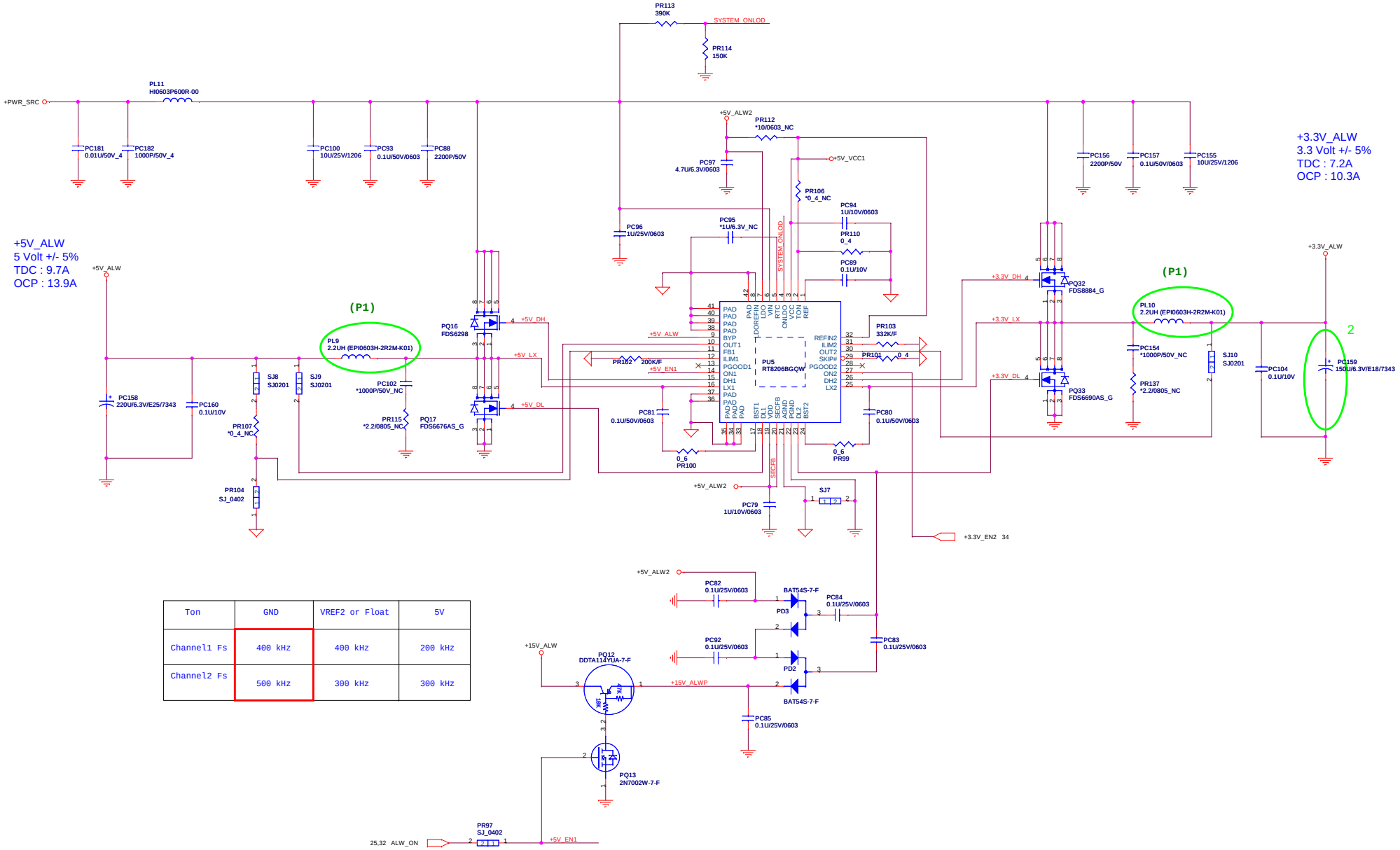

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

Quanta Computer Inc.
PROJECT : V02/R01

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51427ARHBR)	1A

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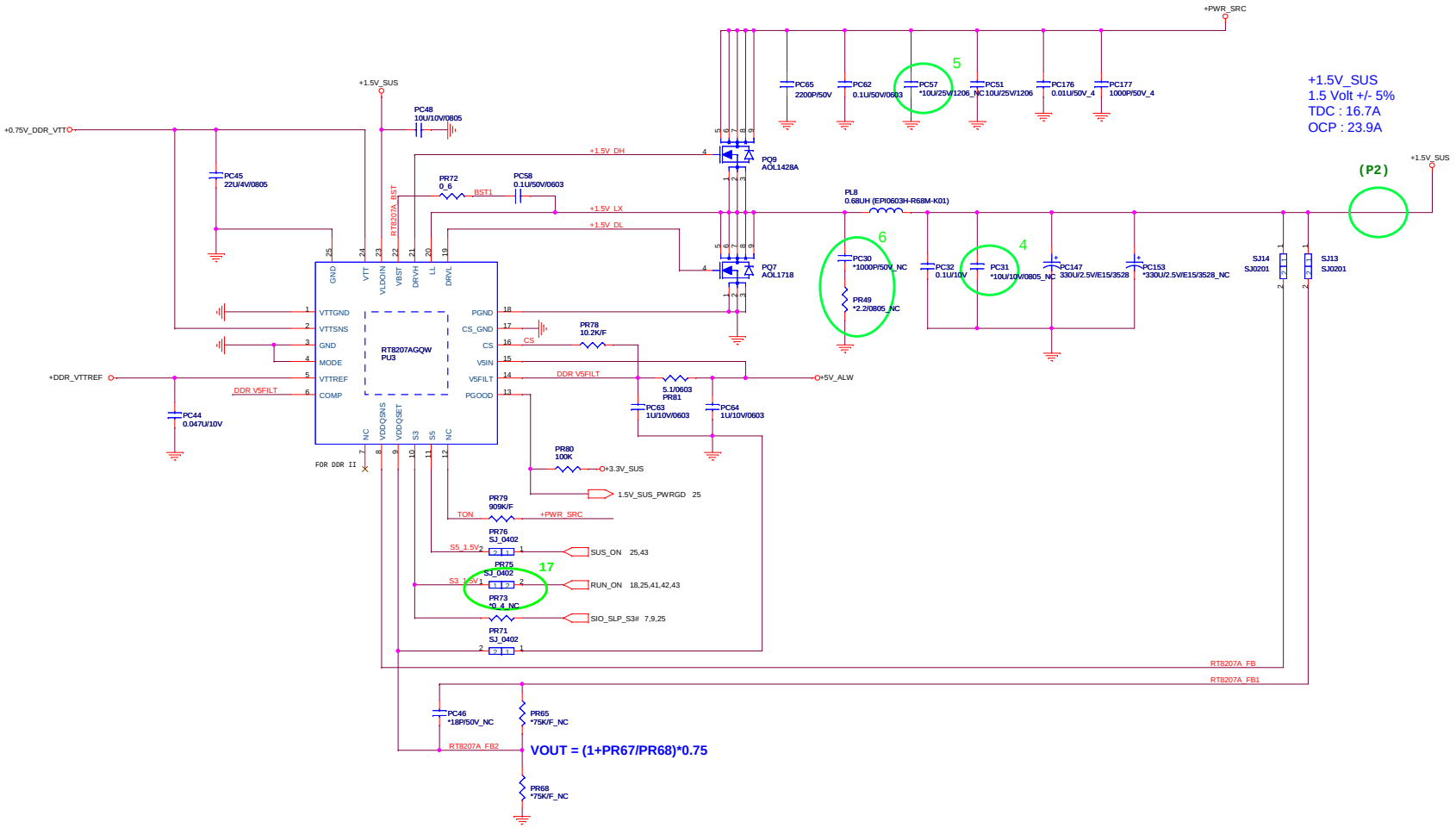

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : V02/R01
Size | Document Number: 1.5_SUS/0.75_DDR_VTT (RT8207AGQW) | Rev 1A
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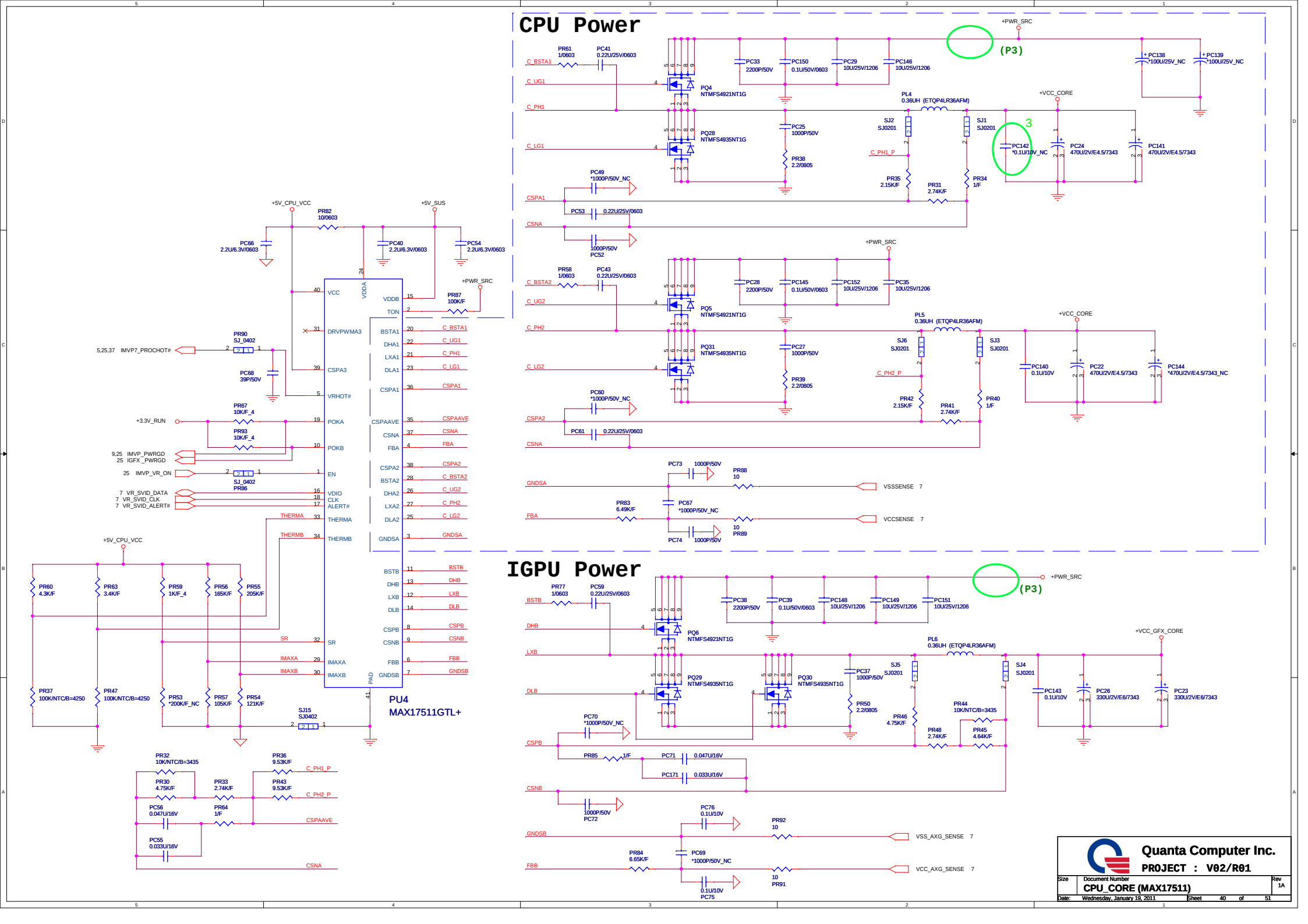
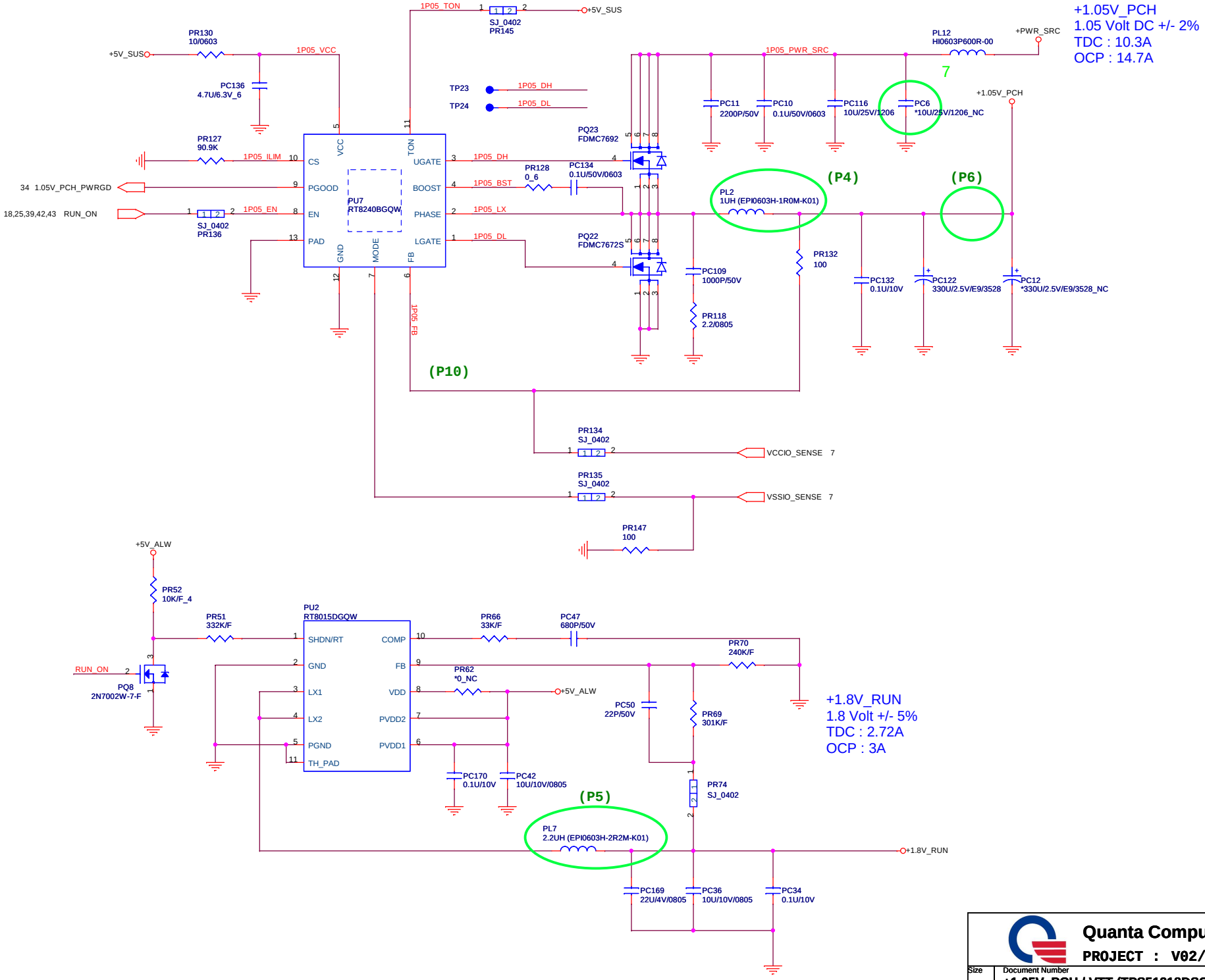

CPU Power
IGPU Power
PU4
MAX17511GTL+
+5V_CPU_VCC
+5V_SUS
+PWR_SRC
+VCC_CORE
+VCC_GFX_CORE
(P3)
VSSSENSE 7
VCCSENSE 7
VSS_AXG_SENSE 7
VCC_AXG_SENSE 7
Quanta Computer Inc.
PROJECT : V02/R01
CPU_CORE (MAX17511)
Wednesday, January 19, 2011


+1.05V_PCH
1.05 Volt DC +/- 2%
TDC : 10.3A
OCP : 14.7A
1P05_TON
SJ_0402
PR145
+5V_SUS
PR130
10/0603
1P05_VCC
PC136
4.7U/6.3V_6
TP23
TP24
1P05_DH
1P05_DL
PR127
90.9K
1P05_ILIM
34 1.05V_PCH_PWRGD
18,25,39,42,43 RUN_ON
1P05_EN
SJ_0402
PR136
PU7
RT8240BGQW
VCC
TON
CS
UGATE
PGOOD
BOOST
EN
PHASE
PAD
LGATE
GND
MODE
FB
PR128
0_6
PC134
0.1U/50V/0603
1P05_BST
1P05_LX
PQ23
FDMC7692
PQ22
FDMC7672S
1P05_FB
PL12
HI0603P600R-00
+PWR_SRC
1P05_PWR_SRC
PC11
2200P/50V
PC10
0.1U/50V/0603
PC116
10U/25V/1206
PC6
*10U/25V/1206_NC
+1.05V_PCH
(P4)
(P6)
PL2
1UH (EPI0603H-1R0M-K01)
PC109
1000P/50V
PR118
2.2/0805
PR132
100
PC132
0.1U/10V
PC122
330U/2.5V/E9/3528
PC12
*330U/2.5V/E9/3528_NC
(P10)
PR134
SJ_0402
VCCIO_SENSE 7
PR135
SJ_0402
VSSIO_SENSE 7
PR147
100
+5V_ALW
PR52
10K/F_4
PR51
332K/F
PU2
RT8015DGQW
SHDN/RT
COMP
GND
FB
LX1
VDD
LX2
PVDD2
PGND
PVDD1
TH_PAD
PR66
33K/F
PC47
680P/50V
PR70
240K/F
PR62
*0_NC
PC50
22P/50V
PR69
301K/F
RUN_ON
PQ8
2N7002W-7-F
PC170
0.1U/10V
PC42
10U/10V/0805
(P5)
PR74
SJ_0402
PL7
2.2UH (EPI0603H-2R2M-K01)
+1.8V_RUN
PC169
22U/4V/0805
PC36
10U/10V/0805
PC34
0.1U/10V
+1.8V_RUN
1.8 Volt +/- 5%
TDC : 2.72A
OCP : 3A
Quanta Computer Inc.
PROJECT : V02/R01
Size
Document Number
+1.05V_PCH / VTT (TPS51218DSCR)
Rev
1A
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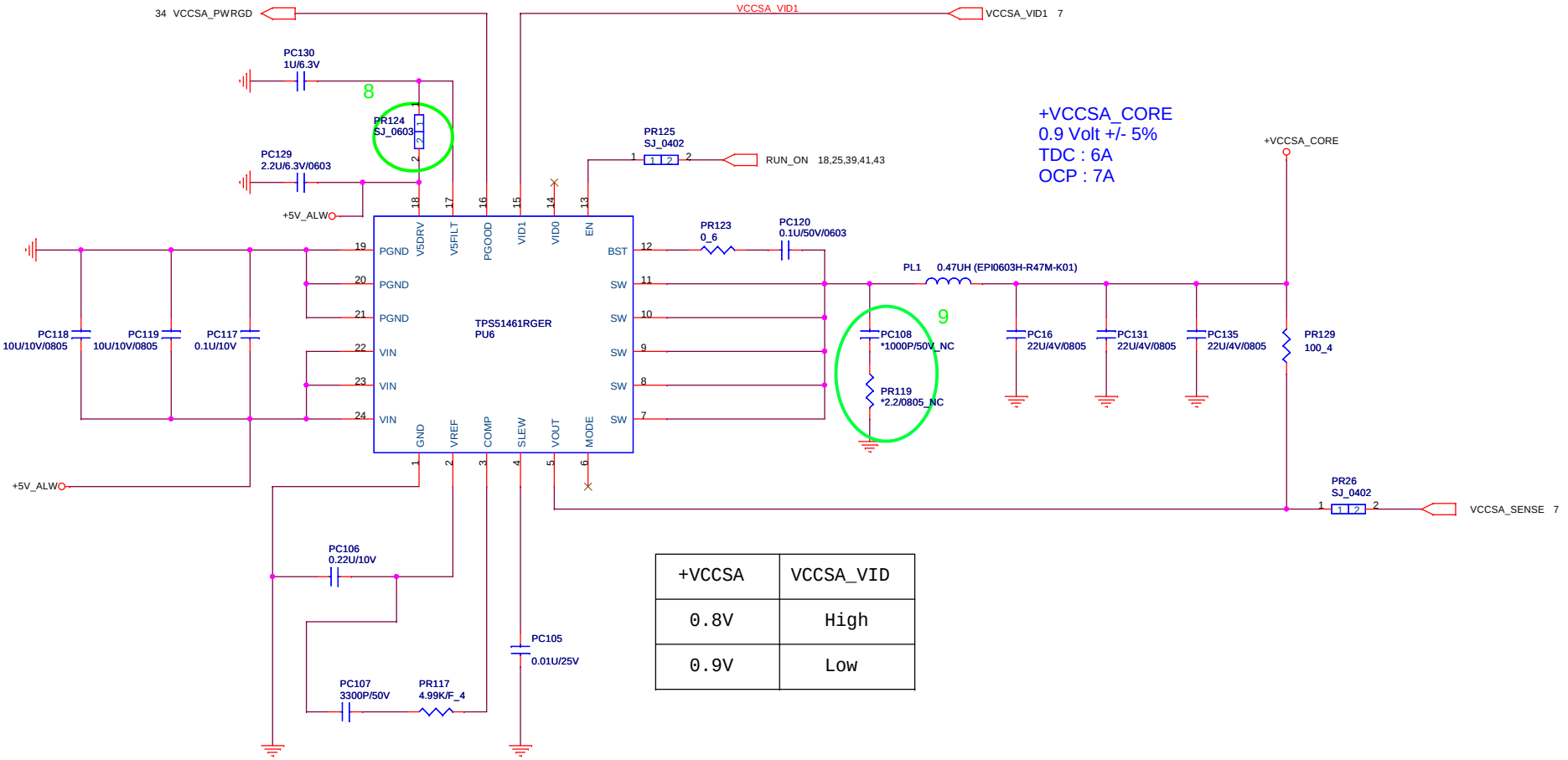

+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.

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Size	Document Number	Rev
	VCCSA (ISL95870A)	1A

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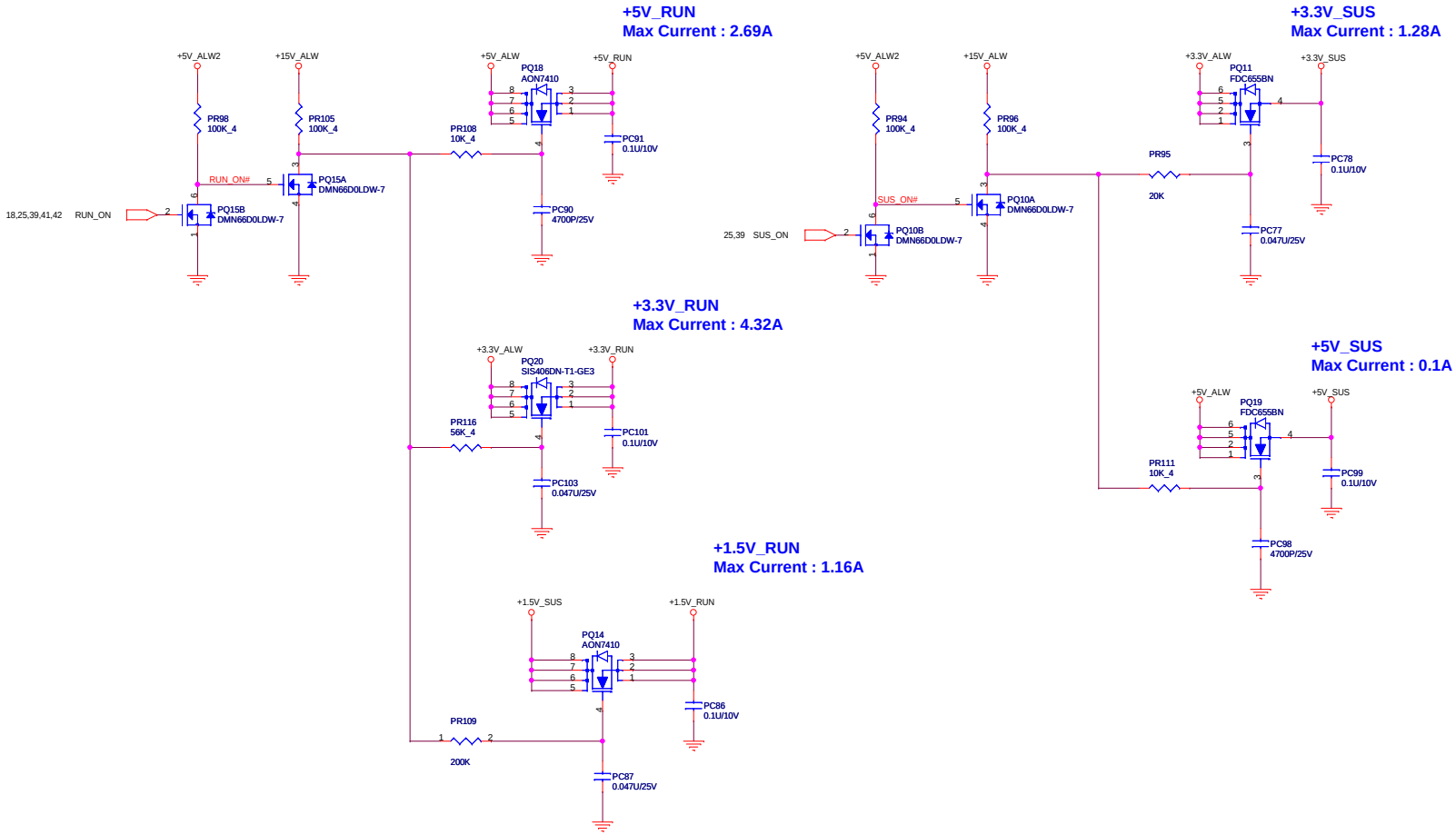

Quanta Computer Inc.		
PROJECT : V02/R01		
Size	Document Number: Load Switch	Rev: 1A
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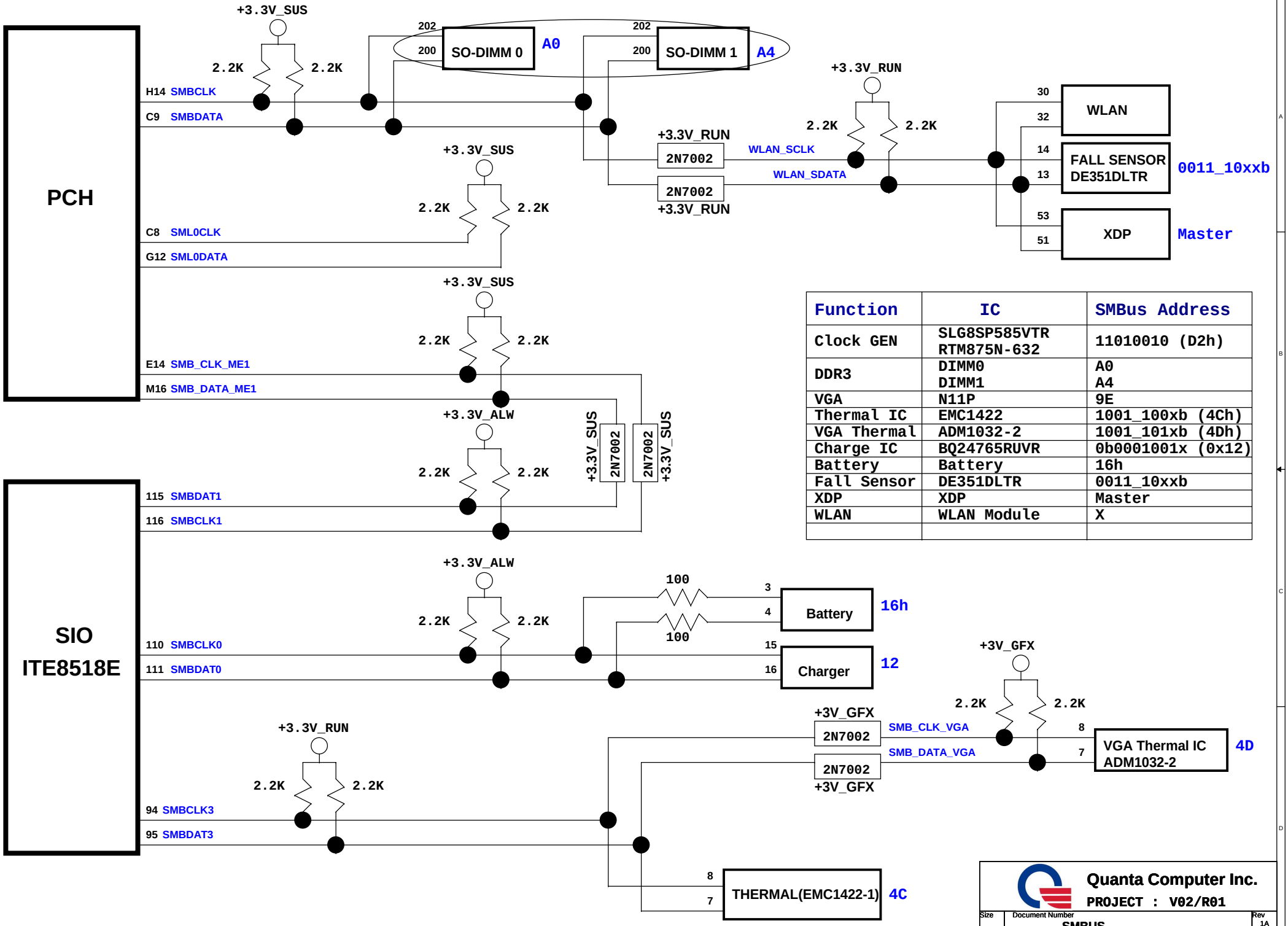

Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001_100xb (4Ch)
VGA Thermal	ADM1032-2	1001_101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011_10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

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Size	Document Number	Rev
	SMBUS	1A

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