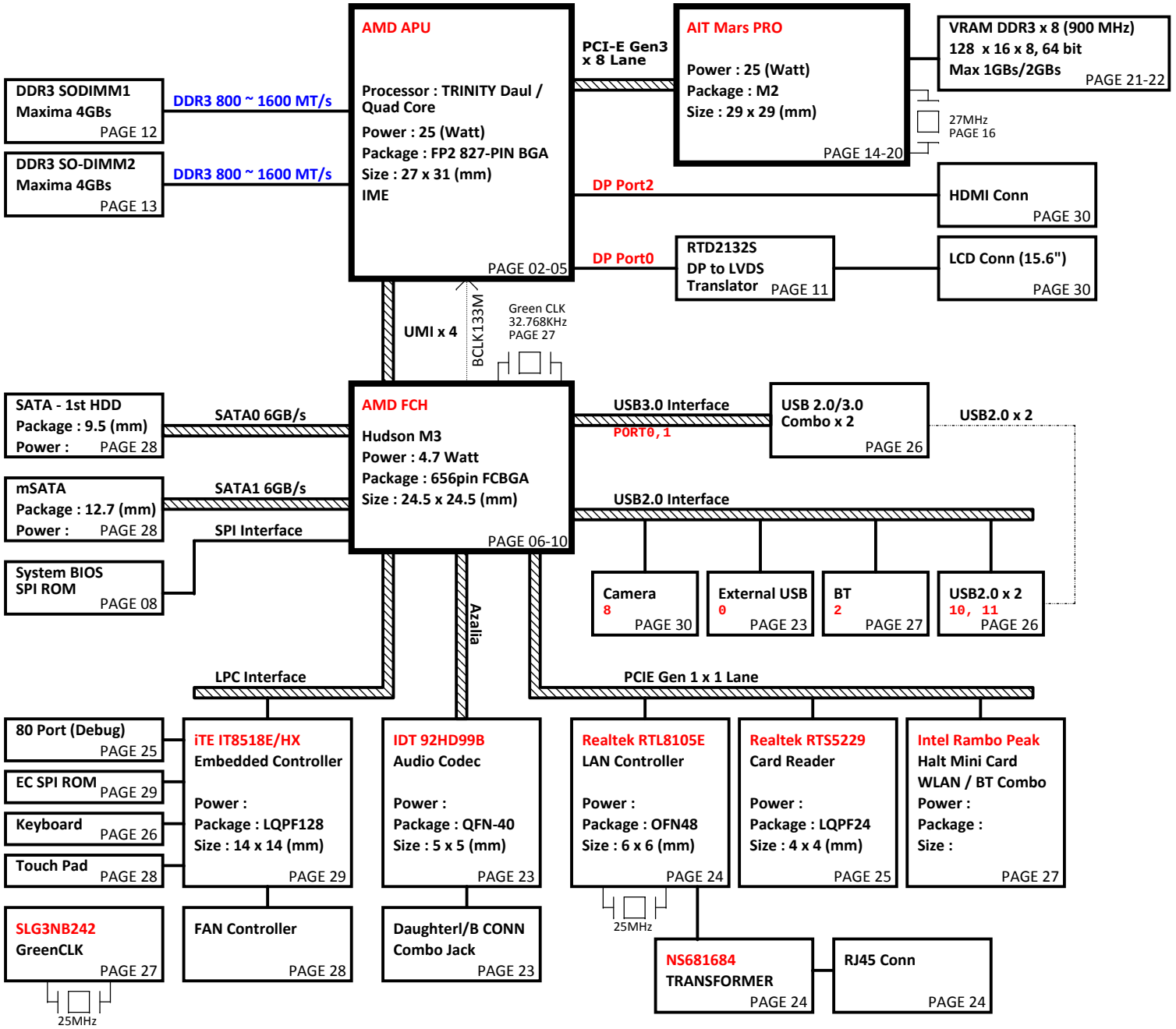
Volks_AMD Comal DIS/UMA (14") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power (+1.5V/+3V/+5V)
(+3VSUSV/+3VLANVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/ +3VS5/+5VS5)

ISL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/ +1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/ +0.75V_DDR_VTT)

Richtek RT8228AZ
PCH Power (+1.1VS5)

RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/ +1.5V_VGA/+1.8V_VGA/+VDDCI)

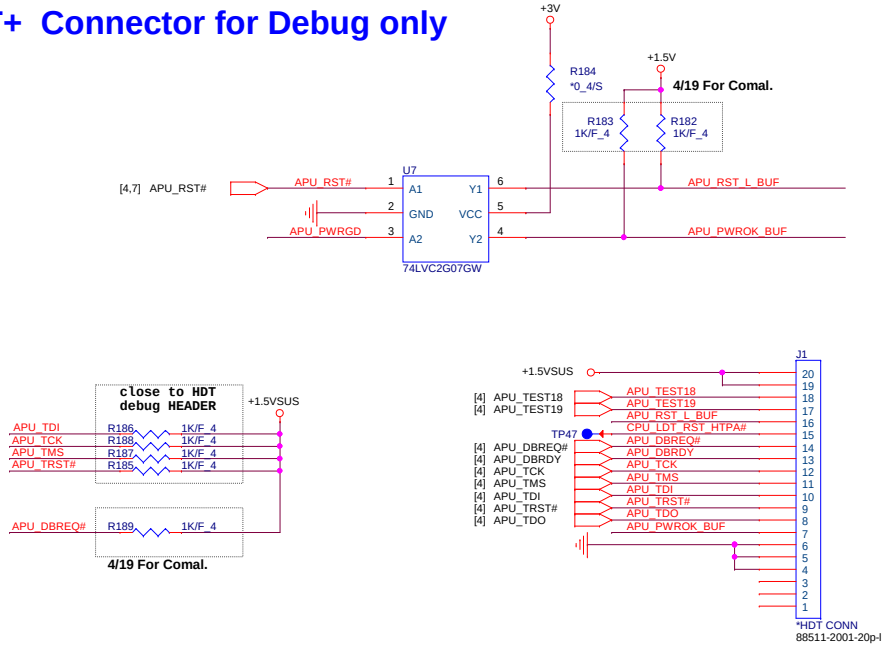
NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
A3	Block Diagram	1A

Date: Thursday, September 20, 2012 | Sheet 1 of 42

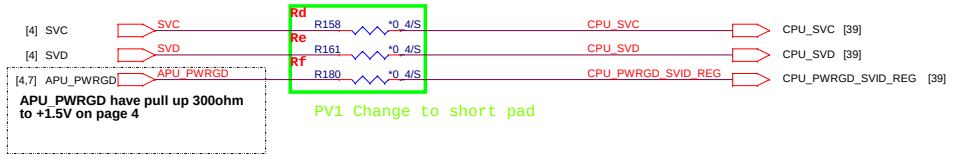
HDT+ Connector for Debug only



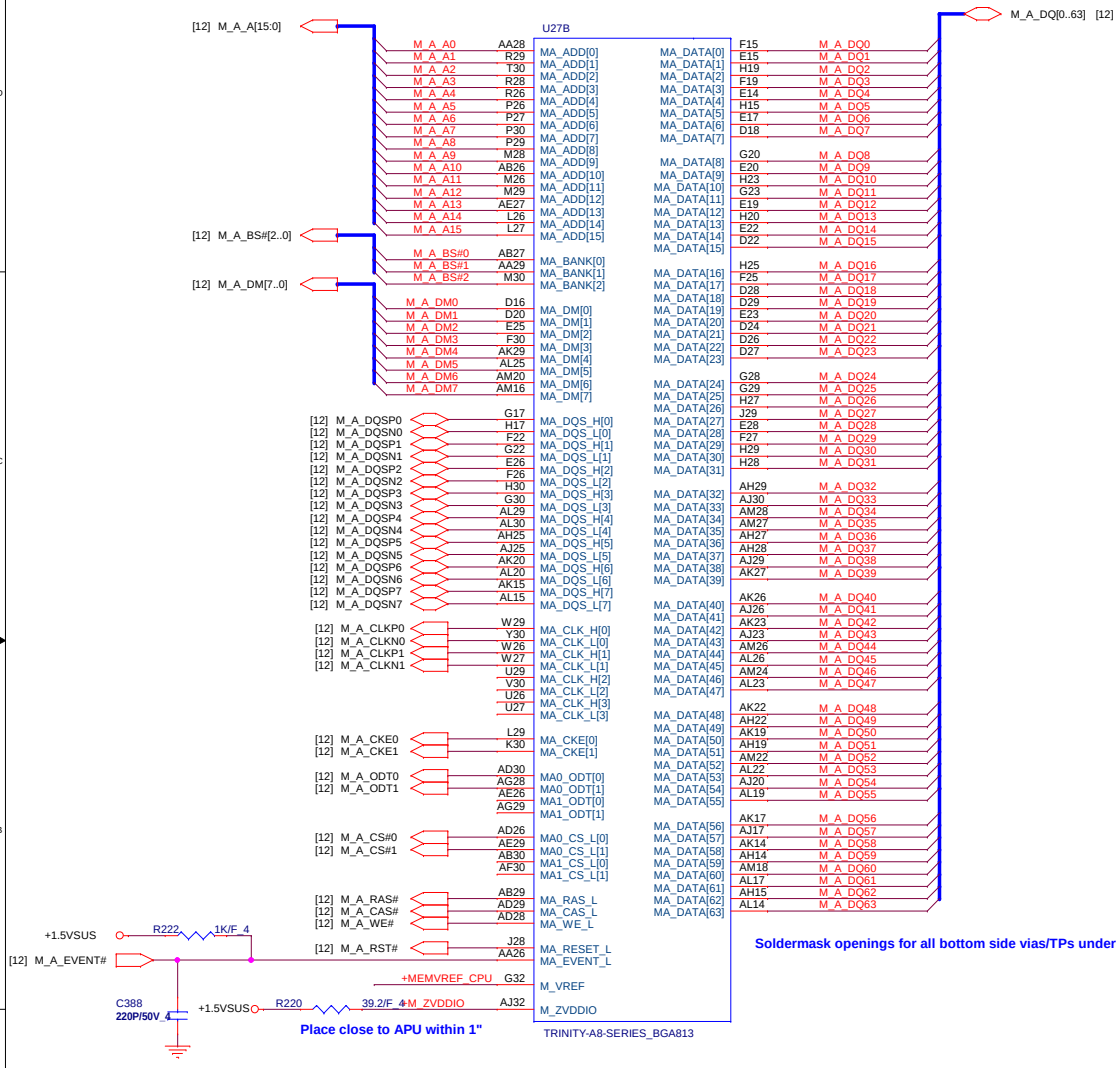
VID Override Circuit

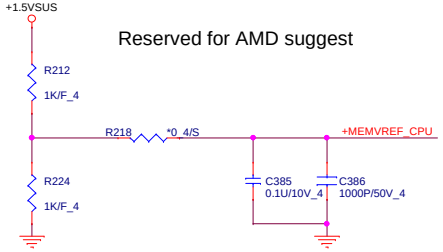
	BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

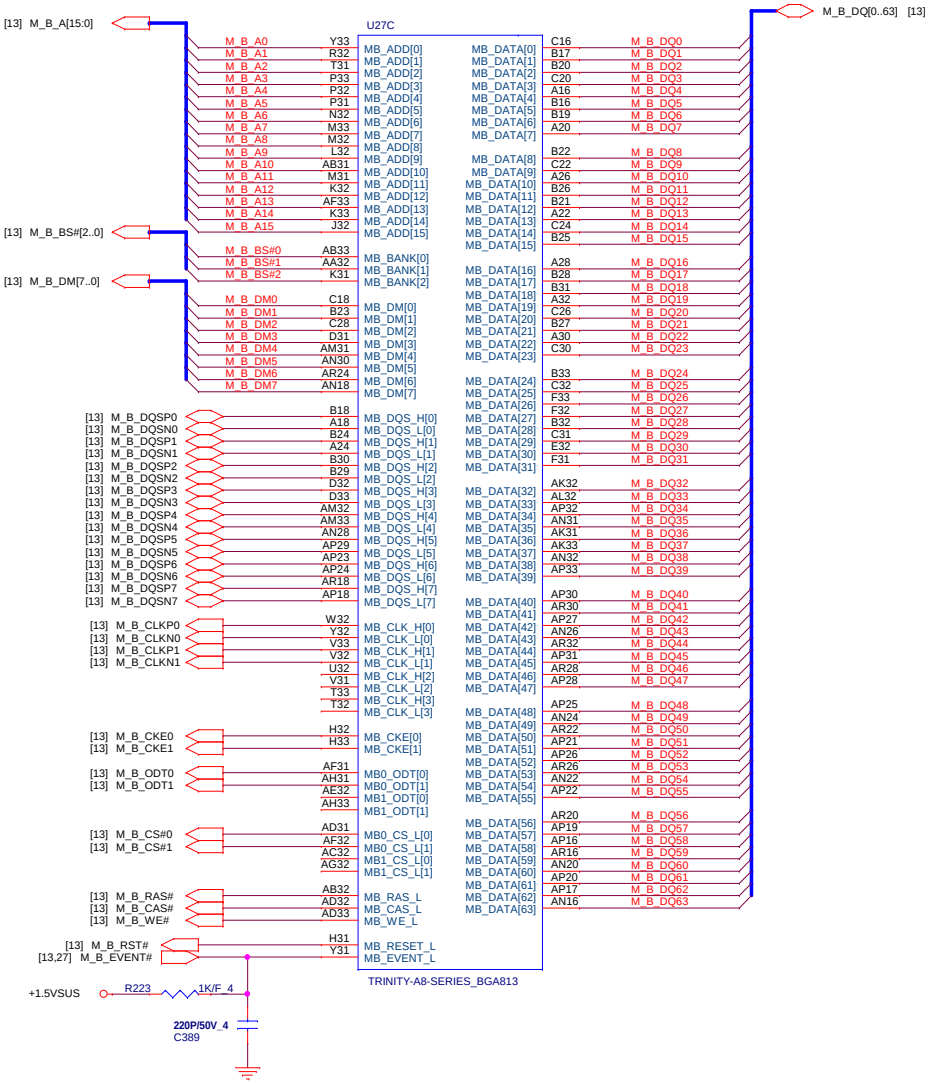
Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
	Size: Custom	Document Number: Llano PCIE/UMI/GPP	Rev: 1A
	Date: Thursday, September 20, 2012	Sheet 2 of 42	







NB5	**PROJECT : VOLKS_Comal 14"** Quanta Computer Inc.	
Size: Custom	Document Number: **Llano DDR3 MEM I/F**	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 3 of 42	

Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

U27D

LVDS

HDMI

4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

To AMD HDT

M_TEST CONNECTION TBD

7/8 For Comal.

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

DMAACTIVE_L controls
entry and exit from the
sleep and power states

PV1 add for HW thermal protect

SI

Thermal

THERMTRIP# shutdown temperature 125度C

4/19 For Comal,
close to APU.

PV1 change GPU thermal protect

PV1 add for HW thermal protect

ADD VGA TEMP_ FAIL function is active Hi

over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

TRINITY-A8-SERIES_BGA813

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	Size: — Document Number: Llano Display/Misc — Rev: 1A
Date: Thursday, September 20, 2012	Sheet 4 of 42

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

EMI suggestion

+VCC_CORE

C361 470P/50V_4 C333 *470P/50V_4 C360 *470P/50V_4

U27E

+VCC_CORE

36A
Maximum IDDspike 50A

C338 22U/6.3VS_8 C339 22U/6.3VS_8 C348 22U/6.3VS_8 C363 22U/6.3VS_8 C317 22U/6.3VS_8 C749 22U/6.3VS_8 C347 22U/6.3VS_8 C319 22U/6.3VS_8

C334 22U/6.3VS_8 C335 22U/6.3VS_8 C311 22U/6.3VS_8 C288 *22U/6.3VS_8 C318 *22U/6.3VS_8 C735 *22U/6.3VS_8 C325 *22U/6.3VS_8

C321 0.22U/10V_4 C354 0.22U/10V_4 C336 180P/50V_4 C341 180P/50V_4 C362 180P/50V_4 C364 0.01U/25V_4 C349 0.01U/25V_4 C352 0.01U/25V_4

+VDDNB_CORE

C762 22U/6.3VS_8 C788 22U/6.3VS_8 C763 22U/6.3VS_8 C764 22U/6.3VS_8

C294 0.22U/10V_4 C295 0.22U/10V_4 C293 180P/50V_4 C291 180P/50V_4 C292 180P/50V_4

+VDDNB_CAP

C300 22U/6.3VS_8 C297 22U/6.3VS_8 C298 22U/6.3VS_8 C299 22U/6.3VS_8 C289 180P/50V_4

+VDDP_CAP

C301 22U/6.3VS_8 C302 *22U/6.3VS_8

+VDDNB_CORE

+VDDNB_CAP

25A
Maximum IDDNBspike 33A

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

+1.5VSUS

C420 4.7U/6.3V_6 C511 4.7U/6.3V_6 C368 4.7U/6.3V_6 C426 4.7U/6.3V_6 C377 0.22U/10V_4 C378 0.22U/10V_4 C800 0.22U/10V_4 C802 0.22U/10V_4

If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows

+1.5VSUS

2.8A Up to DDR3-1333 @ 1.50V VDDIO

C455 0.22U/10V_4 C425 0.22U/10V_4 C458 0.22U/10V_4 C438 0.22U/10V_4 C479 0.22U/10V_4 C365 0.22U/10V_4

C432 180P/50V_4 C429 180P/50V_4 C481 180P/50V_4 C452 180P/50V_4 C373 180P/50V_4

C366 22U/6.3VS_8 C367 22U/6.3VS_8 C414 4.7U/6.3V_6 C421 4.7U/6.3V_6 C415 4.7U/6.3V_6 C369 4.7U/6.3V_6

+1.2V_VDDP

VDDP = 5A

+1.2V R427 *0_8/S +1.2V_VDDP

C770 22U/6.3VS_8 C772 0.22U/10V_4 C771 0.22U/10V_4 C769 22U/6.3VS_8

C774 180P/50V_4 C773 180P/50V_4 C768 *22U/6.3VS_8

+VDDP_CAP

TP43

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)

+1.2V_VDDR_B

C780 0.22U/10V_4 C778 0.22U/10V_4 C777 1000P/50V_4 C779 180P/50V_4 C776 180P/50V_4

R429 *0_8/S +1.2V

TRINITY-A8-SERIES_BGA813

VDDA= 0.75A

+2.5V L21 PBY160808T-221Y-N(220,2A) +2.5V_VDDA

C353 4.7U/6.3V_6 C350 0.22U/10V_4 C351 3300P/50V_4

U27F

TRINITY-A8-SERIES_BGA813

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Llano POWER/GND
Rev: 1A	
Date: Thursday, September 20, 2012	Sheet 5 of 42

+3VS5 NC,no install by default
R146 *2.2K_4 FCH_TEST0
R153 *2.2K_4 FCH_TEST1
R151 *2.2K_4 FCH_TEST2

+3V
R176 2.2K_4 SMB_RUN_CLK
R177 2.2K_4 SMB_RUN_DAT
to DDR3 SMBUS

+3VS5
R148 *1K/F_4 SYS_RST#
SYS_RST# internal 10K pull up

+3VS5
R134 10K/F_4 SCL3
R135 10K/F_4 SDA3
R130 10K/F_4 SCL2
R133 10K/F_4 SDA2
R142 2.2K_4 SCL1
R141 2.2K_4 SDA1
R143 *4.7K_4 FCH_THERMTRIP#
C273 *0.01U/25V_4
R375 10K/F_4 DNBSWON#

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull
Hi resistor from check list
CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V
GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5

This pin is used to power down VGA DAC regulators when CRT no connected

4/19 For Comal.
For Zero ODD

HD audio interface is +3V_S5 voltage

To Azalia

ACZ_SDOUT_R R411 33_4 ACZ_SDOUT_AUDIO [23]
ACZ_SYNC_R R412 33_4 ACZ_SYNC_AUDIO [23]
ACZ_BCLK_R R414 33_4 BIT_CLK_AUDIO [23]
ACZ_RST#_R R425 33_4 ACZ_RST#_AUDIO [23]
ACZ_SDIN0 ACZ_SDIN0 [23]
C275 *33P/50V_4
C280 33P/50V_4

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
[37] VGA_REQ 1 D21 2 CLKREQ1# *RB501V-40
R440 10K/F_4
[36,37,38] DGPU_PWROK 2 Q20 *MMBT3904-7-F 3 1

HUDSON-M3

Part 4 of 5

TP100 PCIE_RST2# AB6
TP92 RI# R2
W7
[29] SUSB# SUSB# T3
[29] SUSC# SUSC# W2
[29] DNBSWON# DNBSWON# J4
[10] FCH_PWRGD FCH_PWRGD N7
FCH_TEST0 T9
TP20 FCH_TEST1 T10
FCH_TEST2 V9
EC_A20GATE AE22
EC_RCIN# AG19
FCH_PME# R9
TP18 SIO_EXT_SMI# C26
[29] SIO_EXT_SMI# GEVENT5# T5
[29] SIO_EXT_SCI# R406 *0_4/S SYS_RST# U4
PCIE_WAKE# K1
[24,27] PCIE_WAKE# C734 *100P/50V_4 V7
[4] FCH_THERMTRIP# FCH_THERMTRIP# R10
+3V R171 10K/F_4 WD_PWRGD AF19
[29] RSMRST# RSMRST# U2
[25] PCIE_CLKREQ_CR# PCIE_CLKREQ_CR# AG24
[24] PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# AE24
AE26
AF22
AH17
AG18
AF24
[23] SPKR R432 *0_4/S FCH_GPIO66 AD26
[12,13] SMB_RUN_CLK SMB_RUN_CLK AD25
[12,13] SMB_RUN_DAT SMB_RUN_DAT T7
[11,28] SCL1 SCL1 R7
[11,28] SDA1 SDA1 AG25
[27] PCIE_CLKREQ_WLAN# CLKREQ1# AG22
[27] RF_OFF1# RF_OFF1# J2
TP38 SMARTVOLT2 AG26
TP21 VGA_PD V8
TP22 GBE_LED0 W8
Y6
V10
AA8
TP28 AF25
TP81 M7
R8
TP97 ODD_PLUGIN# T1
P6
F5
TP14 P5
TP91 FCH_JTAG_TCK J7
TP80 FCH_JTAG_TDI T8
TP19 FCH_JTAG_RST#
R415 *10K/F_4 ACZ_BCLK_R AB3
ACZ_SDOUT_R AB1
R408 *10K/F_4 ACZ_SDIN0 AA2
R403 *10K/F_4 ACZ_SDIN1 Y5
R409 *10K/F_4 ACZ_SDIN2_R Y3
R402 *10K/F_4 ACZ_SDIN3_R Y1
ACZ_SYNC_R AD6
ACZ_RST#_R AE4
TP15 K19
TP12 J19
J21
[27] BT_COMBO_OFF# BT_COMBO_OFF# D21
C20
[14] VGA_RSTB VGA_RSTB D23
[29] VGA_ON_SB VGA_ON_SB C22
F21
E20
F20
A22
E18
A20
J18
H18
G18
B21
K18
D19
A18
C18
B19
B17
A24
D17

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226

ACPI / WAKE UP EVENTS
GPIO
USB 2.0
USB OC
HD AUDIO
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC G8
USB_RCOMP B9 USB_RCOMP_SB R365 11.8K/F_6
USB_FSD1P/GPIO186 H1
USB_FSD1N H3
USB_FSD0P/GPIO185 H6
USB_FSD0N H5
USB_HSD13P H10
USB_HSD13N G10
USB_HSD12P K10
USB_HSD12N J12
USB_HSD11P G12 USBP11+ USBP11+ [26]
USB_HSD11N F12 USBP11- USBP11- [26] USB Combo 3.0/2.0.
USB_HSD10P K12 USBP10+ USBP10+ [26]
USB_HSD10N K13 USBP10- USBP10- [26] USB Combo 3.0/2.0.
USB_HSD9P B11
USB_HSD9N D11
USB_HSD8P E10 USBP8+ USBP8+ [30]
USB_HSD8N F10 USBP8- USBP8- [30] CAMERA
USB_HSD7P C10
USB_HSD7N A10
USB_HSD6P H9
USB_HSD6N G9
USB_HSD5P A8
USB_HSD5N C8
USB_HSD4P F8
USB_HSD4N E8
USB_HSD3P C6
USB_HSD3N A6
USB_HSD2P C5 USBP2+ [27]
USB_HSD2N A5 USBP2- [27] WLAN Min-Card
USB_HSD1P C1
USB_HSD1N C3
USB_HSD0P E1 USBP0+ [23]
USB_HSD0N E3 USBP0- [23] EXternal MIC LEFT side USB 2.0 Connector
USBSS_CALRP C16 R366 1K/F_4
USBSS_CALRN A16 R358 1K/F_4 +FCH_VDD_11_SSUSB_S
USB_SS_TX3P A14
USB_SS_TX3N C14 USB 3.0 Not Implemented: left unconnected.
USB_SS_RX3P C12
USB_SS_RX3N A12
USB_SS_TX2P D15
USB_SS_TX2N B15
USB_SS_RX2P E14
USB_SS_RX2N F14
USB_SS_TX1P F15 USB30_TX1+ [26]
USB_SS_TX1N G15 USB30_TX1- [26]
USB_SS_RX1P H13 USB30_RX1+ [26]
USB_SS_RX1N G13 USB30_RX1- [26]
USB_SS_TX0P J16 USB30_TX0+ [26]
USB_SS_TX0N H16 USB30_TX0- [26]
USB_SS_RX0P J15 USB30_RX0+ [26]
USB_SS_RX0N K15 USB30_RX0- [26]
SCL2/GPIO193 H19 SCL2
SDA2/GPIO194 G19 SDA2
SCL3_LV/GPIO195 G22 SCL3
SDA3_LV/GPIO196 G21 SDA3
E22
EC_PWM0/EC_TIMER0/GPIO197 H22
EC_PWM1/EC_TIMER1/GPIO198 J22 EC_PWM2
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 H21 EC_PWM2 [10]
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201 K21
KSI_1/GPIO202 K22
KSI_2/GPIO203 F22
KSI_3/GPIO204 F24
KSI_4/GPIO205 E24
KSI_5/GPIO206 B23
KSI_6/GPIO207 C24
KSI_7/GPIO208 F18

No need for GPIO200

SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

Hudson-M3-A14

HUDSON-M3

Part 1 of 5

Place these PICE AC coupling cap close to FCH

SI , change to 22Ω & 47Ω for Rise/Fall time issue

9/18 add RP7/RP8 for CLK Slew Rate

Note: CLK_FCH_SRCP/N is 100MHZ SSC

Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_PCIE_VGAP/N is 100MHZ SSC

Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable

PV2 change to non-stuff for Green Clock solution

Add G-sensor signal

PV2 change to non-stuff for Green Clock solution

FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS

PV change to short-pad

LDT_STP# let is NC from schematic recommend

PV2 change to non-stuff for Green Clock solution

S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation

X'tal Stuff'R139 change to 0hm.
Green CLK Stuff'R139 change to 510ohm.

INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).

Hudson-M3-A14

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	Hudson-M3 ACPI/PCI/CLOCK
Size: Custom	Document Number: Hudson-M3 ACPI/PCI/CLOCK
Rev: 1A	
Date: Thursday, September 20, 2012	Sheet 7 of 42

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

U25D

HUDSON-M3

Part 5 of 5

GROUND

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64

VSSAN_HWM

VSSXL

VSSPL_SYS

VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128

VSSPL_DAC VSSAN_DAC VSSANQ_DAC VSSIO_DAC

EFUSE

Hudson-M3-A14

PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

MINISATA

[28] SATA_TXP0 SATA_TXN0 [28] SATA_RXN0 SATA_RXP0 [28] SATA_TXP1 SATA_TXN1 [28] SATA_RXN1 SATA_RXP1

SATA_TXP0 SATA_TXN0 SATA_TXP1 SATA_TXN1

SATA_TX0P SATA_TX0N SATA_RX0N SATA_RX0P SATA_TX1P SATA_TX1N SATA_RX1N SATA_RX1P SATA_TX2P SATA_TX2N SATA_RX2N SATA_RX2P SATA_TX3P SATA_TX3N SATA_RX3N SATA_RX3P SATA_TX4P SATA_TX4N SATA_RX4N SATA_RX4P SATA_TX5P SATA_TX5N SATA_RX5N SATA_RX5P

[28] SATA_LED# R170 *0_4/S SB_SATA_LED#

PV , change to short pad

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

+1.1V_AVDD_SATA R163 1K/F_4 R159 931/F_4 SATA_CALRP SATA_CALRN

4/19 For Comal.

+3V R178 *220/F_6 SB_SATA_LED#

SATA_ACT#/GPIO67

SATA_X1

Integrated Clock Mode: Leave unconnected.

SATA_X2

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

U25B

HUDSON-M3

Part 2 of 5

SERIAL ATA

SD CARD

SD_CLK/SCLK_2/GPIO73 SD_CMD/SLOAD_2/GPIO74 SD_CD#/GPIO75 SD_WP/GPIO76 SD_DATA0/SDATI_2/GPIO77 SD_DATA1/SDATO_2/GPIO78 SD_DATA2/GPIO79 SD_DATA3/GPIO80

GBE LAN

GBE_COL GBE_CRS GBE_MDCK GBE_MDIO GBE_RXCLK GBE_RXD3 GBE_RXD2 GBE_RXD1 GBE_RXD0 GBE_RXCTL/RXDV GBE_RXERR GBE_TXCLK GBE_TXD3 GBE_TXD2 GBE_TXD1 GBE_TXD0 GBE_TXCTL/TXEN GBE_PHY_PD GBE_PHY_RST# GBE_PHY_INTR

GBE_PHY_INTR R147 10K/F_4 +3VS5

+3VS5 R444 10K/F_4

SPI_CS0# *0_4/S R445 SPI_CLK *0_4/S R443 SPI_SO *0_4/S R442 SPI_SI *0_4/S R446

EC_BIOS_CS# [29] EC_BIOS_SPI_CLK_I [29] EC_BIOS_WR# [29] EC_BIOS_RD# [29]

SPI ROM

SPI_DI/GPIO164 SPI_DO/GPIO163 SPI_CLK/GPIO162 SPI_CS1#/GPIO165 ROM_RST#/SPI_WP#/GPIO161

V6 SPI_SI V5 SPI_SO V3 SPI_CLK T6 SPI_CS0# V1 FCH_SPI_WP

TP104 TP103 TP107 TP108 TP98

VGA DAC

VGA_RED VGA_GREEN VGA_BLUE VGA_HSYNC/GPO68 VGA_VSYNC/GPO69 VGA_DDC_SDA/GPO70 VGA_DDC_SCL/GPO71 VGA_DAC_RSET

L30 L32 M29 M28 N30 M33 N32 K31 TP87

VGA MAINLINK

AUX_VGA_CH_P AUX_VGA_CH_N AUXCAL ML_VGA_L0P ML_VGA_L0N ML_VGA_L1P ML_VGA_L1N ML_VGA_L2P ML_VGA_L2N ML_VGA_L3P ML_VGA_L3N ML_VGA_HPD/GPO229

V28 V29 U28 TP95 T31 T33 T29 T28 R32 R30 P29 P28 C29 TP13

HW MONITOR

FANOUT0/GPIO52 FANOUT1/GPIO53 FANOUT2/GPIO54 FANIN0/GPIO56 FANIN1/GPIO57 FANIN2/GPIO58 TEMPIN0/GPIO171 TEMPIN1/GPIO172 TEMPIN2/GPIO173 TEMPIN3/TALERT#/GPIO174

VIN0/GPIO175 VIN1/GPIO176 VIN2/SDATI_1/GPIO177 VIN3/SDATO_1/GPIO178 VIN4/SLOAD_1/GPIO179 VIN5/SCLK_1/GPIO180 VIN6/GBE_STAT3/GPIO181 VIN7/GBE_LED3/GPIO182

N2 SIDE_PORT_ID0 M3 SIDE_PORT_ID1 L2 SIDE_PORT_ID2 N4 BOARD_ID0 P1 BOARD_ID1 P3 BOARD_ID2 M1 BOARD_ID3 M5 BOARD_ID4

NC1 NC2 NC3 NC4 NC5

AG16 AH10 A28 G27 L4

VIN (0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

[27] RF_OFF# RF_OFF# BT_OFF# BT_COMBO_EN# TP99 TP39

[28] ACC_LED# [30] LCD_BK LCD_BK

TEMPIN0 TEMPIN1 TEMPIN2 TEMPIN3

R136 10K/F_4 R137 10K/F_4 R378 10K/F_4 R138 10K/F_4

TEMP (0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

+3VS5 R395 *10K/F_4 BOARD_ID0 R396 10K/F_4
R398 *10K/F_4 BOARD_ID1 R399 10K/F_4
R400 *10K/F_4 BOARD_ID2 R401 10K/F_4
R386 *10K/F_4 BOARD_ID3 R387 10K/F_4
R390 *10K/F_4 BOARD_ID4 R391 10K/F_4
R392 10K/F_4 SIDE_PORT_ID0 R393 *10K/F_4
R384 10K/F_4 SIDE_PORT_ID1 R385 *10K/F_4
R379 *10K/F_4 SIDE_PORT_ID2 R380 10K/F_4

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 SATA/HWM/SPI	1A

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U25C

HUDSON-M3 Part 3 of 5

Hudson-M3-A14

VDDQ--3.3V I/O power 102mA

PV1 Change to short pad

VDDAN_11_ML -- UMI 1.1V analog power

VDDPL_33_USB_S : USB PHY PLL analog power

VDDAN_33_USB_S : USB PHY I/O analog power

VDDAN_11_USB_S : USB PHY PLL analog power

VDDCR_11_USB_S : USB PHY core power

M3 chipset need to stuff for support USB3.0

SI , AMD SR tool review

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power

VDDCR_11_SSUSB_S : USB3.0 PHY core power

if support Modem wake up should be change pull hi to S5 power

1007mA for M3
902mA for M2

VDDCR-- S/B CORE power

VDDAN_11_CLK-- Internal clock Generator I/O power

VDDAN_11_PCIE --PCIE/UMI analog power

VDDPL_11_SYS_S : System Clock Gen PLLs analog power

VDDAN_11_SATA--SATA PHY analog/IO power

if support USB 3.0 wake up should be change pull hi to S5 power

VDDIO_33_S-- 3.3v S5 I/O power

VDDXL_33_S-- 25MHZ XTAL IO power

VDDCR_1.1_S-- 1.1V S5 Core power

if support USB 3.0 wake up should be change pull hi to S5 power

M3 chipset need to stuff for support USB3.0

PROJECT :	VOLKS_Comal 14"
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Hudson-M3 POWER/GND
Rev: 1A	
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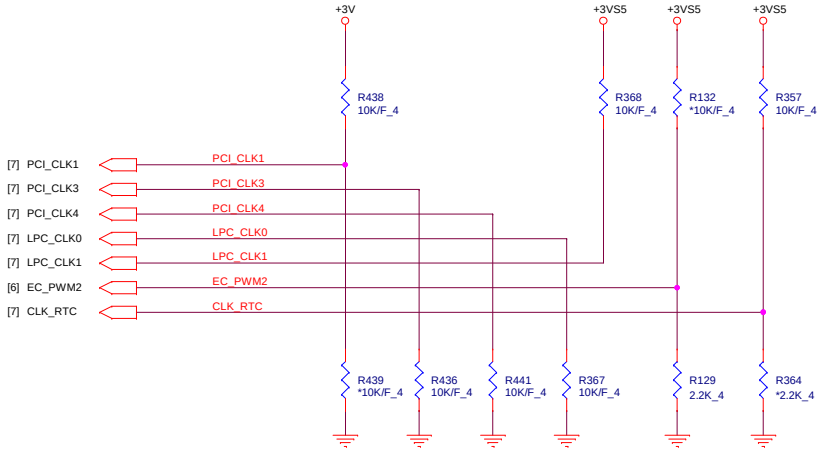
STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

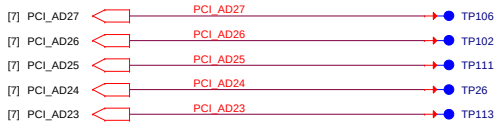


REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

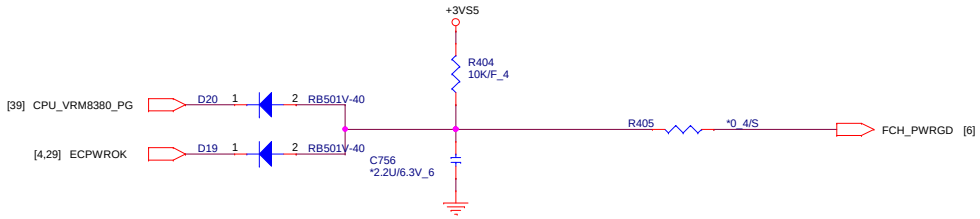
FCH has 15K Internal Pull Up for PCI_AD[27:23]



remove reserve pull low resistor
reserve test point only.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

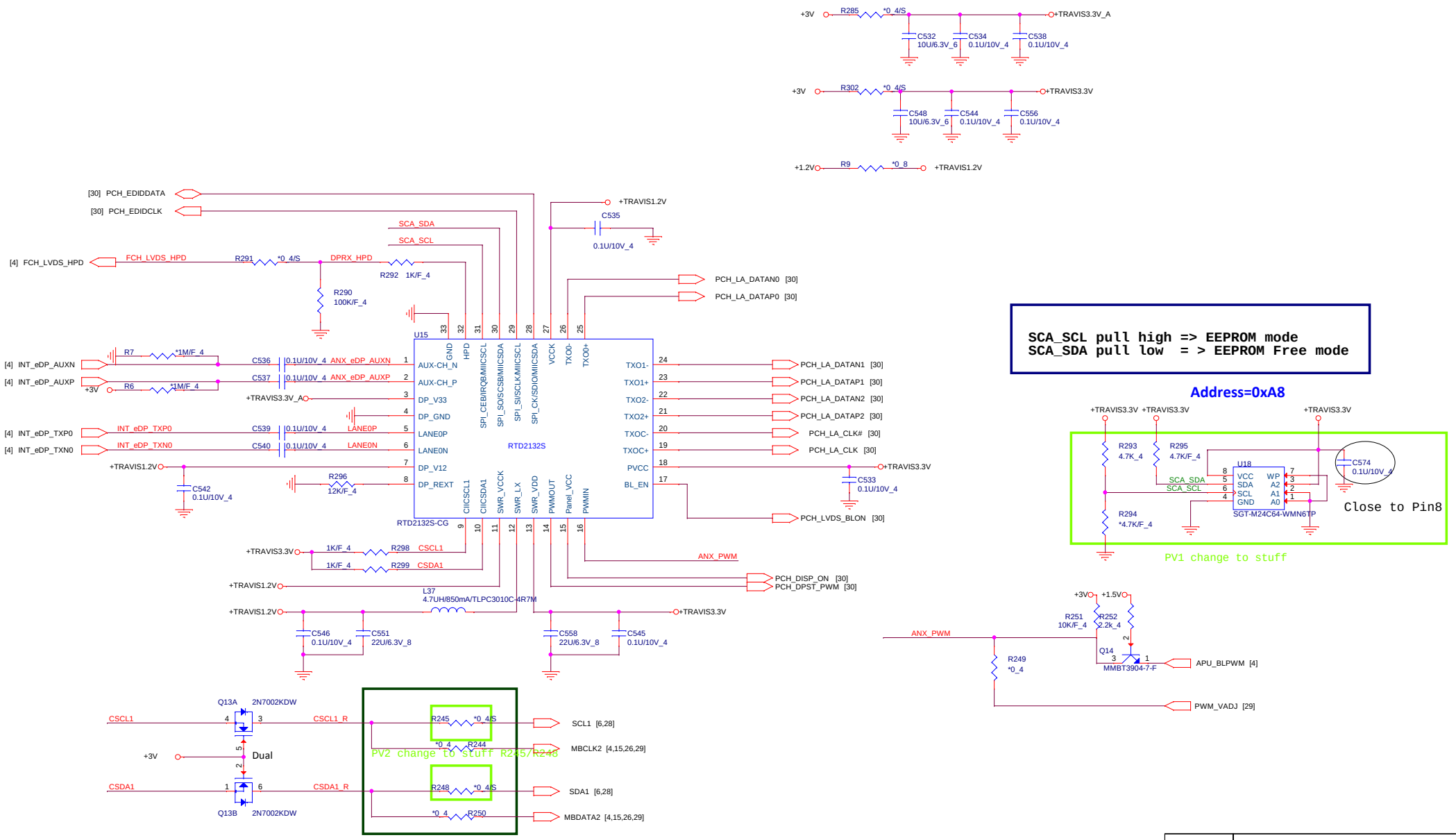


NB5

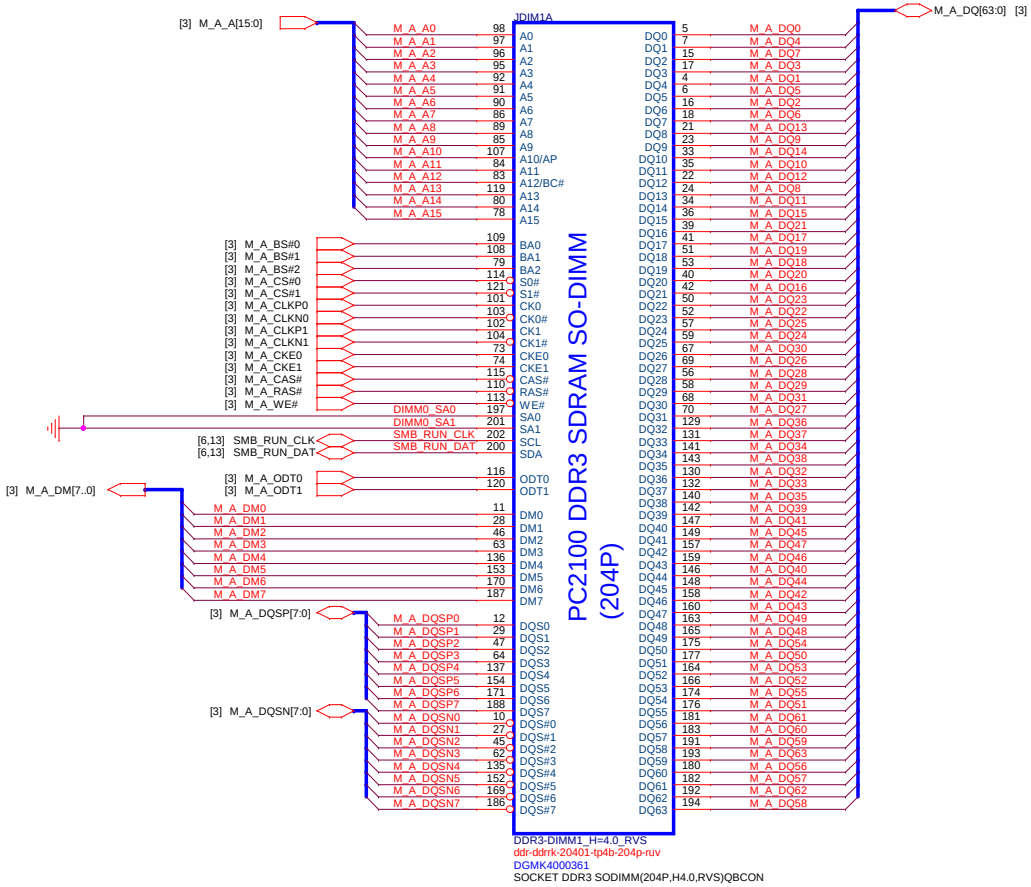
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

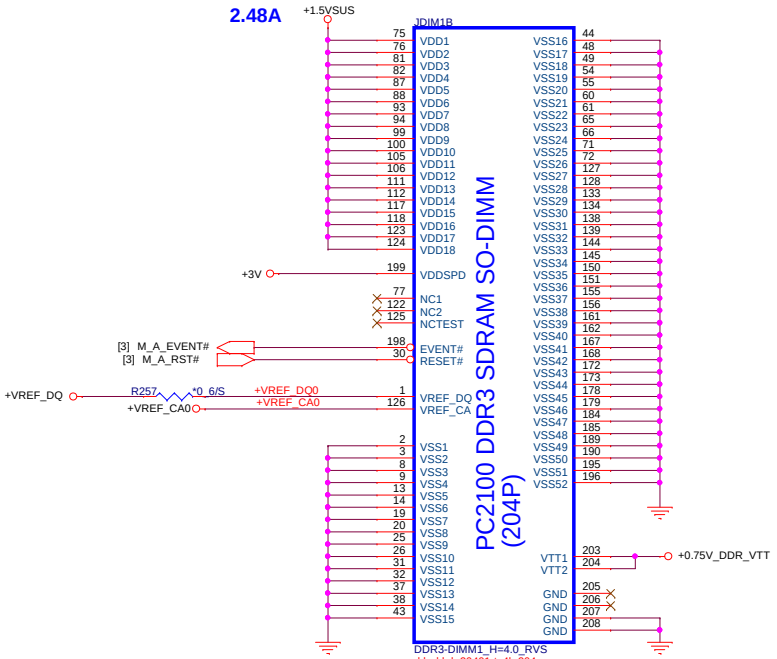
Size	Document Number	Rev
Custom	Hudson-M3 STRAP/PWRGD	1A

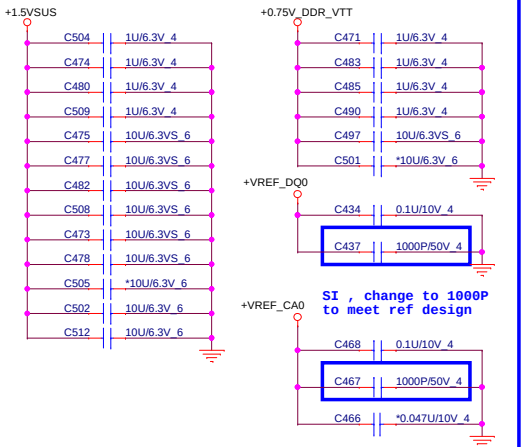
Date: Thursday, September 20, 2012 | Sheet 10 of 42

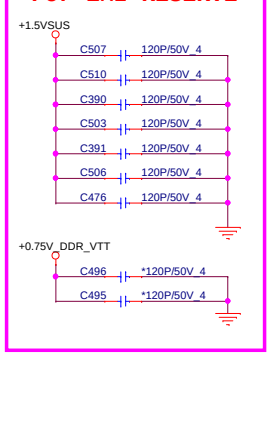


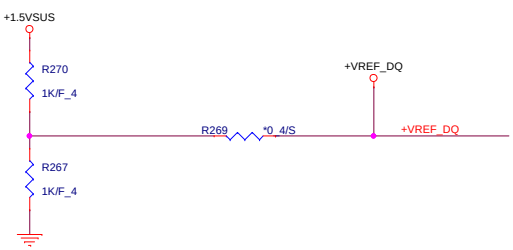
NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: RTD2132S	Rev: 1A
Date: Thursday, September 20, 2012	Sheet 11 of 42	



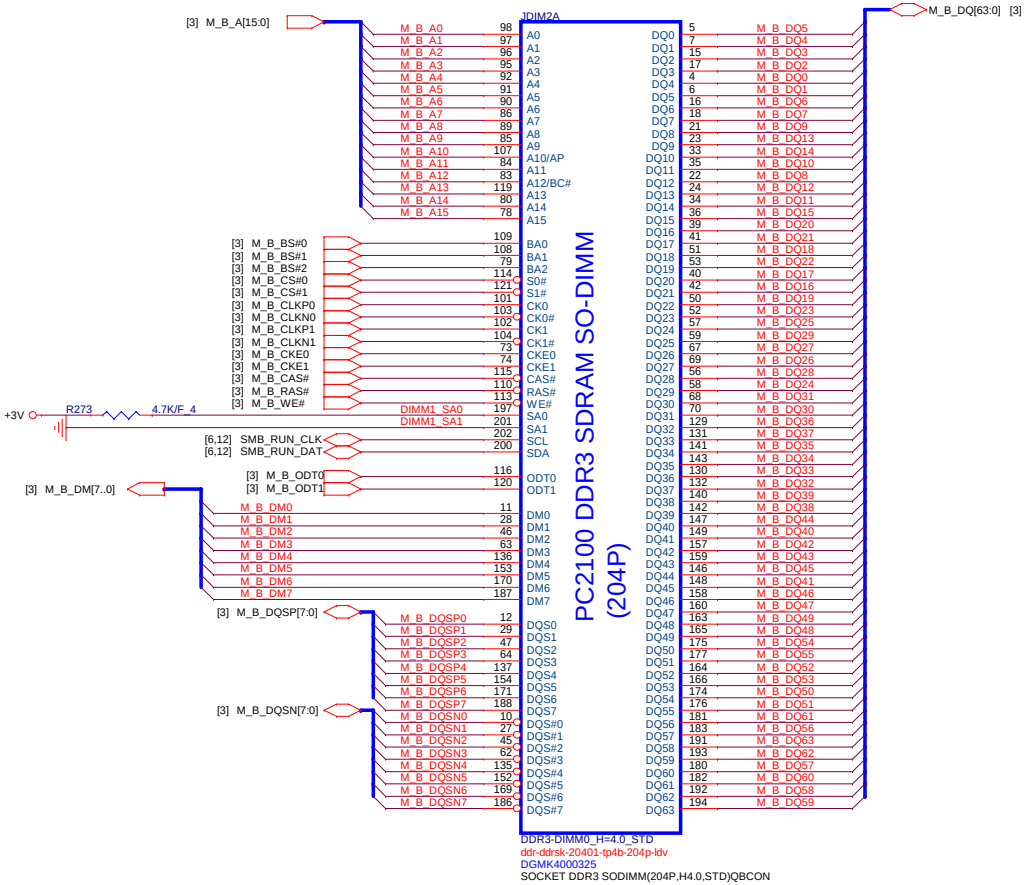


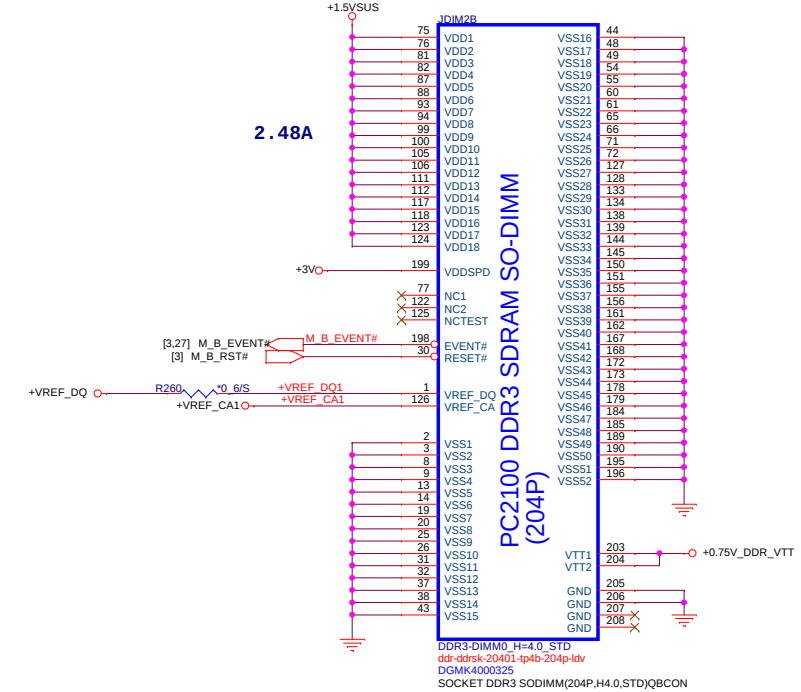






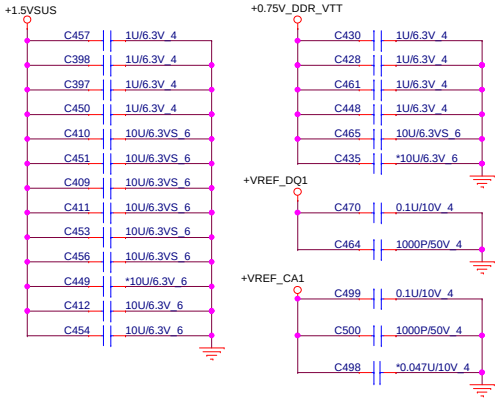
NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 1/2 (5.2H)	Rev: 1A
Date: Thursday, September 20, 2012	Sheet: 12of	42



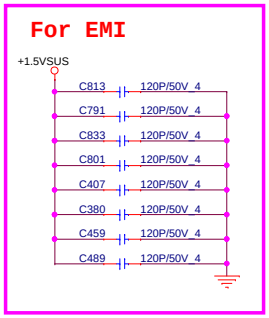


[2,4,6,8,9,10,11,12,14,23,24,25,26,27,28,29,30,36,37,38,41] +3V
[2,3,4,5,12,35,37,41] +1.5VSUS
[12,35] +0.75V_DDR_VTT

Place these Caps near So-Dimm1.



For EMI



PROJECT : VOLKS_Comal 14"

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A

Date: Thursday, September 20, 2012 | Sheet 13of 42

FOR Mars support Gne3: AC cap nees use 0.22u
FOR Thems: AC cap need use 0.1u for Gen2

U21A
PART 1 OF 9

[2] PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	C_PEG_RXP0	C202	*0.22U/10V_4	PEG_RXP0 [2]
[2] PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	C_PEG_RXN0	C203	*0.22U/10V_4	PEG_RXN0 [2]
[2] PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	C_PEG_RXP1	C190	*0.22U/10V_4	PEG_RXP1 [2]
[2] PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	C_PEG_RXN1	C191	*0.22U/10V_4	PEG_RXN1 [2]
[2] PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	C_PEG_RXP2	C200	*0.22U/10V_4	PEG_RXP2 [2]
[2] PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	C_PEG_RXN2	C201	*0.22U/10V_4	PEG_RXN2 [2]
[2] PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	C_PEG_RXP3	C187	*0.22U/10V_4	PEG_RXP3 [2]
[2] PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	C_PEG_RXN3	C186	*0.22U/10V_4	PEG_RXN3 [2]
[2] PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	C_PEG_RXP4	C204	*0.22U/10V_4	PEG_RXP4 [2]
[2] PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	C_PEG_RXN4	C197	*0.22U/10V_4	PEG_RXN4 [2]
[2] PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	C_PEG_RXP5	C188	*0.22U/10V_4	PEG_RXP5 [2]
[2] PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	C_PEG_RXN5	C189	*0.22U/10V_4	PEG_RXN5 [2]
[2] PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	C_PEG_RXP6	C199	*0.22U/10V_4	PEG_RXP6 [2]
[2] PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	C_PEG_RXN6	C198	*0.22U/10V_4	PEG_RXN6 [2]
[2] PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	C_PEG_RXP7	C195	*0.22U/10V_4	PEG_RXP7 [2]
[2] PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	C_PEG_RXN7	C194	*0.22U/10V_4	PEG_RXN7 [2]
	N38	PCIE_RX8P	PCIE_TX8P	N33				
	M37	PCIE_RX8N	PCIE_TX8N	N32				
	M35	PCIE_RX9P	PCIE_TX9P	N30				
	L36	PCIE_RX9N	PCIE_TX9N	N29				
	L38	PCIE_RX10P	PCIE_TX10P	L33				
	K37	PCIE_RX10N	PCIE_TX10N	L32				
	K35	PCIE_RX11P	PCIE_TX11P	L30				
	J36	PCIE_RX11N	PCIE_TX11N	L29				
	J38	PCIE_RX12P	PCIE_TX12P	K33				
	H37	PCIE_RX12N	PCIE_TX12N	K32				
	H35	PCIE_RX13P	PCIE_TX13P	J33				
	G36	PCIE_RX13N	PCIE_TX13N	J32				
	G38	PCIE_RX14P	PCIE_TX14P	K30				
	F37	PCIE_RX14N	PCIE_TX14N	K29				
	F35	PCIE_RX15P	PCIE_TX15P	H33				
	E37	PCIE_RX15N	PCIE_TX15N	H32				

PCI EXPRESS INTERFACE

For Mars NC pin :
N38,M37,M35,L36,L38,K37,K35,J36,J38
H37,H35,G36,G38,F37,F35,E37

FOR Mars NC pin :
N33,N32,N30,N29,L33,L32,L30,L29,K33,K32
J33,J32,K30,K29,H33,H32

CLOCK
[7] CLK_VGA_P — CLK_VGA_P — AB35 — PCIE_REFCLKP
[7] CLK_VGA_N — CLK_VGA_N — AA36 — PCIE_REFCLKN

Install for Mars/ Chelsea
R69 Ra *1K/F_4 — AH16 — TEST_PG

PEGX_RST# — AA30 — PERSTB

*MARS_M2_PRO

CALIBRATION
PCIE_CALR_TX — Y30 — PCIE_CALRP
PCIE_CALR_RX — Y29 — PCIE_CALRN

Mars/ Chelsea Only : Stuff Ra
Do not install For Thames

R373 Ra *1.69K/F_4 — +1.0V_VGA

Install for Thames ONLY: Stuff Rb
Do not install for Chelsea

R371 Rb *1.27K/F_4
R372 Rc *1K/F_4 — +1.0V_VGA

Install 2k for Thames
Install 1k for Mars

	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

+3V
C748 *0.1U/10V_4
*TC7SH08FU U24
[7] GPU_RST#
[6] VGA_RSTB
R383 *330_4 DGPU_HIN_RST#
PEGX_RST#
R374 *100K_4

[16,18,19,37] +1.0V_VGA — +1.0V_VGA

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
NB5
Size: Custom | Document Number: Mars_PCIE_Interface | Rev: 1A
Date: Thursday, September 20, 2012 | Sheet 14 of 42

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D (VEGA)	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- B (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63BFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110	Reserve		
0111	Reserve		
1000	Reserve		
1001	Hynix- D (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63DFR-11C
1010			
1011			
1100			
1101			
1110			
1111			

GPIO30 GPIO12 GPIO16 GPIO20 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
0	0	0	0	0	1.0V
0	0	0	0	1	0.9V
0	0	0	1	0	0.875V
0	0	0	1	1	0.85V
0	0	1	0	0	0.8V
0	0	1	0	1	0.75V

For Mars only : AR1/AW8/AR3/AR8/AU8: all NC pin

For Mars only : DP A to D Port: all NC pin

Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

Mars / Chelsea : AVSSN must be short to gnd

GPIO29, 30 are NC on Thems/ whistler/ Seymour

Thames INSTALL Ra,Rb.

Do not install for Mars/ Chelsea
PS_0 should be tied to GND on Thames

PS_1,PS_2, PS_3 are NC on Thames
Do not install for Thames

Thermal Solution(Close to GPU)

Main:AL0000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Reserve for Power Play

For Mars: Stuff Ra only=> VDDC 1.1V
For Thems: Stuff Ra, Rb=> VDDC 1.0V

For Mars:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

PV, change to 0ohm

PV, change to 0ohm

PV, change to DNI

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT0

PS0 => 11001
PS1 => 00001
PS2 => 00000
PS3 => 11000

[14,16,18,19,37] +1.0V_VGA → +1.0V_VGA
[16,18,19,38] +1.8V_VGA → +1.8V_VGA
[17,18] +3V_DELAY → +3V_DELAY

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
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Fo Mars/ Chelsea
Change La, Lb
Bead to 0 ohm
For Thems: La,Lb:
CX8PG471000/BLM18PG471SN1D/1A_6

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

La
+1.8V_VGA L9 *0_6 +1.8V_DPLL_PVDD
C173 *10U/6.3V_8 C175 *1U/6.3V_4 C174 *0.1U/10V_4
Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

Lb
+1.0V_VGA L8 *0_6 +1.0V_DPLL_VDDC
C165 *10U/6.3V_8 C171 *1U/6.3V_4 C166 *0.1U/10V_4
1.0V(125mA DPLL_VDDC)
DPLL_VDDC : 0.935V @ 140mA
DPLL_PVSS

+1.8V_MPLL_PVDD
*BLM18PG471SN1D/1A_6 L38
C577 *10U/6.3V_8 C575 *1U/6.3V_4 C576 *0.1U/10V_4
MPLL_PVDD : 1.8V @ 150mA

+1.8V_SPLL_PVDD
L2 *HCB1608KF-121T30(120,3000MA)
C61 *10U/6.3V_8 C64 *1U/6.3V_4 C58 *0.1U/10V_4
SPLL_PVDD : 1.8V @ 75mA

+1.0V_SPLL_VDDC
L1 *BLM18PG471SN1D/1A_6
C56 *10U/6.3V_8 C54 *1U/6.3V_4 C57 *0.1U/10V_4
1.0V(125mA DPLL_VDDC)
SPLL_VDDC : 0.935V @ 150mA
SPLL_PVSS

U21I PART 9 OF 9 *MARS_M2_PRO
AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 MPLL_PVDD
H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS
PLLSXTAL
XTALIN AV33 EVGA-XTALI
XTALOUT AU34 EVGA-XTALO
XO_IN AW34 R349 *0_4 EVGA-XTALI
XO_IN2 AW35
CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB

R348 *10M_8 Y2 *27MHZ
*22P/50V_4 C652
*22P/50V_4 C653

Ra
For Mars: Stuff Ra only

Debug only,
for clock observation,
if not needed, DNI
C62 *0.1U/10V_4 C69 *0.1U/10V_4
R39 *51.1/F_4 R45 *51.1/F_4

route 50ohms
single-ended/
100ohms diff and keep short

+1.8V_DPLL_PVDD
R115 Ra *0_4
R114 Rb *0_4
reserve Ra, Rb for future ASIC

For Mars only : AG22 NC

U21F PART 6 OF 9 *MARS_M2_PRO
PCIE_VSS: AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39
GND: F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N8 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27
GND: A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13
VSS_MECH: A39 AW1 AW39

[14,18,19,37] +1.0V_VGA → +1.0V_VGA
[15,18,19,38] +1.8V_VGA → +1.8V_VGA

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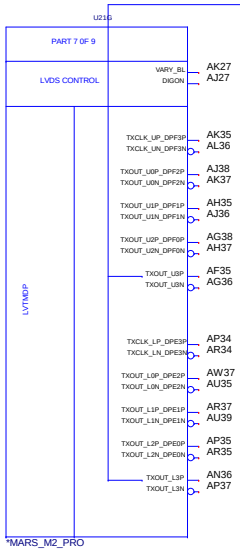
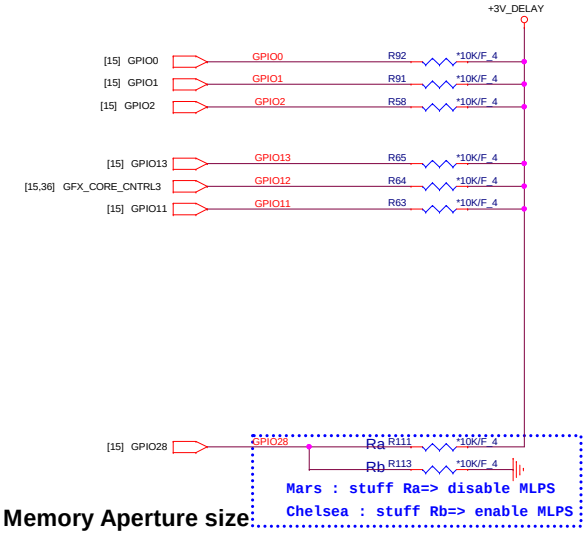
Fo Mars only: AF35, AG36: NC pin
Fo Mars only: AN36, AP37: NC pin





Mars : stuff Ra=> disable MLPS
Chelsea : stuff Rb=> enable MLPS

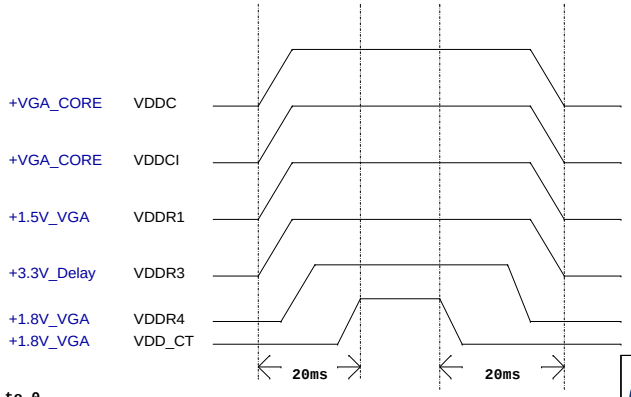
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



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+1.5V_VGA

VDDR1 , 1.5V @ 2A, GDDR5 900MHz

I/O power for the memory interface.

C144 *1U/6.3V_4 C8 *1U/6.3V_4 C7 *1U/6.3V_4 C36 *1U/6.3V_4 C634 *1U/6.3V_4 C74 *1U/6.3V_4 C73 *1U/6.3V_4 C590 *1U/6.3V_4 C27 *1U/6.3V_4 C48 *1U/6.3V_4

C632 *10U/6.3VS_6 C40 *10U/6.3VS_6 C42 *10U/6.3VS_6 C137 *10U/6.3VS_6 C136 *10U/6.3VS_6 C76 *10U/6.3VS_6

C679 *22U/6.3VS_8 C543 *22U/6.3VS_8

U12IE

PART 5 0F 9

MEM I/O

AC7 AD11 AF7 AG10 AJ7 AK8 AL9 G11 G14 G17 G20 G23 G26 G29 H10 J7 J9 K11 K13 K8 L12 L16 L21 L23 L26 L7 M11 N11 P7 R11 U11 U7 Y11 Y7 — VDDR1

PCIE

NC_PCIE_VDDR AA31 AA32 AA33 AA34 W30 Y31 V28 W29 — Mars NC

PCIE_PVDD AB37

+1.8V_VGA

PCIe Digital Power Supply
PCIE_VDDC : 0.935V @ 1.88A (GEN2.0)
PCIE_VDDC : 0.935V @ 2.5A (GEN3.0)

+1.0V_VGA

PCIE_VDDC G30 G31 H29 H30 J29 J30 L28 M28 N28 R28 T28 U28

C673 *0.1U/10V_4 C714 *0.1U/10V_4 C662 *0.1U/10V_4 C685 *1U/6.3V_4 C719 *1U/6.3V_4 C676 *1U/6.3V_4 C697 *1U/6.3V_4 C712 *1U/6.3V_4 C713 *1U/6.3V_4

+1.0V_VGA

C675 *1U/6.3V_4 C674 *1U/6.3V_4 C660 *1U/6.3V_4 C681 *1U/6.3V_4 C715 *10U/6.3VS_6 C716 *10U/6.3VS_6

BIF_VDDC

BACO

BIF_VDDC N27 T27

R360 *0_8

Must always be connected to PCIE_VDDC for Mars

CORE

VDDC AA15 AA17 AA20 AA22 AA24 AA27 AB16 AB18 AB21 AB23 AB26 AB28 AC17 AC20 AC22 AC24 AC27 AD18 AD21 AD23 AD26 AF17 AF20 AF22 AG16 AG18 AH22 AH27 AH28 M26 N24 R18 R21 R23 R26 T17 T20 T22 T24 U16 U18 U21 U23 U26 V17 V20 V22 V24 V27 Y16 Y18 Y21 Y23 Y26 Y28

+VGA_CORE

C146 *1U/6.3V_4 C106 *1U/6.3V_4 C150 *1U/6.3V_4 C121 *1U/6.3V_4 C152 *1U/6.3V_4 C130 *1U/6.3V_4 C65 *1U/6.3V_4 C147 *1U/6.3V_4 C587 *1U/6.3V_4 C148 *1U/6.3V_4

C100 *1U/6.3V_4 C616 *1U/6.3V_4 C622 *1U/6.3V_4 C123 *1U/6.3V_4 C103 *1U/6.3V_4 C119 *1U/6.3V_4 C107 *1U/6.3V_4 C112 *1U/6.3V_4 C623 *1U/6.3V_4 C122 *1U/6.3V_4

C66 *1U/6.3V_4 C151 *1U/6.3V_4 C102 *1U/6.3V_4 C156 *1U/6.3V_4 C116 *1U/6.3V_4 C620 *1U/6.3V_4 C105 *1U/6.3V_4 C621 *1U/6.3V_4 C138 *1U/6.3V_4 C67 *1U/6.3V_4

C608 *10U/6.3VS_6 C599 *10U/6.3VS_6 C603 *10U/6.3VS_6 C602 *10U/6.3VS_6 C598 *10U/6.3VS_6

Reserve for Drop

C126 *10U/6.3VS_6 C109 *10U/6.3VS_6 C127 *10U/6.3VS_6 C609 *10U/6.3VS_6

C114 *330u_2.5V_3528

+VDDCI

VDDCI 0.8-1.15V @ 8.8A

VDDCI AA13 AB13 AC12 AC15 AD13 AD16 M15 M16 M18 M23 N13 N15 N17 N20 N22 R12 R13 R16 T12 T15 V15 Y13

C93 *1U/6.3V_4 C87 *1U/6.3V_4 C91 *1U/6.3V_4 C92 *1U/6.3V_4 C82 *1U/6.3V_4 C95 *1U/6.3V_4 C89 *1U/6.3V_4 C83 *1U/6.3V_4

C115 *10U/6.3VS_6 C88 *10U/6.3VS_6 C104 *10U/6.3VS_6 C84 *1U/6.3V_4 C90 *1U/6.3V_4

ISOLATED CORE I/O

+1.8V_VGA

L11 *0_6

+1.8V_VDD_CT

VDDC_CT: 1.8V @250mA

LEVEL TRANSLATION

VDD_CT AF26 AF27 AG26 AG27

C222 *10U/6.3VS_6 C224 *1U/6.3V_4 C206 *1U/6.3V_4 C223 *1U/6.3V_4 C205 *0.1U/10V_4

I/O

VDDR3 AF23 AF24 AG23 AG24

+3V_VGA

L7 *0_6

+3V_DELAY

VDDR3 : 3.3V @ 60mA

C161 *10U/6.3VS_6 C163 *1U/6.3V_4 C162 *1U/6.3V_4 C154 *1U/6.3V_4

DVP

VDDR4 AD12 AF11 AF12 AF13

+VDDR4

L39 *0_6

VDDR4 : 1.8V @ 300mA

VDDR4 AF15 AG11 AG13 AG15

C582 *10U/6.3VS_6 C586 *10U/6.3VS_6 C584 *1U/6.3V_4 C583 *1U/6.3V_4 C85 *0.1U/10V_4 C585 *0.1U/10V_4

PV, change to DNI

Route as differential pair and connect to the VSEN and RTN pins of the VR through a decoupling and termination circuit.

VOLTAGE SENESE

[36] VGPU_CORE_SENSE — AF28 FB_VDDC

TP61 — AG28 FB_VDDCI

[36] VSS_GPU_SENSE — AH29 FB_GND

*MARS_M2_PRO

[20,21,22,37] +1.5V_VGA
[14,16,19,37] +1.0V_VGA
[15,16,19,38] +1.8V_VGA
[37] +3V_VGA
[36] +VGA_CORE

+1.5V_VGA
+1.0V_VGA
+1.8V_VGA
+3V_VGA
+VGA_CORE

BIF_VDDC

C717 *22U/6.3VS_8 C682 *1U/6.3V_4 C686 *1U/6.3V_4 C718 *10U/6.3VS_6

Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

NB5

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Quanta Computer Inc.

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For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

U21H

PART 8 0F 9

DP_VDDR

DP_VDDC

DP GND

CALIBRATION

*MARS_M2_PRO

DPAB_VDD10

+1.0V_VGA

L41 *0_6

0.5A

C644 *0.1U/10V_4 C645 *1U/6.3V_4 C642 *10U/6.3VS_6

DP_VDDC AP31 AP32 AN33 AP33

For Mars NC

DP_VDDC AP13 AT13 AP14 AP15

DP_VDDC AL33 AM33 AK33 AK34

DPEF_VDD10

+1.0V_VGA

L42 *0_6

0.5A

C659 *0.1U/10V_4 C658 *1U/6.3V_4 C677 *10U/6.3VS_6

For Mars NC

DP_VDDR AN24 AP24 AP25 AP26 AU28 AV29

DP_VDDR AP20 AP21 AP22 AP23 AU18 AV19

+1.8V_VGA

L43 *0_6

0.5A

DPEF_VDD18

C678 *10U/6.3VS_6 C664 *1U/6.3V_4 C663 *0.1U/10V_4

DP_VDDR AH34 AJ34 AF34 AG34 AM37 AL38

DP_VSSR AN27 AP27 AP28 AW24 AW26 AN29 AP29 AP30 AW30 AW32 AN17 AP16 AP17 AW14 AW16 AN19 AP18 AP19 AW20 AW22 AN34 AP39 AR39 AU37 AF39 AH39 AK39 AL34 AV27 AR28 AV17 AR18 AN38 AM35

For Mars :Ra ,Rb : no stuff

For Thems/ Chelsea :
Ra , Rb : stuff 150R

Ra

R108 *150/F_4 AW28 DPAB_CALR

Rb

R341 *150/F_4 AW18 DPCD_CALR

R362 *150/F_4 AM39 DPEF_CALR

[14,16,18,37] +1.0V_VGA
[15,16,18,38] +1.8V_VGA

+1.0V_VGA
+1.8V_VGA

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[21] VMA_ODT0 → VMA_ODT0
[21] VMA_ODT1 → VMA_ODT1
[21] VMA_RAS0# → VMA_RAS0#
[21] VMA_RAS1# → VMA_RAS1#
[21] VMA_CAS0# → VMA_CAS0#
[21] VMA_CAS1# → VMA_CAS1#
[21] VMA_WE0# → VMA_WE0#
[21] VMA_WE1# → VMA_WE1#
[21] VMA_CS0# → VMA_CS0#
[21] VMA_CS1# → VMA_CS1#
[21] VMA_CKE0 → VMA_CKE0
[21] VMA_CKE1 → VMA_CKE1
[21] VMA_CLK0 → VMA_CLK0
[21] VMA_CLK0# → VMA_CLK0#
[21] VMA_CLK1 → VMA_CLK1
[21] VMA_CLK1# → VMA_CLK1#
[21] VMA_WDQS[7..0] → VMA_WDQS[7..0]
[21] VMA_RDQS[7..0] → VMA_RDQS[7..0]
[21] VMA_DM[7..0] → VMA_DM[7..0]
[21] VMA_DQ[63..0] → VMA_DQ[63..0]
[21] VMA_MA[13..0] → VMA_MA[13..0]
[21] VMA_BA0 → VMA_BA0
[21] VMA_BA1 → VMA_BA1
[21] VMA_BA2 → VMA_BA2

U21C
PART 3 OF 9
GDDR5/DDR3
MEMORY INTERFACE A

VMA_DQ0	C37	DQA0_0	
VMA_DQ1	C35	DQA0_1	
VMA_DQ2	A35	DQA0_2	
VMA_DQ3	E34	DQA0_3	
VMA_DQ4	G32	DQA0_4	
VMA_DQ5	D33	DQA0_5	
VMA_DQ6	F32	DQA0_6	
VMA_DQ7	E32	DQA0_7	
VMA_DQ8	D31	DQA0_8	
VMA_DQ9	F30	DQA0_9	
VMA_DQ10	C30	DQA0_10	
VMA_DQ11	A30	DQA0_11	
VMA_DQ12	F28	DQA0_12	
VMA_DQ13	C28	DQA0_13	
VMA_DQ14	A28	DQA0_14	
VMA_DQ15	E28	DQA0_15	
VMA_DQ16	D27	DQA0_16	
VMA_DQ17	F26	DQA0_17	
VMA_DQ18	C26	DQA0_18	
VMA_DQ19	A26	DQA0_19	
VMA_DQ20	F24	DQA0_20	
VMA_DQ21	C24	DQA0_21	
VMA_DQ22	A24	DQA0_22	
VMA_DQ23	E24	DQA0_23	
VMA_DQ24	C22	DQA0_24	
VMA_DQ25	A22	DQA0_25	
VMA_DQ26	F22	DQA0_26	
VMA_DQ27	D21	DQA0_27	
VMA_DQ28	A20	DQA0_28	
VMA_DQ29	F20	DQA0_29	
VMA_DQ30	D19	DQA0_30	
VMA_DQ31	E18	DQA0_31	
VMA_DQ32	C18	DQA1_0	
VMA_DQ33	A18	DQA1_1	
VMA_DQ34	F18	DQA1_2	
VMA_DQ35	D17	DQA1_3	
VMA_DQ36	A16	DQA1_4	
VMA_DQ37	F16	DQA1_5	
VMA_DQ38	D15	DQA1_6	
VMA_DQ39	E14	DQA1_7	
VMA_DQ40	F14	DQA1_8	
VMA_DQ41	D13	DQA1_9	
VMA_DQ42	F12	DQA1_10	
VMA_DQ43	A12	DQA1_11	
VMA_DQ44	D11	DQA1_12	
VMA_DQ45	F10	DQA1_13	
VMA_DQ46	A10	DQA1_14	
VMA_DQ47	C10	DQA1_15	
VMA_DQ48	G13	DQA1_16	
VMA_DQ49	H13	DQA1_17	
VMA_DQ50	J13	DQA1_18	
VMA_DQ51	H11	DQA1_19	
VMA_DQ52	G10	DQA1_20	
VMA_DQ53	G8	DQA1_21	
VMA_DQ54	K9	DQA1_22	
VMA_DQ55	K10	DQA1_23	
VMA_DQ56	G9	DQA1_24	
VMA_DQ57	A8	DQA1_25	
VMA_DQ58	C8	DQA1_26	
VMA_DQ59	E8	DQA1_27	
VMA_DQ60	A6	DQA1_28	
VMA_DQ61	C6	DQA1_29	
VMA_DQ62	E6	DQA1_30	
VMA_DQ63	A5	DQA1_31	
MVREFDA	L18	MVREFDA	
MVREFSA	L20	MVREFSA	

MAA0_0/MAA_0	G24	VMA_MA0	
MAA0_1/MAA_1	J23	VMA_MA1	
MAA0_2/MAA_2	H24	VMA_MA2	
MAA0_3/MAA_3	J24	VMA_MA3	
MAA0_4/MAA_4	H26	VMA_MA4	
MAA0_5/MAA_5	J26	VMA_MA5	
MAA0_6/MAA_6	H21	VMA_MA6	
MAA0_7/MAA_7	G21	VMA_MA7	
MAA1_0/MAA_8	H19	VMA_MA8	
MAA1_1/MAA_9	H20	VMA_MA9	
MAA1_2/MAA_10	L13	VMA_MA10	
MAA1_3/MAA_11	G16	VMA_MA11	
MAA1_4/MAA_12	J16	VMA_MA12	
MAA1_5/MAA_BA2	H16	VMA_BA2	
MAA1_6/MAA_BA0	J17	VMA_BA0	
MAA1_7/MAA_BA1	H17	VMA_BA1	
WCKA0_0/DQMA_0	A32	VMA_DM0	
WCKA0B_0/DQMA_1	C32	VMA_DM1	
WCKA0_1/DQMA_2	D23	VMA_DM2	
WCKA0B_1/DQMA_3	E22	VMA_DM3	
WCKA1_0/DQMA_4	C14	VMA_DM4	
WCKA1B_0/DQMA_5	A14	VMA_DM5	
WCKA1_1/DQMA_6	E10	VMA_DM6	
WCKA1B_1/DQMA_7	D9	VMA_DM7	
EDCA0_0/QSA_0	C34	VMA_RDQS0	
EDCA0_1/QSA_1	D29	VMA_RDQS1	
EDCA0_2/QSA_2	D25	VMA_RDQS2	
EDCA0_3/QSA_3	E20	VMA_RDQS3	
EDCA1_0/QSA_4	E16	VMA_RDQS4	
EDCA1_1/QSA_5	E12	VMA_RDQS5	
EDCA1_2/QSA_6	J10	VMA_RDQS6	
EDCA1_3/QSA_7	D7	VMA_RDQS7	
DDBIA0_0/QSA_0B	A34	VMA_WDQS0	
DDBIA0_1/QSA_1B	E30	VMA_WDQS1	
DDBIA0_2/QSA_2B	E26	VMA_WDQS2	
DDBIA0_3/QSA_3B	C20	VMA_WDQS3	
DDBIA1_0/QSA_4B	C16	VMA_WDQS4	
DDBIA1_1/QSA_5B	C12	VMA_WDQS5	
DDBIA1_2/QSA_6B	J11	VMA_WDQS6	
DDBIA1_3/QSA_7B	F8	VMA_WDQS7	
ADBIA0/ODTA0	J21	VMA_ODT0	
ADBIA1/ODTA1	G19	VMA_ODT1	
CLKA0	H27	VMA_CLK0	
CLKA0B	G27	VMA_CLK0#	
CLKA1	J14	VMA_CLK1	
CLKA1B	H14	VMA_CLK1#	
RASA0B	K23	VMA_RAS0#	
RASA1B	K19	VMA_RAS1#	
CASA0B	K20	VMA_CAS0#	
CASA1B	K17	VMA_CAS1#	
CSA0B_0	K24	VMA_CS0#	
CSA0B_1	K27		
CSA1B_0	M13	VMA_CS1#	
CSA1B_1	K16		
CKEA0	K21	VMA_CKE0	
CKEA1	J20	VMA_CKE1	
WEA0B	K26	VMA_WE0#	
WEA1B	L15	VMA_WE1#	
MAA0_8/MAA_13	H23	VMA_MA13	
MAA1_8/MAA_14	J19		
MAA0_9/MAA_15	M21		
MAA1_9/RSVD	M20		

TP70
TP63

M21, M20

For Mars /Chelsea: reserve

For Thems: NC

*MARS_M2_PRO

+1.5V_VGA
R332 40.2/F_4
C589 *1U/6.3V_4
R331 100/F_4

PLACE MVREFD DIVIDERS AND CAPS CLOSE TO ASIC

+1.5V_VGA
R338 40.2/F_4
C607 *1U/6.3V_4
R337 100/F_4

+1.5V_VGA
Ra R101 *240/F_4 → NC_MEM_CALRN0
Rb R54 *240/F_4 → NC_MEM_CALRN1
Rc R57 *240/F_4 → NC_MEM_CALRN2
Rd R60 *240/F_4 → NC_MEM_CALRP1
Re R105 *120/F_4 → MEM_CALRP0
Rf R67 *240/F_4 → MEM_CALRP2

For Mars / Heathrow /Chelsea
Re stuff 120 ohm 1%
Uninstall Ra, Rb, Rc, Rd , Rf.

For Thames
Install Ra, Rb, Rc Rd Re Rf
install 240 Ohm

[18,21,22,37] +1.5V_VGA → +1.5V_VGA

[22] VMB_ODT0 → VMB_ODT0
[22] VMB_ODT1 → VMB_ODT1
[22] VMB_RAS0# → VMB_RAS0#
[22] VMB_RAS1# → VMB_RAS1#
[22] VMB_CAS0# → VMB_CAS0#
[22] VMB_CAS1# → VMB_CAS1#
[22] VMB_WE0# → VMB_WE0#
[22] VMB_WE1# → VMB_WE1#
[22] VMB_CS0# → VMB_CS0#
[22] VMB_CS1# → VMB_CS1#
[22] VMB_CKE0 → VMB_CKE0
[22] VMB_CKE1 → VMB_CKE1
[22] VMB_CLK0 → VMB_CLK0
[22] VMB_CLK0# → VMB_CLK0#
[22] VMB_CLK1 → VMB_CLK1
[22] VMB_CLK1# → VMB_CLK1#
[22] VMB_WDQS[7..0] → VMB_WDQS[7..0]
[22] VMB_RDQS[7..0] → VMB_RDQS[7..0]
[22] VMB_DM[7..0] → VMB_DM[7..0]
[22] VMB_DQ[63..0] → VMB_DQ[63..0]
[22] VMB_MA[13..0] → VMB_MA[13..0]
[22] VMB_BA0 → VMB_BA0
[22] VMB_BA1 → VMB_BA1
[22] VMB_BA2 → VMB_BA2

+1.5V_VGA
R322 40.2/F_4
C580 *1U/6.3V_4
R323 100/F_4

PLACE MVREFD DIVIDERS AND CAPS CLOSE TO ASIC

+1.5V_VGA
R321 40.2/F_4
C579 *1U/6.3V_4
R320 100/F_4

U21D
PART 4 OF 9
GDDR5/DDR3
MEMORY INTERFACE B

VMB_DQ0	C5	DQB0_0	
VMB_DQ1	C3	DQB0_1	
VMB_DQ2	E3	DQB0_2	
VMB_DQ3	E1	DQB0_3	
VMB_DQ4	F1	DQB0_4	
VMB_DQ5	F3	DQB0_5	
VMB_DQ6	F5	DQB0_6	
VMB_DQ7	G4	DQB0_7	
VMB_DQ8	H5	DQB0_8	
VMB_DQ9	H6	DQB0_9	
VMB_DQ10	J4	DQB0_10	
VMB_DQ11	K6	DQB0_11	
VMB_DQ12	K5	DQB0_12	
VMB_DQ13	L4	DQB0_13	
VMB_DQ14	M6	DQB0_14	
VMB_DQ15	M1	DQB0_15	
VMB_DQ16	M3	DQB0_16	
VMB_DQ17	M5	DQB0_17	
VMB_DQ18	N4	DQB0_18	
VMB_DQ19	P6	DQB0_19	
VMB_DQ20	P5	DQB0_20	
VMB_DQ21	R4	DQB0_21	
VMB_DQ22	T6	DQB0_22	
VMB_DQ23	T1	DQB0_23	
VMB_DQ24	U4	DQB0_24	
VMB_DQ25	V6	DQB0_25	
VMB_DQ26	V1	DQB0_26	
VMB_DQ27	V3	DQB0_27	
VMB_DQ28	Y6	DQB0_28	
VMB_DQ29	Y1	DQB0_29	
VMB_DQ30	Y3	DQB0_30	
VMB_DQ31	Y5	DQB0_31	
VMB_DQ32	AA4	DQB1_0	
VMB_DQ33	AB6	DQB1_1	
VMB_DQ34	AB1	DQB1_2	
VMB_DQ35	AB3	DQB1_3	
VMB_DQ36	AD6	DQB1_4	
VMB_DQ37	AD1	DQB1_5	
VMB_DQ38	AD3	DQB1_6	
VMB_DQ39	AD5	DQB1_7	
VMB_DQ40	AF1	DQB1_8	
VMB_DQ41	AF3	DQB1_9	
VMB_DQ42	AF6	DQB1_10	
VMB_DQ43	AG4	DQB1_11	
VMB_DQ44	AH5	DQB1_12	
VMB_DQ45	AH6	DQB1_13	
VMB_DQ46	AJ4	DQB1_14	
VMB_DQ47	AK3	DQB1_15	
VMB_DQ48	AF8	DQB1_16	
VMB_DQ49	AF9	DQB1_17	
VMB_DQ50	AG8	DQB1_18	
VMB_DQ51	AG7	DQB1_19	
VMB_DQ52	AK9	DQB1_20	
VMB_DQ53	AL7	DQB1_21	
VMB_DQ54	AM8	DQB1_22	
VMB_DQ55	AM7	DQB1_23	
VMB_DQ56	AK1	DQB1_24	
VMB_DQ57	AL4	DQB1_25	
VMB_DQ58	AM6	DQB1_26	
VMB_DQ59	AM1	DQB1_27	
VMB_DQ60	AN4	DQB1_28	
VMB_DQ61	AP3	DQB1_29	
VMB_DQ62	AP1	DQB1_30	
VMB_DQ63	AP5	DQB1_31	
MVREFDB	Y12	MVREFDB	
MVREFSB	AA12	MVREFSB	

MAB0_0/MAB_0	P8	VMB_MA0	
MAB0_1/MAB_1	T9	VMB_MA1	
MAB0_2/MAB_2	P9	VMB_MA2	
MAB0_3/MAB_3	N7	VMB_MA3	
MAB0_4/MAB_4	N8	VMB_MA4	
MAB0_5/MAB_5	N9	VMB_MA5	
MAB0_6/MAB_6	U9	VMB_MA6	
MAB0_7/MAB_7	U8	VMB_MA7	
MAB1_0/MAB_8	Y9	VMB_MA8	
MAB1_1/MAB_9	W9	VMB_MA9	
MAB1_2/MAB_10	AC8	VMB_MA10	
MAB1_3/MAB_11	AC9	VMB_MA11	
MAB1_4/MAB_12	AA7	VMB_MA12	
MAB1_5/BA2	AA8	VMB_BA2	
MAB1_6/BA0	Y8	VMB_BA0	
MAB1_7/BA1	AA9	VMB_BA1	
WCKB0_0/DQMB_0	H3	VMB_DM0	
WCKB0B_0/DQMB_1	H1	VMB_DM1	
WCKB0_1/DQMB_2	T3	VMB_DM2	
WCKB0B_1/DQMB_3	T5	VMB_DM3	
WCKB1_0/DQMB_4	AE4	VMB_DM4	
WCKB1B_0/DQMB_5	AF5	VMB_DM5	
WCKB1_1/DQMB_6	AK6	VMB_DM6	
WCKB1B_1/DQMB_7	AK5	VMB_DM7	
EDCB0_0/QSB_0	F6	VMB_RDQS0	
EDCB0_1/QSB_1	K3	VMB_RDQS1	
EDCB0_2/QSB_2	P3	VMB_RDQS2	
EDCB0_3/QSB_3	V5	VMB_RDQS3	
EDCB1_0/QSB_4	AB5	VMB_RDQS4	
EDCB1_1/QSB_5	AH1	VMB_RDQS5	
EDCB1_2/QSB_6	AJ9	VMB_RDQS6	
EDCB1_3/QSB_7	AM5	VMB_RDQS7	
DDBIB0_0/QSB_0B	G7	VMB_WDQS0	
DDBIB0_1/QSB_1B	K1	VMB_WDQS1	
DDBIB0_2/QSB_2B	P1	VMB_WDQS2	
DDBIB0_3/QSB_3B	W4	VMB_WDQS3	
DDBIB1_0/QSB_4B	AC4	VMB_WDQS4	
DDBIB1_1/QSB_5B	AH3	VMB_WDQS5	
DDBIB1_2/QSB_6B	AJ8	VMB_WDQS6	
DDBIB1_3/QSB_7B	AM3	VMB_WDQS7	
ADBIB0/ODTB0	T7	VMB_ODT0	
ADBIB1/ODTB1	W7	VMB_ODT1	
CLKB0	L9	VMB_CLK0	
CLKB0B	L8	VMB_CLK0#	
CLKB1	AD8	VMB_CLK1	
CLKB1B	AD7	VMB_CLK1#	
RASB0B	T10	VMB_RAS0#	
RASB1B	Y10	VMB_RAS1#	
CASB0B	W10	VMB_CAS0#	
CASB1B	AA10	VMB_CAS1#	
CSB0B_0	P10	VMB_CS0#	
CSB0B_1	L10		
CSB1B_0	AD10	VMB_CS1#	
CSB1B_1	AC10		
CKEB0	U10	VMB_CKE0	
CKEB1	AA11	VMB_CKE1	
WEB0B	N10	VMB_WE0#	
WEB1B	AB11	VMB_WE1#	
MAB0_8/MAB_13	T8	VMB_MA13	
MAB1_8/MAB_14	W8		
MAB0_9/MAB_15	U12		
MAB1_9/RSVD	V12		
DRAM_RST	AH11	DRAM_RST	

need check

TP59
TP9

U12, V12

For Mars /Chelsea: reserve

For Thems: NC

*MARS_M2_PRO

DRAM_RST → R310 *10/F_4 → R304 *51_4 → DRAM_RST_M → DRAM_RST_M [21,22]
R314 *4.99K/F_4
C563 *120P/50V_4

NB5	PROJECT : VOLKS_Comal 14"	
	Quanta Computer Inc.	
Size: Custom	Document Number: Mars_MEM_Interface	Rev: 1A
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CHANNEL A: 256MB/512MB DDR3

Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
NB5
Size: Custom | Document Number: VRAM-A (DDR3 BGA96) | Rev: 1A
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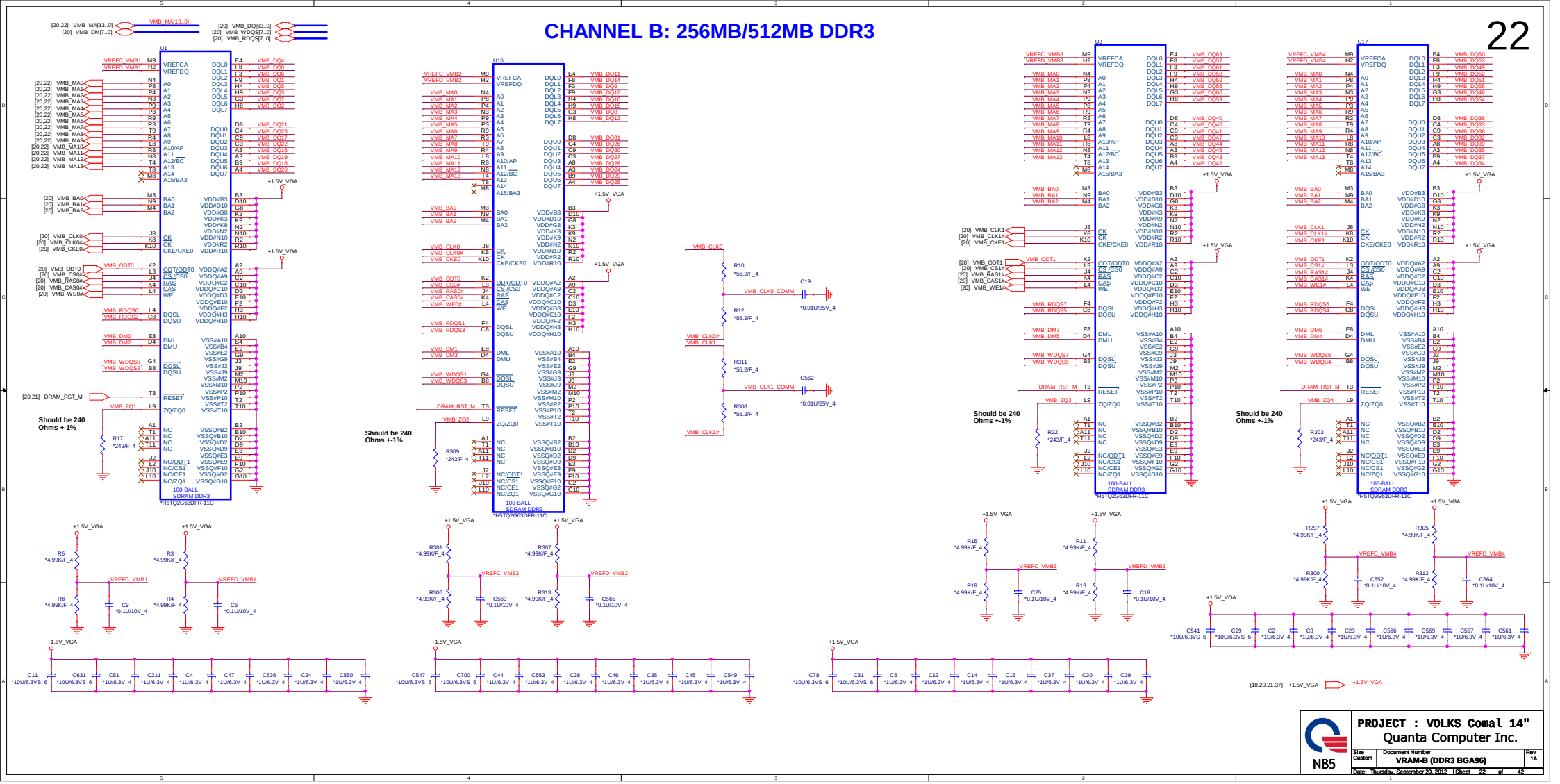
CHANNEL B: 256MB/512MB DDR3



PROJECT : VOLKS_Comal 14"		
Quanta Computer Inc.		
NB5	Size: Custom	Document Number: VRAM-B (DDR3 BGA96) Rev: 1A
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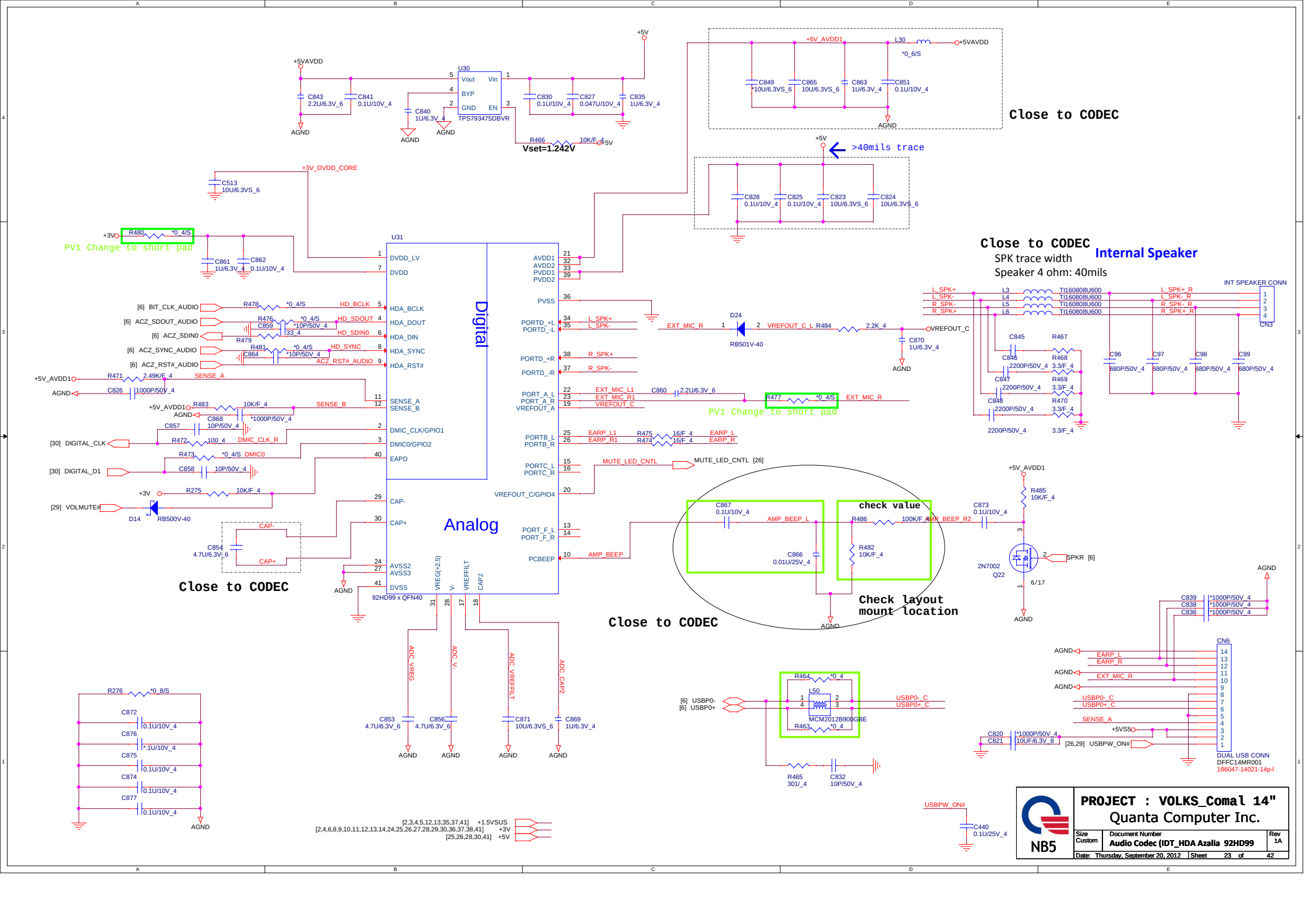
U30
TPS793475DBVR
Vset=1.242V
+5V_AVDD1
L30
*0_6/S
+5VAVDD
Close to CODEC
>40mils trace
+3V_DVDD_CORE
U31
92HD99 x QFN40
Digital
Analog
PV1 Change to short pad
Close to CODEC
SPK trace width
Speaker 4 ohm: 40mils
Internal Speaker
INT SPEAKER CONN
CN3
RB501V-40
D24
VREFOUT_C
EXT_MIC_R
R484
2.2K_4
C870
1U/6.3V_4
PV1 Change to short pad
MUTE_LED_CNTL
MUTE_LED_CNTL [26]
check value
Check layout
mount location
Close to CODEC
2N7002
Q22
SPKR [6]
6/17
CN6
DUAL USB CONN
DFFC14MR001
196047-14021-14p-l
USBPW_ON#
[26,29] USBPW_ON#
MCM2012B900GBE
L50
R464
R463
R465
301/_4
C832
10P/50V_4
C440
0.1U/25V_4
NB5
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
Size Custom
Document Number
Audio Codec (IDT_HDA Azalia 92HD99
Rev 1A
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For EMI 0 ~ 22 ohm

R335 *10_4

LAN_XTAL1 — XTAL1 — XTAL2

Y1 *25MHz

C604 *33P/50V_4

C605 *33P/50V_4

PV2 change to non-stuff for Green Clock solution

Green Clk [27] LAN_XTAL25_IN — R336 510/F_4 — XTAL2

PV2 change to stuff for Green Clock solution

Change to 0603 size for EMI request

75_6 R20 — C33 0.01U/100V_0603

75_6 R21 — C34 0.01U/100V_0603

C555 10P/3KV_1808

U19 NS681684

LAN_MX0+ / LAN_MX0- / LAN_MCT1 / LAN_MX1+ / LAN_MX1- / LAN_MCT0

TD+ TD- CT RD+ RD- CT — TX+ CMT TX- RX- CT RX+

MDI0+ / V_DAC2 / MDI0- / MDI1- / V_DAC1 / MDI1+

C53 0.01U/25V_4

+3V_LAN

+3VLANVCC

C613 *10U/6.3V_8 — C625 0.1U/10V_4 — C614 0.1U/10V_4 — C611 0.1U/10V_4 — C610 0.1U/10V_4

GND VIA x 9 Pcs

+1.05V_LAN

R52 2.49K/F_4 LANRSET

+3V_LAN

LAN_TX# — LAN_GPIOS — R340 1K/F_4 — +3V_LAN

LAN_GLINK100#

U4 RTL8105E

GND AVDD33 AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 AVDD33 DVDD10(NC) LED0 DVDD33 GPIO/SMBALERT LED1/EESK

XTAL2 XTAL1

MDI0+ MDI0- MDI1+ MDI1-

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)

REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB

LAN_GLINK10# — TP1

LAN_ECS_SCL — TP2

+1.05V_LAN

PCIE_WAKE# — PCIE_WAKE# [6,27]

+3V_LAN

ISOLATEB

PLTRST# — LAN_PCIE_RST# [7]

DVDD10 SMBCLK(NC) SMBDATA(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N EVDD10 HSOP HSON GND

+1.05V_LAN

LAN_CLKRQ

[6] PCIE_CLKREQ_LAN# — PCIE_CLKREQ_LAN# R102 *0_4/S

[7] PCIE_TXP1_LAN — PCIE_TXP1_LAN

[7] PCIE_TXN1_LAN — PCIE_TXN1_LAN

[7] CLK_PCIE_LANP — CLK_PCIE_LANP

[7] CLK_PCIE_LANN — CLK_PCIE_LANN

PCIE_RXN1_LAN_L C159 0.1U/10V_4 — PCIE_RXN1_LAN [7]

PCIE_RXP1_LAN_L C158 0.1U/10V_4 — PCIE_RXP1_LAN [7]

EVDD10

+3V

R100 1K/F_4

ISOLATEB

R86 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

+1.05V_LAN

C624 0.1U/10V_4 — C627 0.1U/10V_4 — C628 0.1U/10V_4 — C612 *10U/6.3V_8

EVDD10

C626 1U/6.3V_4 — C619 0.1U/10V_4

+3VLANVCC

R19 62_4 — C26 1000P/50V_4

2P Amber LED(Side-View) LED3

LAN_YLED — LAN_TX#

(Amber)

朝前

+3VLANVCC

R1 62_4

2P WHITE LED(Side-View) LED2

LAN_GLED — LAN_GLINK100#

(White)

C1 1000P/50V_4

朝前

RJ45

CN8 RJ45_CONN

LAN_MX1- / LAN_MX1+ / LAN_MX0- / LAN_MX0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND2 GND1 GND3 GND4

R23 *0_6/S

R2 *0_6/S

C10 68P/50V_4

NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size: Custom	Document Number: LAN RTL8105/RJ45	Rev: 1A
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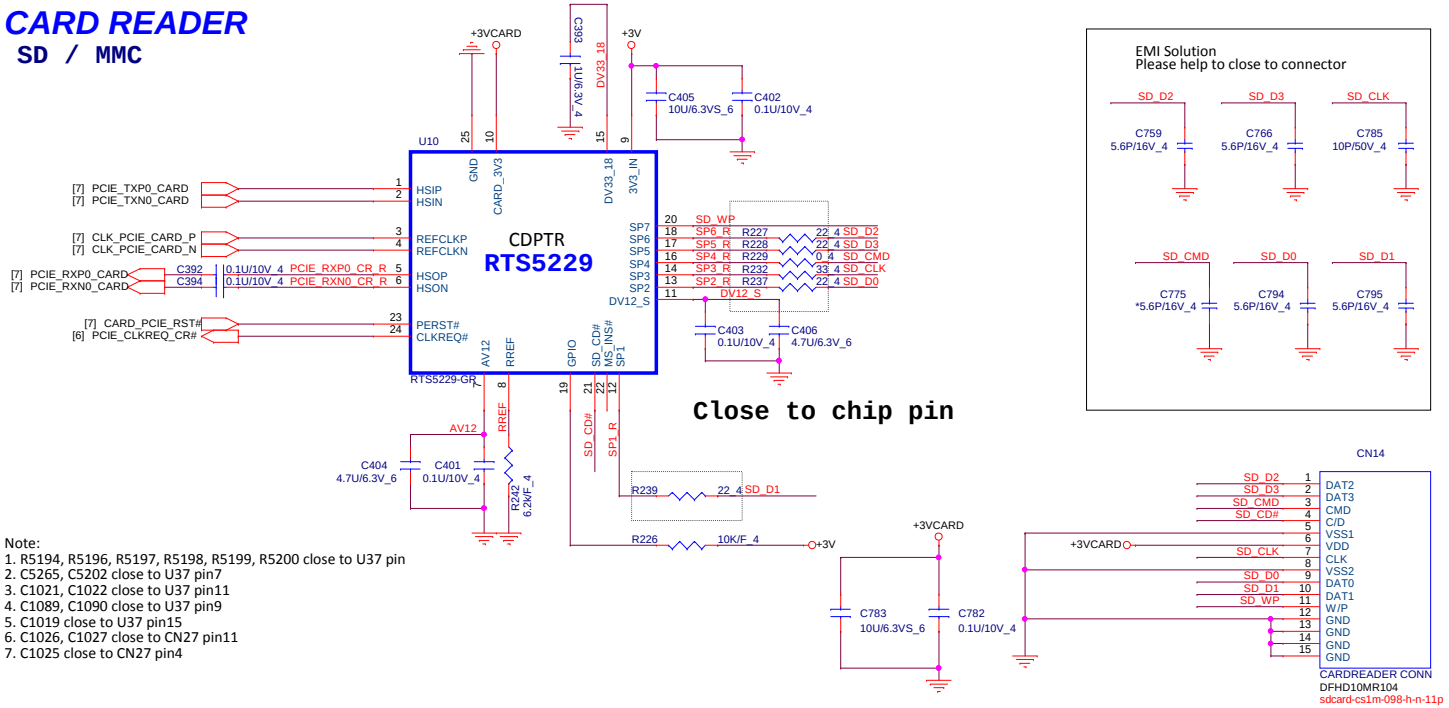
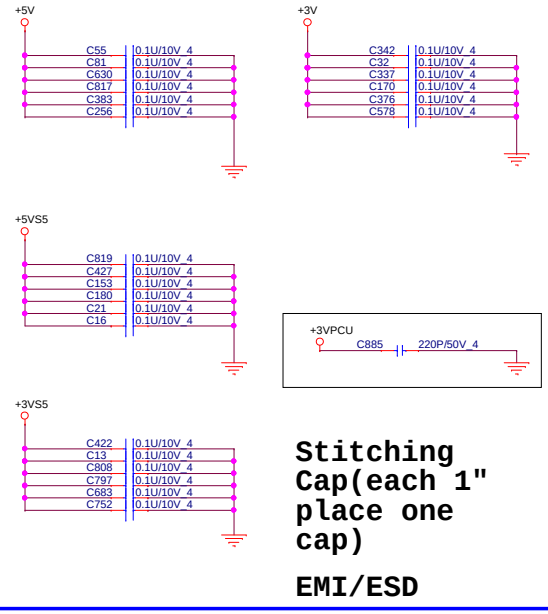
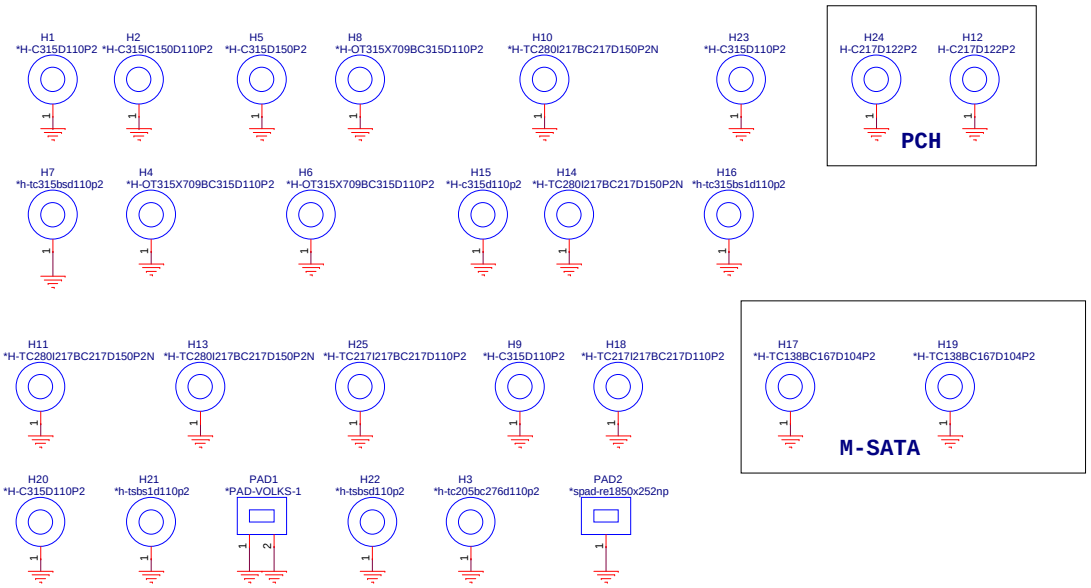
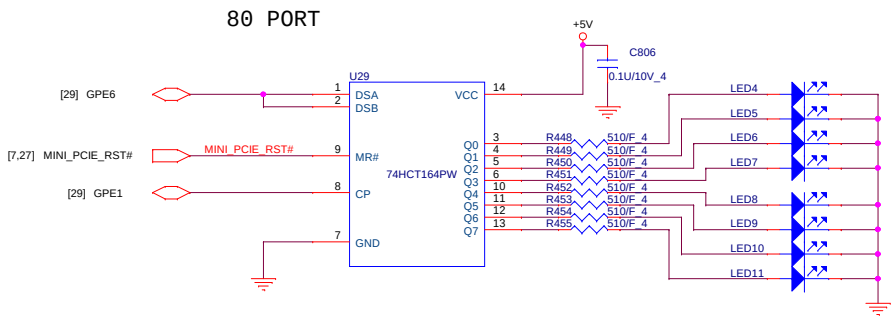
CARD READER
SD / MMC



Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4





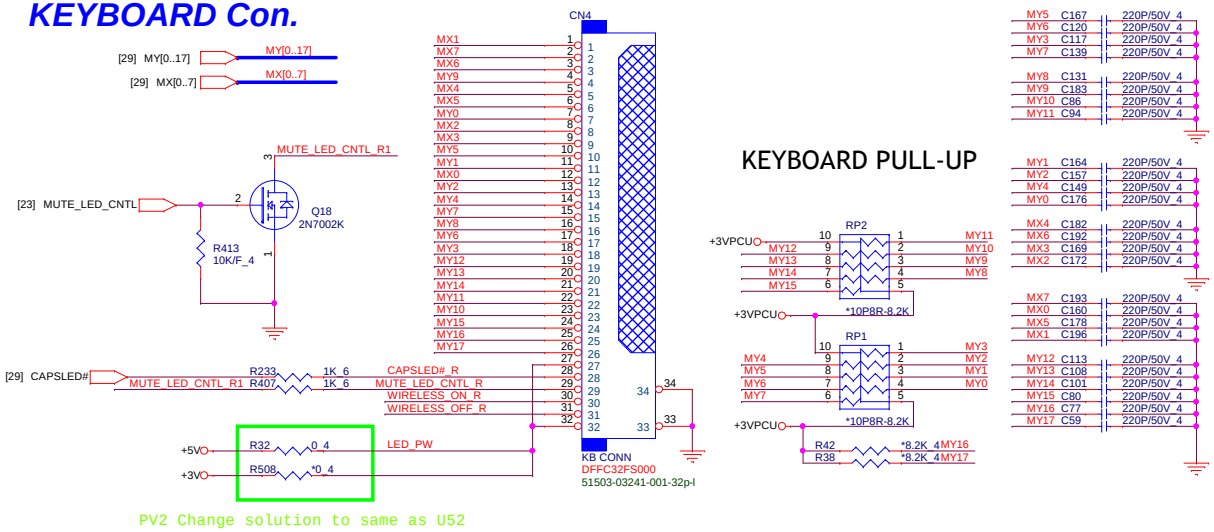


PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader control (RTS5229-GR)	1A
Date: Thursday, September 20, 2012	Sheet 25of 42	

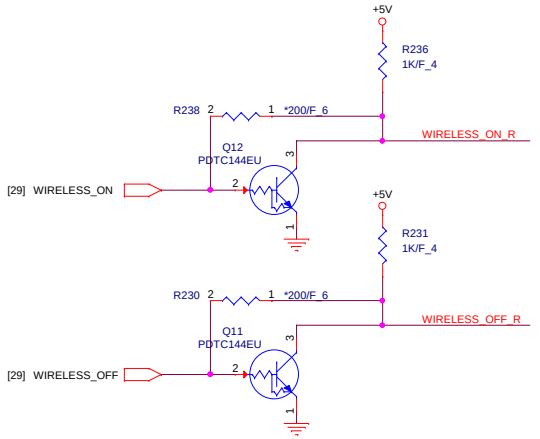
NB5

KEYBOARD Con.

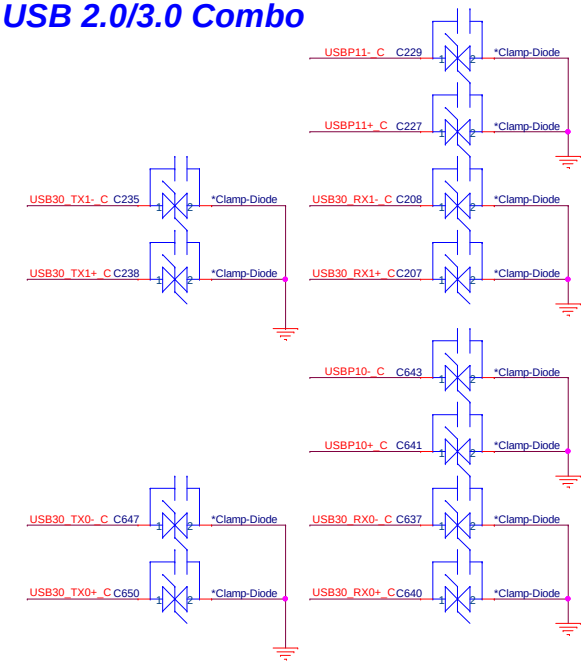


PV2 Change solution to same as U52

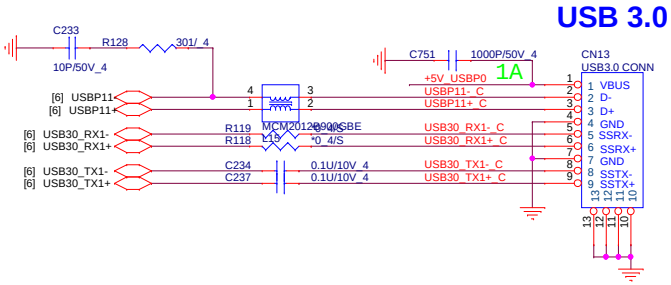
KEYBOARD PULL-UP



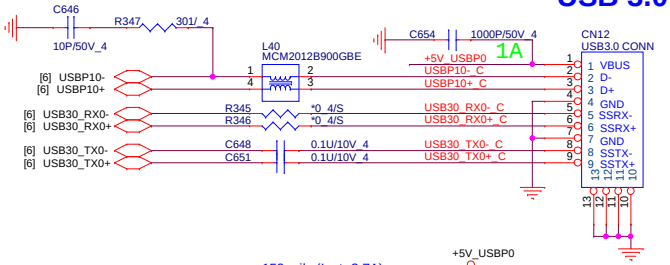
USB 2.0/3.0 Combo

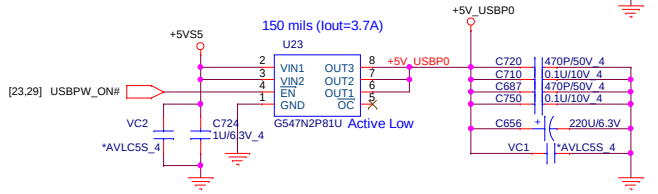


USB 3.0

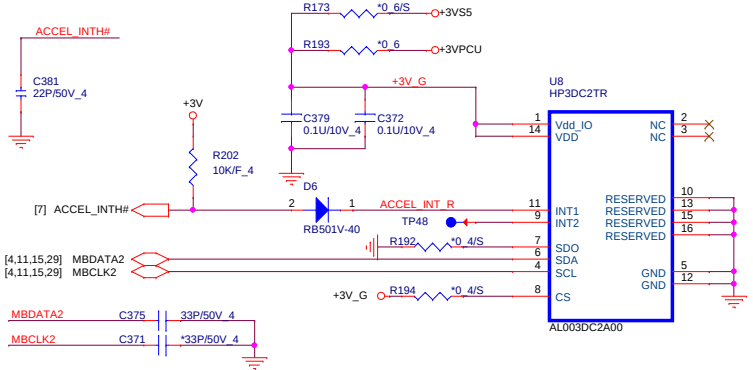


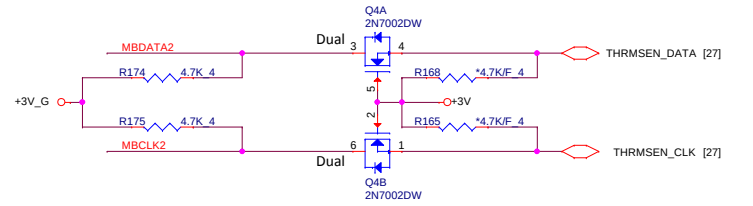
USB 3.0





Accelerometer Sensor





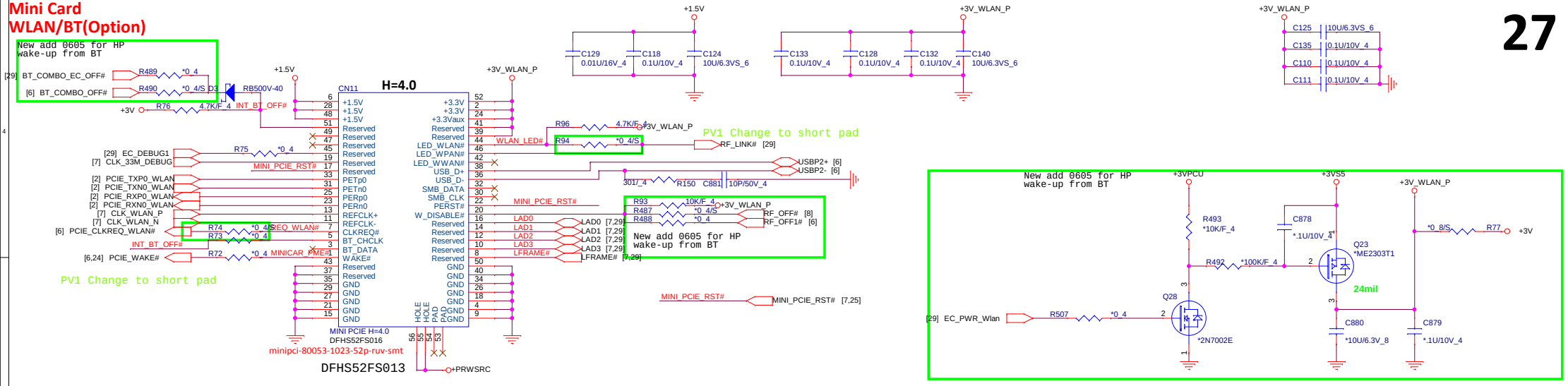
[23,25,32,33,34,35,36,38,39,40,41] +5VS5
[4,7,25,27,28,29,30,31,32] +3VPCU

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

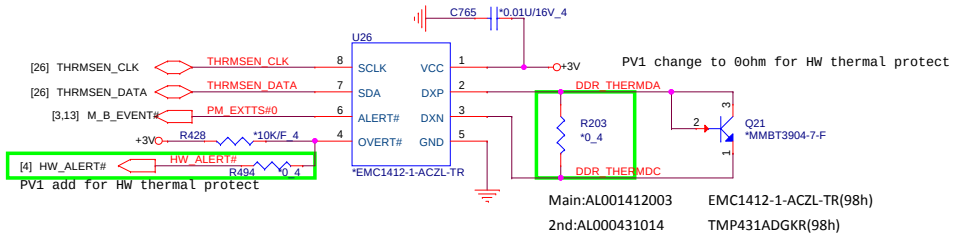
Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A
Date: Thursday, September 20, 2012	Sheet 26of	42

Mini Card WLAN/BT(Option)

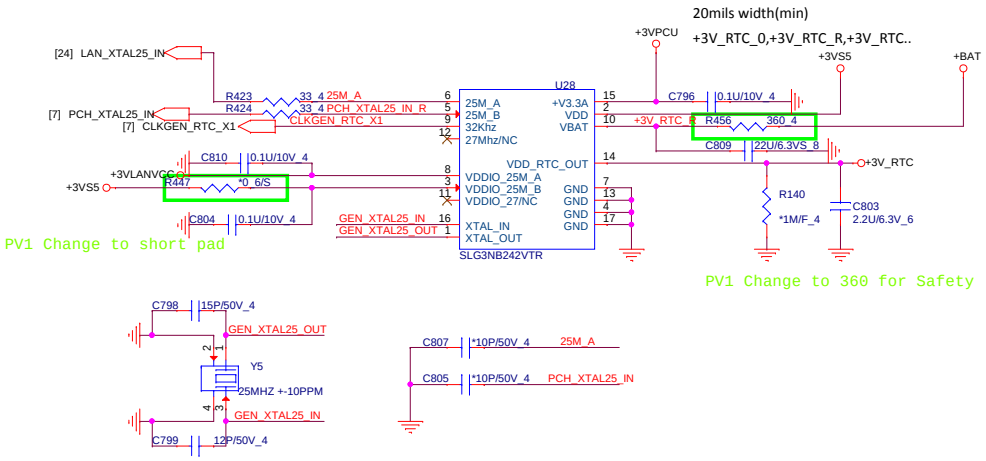


Local Thermal Sensor

DDR3 Thermal Sensor



Green CLK Circuitry



[6,8,9,10,25,26,29,32,34,36,37,41] +3VS5
[2,4,6,8,9,10,11,12,13,14,23,24,25,26,28,29,30,36,37,38,41] +3V
[23,25,26,28,30,41] +5V
[4,7,25,26,28,29,30,31,32] +3VPCU
[2,4,11,28,39,41] +1.5V

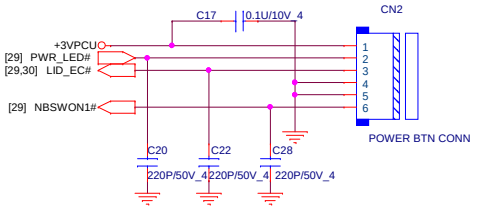
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
Date: Thursday, September 20, 2012	Sheet 27of 42	

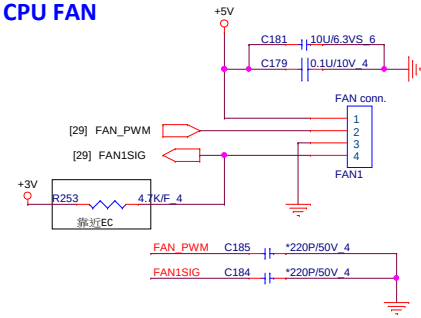
NB5

Power Botton Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

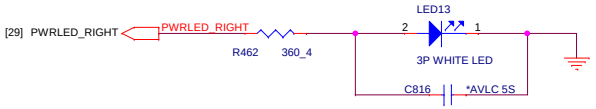


CPU FAN

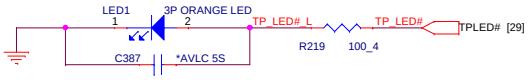


LED Status

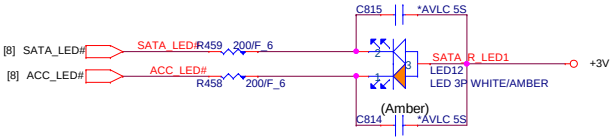
PWR LED



14 "TP LED

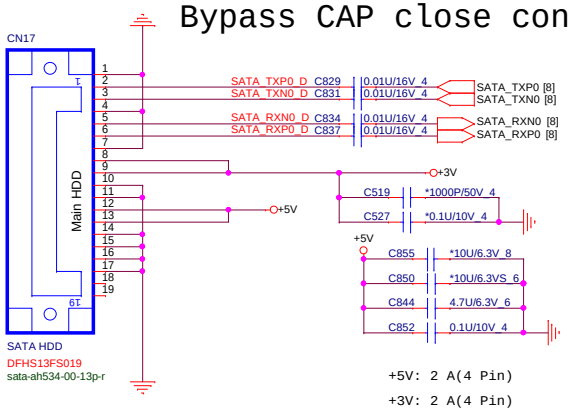


SATA LED

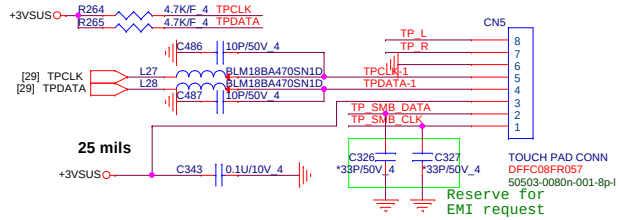


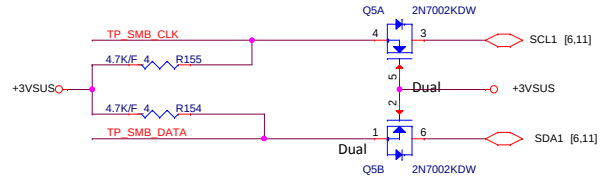
SATA HDD Connector(Cable type)

Bypass CAP close conn

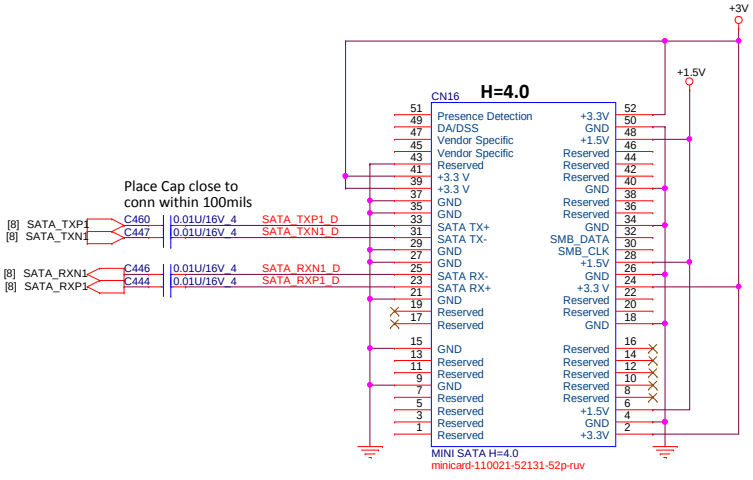


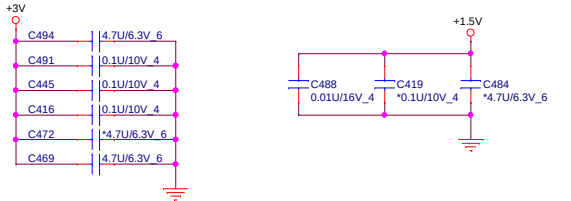
+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)



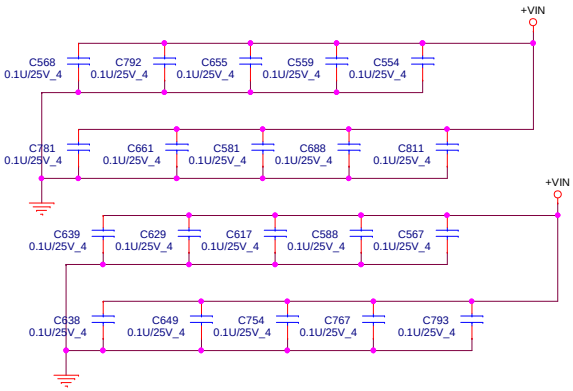


Mini PCI-E Card 2- Full size
mSATA

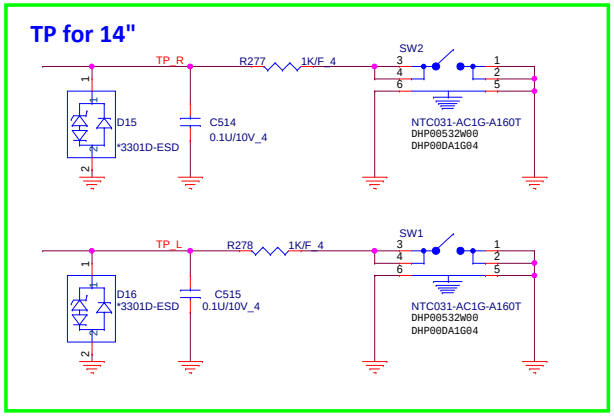




+VIN Cap



TP for 14"



[2,4,6,8,9,10,11,12,13,14,23,24,25,26,27,29,30,36,37,38,41] +3V
[23,25,26,30,41] +5V
[4,7,25,26,27,29,30,31,32] +3VPCU
[2,4,11,27,39,41] +1.5V
[31,37,41] +12VALW

NB5

PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	1A
Date: Thursday, September 20, 2012	Sheet 28of 42	

ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

CAPS LED

CAPSLED# [26]

Q10 2N7002K

500mA

+3VPCU_AC L29 FCM1608KF-121T04

+3VPCU_EC L24 FCM1608KF-121T04

Change to RB500 as Current loss

SCI1# D12 RB501V-40 SIO_EXT_SCI# [6]

DNBSWON1# D13 RB501V-40 DNBSWON# [6]

KBSMI#1 D10 RB501V-40 SIO_EXT_SMI# [6]

IT8518E/HX

LPC: LAD0–LAD3, LFRAME#, LPCPD#/WUI6/GPE6, LPCRST#/WUI4/GPD2, LPCCLK, GA20/GPB5, SERIRQ, ECSMI#/GPD4, ECSCI#/GPD3, WRST#, KBRST#/GPB6, PWUREQ#/BBO/GPC7

GPIO: EGCLK/WUI27/GPE3, EGCS#/WUI26/GPE2, EGAD/WUI25/GPE1, KSO16/SMOSI/GPC3, KSO17/SMISO/GPC5, L80HLAT/BAO/WUI24/GPE0, L80LLAT/WUI7/GPE7, SBUSY/GPG1/ID7, HMOSIGPH6/ID6, HMISO/GPH5/ID5, HSCK/GPH4/ID4, HSCE#/WUI19/GPH3/ID3, CTX1/WUI18/GPH2/SMDAT3/ID2, CRX1/WUI17/GPH1/SMCLK3/ID1, CLKRUN#/WUI16/GPH0/ID0

PS/2: GPC0/TMA0/GPB2, PS2DAT0/TMB1/GPF1, PS2CLK0/TMB0/GPF0, PS2DAT2/WUI21/GPF5, PS2CLK2/WUI20/GPF4

SM_BUS: SMCLK2/WUI22/GPF6/PECI, SMDAT2/WUI23/GPF7, SMCLK0/GPB3, SMDAT0/GPB4, SMCLK1/GPC1, SMDAT1/GPC2

UART: DAC4/DCD0#/GPJ4, DSR0#/GPG6, GINT/CTS0#/GPD5, PS2DAT1/RTS0#/GPF3, DAC5/RIG0#/GPJ5, PS2CLK1/DTR0#/GPF2, RXD/SIN0/GPB0, TXD/SOUT0/GPB1

FLASH: GPG0/FSCK, FMISO/FMOSI/FSCE#/SSCE0#/GPG2

PWM: PWM0/GPA0, PWM1/GPA1, PWM2/GPA2, PWM3/GPA3, PWM4/GPA4, PWM5/GPA5, PWM6/SSCK/GPA6, PWM7/GPA7, TACH0/GPD6, TACH1/TMA1/GPD7, TMR0/WUI2/GPC4, TMR1/WUI3/GPC6

KBMX: KSO0/PD0, KSO1/PD1, KSO2/PD2, KSO3/PD3, KSO4/PD4, KSO5/PD5, KSO6/PD6, KSO7/PD7, KSO8/ACK#, KSO9/BUSY, KSO10/PE, KSO11/ERR#, KSO12/SLCT, KSO13, KSO14, KSO15, KSI0/STB#, KSI1/AFD#, KSI2/INIT#, KSI3/SLIN#, KSI4, KSI5, KSI6, KSI7

WAKE UP: PWRSW/GPE4, RI1#/WUI0/GPD0, RI2#/WUI1/GPD1, WUI5/GPE5, RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7

A/D D/A: ADC0/GPI0, ADC1/GPI1, ADC2/GPI2, ADC3/GPI3, ADC4/WUI28/GPI4, ADC5/WUI29/GPI5, ADC6/WUI30/GPI6, ADC7/WUI31/GPI7

CLOCK: CK32K, CK32KE

AJ085180F04

IT8518E/HX

For GPU thermal

for Battery charge/discharge

for CPU themal

from power button

PV1 Change to short pad

For +VIN noise

HWPG C463 *0.1U/10V_4

FAN1SIG C433 *0.1U/10V_4

DGPU_PR_EN C442 *0.1U/10V_4

Vender	Size	P/N
PME	4M	AKE39ZN0500
GGD	4M	AKE39GN0Q00
AMC	4M	AKE39F-0800
Socket		DFHS08FS023

4M SPI EC ROM

U13 A25LQ32AM-F/Q AKE39F-0800 SOIC8-8-1_27

128K byte SPI EC ROM

U12 *DFHS08FS023 SOIC8-6-1_27

ICT need TP2675 size test point

EMI

SI

TP place on top lay for ICT request

PWR_LED

0424 Fix PWR_LED

Q15 MMBT3904-7-F

Adapter select

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

NB5

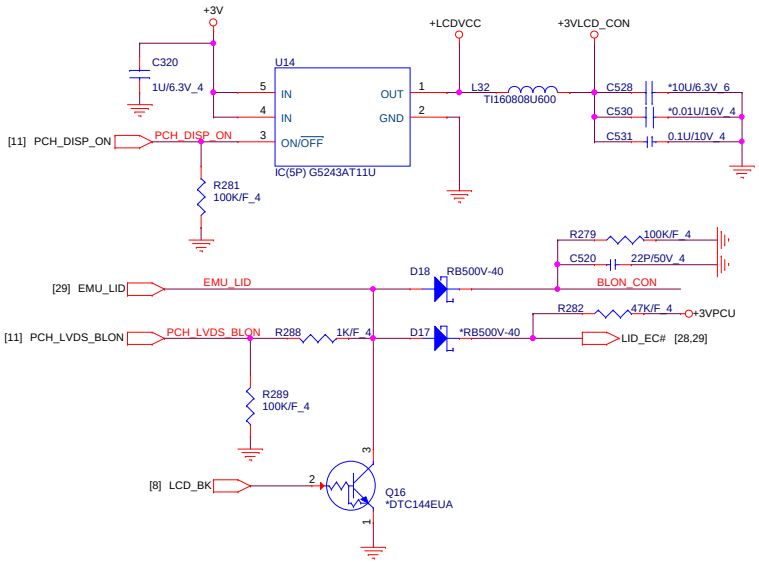
PROJECT : VOLKS_Comal 14"

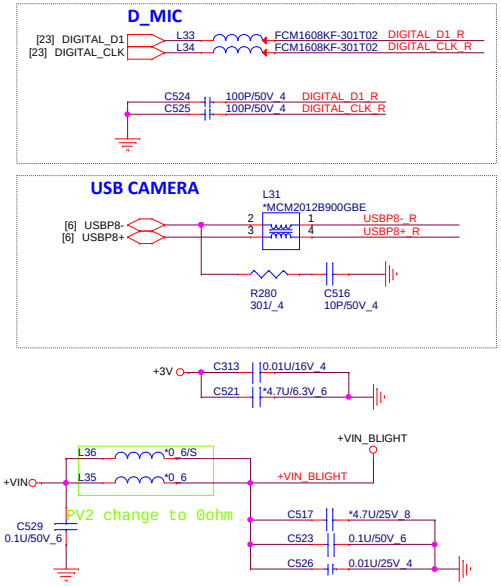
Quanta Computer Inc.

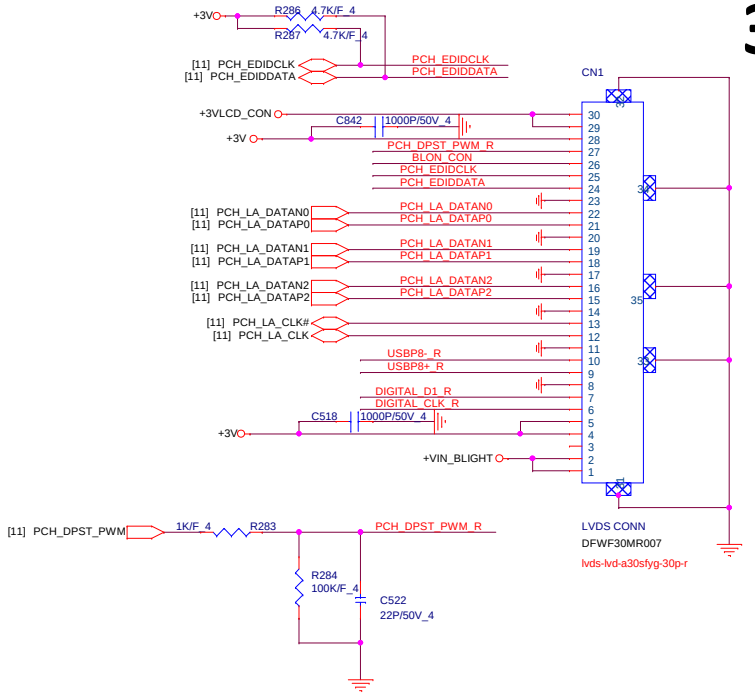
Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

Date: Thursday, September 20, 2012 Sheet 29 of 42

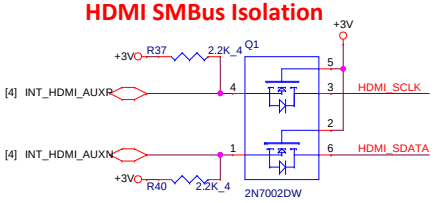
LVDS Conn.

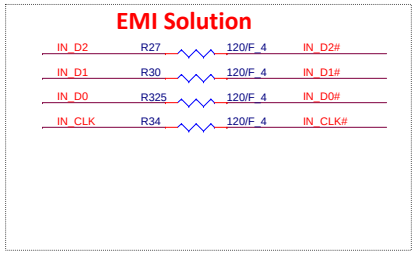


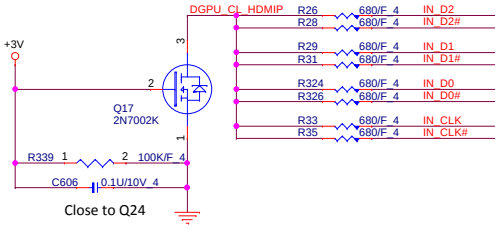


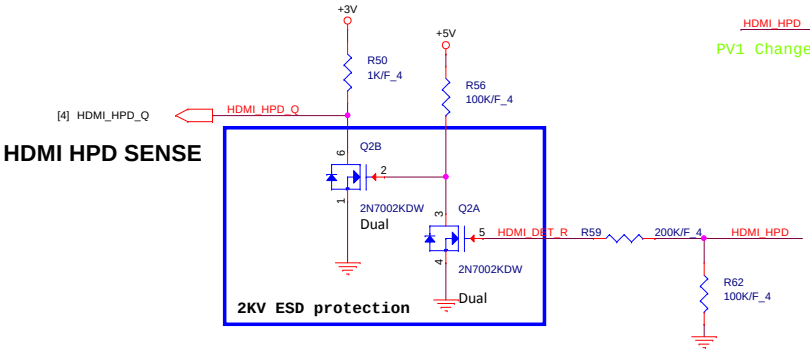


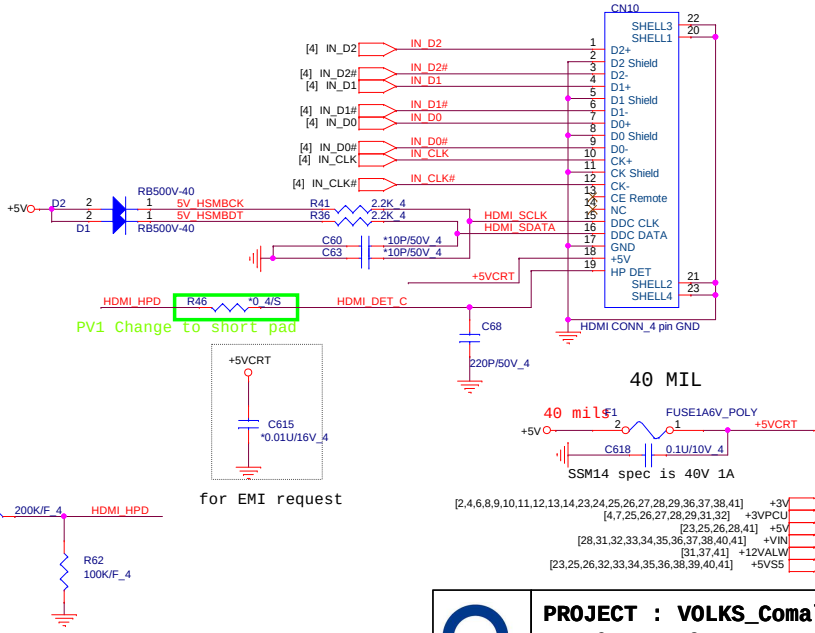
HDMI Conn.









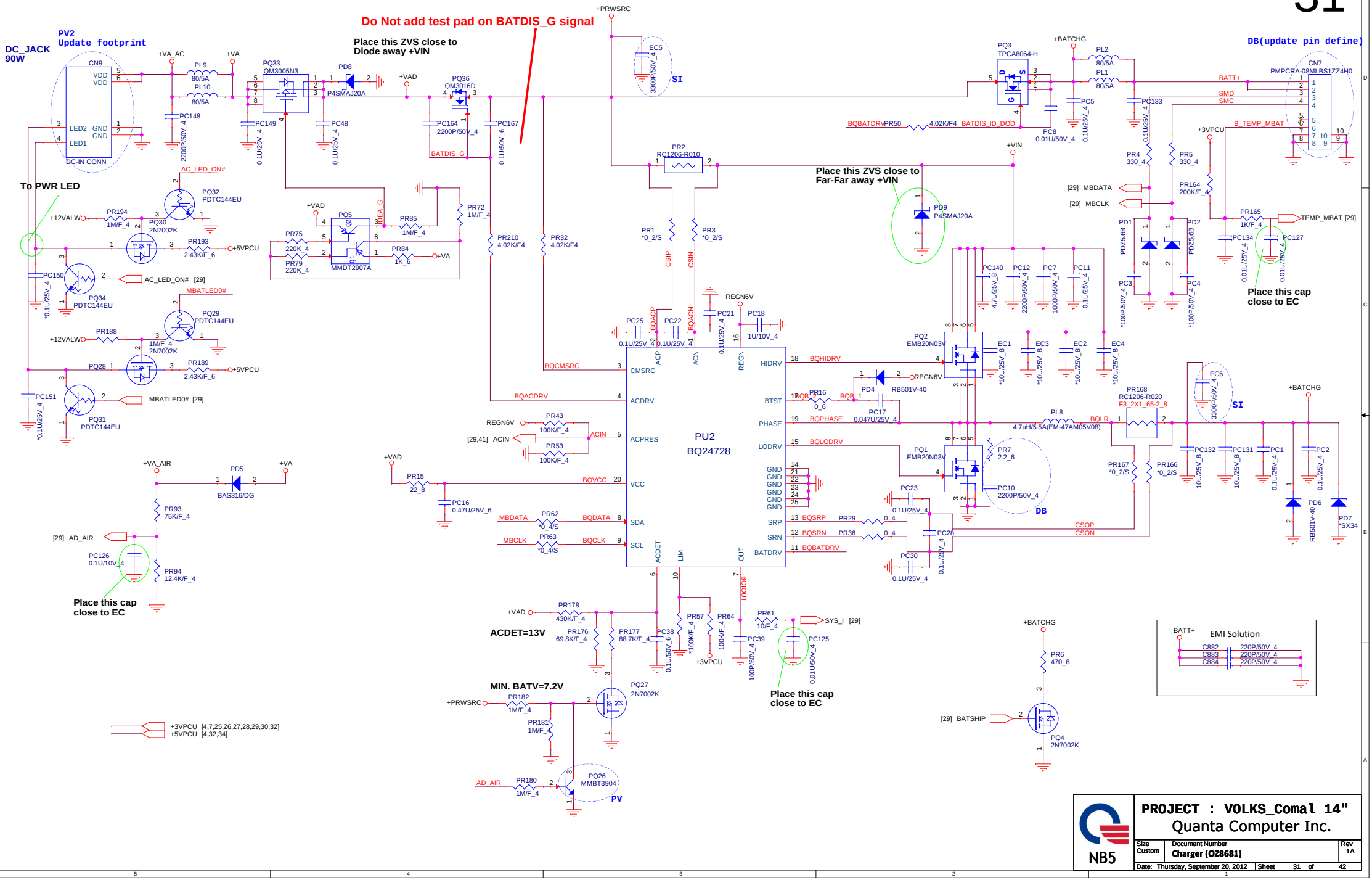


NB5

PROJECT : VOLKS_Comal 14"

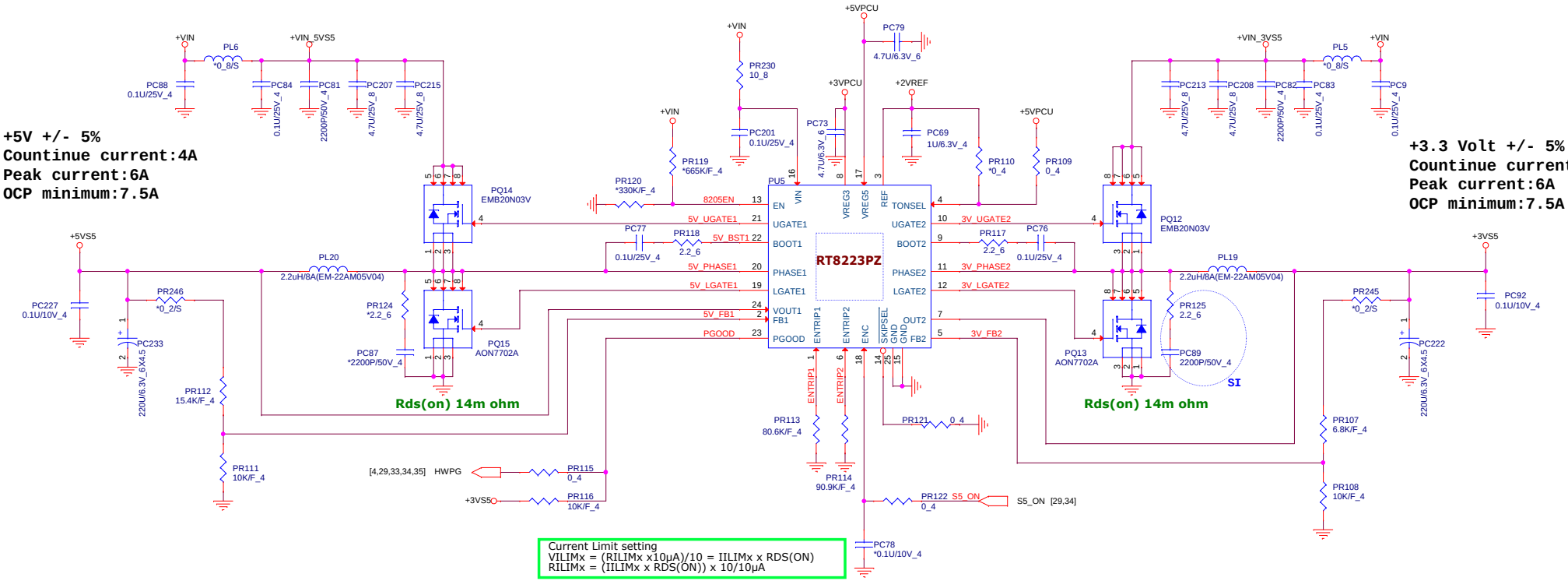
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A
Date: Thursday, September 20, 2012	Sheet 30of 42	

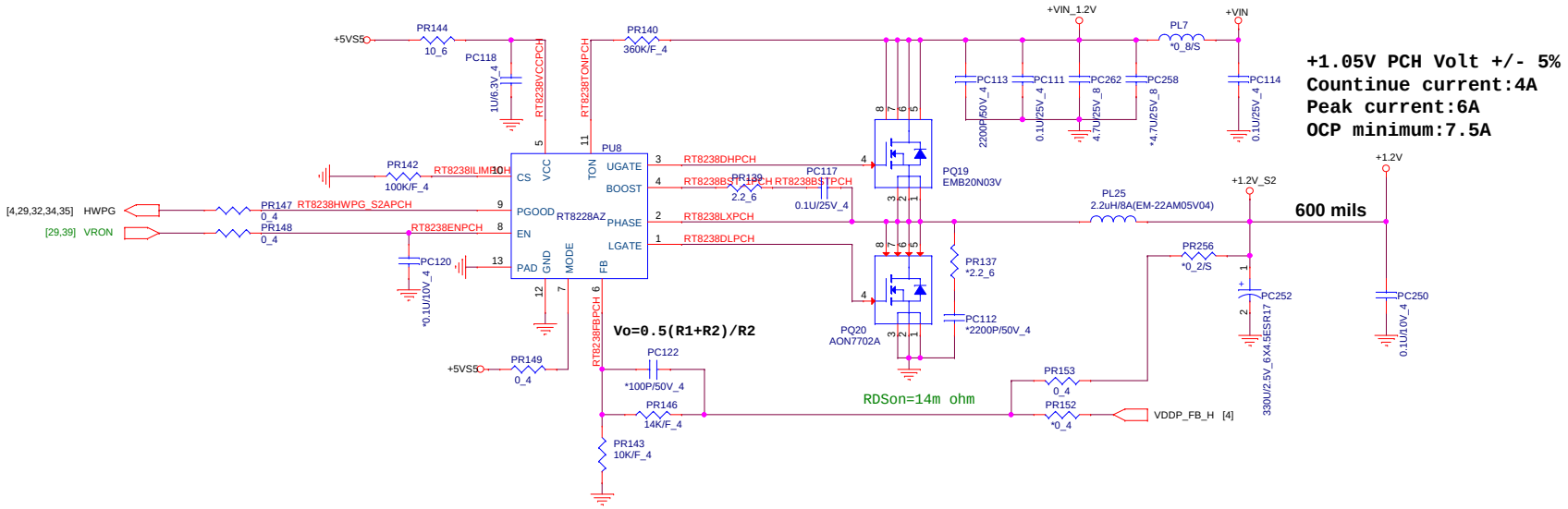

Do Not add test pad on BATDIS_G signal
PV2
Update footprint
DC_JACK
90W
DC-IN CONN
Place this ZVS close to
Diode away +VIN
Place this ZVS close to
Far-Far away +VIN
DB(update pin define)
To PWR LED
PU2
BQ24728
ACDET=13V
MIN. BATV=7.2V
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
EMI Solution
PROJECT : VOLKS_Comal 14"
Quanta Computer Inc.
NB5
Charger (OZ8681)
Thursday, September 20, 2012

+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

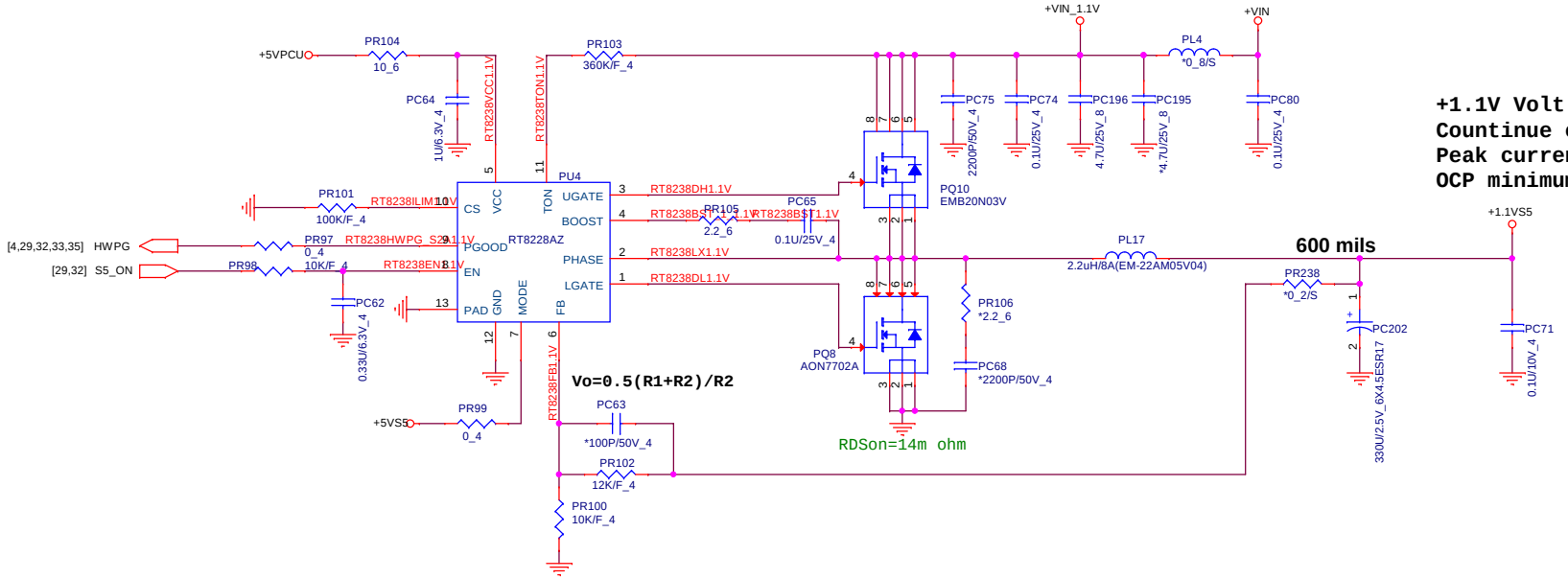
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

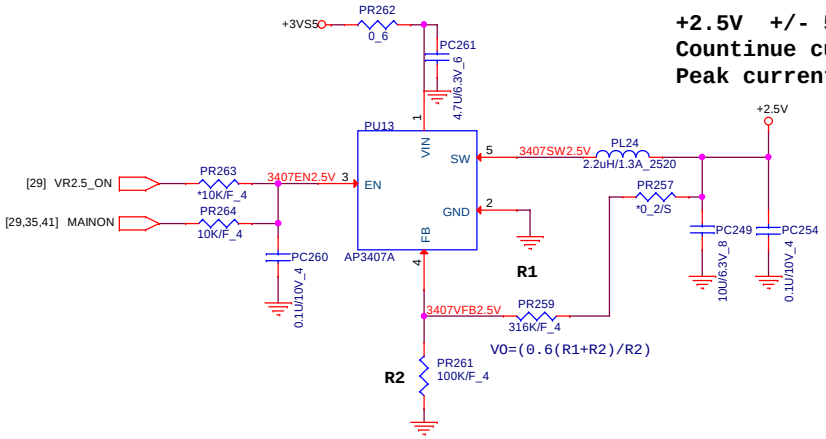


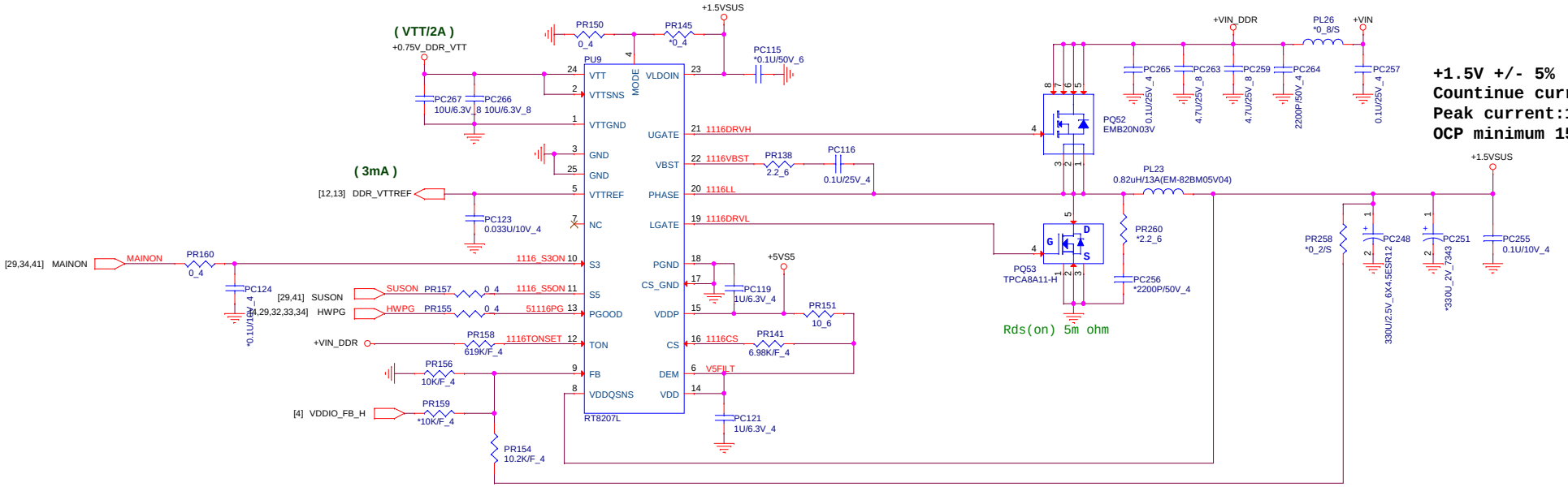
NB5	PROJECT : VOLKS_Comal 14" Quanta Computer Inc.	
Size Custom	Document Number 3/5VS5 (RT8223P)	Rev 1A
Date: Thursday, September 20, 2012	Sheet 32 of 42	



NB5	PROJECT : VOLKS_Comal 14"		
	Quanta Computer Inc.		
Size Custom	Document Number +1.2V (RT8228)		Rev 1A
Date: Thursday, September 20, 2012	Sheet 33	of 42	


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A
Vo=0.5(R1+R2)/R2
RDSon=14m ohm
600 mils
PU4
RT8228AZ
PQ10
EMB20N03V
PQ8
AON7702A
PL17
2.2uH/8A(EM-22AM05V04)
+VIN_1.1V
+VIN
+1.1VS5
+5VPCU
+5VS5
[4,29,32,33,35] HWPG
[29,32] S5_ON


+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
VO=(0.6(R1+R2)/R2)
R1
R2
PU13
AP3407A
+3VS5
+2.5V
[29] VR2.5_ON
[29,35,41] MAINON



+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

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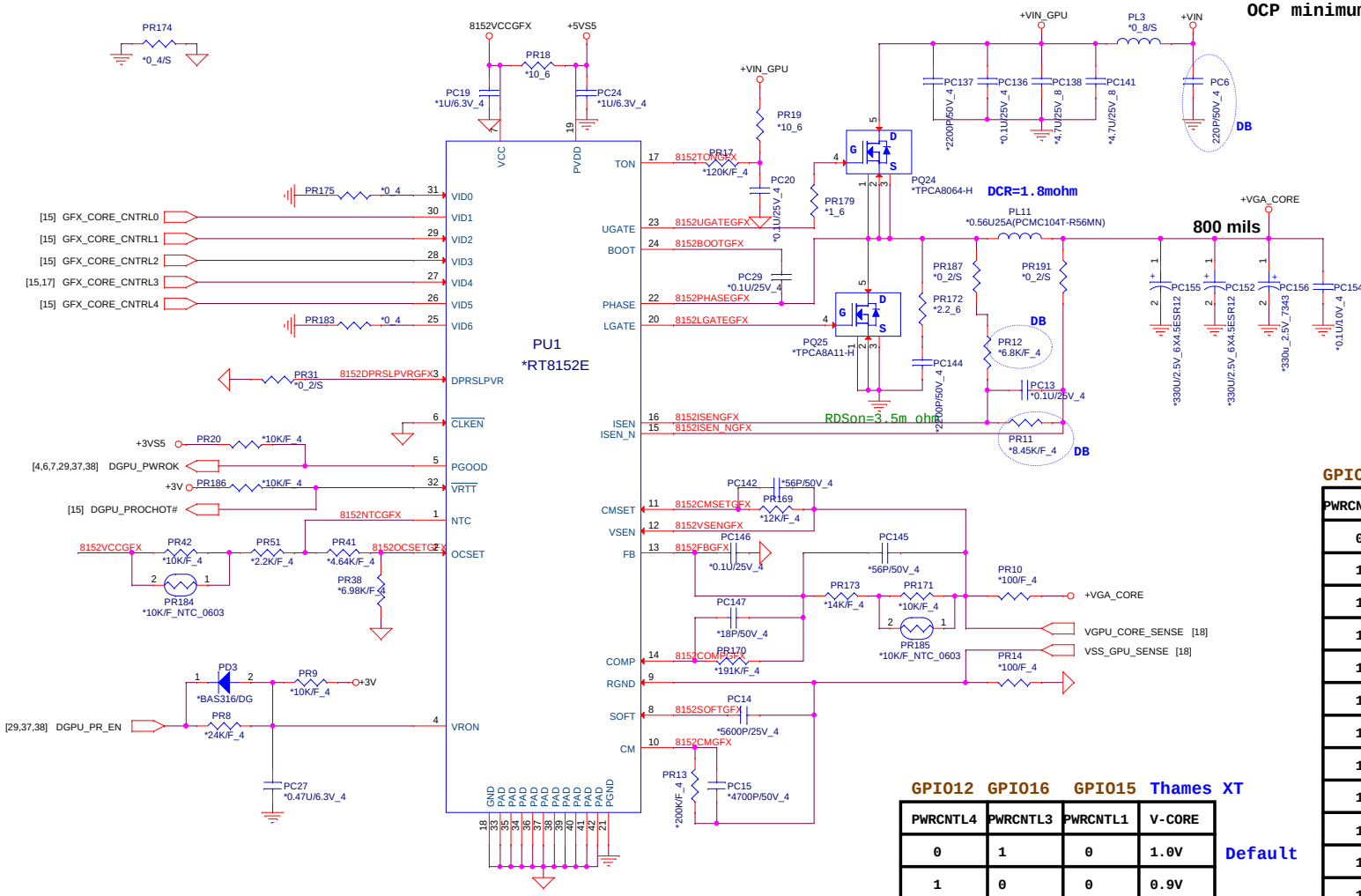
VGA Core

+VGA_UMA +/- 5%
Countinue current:18A
Peak current:22A
OCP minimum 25A



GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Mars XT	
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	Default
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	PV

GPIO12	GPIO16	GPIO15	Thames XT	
PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE	
0	1	0	1.0V	Default
1	0	0	0.9V	
1	0	1	0.875V	

NB5

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Custom	+VGACORE NCP3218G)	1A
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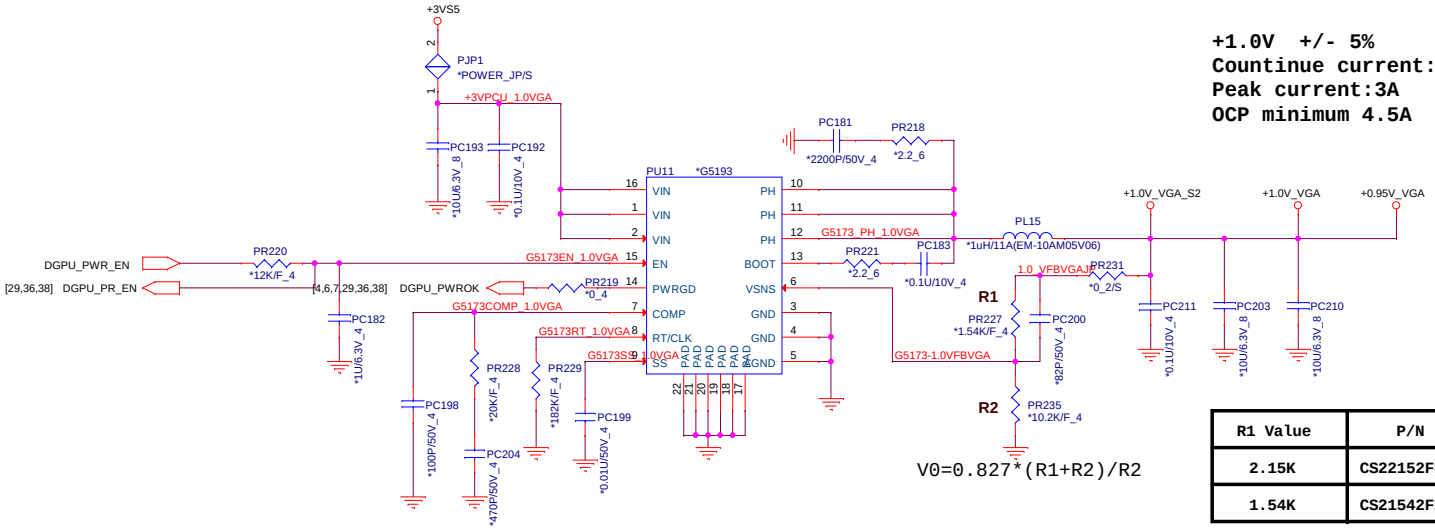


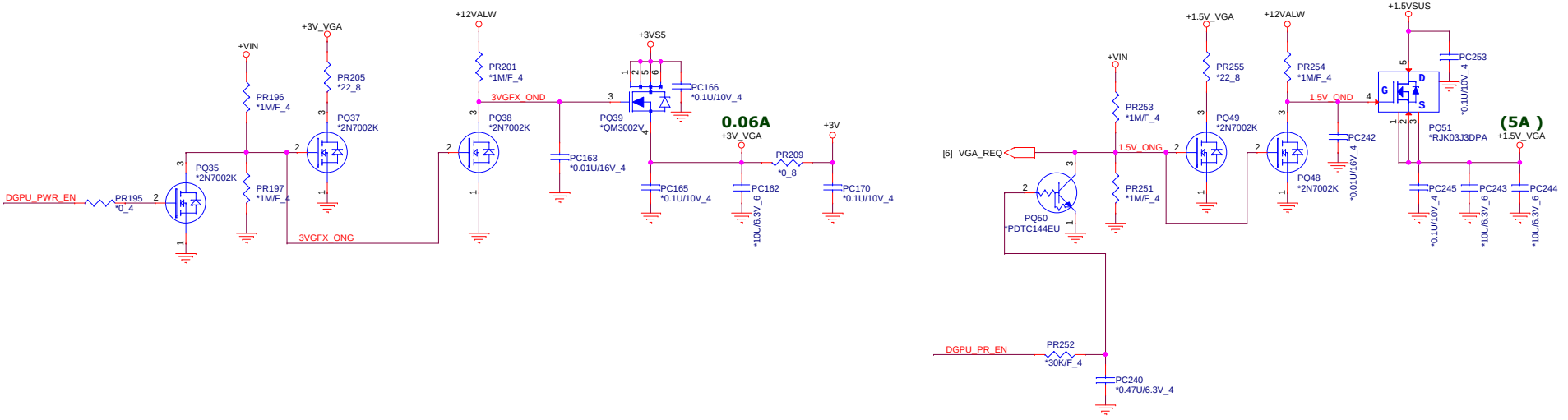
+1.0V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

+3V [2,4,6,8,9,10,11,12,13,14,23,24,25,26,27,28,29,30,36,38,41]
+VIN [28,30,31,32,33,34,35,36,38,40,41]

+3VS5 [6,8,9,10,25,26,27,29,32,34,36,41]
+5VS5 [23,25,26,32,33,34,35,36,38,39,40,41]
+3V_VGA [18]
+12VALW [31,41]
+1.5VSUS [2,3,4,5,12,13,35,41]
+1.5V_VGA [18,20,21,22]
+1.8V_VGA [15,16,18,19,38]
+3V_DELAY [15,17,18]
+VGA_CORE [18,36]

R1 Value	P/N	1.0V_VGA
2.15K	CS22152FB07	1.0V
1.54K	CS21542FB02	0.95V

$$V0=0.827*(R1+R2)/R2$$



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Custom	+VGA POWER	1A

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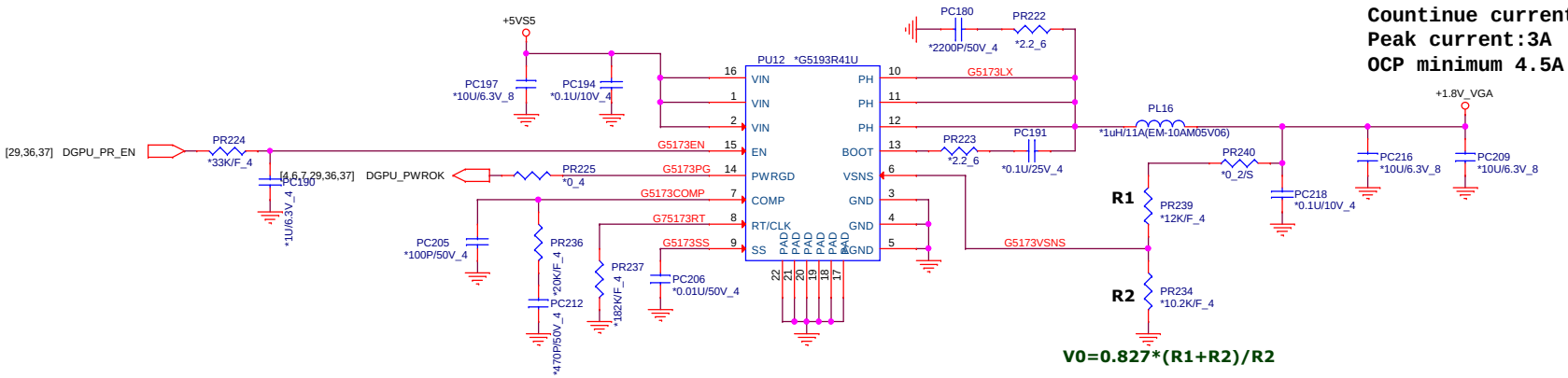
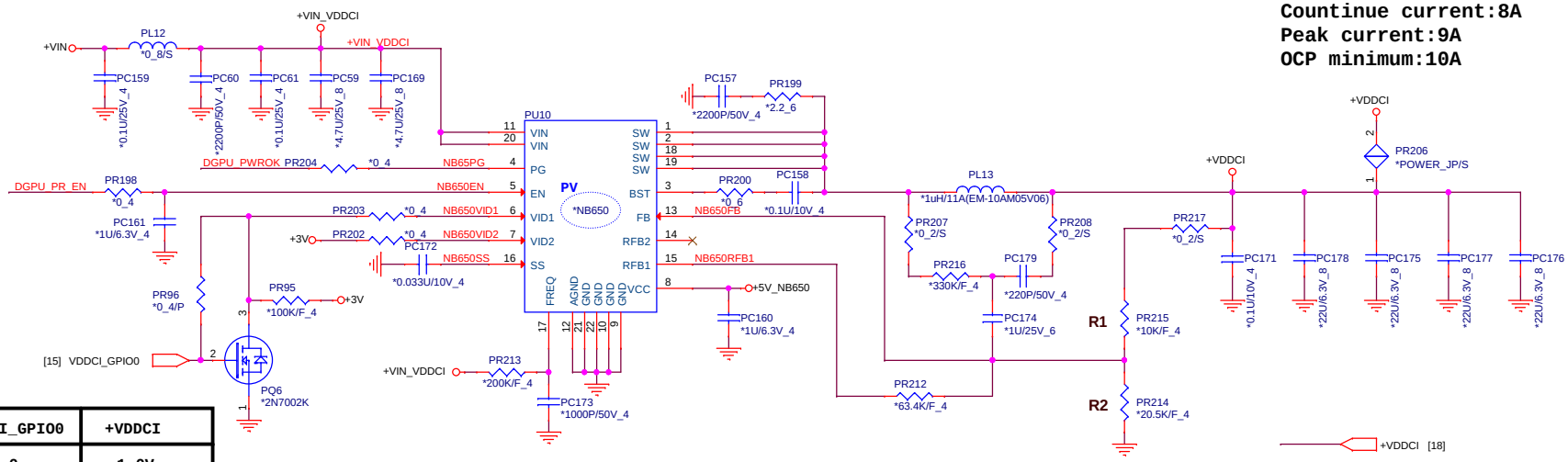
+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A



V0=0.827*(R1+R2)/R2

+VDDCI +/- 5%
Countinue current:8A
Peak current:9A
OCP minimum:10A



VDDCI_GPIO1	VDDCI_GPIO0	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

NB5

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Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A

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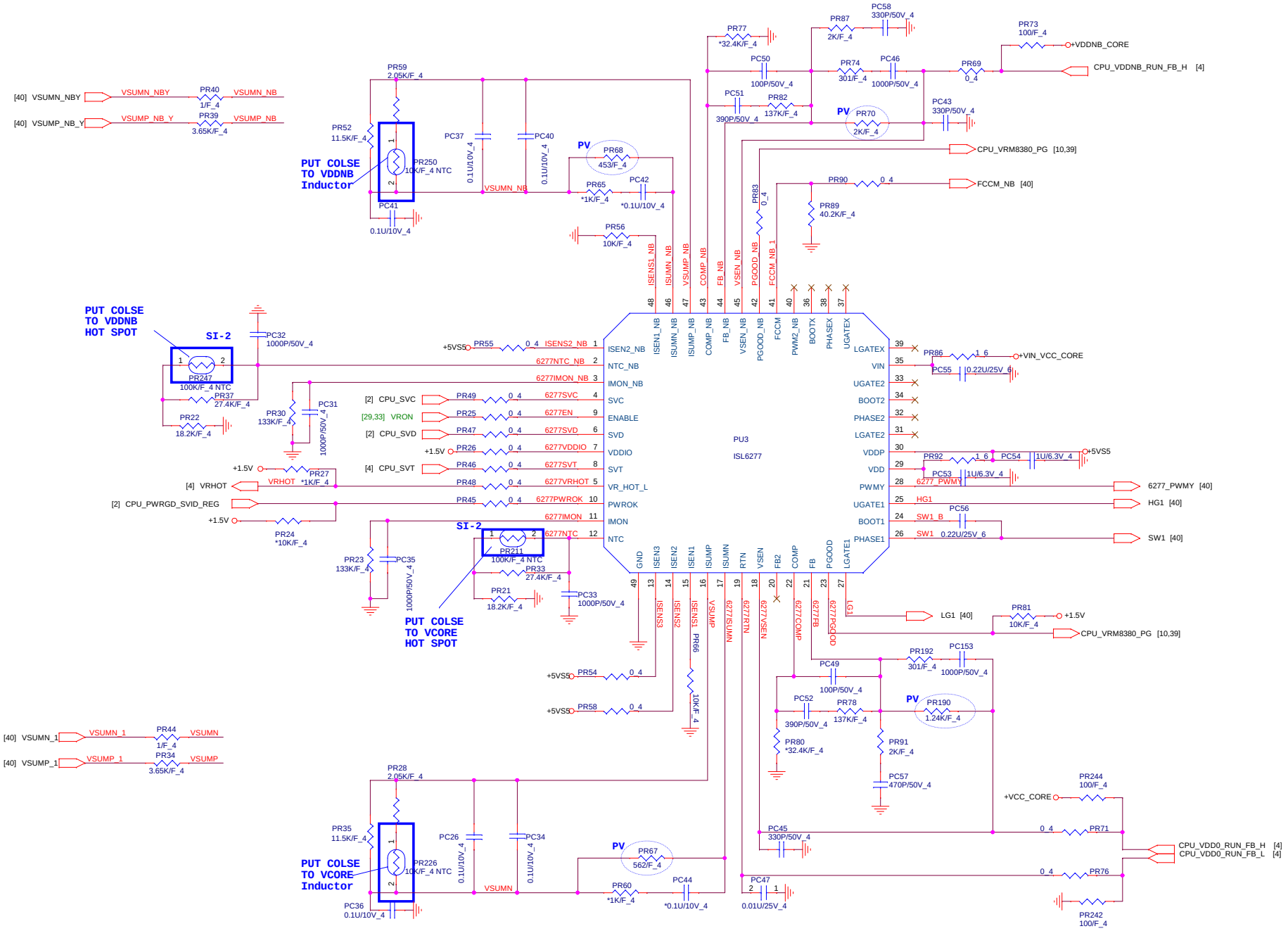

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Quanta Computer Inc.	
NB5	
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Rev: 1A	
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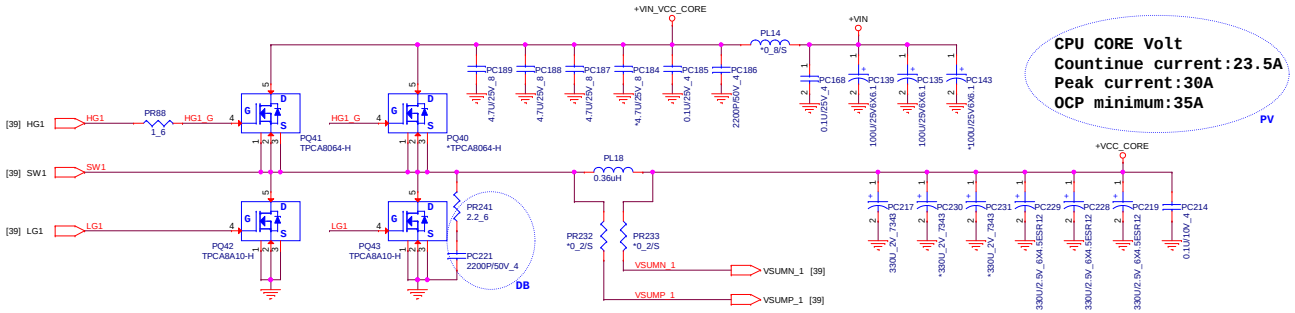

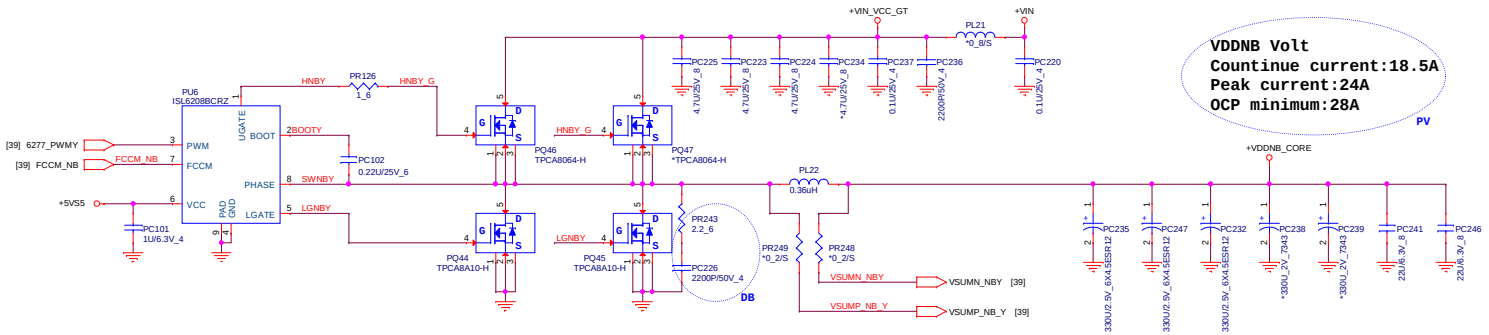

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6208	1A

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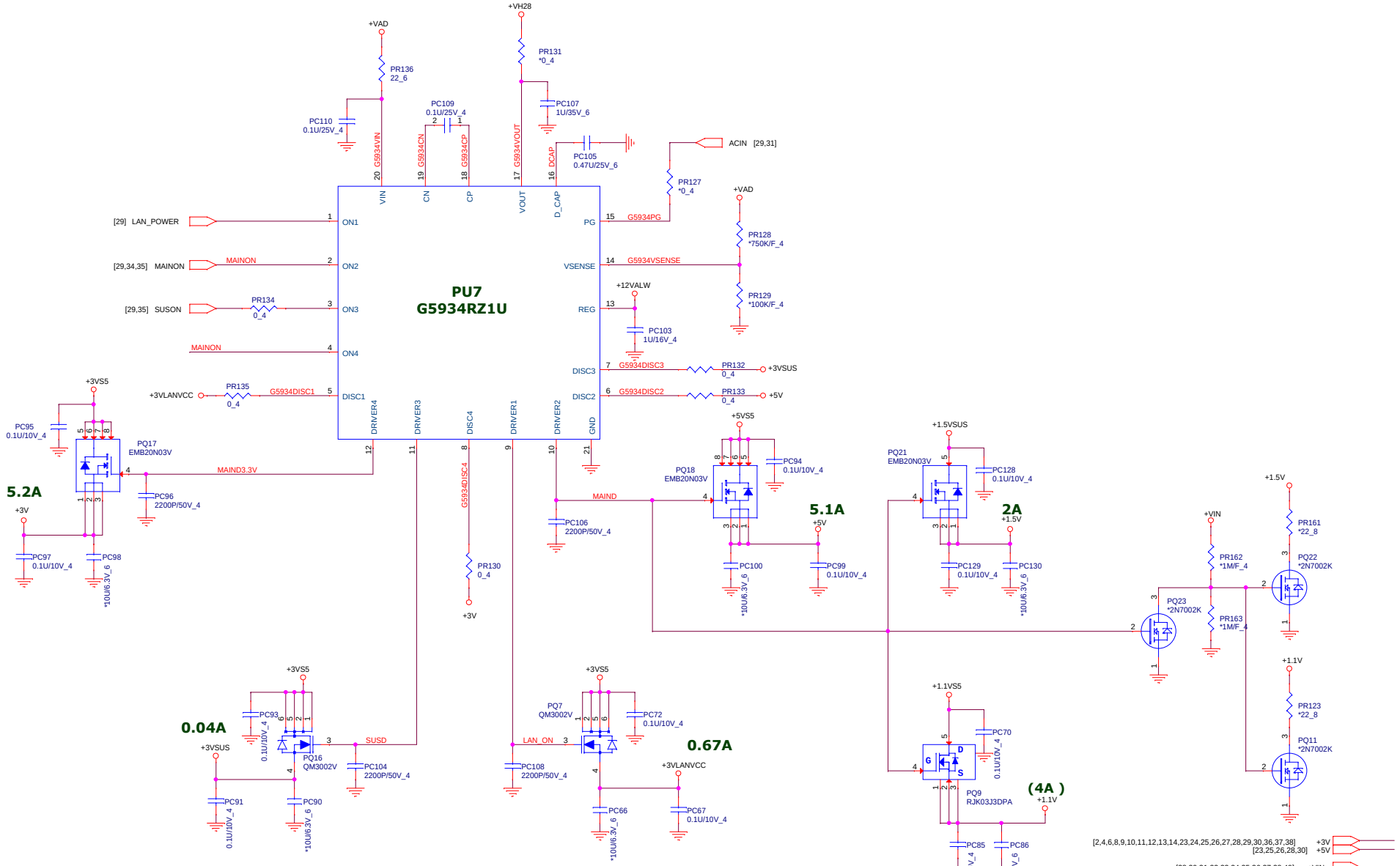

NB5

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Custom	Dis-charge IC (SLG55448V)	1A

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Size	Document Number	Rev
C	History	1A

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