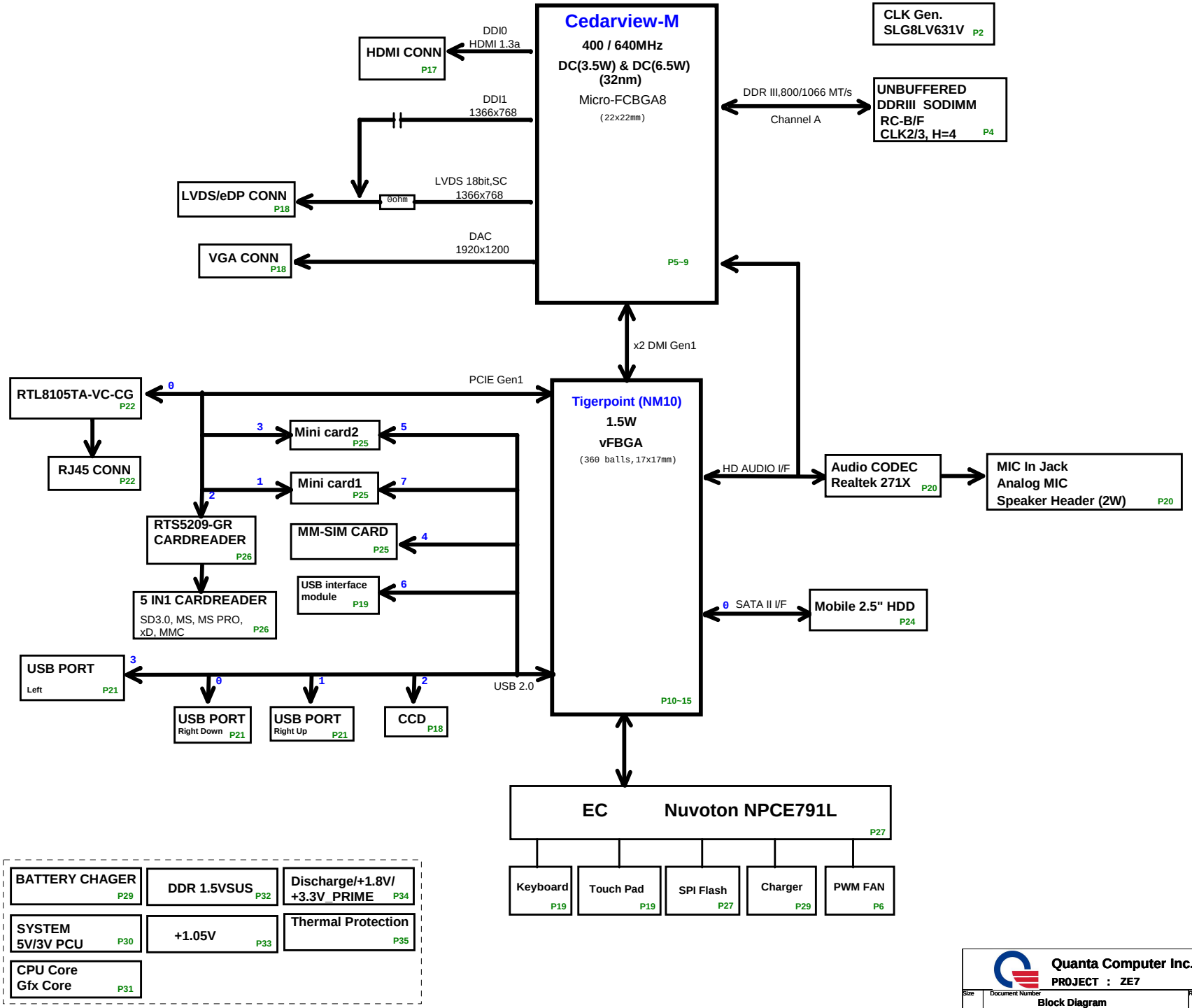
ZE7 Block Diagram (Intel Cedar Trail-M Platform)



Quanta Computer Inc.

PROJECT : ZE7

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	Block Diagram	1B

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CLK GEN (CLK)

02

+3V
L32
PBY160808T-301Y-N/2A/300ohm_6
VDD_CLK_3.3V
Place close to L32
C285 10U/10V_8
C278 .1U/10V_4
C254 .1U/10V_4
C242 .1U/10V_4
0.1uF near every power pin

VDD_CLK_1.5V
+1.5V
R219 2.2/J_6
L27
PBY160808T-301Y-N/2A/300ohm_6
<20100819_FAE Poyueh> Add 2.2ohm resistor for noise suppress
C225 .1U/10V_4
C277 .1U/10V_4
C224 10U/10V_8
Place close to L27
0.1uF near every power pin

VDD_IO can be ranging from 1.05V to 3.3V.

+1.05V
R221 *0/short_6
L28
PBY160808T-301Y-N/2A/300ohm_6
VDD_CLKIO_1.05V
Place close to L28
C228 10U/10V_8
C229 .1U/10V_4
C249 .1U/10V_4
C253 .1U/10V_4
0.1uF near every power pin

U12

5	VDD_REF_3.3		
9	VDD_PCI_3.3		
14	VDD_48M_3.3		
30	VDD_SRC_IO_1.05		
35	VDD_SRC_IO_1.05		
48	VDD_CPU_IO_1.05		
1	NC		
2	NC		
13	NC		
54	NC		
3	XTAL_OUT	CG_XOUT	
4	XTAL_IN	CG_XIN	
7	SDA	SMBDT1	[4,13,25] SMBDT1
8	SCL	SMBCK1	[4,13,25] SMBCK1
15	USB48_1/FSB	FSB	
17	USB48_2	USB_48M	R312 33/J_4 [10] CLKUSB_48
6	REF/FSC	FSC	R293 33/J_4 [13] 14M_ICH
10	PCIF/ITP_EN	ITP_EN	R296 22/J_4 [12] PCLK_ICH; R304 22/J_4 [27] LCLK_EC
11	25MHz/PCI_2/SEL_33MHz	33M_SEL	R291 33/J_4 [25] PCLK_DEBUG
12	VSS_PCI		
16	VSS_48M		
22	VSS_LCD		
24	VSS_SATA		
39	VSS_SRC		
51	VSS_CPU		
56	VSS_REF		
57	Thermal Pad		

23	VDD_CORE_1.5		
45	VDD_CORE_1.5		
36	PCI_STOP#	PM_STPPCI# R	R251 *0/J_4 → PM_STPPCI# [13]
42	CPU_STOP#	PM_STPCPU# R	R229 *0/J_4 → PM_STPCPU# [13]
53	CPU_0		CLK_MCH_BCLK [6]
52	CPU_0#		CLK_MCH_BCLK# [6]
50	CPU_1		CLK_DDR3_REFCLK [8]
49	CPU_1#		CLK_DDR3_REFCLK# [8]
44	SRC_1/CPU_ITP		CLK_PCIE_LANP [22]
43	SRC_1/CPU_ITP#		CLK_PCIE_LANN [22]
41	SRC_2		CLK_PCIE_MNC_P [25]
40	SRC_2#		CLK_PCIE_MNC_N [25]
38	SRC_3		CLK_PCIE_MPC_P [25]
37	SRC_3#		CLK_PCIE_MPC_N [25]
34	SRC_4		CLK_PCIE_DMIP [5]
33	SRC_4#		CLK_PCIE_DMIN [5]
32	SRC_5		CLK_PCIE_MMC_P [26]
31	SRC_5#		CLK_PCIE_MMC_N [26]
28	SRC_6		CLK_PCIE_ICH [10]
27	SRC_6#		CLK_PCIE_ICH# [10]
18	DOT96/SRC7	DREFCLK_R	R299 *0/J_4 → DREFCLK [5]
19	DOT96#/SRC7#	DREFCLK#_R	R300 *0/J_4 → DREFCLK# [5]
20	LCD_CLK		DREFSSCLK [5]
21	LCD_CLK#		DREFSSCLK# [5]
26	SATA		CLK_PCIE_SATA [11]
25	SATA#		CLK_PCIE_SATA# [11]
47	CLKREQ_A#	CLKREQ_LAN# R	R204 475/F_4 → CLKREQ_LAN# [22]
46	CLKREQ_B#	CLKREQ_MPC# R	R199 475/F_4 → CLKREQ_MPC# [25]
29	CLKREQ_C#	CLKREQ_MMC# R	R284 475/F_4 → CLKREQ_MMC# [26]
55	CKPWRGD/PD#	HWPG	HWPG [13,16,27]

<20100803_Sam> Reserve 0ohm to connect to CK505, 10Kohm pull up is required.

From SB		
To CPU (Host CLK)	100 MHz	
To CPU (DDR3 IO CLK)	100 MHz	
To LAN (LAN)	100 MHz	
To Mini Card 2 (3G/Wimax)	100 MHz	<20101109> Place R235/ R241/ R248/ R254 close to U13
To Mini Card 1 (WLAN)	100 MHz	
To CPU (DMI CLK)	100 MHz	
To Card Reader (MMC)	100 MHz	
To SB (DMI CLK)	100 MHz	
To CPU (PLL CLK)	96 MHz	
To CPU (DPLSS CLK)	100 MHz	<20110110> DPL_REFSSCCLK is used to drive internal registers and logics of the display interface and therefore needs to be present at all times.
To SB (SATA CLK)	100 MHz	

<20100819> Add 475ohm resistors to prevent current leakage

Control SRC_1 Register B5b6 for CLKREQ_A#
0 = SRC1, 1=SRC2
Control SRC_3 Register B5b4 for CLKREQ_B#
0 = SRC3, 1=SRC4
Control SRC_5 Register B5b3 for CLKREQ_C#
0 = SRC5, 1=SRC6

C357 *0.1U/10V_4
<20110221> Reserve 0.1F cap to solve that PCICLK (EC 33MHz) sometimes will change to 25MHz after flash BIOS and restart in first time issue.

Y2 14.318MHZ
Load Capacitance=20p
C238 33P/50V_4 CG_XIN
C236 33P/50V_4 CG_XOUT

<Layout note>
Crystal place within 500mil of CK505

R311 *20K/J_4
R310 *100K_4
<20110110> CFG input hardware strapping to allocate PLL assignment.
LOW = Both CPU and SRC clock drive from PLL3
HIGH = CPU clock drive from PLL1, SRC clock drive from PLL3.
Contains 100kΩ pull-down resistor.

SLG8LV631V

+3V R313 *10K/J_4 R306 10K/J_4 ITP_EN
1 = Pin 43/44 as CPU_ITP
0 = Pin 43/44 as SRC_1

+3V R301 10K/J_4 R295 *10K/J_4 33M_SEL
1 = Pin 11 as 33MHz
0= Pin 11 as 25MHz

FSC	FSB	Frequency
0	0	133MHz
0	1	166MHz
1	1	200MHz
1	*0*	***100MHz***

<20100720_Sam> Keep 100MHz as default.

+3V R289 10K/J_4 R259 *10K/J_4 FSC FSB R317 *10K/J_4 R318 10K/J_4 +3V

<EMI>
USB_48M C280 *10P/50V_4
ITP_EN C259 *10P/50V_4
FSB C279 *10P/50V_4
FSC C245 *10P/50V_4
33M_SEL C266 *10P/50V_4

+3V
PM_STPPCI# R R250 10K/J_4
PM_STPCPU# R R230 10K/J_4
CLKREQ_MPC# R R213 10K/J_4
CLKREQ_MMC# R R279 10K/J_4
CLKREQ_LAN# R R212 10K/J_4

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	CLOCK GENERATOR	1B

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	Reserved			1B
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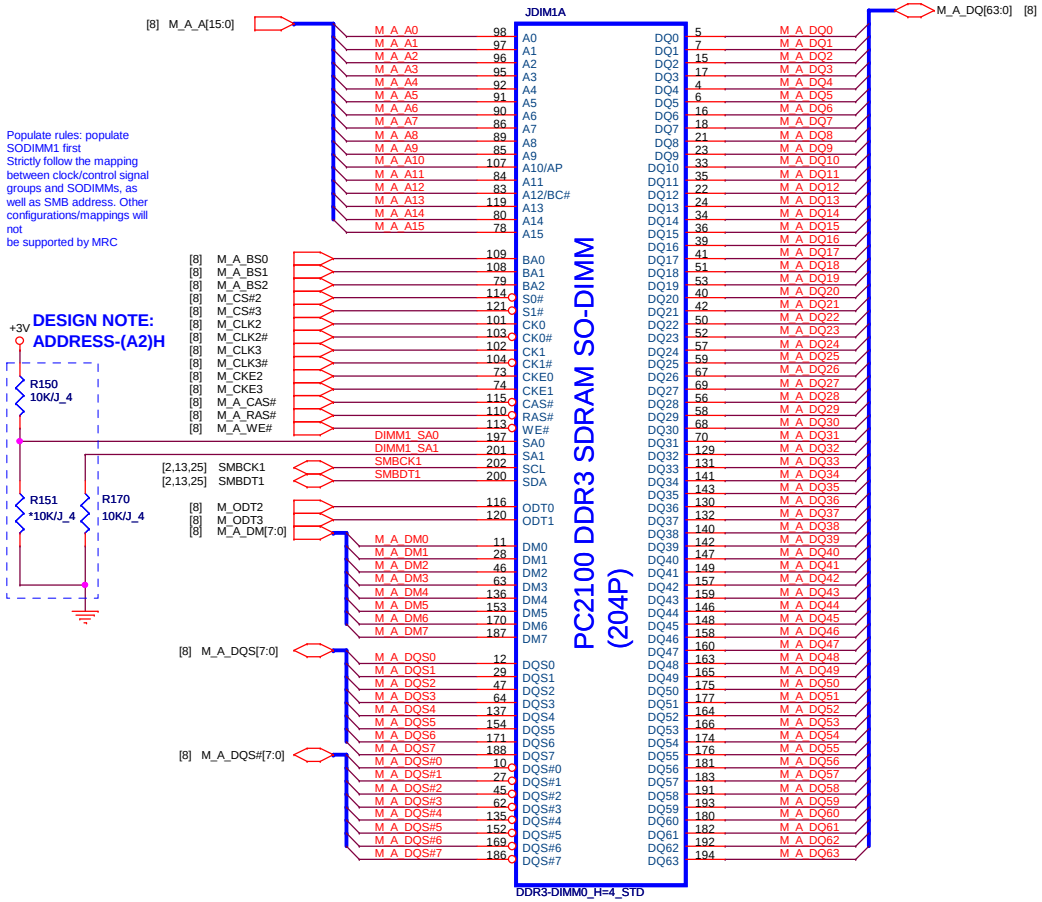
DDR_STD(DDR)

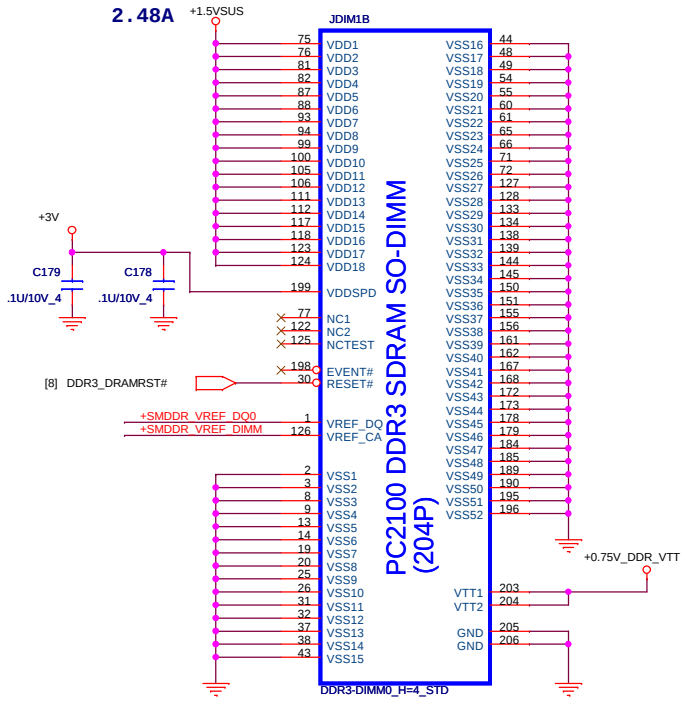
DIMM0 H=4mm

04

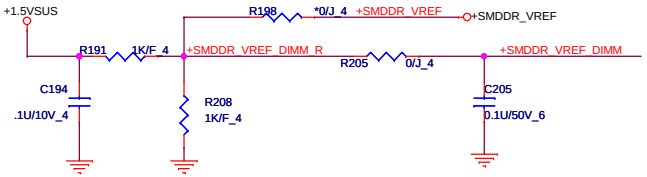
Populate rules: populate SODIMM1 first
Strictly follow the mapping between clock/control signal groups and SODIMMs, as well as SMB address. Other configurations/mappings will not be supported by MRC

DESIGN NOTE: ADDRESS-(A2)H

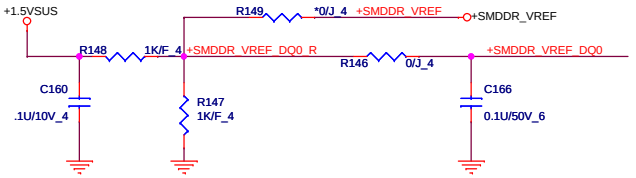


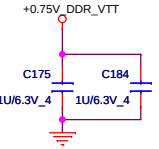


<Layout note>
PLACE TWO 1K RESISTORS CLOSE TO CPU DIMM ON DDR_VREF_CA

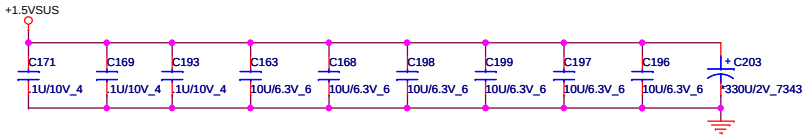


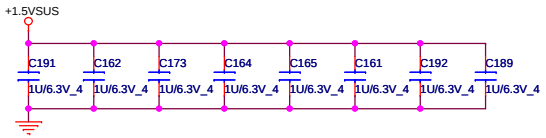
<Layout note>
PLACE TWO 1K RESISTORS CLOSE TO CPU DIMM ON DDR_VREF_DQ



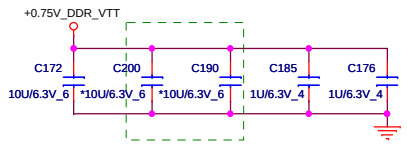


Place these Caps near DIMM0

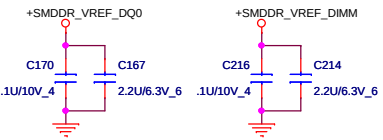




<20100827> Add by DG request



LAYOUT NOTE: PLACE CAPS NEAR DIMM-0



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	DDRIII SO-DIMM-0	1B
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Cedar View (CPU)

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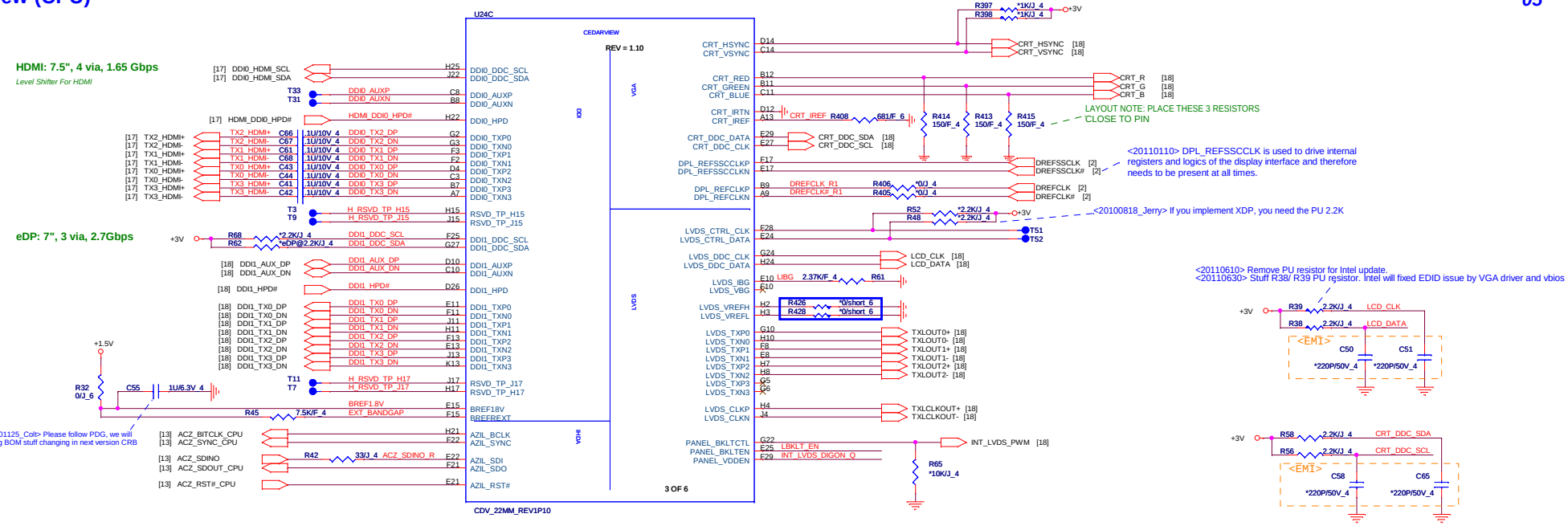
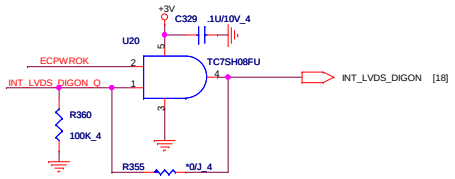
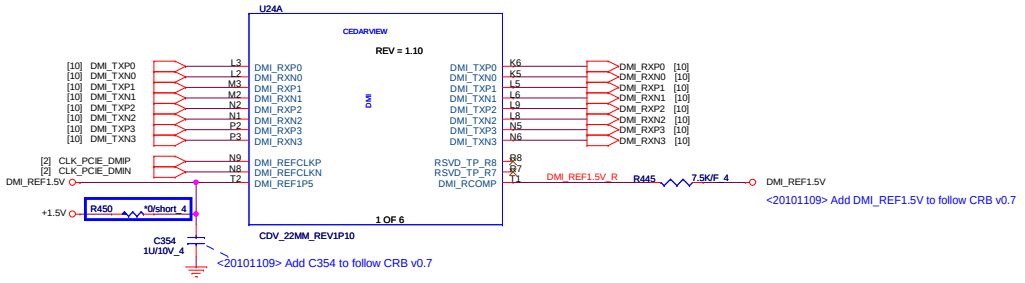
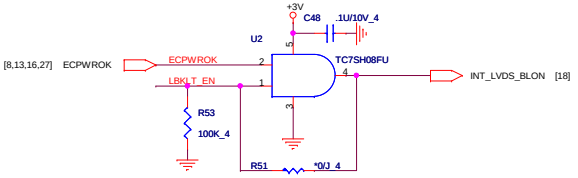


LCD Panel Power (LDS)





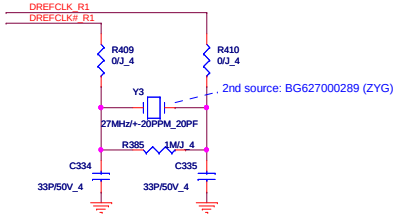
LCD Panel Backlight (LDS)



For HDMI deep color mode support (HDM)

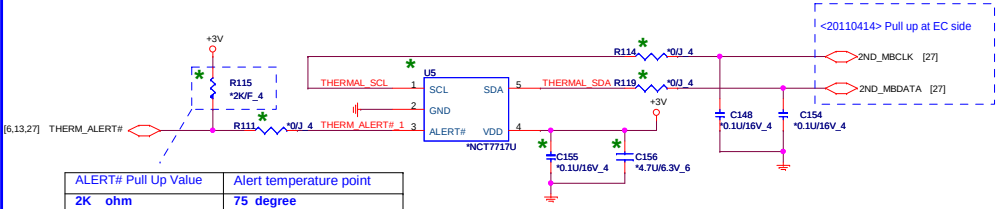
<20100727_Sam> Customer must to use 27MHz due to accuracy concerns(<1000ppm) from Intel silicon perspective.

LAYOUT NOTE: PLACE CLOSE TO PIN



THERMAL SENSOR (THM)

<20110414> Unstuff Thermal Sensor and related circuit.



ALERT# Pull Up Value	Alert temperature point
2K ohm	**75 degree**
7.5K ohm	90 degree
10.5K ohm	100 degree
14K ohm	105 degree
18.7K ohm	110 degree

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	Cedarview DMI/Display	1B

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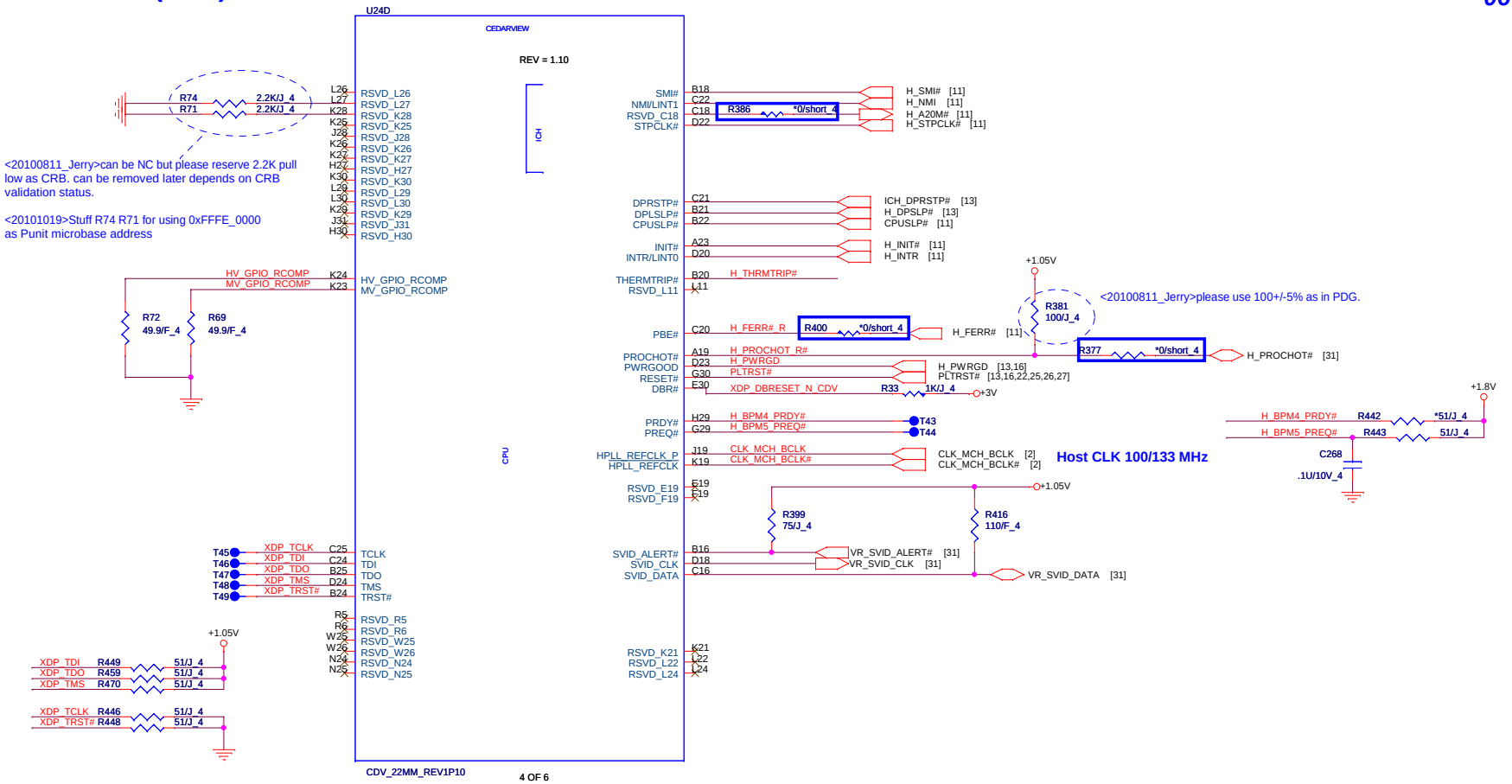
Cedar View (CPU)

06

U24D

CEDARVIEW

REV = 1.10



CDV_22MM_REV1P10

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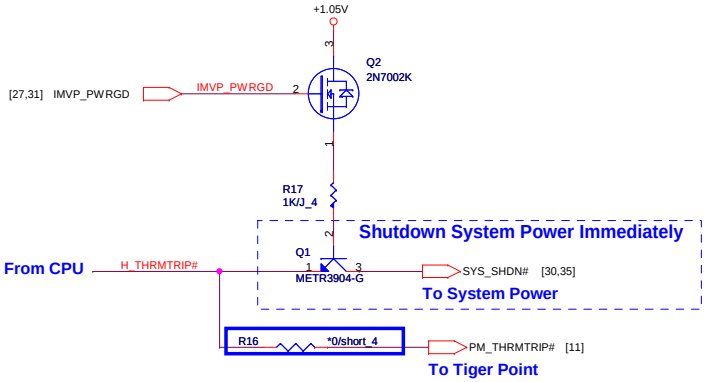
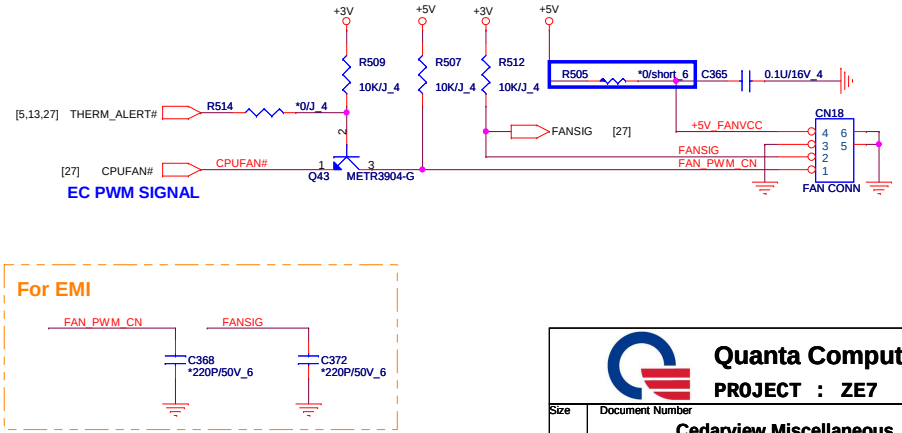
125 Degree Protection(CPU)



CPU FAN CTRL(THM)



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	Cedarview Miscellaneous	1B
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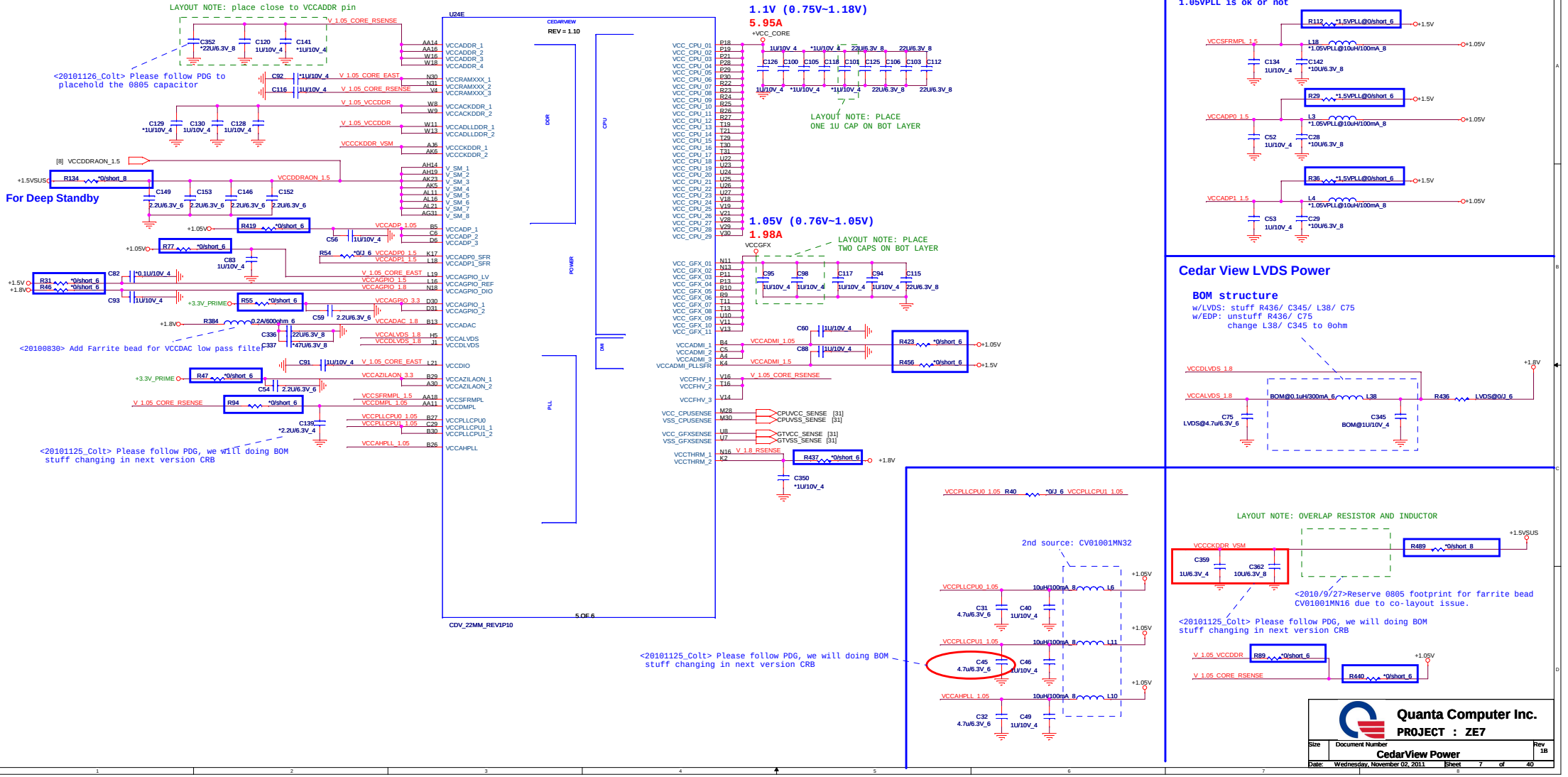
Cedar View (CPU)



Cedar View PLL Power

07

Default stuff 1.5VPLL, Intel verify whether 1.05VPLL is ok or not

Cedar View LVDS Power

BOM structure

w/LVDS: stuff R436/ C345/ L38/ C75
w/EDP: unstuff R436/ C75
change L38/ C345 to 0ohm

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	CedarView Power	1B
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Cedar View (CPU)

08

U24B

CEDARVIEW

REV = 1.10

<Layout note>
PLACE RESISTORS AND CAP CLOSE TO CPU DDR_VREF PIN

[7] VCCDDRAON_1.5 — R482 1K/F_4 — +SMDDR_VREF — R492 *0/J_4 — R483 *0/short_4 — R493 1K/F_4 — C360 0.1U/16V_4

<20100810_Jerry> Please refer to Cedar Trail CPET HW section(#454349),
it is to implement Deep Standby. And please waiting the whitepaper for implementation detail.

<20100817_Jerry>DELAY_VR_PWRGOOD on CDV should be connected to the XDP_PWRGOOD because the SV folks expressed a preference on using PWROK over PWRGOOD for CDV. This has changed from PNV to CDV.

[5,13,16,27] ECPWROK — R99 121/F_4 — T53 — R98 100/F_4

<20110520>Change 12.1K to 121ohm to follow CRBv1.5

<20110520>Change 10K to 100ohm to follow CRBv1.5

R485 274/F_4 — R488 22.6/F_4 — C361 *0.01U/25V_4 — R484 33.2/F_4

<20100811_Jerry> R485 please follow CRB schematic. (274ohm)

[4] M_A_A[15:0]	M_A_A0	AK14	DDR3_MA0	
	M_A_A1	AK16	DDR3_MA1	
	M_A_A2	AJ14	DDR3_MA2	
	M_A_A3	AJ16	DDR3_MA3	
	M_A_A4	AK18	DDR3_MA4	
	M_A_A5	AH18	DDR3_MA5	
	M_A_A6	AJ18	DDR3_MA6	
	M_A_A7	AK20	DDR3_MA7	
	M_A_A8	AJ20	DDR3_MA8	
	M_A_A9	AH20	DDR3_MA9	
	M_A_A10	AJ12	DDR3_MA10	
	M_A_A11	AK21	DDR3_MA11	
	M_A_A12	AJ21	DDR3_MA12	
	M_A_A13	AJ8	DDR3_MA13	
	M_A_A14	AH22	DDR3_MA14	
	M_A_A15	AJ22	DDR3_MA15	
[4] M_A_WE#	M_A_WE#	AH10	DDR3_WE#	
[4] M_A_CAS#	M_A_CAS#	AJ10	DDR3_CAS#	
[4] M_A_RAS#	M_A_RAS#	AJ11	DDR3_RAS#	
[4] M_A_BS0	M_A_BS0	AK12	DDR3_BS0	
[4] M_A_BS1	M_A_BS1	AH13	DDR3_BS1	
[4] M_A_BS2	M_A_BS2	AK22	DDR3_BS2	
		AH12	DDR3_CS#0	
		AH8	DDR3_CS#1	
[4] M_CS#2	M_CS#2	AK11	DDR3_CS#2	
[4] M_CS#3	M_CS#3	AK8	DDR3_CS#3	
		AH23	DDR3_CKE0	
		AJ24	DDR3_CKE1	
[4] M_CKE2	M_CKE2	AK24	DDR3_CKE2	
[4] M_CKE3	M_CKE3	AH24	DDR3_CKE3	
		AK10	DDR3_ODT0	
		AK7	DDR3_ODT1	
[4] M_ODT2	M_ODT2	AL9	DDR3_ODT2	
[4] M_ODT3	M_ODT3	AJ7	DDR3_ODT3	
		AG15	DDR3_CK0	
		AF15	DDR3_CK#0	
		AF12	DDR3_CK1	
		AG12	DDR3_CK#1	
[4] M_CLK2	M_CLK2	AD17	DDR3_CK2	
[4] M_CLK2#	M_CLK2#	AC17	DDR3_CK#2	
[4] M_CLK3	M_CLK3	AC15	DDR3_CK3	
[4] M_CLK3#	M_CLK3#	AD15	DDR3_CK#3	
	DDR3_DRAMRST#_R	AK25	DDR3_DRAMRST#	
	DDR_VREF	AJ27	DDR3_VREF	
		AL28	DDR3_VREF_NCTF	
[2] CLK_DDR3_REFCLK		AC19	DDR3_REFP	
[2] CLK_DDR3_REFCLK#		AB19	DDR3_REFN	
	DDRAM_PWROK	AA5	DDR3_DRAM_PWROK	1.5V
	DELAY_VR_PWRGD_CDV	W7	DDR3_VCCA_PWROK	1.5V
	M_ODTPU	AJ26	DDR3_ODTPU	
	M_CMDPU	AJ25	DDR3_CMDPU	
	M_DQPU	AK27	DDR3_DQPU	
		AB11	RSVD_TP_AB11	
		AB13	RSVD_TP_AB13	
		AF19	RSVD_TP_AF19	
		AG19	RSVD_TP_AG19	
[4] M_A_DM[7:0]	M_A_DM0	Y28	DDR3_DM0	
	M_A_DM1	AB26	DDR3_DM1	
	M_A_DM2	AE30	DDR3_DM2	
	M_A_DM3	AB21	DDR3_DM3	
	M_A_DM4	AG11	DDR3_DM4	
	M_A_DM5	AG2	DDR3_DM5	
	M_A_DM6	AB8	DDR3_DM6	
	M_A_DM7	AA3	DDR3_DM7	

M_A_DQ[63:0] [4]	M_A_DQ0	Y30	DDR3_DQ0	
	M_A_DQ1	Y29	DDR3_DQ1	
	M_A_DQ2	AC30	DDR3_DQ2	
	M_A_DQ3	AC31	DDR3_DQ3	
	M_A_DQ4	W31	DDR3_DQ4	
	M_A_DQ5	W28	DDR3_DQ5	
	M_A_DQ6	AB28	DDR3_DQ6	
	M_A_DQ7	AB30	DDR3_DQ7	
	M_A_DQ8	AA24	DDR3_DQ8	
	M_A_DQ9	AA22	DDR3_DQ9	
	M_A_DQ10	AE27	DDR3_DQ10	
	M_A_DQ11	AE26	DDR3_DQ11	
	M_A_DQ12	AB27	DDR3_DQ12	
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	M_A_DQ14	AD25	DDR3_DQ14	
	M_A_DQ15	AD27	DDR3_DQ15	
	M_A_DQ16	AD29	DDR3_DQ16	
	M_A_DQ17	AE29	DDR3_DQ17	
	M_A_DQ18	AJ30	DDR3_DQ18	
	M_A_DQ19	AK29	DDR3_DQ19	
	M_A_DQ20	AD28	DDR3_DQ20	
	M_A_DQ21	AD30	DDR3_DQ21	
	M_A_DQ22	AG30	DDR3_DQ22	
	M_A_DQ23	AJ29	DDR3_DQ23	
	M_A_DQ24	AE24	DDR3_DQ24	
	M_A_DQ25	AG24	DDR3_DQ25	
	M_A_DQ26	AD22	DDR3_DQ26	
	M_A_DQ27	AC21	DDR3_DQ27	
	M_A_DQ28	AG27	DDR3_DQ28	
	M_A_DQ29	AG25	DDR3_DQ29	
	M_A_DQ30	AG21	DDR3_DQ30	
	M_A_DQ31	AE21	DDR3_DQ31	
	M_A_DQ32	AD13	DDR3_DQ32	
	M_A_DQ33	AD11	DDR3_DQ33	
	M_A_DQ34	AC8	DDR3_DQ34	
	M_A_DQ35	AG7	DDR3_DQ35	
	M_A_DQ36	AG13	DDR3_DQ36	
	M_A_DQ37	AE13	DDR3_DQ37	
	M_A_DQ38	AD10	DDR3_DQ38	
	M_A_DQ39	AF8	DDR3_DQ39	
	M_A_DQ40	AH2	DDR3_DQ40	
	M_A_DQ41	AG3	DDR3_DQ41	
	M_A_DQ42	AD2	DDR3_DQ42	
	M_A_DQ43	AD3	DDR3_DQ43	
	M_A_DQ44	AH4	DDR3_DQ44	
	M_A_DQ45	AK3	DDR3_DQ45	
	M_A_DQ46	AE2	DDR3_DQ46	
	M_A_DQ47	AD4	DDR3_DQ47	
	M_A_DQ48	AD7	DDR3_DQ48	
	M_A_DQ49	AD6	DDR3_DQ49	
	M_A_DQ50	AA6	DDR3_DQ50	
	M_A_DQ51	AB5	DDR3_DQ51	
	M_A_DQ52	AE8	DDR3_DQ52	
	M_A_DQ53	AE5	DDR3_DQ53	
	M_A_DQ54	AB9	DDR3_DQ54	
	M_A_DQ55	AA8	DDR3_DQ55	
	M_A_DQ56	AB2	DDR3_DQ56	
	M_A_DQ57	AB4	DDR3_DQ57	
	M_A_DQ58	W4	DDR3_DQ58	
	M_A_DQ59	V3	DDR3_DQ59	
	M_A_DQ60	AC2	DDR3_DQ60	
	M_A_DQ61	AB3	DDR3_DQ61	
	M_A_DQ62	Y2	DDR3_DQ62	
	M_A_DQ63	W1	DDR3_DQ63	
M_A_DQS[7:0] [4]	M_A_DQS0	AA30	DDR3_DQS0	
	M_A_DQS1	AB24	DDR3_DQS1	
	M_A_DQS2	AF30	DDR3_DQS2	
	M_A_DQS3	AE22	DDR3_DQS3	
	M_A_DQS4	AG10	DDR3_DQS4	
	M_A_DQS5	AF4	DDR3_DQS5	
	M_A_DQS6	AB6	DDR3_DQS6	
	M_A_DQS7	Y3	DDR3_DQS7	
M_A_DQS#[7:0] [4]	M_A_DQS#0	AA31	DDR3_DQS#0	
	M_A_DQS#1	AB25	DDR3_DQS#1	
	M_A_DQS#2	AE29	DDR3_DQS#2	
	M_A_DQS#3	AE22	DDR3_DQS#3	
	M_A_DQS#4	AE10	DDR3_DQS#4	
	M_A_DQS#5	AE3	DDR3_DQS#5	
	M_A_DQS#6	AB7	DDR3_DQS#6	
	M_A_DQS#7	AA2	DDR3_DQS#7	

DDR3

CDV_22MM_REV1P10

2 OF 6

DRAM Reset (CPU)

<20110520>Need to confirm with Intel if we need to add series 100ohm resistor

+1.5VSUS — R538 *1K/F_4

<20110607>Keep original design first for DRAMRST#

<20110707_Nick> Please un-stuff 1K pull up

[4] DDR3_DRAMRST# — R537 *0/short_4 — DDR3_DRAMRST#_NS — R539 *0/short_4 — DDR3_DRAMRST#_R

C159 0.1U/16V_4

<20110607>Keep original design first for DRAMRST#

<20110707_Nick> Please stuff 100K pull down

<20110727> Add C159 to suppress glitch

R474 100K/J_4

<20110727>Connect DDRAM_PWROK between CDV and RT8207L to meet JEDEC timing spec

+1.5VSUS

VCCDDRAON_1.5 — R100 10K/J_4

[27,32] DDRAM_PWROK — R97 *0/J_4 — C388 *1U/10V_6

<20110727> Reserve C388 for RC delay

Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	CedarView DDR	1B

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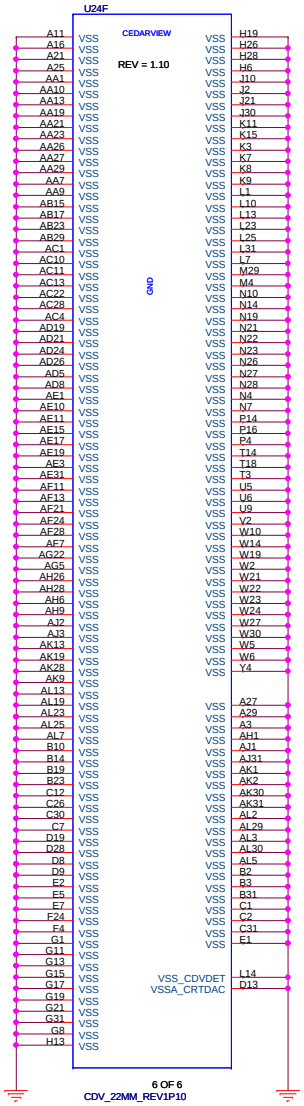
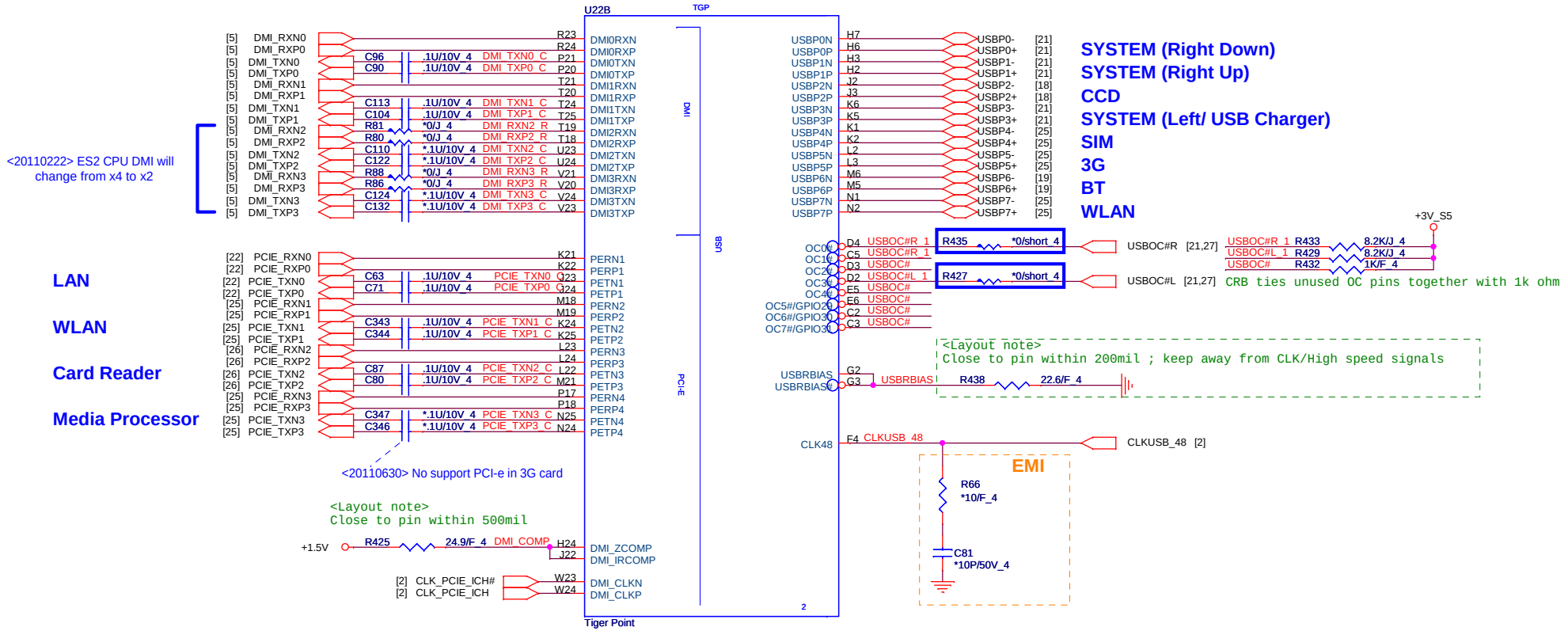
Cedar View (CPU)



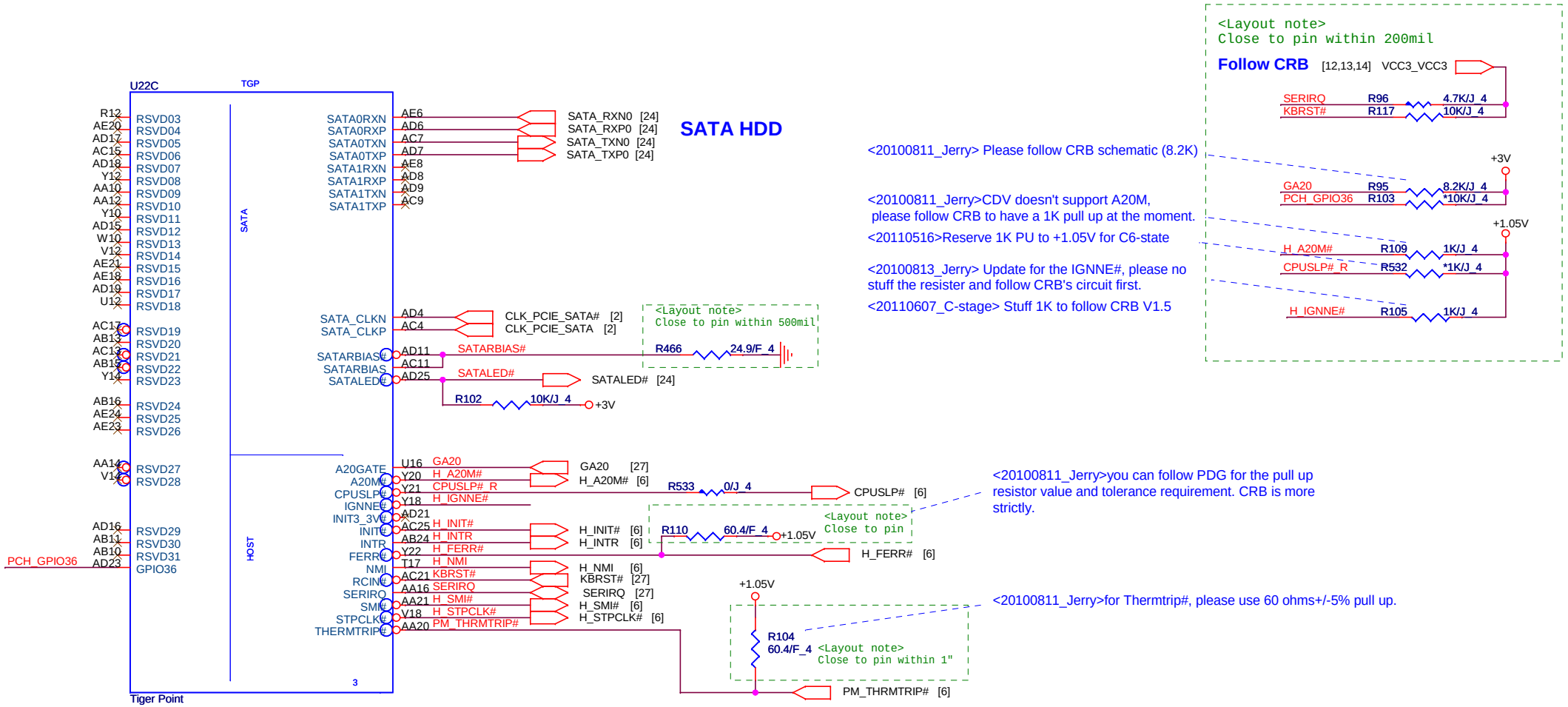
Quanta Computer Inc.	
PROJECT : ZE7	
Size	Document Number: CedarView GND/ Deep Standby — Rev: 1B
Date: Wednesday, November 02, 2011	Sheet 9 of 40

Tiger Point (CLG)



Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: Tiger Point DMI/PCIE/USB	Rev: 1B
Date: Wednesday, November 02, 2011	Sheet 10 of 40	

Tiger Point (CLG)



<20100811_Jerry> Please follow CRB schematic (8.2K)

<20100811_Jerry>CDV doesn't support A20M, please follow CRB to have a 1K pull up at the moment.

<20110516>Reserve 1K PU to +1.05V for C6-state

<20100813_Jerry> Update for the IGNNE#, please no stuff the resister and follow CRB's circuit first.

<20110607_C-stage> Stuff 1K to follow CRB V1.5

<20100811_Jerry>you can follow PDG for the pull up resistor value and tolerance requirement. CRB is more strictly.

<20100811_Jerry>for Thermtrip#, please use 60 ohms+/-5% pull up.

Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: Tiger Point Sata/Host	Rev: 1B
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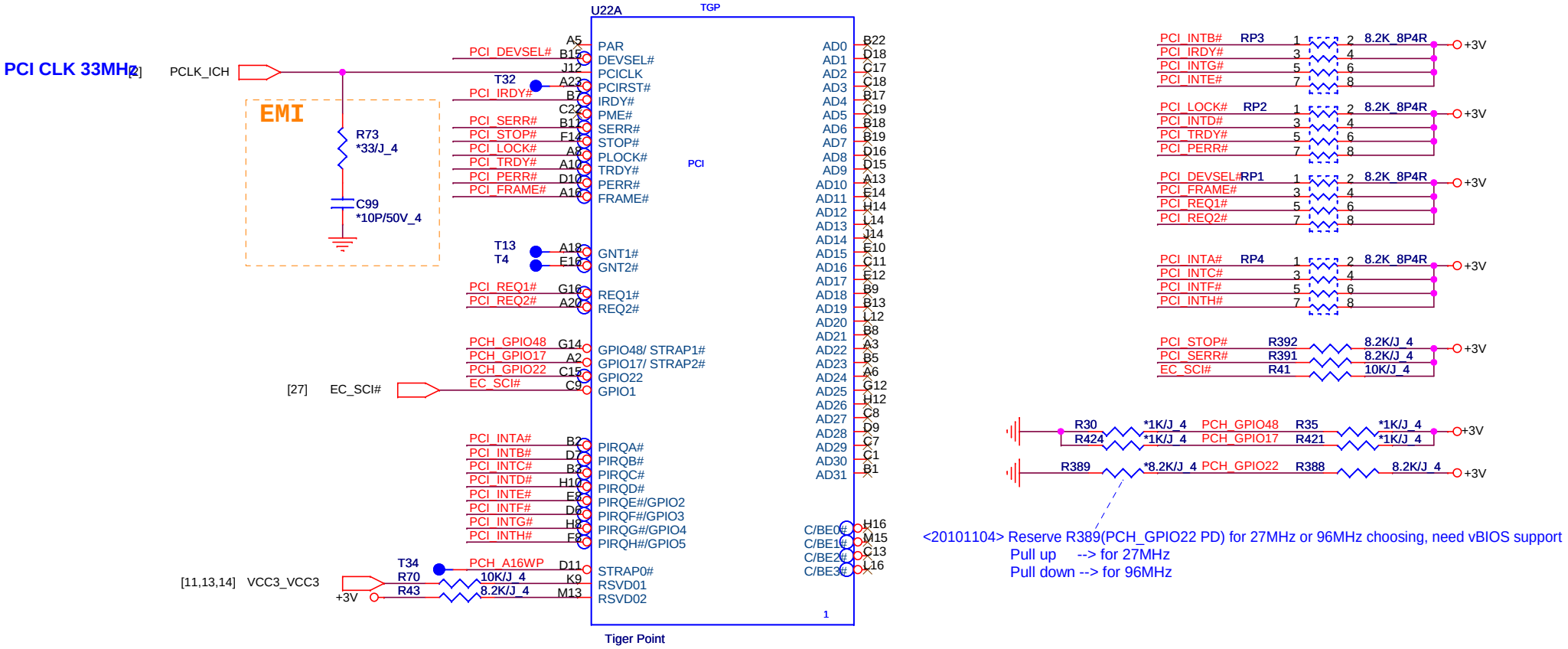
Tiger Point (CLG)



<20101104> Reserve R389(PCH_GPIO22 PD) for 27MHz or 96MHz choosing, need vBIOS support
Pull up --> for 27MHz
Pull down --> for 96MHz

<20090601(A1A)_Checklist Rev0.7>
Strap1#/strap2#: signals have weak internal pull-ups

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	***1***	***LPC (CURRENTLY USE)***

A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default

PCI_GNT#2	Internal PU Should not be PD

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	TigerPoint PCI	1B
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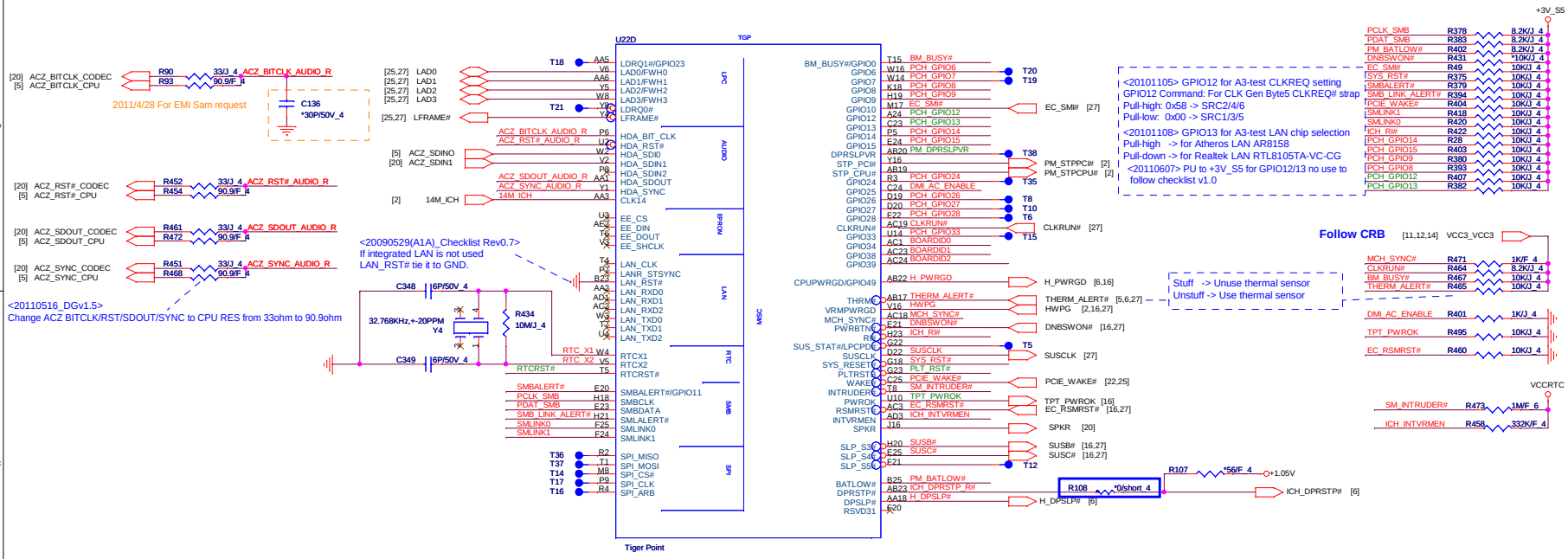
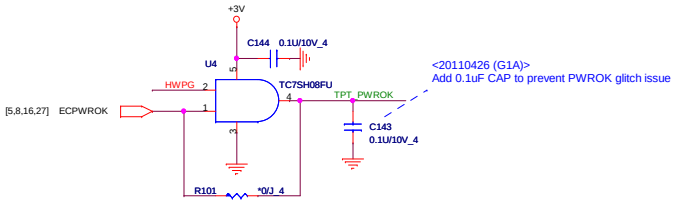
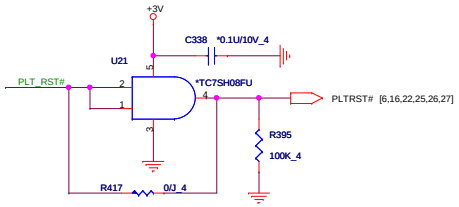
Tiger Point (CLG)



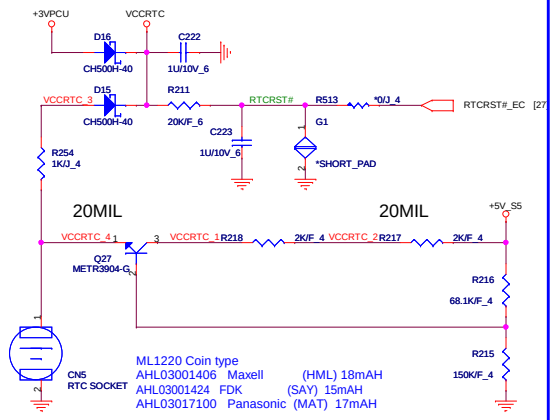
TPT Power OK (CLG)



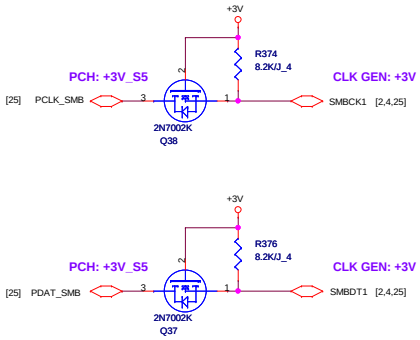
Platform Reset (CLG)



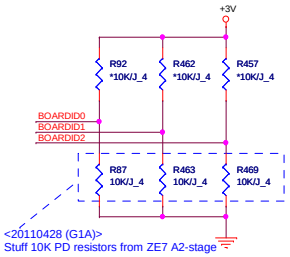
RTC (RTC)



Clock GEN I2C Level Shift



Mother Board ID (CLG)



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	TPT ACZ/GPIO/RTC	1B

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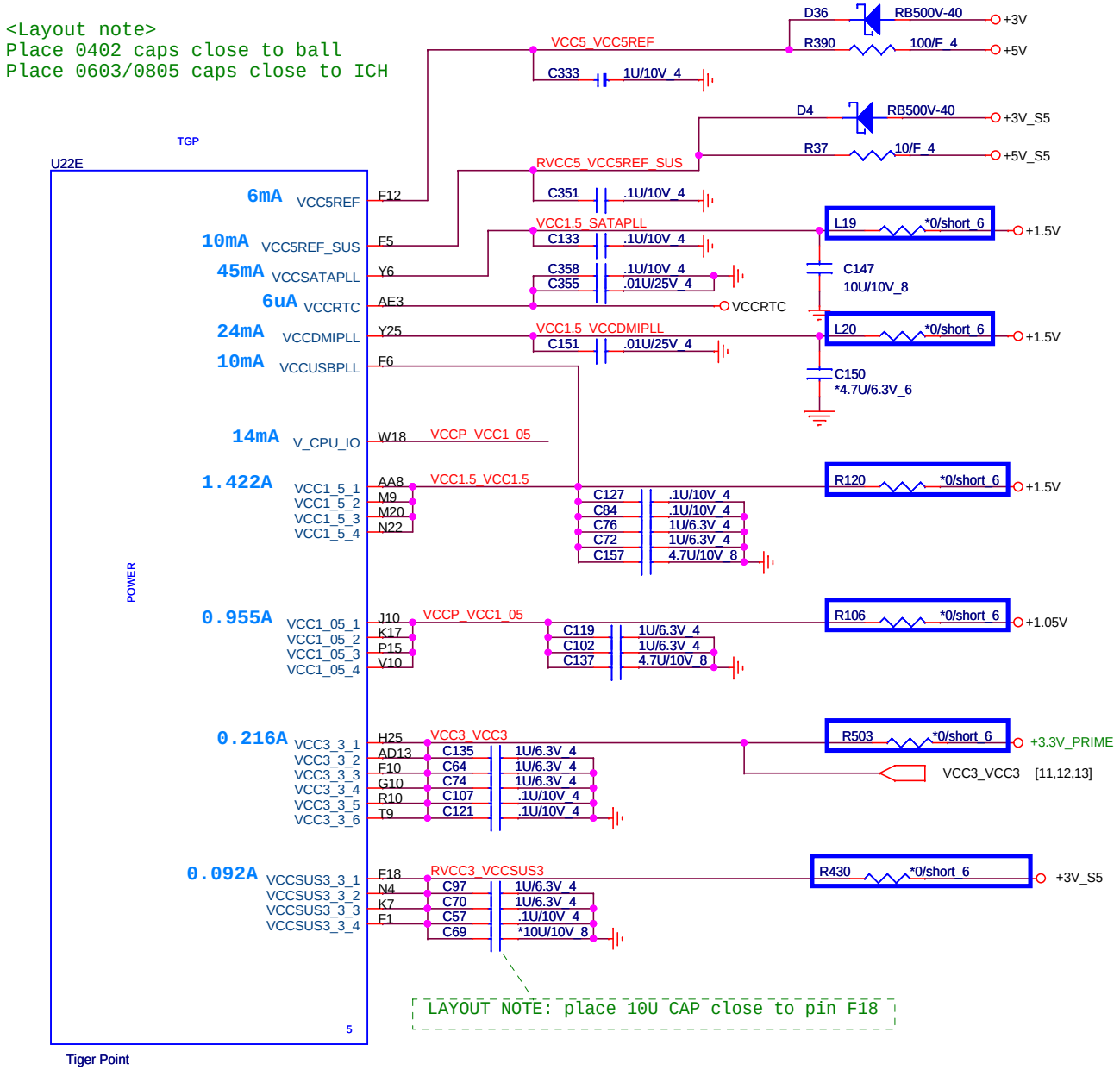
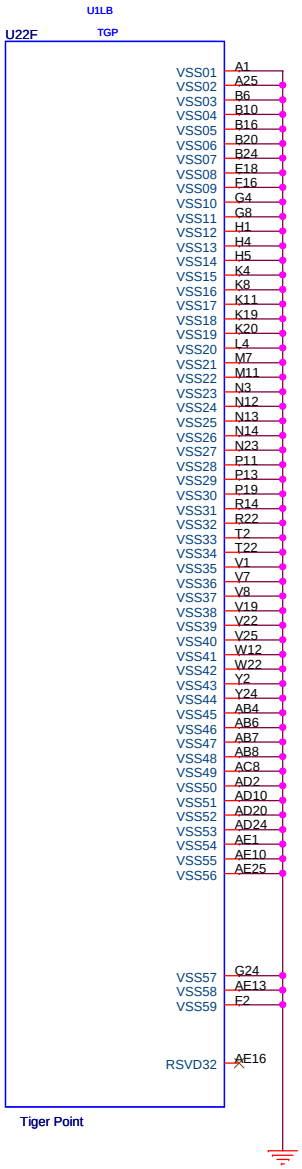
Tiger Point (CLG)



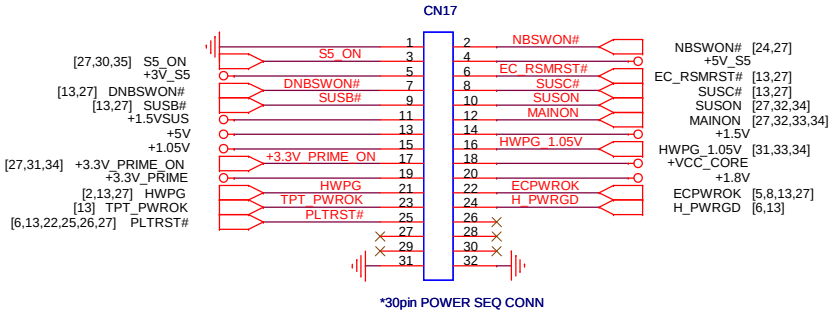
Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: TigerPoint Power	Rev: 1B
Date: Wednesday, November 02, 2011	Sheet 14 of 40	

Tiger Point (CLG)



Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: TigerPoint GND	Rev: 1B
Date: Wednesday, November 02, 2011	Sheet 15 of 40	

Power Sequence Connector 30pin (CPU)



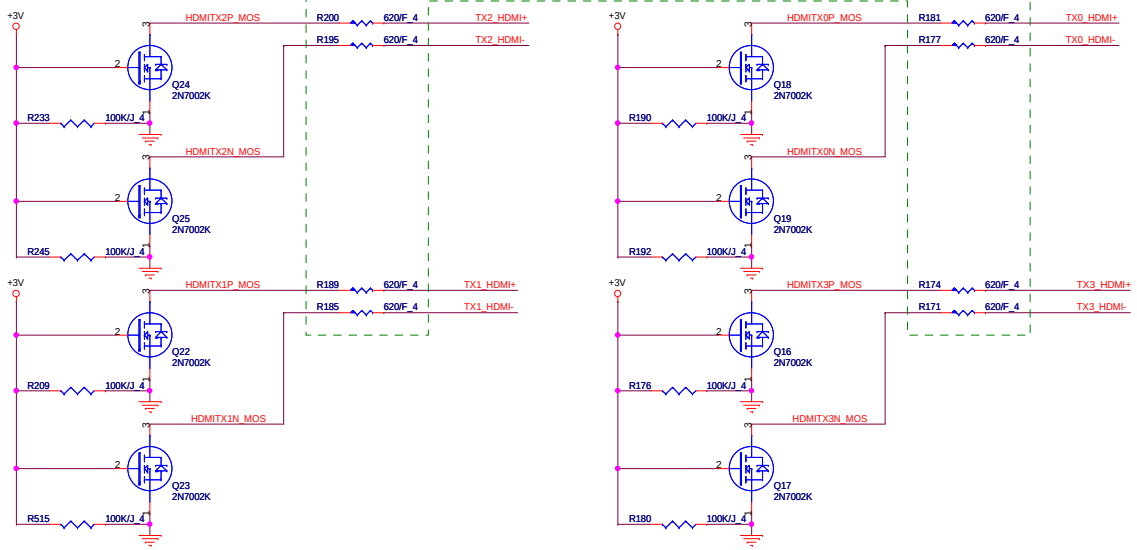
*30pin POWER SEQ CONN

1	GND	11	+1.5VSUS	21	HWPG
2	NBSWON#	12	MAINON	22	ECPWROK
3	S5_ON	13	+5V	23	TPT_PWROK
4	+5V_S5	14	+1.5V	24	H_PWRGD
5	+3V_S5	15	+1.05V	25	PLTRST#
6	RSMRST#	16	HWPG_1.05V	26	RESERVE
7	DNBSWON#	17	VRON	27	RESERVE
8	SUSC#	18	+VCC_CORE	28	RESERVE
9	SUSB#	19	+3.3V_PRIME	29	RESERVE
10	SUSON	20	+1.8V	30	RESERVE

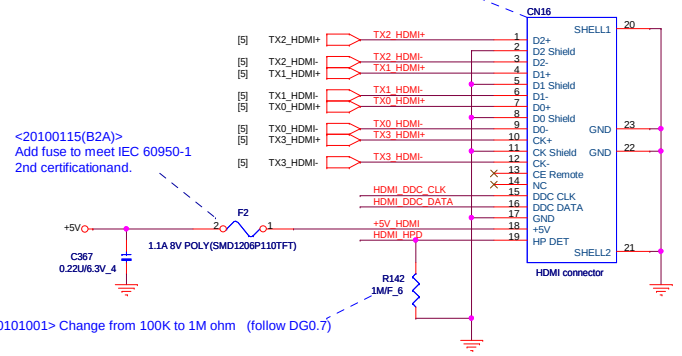
HDMI (HDM)

Level Shifter motherboard topology for max data rate of 1.65Gb/s

Close to HDMI connector

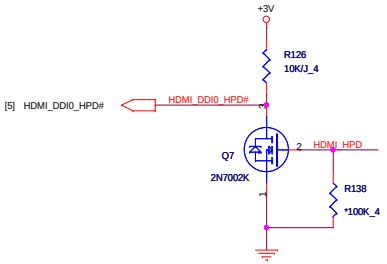


<20101209> Change to DFHS19FR015 by ME design change



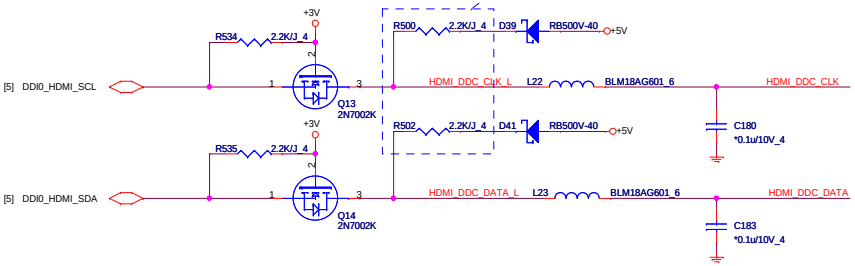
<20100115(B2A)>
Add fuse to meet IEC 60950-1
2nd certificationand.

<20101001> Change from 100K to 1M ohm (follow DG0.7)



SDVO I2C Control (HDM)

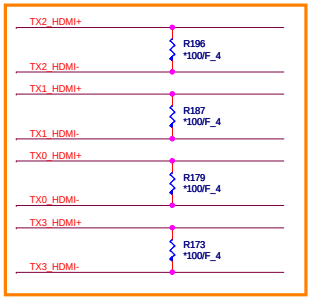
<20100909_Jennifer> Change R500/ R502 from 1.5k to 2.2k to follow CRB.



The DDC signals are rated at 5V at connector. The passgate can also be used to protect against back-power
when computer is OFF but the display is ON and still pulled up to 5 V.

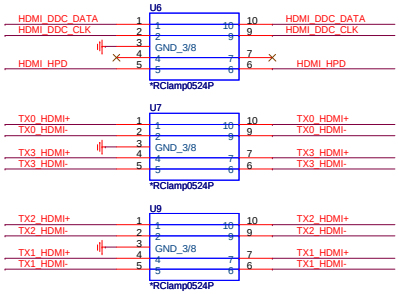
EMI reserve for HDMI (EMC)

Close to HDMI Connector



ESD Protect (HDM)

Close to HDMI Connector



Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	HDMI	1B
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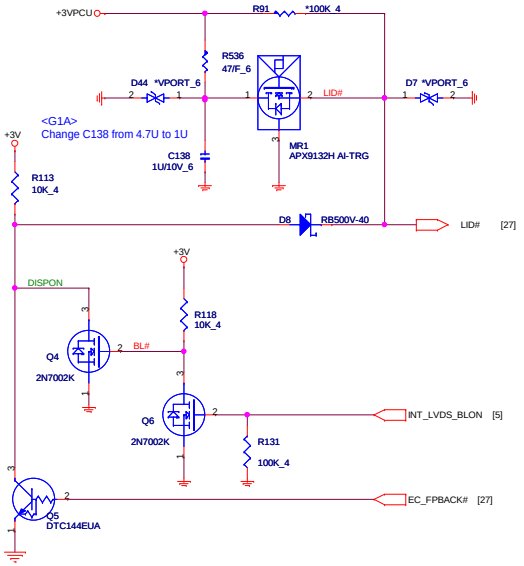
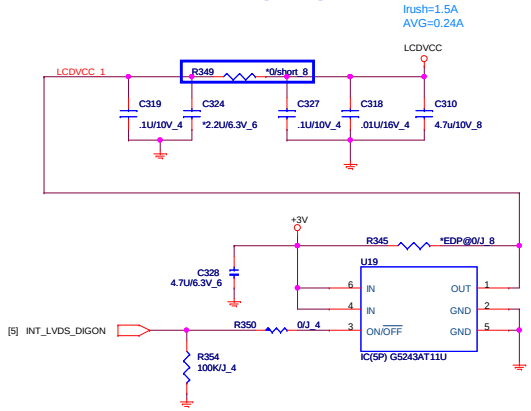
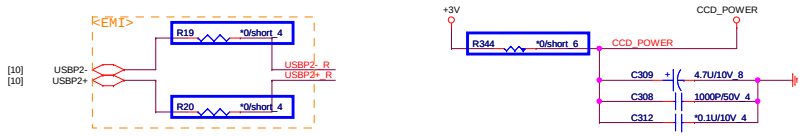
HALL IC (HSR)



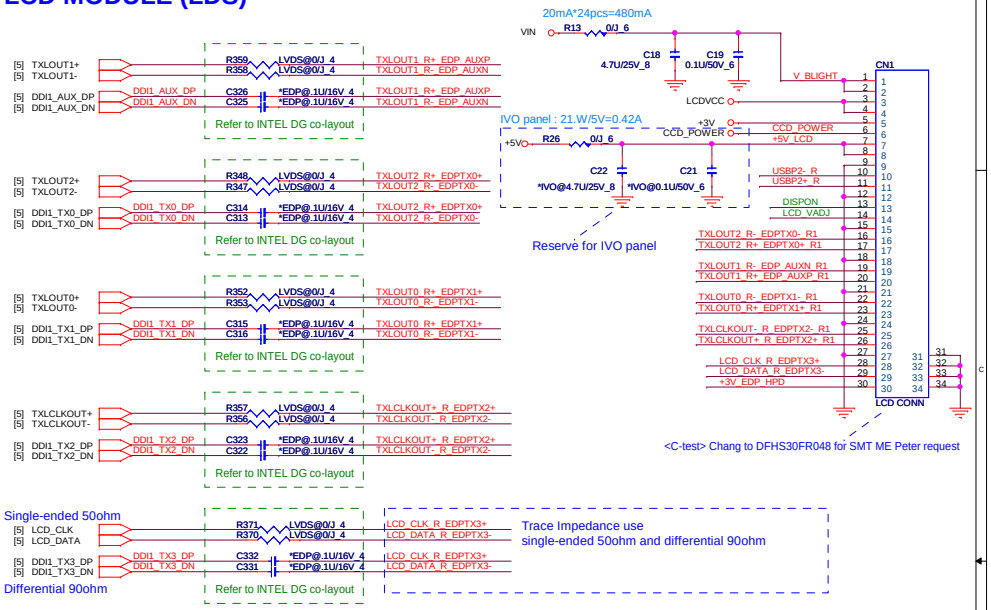
LCD POWER SWITCH (LDS)



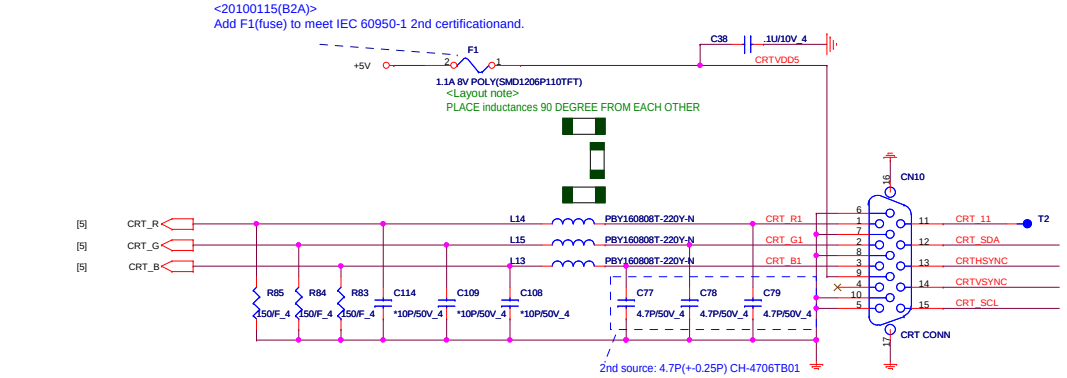
CAMERA POWER (CCD)

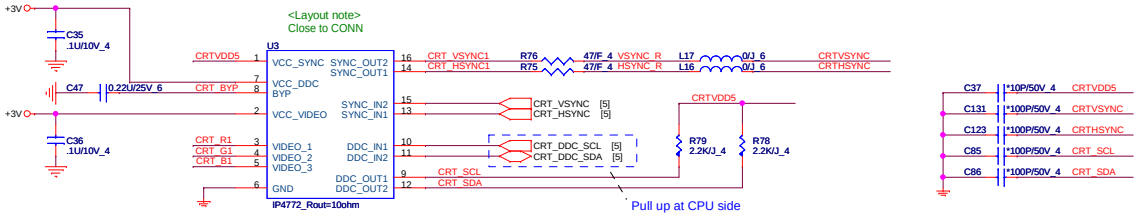


LCD MODULE (LDS)

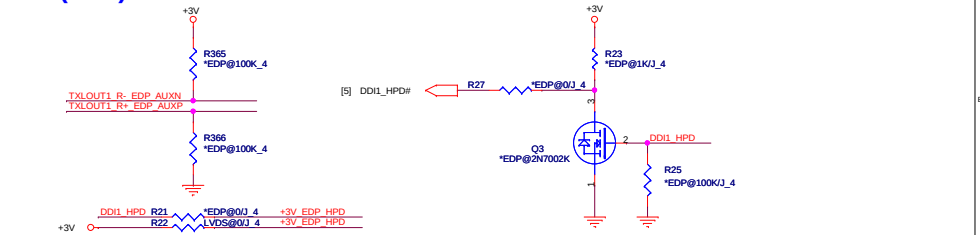


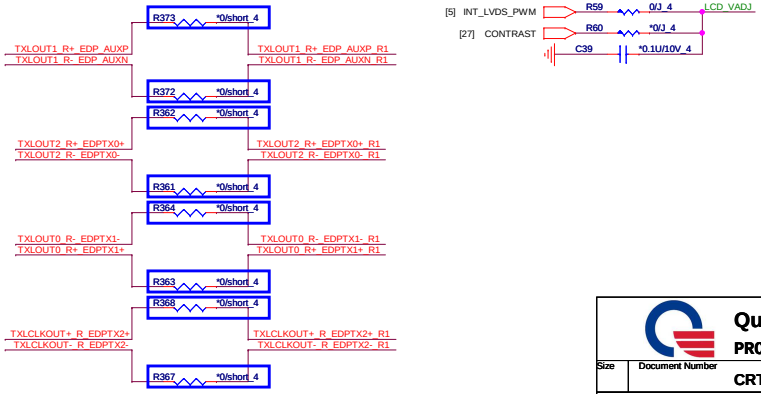
CRT(CRT)





eDP (LDS)





Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	CRT/LVDS/EDP	1B

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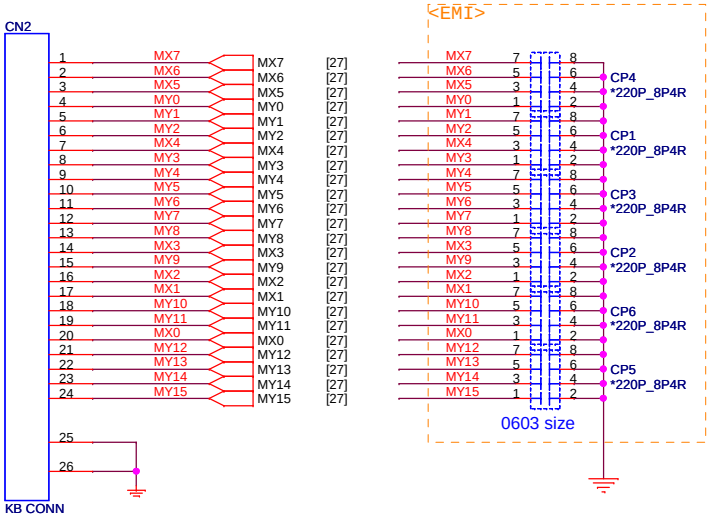
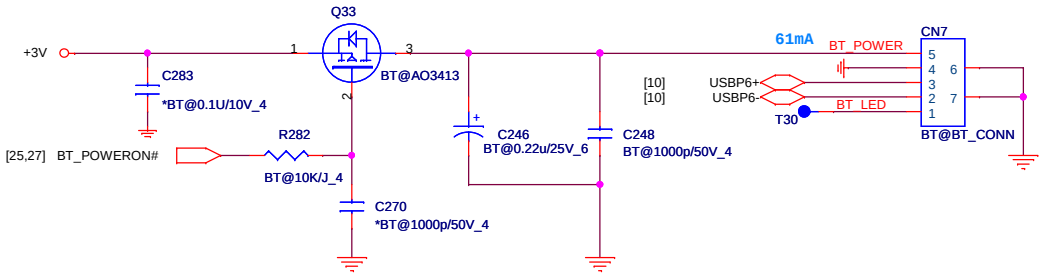
KEYBOARD (KBC)

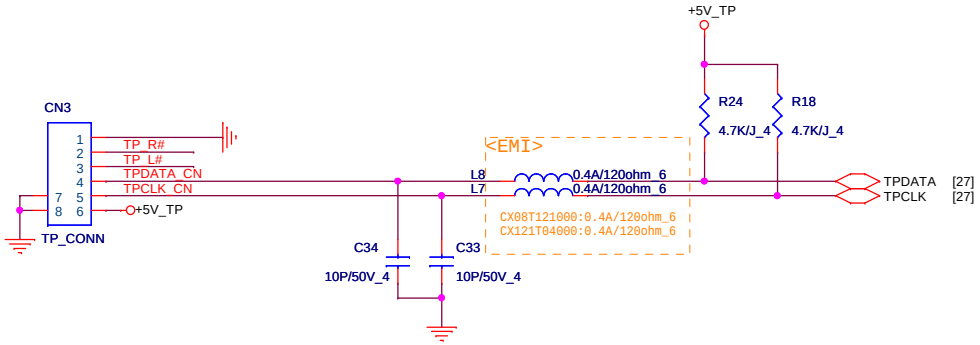
<20110214(E1A)>
Change CP1~CP6 footprint from
8p4r-0402-smt to 8P4R, for SMT open issue.



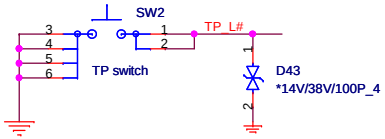
BLUETOOTH (BTM)

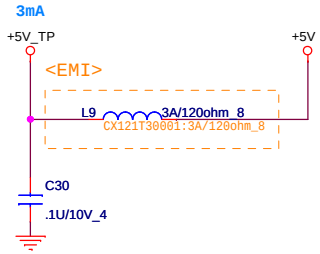


TOUCH PAD (TPD)

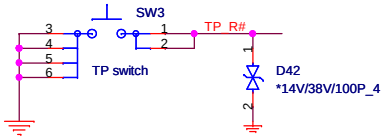


Left Button





Right Button



Quanta Computer Inc. PROJECT : ZE7		
Size	Document Number: KB/BT/TP/LED/Power Connector	Rev: 1B
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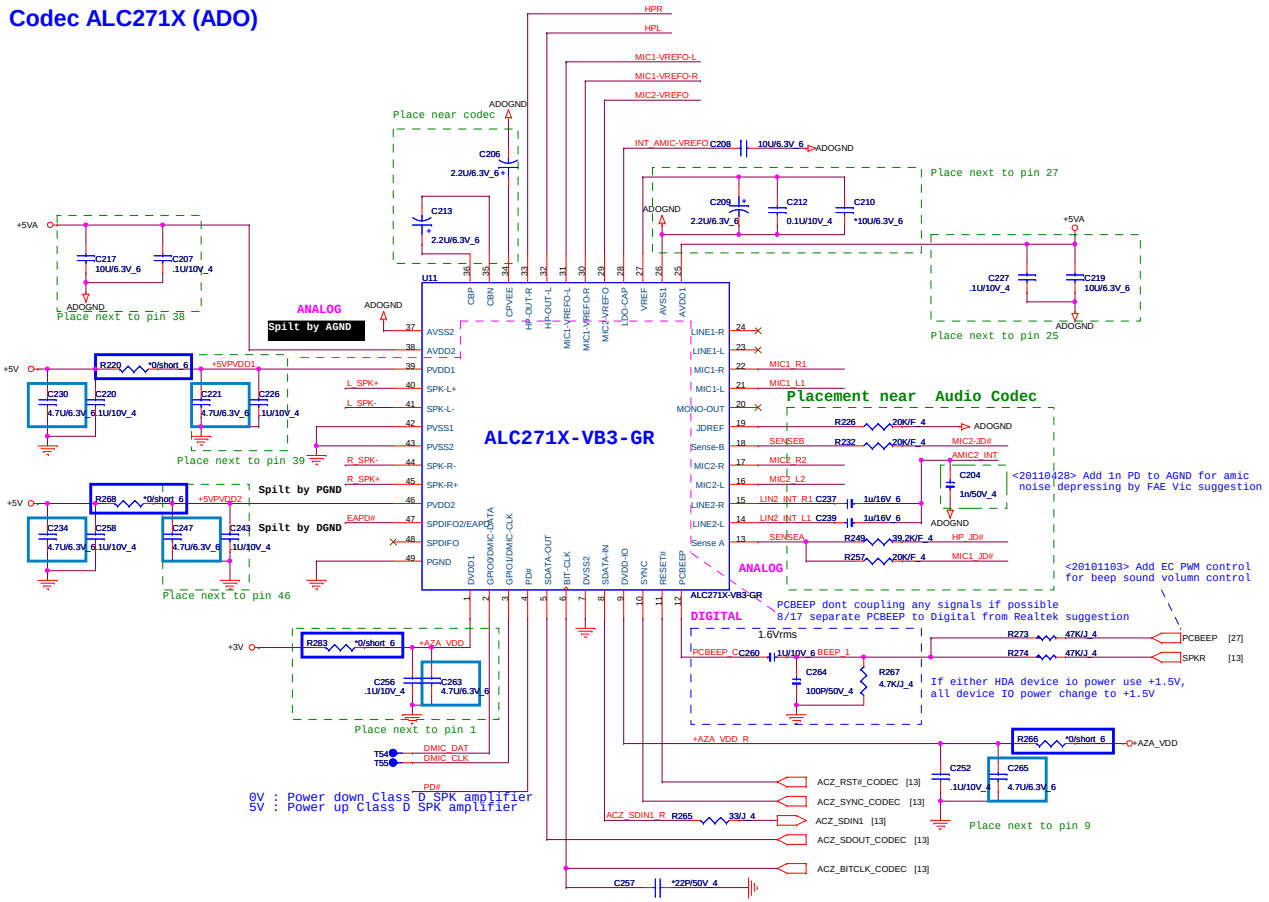
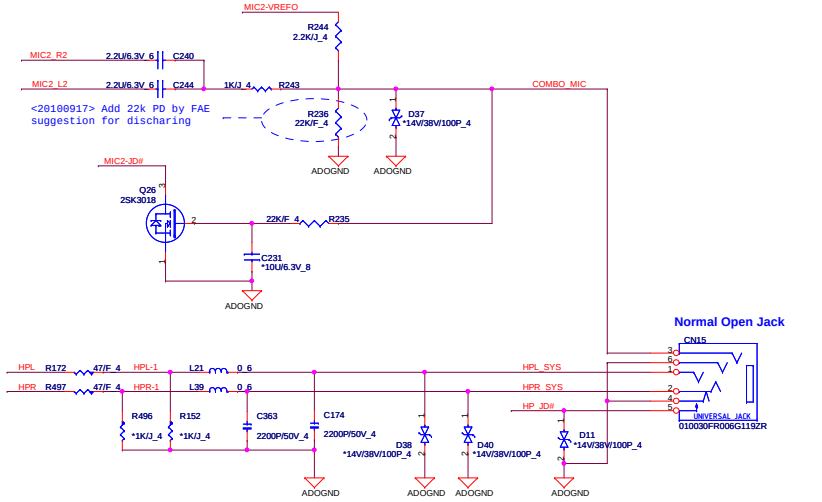
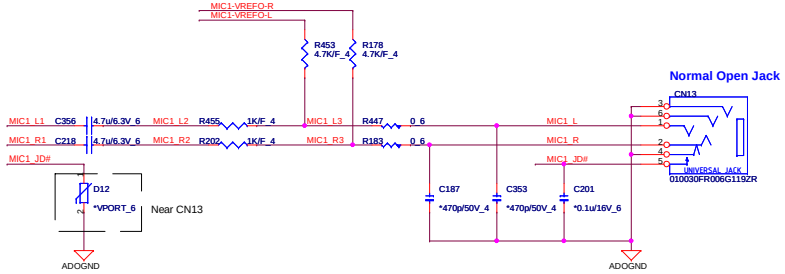
Codec ALC271X (ADO)



EARPHONE (AMP)

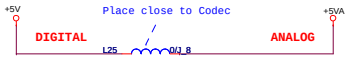


MIC (AMP)

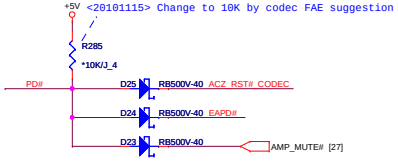


Power (ADO)

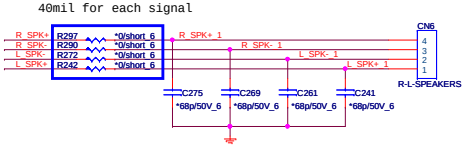
Demodulation Filter



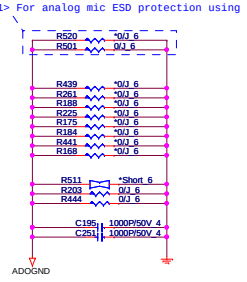
Mute (ADO)



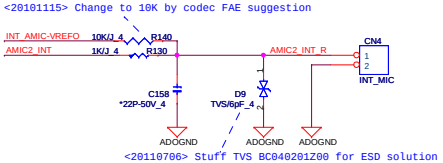
Internal Speaker (AMP)



GND



Internal Analog MIC (AMP)

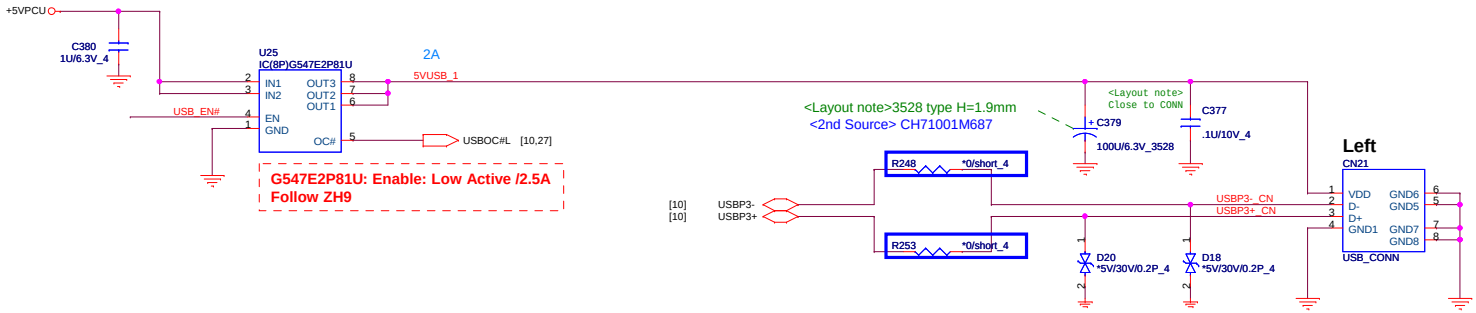


Quanta Computer Inc.
PROJECT : ZE7

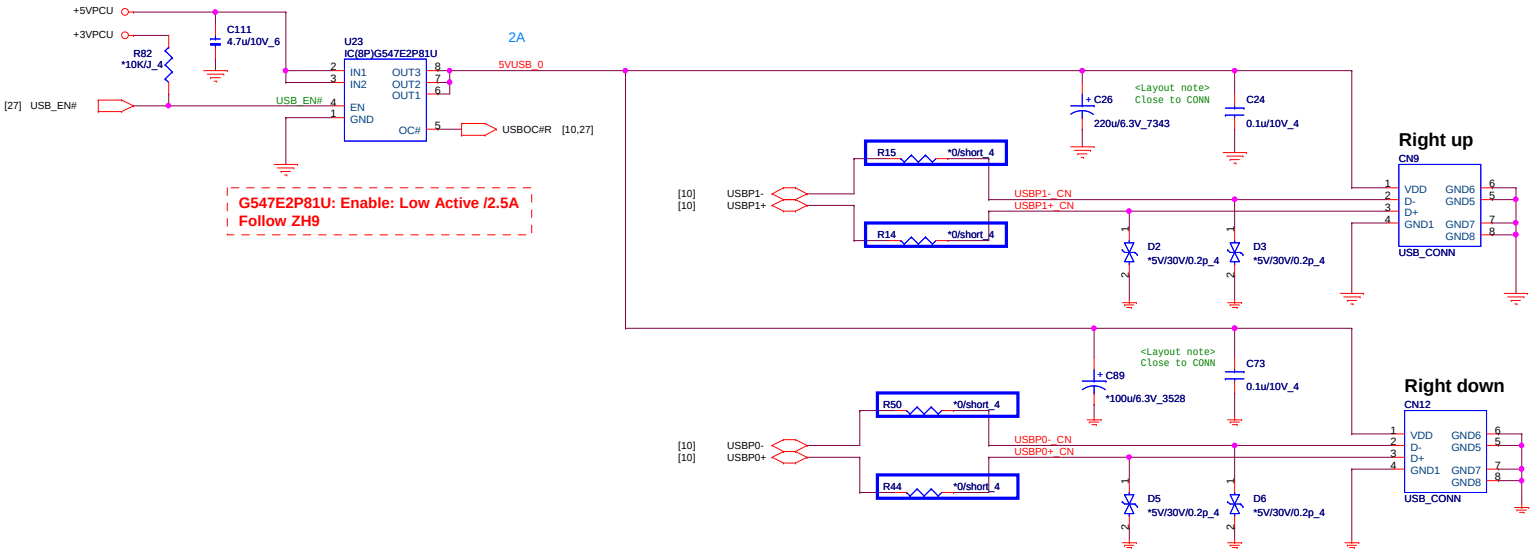
Size	Document Number	Rev
	ALC271X / AMP / SPK	1B

Date: Wednesday, November 02, 2011 Sheet 20 of 40

USB Left (USB)

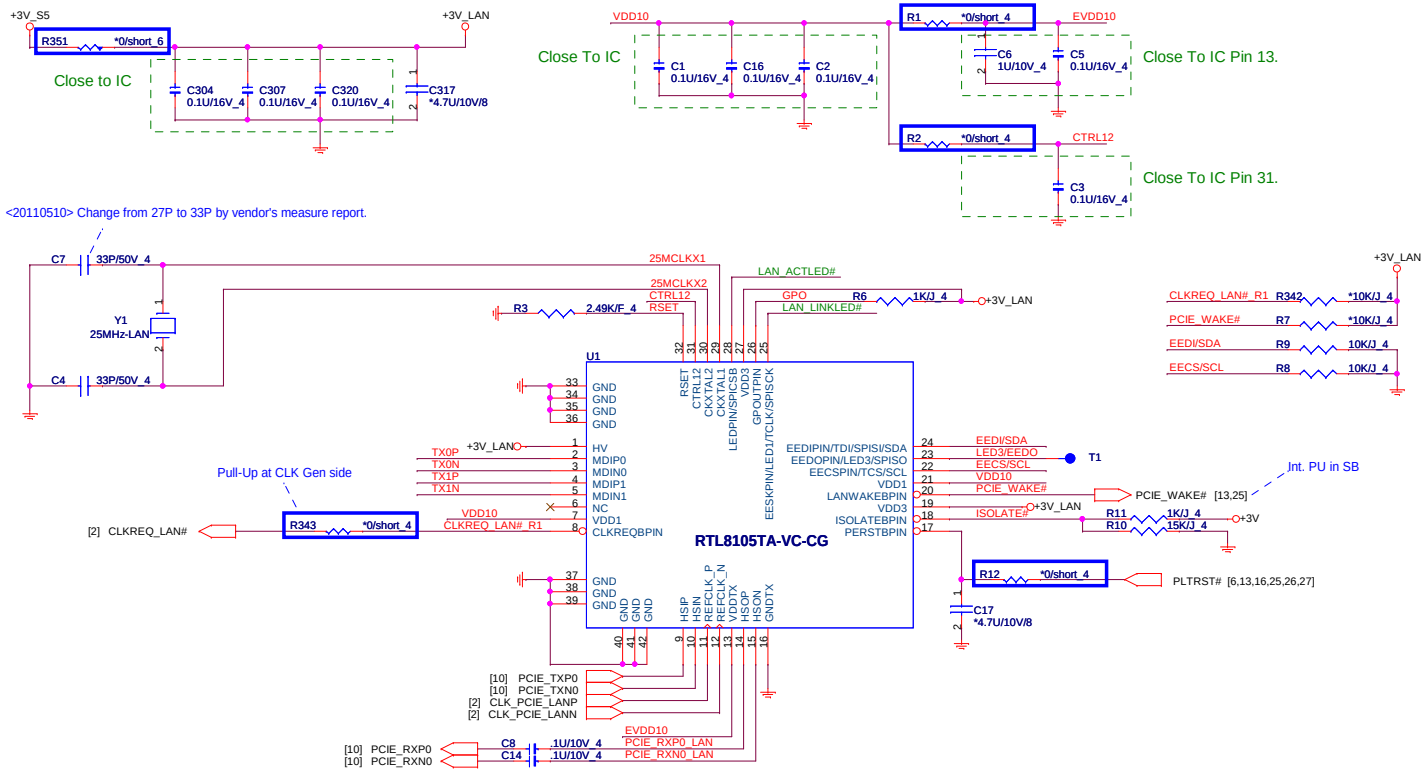


USB Right (USB)

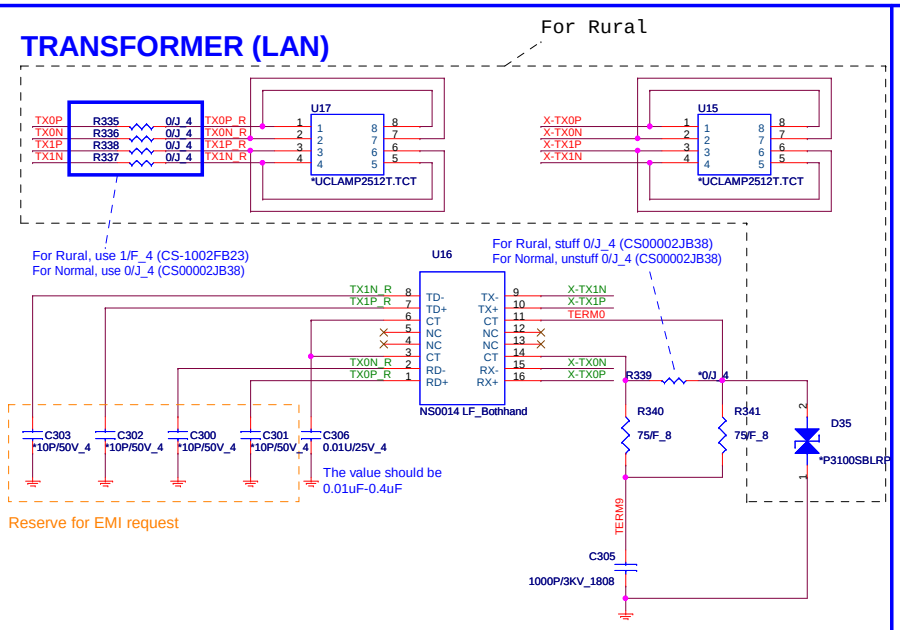


Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: USB Port	Rev: D3E
Date: Wednesday, November 02, 2011	Sheet 21 of 43	

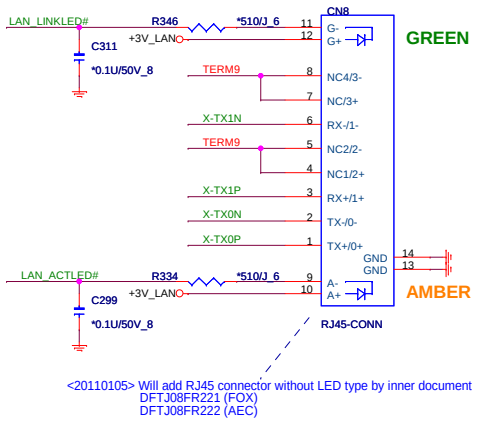
LAN (LAN)



TRANSFORMER (LAN)



RJ45 Connector (LAN)



<20110105> Will add RJ45 connector without LED type by inner document
DFTJ08FR221 (FOX)
DFTJ08FR222 (AEC)

Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	LAN RTL8105TA-VC-CG	1B

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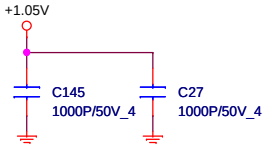
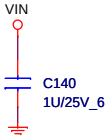
Stitching Capacitor (CLG)

For RF Request



For CRT R/G/B Signals



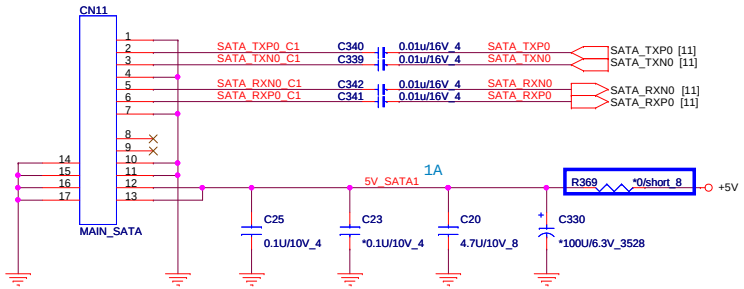
Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	Stitching Cap	1B

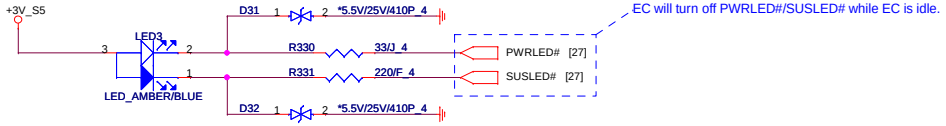
Date: Wednesday, November 02, 2011 Sheet 23 of 40

2.5" SATA HDD (HDD)

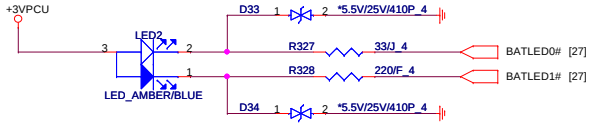


LED/SW (UIF)

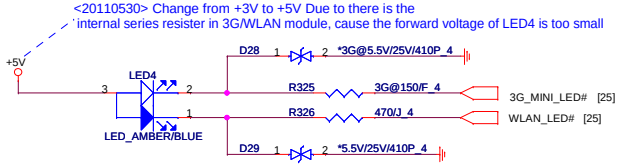
PWR LED
SUS LED



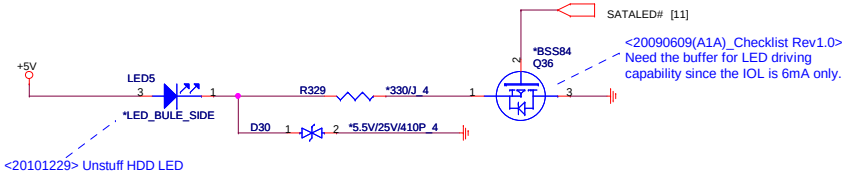
FULL LED
CHG LED



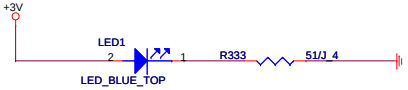
3G LED
WLAN LED



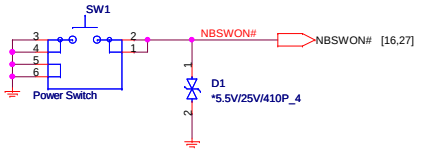
HDD LED



PWR indicator



PWR button



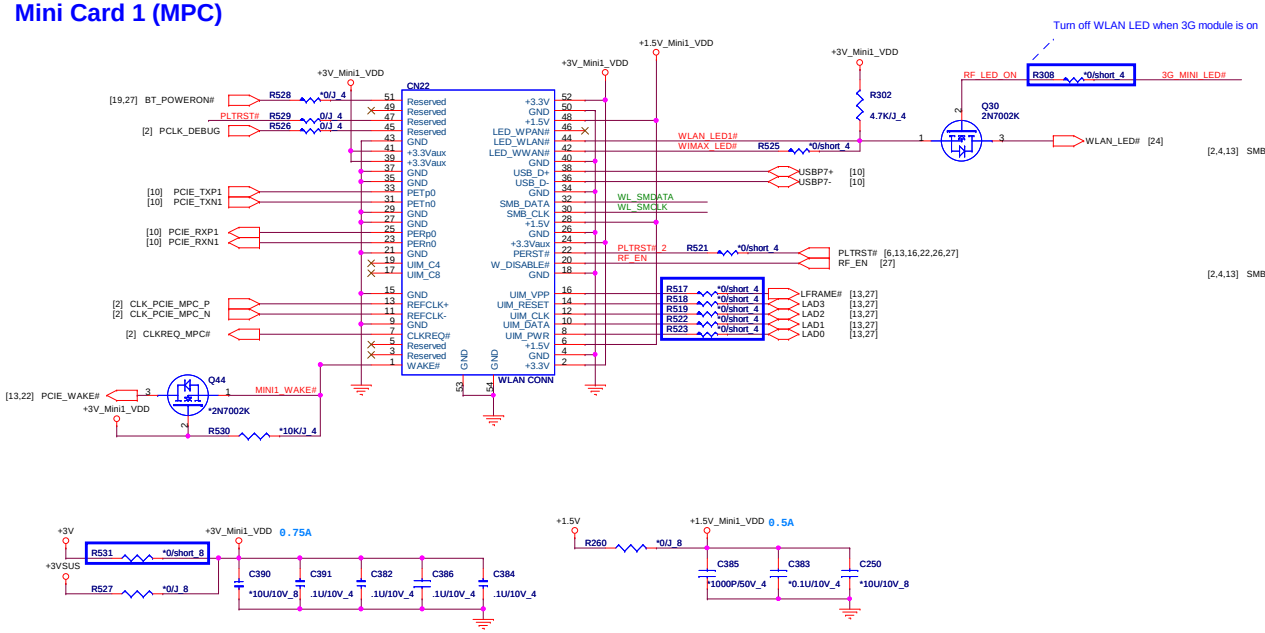
Quanta Computer Inc.

PROJECT : ZE7

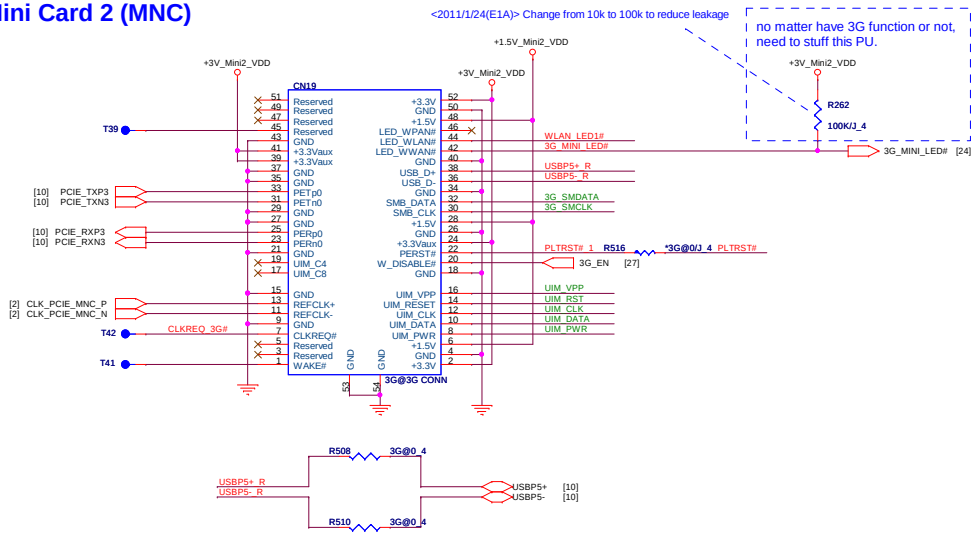
Size	Document Number	Rev
	SATA HDD/LED/SW	1B

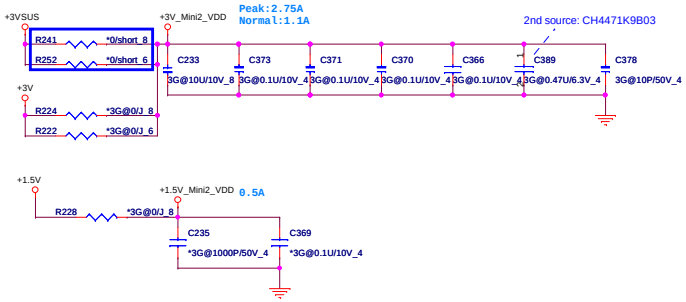
Date: Wednesday, November 02, 2011 Sheet 24 of 40

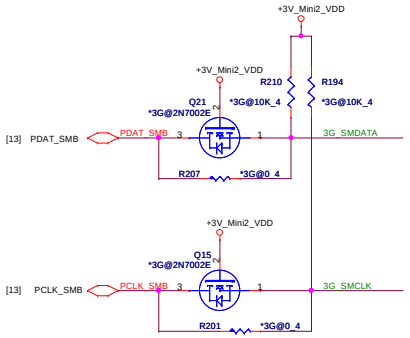
Mini Card 1 (MPC)



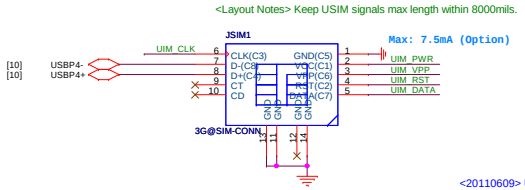
Mini Card 2 (MNC)

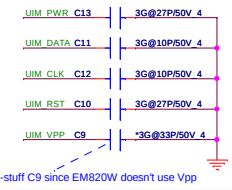


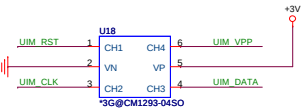


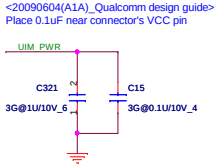


MultiMedia SIM (MNC)







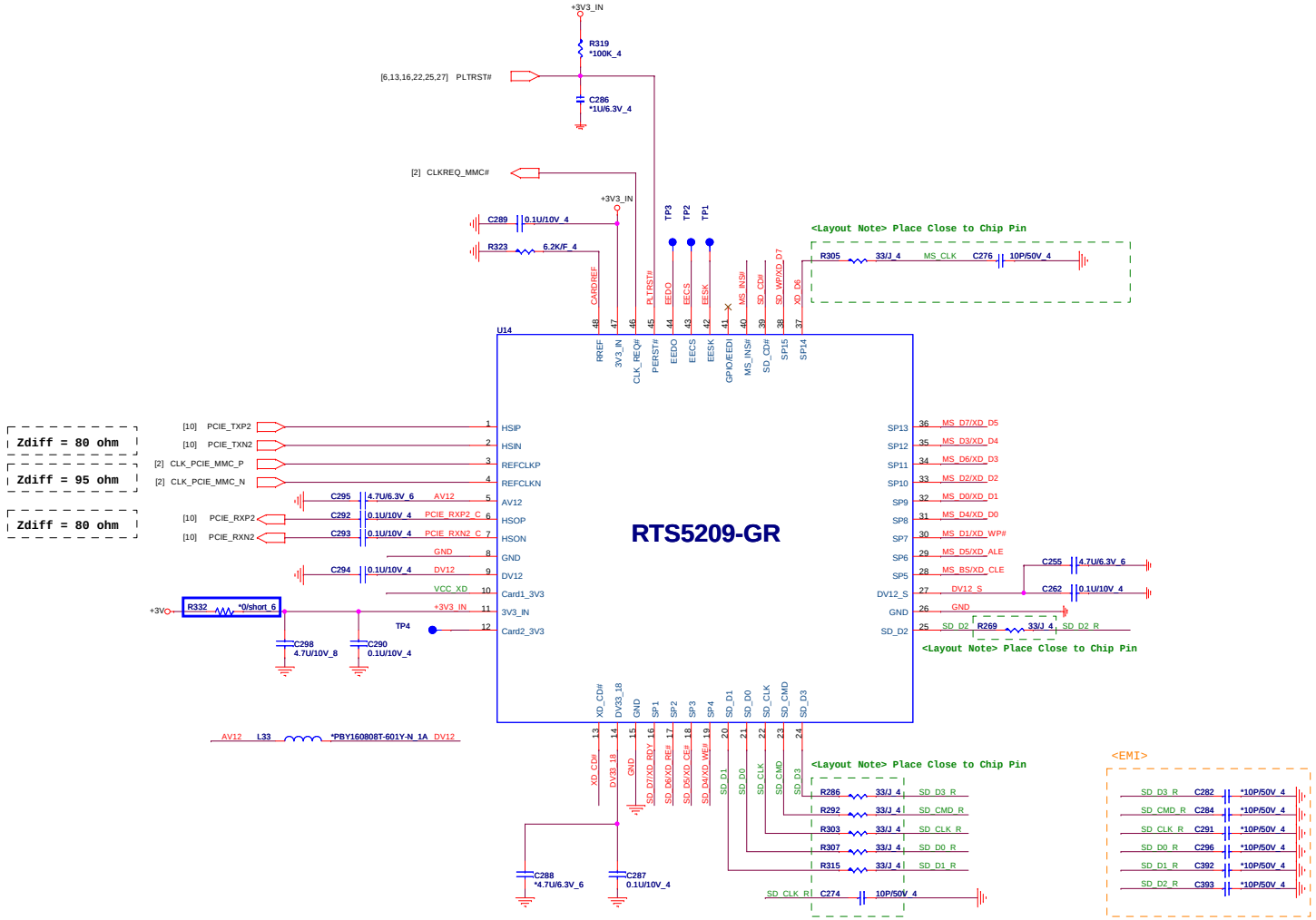


Quanta Computer Inc.
PROJECT : ZE7

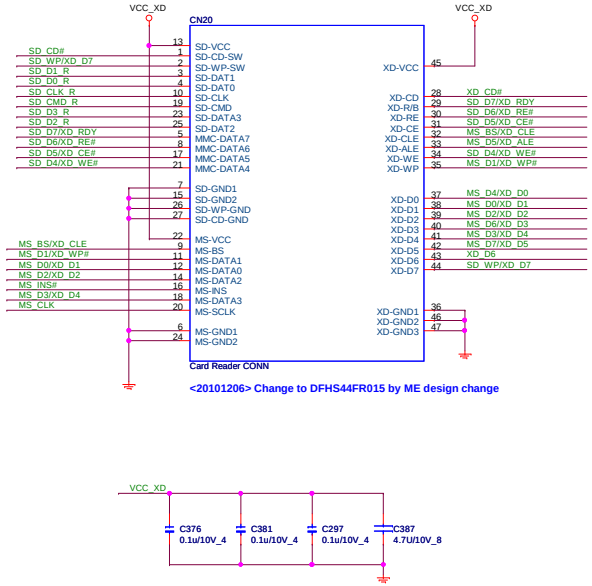
Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1B

Date: Wednesday, November 02, 2011 Sheet 25 of 40

Card reader controller (MMC)

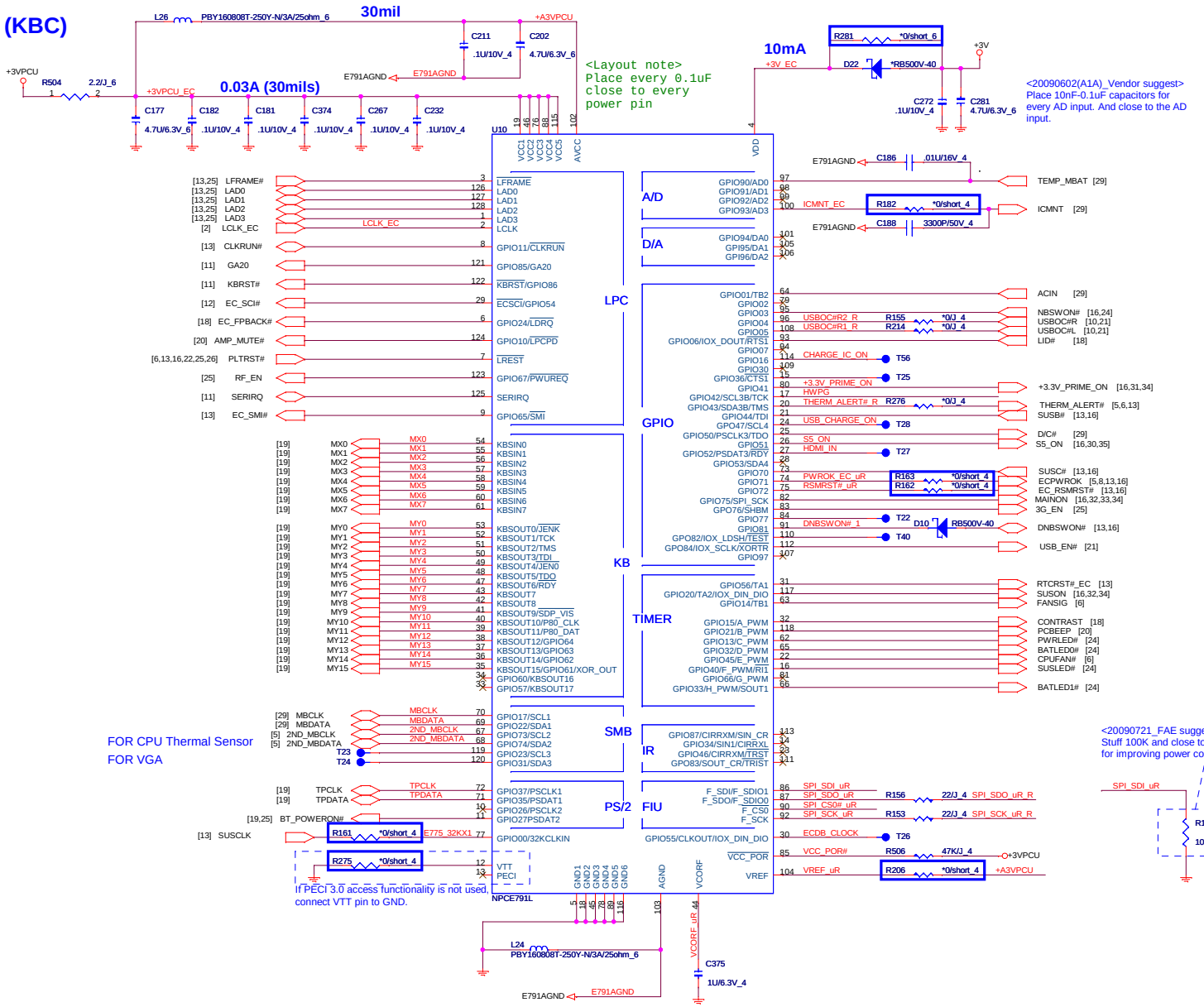


5 IN 1 Card Reader CONN (MMC)



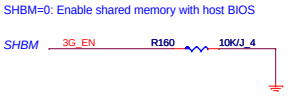
Quanta Computer Inc.			
PROJECT : ZE7			
Size	Document Number		Rev
	RTS5209-GR (Card Reader)		1B
Date: Wednesday, November 02, 2011	Sheet 26 of 40		

EC (KBC)



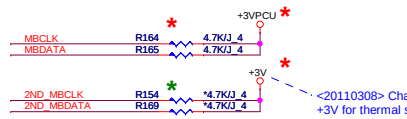
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS



1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

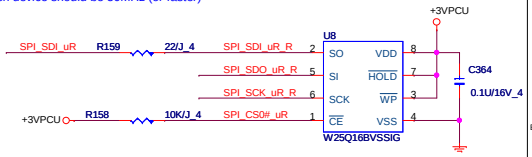


1ST: Battery
2ND: CPU Thermal Sensor / DTS
3RD: VGA Thermal Sensor

<20090831(A1A)_EC team suggest>
1.change R166/R167 to 1M or 100K ohm
2.change PWR/SUS LED's power from +3VPCU to +3V_S5 or +3VSUS
can reduce pull-high resistor of SUSLED#/PWRLED#

SPI FLASH(KBC)

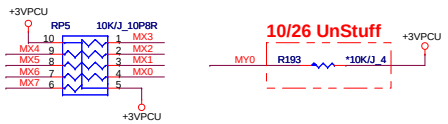
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)



ZS9 A1~A3-test	W25Q16BVSSIG	AKE38FP0N01	16M bit
ZS9 A4-test	W25Q16CVSSIG	AKE38ZP0N02	16M bit
ZS9 A5-test	MX25L1606EM2I-12G	AKE38FP0Z01	16M bit
ZS9 A6-test	MX25L1606EM2I-12G	AKE38FP0Z01	16M bit
ZS9 A7-test	W25Q16BVSSIG	AKE38FP0N01	16M bit

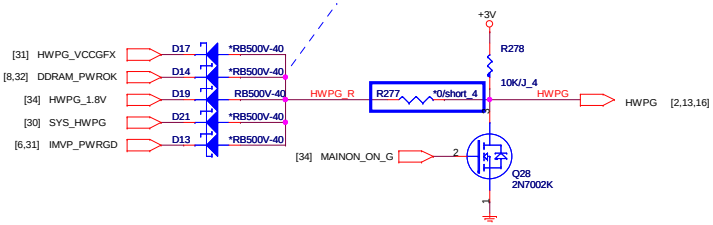
Winbond W25Q16BVSSIG AKE38FP0N01
EON EN25F16-75HCP AKE38ZA0Q00
MXIC MX25L1606EM2I-12G AKE38FP0Z01 (ZE6 MAC ID fail)

INTERNAL KEYBOARD STRIP SET (KBC)



HWPG (KBC)

<20110829> DDRAM_PWROK no need connecting to EC side



<EMI>

Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	NPCE791L & FLASH	1B

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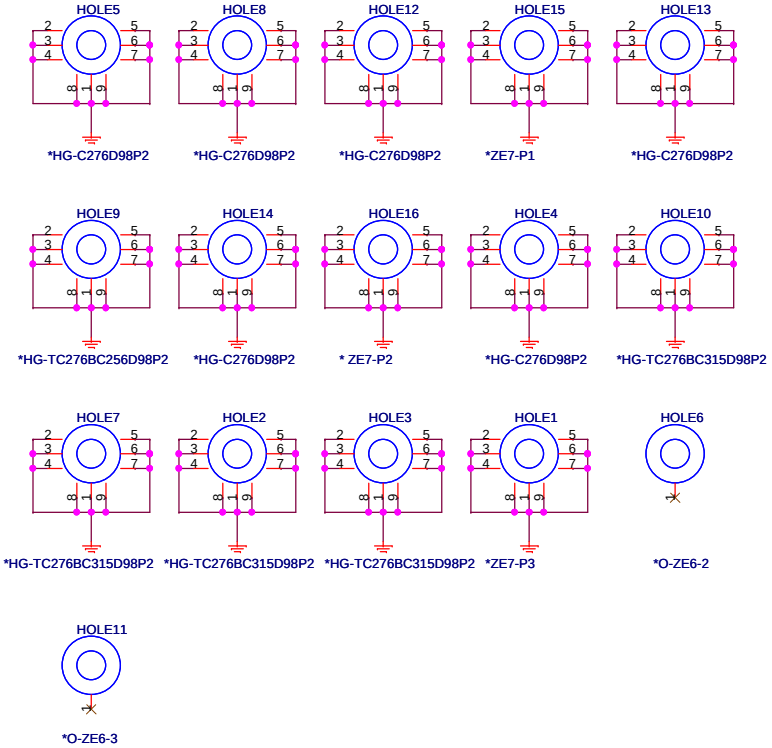
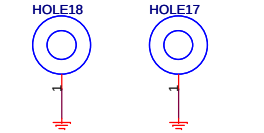
HOLE (OTH)

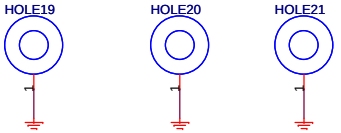
TOP(HDD Hole)



BOT(Thermal Hole)



BOT(Mini-PCIe Hole)



LED ESD PAD

TP ESD PAD

Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: EMI/Hole	Rev: 1B
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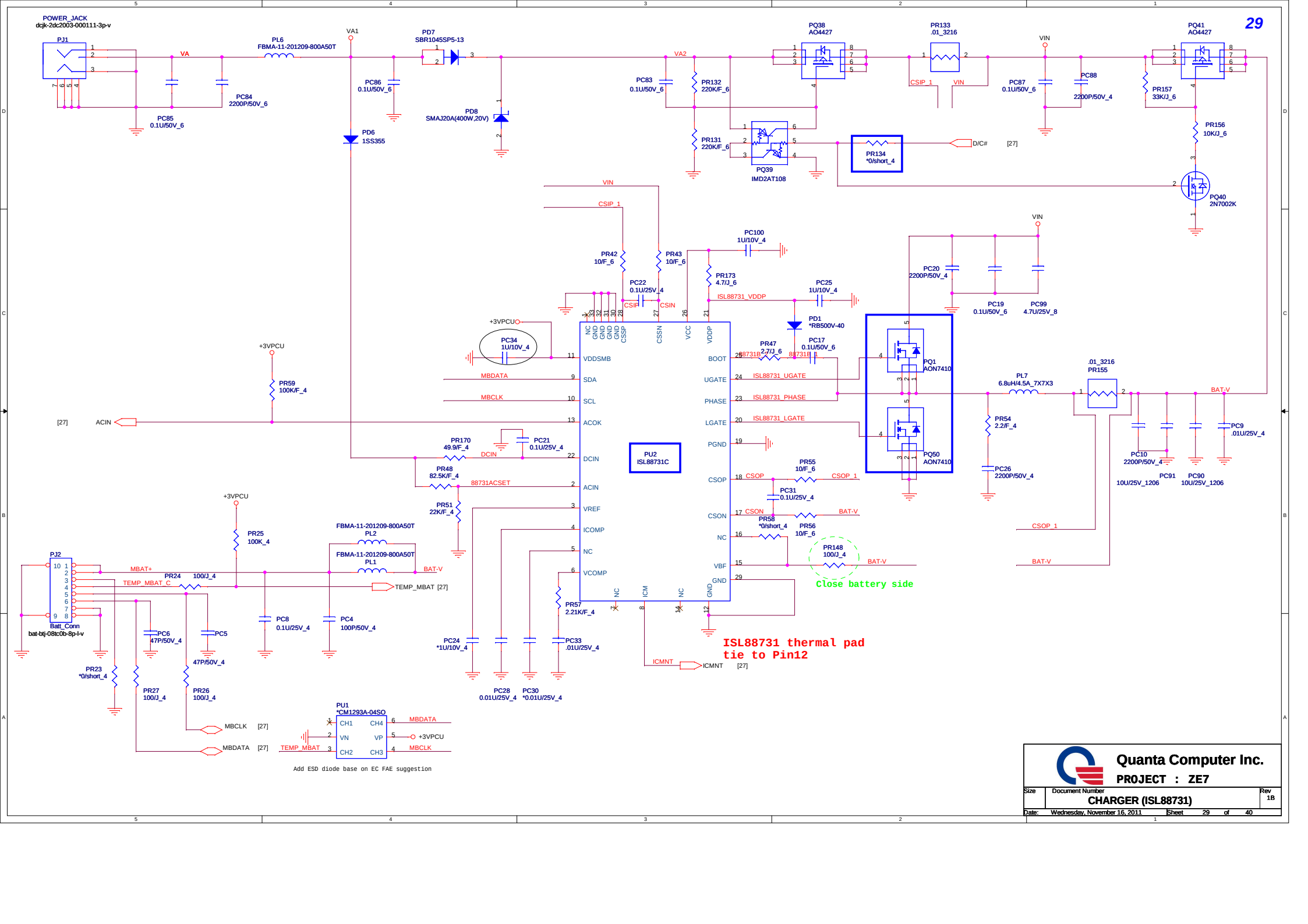
29
POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ1
VA
PL6
FBMA-11-201209-800A50T
VA1
PD7
SBR1045SP5-13
PC84
2200P/50V_6
PC85
0.1U/50V_6
PC86
0.1U/50V_6
PD6
1SS355
PD8
SMAJ20A(400W,20V)
VA2
PQ38
AO4427
PR133
.01_3216
VIN
PQ41
AO4427
PC83
0.1U/50V_6
PR132
220K/F_6
PR131
220K/F_6
PQ39
IMD2AT108
CSIP_1
PC87
0.1U/50V_6
PC88
2200P/50V_4
PR157
33K/J_6
PR156
10K/J_6
PR134
*0/short_4
D/C#
[27]
PQ40
2N7002K
PC100
1U/10V_4
PR42
10/F_6
PR43
10/F_6
PR173
4.7/J_6
PC22
0.1U/25V_4
CSIP
CSIN
ISL88731_VDDP
PC25
1U/10V_4
PD1
*RB500V-40
PC20
2200P/50V_4
PC19
0.1U/50V_6
PC99
4.7U/25V_8
+3VPCU
PC34
1U/10V_4
PR59
100K/F_4
[27]
ACIN
MBDATA
MBCLK
PR170
49.9/F_4
PC21
0.1U/25V_4
DCIN
PR48
82.5K/F_4
88731ACSET
PR51
22K/F_4
PU2
ISL88731C
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
PR47
2.7/J_6
88731BOOT
88731BOOT_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PQ1
AON7410
PQ50
AON7410
PR55
10/F_6
CSOP
CSOP_1
PC31
0.1U/25_4
CSON
PR58
*0/short_4
PR56
10/F_6
BAT-V
PR148
100/J_4
Close battery side
PR57
2.21K/F_4
PC24
*1U/10V_4
PC28
0.01U/25V_4
PC30
*0.01U/25V_4
PC33
.01U/25V_4
ICMNT
ICMNT
[27]
ISL88731 thermal pad
tie to Pin12
PL7
6.8uH/4.5A_7X7X3
.01_3216
PR155
PR54
2.2/F_4
PC26
2200P/50V_4
PC10
2200P/50V_4
PC91
10U/25V_1206
PC90
10U/25V_1206
PC9
.01U/25V_4
BAT-V
CSOP_1
BAT-V
PJ2
Batt_Conn
bat-btj-08tc0b-8p-l-v
MBAT+
TEMP_MBAT_C
PR24
100/J_4
PR25
100K_4
FBMA-11-201209-800A50T
PL2
FBMA-11-201209-800A50T
PL1
BAT-V
TEMP_MBAT
[27]
PC6
47P/50V_4
PC5
47P/50V_4
PC8
0.1U/25V_4
PC4
100P/50V_4
PR23
*0/short_4
PR27
100/J_4
PR26
100/J_4
MBCLK
[27]
MBDATA
[27]
PU1
*CM1293A-04SO
CH1
VN
CH2
CH4
VP
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZE7
Size
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CHARGER (ISL88731)
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1B
Date:
Wednesday, November 16, 2011
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40

MAIND [32,34]
SUSD [34]
SYS_SHDN# [6,35]

[27] SYS_HWPG

+5VPCU
5 Volt +/- 5%
TDC : 4.858A
PEAK : 6.5A
OCP : 8A
Width : 200mil

+3VPCU
3 Volt +/- 5%
TDC : 2.368A
PEAK : 3.16A
OCP : 4A
Width : 100mil

PU3 RT8223M

OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
~94.32K

OCP:4A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=4-(1.9/2)=3.05A
Vth=3.05A*14mOhm=42.7mV
R(Ilim)=(42.7mV*10)/10uA
=42.7K

PQ32 DTC144EU
PQ33 2N7002K
PQ16 2N7002K
PQ34 2N7002K
PQ35 AO3404
PQ12 AO3404
PQ22 AO3404
PQ15 AO3404
PQ24 AO3404

TDC : 0.008A
PEAK : 0.01A
Width : 10mil

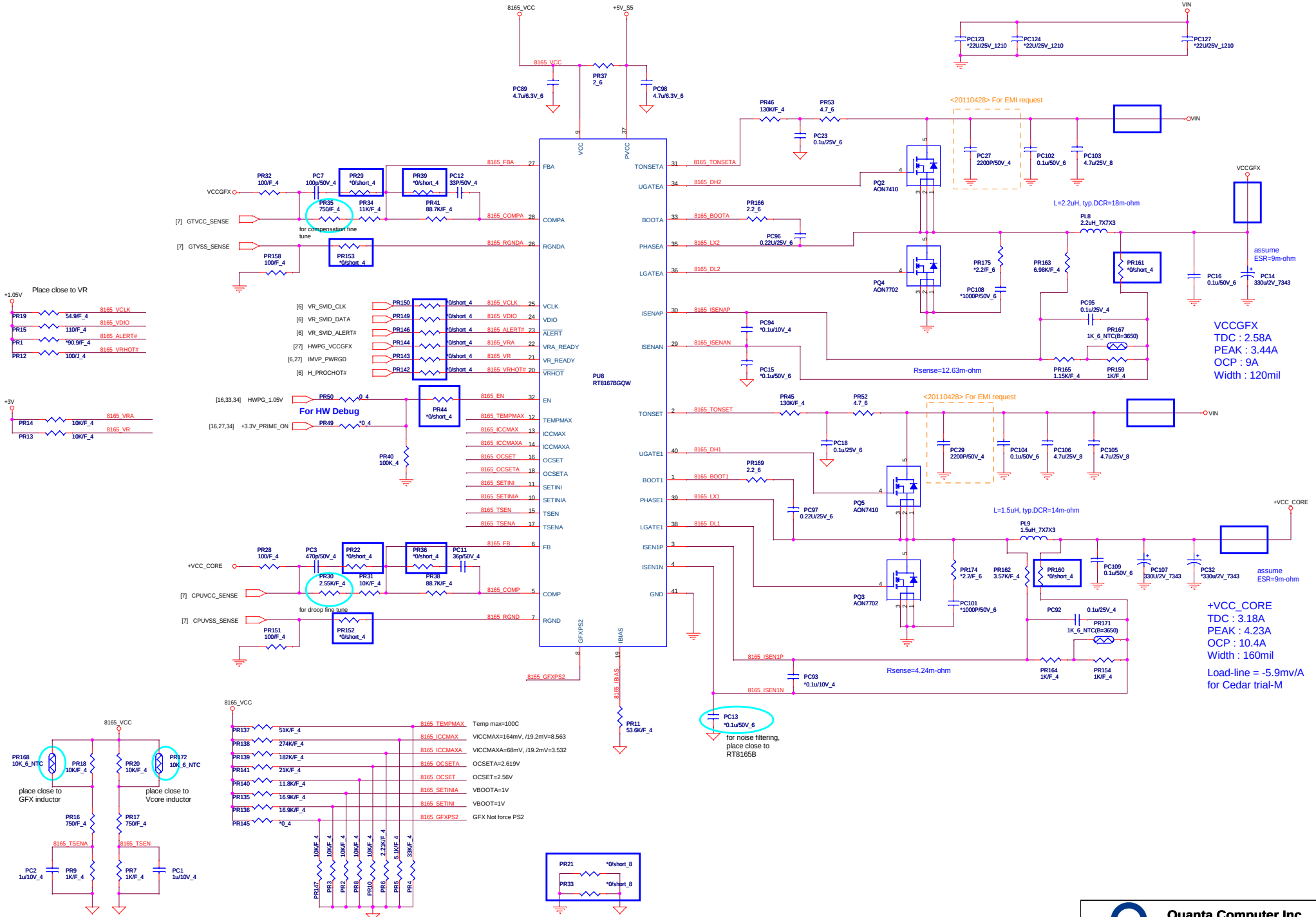
TDC : 1.858A
PEAK : 2.477A
Width : 80mil

TDC : 1.03A
PEAK : 1.38A
Width : 50mil

TDC : 0.15A
PEAK : 0.2A
Width : 10mil

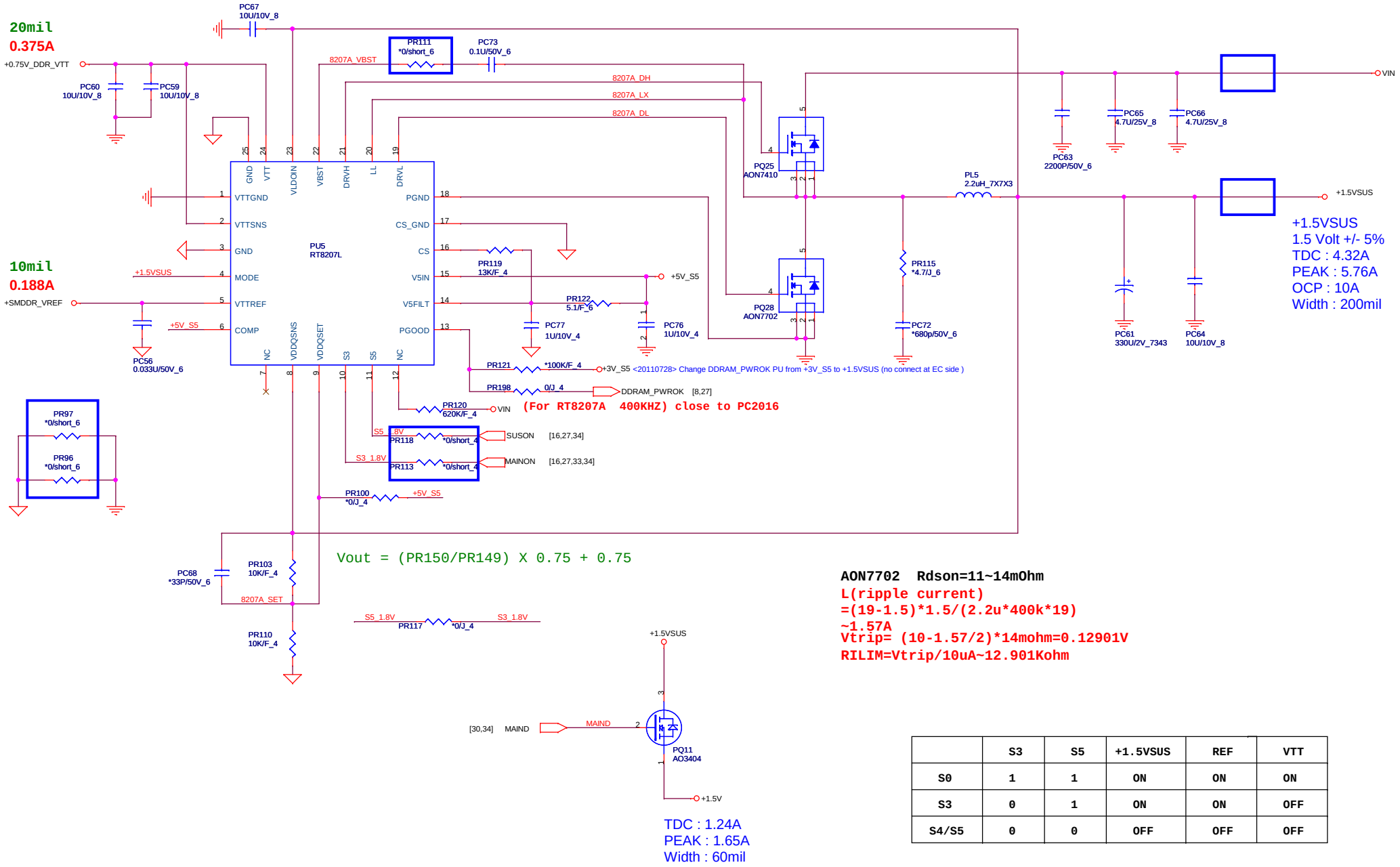
TDC : 0.94A
PEAK : 1.25A
Width : 40mil

Quanta Computer Inc.
PROJECT : ZE7
Size | Document Number: SYSTEM 5V/3V (RT8206) | Rev: 1B
Date: Wednesday, November 02, 2011 | Sheet 30 of 40



Quanta Computer Inc.			
PROJECT : ZE7			
Size	Document Number		Rev
	CPU CORE (RT8165B)		1B
Date: Wednesday, November 02, 2011		Sheet 31 of 40	

[PWM]



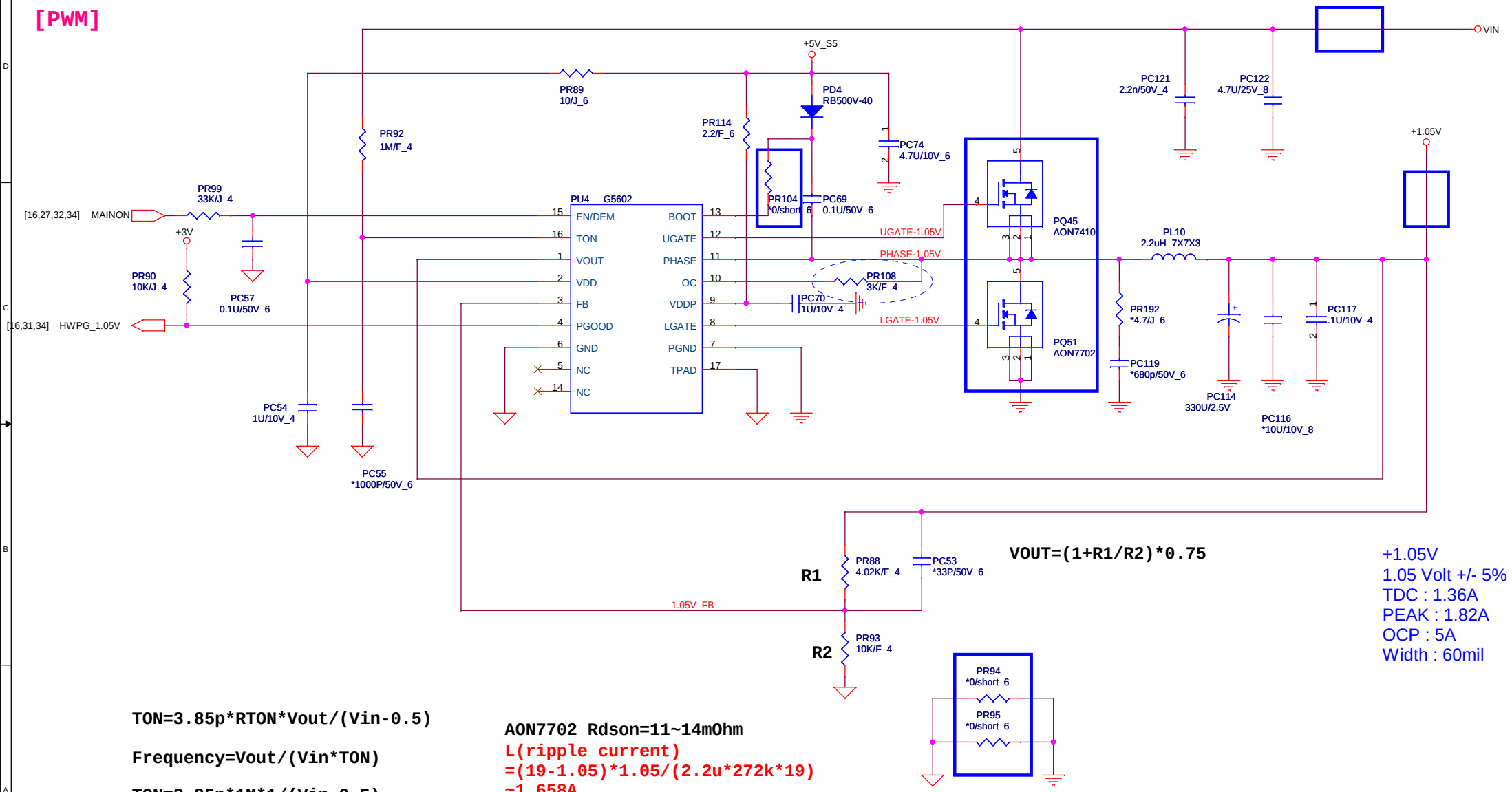
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1B
Date: Wednesday, November 02, 2011	Sheet 32 of 40	

[PWM]



VOUT=(1+R1/R2)*0.75

+1.05V
1.05 Volt +/- 5%
TDC : 1.36A
PEAK : 1.82A
OCP : 5A
Width : 60mil

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AON7702 Rdson=11~14mOhm

L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.658A

Rth=14m*(5-0.829)/20uA
RILIM=2.92Kohm

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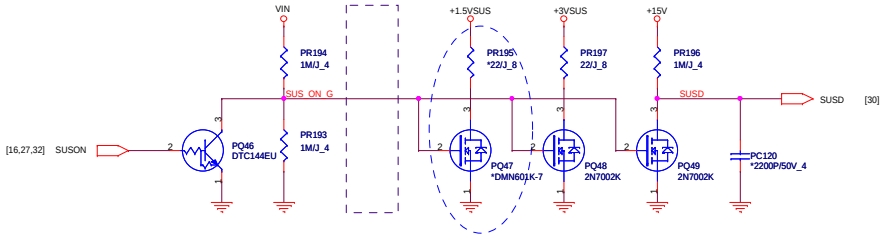
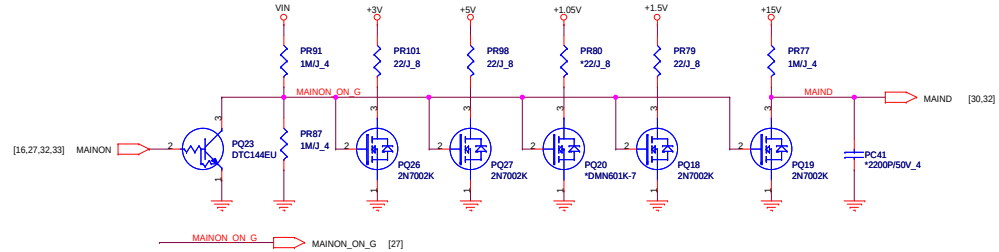
PROJECT : ZE7

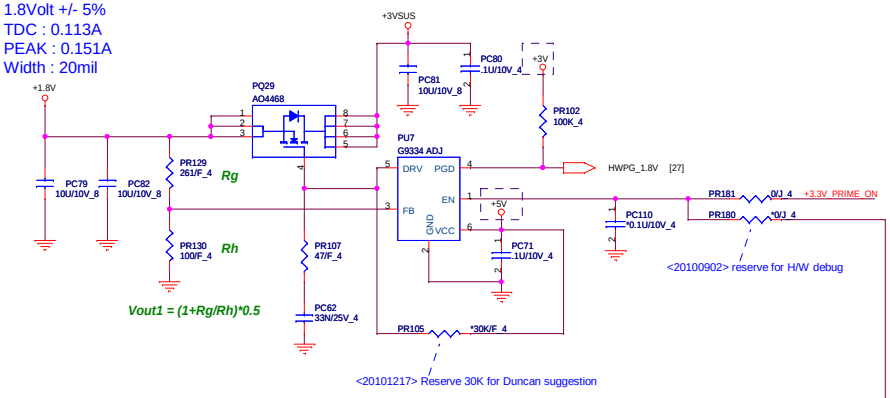
Size	Document Number	Rev
	+1.05V(UP6111AQDD)	1B
Date: Wednesday, November 02, 2011	Sheet 33 of 40	

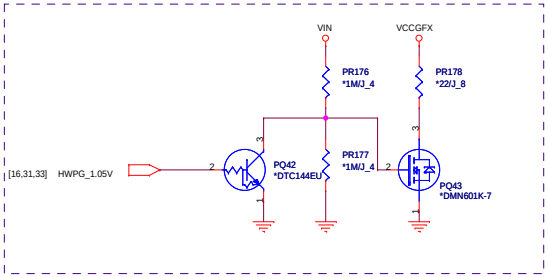




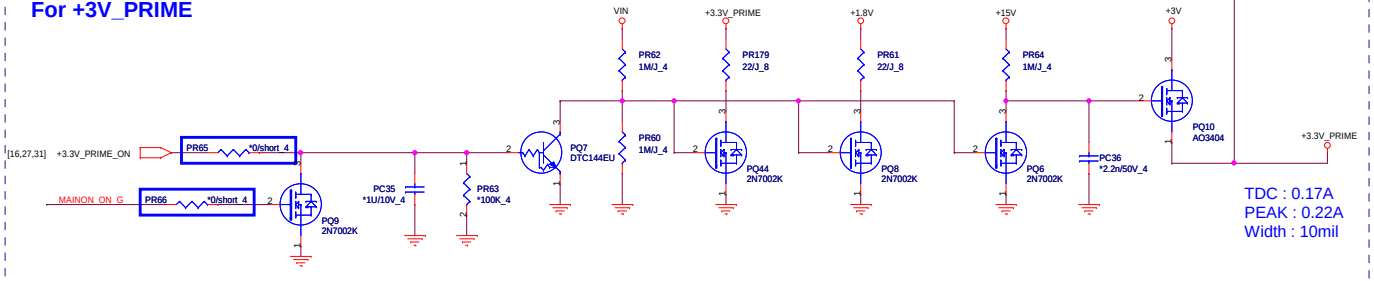
Reserve For VCCGFX

+1.8V
1.8Volt +/- 5%
TDC : 0.113A
PEAK : 0.151A
Width : 20mil





For +3V_PRIME



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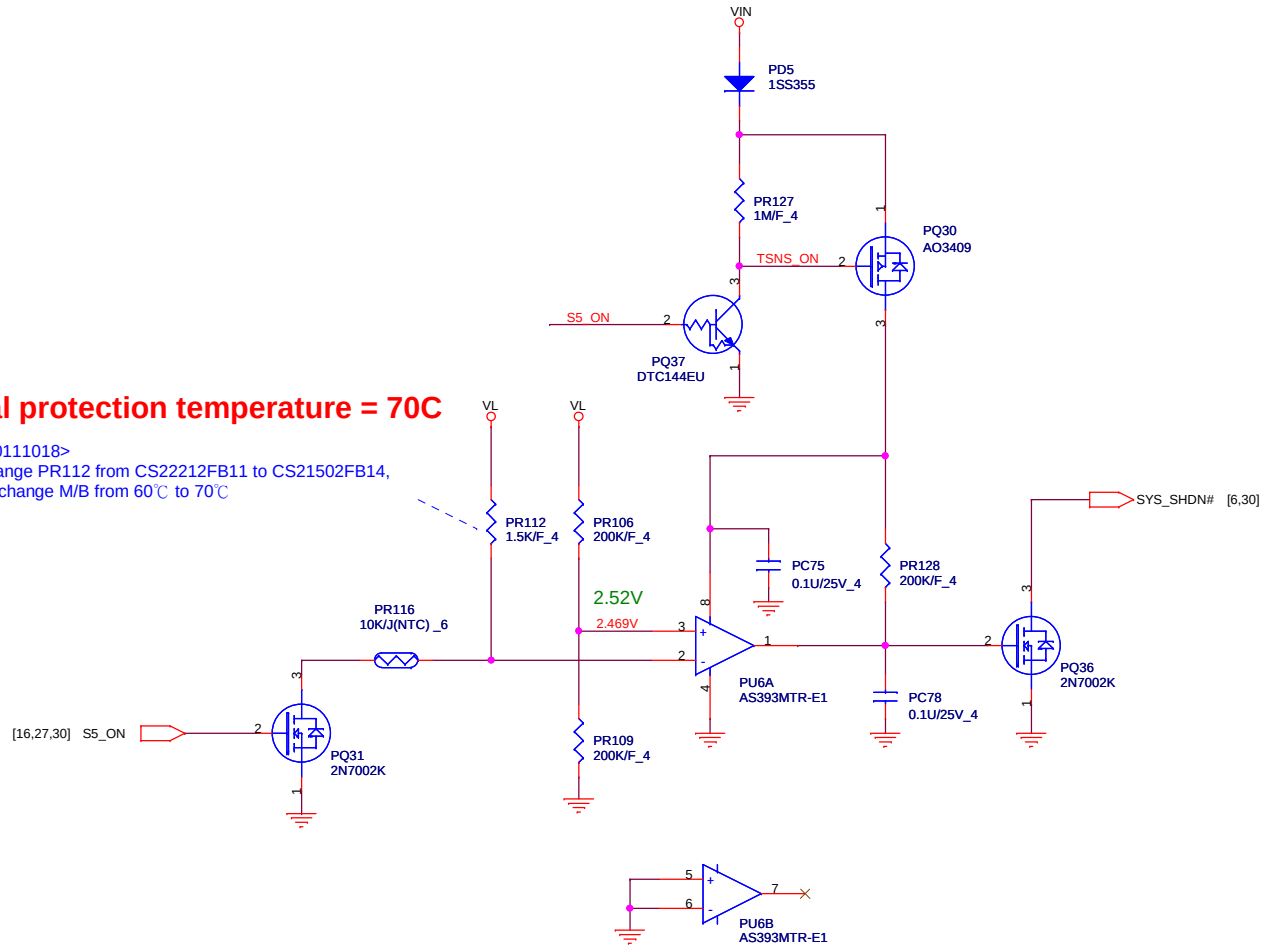
PROJECT : ZE7

Size	Document Number	Rev
	Discharge/1.8V	1B
Date: Wednesday, November 02, 2011	Sheet 34 of 40	

Thermal Protection (DCD)

Thermal protection temperature = 70C

<20111018>
Change PR112 from CS22212FB11 to CS21502FB14,
for change M/B from 60℃ to 70℃



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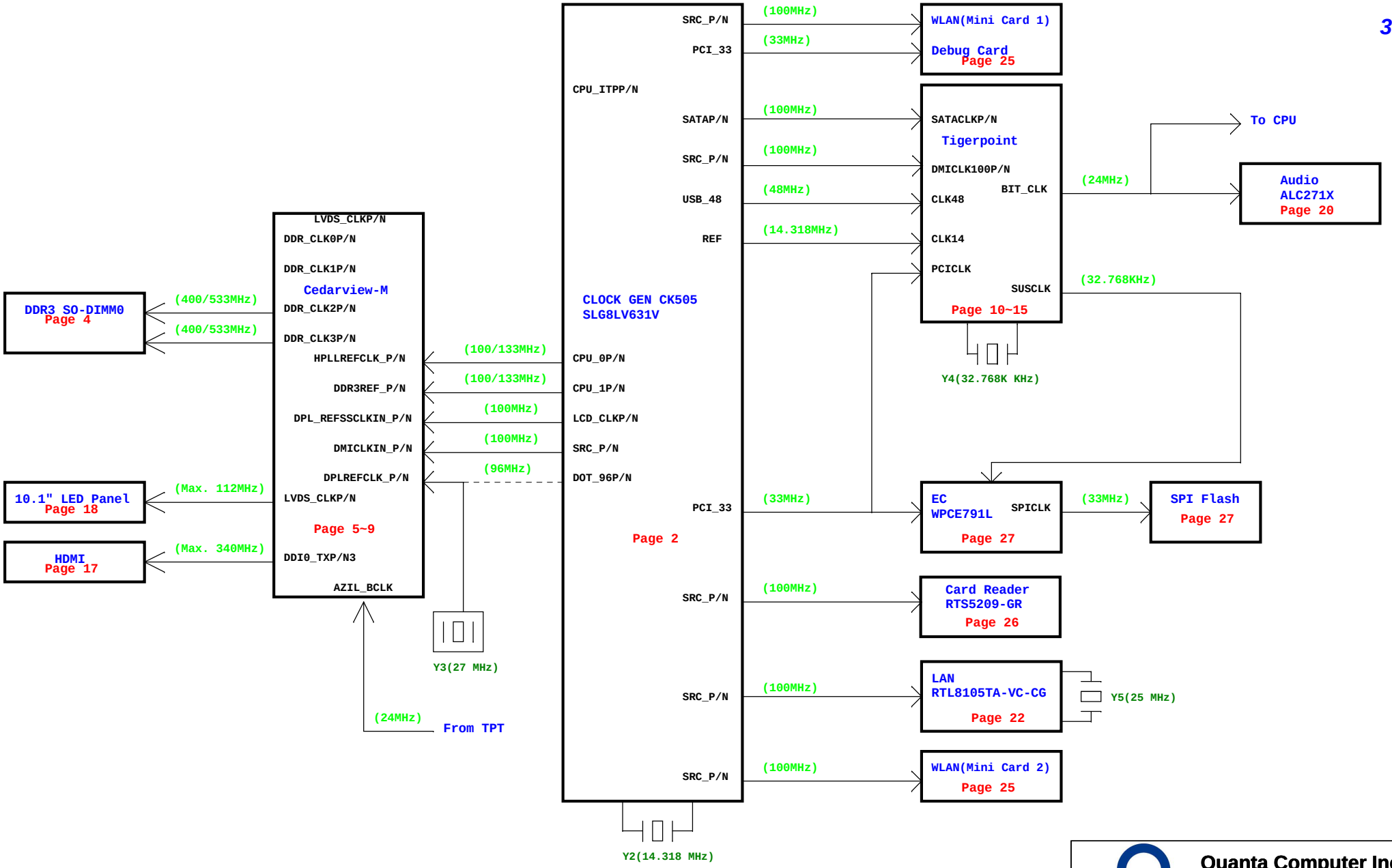
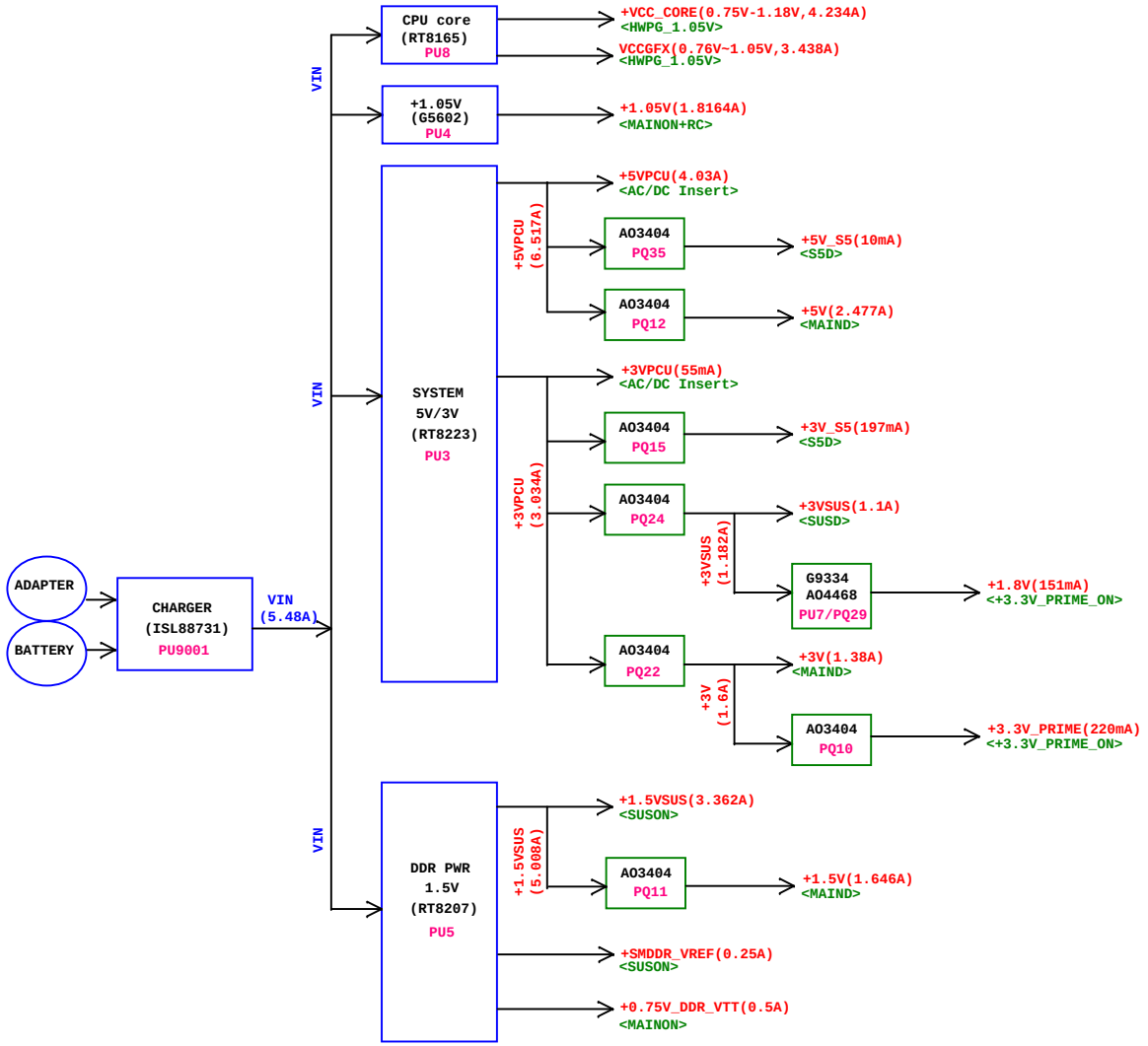
Size	Document Number	Rev
	Thermal protect	1B
Date: Wednesday, November 02, 2011	Sheet 35 of 40	



Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: Clock Distribution Diagram	Rev 1B
Date: Wednesday, November 02, 2011	Sheet 36 of 40	



BOM Structure

	Function	Description	
3G	3G@	w/ 3G module	stuff 3G@
		w/o 3G module	unstuff 3G@
BT	BT@	w/ BT module	stuff BT@
		w/o BT module	unstuff BT@
LVDS/EDP	LVDS@	w/ LVDS (default)	stuff LVDS@ L38: CV+1003JN01 (0.1UH) C334: CH5102K9B06 (1UF)
	EDP@	w/ EDP	stuff EDP@ L38: CS00003J951 (0ohm) C334:CS00002JB38 (0ohm)
PLL Power	1.5VPLL@	w/ 1.5VPLL (default)	stuff 1.5VPLL@
	1.05VPLL@	w/ 1.05VPLL	stuff 1.05VPLL@

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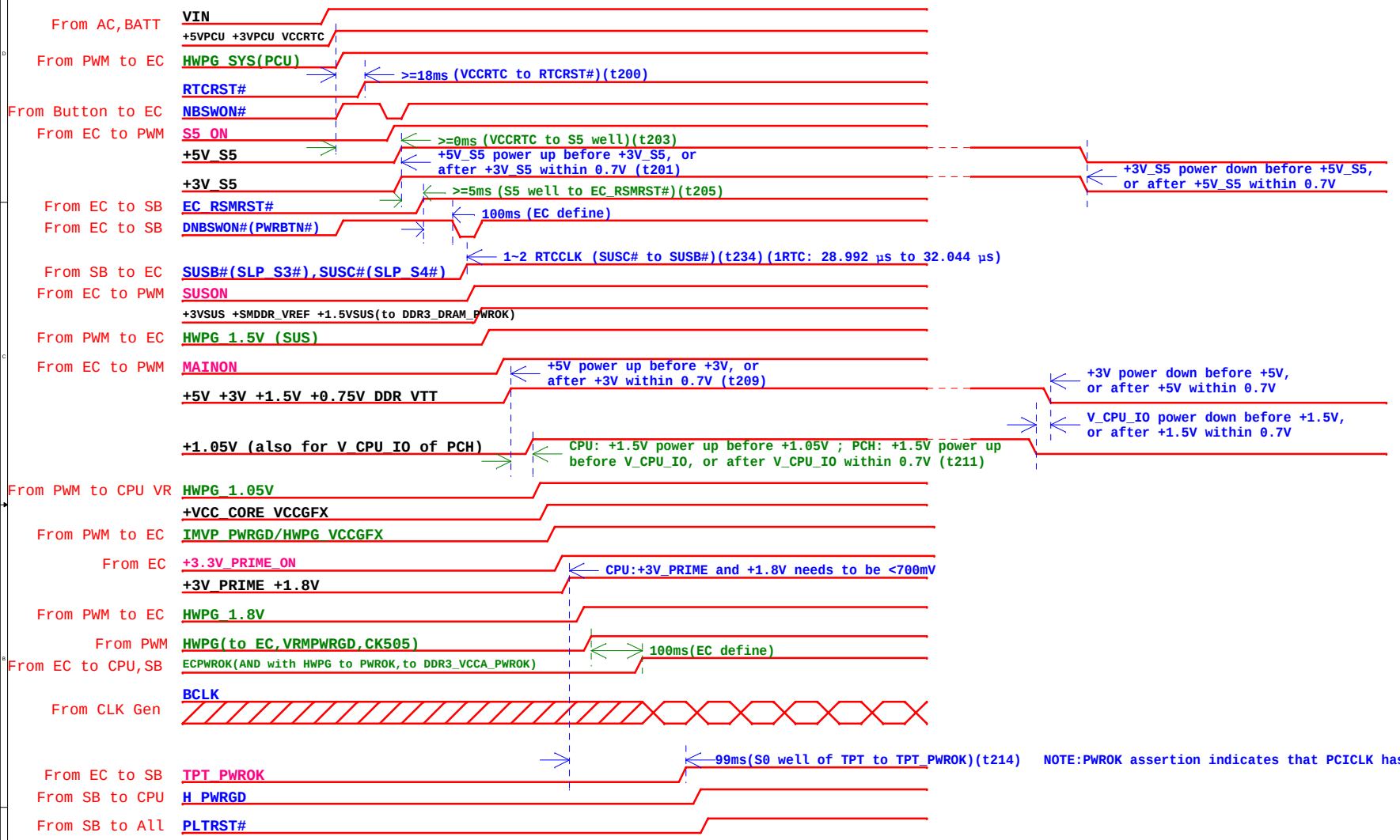
PROJECT : ZE7
Size | Document Number | Rev 1B
Power Tree
Date: Wednesday, November 02, 2011 | Sheet 37 of 46

JE01_CT(Cedar Trail) Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

	CLK GEN	RAM	*Mini Card (WLAN)	*XDP	
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V	
Power Plane	+3V	+3V	+3V	+3V	
MOS CKT (Level shift)	Stuff	Stuff	Stuff	Stuff	

*=Reserve

EC SMBUS Table

	Battery	CPU Thermal Sensor	GFX Thermal Sensor
EC791 SDA1 / SCL1 (+3VPCU)	V		
EC791 SDA2 / SCL2			
EC791 SDA3 / SCL3			
Power Plane	+3VPCU		
MOS CKT (Level shift)	X		

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Size | Document Number: Power Sequence | Rev 1B
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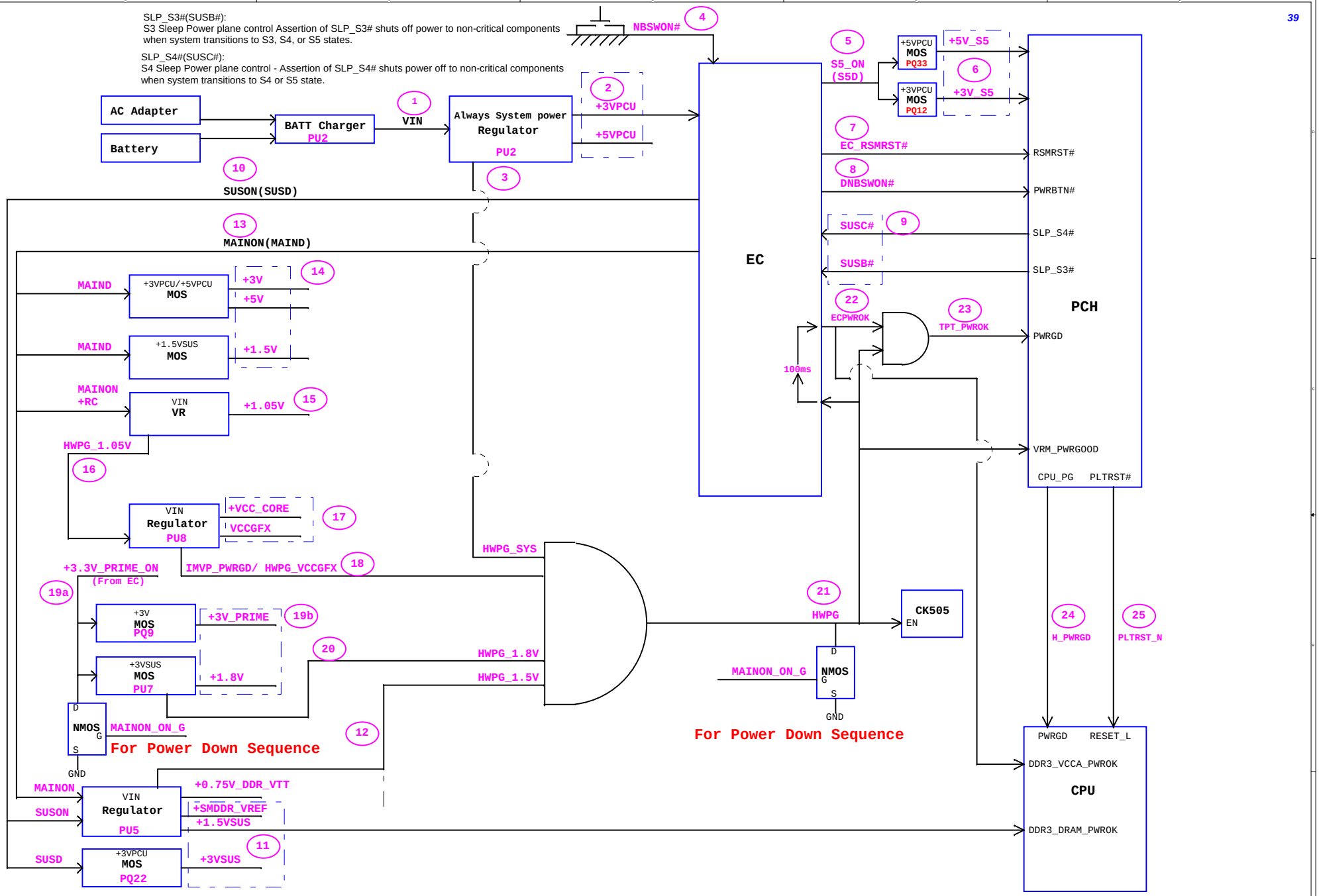
SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S4#(SUSC#):
S4 Sleep Power plane control - Assertion of SLP_S4# shuts power off to non-critical components when system transitions to S4 or S5 state.



Quanta Computer Inc.
PROJECT : ZE7
power sequence block diagram
Rev 1B
Wednesday, November 07, 2012
Sheet 39 of 40

Model	REV	CHANGE LIST
ZE7 MB	1A	First Released (PCB: A)
	1B	<Page 5> Update CPU P/N to MP P/N <Page 19> Un-stuff CA122084N98 at CP1 - CP6 by EMI confirmation <Page 18> Stuff R26 CS00003J951 (0/J_6) for +5V_LCD (IVO panel) Change 0ohm resistors to short PAD

MODEL	ZE7	
	FROM	To
	1A	1B

DOC NO.					
PROJECT MODEL :	ZE7	APPROVED BY:		DATE:	2011/11/2
PART NUMBER:		DRAWING BY:		REVISON:	1B

Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	Change List1	1B

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