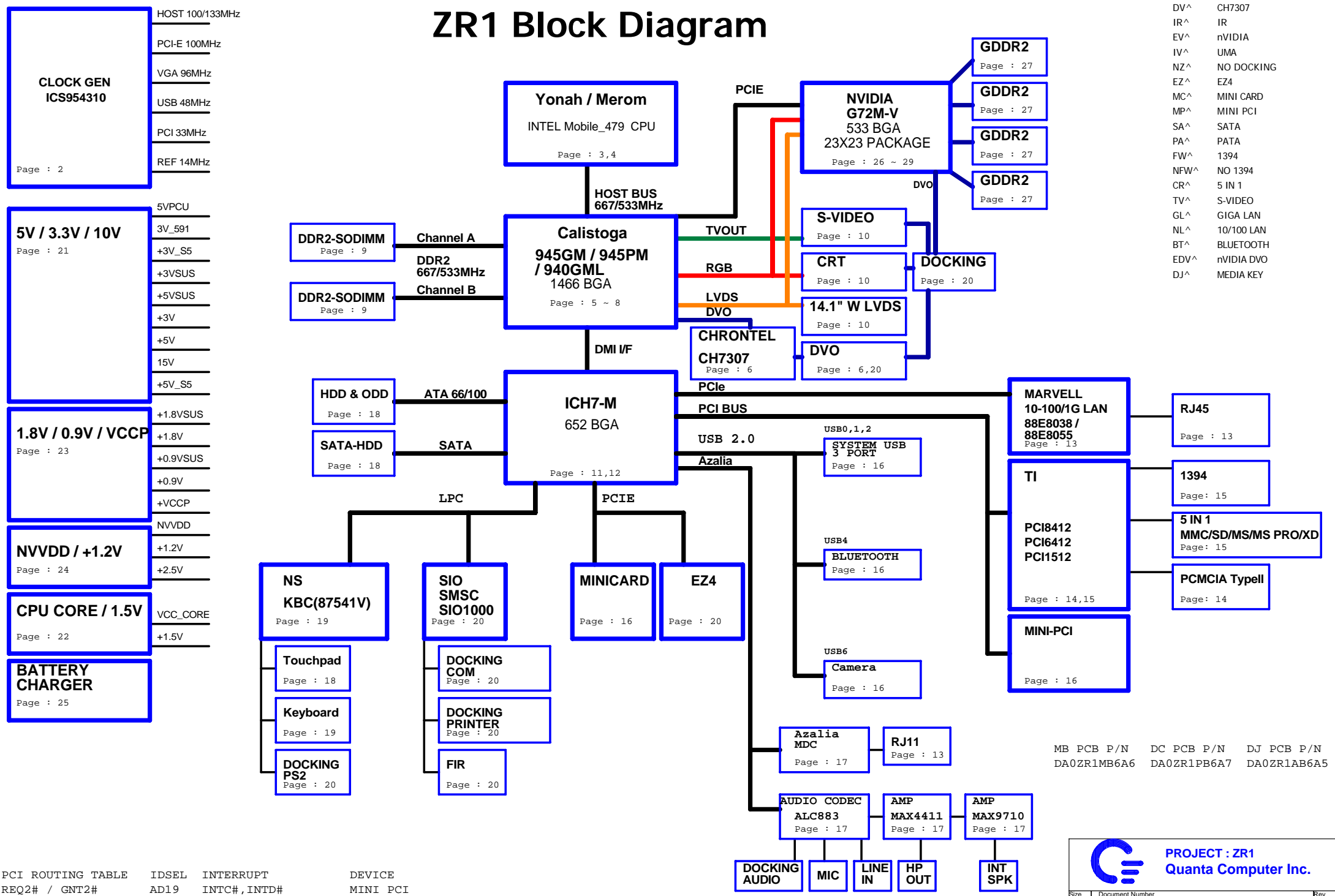


ZR1 Block Diagram



- DV^ CH7307
- IR^ IR
- EV^ nVIDIA
- IV^ UMA
- NZ^ NO DOCKING
- EZ^ EZ4
- MC^ MINI CARD
- MP^ MINI PCI
- SA^ SATA
- PA^ PATA
- FW^ 1394
- NFW^ NO 1394
- CR^ 5 IN 1
- TV^ S-VIDEO
- GL^ GIGA LAN
- NL^ 10/100 LAN
- BT^ BLUETOOTH
- EDV^ nVIDIA DVO
- DJ^ MEDIA KEY

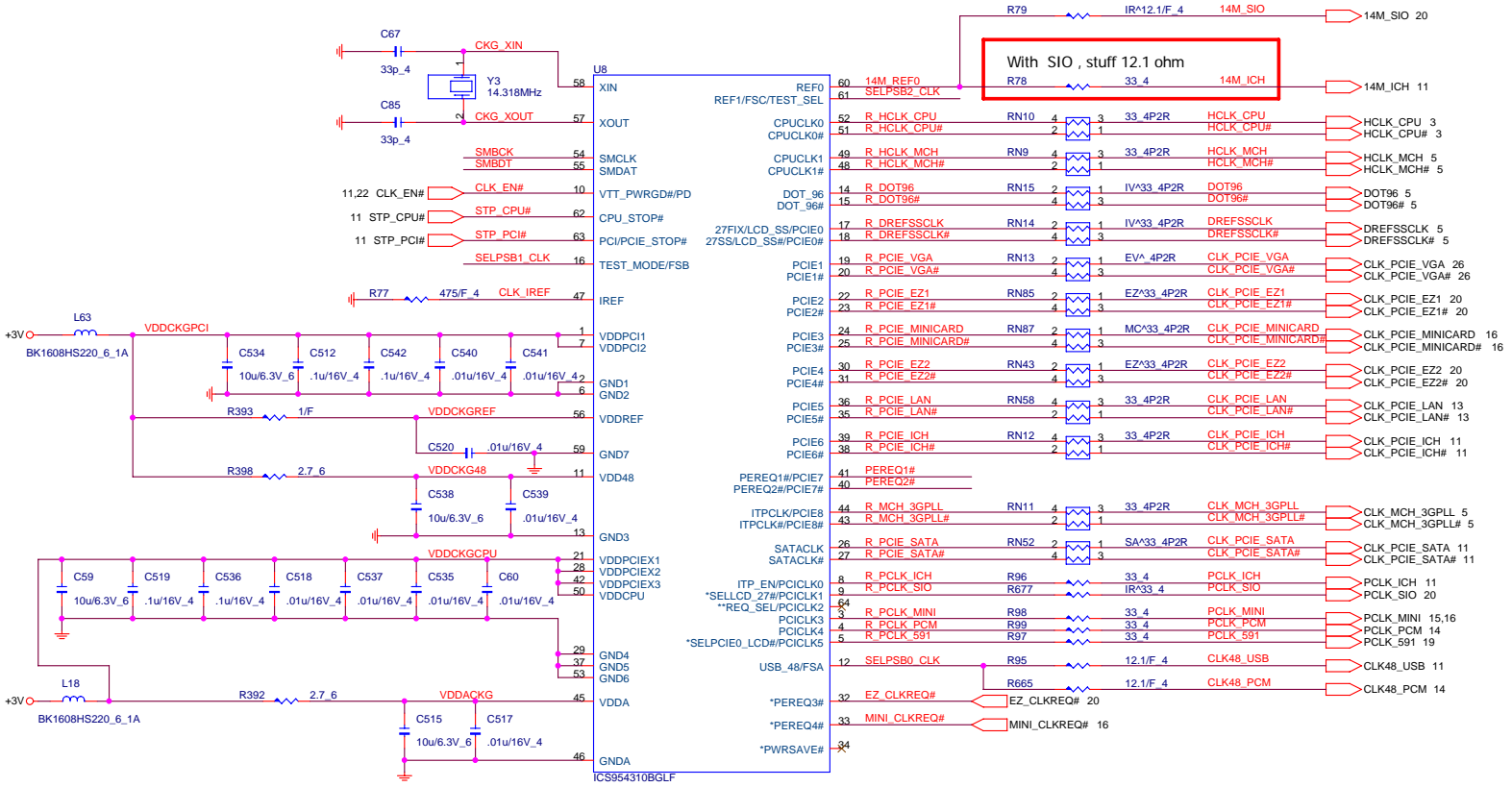
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ2# / GNT2#	AD19	INTC#, INTD#	MINI PCI
REQ0# / GNT0#	AD25	INTE#, INTF#, INTG#	TI XX12

MB PCB P/N DC PCB P/N DJ PCB P/N
 DA0ZR1MB6A6 DA0ZR1PB6A7 DA0ZR1AB6A5

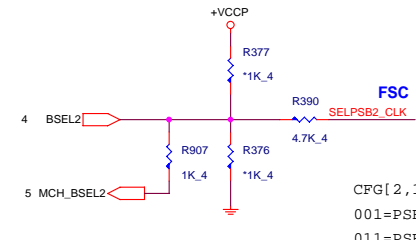
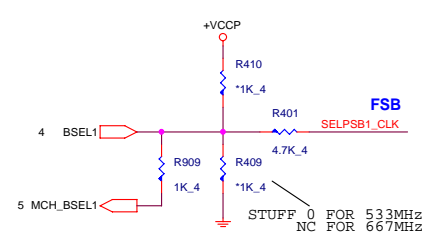
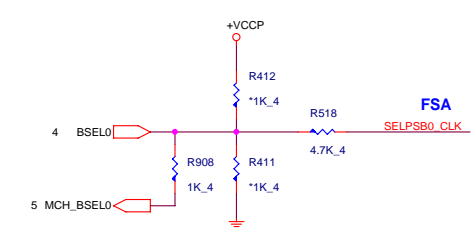
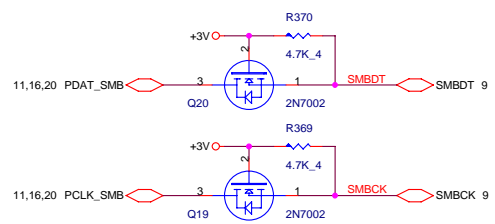
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
BLOCK DIAGRAM		1A
Date:	Wednesday, March 29, 2006	Sheet 1 of 29

CLOCK GENERATOR



PEREQ1# --> PCIE0 & PCIE6
 PEREQ2# --> PCIE1 & PCIE8
 PEREQ3# --> PCIE2 & PCIE4
 PEREQ4# --> PCIE3 & PCIE5 & PCIE7



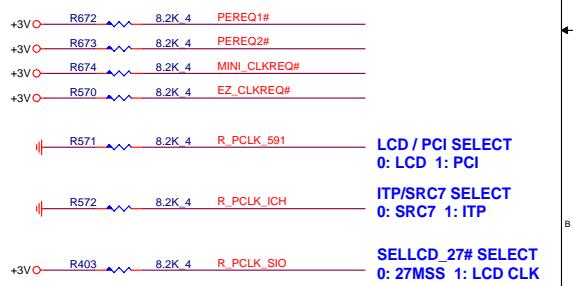
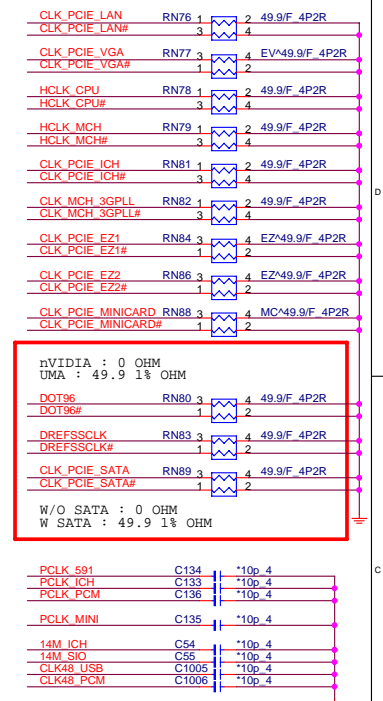
CFG[2,1,0]
 001=PSB533
 011=PSB667

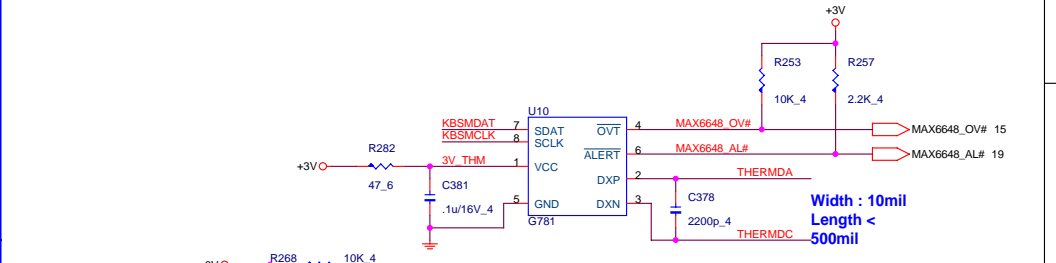
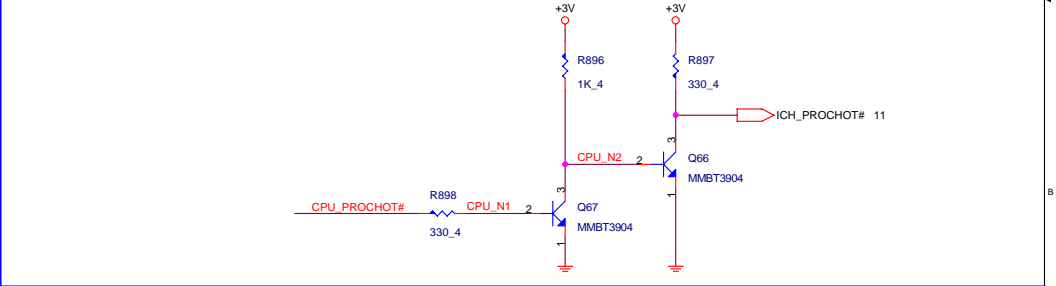
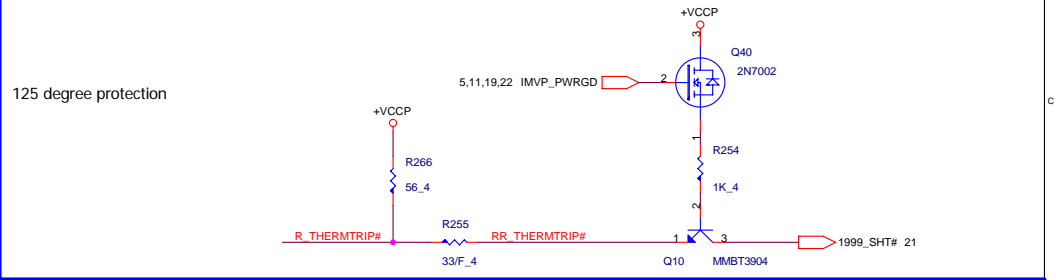
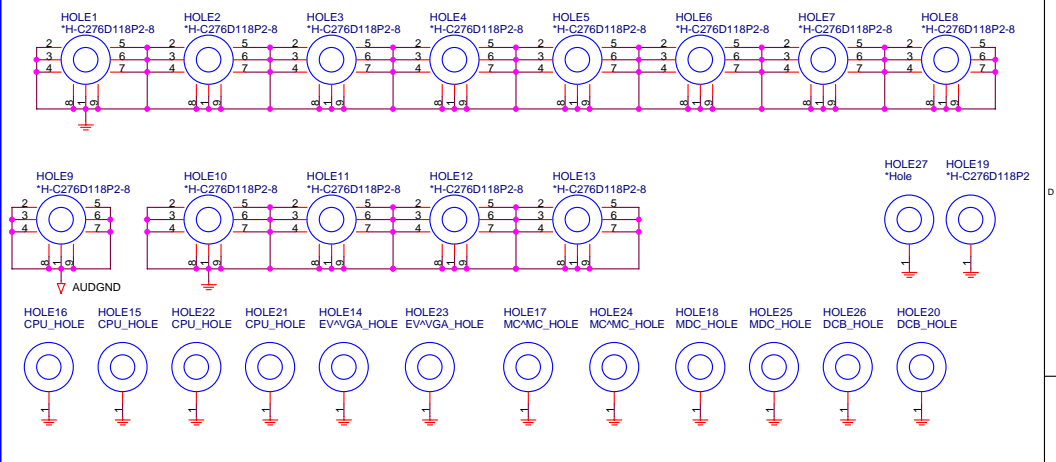
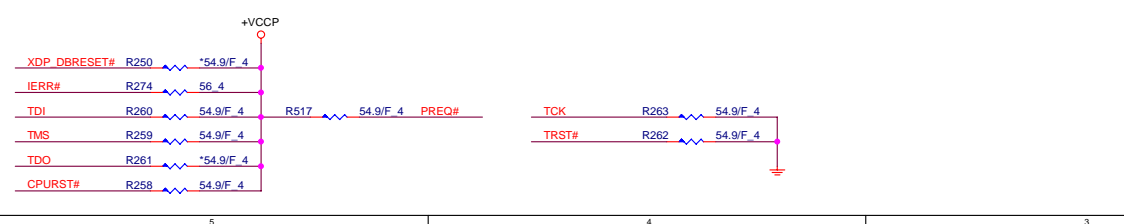
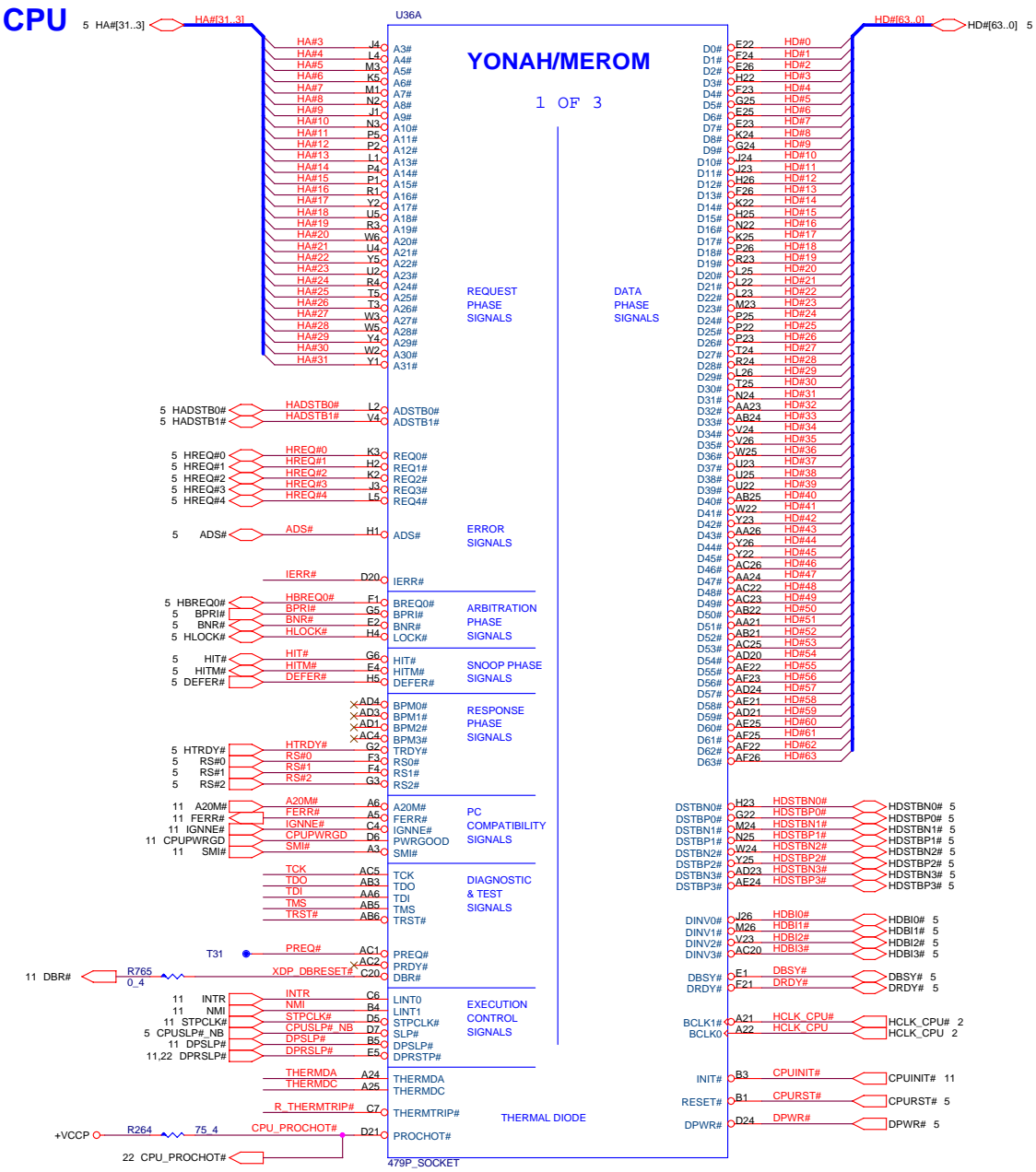
FSB SETTING

FSC	FSB	FSA	CPU	PCIE	PCI
0	0	0	266	100	33
0	0	1	133	100	33
0	1	0	200	100	33
0	1	1	166	100	33
1	0	0	333	100	33
1	0	1	100	100	33
1	1	0	400	100	33
1	1	1	200	100	33

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Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date:	Wednesday, March 29, 2006	Sheet 2 of 29





CPU

COMPO - COMP3

Width : 20mil
Length < 500mil

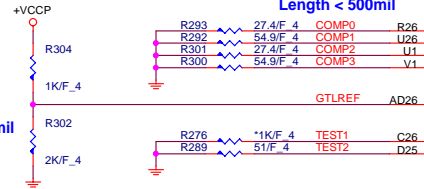
U36B

YONAH/MEROM

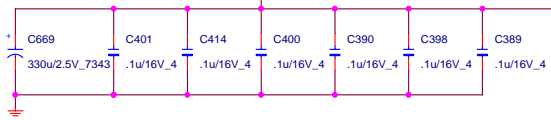
2 OF 3

POWER,
RESERVED
SIGNALS

GTLREF
Width : 5mil
Length < 500mil



+VCCP



- V6 VCCP00
- G21 VCCP01
- K6 VCCP02
- M6 VCCP03
- K2 VCCP04
- J21 VCCP05
- K21 VCCP06
- M21 VCCP07
- N21 VCCP08
- R21 VCCP09
- R6 VCCP10
- T21 VCCP11
- T6 VCCP12
- V21 VCCP13
- W21 VCCP14
- VCCP15

- AA1 RSVCO0
- AA2 RSVCO1
- AA3 RSVCO2
- M4 RSVCO3
- N5 RSVCO4
- T2 RSVCO5
- V3 RSVCO6
- B2 RSVCO7
- C3 RSVCO8
- B25 RSVCO9
- T22 RSVCO10
- D2 RSVCO11
- F6 RSVCO12
- D3 RSVCO13
- C1 RSVCO14
- AF1 RSVCO15
- D22 RSVCO16
- C23 RSVCO17
- C24 RSVCO18
- RSVC19

- 2 BSEL0 BSEL0 B22 BSEL0
- 2 BSEL1 BSEL1 B23 BSEL1
- 2 BSEL2 BSEL2 C21 BSEL2

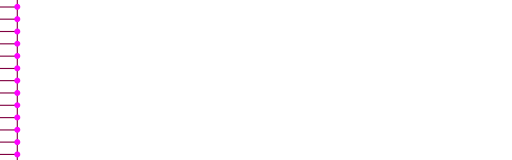
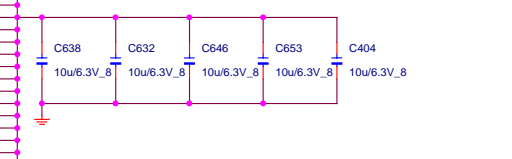
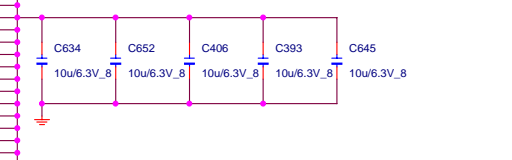
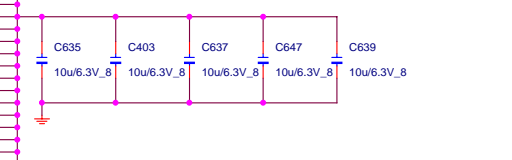
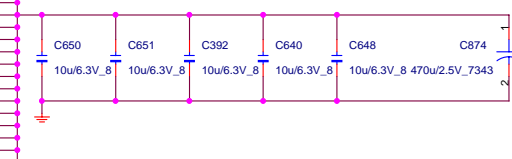
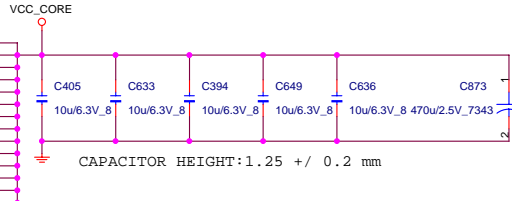
- 22 PSI# PSI# AE6 PSI#

- 22 CPU_VID0 CPU_VID0 AD6 VID0
- 22 CPU_VID1 CPU_VID1 AE5 VID1
- 22 CPU_VID2 CPU_VID2 AF4 VID2
- 22 CPU_VID3 CPU_VID3 AF4 VID3
- 22 CPU_VID4 CPU_VID4 AE3 VID4
- 22 CPU_VID5 CPU_VID5 AF2 VID5
- 22 CPU_VID6 CPU_VID6 AE2 VID6

- 22 VCCSENSE VCCSENSE AF7 VCCSENSE

- 22 VSSSENSE VSSSENSE AE7 VSSSENSE

VCC CORE

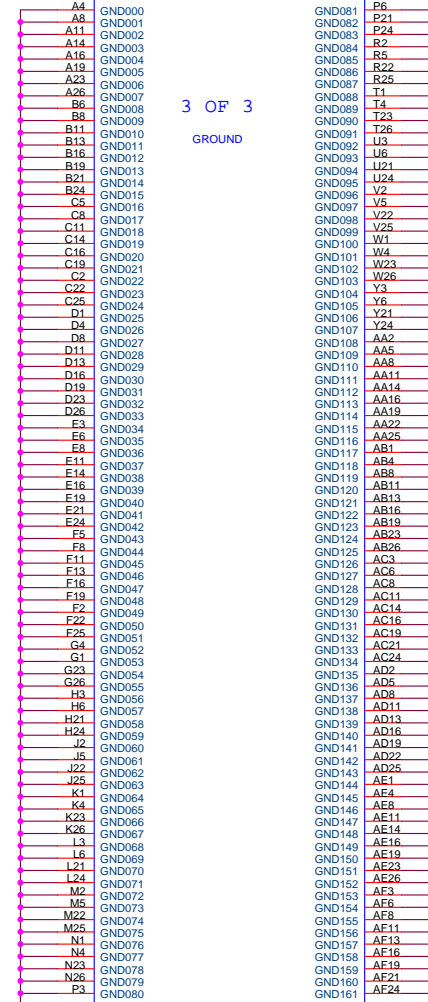


U36C

YONAH/MEROM

3 OF 3

GROUND



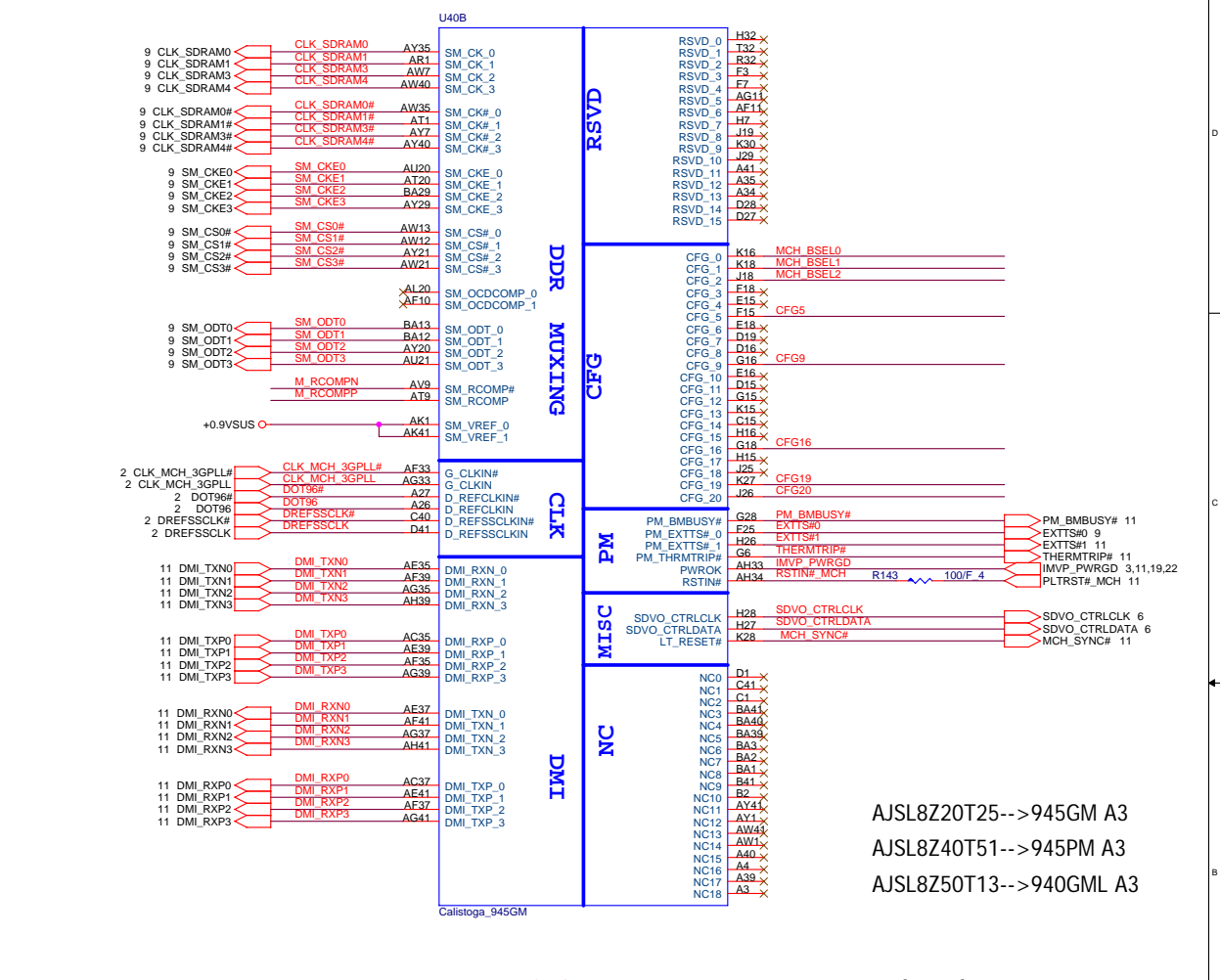
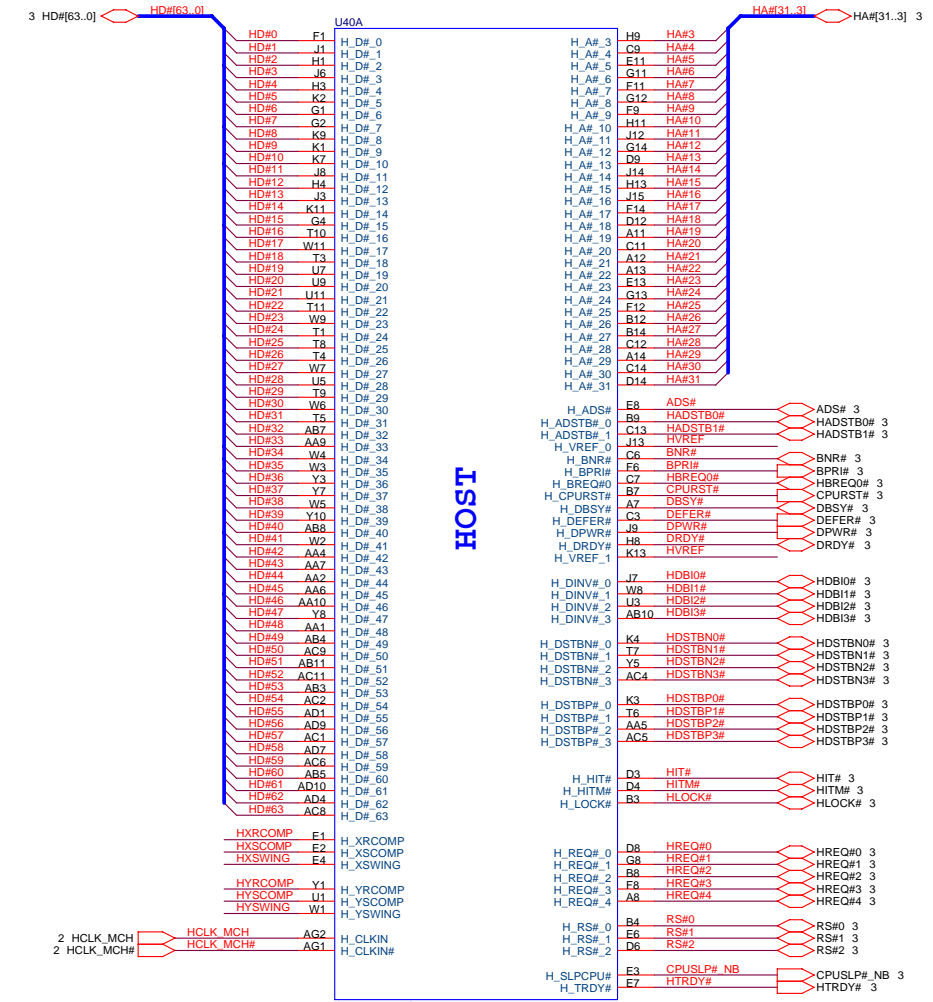
479P_SOCKET

479P_SOCKET

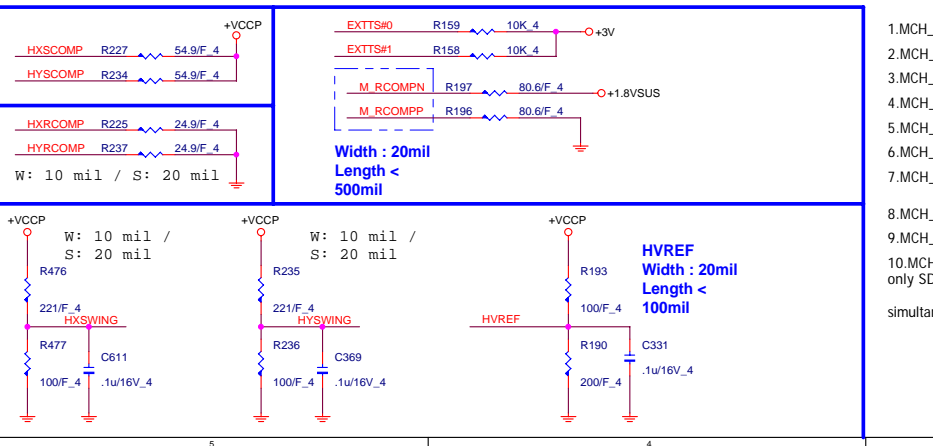


PROJECT : ZR1
Quanta Computer Inc.

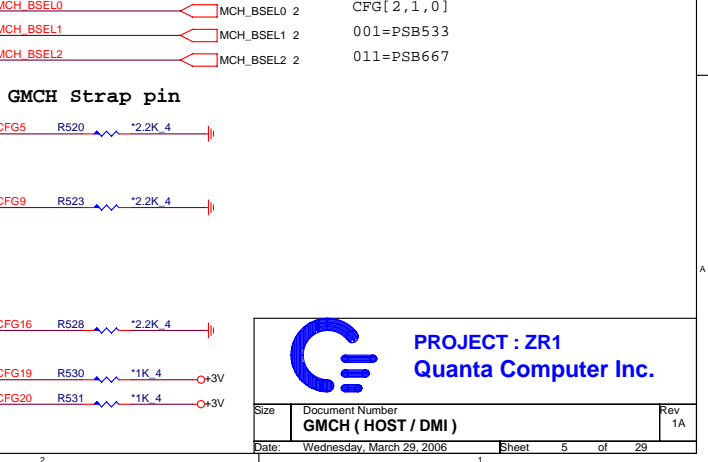
NB_945GM/PM/940GML




AJSL8Z20T25-->945GM A3
 AJSL8Z40T51-->945PM A3
 AJSL8Z50T13-->940GML A3



- MCH_CFG_5 : Low = DMI X2, High=DMIX4
- MCH_CFG_6 : Low = Moby Dick, High = Calistoga (Default)
- MCH_CFG_7 : Low = RSVD, High = Mobile CPU
- MCH_CFG_9 PCI Exp Graphics Lane: Low =Reverse lane ,High=Normal
- MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled, High= Dynamic ODT Enabled.
- MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- MCH_CFG_20 PCIe Backward interoperability mode: Low= only SDVO or PCIe x1 is operational (defaults) , High=SDVO and PCIe x1 are operation simultaneously via the PEG port.

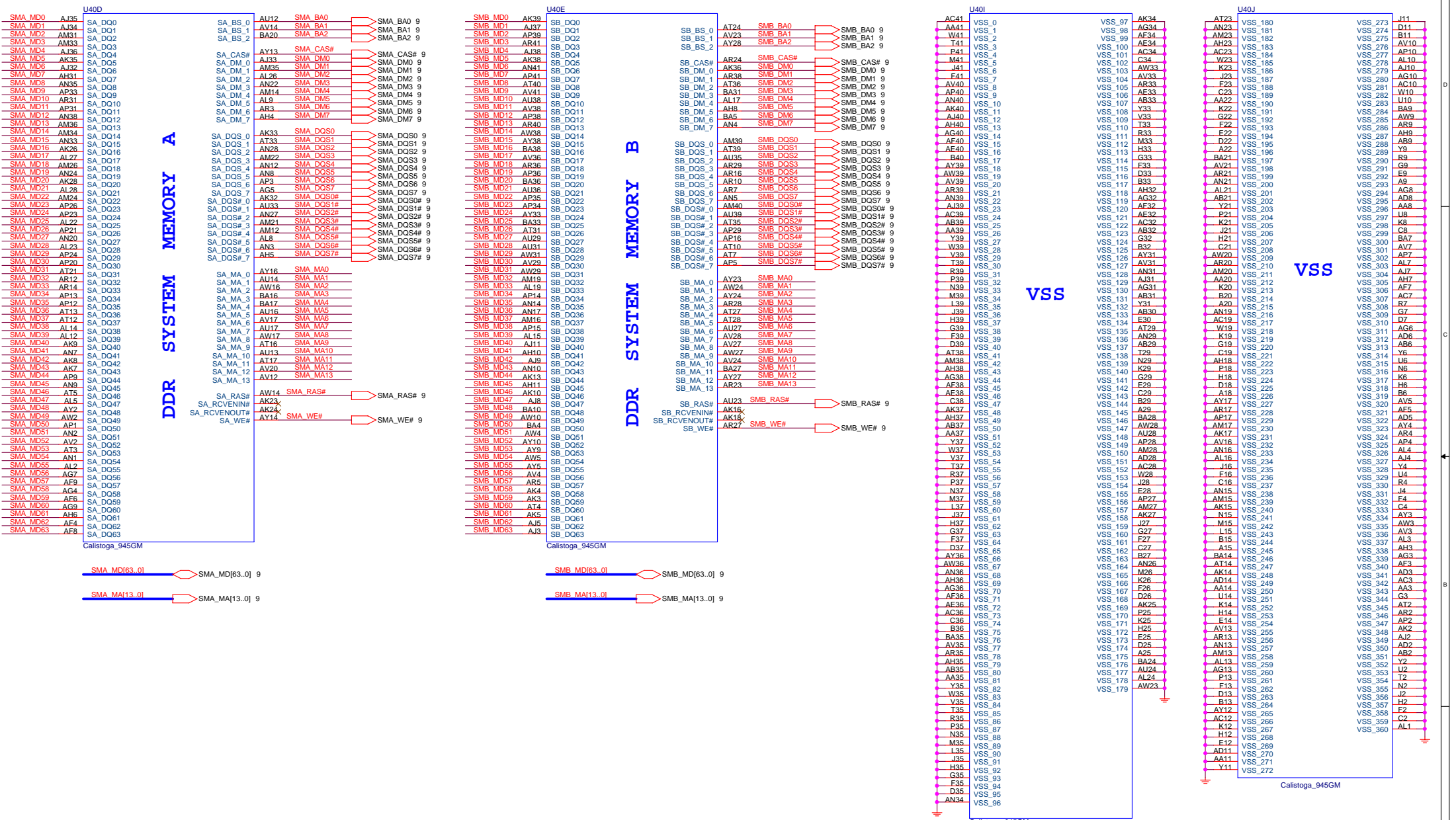




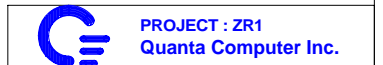
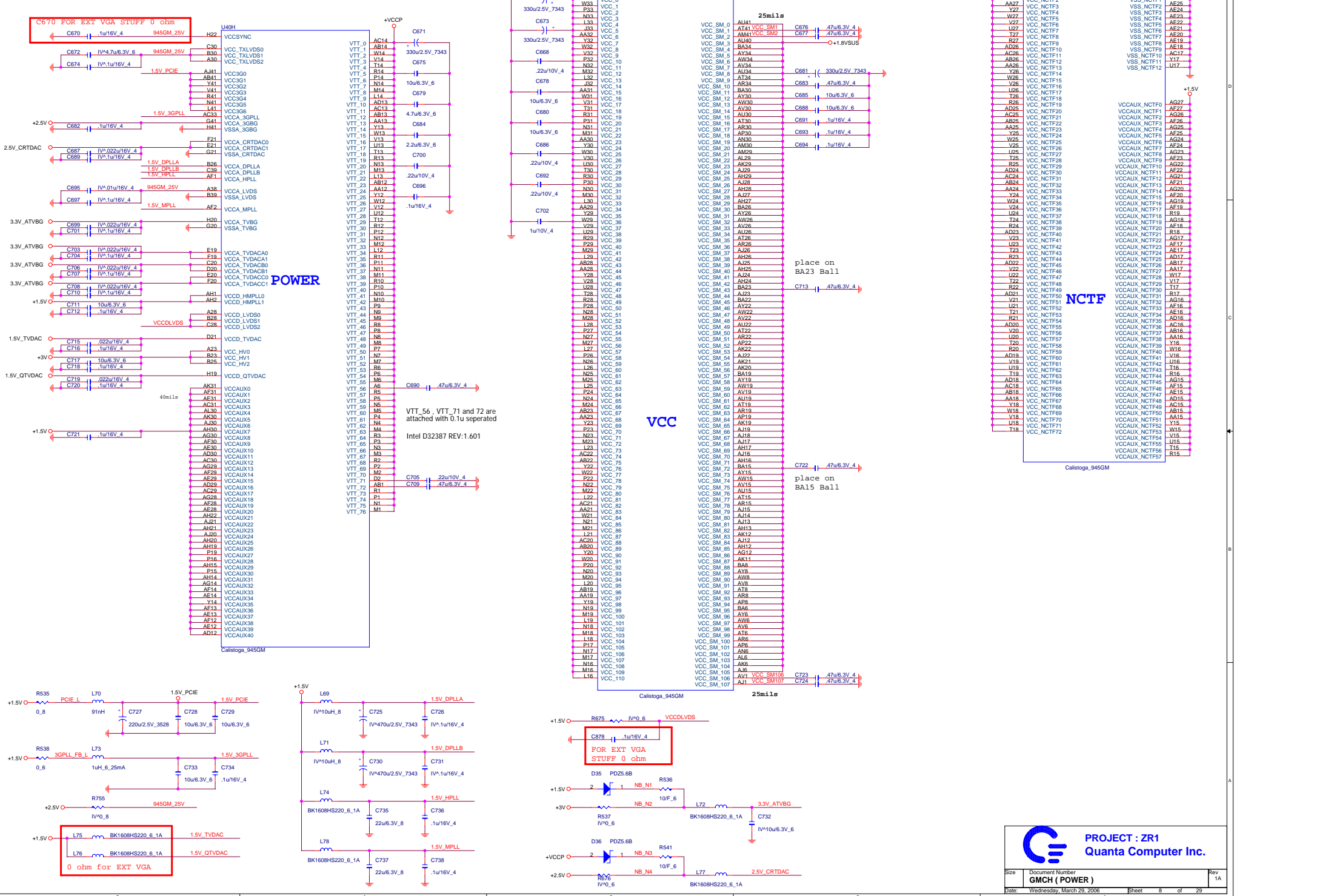
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (HOST / DMI)	1A
Date:	Wednesday, March 29, 2006	Sheet 5 of 29

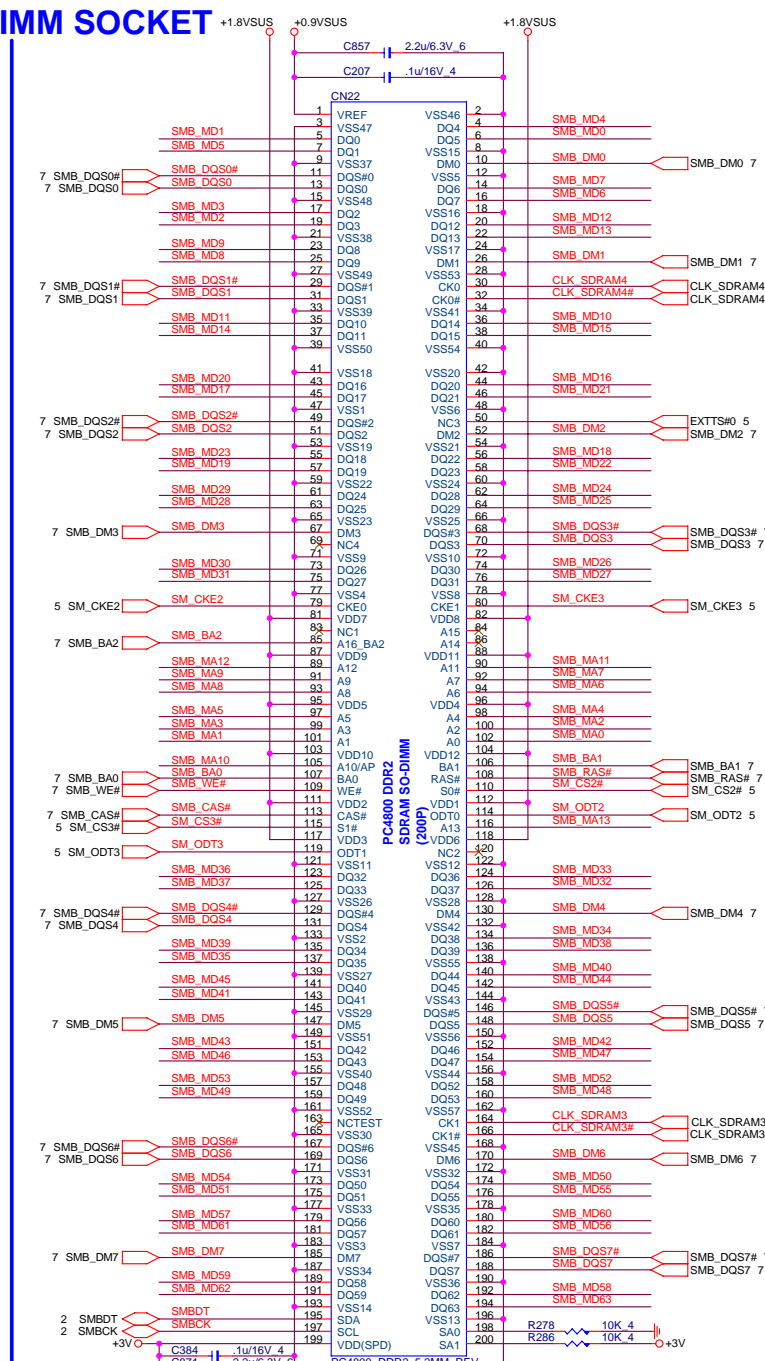
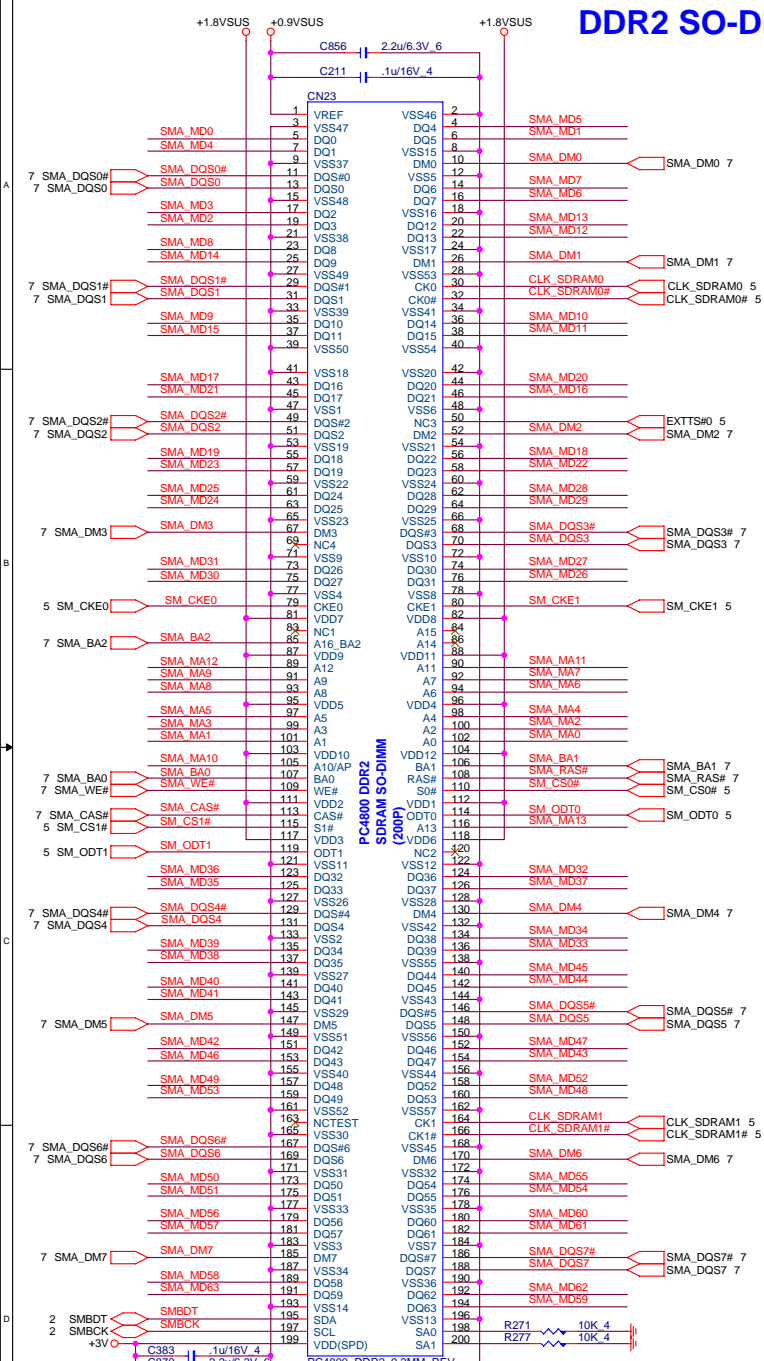
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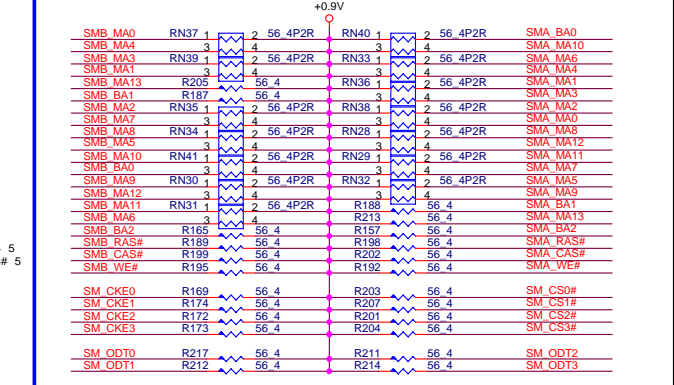
NB_945GM/PM/940GML



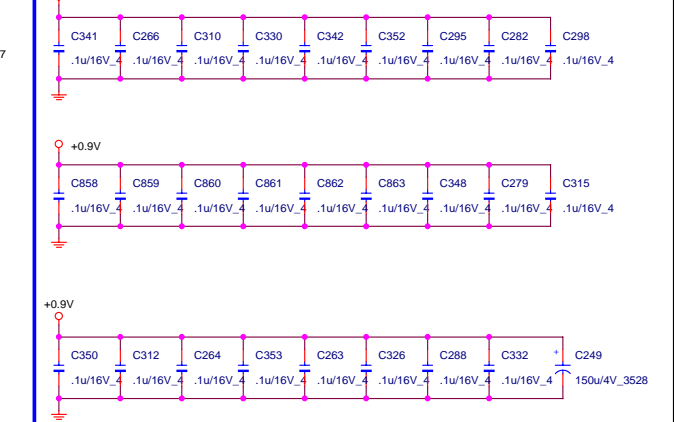
DDR2 SO-DIMM SOCKET



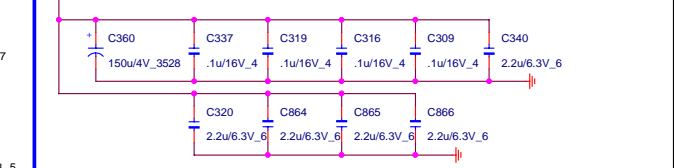
DDR2 TERMINATOR



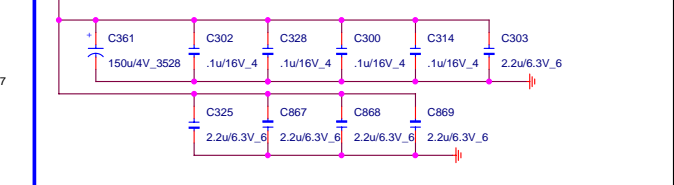
TERMINATOR DECOUPLING CAPACITOR



CLOSE SO-DIMM SOCKET CAPACITORS

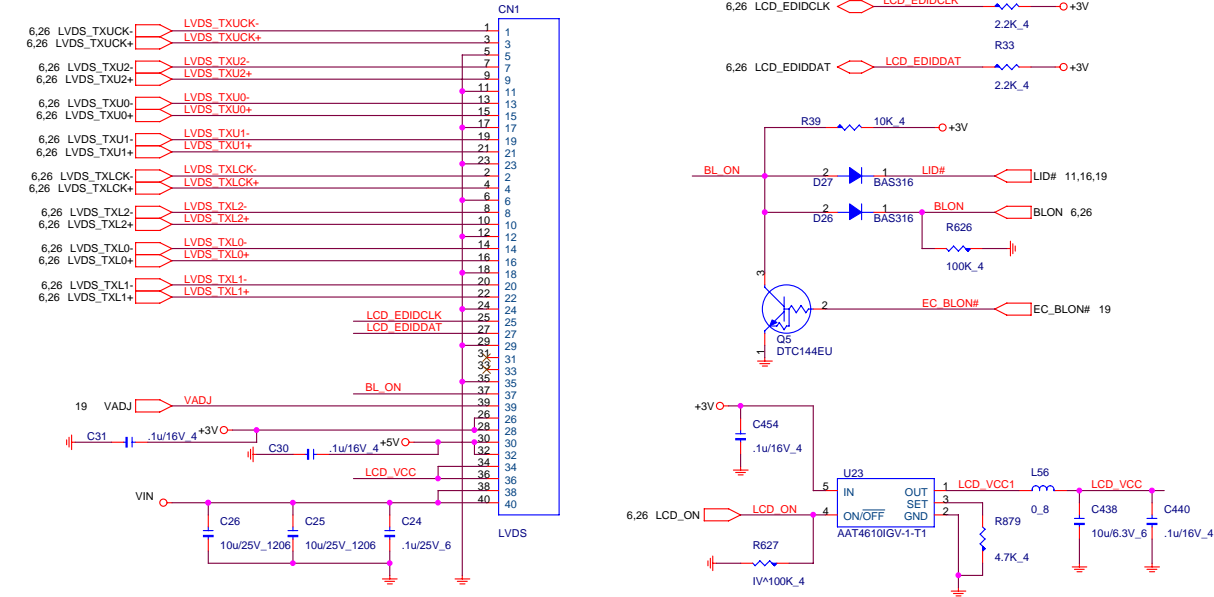


CLOSE SO-DIMM SOCKET CAPACITORS

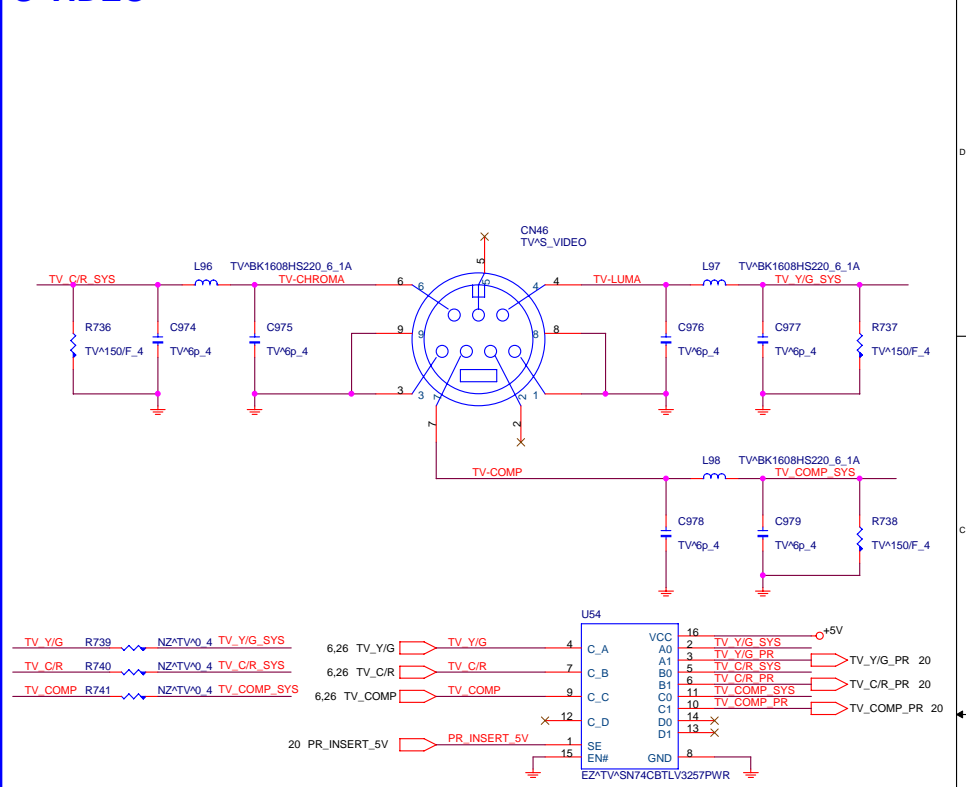


PROJECT : ZR1
 Quanta Computer Inc.

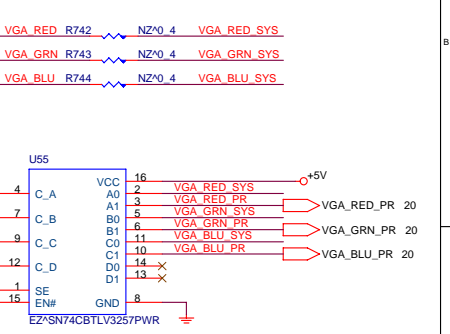
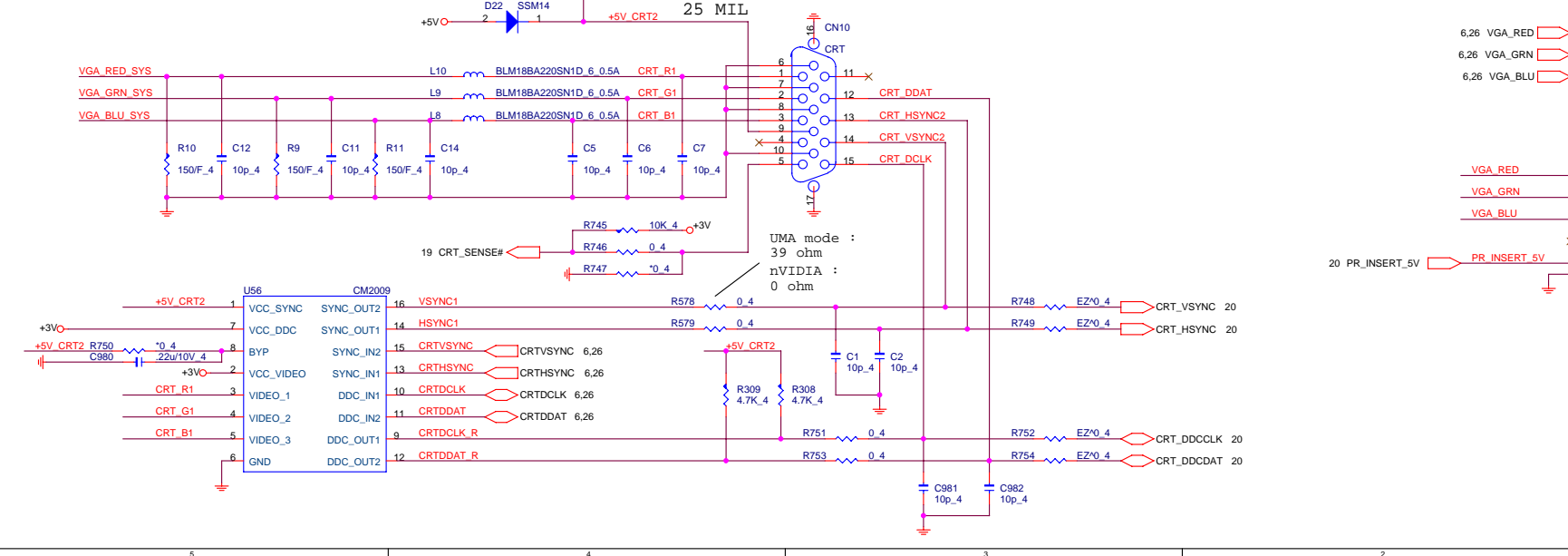
LVDS

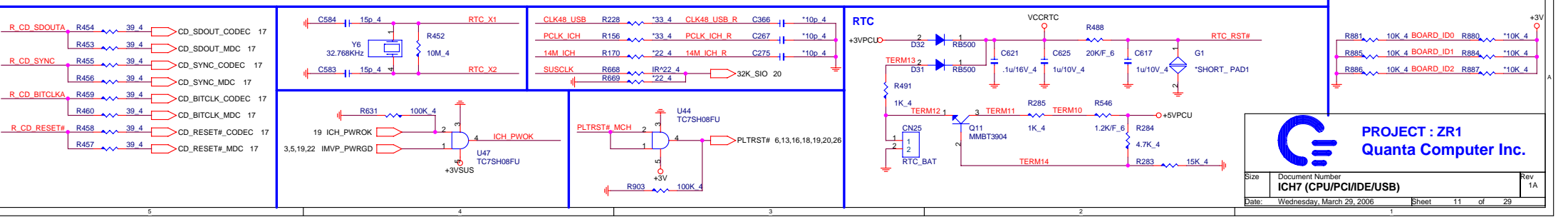
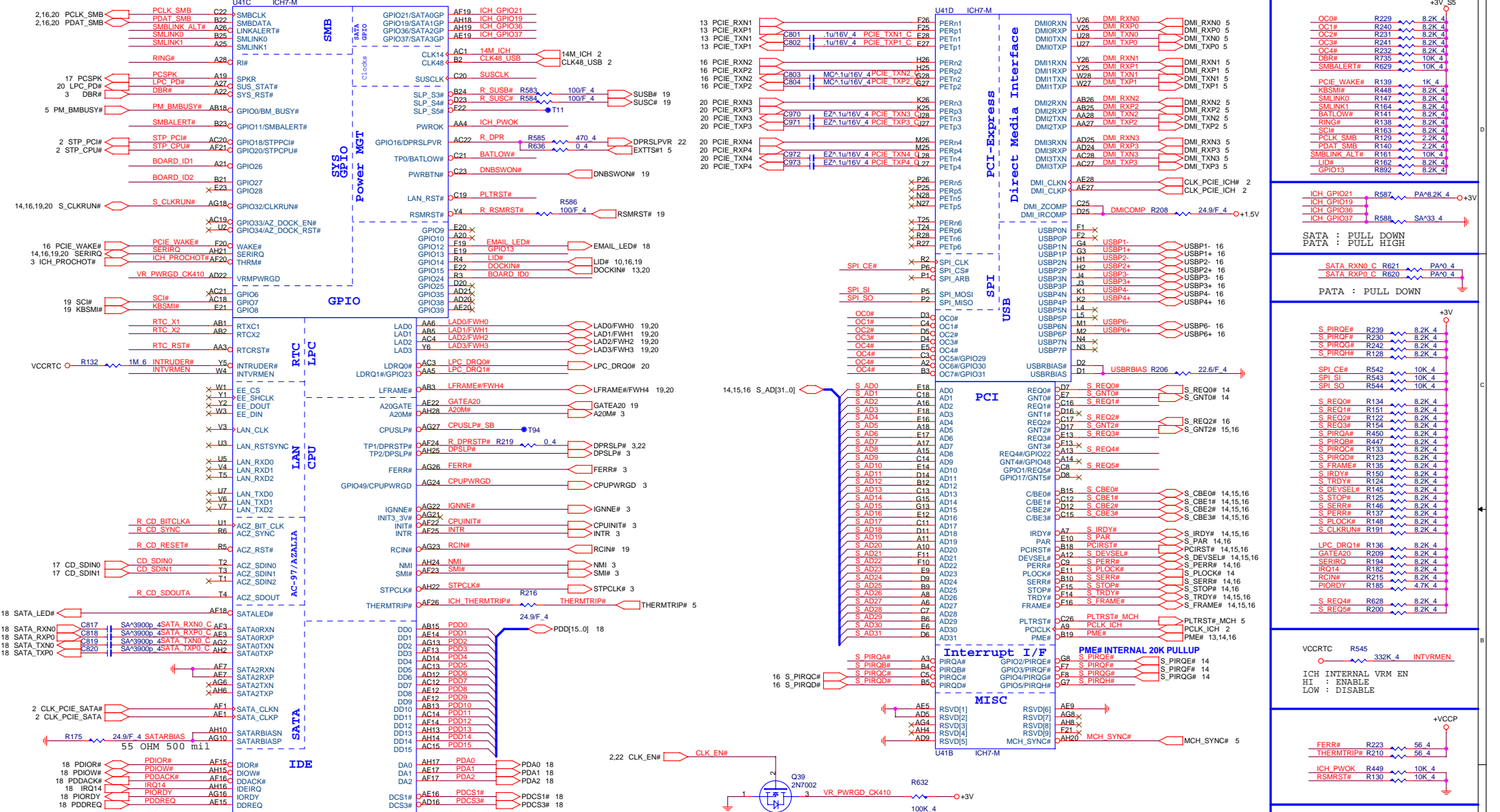


S-VIDEO



CRT

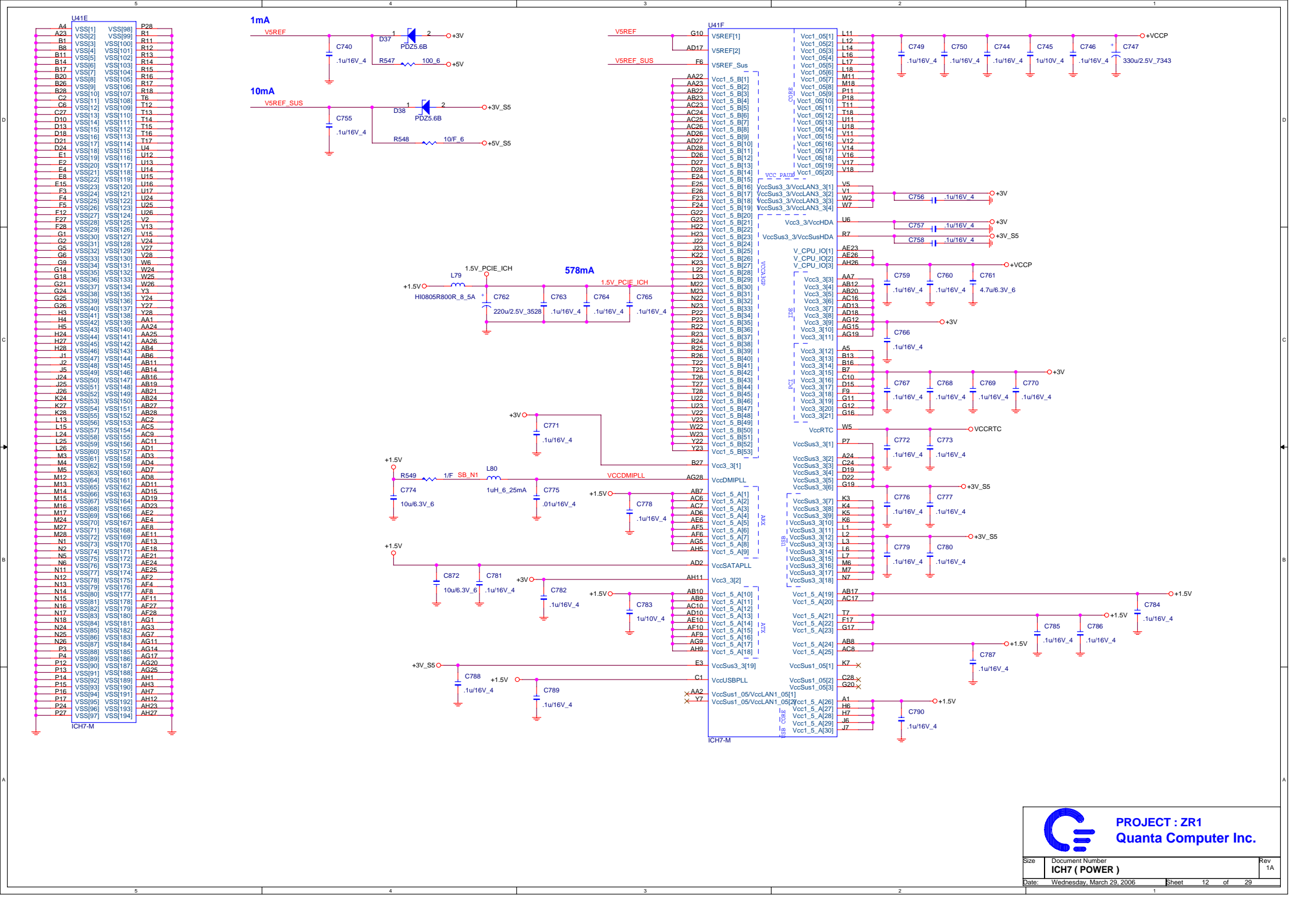




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Quanta Computer Inc.

Size	Document Number	Rev
	ICH7 (CPU/PCIE/IDE/USB)	1A

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1mA

10mA

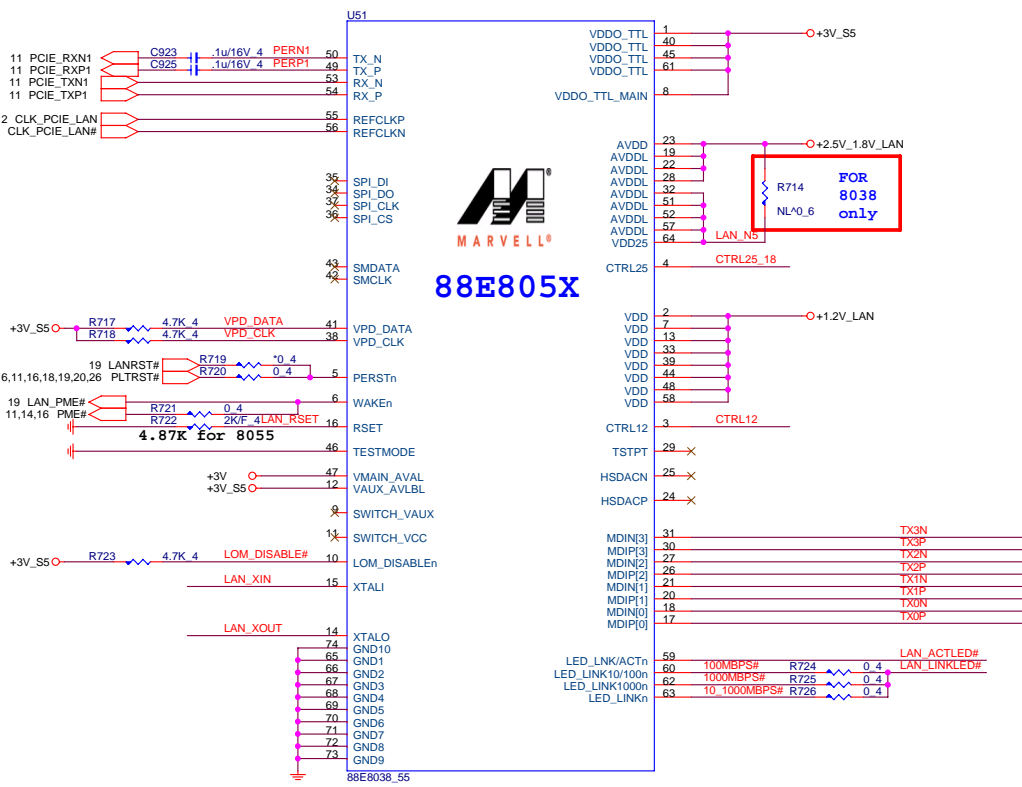
578mA

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Quanta Computer Inc.

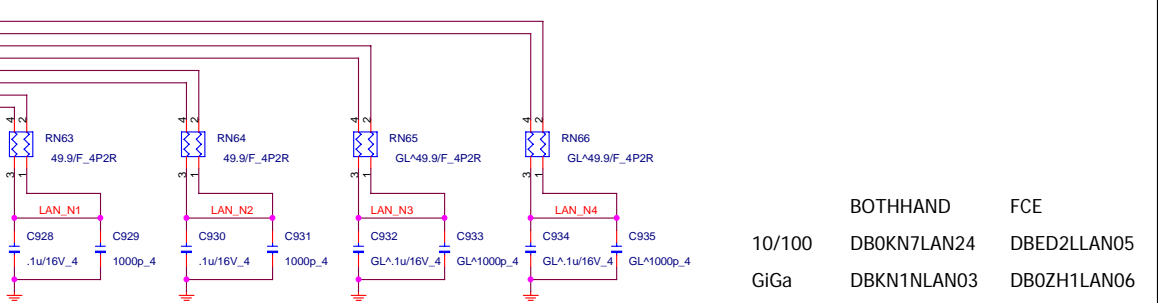
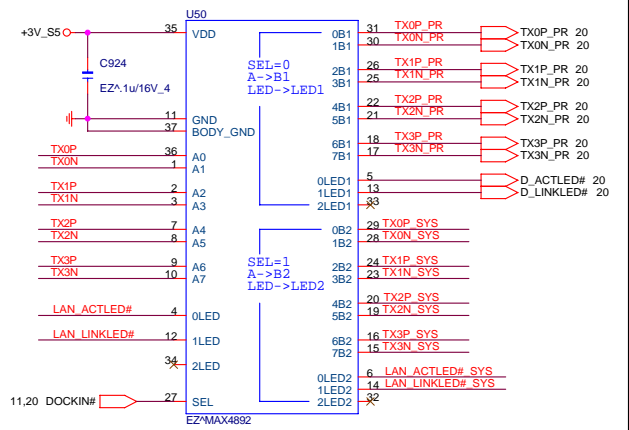
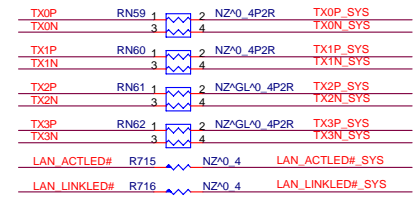
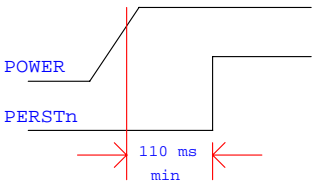
Size	Document Number	Rev
	ICH7 (POWER)	1A
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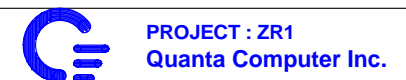
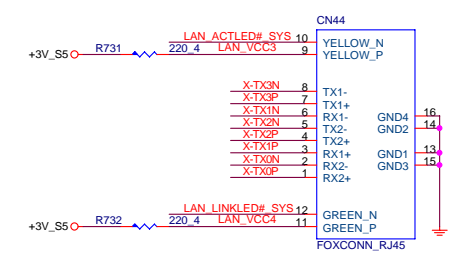
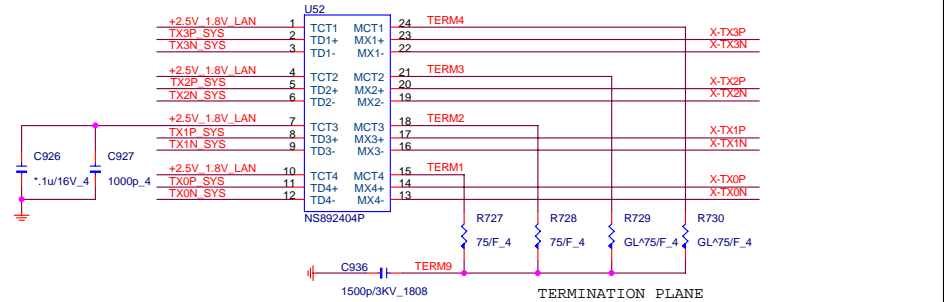
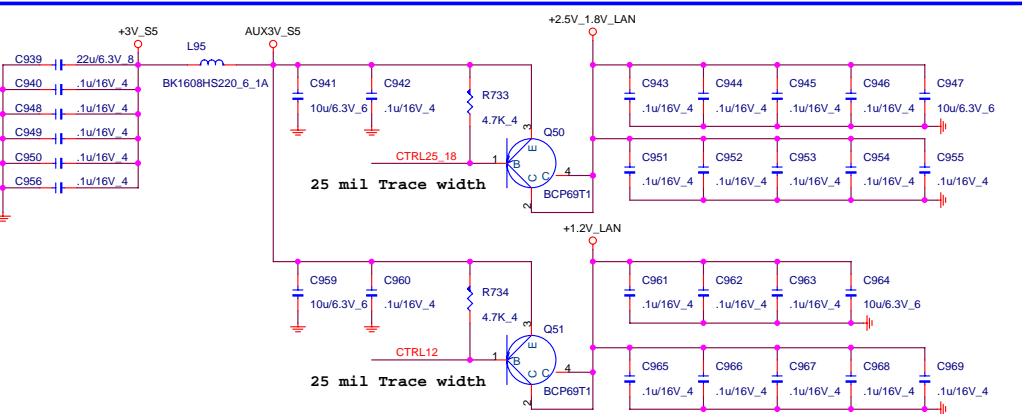
88E805X



RESET TIMING

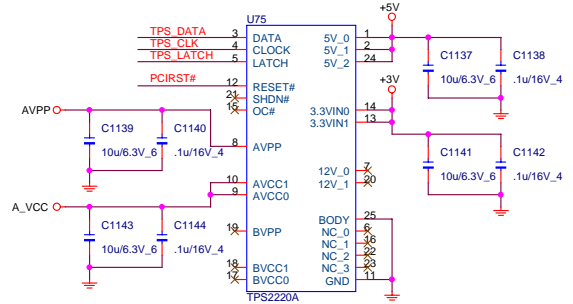
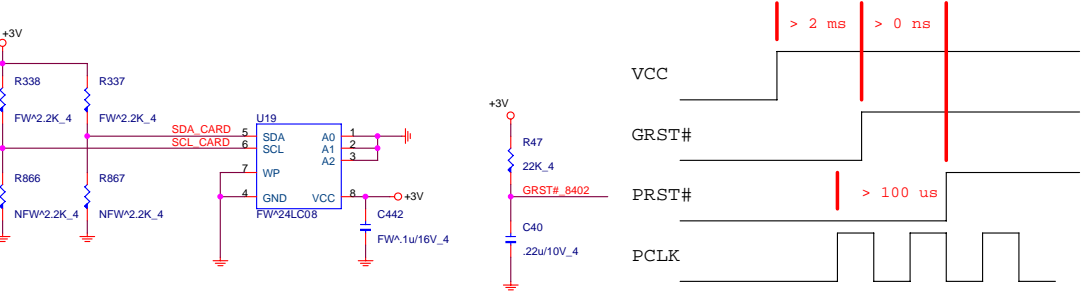
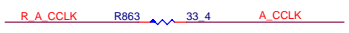
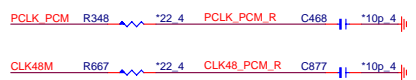
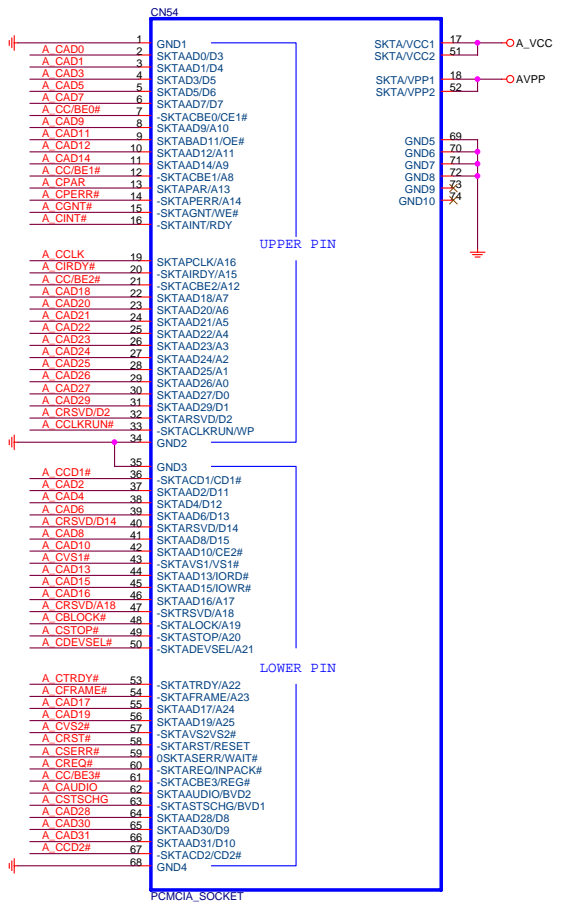
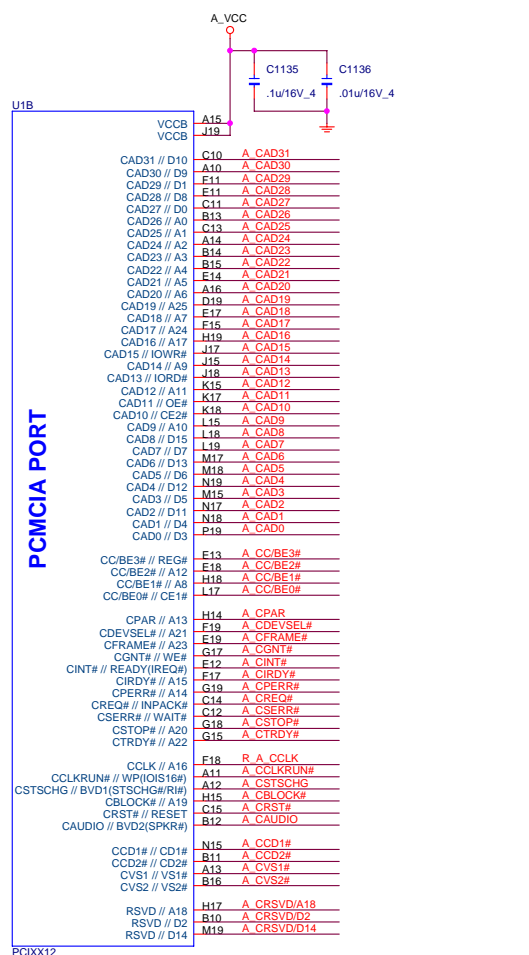
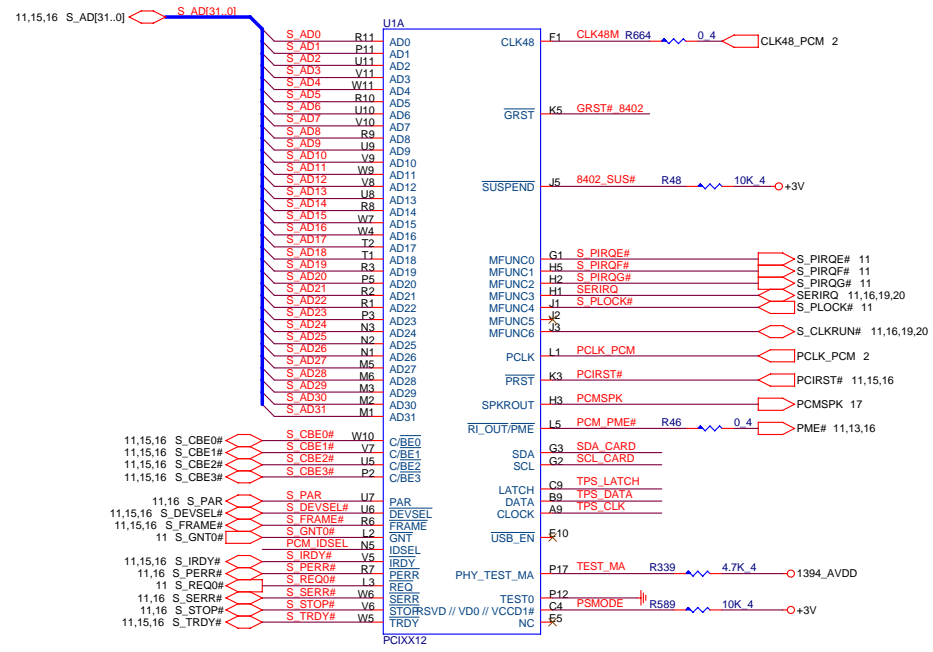
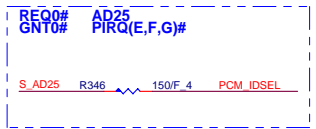


BOTHAND FCE
10/100 DB0KN7LAN24 DBED2LLAN05
GiGa DBKN1NLAN03 DBOZH1LAN06



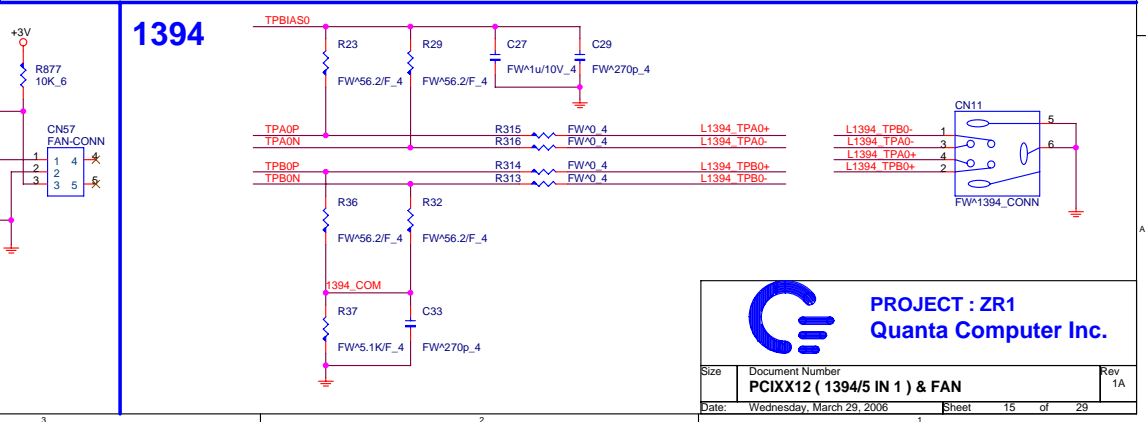
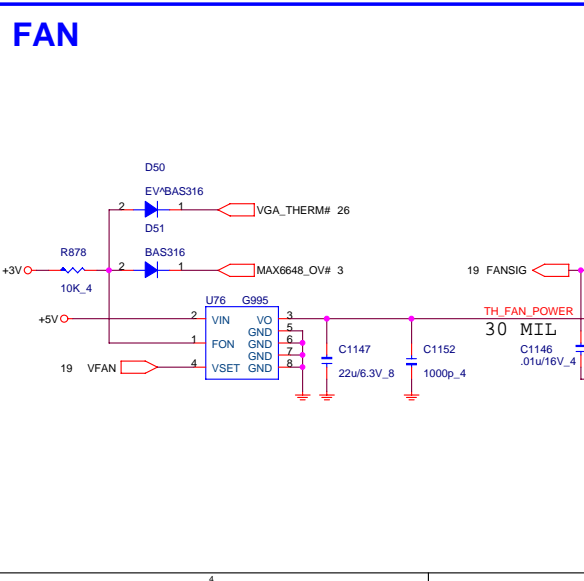
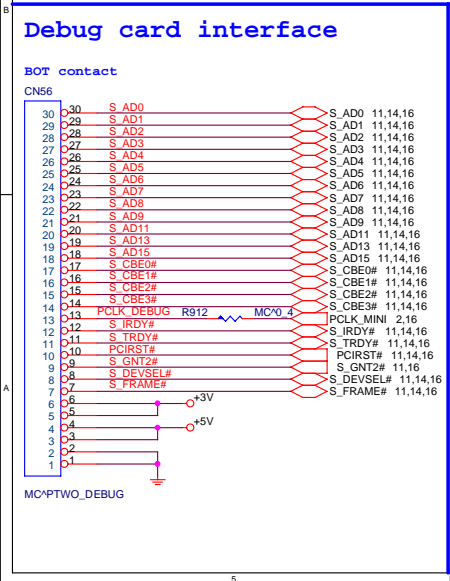
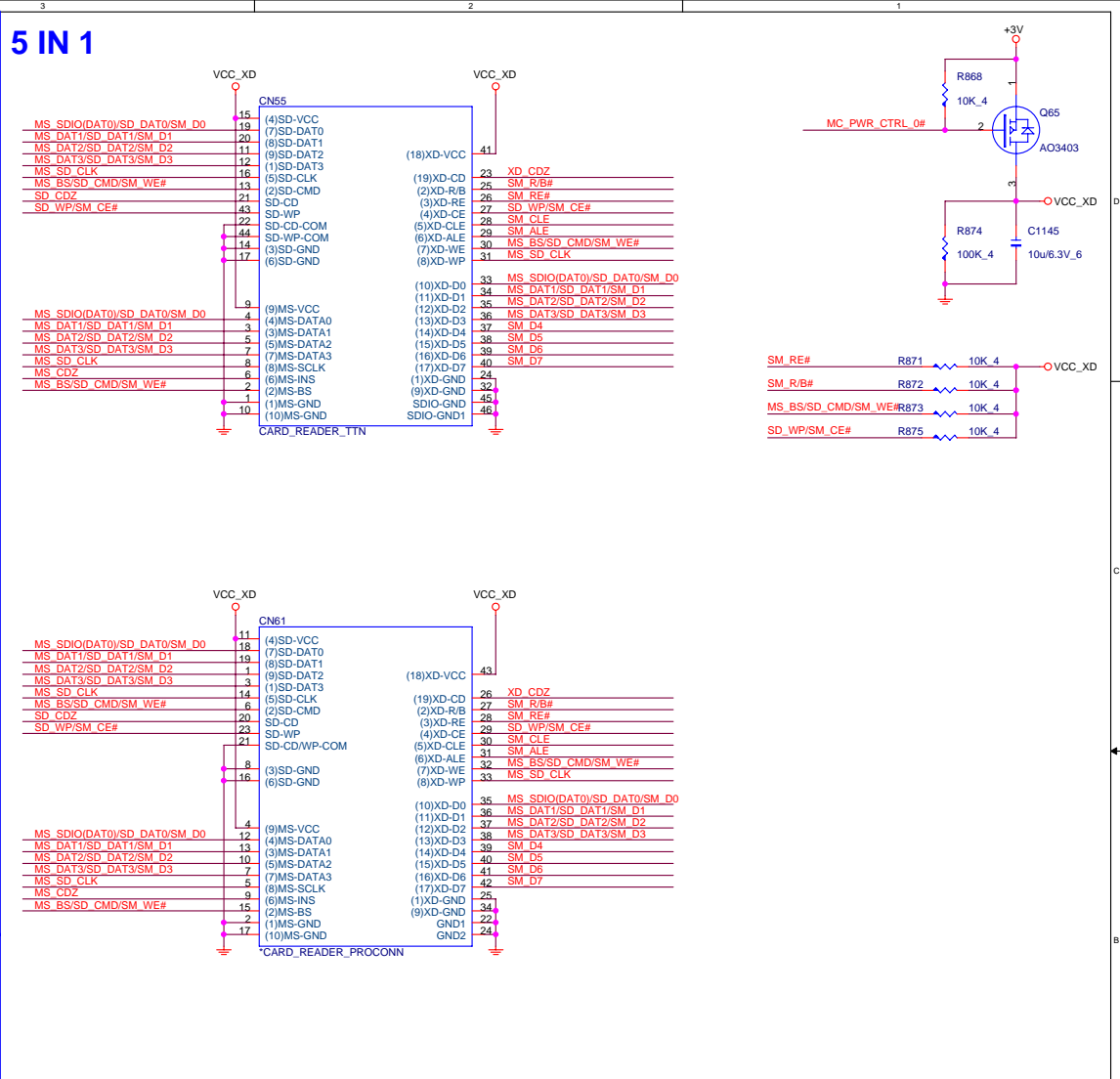
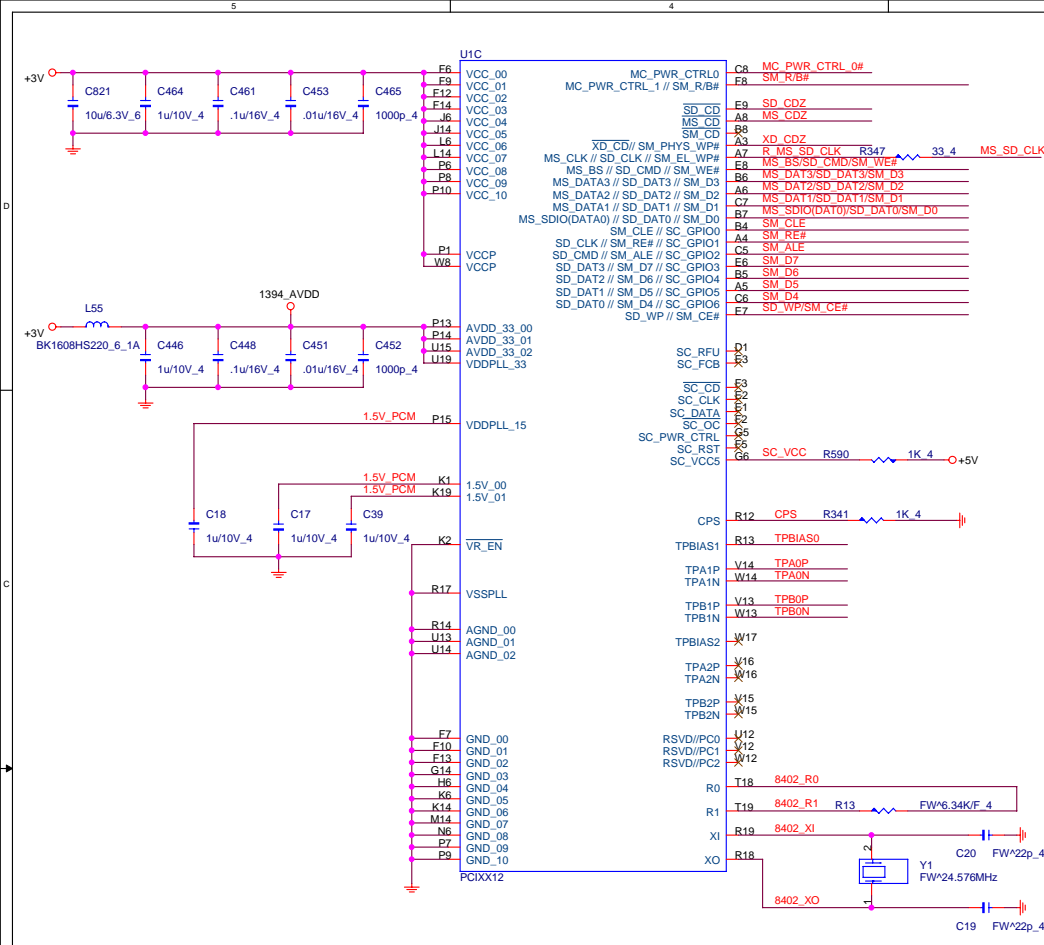
PCIXX12_PCMCIA

PCI8412 : AJ084120T08 PCMCIA / 1394 / 5 IN 1
 PCI6412 : AL064120T04 PCMCIA / 5 IN 1
 PCI1512 : AJ015120T02 PCMCIA

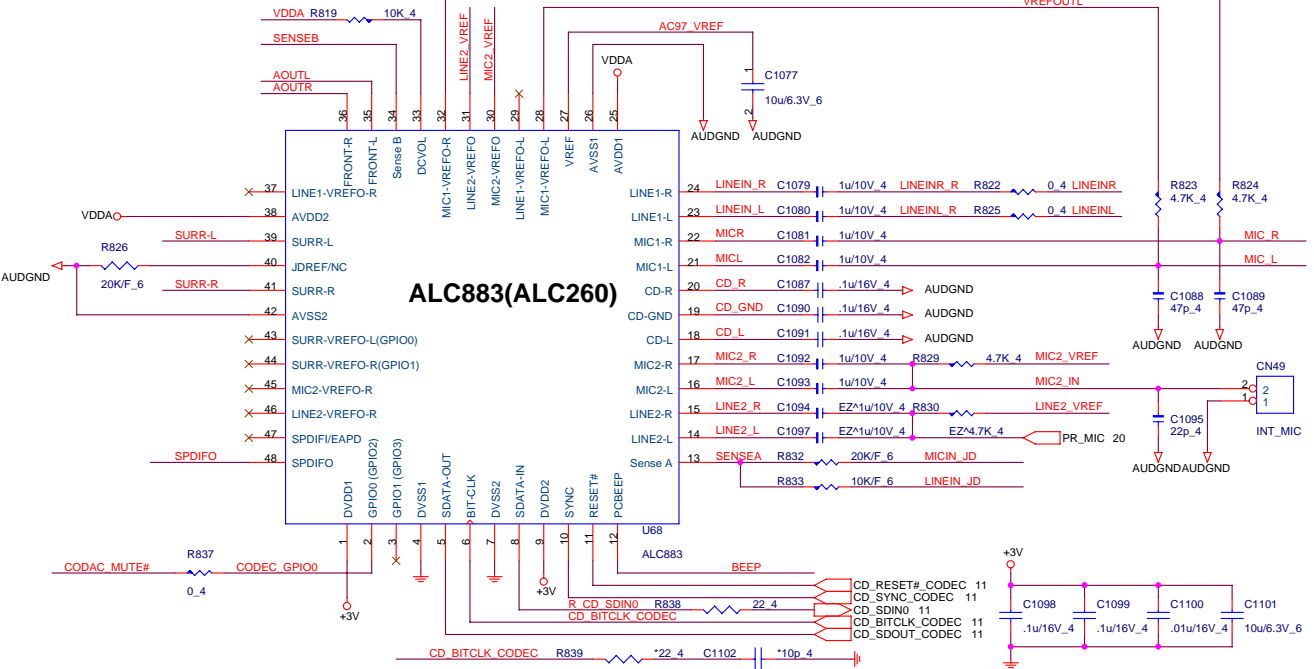


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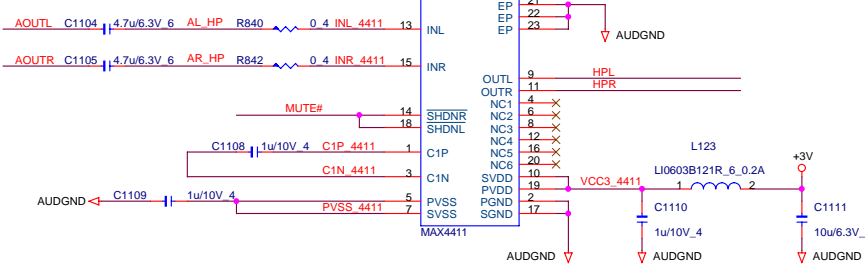
Size	Document Number	Rev
	PCIXX12 (PCMCIA)	1A
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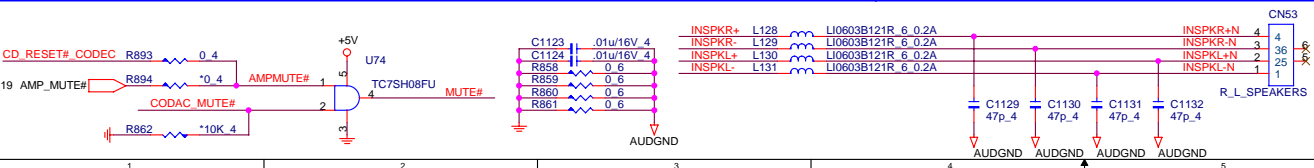
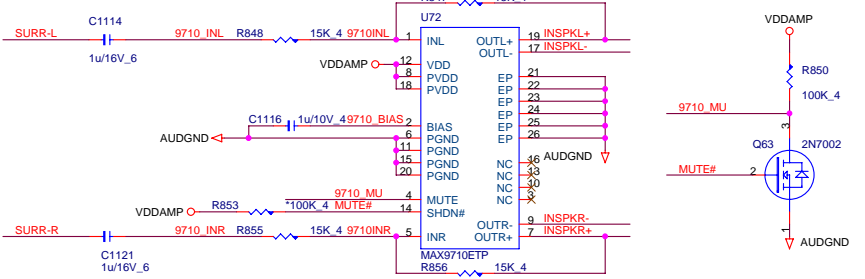
Audio Codec_ALC883



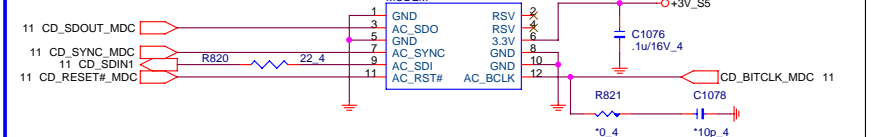
LINE OUT Amplifier



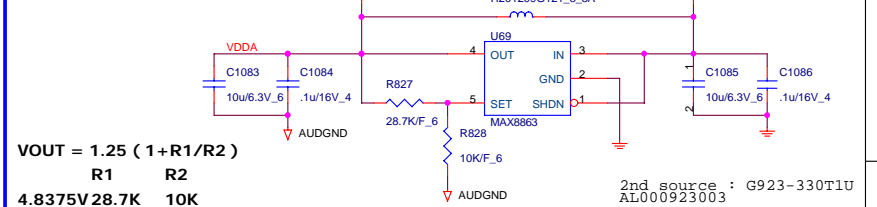
SPEAKER Amplifier



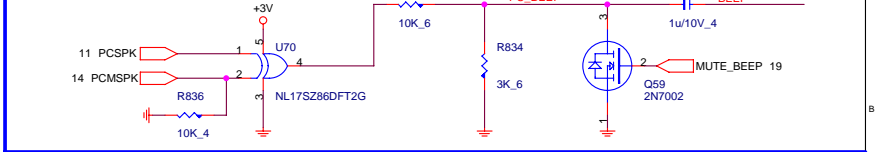
MDC



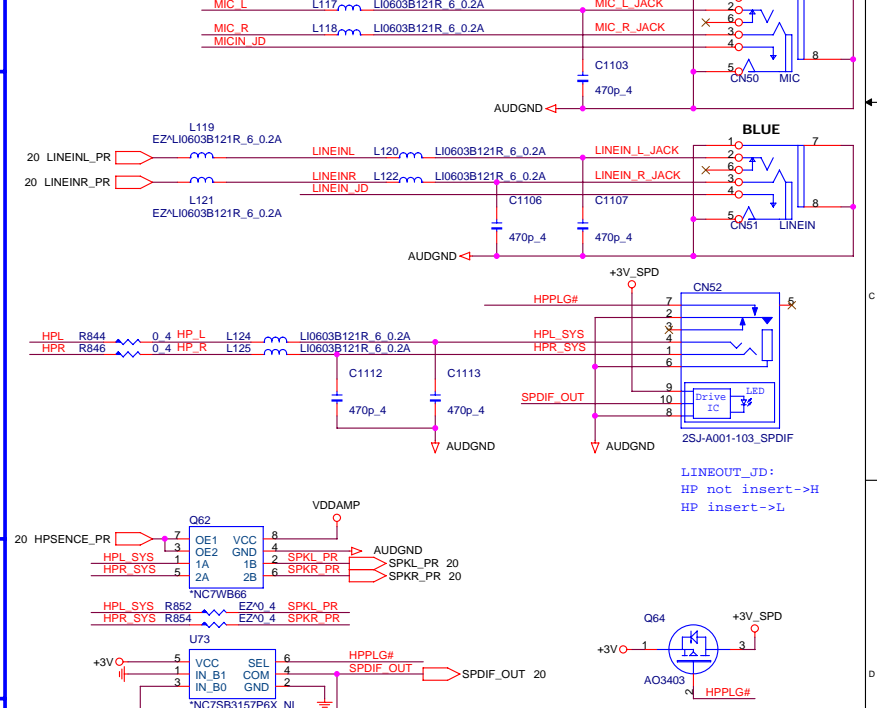
Audio Codec Power



BEEP



Audio Jack

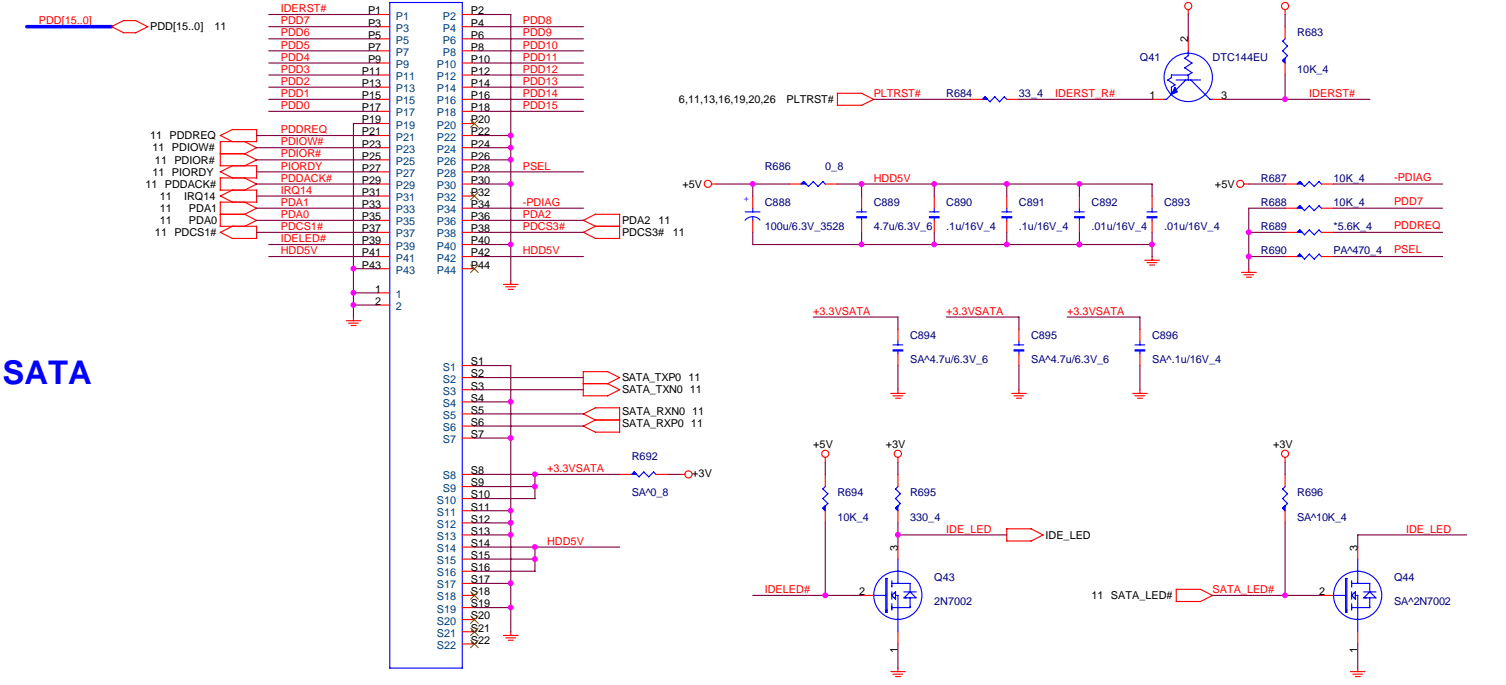


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Quanta Computer Inc.

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Audio Codec (ALC883)
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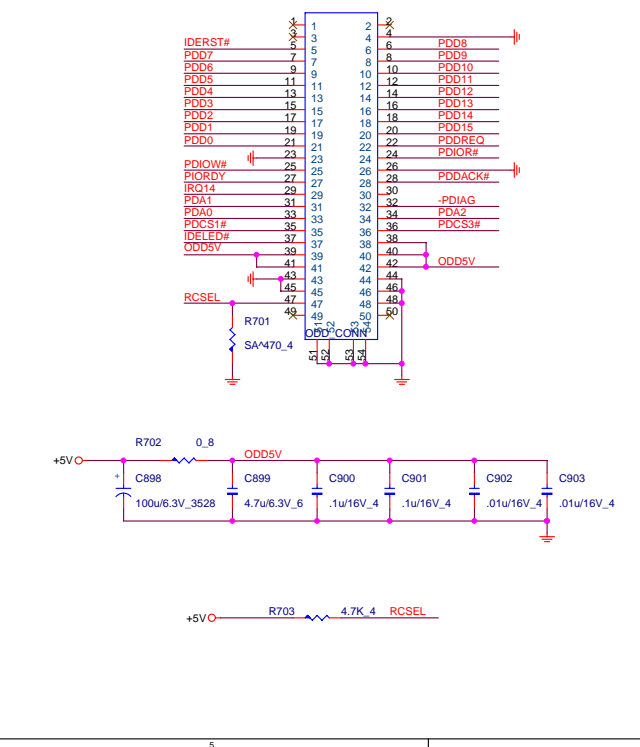
Rev 1A

HDD

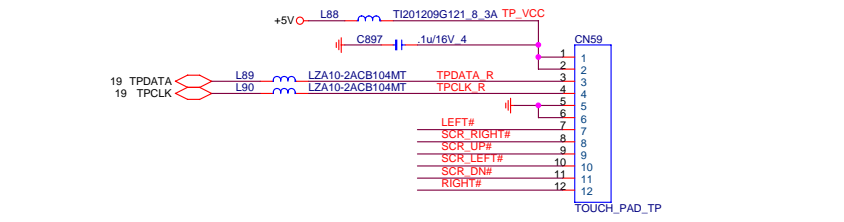


SATA

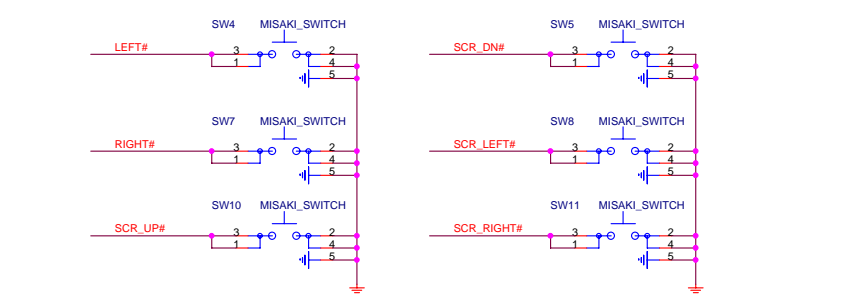
ODD



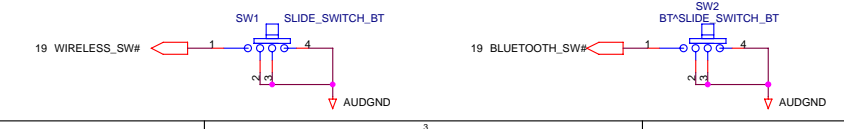
TP CONN



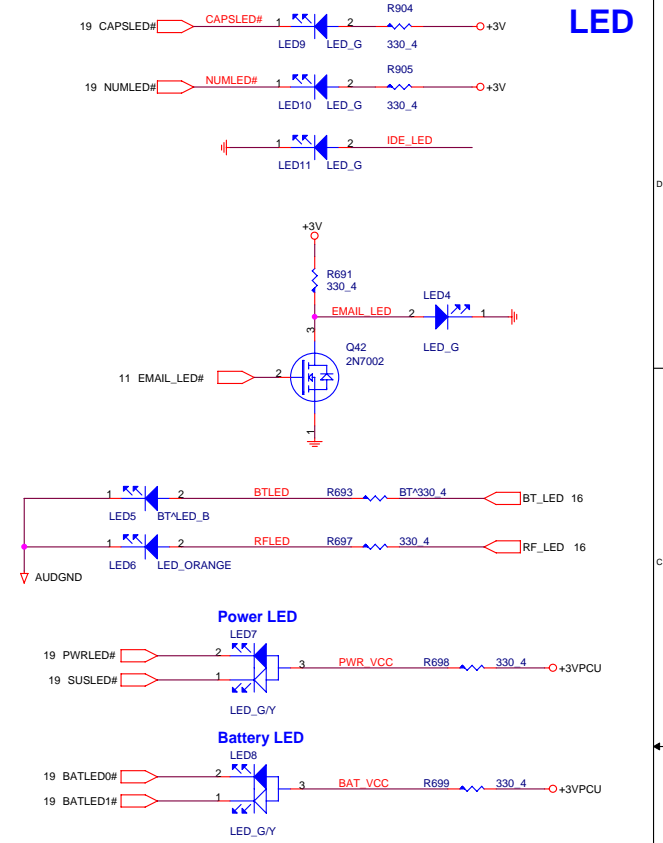
TP SWITCH



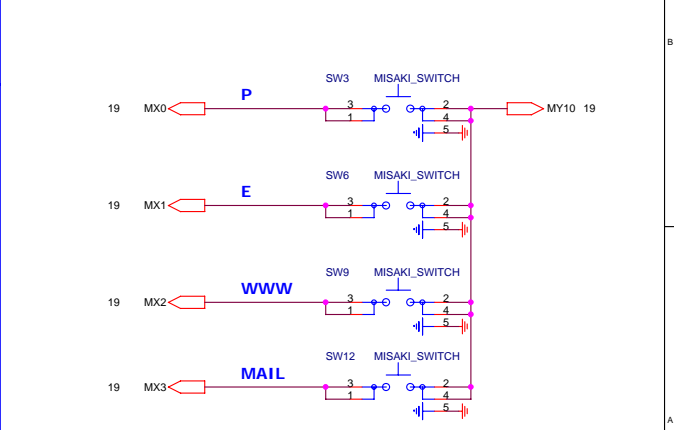
WL & BT SWITCH



LED



QUICK KEY SWITCH

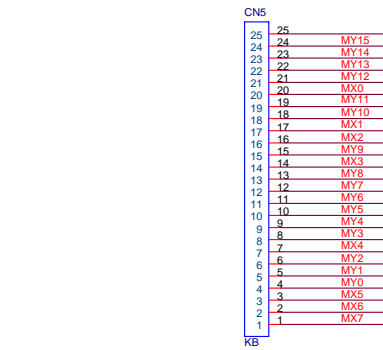
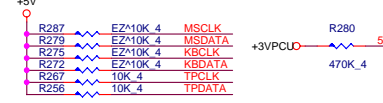
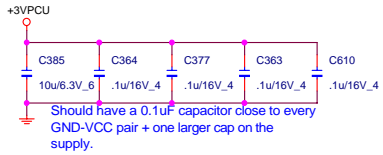


PROJECT : ZR1
Quanta Computer Inc.

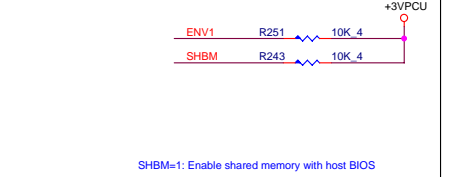
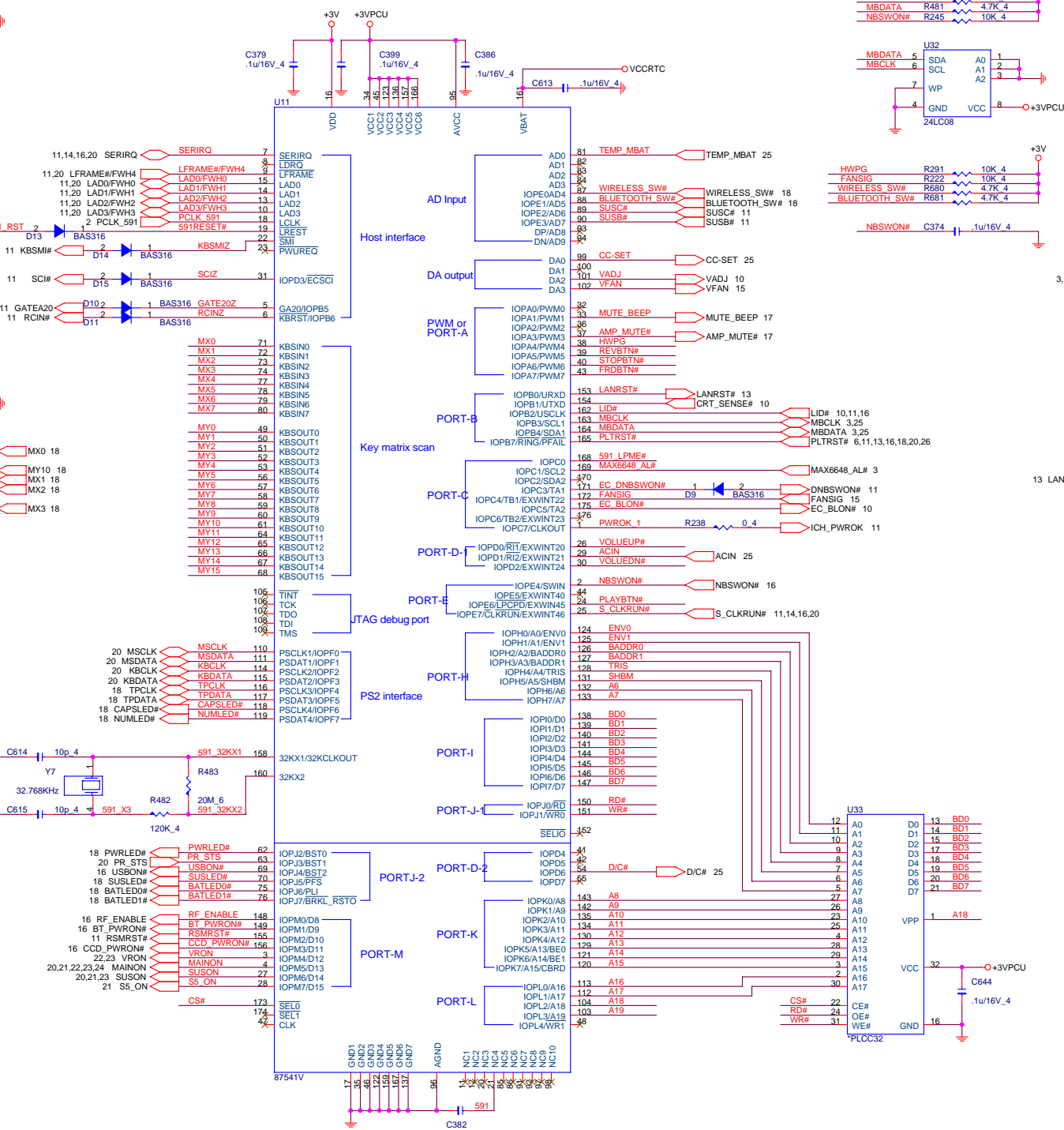
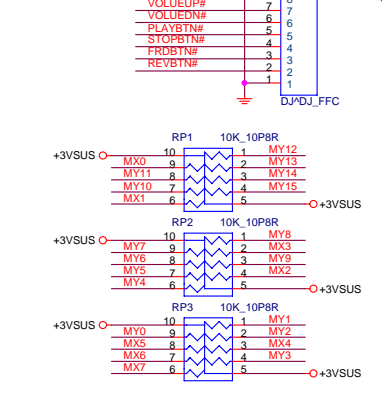
Size	Document Number	Rev
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K/B CONTROLLER

PCLK_591 R270 *22 4 PCLK_591 R C380 *10p_4



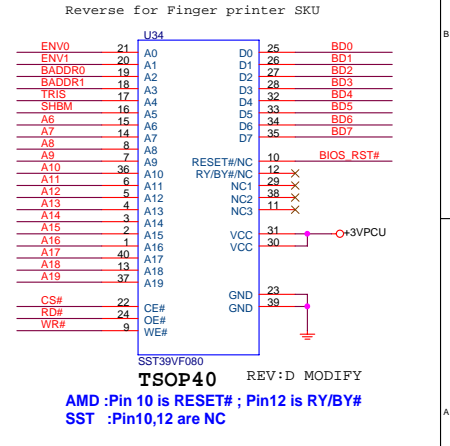
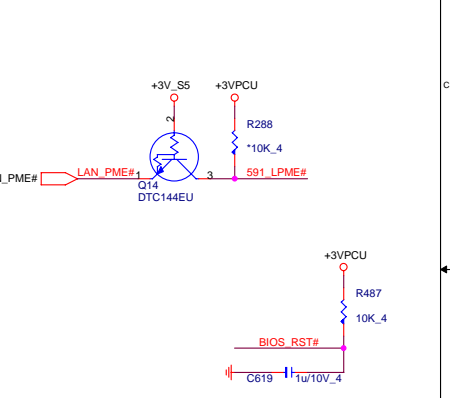
AUDIO DJ



SMBus=1: Enable shared memory with host BIOS

I/O Address		
BAADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	HCFGBAH, HCFGBAL	HCFGBAH, HCFGBAL
1 1	Reserved	Reserved

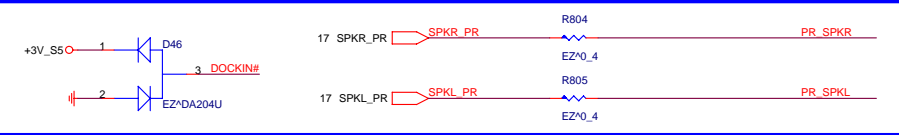
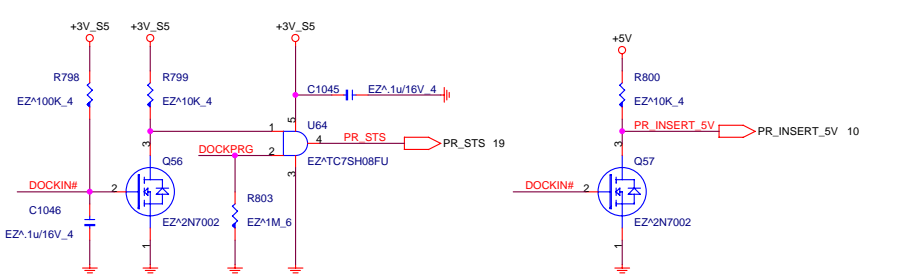
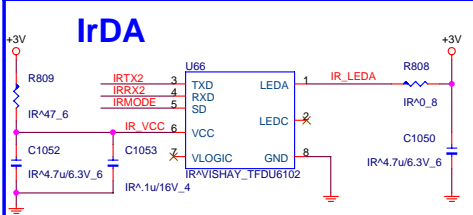
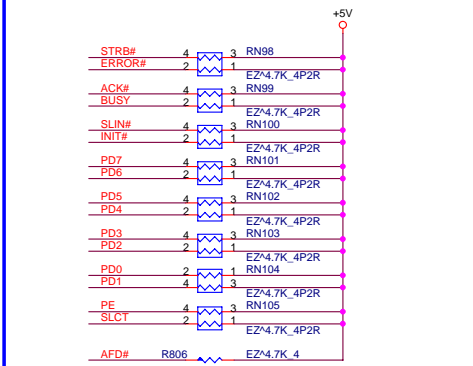
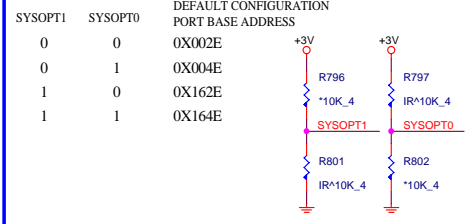
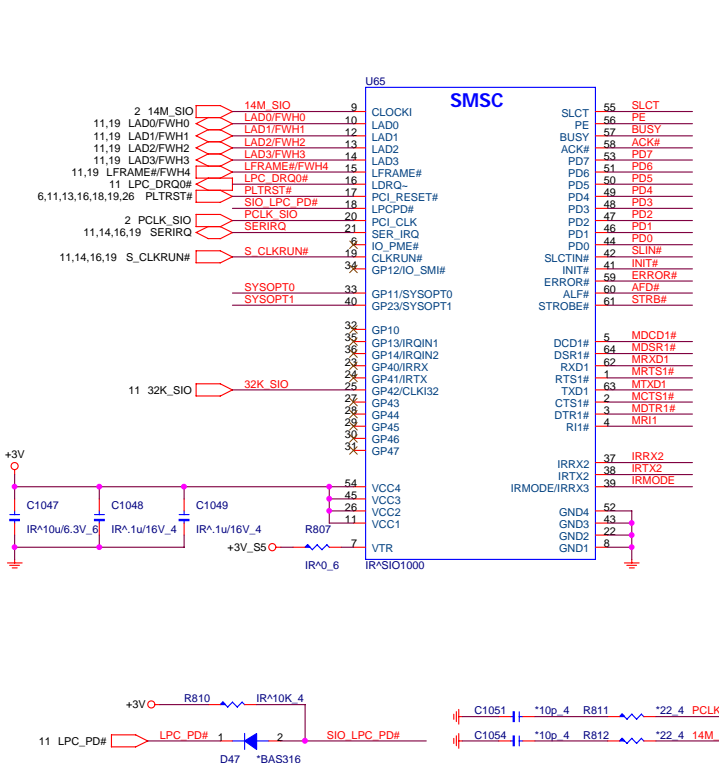
Pin connections for HWPG_CPUIO, HWPG_SYS, HWPG_DDR, IMVP_PWRGD, and VGA_PWRGD.



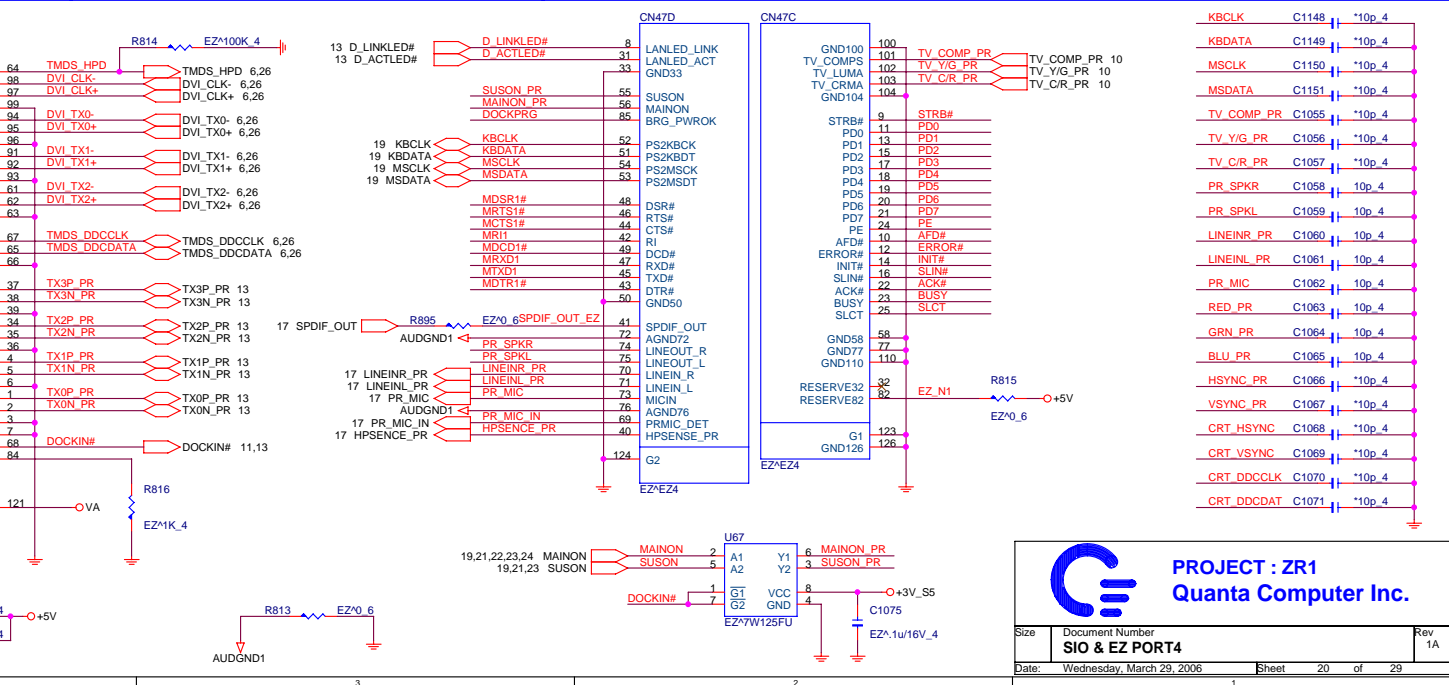
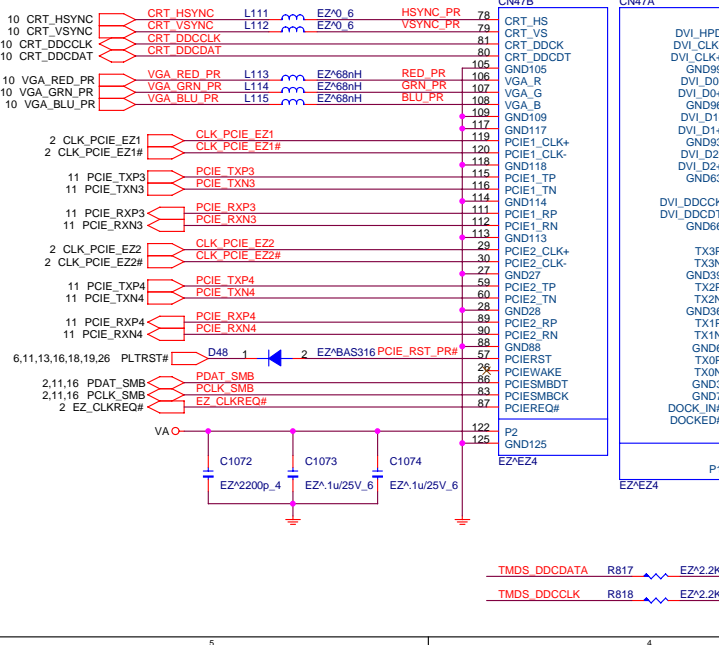
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	EC PC87541V	1A
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SMSC SIO1000



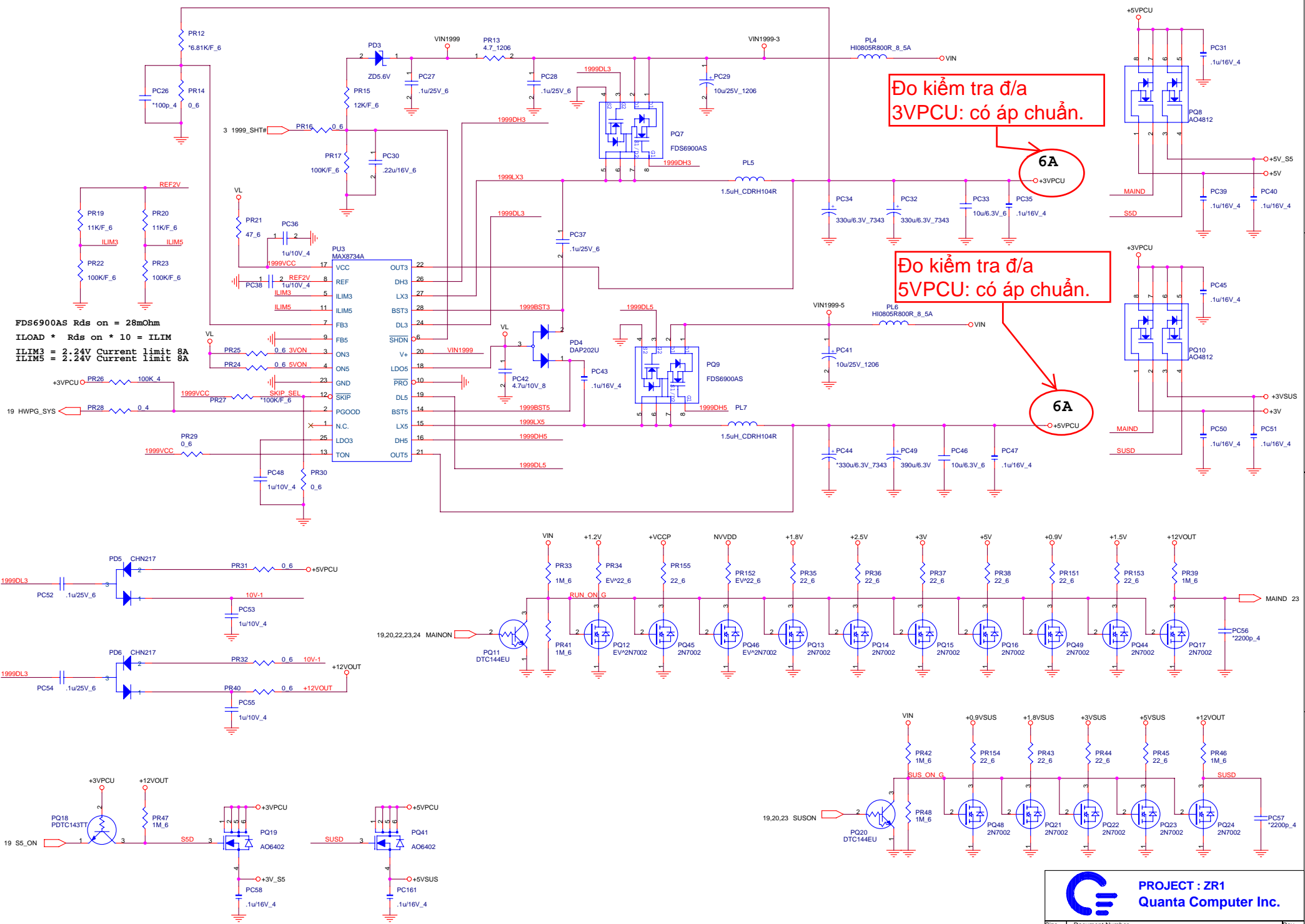
EZ4





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	SIO & EZ PORT4	1A
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FDS6900AS Rds on = 28mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM3 = 2.24V Current limit 8A
 ILIM5 = 2.24V Current limit 8A

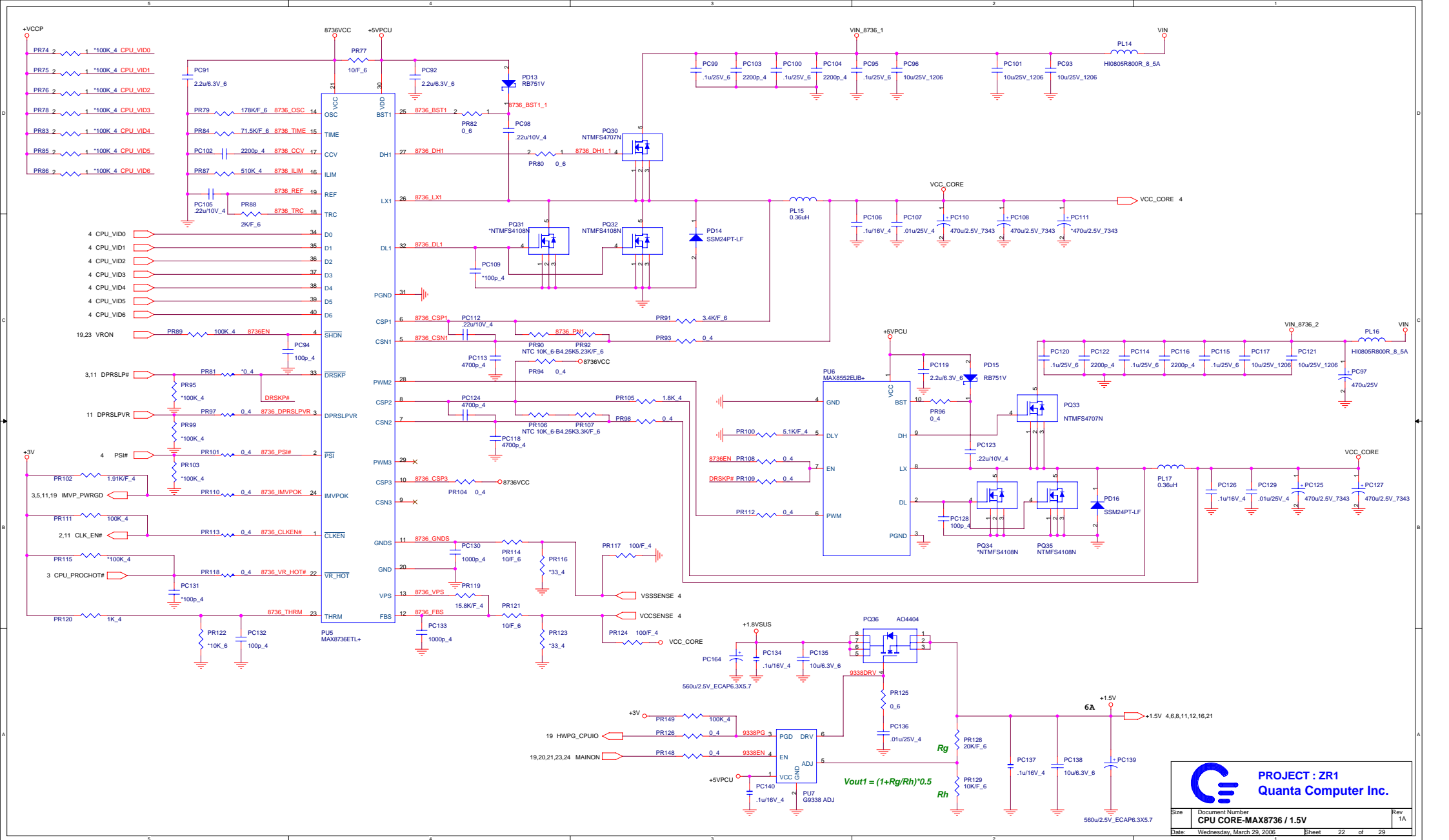
Đo kiểm tra đ/a
 3VPCU: có áp chuẩn.

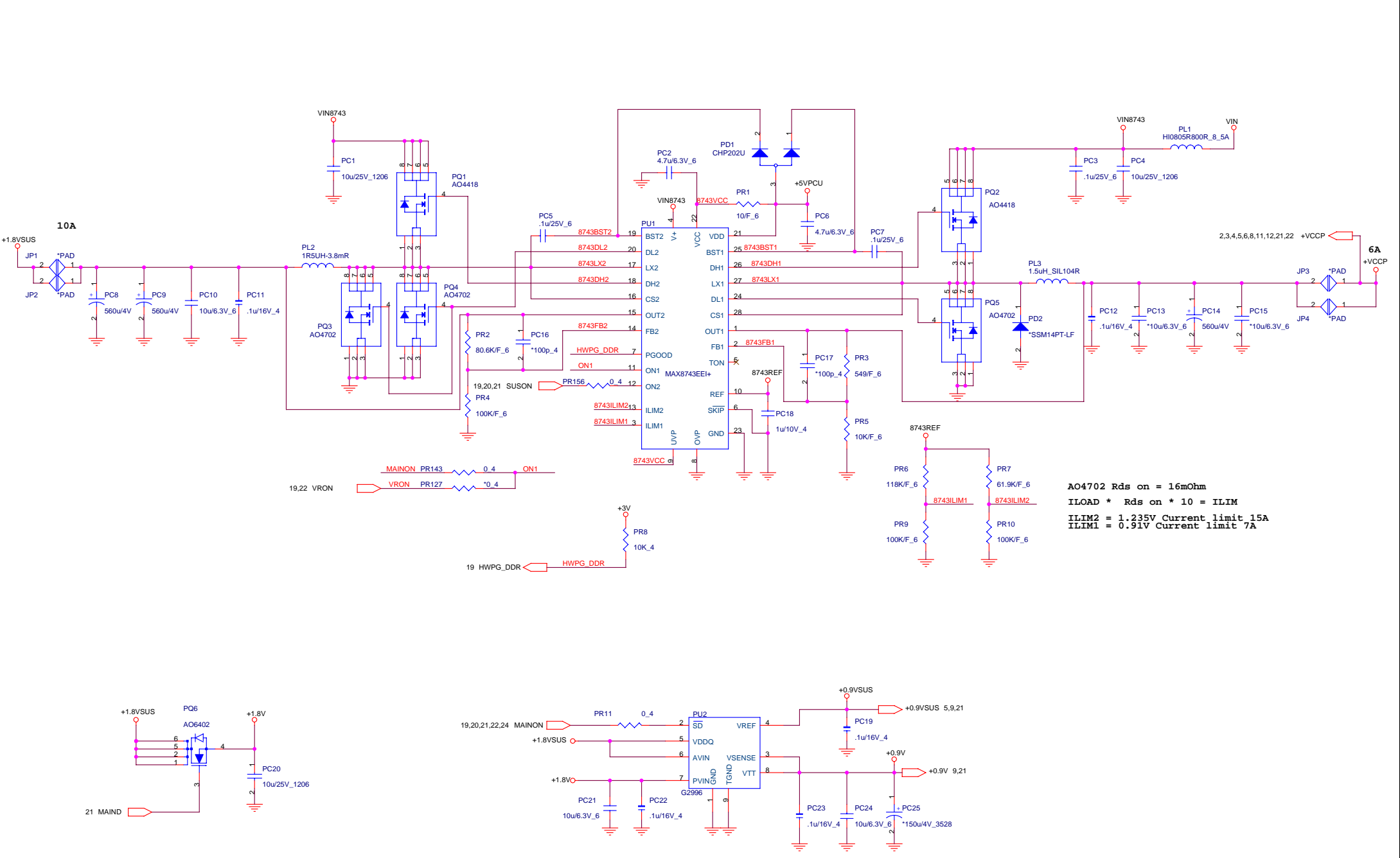
6A

Đo kiểm tra đ/a
 5VPCU: có áp chuẩn.


6A

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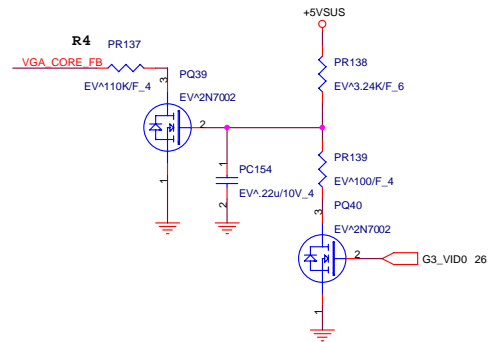
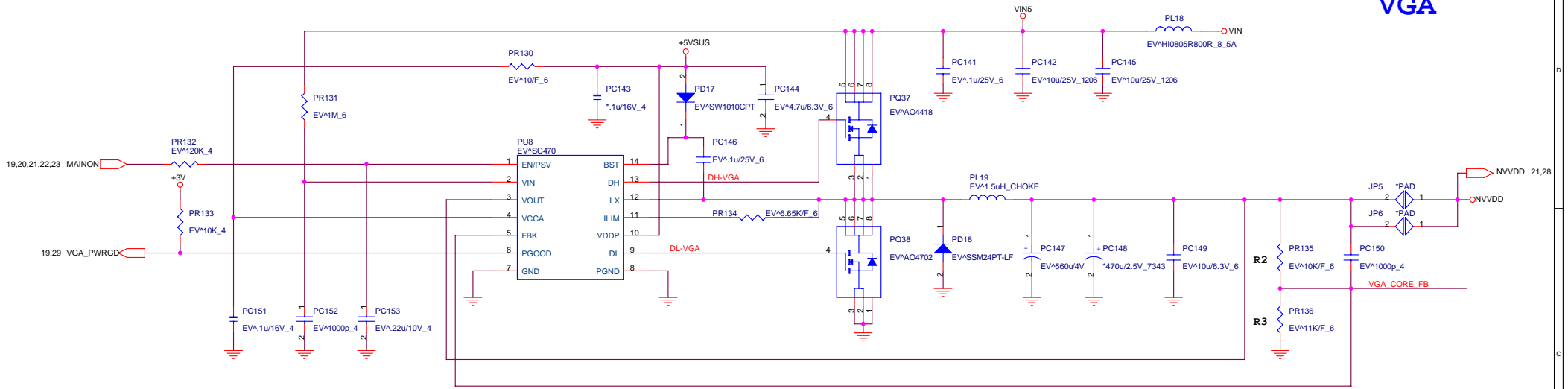




AO4702 $R_{ds\ on} = 16m\Omega$
ILOAD * $R_{ds\ on}$ * 10 = **ILIM**
ILIM2 = 1.235V Current limit 15A
ILIM1 = 0.91V Current limit 7A

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	1.8VSUS / +VCCP / 0.9V	1A
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VGA



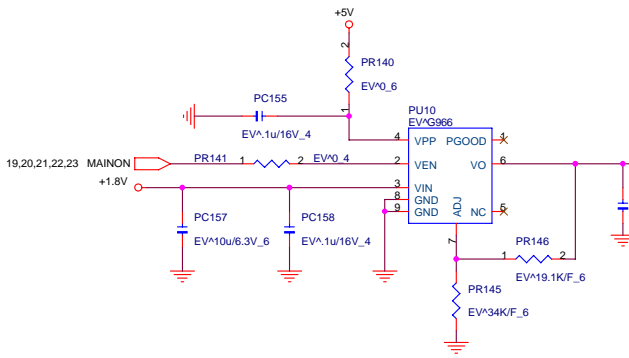
$HI \rightarrow VOUT = (1 + R2/R3) * 0.5$
 $LO \rightarrow VOUT = (1 + R2 / (R3 // R4)) * 0.5$

M52P (G)
 PR1 : 10K
 PR4 : 11K
 PR2 : 110K

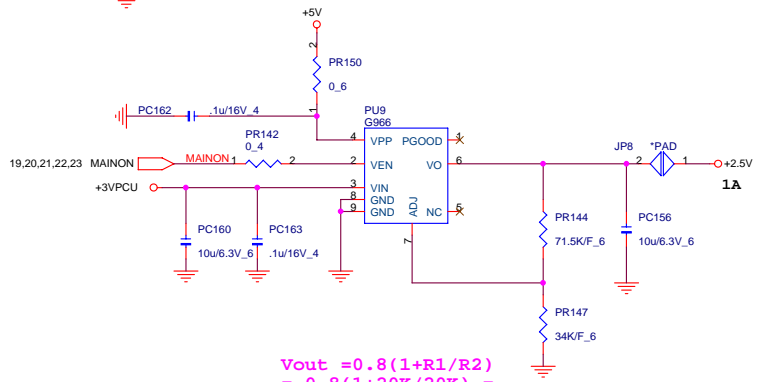
M54P
 PR1 : 12K
 PR4 : 12K
 PR2 : 60.4K

Power Play Mode

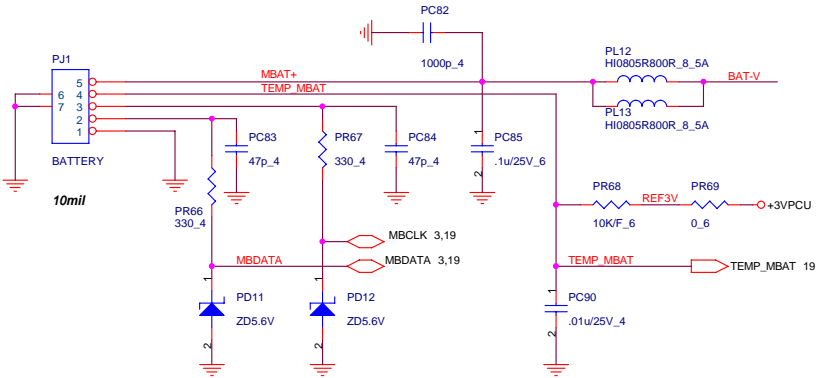
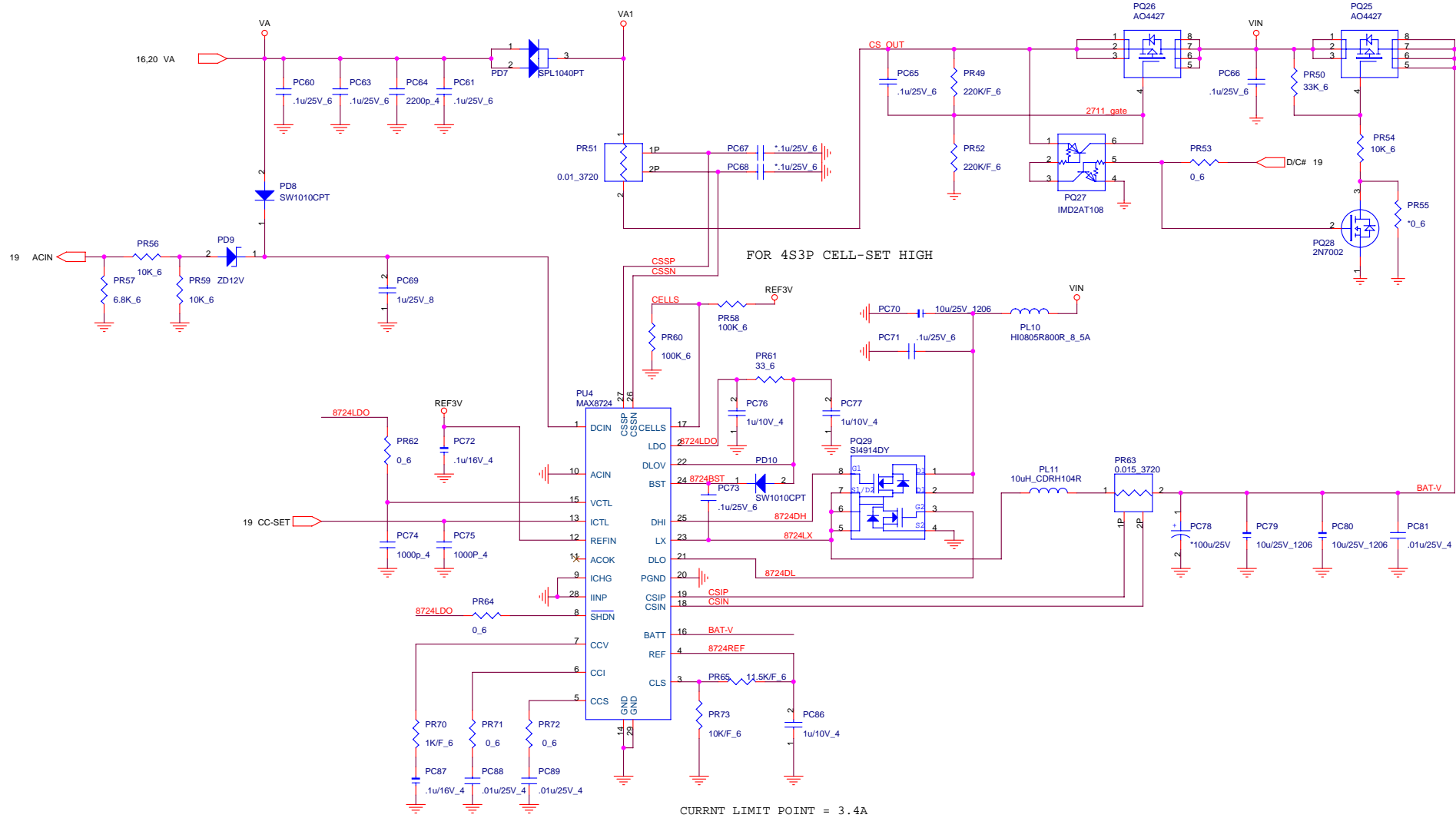
VGA_PWR_SW	VGA_CORE
HI	0.95V--M52P (G) 1.0V --M54P
Default LO	1.0V--M52P (G) 1.1V--M54P



$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 1.2V$

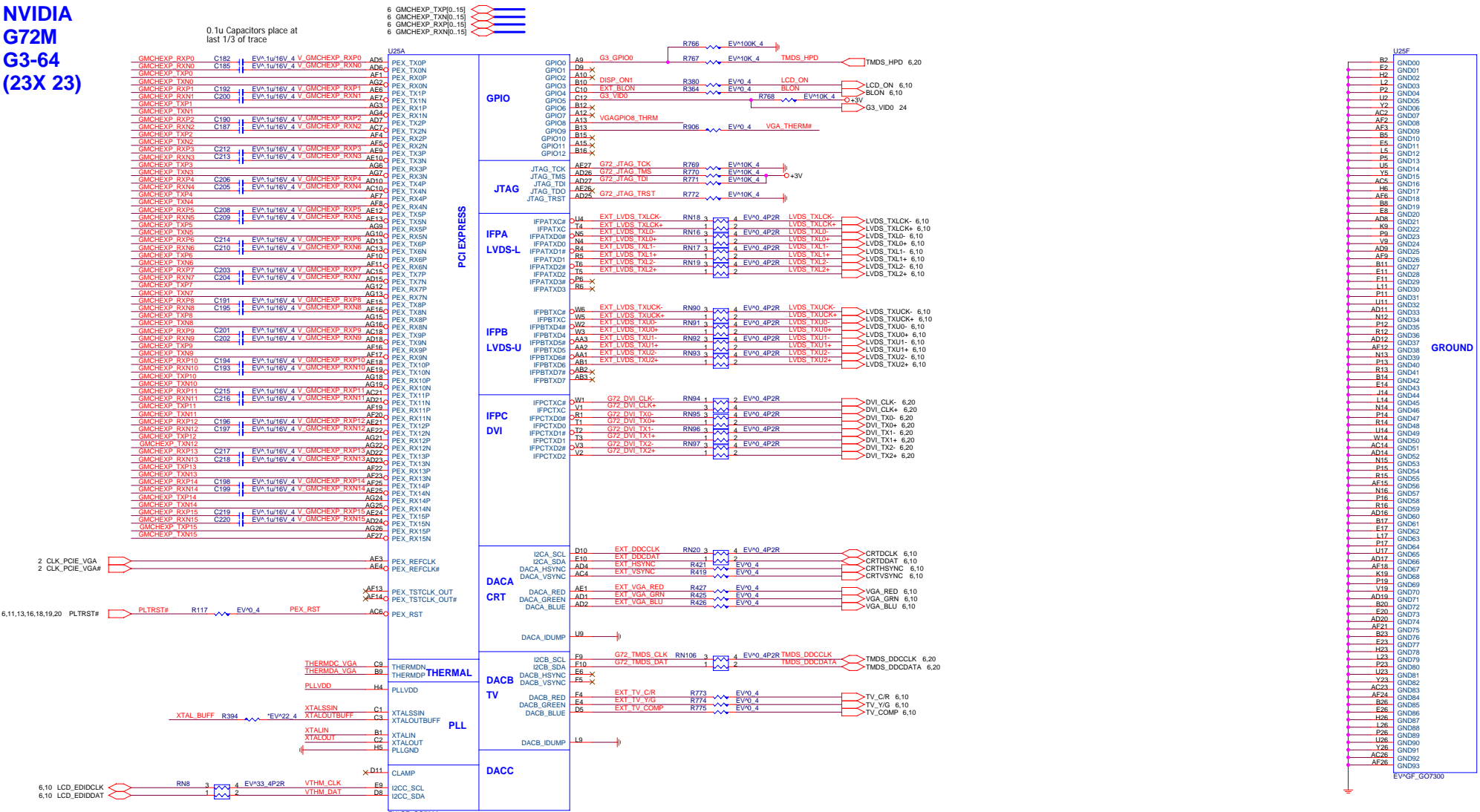


$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 2.5V$



NVIDIA G72M G3-64 (23X 23)

0.1u Capacitors place at last 1/3 of trace



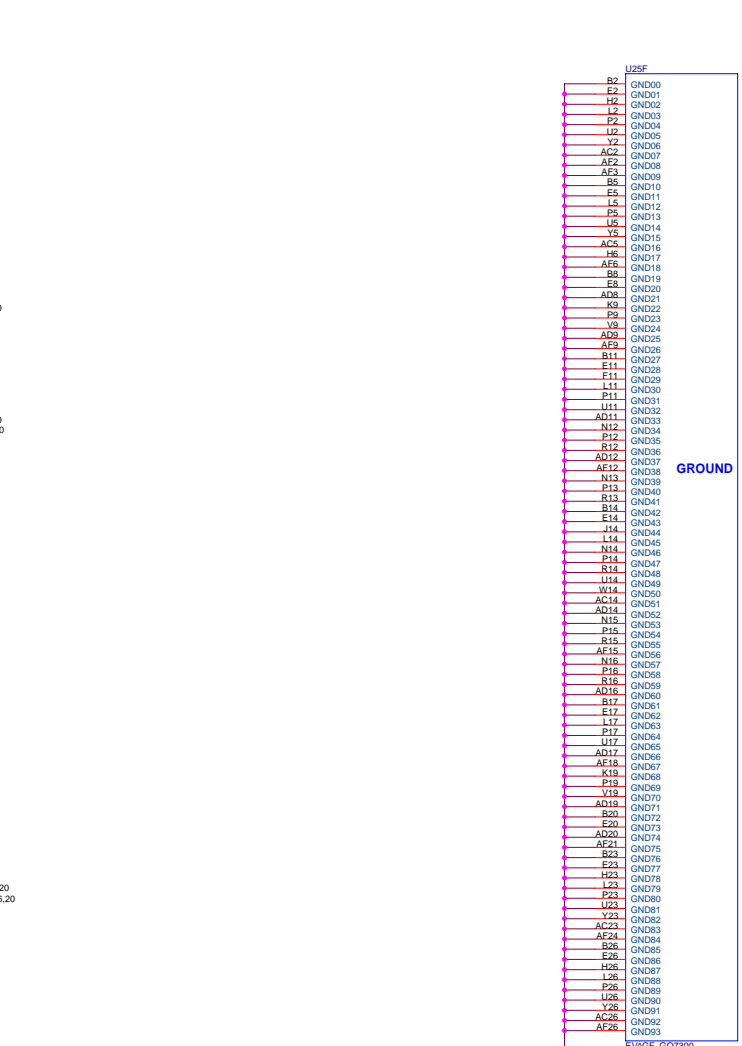
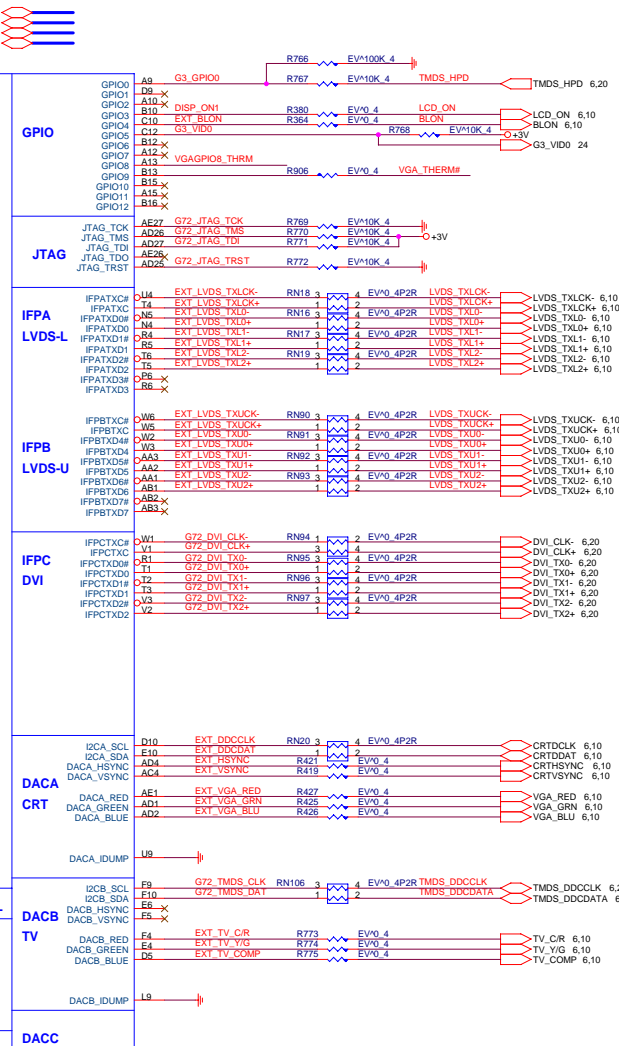
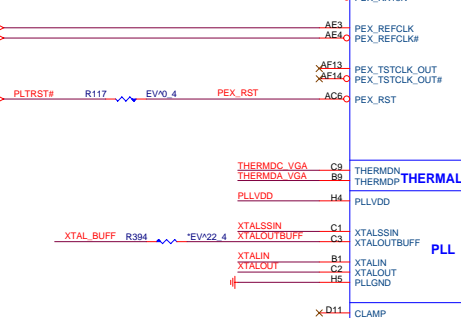
2 CLK_PCIE_VGA
2 CLK_PCIE_VGA#

6.11,13,16,18,19,20 PLTRST#

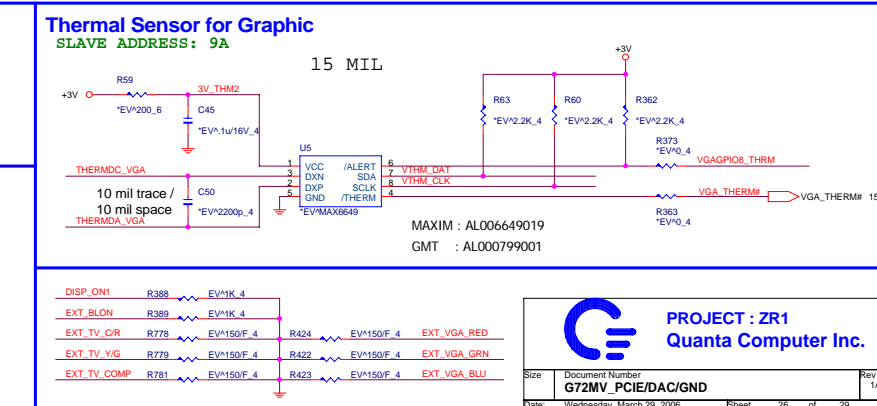
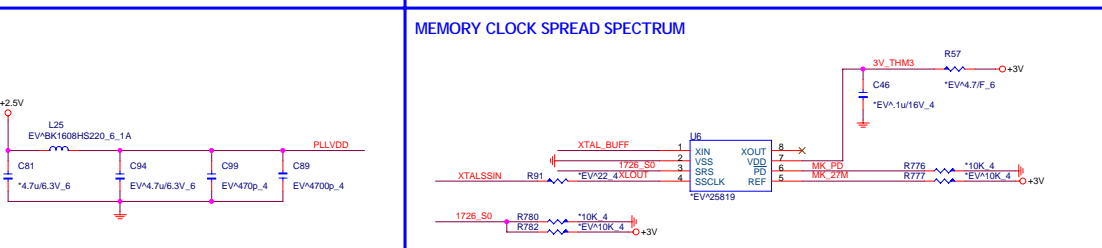
6.10 LCD_EDIDCLK
6.10 LCD_EDIDDAT

U25A

GMCEXP_RXP0	C182	EVA:1u16V_4 V	GMCEXP_RXP0	AE3	PEX_TX0P
GMCEXP_RXN0	C185	EVA:1u16V_4 V	GMCEXP_RXN0	AE4	PEX_TX0N
GMCEXP_TXP0	AE1			AGC0	PEX_RX0P
GMCEXP_TXN0	AGC0			AE7	PEX_RX0N
GMCEXP_RXP1	C192	EVA:1u16V_4 V	GMCEXP_RXP1	AE7	PEX_TX1P
GMCEXP_RXN1	C200	EVA:1u16V_4 V	GMCEXP_RXN1	AE7	PEX_TX1N
GMCEXP_TXP1	AG4			AE7	PEX_RX1P
GMCEXP_TXN1	AG4			AE7	PEX_RX1N
GMCEXP_RXP2	C190	EVA:1u16V_4 V	GMCEXP_RXP2	AD7	PEX_TX2P
GMCEXP_RXN2	C187	EVA:1u16V_4 V	GMCEXP_RXN2	AD7	PEX_TX2N
GMCEXP_TXP2	AF4			AE7	PEX_RX2P
GMCEXP_TXN2	AF4			AE7	PEX_RX2N
GMCEXP_RXP3	C212	EVA:1u16V_4 V	GMCEXP_RXP3	AE7	PEX_TX3P
GMCEXP_RXN3	C213	EVA:1u16V_4 V	GMCEXP_RXN3	AE7	PEX_TX3N
GMCEXP_TXP3	AG6			AE7	PEX_RX3P
GMCEXP_TXN3	AG6			AE7	PEX_RX3N
GMCEXP_RXP4	C206	EVA:1u16V_4 V	GMCEXP_RXP4	AD10	PEX_TX4P
GMCEXP_RXN4	C205	EVA:1u16V_4 V	GMCEXP_RXN4	AD10	PEX_TX4N
GMCEXP_TXP4	AF7			AE7	PEX_RX4P
GMCEXP_TXN4	AF7			AE7	PEX_RX4N
GMCEXP_RXP5	C208	EVA:1u16V_4 V	GMCEXP_RXP5	AE10	PEX_TX5P
GMCEXP_RXN5	C209	EVA:1u16V_4 V	GMCEXP_RXN5	AE10	PEX_TX5N
GMCEXP_TXP5	AG9			AE7	PEX_RX5P
GMCEXP_TXN5	AG9			AE7	PEX_RX5N
GMCEXP_RXP6	C214	EVA:1u16V_4 V	GMCEXP_RXP6	AE10	PEX_TX6P
GMCEXP_RXN6	C210	EVA:1u16V_4 V	GMCEXP_RXN6	AE10	PEX_TX6N
GMCEXP_TXP6	AF9			AE7	PEX_RX6P
GMCEXP_TXN6	AF9			AE7	PEX_RX6N
GMCEXP_RXP7	C203	EVA:1u16V_4 V	GMCEXP_RXP7	AE10	PEX_TX7P
GMCEXP_RXN7	C204	EVA:1u16V_4 V	GMCEXP_RXN7	AE10	PEX_TX7N
GMCEXP_TXP7	AG12			AE7	PEX_RX7P
GMCEXP_TXN7	AG12			AE7	PEX_RX7N
GMCEXP_RXP8	C191	EVA:1u16V_4 V	GMCEXP_RXP8	AE10	PEX_TX8P
GMCEXP_RXN8	C195	EVA:1u16V_4 V	GMCEXP_RXN8	AE10	PEX_TX8N
GMCEXP_TXP8	AG10			AE7	PEX_RX8P
GMCEXP_TXN8	AG10			AE7	PEX_RX8N
GMCEXP_RXP9	C201	EVA:1u16V_4 V	GMCEXP_RXP9	AE10	PEX_TX9P
GMCEXP_RXN9	C202	EVA:1u16V_4 V	GMCEXP_RXN9	AE10	PEX_TX9N
GMCEXP_TXP9	AE16			AE7	PEX_RX9P
GMCEXP_TXN9	AE16			AE7	PEX_RX9N
GMCEXP_RXP10	C194	EVA:1u16V_4 V	GMCEXP_RXP10	AE10	PEX_TX10P
GMCEXP_RXN10	C193	EVA:1u16V_4 V	GMCEXP_RXN10	AE10	PEX_TX10N
GMCEXP_TXP10	AG16			AE7	PEX_RX10P
GMCEXP_TXN10	AG16			AE7	PEX_RX10N
GMCEXP_RXP11	C215	EVA:1u16V_4 V	GMCEXP_RXP11	AE21	PEX_TX11P
GMCEXP_RXN11	C216	EVA:1u16V_4 V	GMCEXP_RXN11	AE21	PEX_TX11N
GMCEXP_TXP11	AE19			AE7	PEX_RX11P
GMCEXP_TXN11	AE19			AE7	PEX_RX11N
GMCEXP_RXP12	C196	EVA:1u16V_4 V	GMCEXP_RXP12	AE20	PEX_TX12P
GMCEXP_RXN12	C197	EVA:1u16V_4 V	GMCEXP_RXN12	AE20	PEX_TX12N
GMCEXP_TXP12	AG21			AE7	PEX_RX12P
GMCEXP_TXN12	AG21			AE7	PEX_RX12N
GMCEXP_RXP13	C217	EVA:1u16V_4 V	GMCEXP_RXP13	AD22	PEX_TX13P
GMCEXP_RXN13	C218	EVA:1u16V_4 V	GMCEXP_RXN13	AD22	PEX_TX13N
GMCEXP_TXP13	AG22			AE7	PEX_RX13P
GMCEXP_TXN13	AG22			AE7	PEX_RX13N
GMCEXP_RXP14	C198	EVA:1u16V_4 V	GMCEXP_RXP14	AE23	PEX_TX14P
GMCEXP_RXN14	C199	EVA:1u16V_4 V	GMCEXP_RXN14	AE23	PEX_TX14N
GMCEXP_TXP14	AG24			AE7	PEX_RX14P
GMCEXP_TXN14	AG24			AE7	PEX_RX14N
GMCEXP_RXP15	C219	EVA:1u16V_4 V	GMCEXP_RXP15	AE24	PEX_TX15P
GMCEXP_RXN15	C220	EVA:1u16V_4 V	GMCEXP_RXN15	AE24	PEX_TX15N
GMCEXP_TXP15	AG26			AE7	PEX_RX15P
GMCEXP_TXN15	AG26			AE7	PEX_RX15N

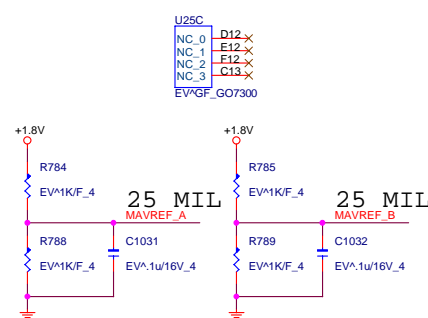
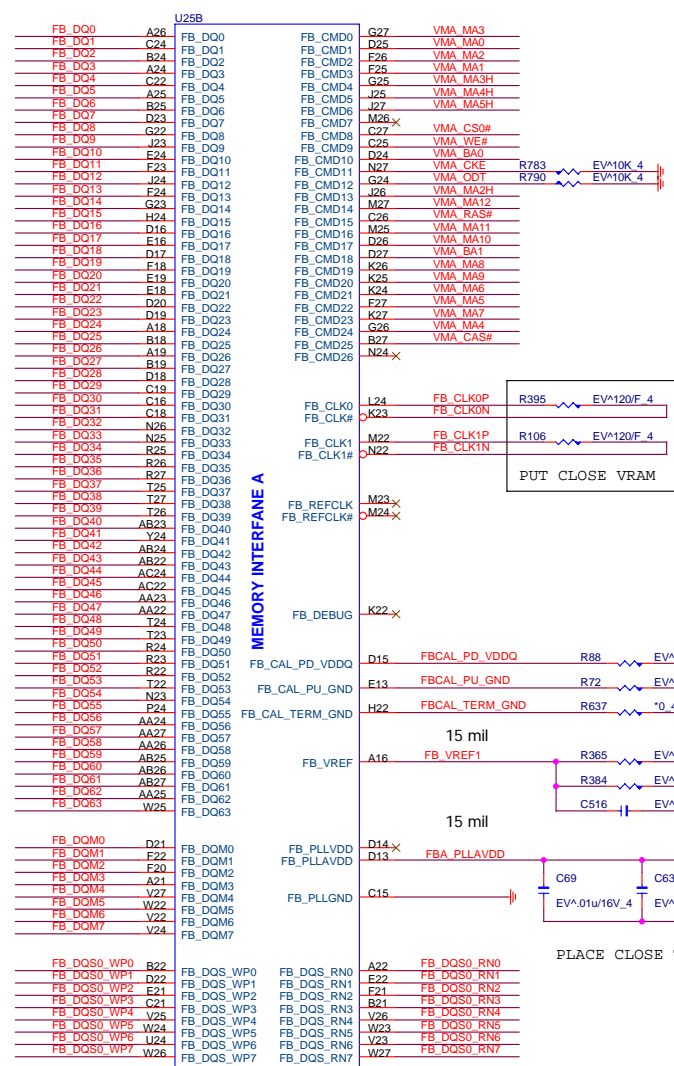


EV*G*_G07300

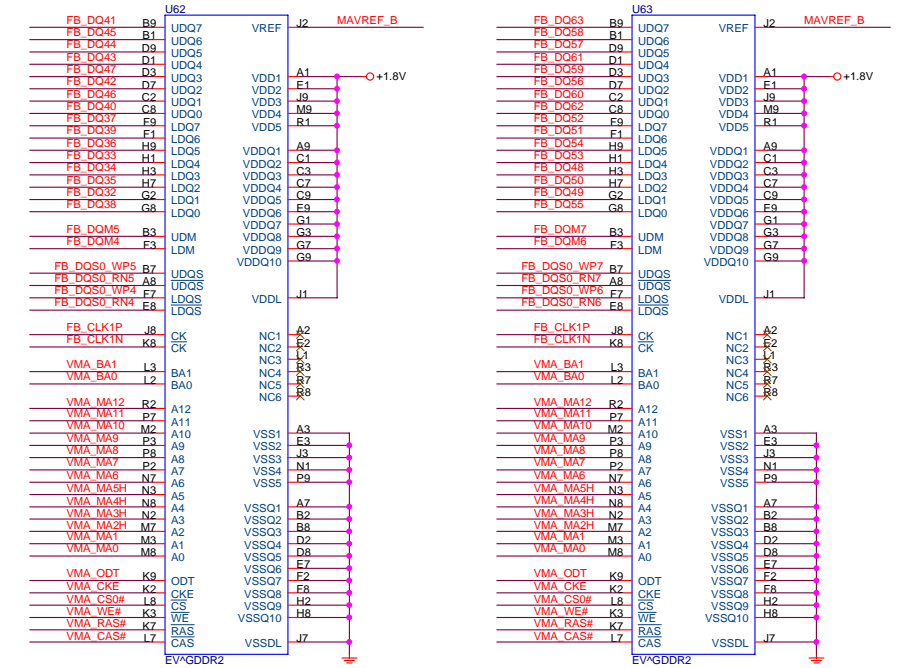
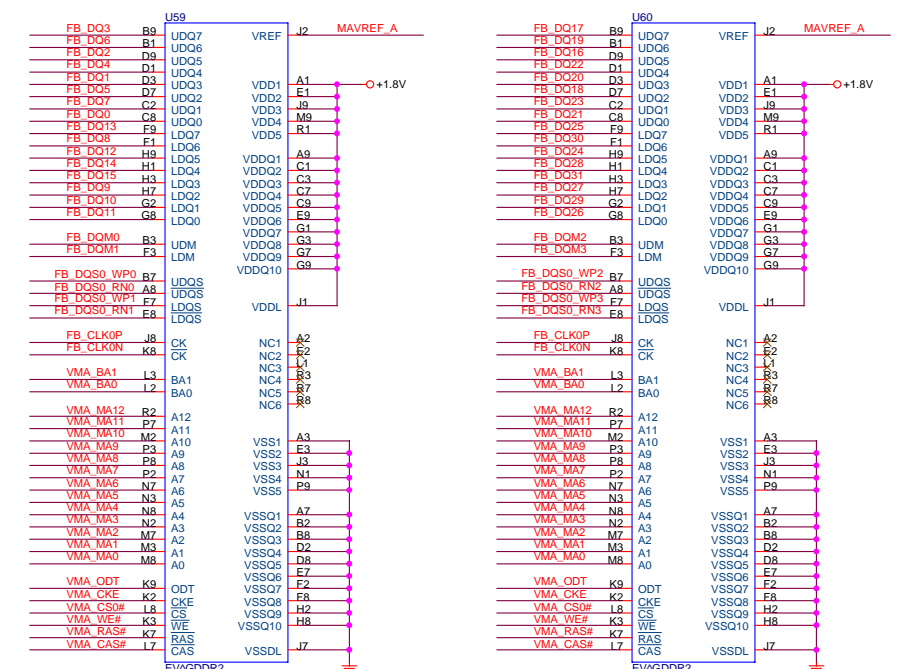


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G72MV_PCIE/DAC/GND
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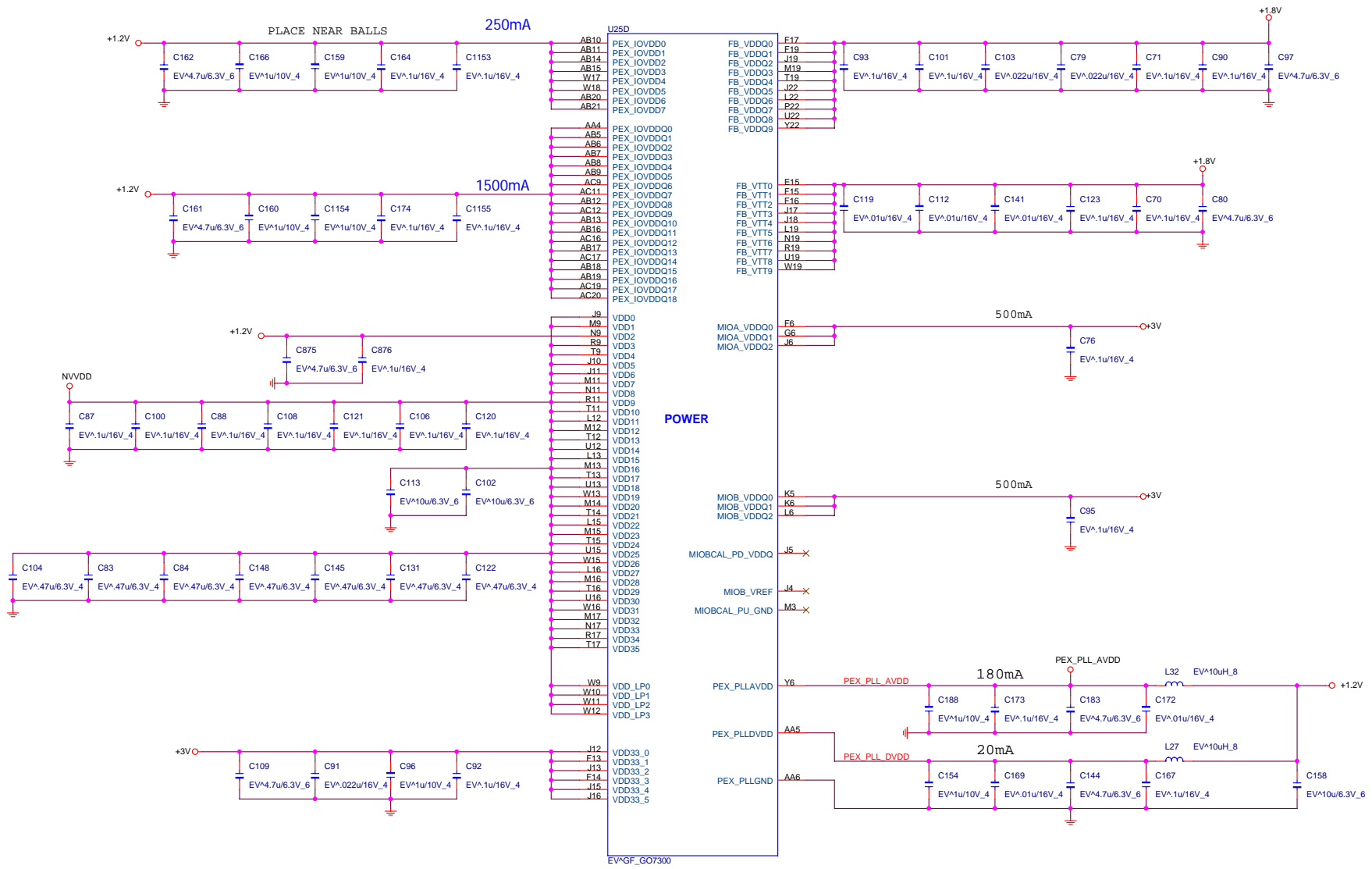
PLACE CLOSE TO BALLS

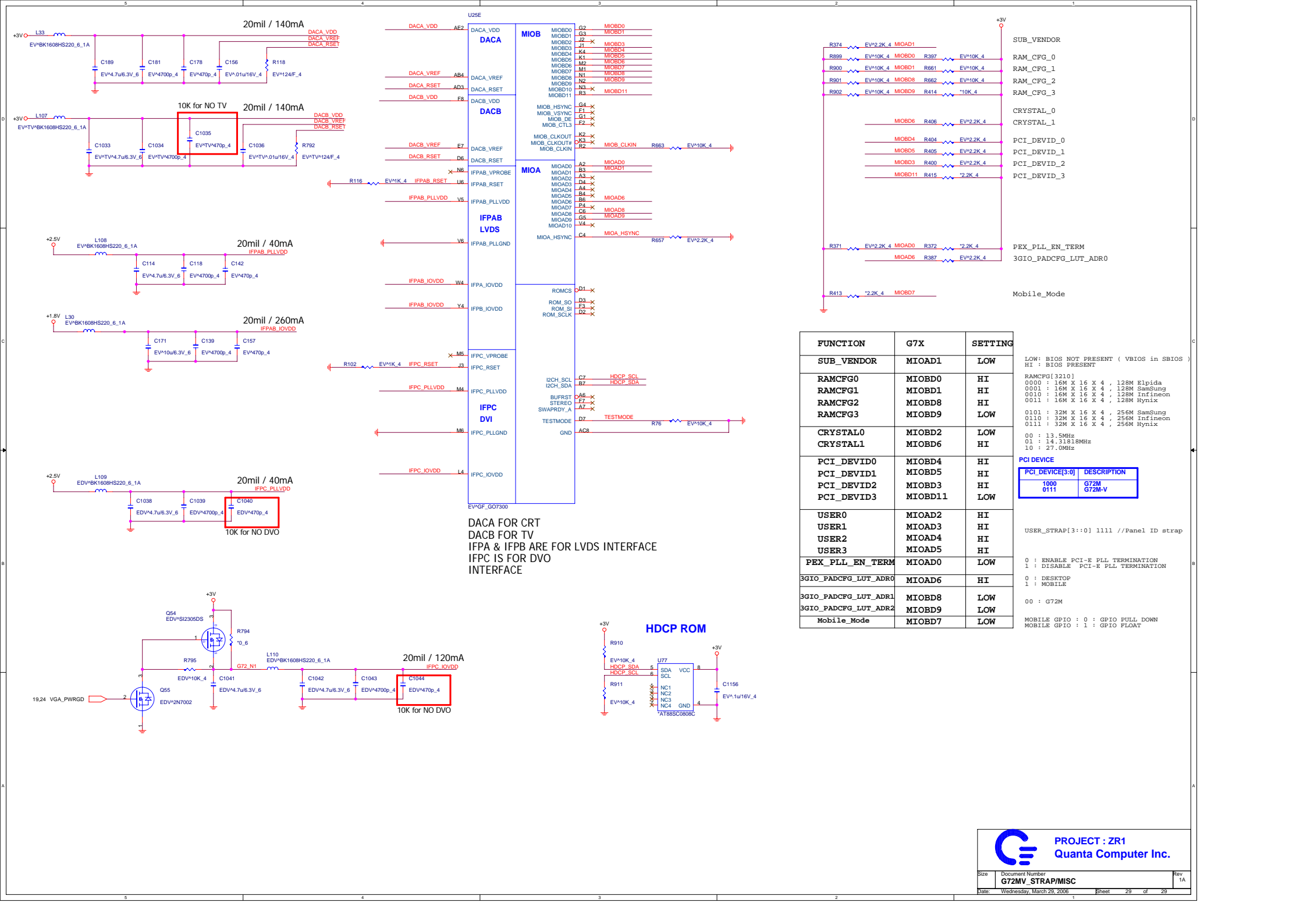


- SAMSUNG 16M*16 --> AKD5JGBT509
- SAMSUNG 32M*16 --> AKD5FGBT501
- INFI 16M*16 --> AKD5JG-T*08
- INFI 32M*16 --> AKD5FG-T*00
- HYNIX 16M*16 --> AKD5JG-TW12
- HYNIX 32M*16 --> AKD5FG-TW14

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	G72MV_MEMORY A/B/C/D	1A
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DACA FOR CRT
 DACB FOR TV
 IFPA & IFPB ARE FOR LVDS INTERFACE
 IFPC IS FOR DVO INTERFACE

FUNCTION	G7X	SETTING
SUB_VENDOR	MIOAD1	LOW
RAMCFG0	MIOBD0	HI
RAMCFG1	MIOBD1	HI
RAMCFG2	MIOBD8	HI
RAMCFG3	MIOBD9	LOW
CRYSTAL0	MIOBD2	LOW
CRYSTAL1	MIOBD6	HI
PCI_DEVID0	MIOBD4	HI
PCI_DEVID1	MIOBD5	HI
PCI_DEVID2	MIOBD3	HI
PCI_DEVID3	MIOBD11	LOW
USER0	MIOAD2	HI
USER1	MIOAD3	HI
USER2	MIOAD4	HI
USER3	MIOAD5	HI
PEX_PLL_EN_TERM	MIOAD0	LOW
3GIO_PADCFG_LUT_ADR0	MIOAD6	HI
3GIO_PADCFG_LUT_ADR1	MIOBD8	LOW
3GIO_PADCFG_LUT_ADR2	MIOBD9	LOW
Mobile_Mode	MIOBD7	LOW

LOW: BIOS NOT PRESENT (VBIOS in SBIOS)
 HI: BIOS PRESENT

```
RAMCFG[3210]
0000 : 16M X 16 X 4 . 128M Elpida
0001 : 16M X 16 X 4 . 128M Samsung
0010 : 16M X 16 X 4 . 128M Infineon
0011 : 16M X 16 X 4 . 128M Hynix
0101 : 32M X 16 X 4 . 256M Samsung
0110 : 32M X 16 X 4 . 256M Infineon
0111 : 32M X 16 X 4 . 256M Hynix
```

PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M
0111	G72M-V

USER_STRAP[3:10] 1111 //Panel ID strap

0 : ENABLE PCI-E PLL TERMINATION
 1 : DISABLE PCI-E PLL TERMINATION

0 : DESKTOP
 1 : MOBILE

00 : G72M

MOBILE GPIO : 0 : GPIO PULL DOWN
 MOBILE GPIO : 1 : GPIO FLOAT

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