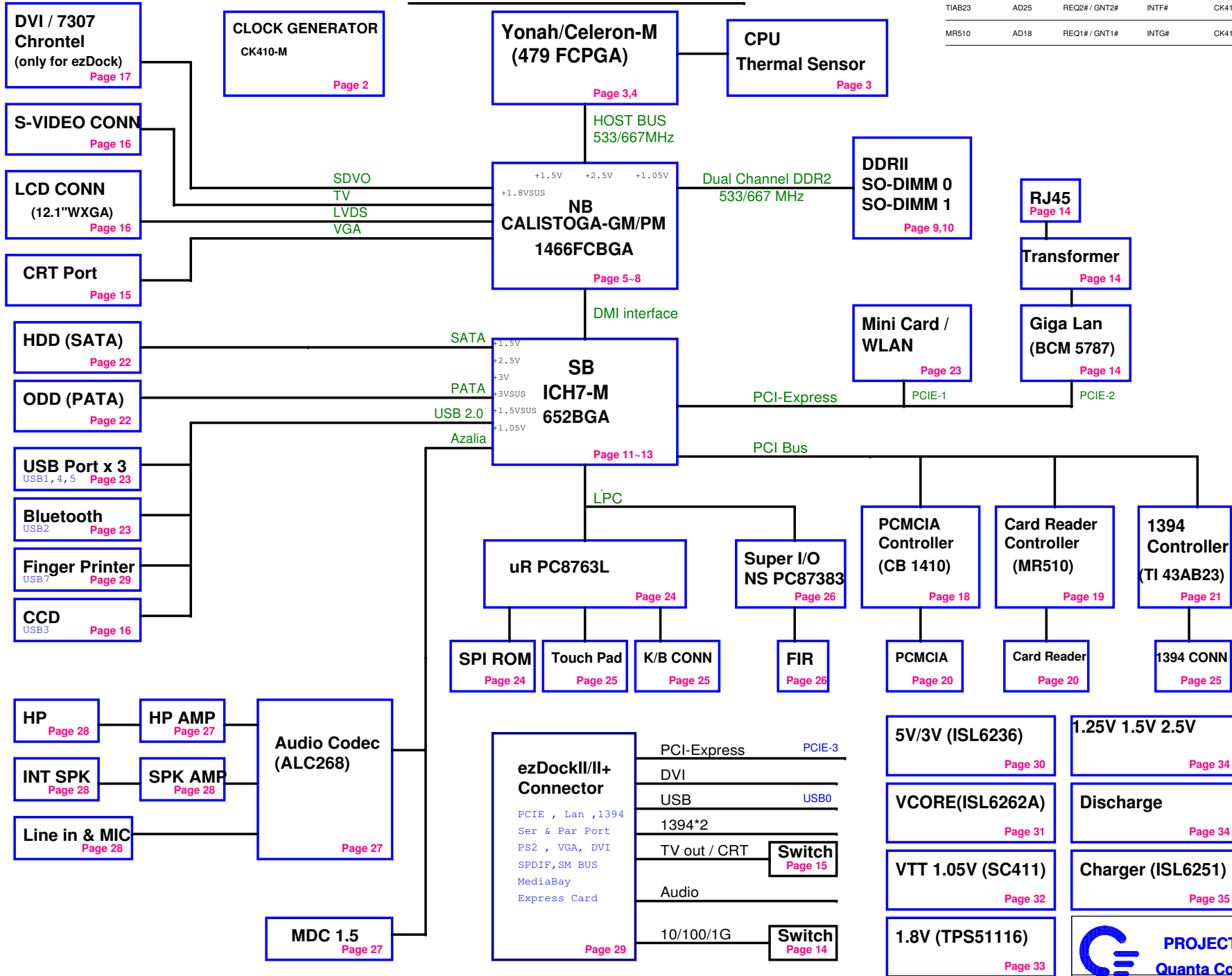
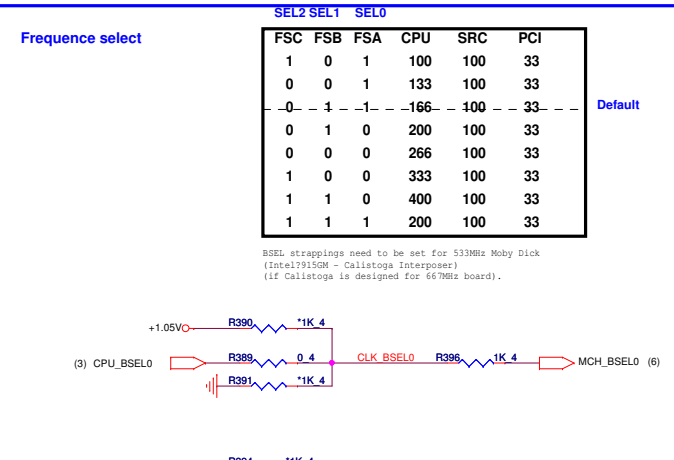
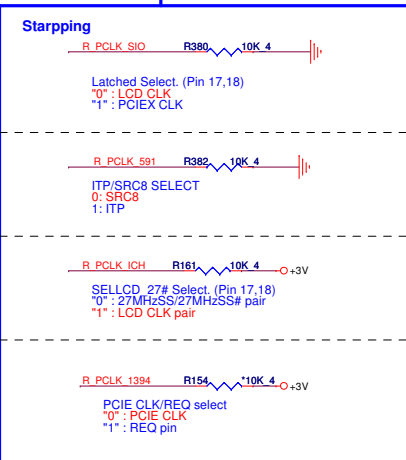
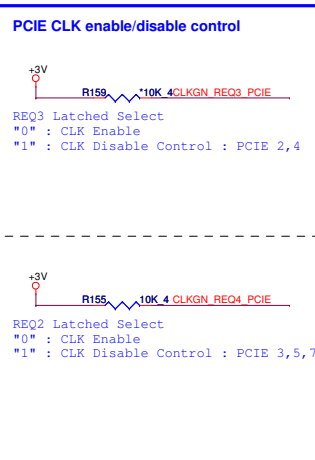
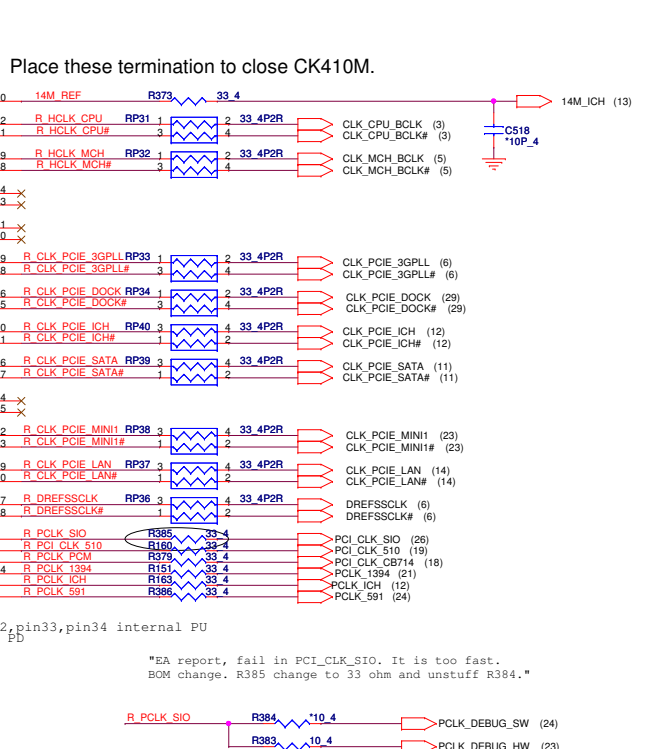
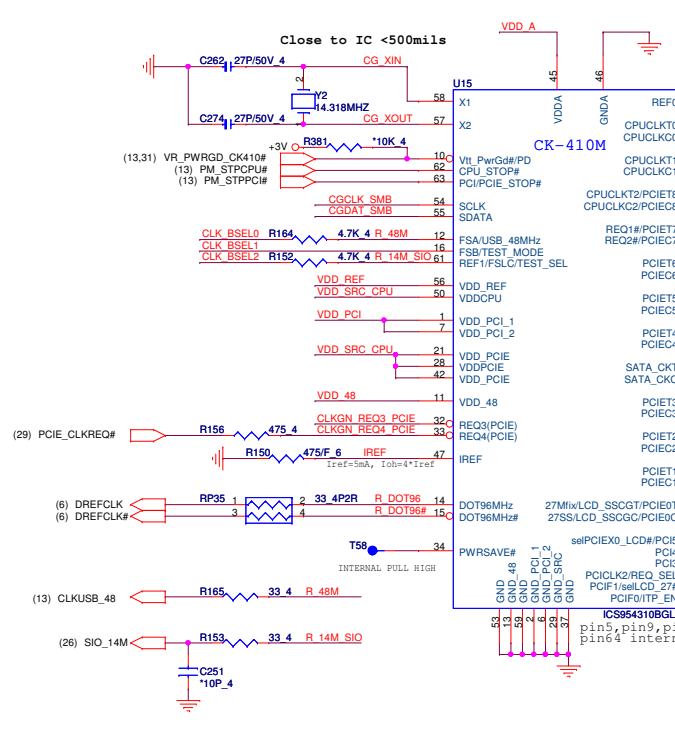
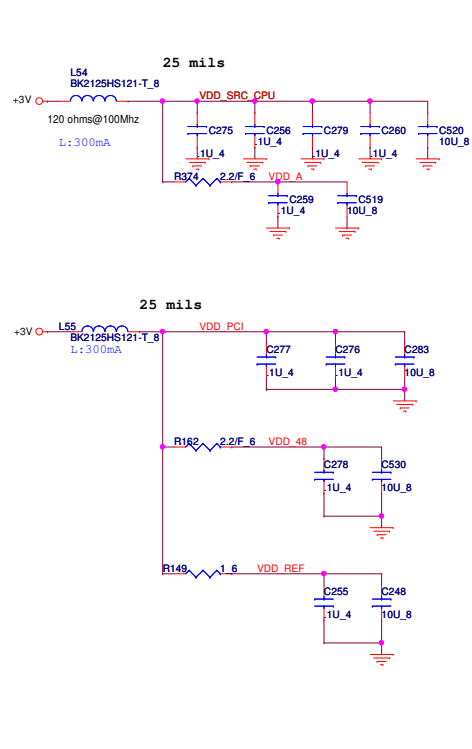


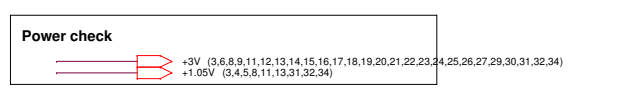
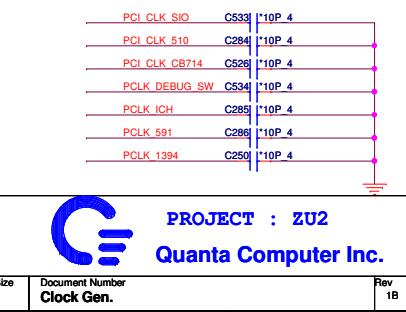
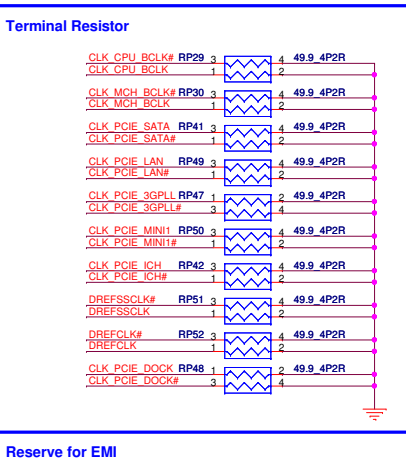
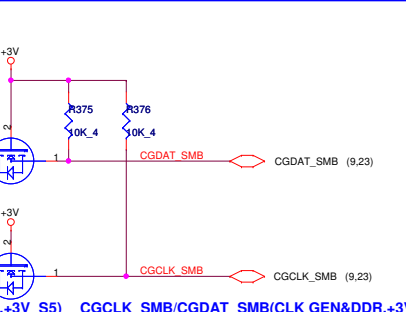
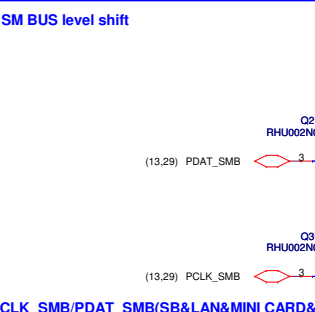
# ZU2 SYSTEM BLOCK DIAGRAM

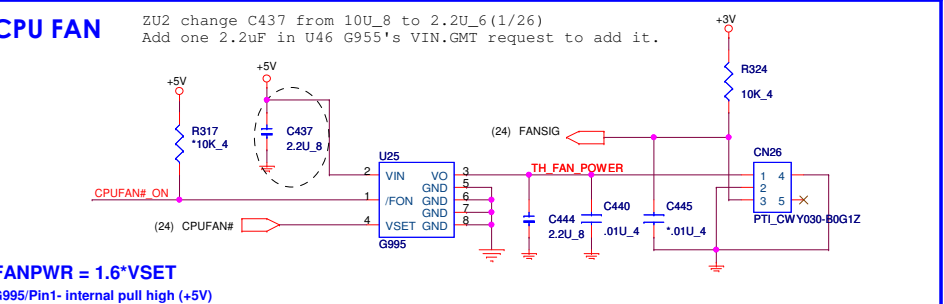
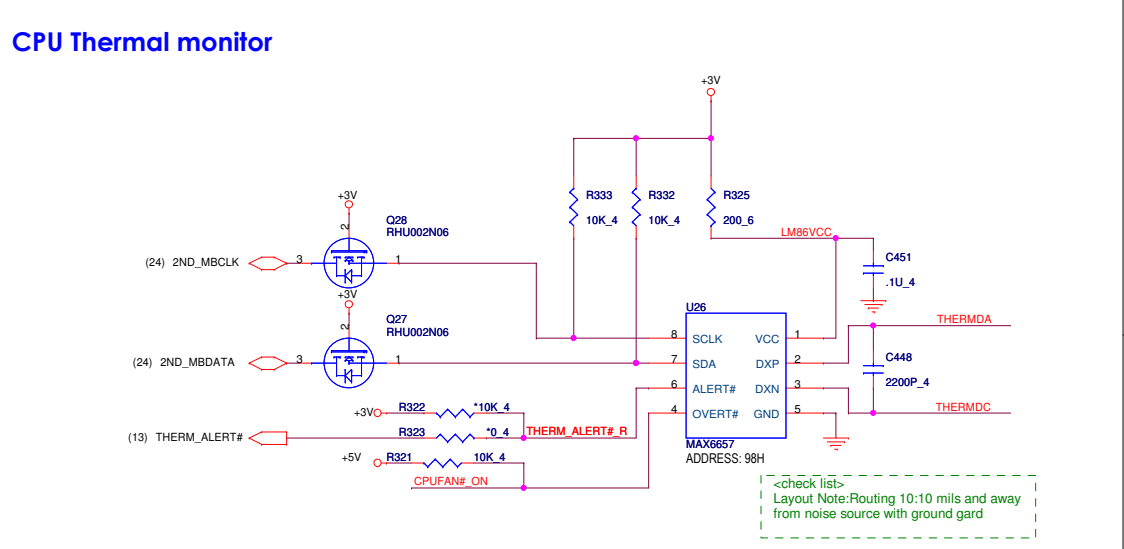
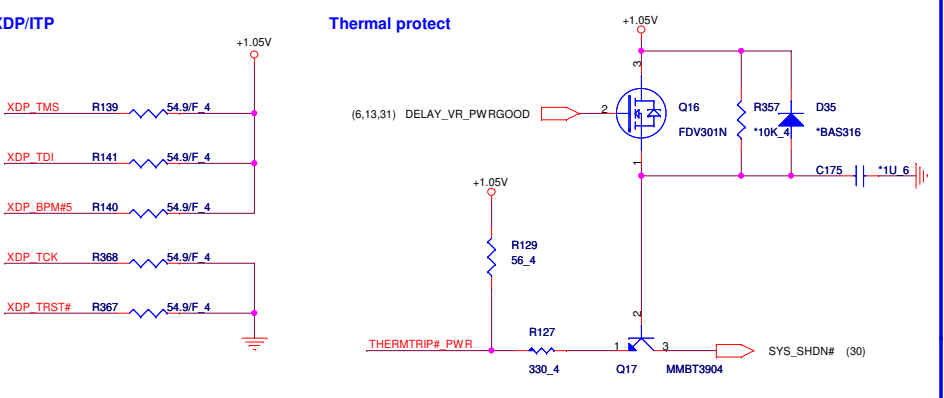
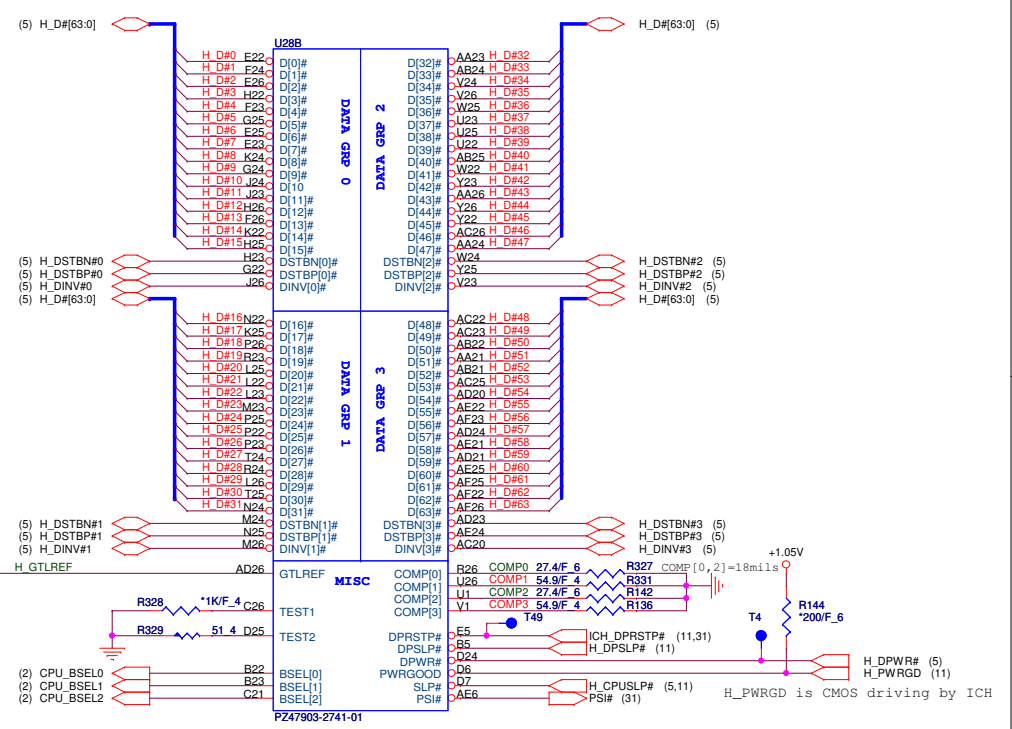
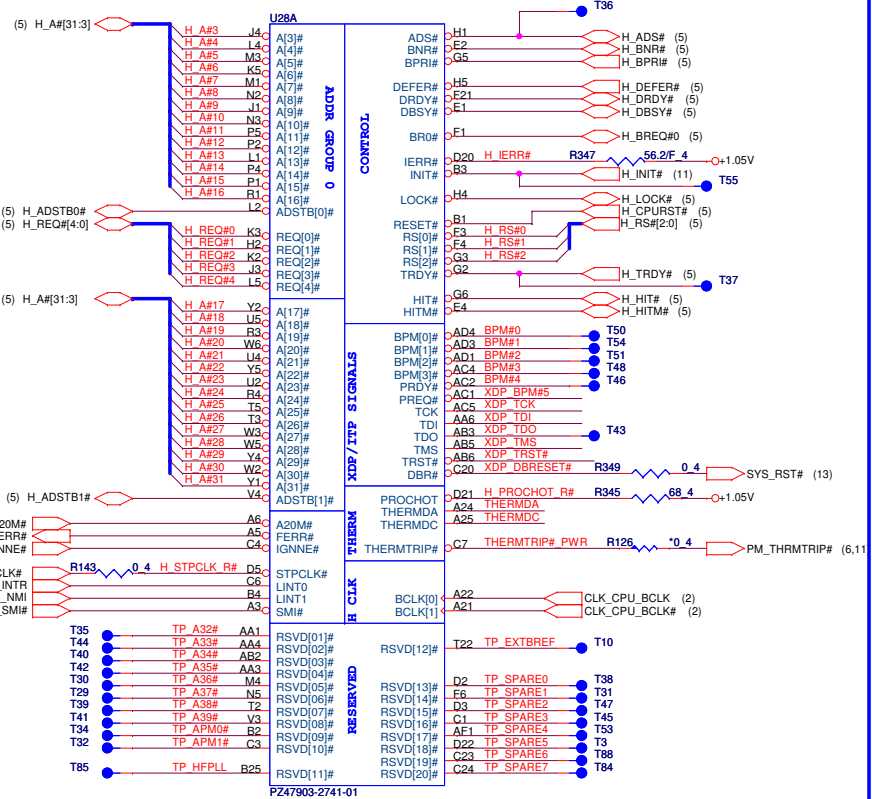
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTE#	CK410/PC13
TIAB23	AD25	REQ2# / GNT2#	INTF#	CK410/PC18
MR510	AD18	REQ1# / GNT1#	INTG#	CK410/PC14



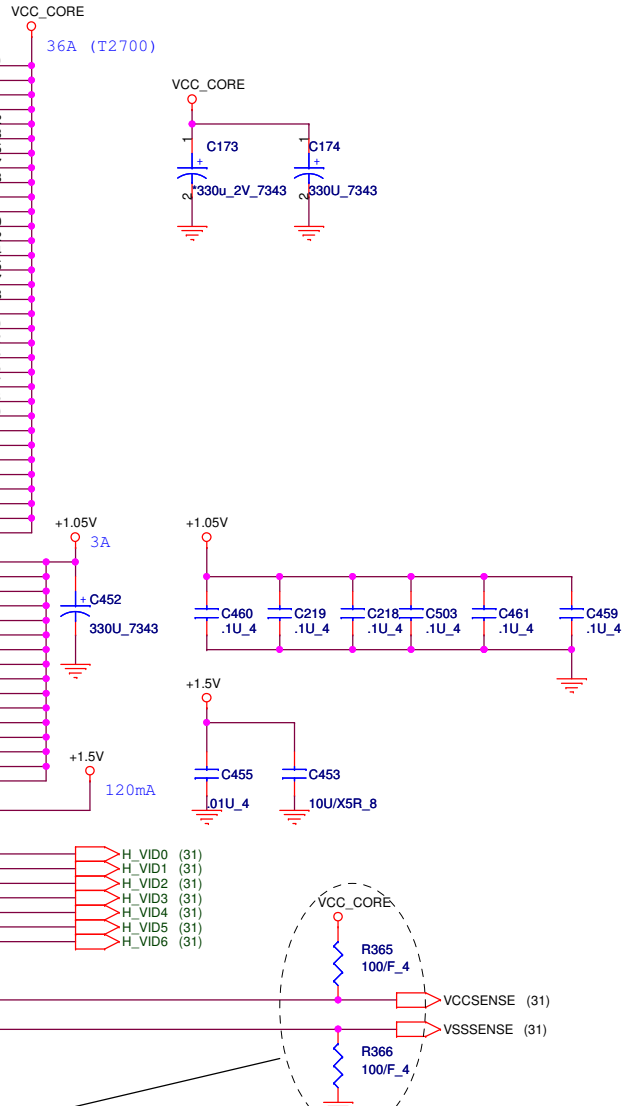
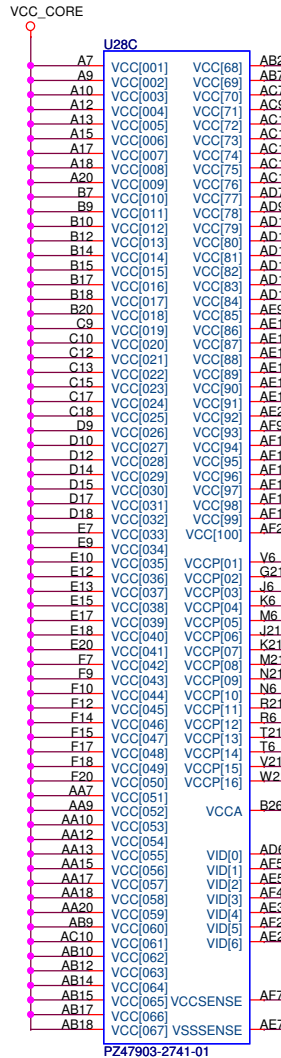
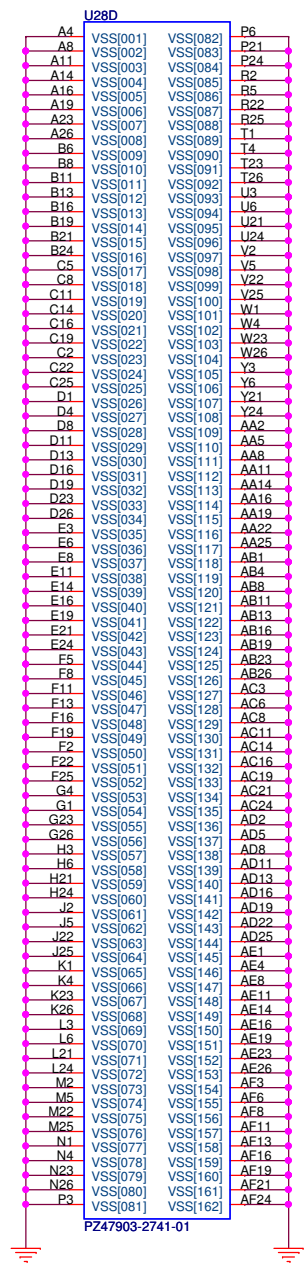


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

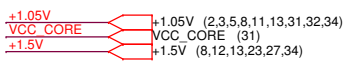




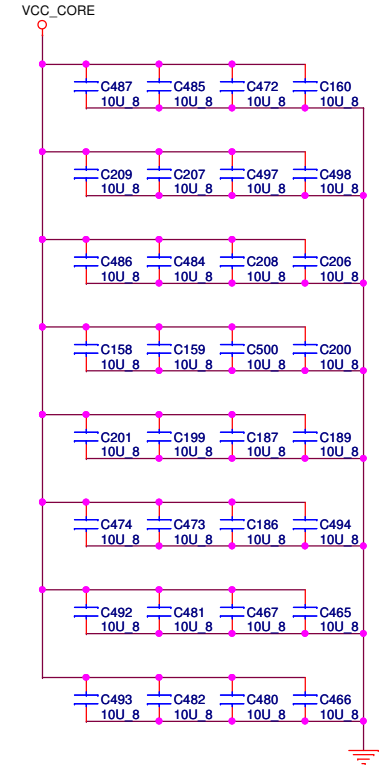
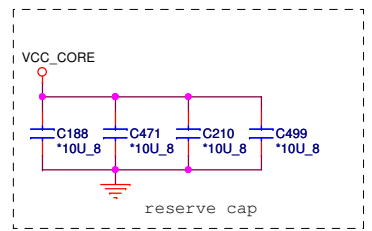
		PROJECT : ZU2	
		Quanta Computer Inc.	
Size	Document Number		Rev
	YOHNA (HOST)		1A
Date:	Thursday, March 22, 2007	Sheet	3 of 39



Add 100\_F PU on VCCSENSE.  
 Add 100\_F PD on VSSSENSE.  
 Check intel circuit by Alan(1/26)



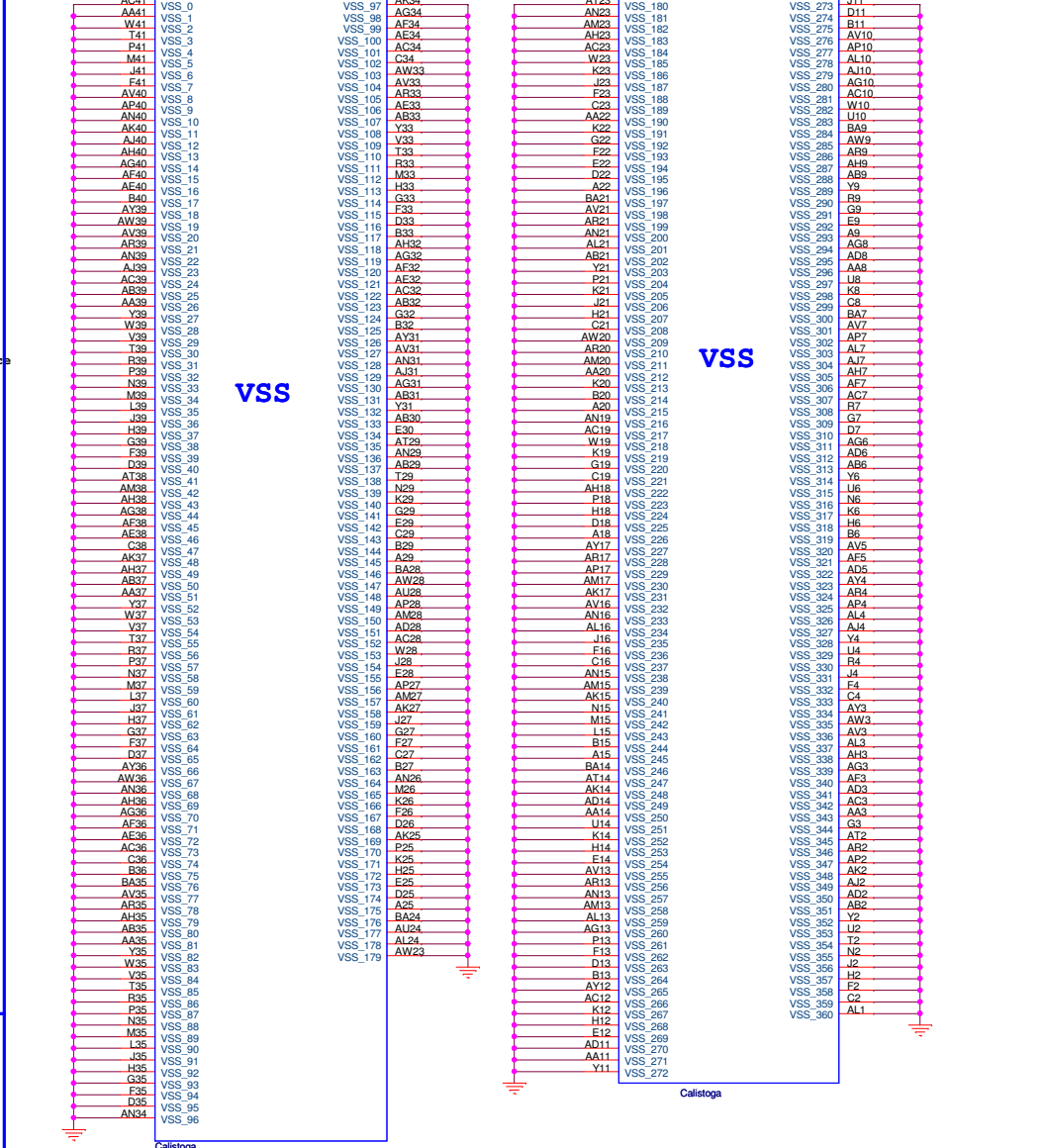
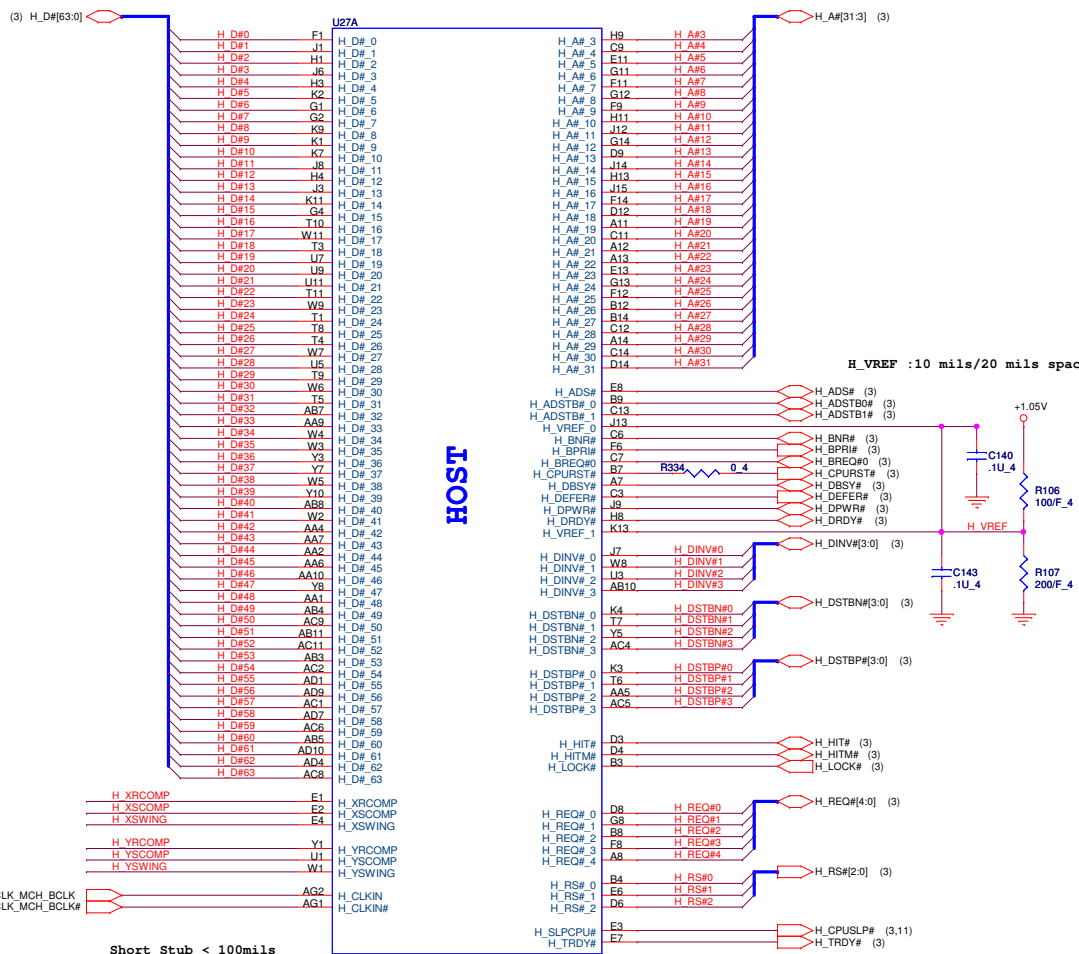
## VCC\_CORE CAP.



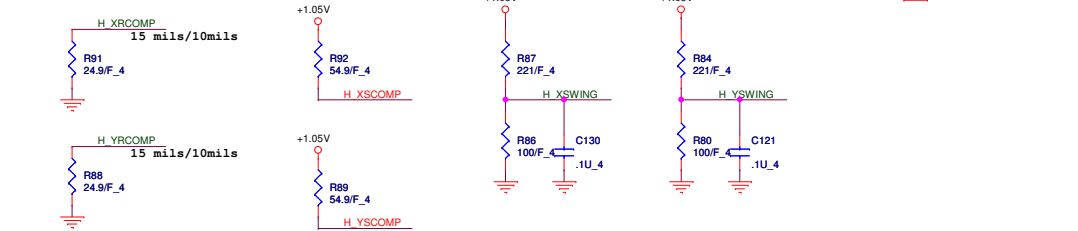
**PROJECT : ZU2**

**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Yonah/Merom CPU(Power/GND)-2</b>	1A
Date:	Thursday, March 22, 2007	Sheet 4 of 39



**Slew/IO Buffer COMP.**

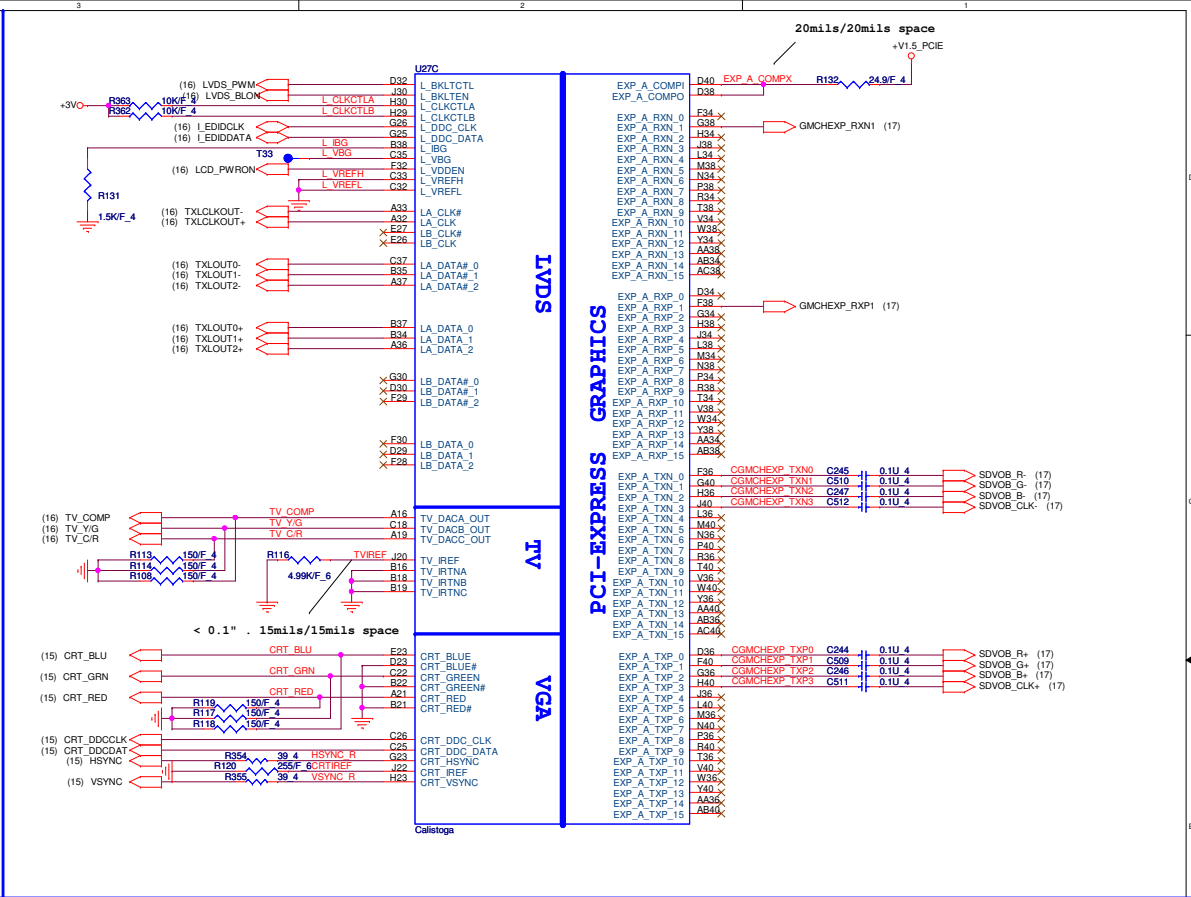
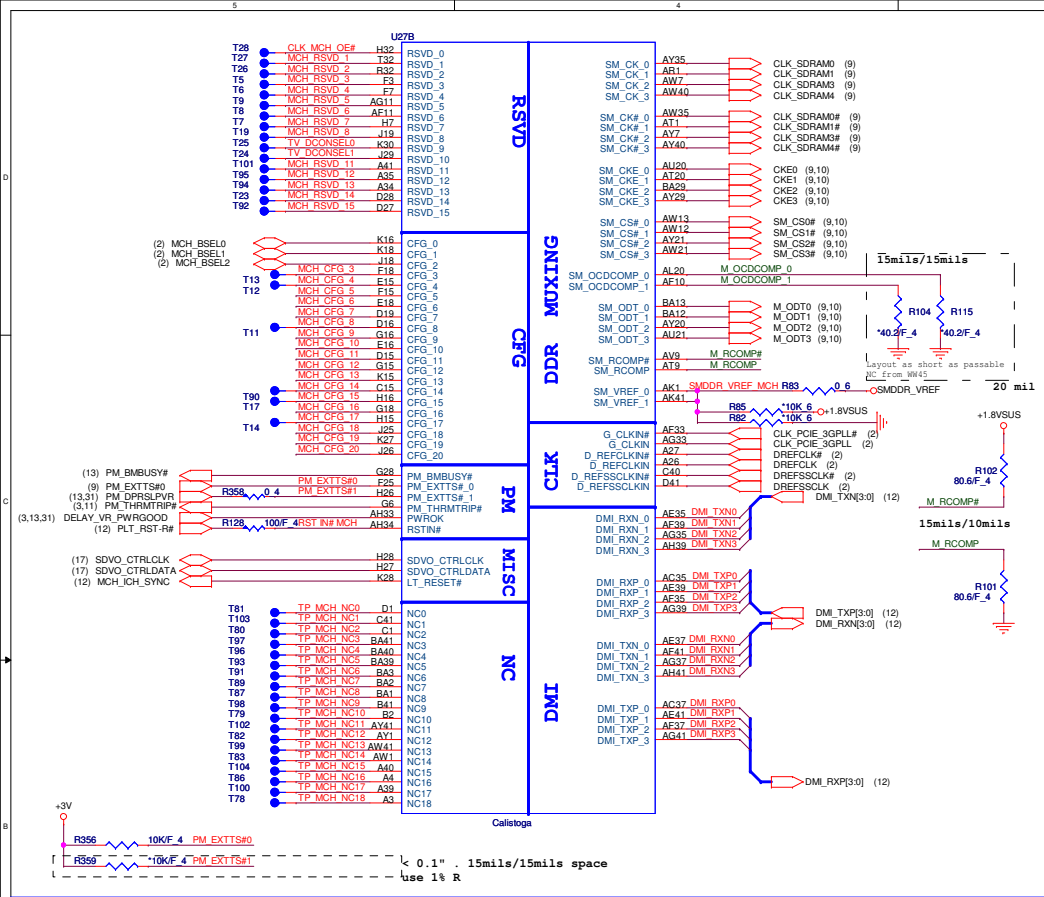


COMPONENTS	P/N
945GM	AJSL8Z20T25
ICH7-M	AJSL8YB0T21

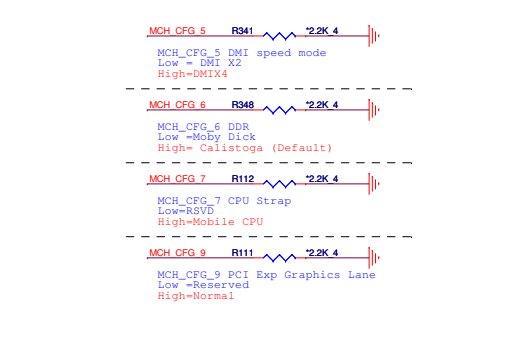
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>GMCH (HOST/GND)</b>	1A
Date:	Thursday, March 22, 2007	Sheet 5 of 39





**GMCH Strap pin** CFG[3..17] has internal PU



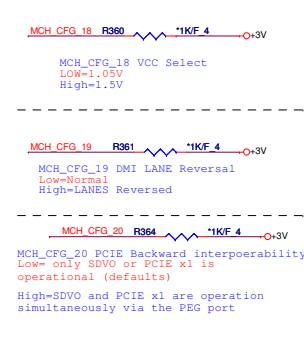
MCH\_CFG\_10 Host PLL VCC Select  
Low=Reserved  
High=Mobility

MCH\_CFG\_11 PSB 4x CLK ENABLE  
Low=Reserved  
High=Callistoga

MCH\_CFG\_12,13 XOR/ALLZ  
0,0=Partial clock gating disable  
0,1=All-2 mode enable  
1,0=XOR mode enable  
1,1=Normal

MCH\_CFG\_16 PSB Dynamic ODT  
Low=Dynamic ODI Disabled  
High=Dynamic ODI Enabled

CFG[18..20] has internal PD



MCH\_CFG\_18 VCC Select  
Low=1.05V  
High=1.5V

MCH\_CFG\_19 DMI LANE Reversal  
Low=Normal  
High=LANES Reversed

MCH\_CFG\_20 PCIe Backward interoperability mode  
Low= only SDVO or PCIe x1 is operational (defaults)  
High=SDVO and PCIe x1 are operation simultaneously via the PEG port

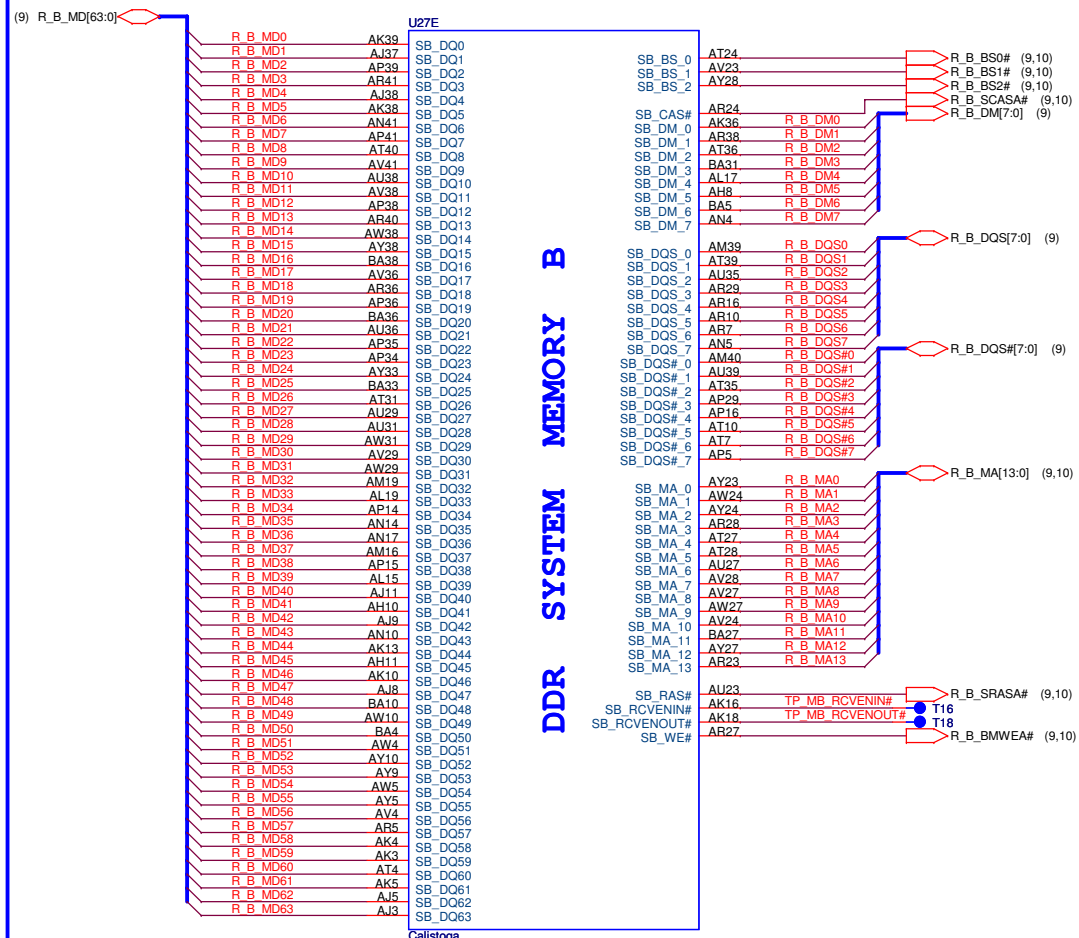
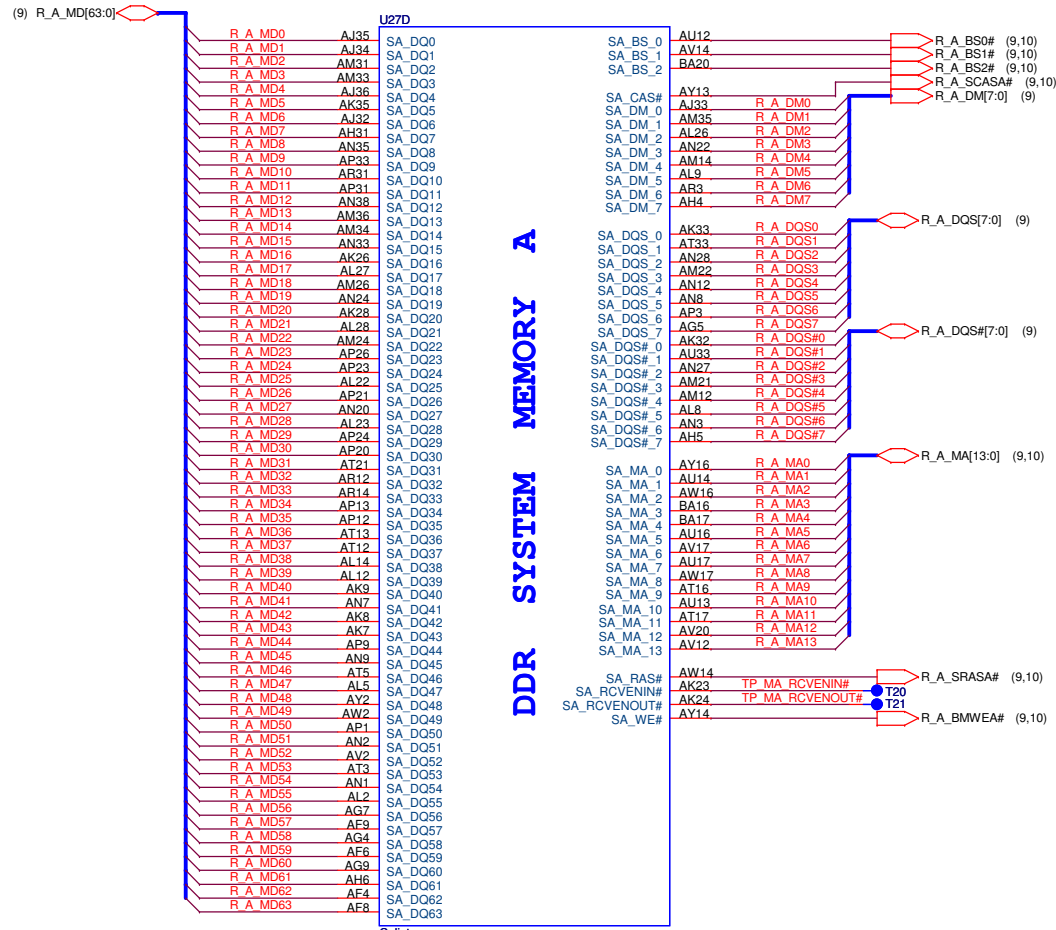


**PROJECT : ZU2**

**Quanta Computer Inc.**

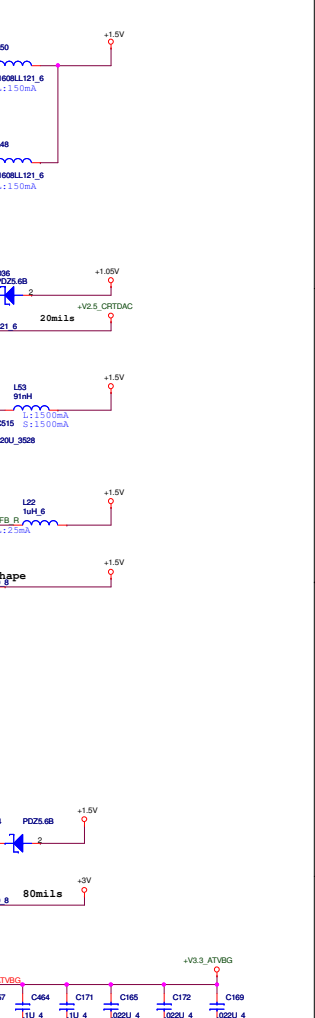
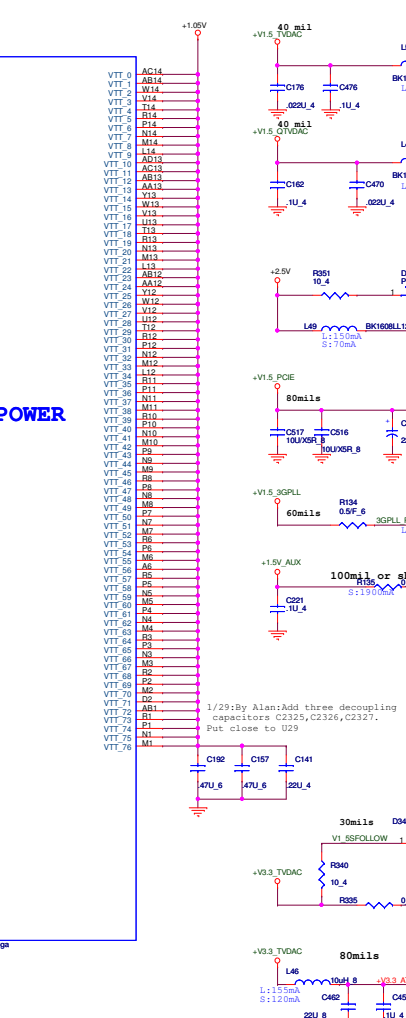
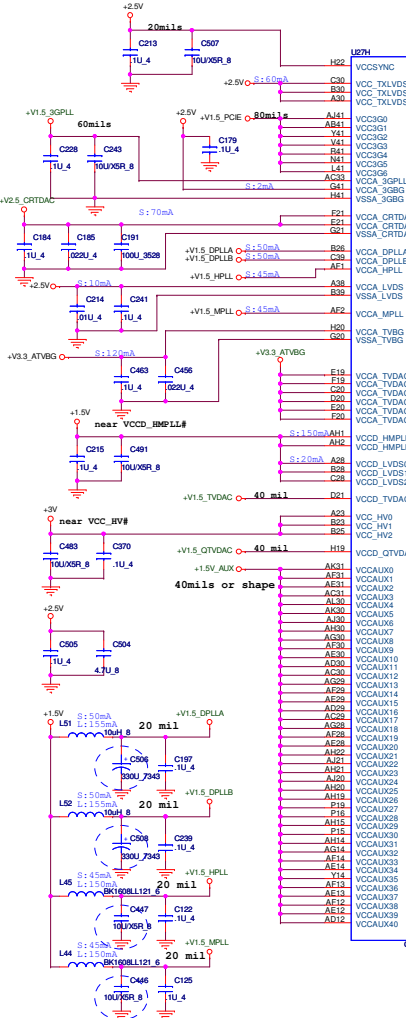
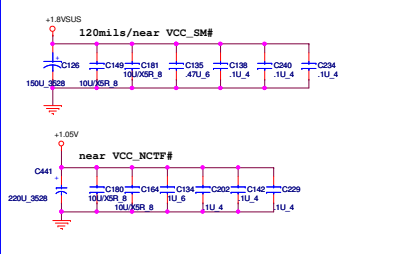
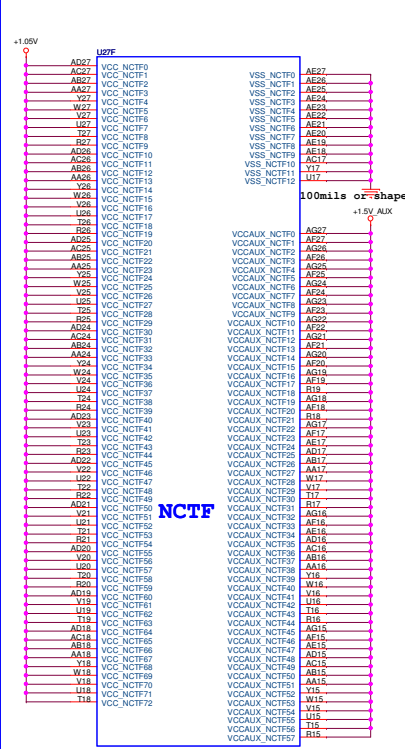
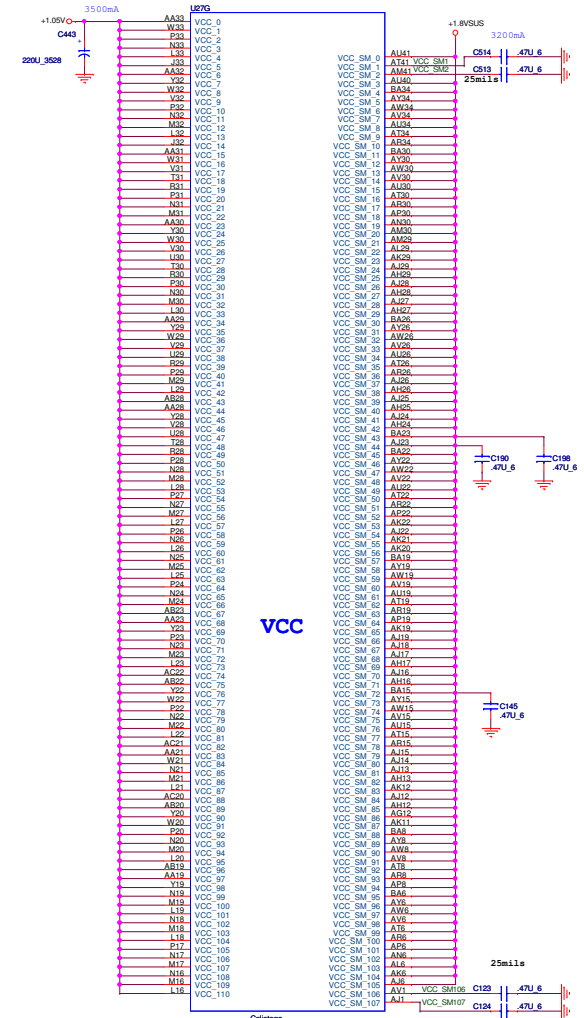
Size: Document Number: **GMCH (DMI&PCIE&VGA)** Rev: 1A

Date: Thursday, March 22, 2007 Sheet: 6 of 39

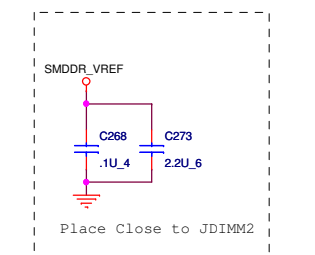
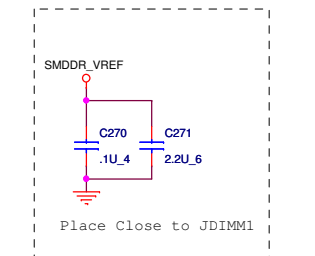
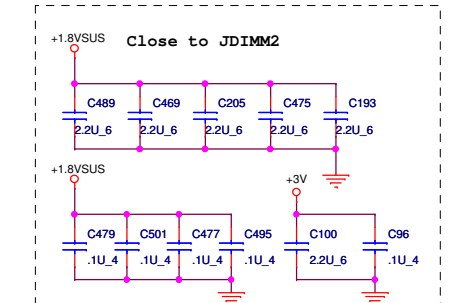
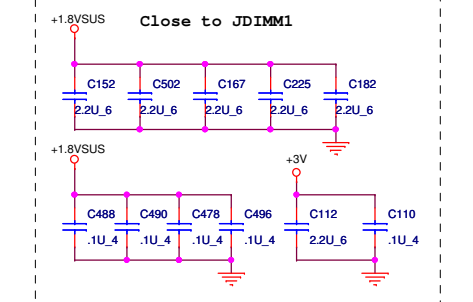
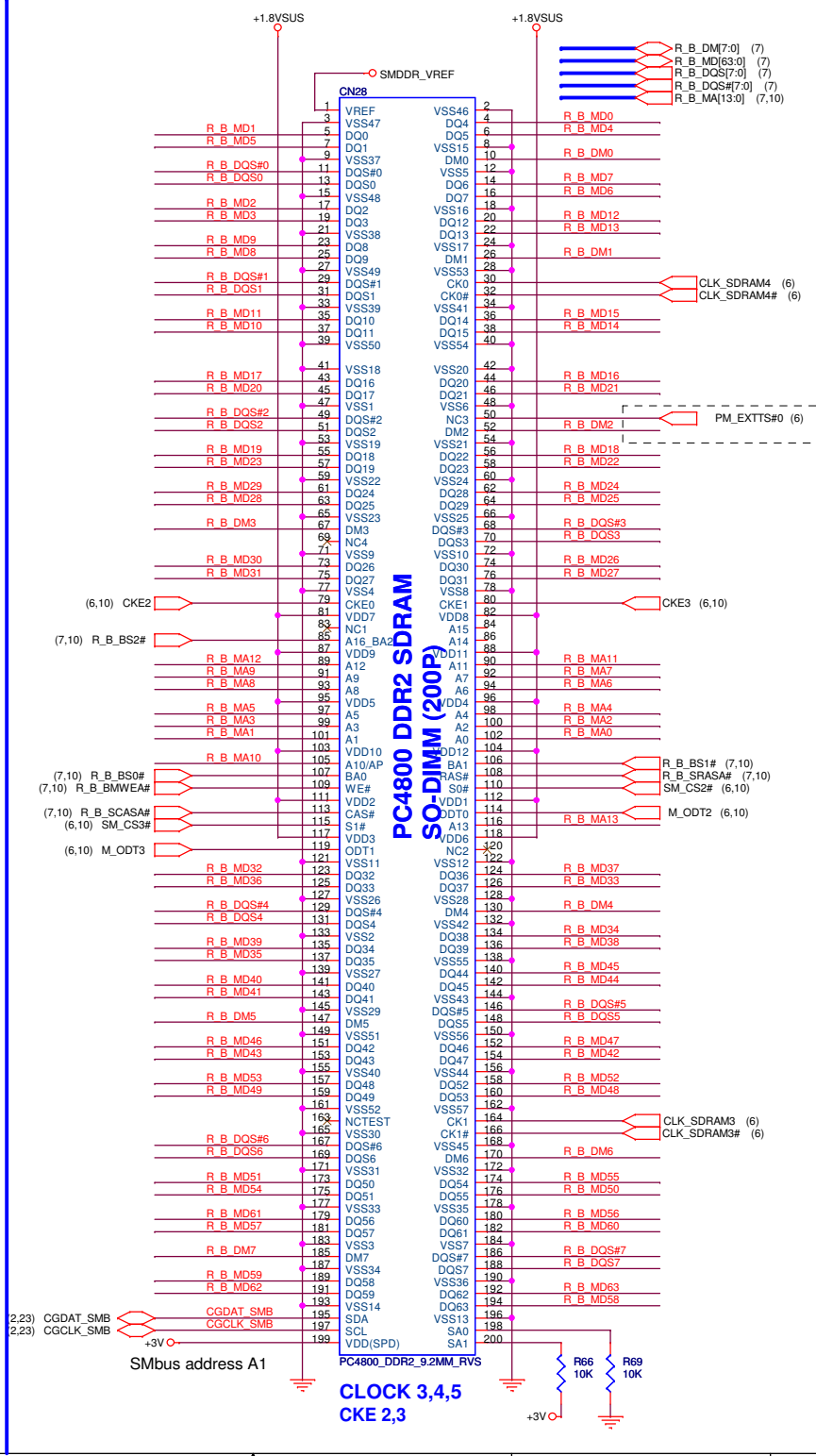
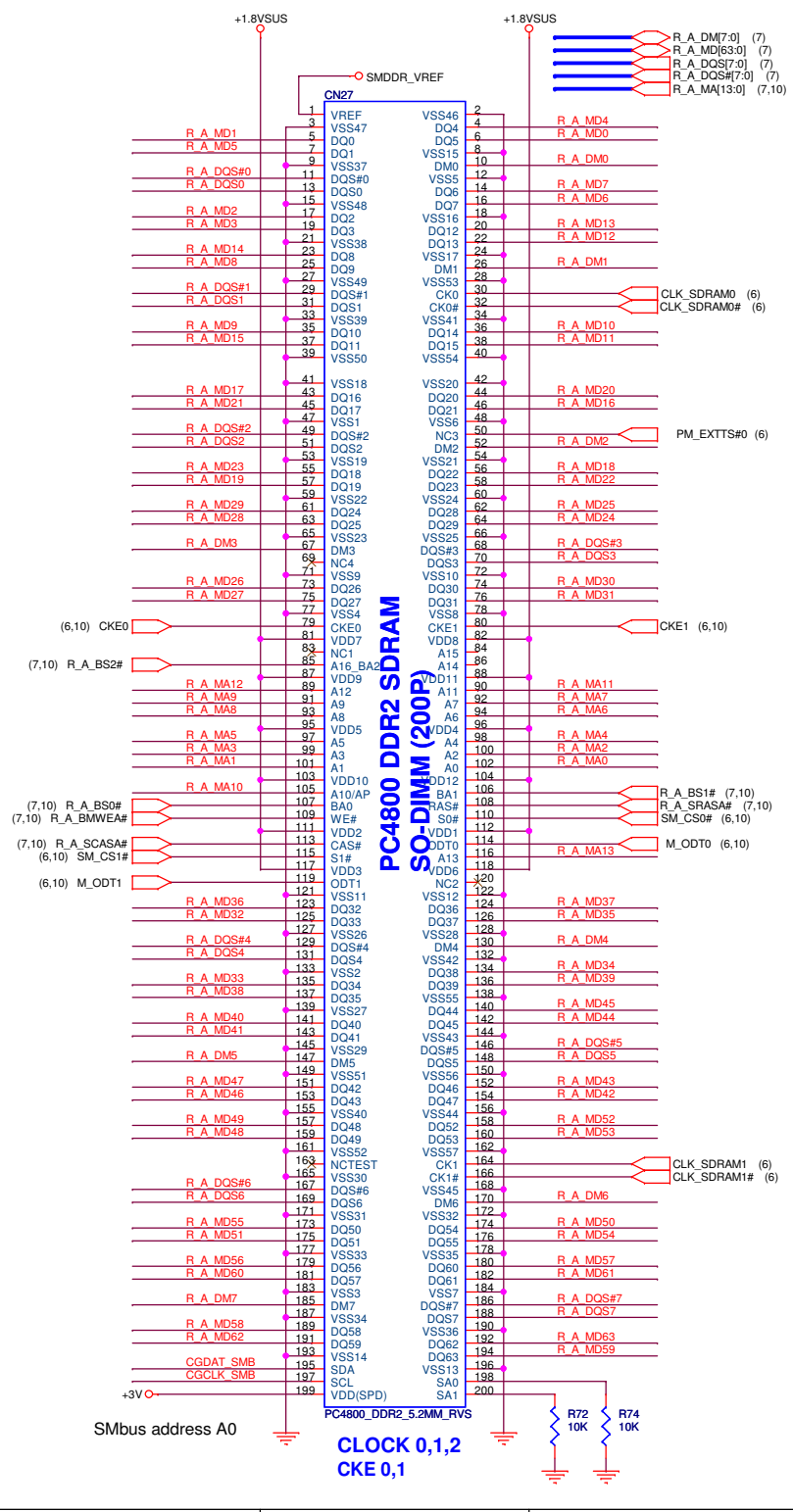


**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>GMCH (DDR2)</b>	1A
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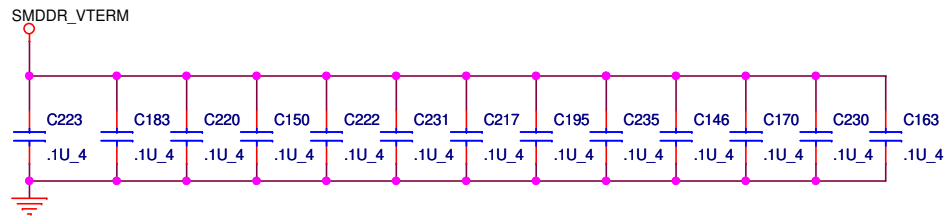




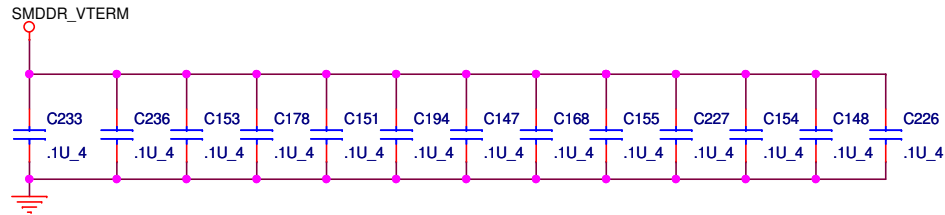
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size Document Number  
**DDR2 SO-DIMM (200P)**

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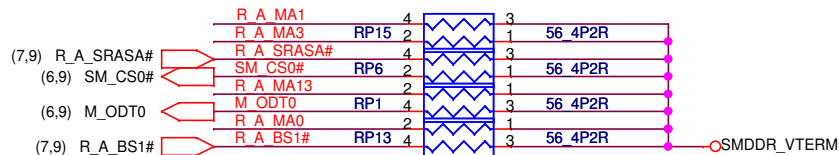
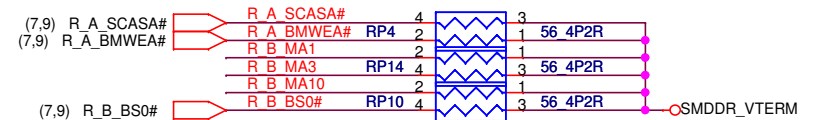
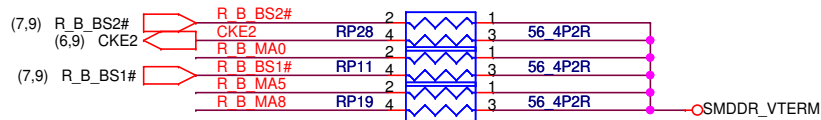
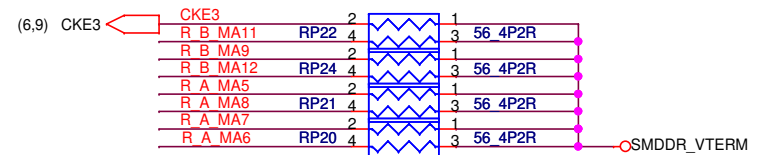
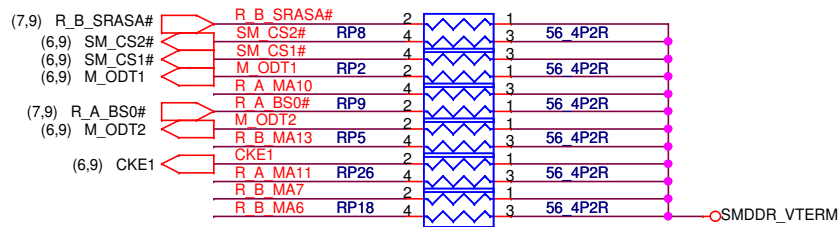
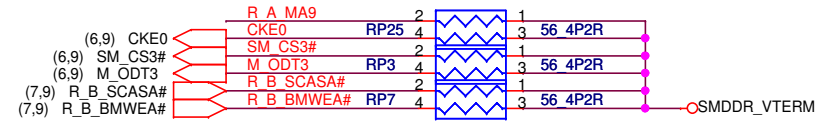
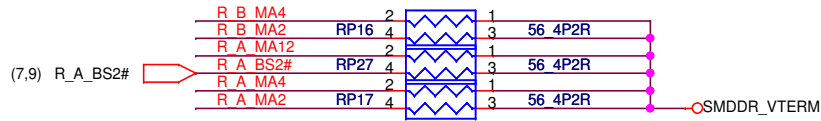
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM

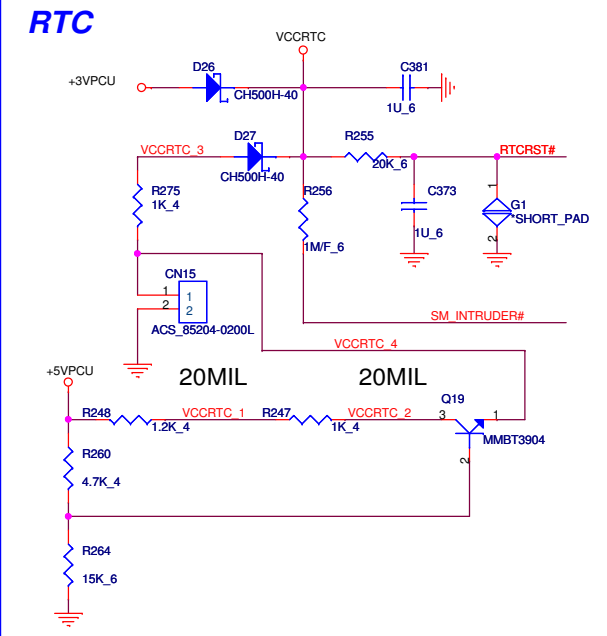
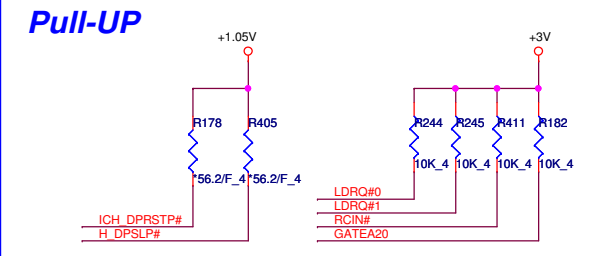
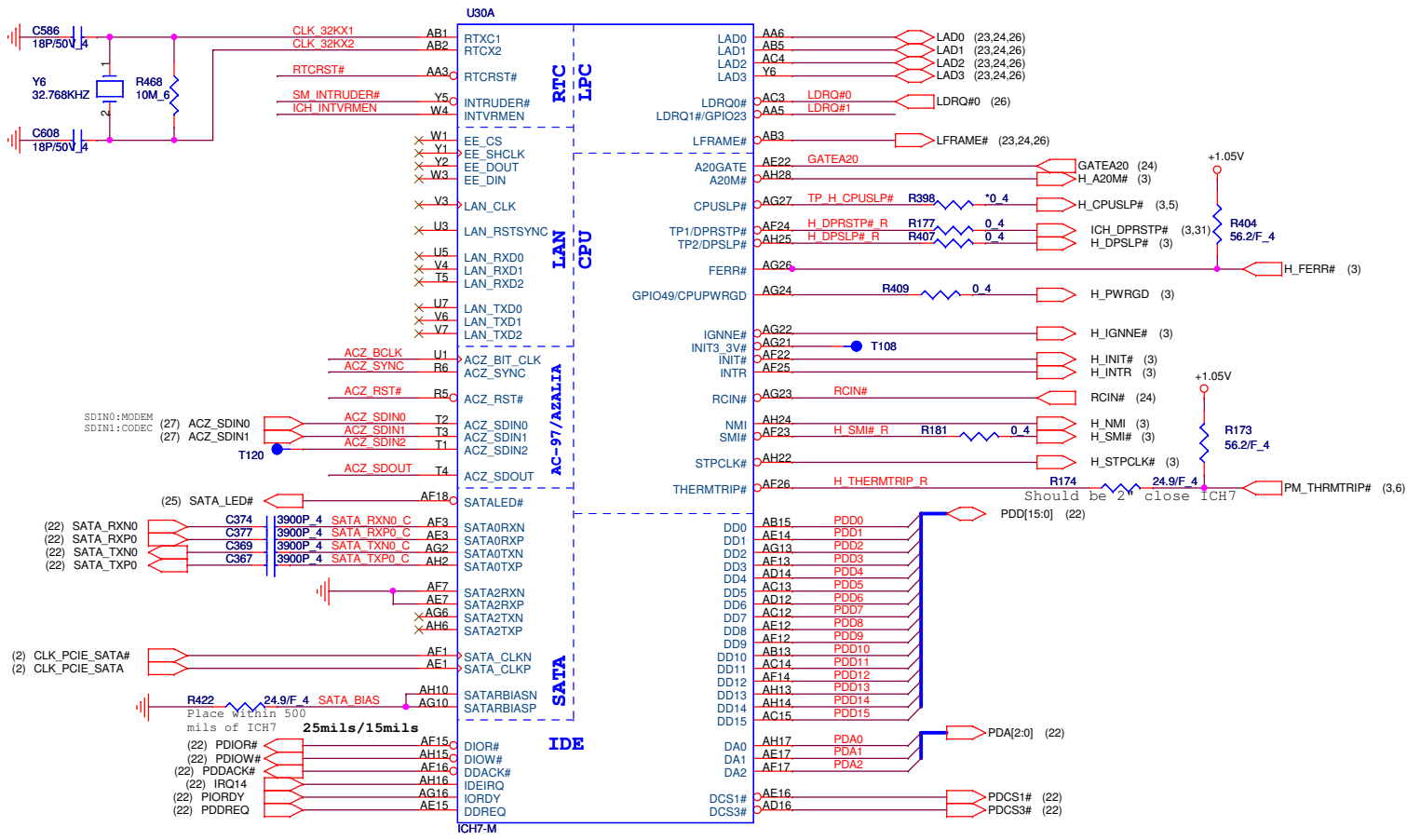
R\_A\_MA[0..13] (7,9)

R\_B\_MA[0..13] (7,9)

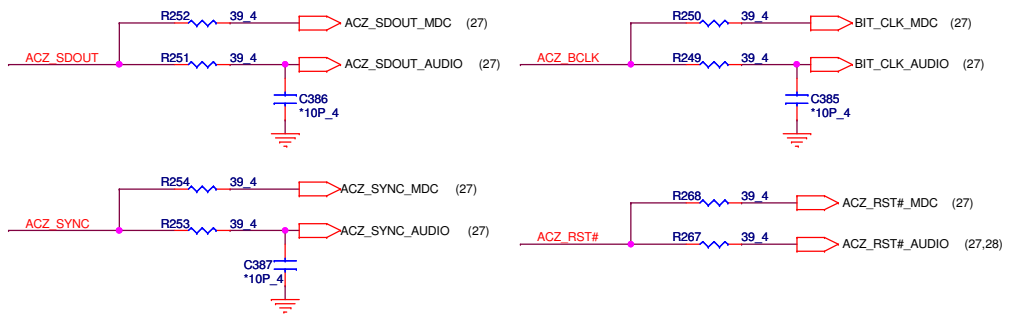


**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR2 RES. ARRAY</b>	1A
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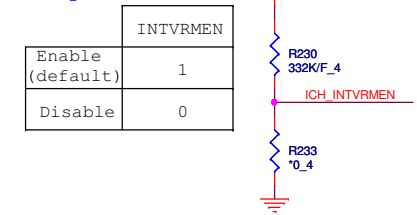


**HDA interface**



COMPONENTS	P/N
945GM	AJSL8Z20T25
ICH7-M	AJSL8YB0T21

**ICH7 internal VR enable strap**

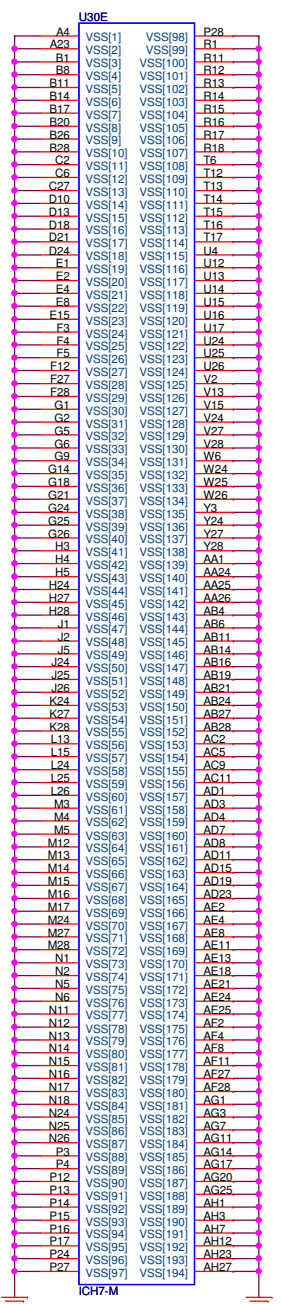
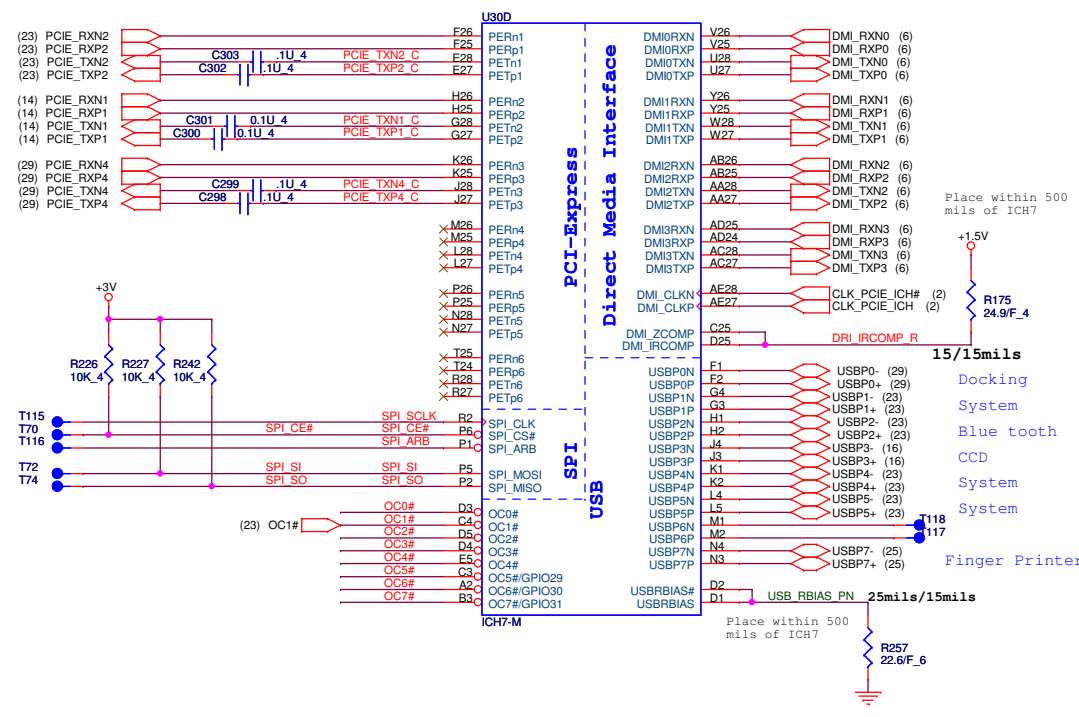


	INTRVDMEN
Enable (default)	1
Disable	0

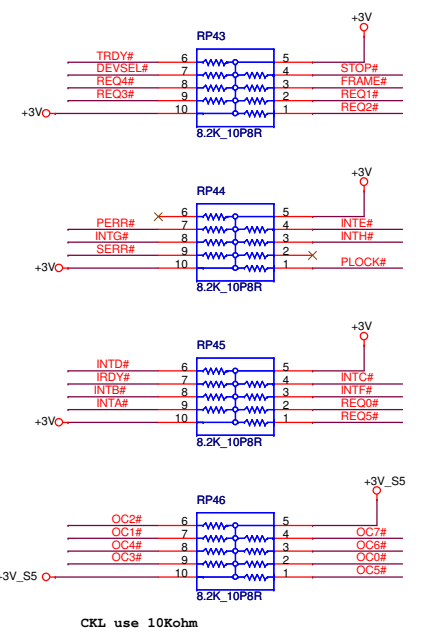
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>ICH7-M (CPU, SATA, IDE,LPC)</b>	1A
Date:	Thursday, March 22, 2007	Sheet 11 of 39

MINI CARD  
Giga LAN  
Docking



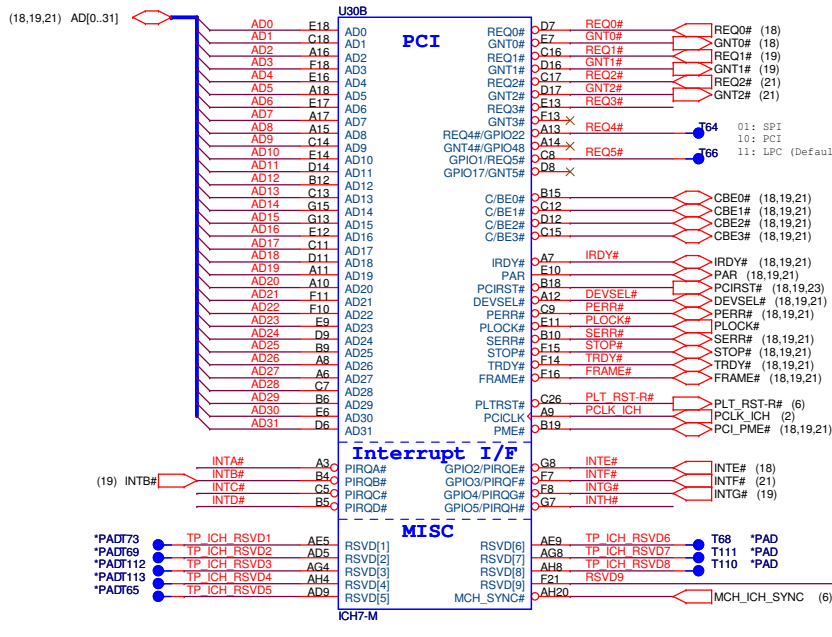
### Pull-UP resistor



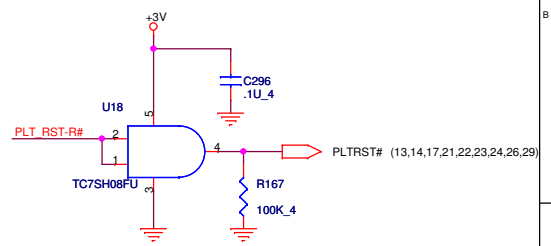
CKL use 10Kohm

### ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



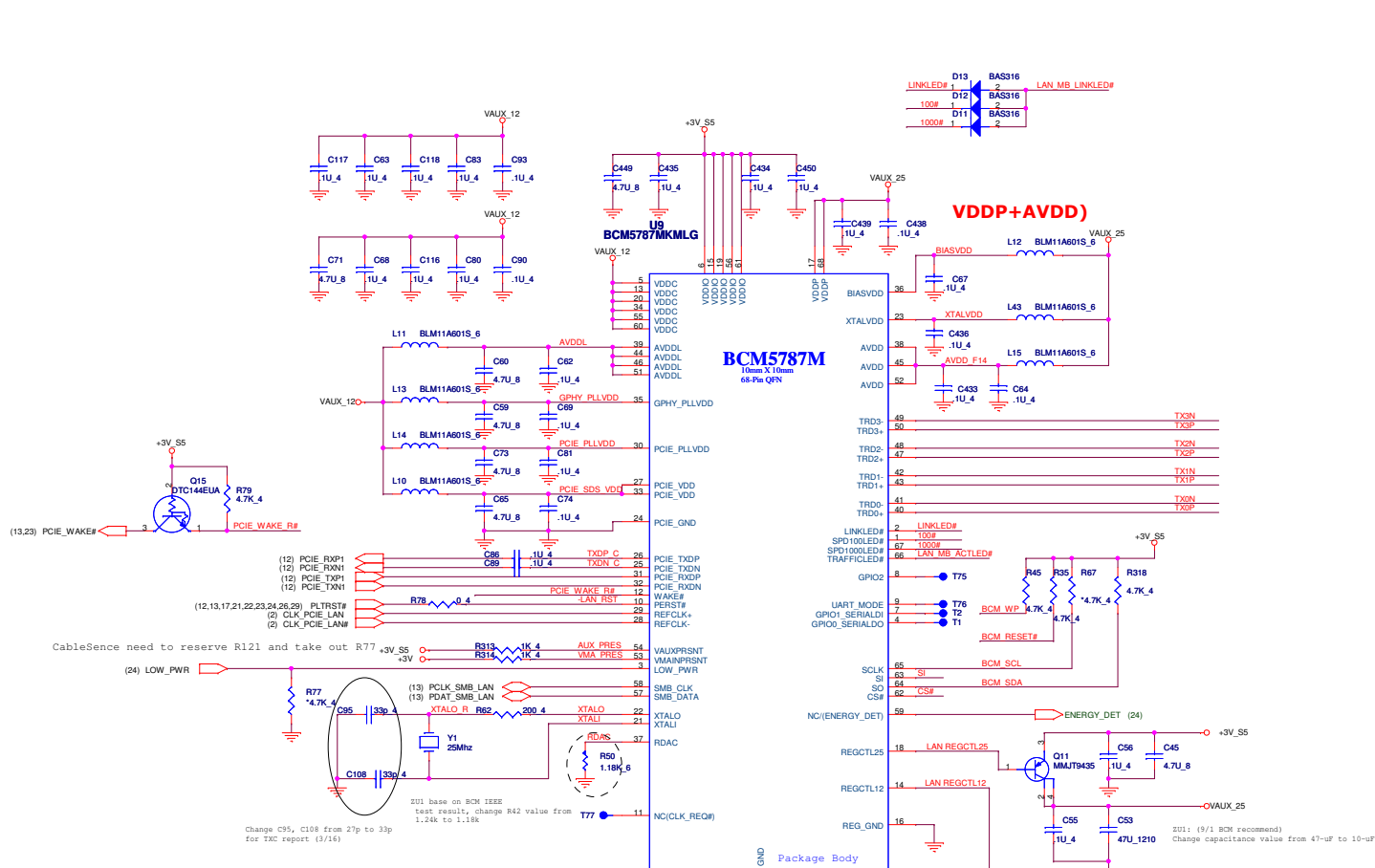
### Platform Reset



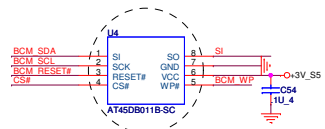




# Giga LAN BCM5787M

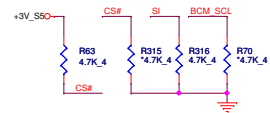


## Flash ROM/EEPROM

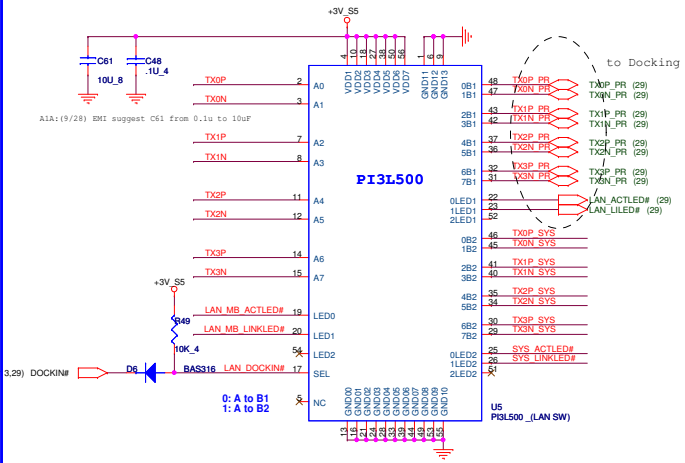


EEPROM Strapping

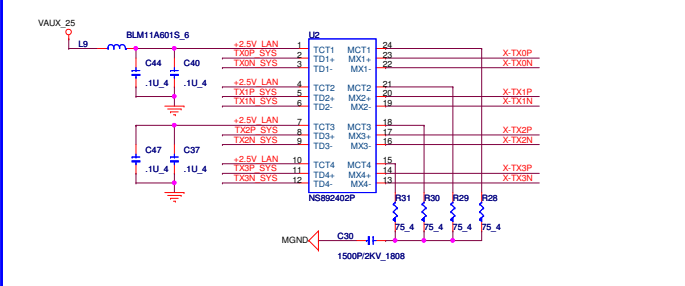
	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1



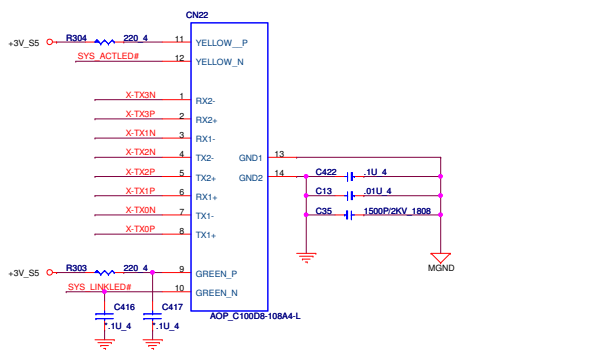
## LAN Switch



## LAN Transformer

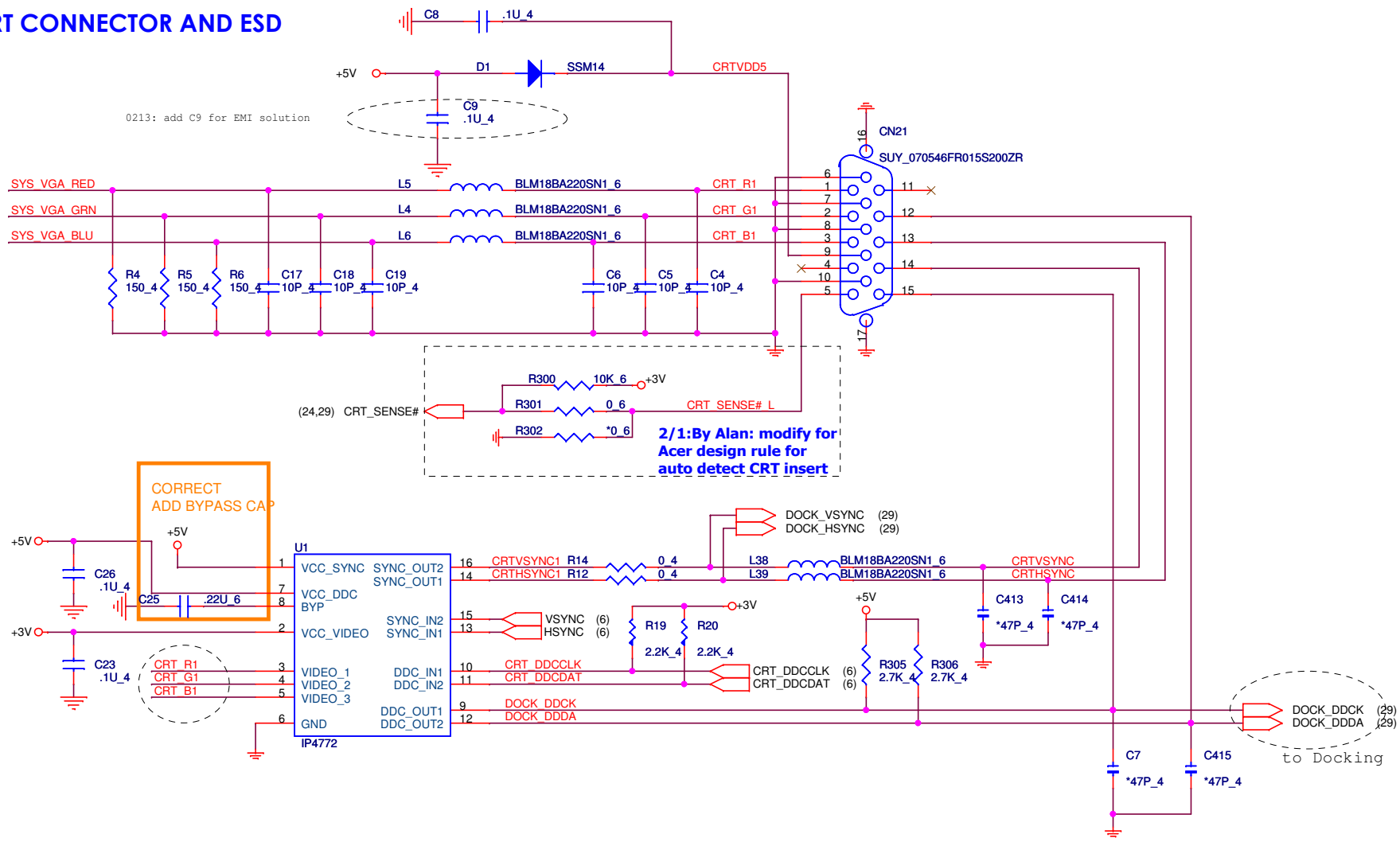


## RJ45

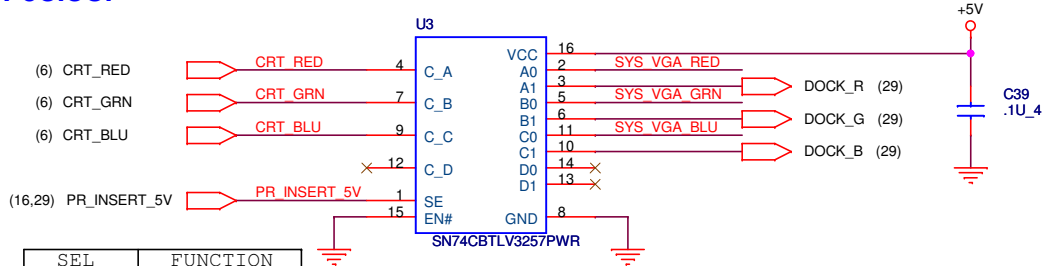


**PROJECT : ZU2**  
**Quanta Computer Inc.**


# CRT CONNECTOR AND ESD



# CRT Select



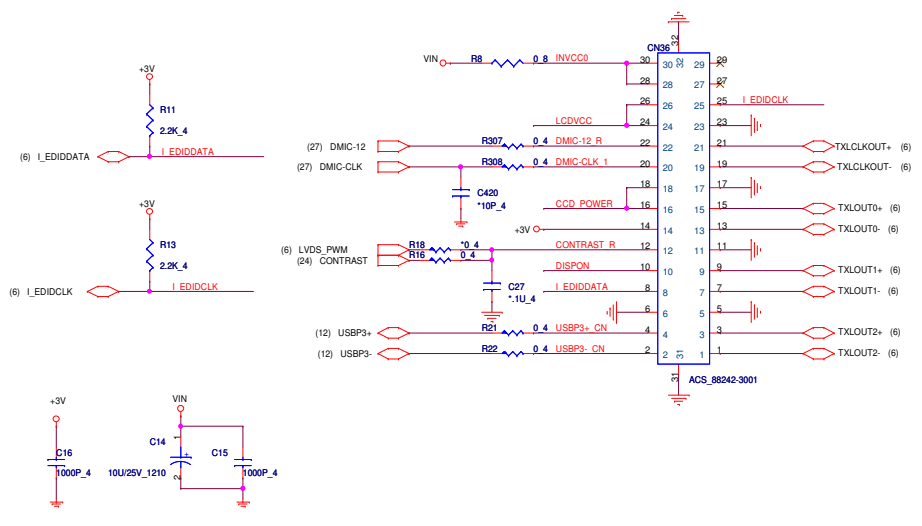
SEL	FUNCTION
LOW	IN_0
HIGH	IN_1



**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CRT</b>	<b>1A</b>
Date:	Thursday, March 22, 2007	Sheet 15 of 39

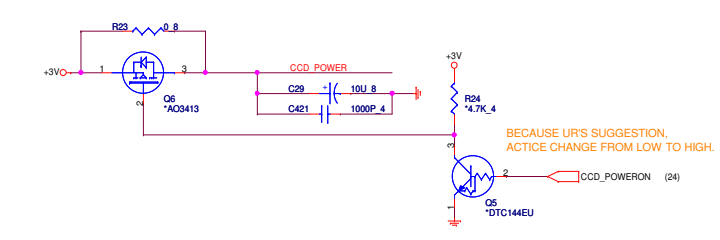
**LVDS**



ZU1:(12/28) EMI request: reserve L-C footprint for debug use (R52,C650)

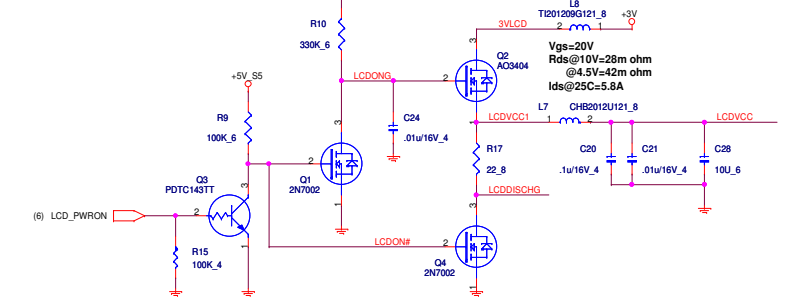
(3/19)Change MB LCD connector pin define(CN3) and LCD cable pin define to cover production line issue (Inverter short with signal to burn system)->ZR1 issue  
 (1)pin 27,29->NC  
 (2)pin 8->INT\_LVDS\_EDIDDATA

**CAMERA MODULE**



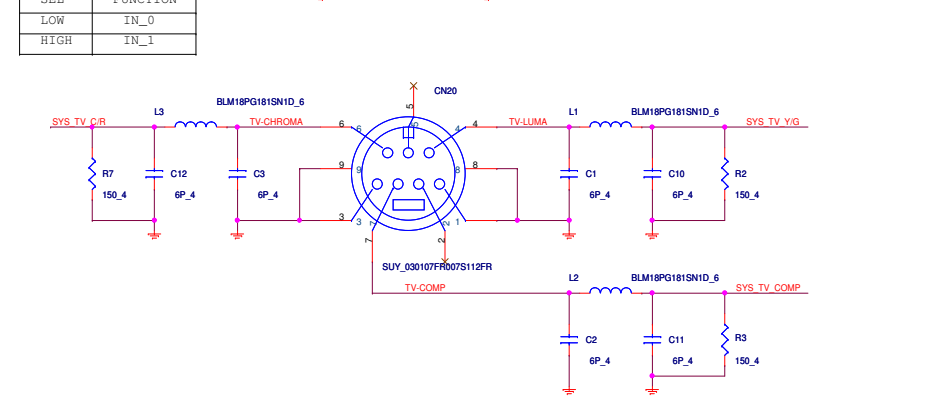
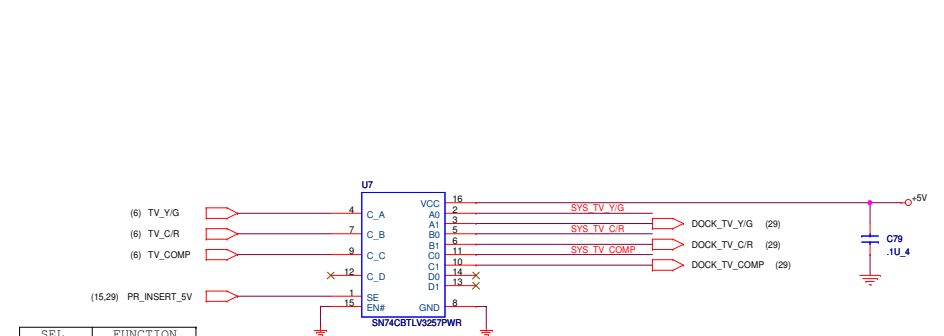
BECAUSE UR'S SUGGESTION, ACTICE CHANGE FROM LOW TO HIGH.

**LCD Power**

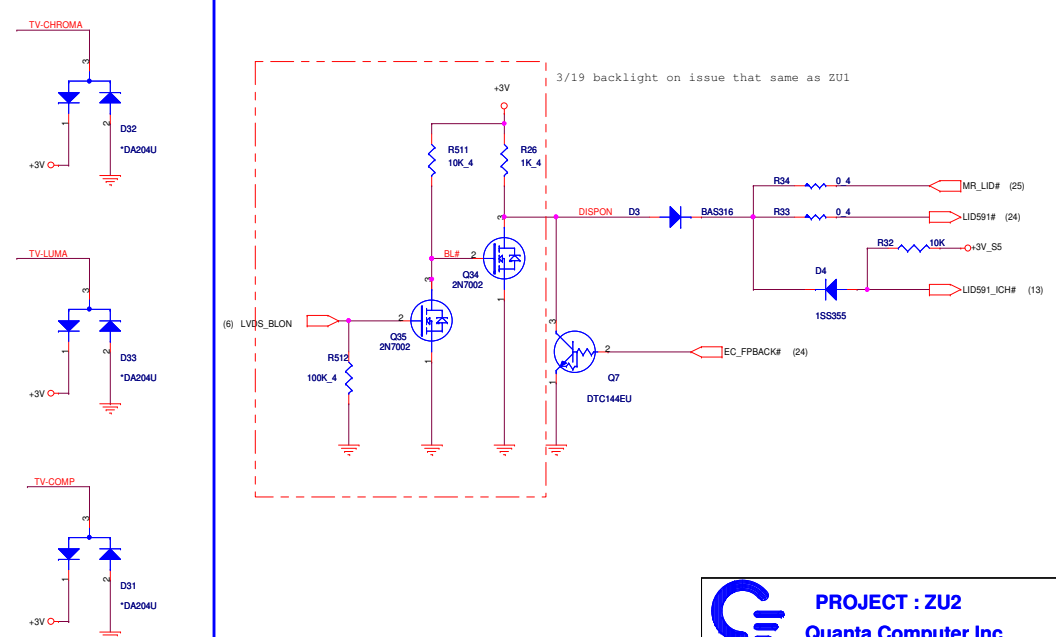


1/29:By Alan: AAT4280 fail on power ON rising time and falling time. EA.Additionally, some LCD panels will have garbage. follow ZR1 circuit.

**TV Out (SVHS) MiniDIN 7-pin**

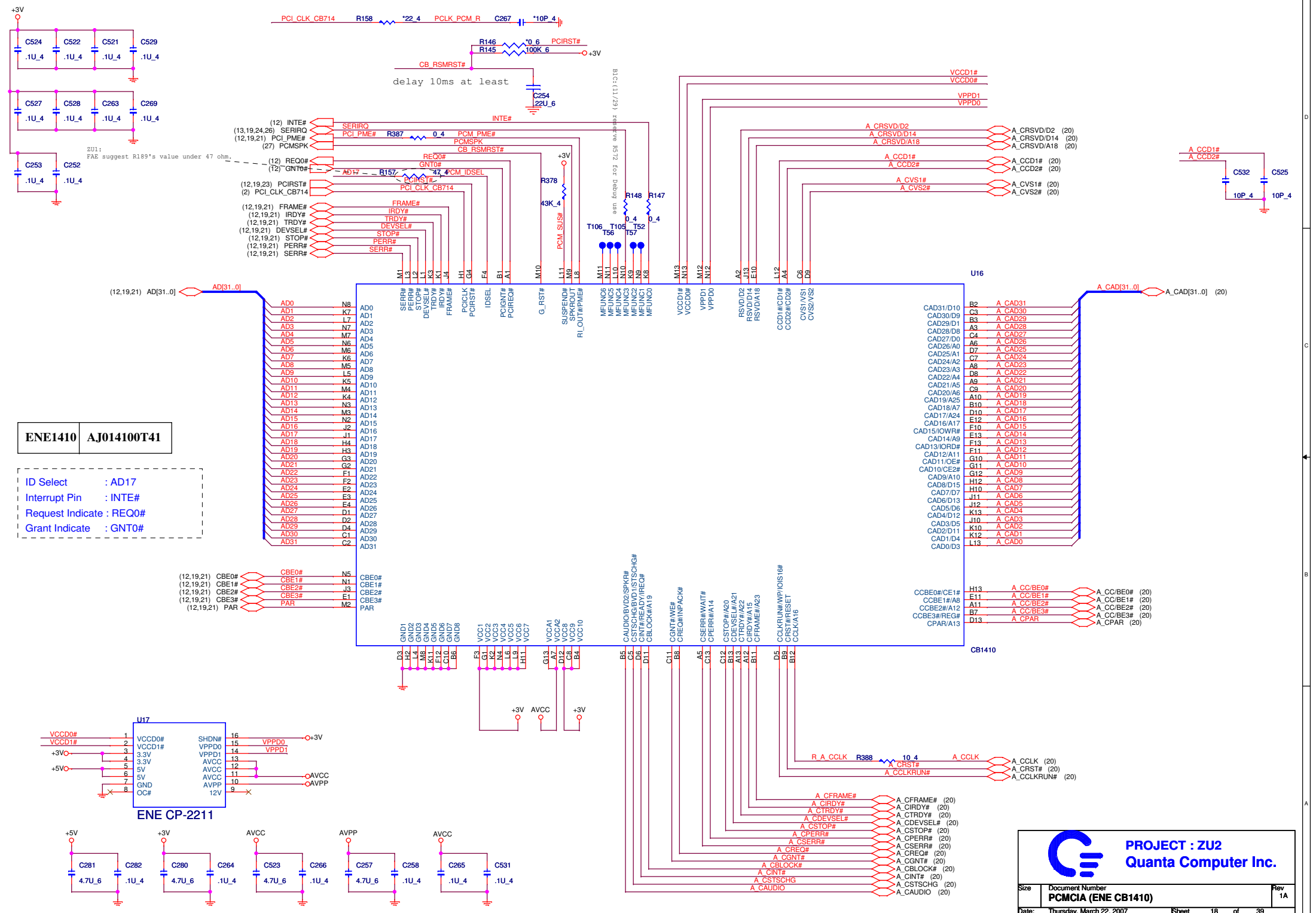


**MR Sensor**



3/19 backlight on issue that same as ZU1



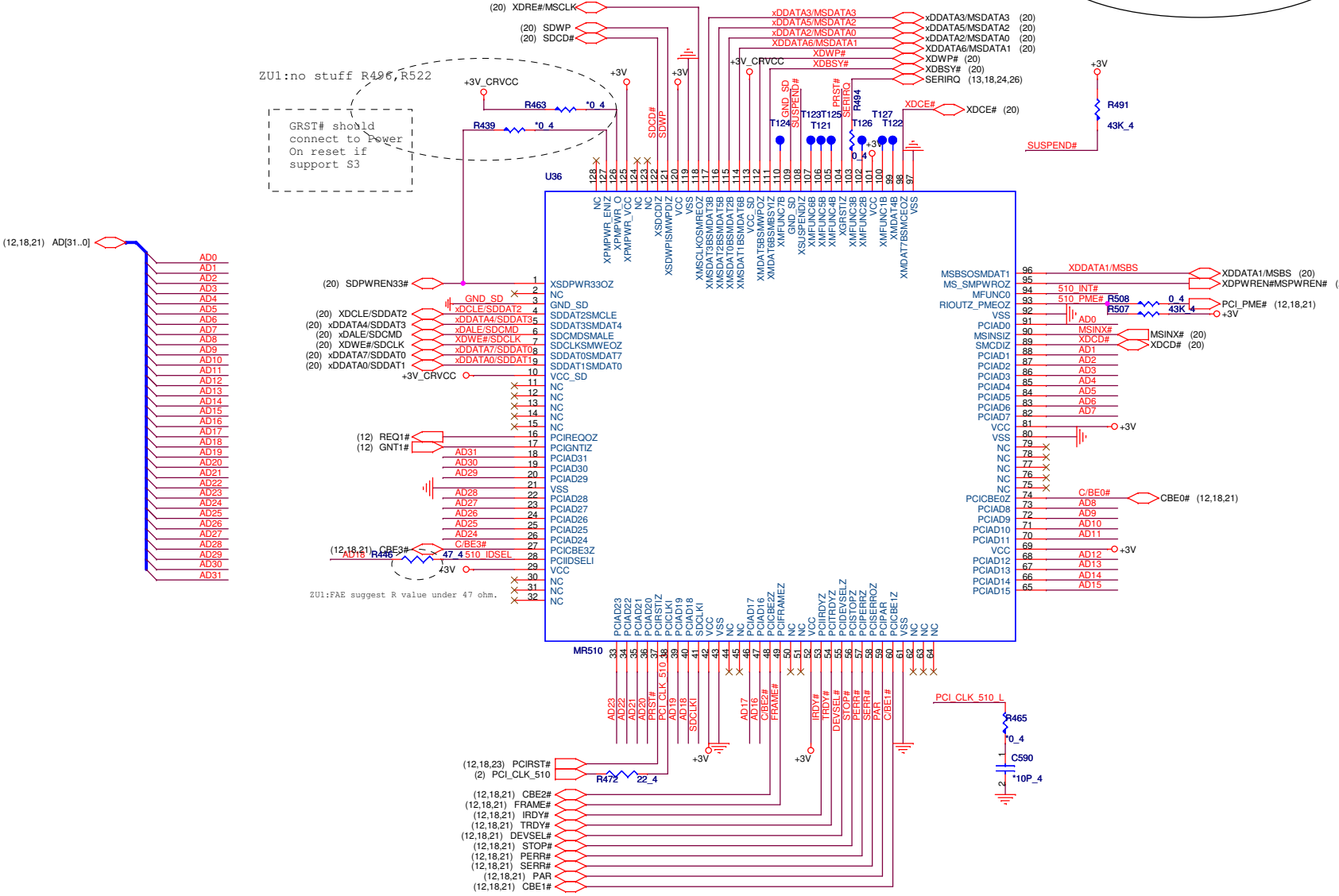


**ENE1410 AJ014100T41**

ID Select : AD17  
 Interrupt Pin : INTE#  
 Request Indicate : REQ0#  
 Grant Indicate : GNT0#



ID Select : AD18  
 Interrupt Pin : INTG#  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#



ZU1: no stuff R496, R522

GRST# should connect to Power On reset if support S3

(20) SDPWREN33#

(20) XDCLE/SDDAT2

(20) XDDATA4/SDDAT3

(20) XDALE/SDCMD

(20) XDWE#/SDCLK

(20) XDDATA7/SDDAT0

(20) XDDATA0/SDDAT1

(12) REQ1#

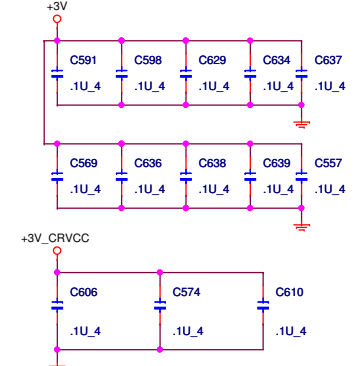
(12) GNT1#

(12,18,21) CBE3#

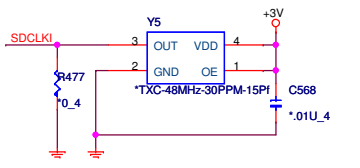
(12,18,21) CBE0#

ZU1:FAE suggest R value under 47 ohm.

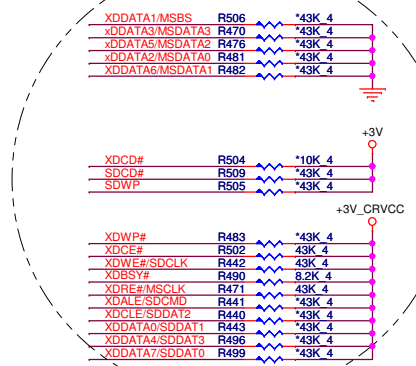
### Decoupling CAP.



### 48MHz CLK



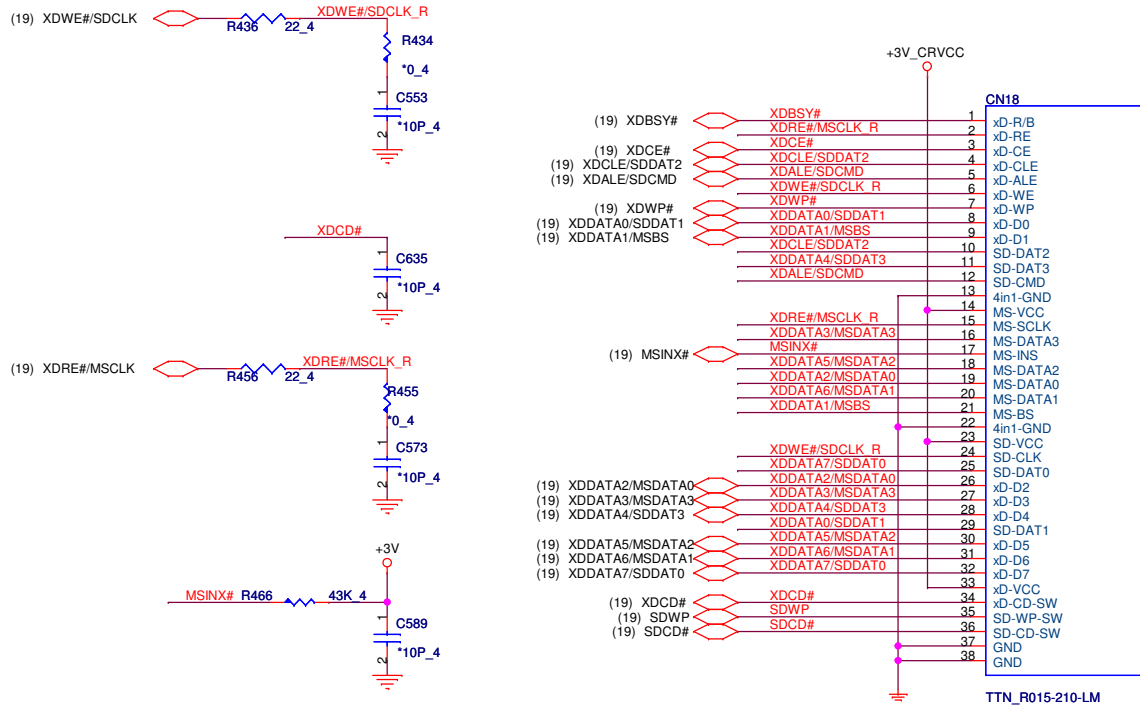
### PU/PD



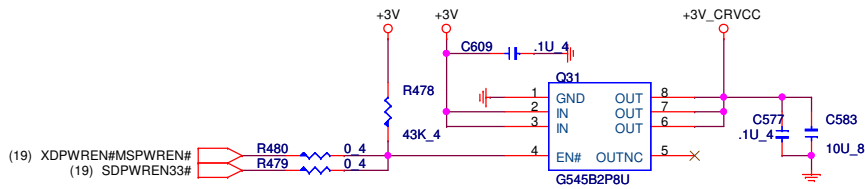
0213: follow ZU1 for cost down issue with FAE

**PROJECT : ZU2**  
**Quanta Computer Inc.**

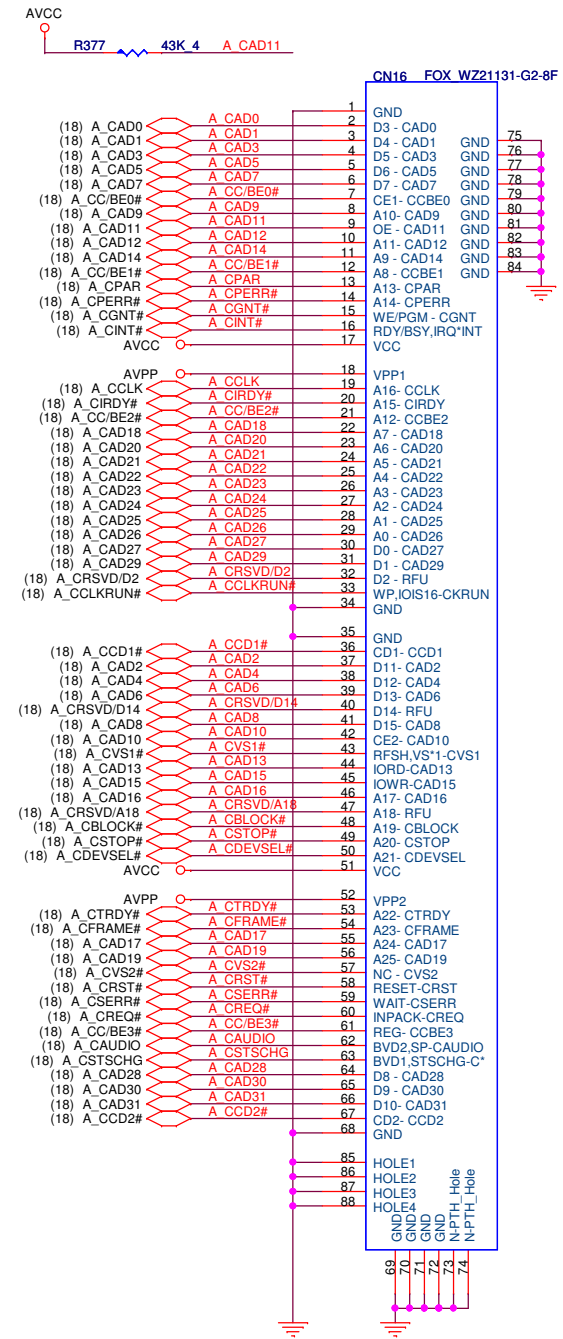
# CardReader




# CardReader Power switch



# PCMCIA



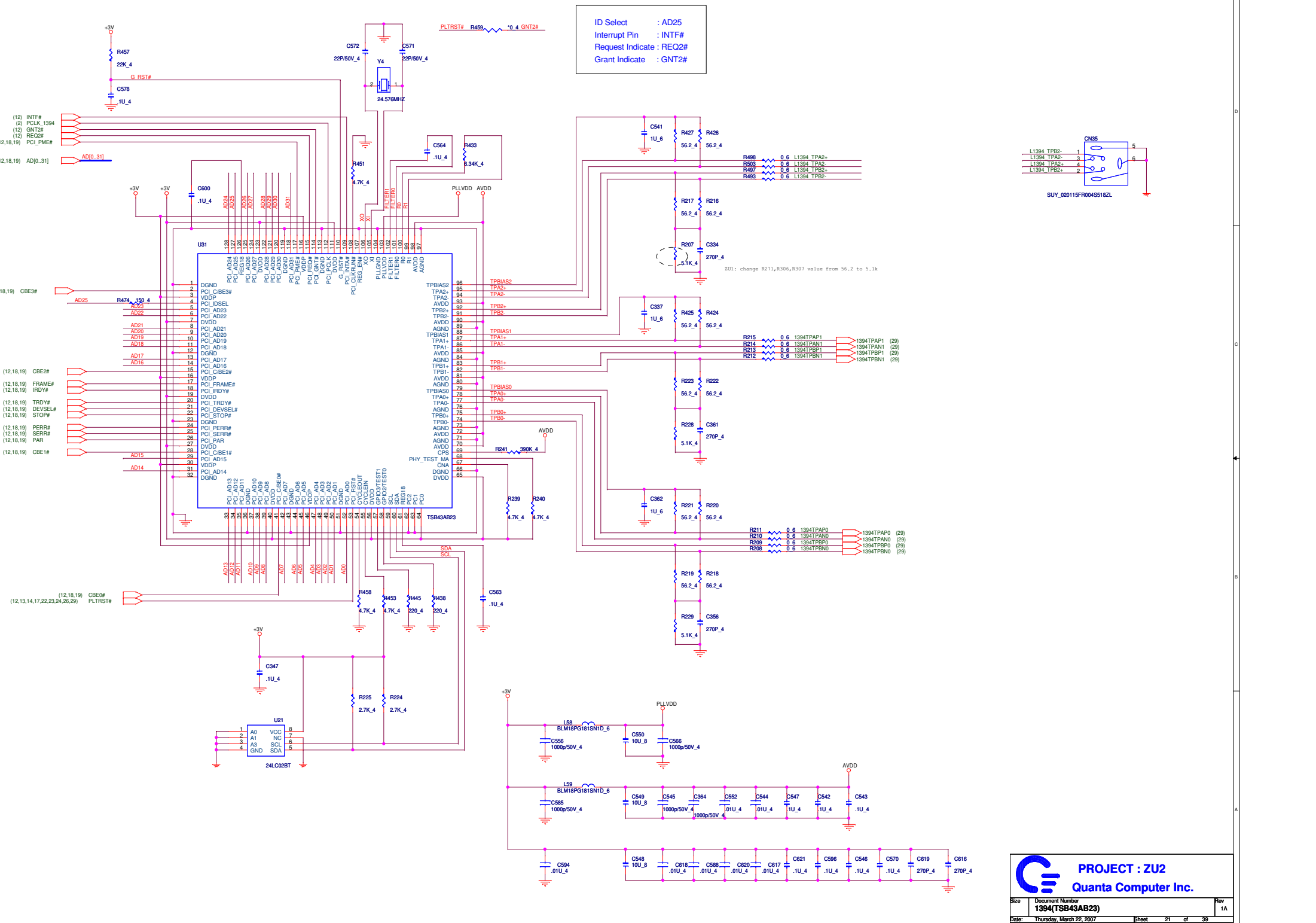


## PROJECT : ZU2

### Quanta Computer Inc.

Size	Document Number	Rev
	<b>CARD Reader &amp; PCMCIA SLOT</b>	1A
Date:	Thursday, March 22, 2007	Sheet 20 of 39

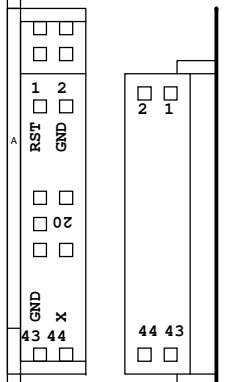
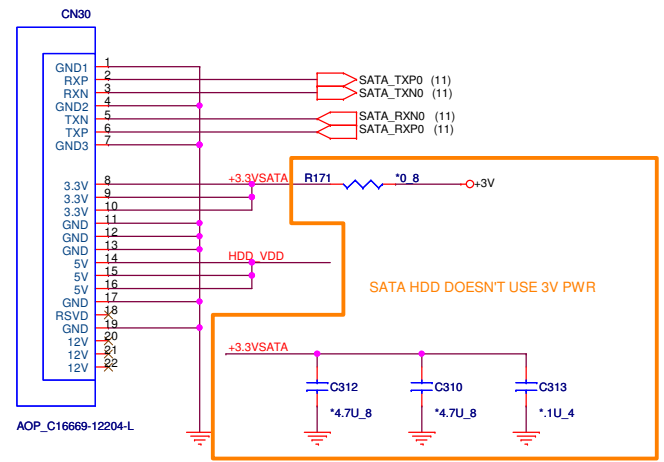
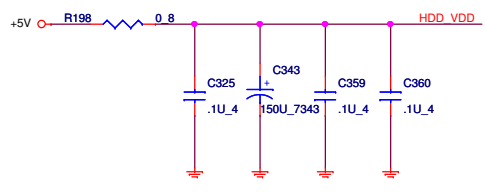
ID Select : AD25  
 Interrupt Pin : INTF#  
 Request Indicate : REQ2#  
 Grant Indicate : GNT2#



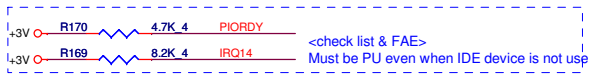
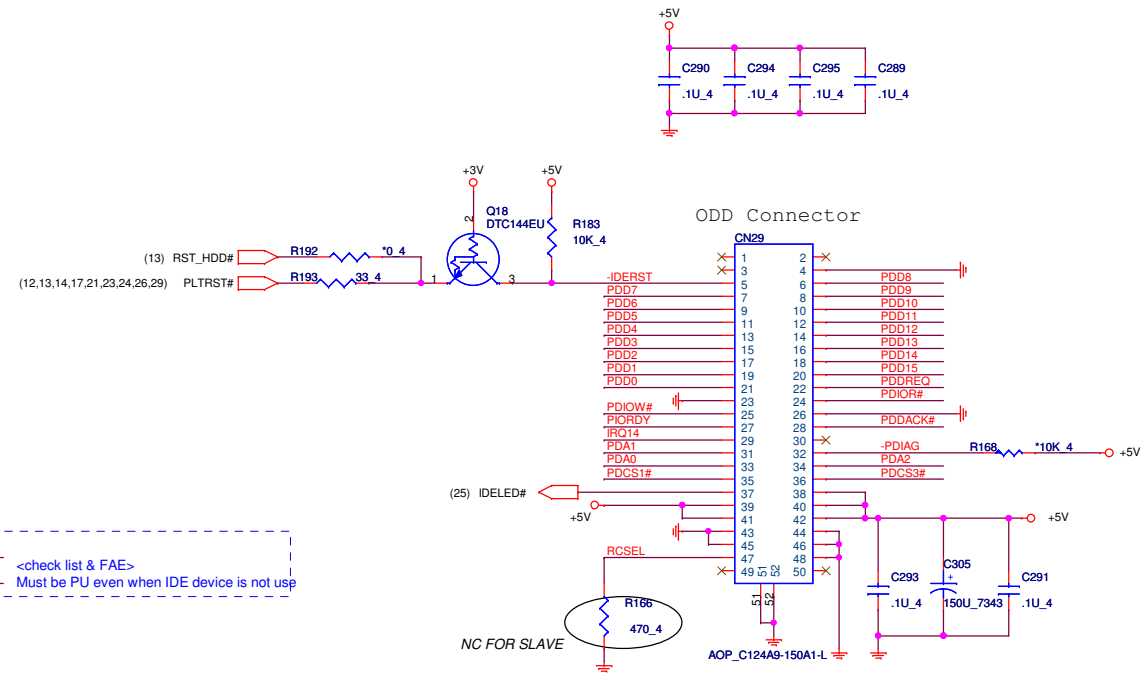
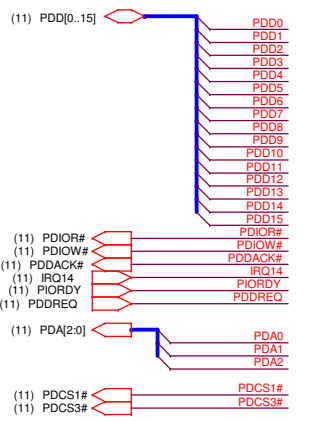
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>1394(TSB43AB23)</b>	1A
Date:	Thursday, March 22, 2007	Sheet 21 of 39

**SATA HDD**



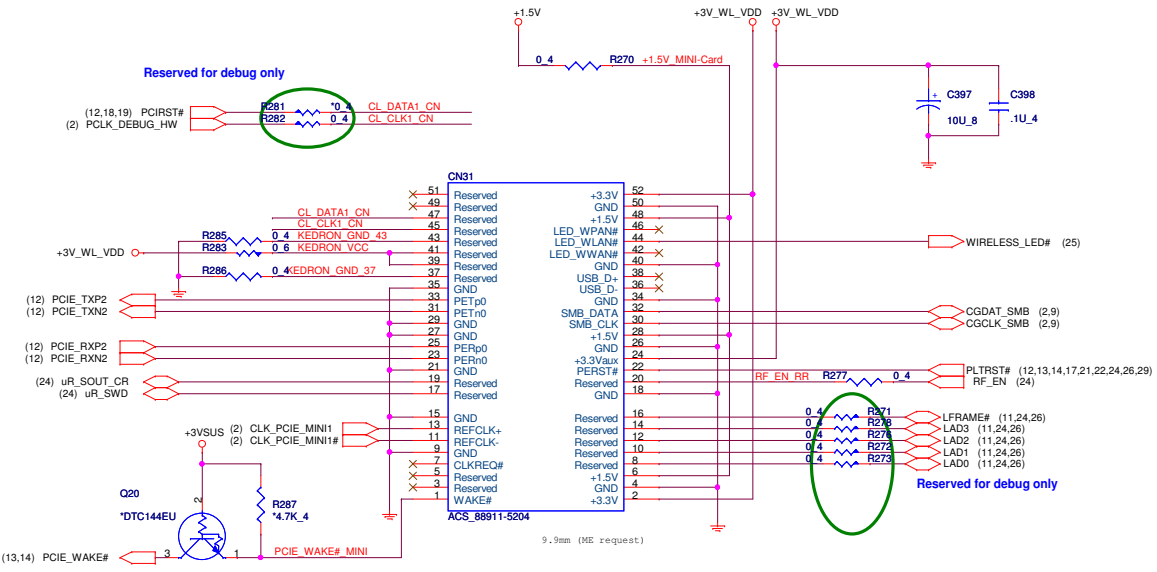
**PATA ODD**



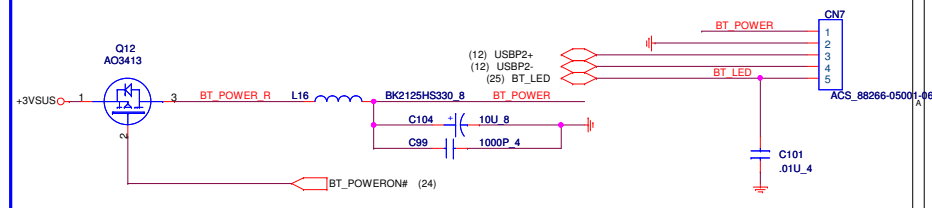
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>SATA-HDD &amp; PATA-ODD</b>	1A
Date:	Thursday, March 22, 2007	Sheet 22 of 39

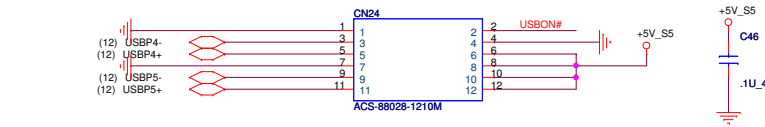
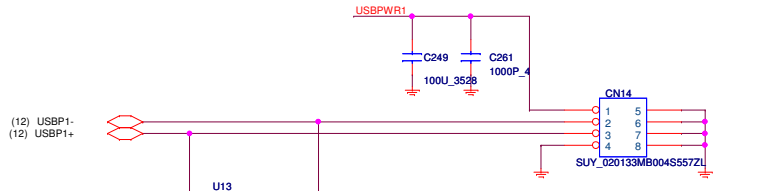
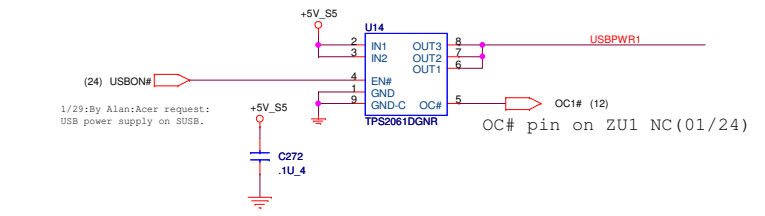
# MINI-Card




# BLUETOOTH MODULE CONNECTOR



# System USB

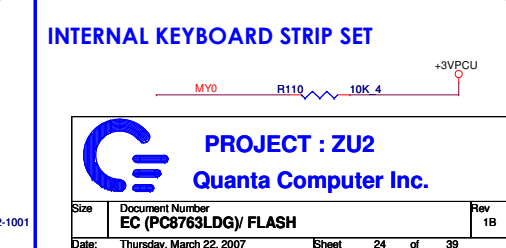
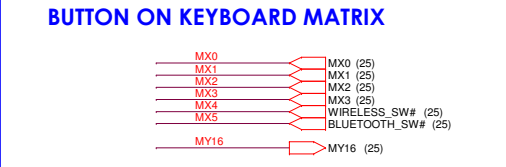
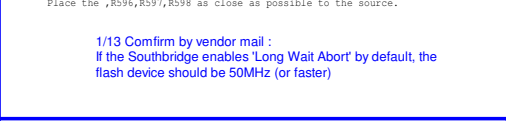
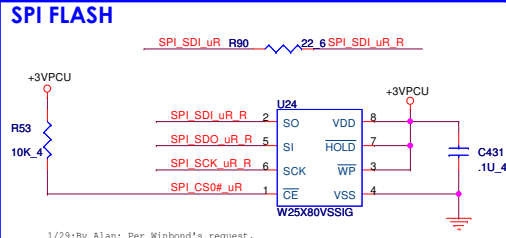
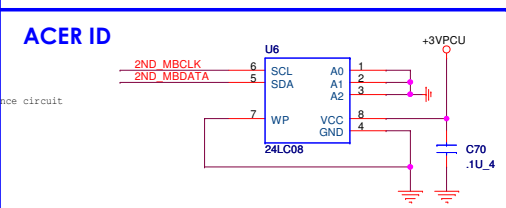
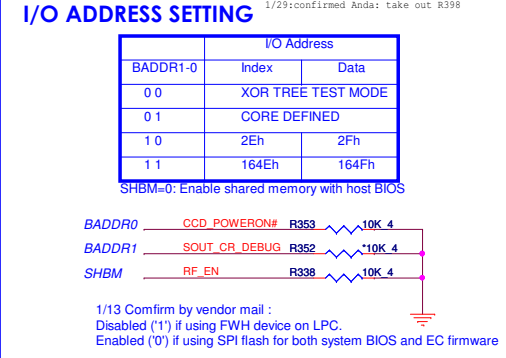
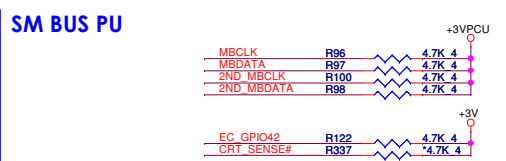
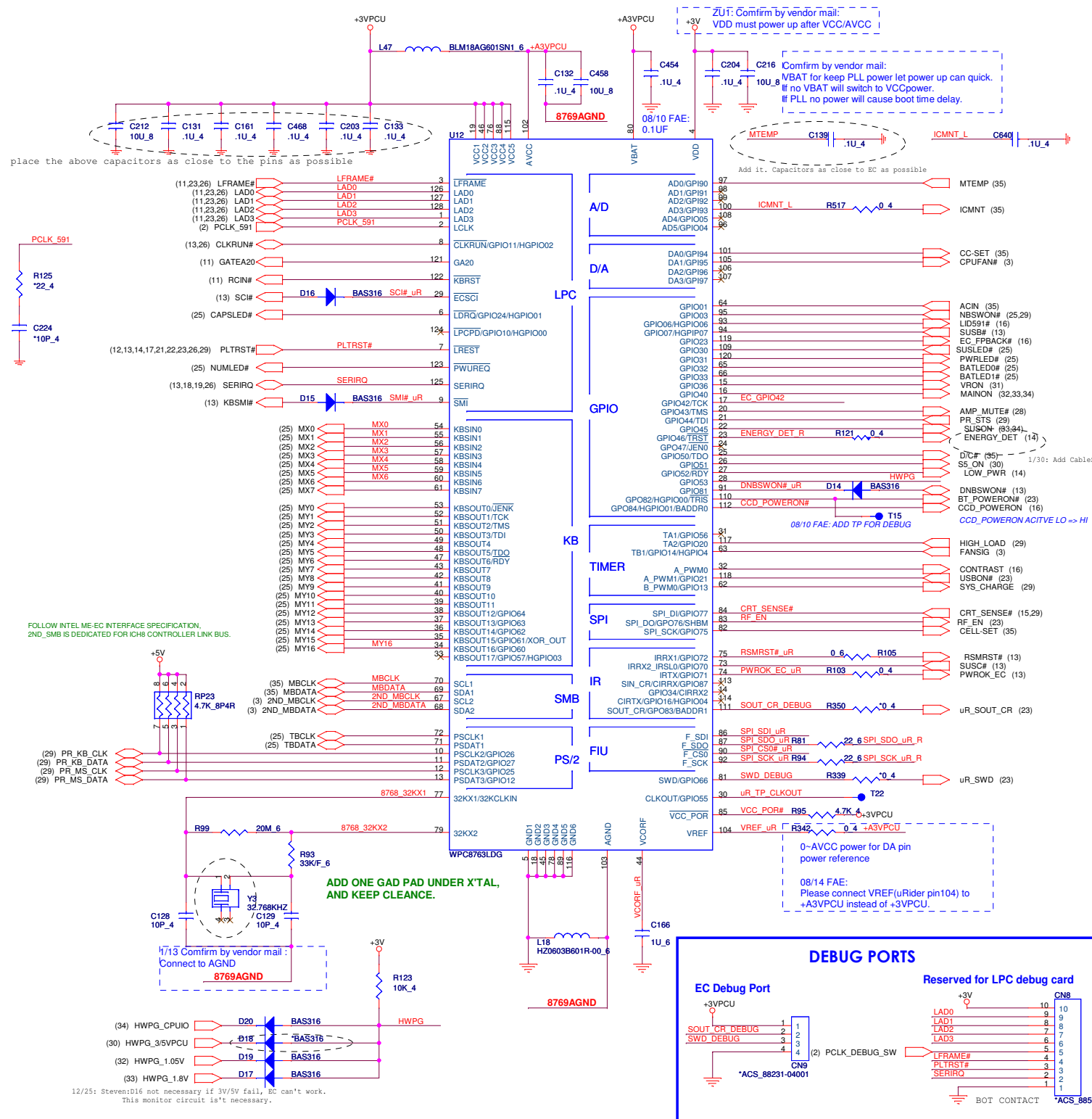




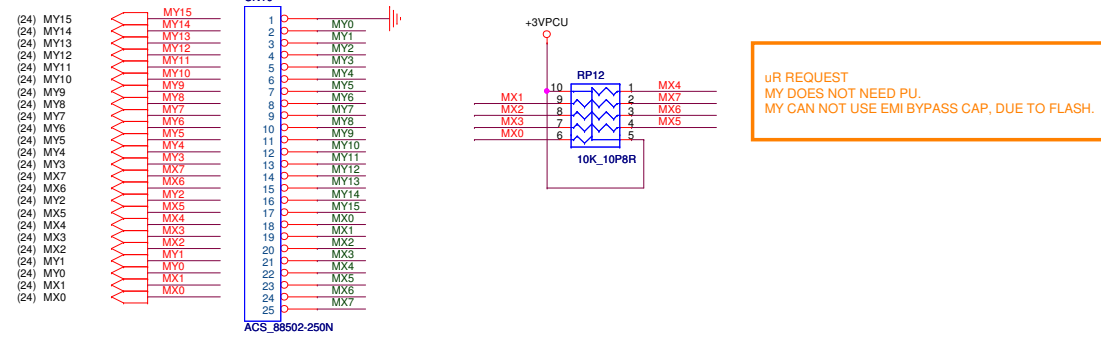
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Mini card/USB/Bluetooth</b>	<b>1B</b>
Date:	Wednesday, March 28, 2007	Sheet 23 of 39

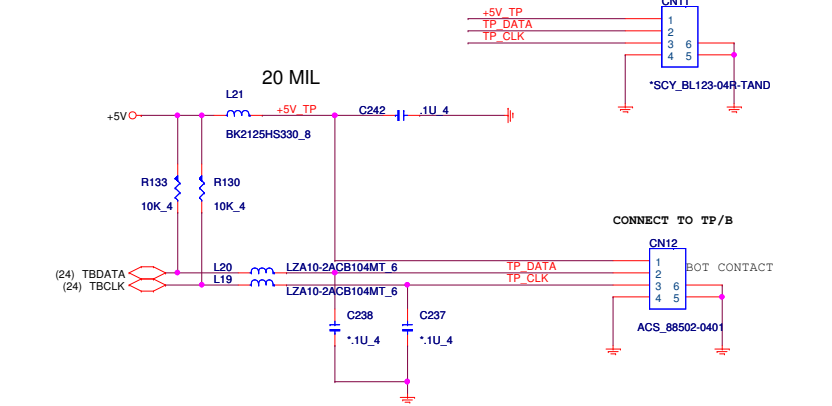




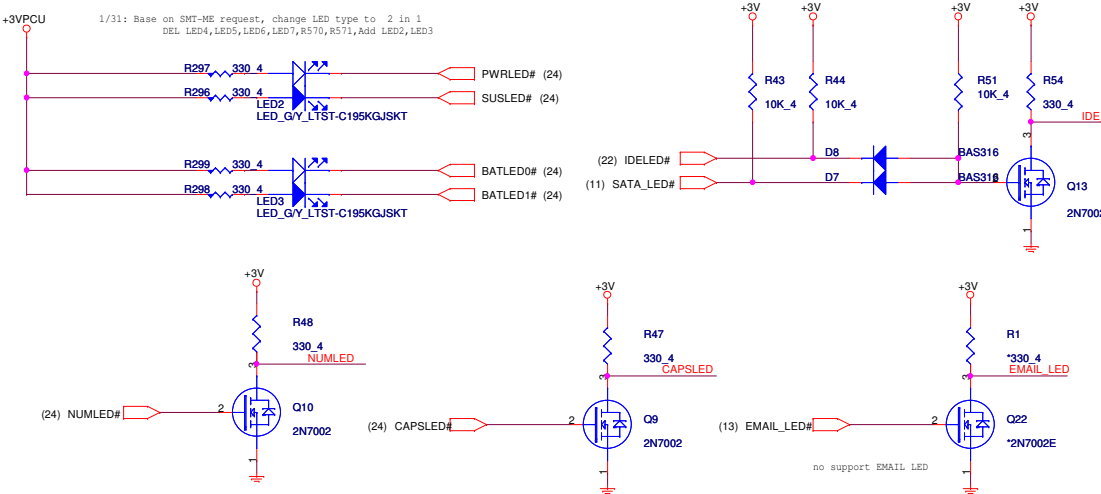
# INT K/B



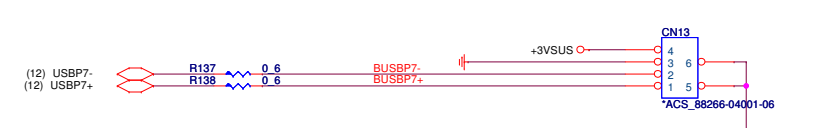
# TOUCH PAD



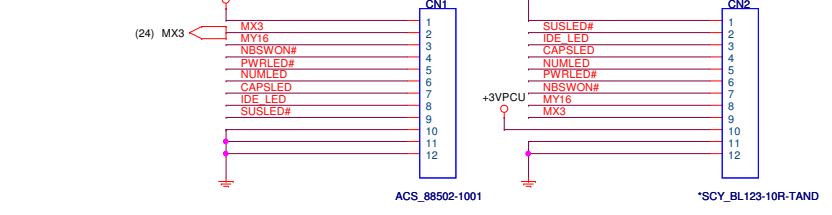
# LED



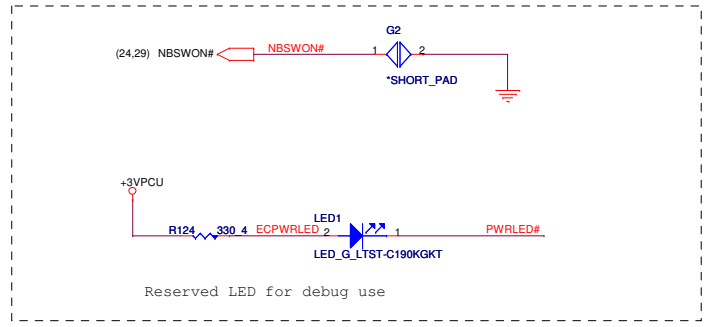
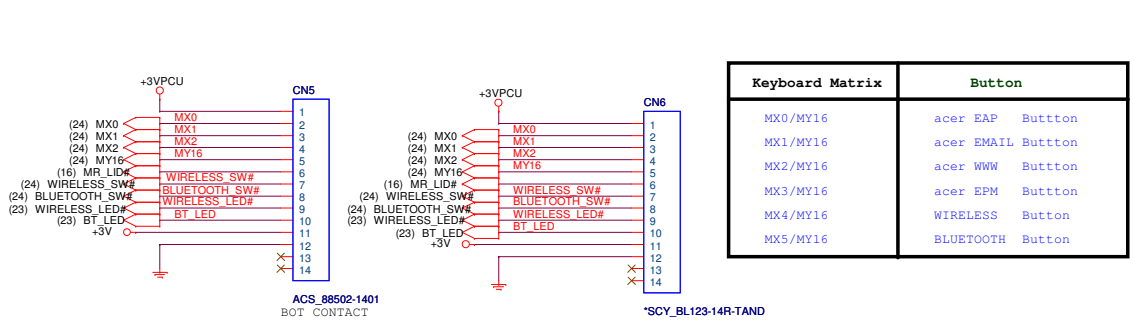
# Finger Printer



# LED Board

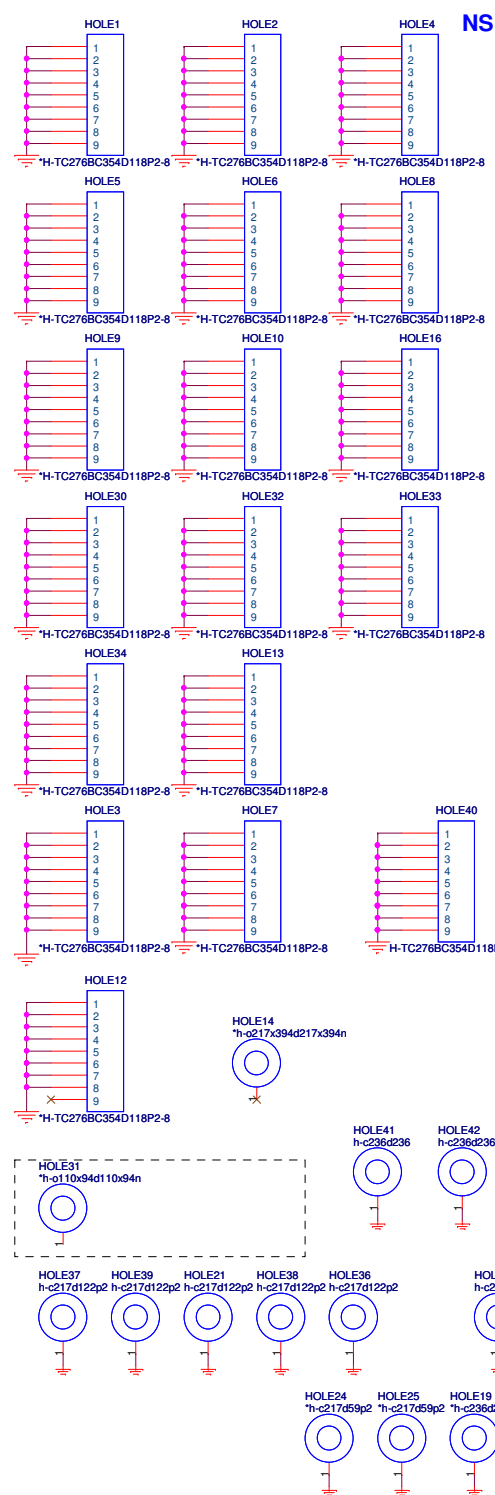


# Function Board

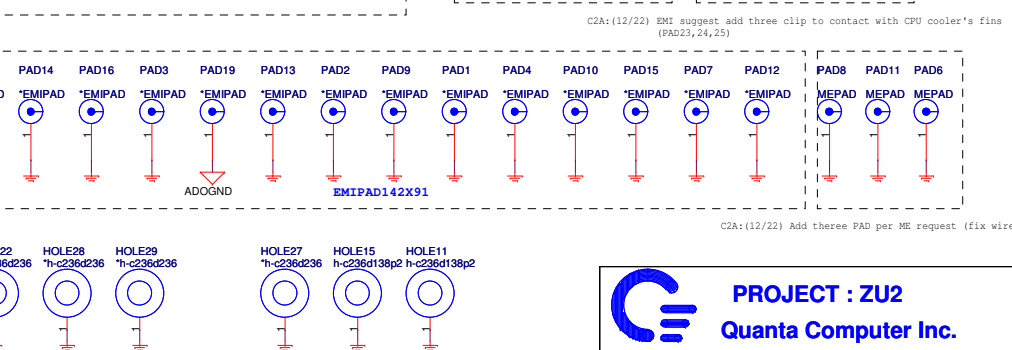
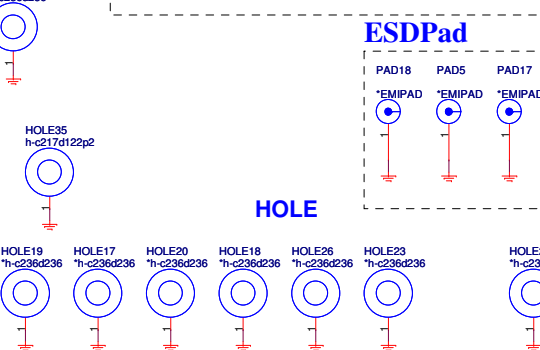
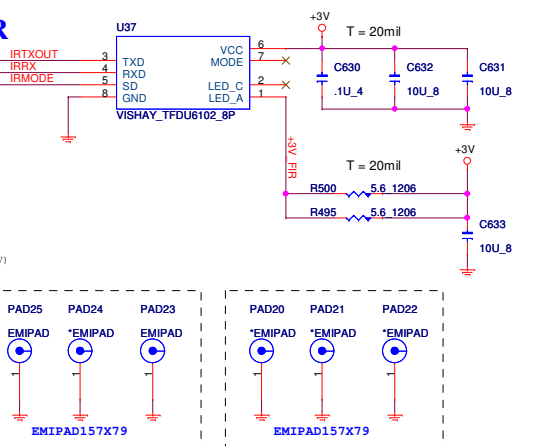
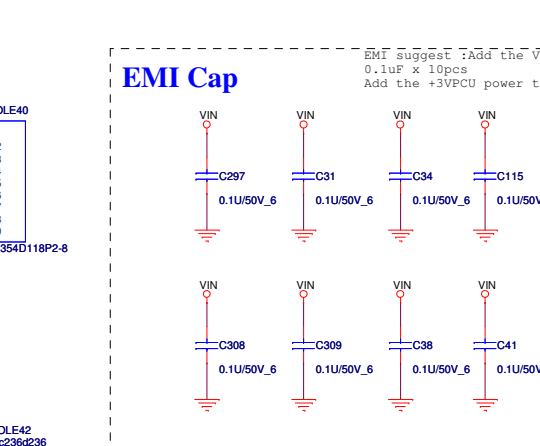
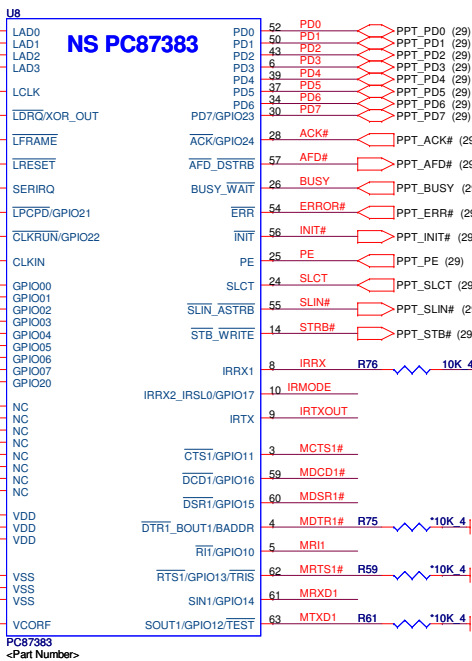
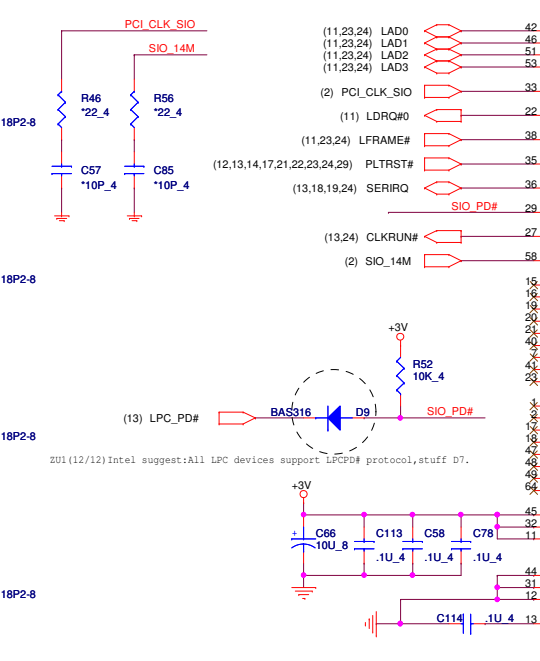


**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>SWITCH,LED,KB,Finger,TP</b>	1B
Date:	Tuesday, March 27, 2007	Sheet 25 of 39



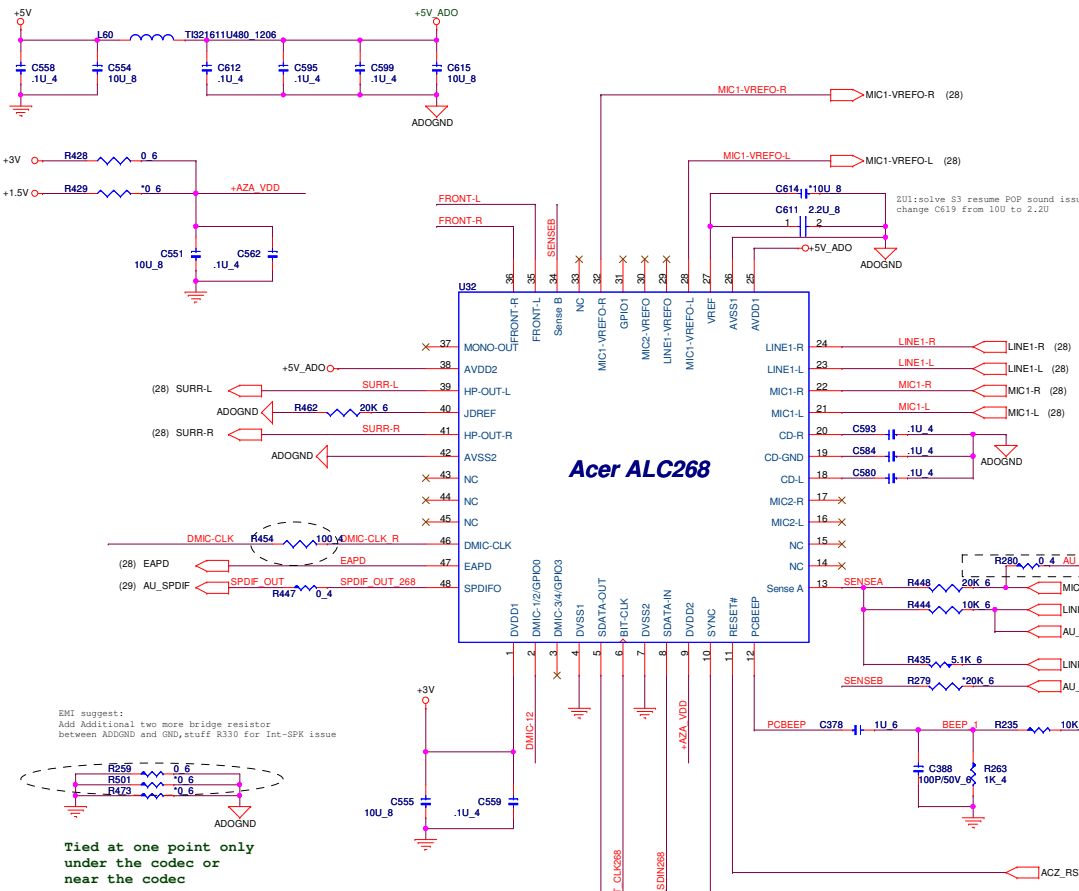
### NS SIO PC87383



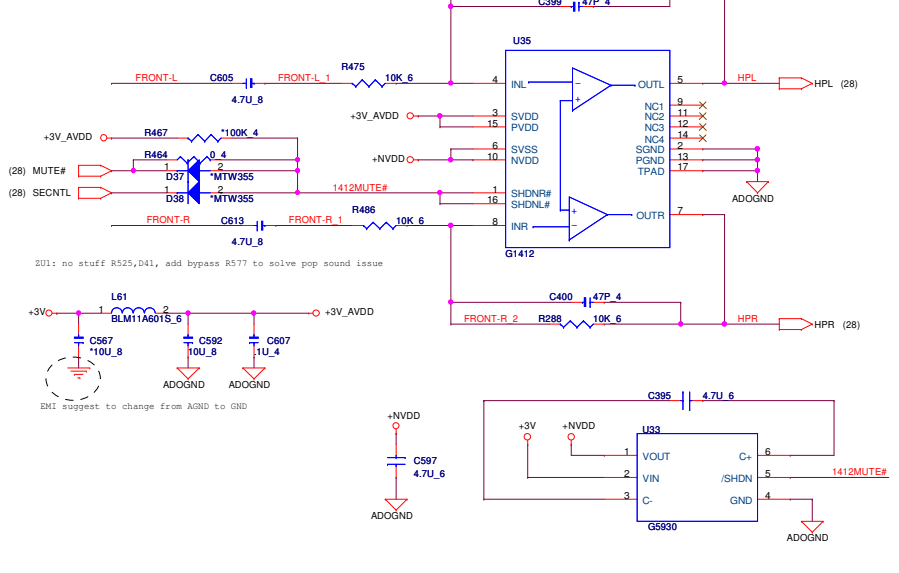
**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size: Document Number: SUPER-IO/FIR/HOLE Rev: 1A  
 Date: Thursday, March 22, 2007 Sheet: 26 of 39

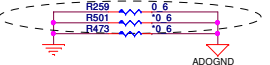
**CODEC (ALC268)**



**LINE OUT Amplifier**

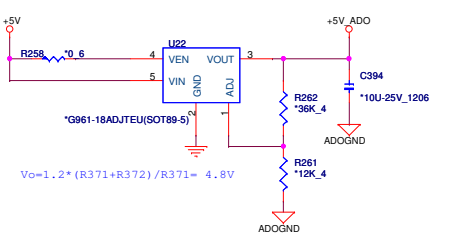


EMI suggest:  
Add Additional two more bridge resistor between ADOGND and GND,stuff R330 for Int-SPK issue

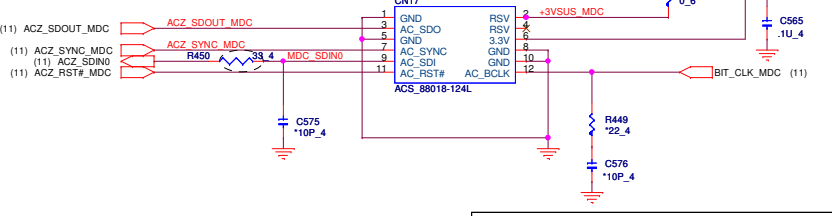


Tied at one point only under the codec or near the codec

**Reserve Audio power**



**MDC**

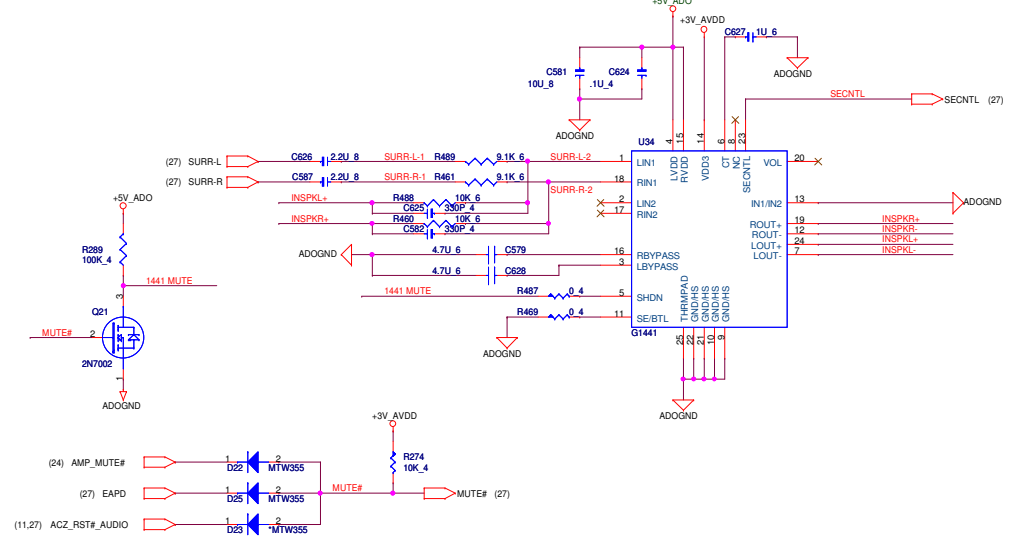


**PROJECT : ZU2**  
**Quanta Computer Inc.**

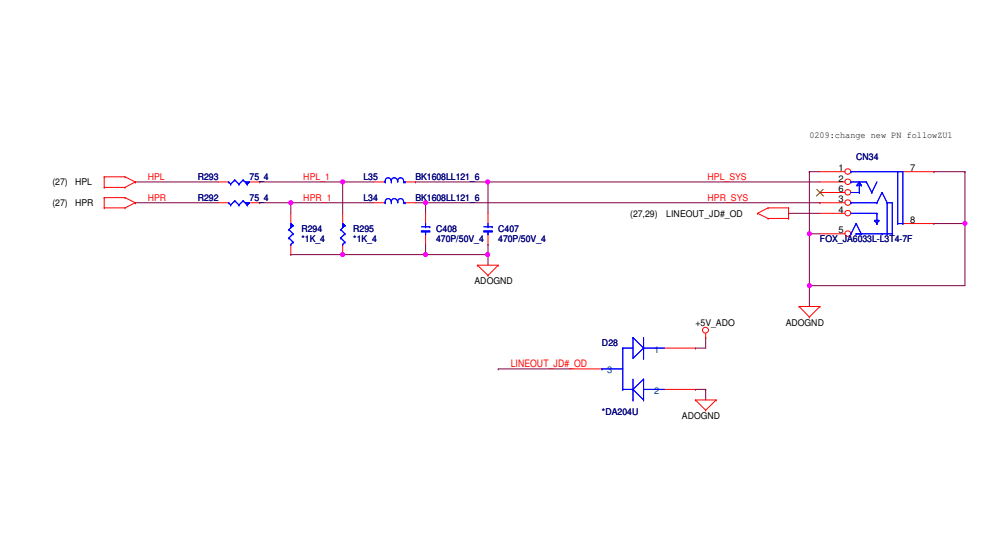
Size Document Number  
**AUDIO(ALC268)/AMP/MDC** Rev 1A

Date: Thursday, March 22, 2007 Sheet 27 of 39

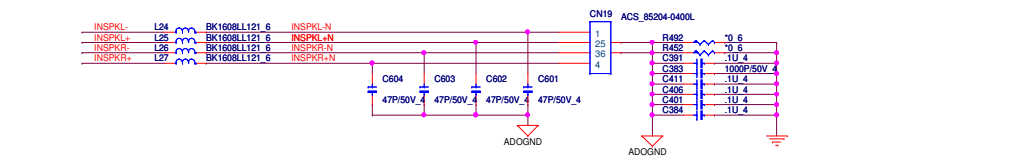
# Speaker Amplifier



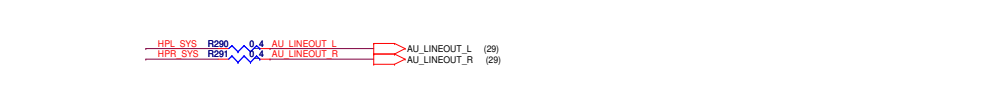
# SYSTEM LINE OUT



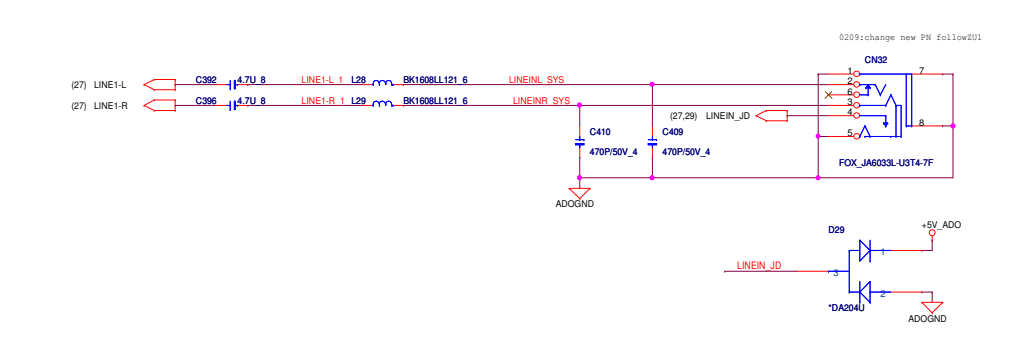
# SPEAKER



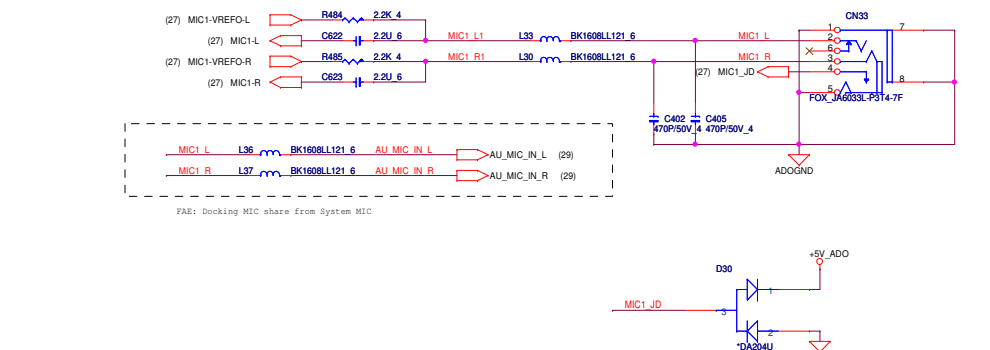
# Docking LINE OUT/SPDIF



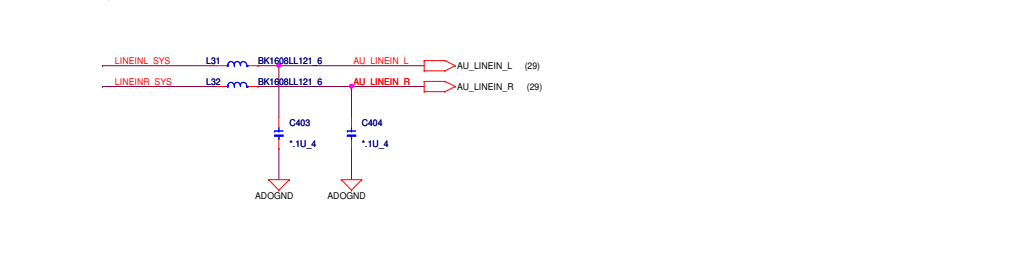
# SYSTEM LINE IN



# SYSTEM MIC

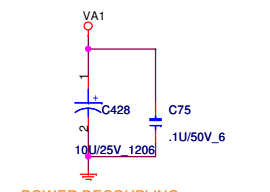
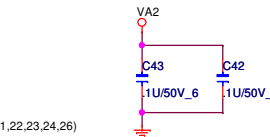
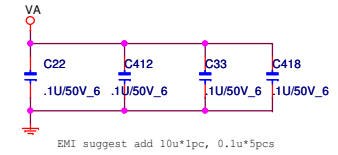


# Docking LINE IN

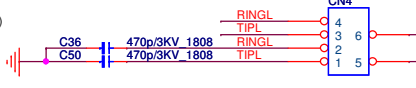


### 3/16 Modify D5 Footprint from SBM1040-3P to SBM1040-3P-ZU1

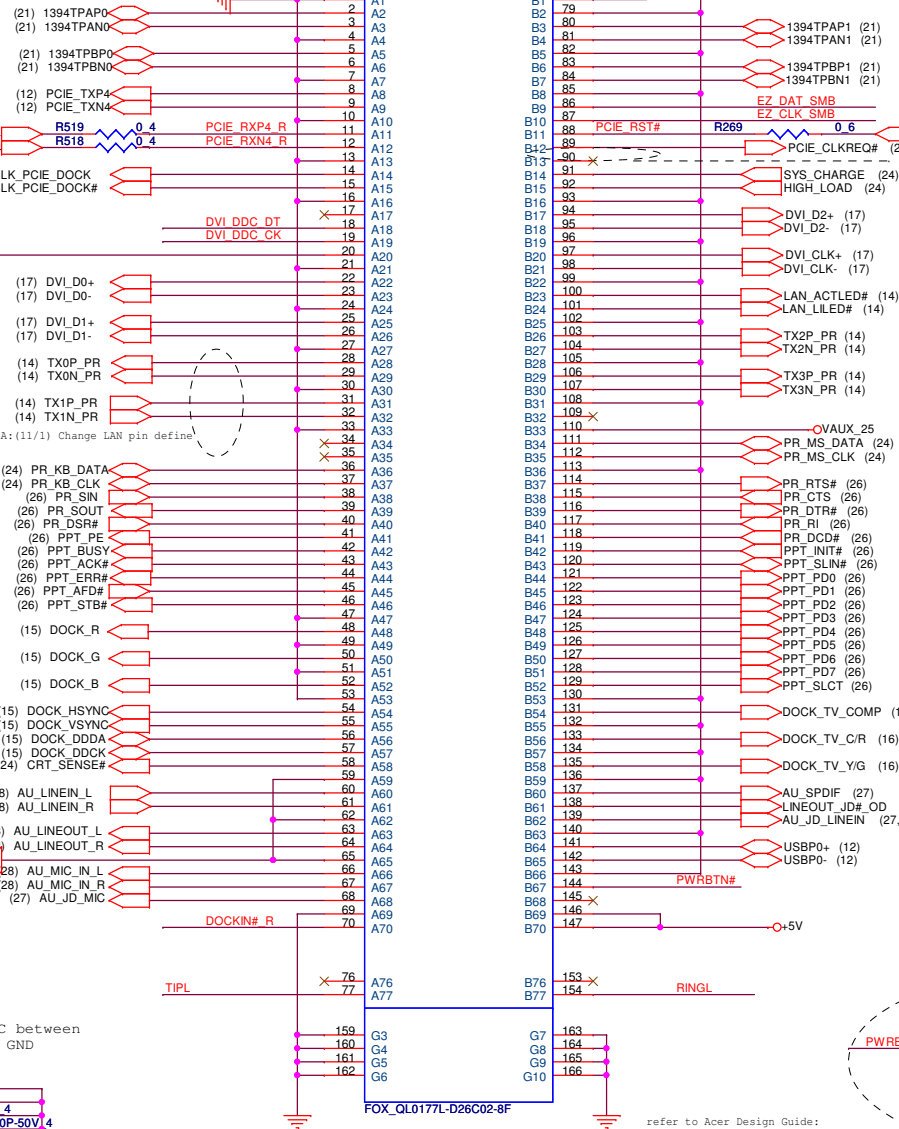
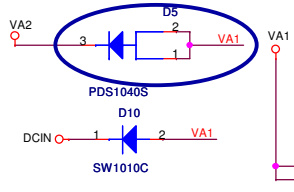
1/31:Acer DVR1012\_Design Requirement Checklist:  
The system side should have a diode to block the AC adaptor power coming from ezDock.



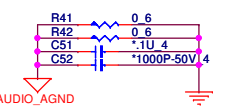
POWER DECOUPLING



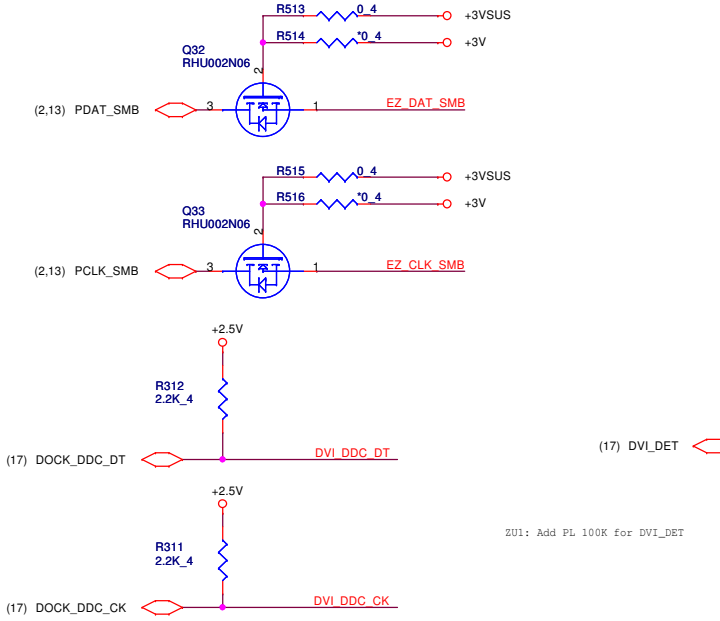
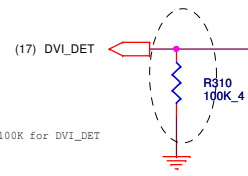
refer to Acer Design Guide:  
this signal is asserted to power on the system.  
A buffer used for PWRBTN# on the system side  
may be necessary to prevent the signal interfered  
by the contact noise.



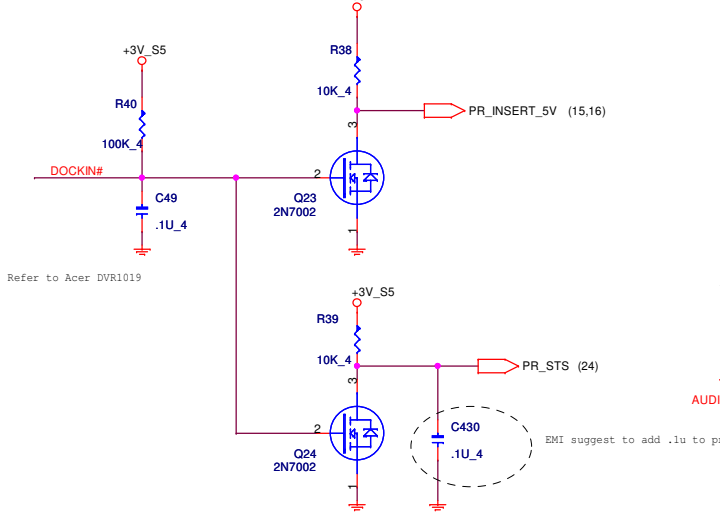
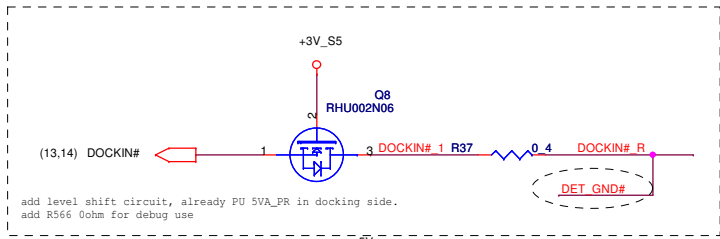
ZU1: Add R and C between  
AUDIO\_AGND and GND



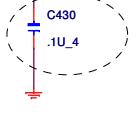
ZU1: Add PL 100K for DVI\_DET




- (1) Remove Level-shift circuit (already in docking side)
- (2) change Power from +3V to +2.5V
- (3) stuff 2.2k (R374, R375)



EMI suggest to add .1u to prevent noise



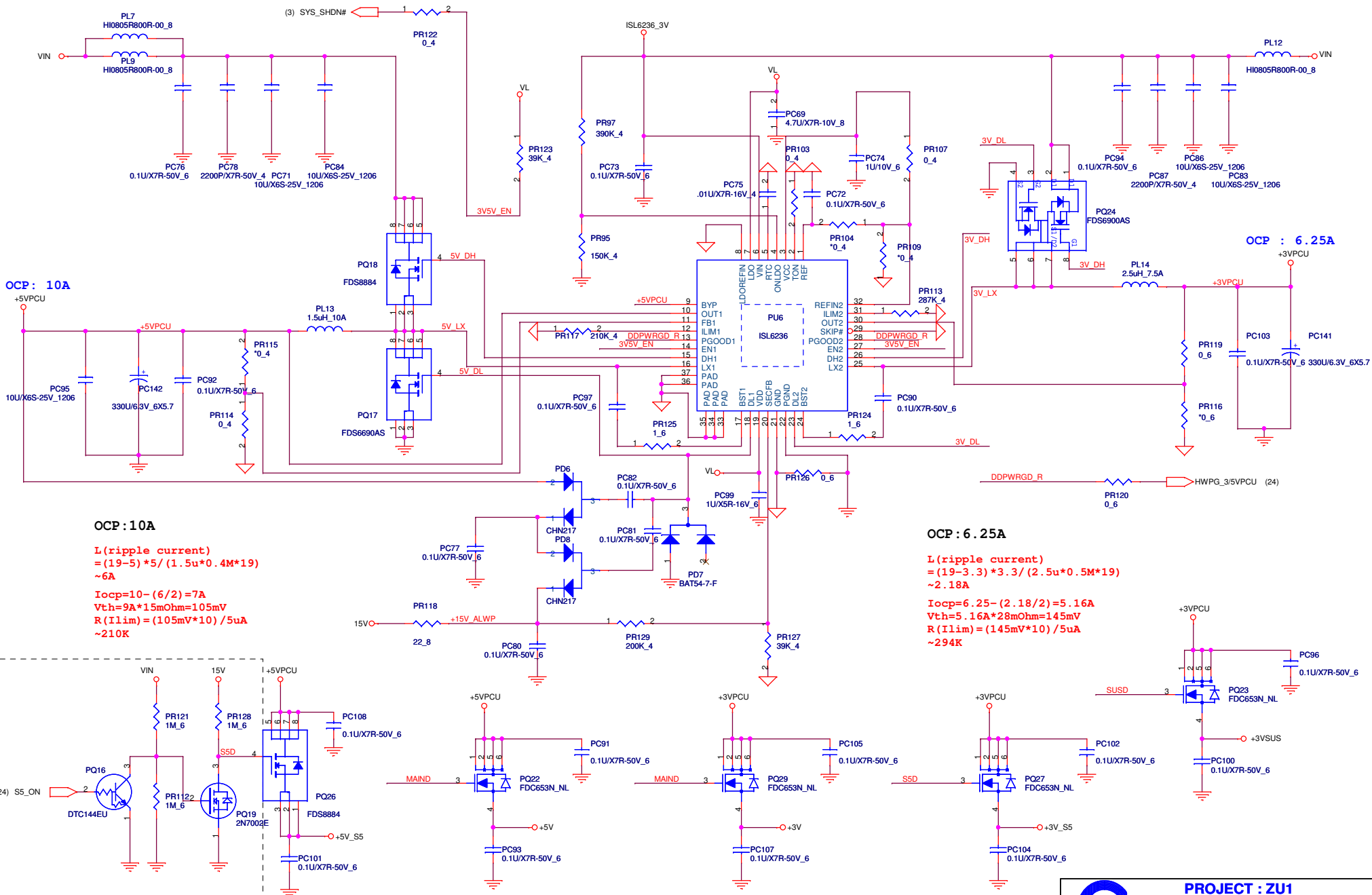


**PROJECT : ZU2**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Docking(ezDockII/II+)</b>	<b>1B</b>
Date:	Friday, March 23, 2007	Sheet 29 of 39



MAIND → MAIND (34)  
 SUSD → SUSD (34)

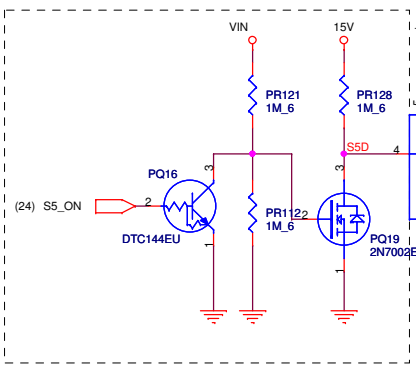


OCP: 10A

OCP: 10A  
 $L(\text{ripple current}) = (19-5) * 5 / (1.5 * 0.4 * 19) \sim 6A$   
 $I_{ocp} = 10 - (6/2) = 7A$   
 $V_{th} = 9A * 15m\Omega = 105mV$   
 $R(I_{lim}) = (105mV * 10) / 5\mu A \sim 210K$

OCP: 6.25A

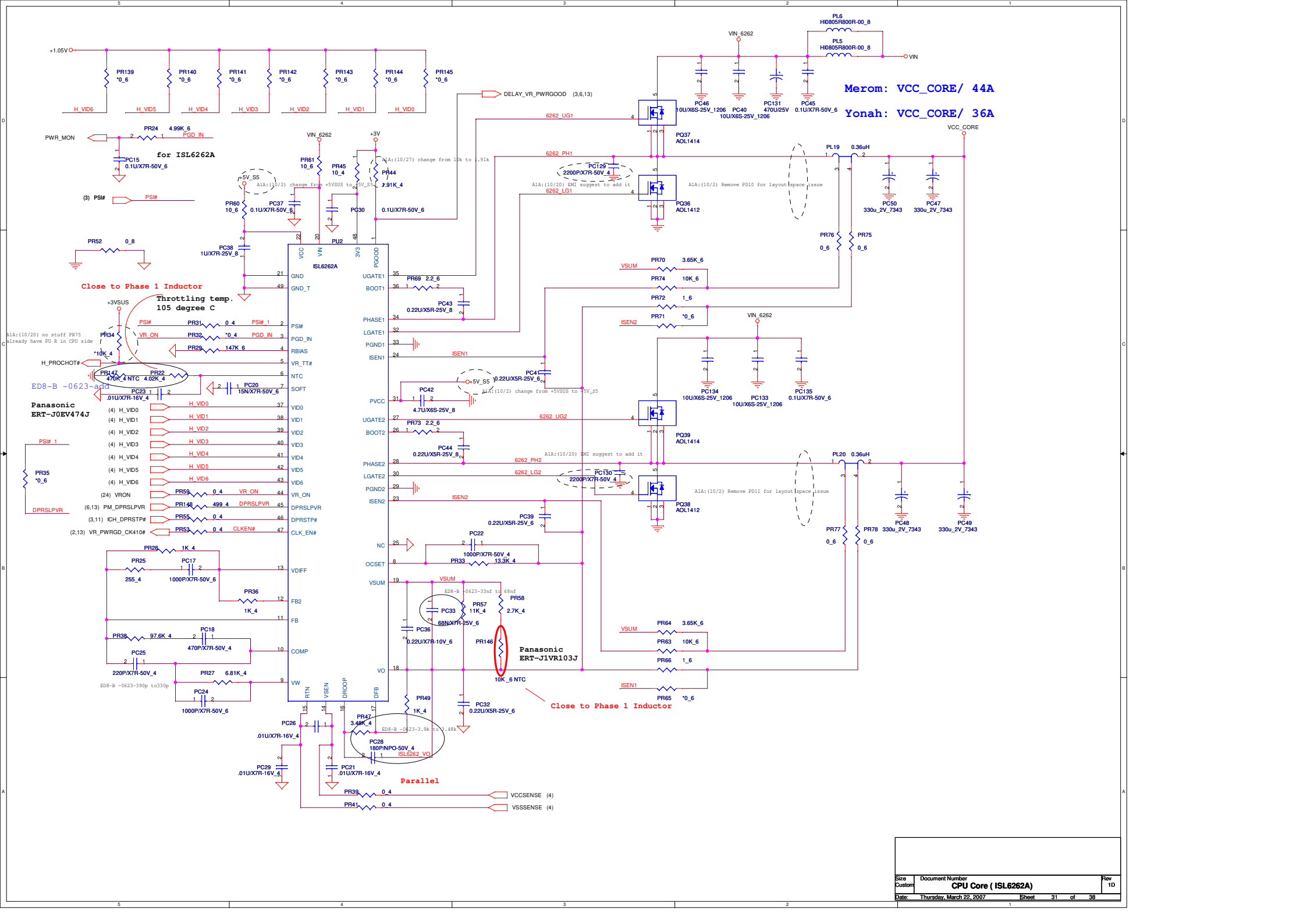
OCP: 6.25A  
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (2.5 * 0.5 * 19) \sim 2.18A$   
 $I_{ocp} = 6.25 - (2.18/2) = 5.16A$   
 $V_{th} = 5.16A * 28m\Omega = 145mV$   
 $R(I_{lim}) = (145mV * 10) / 5\mu A \sim 294K$

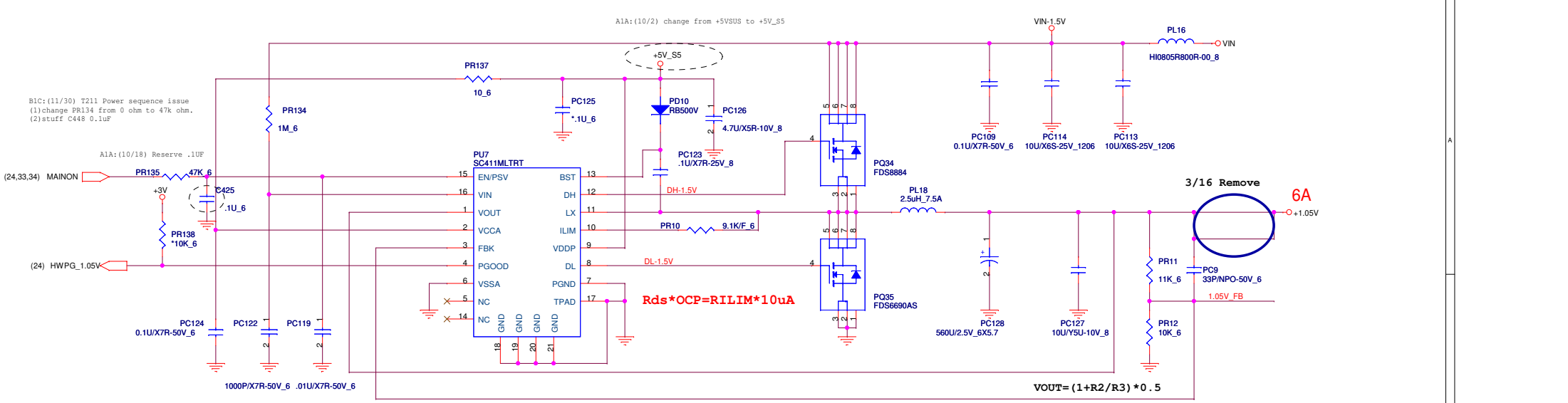


C2A: (12/10) change S5\_ON control circuit  
 B1C: (11/29) change PQ26 from FDS6690AS (BAM66900022) to FDS8884 (BAM88840006)

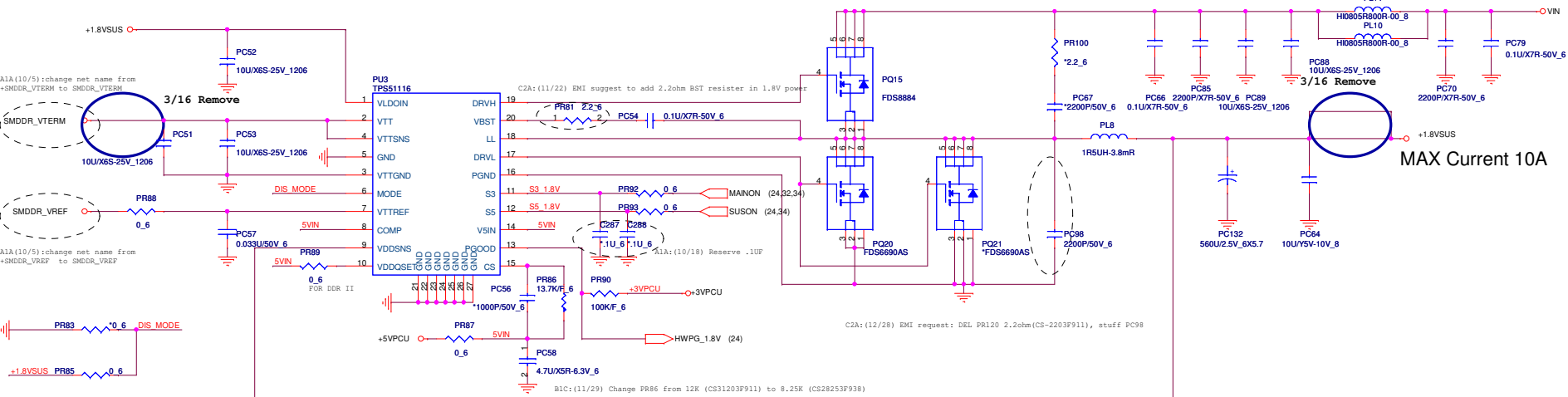
**PROJECT : ZU1**  
**Quanta Computer Inc.**

Size	Document Number	Rev 1D
	<b>SYSTEM 5V/3V (ISL6236)</b>	
Date:	Friday, March 23, 2007	Sheet 30 of 38





B1C: (11/29) Change PR8 from 20K(CS32003P933) to 6.65K ohm (CS26653P911)



A1A(10/5):change net name from +SMDDR\_VTERM to SMDDR\_VTERM

A1A(10/5):change net name from +SMDDR\_VREF to SMDDR\_VREF

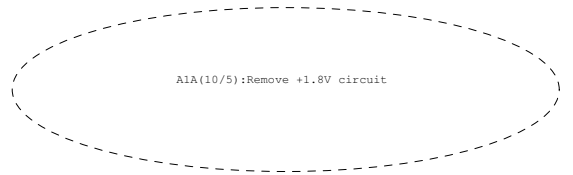
C2A: (11/22) EMI suggest to add 2.2ohm BST resistor in 1.8V power

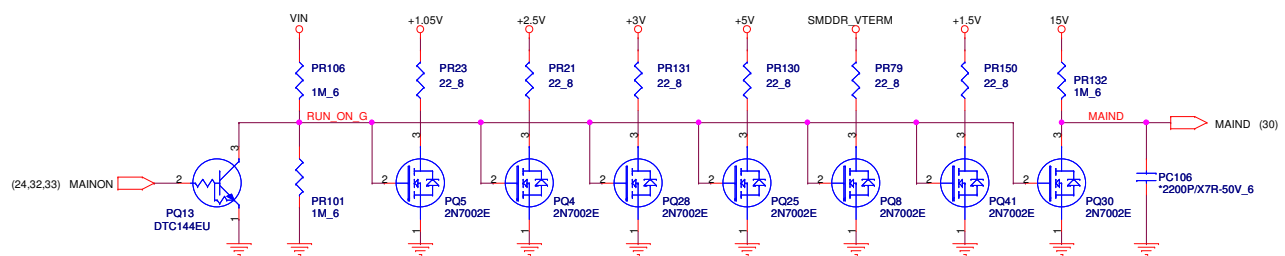
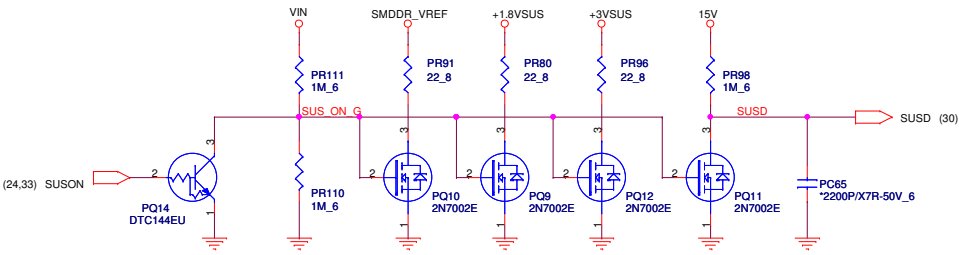
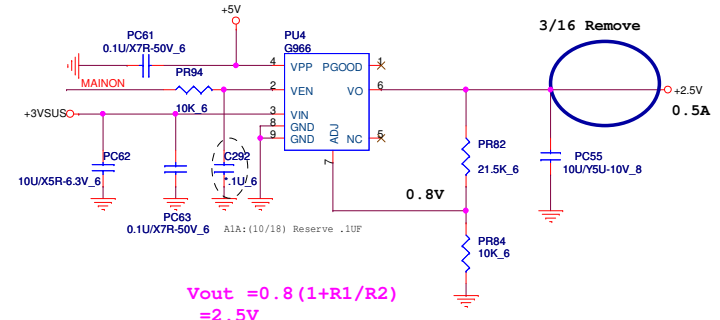
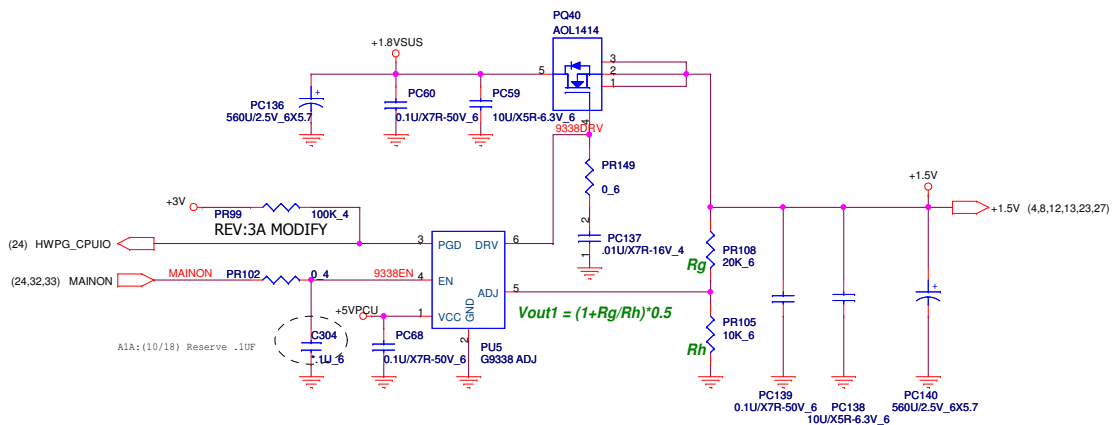
A1A: (10/18) Reserve .1uF

C2A: (12/28) EMI request: DEL PR120 2.2ohm(CS-2203F911), stuff PC98

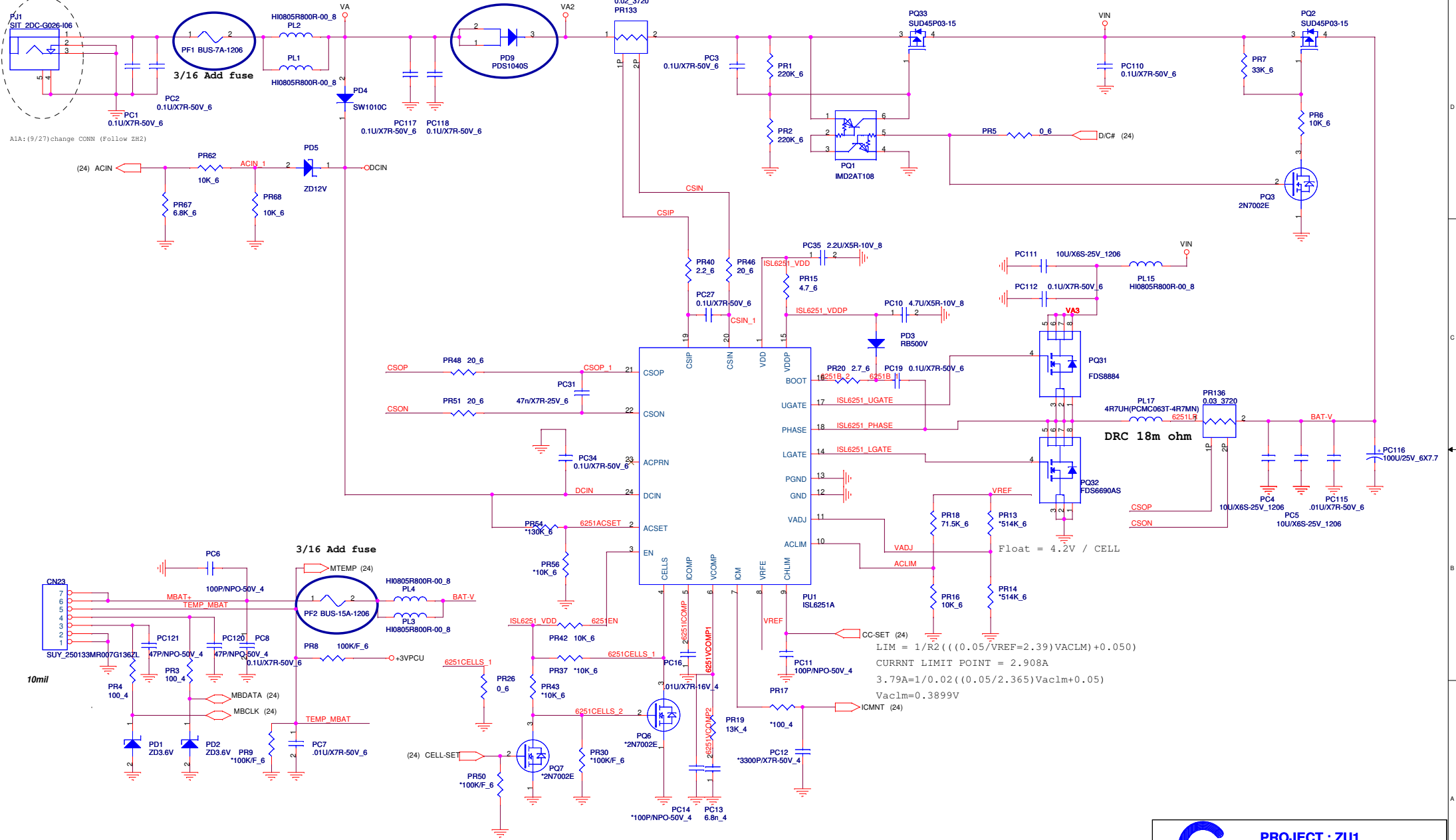
B1C: (11/29) Change PR86 from 12K (CS31203F911) to 8.25K (CS28253F938)

B1C: (12/11) Change PR86 from 8.25K (CS28253F938) to 14K (CS31403F919)





3/16 Modify PD9 Footprint from SBM1040-3P to SBM1040-3P-ZU1



CELL-SET = Hi ----> Cells = VDD ---->4S  
CELL-SET = Low ----> Cells = GND ---->3S

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