

R2J20656ANP

R07DS0201EJ0100

Rev.1.00

Integrated Driver - MOS FET (DrMOS)

Jan 25, 2011

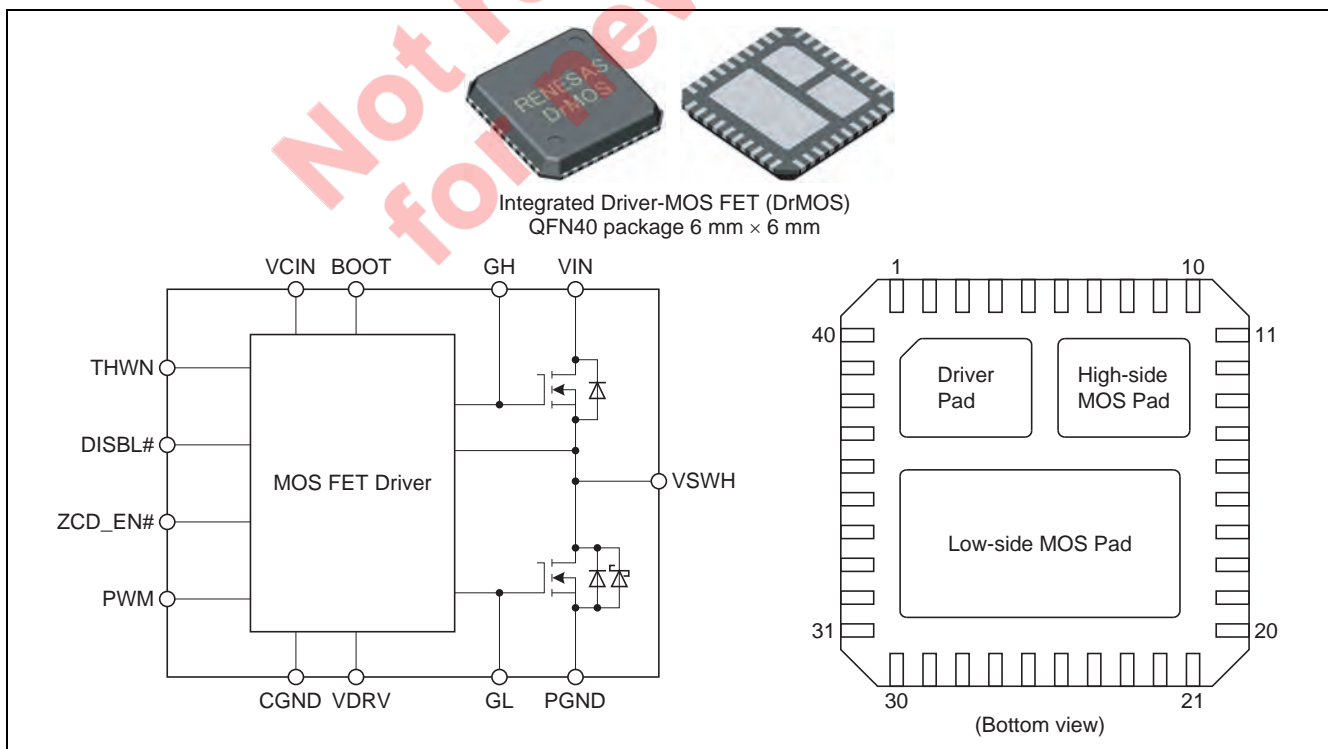
Description

The R2J20656ANP multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver, making this device suitable for large-current buck converters. The chip also incorporates a high-side bootstrap switch, eliminating the need for an external SBD for this purpose.

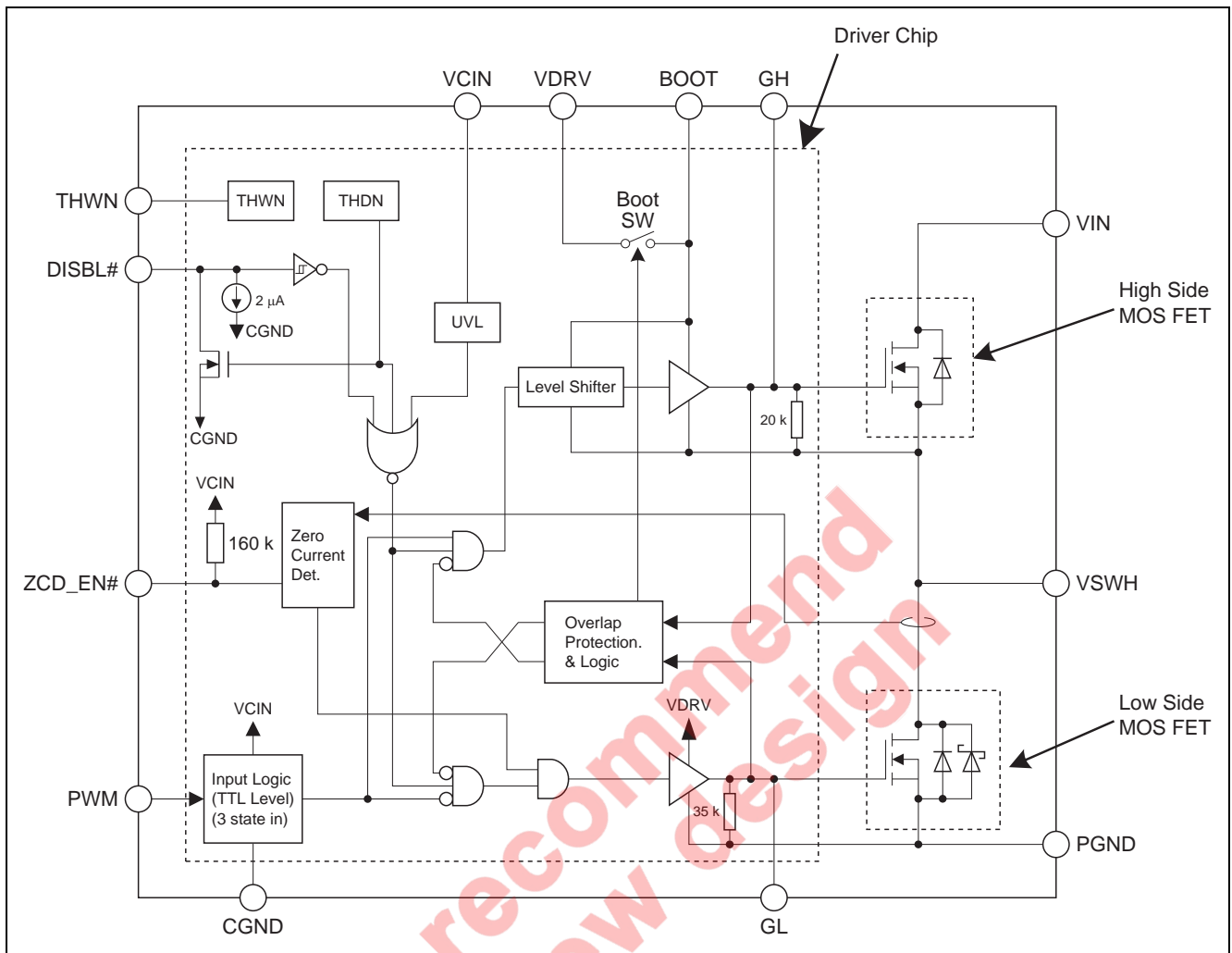
Features

- Compliant with Intel 6 × 6 DrMOS Specification.
- Built-in power MOS FET suitable for Notebook, Desktop, Server application.
- Low-side MOS FET with built-in SBD for lower loss and reduced ringing.
- Built-in driver circuit which matches the power MOS FET
- Built-in tri-state input function which can support a number of PWM controllers
- High-frequency operation (above 1 MHz) possible
- VIN operating-voltage range: 27 Vmax
- Large average output current (Max.35 A)
- Achieve low power dissipation
- Controllable driver: Remote on/off
- Zero current detection for a diode emulation operation
- Double thermal protection: Thermal Warning & Thermal Shutdown
- Built-in bootstrapping Switch
- Small package: QFN40 (6 mm × 6 mm × 0.95 mm)
- Pb-free/Halogen-Free

Outline



Block Diagram



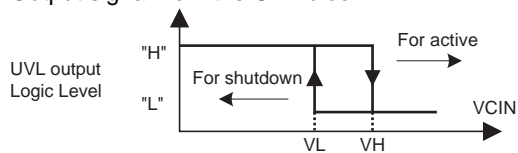
Notes: 1. Truth table for the DISBL# pin

| DISBL# Input | Driver Chip Status |
|--------------|----------------------------|
| "L" | Shutdown (GL, GH = "L") |
| "Open" | Shutdown (GL, GH = "L") |
| "H" | Enable (GL, GH = "Active") |

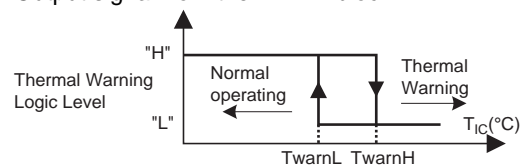
2. Truth table for the ZCD_EN# pin

| ZCD_EN# Input | Driver Chip Status |
|---------------|------------------------------|
| "L" | "Diode Emulation Mode" |
| "Open" | "Continuous Conduction Mode" |
| "H" | "Continuous Conduction Mode" |

3. Output signal from the UVL block



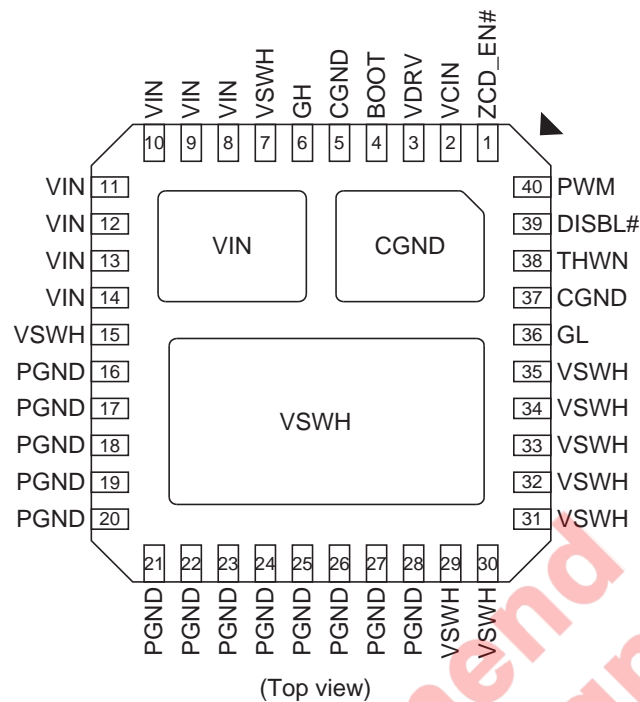
4. Output signal from the THWN block



5. Truth table for the THDN block

| Driver IC Temp. | Driver Chip Status |
|-----------------|-------------------------------------|
| < 150°C | Enable (GL, GH = "Active") |
| > 150°C | Shutdown (GL, GH = "L") (latch-off) |

Pin Arrangement



Note: All die-pads (three pads in total) should be soldered to PCB.

Pin Description

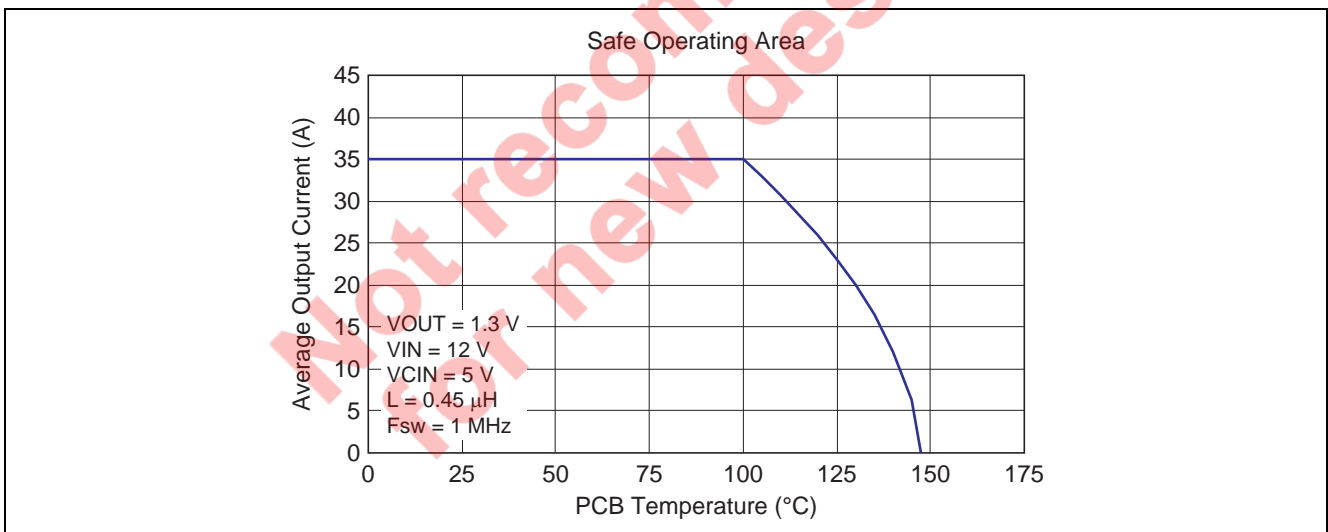
| Pin Name | Pin No. | Description | Remarks |
|----------|----------------------|------------------------------------|---|
| ZCD_EN# | 1 | Zero current detection enable | When asserted "L" signal, zero crossing detection is enabled |
| VCIN | 2 | Control input voltage (+5 V input) | Driver Vcc input |
| VDRV | 3 | Gate supply voltage (+5 V input) | 5 V gate drive |
| BOOT | 4 | Bootstrap voltage pin | To be supplied +5 V through internal switch |
| CGND | 5, 37, Pad | Control signal ground | Should be connected to PGND externally |
| GH | 6 | High-side gate signal | Pin for monitor |
| VIN | 8 to 14, Pad | Input voltage | |
| VSWH | 7, 15, 29 to 35, Pad | Phase output/Switch output | |
| PGND | 16 to 28 | Power ground | |
| GL | 36 | Low-side gate signal | Pin for monitor |
| THWN | 38 | Thermal warning | Thermal warning when over 115°C |
| DISBL# | 39 | Signal disable | Disabled when DISBL# is "L". This Pin is pulled low when internal IC over the thermal shutdown level, 150°C. |
| PWM | 40 | PWM drive logic input | 5 V logic input |

Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Rating | Units | Note |
|--------------------------------|---------------------------------|--------------------|-------|------|
| Power dissipation | Pt(25) | 25 | W | 1 |
| | Pt(110) | 8 | | |
| Average output current | Iout | 35 | A | |
| Input voltage | VIN(DC) | -0.3 to +27 | V | 2 |
| | VIN(AC) | 30 | | 2, 4 |
| Supply voltage & Drive voltage | VCIN & VDRV | -0.3 to +6 | V | 2 |
| Switch node voltage | VSWH(DC) | 27 | V | 2 |
| | VSWH(AC) | 30 | | 2, 4 |
| BOOT voltage | VBOOT(DC) | 32 | V | 2 |
| | VBOOT(AC) | 36 | | 2, 4 |
| I/O voltage | Vpwm, Vdisble, Vlsdbl, Vthwn | -0.3 to VCIN + 0.3 | V | 2, 5 |
| THWN/THDN current | Ithwn, Ithdn | 0 to 1.0 | mA | |
| Operating junction temperature | Tj-opr | -40 to +150 | °C | |
| Storage temperature | Tstg | -55 to +150 | °C | |

- Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(110) represents 110°C.
 2. Rated voltages are relative to voltages on the CGND and PGND pins.
 3. For rated current, (+) indicates inflow.
 4. The specification values indicated "AC" are limited within 10 ns.
 5. $VCIN + 0.3 V < 6 V$



Recommended Operating Condition

| Item | Symbol | Rating | Units | Note |
|--------------------------------|-----------------|------------|-------|------|
| Input voltage | V _{IN} | 4.5 to 22 | V | |
| Supply voltage & Drive voltage | VCIN & VDRV | 4.5 to 5.5 | V | |

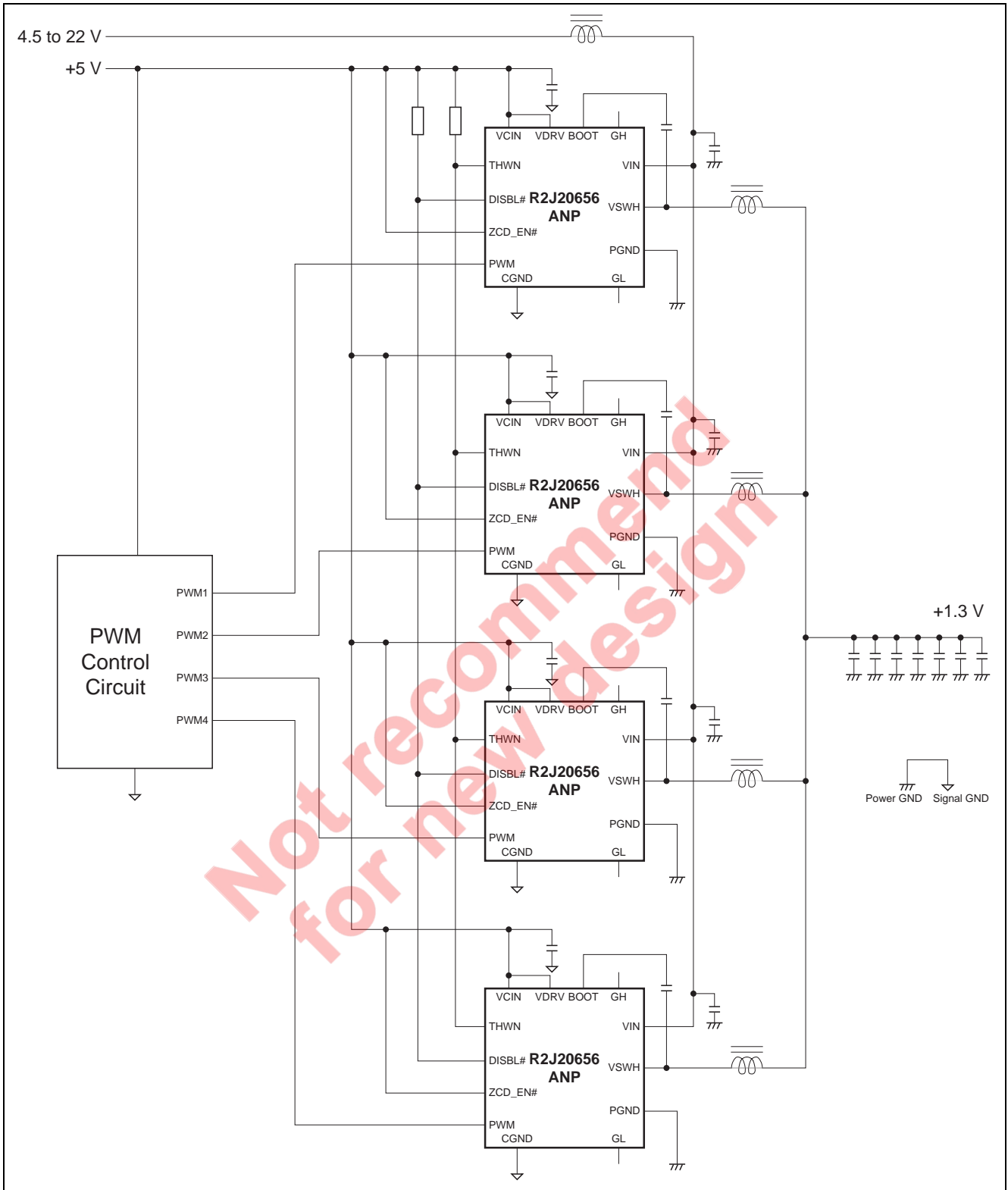
Electrical Characteristics

(T_a = 25°C, VCIN = 5 V, VDRV = 5 V, VSWH = 0 V, unless otherwise specified)

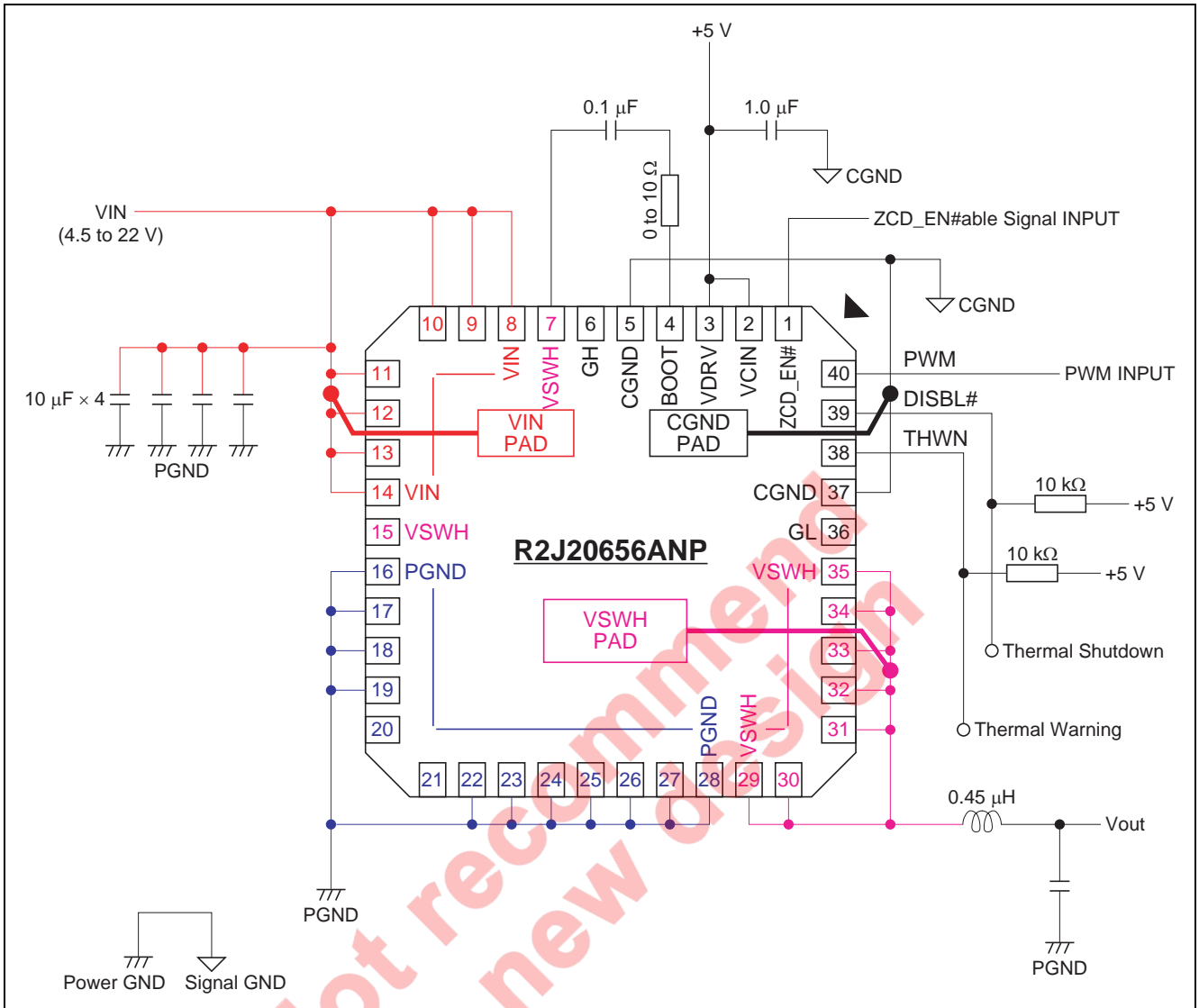
| Item | | Symbol | Min | Typ | Max | Units | Test Conditions |
|------------------|---------------------------|--------------------------|-----|------|-----|-------|---|
| Supply | VCIN start threshold | V _H | 4.1 | 4.3 | 4.5 | V | |
| | VCIN shutdown threshold | V _L | 3.6 | 3.8 | 4.0 | V | |
| | UVLO hysteresis | dUVL | — | 0.5 | — | V | V _H - V _L |
| | VCIN operating current | I _{CIN} | — | 49 | — | mA | f _{PWM} = 1 MHz, Ton_pwm = 120 ns |
| | VCIN disable current | I _{CIN-DISBL} | — | — | 150 | μA | DISBL# = 0 V, PWM = ZCD_EN# = Open |
| PWM input | PWM input high level | V _{H-PWM} | 4.0 | — | — | V | 5.0 V PWM interface |
| | PWM input low level | V _{L-PWM} | — | — | 0.8 | V | |
| | PWM input resistance | R _{IN-PWM} | 6.5 | 12.5 | 25 | kΩ | PWM = 1 V |
| | PWM input tri-state range | V _{IN-tri} | 1.5 | — | 3.2 | V | 5.0 V PWM interface |
| | Shutdown hold-off time | t _{HOLD-OFF} *1 | — | 150 | — | ns | |
| DISBL# input | Enable level | V _{ENBL} | 2.0 | — | — | V | |
| | Disable level | V _{DISBL} | — | — | 0.8 | V | |
| | Input current | I _{DISBL} | — | 2.0 | 5.0 | μA | DISBL# = 1 V |
| | THDN on resistance | R _{THDN} *1 | 0.2 | 0.5 | 1.0 | kΩ | DISBL# = 0.2 V |
| ZCD_EN# | ZCD disable level | V _{zcdisbl} | 2.0 | — | — | V | |
| | ZCD enable level | V _{zcden} | — | — | 0.8 | V | |
| | Input current | I _{zcden} | -52 | -25 | -12 | μA | ZCD_EN# = 1 V |
| Thermal warning | Warning temperature | T _{THWN} *1 | 100 | 115 | 130 | °C | Driver IC temperature |
| | Temperature hysteresis | T _{HYS} *1 | — | 15 | — | °C | |
| | THWN on resistance | R _{THWN} *1 | 0.2 | 0.5 | 1.0 | kΩ | THWN = 0.2 V |
| | THWN leakage current | I _{LEAK} | — | — | 1.0 | μA | THWN = 5 V |
| Thermal shutdown | Shutdown temperature | T _{stdn} *1 | 130 | 150 | — | °C | Driver IC temperature |

Note: 1. Reference values for design. Not 100% tested in production.

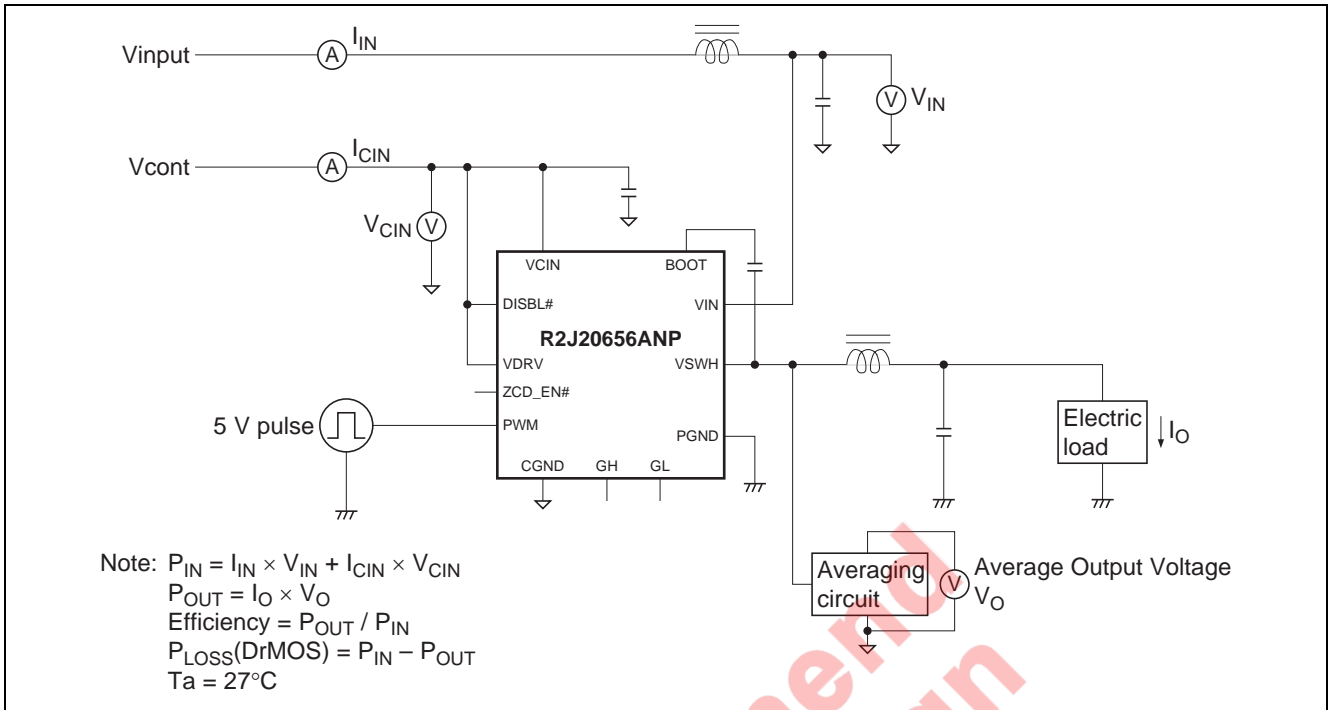
Typical Application



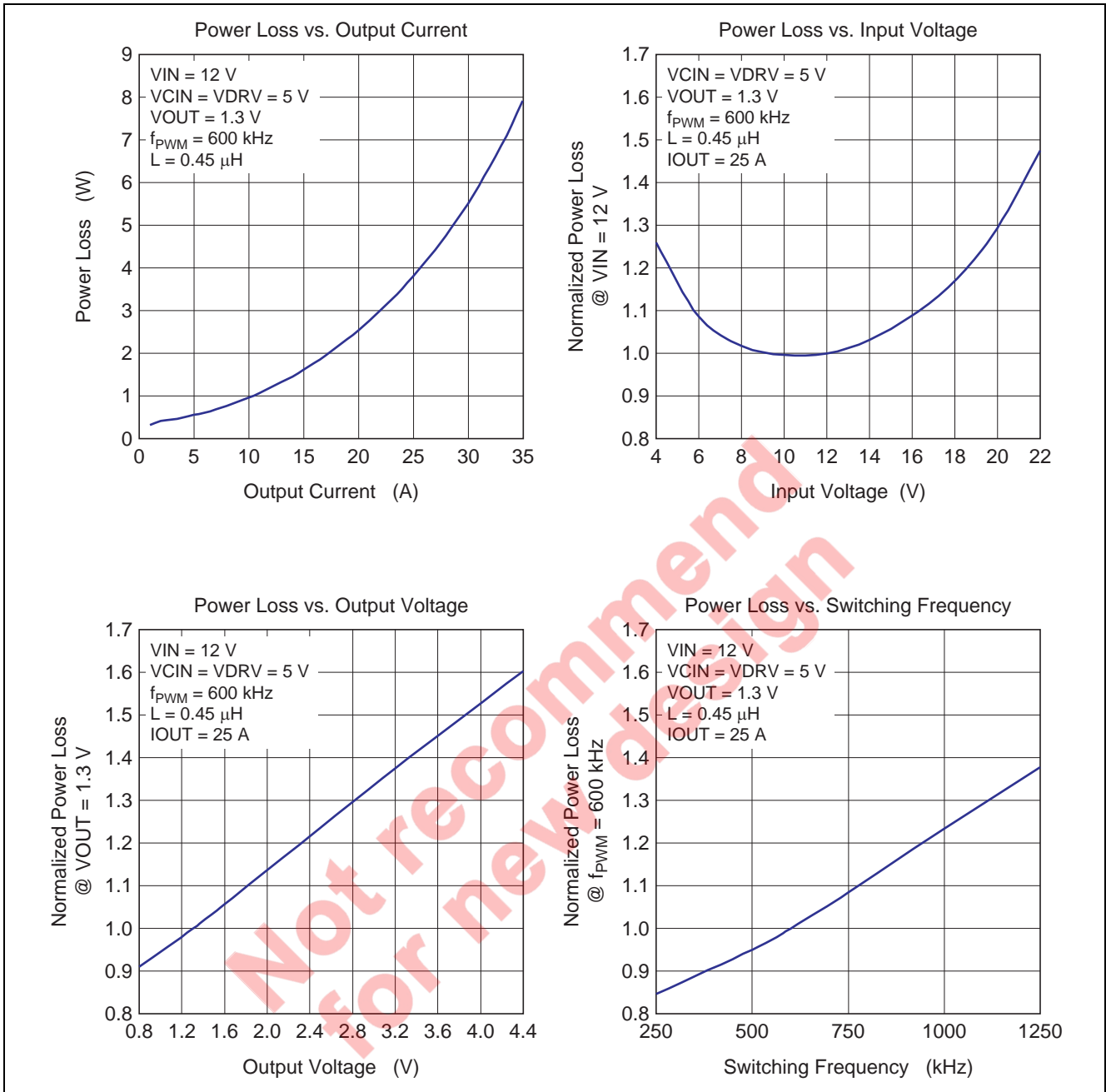
Pin Connection

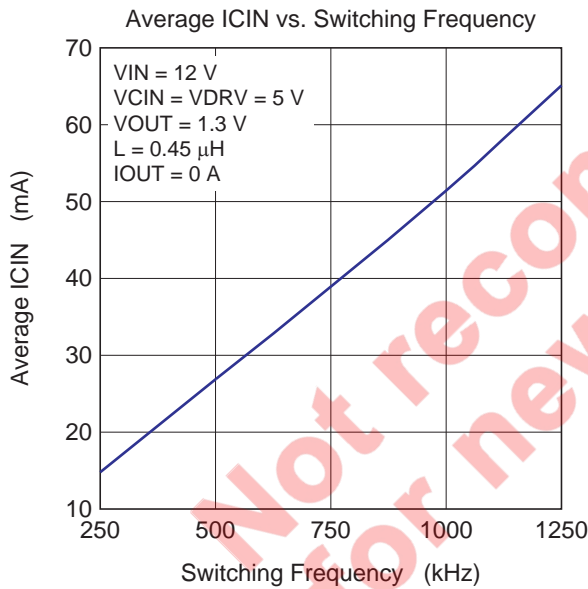
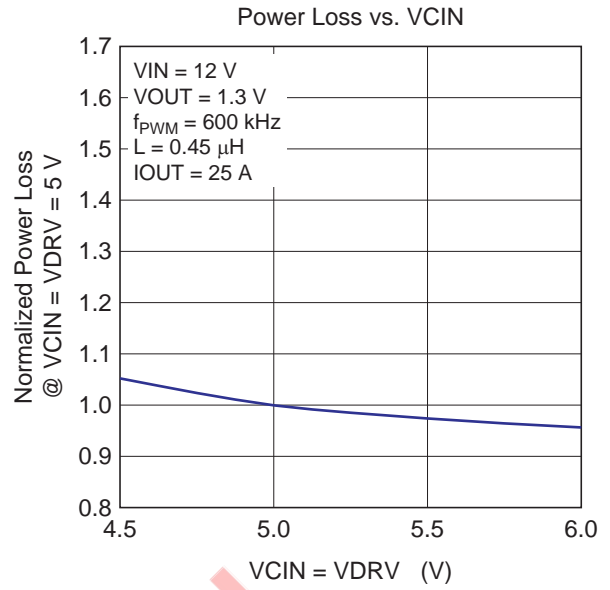
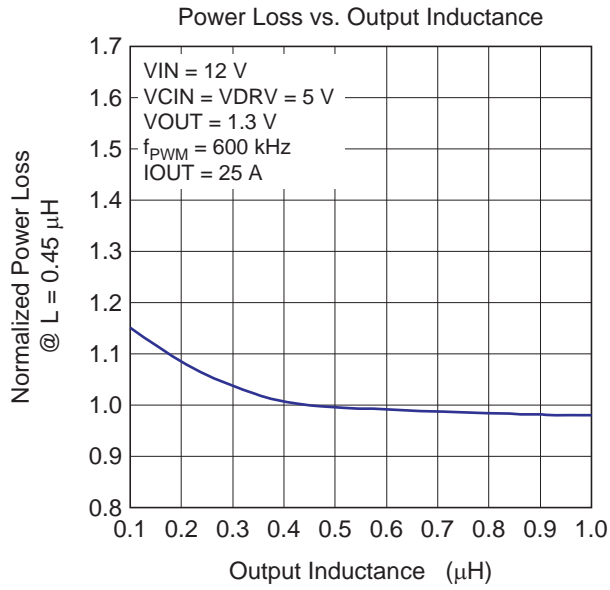


Test Circuit



Typical Data





Not recommended for new design

Description of Operation

The DrMOS multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. Since the parasitic inductance between each chip is extremely small, the module is highly suitable for use in buck converters to be operated at high frequencies. The control timing between the high-side MOS FET, low-side MOS FET, and driver is optimized so that high efficiency can be obtained at low output-voltage.

VCIN & DISBL#

The VCIN pin is connected to the UVL (under-voltage lockout) module, so that the driver is disabled as long as VCIN is 4.3 V or less. On cancellation of UVL, the driver remains enabled until the UVL input is driven to 3.8 V or less. The signal on pin DISBL# also enables or disables the circuit.

Voltages from -0.3 V to VCIN can be applied to the DISBL# pin, so on/off control by a logic IC or the use of a resistor, etc., to pull the DISBL# line up to VCIN are both possible.

| VCIN | DISBL# | Driver State |
|------|--------|----------------------|
| L | * | Disable (GL, GH = L) |
| H | L | Disable (GL, GH = L) |
| H | H | Active |
| H | Open | Disable (GL, GH = L) |

The pulled-down MOS FET, which is turned on when internal IC temperature becomes over thermal shutdown level, is connected to the DISBL# pin. The detailed function is described in THDN section.

PWM & ZCD_EN#

The PWM pin is the signal input pin for the driver chip. The input-voltage range is -0.3 V to $(VCIN + 0.3)$ V. When the PWM input is high, the gate of the high-side MOS FET (GH) is high and the gate of the low-side MOS FET (GL) is low.

| PWM | GH | GL |
|-----|----|----|
| L | L | H |
| H | H | L |

The ZCD_EN# pin is the Zero Current Detection Operation Enable pin for "Diode Emulation Mode (DEM)" when ZCD_EN# is low. This function improves light load efficiency by preventing negative inductor current from output capacitor. Driver IC monitors inductor current and when inductor current crosses zero, driver IC turn off Low side MOS FET automatically.

Figure 1.1 shows the Typical high side and low side gate switching and Inductor current (IL) during Continuous Conduction Mode (CCM), and figure 1.2 shows DEM when asserting Zero Current Detection Enable signal.

ZCD_EN# pin is internally pulled up to VCIN with 160 k Ω resistor. When Zero current detection function is not used, keep this pin open or pulled up to VCIN.

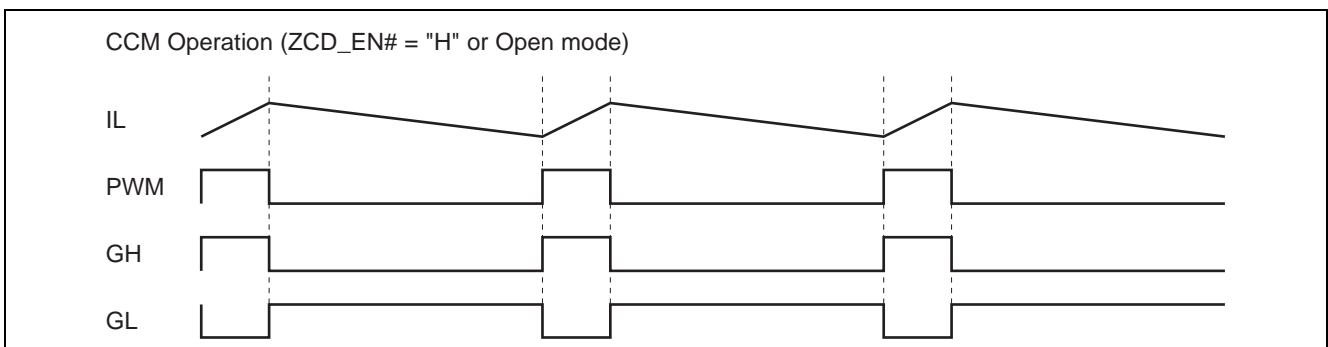


Figure 1.1 Typical Signals during CCM

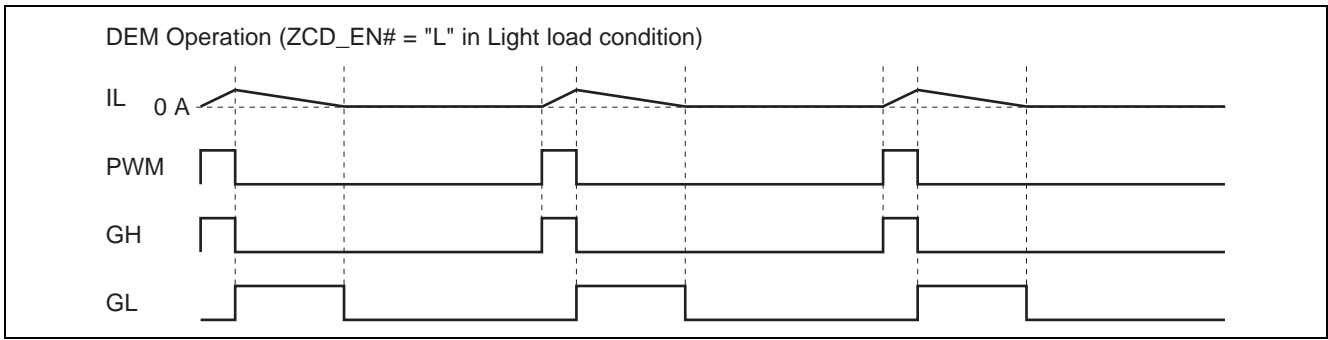


Figure 1.2 Typical Signals during DEM

The PWM input is TTL level and has hysteresis. When the signal route from the control IC is high impedance, the tri-state function turns off the high- and low-side MOS FETs. This function operates when the PWM input signal stays in the input hysteresis window for 150 ns (typ.). After the tri-state mode has been entered and GH and GL have become low, a PWM input voltage of 4.0 V or more is required to make the circuit return to normal operation.

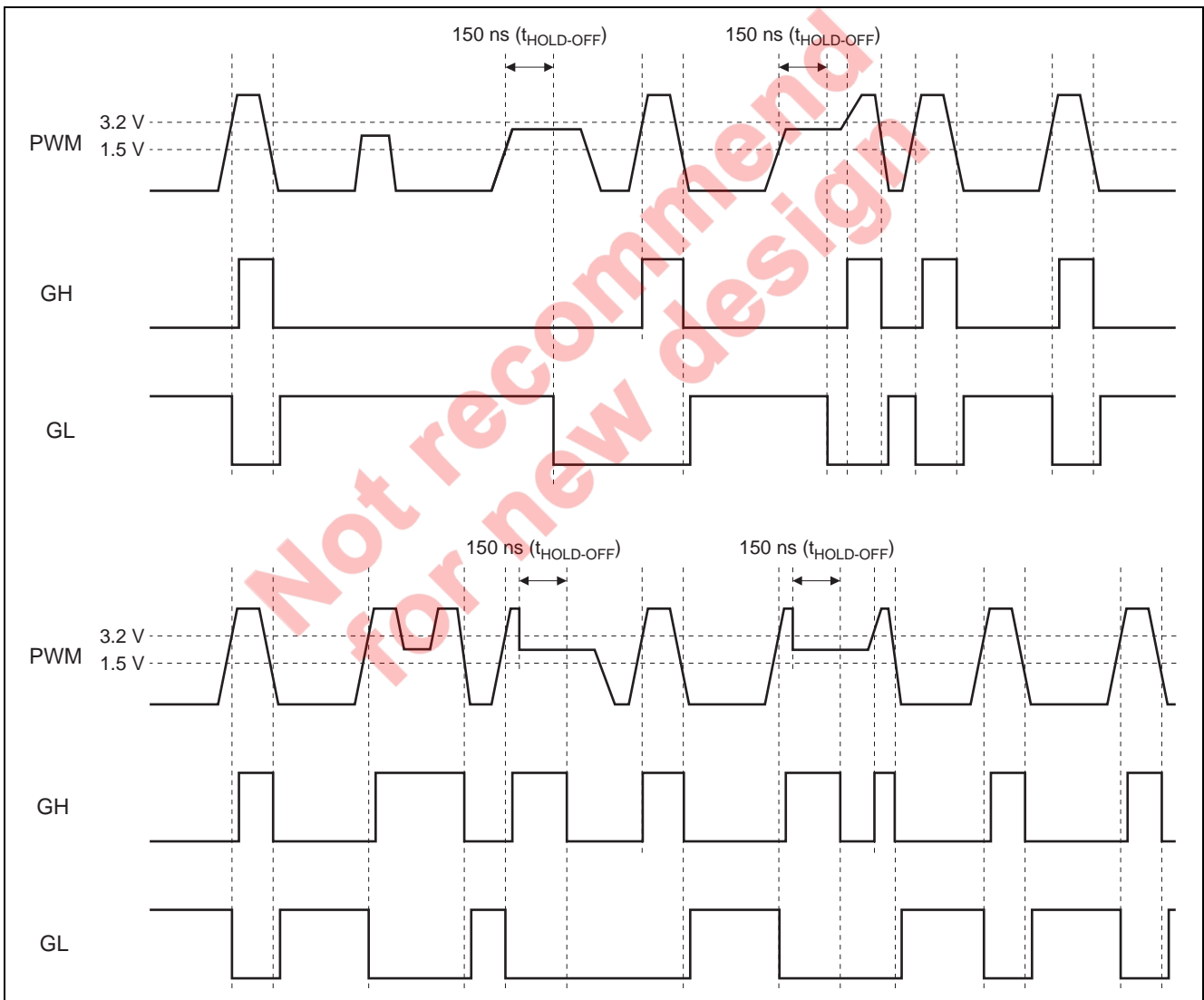


Figure 2 PWM Shutdown-Hold Time Signal

The equivalent circuit for the PWM-pin input is shown in the next figure. M1 is in the ON state during normal operation; after the PWM input signal has stayed in the hysteresis window for 150 ns (typ.) and the tri-state detection signal has been driven high, the transistor M1 is turned off.

When VCIN is powered up, M1 is started in the OFF state regardless of PWM Low or Open state. After PWM is asserted high signal, M1 becomes ON and shifts to normal operation.

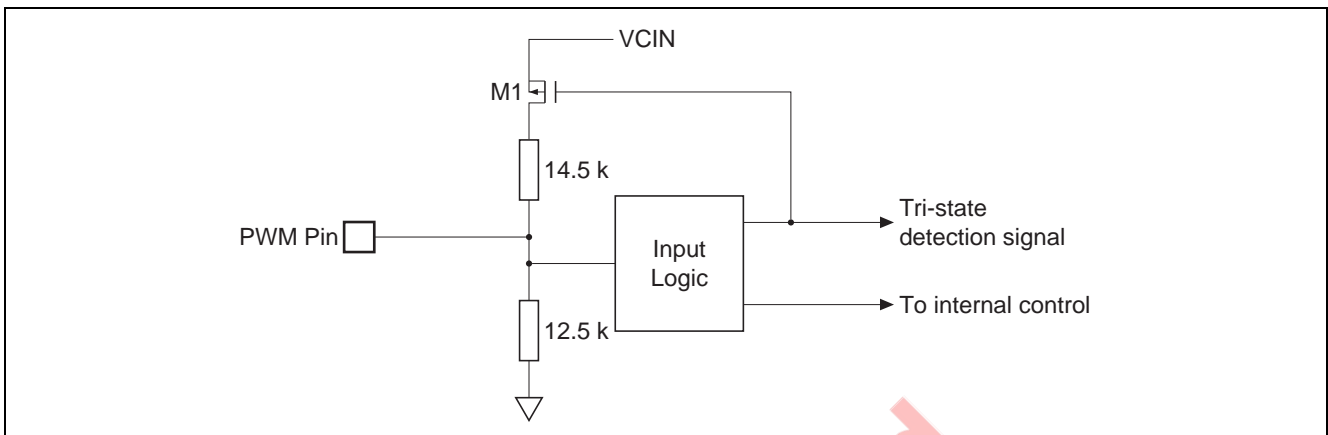


Figure 3 Equivalent Circuit for the PWM-pin Input

THWN & THDN

This device has two level thermal detection, one is thermal warning and the other is thermal shutdown function.

This Thermal Warning feature is the indication of the high temperature status.

THWN is an open drain logic output signal and need to connect a pull-up resistor (ex.51 k Ω) to THWN for Systems with the thermal warning implementation.

When the chip temperature of the internal driver IC becomes over 115°C, Thermal warning function operates.

This signal is only indication for the system controller and does not disable DrMOS operation.

When thermal warning function is not used, keep this pin open.

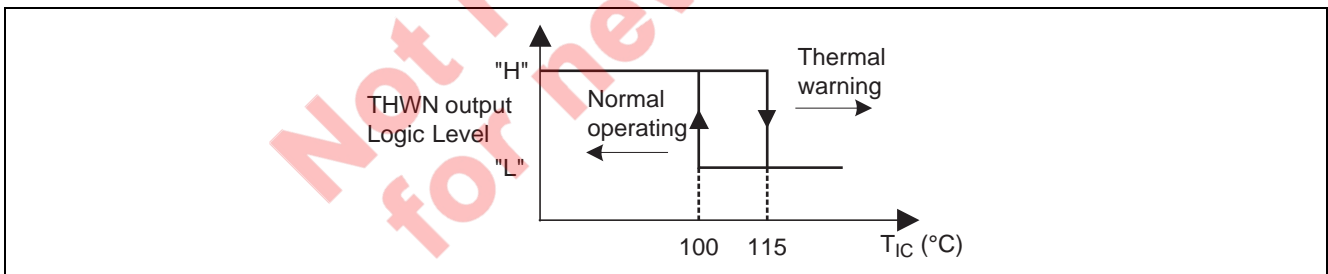


Figure 4 THWN Trigger Temperature

THDN is an internal thermal shutdown signal when driver IC becomes over 150°C.

This function makes High Side MOS FET and Low Side MOS FET turn off for the device protection from abnormal high temperature situation and at the same time DISBL# pin is pulled low internally to give notice to the system controller. Once thermal shutdown function operates, driver IC keeps DISBL# pin pulled low until VCIN becomes under UVL level (3.8 V).

Figure 5 shows the example of two types of DISBL# connection with the system controller signal.

| Driver IC Temp. | Driver Chip Status |
|-----------------|----------------------------|
| < 150°C | Enable (GL, GH = "Active") |
| > 150°C | Shutdown (GL, GH = "L") |

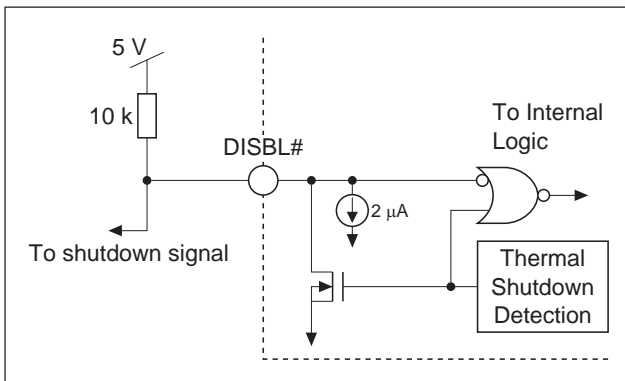


Figure 5.1 THDN Signal to the System Controller

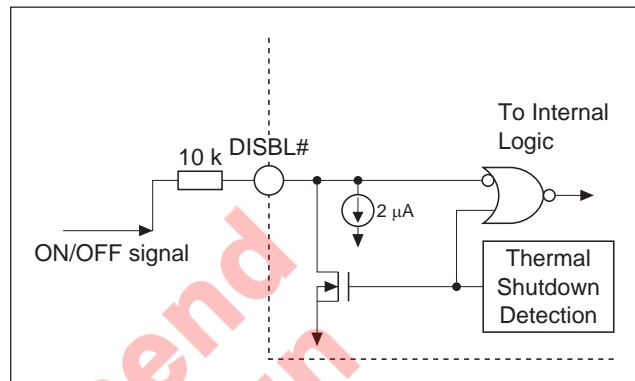


Figure 5.2 ON/OFF Signal from the System Controller

MOS FET

The MOS FETs incorporated in R2J20656ANP are highly suitable for synchronous-rectification buck conversion. For the high-side MOS FET, the drain is connected to the VIN pin and the source is connected to the VSWH pin. For the low-side MOS FET, the drain is connected to the VSWH pin and the source is connected to the PGND pin.

Not recommended for new designs

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