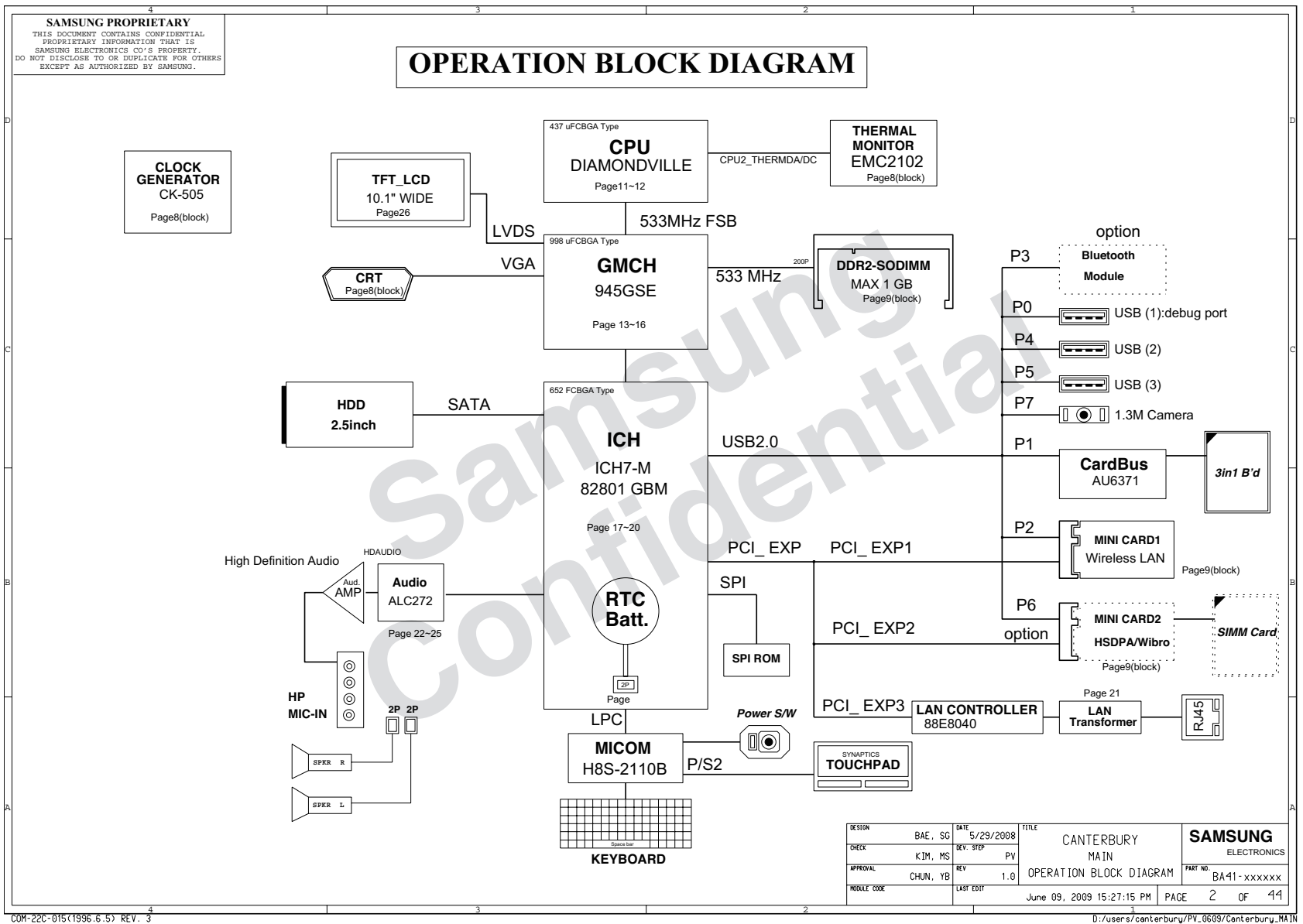


8. Block Diagram and Schematic

| <p style="text-align: center;">SAMSUNG PROPRIETARY THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS SAMSUNG ELECTRONICS CO.'S PROPERTY. DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS EXCEPT AS AUTHORIZED BY SAMSUNG.</p> <div style="text-align: center; border: 1px solid black; padding: 10px; margin: 20px 0;"> <h2 style="margin: 0;">CANTERBURY SPRINGFIELD</h2> </div> <div style="border: 1px solid black; padding: 10px; margin: 10px 0;"> <p>CPU : INTEL DIAMONDVILLE Chip Set : INTEL 945GSE Remarks :</p> <p>Model Name : CANTERBURY SPRINGFIELD</p> <p>PCB Part No : BA41-01122A (GCE) BA41-01123A (NY) BA41-01124A (HST) BA41-01125A (TRI)</p> <p>Dev. Step : PR1 Revision : 1.0 T.R. Date : 2009.07.13</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 33%;">DRAW</th> <th style="width: 33%;">CHECK</th> <th style="width: 33%;">APPROVAL</th> </tr> </thead> <tbody> <tr> <td style="height: 40px;"></td> <td></td> <td></td> </tr> </tbody> </table> </div> | DRAW | CHECK | APPROVAL | | | | <h3 style="text-align: center; border-bottom: 1px solid black; margin-bottom: 10px;">Table of Contents</h3> <p>Page. 1 ---- COVER Page. 2 ---- OPERATION BLOCK DIAGRAM Page. 3 ---- POWER SEQUENCE Page. 4 ---- CLOCK DISTRIBUTION Page. 5 ---- BOARD INFORMATION Page. 6 ---- CLOCK GENERATOR (CK-505M) Page. 7~8 --- DIAMONDVILLE (N270) Page. 9 ---- THERMAL MONITOR Page. 10~13 - CALISTOGA (INTEL945GSE) Page. 14~15 - DDR2 ON BOARD Page. 16 --- DDR2 TERMINATION Page. 17 --- DDR2 SODIMM Page. 18~21 - ICH7-M Page. 22 --- BIOS CODE Page. 23 --- LCD (LVDS) CONN. Page. 24 --- CRT CONN. Page. 25 --- HDD CONNECTOR (SATA) Page. 26 --- MICOM Page. 27~29 - LAN (GIGABIT) Page. 30 --- USB Page. 31 --- MINI-CARD (Wireless) Page. 32~33 - CARDBUS CONTROLLER (AU6371) Page. 34 --- 3IN1 SUB Page. 35 --- AUDIO CODEC (ALC262-GR) Page. 36 --- AMP & SPEAKER & MIC Page. 37 --- KBD CONN & DEBUG PORT Page. 38 --- CHARGER Page. 39 --- P3.3V AUX & P5V_AUX Page. 40 --- DDR2 POWER Page. 41 --- CHIPSET POWER (P 1.05V & P 1.5V) Page. 42 --- CPU VRM POWER (VCC_CORE) Page. 43 --- SWITCHED POWER Page. 44 --- POWER DISCHARGER Page. 45 --- LED FPC CONNECTOR POWER S/W Page. 46 --- TRANSMITTER Page. 47 --- MOUNT HOLE Page. 49~50 - TEST POINTS</p> |
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

| Devices | IDSEL# | REQ/GNT# | Interrupts |
|---------------------------|----------------|-------------|------------|
| USB Hub to PCI | AD29(internal) | Programable | |
| LPC Bridge/IDE/AC97/SMBUS | AD30(internal) | | |
| Internal MAC | AD31(internal) | | |
| | AD24(internal) | | |

I²C / SMB Address

| Devices | Address | Hex | Bus |
|---------------------------|-----------|-----|------------------------------------|
| ICH7M | Master | - | SMBUS Master |
| CK-S5SM (Clock Generator) | 1101 001X | D2h | Clock, Unused Clock Output Disable |
| SDIMM0 | 1010 000X | A6h | - |
| CPU Thermal Sensor | 0111 101X | 7Ah | Thermal Sensor |

USB PORT Assign

| Port Number | ASSIGNED TO | Port Number | ASSIGNED TO |
|-------------|--------------|-------------|-------------|
| UHCL_0 | 0 | UHCL_2 | 4 |
| | USB PORT | | USB PORT |
| | 3-IN-1 | | 1 |
| UHCL_1 | 2 | | 6 |
| | Wireless LAN | | HSDPA |
| | BLUETOOTH | UHCL_3 | 7 |
| | | | CAMERA |

PCI Express Assign

| Port Number | ASSIGNED TO |
|-------------|---------------------------|
| 1 | Mini Card 1(Wireless LAN) |
| 2 | Mini Card 2 (HSDPA/Wibro) |
| 3 | LOM |

Voltage Rails

| Power Rail | Descriptions |
|---------------------|---|
| PRTC_BAT | 3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. |
| VDC | Primary DC system power supply (9 to 19V) |
| P1.05V(VCCP) | VTT for CPU, Callisoga & ICH7-M |
| P3.3V_MICOM | 3.3V always power rail(for Micom) |
| P1.5V | 1.5V switched power rail (off in S3-S5) |
| P1.8V_AUX | 1.8V power rail for DDR (off in S4-S5) |
| P0.9V | 0.9V power rail for DDR (off in S4-S5) |
| P5V_AUX | 5.0V power rail (off in S4-S5) |
| P3.3V_AUX | 3.3V power rail (off in S4-S5) |
| P5V | 5.0V switched power rail (off in S3-S5) |
| P3.3V | 3.3V switched power rail (off in S3-S5) |
| CPU_CORE | Core voltage for Atom CPU |

| | | | | | | |
|-------------|----------|-----------|----------|---------------------------|---|-------------------------------|
| DRAWN | BAE, SG | DATE | 5/2/2006 | TITLE | CANTERBURY MAIN BOARD INFORMATION | SAMSUNG ELECTRONICS |
| CHECK | KIM, MS | REV. STEP | PV | | | PART NO. |
| APPROVAL | CHUN, YB | REV | 1.0 | | | BA41-xxxxxx |
| MODULE CODE | | LAST EDIT | | June 09, 2009 15:27:15 PM | PAGE | 3 OF 44 |

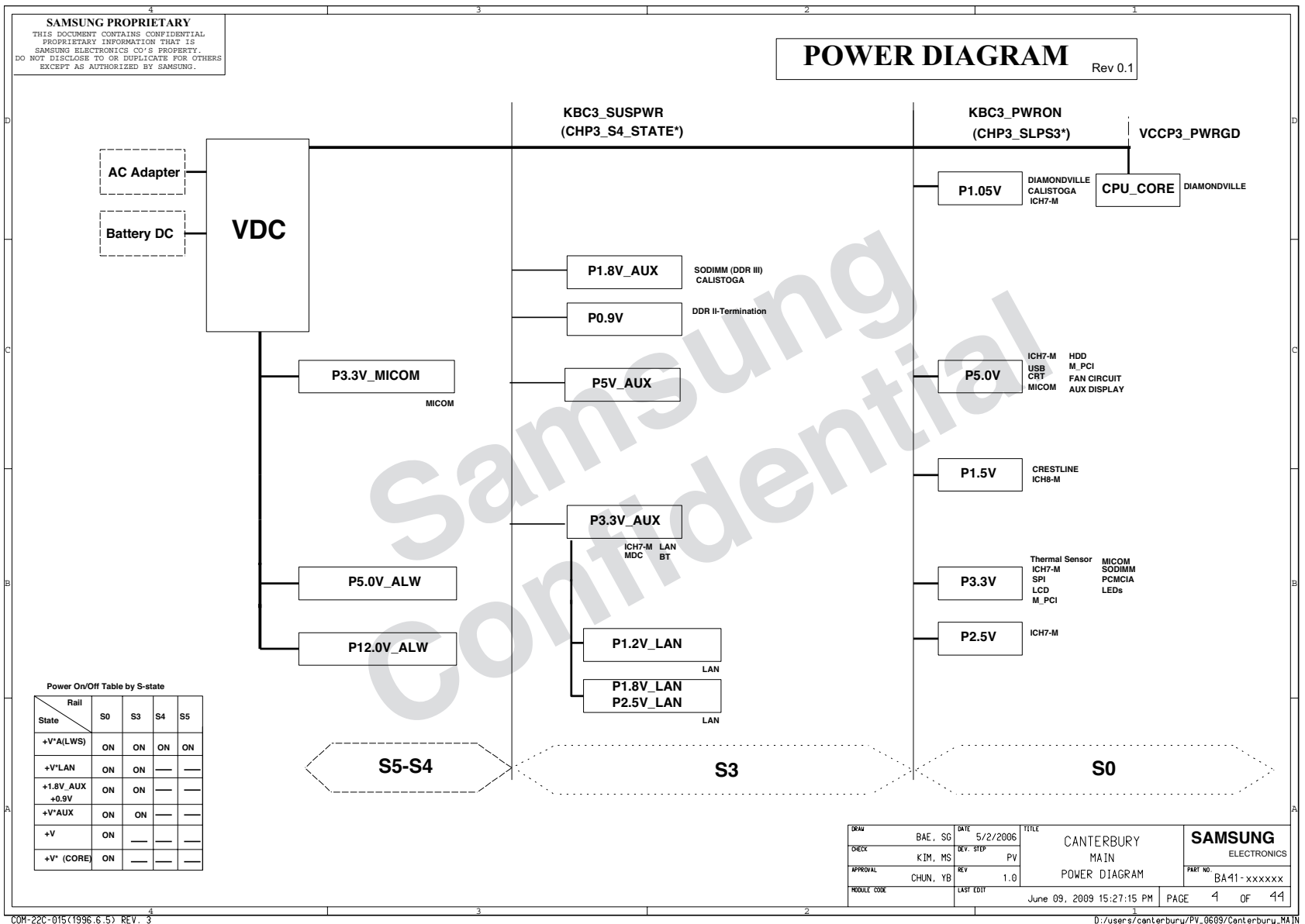
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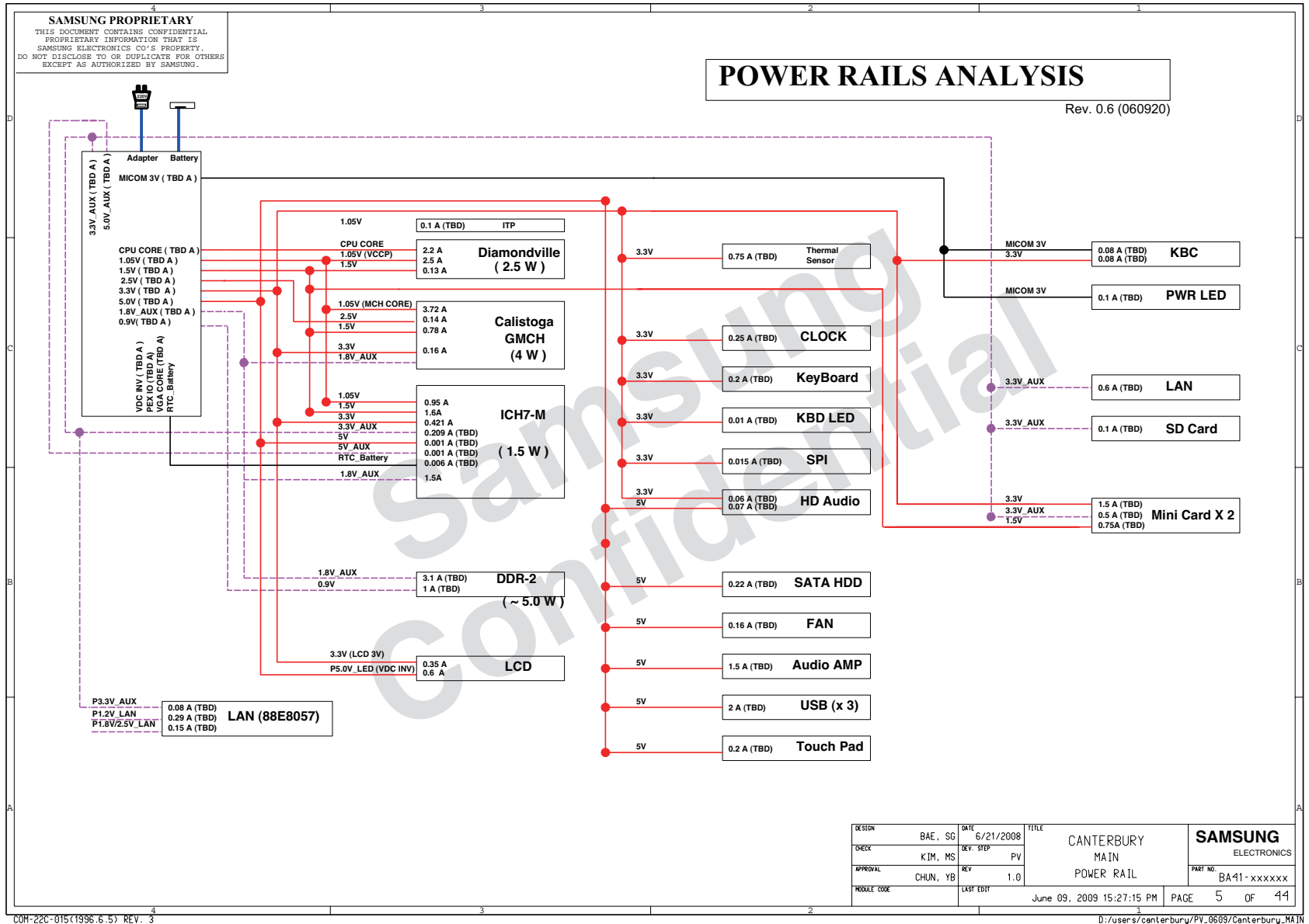
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8-3

8. Block Diagram and Schematic



8. Block Diagram and Schematic

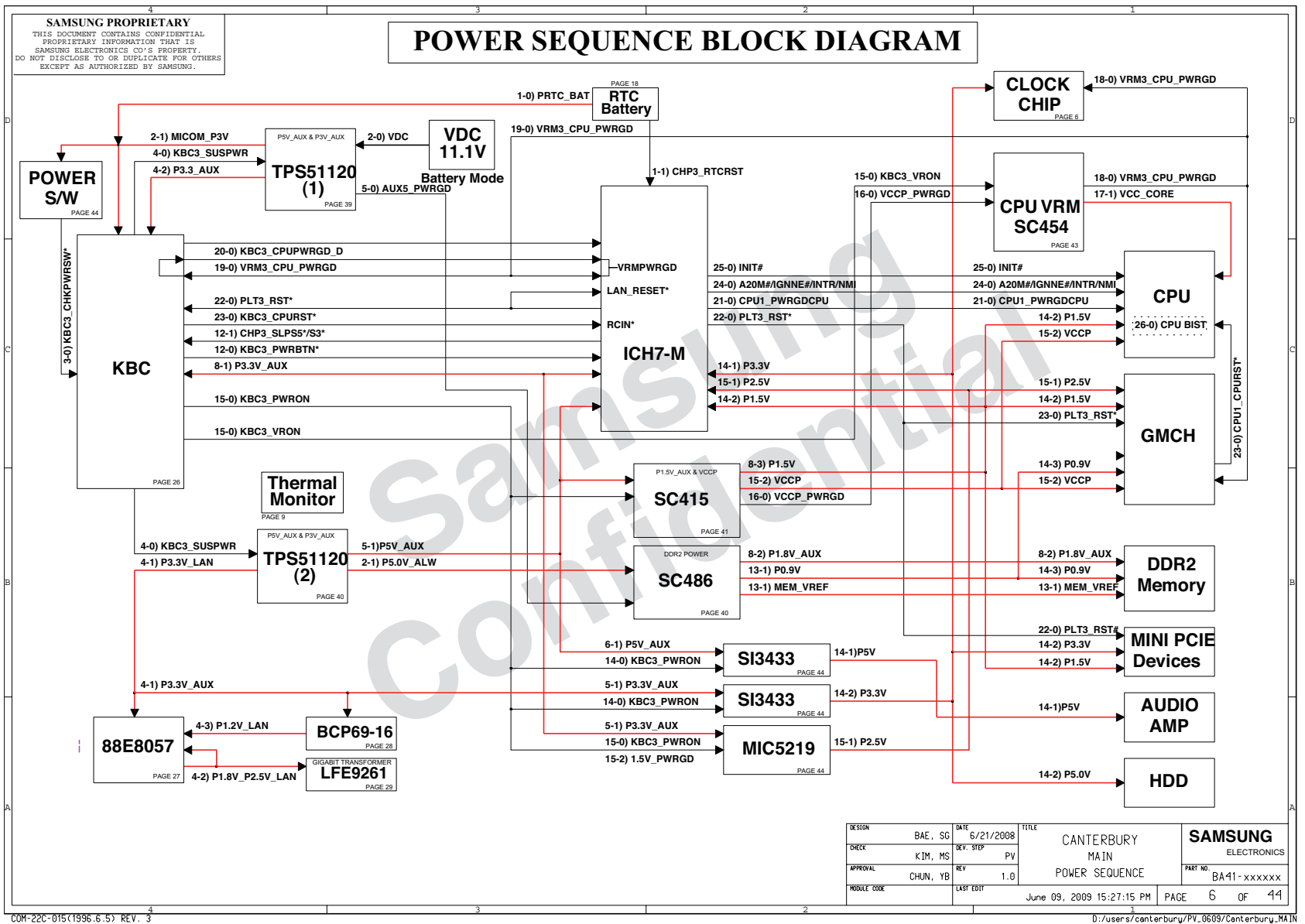


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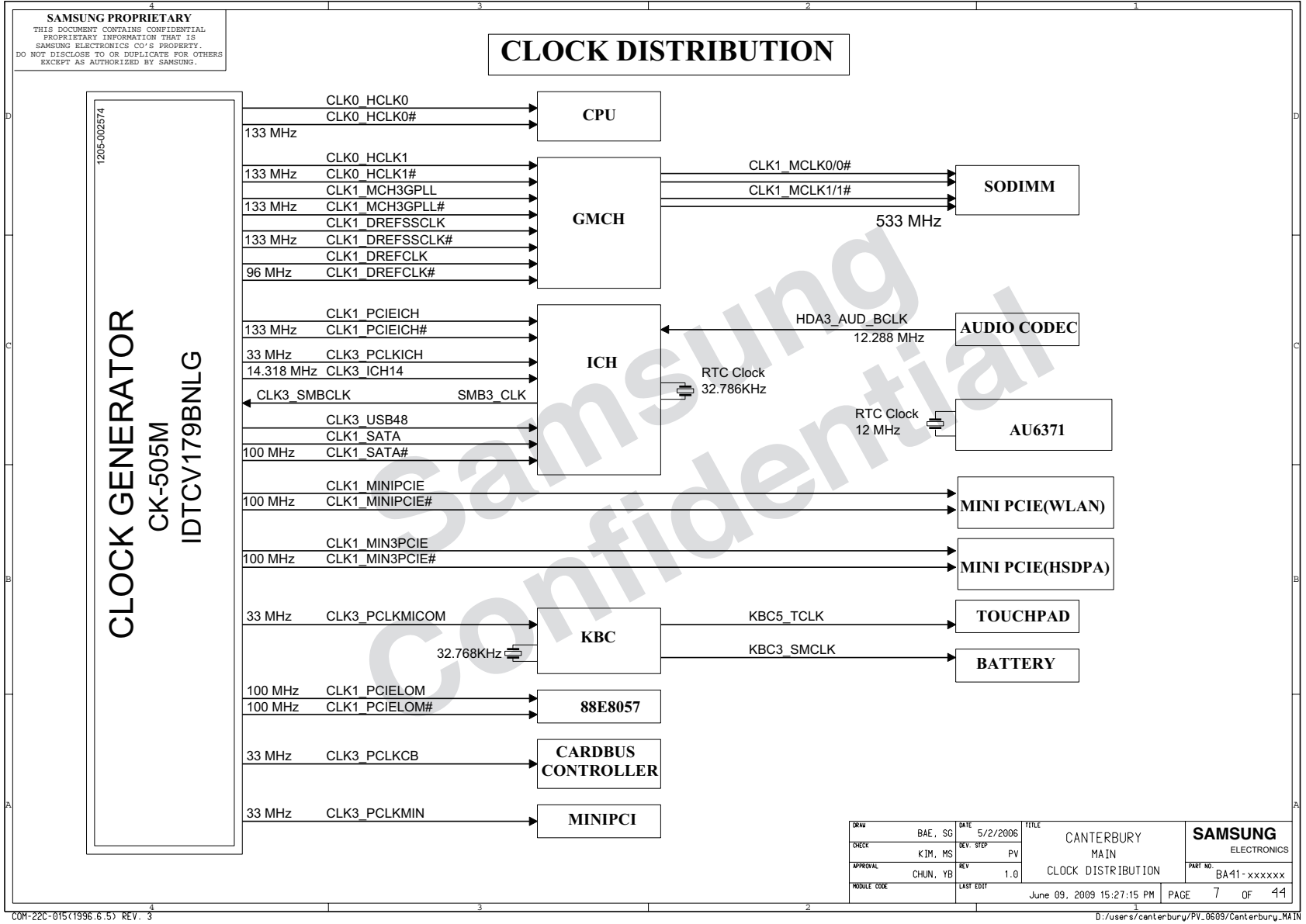
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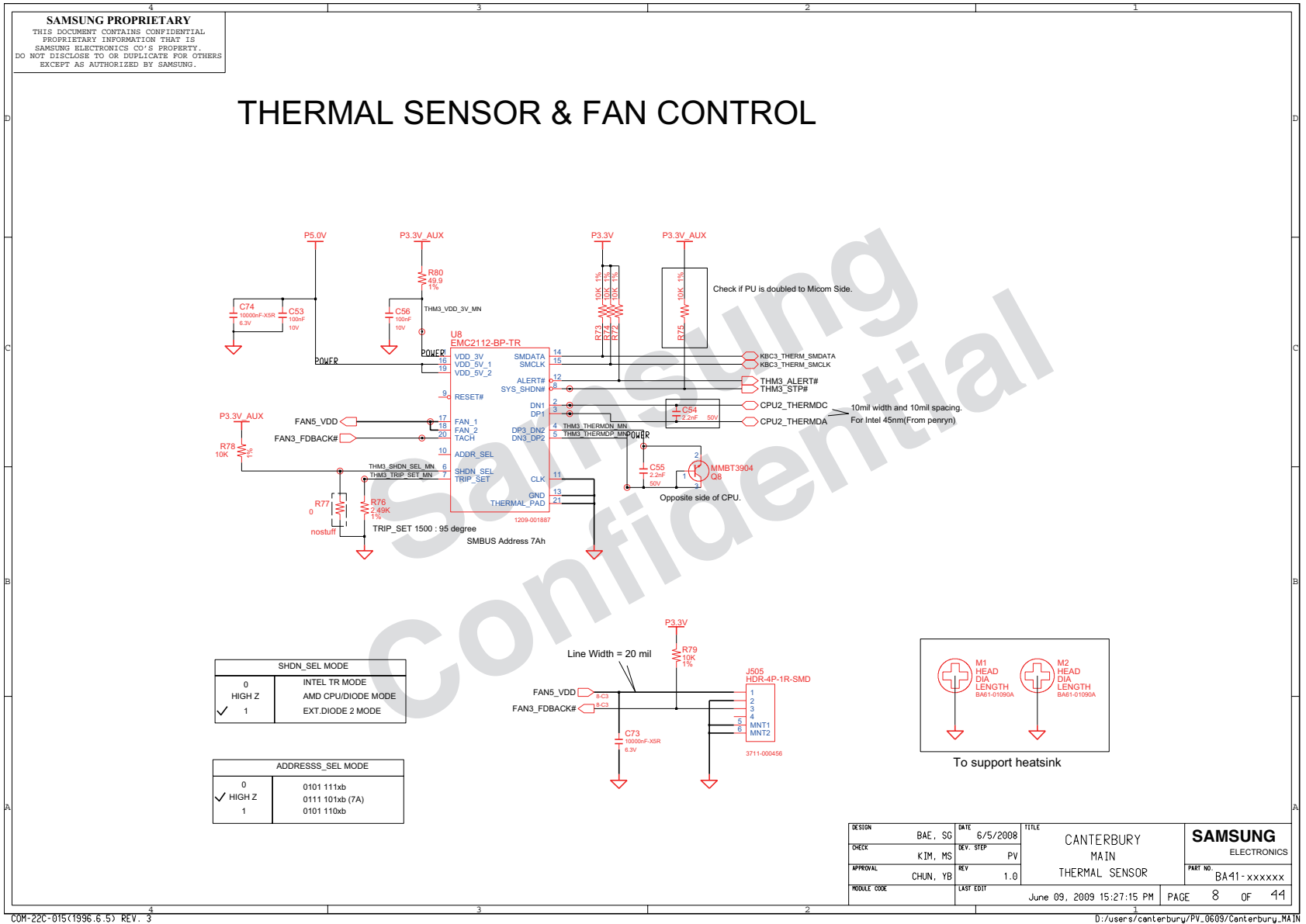
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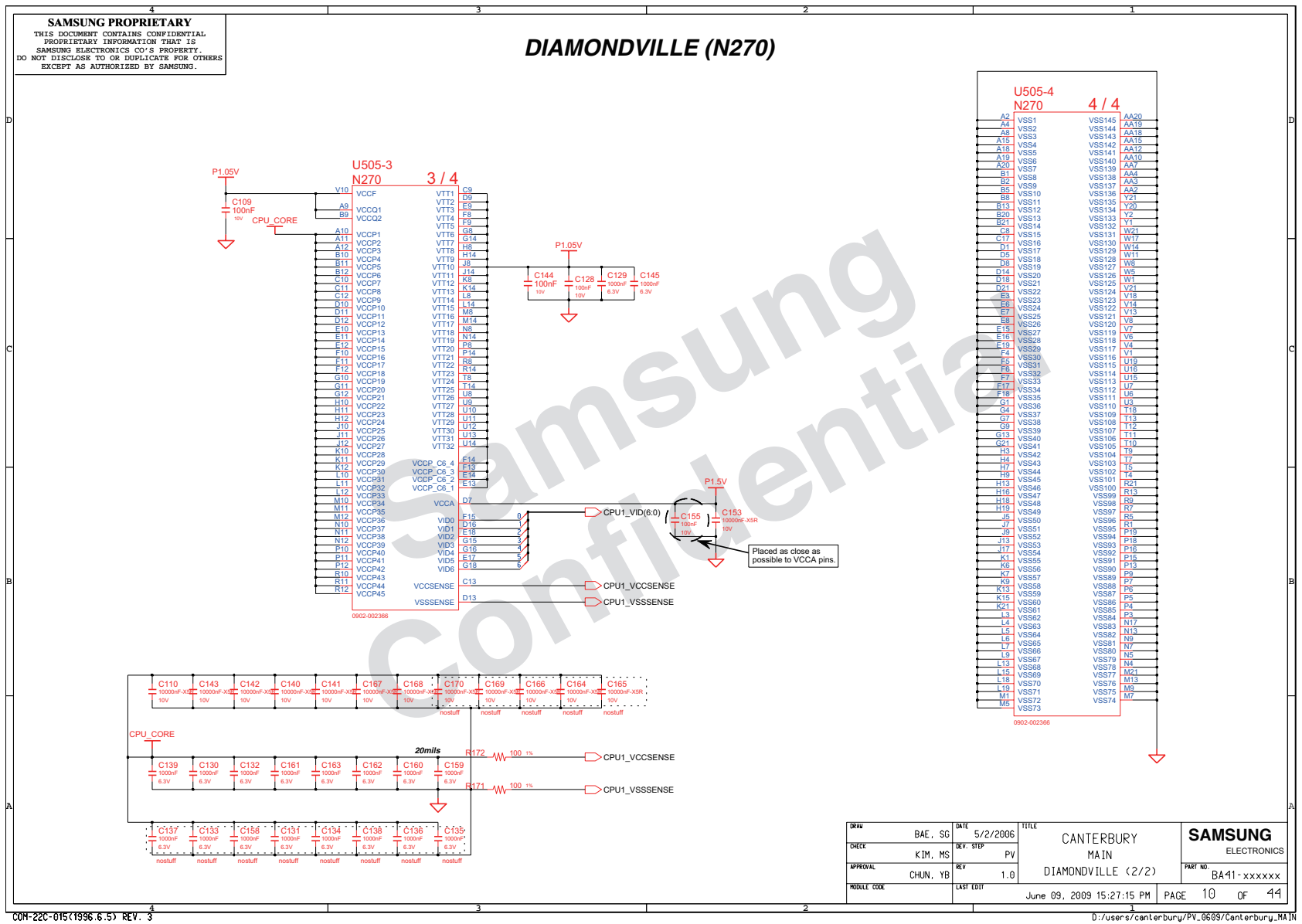
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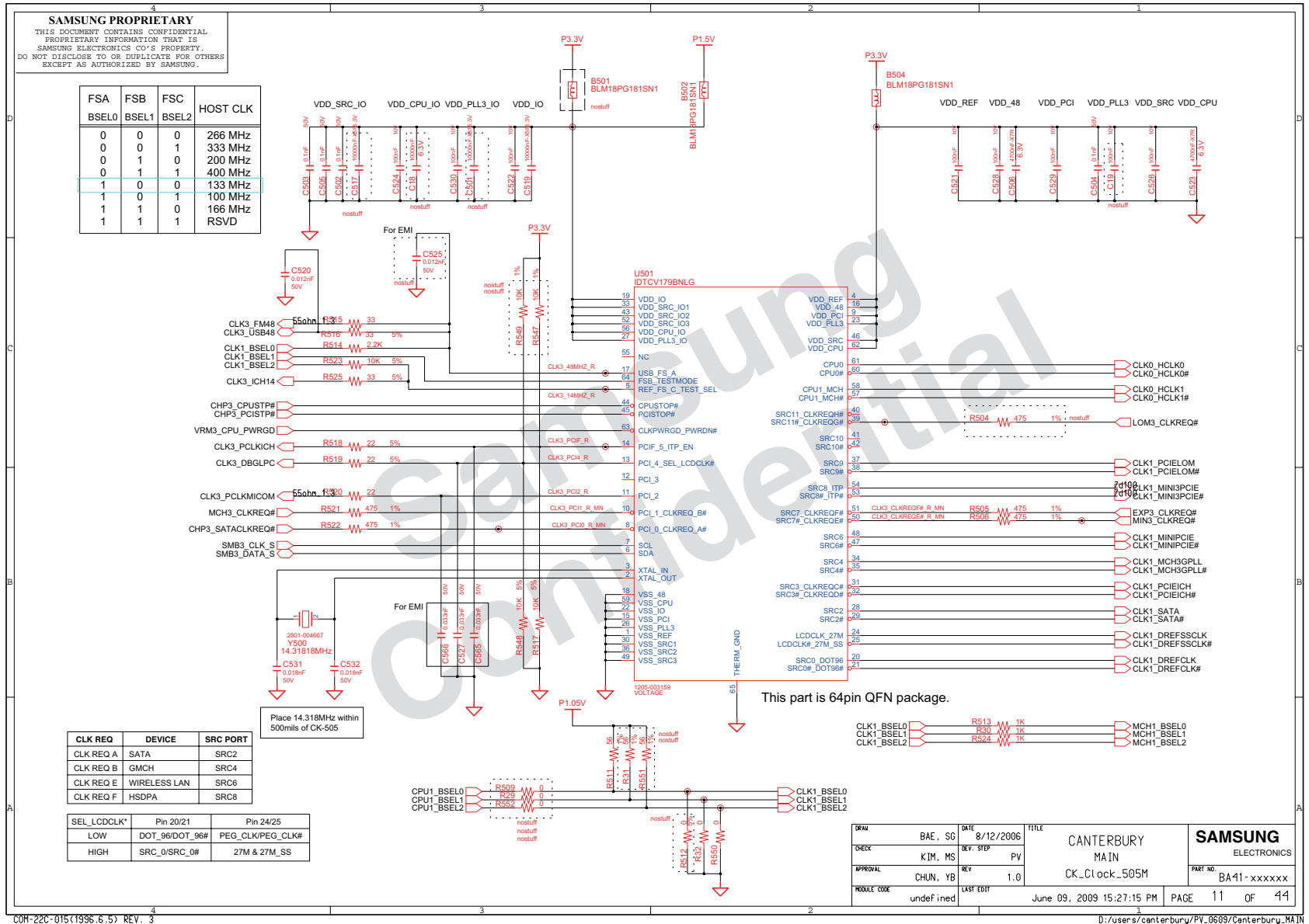
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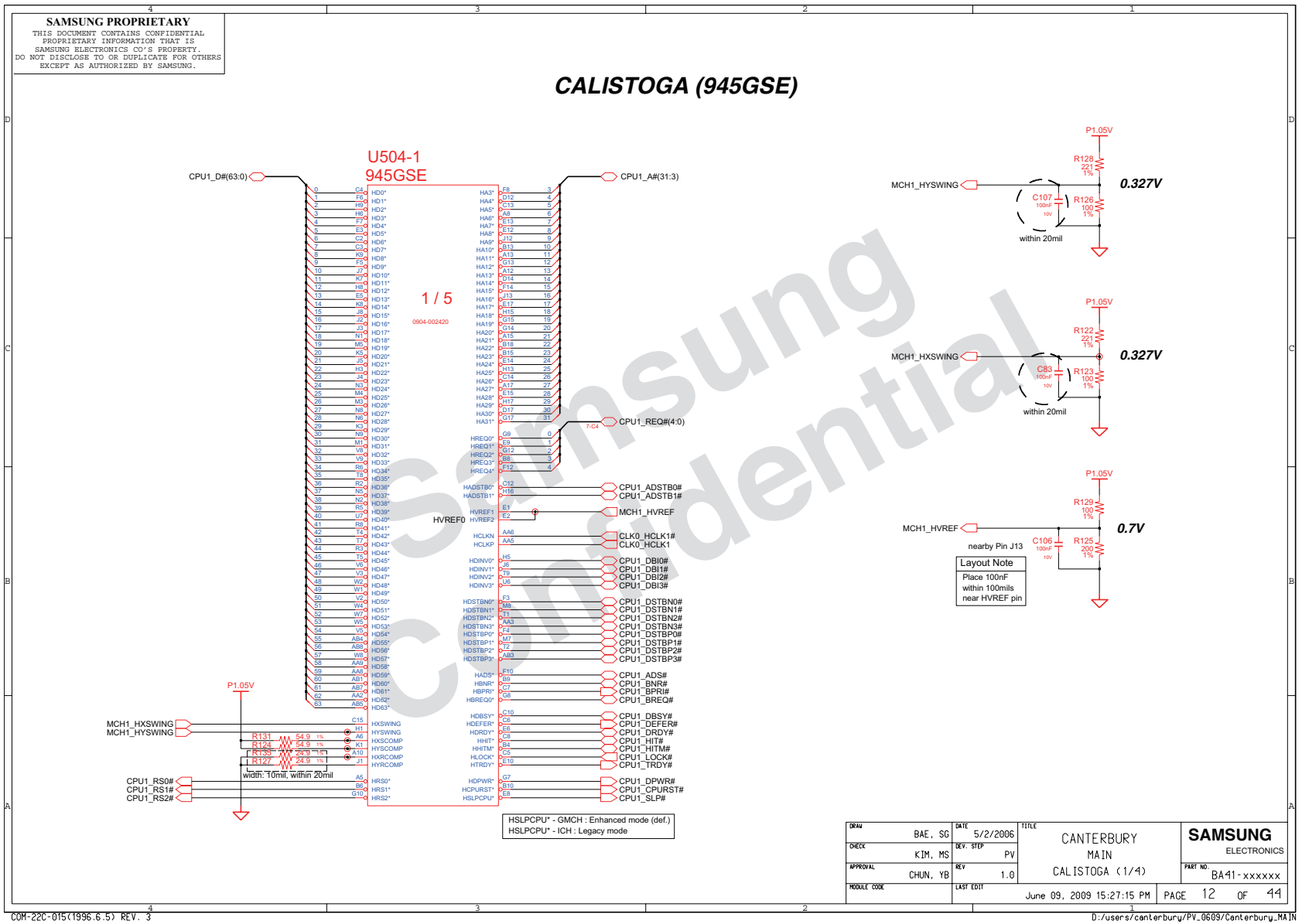
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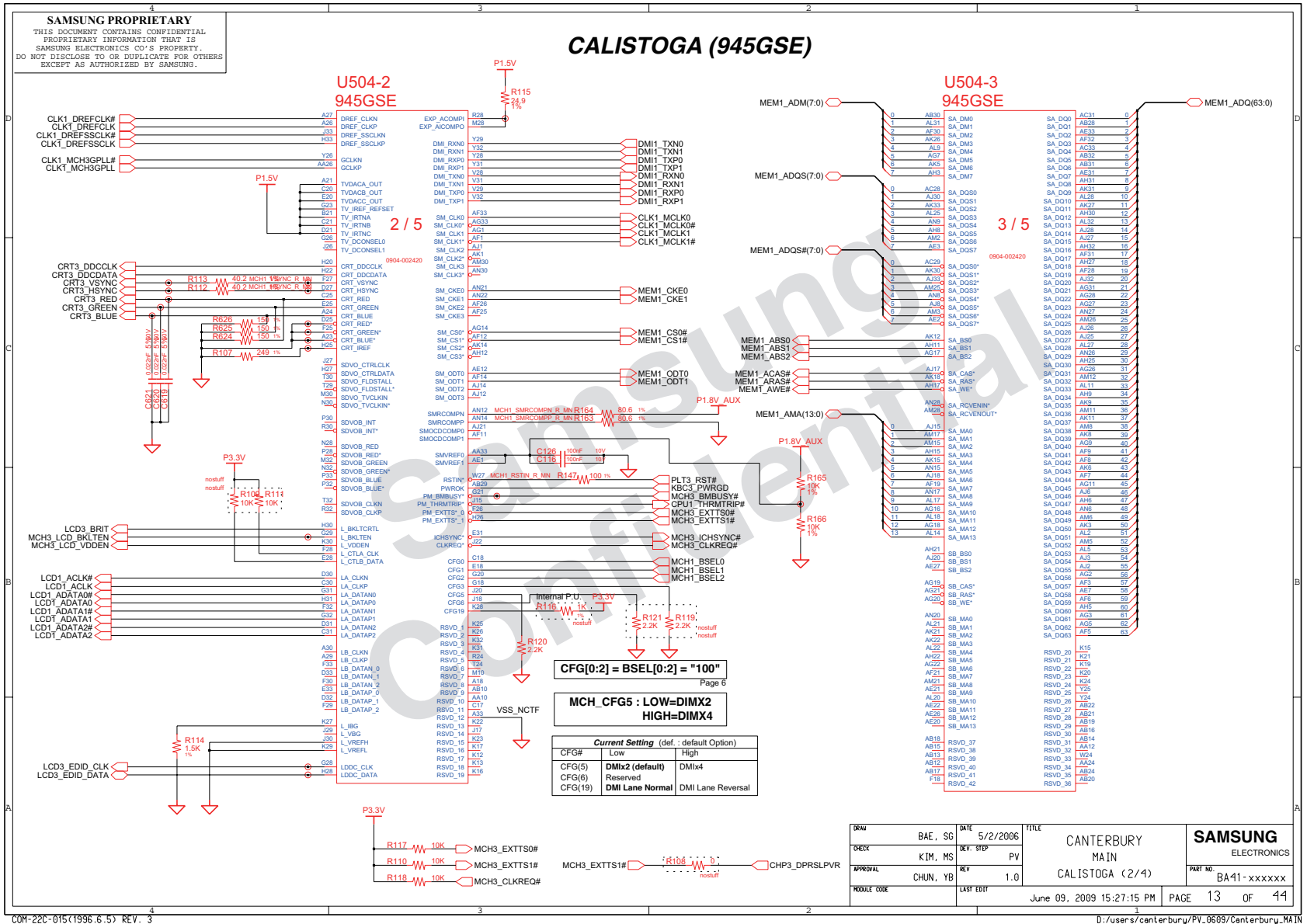
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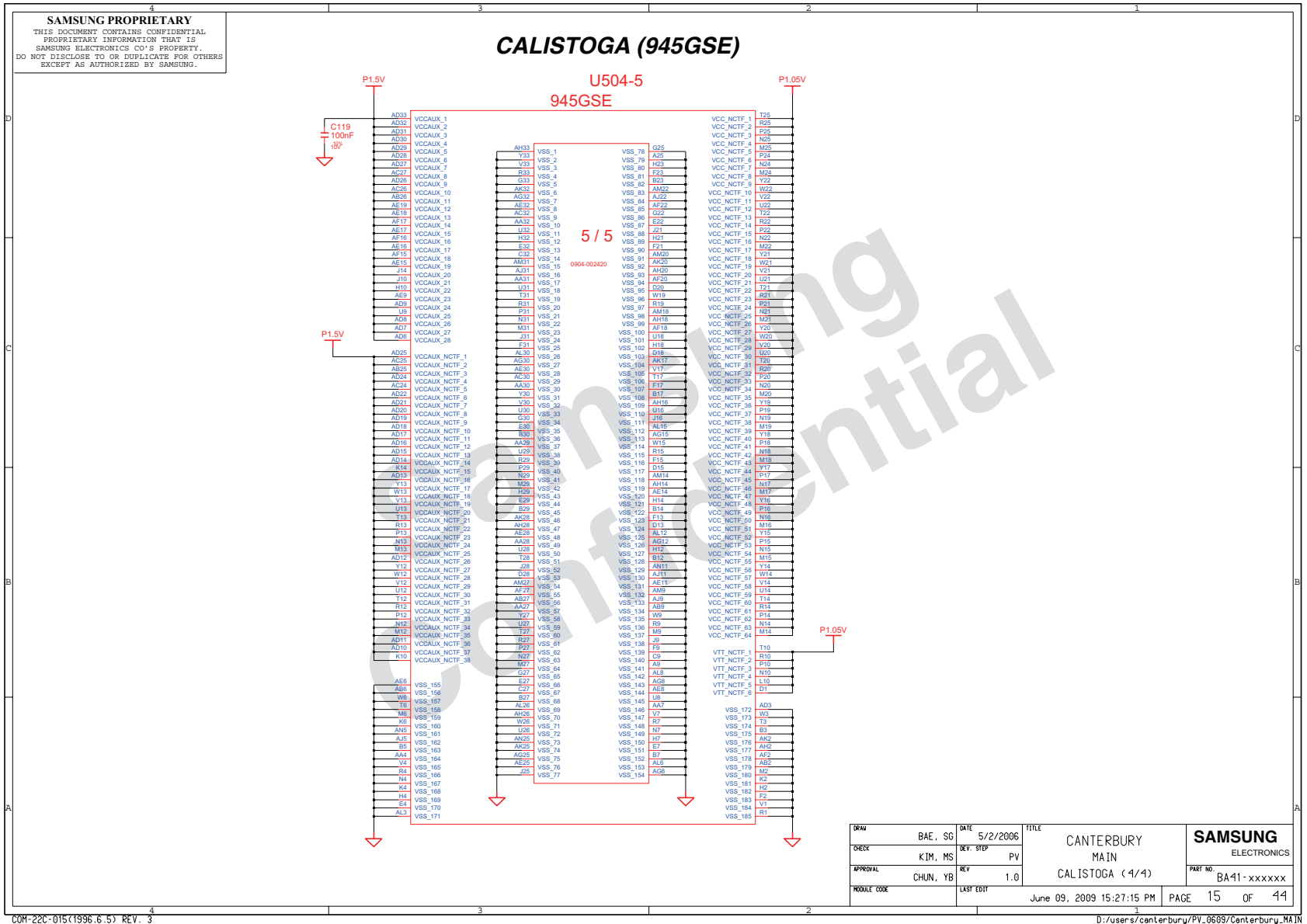
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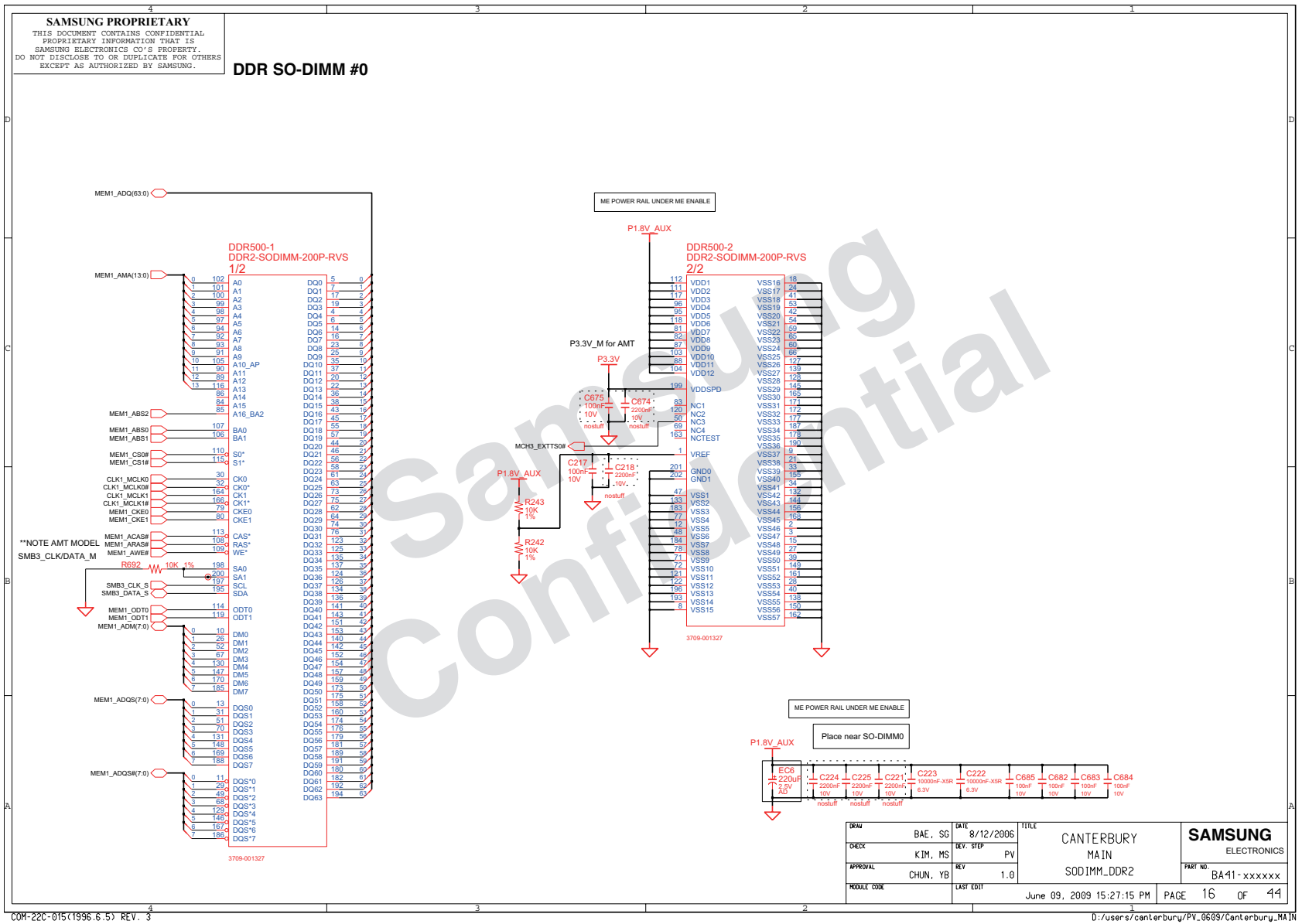
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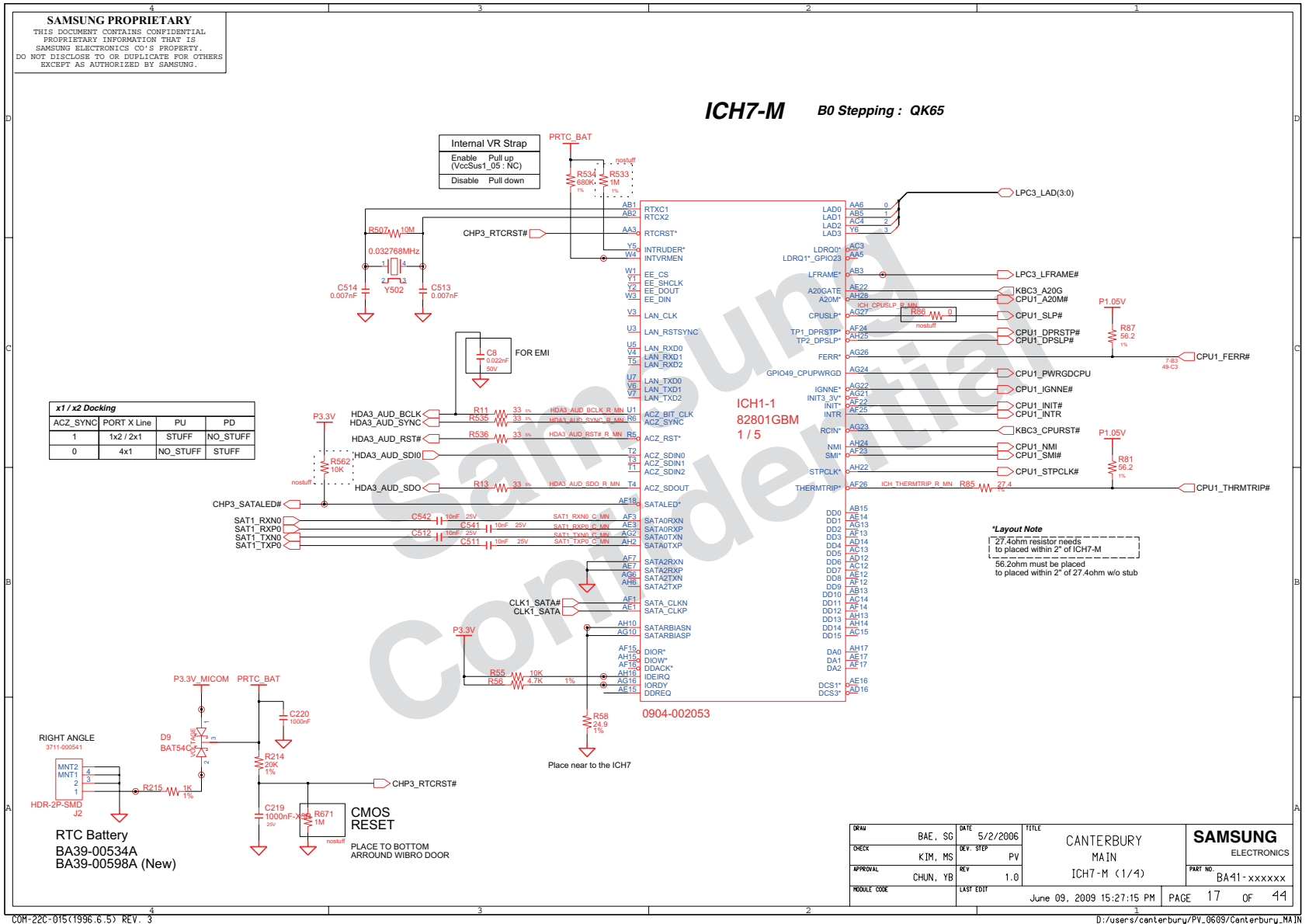
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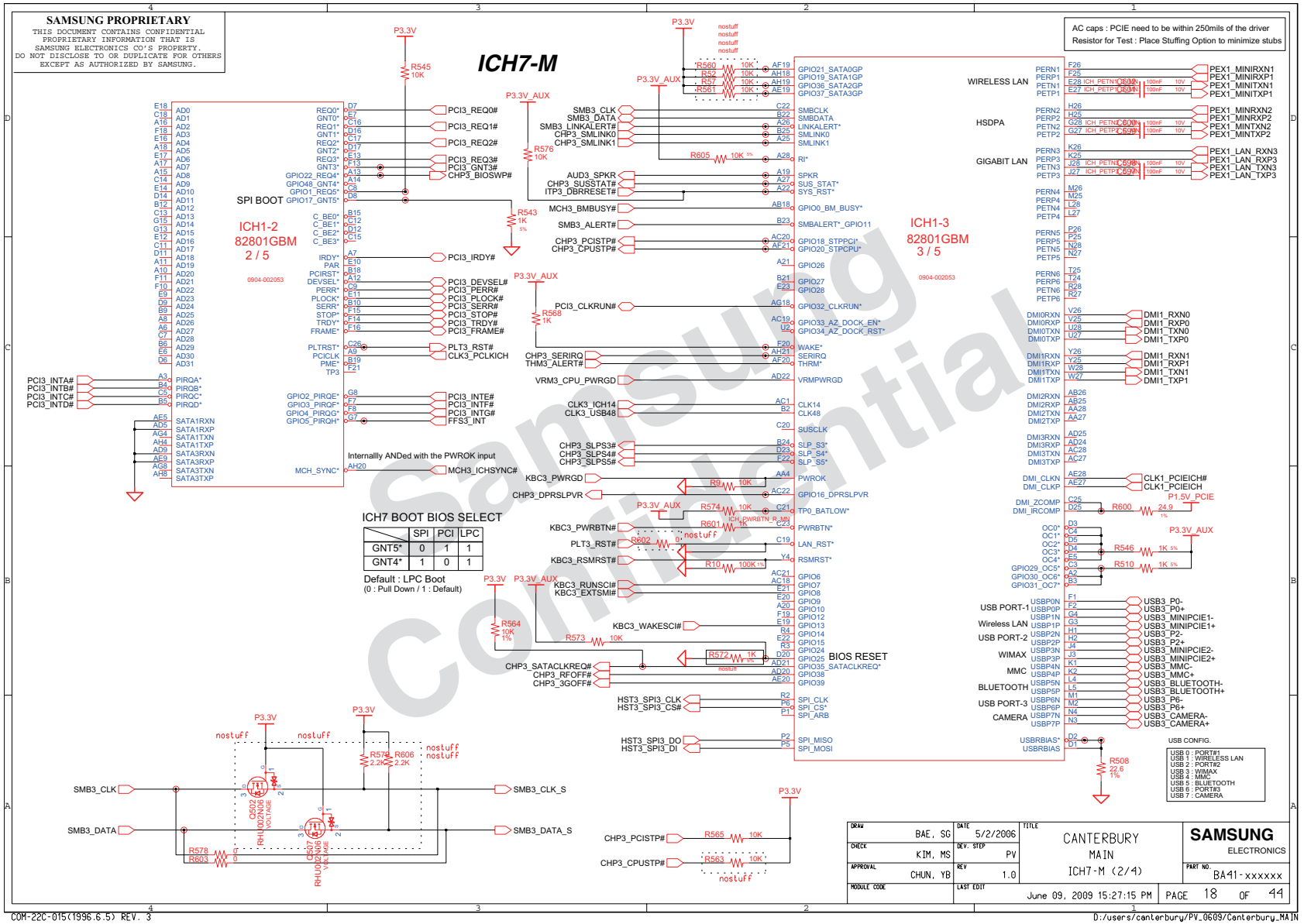
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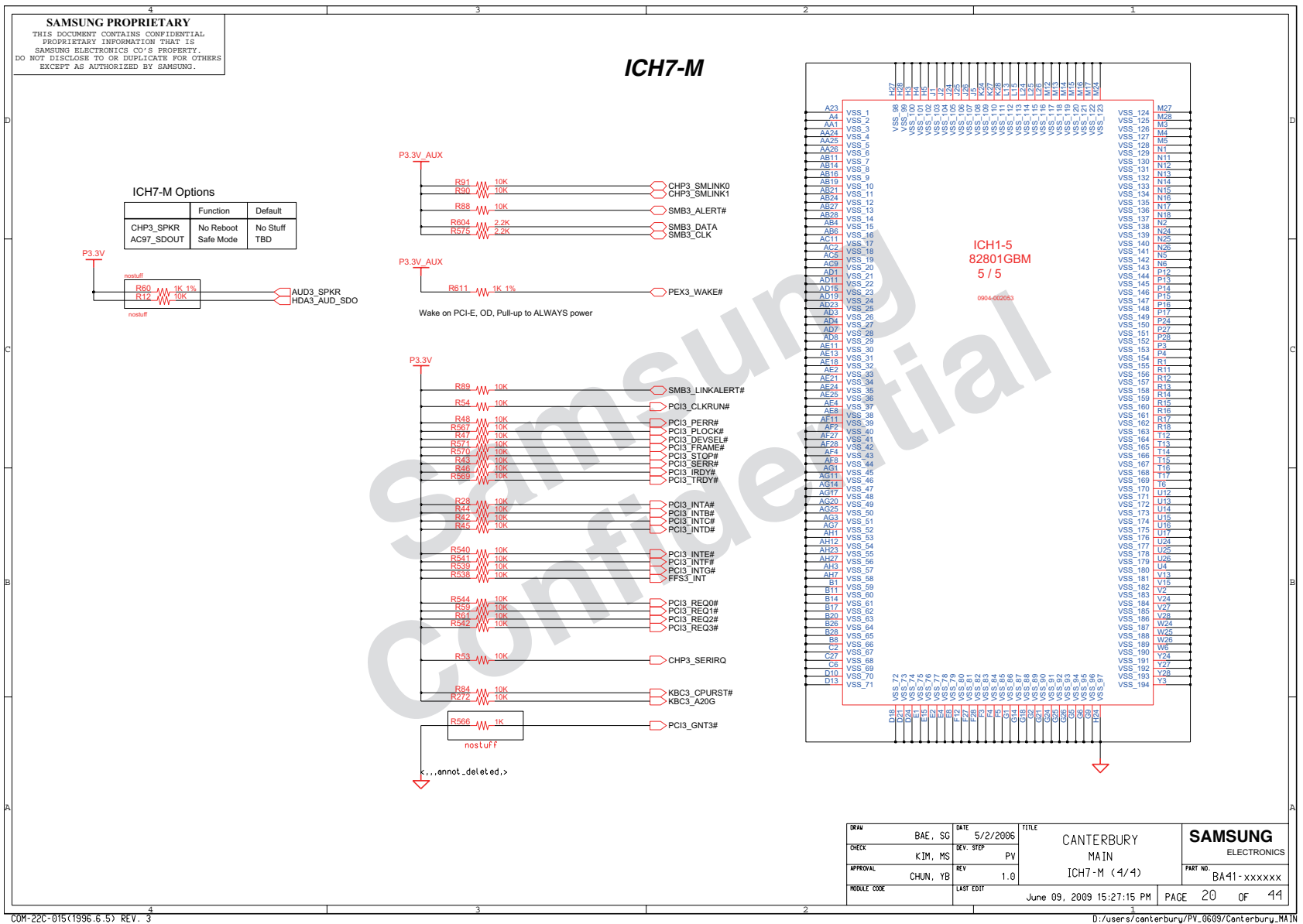


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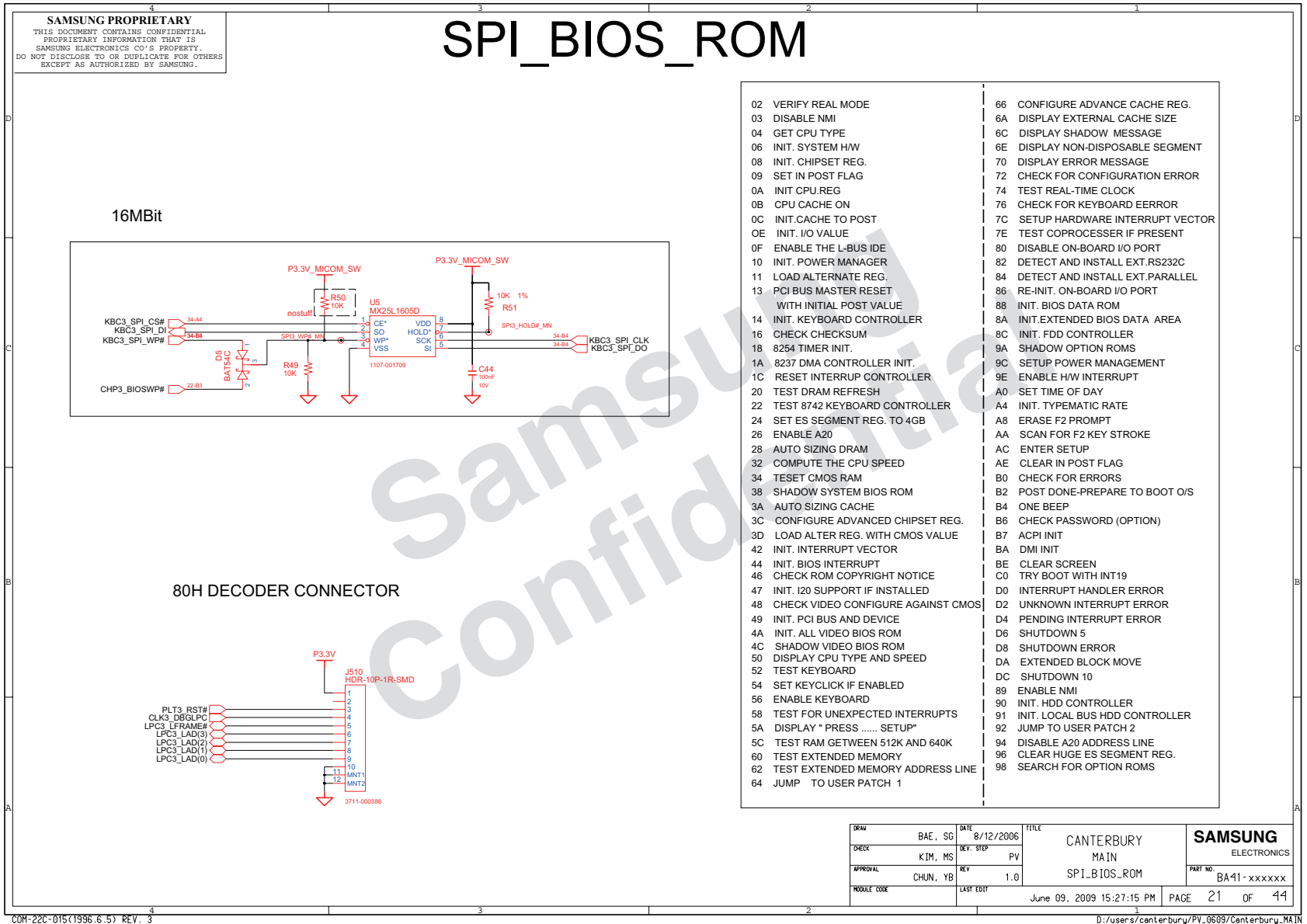
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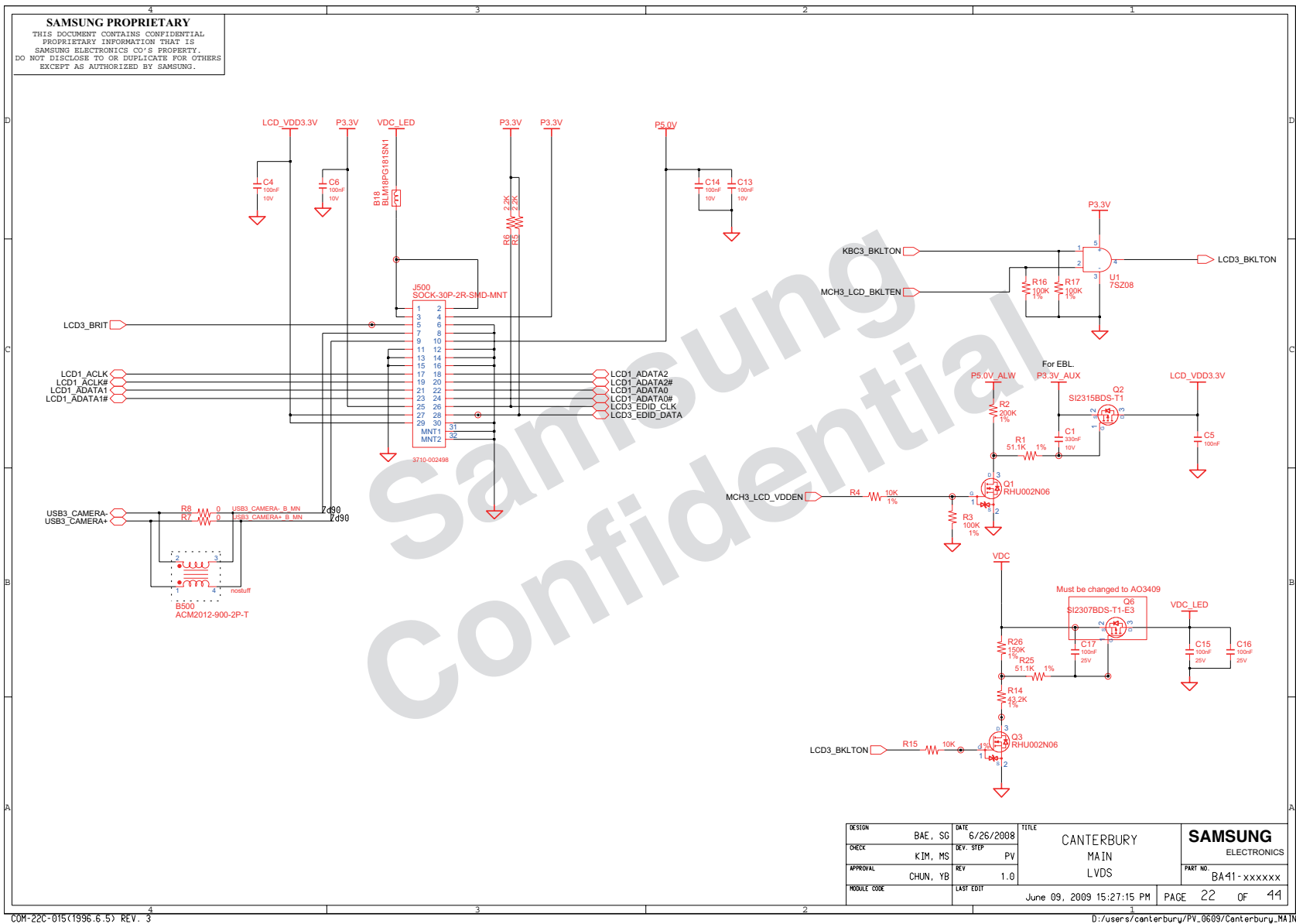


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| APPROVAL | CHUN, YB | LAST EDIT | June 09, 2009 15:27:15 PM | PAGE | 20 OF 44 | |
| MODULE CODE | | | | | | |

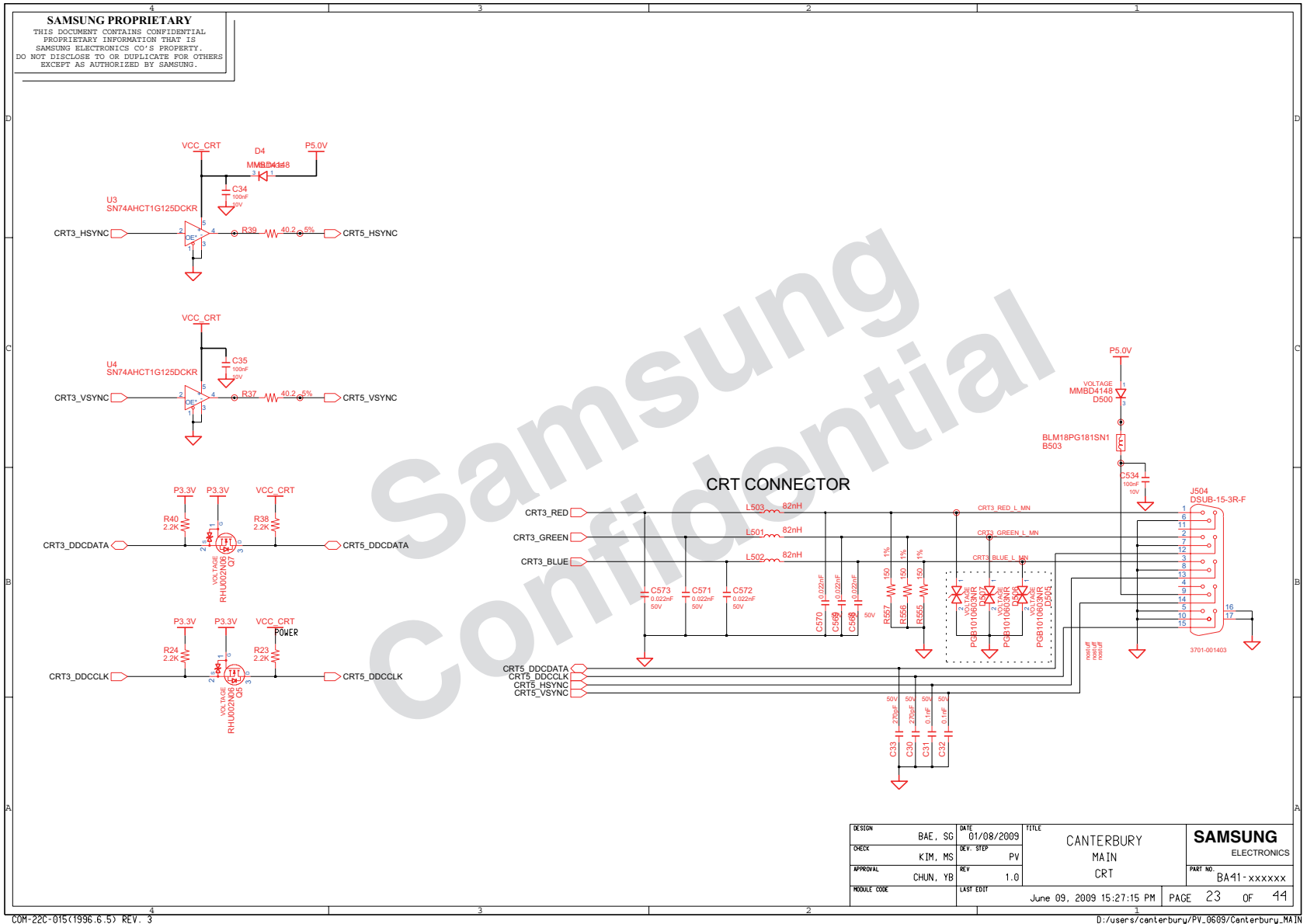
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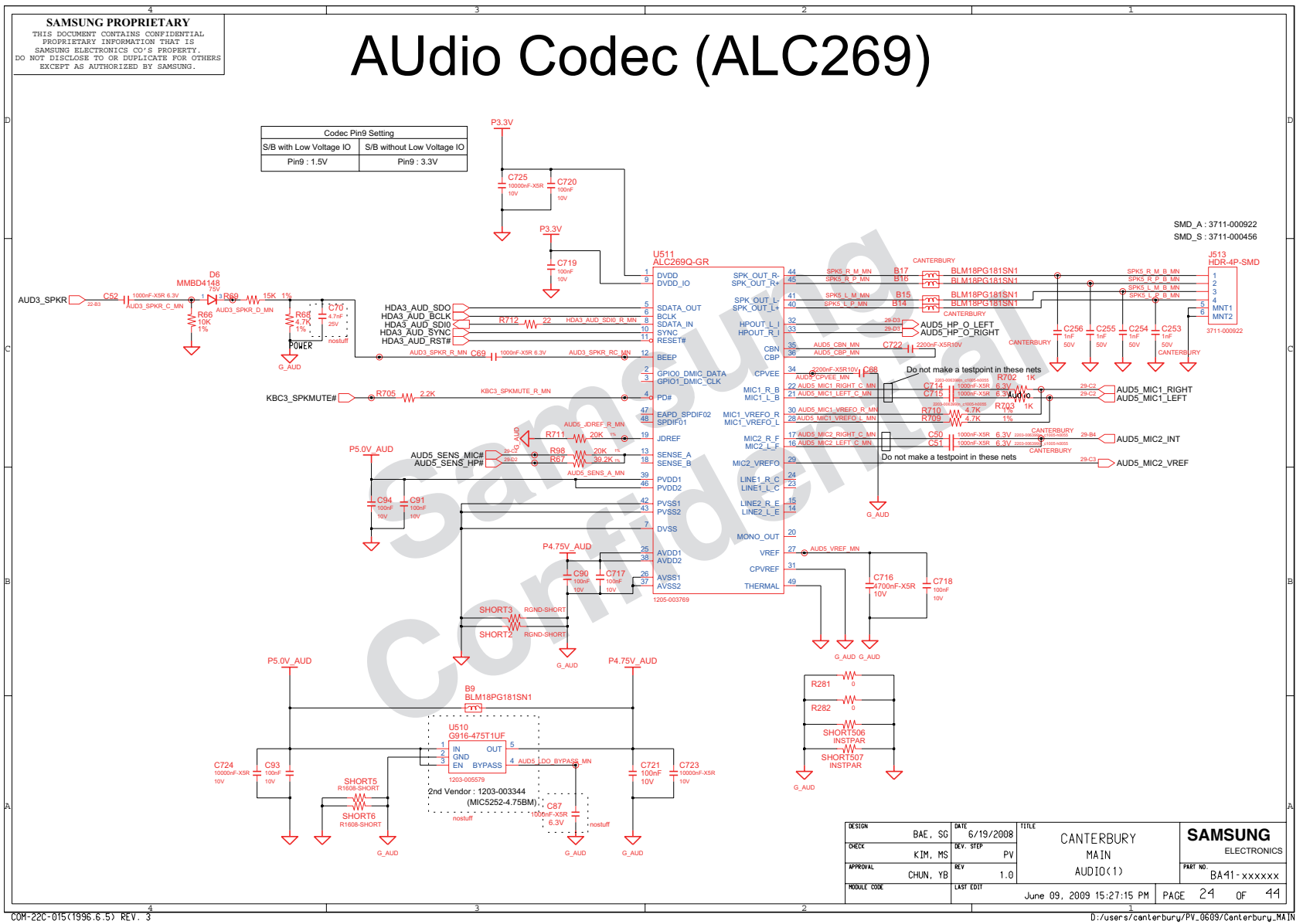
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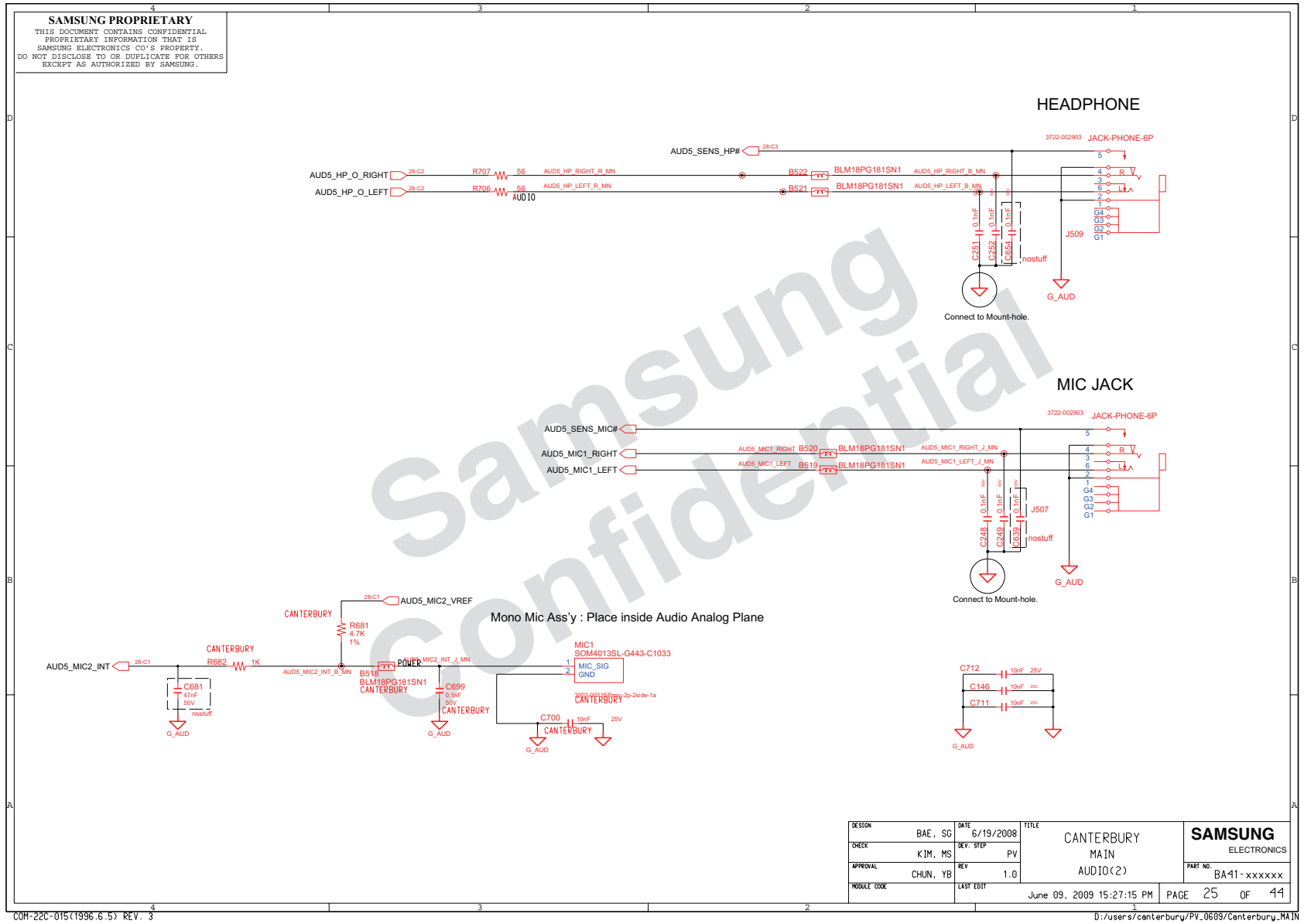
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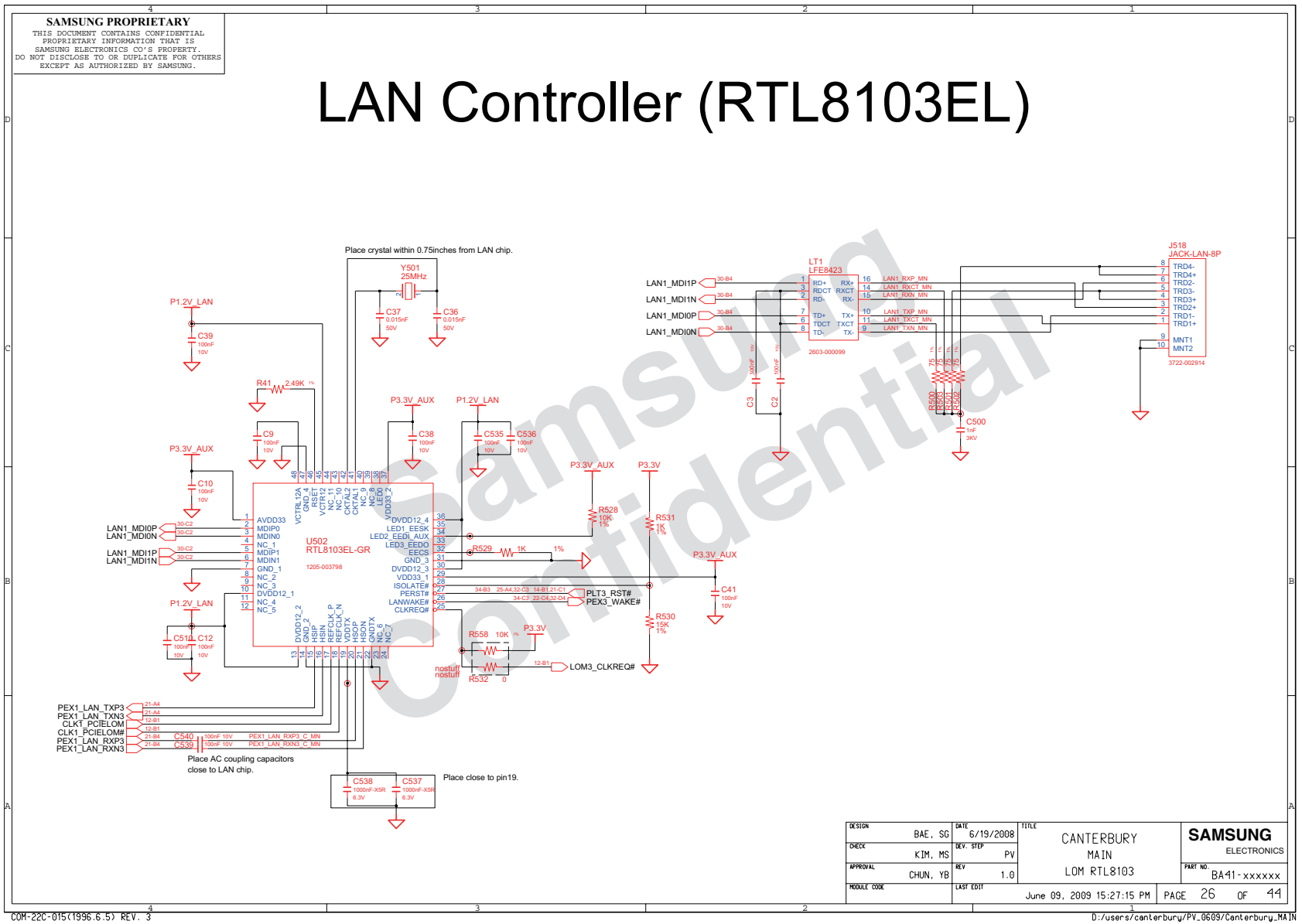
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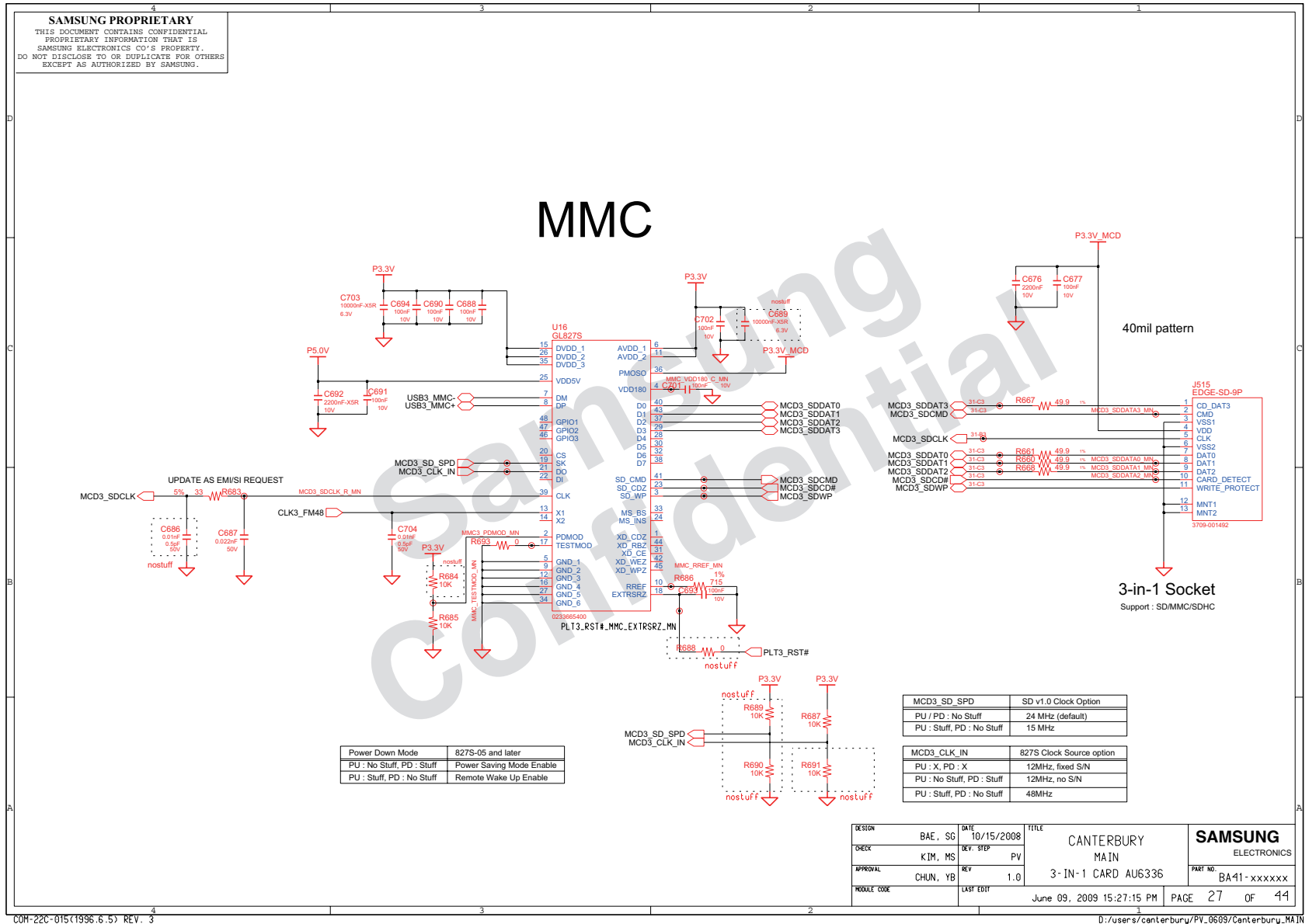
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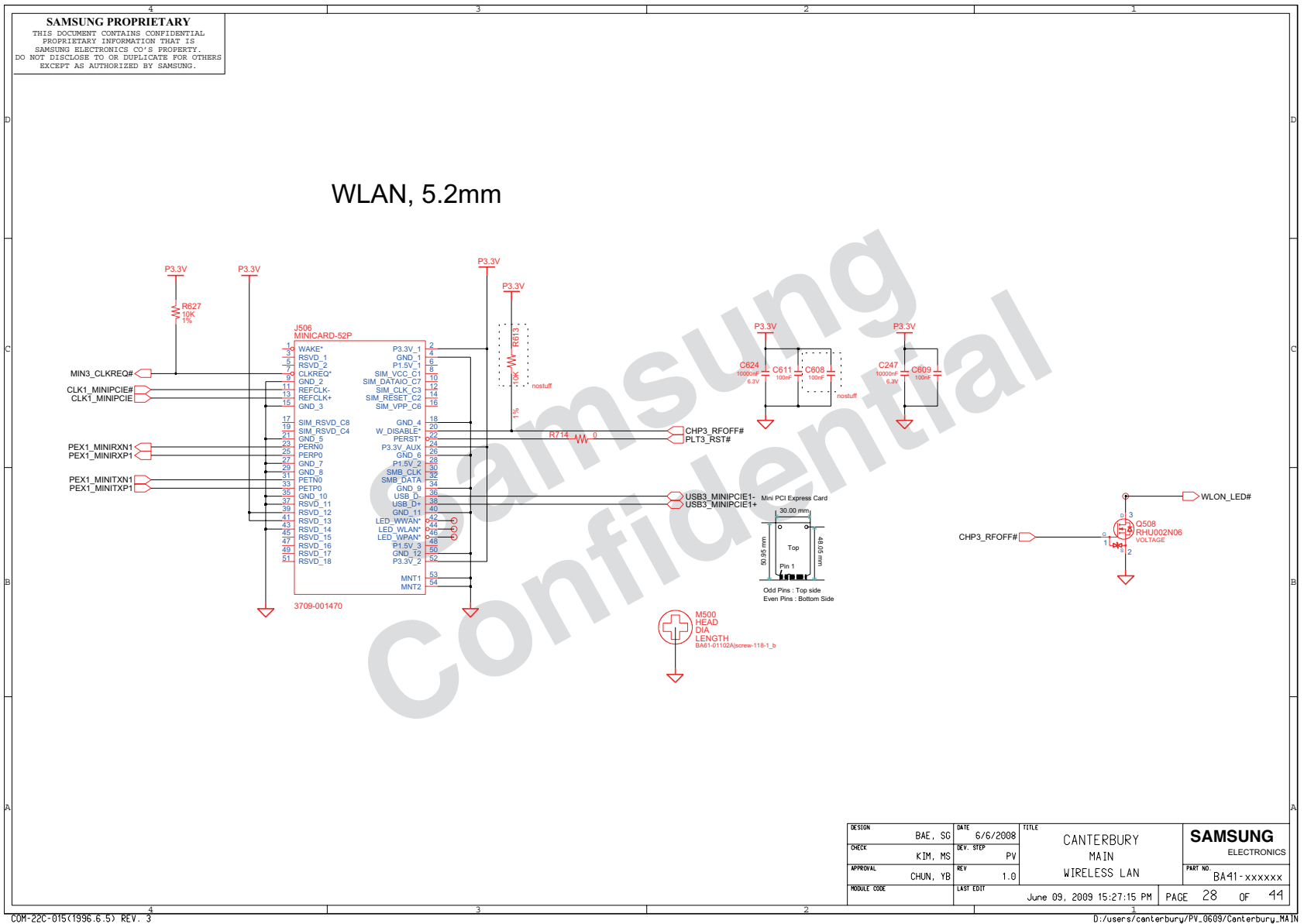
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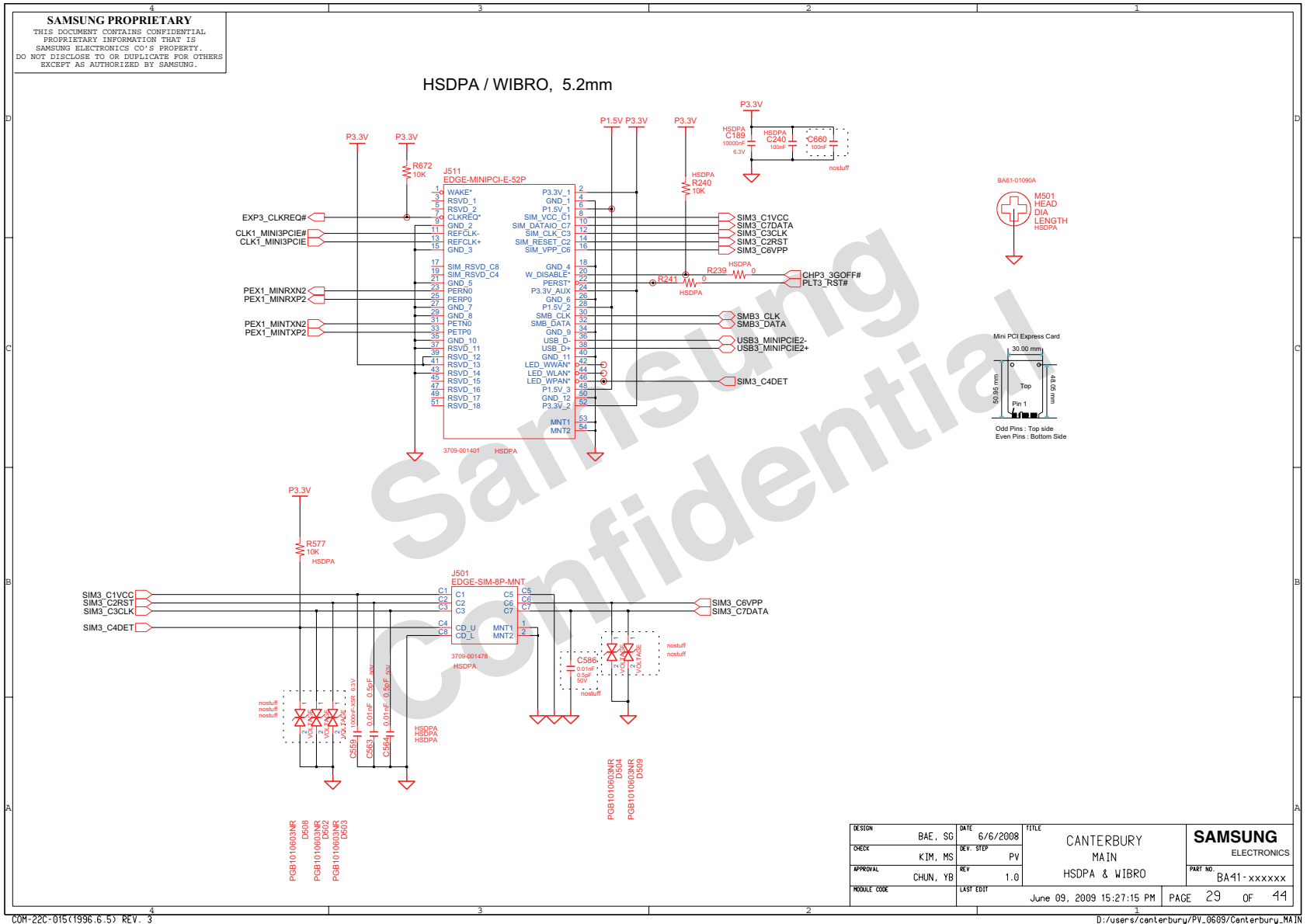


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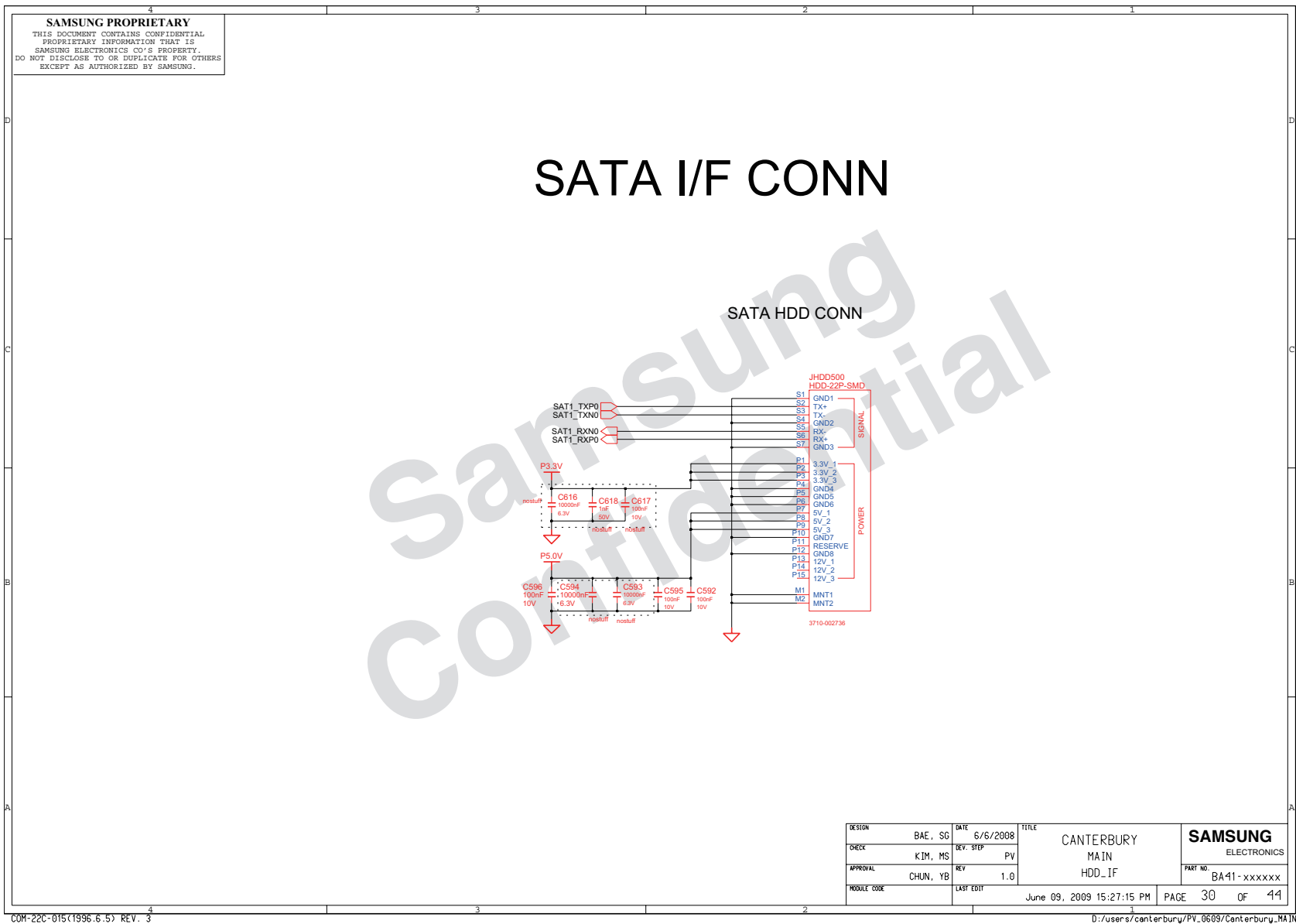


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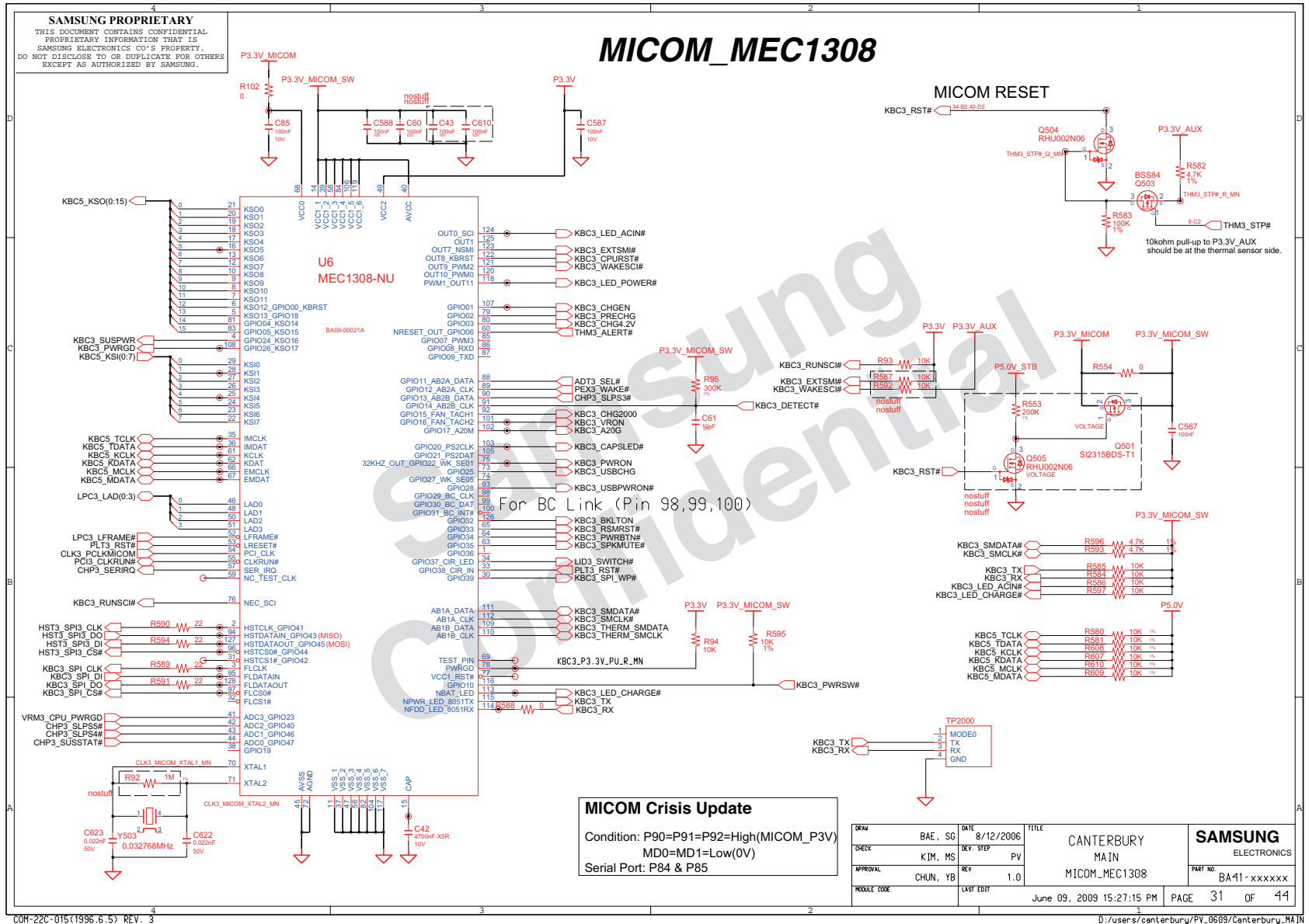
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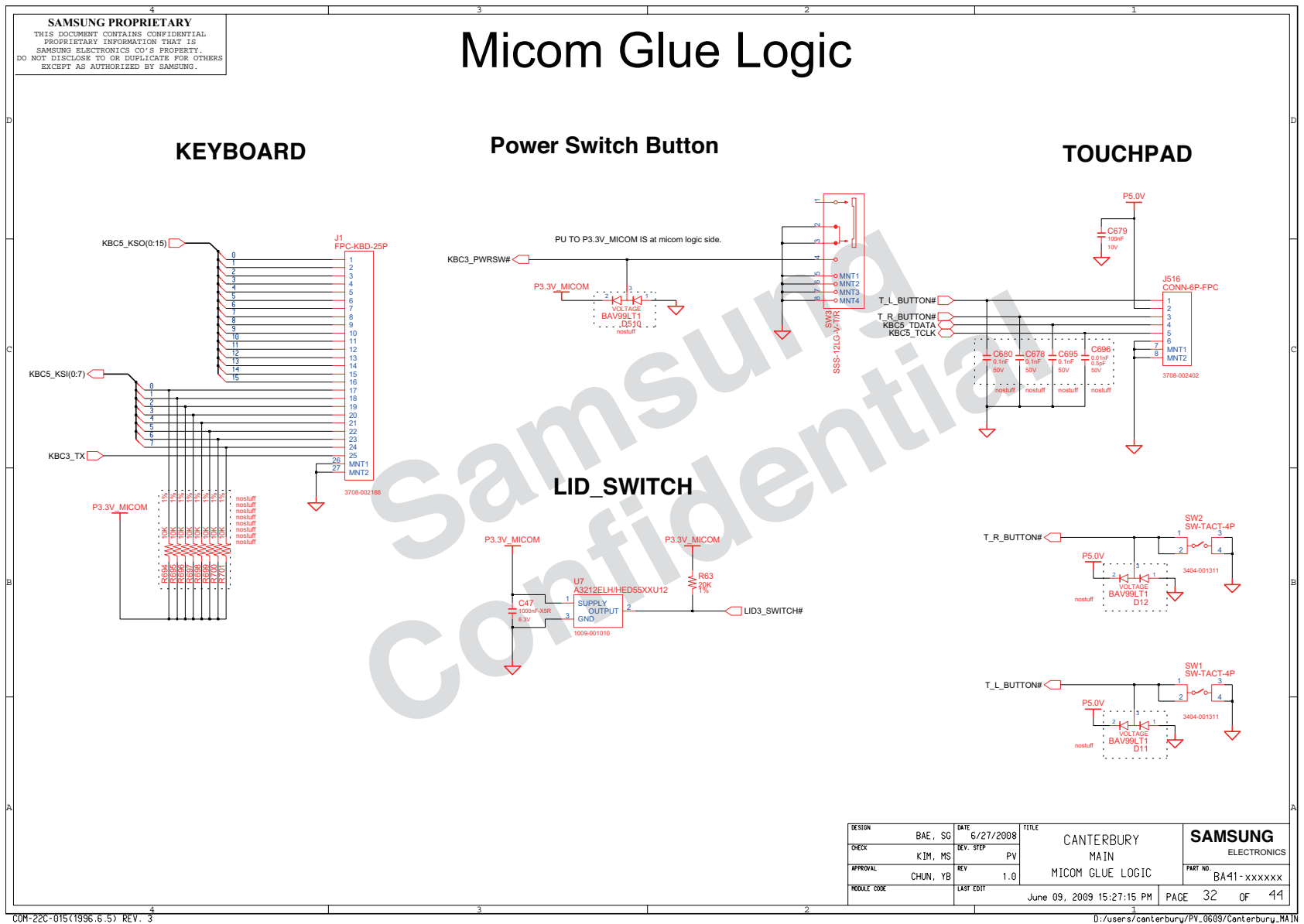
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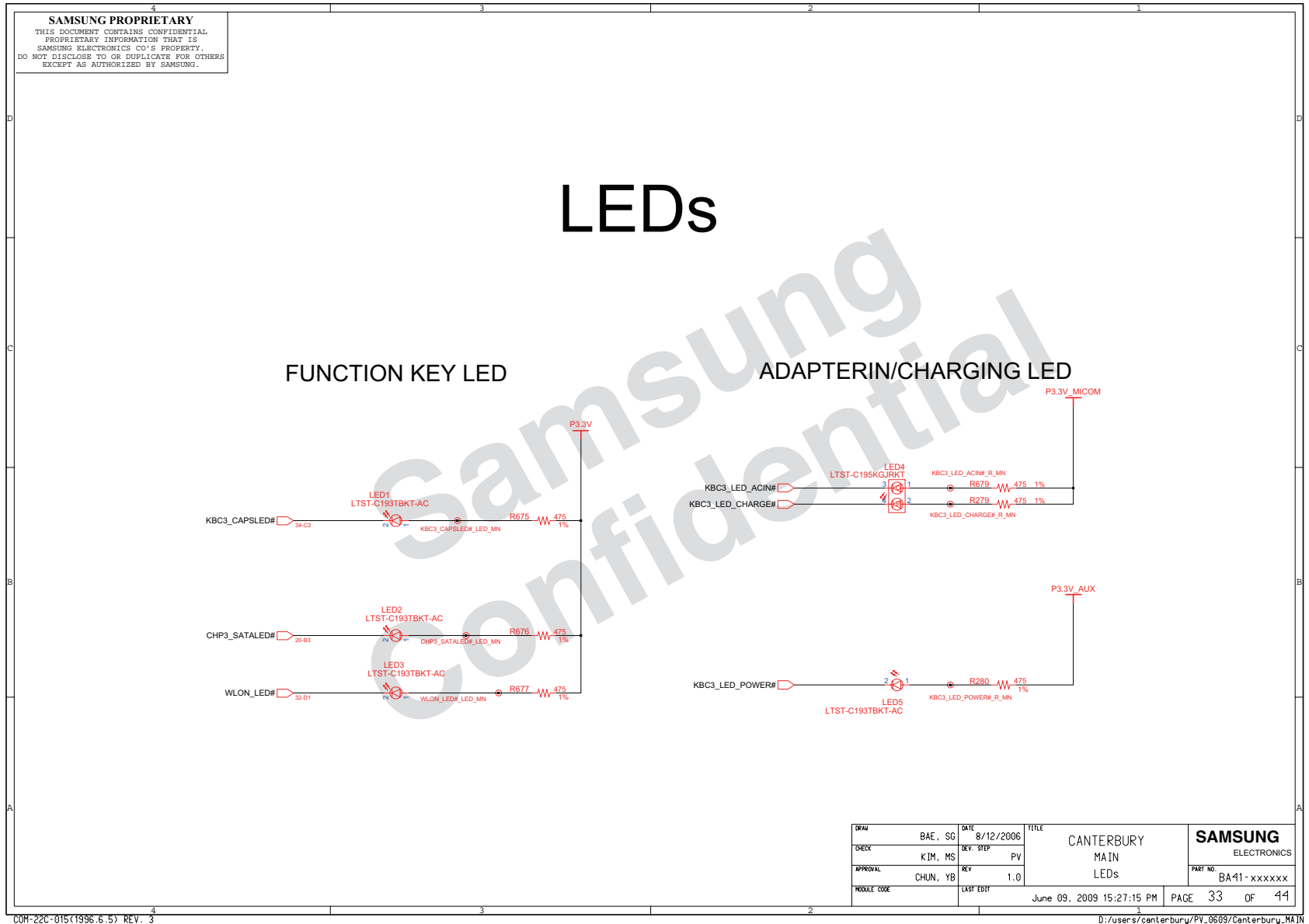
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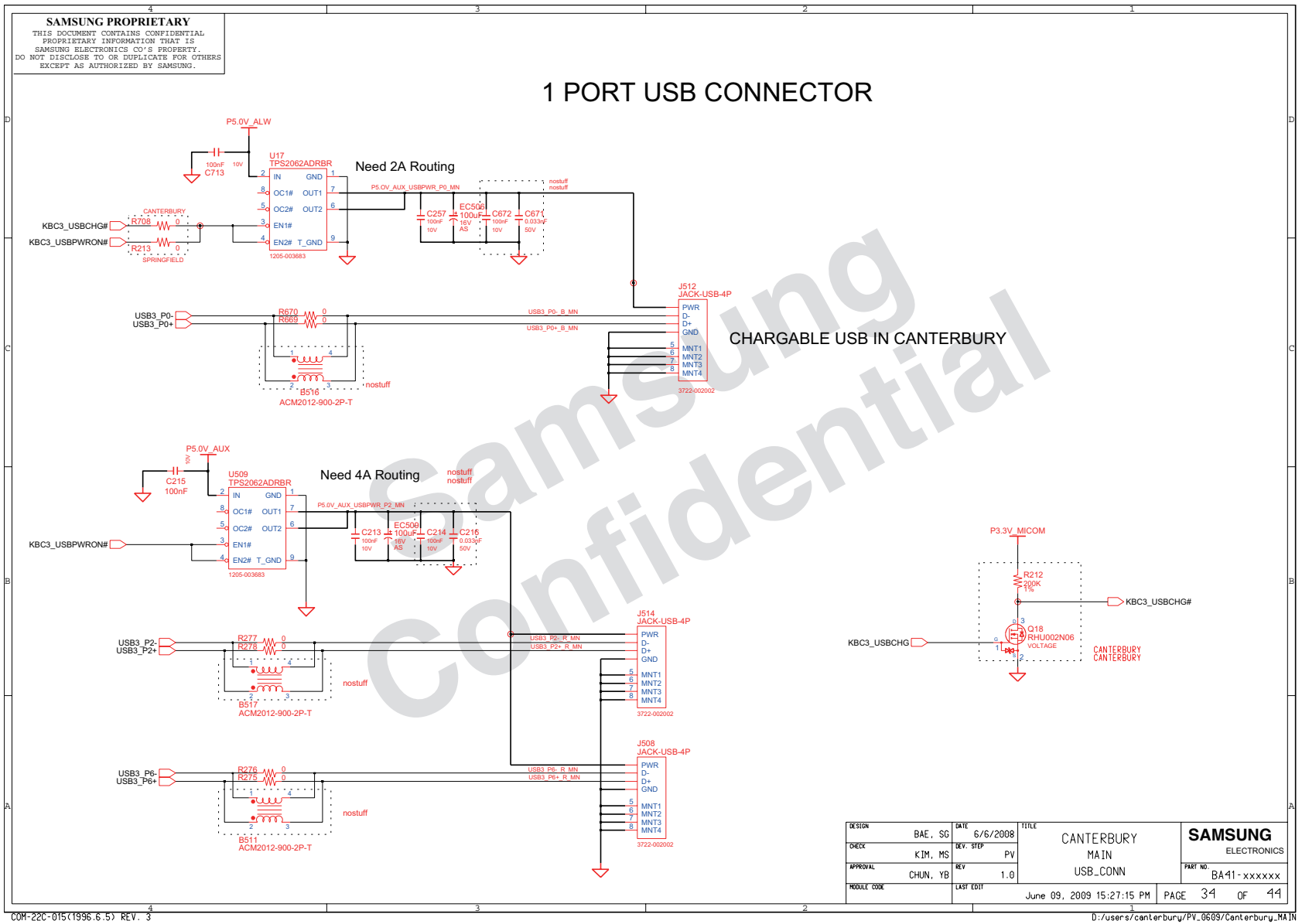
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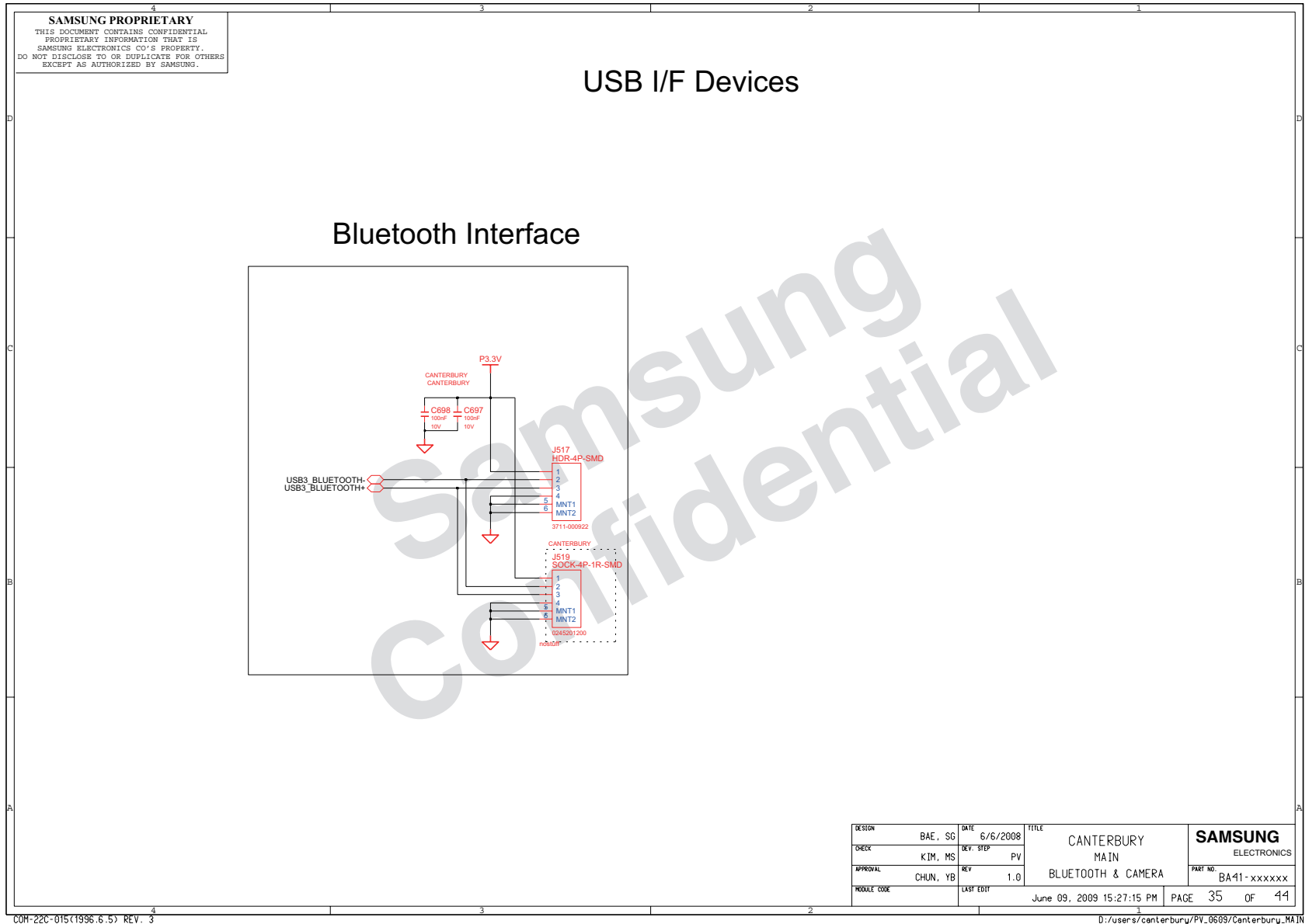
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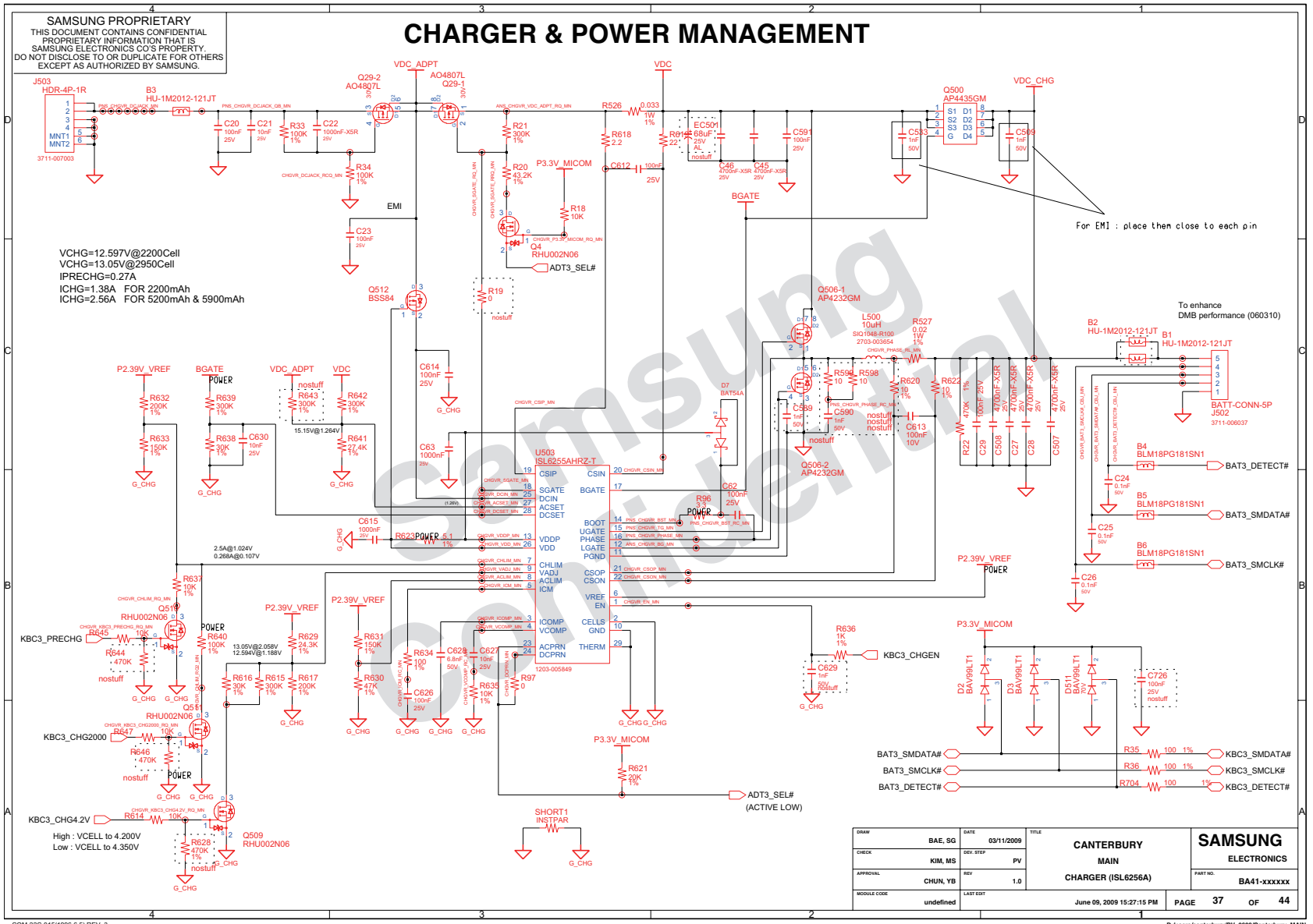
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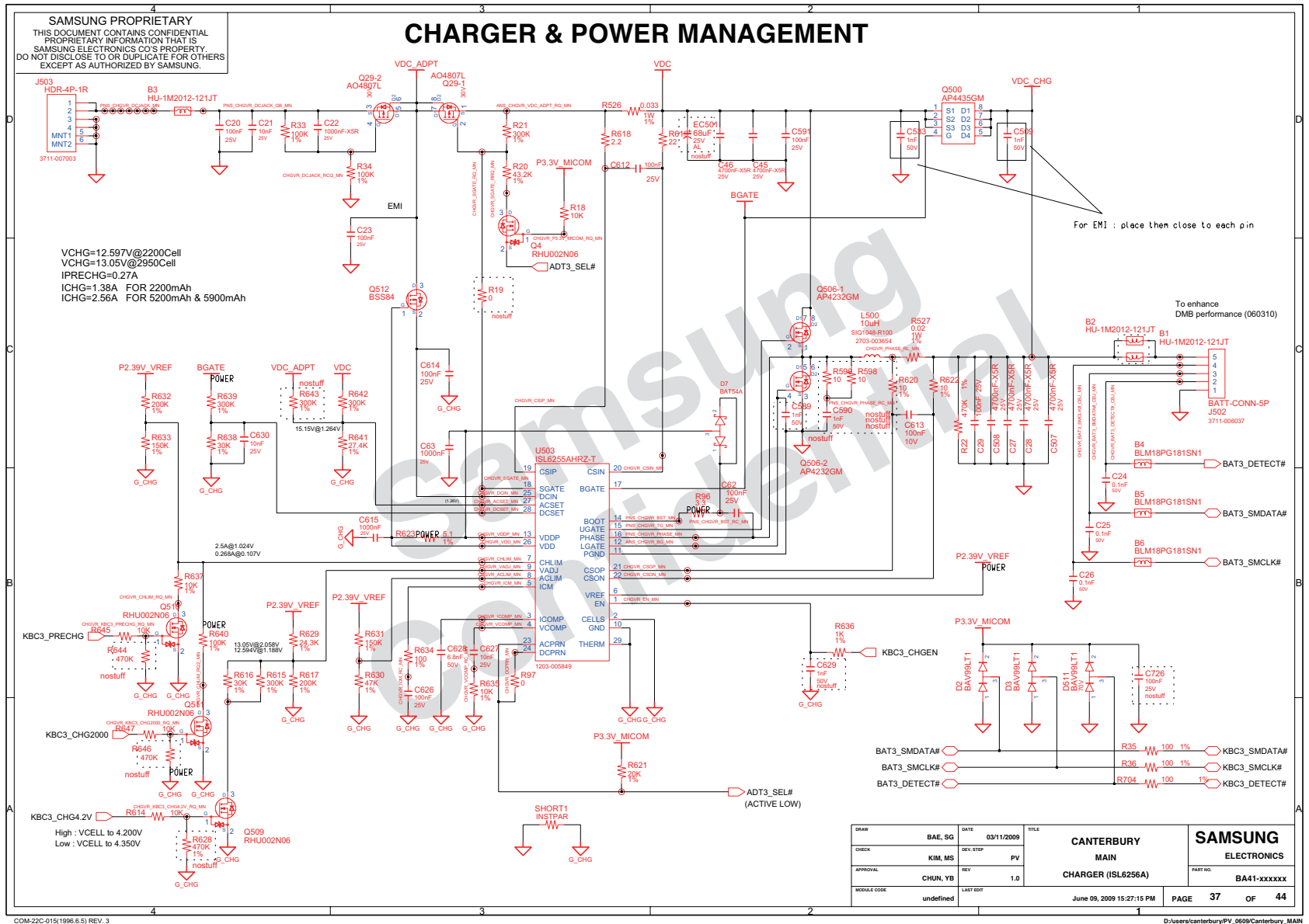
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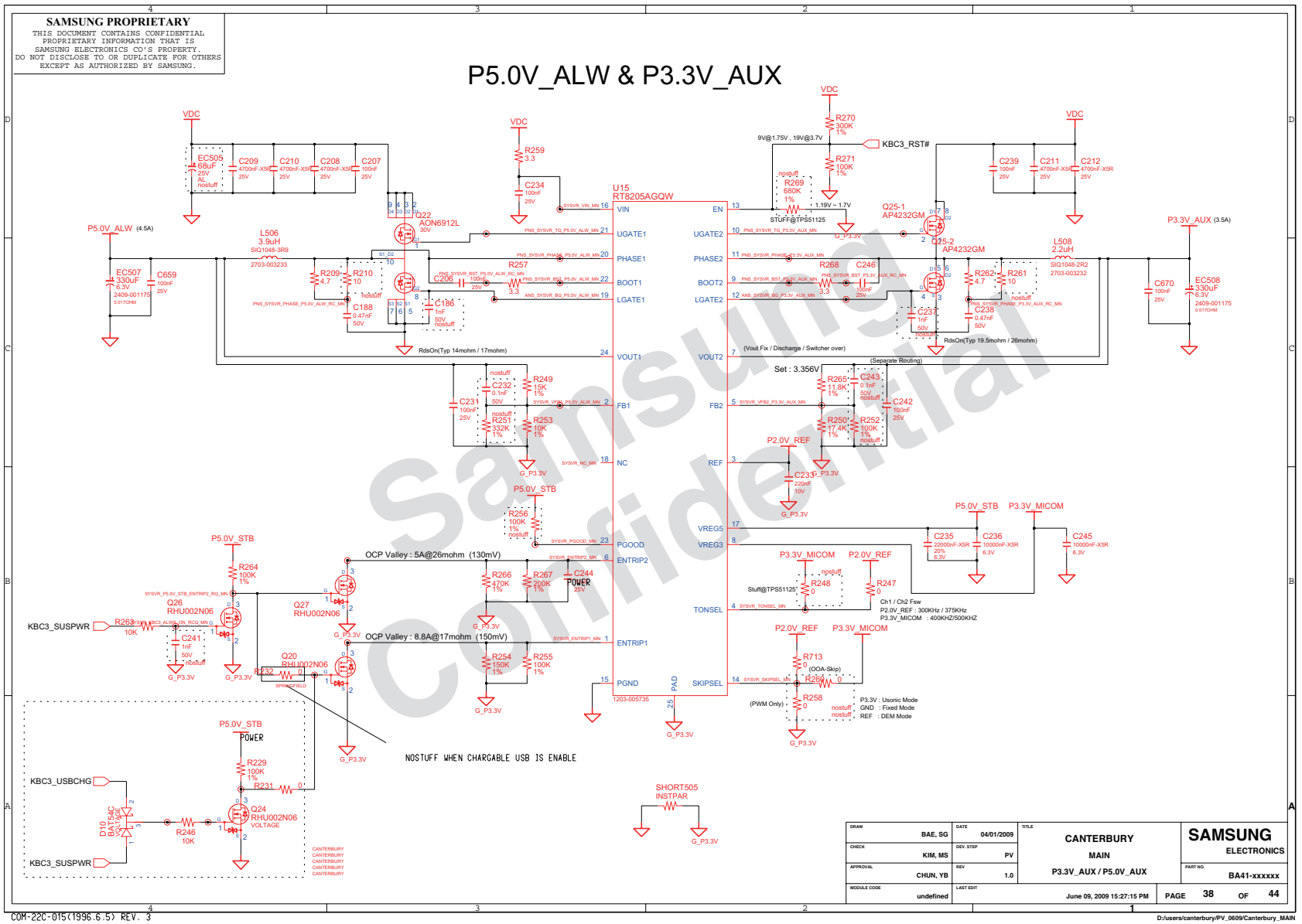
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8. Block Diagram and Schematic

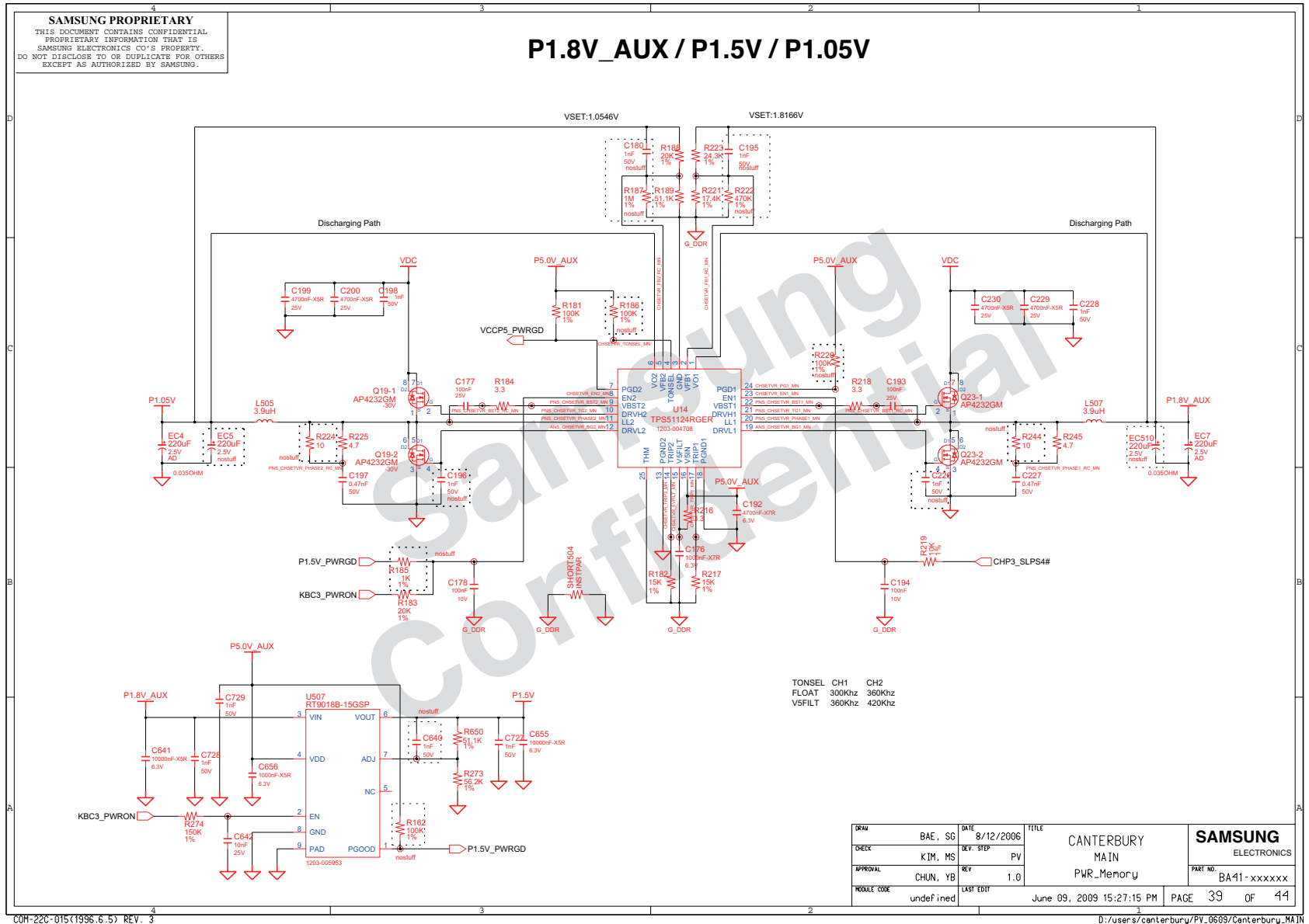


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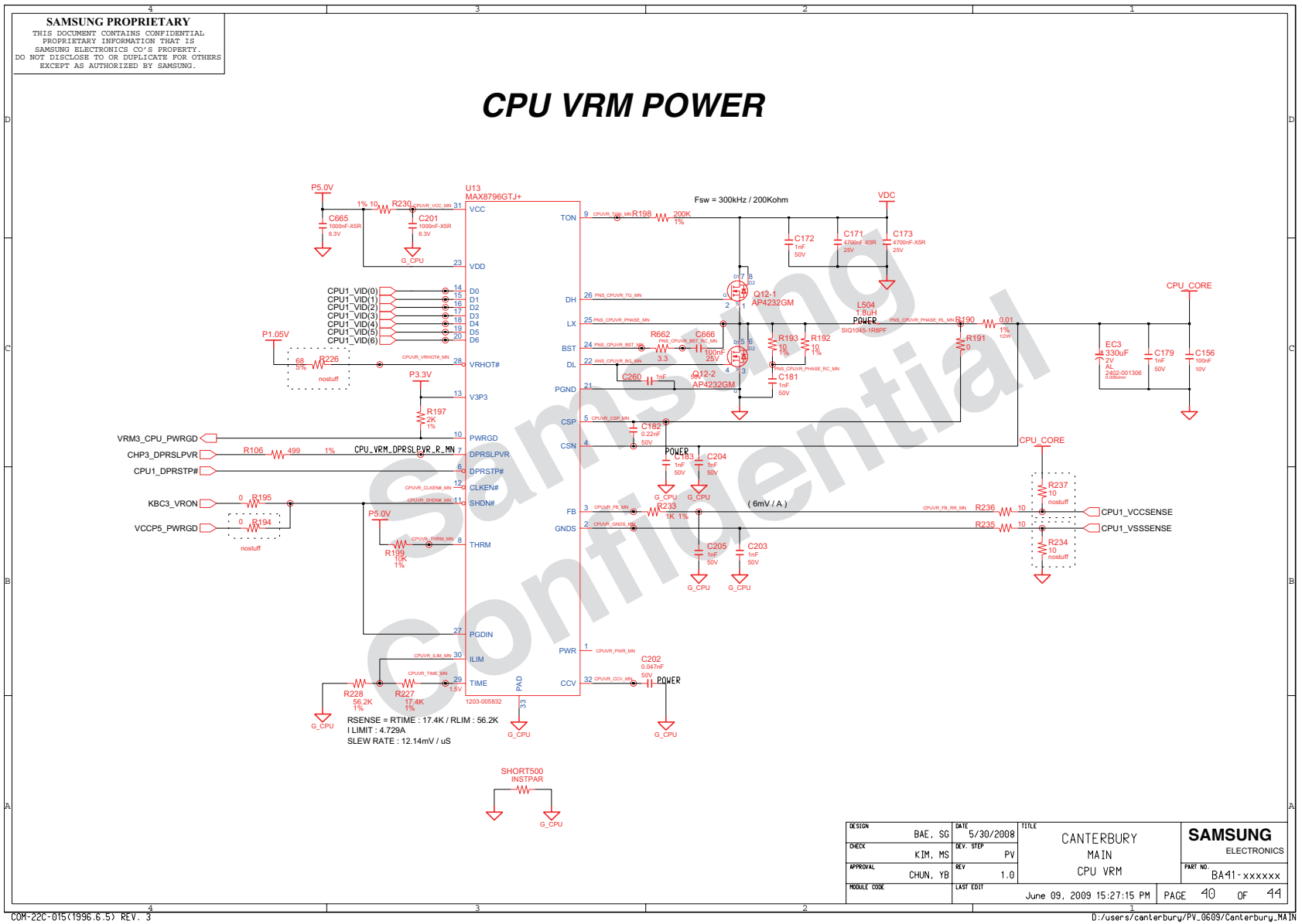


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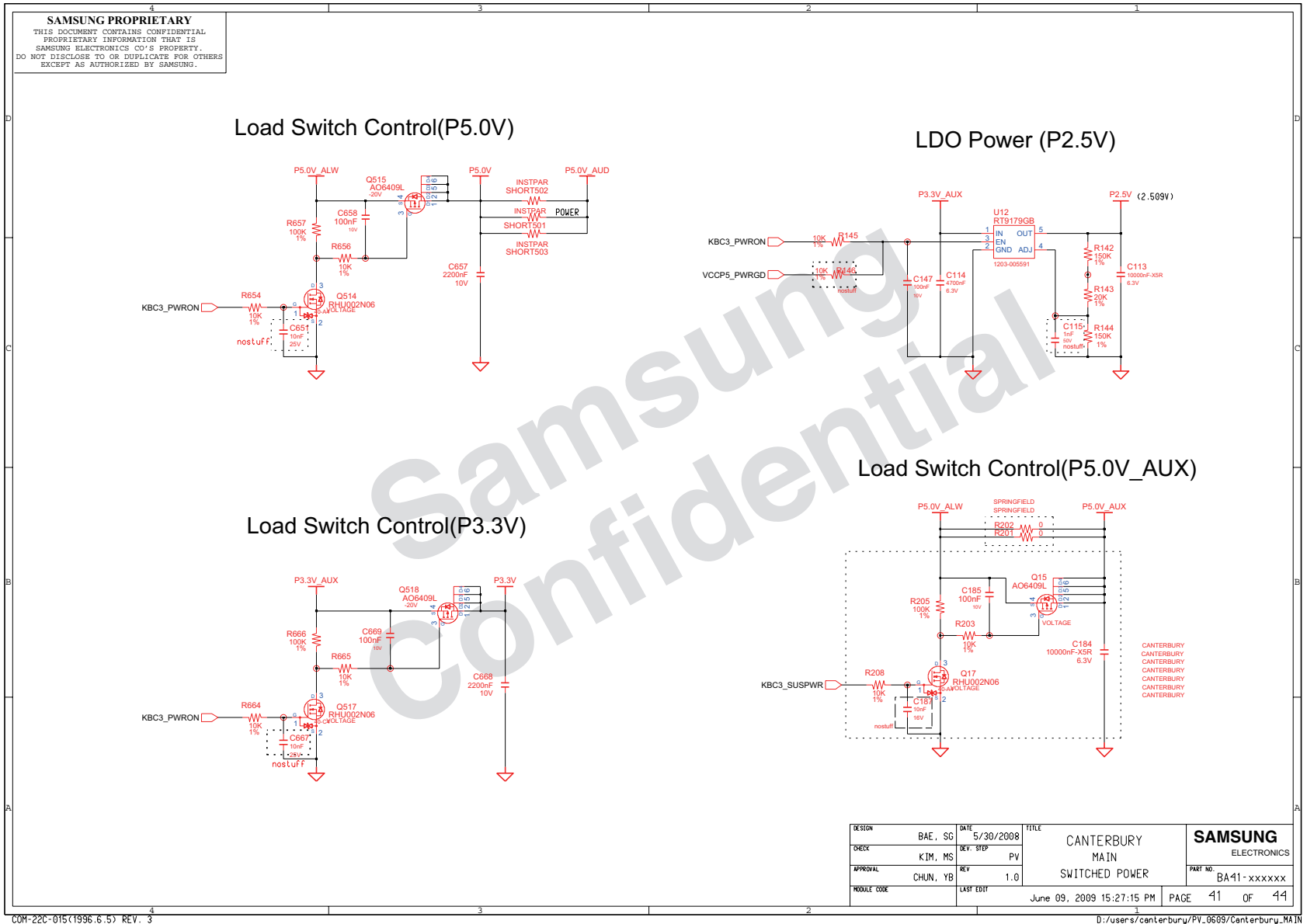
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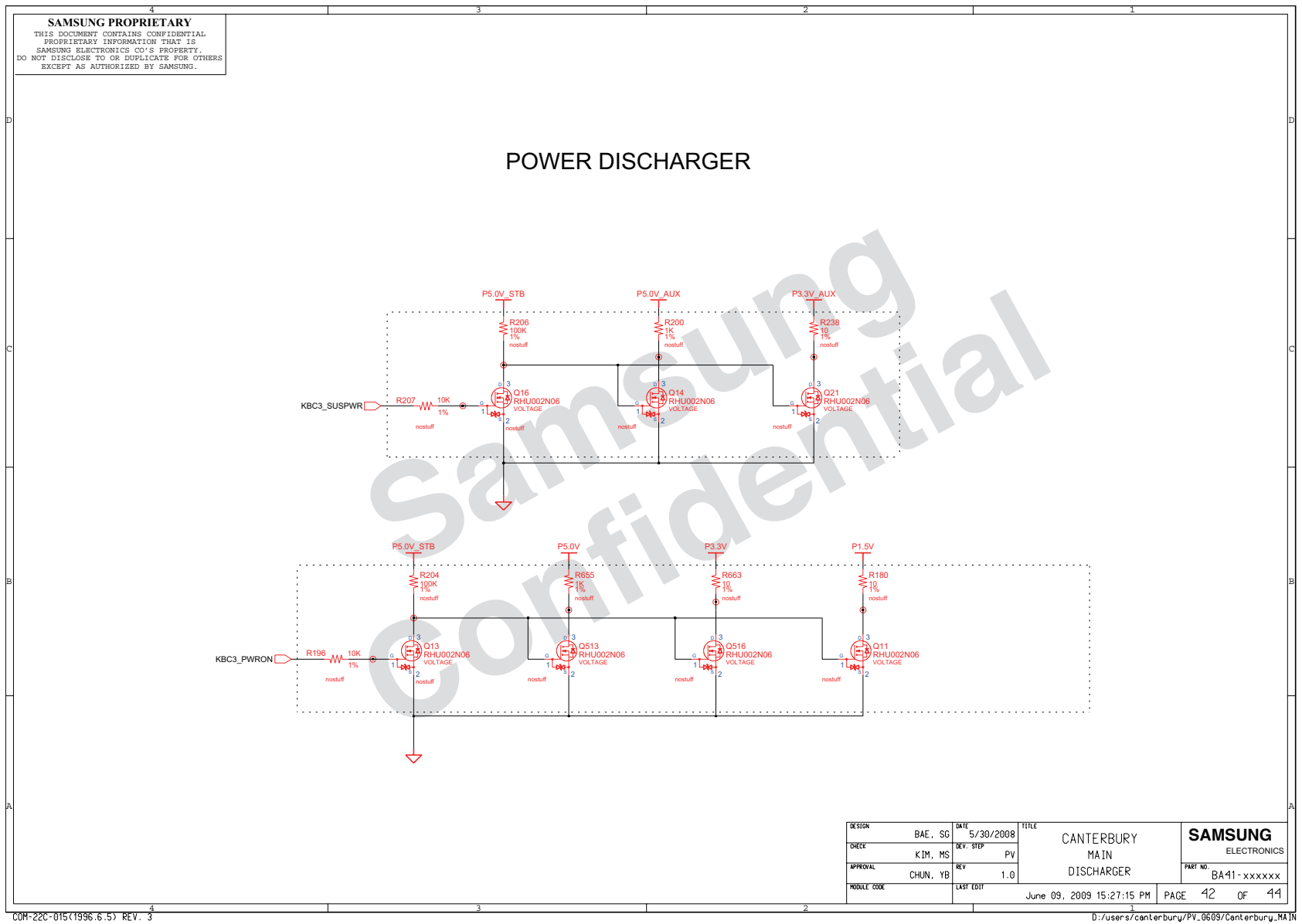
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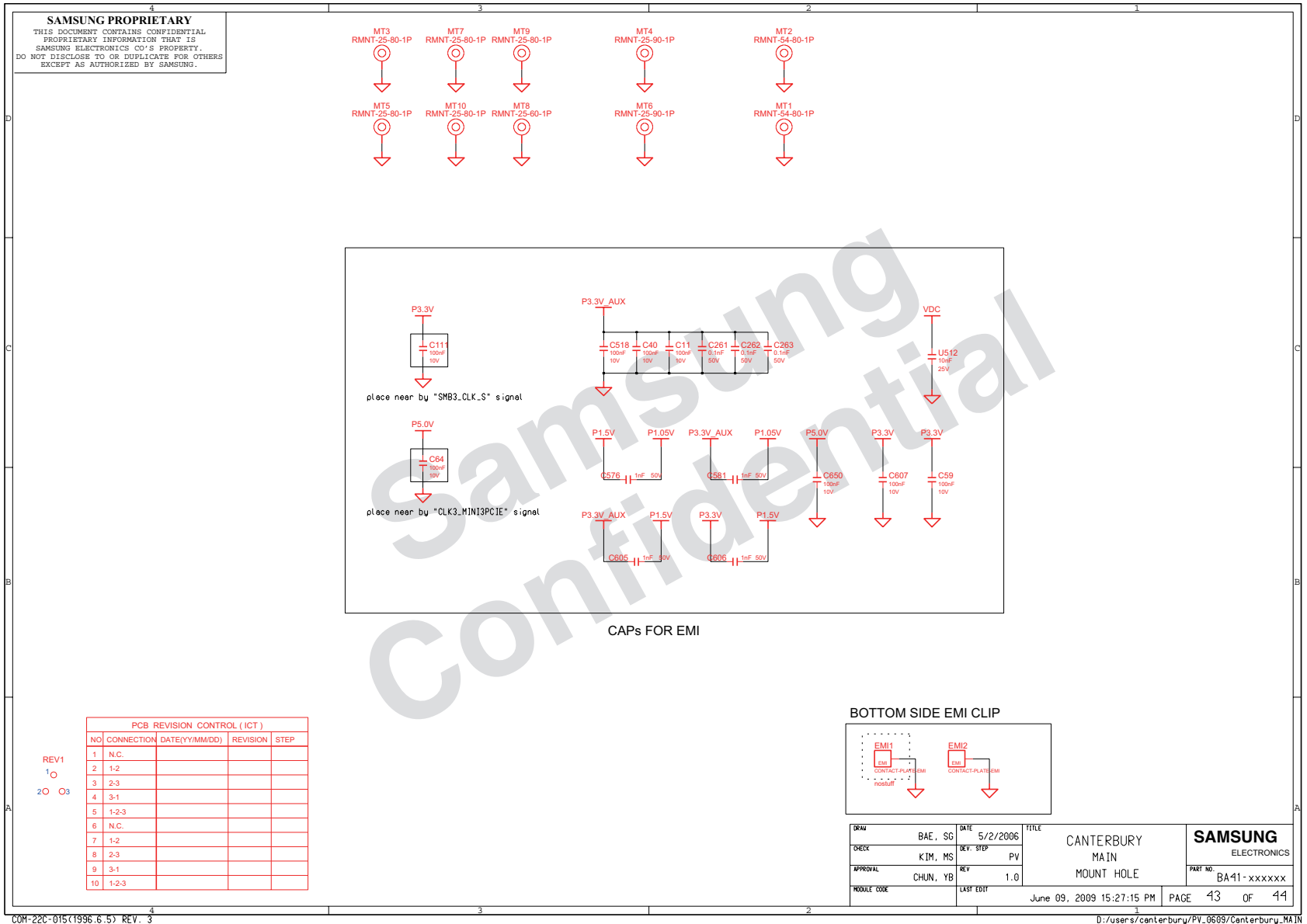
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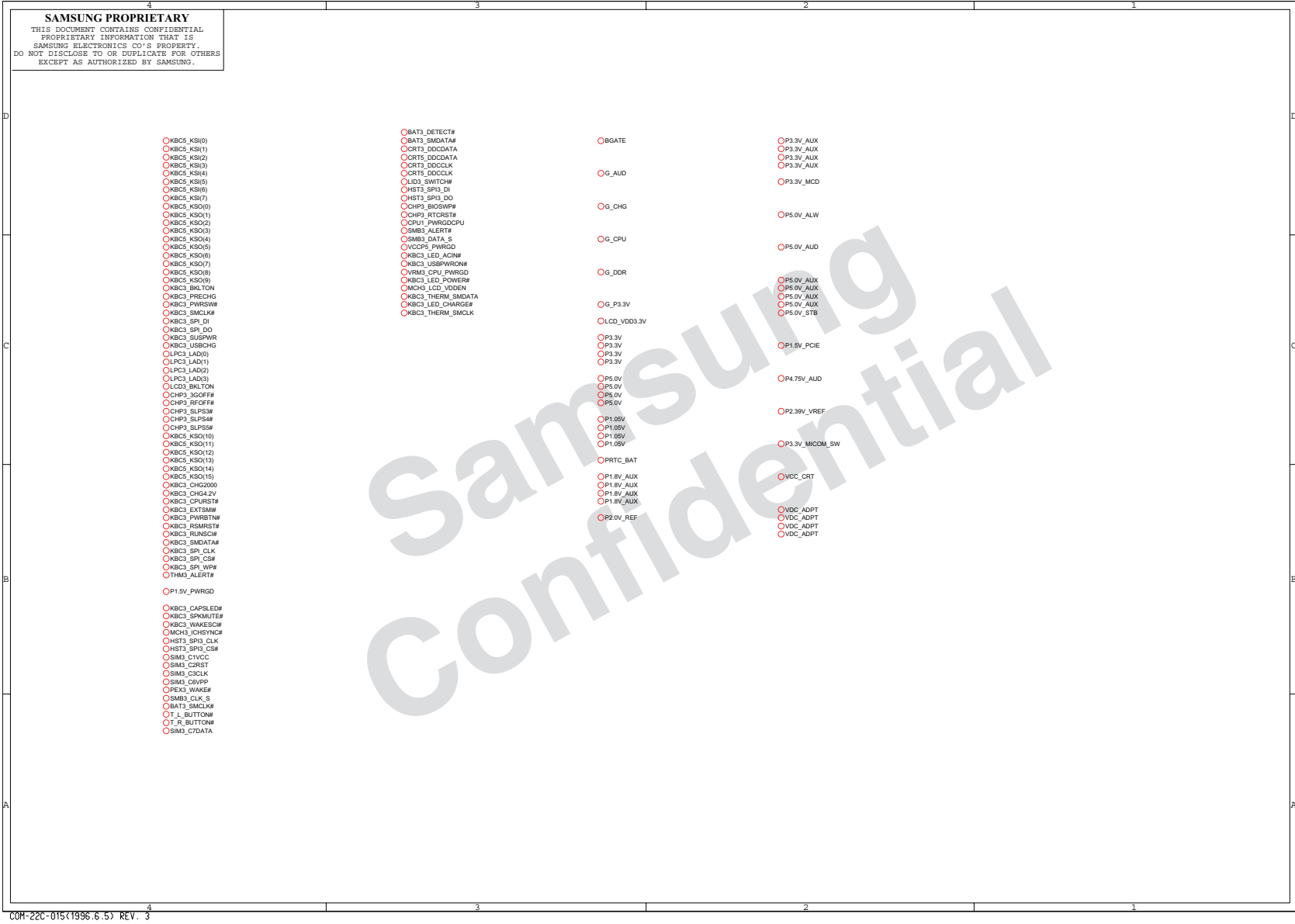
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