

Troubleshooting Manual

W995



ABOUT

General information

The purpose of this document is to provide enhanced technical information for Sony Ericsson repair technicians in order to assist during service, repair and troubleshooting operations on Sony Ericsson mobile phones. It should be used as a complement to other repair instructions and tools as notified by the local Sony Ericsson representative.

To search for components throughout the entire document use the “search” function in Adobe Acrobat Reader 7.0 (or later version) and enter the component name or other word. Use zoom to enlarge.

For easier navigation of the document you can use the bookmarks that appear in the Bookmarks tab on the left side of the Adobe Acrobat Reader window. Each bookmark jumps to a page in the document.

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Note

When disassembling and reassembling the phone the instructions and processes described in the Mechanical Working Instructions, the Generic Repair Manual and the Repair Center Handbook must be followed.

Revision History

Rev.	Date	Changes / Comments
1	06/24/2009	Initial revision.

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W995 Equipment List



Info: Additional information about the equipment used for TRS can be found in the following location: *CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf or matrix.xls – W Model Tab.*

Troubleshooting Fixture

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: 1222-7302

Note! Additional information about the TRS Fixture Kit can be found in the Trouble Shooting Fixtures Setup Instructions document which is included in this TRS Manual.

Dummy Battery

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: 1208-5627

Note! The resistance between GND and BDATA should be approximately 27K Ohm.

Instruments

Power Supply Channel 1 (VBATT)

Agilent 6632B or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Instrument Settings:
Voltage: **3.8 Volt**
Limiter: **2.0 A**

Note! Maximal cable length between the Power Supply Channel 1 VBATT and the dummy battery must be maximum 1m. The cable must have a capacity for at least 16A.

Power Supply Channel 2 (DCIO/SEPI)

Agilent 6632B or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Instrument Settings:
Voltage: **5.0 Volt**
Limiter: **2.0 A**

Oscilloscope

Agilent DSO7052A or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Digital Multimeter (DMM)

Fluke 83 or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Note! The 0, 64 mm Test Probes is recommended by Sony Ericsson when the DMM is in use. See Picture 1.

Picture 1



Spectrum Analyzer

R&S FSL 9 kHz – 3 GHz or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

RF probe

HP 85024A or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Mobile Phone Tester

Yokogawa VC200 or similar
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

FM Signal Generator

R&S SMC100A or similar
Location: -

PC Package & PC Software

PC Package (Computer)

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Urquell Fault Trace SW with project file

Location: CSPN – Repair Instructions – Electrical – W995 – Trouble Shooting Application – Project
File: W995, W995a Project_R1A

Drivers

SEPI BOX Drivers
Location: <http://emma.extranet.sonyericsson.com> /– Drivers – DSS / SEPI / SEMUTS

SE Communication Interface SEPI BOX

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: LTN 214 1484
See Picture 2.

Picture 2



Cables

USB Computer Cable

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
See Picture 3.

Picture 3



DSU-60/USB Cable

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: KRY 101 1413

RF Test Cable Flexible

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: RPM 119 885
See Picture 4.

Picture 4



SEPI Interface Cable – A1

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: KRY 101 1119/1
See Picture 5.

Picture 5



Power Cable RED to Power Supply Channel 1 (VBATT)

Maximum Length: 1m
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Power Cable BLACK to Power Supply Channel 1 (VBATT)

Maximum Length: 1m
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Customized Power Supply Channel 2 Cable (DCIO/SEPI)

Customize the cable according to following instructions below:
(Step 1, Step 2, Step 3 and Step 4)

Step 1:

Take the CST-75 battery charger and cut off the charger according to Picture 6.

Picture 6



Note! The Cable length must be exact 1.3m.

Step 2:

Connect the CST-75 charger Red or White wire to the Plus Output and the Black wire to the Minus (GND) Output at backside of the Power Supply Channel 2 (DCIO/SEPI) according to Picture 7.

Picture 7



Step 3:

Cut off insulating material from inside of the charger plug according to Picture 8.

Picture 8



Step 4:

Connect DCIO Cable and SEPI Interface Cable – A1 according to Picture 9.

Picture 9



Picture 10



Note! This setup is wrong.

Connections Instructions for the Dummy Battery

This setup is correct when the Dummy Battery is in use.
See Pictures 11 and 12.

Picture 11



Picture 12



Test Cards

Local SIM

Any functional Local SIM Card
See Picture 13.

Picture 13



Test SIM GSM/UMTS

One Test SIM GSM/UMTS is needed to perform Current Consumption Test, see Picture 14.
Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Note! To buy a Test SIM GSM/UMTS, please contact your supplier of test equipment.

Picture 14



Sony Memory Stick M2

Any functional Memory Stick Micro M2 Card
See Picture 15.

Picture 15



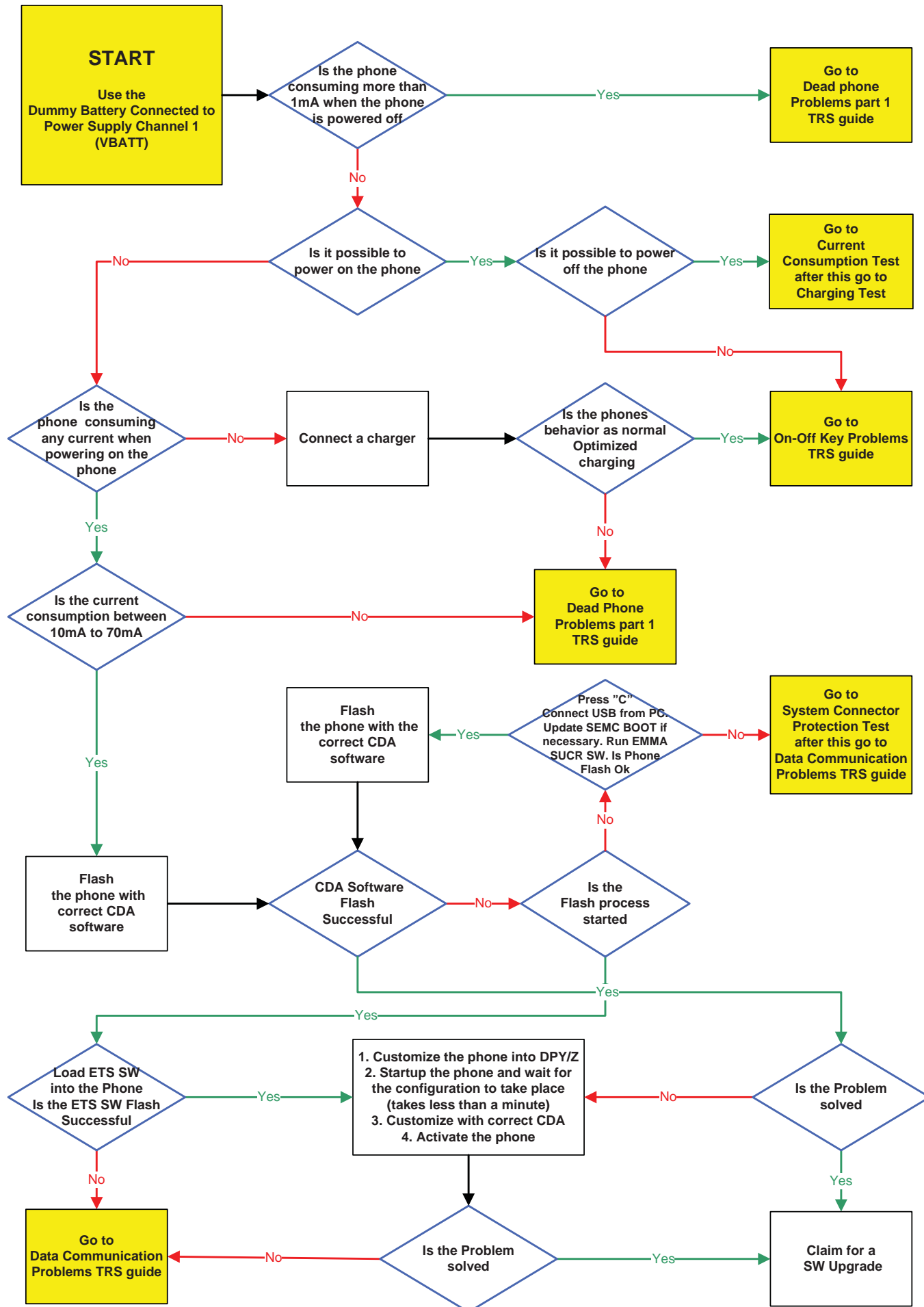
SMK RF Probe

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf
Part number: SXA 109 6356
See Picture 16.

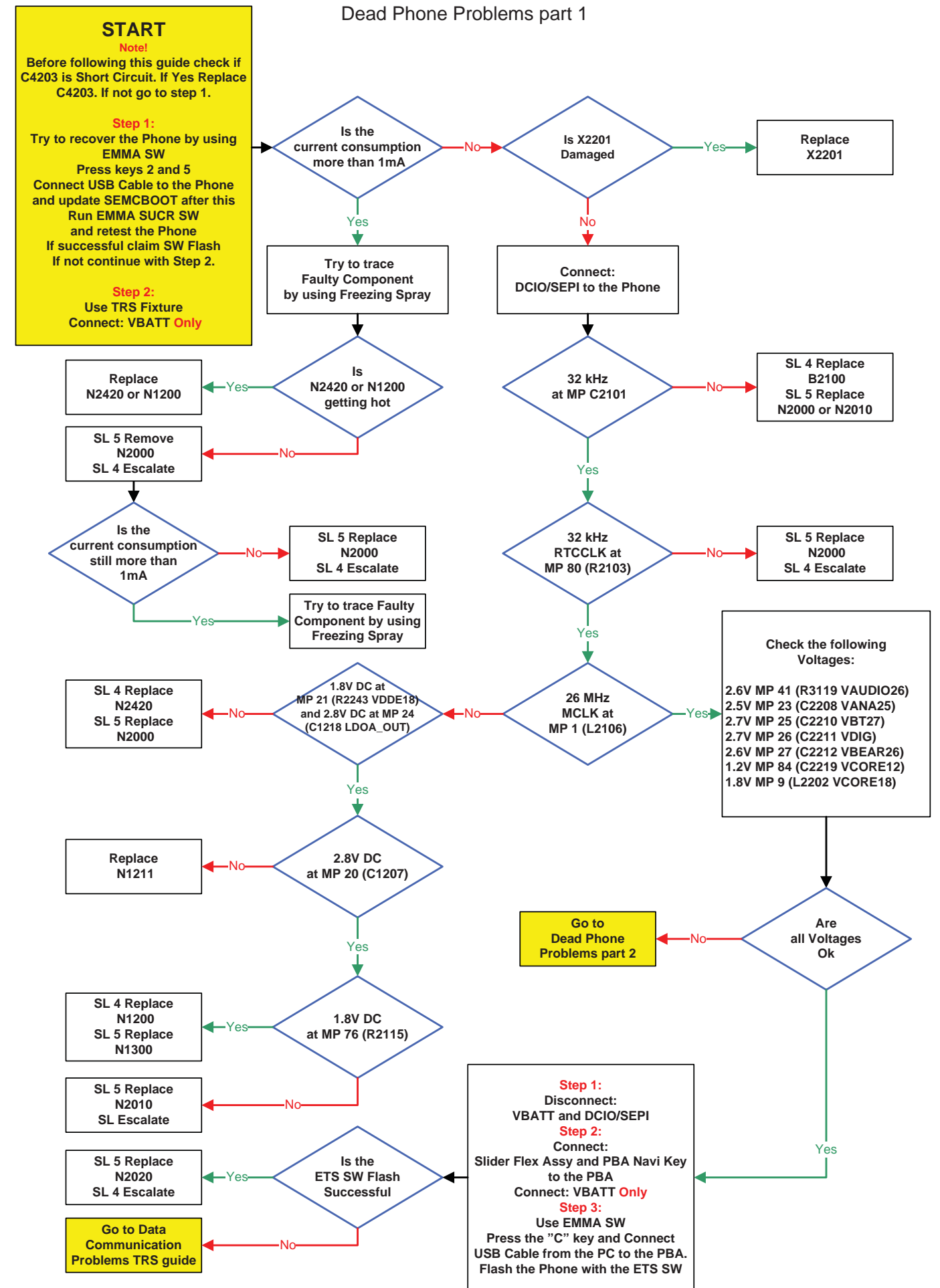
Picture 16



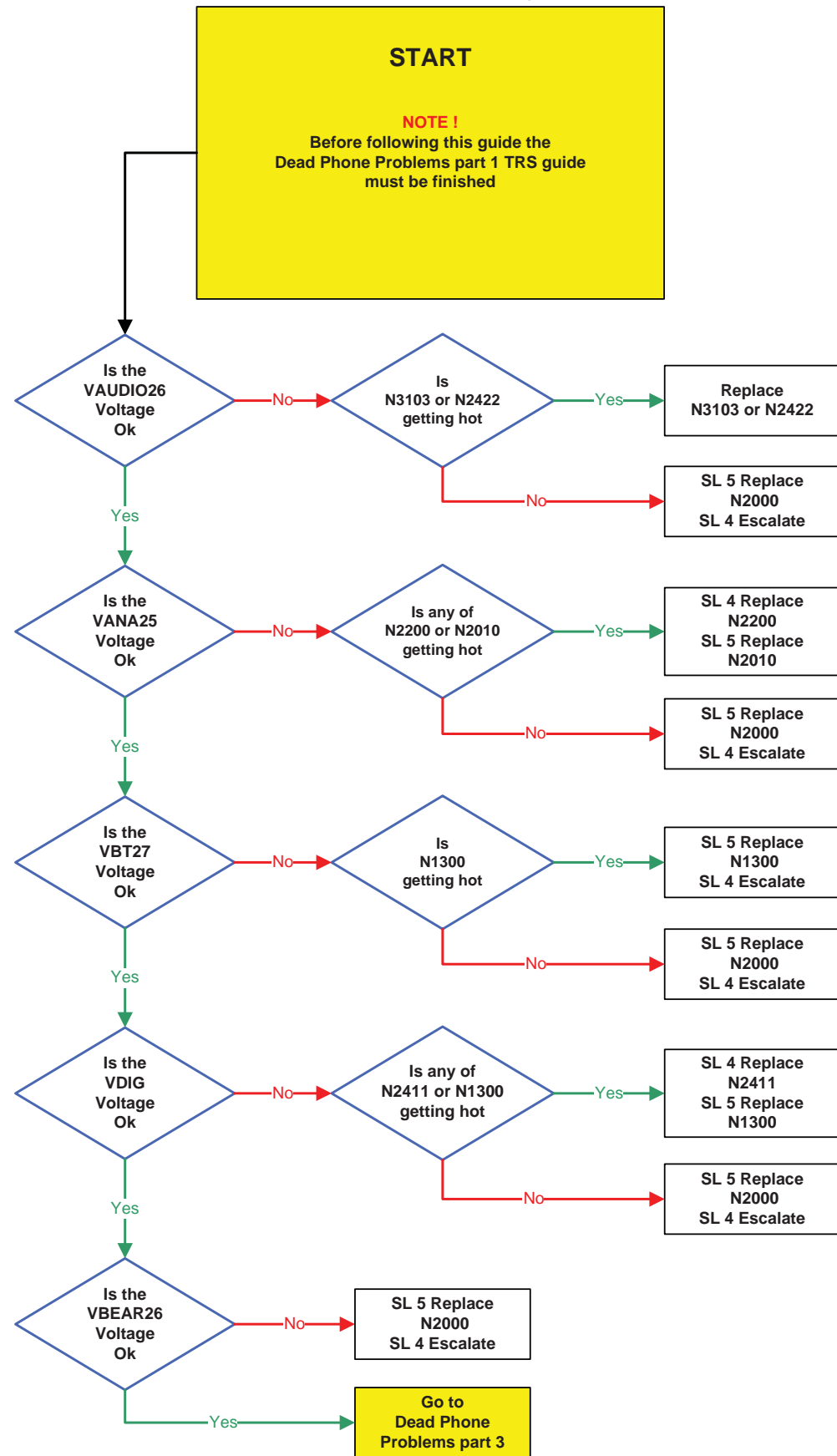
Power On/Off Problems



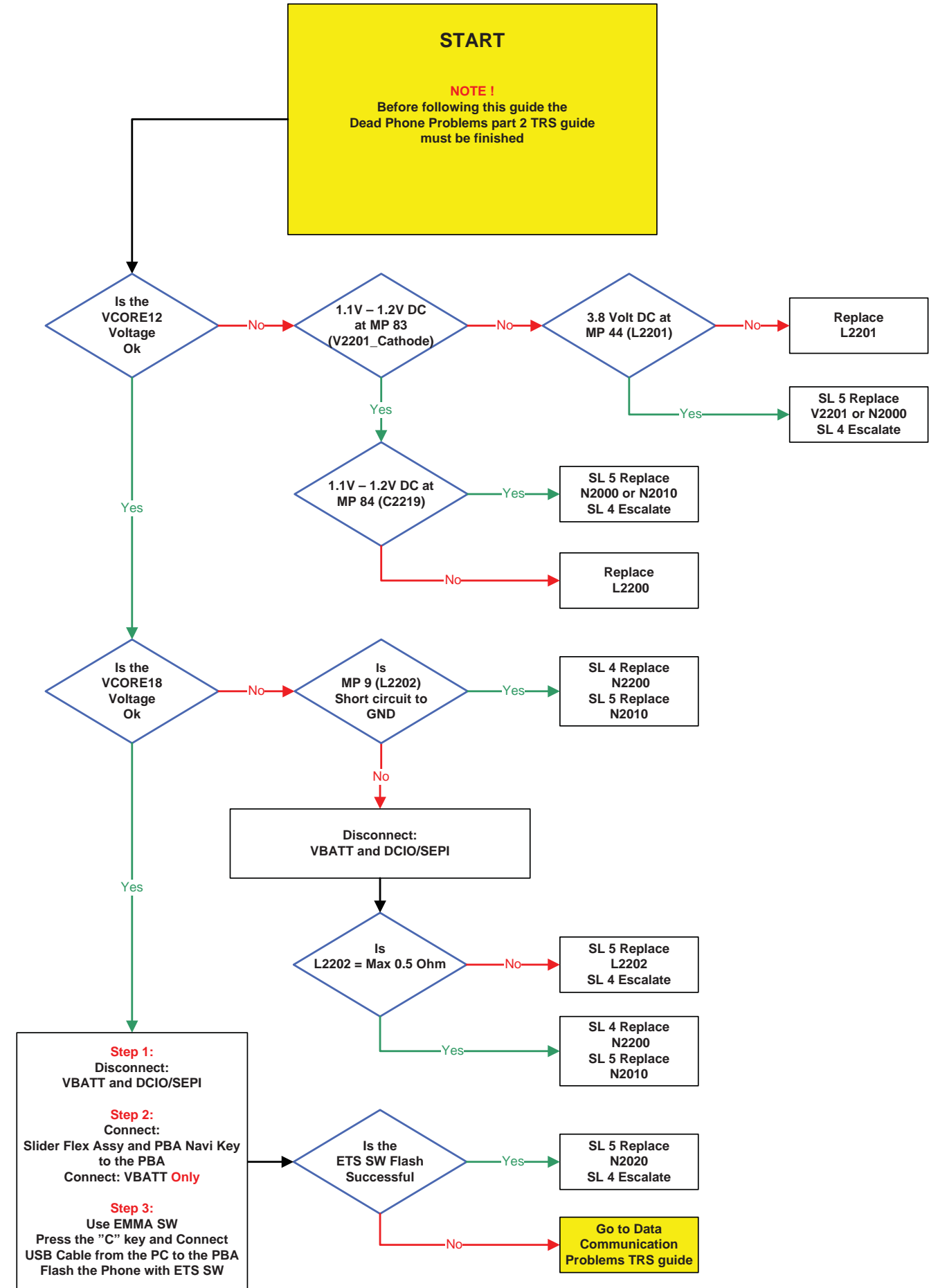
Dead Phone Problems part 1



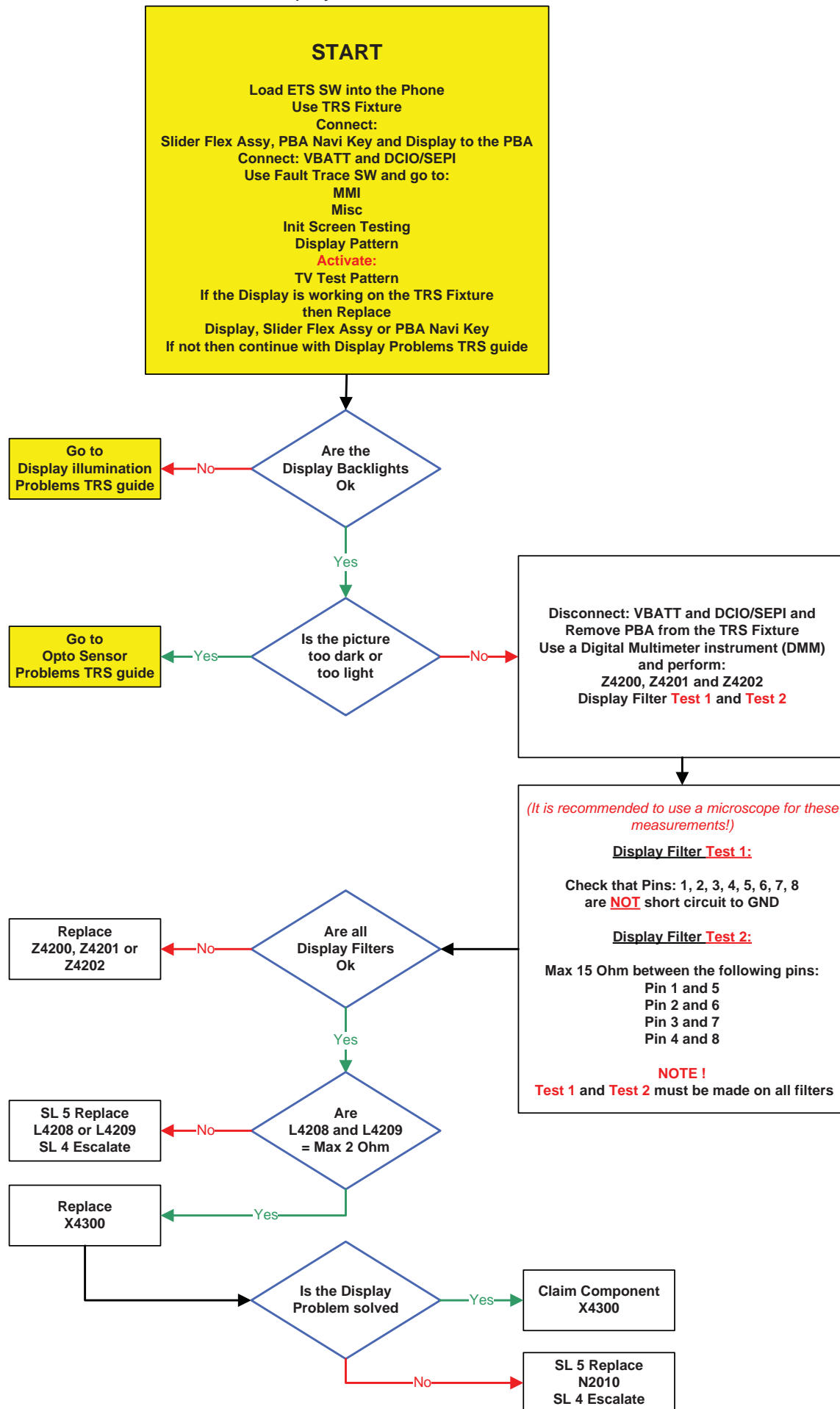
Dead Phone Problems part 2



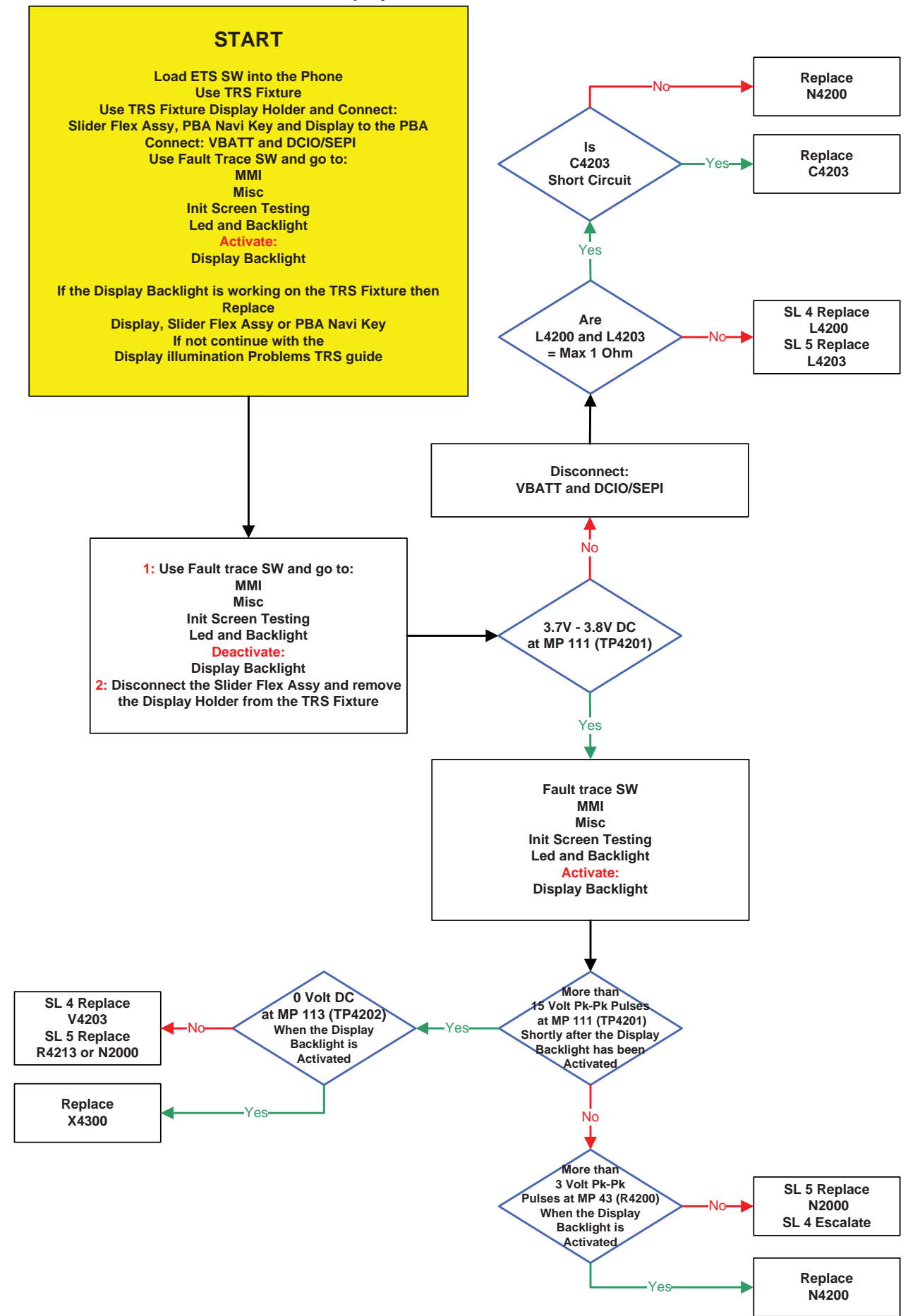
Dead Phone Problems part 3



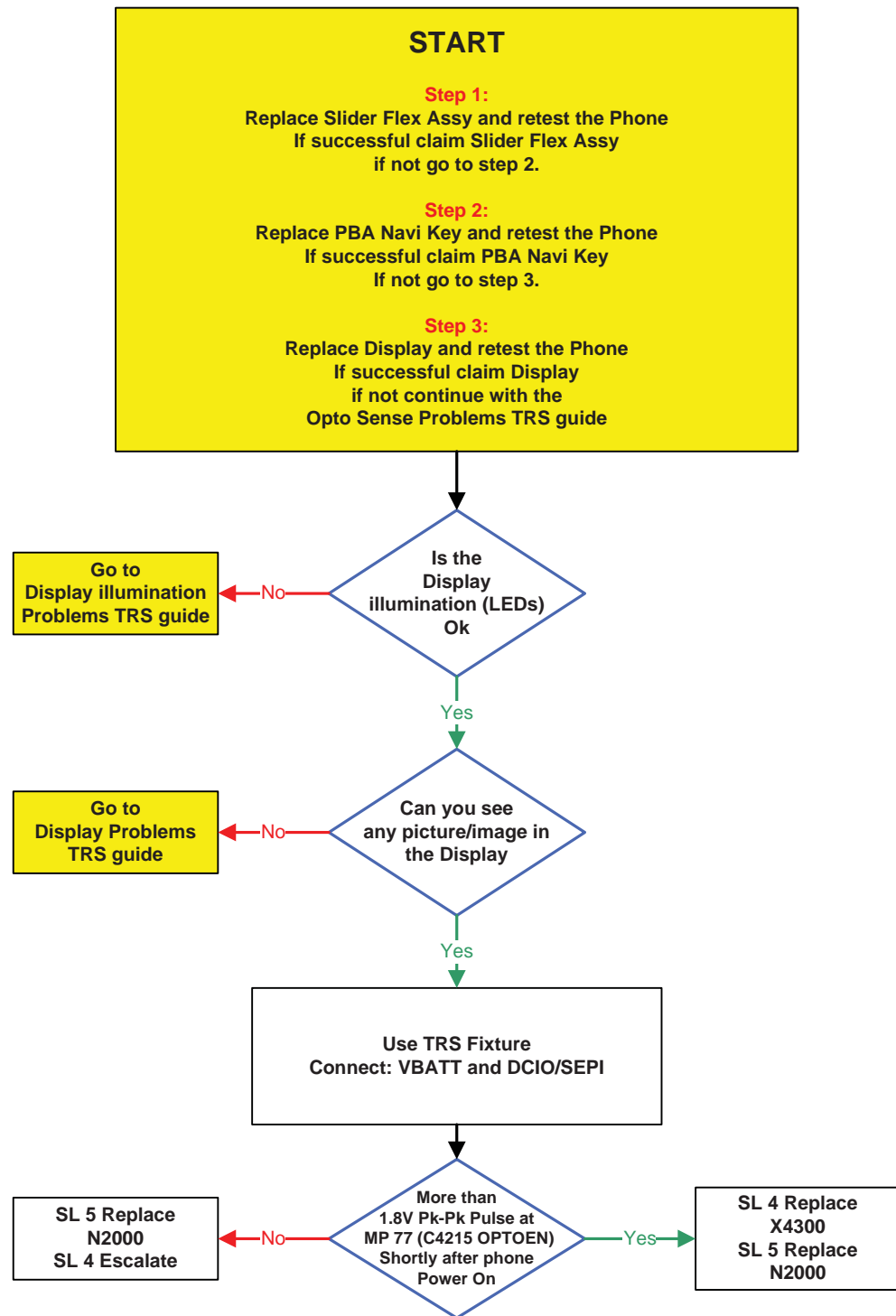
Display Problems



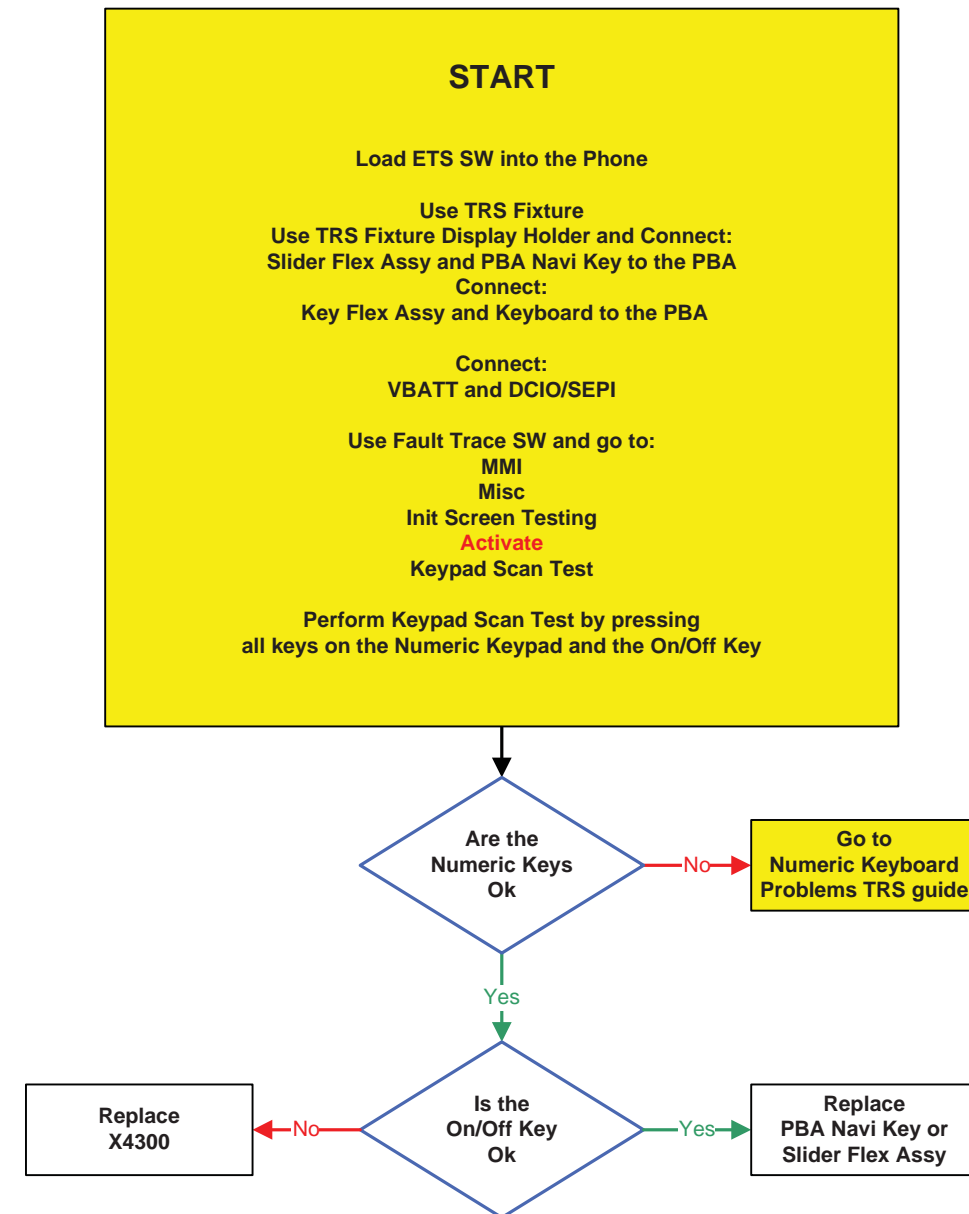
Display Illumination Problems



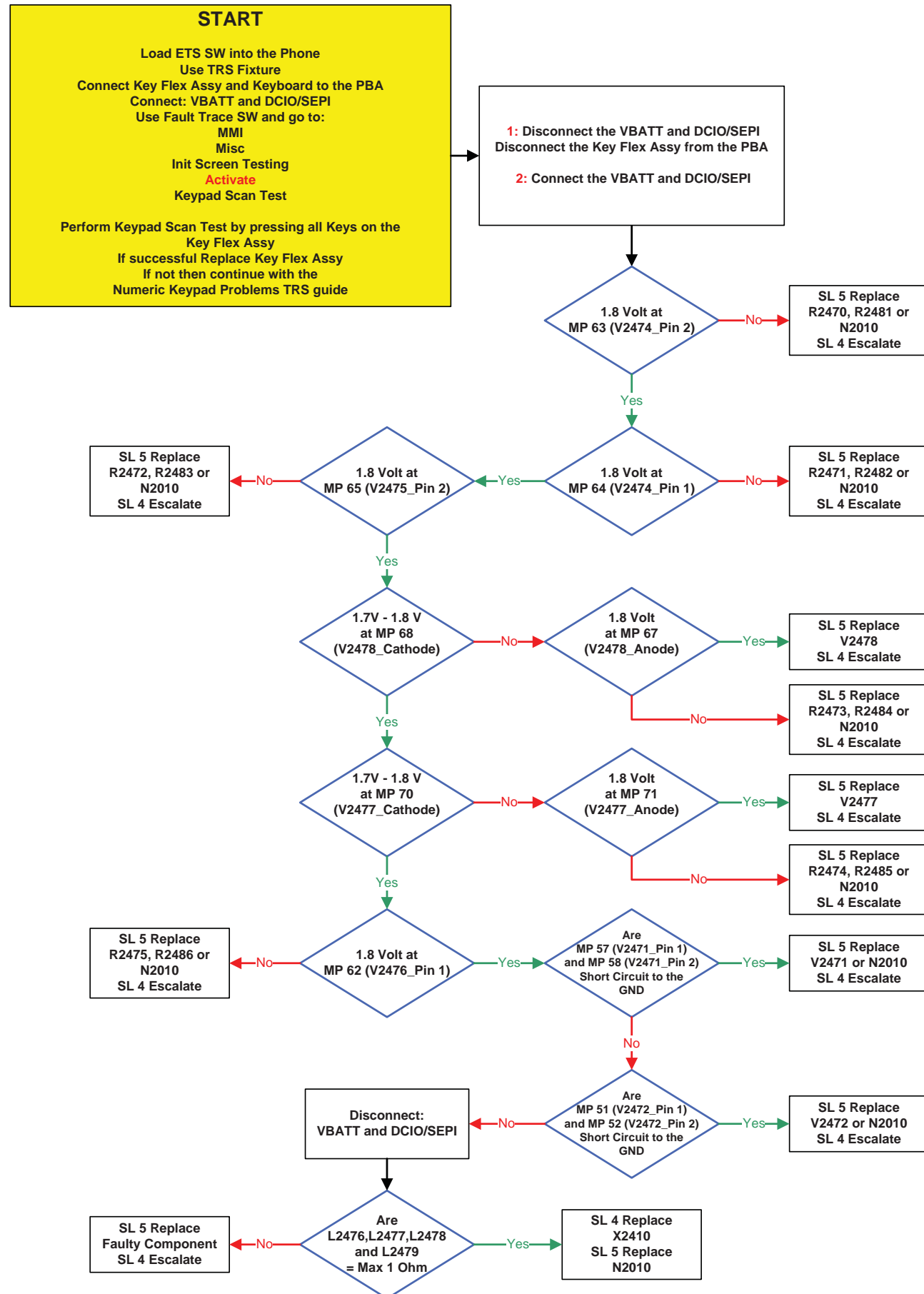
Opto Sensor Problems



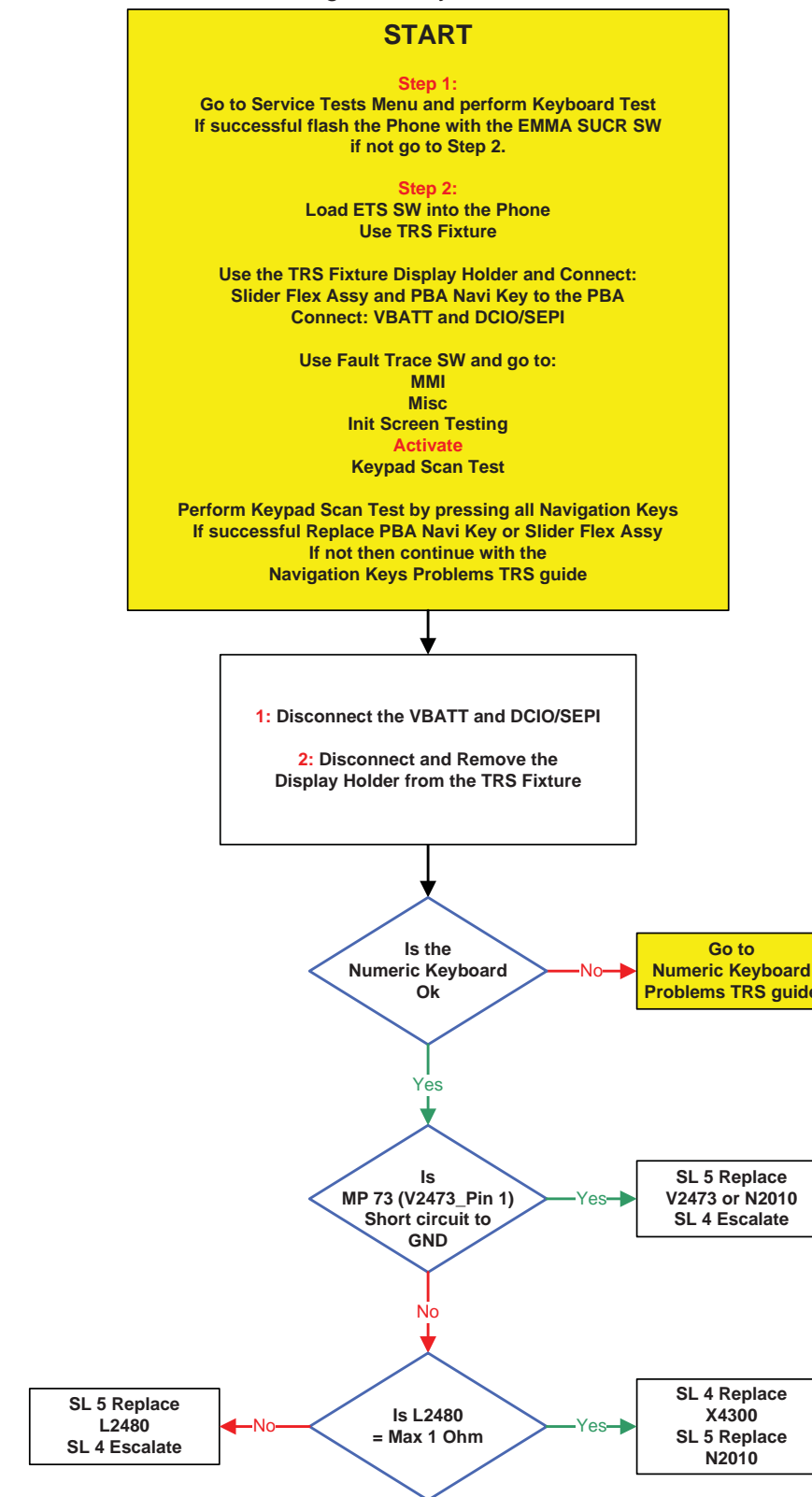
On/Off Key Problems



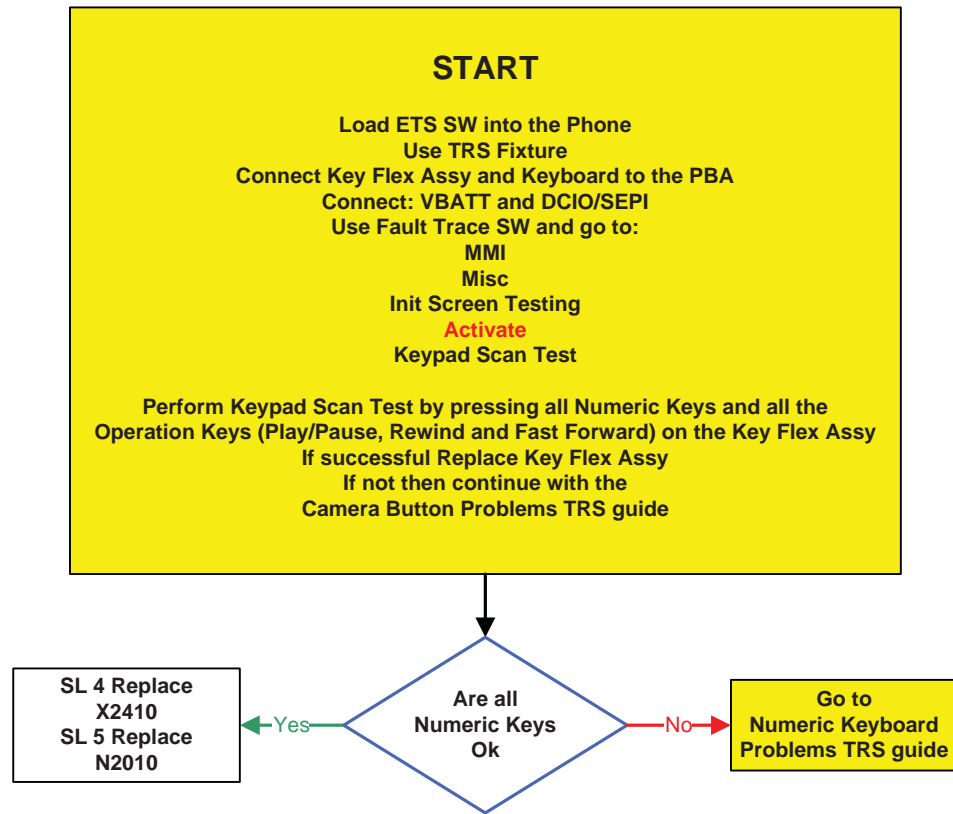
Numeric Keyboard Problems



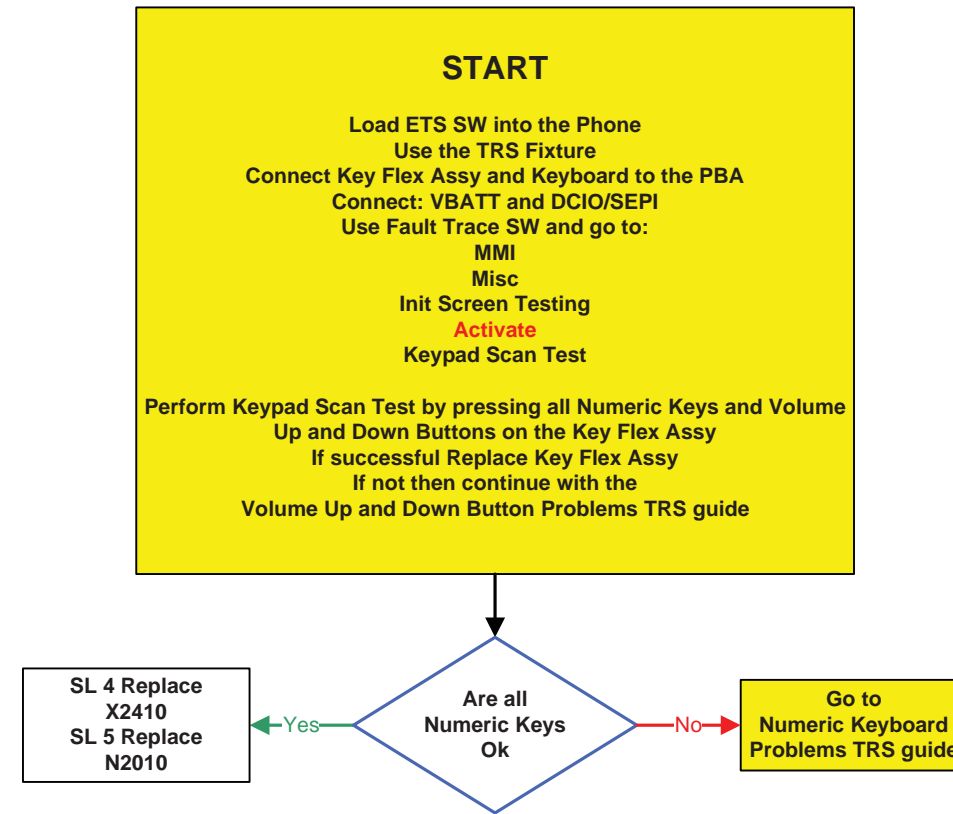
Navigation Keys Problems



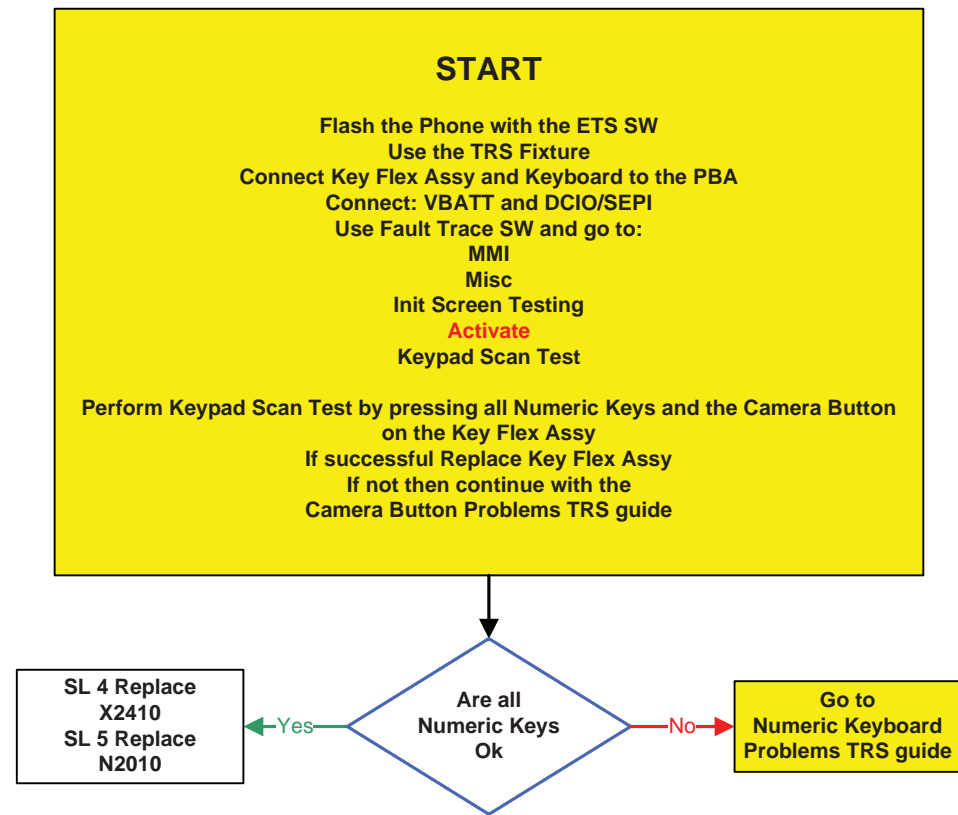
Operation Keys Problems



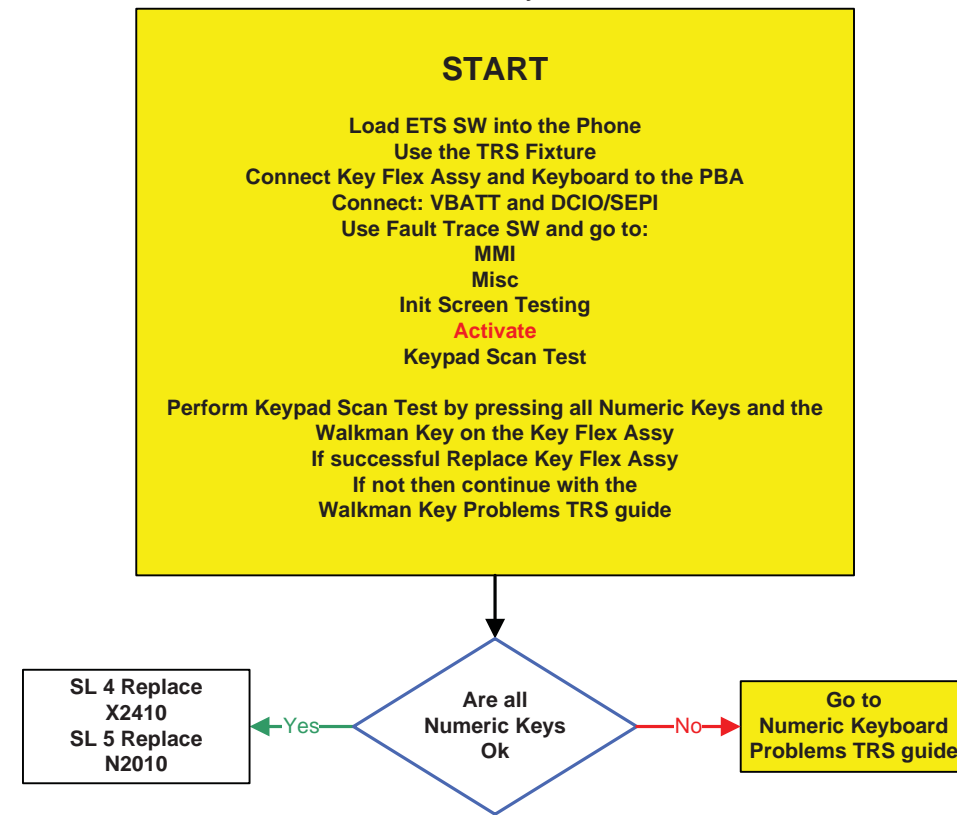
Volume Up and Down Button Problems



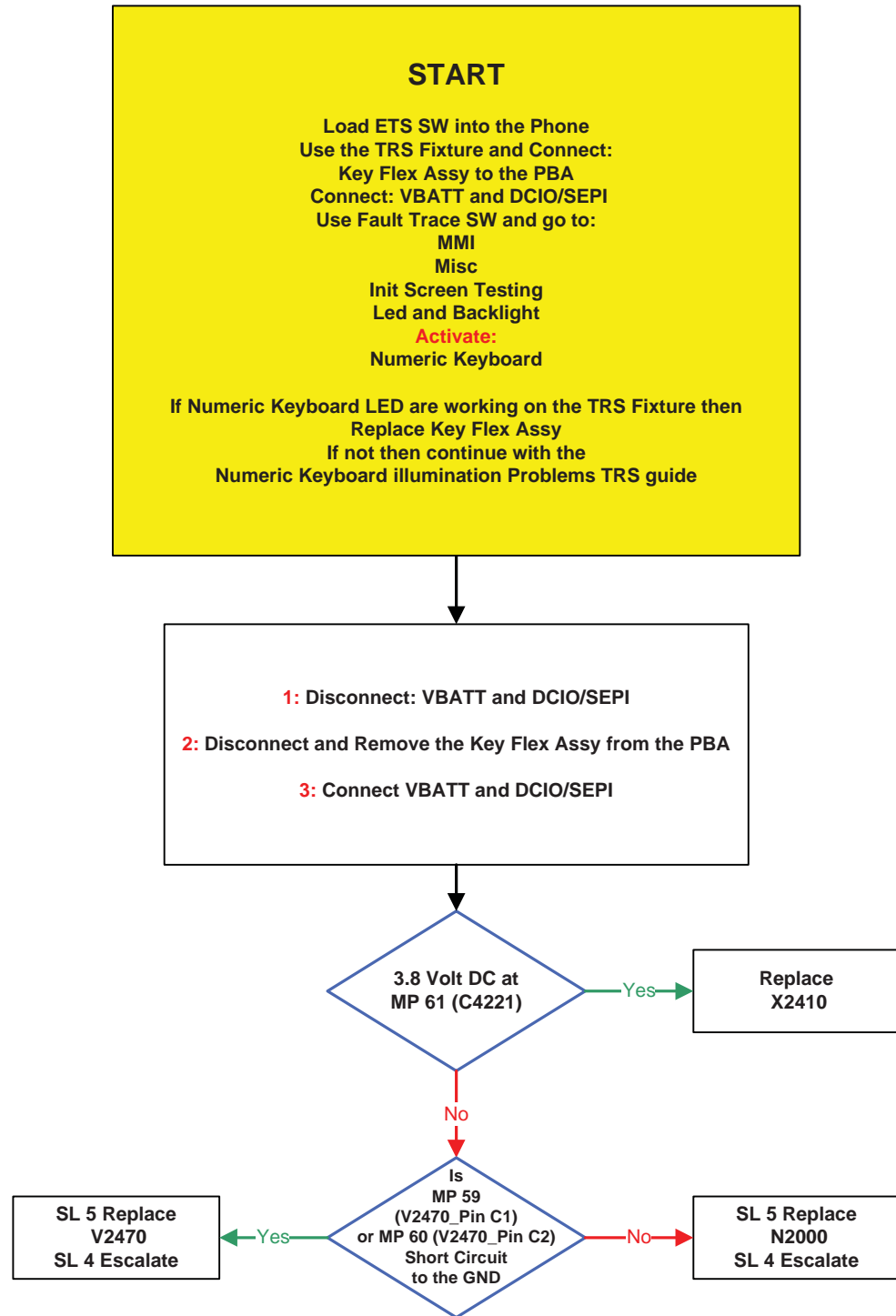
Camera Button Problems



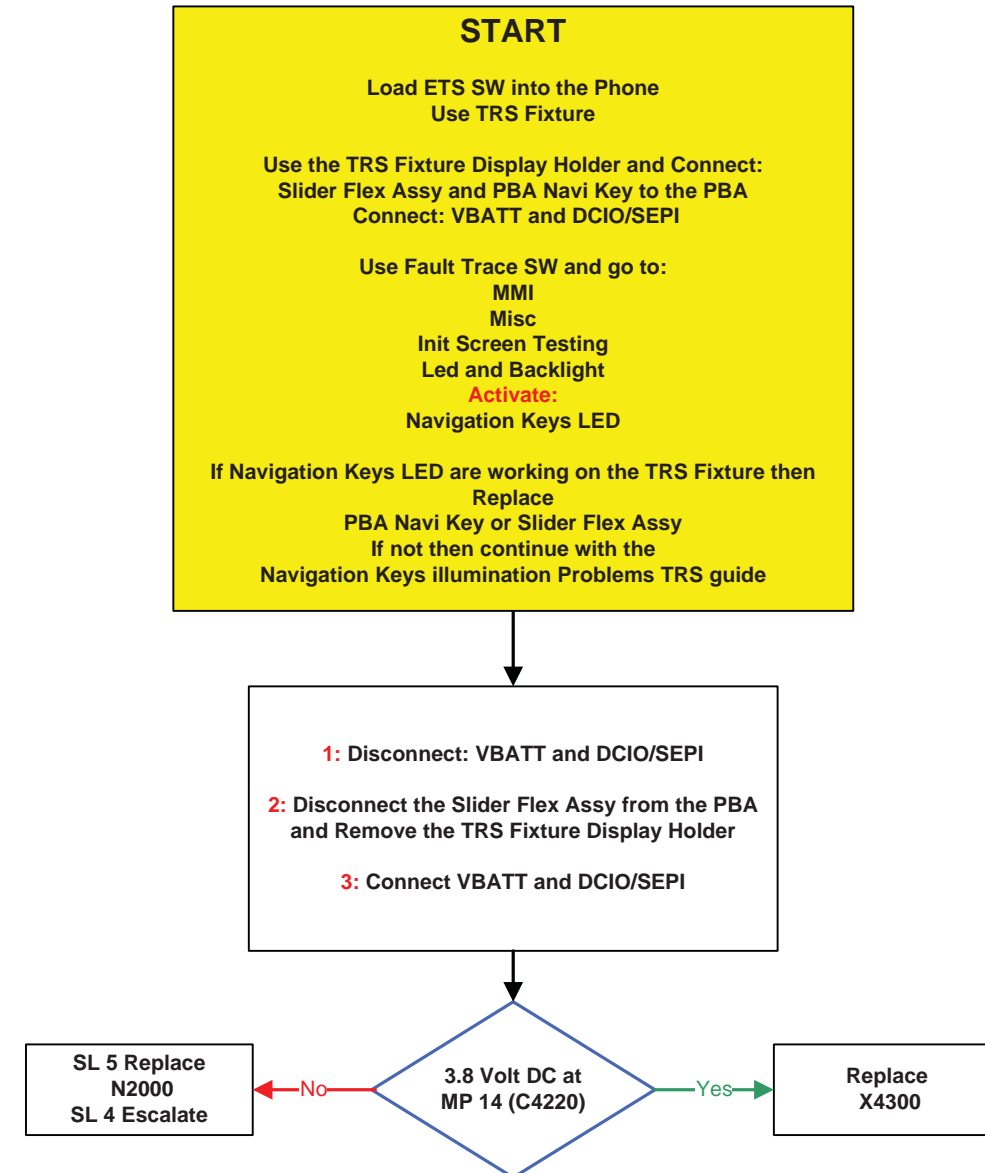
Walkman Key Problems



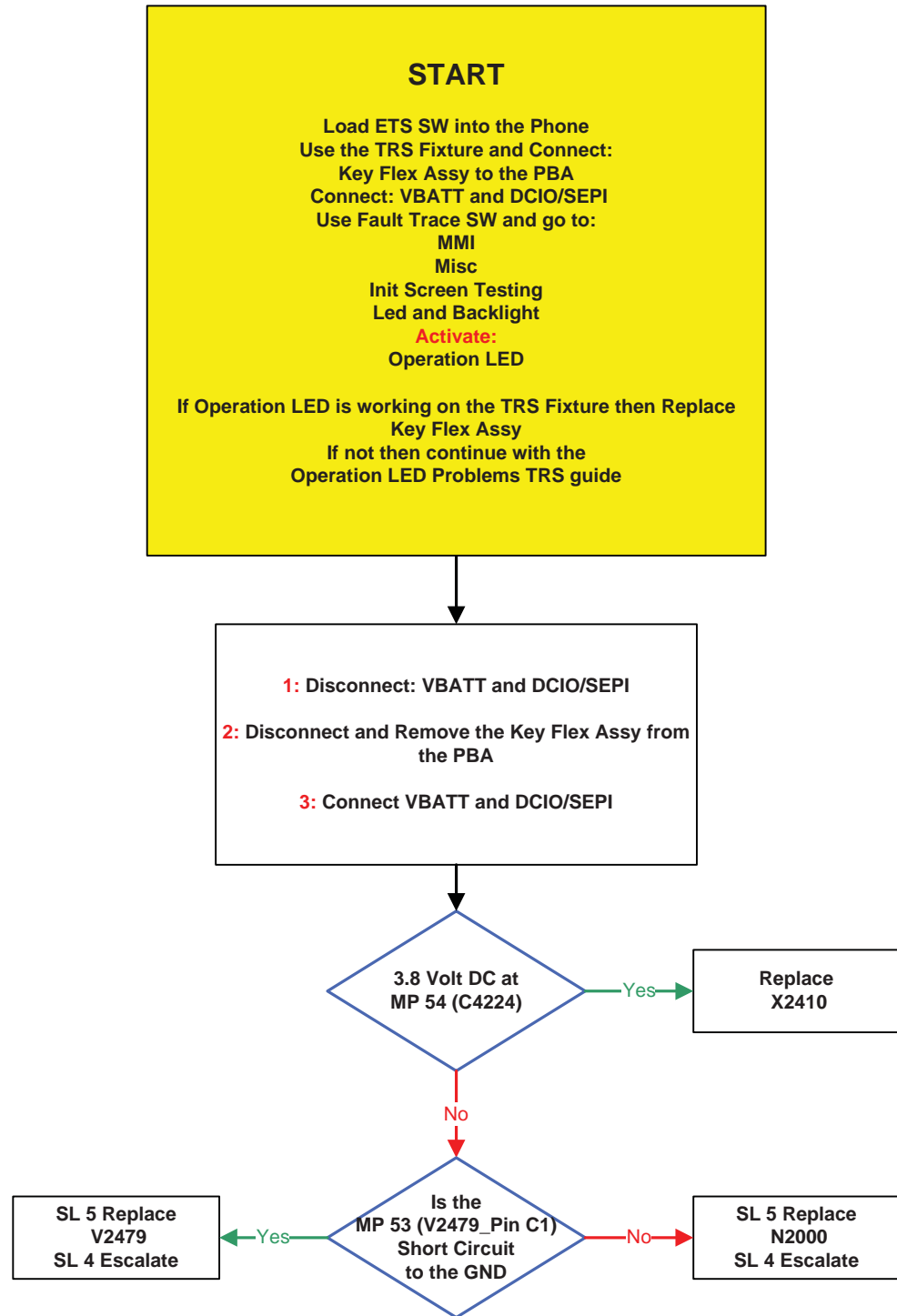
Numeric Keyboard illumination Problems



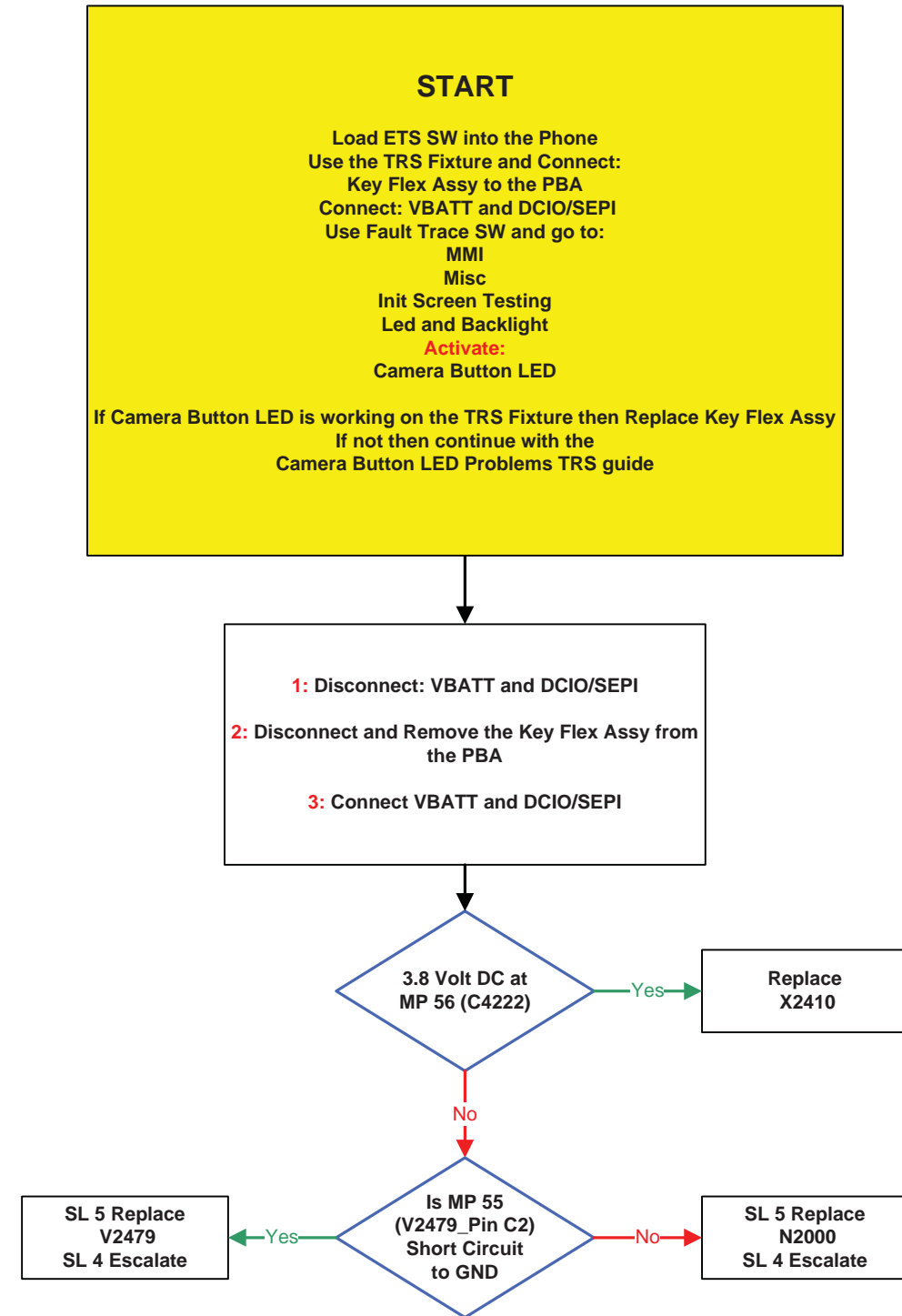
Navigation Keys illumination Problems



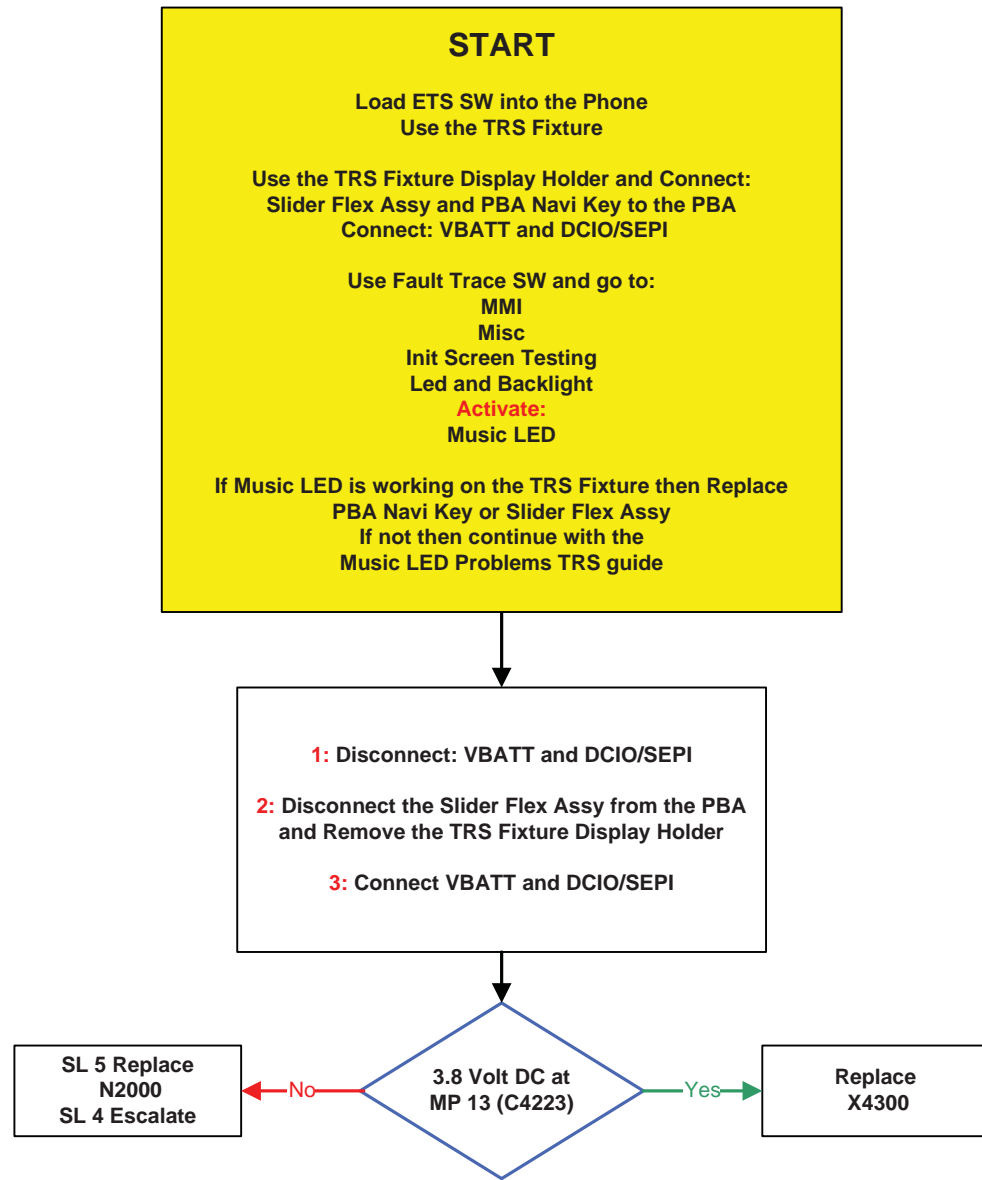
Operation LED Problems



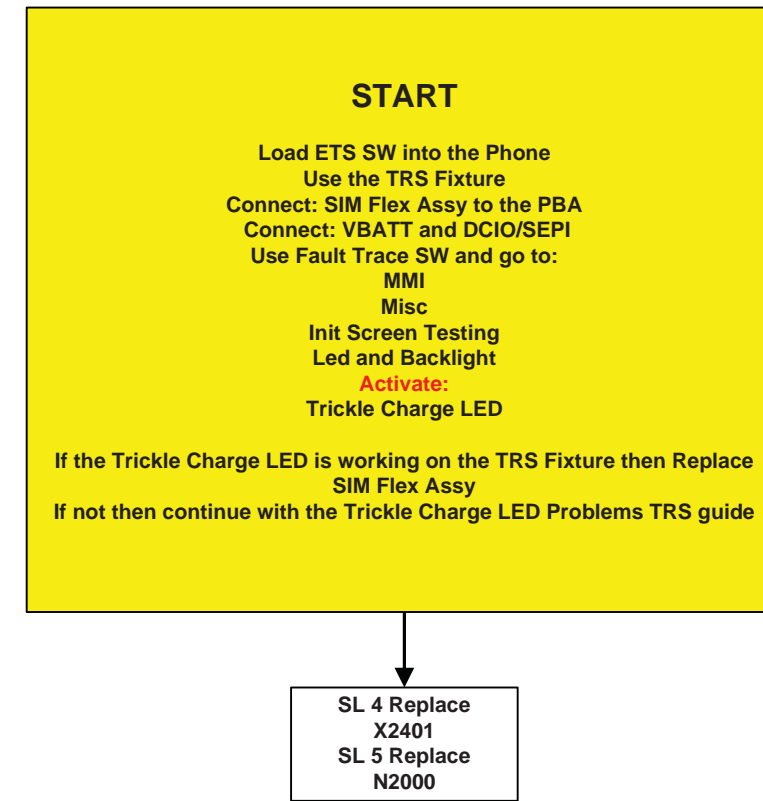
Camera Button LED Problems



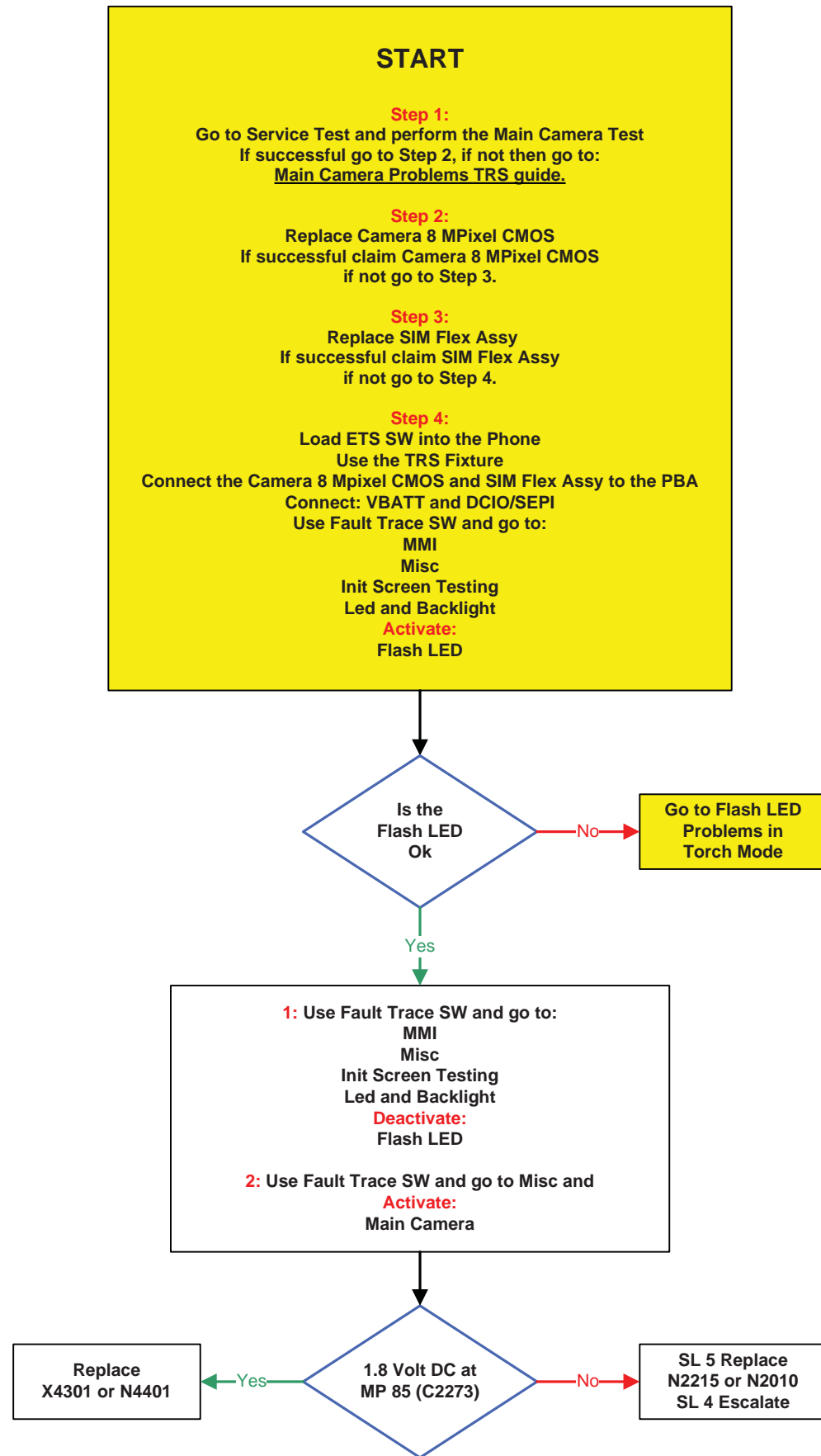
Music LED Problems



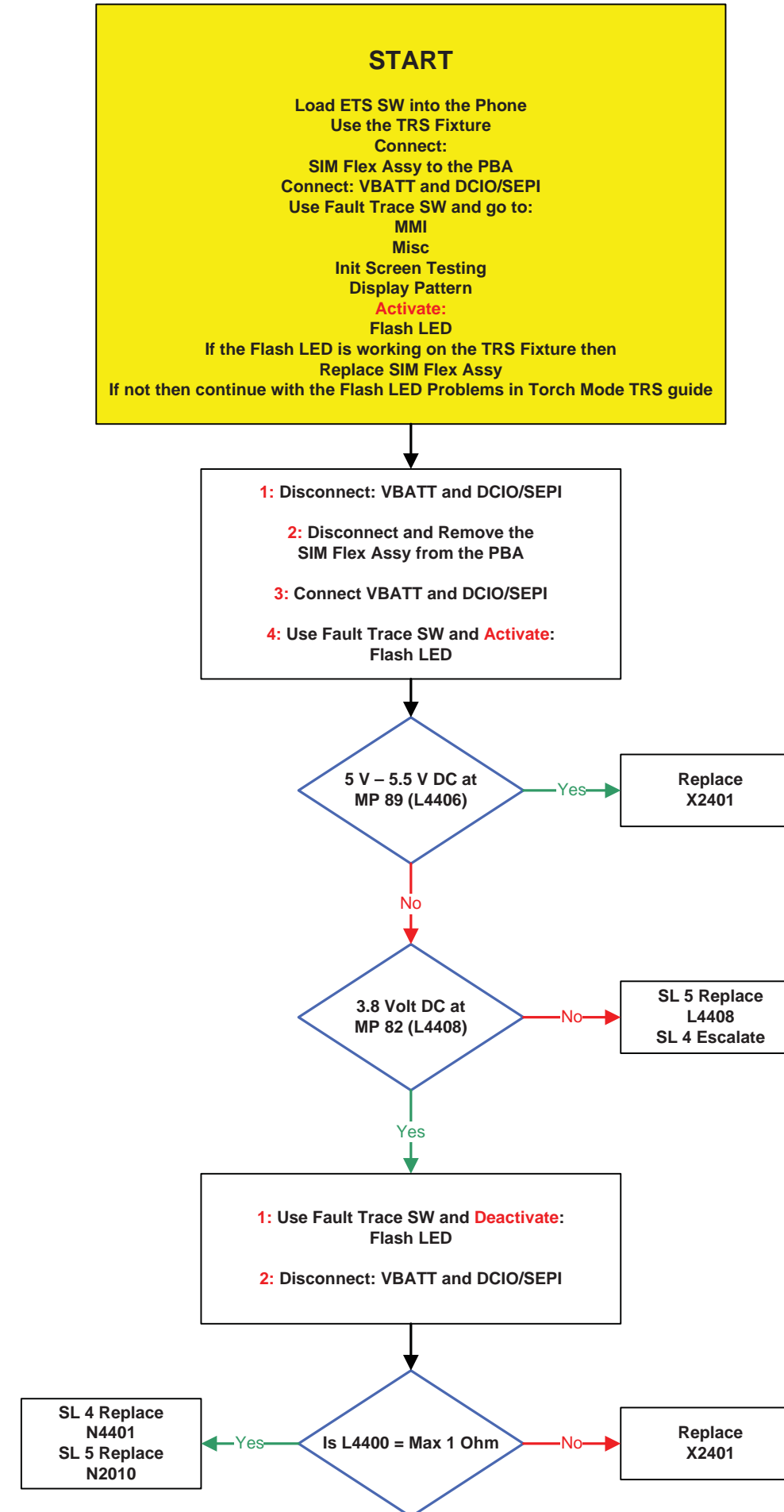
Trickle Charge LED Problems



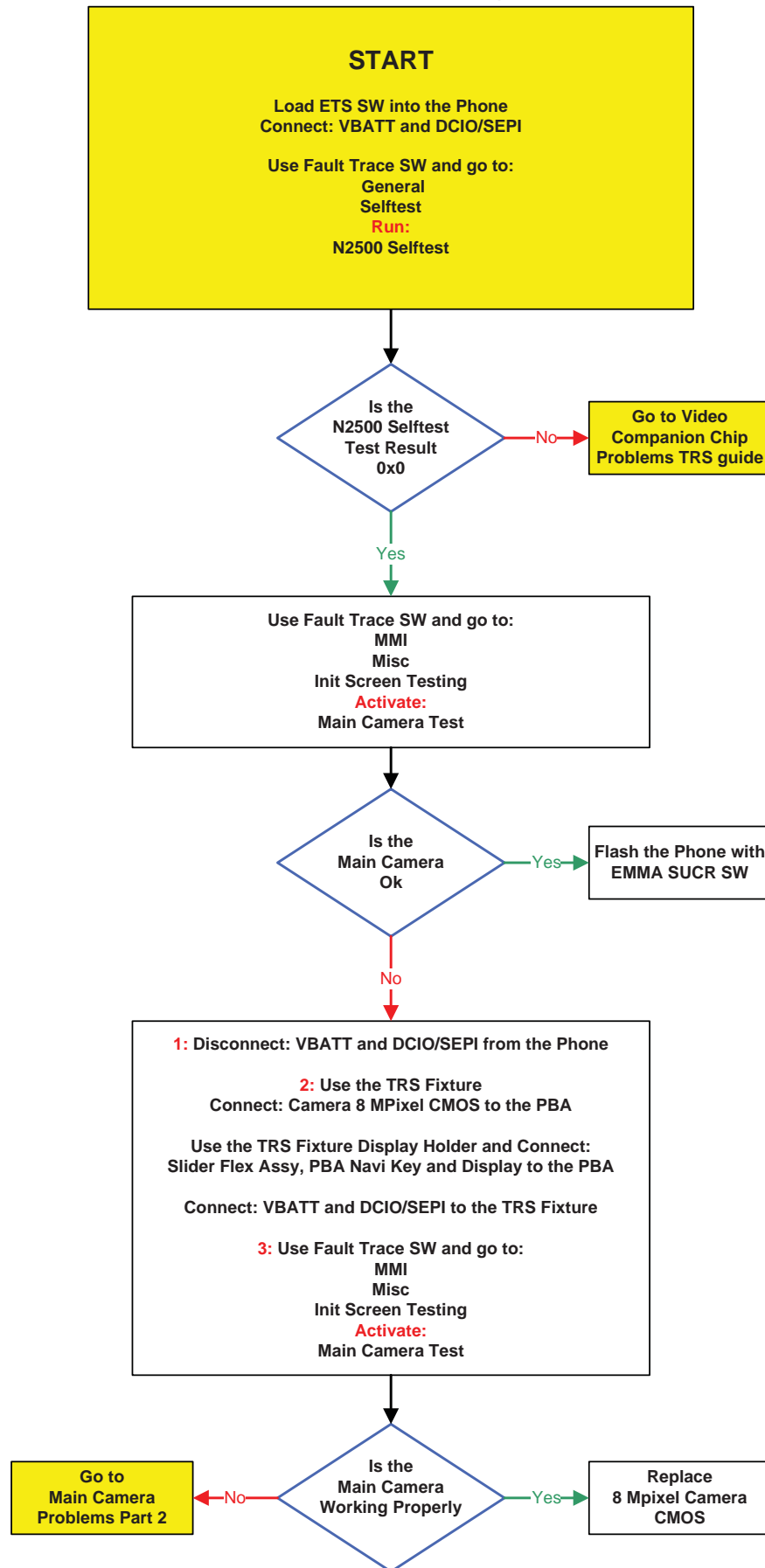
Flash LED Problems in Camera Mode



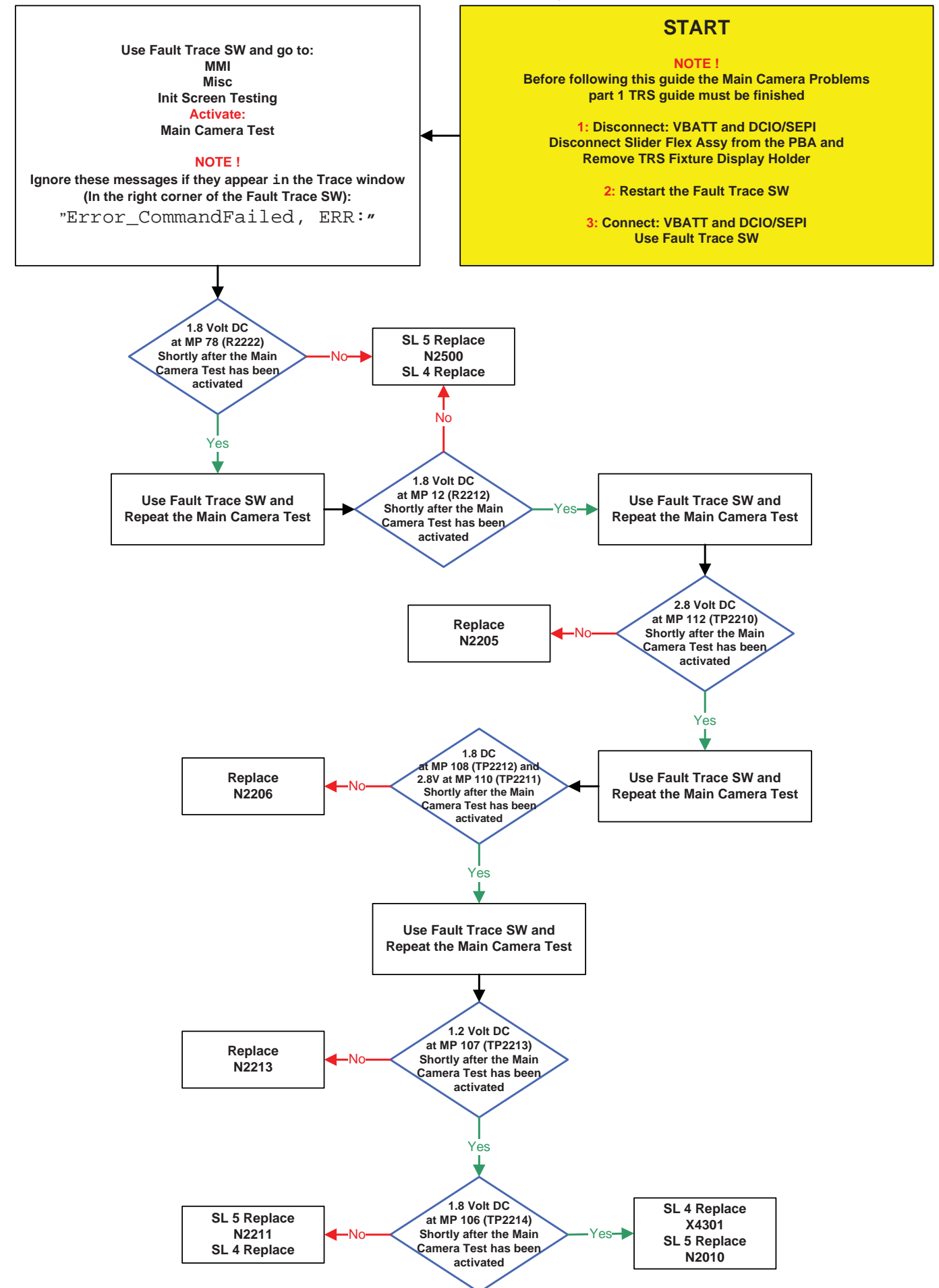
Flash LED Problems in Torch Mode



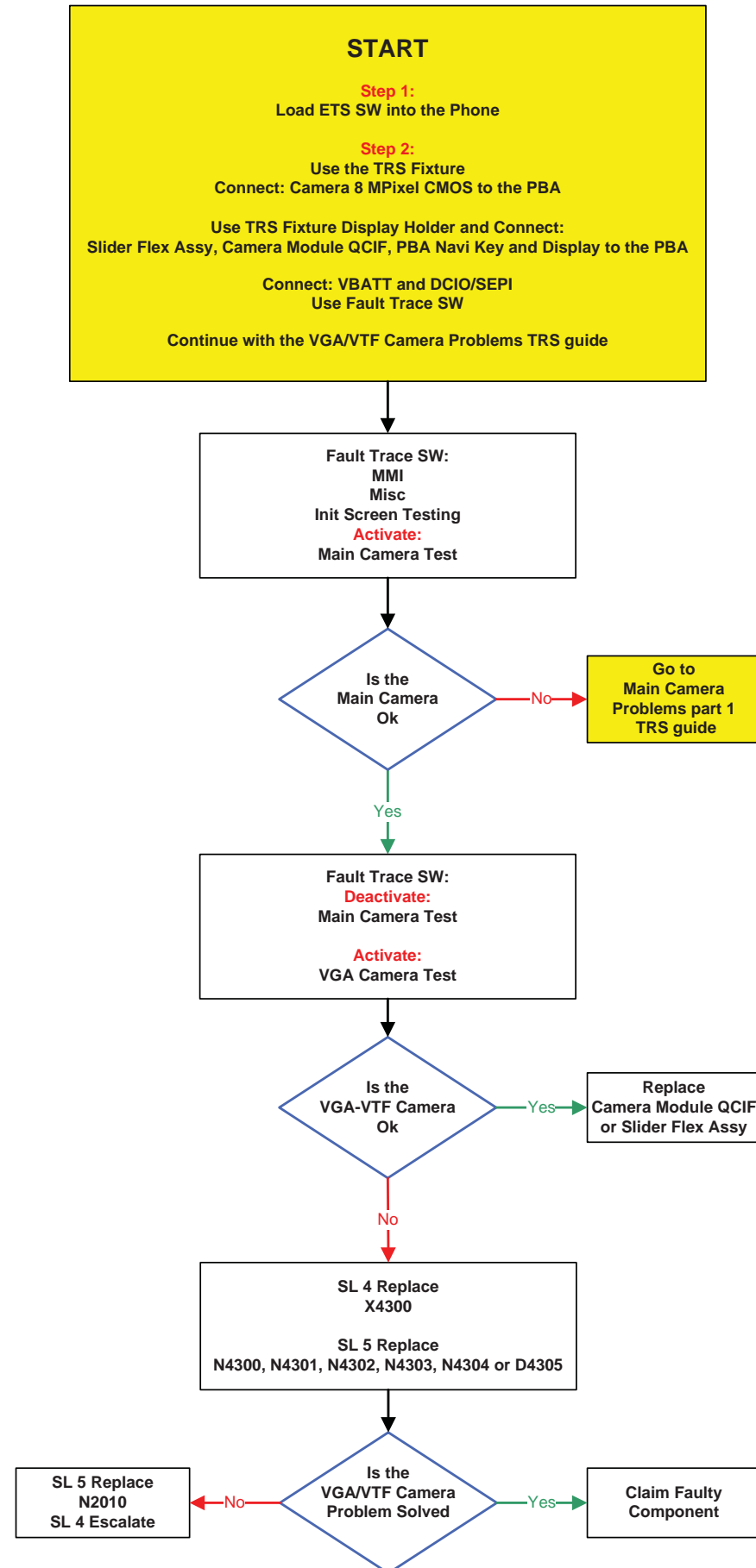
Main Camera Problems part 1



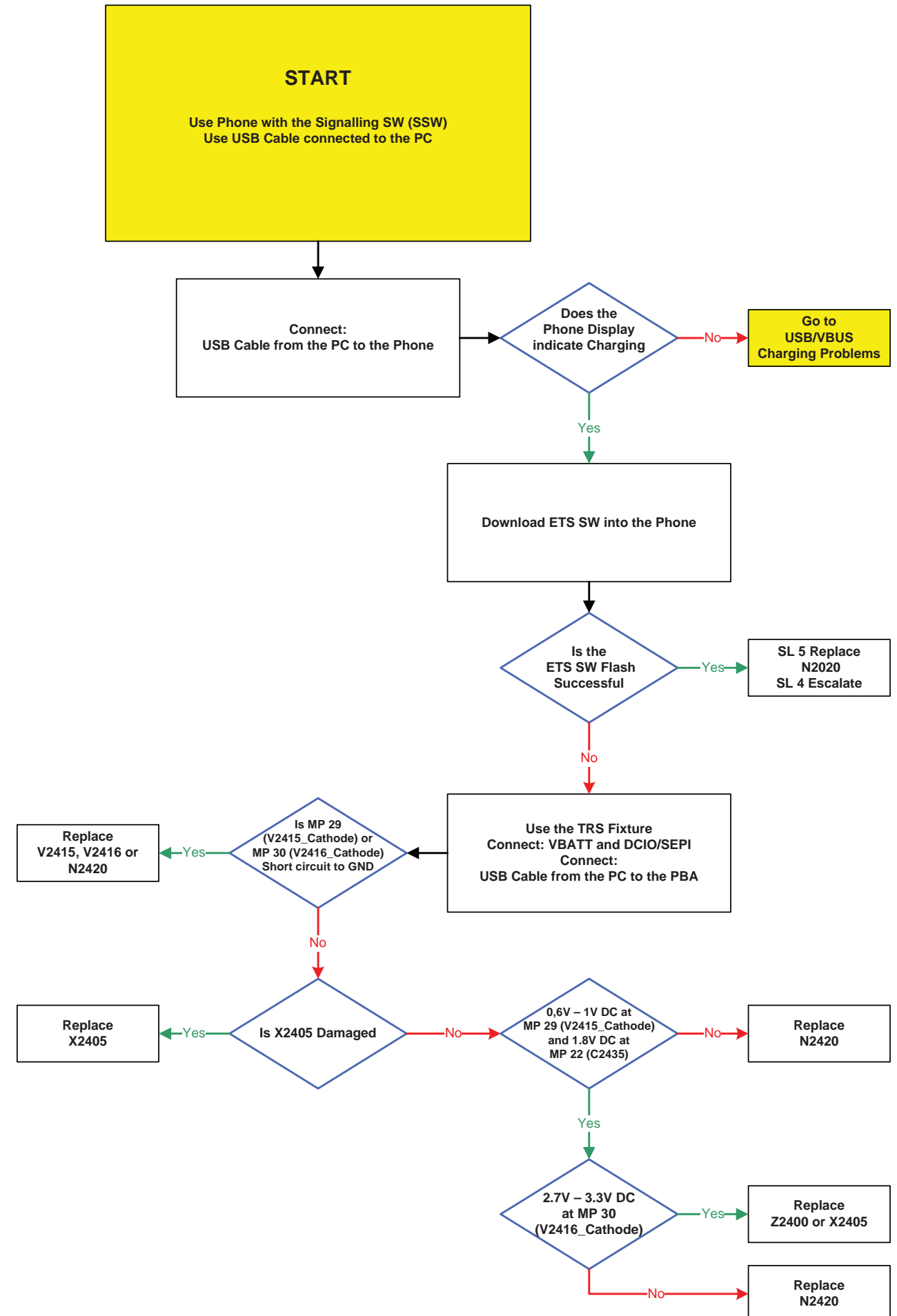
Main Camera Problems part 2



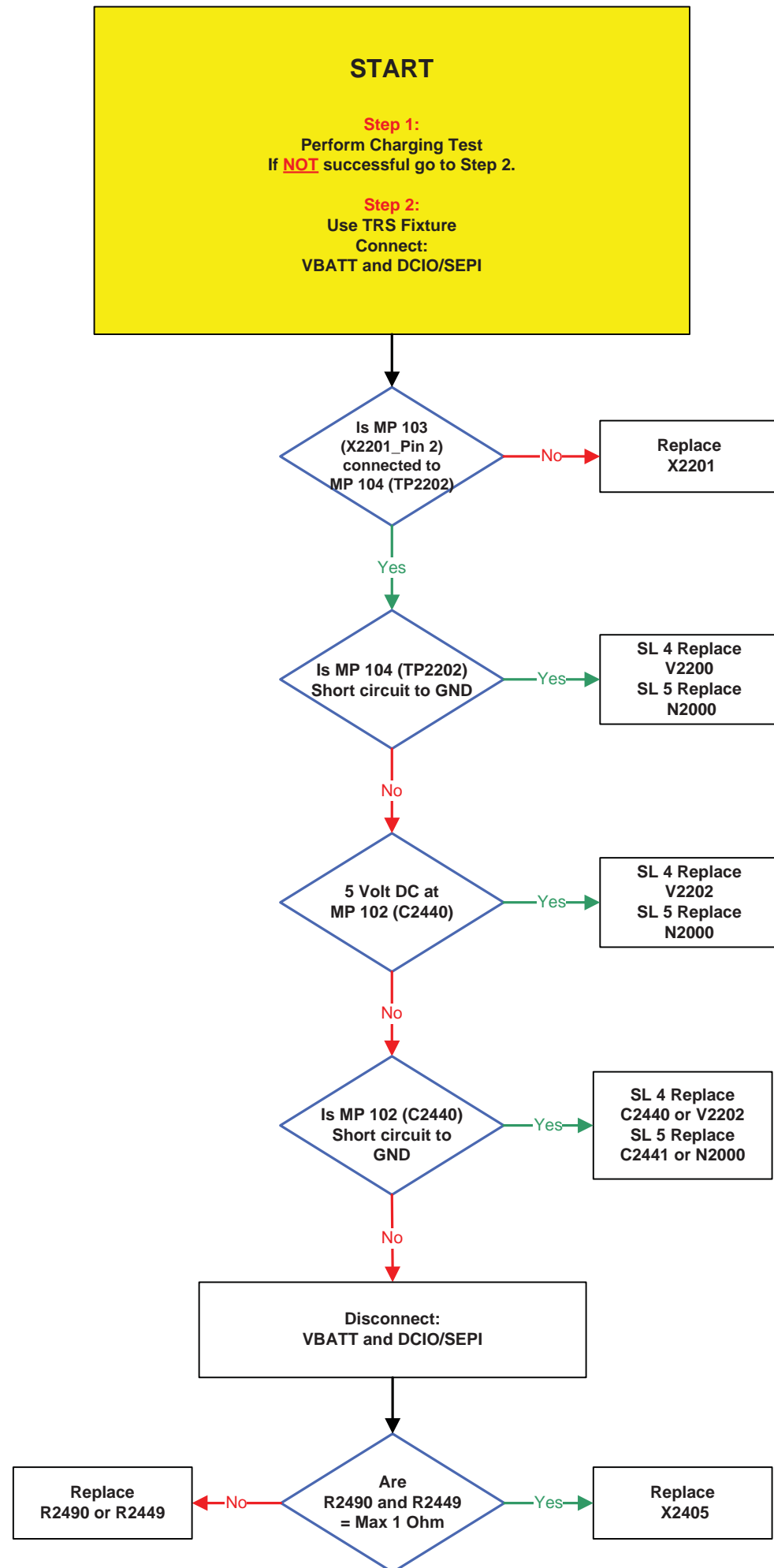
VGA/VTF Camera Problems



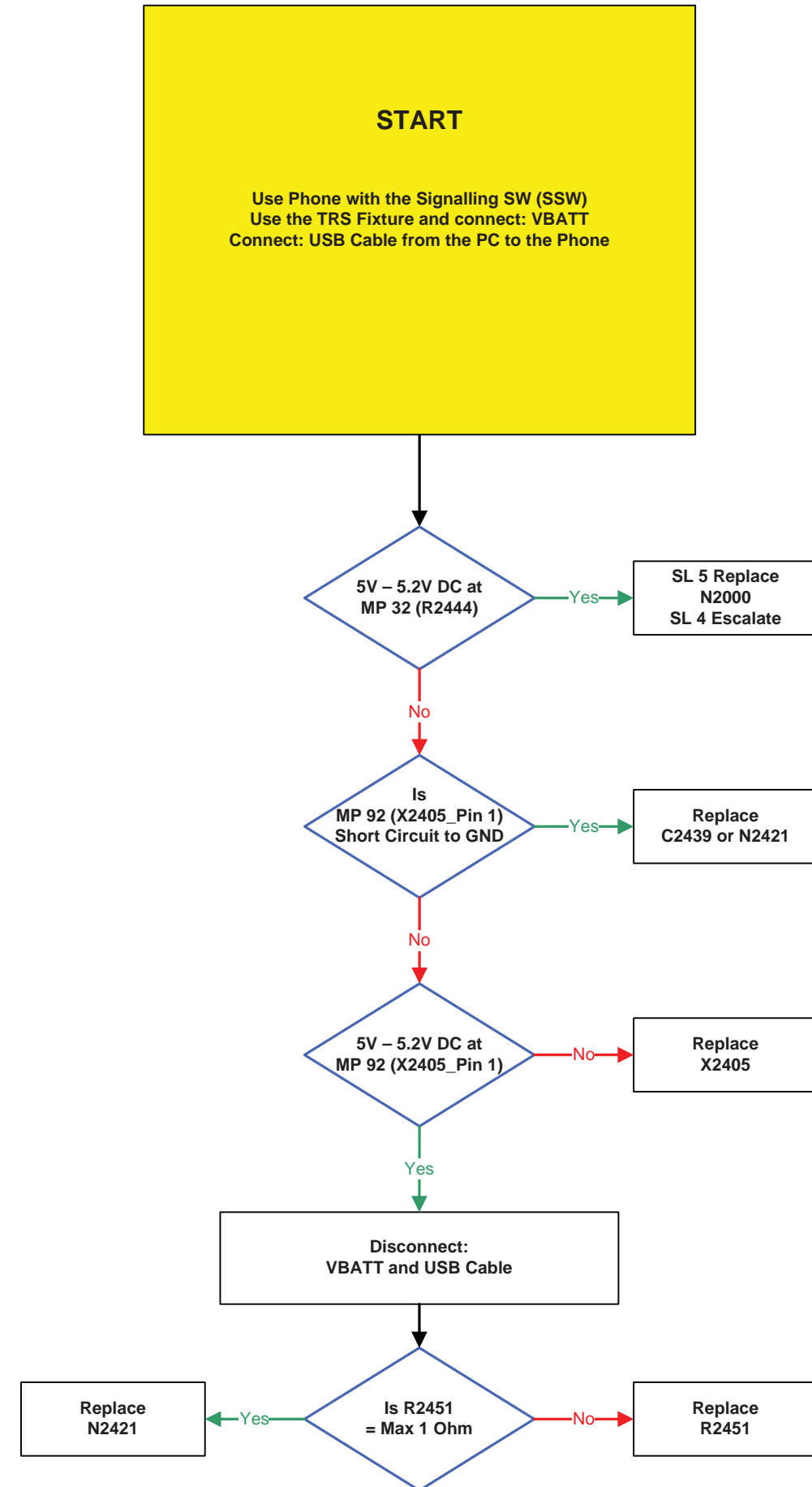
Data Communication Problems



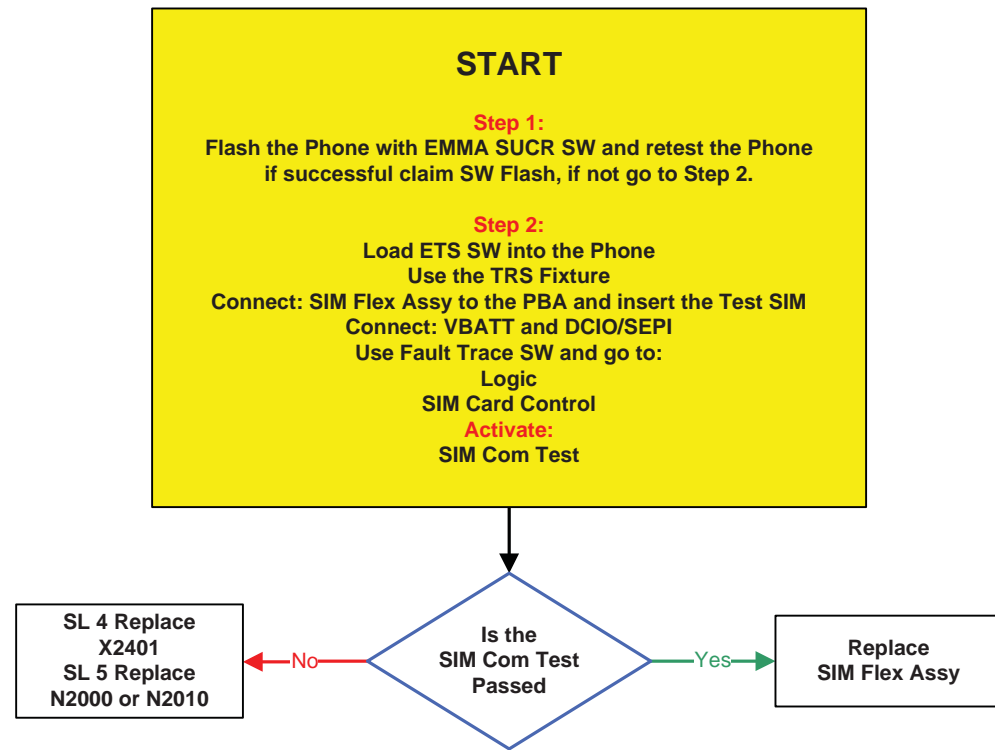
Charging Problems



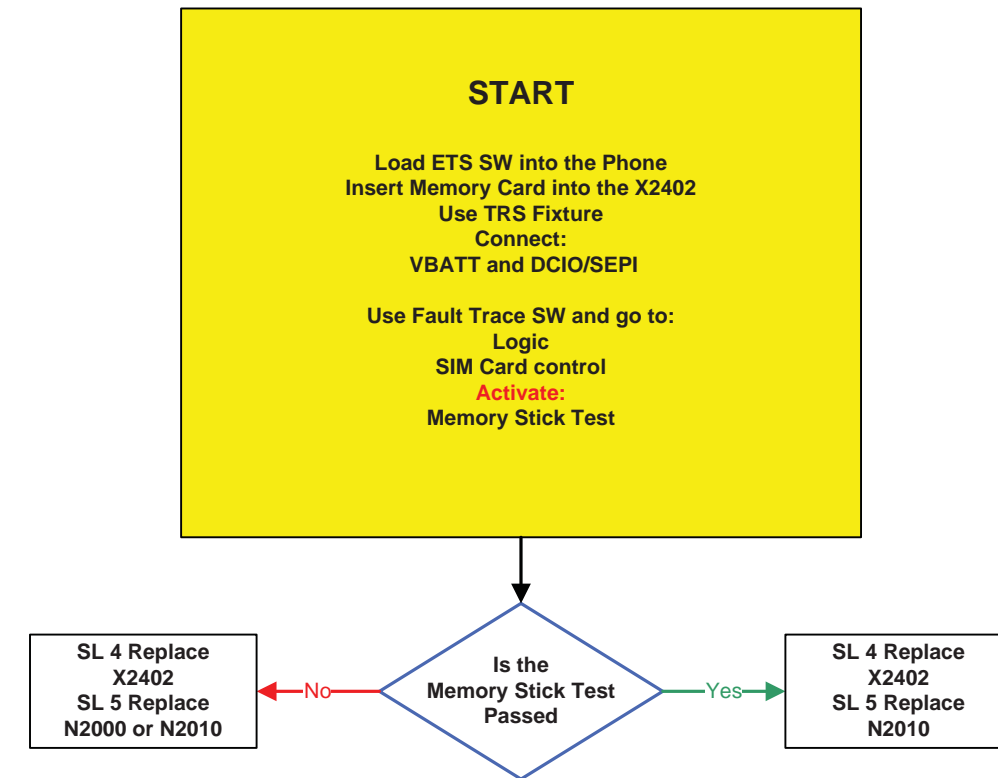
USB/VBUS Charging Problems



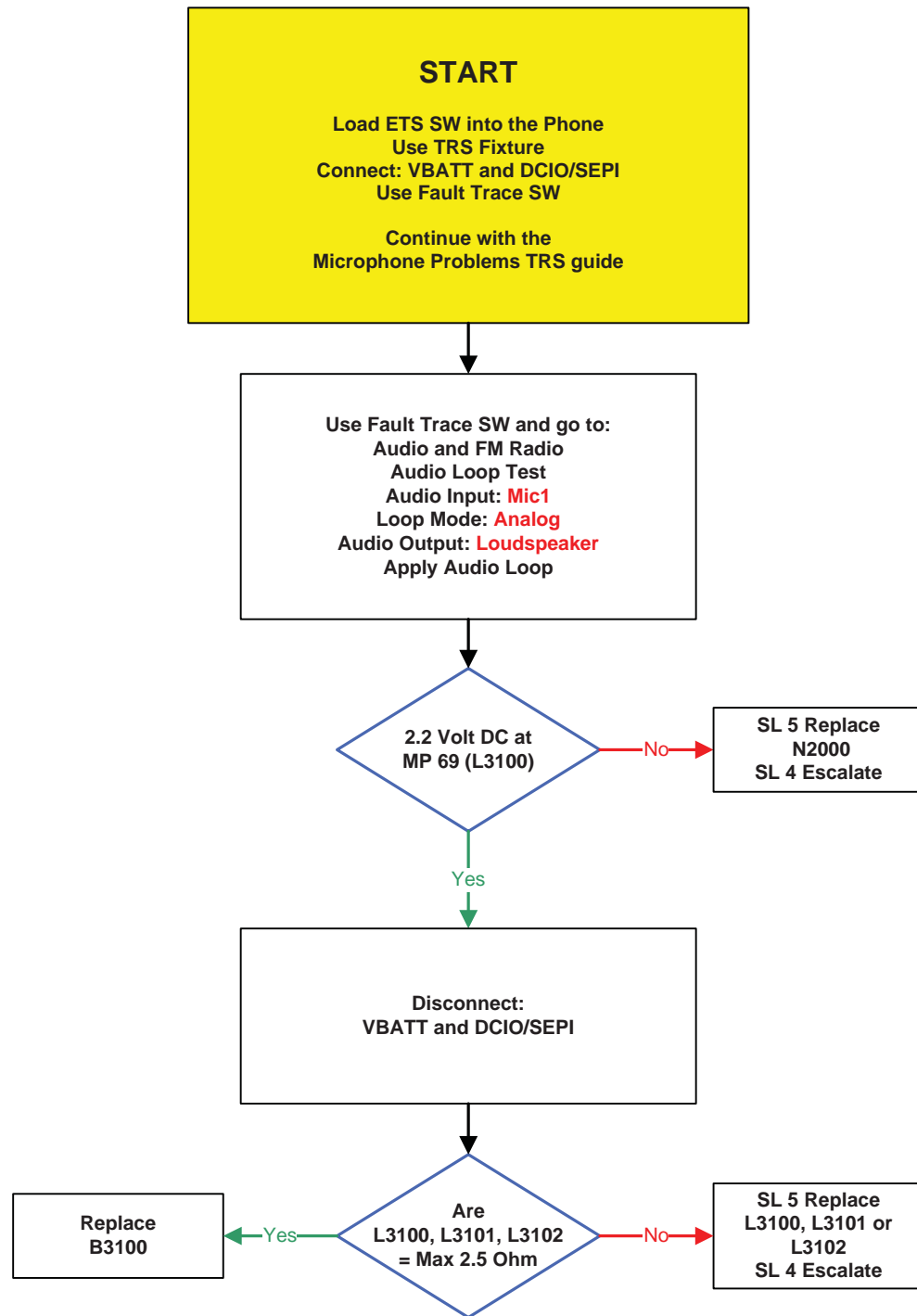
SIM Problems



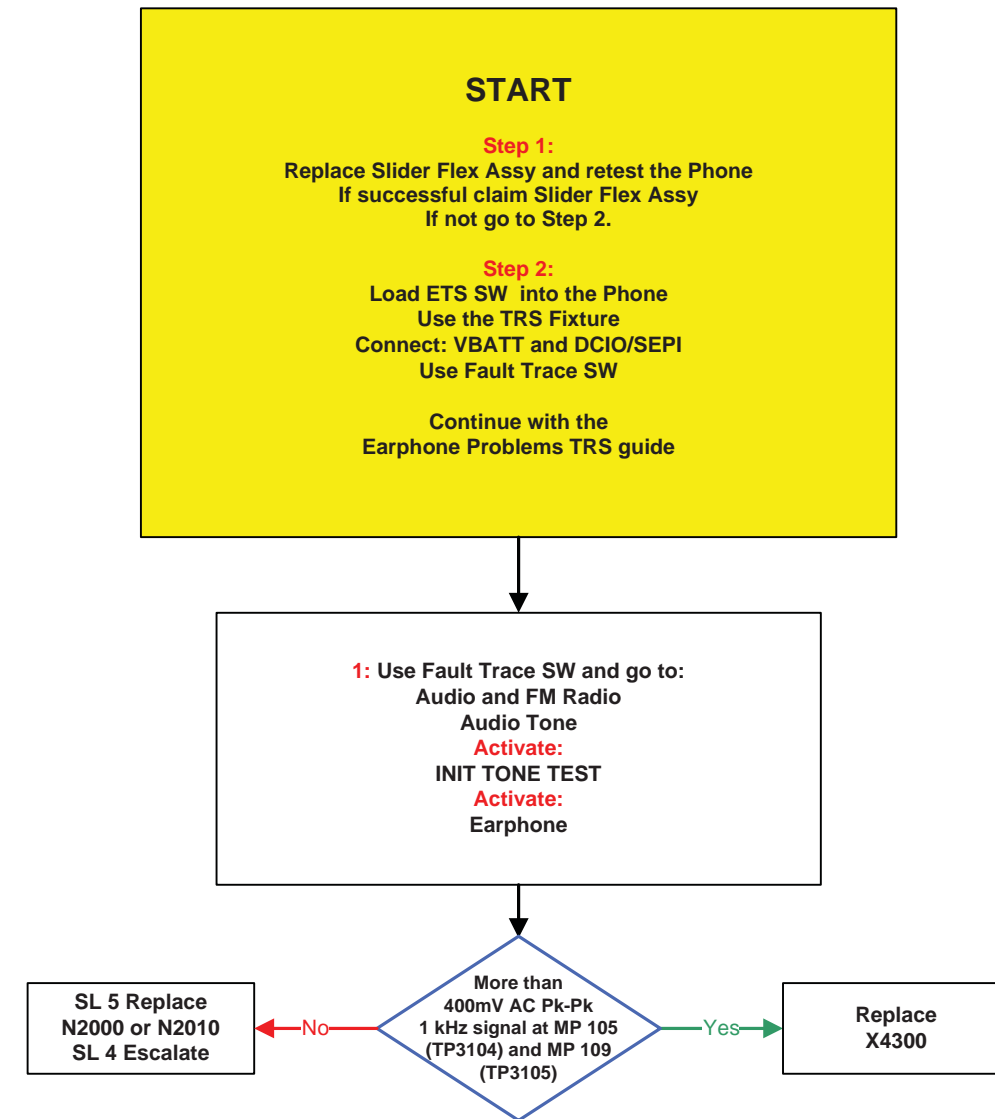
Memory Stick Problems



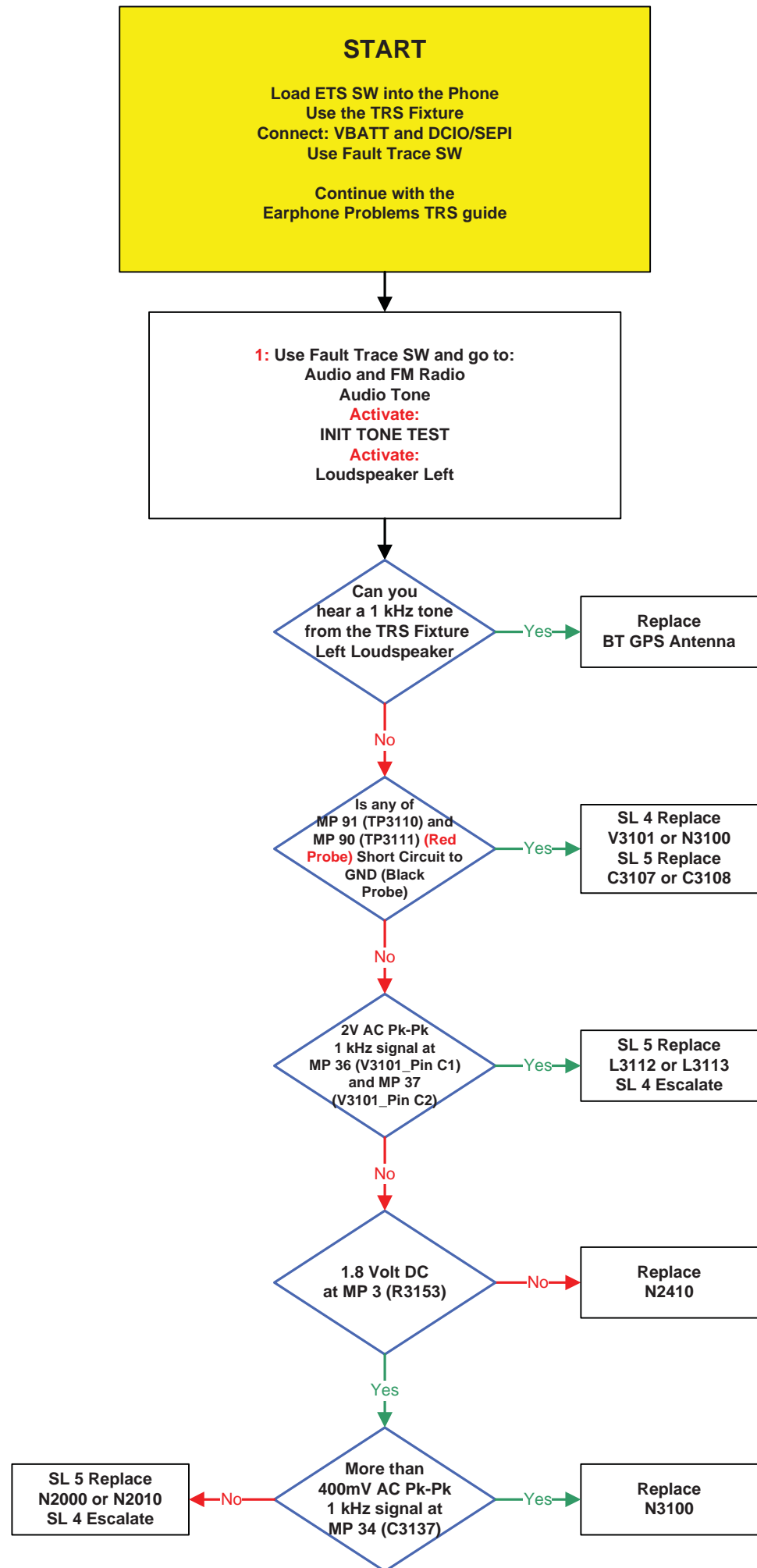
Microphone Problems



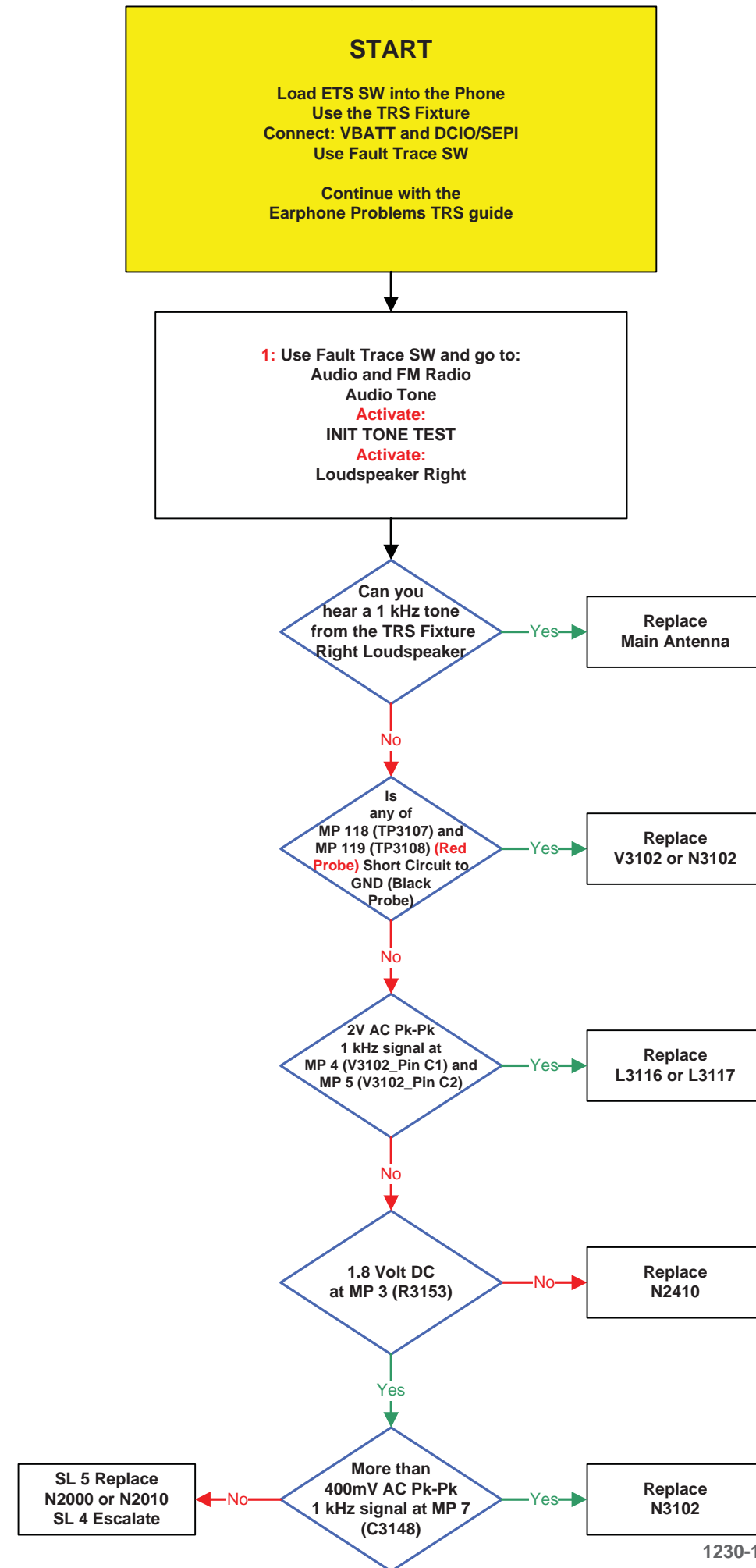
Earphone Problems



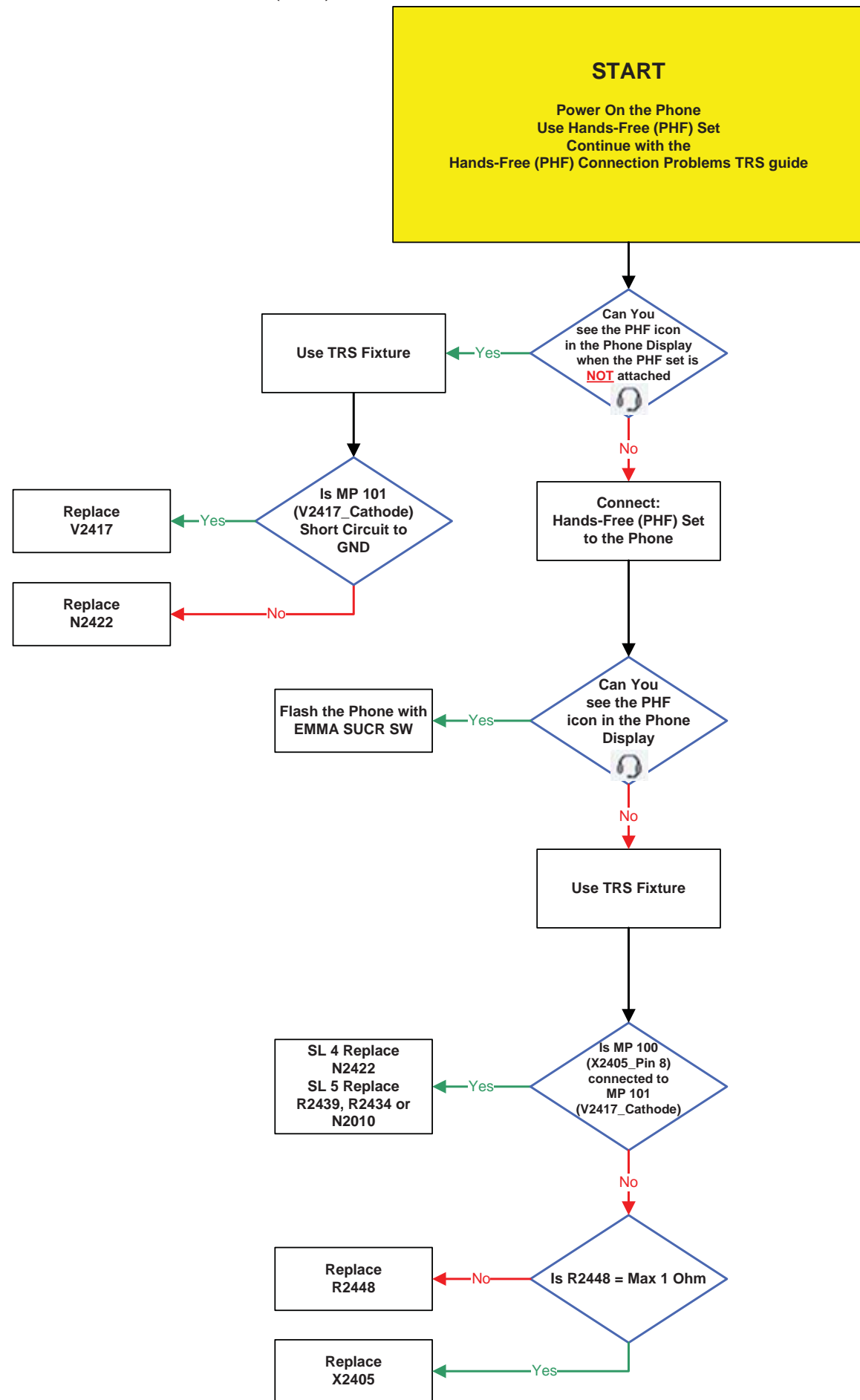
Loudspeaker Left Problems



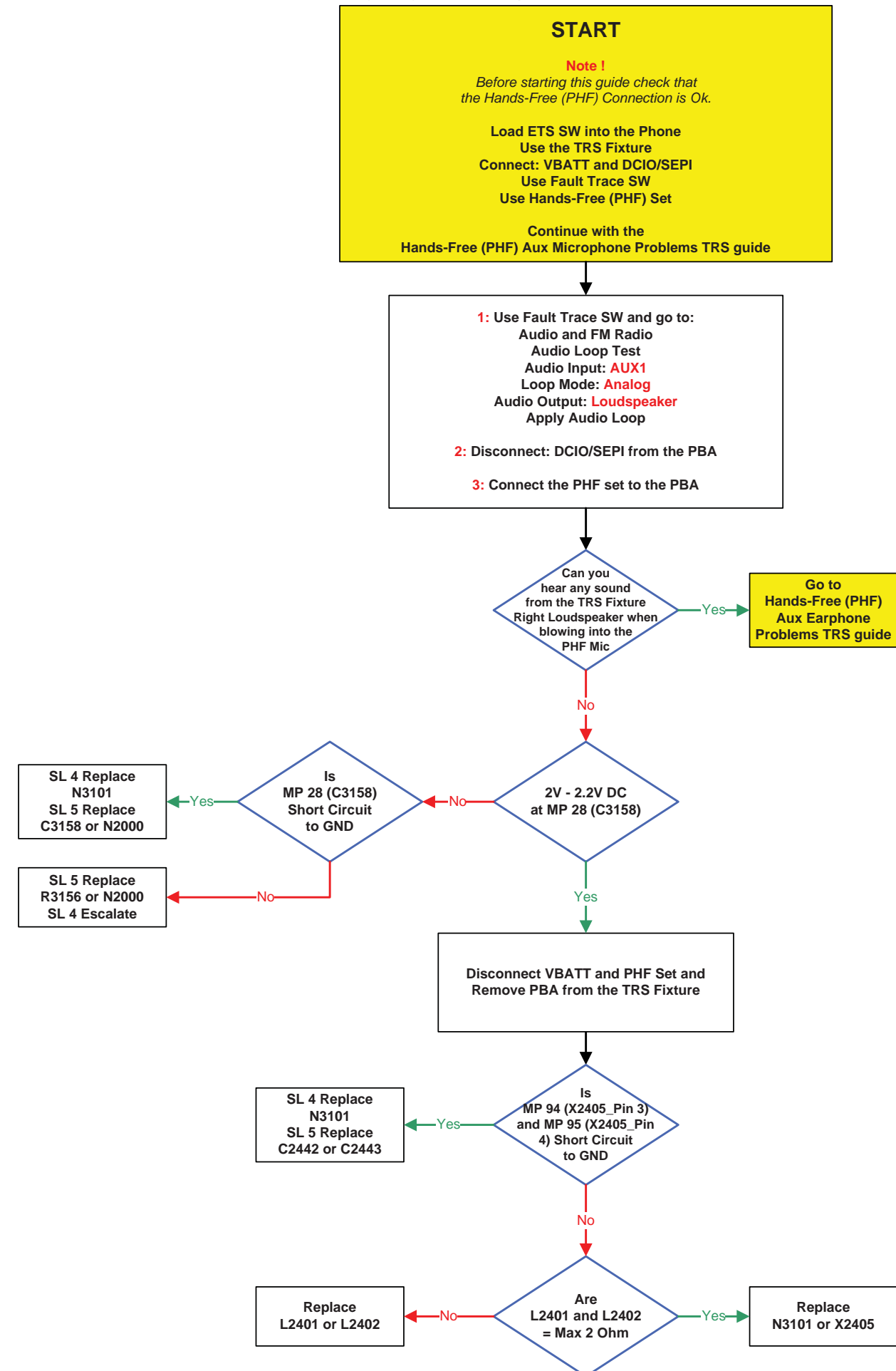
Loudspeaker Right Problems



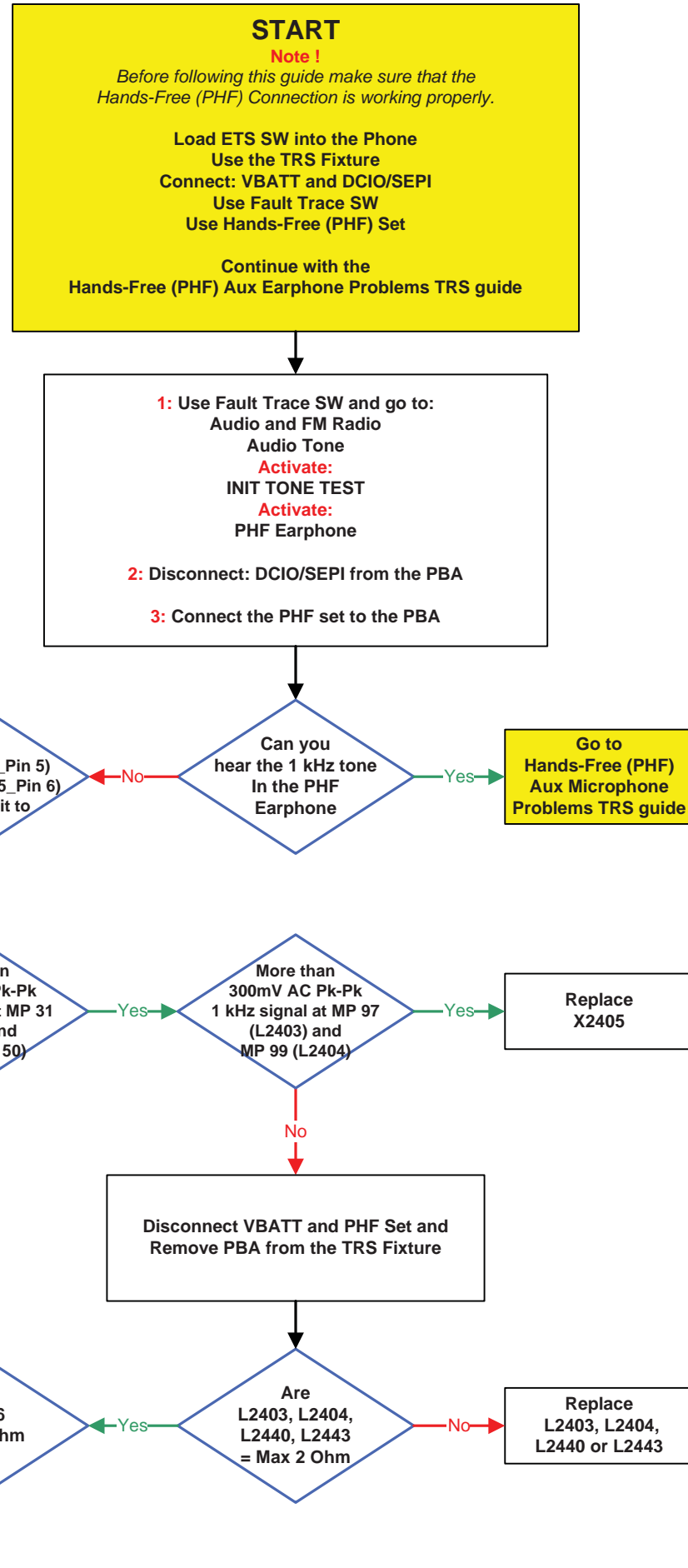
Hands-Free (PHF) Connection Problems



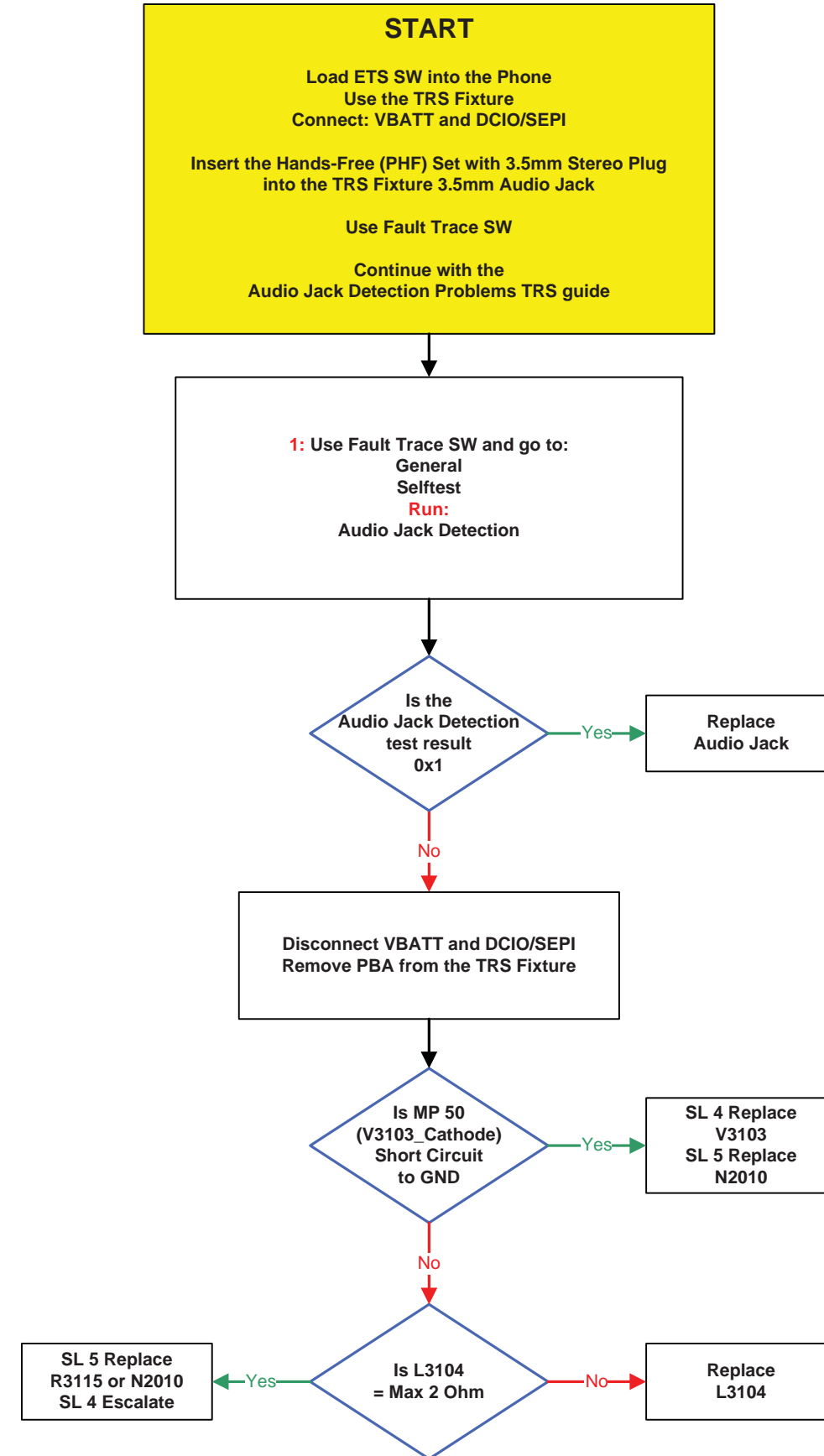
Hands-Free (PHF) Aux Microphone Problems



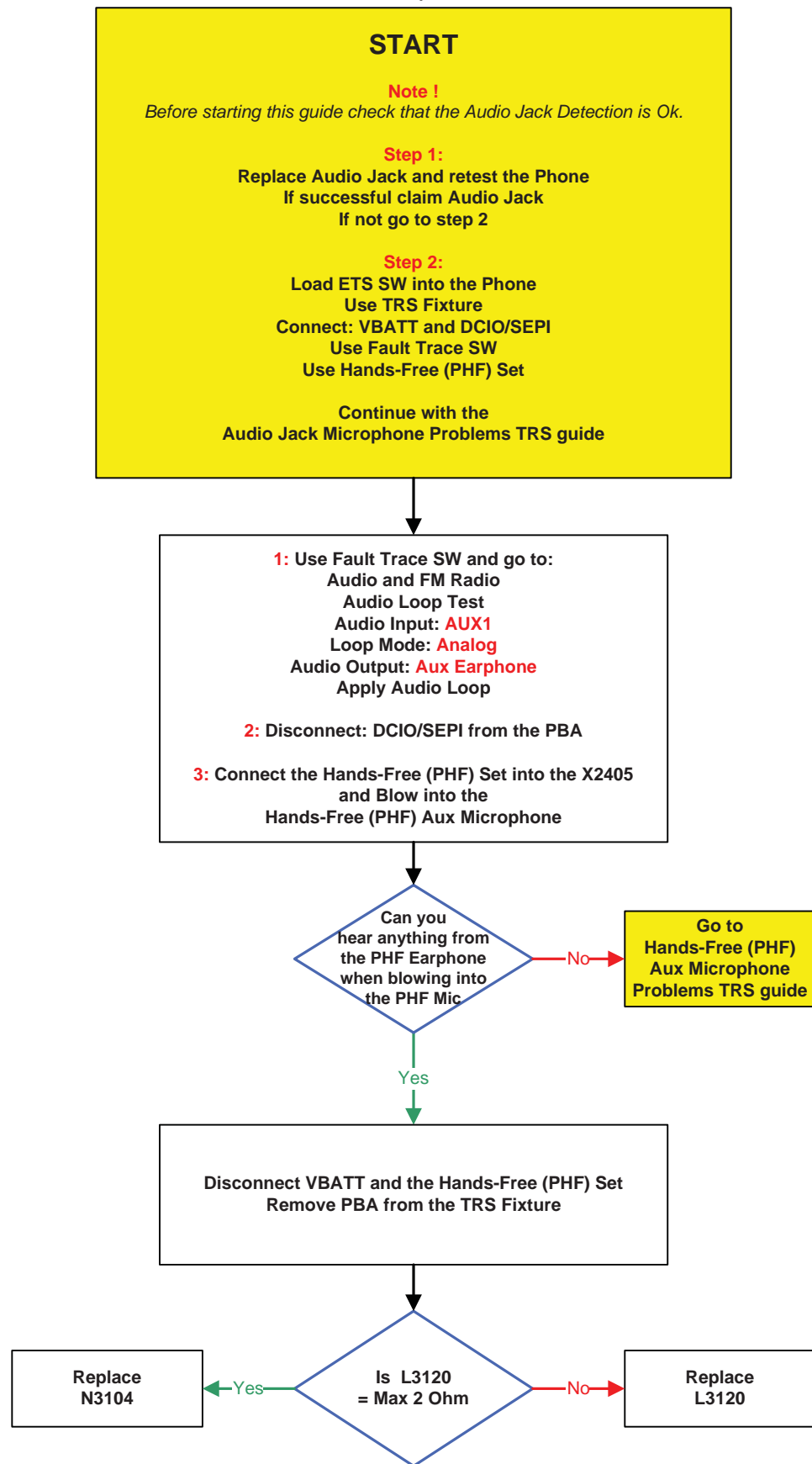
Hands-Free (PHF) Aux Earphone Problems



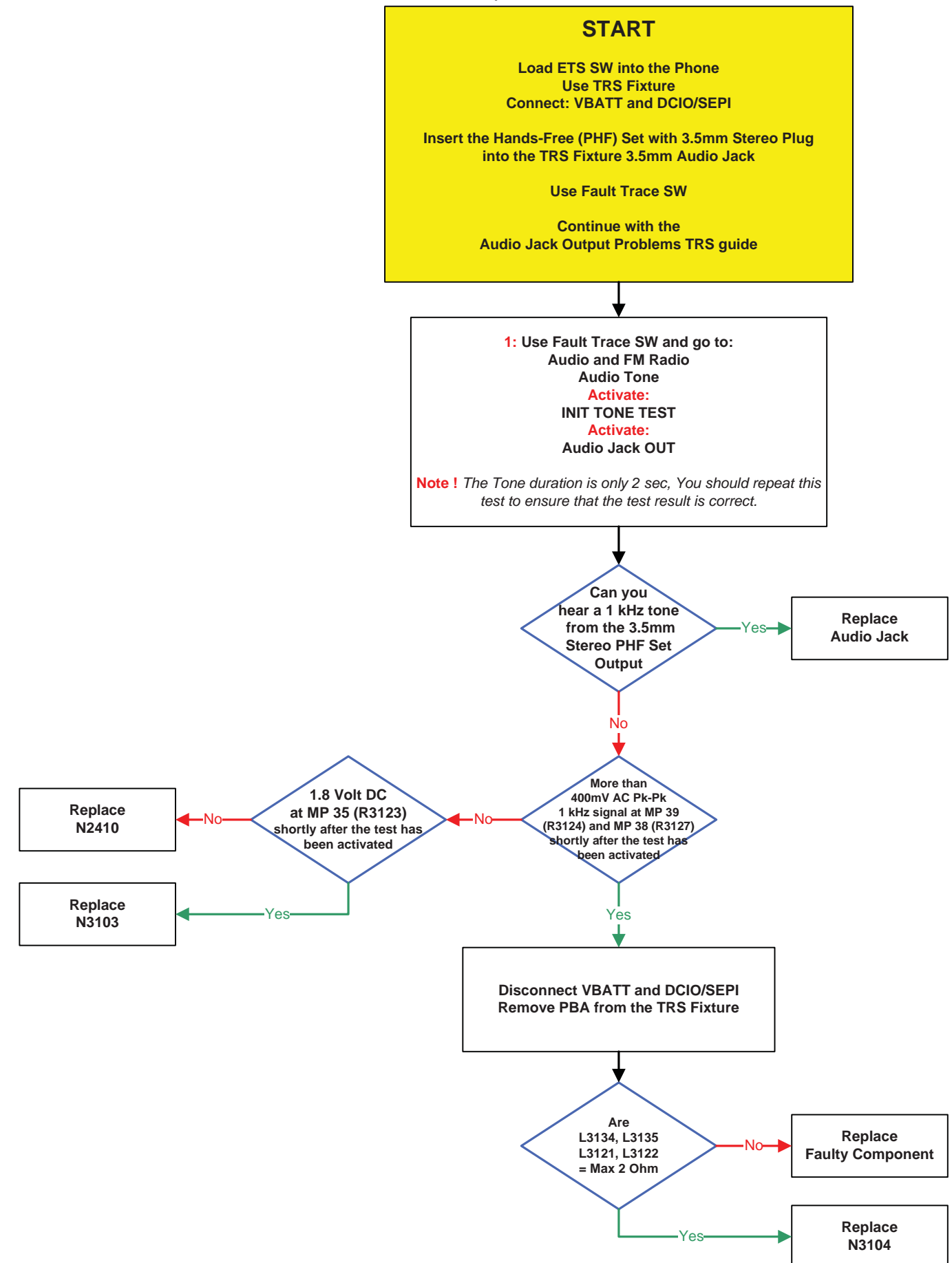
Audio Jack Detection Problems



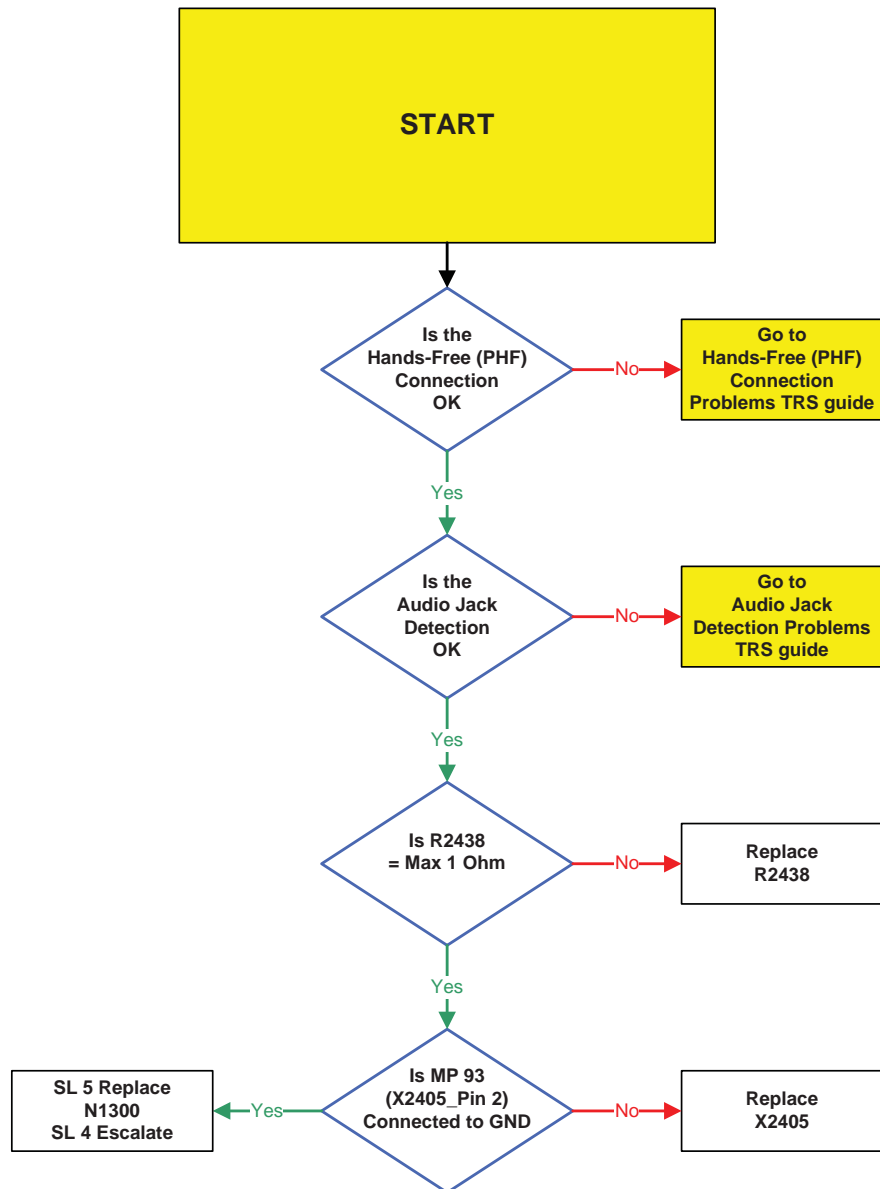
Audio Jack Microphone Problems



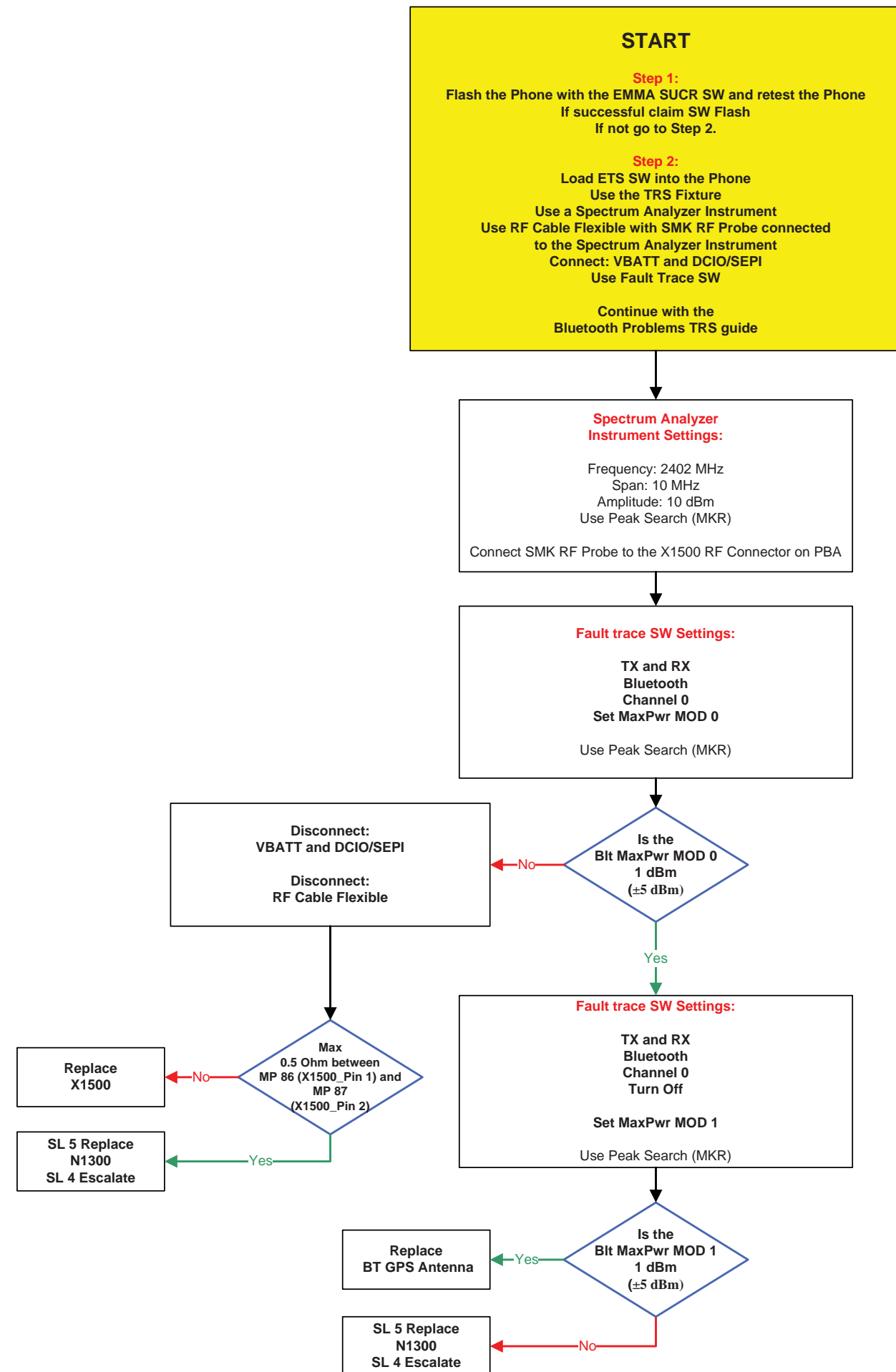
Audio Jack Output Problems



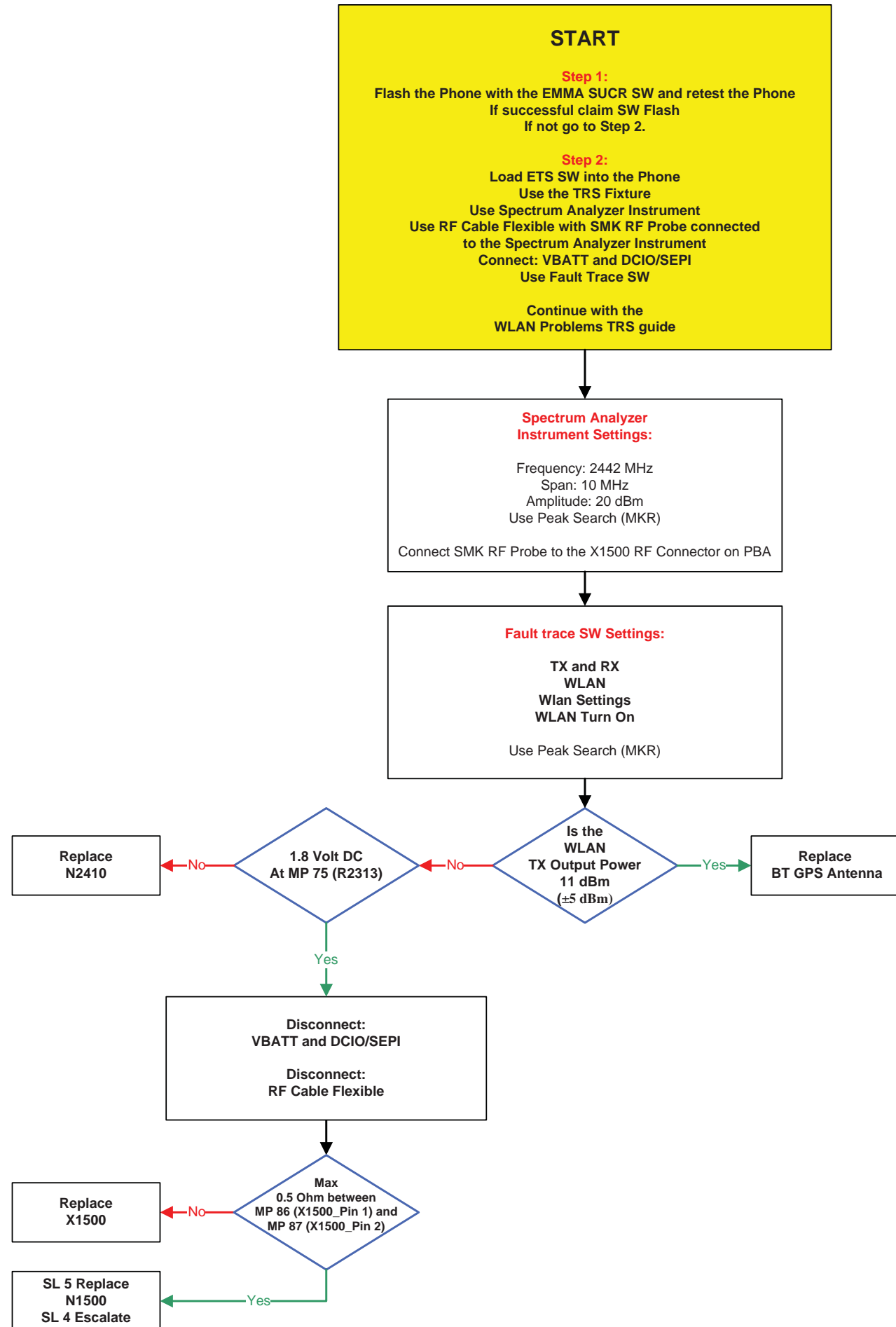
FM Radio Problems



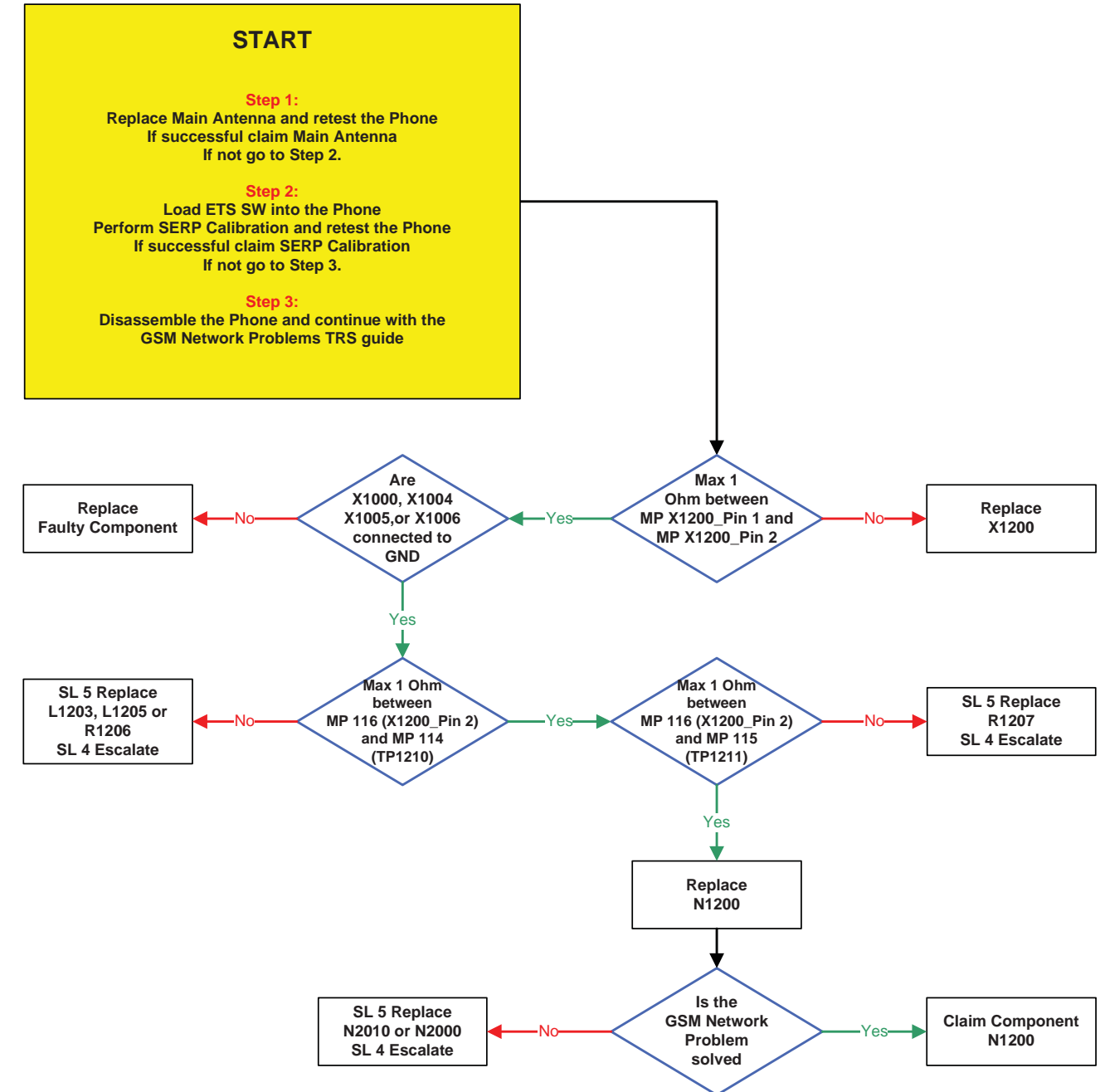
Bluetooth Problems



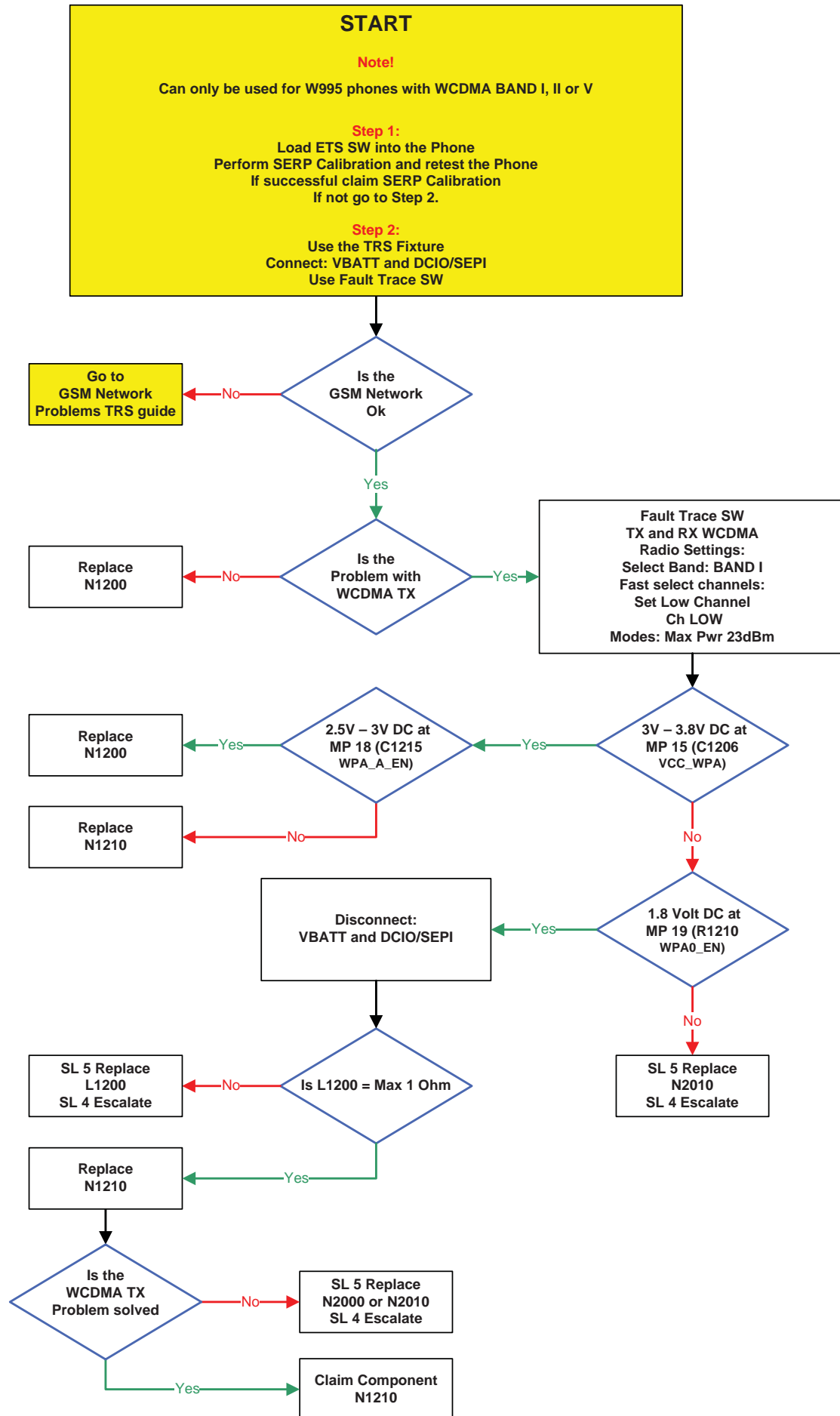
WLAN Problems



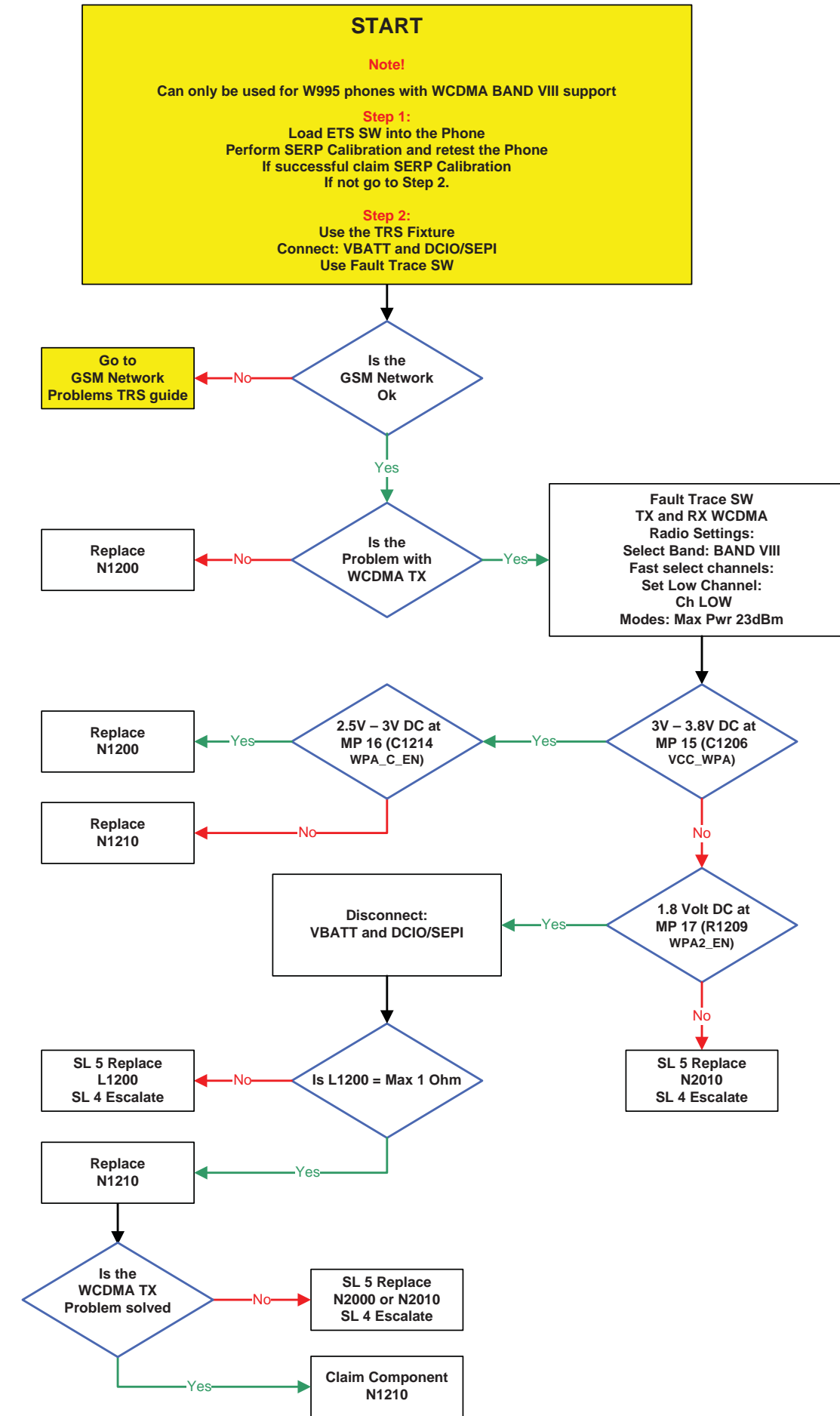
GSM Network Problems



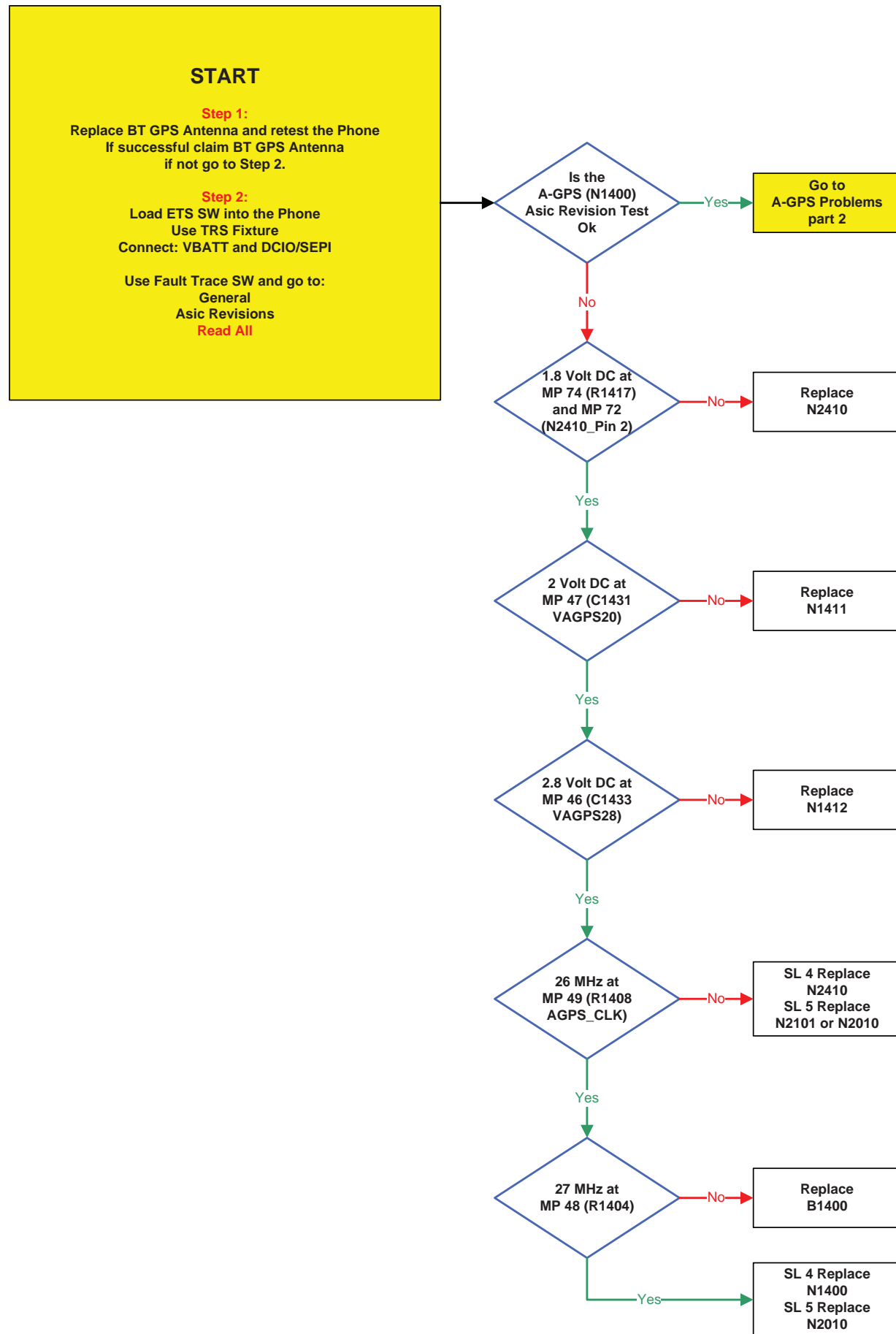
WCDMA BAND I,II,V Network Problems



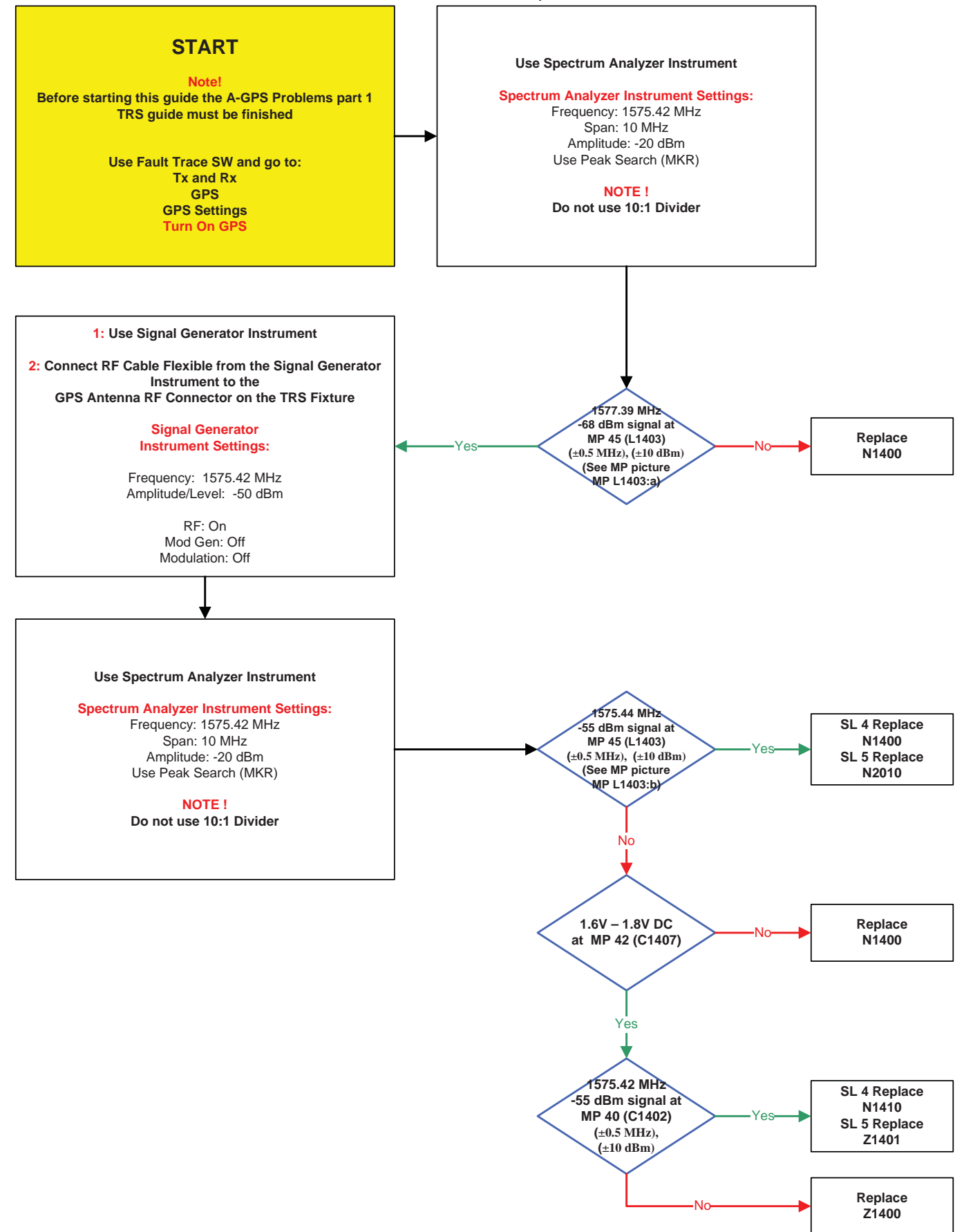
WCDMA BAND VIII Network Problems



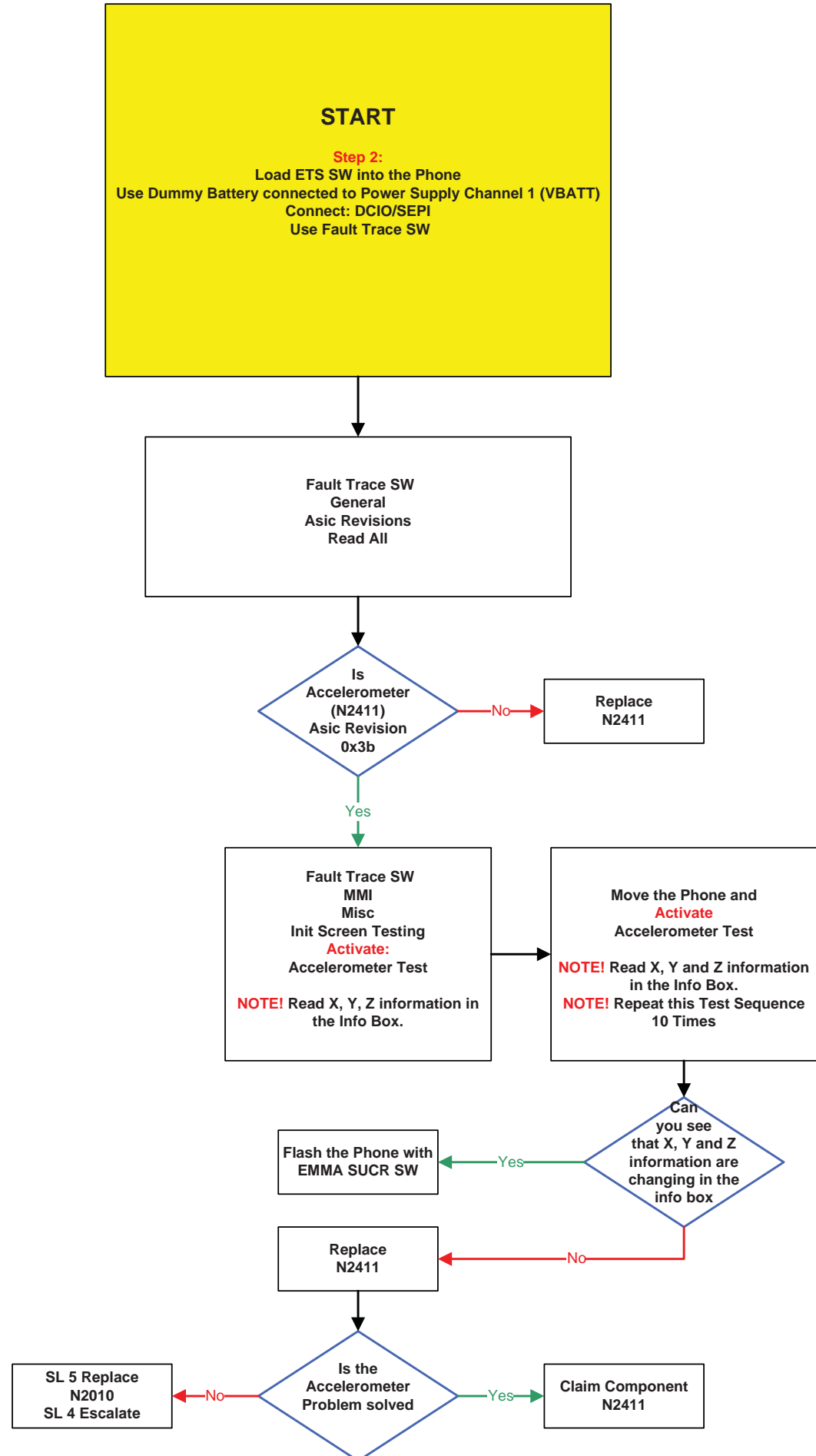
A-GPS Problems part 1



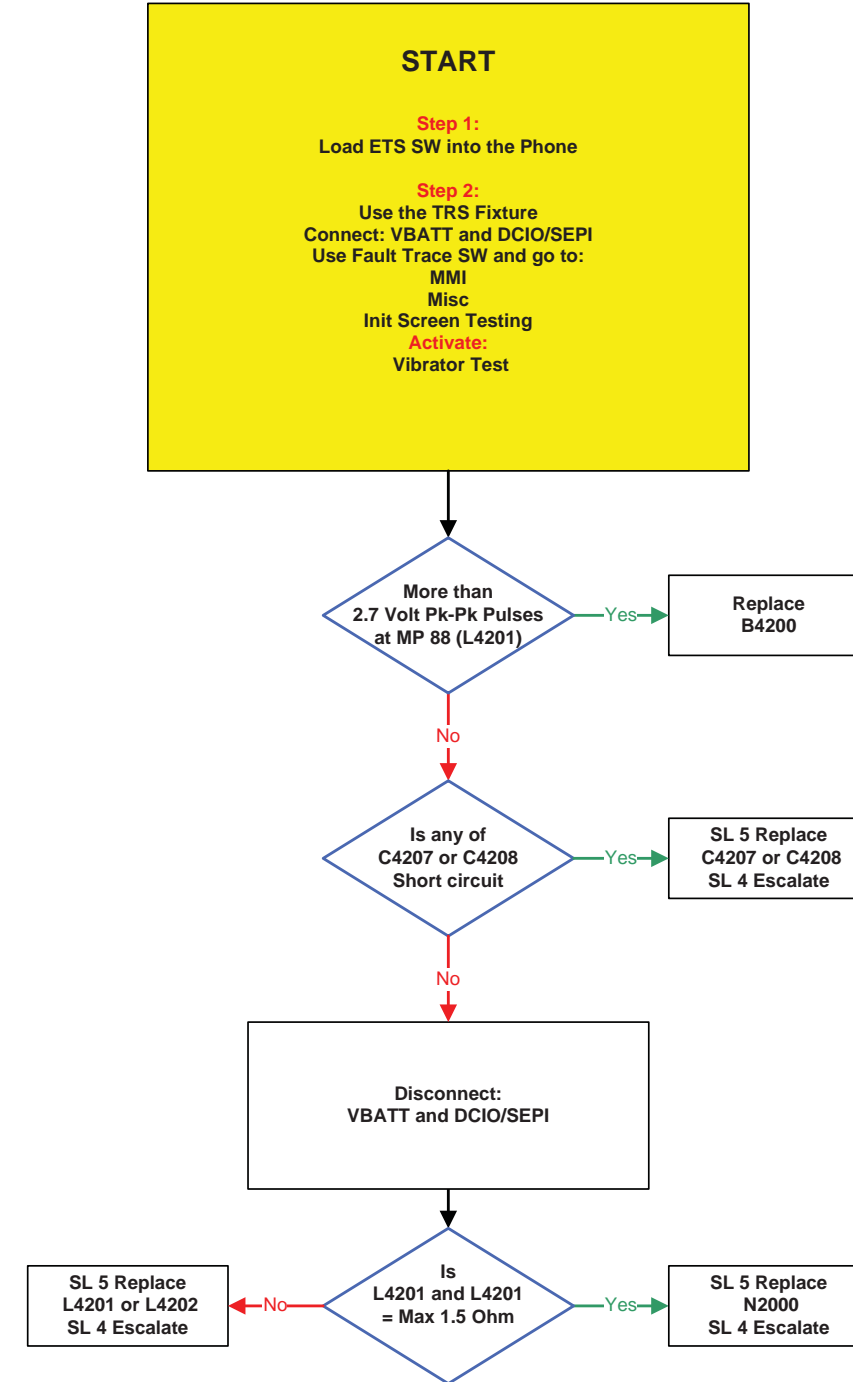
A-GPS Problems part 2



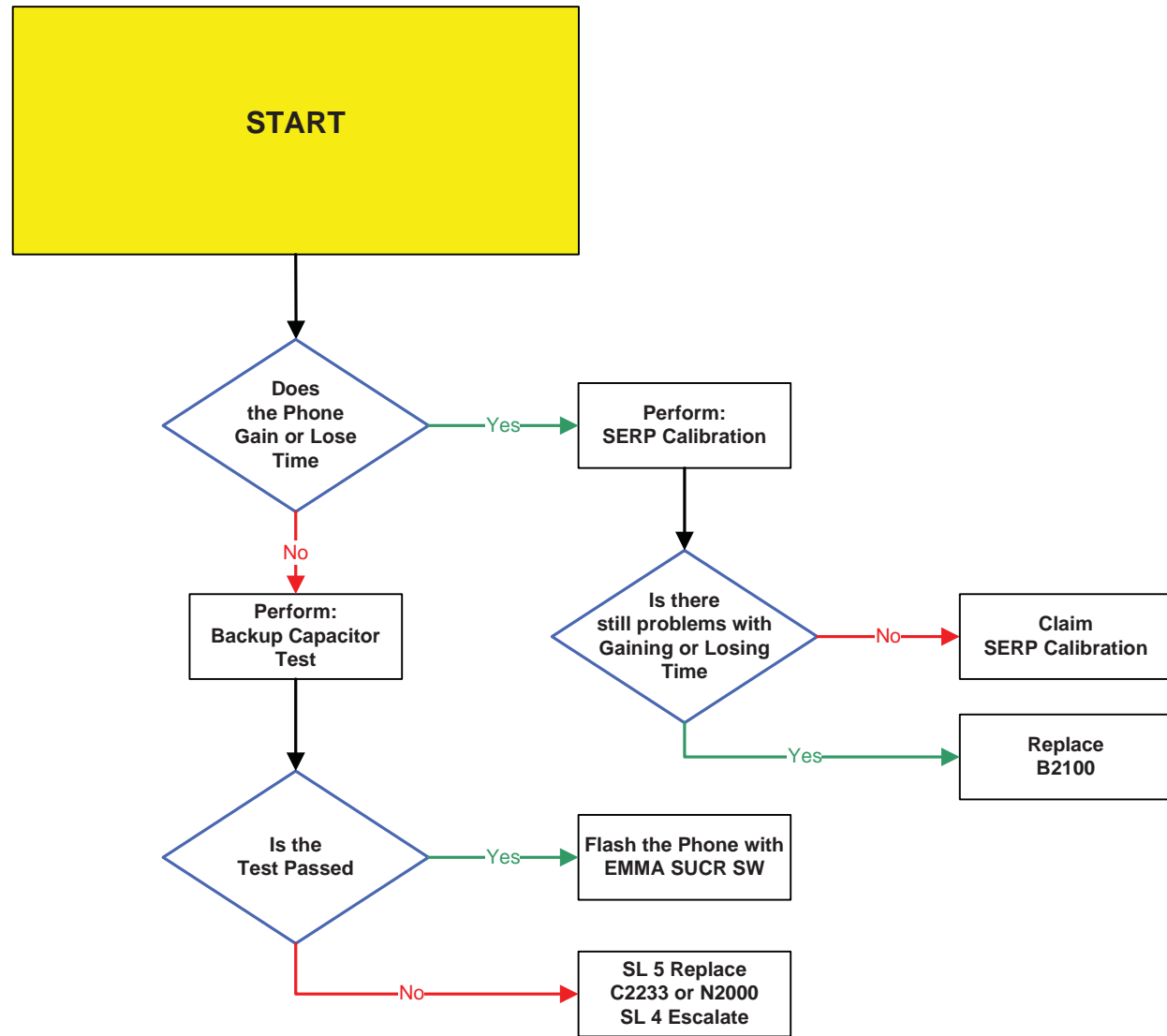
Accelerometer Problems



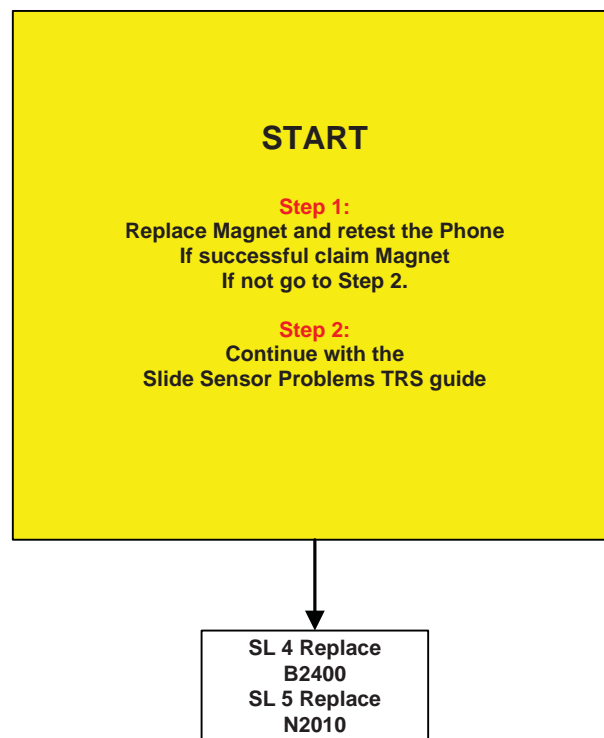
Vibrator Problems



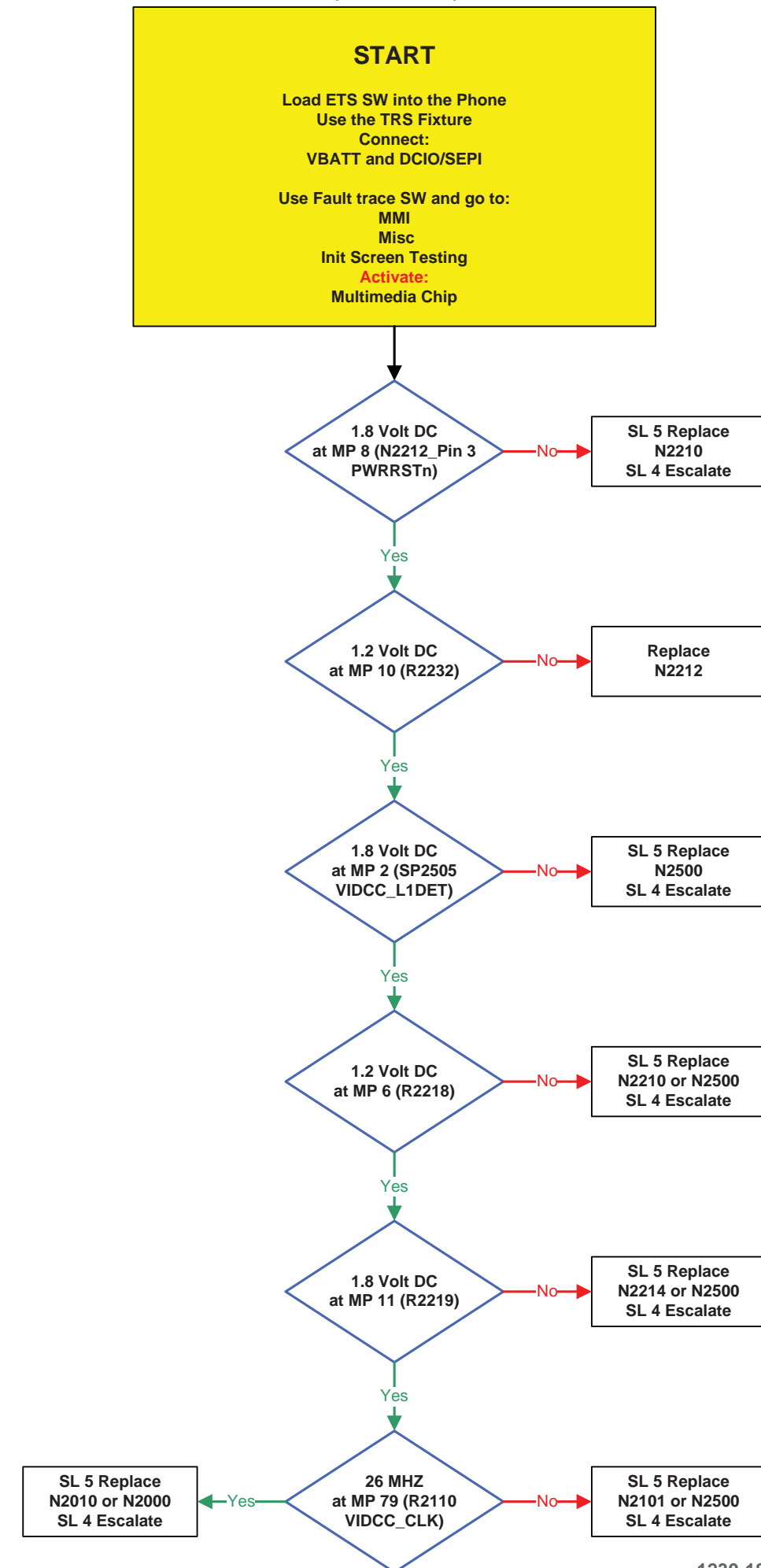
Real Time Clock Problems



Slide Sensor Problems



Video Companion Chip Problems



System Connector Protection Test

Perform the Ohm measurements by using the DMM instrument (Fluke).

Note! The Battery must be removed from the Phone during this test.

Note! Connect the Black probe to the X2405_PIN 9 (GND).



PIN_1 PIN_9 GND PIN_12

System Conn. X2405 (PIN Position)	Ohm Measurements (Ohm)	SL 4 (Repair Action)	SL 5 (Repair Action)
1	OL	If lower or higher then go to: USB/VBUS Charging Problems TRS guide	No Action
2	0	If lower or higher then go to: FM Radio Problems or Hands-Free (PHF) Aux Earphone Problems TRS guide	No Action
3	10k - 12k	If lower or higher then go to: Hands-Free (PHF) Aux Microphone Problems TRS guide	No Action
4	0.9k - 1.1k	If lower or higher then go to: Hands-Free (PHF) Aux Microphone Problems TRS guide	No Action
5	0.9k - 1.1k	If lower or higher then go to: Hands-Free (PHF) Aux Earphone Problems TRS guide	No Action
6	0.9k - 1.1k	If lower or higher then go to: Hands-Free (PHF) Aux Earphone Problems TRS guide	No Action
7	OL	Not Connected	Not Connected
8	400k - 700k	If lower or higher then go to: Hands-Free (PHF) Connection Problems TRS guide	No Action
9	GND	If lower or higher then go to: Charging Problems TRS guide	No Action
10	35k - OL	If lower or higher then go to: Data Communication Problems TRS guide	No Action
11	250k - 360k	If lower or higher then go to: Data Communication Problems TRS guide	No Action
12	85k - 110k	If lower or higher then go to: Charging Problems TRS guide	No Action

Current Consumption Test

Step 1:

Insert a Local SIM Card and use the phone with the Signalling SW (SSW). Use Dummy Battery connected to Power Supply Channel 1 (VBATT). Instrument settings: Voltage: 3.8 Volt, Limiter 3A.

Note! The Dummy Battery should have approximately 27K Ohm resistance between GND and BDATA.

Measure the current consumption when the Phone is turned off. Take a note of the current consumption at Power Supply Channel 1 (VBATT).

The Current consumption in off mode should be less than 1mA. If more than 1mA go to [Dead Phone Problems part 1 TRS guide](#).

Step 2:

Turn the Phone On:

Measure the deep sleep current max 6mA typical between **0-3mA**. Make sure that the operator is running with deep sleep mode.

Note! This operation can be switched off by operator if network is busy or heavily-loaded.

If the phone is using more than 6mA, then go to EMMA and run Software Update Contents Refresh (SUCR SW).

Step 3 with Fault Trace SW application:

- Flash the phone with ETS SW
- Use Dummy Battery connected to the Power Supply Channel 1 (VBATT)
- Use Fault Trace SW

Connect the:

- Dummy Battery connected to the Power Supply Channel 1 (VBATT): Instrument settings: Voltage: 3.8 Volt, Limiter 3 A
- Connect DCIO/SEPI to the phone: Instrument settings: Voltage: 5 Volt, Limiter 2 A

Perform the following tests:

- **Max TX Power GSM 850 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: GSM 850
Channel: 128
Power Level: 5

- Limits GSM 850 MHz
- Transmitter Current Limits: **320mA**
- **Tolerance: ±20%**

- **Max TX Power GSM 900 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: GSM 900
Channel: 1
Power Level: 5

Limits GSM 900 MHz

- Transmitter Current Limits: **120mA**
- **Tolerance: ±20%**

- **Max TX Power DCS 1800 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: DCS 1800
Channel: 512
Power Level: 0

Limits DCS 1800 MHz

- Transmitter Current Limits: **225mA**
- **Tolerance: ±20%**

- **Max TX Power PCS 1900 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: PCS 1900
Channel: 512
Power Level: 0

Limits PCS 1900 MHz

- Transmitter Current Limits: **230mA**
- **Tolerance: ±20%**

- **Max TX Power WCDMA BAND I**

Note! Valid only for the W995 with WCDMA BAND I support.

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

Limits WCDMA BAND I

- Transmitter Current Limits: **750mA**
- **Tolerance: ±20%**

- **Max TX Power WCDMA BAND II**

Note! Valid only for the W995 with WCDMA BAND II support.

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

Limits WCDMA BAND I

- Transmitter Current Limits: **500mA**
- **Tolerance: ±20%**

- **Max TX Power WCDMA BAND V**

Note! Valid only for the W995 with WCDMA BAND V support.

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

Limits WCDMA BAND I

- Transmitter current: **530mA**
- **Tolerance: ±20%**

- **Max TX Power WCDMA BAND VIII**

Note! Valid only for the W995 with WCDMA BAND VIII support.

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

Limits WCDMA BAND I

- Transmitter current: **660mA**
- **Tolerance: ±20%**

If the current consumption is out of the test limits then try to solve the problem by running SERP Calibration.

If there are still problems with the current consumption then go to the following TRS guides:

**GSM Network problems,
WCDMA I, II, V Network Problems or
WCDMA VIII Network Problems**

If the current consumption is within the test limits then go to: **Charging Test.**

Backup Capacitor Test

To perform this test use:

- Phone with the ETS SW
- Power Supply Channel 1 VBATT: Instrument settings: Voltage: 3.8V, Limiter: 2A
- Power Supply Channel 2 DCIO/SEPI: Instrument settings Voltage: 5V, Limiter: 2A

This test should be performed in 3 steps:

Step1:

Measure the voltage at the Back up capacitor by using **Fault Trace SW- Logic - ADC Values – Read ADC Value** (Reading 1).

Step2:

This step should be made **30 seconds** after Step 1. Measure the voltage at the Backup capacitor by using **Fault Trace SW - Logic – ADC Values - ADC Channels – Read ADC Value** (Reading 2).

Step3:

Compare the difference between Reading 1 and Reading 2 with the reference table below. If the Reading 1 value is between 50 and 680 go to Interval 1, if between 681 and 800 go to Interval 2, if between 801 and 880 go to Interval 3 and compare with the Reading 2 – Reading 1 Min and Max Limits.

Reference Table:

	Min	Max	Unit
Absolute readout Reading 1	50	880	Dec

Reading 1 (Dec)	Reading 2 – Reading 1 (Dec)	
	Min	Max
Interval 1 (50 – 680)	20	210
Interval 2 (681 – 800)	5	30
Interval 3 (801 – 880)	0	10

Note! The upper table contains the absolute limits for the readouts. The lower table contains the allowed delta between the first and the second readout, separated in time with 30 seconds.

Note! If the readings are out of limits then **SL 5 replace C2233** (Backup Capacitor) If the problem persists then **SL 5 Replace N2000 SL 4 Escalate**.

Charging Test

To perform this test use:

- Phone with the Signalling SW (SSW)
- Dummy Battery connected to Power Supply Channel 1 (VBATT)
Note! The Dummy Battery should have approximately 27K Ohm resistance between GND and BDATA.
- Power Supply Channel 1 (VBATT)
Instrument settings:
Voltage: from 3.0 Volt to 4.2 Volt, according to VBATT row in the Reference Table.
Limiter: 2A
- Power Supply Channel 2 (DCIO/SEPI)
Instrument settings:
Voltage: 5V
Limiter: 2A

Test instructions:

- Disconnect the DCIO/SEPI Cable between each measurement and wait for phone to shut down when changing VBATT voltage.
- Take a note of the current measurements at Power Supply Channel 2 DCIO/SEPI and Display Charging Indicator X seconds after DCIO/SEPI cable has been inserted according to the Test Time row in the reference table below.
- Compare the test results with the reference table below, tolerance +/-20%.

Reference Table

VBATT x Volt	3.0v	3.1v	3.2v	3.3v	3.4v	3.5v	3.6v	3.7v	3.8v	3.9v	4.0v	4.1v	4.2v
Test Time x sec.	15s	15s	15s	25s	25s	25s	30s	30s	30s	30s	30s	30s	45s
DCIO/SEPI Current mA	250mA	250mA	250mA	500mA	600mA	700mA	900mA	900mA	900mA	900mA	900mA	850mA	0mA
Display indicate charging	Nothing	Nothing	Nothing	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Fully Charged

Note! The Power Supply Channel 1 (VBATT) must allow reverse current.

If the charging current is **NOT** equal to the reference table then go to: [Charging Problems TRS Guide](#)

If the charging current is equal to the reference table then insert the normal battery and test the charging current to verify that the phone battery is working properly.

Measure the voltage at the battery to define the current level.

If the battery is receiving the right current the phone and the battery are working properly.

ASIC Revision Test

Note! The Keypad Scan Test must be Deactivated during this test.

Purpose:

- Verify that the ASIC is correctly mounted, the communication works and that the revision is correct.

The tested ASICs are:

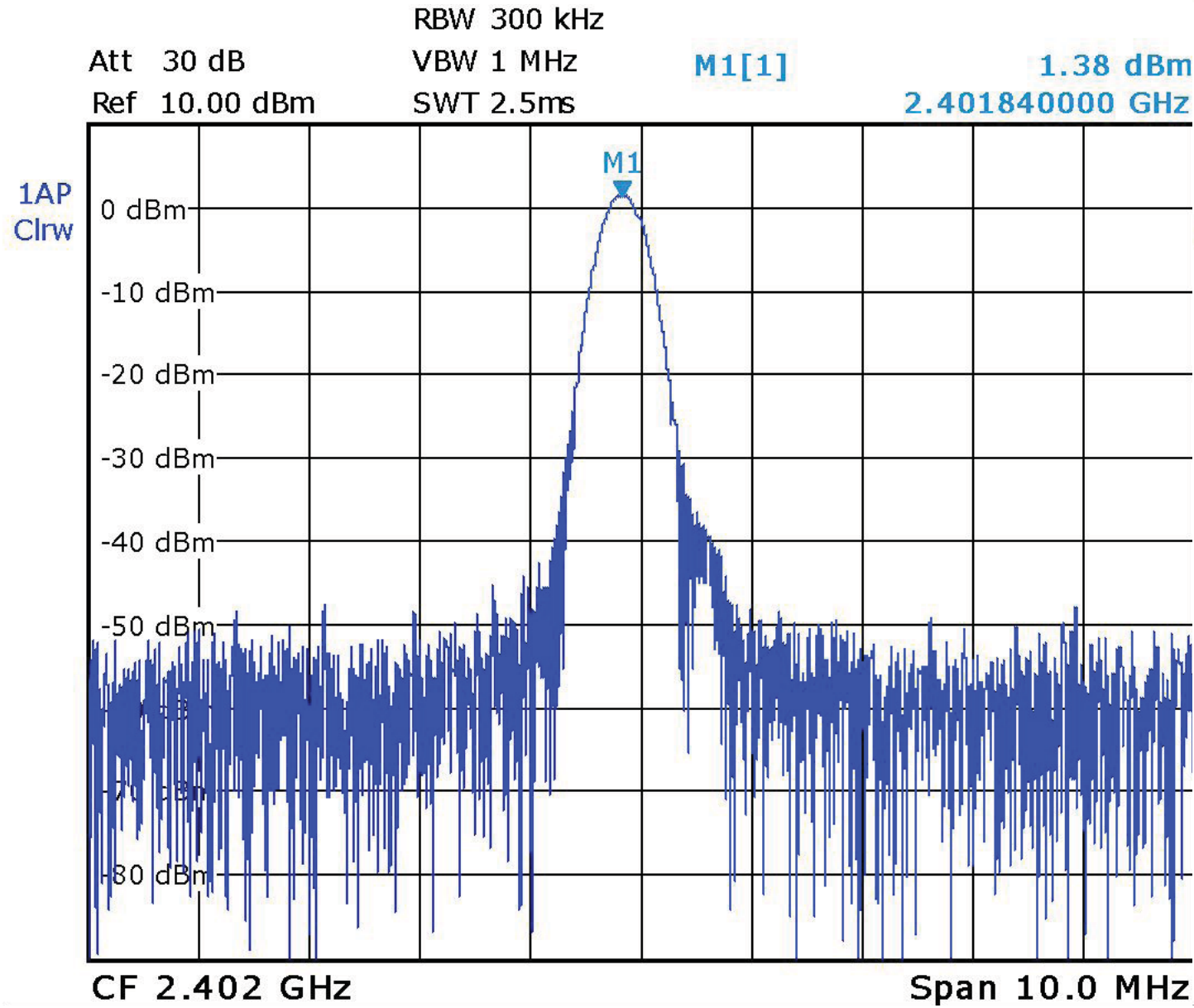
- N2010 (Kajsa)
- N2000 (Vera)
- N1300 (Bluetooth and FM Radio ASIC)
- N2411 (Accelerometer)
- N1400 (A-GPS Module)

To perform this test use:

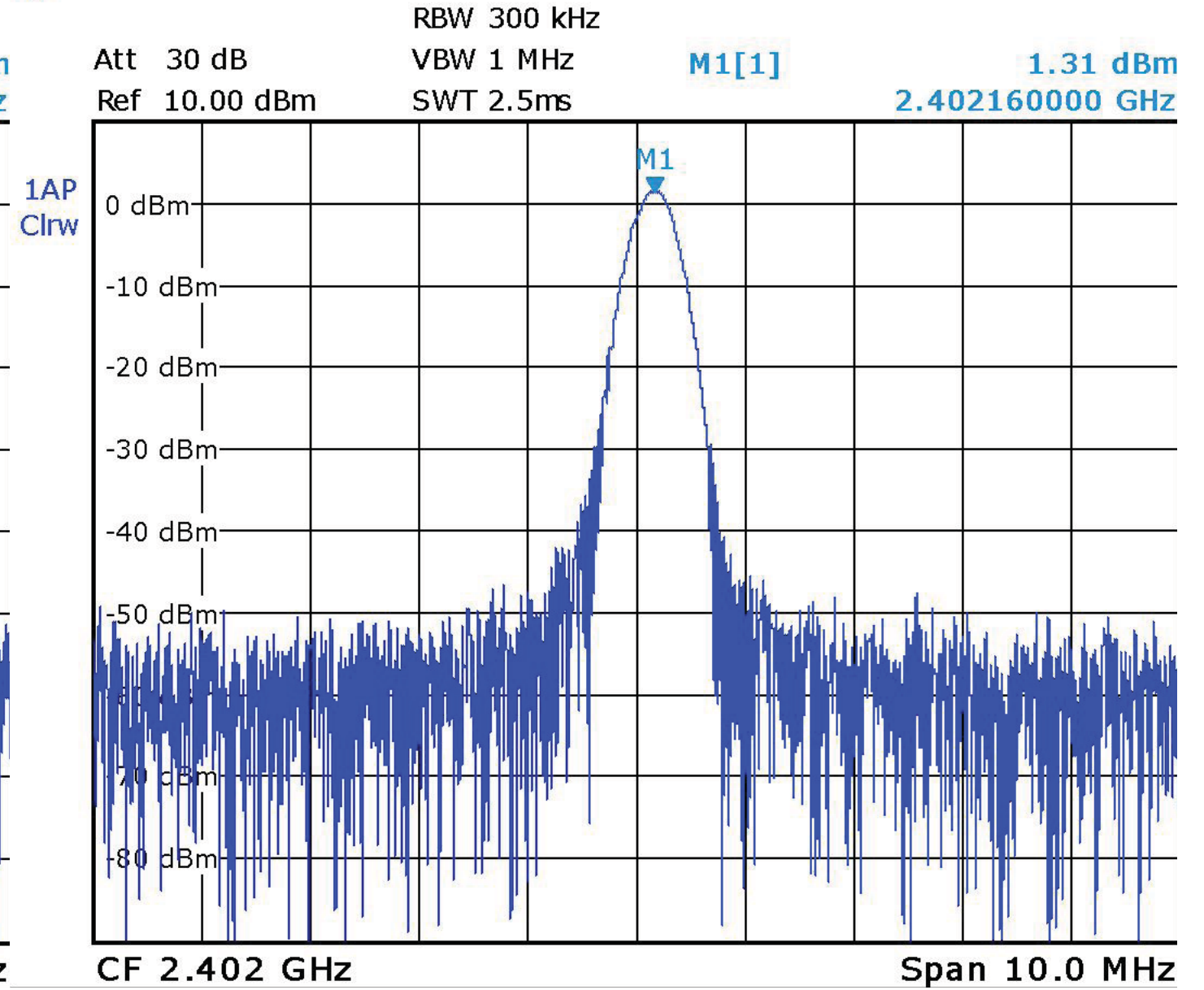
- Phone with the ETS SW
- TRS Fixture
- Power Supply Channel 1 VBATT (Voltage: 3.8V, Limiter: 2A)
- Power supply Channel 2 DCIO/SEPI (Voltage: 5V, Limiter: 2A)
- Fault Trace SW and go to: General – Asic Revisions – Read All

Reference Table:

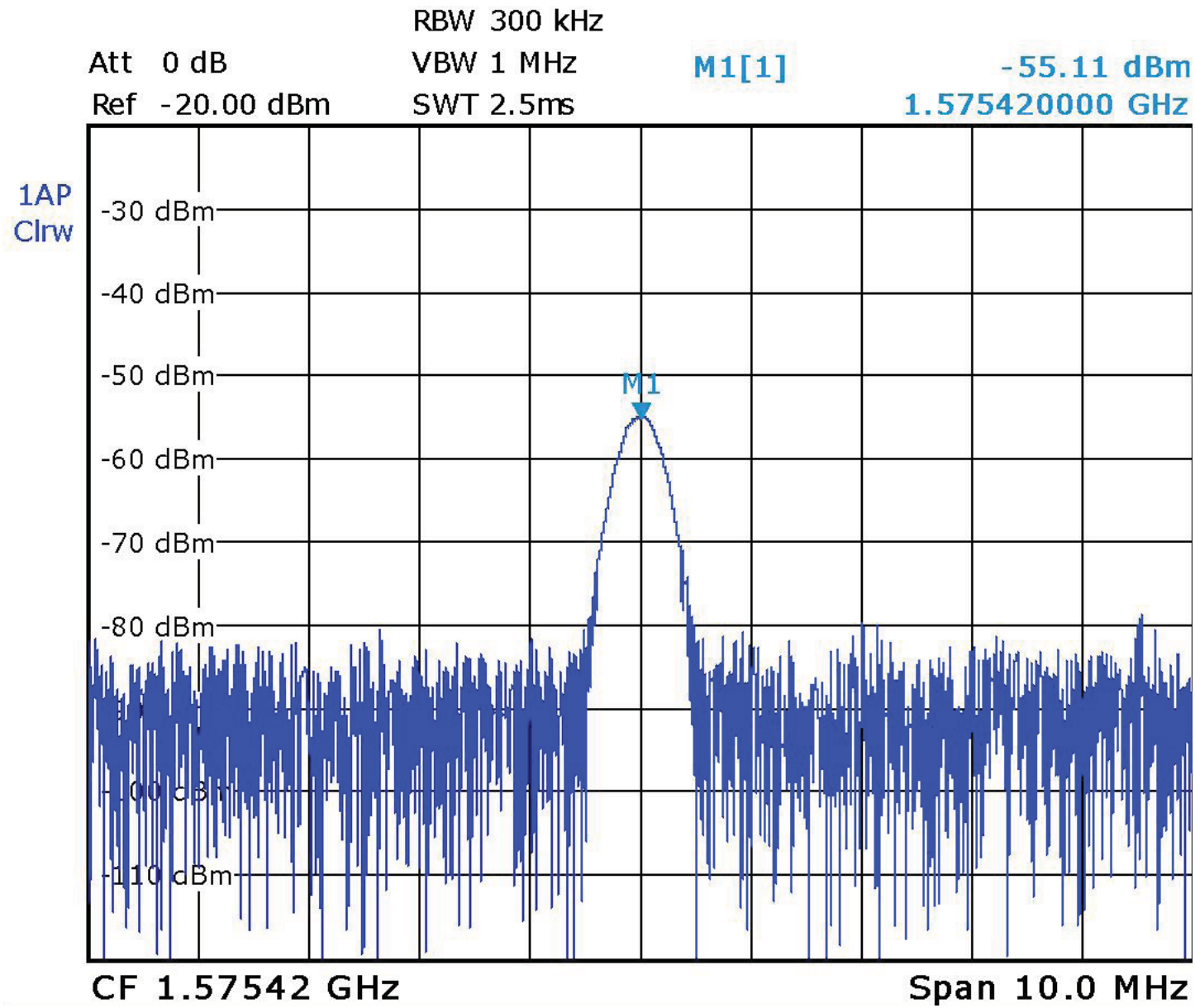
ASIC	Part number	Description	Return value (hex)
N2010	1210-4190	CPU (Kajsa)	0xE9
N2000	1202-0639	Power Management (Vera)	0xC8
N1300	1200-9840	Bluetooth:	
		Firmware Revision	0x5,0x3
		Chip ID	0x0,0x0,0x0,0x0 Will always return 0 on STLC because Chip ID is not supported.
N2411	1204-5837	Accelerometer	0x3b
N1400	1200-0700	A-GPS Module	254,0,253,192,0,242,113,9,16,252
N1300	1200-9840	FM Radio	When FM Radio is On : 0x1253 When FM Radio is Off : 0x1200



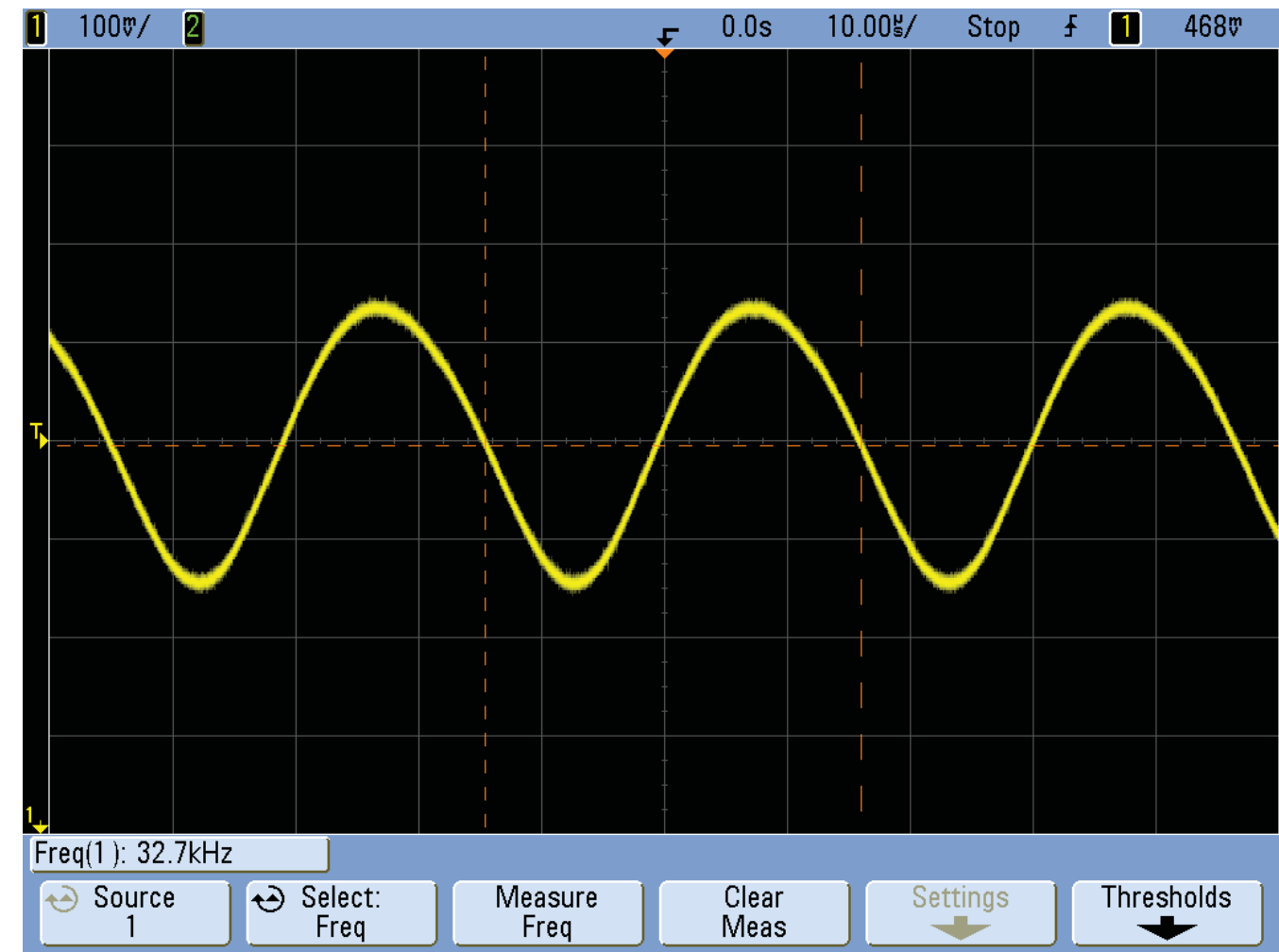
Blt MaxPwr MOD 0



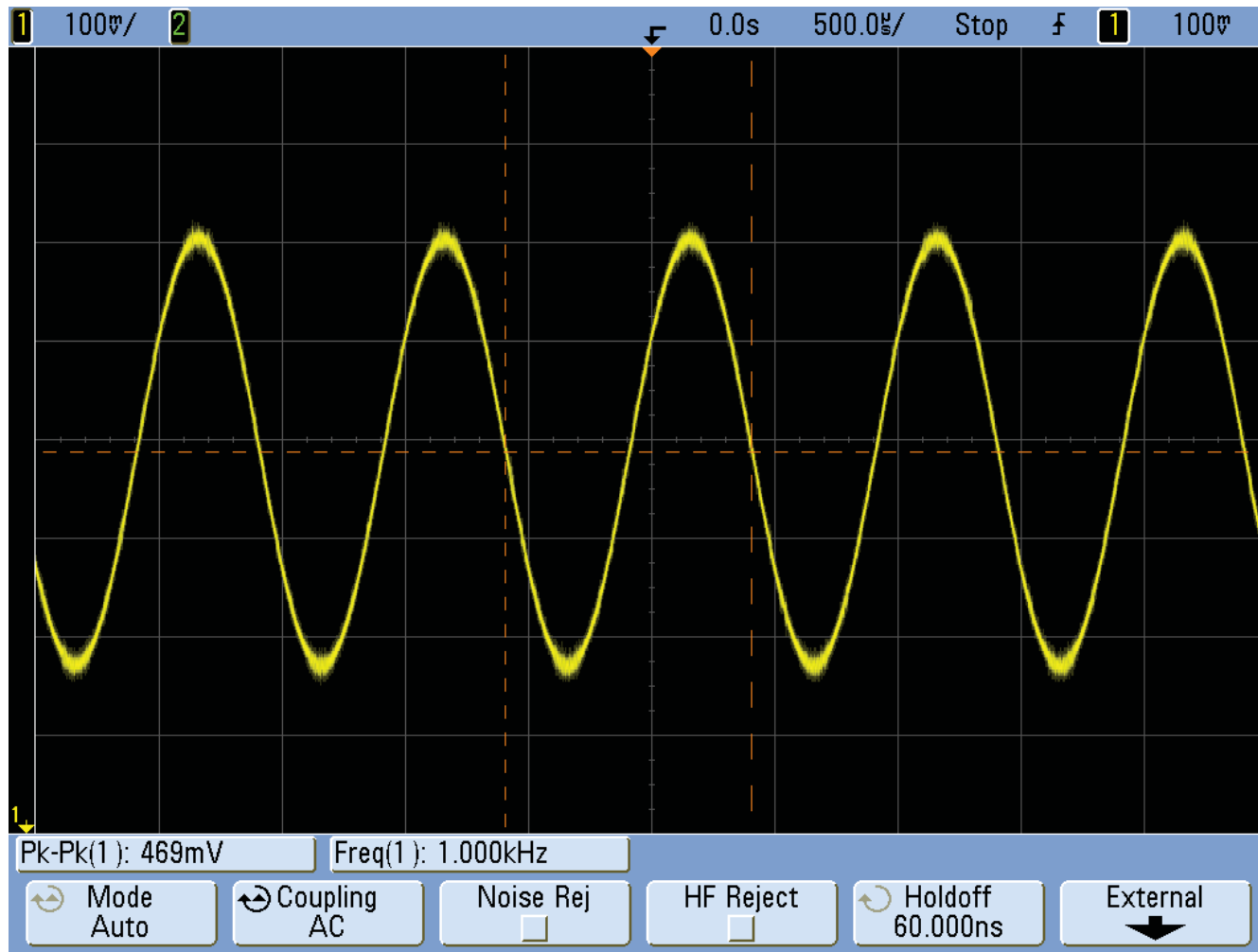
Blt MaxPwr MOD 1



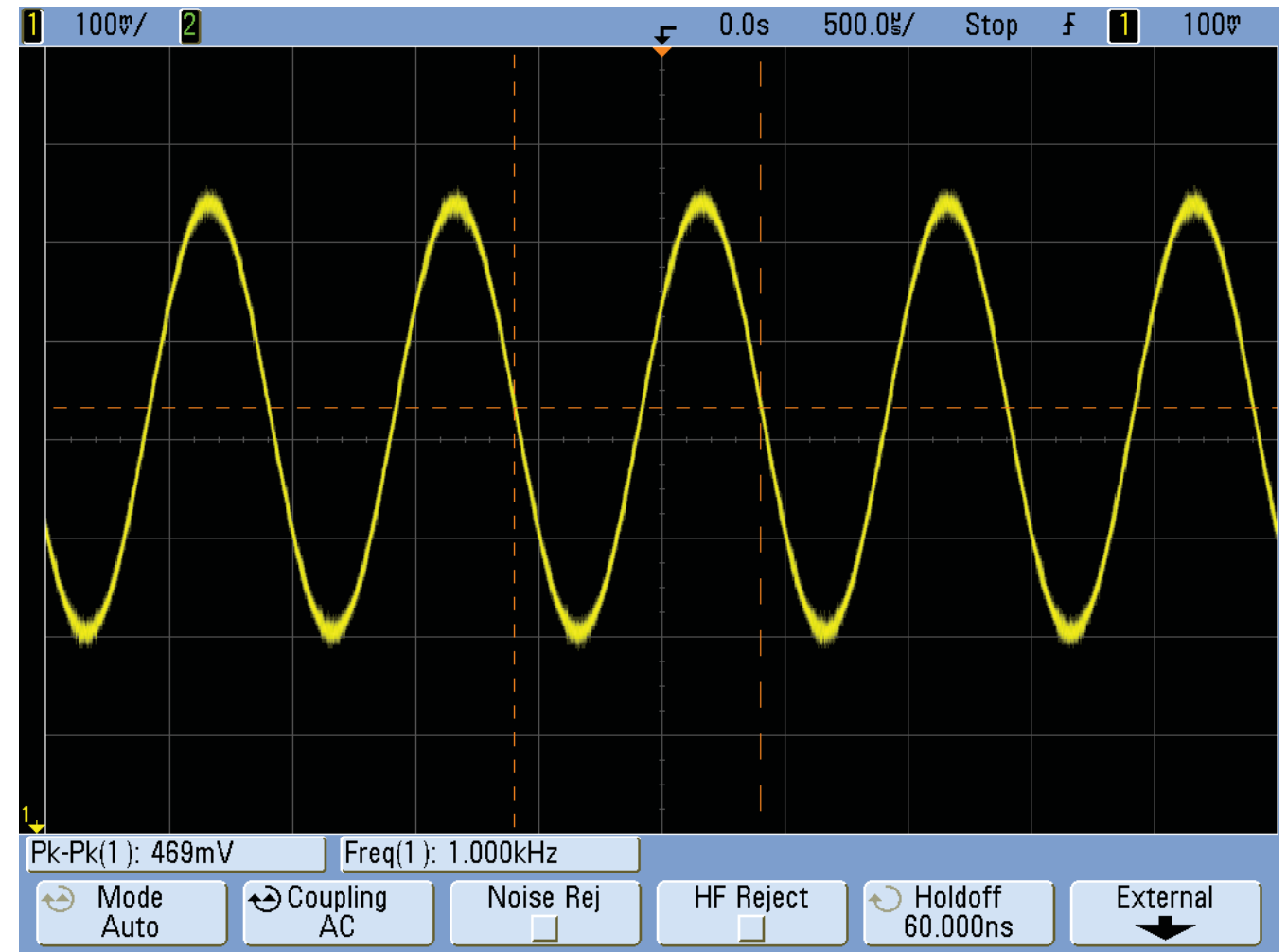
MP 40 - C1402



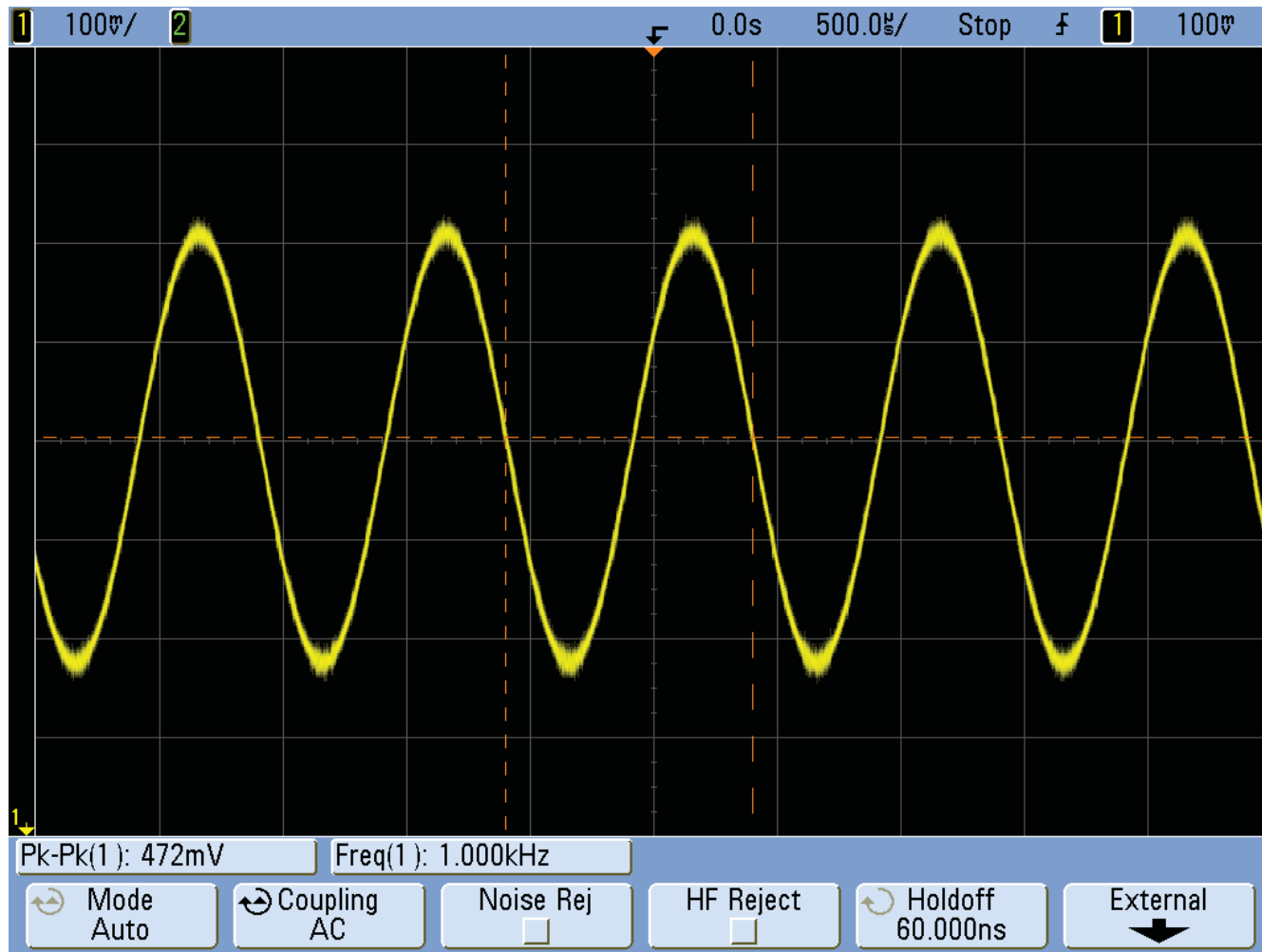
MP 81 - C2101 (32.7 kHz)



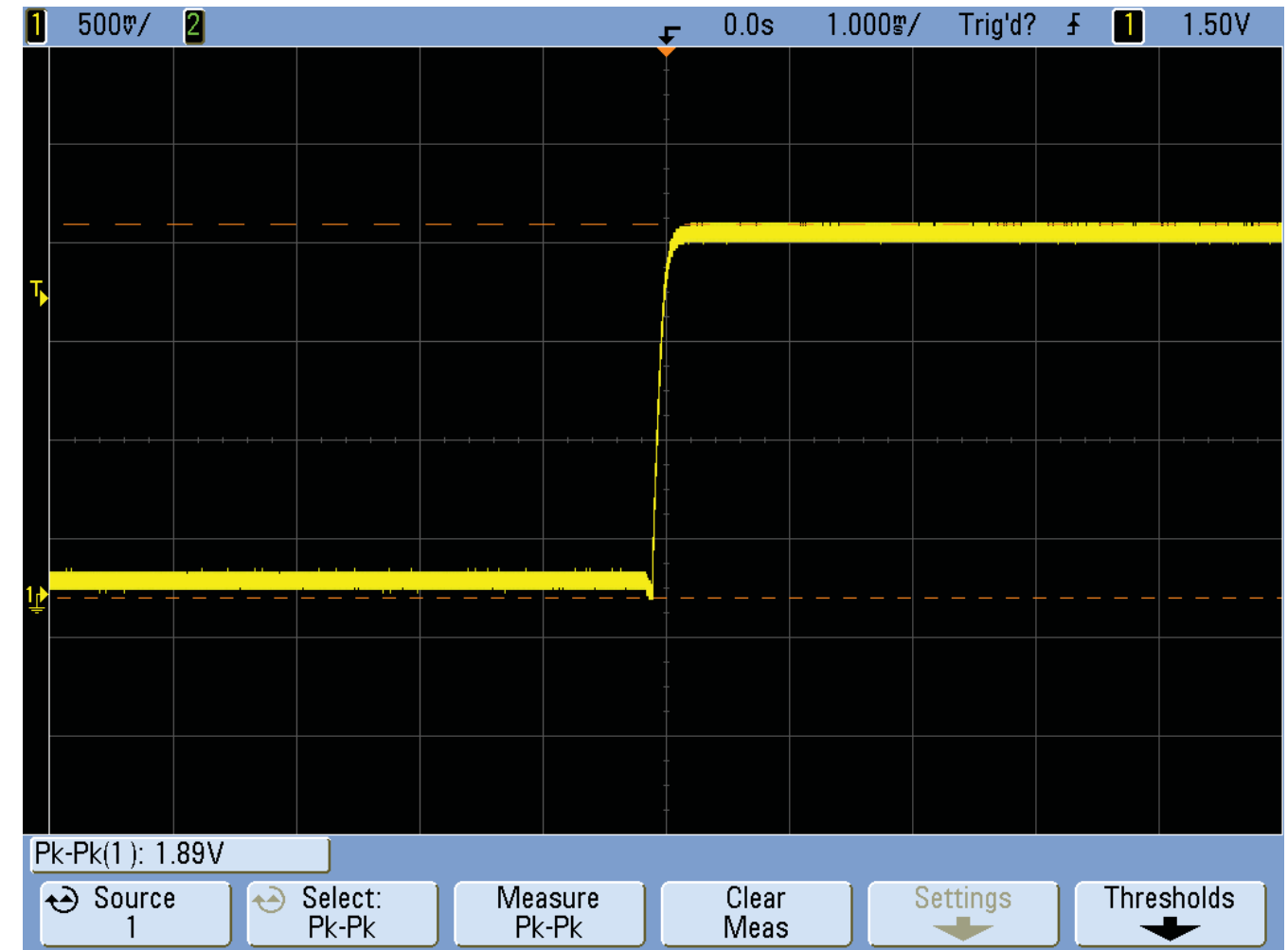
MP 34 - C3137 (BEARP_OUT)



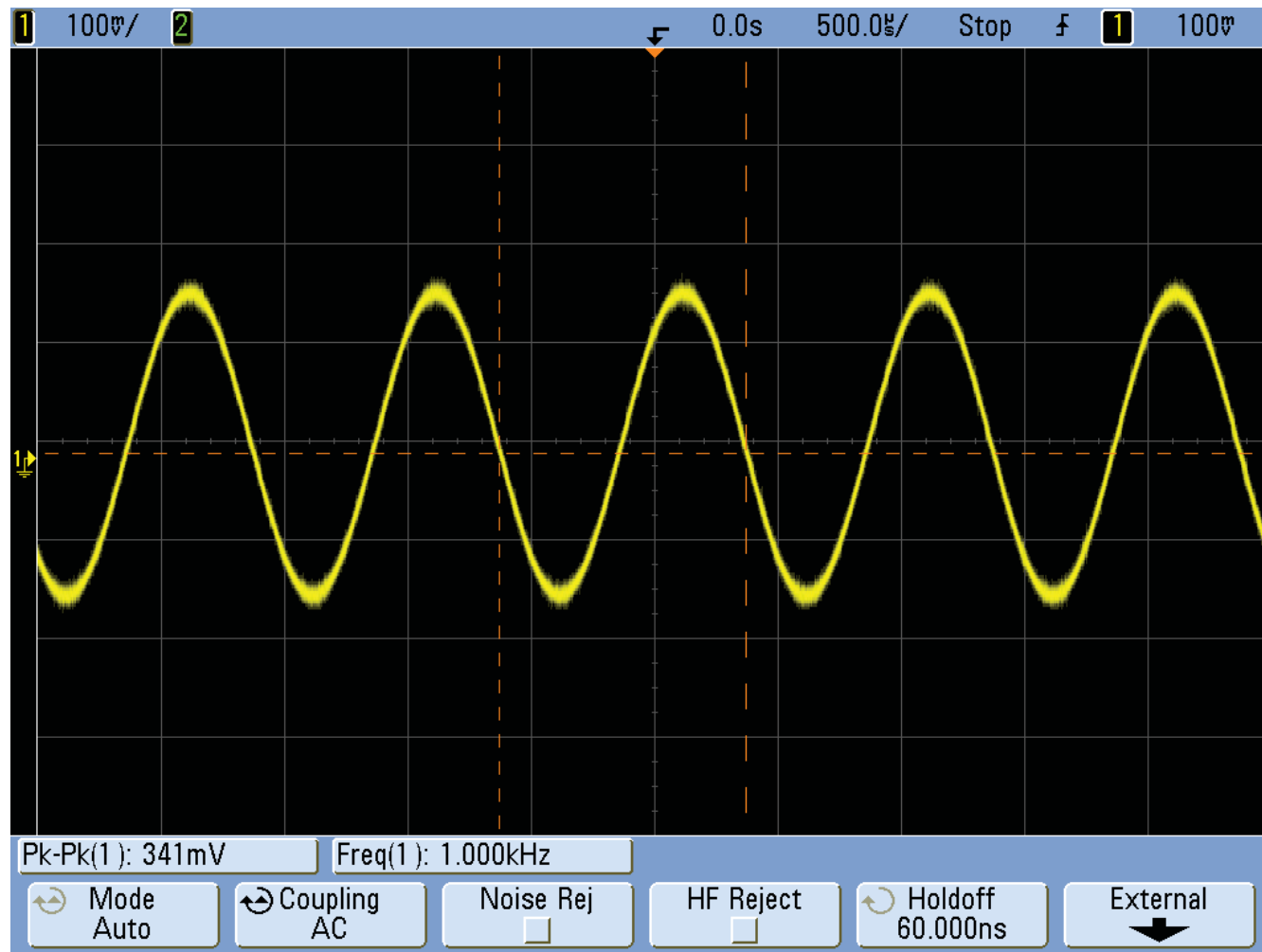
MP 7 - C3148 (BEARN_OUT)



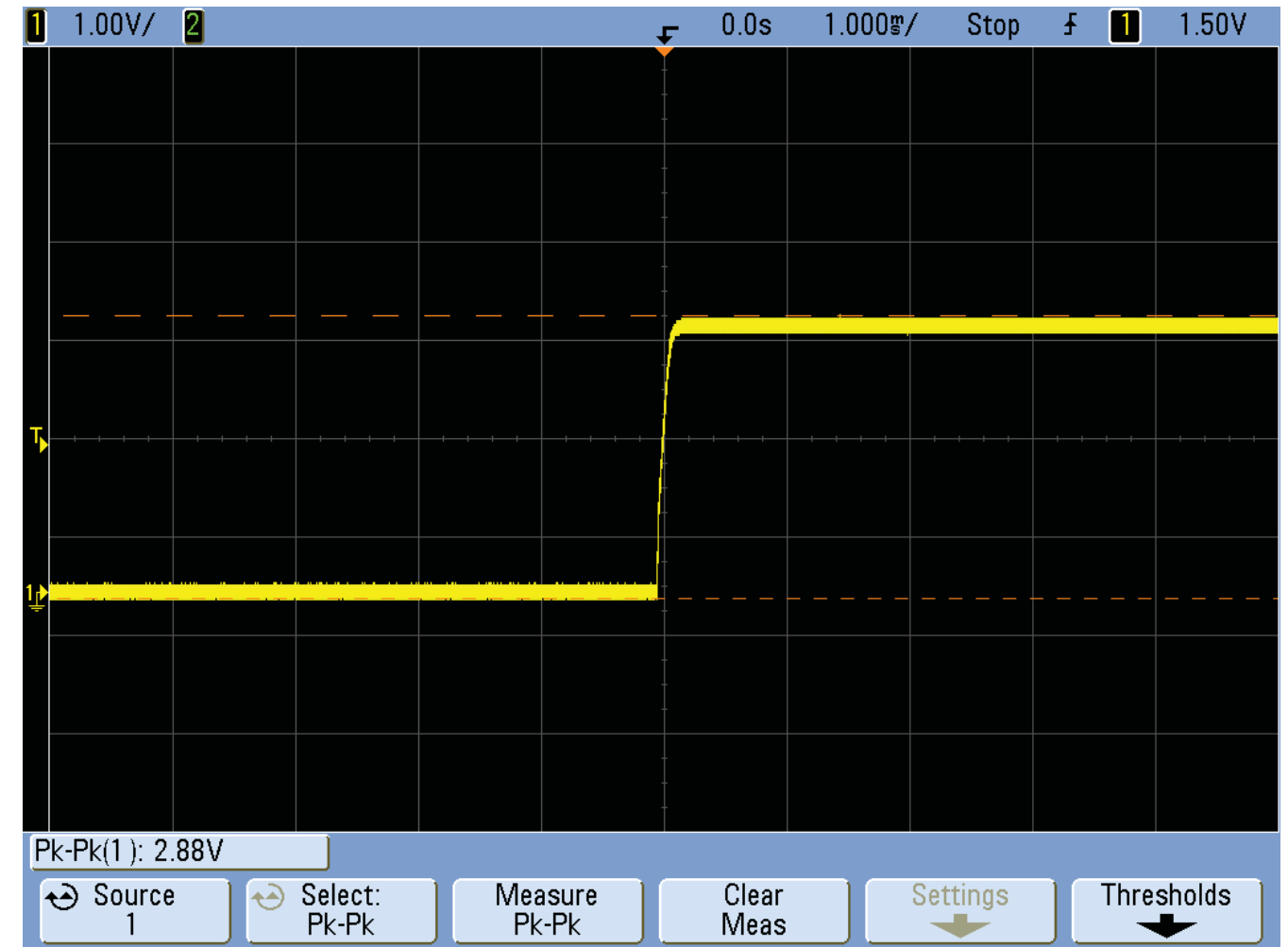
MP 31 - C3149 (AUXO2_OUT) and MP 33 - C3150 (AUXO1_OUT)



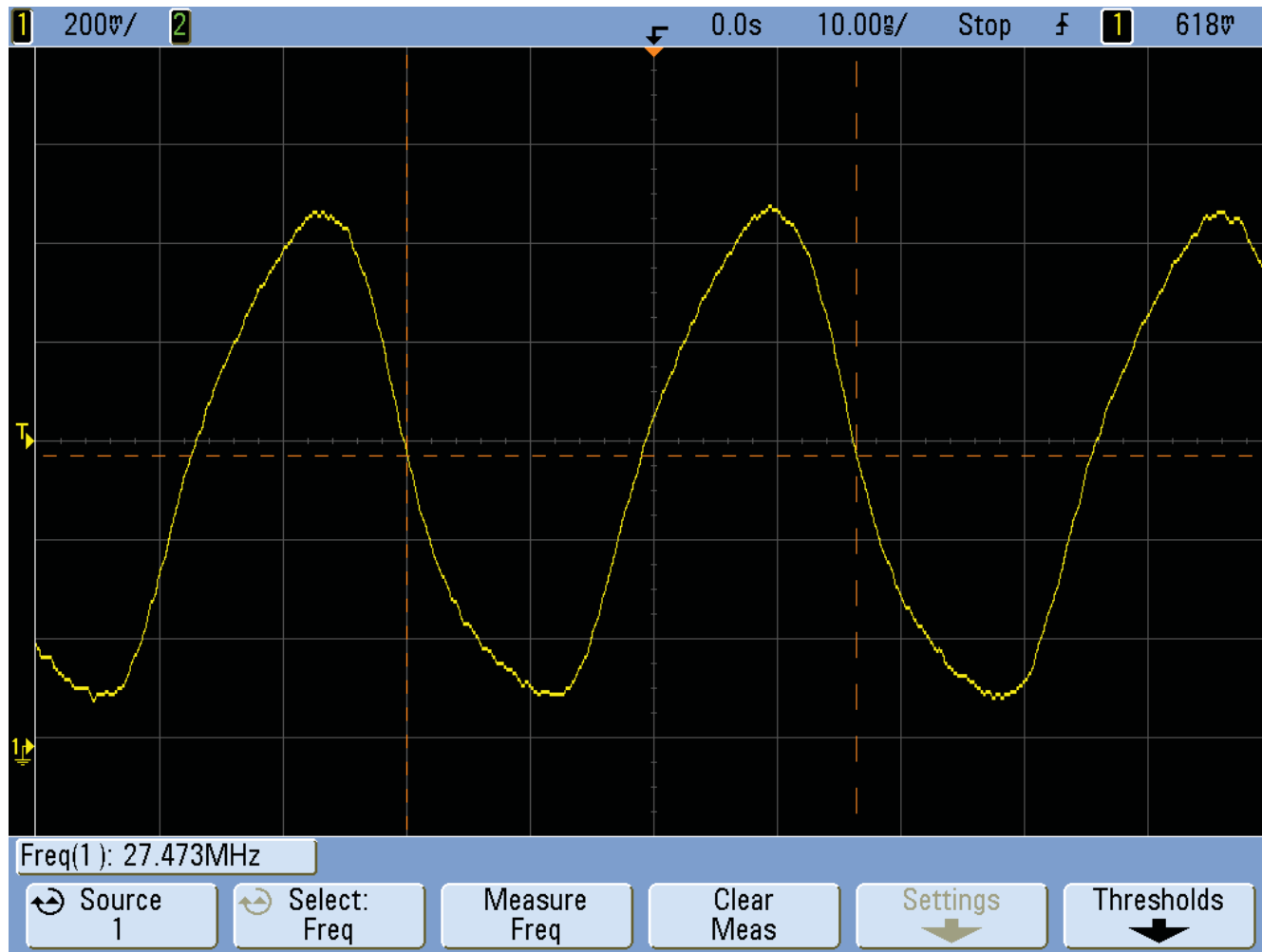
MP 77 - C4215 (OPTO_EN)



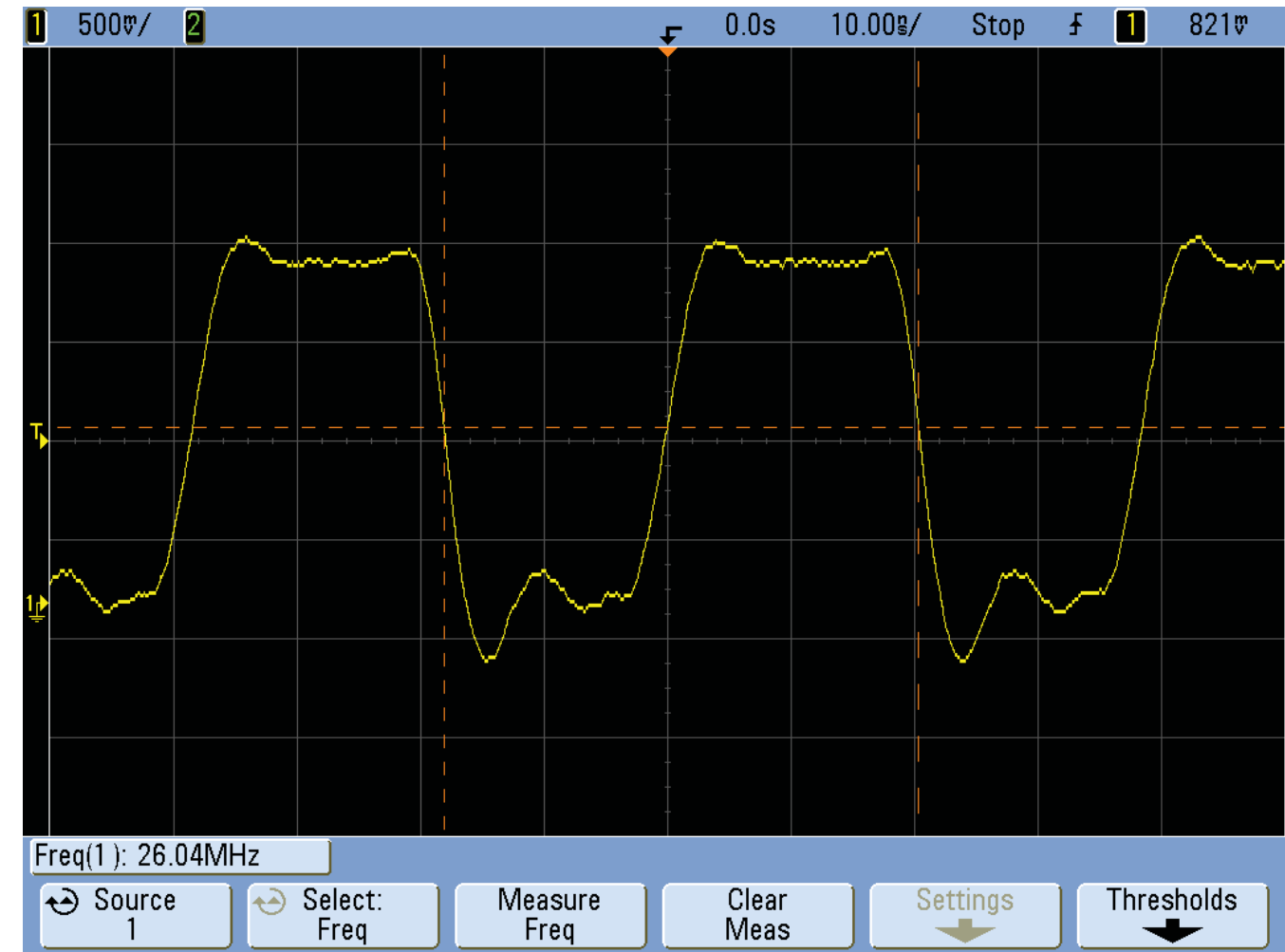
MP 97 - L2403 (SPEAKER_L) and MP 99 - L2404 (SPEAKER_R)



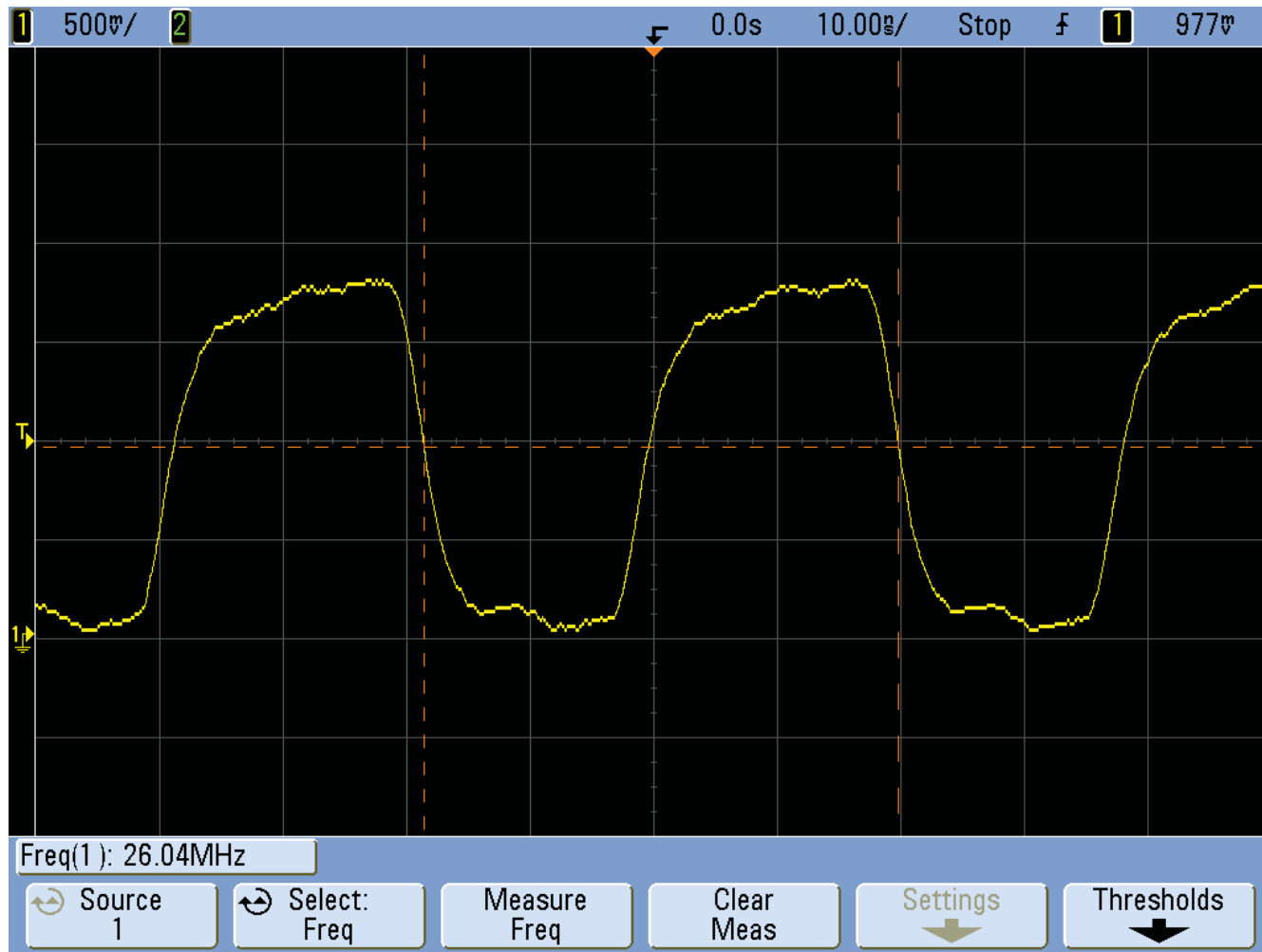
MP 88 - L4201 (VIBR_OUT)



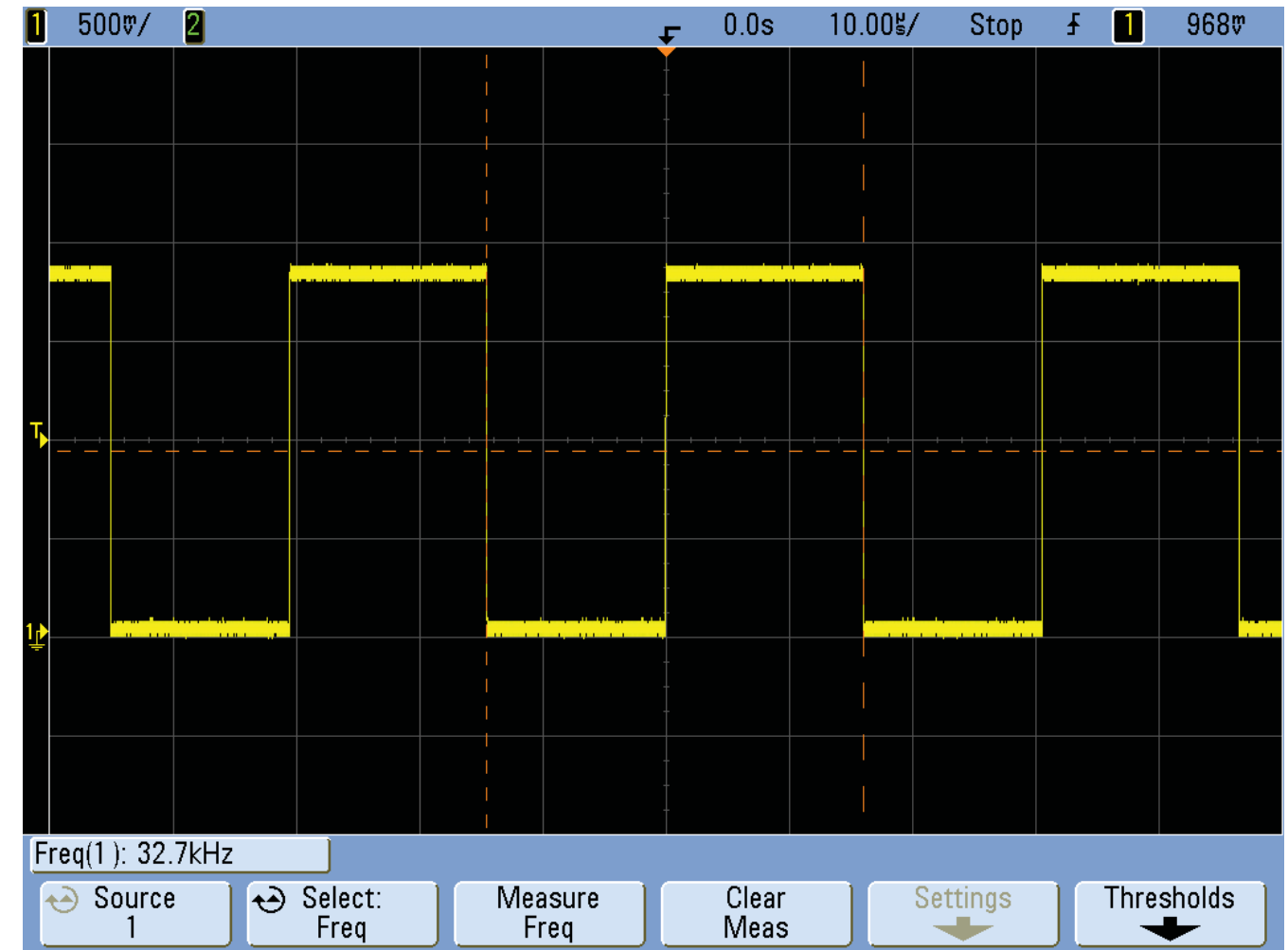
MP 48 - R1404 (27 MHz)



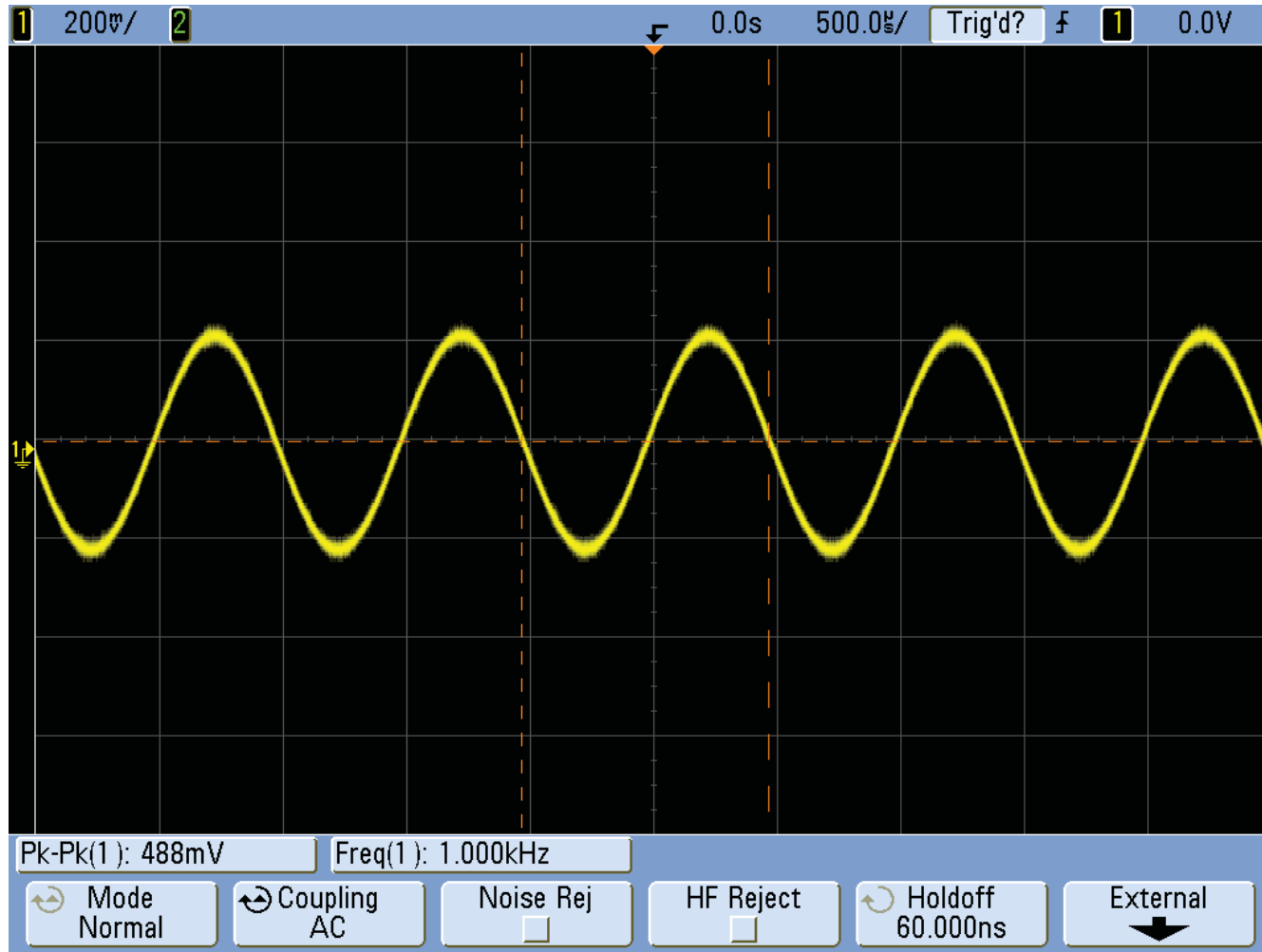
MP 49 - R1408 (26 MHz AGPS_CLK)



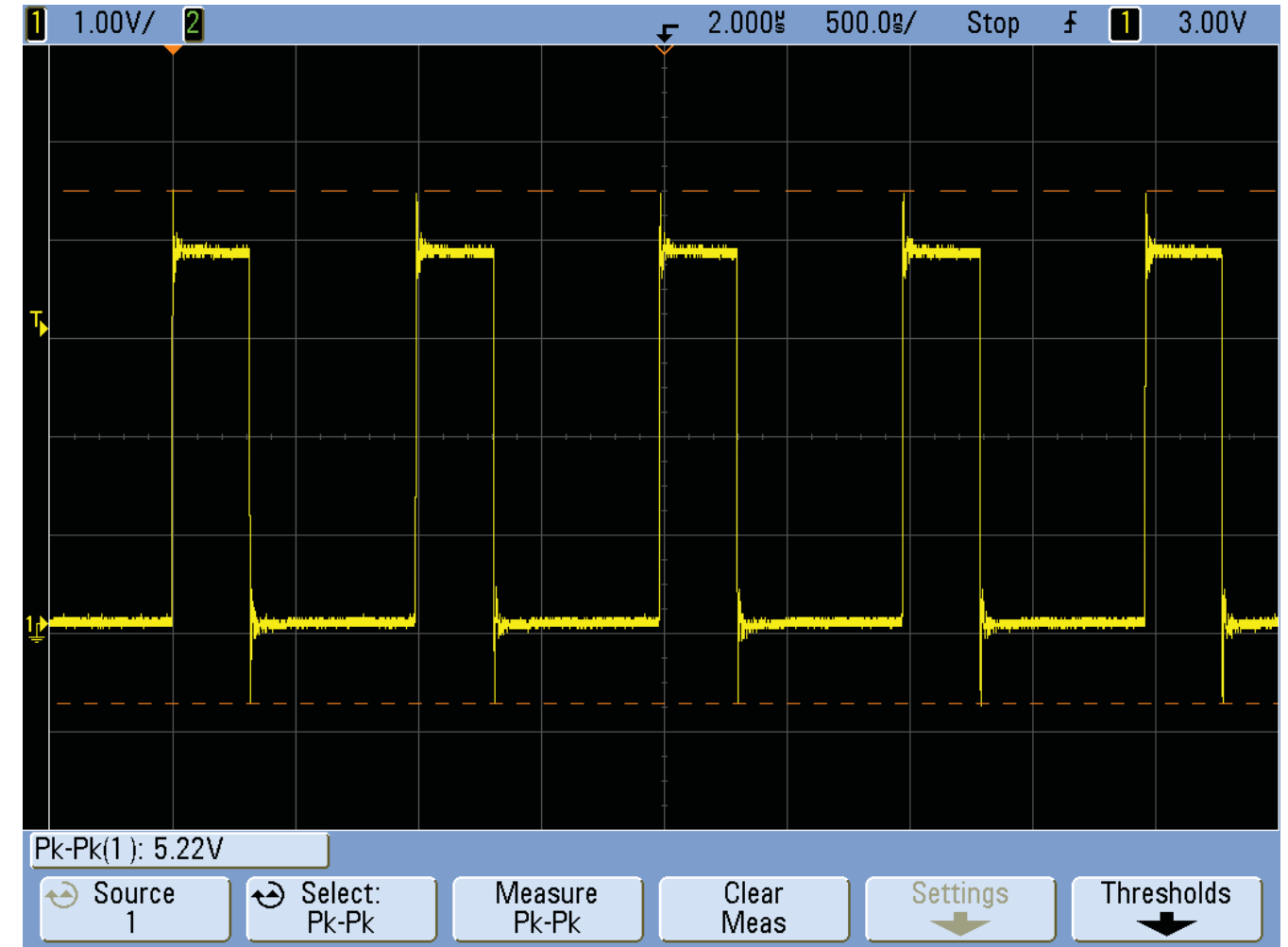
MP 80 -R2103 (26 MHz MCLK)



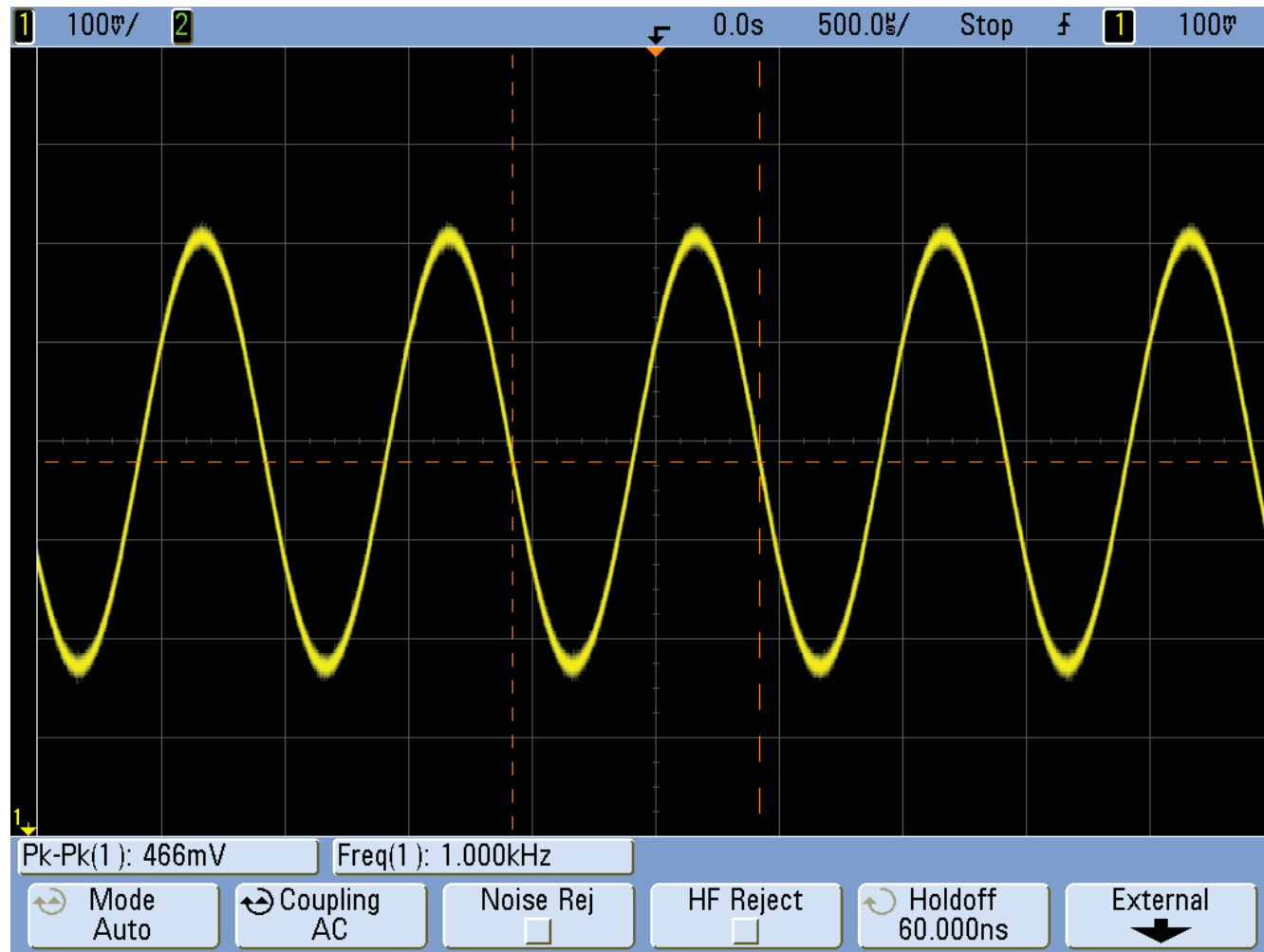
MP 80 - R2103 (32.7 kHz RTCCLK)



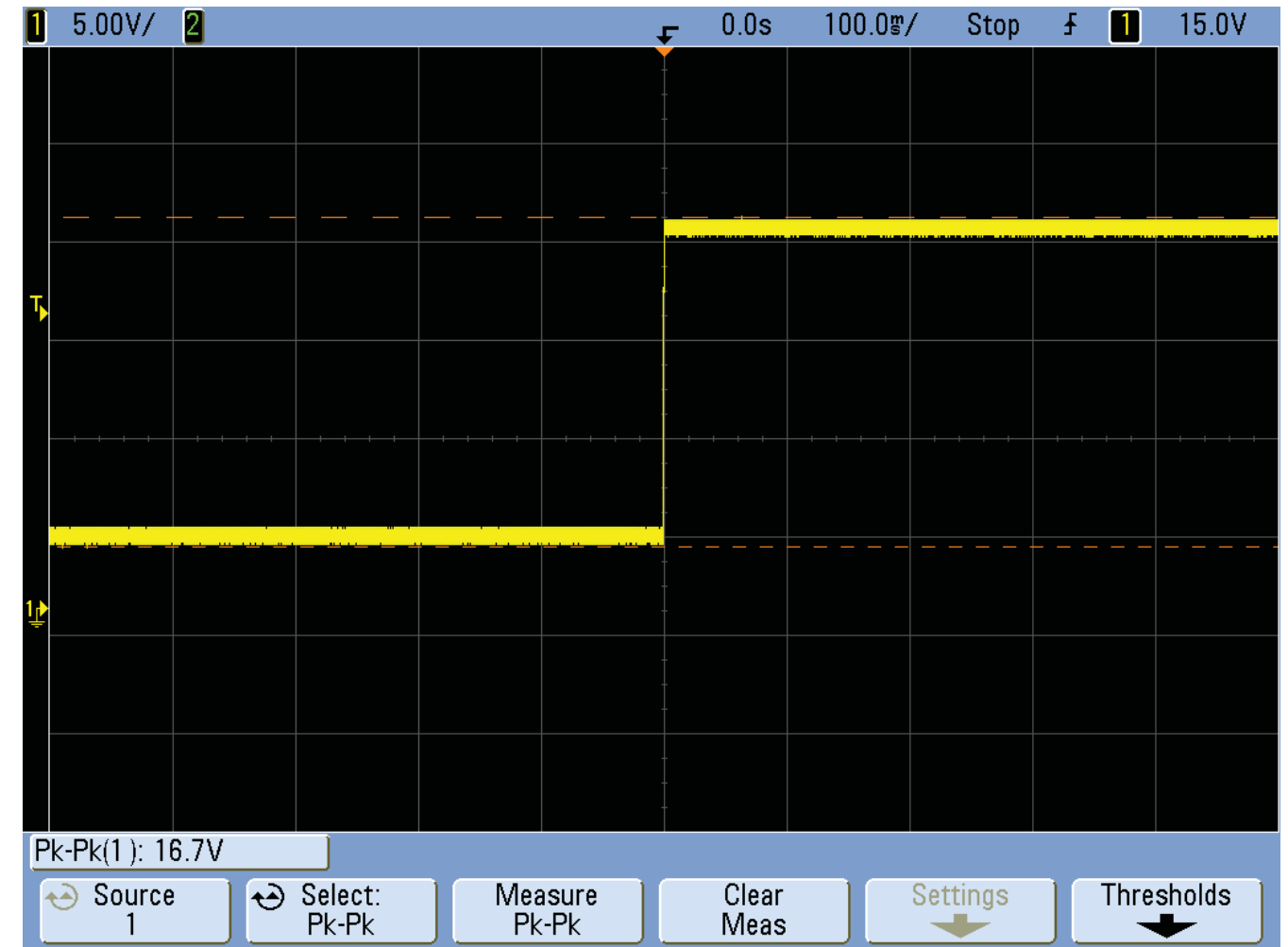
MP 39 - R3124 and MP 38 - R3127



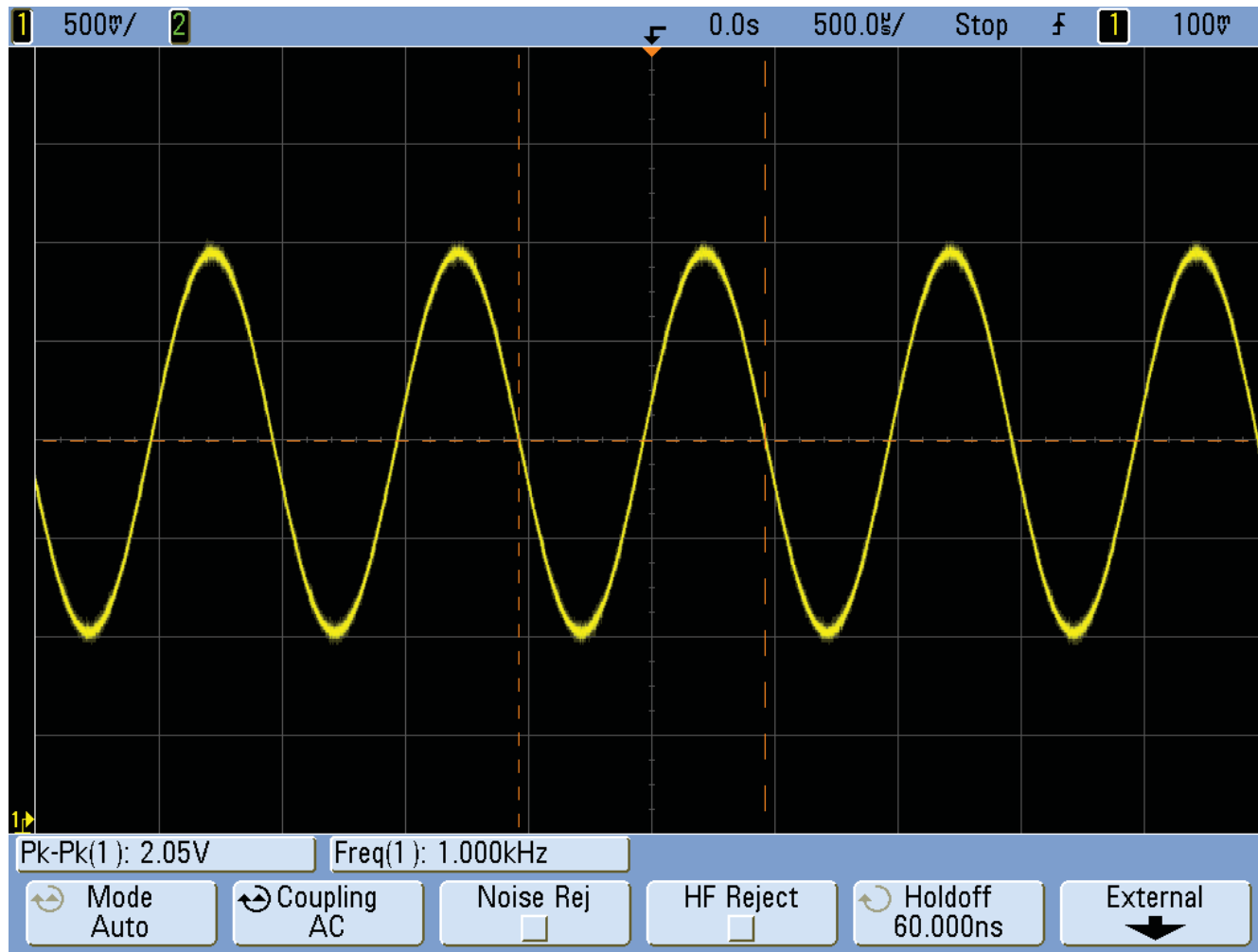
MP 43 - R4200



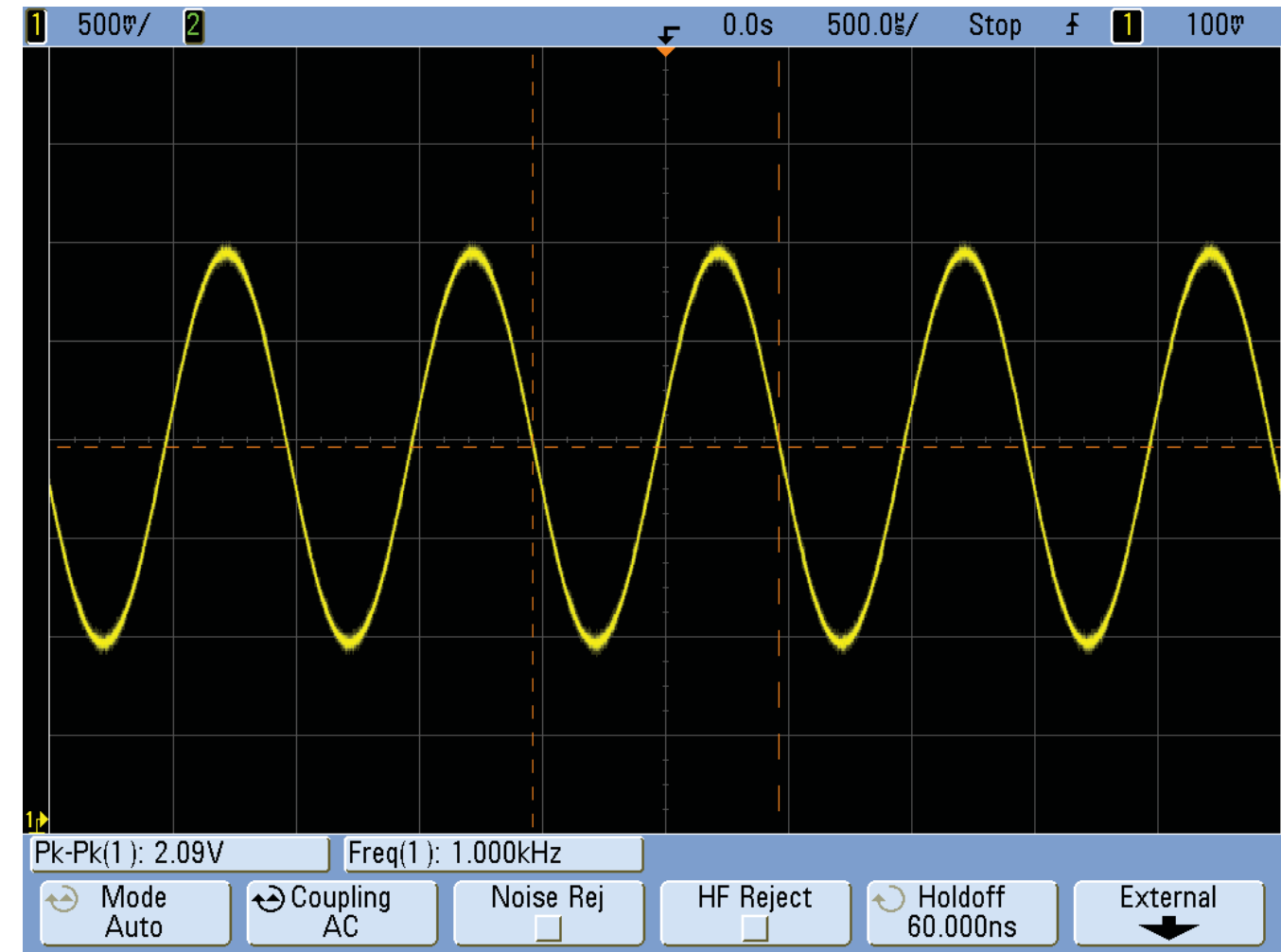
MP 105 - TP3104 (SPKRP_OUT and MP 109 - TP3105 (SPKRN_OUT)



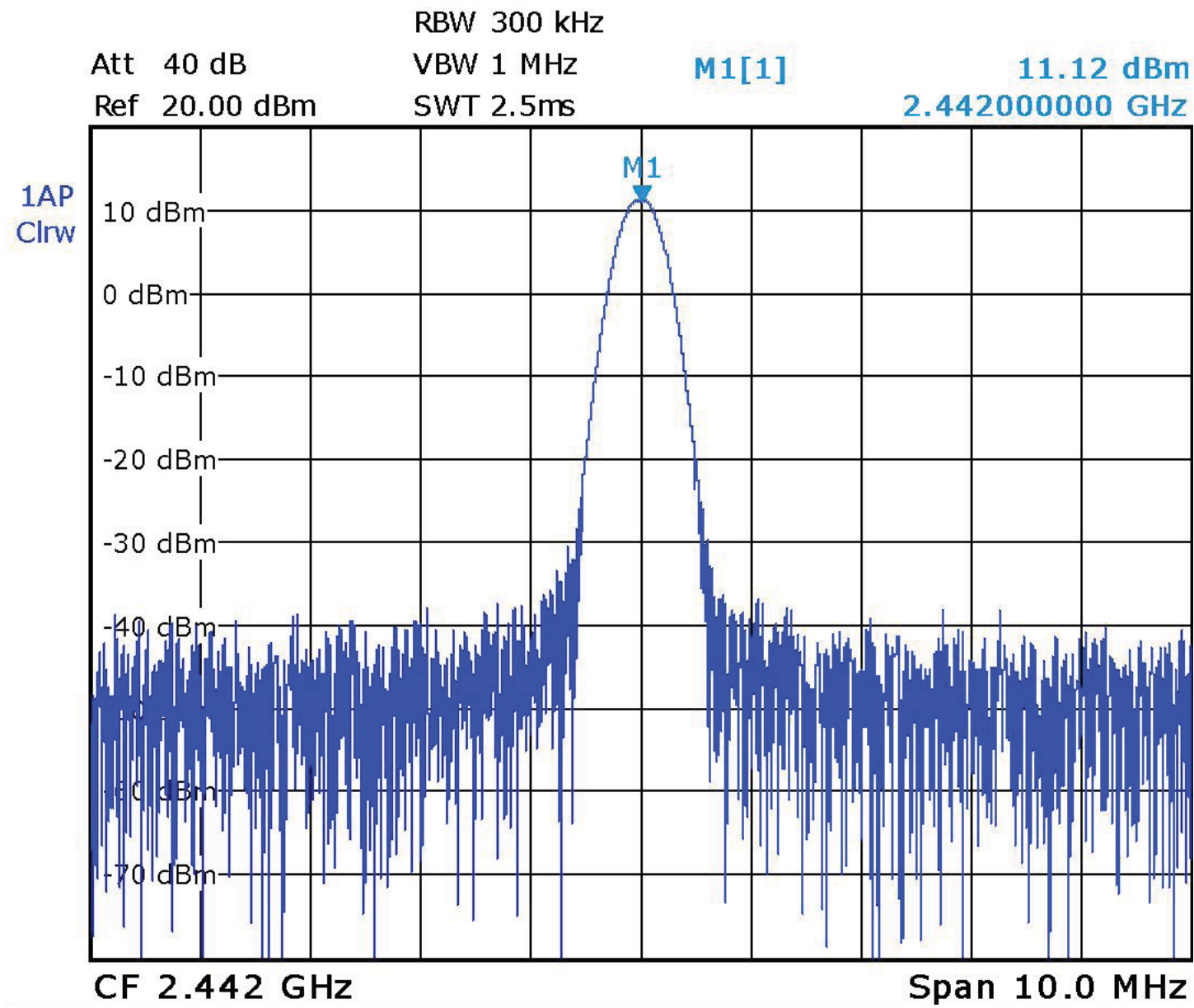
MP 111 - TP4201



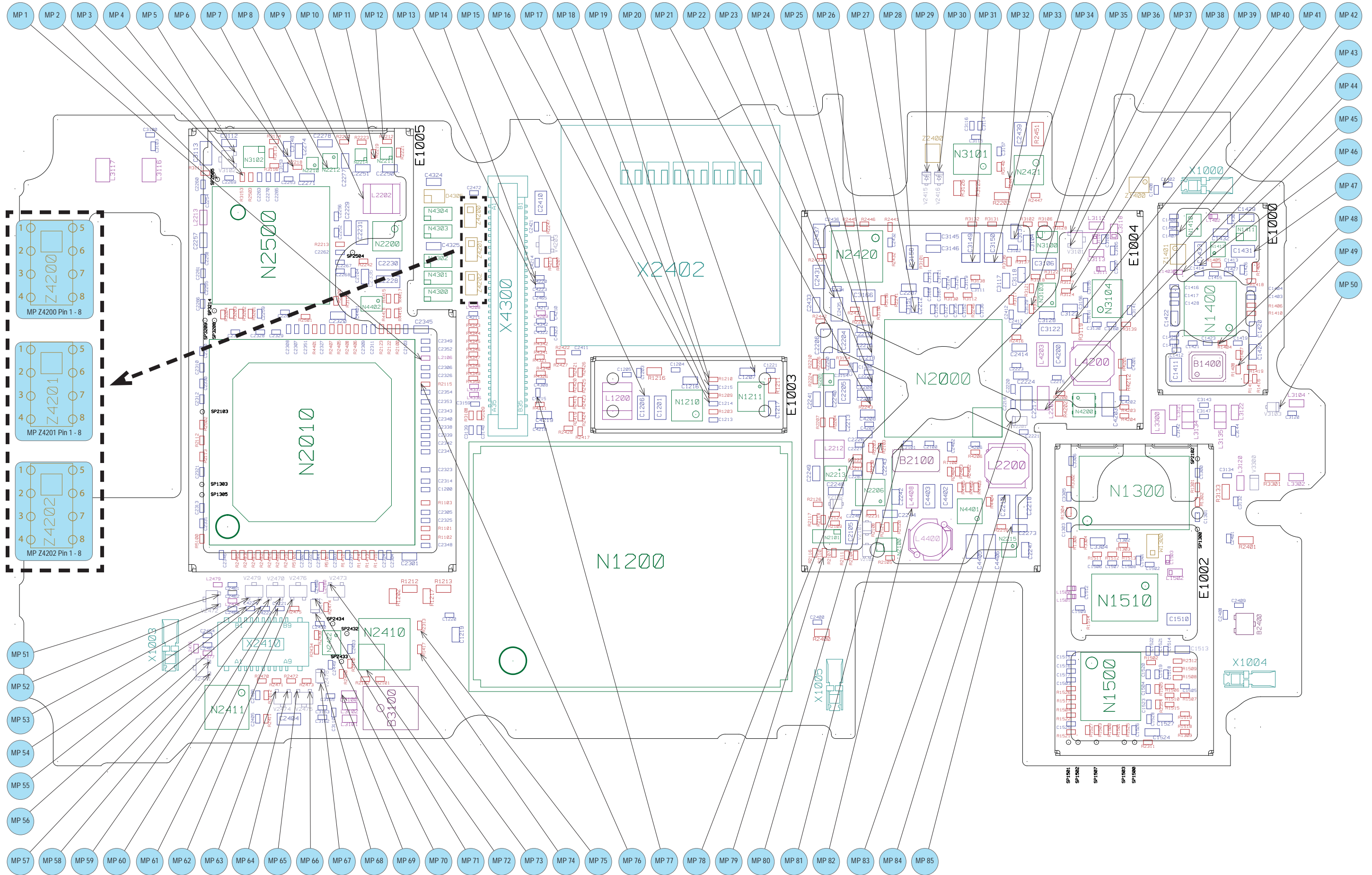
MP 36 - V3101_Pin C1 and MP 37 - V3101_Pin C2



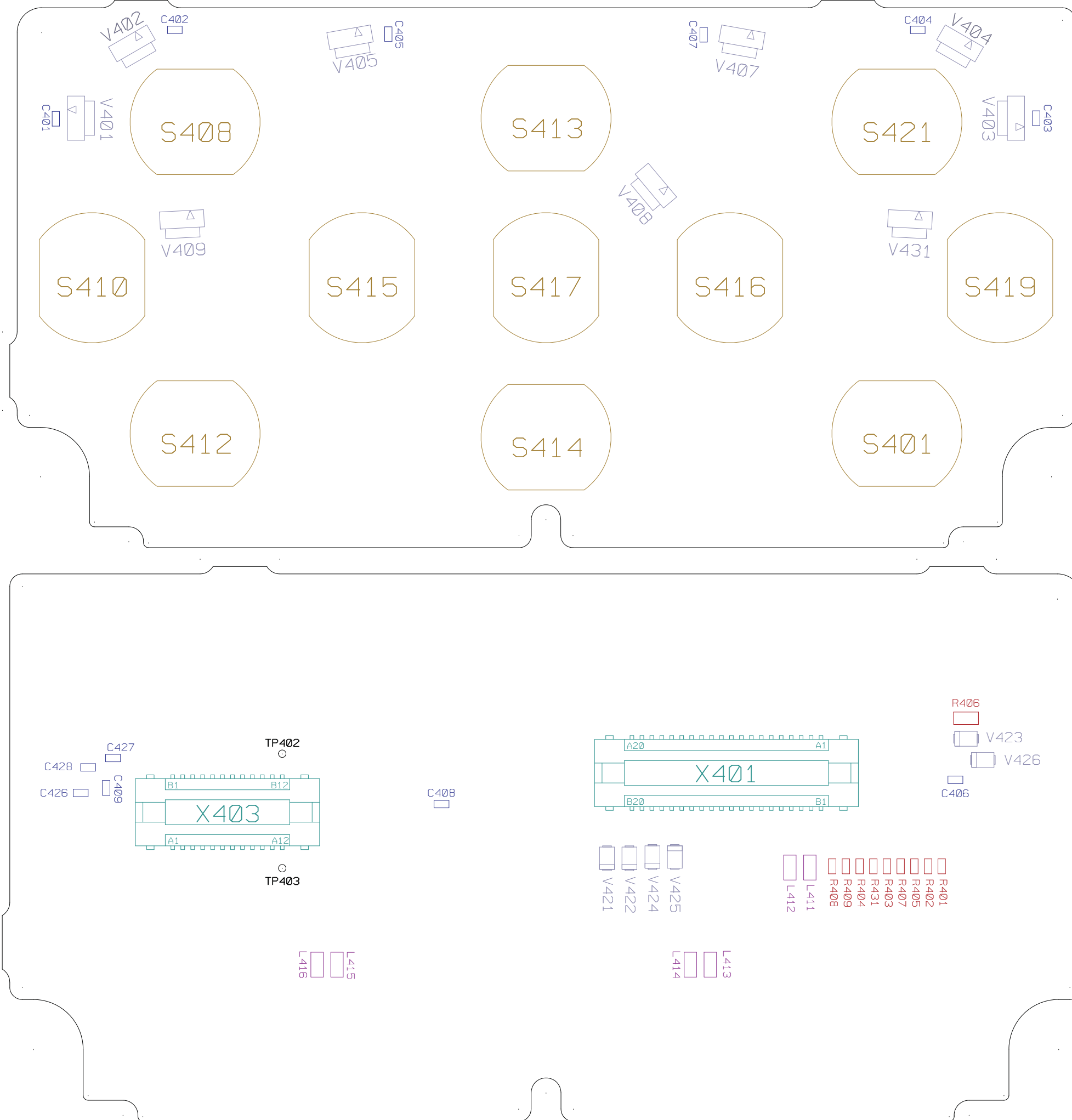
MP 4 - V3102_Pin C1 and MP 5 - V3102_Pin C2

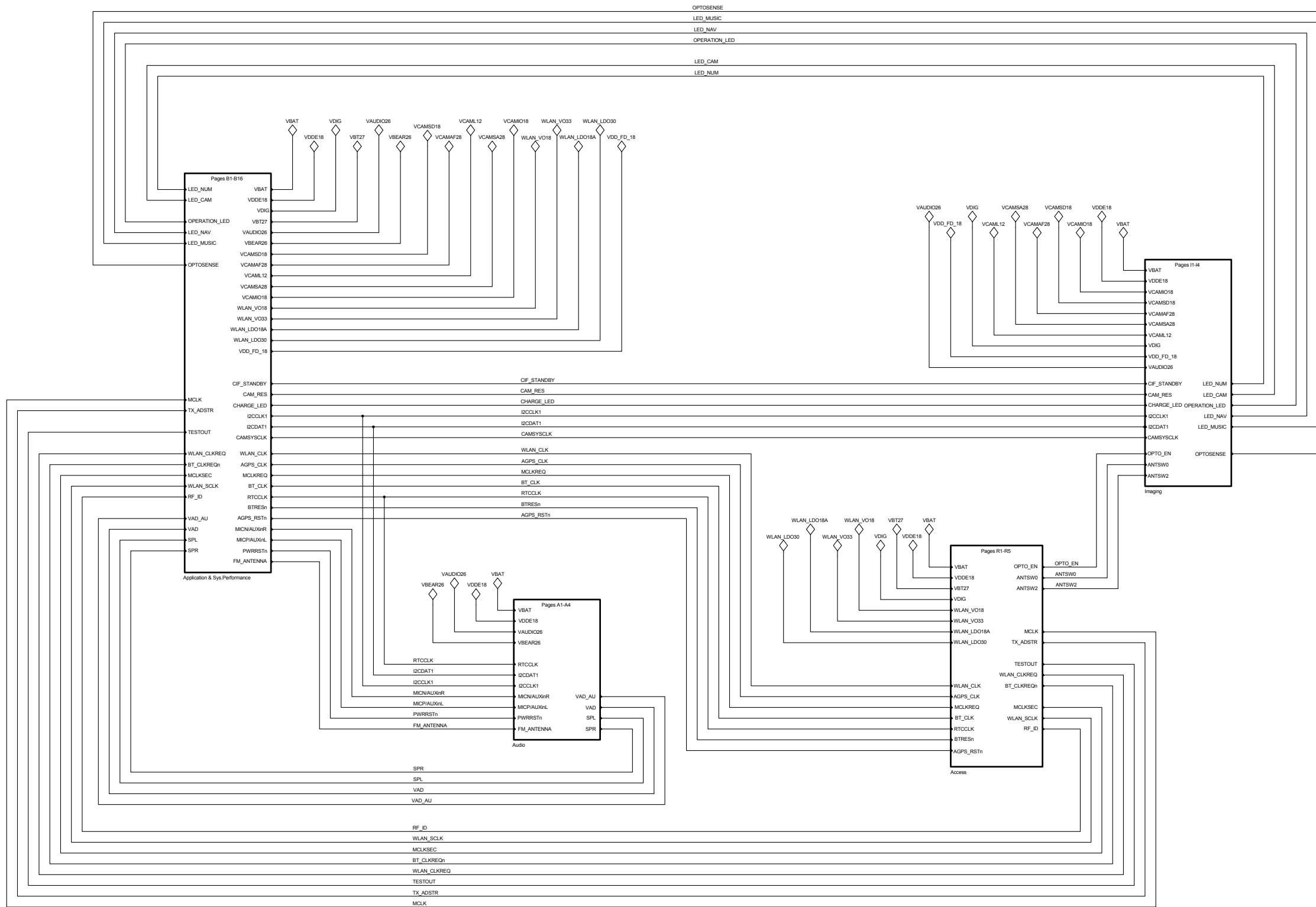


WLAN Tx Output Power



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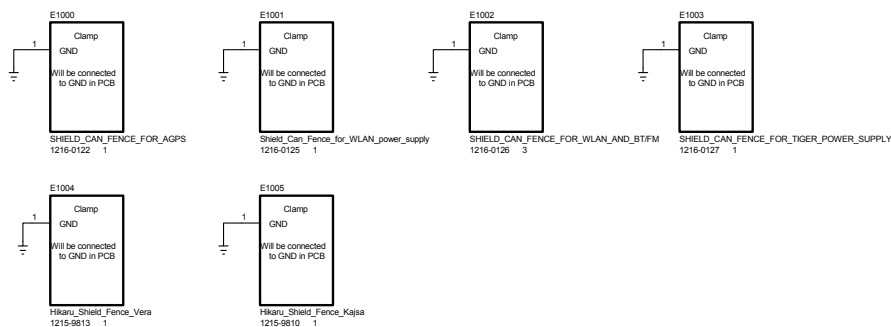
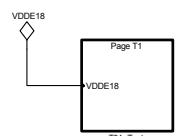
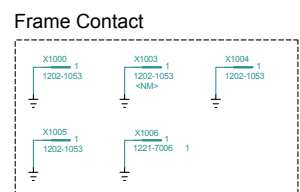
Port	Usage	Page
AccGPIO00	USB_HSTP	B14
AccGPIO01	USB_HSDIR	B14
AccGPIO02	CTMS	B14
AccGPIO03	OFMS	B14
AccGPIO04	USB_HINCLK	B14
AccGPIO05	USB_HSNXT	B14
AccGPIO06	USB_HSDATA4	B14
AccGPIO07	USB_HSDATA5	B14
AccGPIO08	USB_HSDATA6	B14
AccGPIO09	USB_HSDATA7	B14
AccGPIO10	UART3_RX	R04
AccGPIO11	UART3_TX	R04
AccGPIO12	UART3_CTS	R04
AccGPIO13	UART3_RTS	R04
AccGPIO14	CH_DET_DP	B14
AccGPIO15	CH_DET_DM	B14
AccGPIO16	USB_HSCHP_SEL	B14
AccGPIO17	AGPS_SYNC	R04
AccGPIO18	USB_HSDATA3	B14
AccGPIO19	WLAN_SPI_CSn	R05
AccGPIO20	ACC_SPI_DI	R03
AccGPIO21	ACC_SPI_DO	R03
AccGPIO22	ACC_SPI_CLK	R03
AccGPIO23	OVP_FLAG	B14
AccGPIO24	not used	T01
AccGPIO25	WLAN_SPI_IRQ	R05
AccGPIO26	BT_SPI_CSn	R03
AccGPIO27	BT_SPI_INT	R03

Port	Usage	Page
BTGPIO0	WLAN_CONF_IRMn	R03
BTGPIO8	WLAN_BT_STATE	R03
BTGPIO9	not used	R03
BTGPIO10	not used	R03
BTGPIO11	WLAN_BT_PRIORITY	R03
BTGPIO16	not used	R03

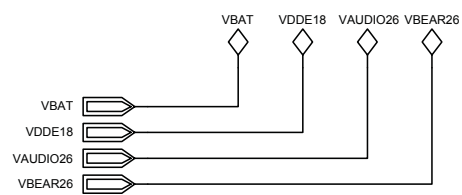
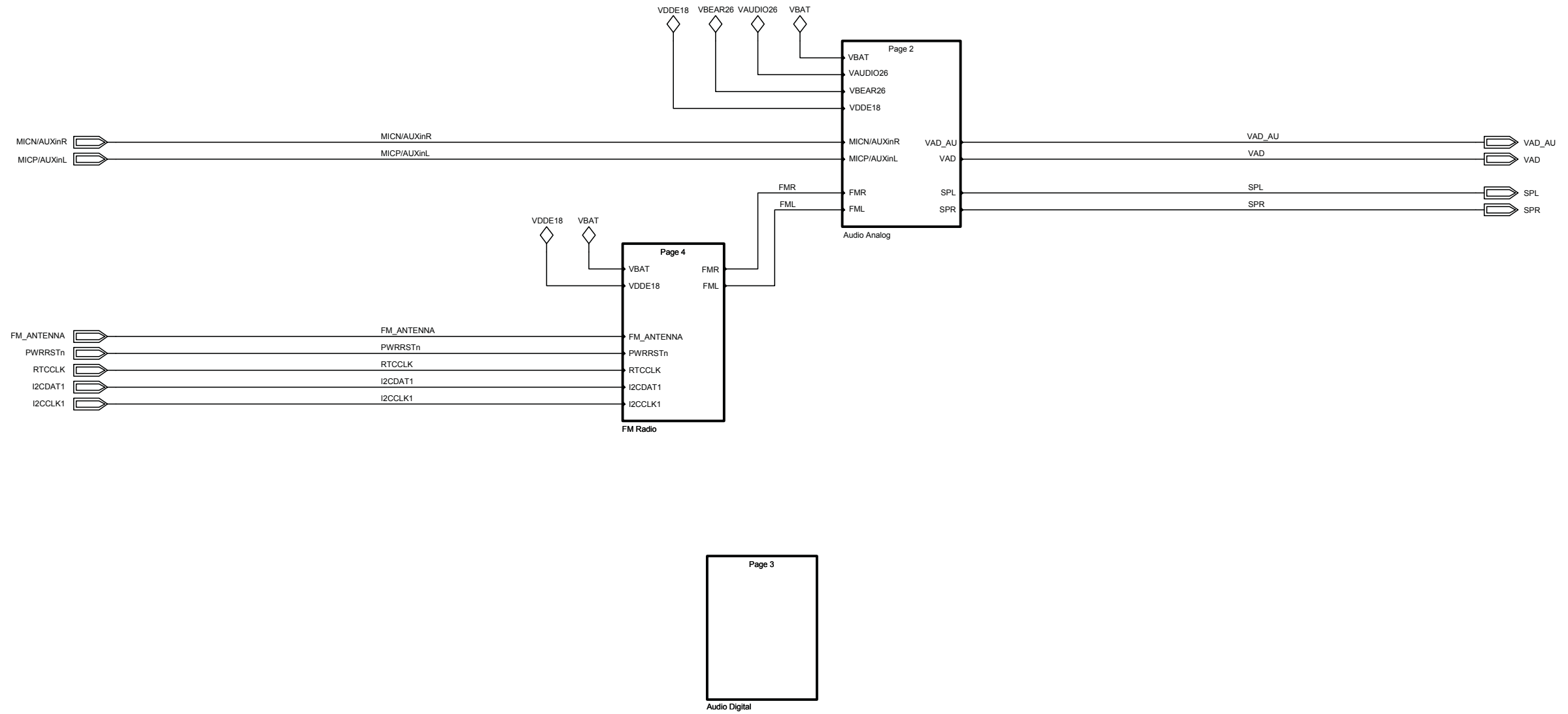
Port	Usage	Page
AppGPIO00	FM_INT	A04
AppGPIO01	APP_LOG	B14
AppGPIO02	CAMREQ	R03
AppGPIO03	FLASH_PROT_EN	B06
AppGPIO04	COVER_OPEN	R03
AppGPIO05	VIDCC_SPI_CS	B16
AppGPIO06	not used	T01
AppGPIO07	VIDCC_SPI_DI	B16
AppGPIO08	VIDCC_SPI_DO	B16
AppGPIO09	VIDCC_SPI_CLK	B16
AppGPIO10	AGPS_CLK_EN	B03
AppGPIO11	AU_SWITCH	A02
AppGPIO12	MSDETECT	B13
AppGPIO13	FLASH_DR_RST	B04
AppGPIO14	not used	T01
AppGPIO15	DCON	xxx
AppGPIO16	VIDCC_INT	B16
AppGPIO17	not used	T01
AppGPIO18	VIDCC_RESn	B16
AppGPIO19	not used	T01

Port	Usage	Page
GIO_P0	not used	B16
GIO_P1	not used	B16
GIO_P2	not used	B16
GIO_P3	not used	B16
PO0	CAM_LDO_EN	B16
PO1	CIF_STANDBY	B16
PO2	VCAMSD_EN	B16
PO3	CAMRESn	B16
PO4	VIDCC_L1DET	B16
PO5	VIDCC_L1_EN	B16
PO6	VIDCC_SDR_EN	B16
PO7	VIDCC_CLKREQn	B16

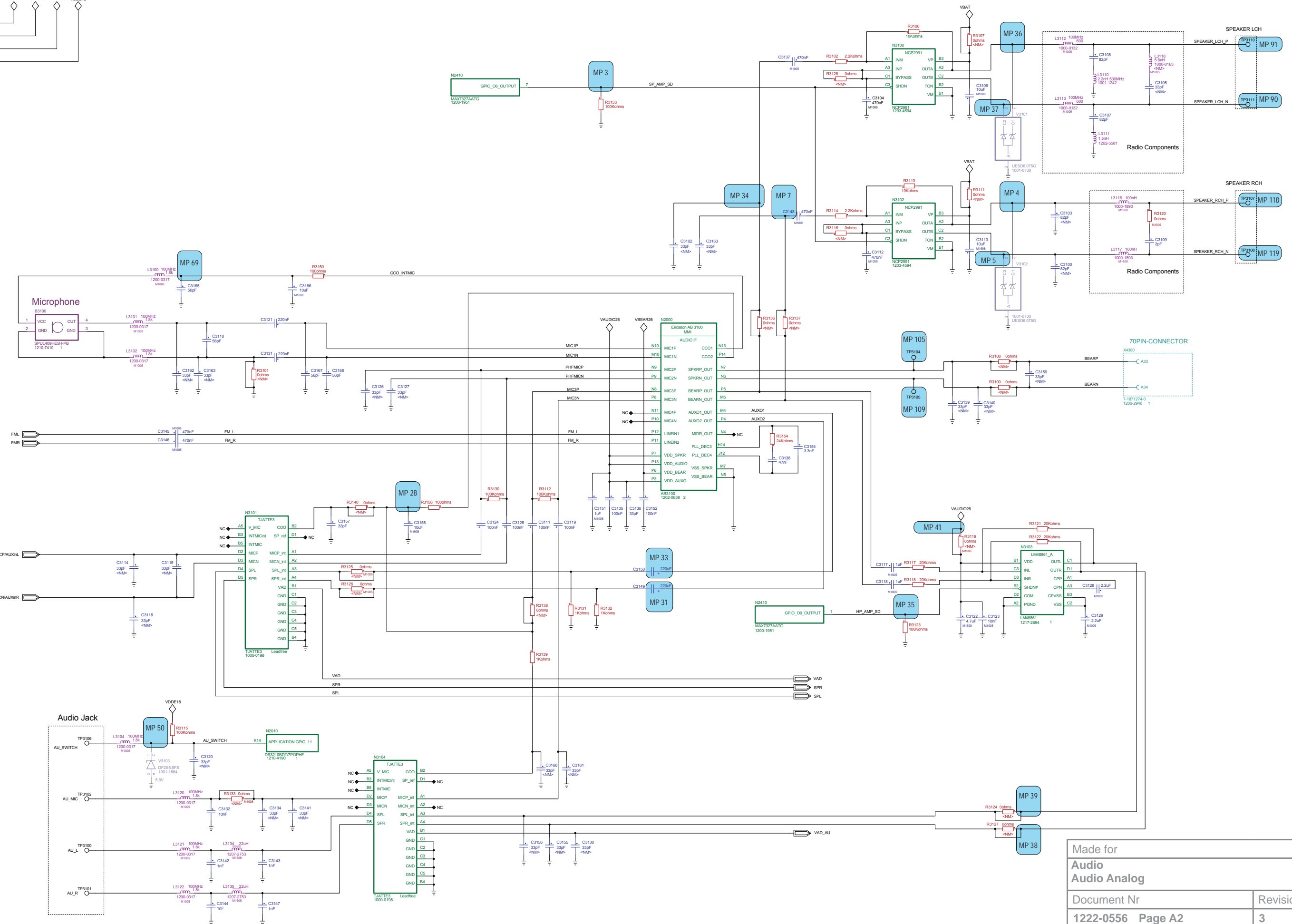
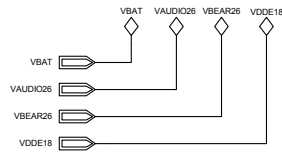
Port	Usage	Page
GPIO_00	HP_AMP_SD	B04
GPIO_01	AGPS_LDO_EN	R04
GPIO_06	SP_AMP_SD	A02
GPIO_07	AGPS_PWRON	R04
GPIO_08	not used	T01
GPIO_09	WLAN_RSTn_P0n	R05
GPIO_10	WLAN_P0n	B10
GPIO_11	not used	T01
GPIO_12	not used	T01
GPIO_13	not used	T01
GPIO_14	not used	T01
GPIO_15	not used	T01
GPIO_P2	AGPS_CLKREQn	R03
GPIO_P3	not used	T01
GPIO_P4	not used	T01
GPIO_P5	not used	T01



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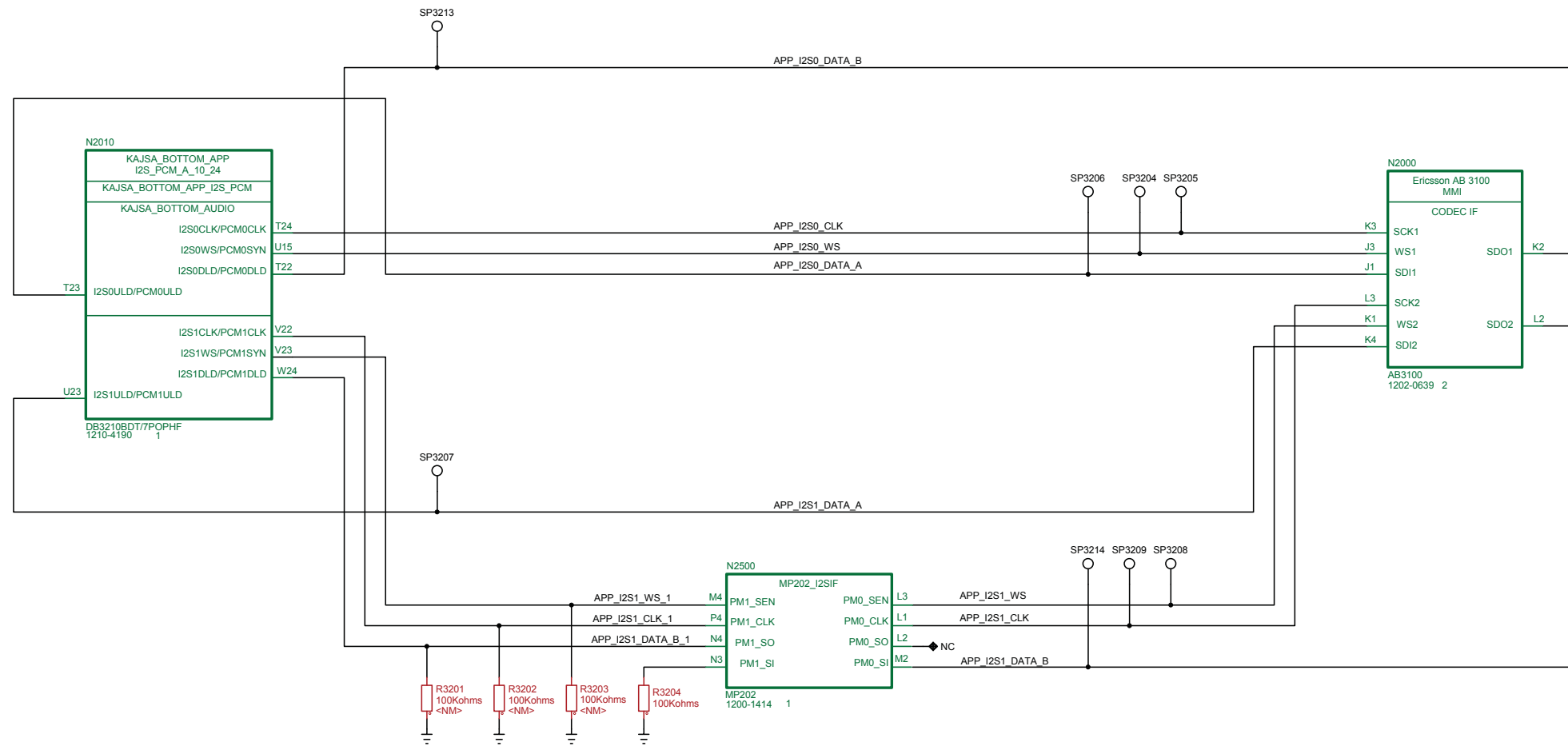


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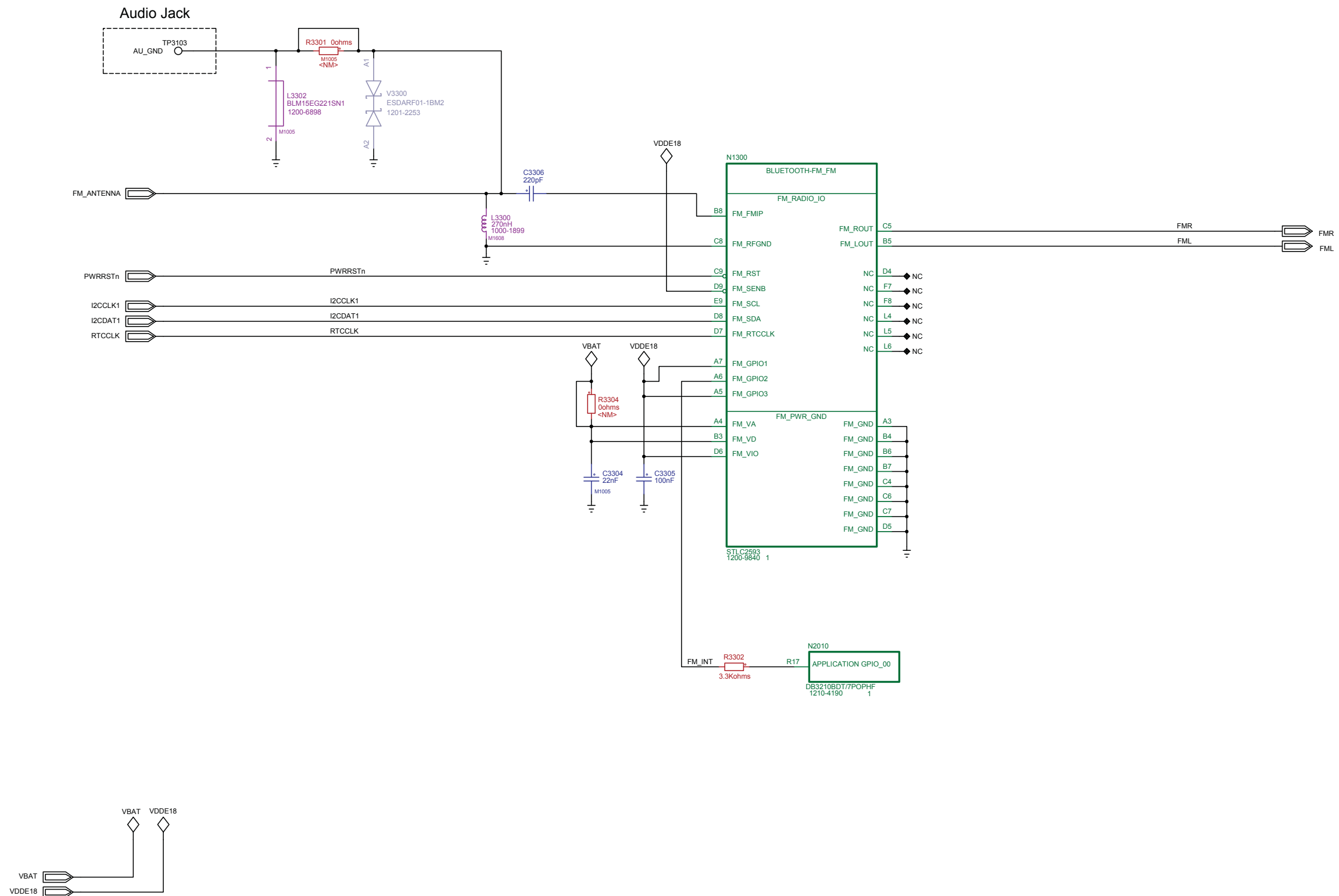
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Audio	
Audio Analog	
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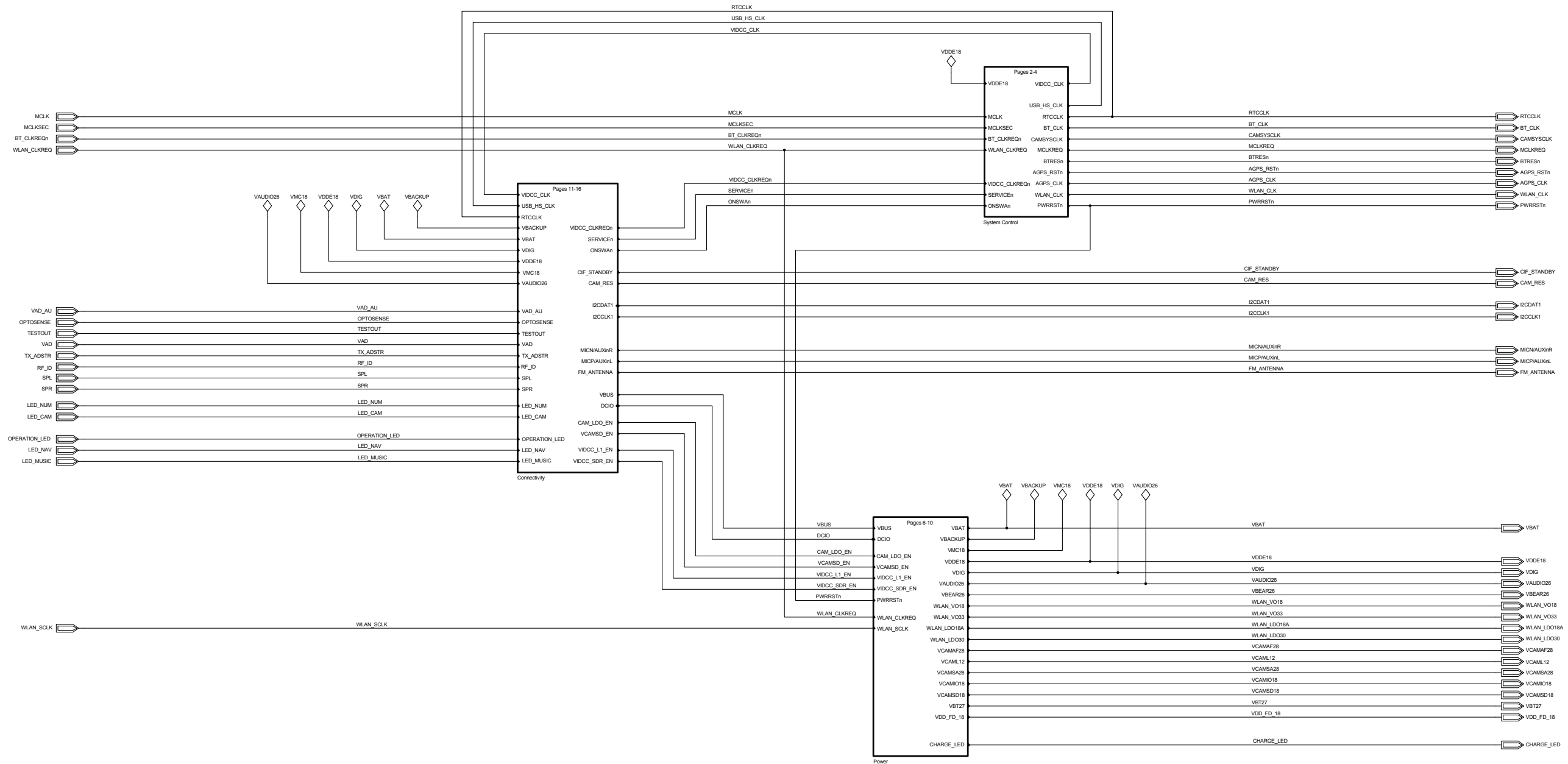


MEASUREMENT POINTS

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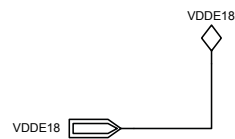
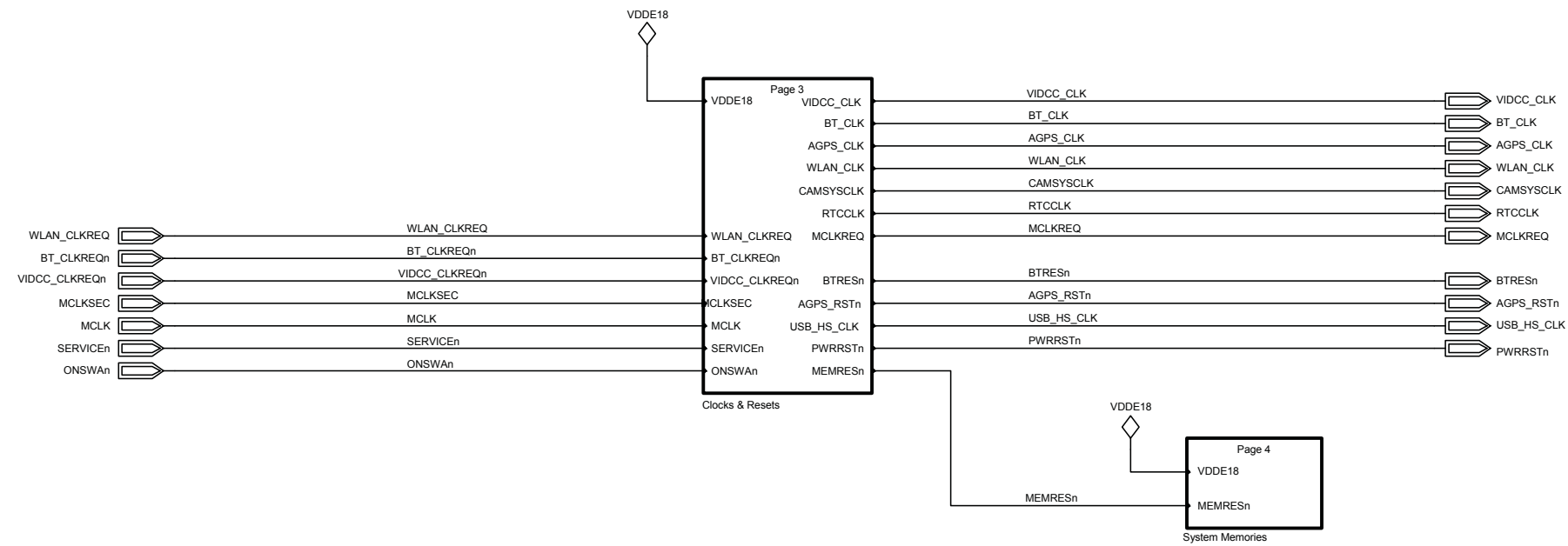


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Audio FM Radio	
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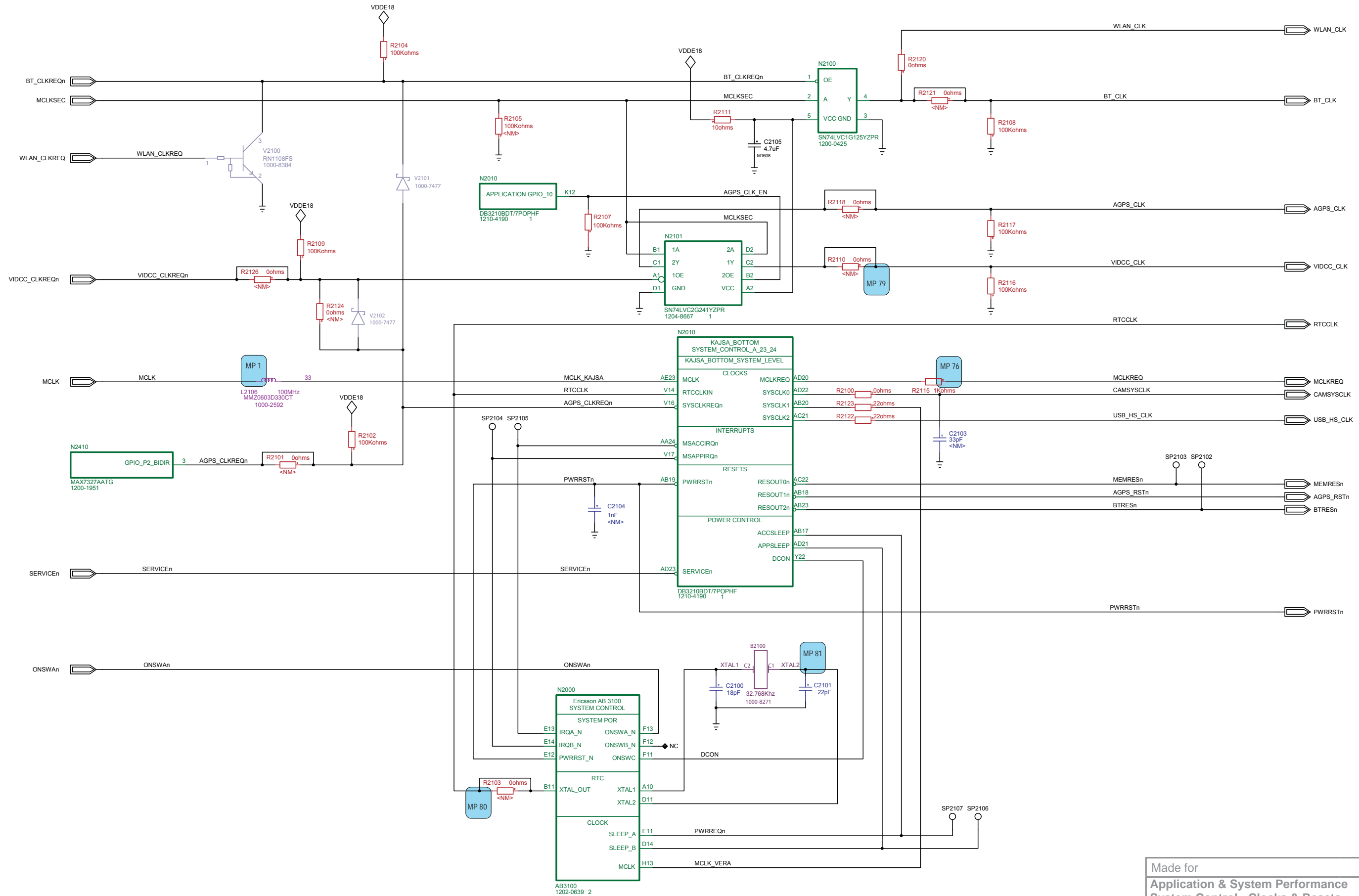


MEASUREMENT POINTS

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Application & System Performance Top	
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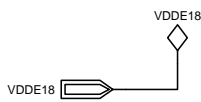
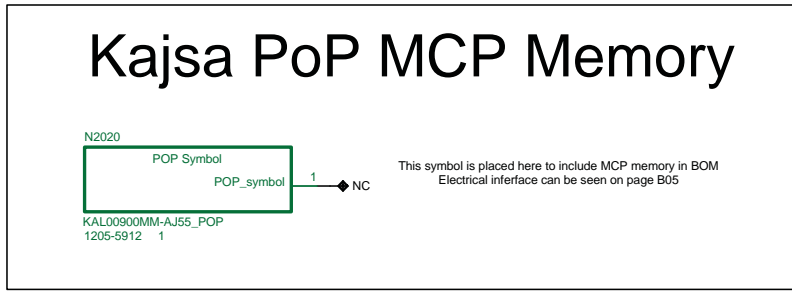
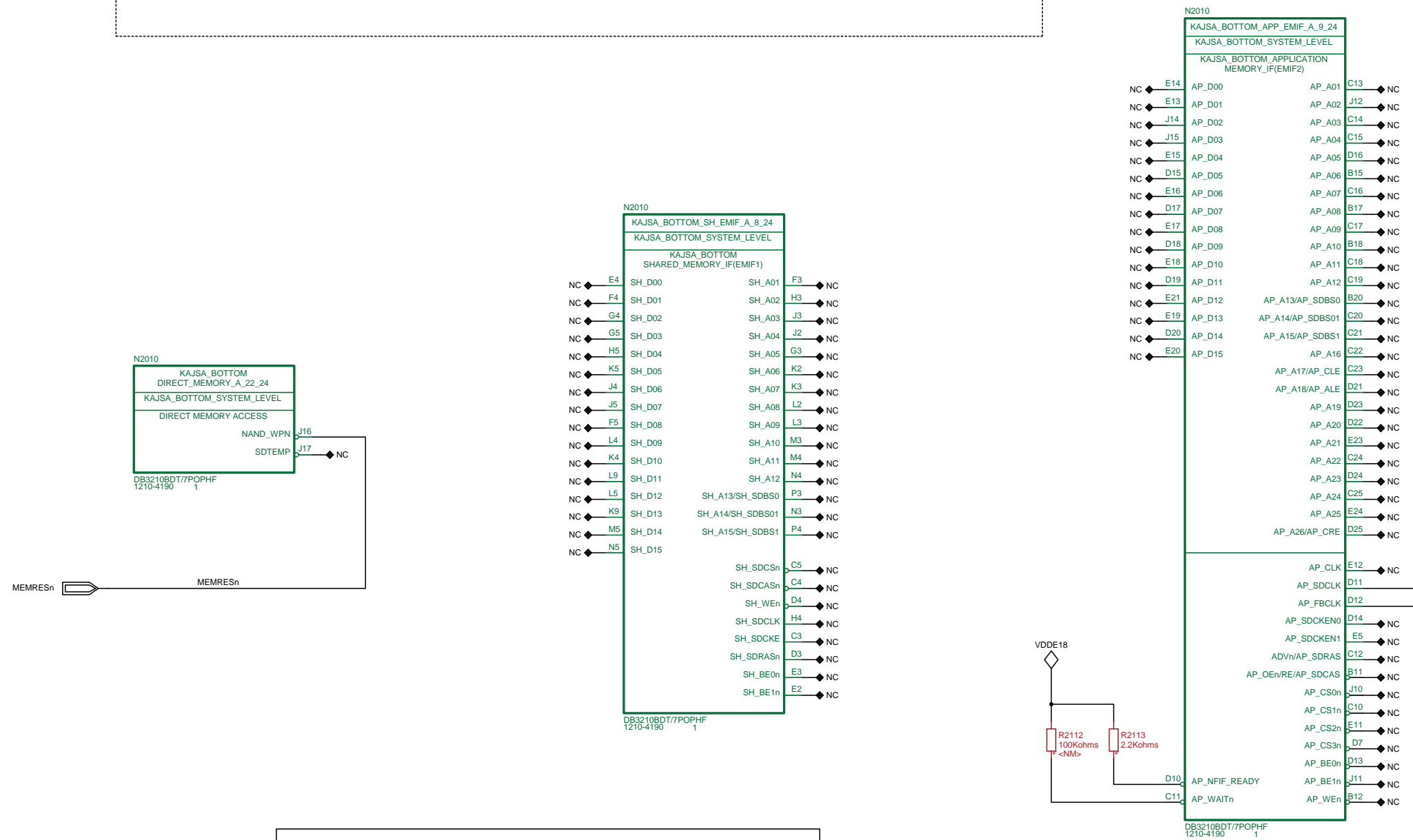


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Application & System Performance System Top	
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Application & System Performance	
System Control - Clocks & Resets	
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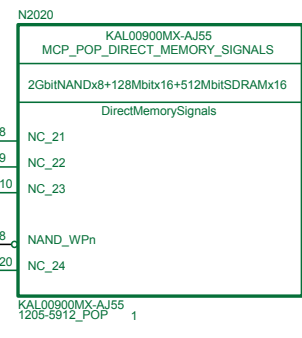
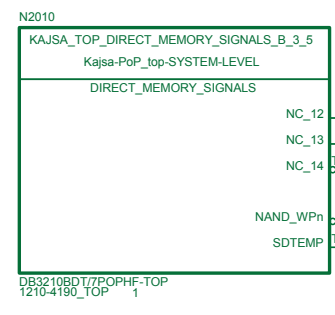
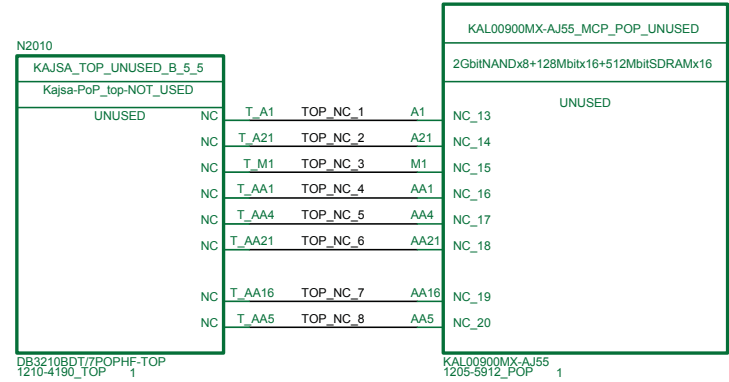
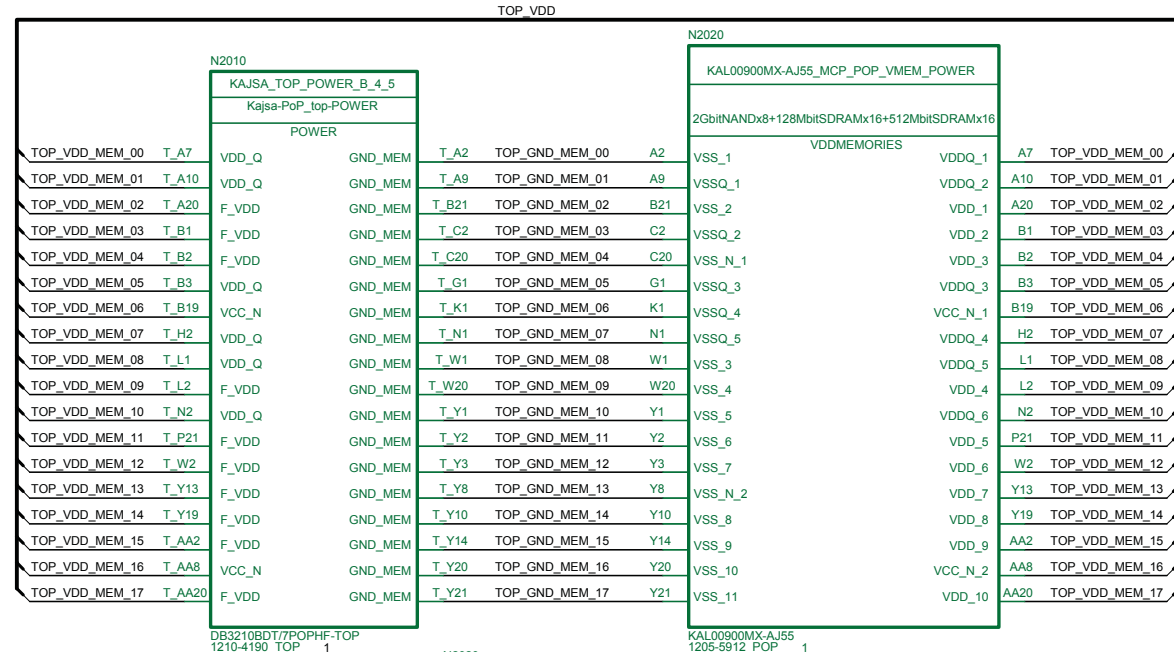
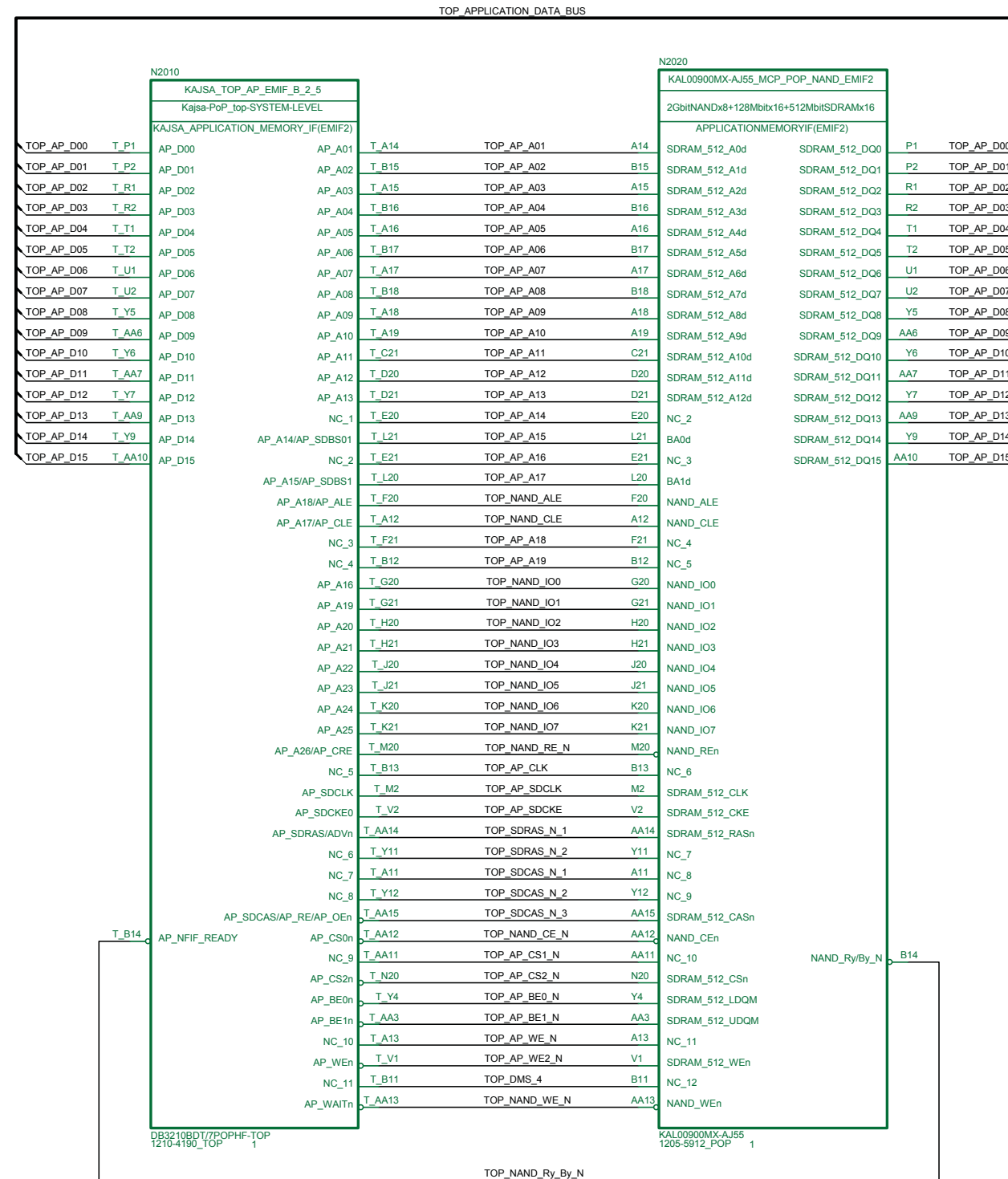
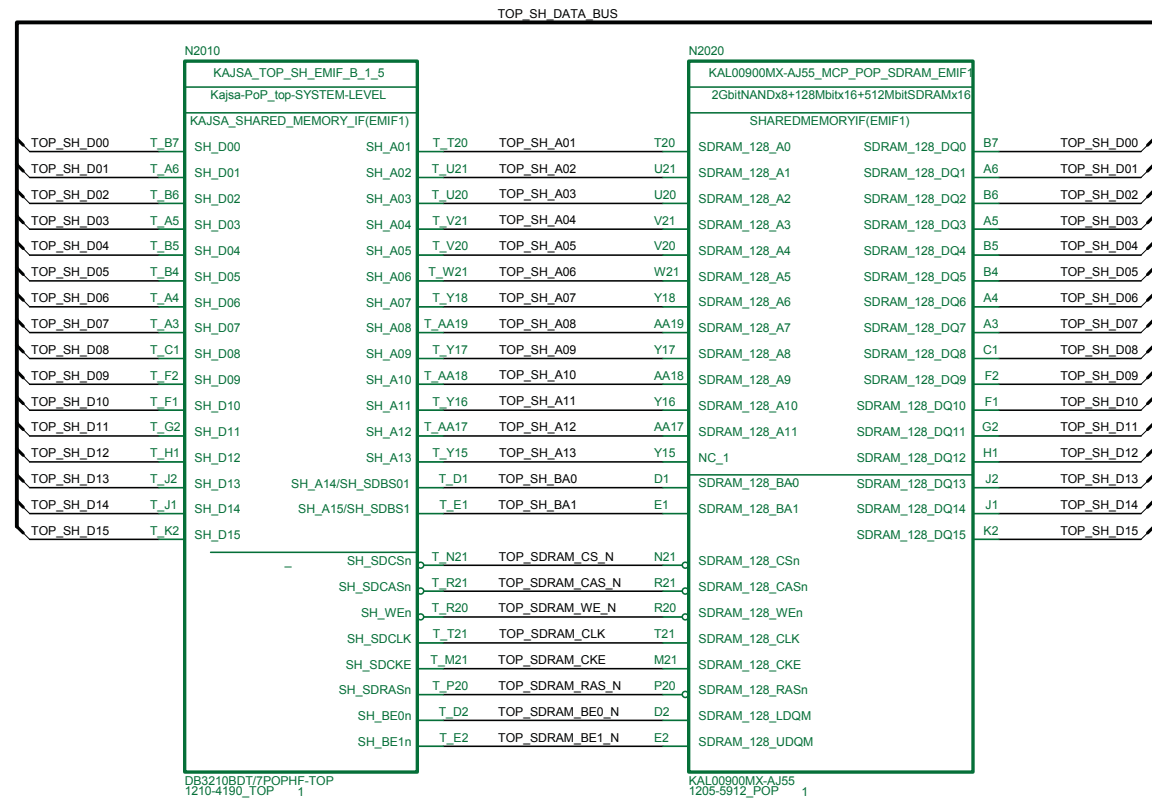
Even if these pins (EMIF) are left unconnected, they are still active due to PoP interface.



MEASUREMENT POINTS

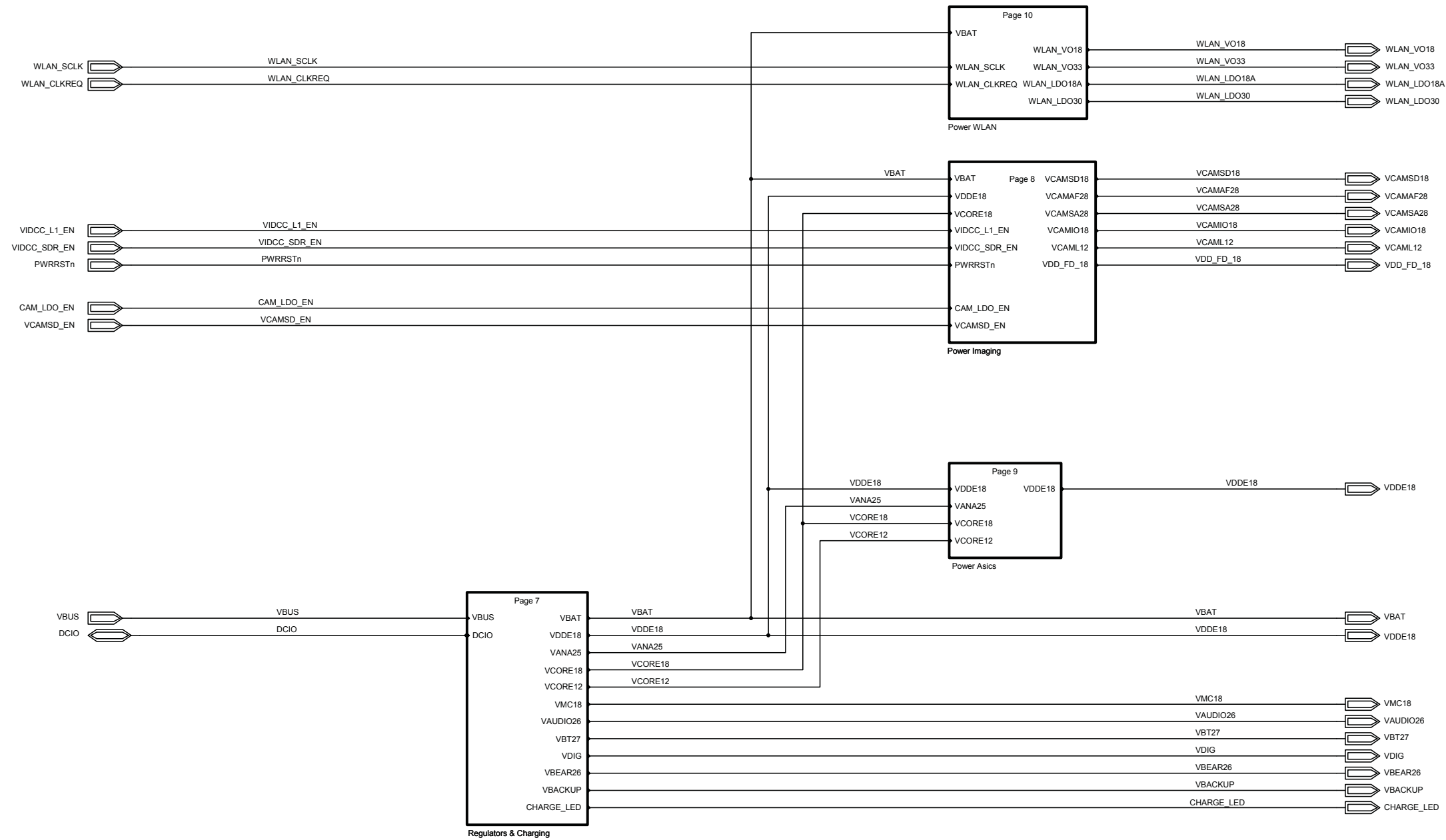
Made for	
Application & System Performance System Memories	
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Kajsa Pop Top and Memory PoP connection
Not to be included in packaging

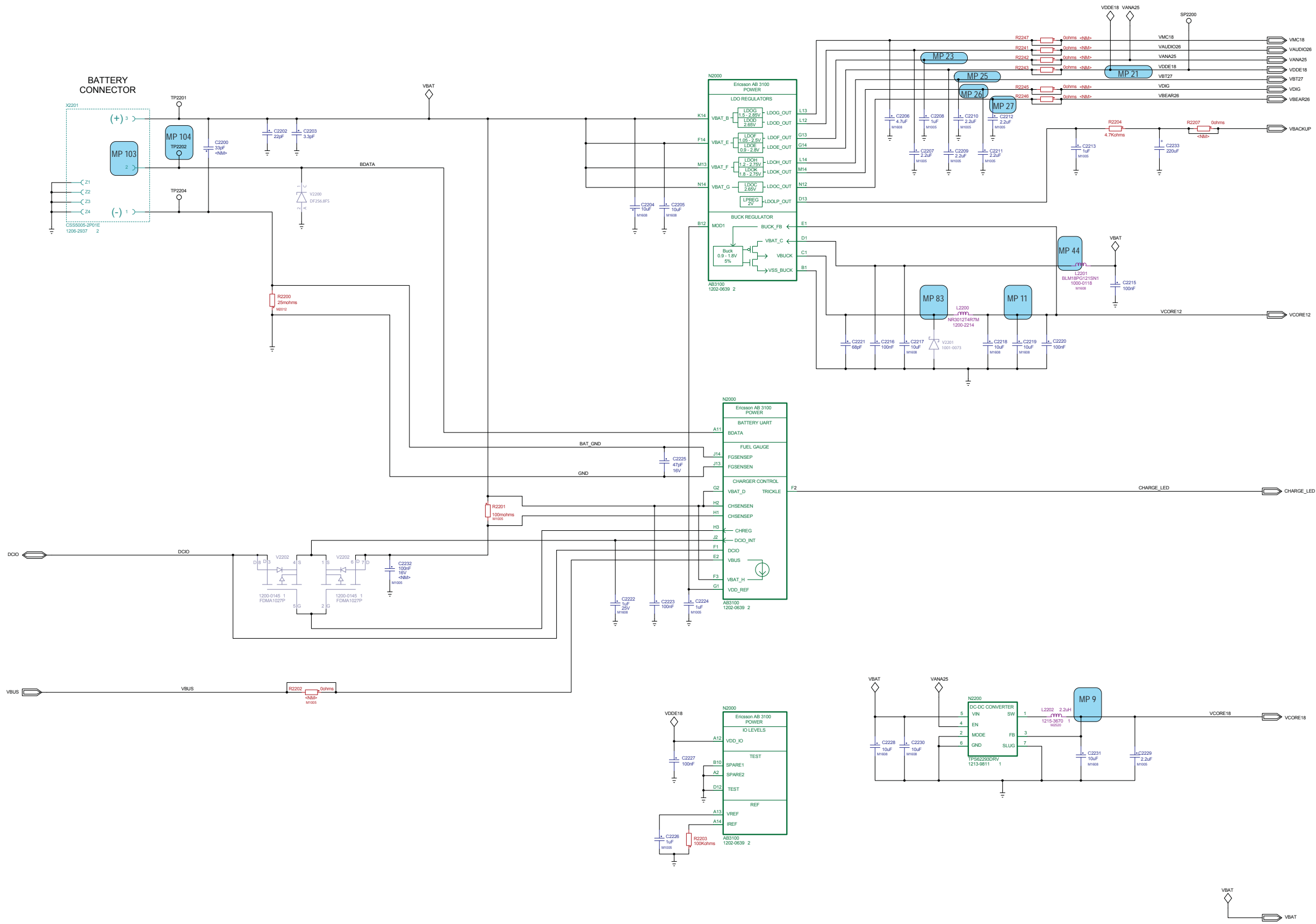


Made for	
Application & System Performance System PoP IF	
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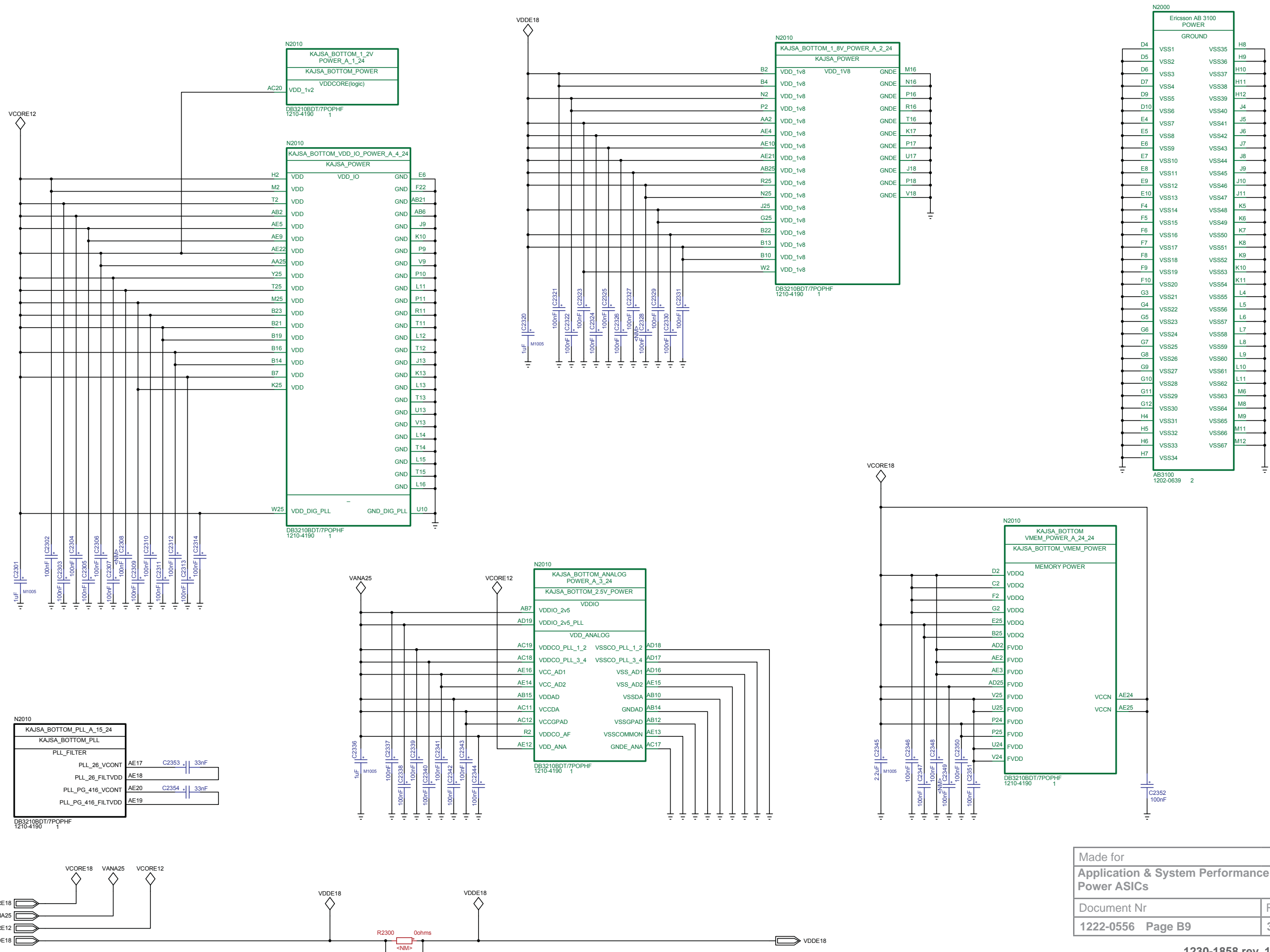
MEASUREMENT POINTS



Made for	
Application & System Performance Power Top	
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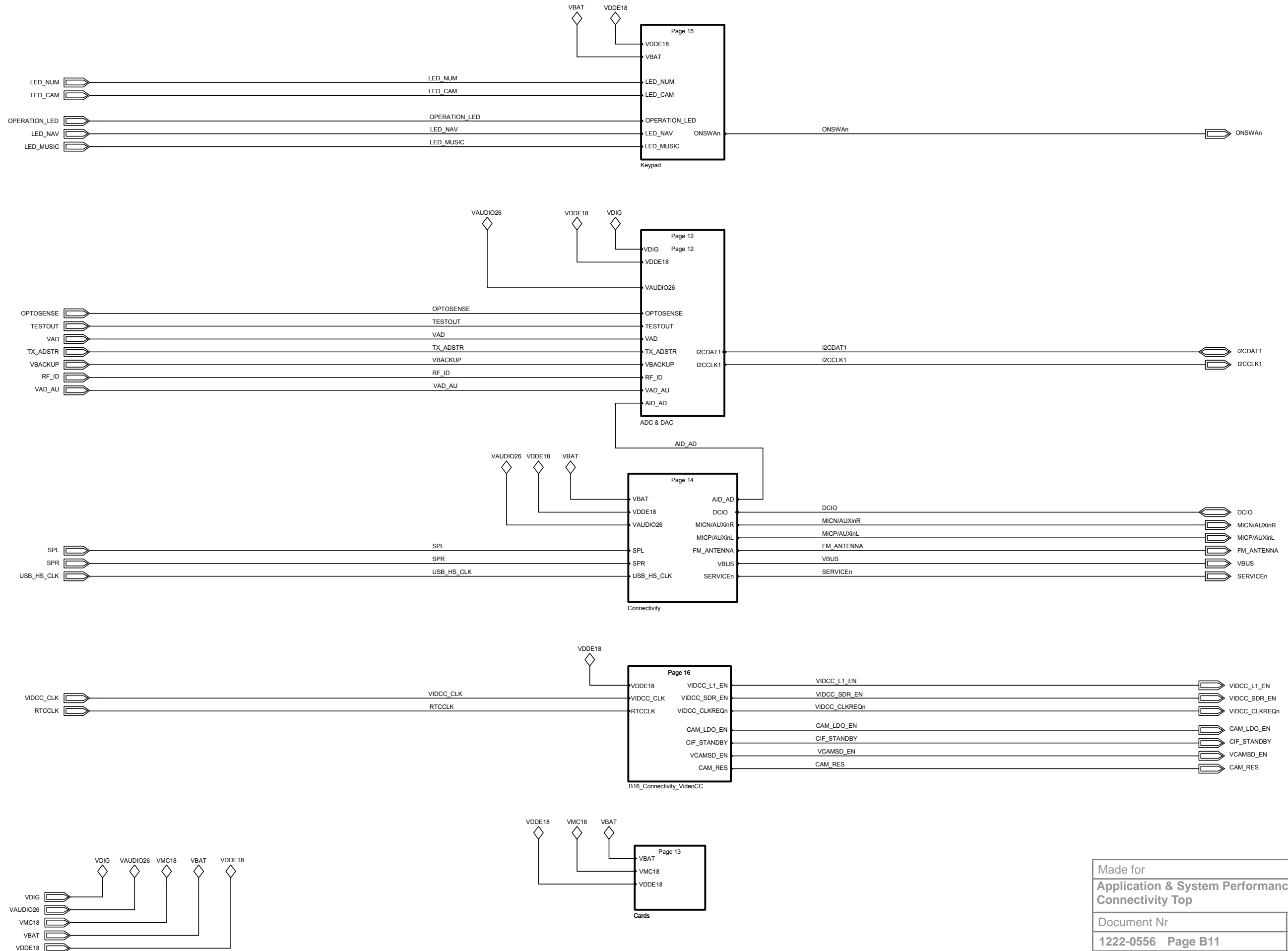


Made for	
Application & System Performance	
Power - Regulators & Charging	
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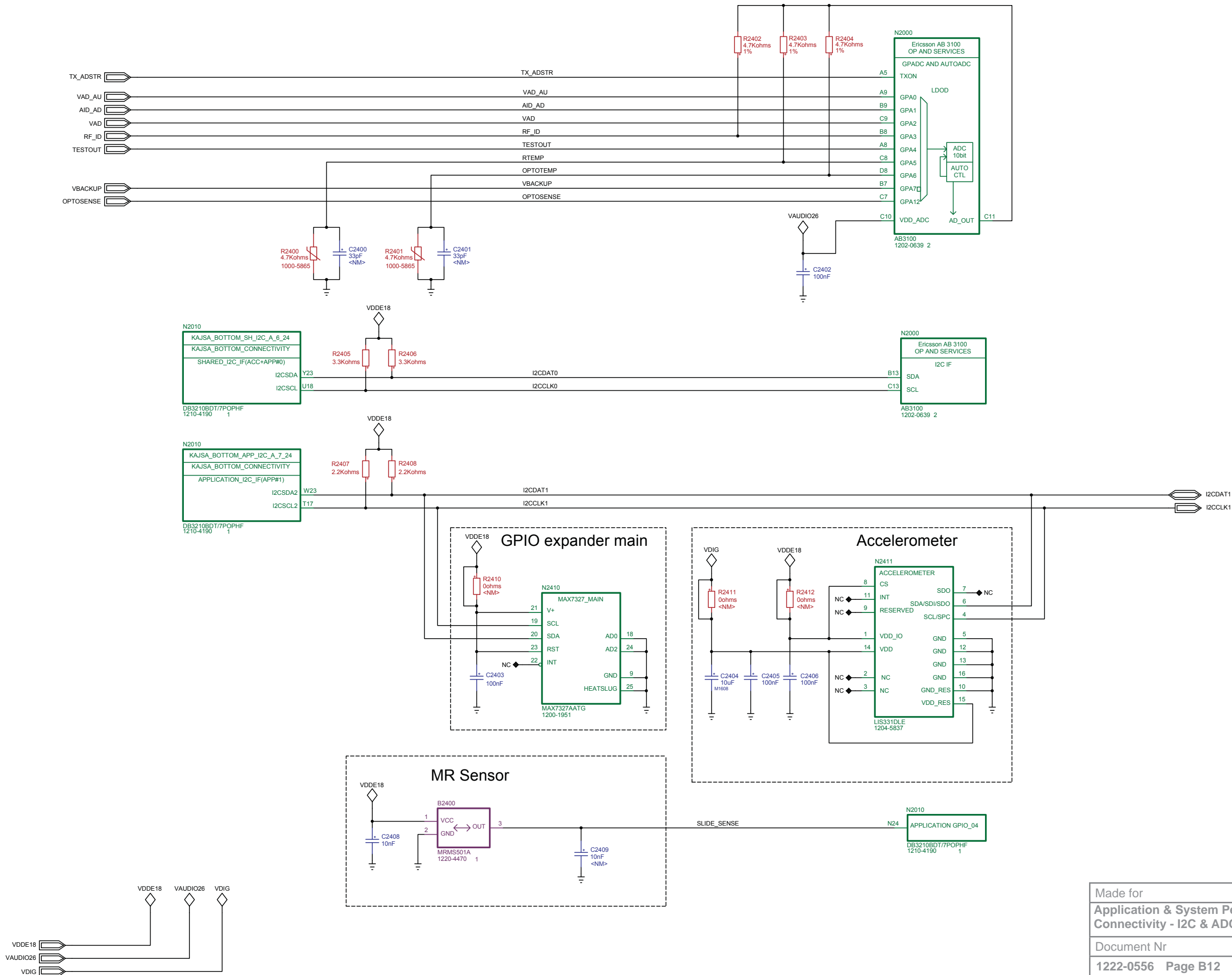


MEASUREMENT POINTS

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Application & System Performance Power ASICs	
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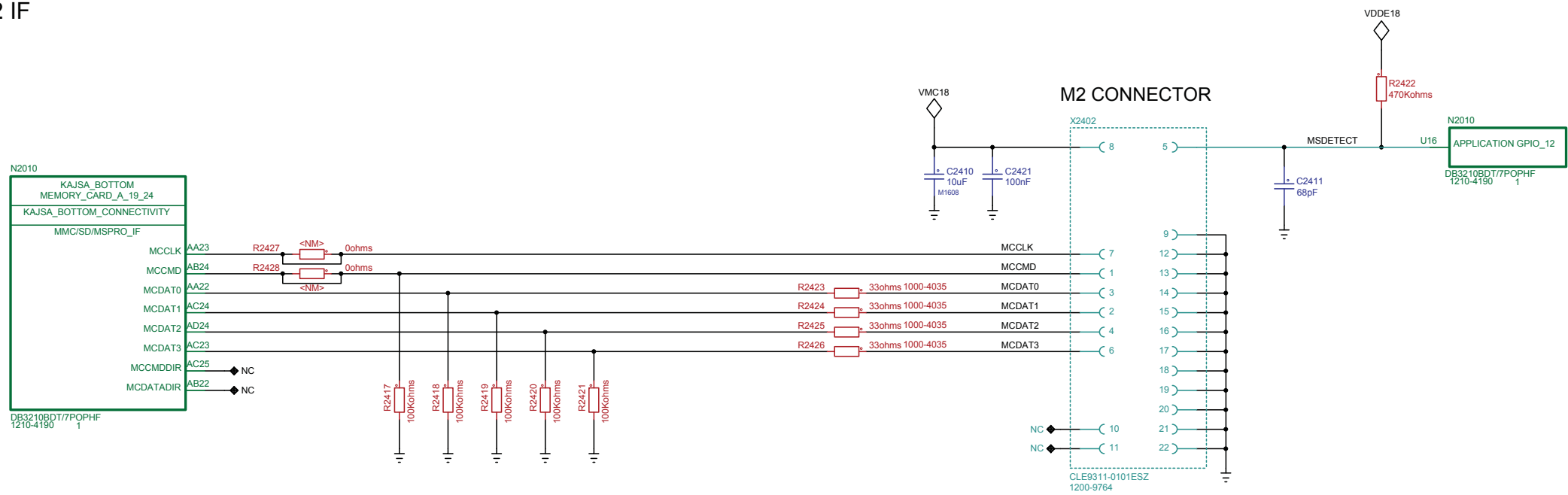


Made for Application & System Performance Connectivity Top	
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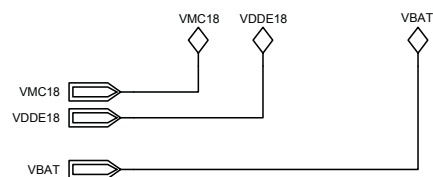
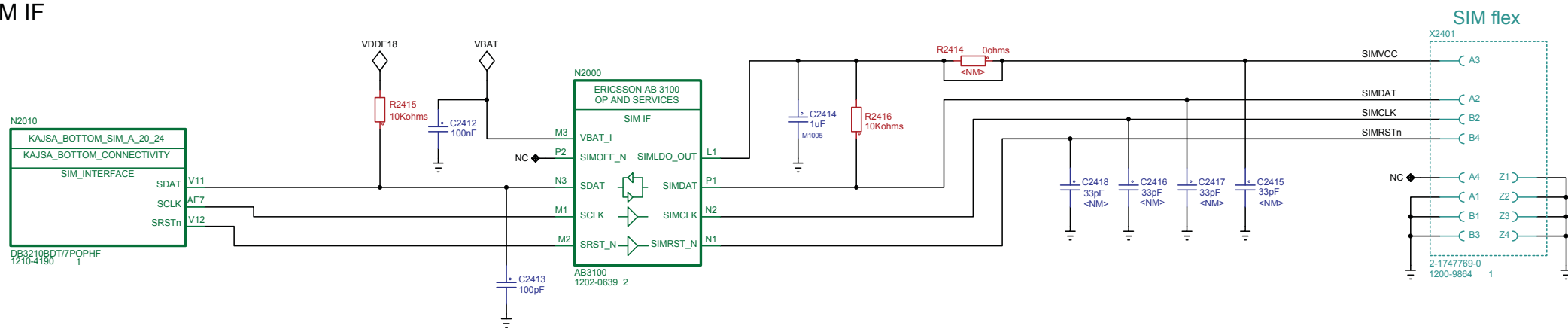


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Application & System Performance	
Connectivity - I2C & ADC	
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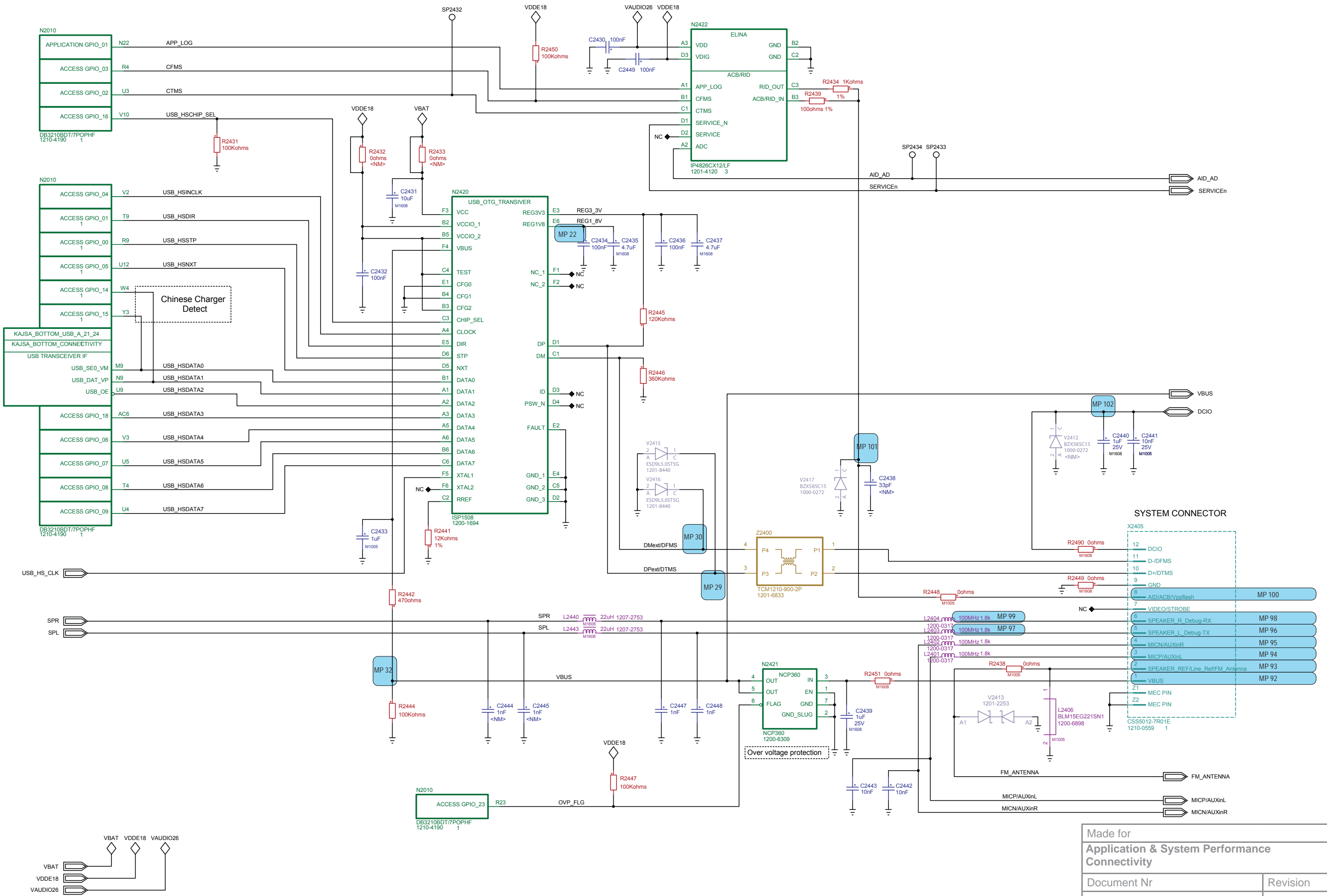
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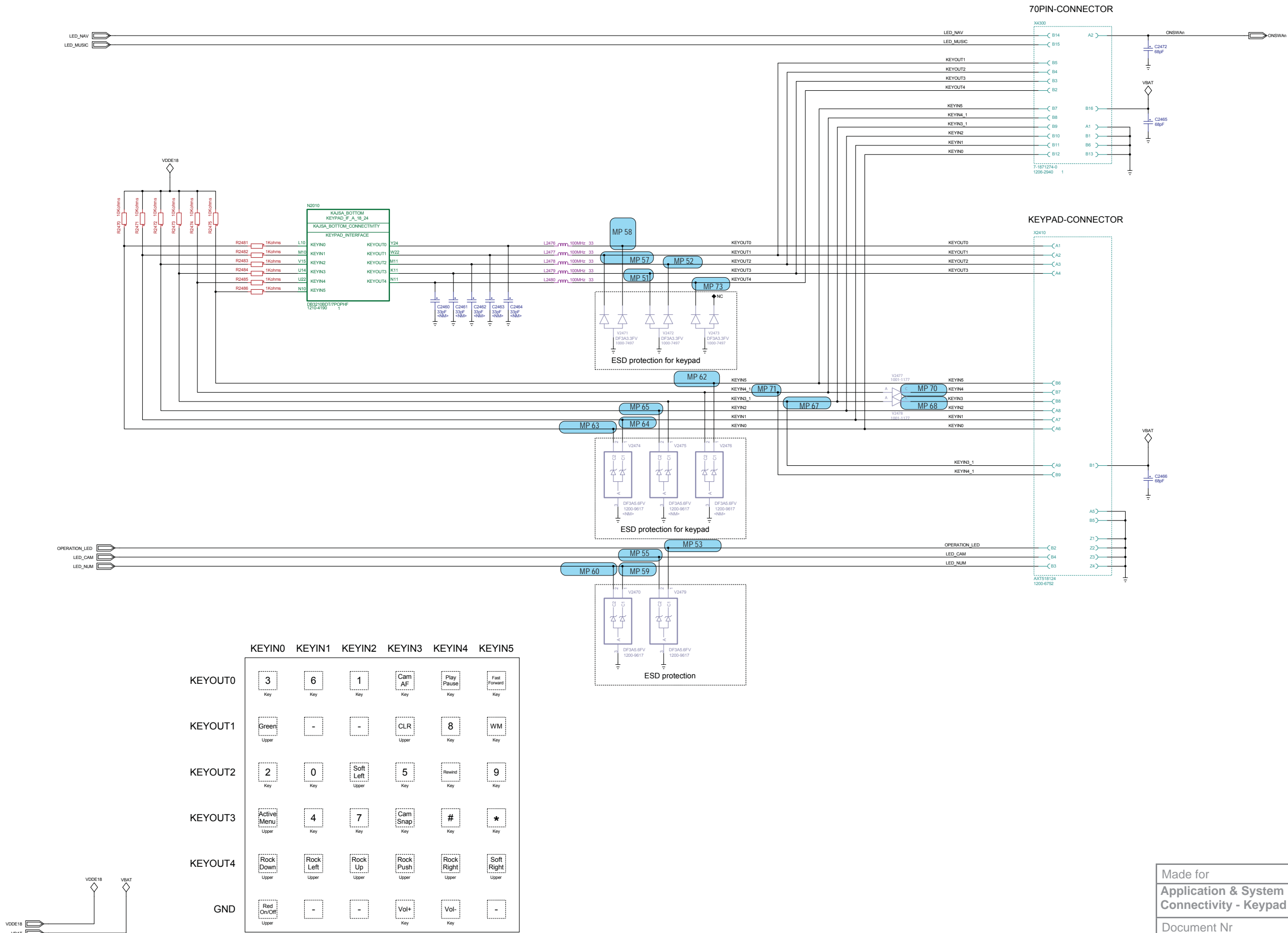
SIM IF



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Application & System Performance	
Connectivity - Cards	
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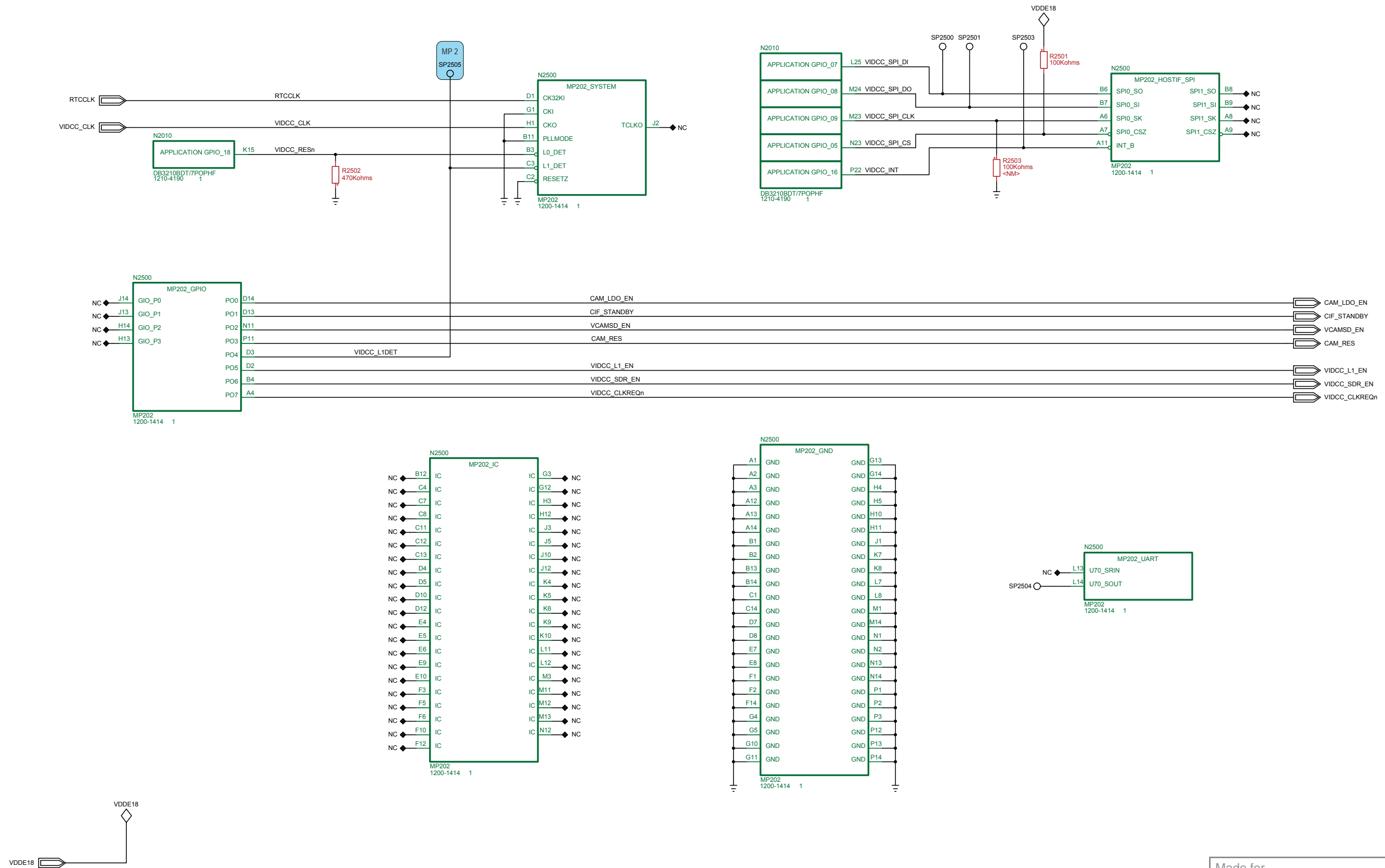


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Application & System Performance Connectivity	
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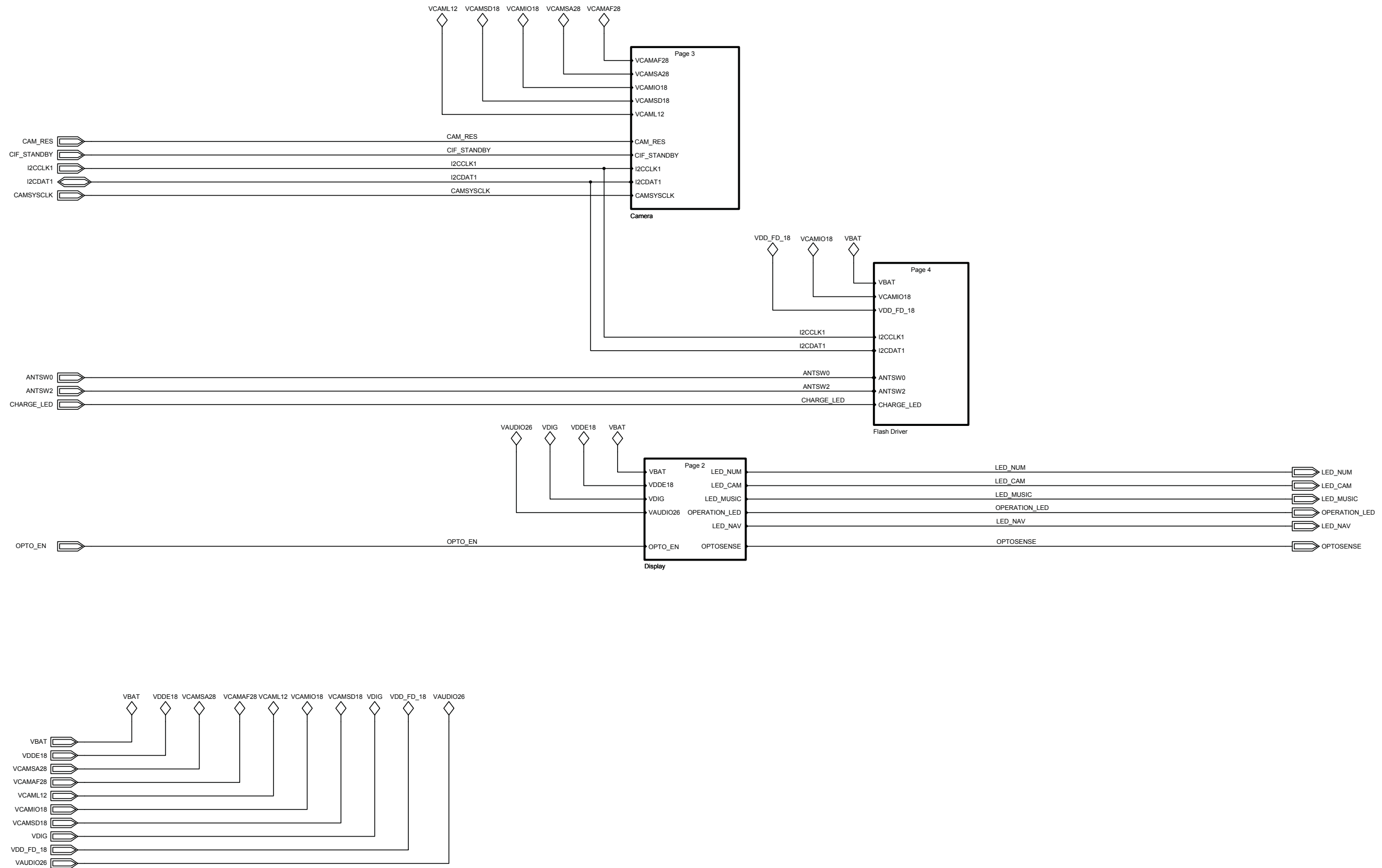


MEASUREMENT POINTS

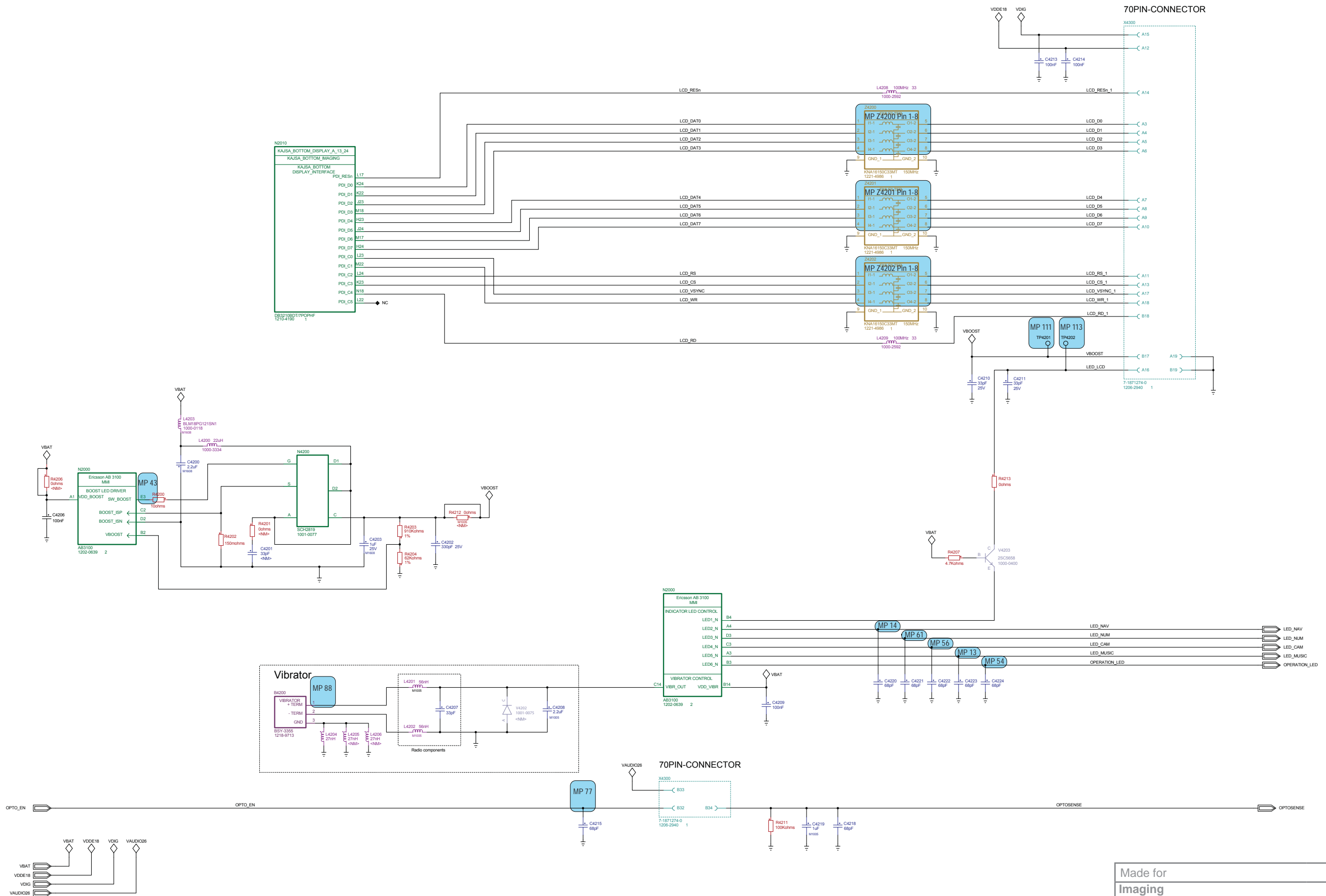
Made for Application & System Performance Connectivity - Keypad	
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Application & System Performance Connectivity - Video Companion Chip	
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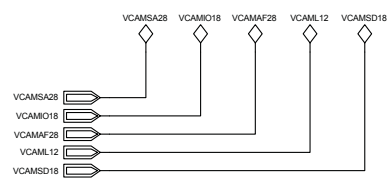
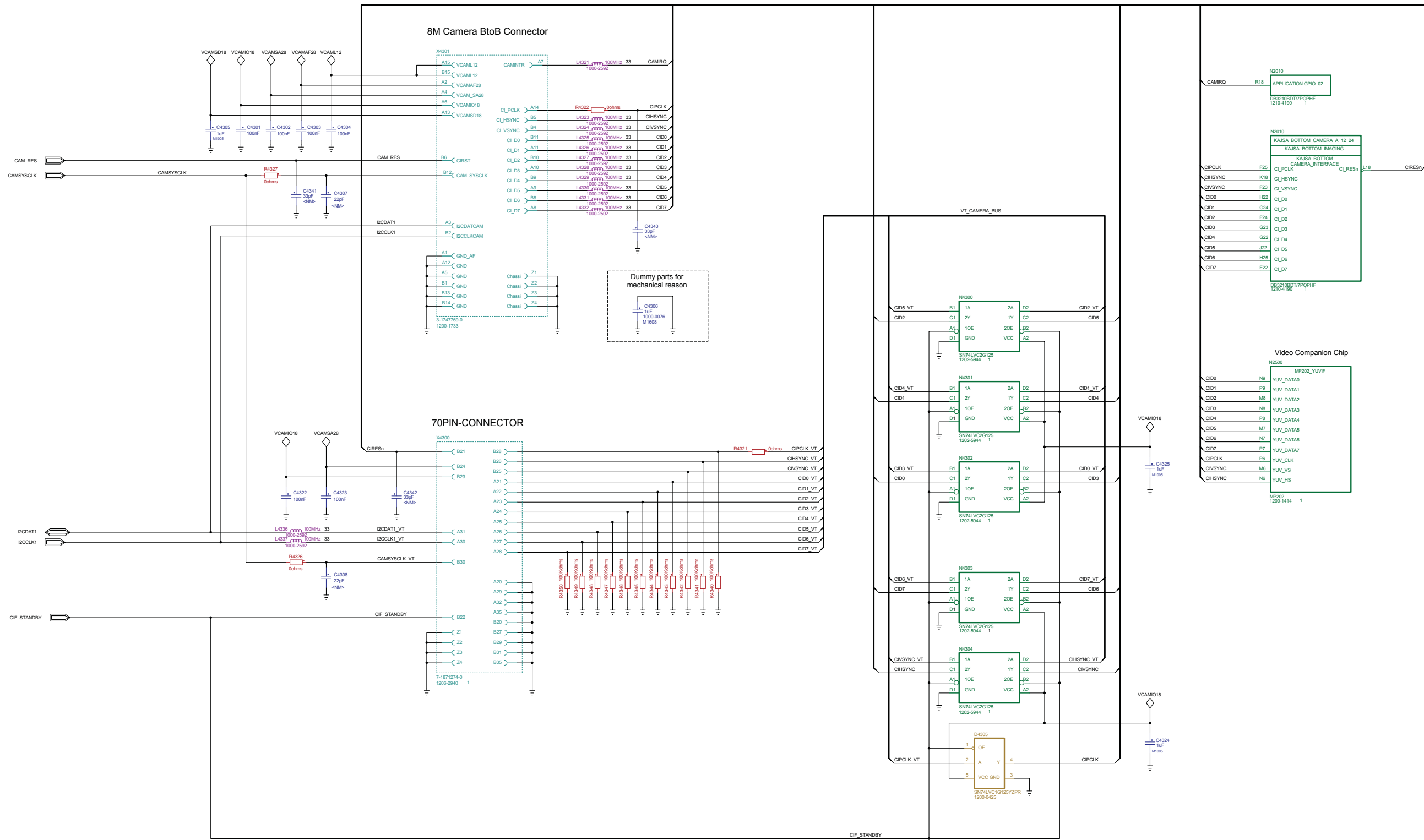


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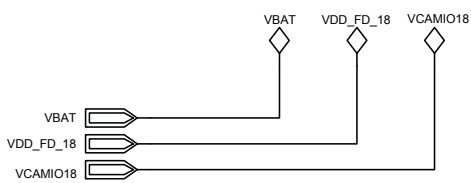
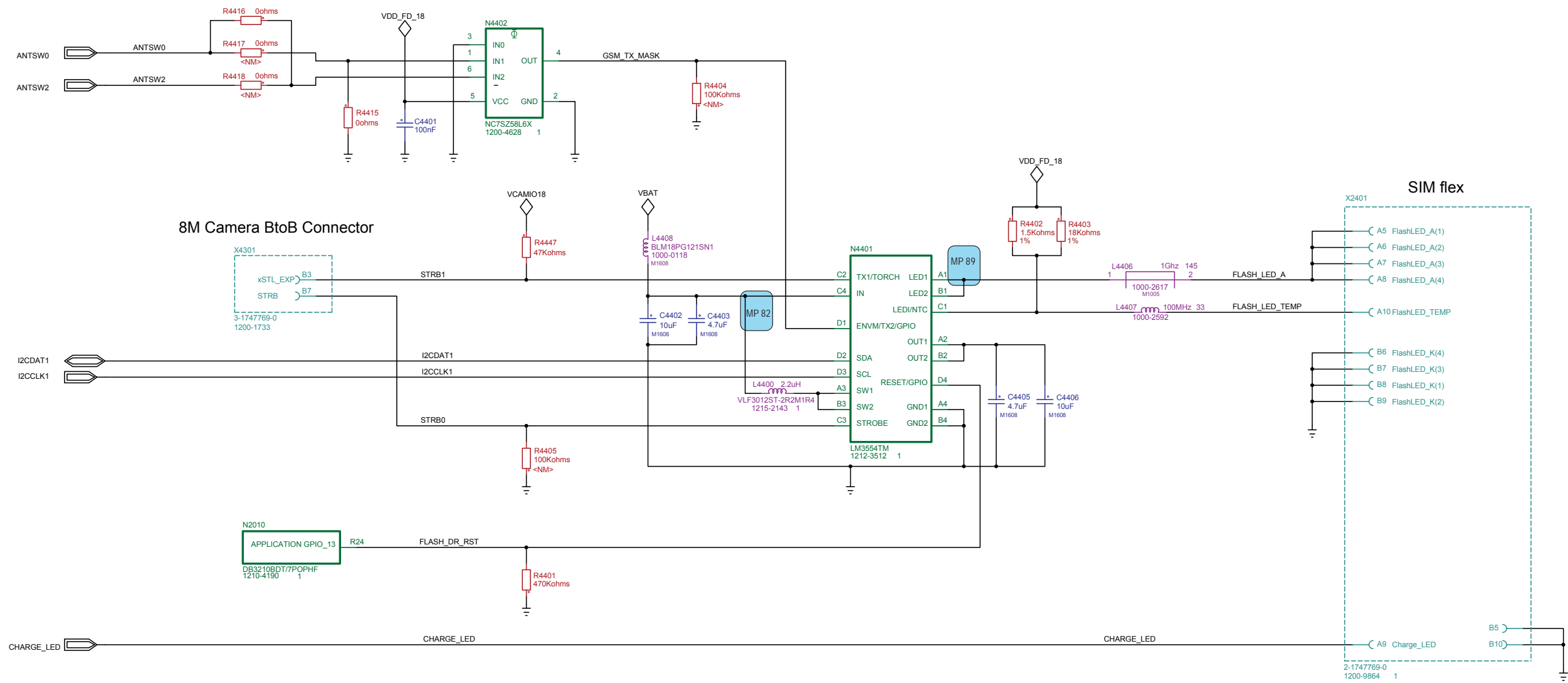
MEASUREMENT POINTS

Made for Imaging Display	
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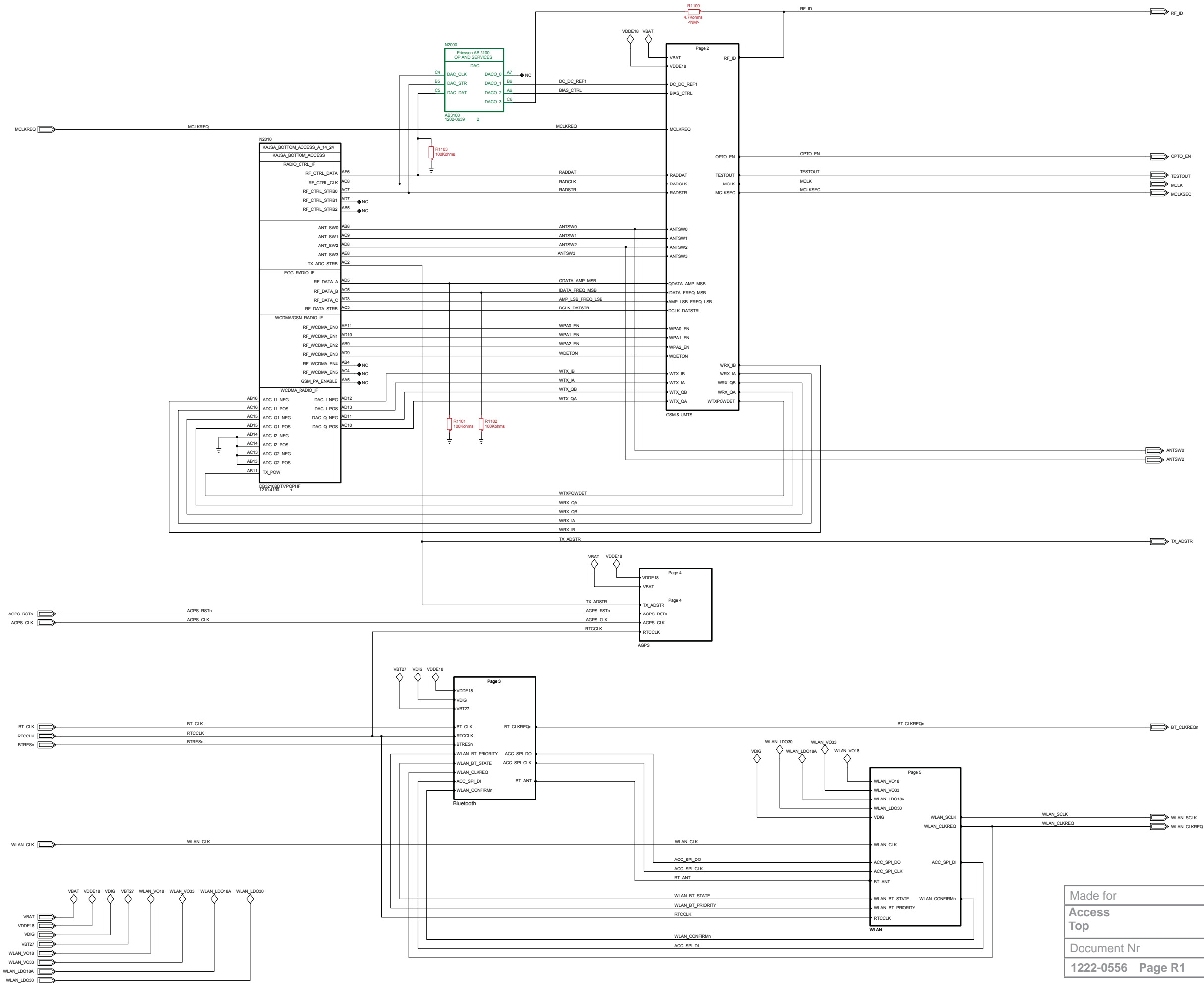
MEASUREMENT POINTS

Made for Imaging Camera	
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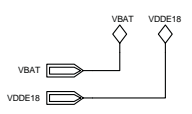
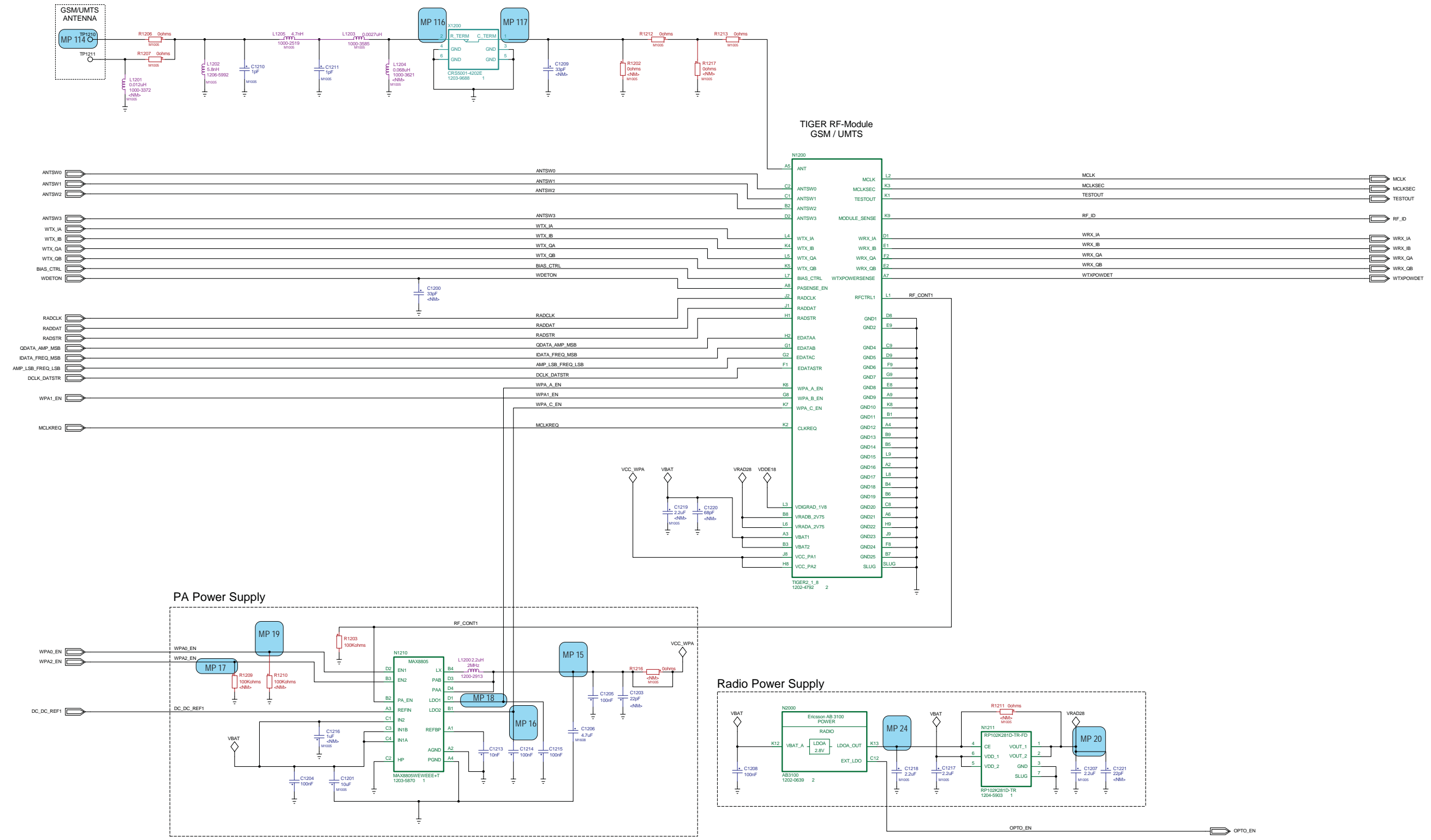


MEASUREMENT POINTS

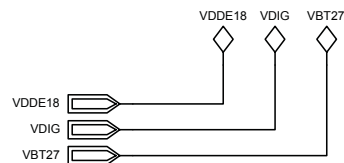
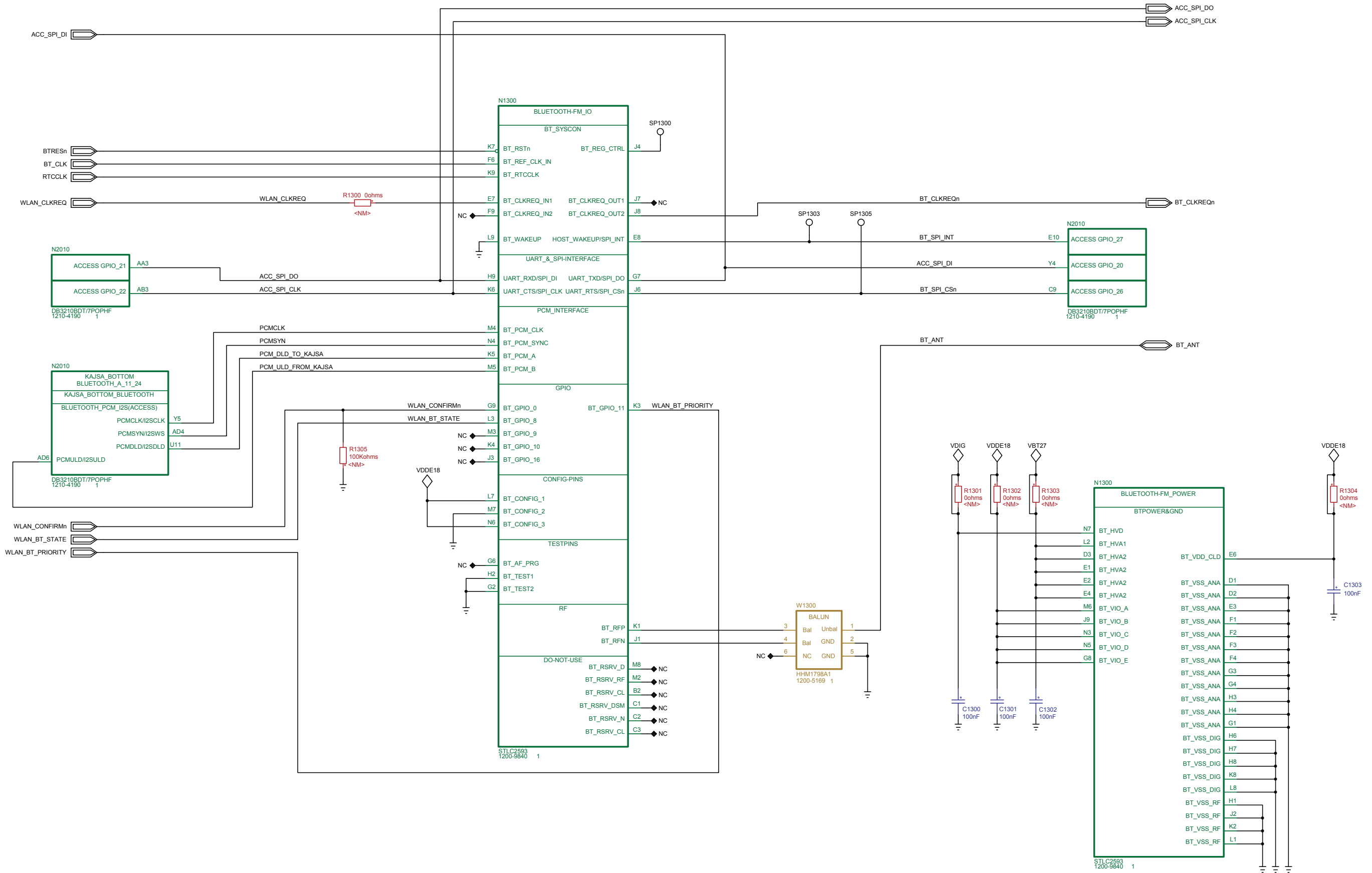
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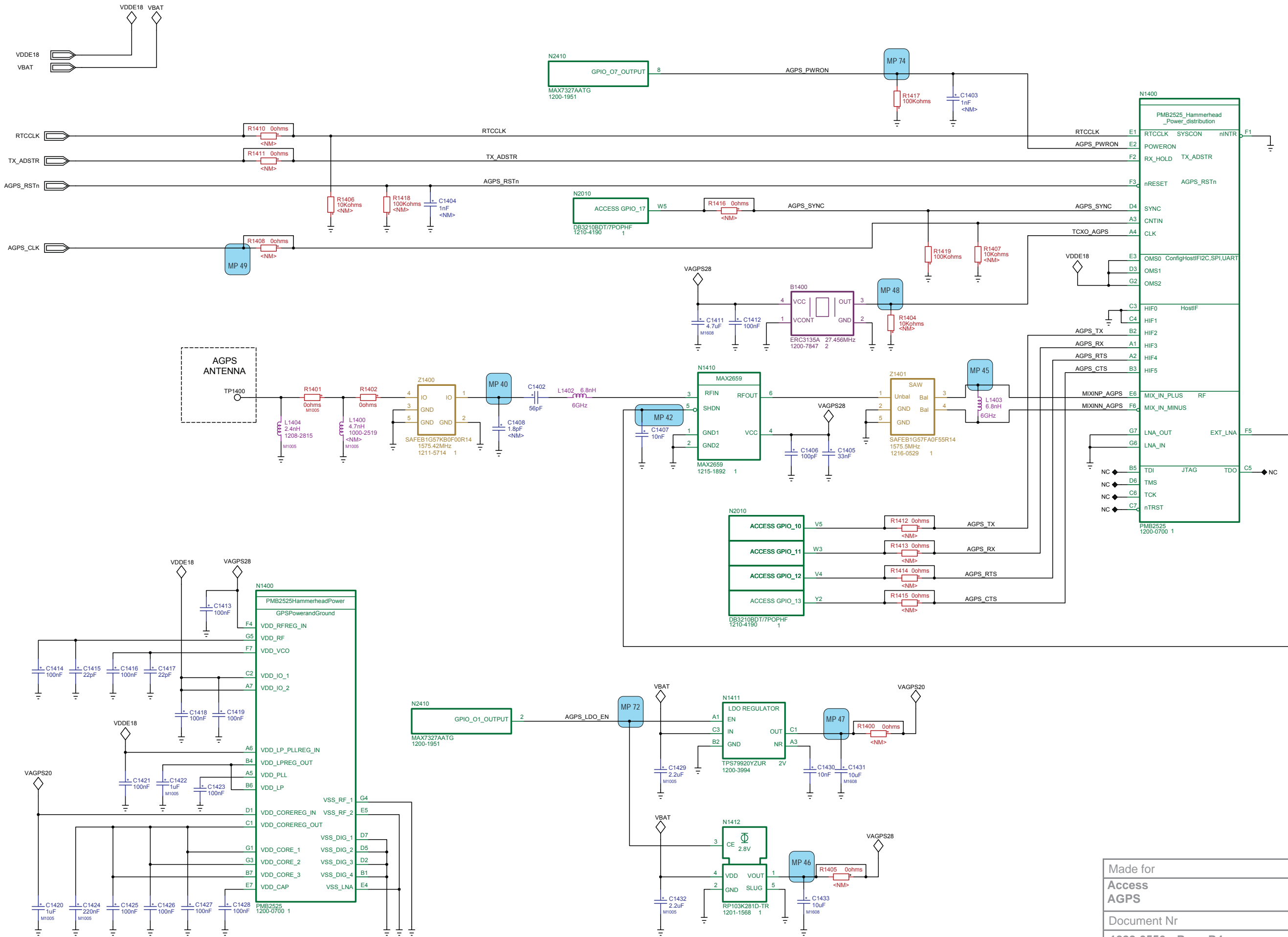
Made for Access Top	
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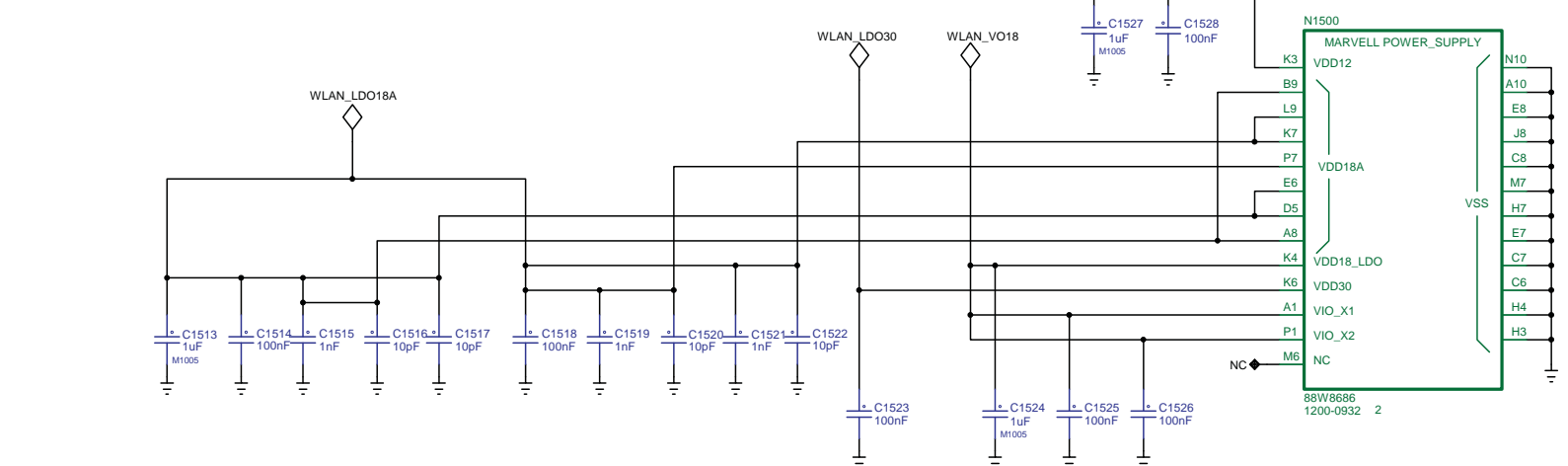
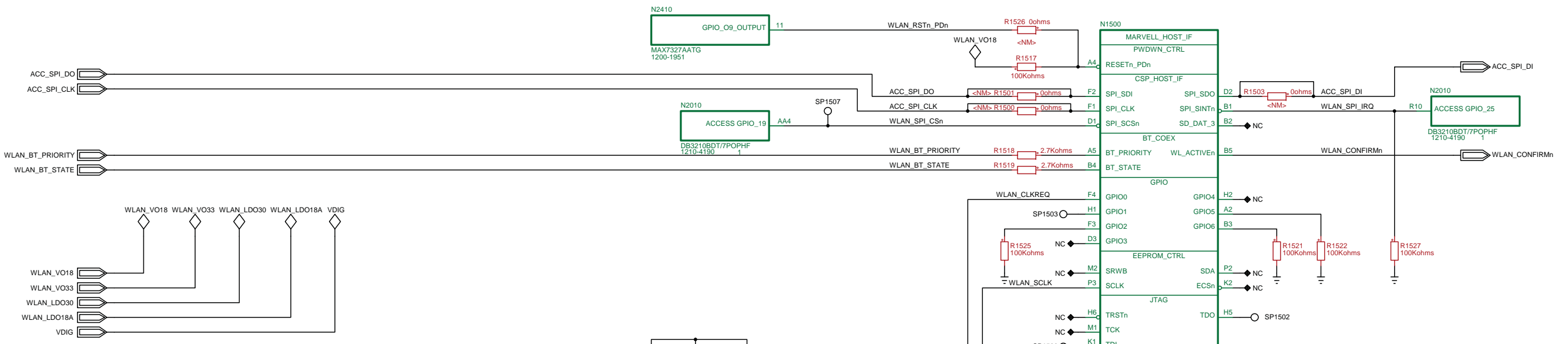
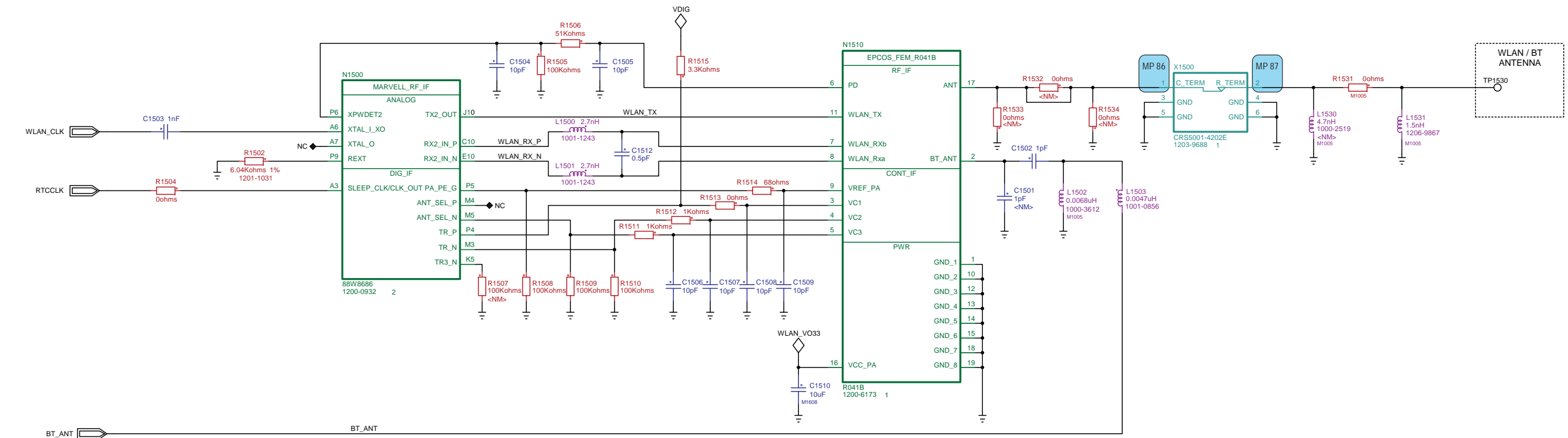
Made for	
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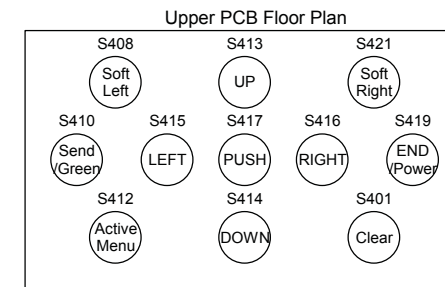
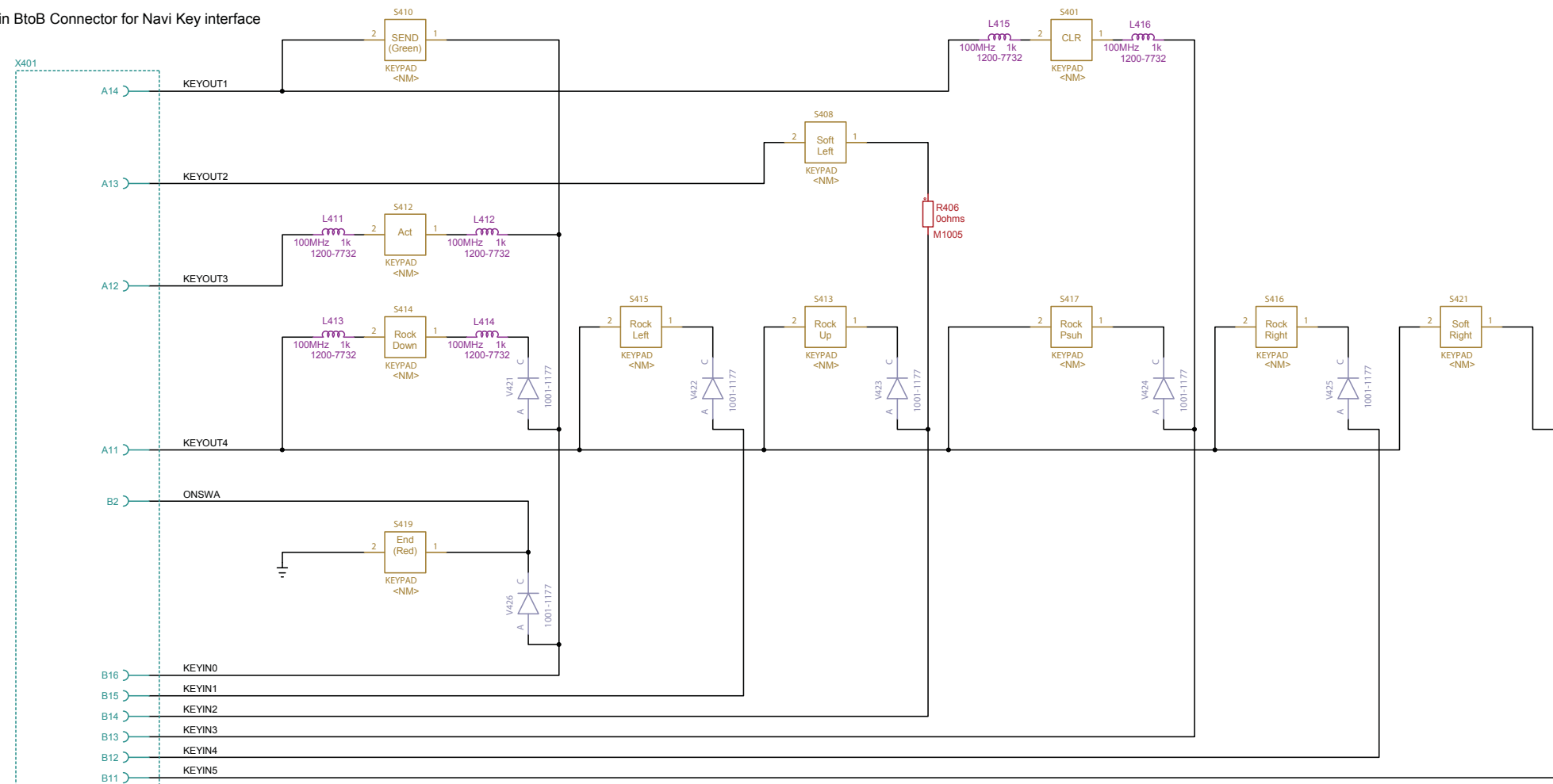


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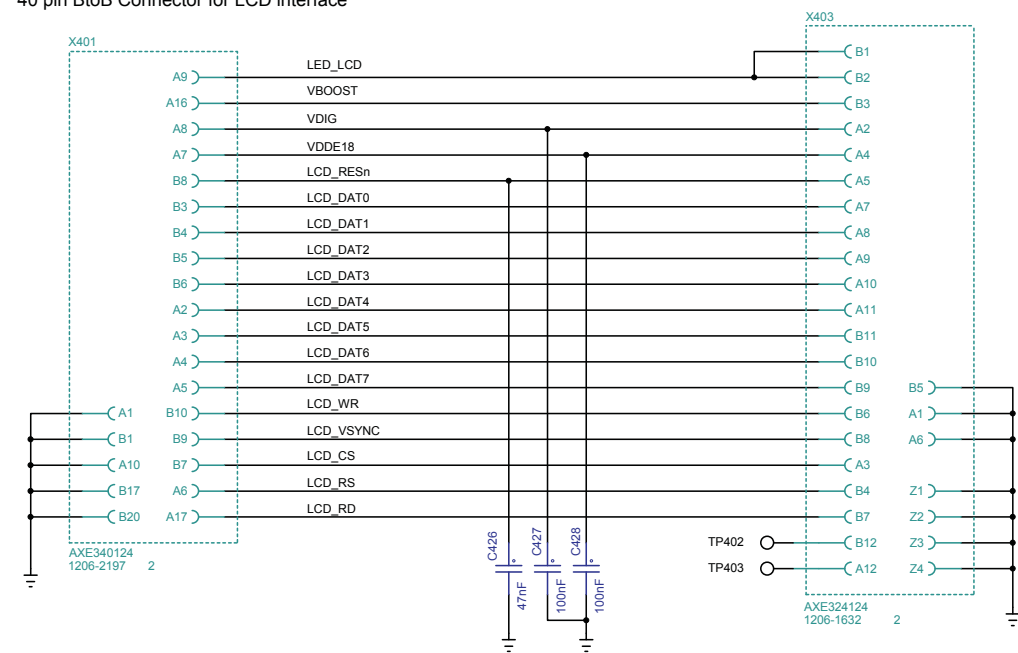
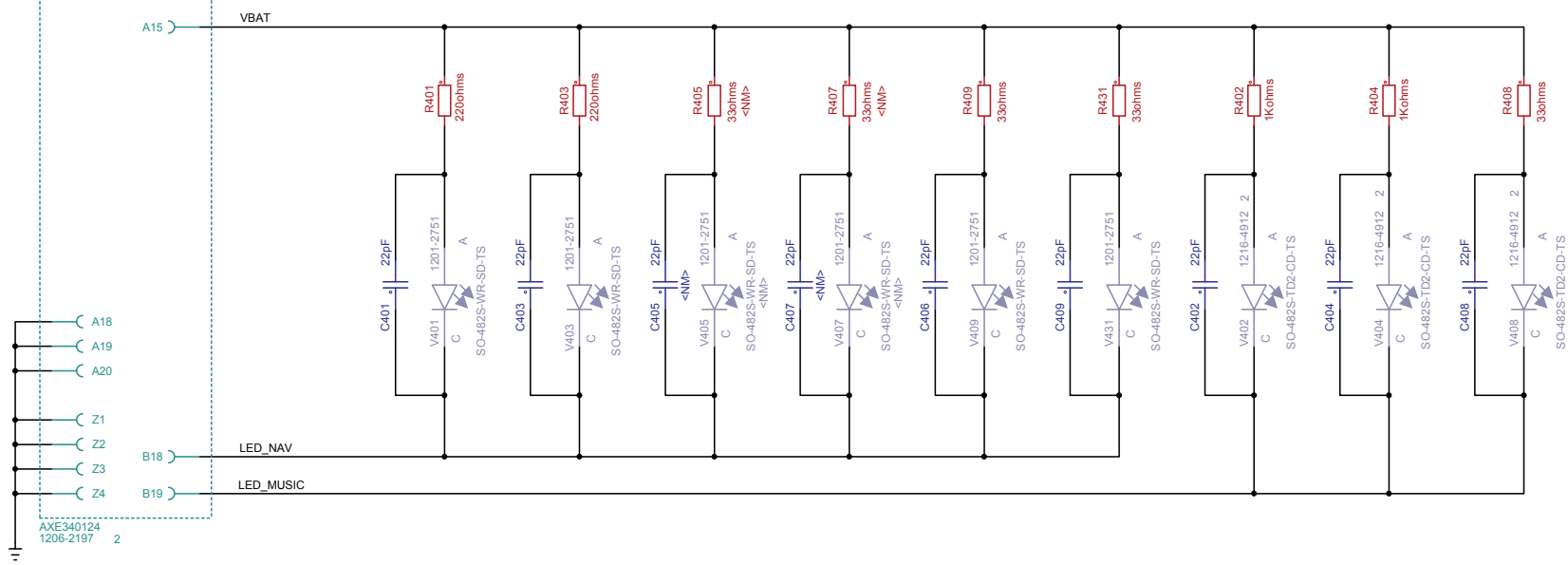


Made for	
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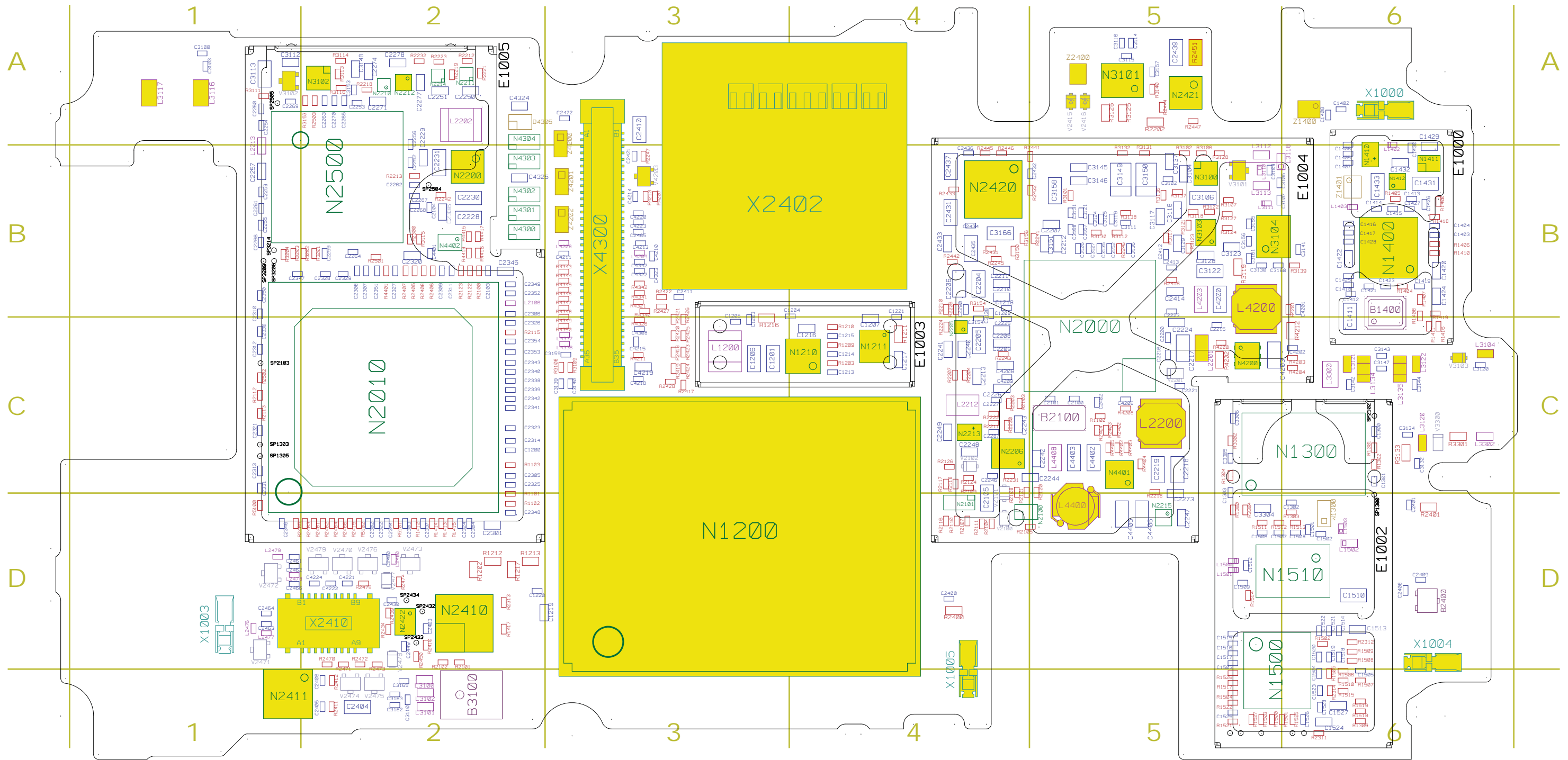
40 pin BtoB Connector for Navi Key interface



40 pin BtoB Connector for LCD interface

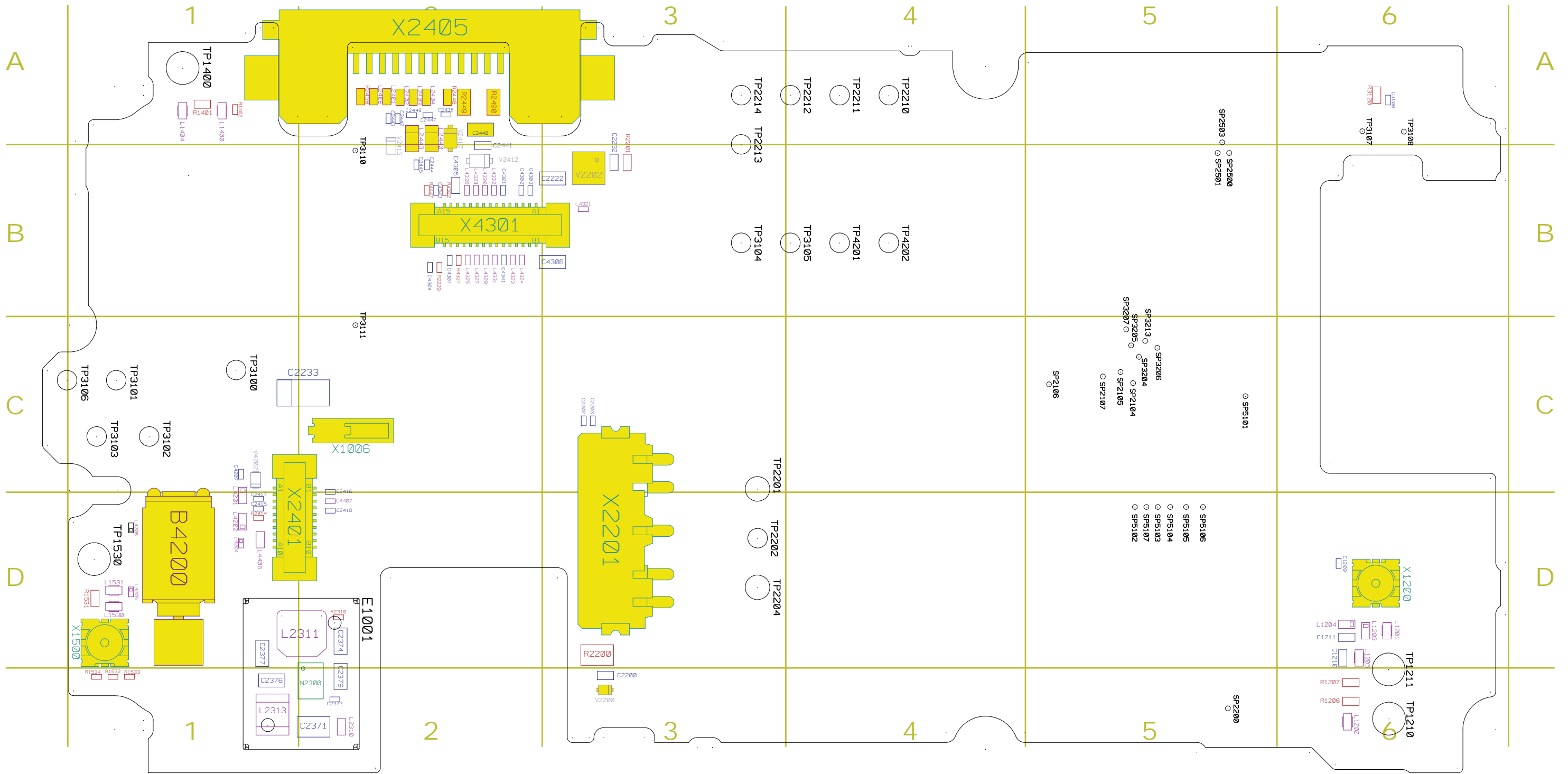


Made for Upper PBA	
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L1200	1200-2913	C3	L3104	1200-0317	C6	L4408	1000-0118	C5	N2212	1215-2684	A2	N4401	1212-3512	C5	R1515	1000-4134	E6	R2123	1000-4034	B2	R2417	1000-0231	C3	R2470	1000-0175	D2	R3118	1000-4049	B5	R4321	1000-0181	B3	V2100	1000-8384	D4	X2402	1200-9764	B3
L1402	1208-6208	B6	L3110	1001-1242	B5	N1200	1210-9870	D3	N2213	1208-4678	C4	N4402	1200-4628	B2	R1517	1000-0376	E5	R2203	1000-0376	C4	R2418	1000-0231	C3	R2471	1000-0175	D2	R3121	1000-4049	B5	R4326	1000-0181	C3	V2101	1000-7477	D4	X2410	1200-6752	D2
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L1500	1001-1243	D5	L3112	1000-0132	B5	N1211	1204-5903	C4	N2215	1201-6460	D5	R1102	1000-0231	D2	R1519	1000-4133	E6	R2210	1000-0231	C3	R2420	1000-0231	C3	R2473	1000-0175	D2	R3123	1000-0231	B5	R4341	1000-0231	B3	V2201	1001-0073	C5	Z1400	1211-5714	A6
L1501	1001-1243	D5	L3113	1000-0132	B5	N1300	1200-9840	C6	N2410	1200-1951	D2	R1103	1000-0231	C2	R1521	1000-0376	E5	R2211	1000-4053	C4	R2421	1000-0231	C3	R2474	1000-0175	D2	R3130	1000-0231	B5	R4342	1000-0231	B3	V2415	1201-8440	A5	Z1401	1216-0529	B6
L1502	1000-3612	D6	L3116	1000-1893	A1	N1400	1200-0700	B6	N2411	1204-5837	E1	R1203	1000-0231	C4	R1522	1000-0376	E5	R2212	1000-0231	A2	R2422	1000-4063	B3	R2475	1000-0175	D2	R3131	1000-0172	B5	R4343	1000-0231	B3	V2416	1201-8440	A5	Z2400	1201-6833	A5
L1503	1001-0856	D6	L3117	1000-1893	A1	N1410	1215-1892	B6	N2420	1200-1694	B4	R1212	1000-0179	D2	R1525	1000-0376	E6	R2222	1000-0249	C4	R2423	1000-4035	C3	R2481	1000-0172	D2	R3132	1000-0172	B5	R4344	1000-0231	B3	V2470	1200-9617	D2	Z4200	1221-4986	A3
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L2201	1000-0118	C5	L3122	1200-0317	C6	N1500	1200-0932	E5	N2500	1200-1414	B2	R1419	1000-0231	B6	R2102	1000-0231	D2	R2313	1000-0231	D2	R2426	1000-4035	C3	R2484	1000-0172	D2	R3153	1000-0231	A2	R4347	1000-0231	B3	V2473	1000-7497	D2			
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L2479	1000-2592	D1	L4208	1000-2592	B3	N2200	1213-9811	B2	N4300	1202-5944	B2	R1510	1000-0376	E6	R2115	1000-0230	C2	R2406	1000-0230	B2	R2439	1000-0377	D2	R2491	1000-0175	D2	R4203	1200-1061	C6	R4417	1000-0181	B2	V3300	1201-2253	C6			
L2480	1000-2592	D2	L4209	1000-2592	B3	N2205	1201-9680	C4	N4301	1202-5944	B2	R1508	1000-0376	D6	R2116	1000-0231	D4	R2407	1000-0388	B2	R2440	1000-0230	B4	R2492	1000-0175	D2	R4204	1000-4160	C6	R4418	1000-0181	B2	V4203	1000-0400	B3			
L3100	1200-0317	E2	L4336	1000-2592	C3	N2206	1201-6517	C4	N4302	1202-5944	B2	R1512	1000-0230	D5	R2117	1000-0231	D4	R2408	1000-0388	B2	R2441	1203-6621	B4	R2493	1000-0175	A2	R4207	1000-0249	B3	R4419	1000-0181	B2	X1000	1202-1053	A6			
L3101	1200-0317	E2	L4337	1000-2592	C3	N2210	1201-9681	A2	N4303	1202-5944	B2	R1513	1000-0181	D6	R2120	1000-0181	C5	R2409	1000-0388	B2	R2442	1000-0240	B4	R2494	1000-0231	B3	R4208	1000-0249	B3	R4420	1000-0231	C3	X1004	1202-1053	D6			

R - Replaceable
See Appendix for more information.



B4200	1218-9713	D1	C2376	1000-0061	E1	C4207	1000-0056	C1	L1404	1208-2815	A1	L2440	1207-2753	A2	L4327	1000-2592	B2	R1207	1000-0179	E6	R3120	1000-0179	A6	X1500	1203-9688	D1
C1210	1000-5941	D6	C2377	1000-0061	D1	C4301	1000-0048	B2	L1531	1206-9867	D1	L2443	1207-2753	A2	L4328	1000-2592	B2	R1401	1000-0179	A1	R4322	1000-0181	B2	X2201	1206-2937	D3
C1211	1000-5941	D6	C2379	1000-0061	E2	C4302	1000-0048	B2	L2310	1200-6898	E2	L4201	1000-0360	D1	L4329	1000-2592	B2	R1402	1000-0181	A1	R4327	1000-0181	B2	X2401	1200-9864	D1
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C2203	1000-0064	C3	C2441	1000-0057	B2	C4304	1000-0048	B2	L2313	1215-3670	E1	L4204	1001-0374	D1	L4331	1000-2592	B2	R2200	1214-4223	D3	V2200	1000-0262	E3	X4301	1200-1733	B2
C2222	1000-0076	B3	C2442	1000-0045	A2	C4305	1000-0051	B2	L2401	1200-0317	A2	L4321	1000-2592	B3	L4332	1000-2592	B2	R2201	1000-4376	B3	V2202	1200-0145	B3			
C2233	1205-9750	C2	C2443	1000-0045	A2	C4306	1000-0076	B3	L2402	1200-0317	A2	L4406	1000-2617	D1	L4407	1000-2592	B2	R2438	1000-0179	A2	V2413	1201-2253	B2			
C2371	1204-0254	E2	C2447	1000-0047	A2	L1202	1206-5992	E6	L2403	1200-0317	A2	L4407	1000-2592	D2	R2448	1000-0179	A2	R2448	1000-0179	A2	V2417	1000-0272	A2			
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C2374	1000-0061	D2	C3109	1000-6062	A6	L1205	1206-5992	D6	L2406	1200-6898	A2	L4326	1000-2592	B2	R2490	1000-0257	A2	R2490	1000-0257	A2	X1200	1203-9688	D6			

R - Replaceable
See Appendix for more information.

W995 Function Overview



General Information

Size

97 x 49 x 15 mm

Weight

113 grams

Colors

Progressive Black
Cosmic Silver
Energetic Red

Screen

Main screen: 262,144 colour TFT, scratch-resistant
Resolution: 240 x 320 pixels
Size: 2.6 inches

Phone memory

Up to 118MB
Memory card support: Memory Stick Micro™ (M2™)

Talk time

GSM/GPRS: Up to 9 hrs
UMTS: Up to 4 hrs

Standby time

GSM/GPRS: Up to 370 hrs
UMTS: Up to 360 hrs

Video call time:

Video call time: Up to 3 hr 30 min

Music listening time:

Up to 20 hrs

Networks

W995:

GSM/GPRS/EDGE 850/900/1800/1900
UMTS/HSUPA 900/2100

W995a:

GSM/GPRS/EDGE 850/900/1800/1900
UMTS/HSUPA 850/1900/2100

Note! The Network support depends on variant and market.

Features

Camera

8.1 megapixel camera
Auto focus
Up to 16x digital zoom
Face Detection
Photo fix
Photo flash
Video light
Picture blogging
Video blogging
Video recording
Image and video stabilizer
PictBridge

Music

Walkman™ player
Clear Stereo
Clear Bass
Album art
3.5 mm audio jack
Stereo speakers
PlayNow™
SensMe™
Shake Control
TrackID™
Bluetooth™ stereo (A2DP)
Music tones (MP3/AAC)

Web

Access NetFront™ Web browser
Web feeds
Photo feeds

Communication

Polyphonic ringtones
Speakerphone
Vibrating alert
Video calling
Note! The Video Call support depends on variant and the market.

Messaging

Email
Text messaging (SMS)
Chat View
Picture messaging (MMS)
Exchange ActiveSync®
Instant messaging
Predictive text input
Sound recorder

Design

- Auto rotate
- Picture wallpaper
- Wallpaper animation

Entertainment

- Media
- YouTube™
- 3D games
- Motion gaming
- Java
- FM radio with RDS
- Video streaming
- Video viewing
- Walk Mate

Organiser

- Alarm clock
- Calculator
- Calendar
- Flight mode
- Notes
- Phone book
- Stopwatch
- Tasks
- Timer

Location-based services

- aGPS
- Geo tagging of photos
- Google Maps™
- Wayfinder Navigator (3-month trial version)

Connectivity

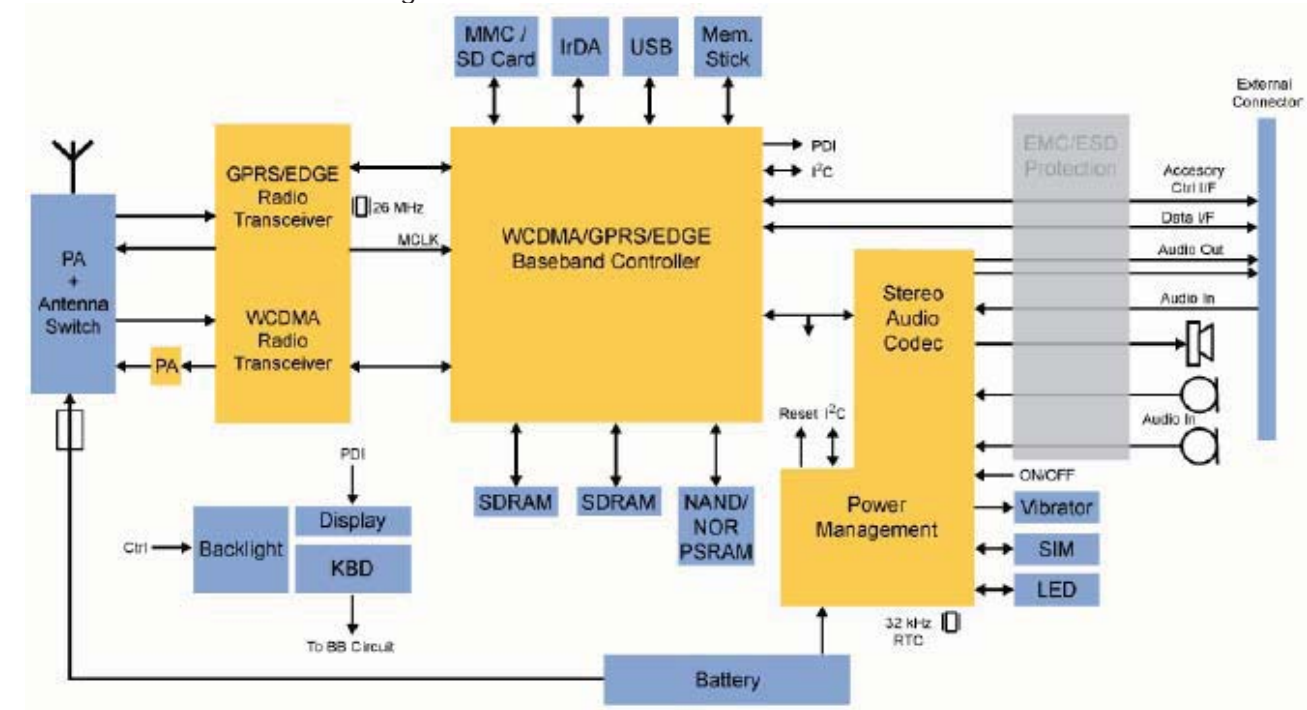
- Bluetooth™ technology
- Modem
- Synchronization
- DLNA Certified™
- Wi-Fi™
- USB mass storage
- USB support

Hardware Overview

Platform Information

The W995 and W995a are using the U365 platform provided by Ericsson Mobile Platform (EMP).

The U365 Platform Block Diagram Overview:



Baseband Part

Analog Baseband Controller N2000 (Vera)

This component is not replaceable on SL 4 because Baseband calibration is required. The analog baseband controller is the main power management circuit. It has converters and regulators that generate a number of supply voltages, each optimized for its load.

The analog baseband controller is a mixed digital and analog device that supports the following circuitry:

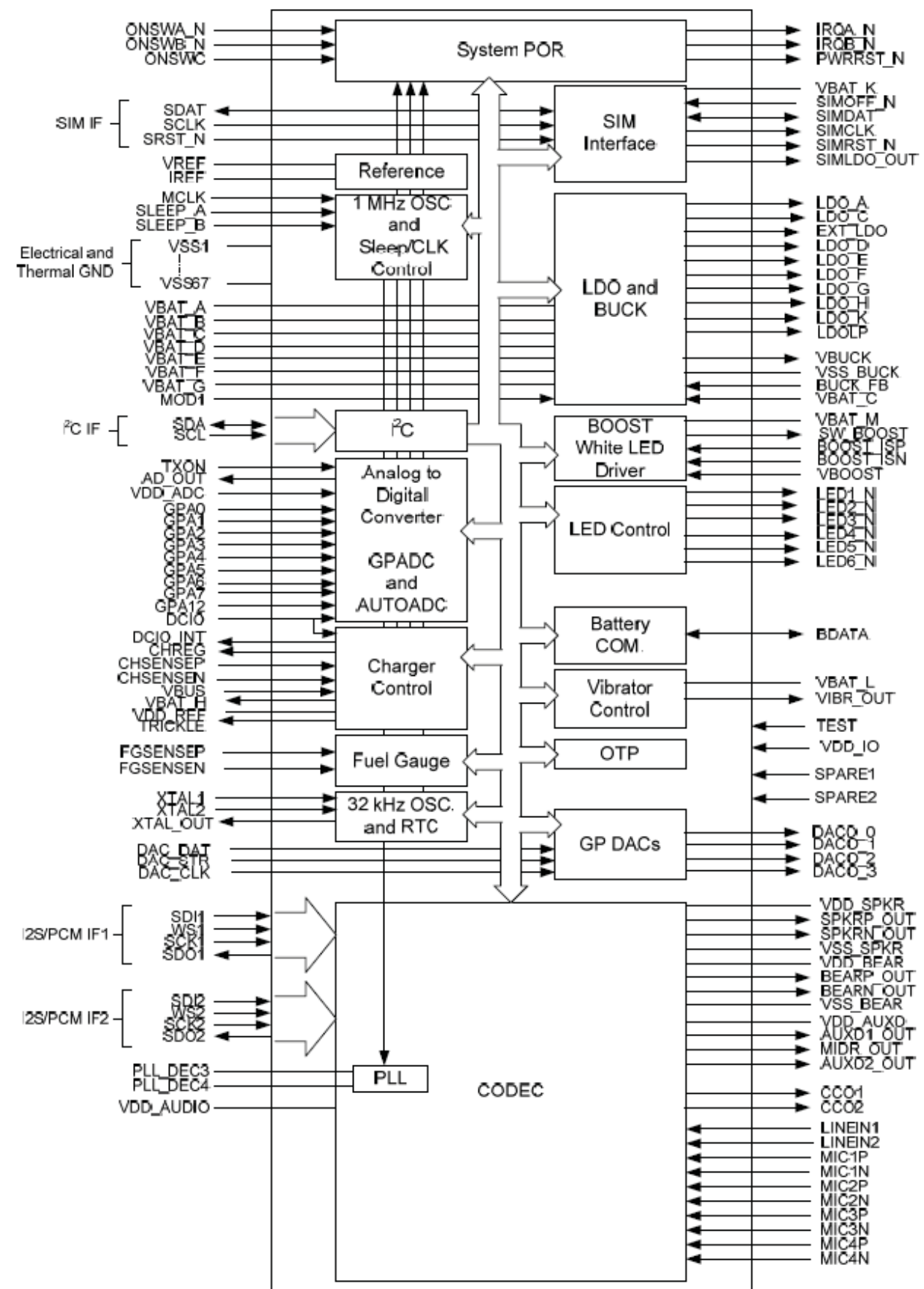
- Power management circuitry
- Voltage regulation circuitry
- Eight Low Dropout (LDO) regulators and low power regulator
- 600 mA integrated Buck regulator
- Boost step-up DC/DC converter for White Light Emitting Diode (WLED) driving
- Battery charging and communication circuitry
- Battery fuel gauging circuitry
- Analog-to-Digital Converter (ADC)
- Digital-to-Analog Converter (DAC)
- SIM interface
- Six programmable LED drivers
- Accurate band gap reference
- Vibrator driver
- Real Time Clock (RTC)
- 8-byte One-Time Programmable (OTP) memory
- Pulse Code Modulation (PCM) voice coder/decoder
- PCM audio coder/decoder
- Microphone interface
- Stereo line input
- Earphone driver
- Earpiece driver
- 8-Ω speaker driver / Stereo line output

The analog baseband controller is controlled by an I2C™ interface. It also comprises the main power management circuits, equipped with a number of converters and regulators for generating the required supply voltages.

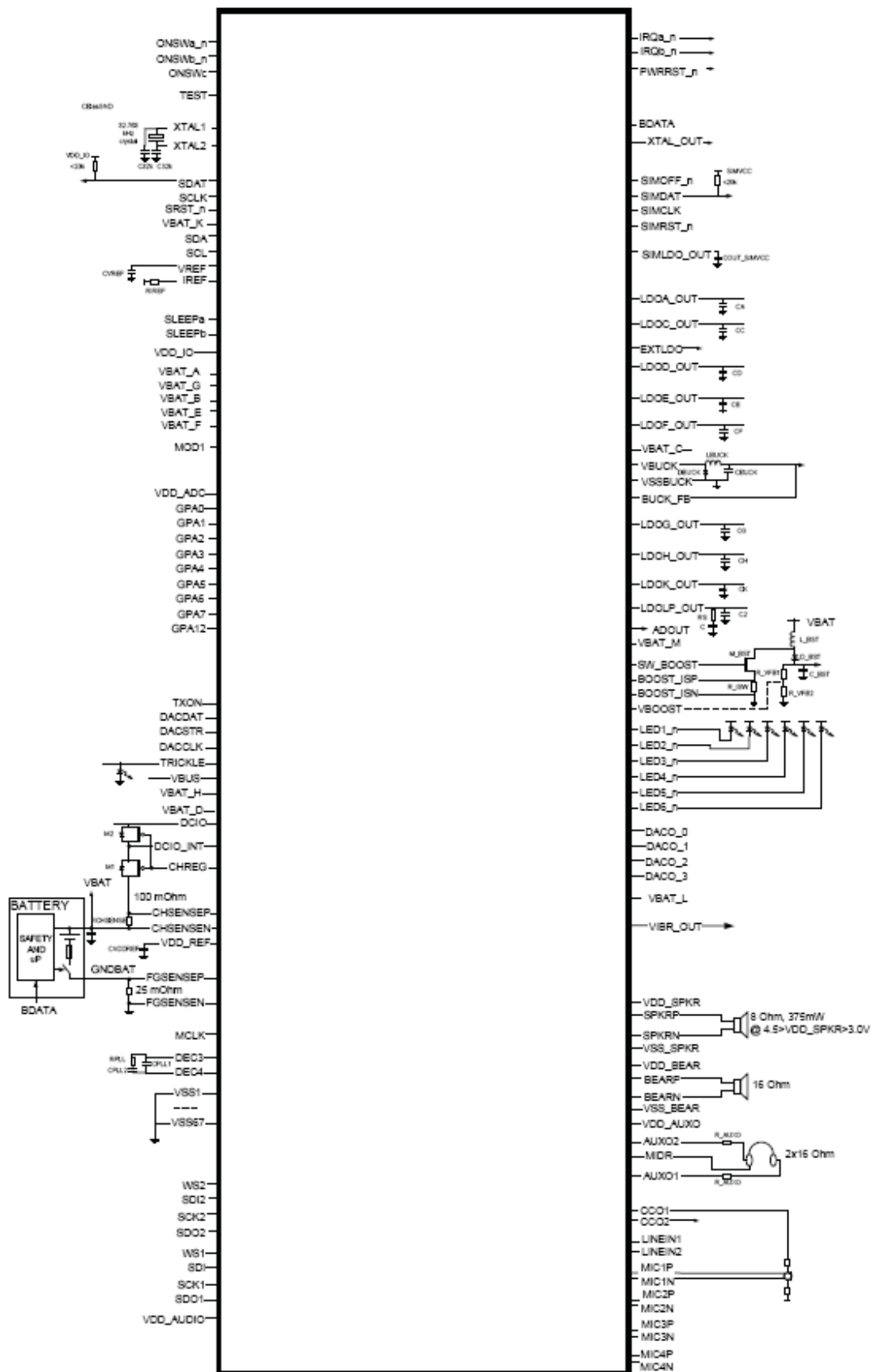
The analog baseband controller supports the following features:

- Lithium battery
- Full audio CODEC functionality
- Supports stereo audio sampling rates of 8/16 kHz voice coding/decoding and 44.1/48 kHz for high quality audio recording/playback (for example MIDI and MP3 applications)
- Double CODEC I2S/PCM interfaces
- Flexible microphone interface
- Integrated headphone amplifiers
- Integrated earpiece amplifiers
- Integrated speaker amplifier
- Integrated flexible audio mixing functionality
- Boost driver capable of driving up to four WLEDs in series, supplying 50 mA
- Designed to meet power management demands of GSM and WCDMA
- Automated power management ADC to relieve CPU
- Battery identification and communication
- Single-terminal charger and accessory power interface for compact connector design
- Integrated USB charging
- OTP memory
- Integrated hardware fuel gauge to accurately monitor battery capacity
- Reduced number of external components as a result of integrated programmable LED and vibrator drivers
- 32 kHz real time clock with alarm wake up capability
- Designed to support two host controllers.

Functional Blocks of the Analog Baseband Controller:



Connection Diagram of the Analog Baseband Controller:



Charger Control

A programmable charger is used for battery charging. Limits can be set for the output voltage at CHSENSE- and the output current from DCIO through the sense resistor to CHSENSE-. The programmable charger is enabled or disabled by the assertion/negation of the external signal DCIO. Parts of the programmable charger are activated and deactivated depending on the level of VBAT. The rest of the programmable charger is activated and deactivated through I2C.

The programmable charger supports the following functions:

- Constant current charging
- Constant voltage charging
- Trickle charging
- PWM controlled charging
- Over-voltage and over current detection
- Watchdog termination
- DCIO assertion/removal detection
- Voltage and current measure functions
- Low resistive path (reverse mode)

The programmable charger is able to control the voltage and limit the current to a load seen at CHSENSE-. The programmable charger can also be run in PWM mode to turn the charging on and off in accordance with the particular period and duty cycle. When the charging is on, it is set to the current and voltage selected by I2C.

A low resistive path from VBAT to DCIO can be formed when DCIO is not detected. When this setting is done in the appropriate registers, a lowering of CHREG to 0 V turns on the external pass device. The pass device is automatically turned off when an external source is detected on DCIO, or when the watchdog termination block times out. The watchdog termination block must be active when the external switch is enabled, both in normal charging mode and in the low resistive path mode. The watchdog is set through the serial interface, and if it has not been set again before timeout, the watchdog turns off the external switch. The watchdog is disregarded during trickle charging. When no battery is present, the system can be booted and supplied from DCIO by applying the correct voltage on DCIO.

USB Charger

The analog baseband controller contains a standalone USB charger. The USB charger has a separate input and incorporates full functionality during low VBAT.

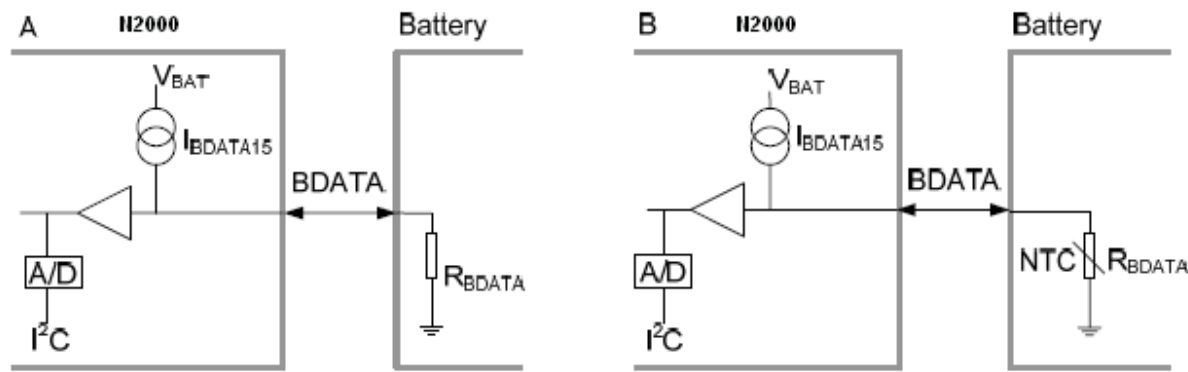
The programmable charger supports the following functions:

- Trickle charging
- Constant current charging
- Watchdog termination
- Trickle LED indication
- VBUS assertion/removal detection

Resistance Identification and Temperature Measurement

The resistance identification mode utilizes the constant current source to feed the battery data output while monitoring the voltage at the battery data node with general purpose ADC the conversion is started through I2C.

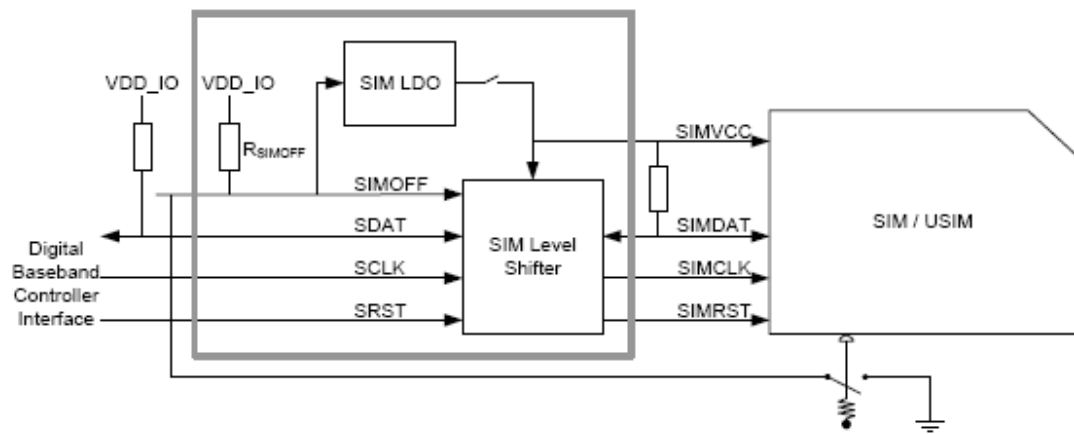
Resistance Identification (A) and Temperature Measurement (B):



SIM Interface

The SIM interface supplies level is shifting between the digital baseband controller and the SIM/USIM card. Moreover, hard-wired SIM deactivation functionality manages removal of a SIM card that has not been powered down.

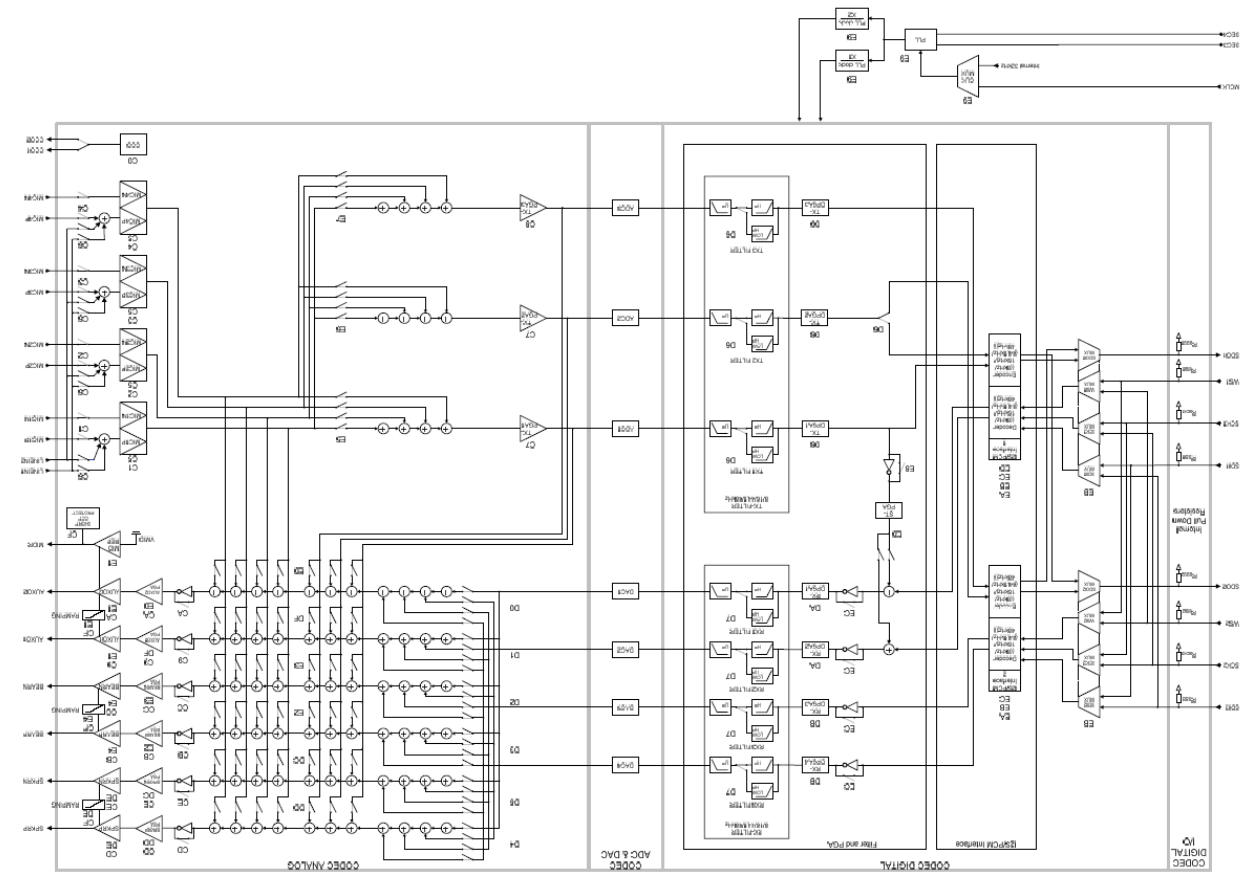
Block Diagram of the SIM Interface:



CODEC Overview

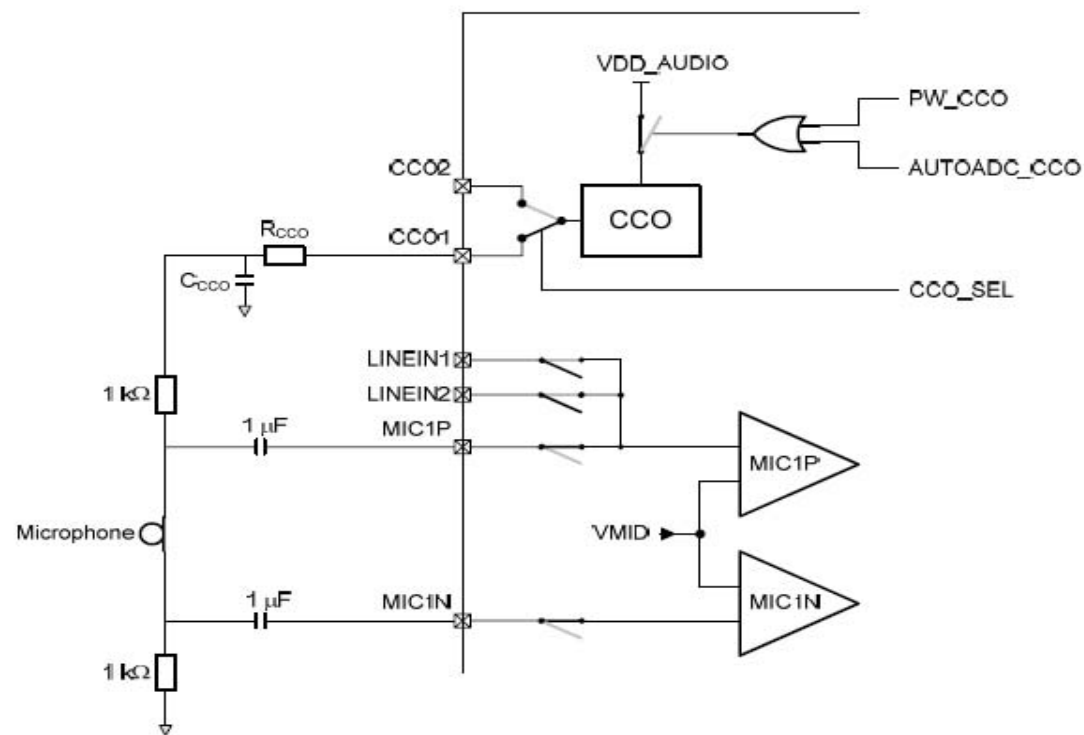
The CODEC is encoding analog audio signals and analog voice signals into digital signals using Analog to Digital converters (ADCs). This is done in the coder section of the CODEC, also named the TX path (transfer section). The CODEC is also decoding digital audio signals and digital voice signals into analog signals using DACs. This is done in the decoder section of the CODEC, also named the RX path (receiver section).

CODEC Block Schematic:



CODEC CCO Voltage Source

There is an internal voltage source CCO that provides the necessary drive current for electret microphones. The voltage source is I²C programmable to 2.2 V or 2.4 V. The source can be disabled during standby. A typical use case with a microphone connected to MIC1 and the CCO is shown in picture below.



Earphone Amplifier

The earphone amplifiers (BEARP and BEARN) are mainly intended to be differentially configured and drive a low impedance dynamic transducer (earpiece) but they can also be single ended configured. The BEARP and BEARN amplifiers can be powered down by the I2C. The amplifiers can exhibit high impedance to 1.4V or low impedance to ground when powered-down. Fifty-one gains are available for BEARP and BEARN: from +15dB down to -60dB in 1.5dB steps. When the BEARP and BEARN outputs are operating in differential mode, an I²C selectable bit must invert one of the inputs.

Speaker Amplifier

The speaker amplifiers, SPKRP and SPKRN, are intended to drive a low impedance (8Ω) speaker in a differential mode or to be used as a stereo configured line output amplifier supporting external high power amplifiers. The output buffer shall exhibit low impedance to ground when powered-down and the current consumption shall be minimal. When the SPKRP and SPKRN outputs are operating in differential mode, an I²C selectable bit must invert one of the inputs.

**Digital Baseband Controller (CPU)
N2010 (Kajsa)**

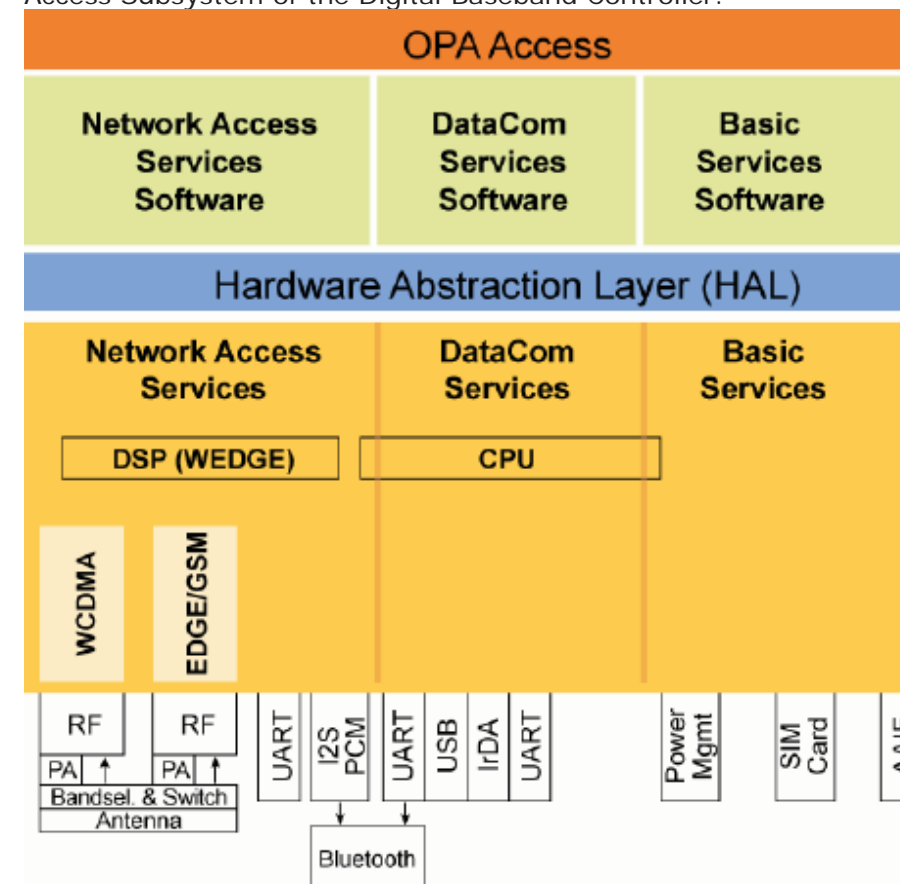
This component is not replaceable on SL 4 because Baseband calibration is required. The Digital Baseband Controller is divided in two subsystems: Access and Application

Access Subsystem

All modem functionality in the digital baseband controller resides in the Access subsystem. This includes EDGE/GPRS/GSM interface, WCDMA interface, USB, IrDA, and other peripheral modules. The control CPU is an ARM926 and a DSP is used for signal processing and layer one control code.

The main communication between the blocks in the Access subsystem is done through the Advanced High-performance Bus (AHB) matrix, which is a set of control buses connecting the different parts together. A block called Syscon is responsible for distributing clocks and resets to all parts of the Access subsystem. This block is under SW control. The Access subsystem is connected to the Shared EMIF, an interface for communication with an external SDRAM. The Shared EMIF is shared between the Access subsystem and the Application subsystem.

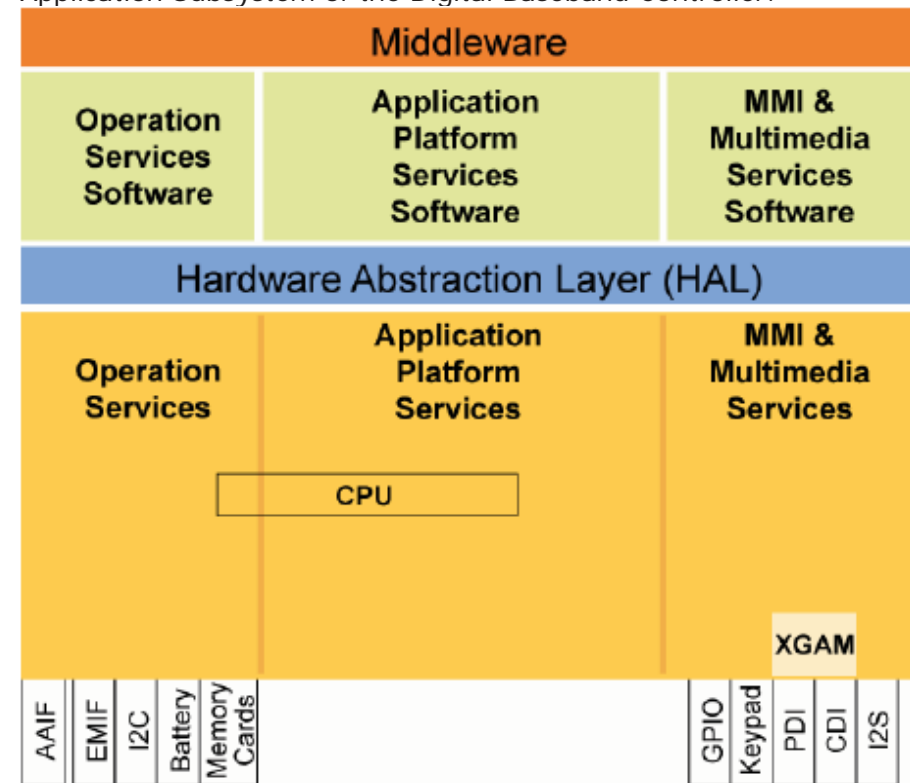
Access Subsystem of the Digital Baseband Controller:



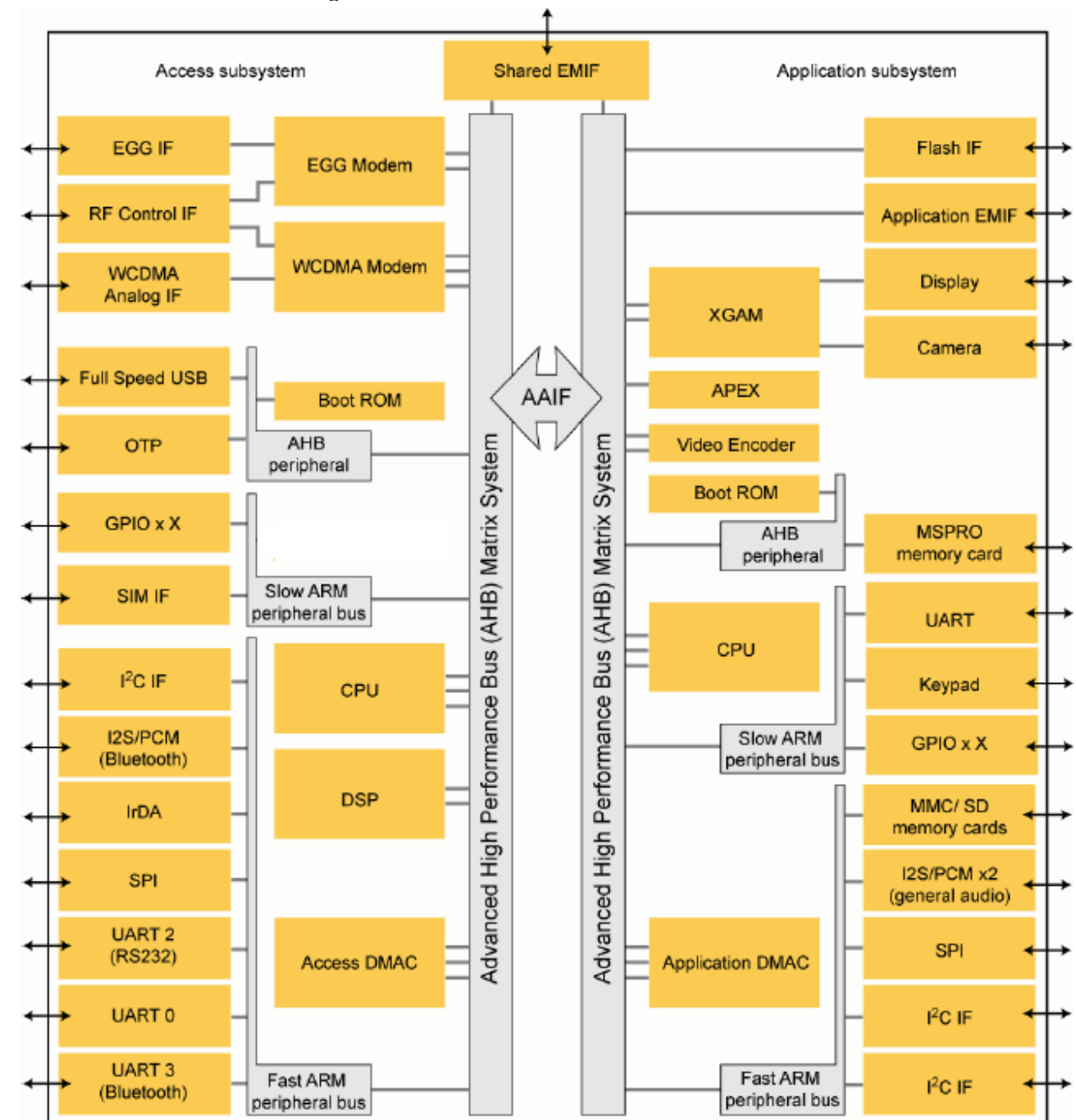
Application Subsystem

The Application subsystem contains functionality related to functions such as MMI, graphics, audio and memory media. The control CPU is an ARM926 with three external memory interfaces, one shared with the Access subsystem and two dedicated for the Application subsystem. The Application subsystem contains several blocks. The main communication between the blocks is done through the Advanced High performance bus (AHB) matrix, which is a set of control buses connecting the different parts. A block called Syscon is responsible for distributing clocks and resets to all parts of the Application subsystem. This block is under SW control. The Application subsystem is connected to the Shared EMIF that is used for code execution or data storage. In addition, a dedicated EMIF that support SDRAM or static memory like NOR, PsRAM or NAND are also available. The Application EMIF is a general interface for communication with, for example external SDRAM, PSRAM, NOR flash, NAND flash and companion chips

Application Subsystem of the Digital Baseband Controller:



The functional blocks of the Digital Baseband Controller:



Keypad

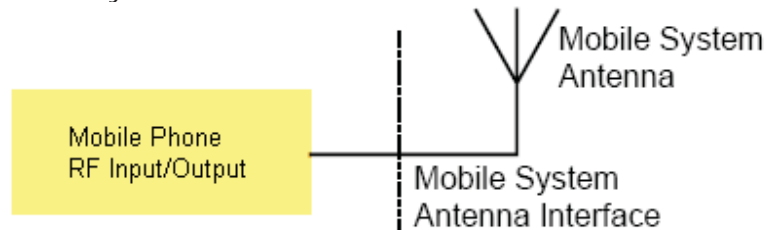
The keypad interface block supports up to 30 keys with 65 columns and 6 rows and operates in both scan and idle mode. The keypad scan is performed by software. Any transition in the state of the column inputs is written directly to the register. The keypad interface differentiates between single key presses, simultaneous presses of any keys with a function key, and any key releases. The period between successive scans is programmable over the range 5 ms to 80 ms, in 5 ms steps. During scan mode, the keypad generates an interrupt whenever a valid keypad state change occurs (including a release of any pressed keys). The scan function is disabled during system power-up. The keypad is able to detect at least four simultaneous key presses. Not all combinations are supported.

Radio Part

Antenna

The mobile system antenna interface connects the Wideband Code Division Multiple Access (WCDMA) and Global System for Mobile Communication (GSM) input/output to the antenna of the Mobile Phone. It is a bi-directional RF interface containing signals in the range 800 MHz to 2.2 GHz. The mobile system antenna interface is the interface between the Mobile Phone Radio Frequency (RF) input/output and the mobile system antenna. The interface handles the GSM 850, EGSM 900, GSM 1800, GSM 1900 and WCDMA Band I, II and V, RF inputs/outputs.

Mobile System Antenna Interface:



Radio Module N1200 (Tiger)

Front End

The Front End block connects the proper block in the radio system to the antenna. The Front End has two inputs for EDGE/GSM/GPRS, one for low band (850/900 MHz) and one for high band (1800/1900 MHz). The EDGE/GSM/GPRS power amplifier output is filtered by the low pass filter in the Front End and then connected to the antenna through a switch. In receive mode, the EDGE/GSM/GPRS signal from the antenna passes through the switch to one of the four receive SAW filters. The SAW filter provides receive band selectivity. In GSM/GPRS/EDGE systems, transmit and receive operations are divided in time and the switch connects the proper block in accordance with the mode of operation (that is, transmit or receive; one at a time).

In WCDMA the transmit outputs from the WCDMA transceiver are filtered by an external SAW filter that cleans up the spectrum. The SAW filter output is connected to the power amplifier, one for each band. For power control, a sample of the transmit output is taken by a directional coupler and converted to a DC level by the power detection circuit. This signal is used to control the transmitter output power. The transmit signal passes through an isolator and then a duplexer. The duplexer output is selected by the switch in the Front End for connection to the antenna. In WCDMA receive mode the signal from the antenna is switched by the Front End to the correct duplexer. The output from the duplexer is connected to the LNA input in the WCDMA receiver.

Transceiver

The transceiver is a multi-mode transceiver for WCDMA/EDGE/GPRS/GSM. The EDGE/GPRS/GSM part of the transceiver use a digital baseband interface that is shared between received and transmitted data. The receive interface is based on I and Q data and the transmitter interface is based on envelope and frequency data. The WCDMA part of the transceiver use differential analog in-phase and quadrature-phase interfaces, which is an IQ-interface, in the receiver and the transmitter data paths.

Frequency Generation

The 26 MHz reference signal is used as the reference for the on-chip synthesizers. To cover the required frequency range, the integrated Voltage Controlled Oscillator (VCO) operates at twice the frequency for band 1800/1900/2100, and at four times the desired frequency for band 800/900. The two synthesizers are controlled through the serial bus from the access side of the digital baseband controller.

EDGE/GPRS/GSM Transmitter Part

Polar modulation transmitter architecture based on the direct phase/frequency modulation/synthesizer architecture is implemented for GSM, GPRS and EDGE. This architecture has the capability of generating both the GSM/GPRS constant envelope GMSK modulation and the linear EDGE 8-PSK modulation in a very cost efficient way. The motivation for a polar modulation transmitter architecture compared to traditionally linear architectures is to reduce the output noise (thus eliminating the need for off-chip filters) reduce the power consumption by utilizing non-linear switching analog signal processing blocks, and to eliminate the need for an RF isolator.

In brief, the phase/frequency modulator in this polar modulation architecture is a sigma-delta controlled fractional-N frequency synthesizer with an additional frequency insertion point after the loop filter at the input of the VCO. The Phase-locked Loop (PLL) has two information inputs: the divider ratio in the feedback path and a direct path to the VCO. The phase locked loop generates the radio frequency carrier including the phase modulation information at the desired channel frequency.

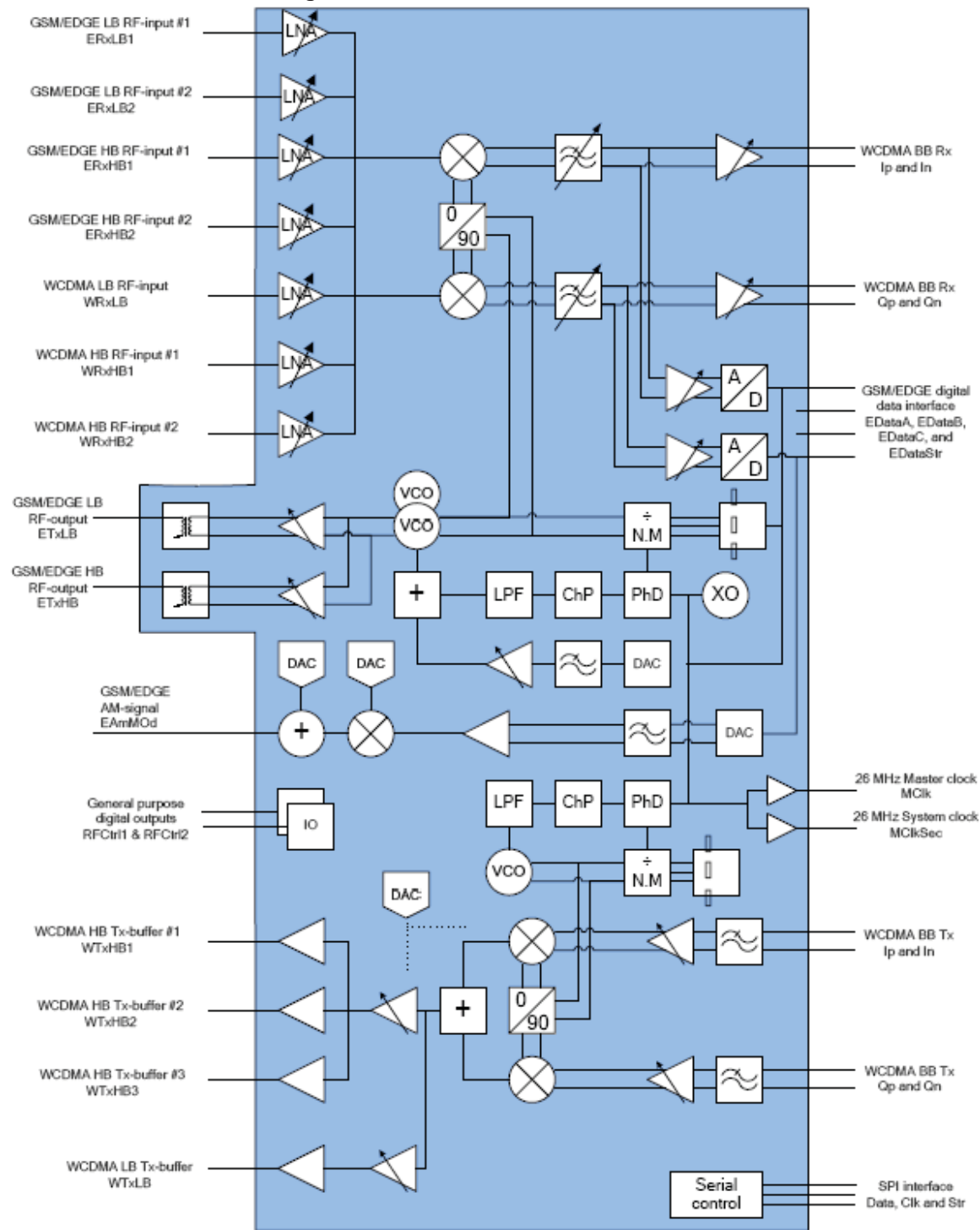
WCDMA Transmitter Part

The WCDMA transmitter architecture is an on frequency linear direct up-conversion IQ-modulator. The in-phase and quadrature-phase reconstruction filters are fully integrated and a programmable gain amplifier implements the gain control. An external SAW filter between the WCDMA circuit and the power amplifier is used to improve noise performance. After the power amplifier, the signal is sent through an isolator and through the duplex filter, which directs the transmit signal to the antenna connector through the antenna switch. The supply voltage and bias of the power amplifier are adapted depending on the output power to achieve high efficiency at every transmitter power level. A high efficiency DC/DC converter regulates the supply voltage and the bias operation point is controlled by a D/A-converter in the WCDMA radio circuit.

Receiver Part

The receiver architecture is a direct down-conversion zero-IF receiver with integrated low-pass filters. The complete receiver with seven Low Noise Amplifiers (LNAs), one for each supported band, is integrated on chip. After the down-conversion, the in-phase and quadrature-phase components are low pass filtered and if the receiver is in EDGE/GPRS/GSM mode the signals are fed to the integrated high dynamic range sigma-delta A/D-converters.

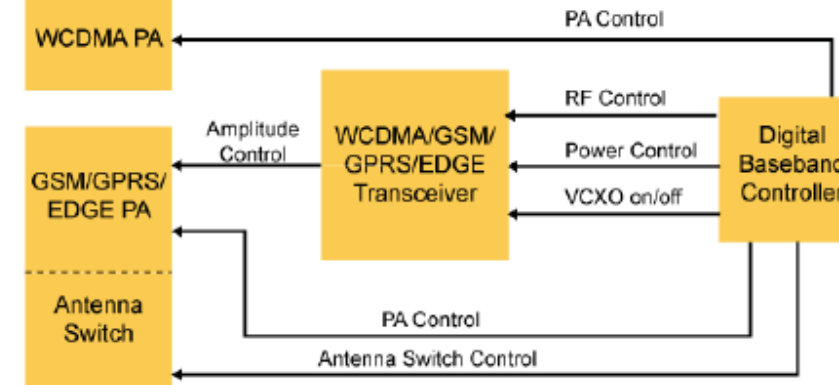
Ericsson RF 3300 Block Diagram:



RF System Control

The access side of the digital baseband controller controls the overall radio system. In both EDGE/GSM/GPRS and WCDMA air interface mode, the digital baseband controller controls the radio system through a three-wire serial bus. The digital baseband controller also manages PA band control and the antenna switch mechanism in the front end module. The 26 MHz VCXO clock residing in the transceiver is turned on only when required and initiated by the digital baseband controller.

The control flow for the RF system:



EDGE/GPRS/GSM

TX Frequency, Channel and Power Level Range:

GSM 850:

TX Frequency Range: 824,2 MHz – 848,8 MHz
Channel Range TX: 128 – 251
Power Level: Min 19 – Max 5

GSM 900:

TX Frequency Range: 890,2 MHz – 914,8 MHz
Channel Range TX: 1 - 124
Power Level: Min 19 – Max 5

EGSM 900:

TX Frequency Range: 880,2 MHz – 889,8 MHz
Channel Range TX: 975 - 1023
Power Level: Min 19 – Max 5

DCS 1800:

TX Frequency Range: 1710,2 MHz – 1784,8 MHz
Channel Range TX: 512 – 885
Power Level: Min 15 – Max 0

PCS 1900:

TX Frequency Range: 1850,2 MHz – 1909,8 MHz
Channel Range TX: 512 - 810
Power Level: Min 15 – Max 0

RX Frequency and Channel Range:

GSM 850:

RX Frequency Range: 869,2 MHz – 893,8 MHz
Channel Range RX: 128 – 251

GSM 900:

Frequency Range: 935,2 MHz – 959,8 MHz
Channel Range RX: 1 - 124

EGSM 900:

RX Frequency Range: 925,2 MHz – 934,8 MHz
Channel Range RX: 975 – 1023

DCS 1800:

RX Frequency Range: 1805,2 MHz – 1879,8 MHz
Channel Range RX: 512 – 885

PCS 1900:

RX Frequency Range: 1930,2 MHz – 1989,8 MHz
Channel Range RX: 512 - 810

WCDMA

Note! The WCDMA Network support depends on variant and market.

TX and RX Frequency and Channel Range

Band I:

Channel Range TX: 9612 - 9888
TX Frequency Range: 1920 – 1980 MHz
Channel Range RX: 10562 - 10838
RX Frequency Range: 2110 – 2170 MHz

Band II:

Channel Range TX: 9262 - 9538
TX Frequency Range: 1850 – 1910 MHz
Channel Range RX: 9662 - 9938
RX Frequency Range: 1930 – 1990 MHz

Band IV:

Channel Range TX: 1312 - 1513
TX Frequency Range: 1710 – 1755 MHz
Channel Range RX: 1537 – 1738
RX Frequency Range: 2110 – 2155 MHz

Band V:

Channel Range TX: 4132 – 4233
TX Frequency Range: 824 – 849 MHz
Channel Range RX: 4357 – 4458
RX Frequency Range: 869 – 894 MHz

Band VIII

Channel Range TX: 2712 – 2863
TX Frequency Range: 880 – 915 MHz
Channel Range RX: 2937 – 3088
RX Frequency Range: 925 – 960 MHz

Bluetooth and FM Radio

The Bit/FM Radio circuit combines Bluetooth and FM tuner functionality into one.

Bluetooth

The Bluetooth implementation is compliant with Bluetooth specification 2.1 + EDR. The Bluetooth™ transceiver has frequency channels with 1 MHz separation from 2402 to 2480 MHz. The same band is used for both transmission and reception. This gives 79 frequency channels.

Receiver

The Bluetooth section implements a low-IF receiver for Bluetooth modulated input signals. The radio signal is taken from a balanced RF input and amplified by an LNA. The mixers are driven by two quadrature LO signals, which are locally generated from a VCO signal running at twice the frequency. The I and Q mixer output signals are band pass filtered by a poly-phase filter for channel filtering and image rejection. The output of the band pass

filter is amplified by a VGA to the optimal input range for the A/D converter. Further channel filtering is done in the digital part. The digital part demodulates the GFSK, π/4-DQPSK or 8-DPSK coded bit stream by evaluating the phase information. RSSI data is extracted. Overall automatic gain amplification in the receive path is controlled digitally. The RC time constants for the analog filters are automatically calibrated on chip.

Transmitter

The transmitter uses the serial transmit data from the Bluetooth Controller. The transmitter modulator converts this data into GFSK, π/4-DQPSK or 8-DPSK modulated I and Q digital signals for respectively 1, 2 and 3 Mbps transmission speed. These signals are then converted to analog signals that are low pass filtered before up-conversion. The carrier frequency drift is limited by a closed loop PLL.

FM Radio

FM Receiver

The receiver uses a digital low-IF architecture. The receive (RX) section integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer down converts the RF signal to low-IF. The quadrature mixer output is amplified, filtered and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the use of digital signal processing (DSP) to perform channel selection, FM demodulation and stereo audio processing.

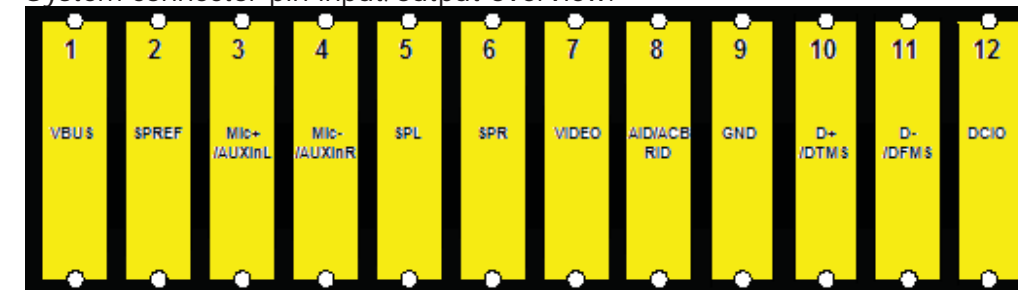
Tuning

The receiver uses frequency synthesizer technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency is defined as: Freq (MHz) = Spacing (kHz) × Channel + Bottom of Band (MHz)

External Connectors

External units are connected to the transceiver by means of a 12-pin connector on the bottom of the phone.

System connector pin input/output overview:



Clocks

Clock Distribution

The clocking for the access and application subsystems is separated. This means that the subsystems can wake up or go to sleep mode independently. The access subsystem is clocked by the 26 MHz Voltage Controlled Crystal Oscillator (VCXO) located in the GSM/EDGE circuit. When the access subsystem has a job to do, the Master Clock (MCLK) signal is requested from the RF part. Most other clocks needed within the access subsystem are generated from the MCLK. Some minor parts like sleep timer and cable detect use the 32 kHz real-time clock. The 32 kHz real-time clock clocks the application subsystem, and all other internal clocks needed within the application subsystem are

generated from this clock. However, when audio is transferred between the application and the access subsystems, the MCLK is used.

**Master Clock
(26 MHz)**

The 26.00 MHz VCXO-based MCLK is distributed as a square wave signal from the GSM/EDGE circuit. In order to have full control over the load on the MCLK, only the access side of the digital baseband controller is allowed to request the MCLK. However, by indirect means also the application side CPU can issue the request. A VCXO-based square wave is also distributed to the WCDMA circuit, but is turned on only upon a command from the digital baseband controller.

**Real-time Clock
(32. 768 kHz)**

A 32.768 kHz crystal oscillator provides a low frequency clock whenever the platform has power. This clock is used to keep the Real-Time Clock (RTC) block functioning, so that the platform can keep track of the time and date. The low frequency clock is generated in the analog baseband controller and distributed to the digital baseband controller, and if necessary to external devices like Bluetooth, FM radio and A-GPS.

A-GPS

The Assisted GPS functionality in the phone is realized with the Global Locate Hammerhead GPS module. The Global Locate Hammerhead belongs to the Type 2 GPS solutions. The PMB 2525 Hammerhead II GPS IC is a GPS single chip device containing a complete radio frequency front-end as well as the signal processing functionality in a single die. The device allows the usage of assistance data by supporting A-GPS (assisted GPS) standards (RRLP, RRC, OMA SUPL). One of three serial interfaces, UART, I²C or SPI, is used for communication with the host system.

Clock Reference Frequency

The platform provides two reference frequencies, a 32.768 kHz clock (RTCCLK) from the Analog Baseband Controller, and a 26 MHz reference clock (SYSCLK) from the Digital Baseband Controller. The RTCCLK is used by the phone real time clock function. The RTCCLK is distributed to the A-GPS module as a logical square wave. SYSCLK is derived from the reference modulation clock MCLK to the platform access system and is distributed from the Digital Baseband Controller to the A-GPS module. This 26 MHz clock is synchronized with the cellular network to an accuracy of ±0.1 ppm. Automatic frequency updates can also cause large frequency corrections, with associated phase discontinuities. In order to isolate the A-GPS module for the unstable effects of SYSCLK, an external reference clock is required. This external reference frequency provided by a TCXO is required to provide a clock with very high short term stability. The frequency of the TCXO is calibrated against the cellular reference clock by the A-GPS module enabling the use of a more economical less accurate TCXO.

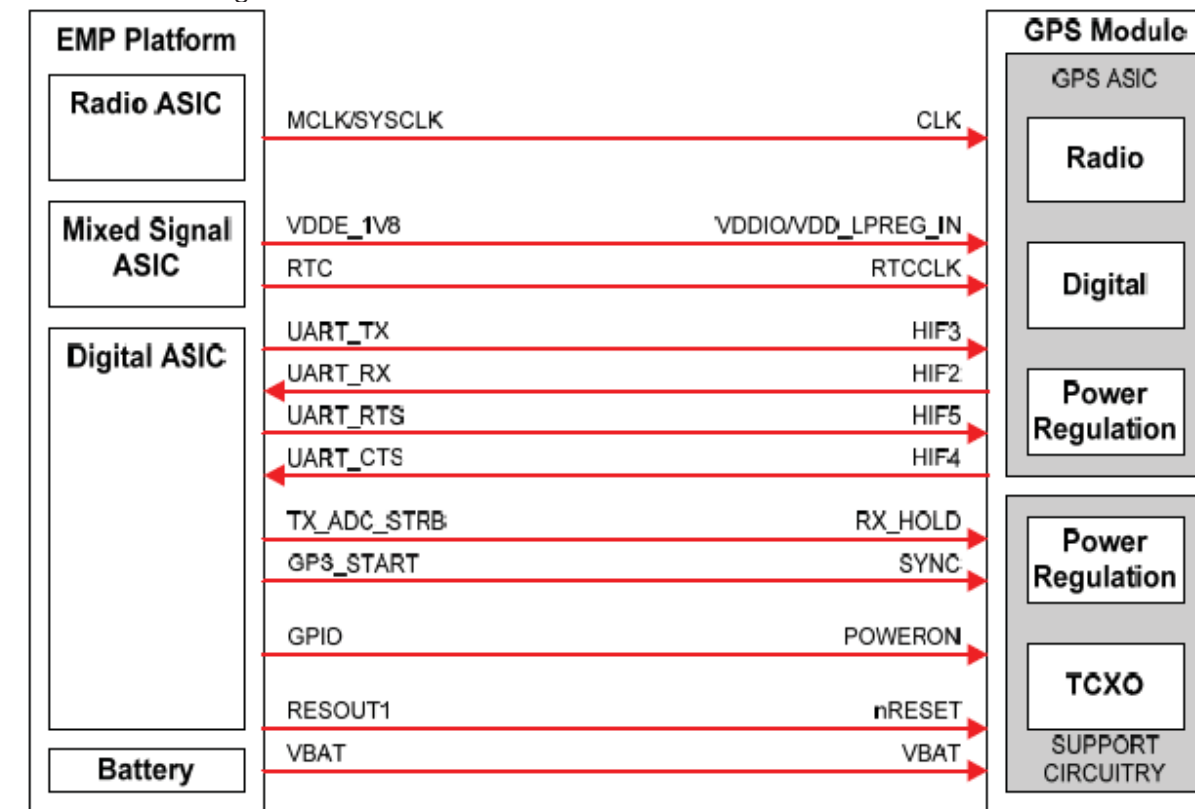
Interface and Control

The Interface and control consists of system timing and control. The control interface includes a communication link where both data and control information are transferred between platform and the A-GPS module. Data and command information is transferred using a full-duplex Universal Asynchronous Receiver Transmitter (UART) interface.

Other control signals include the following:

- A GPIO or platform reset used as a reset signal (nRESET) to the GPS module.
- A Transmission On signal (TXON/ RX_HOLD), is used to indicate to the A-GPS module when the ME is transmitting. The A-GPS modules receiver is disabled whilst the ME is transmitting.
- A hardware timing pulse (GPSSTART/SYNC) providing the A-GPS module with a highly accurate timing reference. The A-GPS is able to accurately synchronize its GPS time to this reference pulse.
- A GPIO used as an enable (POWERON) signal to the GPS module.
- A GPIO used for power control for the GPS module.

A-GPS Block Diagram:



WLAN (Wi-Fi)

This WLAN module is based on the new Marvell 88W8686 chipset. WLAN module is designed to support IEEE 802.11a or 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11b data rates of 1, 2, 5.5 and 11 Mbps. For security the WLAN module supports the IEEE 802.11i security standard through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) security mechanism. For video, voice and multimedia applications the WLAN module supports 802.11e Quality of Service (QoS). The 3-wire Bluetooth / WiFi co-existence interface is also supported. The WLAN module has a fully integrated RF to baseband transceiver that operates in both the 2.4 GHz ISM radio band for 802.11g/b WLAN applications and 5 GHz UNII radio band for 802.11a WLAN applications. It contains all the circuitry to support both transmit and receive operations. The integrated LNA and AGC on the receive path is seamlessly controlled by baseband functions. Integrated transmitters up-convert the quadrature baseband signal and the deliver the RF signals to external power amplifiers for 2.4 GHz and 5 GHz radio band transmission. Local oscillator frequencies are generated by a fully integrated programmable frequency synthesizer. The loop bandwidth is optimized for phase noise and dynamic performance and quadrature signals are generated on-chip.

BT/WLAN Co-existence

Standards bodies did not fully anticipate the range of scenarios in which WLAN and Bluetooth would compete for the same spectrum therefore IEEE 802.11 (WLAN) and Bluetooth use the same 2.4 GHz ISM frequency band (although they use different access mechanisms). They also did not include comprehensive, robust, and cooperative mechanisms in their respective standards to mitigate interference. Since no mechanism for exchanging signal status information has been built into the two standards, the task of minimizing interference must be accomplished by other means. Co-location refers to the situation where both Bluetooth and WLAN are in functional mode, that is, they are both fully radio operational, performing either transmission or reception activities (or ready to do so immediately). They also either share an antenna or each module has its own antenna, on the same device. Because both Bluetooth and WLAN operate in the same unlicensed ISM band (2.4GHz), steps are required to avoid disturbances and allow coexistence. The HW solution is a single antenna controlled by an Antenna Switch with 3-wired lines between WLAN Device and BT Device. The used algorithm to decision whether

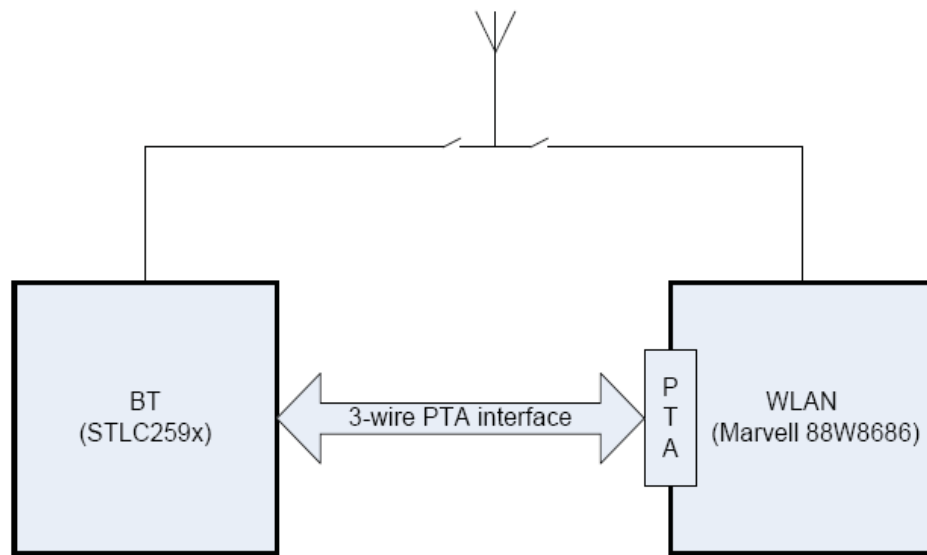
WLAN device or BT device gets the antenna is Packet Traffic Arbitration (PTA). WLAN LD configures the PTA during startup of the WLAN device. All PTA parameters are stored in GDFS. The PTA is configured to prioritize BT traffic if it is a BT high request. All WLAN traffic should have priority before any BT traffic that is categorized as BT low requests.

WLAN Driver sends status events to BT Driver to inform about:

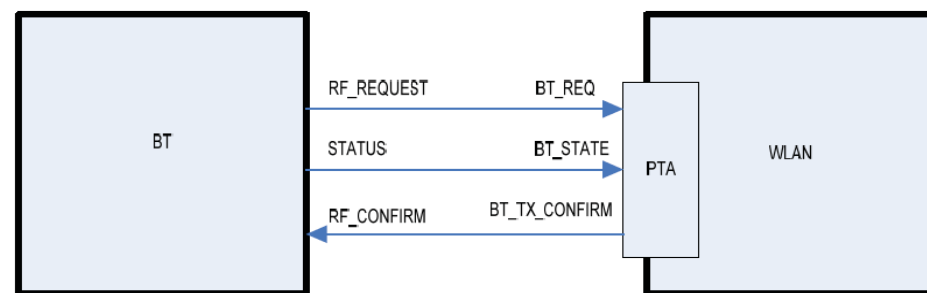
- WLAN startup and shutdown
- WLAN association and disassociation
- The current WLAN channel in use

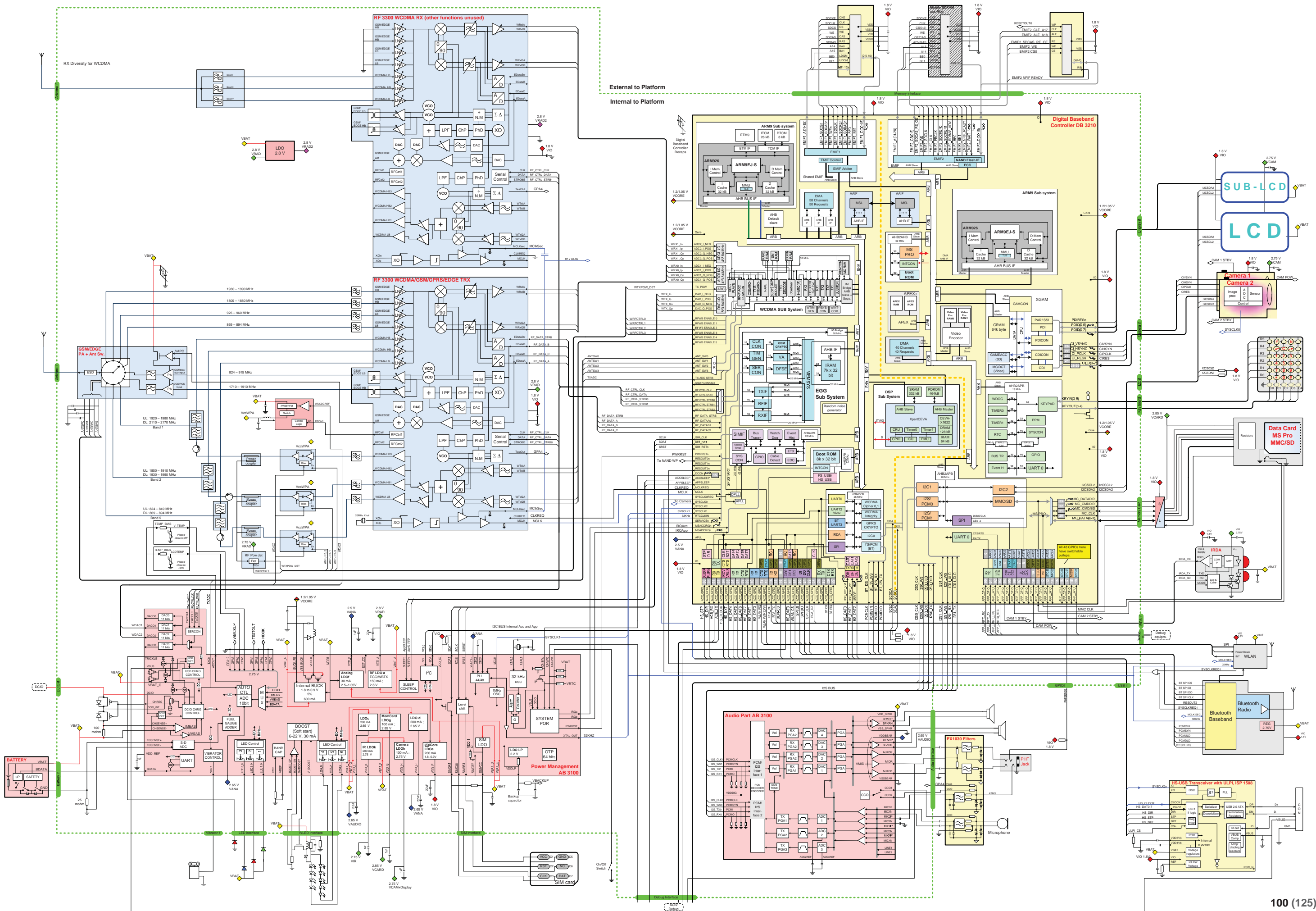
In the cases of WLAN startup and shutdown the BT Logical Driver configures the BT Device to request the antenna from PTA or not. BT LD also monitors if WLAN have any connection running. In that case, BT avoids the BT frequencies mapping to the WLAN channel. WLAN monitors if BT has started any BT Inquiry or page. If this happens any link loss mechanisms should be temporary turned off for the BT Inquiry or page period.

Bluetooth and WLAN PTA Mechanism:

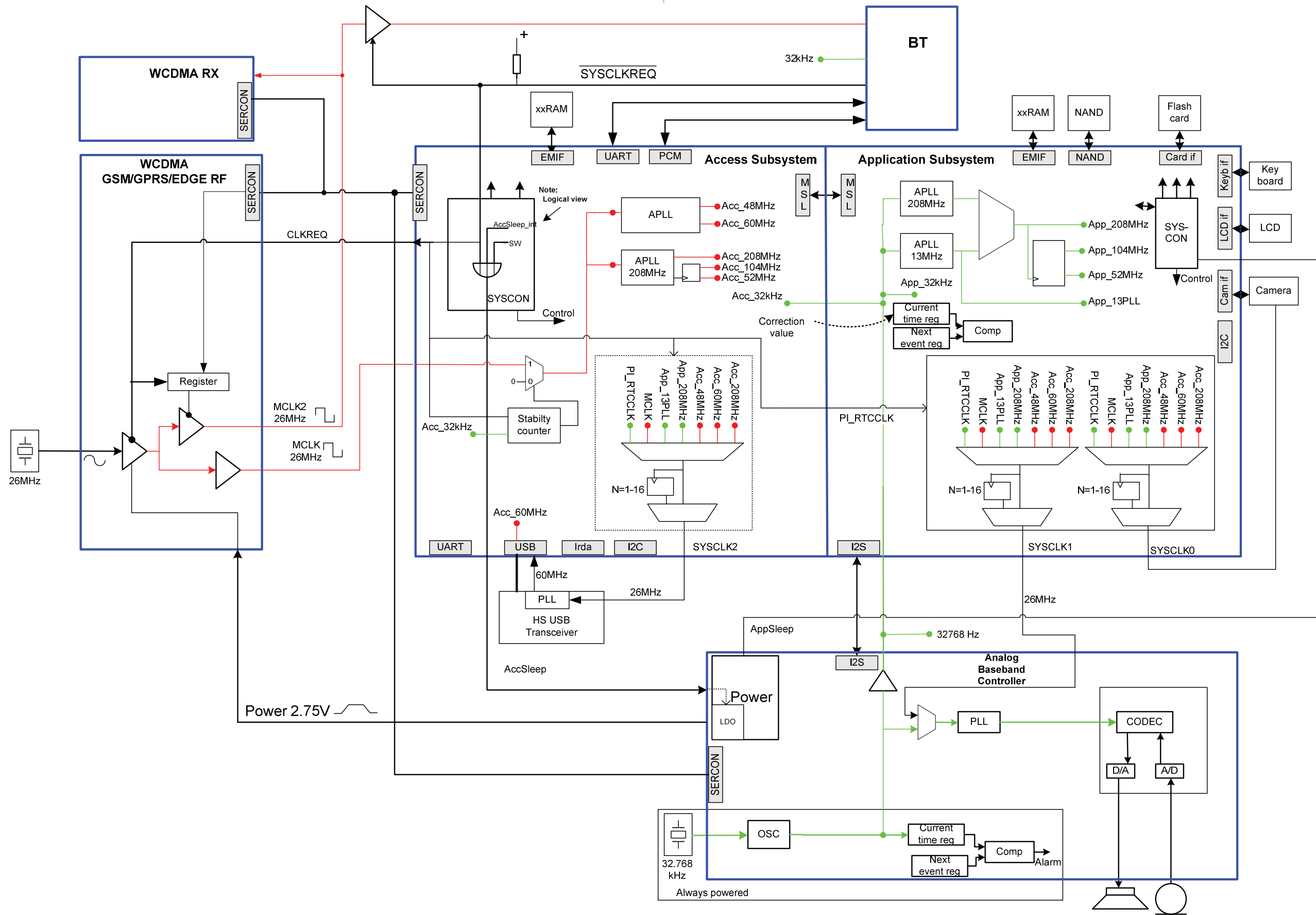


Bluetooth and WLAN Chip 3-wire Interface:





FUNCTIONAL OVERVIEW



Replaceable Components

EXPLANATION OF ABBREVIATIONS USED IN THE COLUMN 'COMMENTS' BELOW

COMPONENT LOCATION

P = Primary side
S = Secondary side

MOISTURE SENSITIVITY LEVEL

MSLX (X = 1, 2, 2A, 3, 4, 5, 5A or 6)

**For more information on moisture sensitivity levels:
Refer to 1220-1336: Generic Repair Manual – electrical, section 'Moisture & Baking'!**

REPAIR METHOD

HA = Hot Air (removal & mounting)
ST = Soldering Tool (removal & mounting)
HA/ST = Hot Air for removal - Soldering Tool for mounting
BGA = BGA Station
BH = Bottom Heater

CALIBRATION

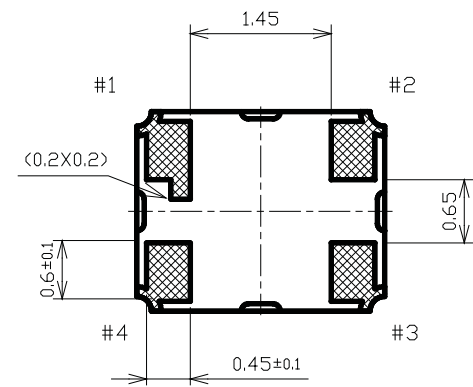
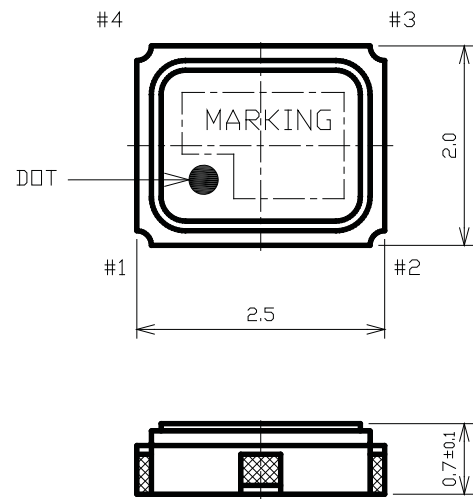
C = Calibration of the phone is required after replacing the component

Calibration to be done by authorized centers only!

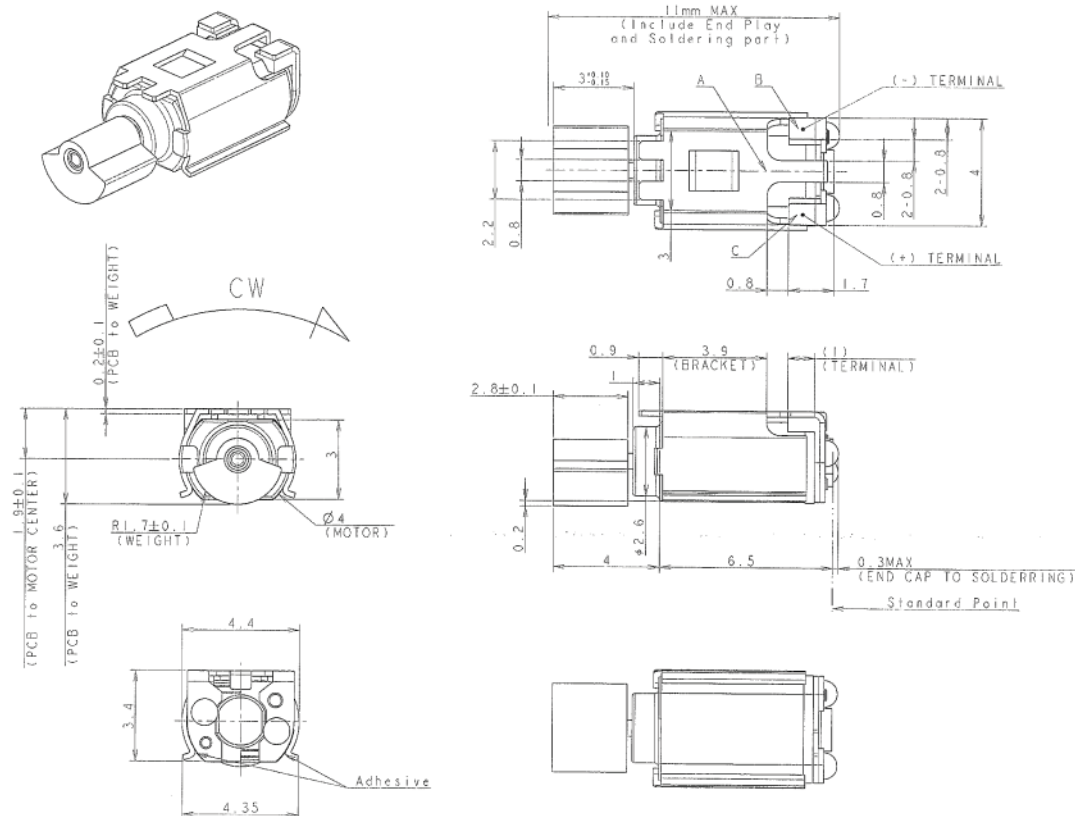
Position	Component	Part no.	Comments	Page
B1400	Osc TCXO 27,456 MHz	1200-7847	P HA	104
B2100	Crystal 32768Hz	RTM501911/2R1A	P HA C	104
B2400	IC	1220-4470	P HA	104
B3100	Microphone	1210-7410	P BGA ⇒1	104
B4200	Vibrator	1218-9713	S HA ⇒2	104
C2439	Capacitor Ceramic 1,0 uF +/-10% 25,0 V K	RJC5163237/1	P HA ⇒3	105
C2440	Capacitor Ceramic 1,0 uF +/-10% 25,0 V K	RJC5163237/1	S HA ⇒4	105
C4203	Capacitor Ceramic 1,0 uF +/-10% 25,0 V K	RJC5163237/1	P HA Note Fence cut	105
E1003	Shield Can Fence Tiger power supply	1216-0127	P BGA ⇒5	
L2200	Ind WW 4.7 uH K3012	1200-2214.1	P HA	105
L2201	120ohm 0603 2A 50mohm Bead	REG70605/15R1	P HA Note Fence cut	
L2401	Inductor	REG70618/20	S HA	105
L2402	Inductor	REG70618/20	S HA	105
L2403	Inductor	REG70618/20	S HA	105
L2404	Inductor	REG70618/20	S HA	105
L2406	Ind Chip 0, H	1200-6898	S HA	105
L2440	Ind Chip 22.0 uH 20% 1608(0603)	1207-2753	S HA	105
L2443	Ind Chip 22.0 uH 20% 1608(0603)	1207-2753	S HA	105
L3104	Inductor	REG70618/20	P HA	105
L3116	100nH 5% 0603 0.22A	REG7044243/1	P HA	105
L3117	100nH 5% 0603 0.22A	REG7044243/1	P HA	105
L3120	Inductor	REG70618/20	P HA	105
L3121	Inductor	REG70618/20	P HA	105
L3122	Inductor	REG70618/20	P HA	105
L3134	Ind Chip 22.0 uH 20% 1608(0603)	1207-2753	P HA	105
L3135	Ind Chip 22.0 uH 20% 1608(0603)	1207-2753	P HA	105
L4200	22uH 20% 3x3x1.2mm 0.375A 0.63ohm	REG7245512/22M	P HA	105
L4400	Ind WW 2.2uH 20% 2.8x3.0x1.2	1215-2143	P HA	106

Position	Component	Part no.	Comments	Page
N1210	IC Linear	1203-5870	P HA	106
N1211	IC Vreg PLP1820-6	1204-5903	P HA	106
N1400	A-GPS	1200-0700	P HA	107
N1410	IC Amp MicroDFN-6	1215-1892	P HA	107
N1411	IC Vreg CS-5	1200-3994	P HA	107
N1412	IC Vreg PLP1010-4	1201-1568	P HA	107
N2200	IC Vreg	1213-9811	P HA Note Fence cut	108
N2205	IC Vreg	1201-9680	P HA Note Fence cut	108
N2206	LDO Dual 2.8 V & 1.8 V.	1201-6517	P HA	108
N2212	IC Vreg	1215-2684	P HA	108
N2213	Step Down Converter 500mA	1208-4678	P HA	108
N2410	IC IF 3.5x3.5x0.8 thin QFN	1200-1951	P HA	108
N2411	ASIC	1204-5837	P HA	109
N2420	IC IF ISP1508 ES3 (3.5*3.5*0.8)	1200-1694	P HA	110
N2421	IC ESD Prot UDFN 6 2x2 mm	1200-6309	P HA	109
N2422	ASIC Baseband	1201-4120	P HA	109
N3100	IC Amplifier 500mA	1203-4594	P HA	109
N3101	ASIC Tjatte3 CSP20	ROP1013074/1R1A	P HA	111
N3102	IC Amp 9-pin Flip Chip CSP	1203-4594	P HA	109
N3103	IC Amp	1217-2694	P HA	111
N3104	ASIC Tjatte3 CSP20	ROP1013074/1R1A	P HA	111
N4200	Trans N-ch FET	RYN901936/1	P HA Note Fence cut	111
N4401	IC Dri CS-16	1212-3512	P HA	111
R2438	Resistor 0.0 Ohm +/-5% NA mW K0402	REP622001/0	S HA	
R2448	Resistor 0.0 Ohm +/-5% NA mW K0402	REP622001/0	S HA	
R2449	Resistor 0, Ohm +/-50m 63 mW K0603	REP623001/0	S HA	112
R2451	Resistor 0, Ohm +/-50m 63 mW K0603	REP623001/0	P HA	112
R2490	Resistor 0, Ohm +/-50m 63 mW K0603	REP623001/0	S HA	112
V2200	Diode	RKZ223911/1	S HA	112
V2202	Transistor	1200-0145	S HA	112
V2415	Diode	1201-8440	P HA	112
V2416	Diode	1201-8440	P HA	112
V2417	Diode	RKZ223905/2	S HA	112
V3101	Dual ESD protection diode 6V	RKZ223914/2	P HA	
V3102	Dual ESD protection diode 6V	RKZ223914/2	P HA	
V3103	ZenerDiode, 5.6V, Pb-free	RKZ223911/3	P HA	112
V4203	Trans NPN 1.2X1.2X0.5	RYN1216043/1	P HA	
X1000	Conn Leaf Spring 1p	1202-1053	P HA	113
X1004	Conn Leaf Spring 1p	1202-1053	P HA	113
X1005	Conn Leaf Spring 1p	1202-1053	P HA	113
X1006	Conn Leaf Spring 1p	1221-7006	S HA	113
X1200	Connector	1203-9688	S HA/ST	113
X1500	Connector	1203-9688	S HA/ST	113
X2201	Conn Pogopin 5p	1206-2937	S BGA	113
X2401	Conn BtB	1200-9864	S HA	113
X2402	Memory card reader	1200-9764	P BGA	114
X2405	Connector	1210-0559	S HA/ST	114
X2410	Conn BtB Receptacle 18p	1200-6752	P HA	114
X4300	Conn BtB Receptacle 70p	1206-2940	P BGA	115
X4301	Conn BtB 30 pin	1200-1733	S HA	115
Z1400	Filter SAW 1.575 GHz	1211-5714	P HA	115
Z2400	Filter	1201-6833	P HA	115
Z4200	Filter 150.0 MHz	1221-4986	P HA	115
Z4201	Filter 150.0 MHz	1221-4986	P HA	115
Z4202	Filter 150.0 MHz	1221-4986	P HA	115
N1200	Tiger 1,2,5	1218-1883	P BGA C A variant band 1,2,5	
N1200	Pre-bumped Tiger II Band 1,8	1218-1888	P BGA C I variant band 1,8	

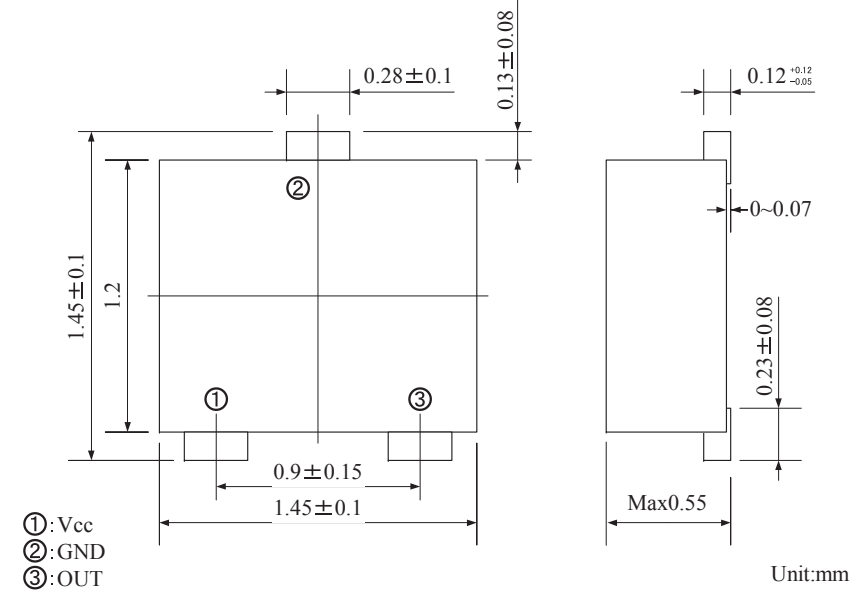
B1400 Osc TCXO 27,456 MHz 1200-7847



B4200 Vibrator 1218-9713

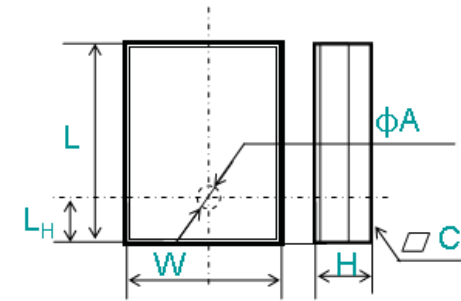


B2400 IC 1220-4470

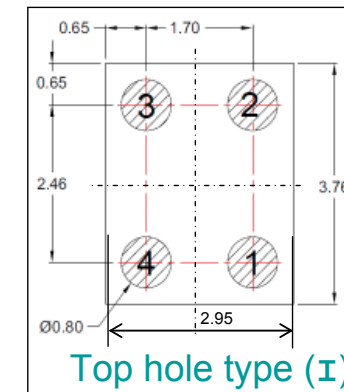


B3100 Microphone 1210-7410

Package outline



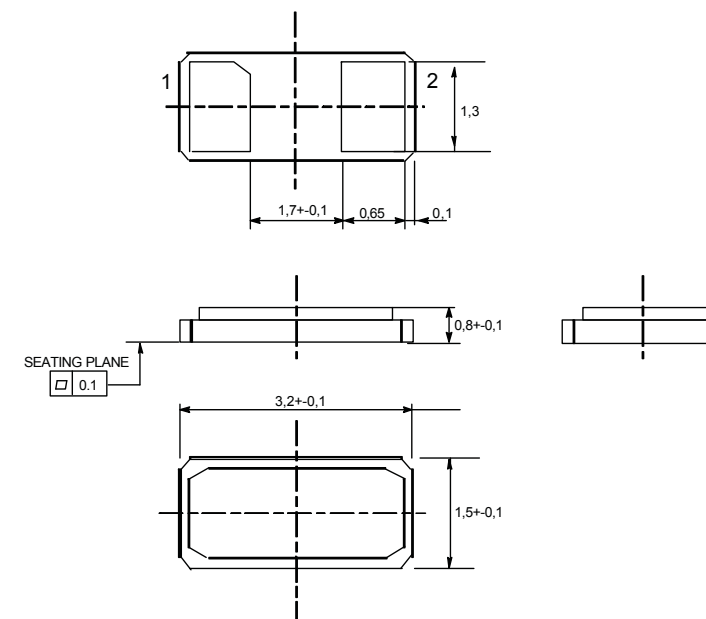
Pad design



Item	Dimension	Tolerance (+/-)	Units
Length (L)	3.76	0.10	mm
Width (W)	2.95	0.10	mm
Height (H)	1.10	0.10	mm
Hole height (L _H)	1.18	0.10	mm
Acoustic Port Diameter (ΦA)	0.50	0.10	mm
Co-planarity (C _p)	<0.05	-	mm

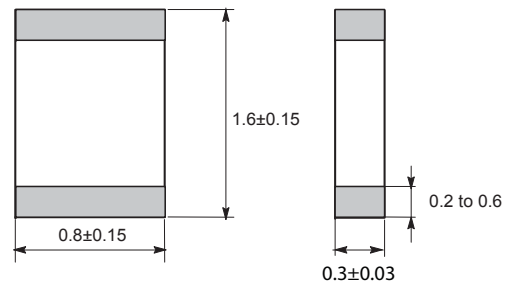
PIN Designation	
Pin #	Function
1	Power
2	Ground
3	Ground
4	Output

B2100 Crystal 32768Hz RTM501911/2R1A

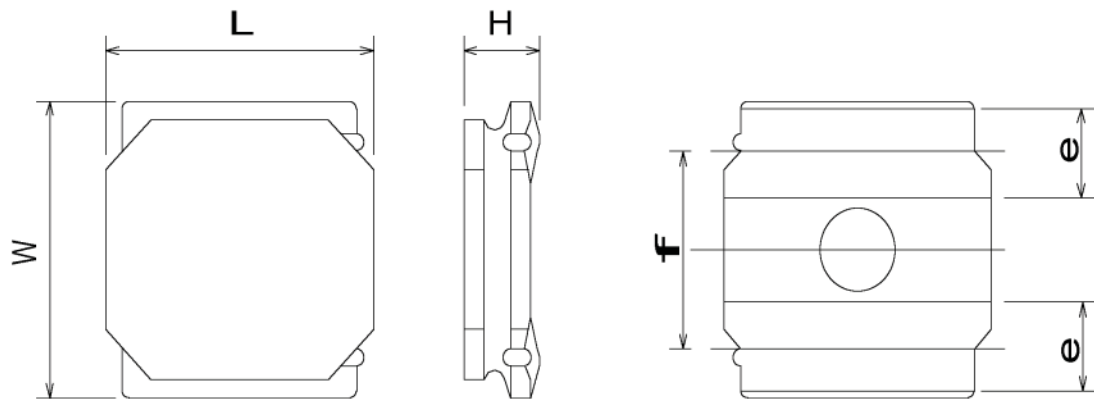


C2439, C2440, C4203 Capacitor Ceramic 1,0 uF +/-10% 25,0 V K RJC5163237/1

Dimensions in mm.



L2200 Ind WW 4.7 uH K3012 1200-2214.1

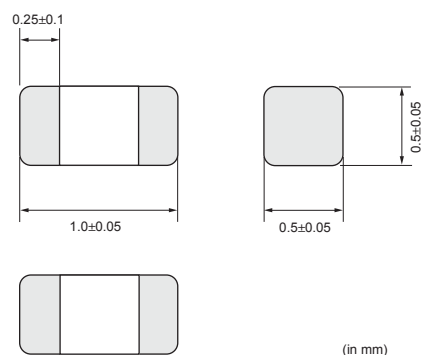


Description	Mark	Dimensions
Length	L	3.0±0.1
Width	W	3.0±0.1
Height	H	1.2Max.
Width of Electrode	e	0.9±0.2
Space between electrodes	f	1.9±0.2

(Unit: mm)

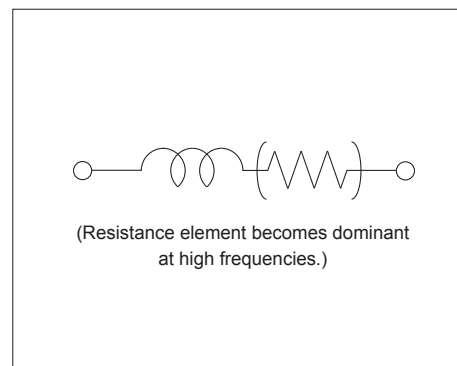
L2401-04, L3104, L3120-22 Inductor REG70618/20

■ Dimension

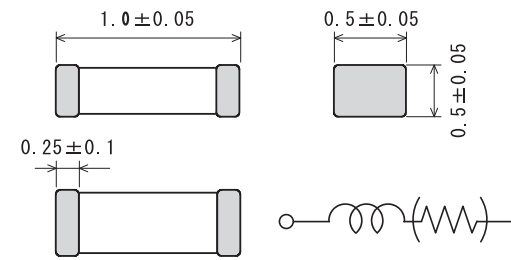


(in mm)

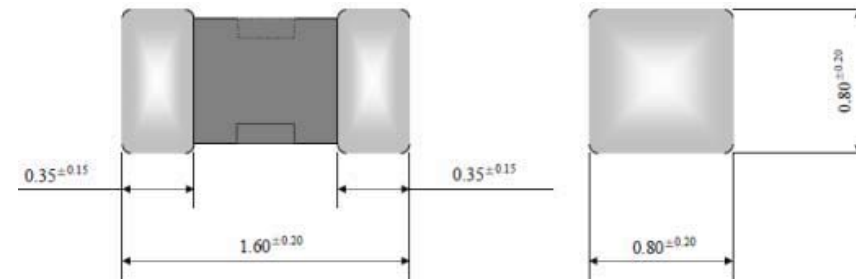
■ Equivalent Circuit



L2406 Ind Chip 0, H 1200-6898



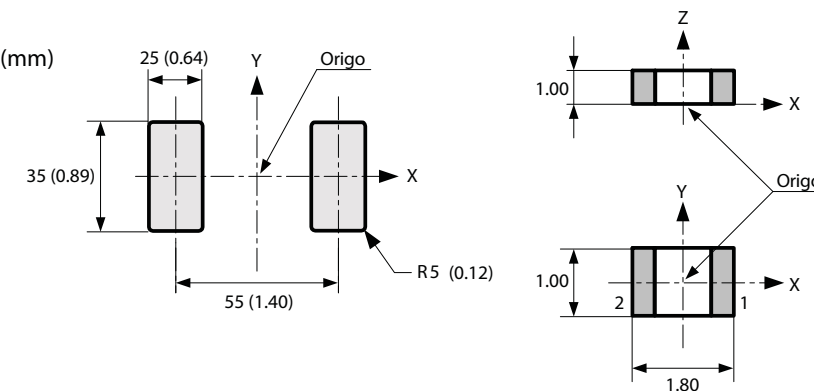
L2440, L2443, L3134-35 Ind Chip 22.0 uH 20% 1608(0603) 1207-2753



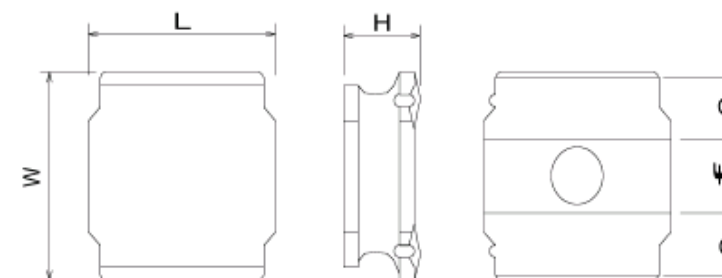
L3116-17 100nH 5% 0603 0.22A REG7044243/1

All dimensions in mm or in MIL (mm)
Y = Nominal direction of feed

Mounting Symbol

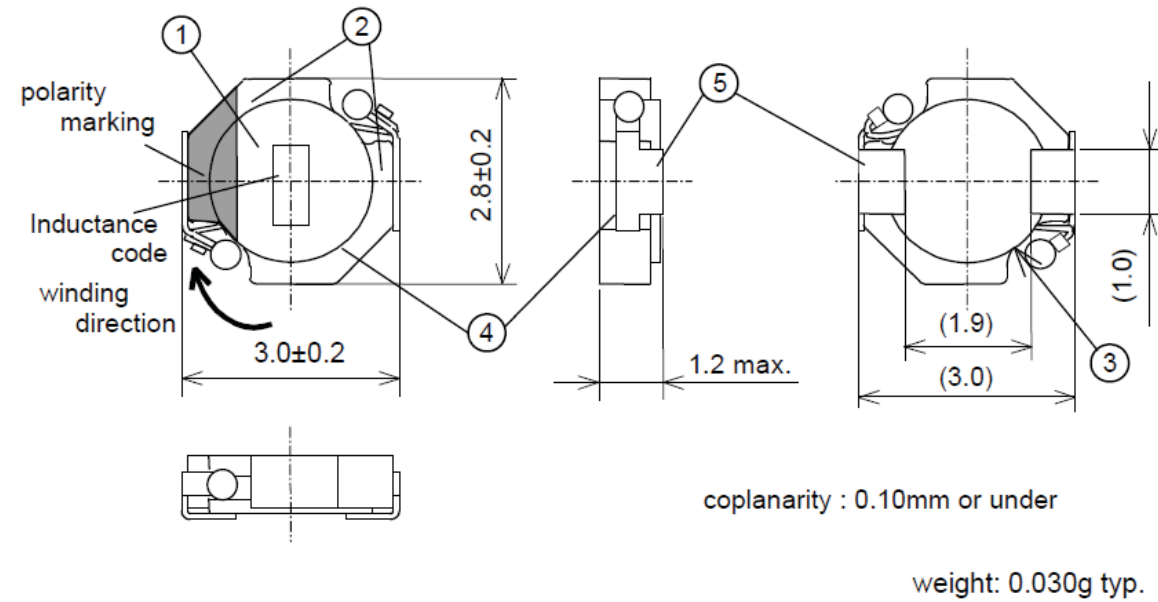


L4200 22uH 20% 3x3x1.2mm 0.375A 0.63ohm REG7245512/22M



Size (mm)	3012
L	3.0+/-0.1
W	3.0+/-0.1
H	1.2 max
e (width of electrode)	0.9+/-0.2
f (space between electrodes)	1.0+/-0.2

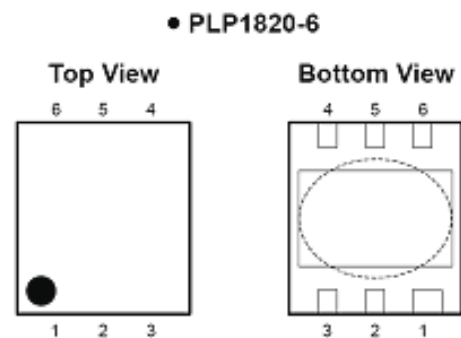
L4400 Ind WW 2.2uH 20% 2.8x3.0x1.2 1215-2143



- Note: 1. Marking indicates polarity and inductance code.
 2. Polarity marking is the mark from which side terminal wire is wound clockwise.
 3. Dimensions in parentheses are reference values.

N1211 IC Vreg PLP1820-6 1204-5903

PIN CONFIGURATIONS



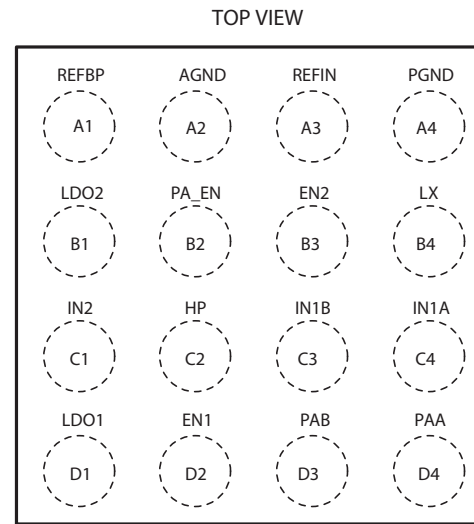
• PLP1820-6*

Pin No.	Symbol	Description
1	V _{OUT}	Output Pin
2	V _{OUT}	Output Pin
3	GND	Ground Pin
4	CE	Chip Enable Pin
5	V _{DD}	Input Pin
6	V _{DD}	Input Pin

* Tab in the parts have GND level.
 (They are connected to the back side of this IC.)
 Do not connect to other wires or land patterns.

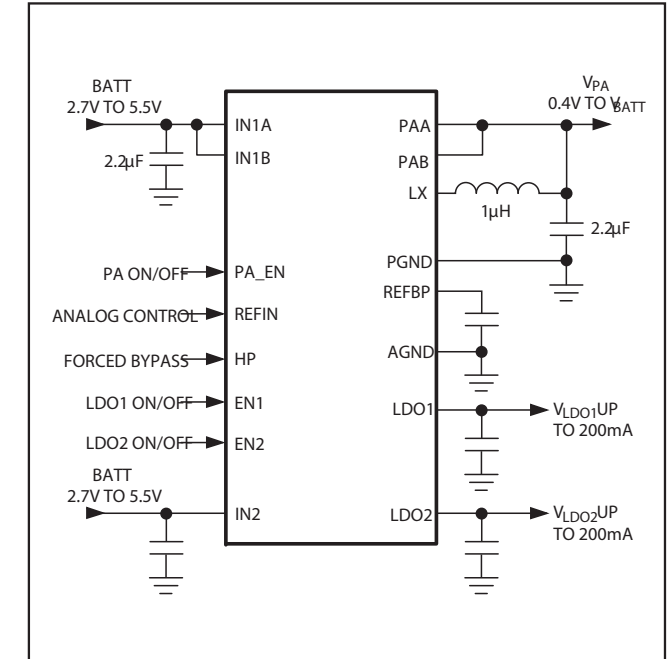
N1210 IC Linear 1203-5870

Pin Configuration



(BUMP IN BOTTOM)
 16-Bump, 2mm x 2mm WLP

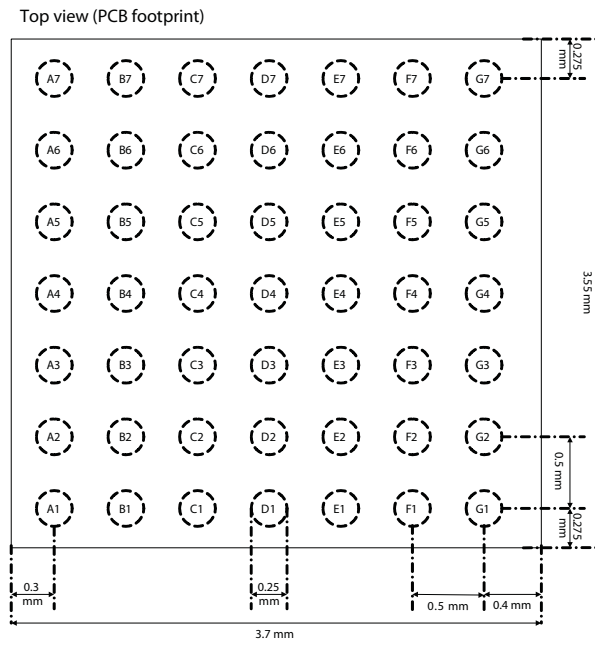
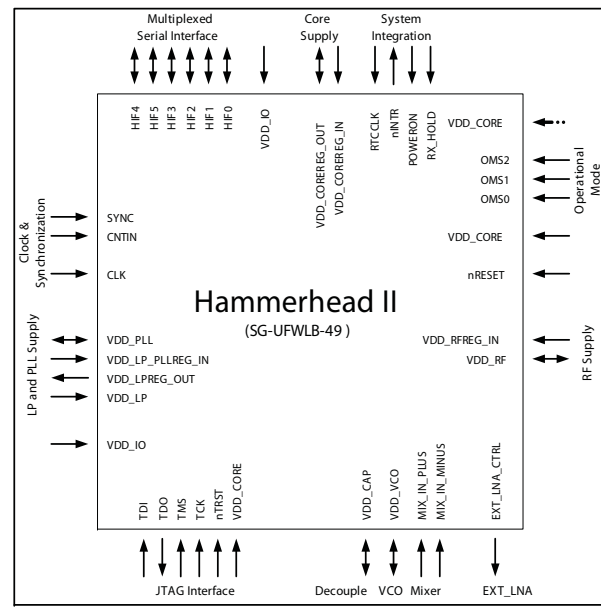
Typical Operating Circuit



Pin Description

PIN	NAME	FUNCTION
A1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.22µF ceramic capacitor to reduce noise on the LDO outputs. REFBP is internally pulled down through a 1k Ω resistor during shutdown.
A2	AGND	Low-Noise Analog Ground
A3	REFIN	DAC-Controlled Input. The output of the PA step-down converter is regulated to 2 x V _{REFIN} . When V _{REFIN} reaches 0.465 x V _{IN2} , bypass mode is enabled.
A4	PGND	Power Ground for PA Step-Down Converter
B1	LDO2	200mA LDO Regulator 2 Output. Bypass LDO2 with a 1µF ceramic capacitor as close as possible to LDO2 and AGND. LDO2 is internally pulled down through a 1k Ω resistor when this regulator is disabled.
B2	PA_EN	PA Step-Down Converter Enable Input. Connect to IN ₋ or logic-high for normal operation. Connect to GND or logic-low for shutdown mode.
B3	EN2	LDO2 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
B4	LX	Inductor Connection. Connect an inductor from LX to the output of the PA step-down converter.
C1	IN2	Supply Voltage Input for LDO1, LDO2, and Internal Reference. Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 2.2µF ceramic capacitor as close as possible to IN2 and AGND. Connect IN2 to the same source as IN1A and IN1B.
C2	HP	High-Power Mode Set Input. Drive HP high to invoke forced bypass mode. Bypass mode connects the input of the PA step-down converter directly to its output through the internal bypass MOSFET. Drive HP low to disable the forced bypass mode.
C3, C4	IN1B, IN1A	Supply Voltage Input for PA Step-Down Converter. Connect IN1 ₋ to a battery or supply voltage from 2.7V to 5.5V. Bypass the connection of IN1 ₋ with a 2.2µF ceramic capacitor as close as possible to IN1 ₋ and PGND. IN1A and IN1B are internally connected together. Connect IN1 ₋ to the same source as IN2.
D1	LDO1	200mA LDO Regulator 1 Output. Bypass LDO1 with a 1µF ceramic capacitor as close as possible to LDO1 and AGND. LDO1 is internally pulled down through a 1k Ω resistor when this regulator is disabled.
D2	EN1	LDO1 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
D3, D4	PAB, PAA	PA Connection for Bypass Mode. Internally connected to IN1 ₋ using the internal bypass MOSFET during bypass mode. PA ₋ is connected to the internal feedback network. Bypass PA ₋ with a 2.2 µF ceramic capacitor as close as possible to PA ₋ and PGND.

N1400 A-GPS 1200-0700

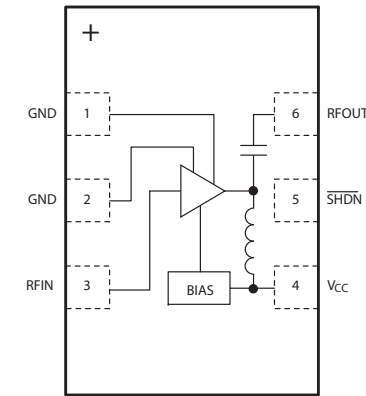


Pin No.	Pin Name	Pad Type	Pad Usage	O/P State	Pad Functional Description
A1	HIF3 UART_RXD / UART_RXD / I ² C_GROUP1 / SPL_nSCS	I/O	I	-	Host Interface OMS(2:0)=1,1,1; UART Interface: Data Input OMS(2:0)=1,1,0; UART Interface: Data Input (Ignored) OMS(2:0)=1,0,1; Selection of I ² C group address OMS(2:0)=1,0,0; SPI chip select
A2	HIF4 UART_nRTS / UART_nRTS / I ² C_A0 / SPL_SI	I/O	O	Z	Host Interface OMS(2:0)=1,1,1; UART Interface: hardware flow control OMS(2:0)=1,1,0; UART Interface: hardware flow control (Tristated) OMS(2:0)=1,0,1; Selection of I ² C group address bit 0 OMS(2:0)=1,0,0; SPI serial data input
A3	CNTIN	I	I	-	Digital high accuracy frequency reference
A4	CLK	I/AI	I	-	Clock signal input. Selectable as digital or analog input
A5	VDD_PLL	PI/PD	-	-	Digital PLL supply Decoupling
A6	VDD_LP_PLLREG_I N	PI	-	-	PLL voltage and Low Power core regulator input
A7	VDD_IO	PI	-	-	Digital I/O supply
B1	VSS_DIG	GND	-	-	
B2	HIF2 UART_TXD / UART_TXD / I ² C_GROUP0 / SPL_SCK	I/O	O	Z	Host Interface OMS(2:0)=1,1,1; UART Interface: Data Output OMS(2:0)=1,1,0; UART Interface: Data Output (Tristated) OMS(2:0)=1,0,1; Selection of I ² C group address OMS(2:0)=1,0,0; SPI clock
B3	HIF5 UART_nCTS / UART_nCTS / I ² C_GROUP1 / SPL_SO	I/O	I	Z	Host Interface OMS(2:0)=1,1,1; UART Interface: hardware flow control OMS(2:0)=1,1,0; UART Interface: hardware flow control (Ignored) OMS(2:0)=1,0,1; not used (tie to "0") OMS(2:0)=1,0,0; SPI serial data output
B4	VDD_LPREG_OUT	PO	-	-	Low Power core regulator output
B5	TDI	I/O	I	PU "C"	Serial Data Input (JTAG, IEEE 1149.1)
B6	VDD_LP	PI	-	-	Low Power supply
B7	VDD_CORE	PI	-	-	Digital core supply
C1	VDD_COREREG_O UT	PO	-	-	Digital core voltage regulator output
C2	VDD_IO	PI	-	-	Digital I/O supply

C3	HIF0 / / I ² C_SCL /	I/O	I	-	Host Interface OMS(2:0)=1,1,1; not used (tie to "0") OMS(2:0)=1,1,0; not used (tie to "0") OMS(2:0)=1,0,1; I ² C clock OMS(2:0)=1,0,0; not used (tie to "0")
C4	HIF1 / / I ² C_SDA /	I/O	I	-	Host Interface OMS(2:0)=1,1,1; not used (tie to "0") OMS(2:0)=1,1,0; not used (tie to "0") OMS(2:0)=1,0,1; I ² C data OMS(2:0)=1,0,0; not used (tie to "0")
C5	TD0	I/O	O	Z	Serial Data Output (JTAG, IEEE 1149.1)
C6	TCK	I/O	I	PD "C"	Clock (JTAG, IEEE 1149.1)
C7	hTRST	I/O	I	PD "A"	Reset Input (JTAG, IEEE 1149.1)
D1	VDD_COREREG_IN	PI	-	-	Digital core voltage regulator supply
D2	VSS_DIG	GND	-	-	
D3	OMS1	I/O	I	-	Operational mode select / Bus interface select
D4	SYNC	I	I	-	Digital reference time pulse
D5	VSS_DIG	GND	-	-	
D6	TMS	I/O	I	PU "C"	State Machine Control Signal (JTAG, IEEE 1149.1)
D7	VSS_DIG	GND	-	-	
E1	RTCLK	I/O	I	Hyst	32.768kHz clock signal input
E2	POWERON	I/O	I	0	Power On signal to chip
E3	OMS0	I/O	I	-	Operational mode select / Bus interface select
E4	VSS_LNA	GND	-	-	
E5	VSS_RF	GND	-	-	
E6	MIX_IN_PLUS	AI	AI	-	Differential mixer input
E7	VDD_CAP	PI/O	PI/O	(Z) (Z)	RF Digital Supply Decoupling
F1	hINTR	I/O	O	OD (Z) (Z)	Interrupt request signal to host
F2	RX_HOLD	I/O	I	-	RX_HOLD signal (From host to indicate that the host is transmitting)
F3	hRESET	I/O	I	Hyst 0	Chip reset signal
F4	VDD_RFREG_IN	PI	-	-	RF voltage regulator input
F5	EXT_LNA_CTRL0	AI/O	O	-	External LNA control
F6	MIX_IN_MINUS	AI	AI	-	Differential mixer input
F7	VDD_VCO	PI/O	PI/O	(Z) (Z)	Buffer capacitor for VCO supply
G1	VDD_CORE	PI	-	-	Digital core supply
G2	OMS2	I/O	I	-	Operational mode select
G3	VDD_CORE	PI	-	-	Digital core supply
G4	VSS_RF	GND	-	-	
G5	VDD_RF	PI/O	-	-	RF Analog Supply Decoupling
G6	VSS	AI	AI	-	
G7	N.C.	AO	AO	-	This ball should be left unconnected

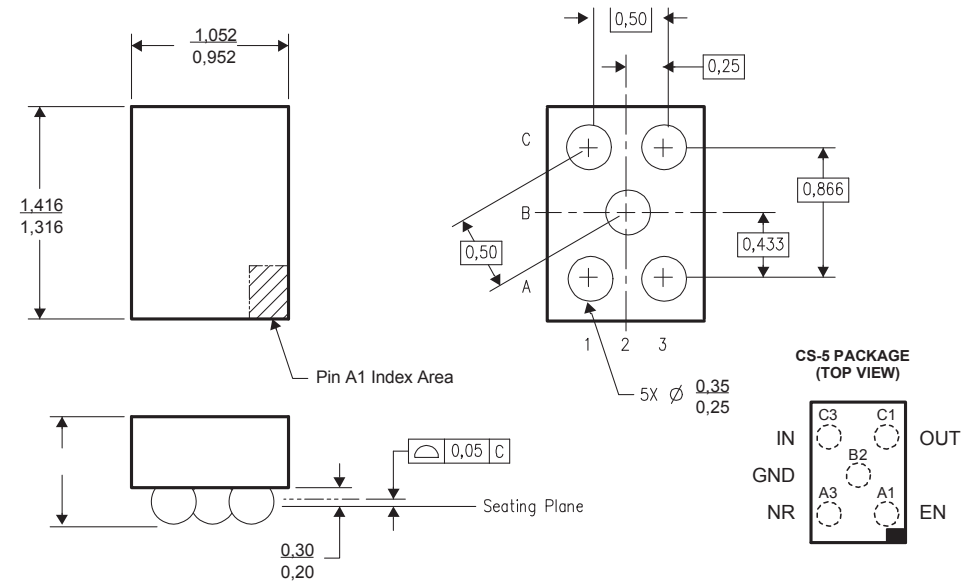
Pad Type	Description	Comments
GND	Chip Ground	All signals are referred to this
PI	Power In	Supply to a voltage domain
PO	Power Out	Regulator Output
PI/O	Power Out	Supply to a voltage domain and regulator Output
I/O	Digital Signal Pad	All Digital Pads are I/O Pads which are configured internally as required. - All are configured as Push-Pull except those marked as OD (open drain) - All have hysteresis by default, but is only mentioned when it is required for correct system operation.
AI	Analog Input	
AO	Analog Output	
AI/O	Analog Input/Output	Bidirectional analog pad.
PU	Internal Pull Up	
PD	Internal Pull Down	

N1410 IC Amp MicroDFN-6 1215-1892

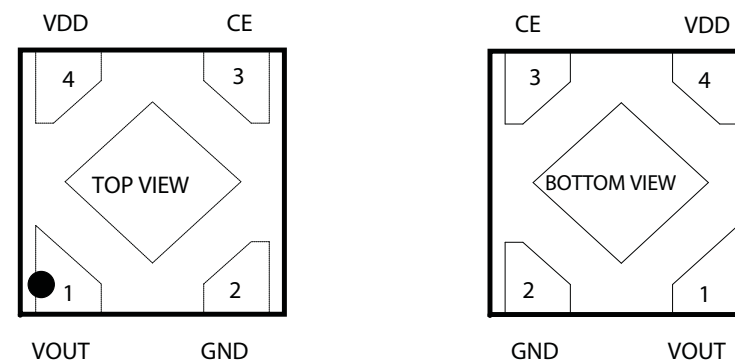


N1411 IC Vreg CS-5 1200-3994

Dimensions in mm and tolerance 0.1 mm unless noted.



N1412 IC Vreg PLP1010-4 1201-1568

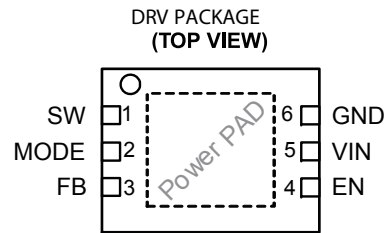


Pin No.	Symbol	Description
1	V _{OUT}	Output Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	V _{DD}	Input Pin

Tab is GND level. (They are connected to the reverse side of this IC.)

N2200 IC Vreg 1213-9811

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

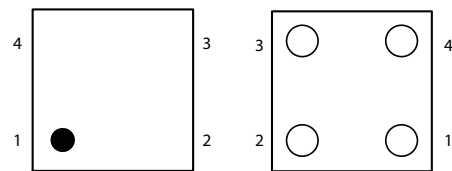
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V _{IN}	5	PWR	V _{IN} power supply pin.
GND	6	PWR	GND supply pin
EN	4	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	1	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
FB	3	I	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
MODE	2	I	MODE pin = high forces the device to operate in fixed-frequency PWM mode. Mode pin = low enables the Power Save Mode with automatic transition from PFM mode to fixed-frequency PWM mode.

N2205 IC Vreg 1201-9680

PIN CONFIGURATIONS

Mark Side

Bump Side



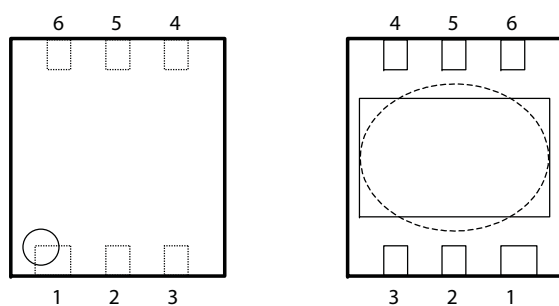
PIN DESCRIPTION

Pin No.	Symbol	Description
1	V _{DD}	Input Pin
2	CE	Chip Enable Pin
3	GND	Ground Pin
4	V _{OUT}	Output Pin

N2206 LDO Dual 2.8 V & 1.8 V 1201-6517

Top View

Bottom View

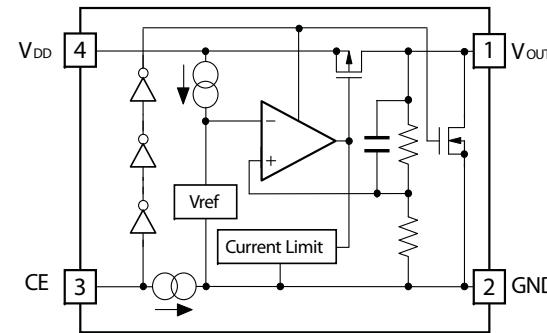


Pin No.	Symbol	Description
1	V _{OUT2}	Output Pin 2
2	V _{DD}	Input Pin
3	V _{OUT1}	Output Pin 1
4	GND	Ground Pin
5	CE 1	Chip Enable Pin 1
6	CE 2	Chip Enable Pin 2

* Tab in the parts have GND level.
(They are connected to the reverse side of this IC.)
Do not connect to other wires or land patterns.

N2212 IC Vreg 1215-2684

Block Diagram



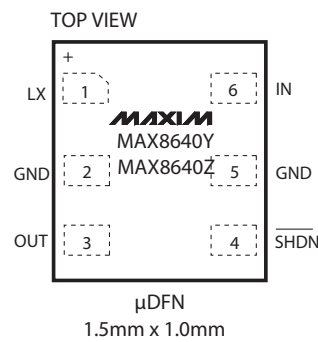
Pin Description

Pin No.	Symbol	Description
1	V _{OUT}	Output Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	V _{DD}	Input Pin

Tab is GND level. (They are connected to the back side of the IC.)
Do not connect to other wires or land patterns.

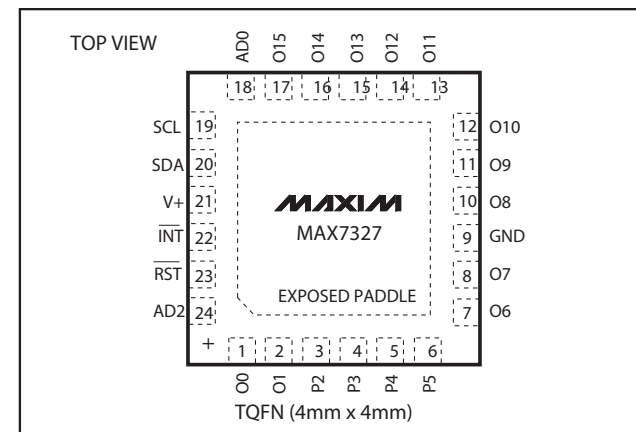
N2213 Step Down Converter 500mA 1208-4678

Pin Configuration

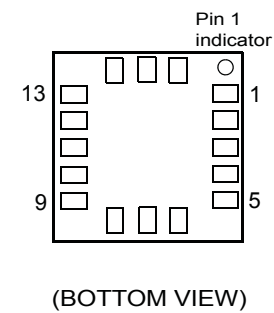
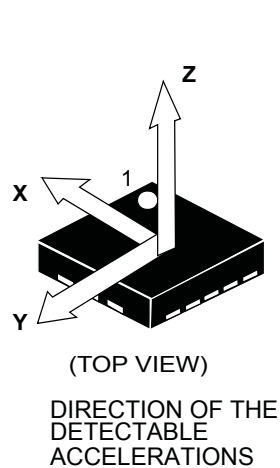


N2410 IC IF 3.5x3.5x0.8 thin QFN 1200-1951

Pin Configurations



N2411 ASIC 3-Axis Accelerometer 1204-5837

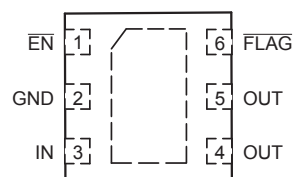


Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not Connected
3	NC	Not Connected
4	SCL SPC	I ² C Serial Clock (SCL) SPI Serial Port Clock (SPC)
5	GND	0V supply
6	SDA SDI SDO	I ² C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
7	SDO	SPI Serial Data Output I ² C less significant bit of the device address
8	CS	SPI enable I ² C/SPI mode selection (1: I ² C mode; 0: SPI enabled)
9	Reserved	Leave unconnected
10	Reserved	Connect to Gnd
11	INT	Inertial interrupt
12	GND	0V supply
13	GND	0V supply
14	Vdd	Power supply
15	Reserved	Connect to Vdd
16	GND	0V supply

N2421 IC ESD Prot UDFN 6 2x2 mm 1200-6309

PIN CONNECTIONS

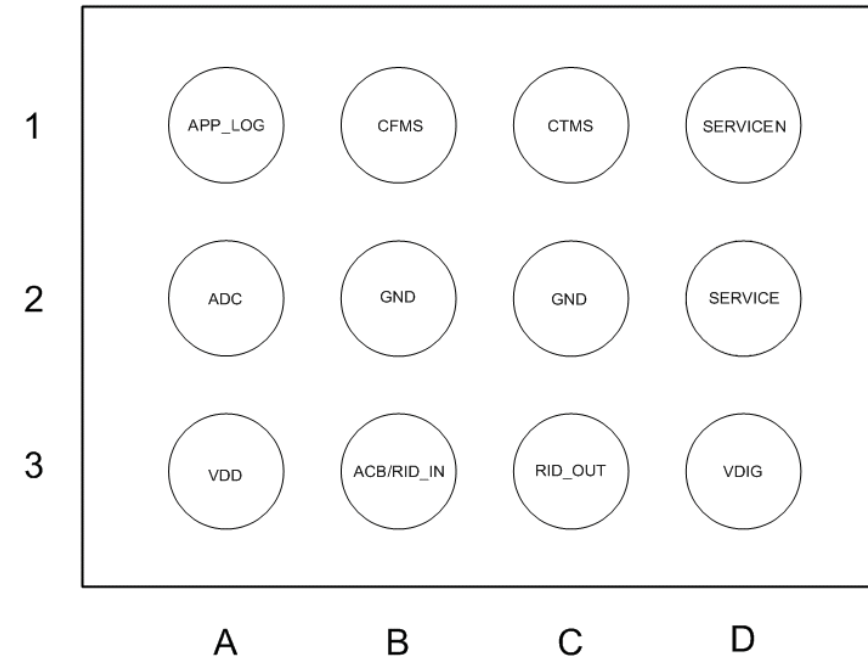


PIN FUNCTION DESCRIPTION

Pin No.	Name	Type	Description
1	EN	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the EN pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
2	GND	POWER	Ground
3	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 µF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
4, 5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 µF capacitor must be connected to these pins. The two OUT pins must be hardwired to common supply.
6	FLAG	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The FLAG pin goes low when input voltage exceeds OVLO threshold. Since the FLAG pin is open drain functionality, an external pull up resistor to V _{CC} must be added.

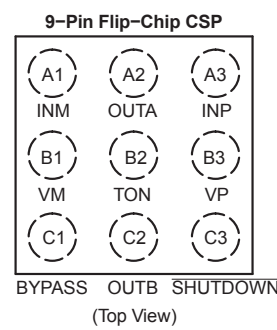
N2422 Asic Baseband 1201-4120

Pin-out, top view; bumps down.



N3100, N3102 IC Amp 9-pin Flip Chip CSP 1203-4594

PIN CONNECTIONS

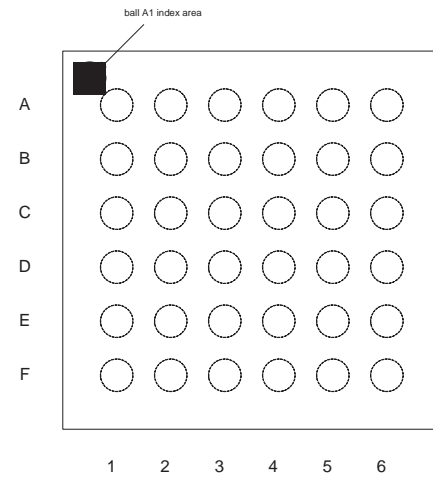


PIN DESCRIPTION

Flip-Chip	Name	Type	Description
A1	INM	I	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R _f and to the input resistor R _{in} .
A2	OUTA	O	Negative output of the NCP2991. Connected to the load and to the feedback resistor R _f .
A3	INP	I	Positive input of the first amplifier, receives the common mode voltage.
B1	VM	I	Analog Ground.
B2	TON	I	TON pin selects 2 different Turn On times: TON = GND -> 30 ms TON = VP -> 15 ms
B3	VP	I	Positive analog supply of the cell. Range: 2.2 V-5.5 V.
C1	BYPASS	I	Bypass capacitor pin which provides the common mode voltage (V _p /2).
C2	OUTB	O	Positive output of the NCP2991. Connected to the load.
C3	SHUTDOWN	I	The device enters in shutdown mode when a low level is applied on this pin.

N2420 IC IF ISP1508 ES3 (3.5*3.5*0.8) 1200-1694

Pin Diagram



ISP1508 TFBGA36 pinout (top view)

Pin Description

Symbol ¹	Ball No	Type ²	Description
RREF	C2	AI/O	Resistor reference. Connect through 12kΩ ±1% to GND.
DM	C1	AI/O	Connect to D- pin of the USB connector <ul style="list-style-type: none"> • USB mode: D- input/output • UART mode: TXD output
DP	D1	AI/O	Connect to D+ pin of the USB connector <ul style="list-style-type: none"> • USB mode: D+ input/output • UART mode: RXD input
FAULT	E2	I	Input for Vbus digital over-current or fault detector signal. If this pin is not in use, connect it to GND Plain input, 5V tolerant
ID	D3	I	identification (ID) pin of the mini-USB cable. If this pin is not in use, leave this pin open(there's internal pull-up). Plain input, TTL
VBUS	F4	AI/O	Connect to VBUS pin of the USB connector.
VCC	F3	P	Input supply voltage or battery source. Nominally 3.0V to 4.5V. Note: Below 3.0V, USB FS and LS transactions are not guaranteed to work though some devices may work with ISP1508 at these voltages.
PSW_N	D4	OD	Controls an external, active low VBUS power switch or charge pump. An external pull up resistor is required. Open drain,output, 5V tolerant.
REG3V3	E3	P	3.3V regulator output for USB mode or 2.7V regulator output for UART mode; requiring parallel 0.1 uF and 4.7 uF capacitors. Internally powers ATX and other analog circuits. Should not be used to power external circuits.
XTAL1	F5	AI/O	Crystal/clock input. 1.8V peak input allowed. Frequency depends on status on CFG1 and CFG2 pins.
XTAL2	F6	AI/O	Crystal output. If crystal is not in use, leave this pin open
CHIP_SEL	C3	I	Active HIGH chip select input. <ul style="list-style-type: none"> • When this pin is none-active, ULPI pins will be in 3-state and the chip

¹ Symbol names ending with underscore N (for example, NAME_N) indicate active low signals

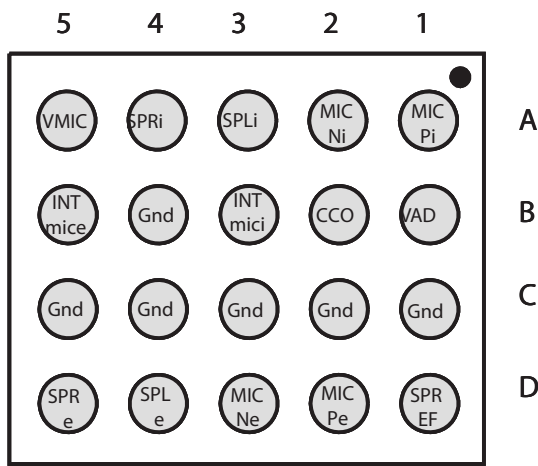
² I=input; O=output; I/O = Digital Input/Output; OD = Open Drain Output; AI/O = Analog Input/Output; P = Power or Ground pin

			is in power down <ul style="list-style-type: none"> • When this pin is active, ULPI pins will operate normally. If this pin is not in use, connect to VCC(I/O) directly. plain input
CFG0	E1	I	Select SDR/DDR operation <ul style="list-style-type: none"> • LOW: SDR • HIGH: DDR plain input
CFG1	B4	I	Select crystal/clock frequency with CFG2; see Error! Reference source not found. plain input
CFG2	B3	I	Select crystal/clock frequency with CFG1; see Error! Reference source not found. plain input
REG1V8	E6	P	1.8V regulator output; requiring parallel 0.1 uF and 4.7 uF capacitors. Internally powers the digital core. Should not be used to power external circuits.
DIR	E5	O	ULPI direction signal. Slew rate controlled output
STP	D6	I	ULPI stop signal. Push-pull input.
NXT	D5	O	ULPI next signal. Slew rate controlled output
DATA7	C6	I/O	ULPI data pin 7. Slew rate controlled output; Plain input.
DATA6	B6	I/O	ULPI data pin 6. Slew rate controlled output; Plain input.
DATA5	A6	I/O	ULPI data pin 5. Slew rate controlled output; Plain input.
DATA4	A5	I/O	ULPI data pin 4. Slew rate controlled output; Plain input.
VCC(I/O)	B2, B5	P	Input I/O supply voltage. 1.4V-1.95V. A 0.1 uF decoupling capacitor is recommended. Note: only SDR timing is possible for ULPI with VCC(I/O) < 1.65V
DATA3	A3	I/O	ULPI data pin 3. Slew rate controlled output; Plain input.
DATA2	A2	I/O	ULPI data pin 2. Slew rate controlled output; Plain input.
DATA1	A1	I/O	ULPI data pin 1. Slew rate controlled output; Plain input.
DATA0	B1	I/O	ULPI data pin 0. Slew rate controlled output; Plain input.
CLOCK	A4	I/O	60MHz clock output when crystal is attached or clock is applied on XTAL1 pin. Requires 60MHz clock input when a crystal is not attached. Slew rate controlled output; Plain input.
TEST	C4	-	Connect to VCC(I/O) directly for normal operation
NC	F1, F2	-	Not Connected.
GND	E4,C5,D2	P	ground supply.

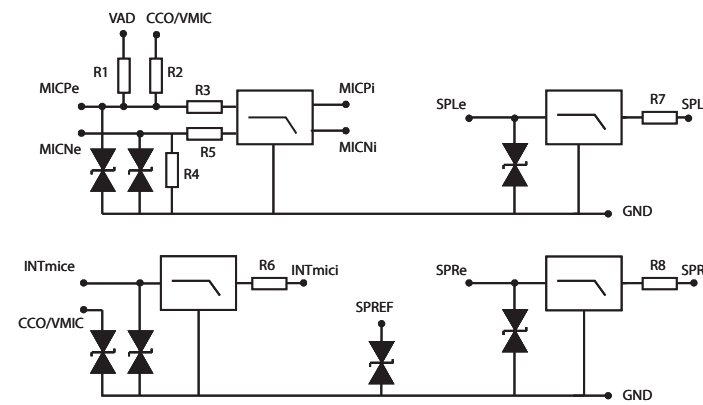
Pin Description for ISP1508

N3101, N3104 ASIC Tjatte 3 CSP20 ROP1013074/1R1A

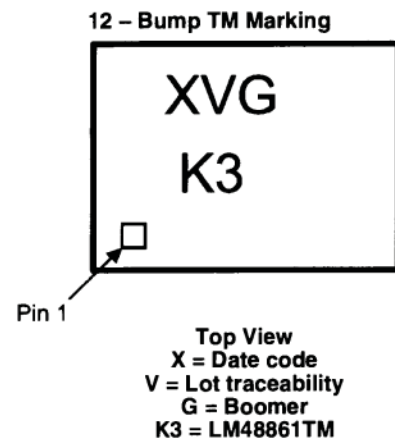
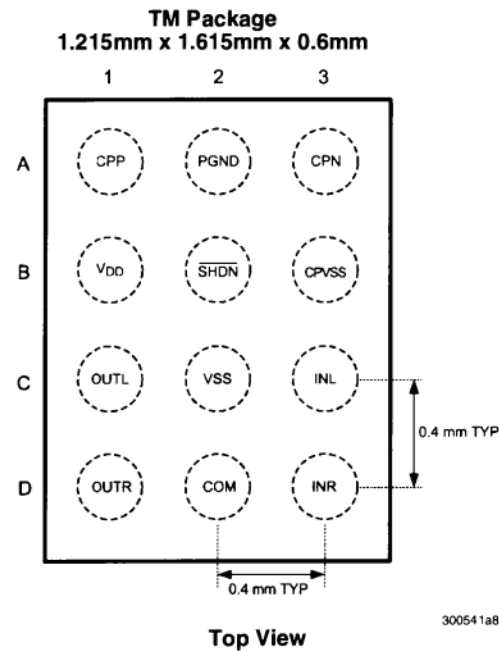
Pin configuration (Bump side)



Electrical diagram



N3103 IC Amp 1217-2694

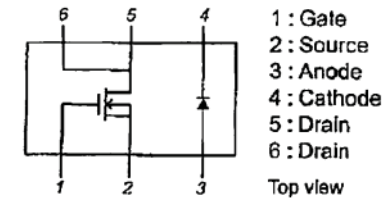


Bump Description

Bump	Name	Description
A1	CPP	Charge Pump Flying Capacitor Positive Terminal
A2	PGND	Power Ground
A3	CPN	Charge Pump Flying Capacitor Negative Terminal
B1	V _{DD}	Positive Power Supply
B2	SHDN	Active Low Shutdown
B3	CPV _{SS}	Charge Pump Output
C1	OUTL	Left Channel Output
C2	V _{SS}	Negative Power Supply
C3	INL	Left Channel Input
D1	OUTR	Right Channel Output
D2	COM	Ground reference for inputs and HP
D3	INR	Right Channel Input

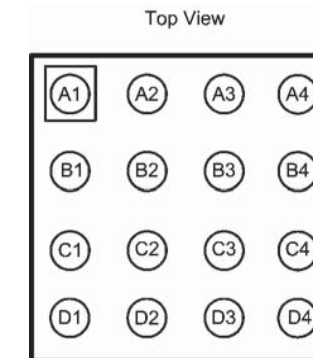
N4200 Trans N-ch FET RYN901936/1

Electrical Connection



N4401 IC Dri CS-16 1212-3512

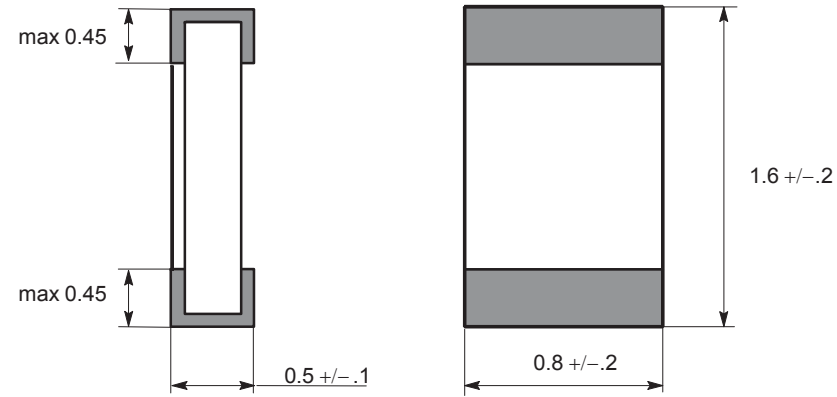
Connection Diagram



Pin Descriptions

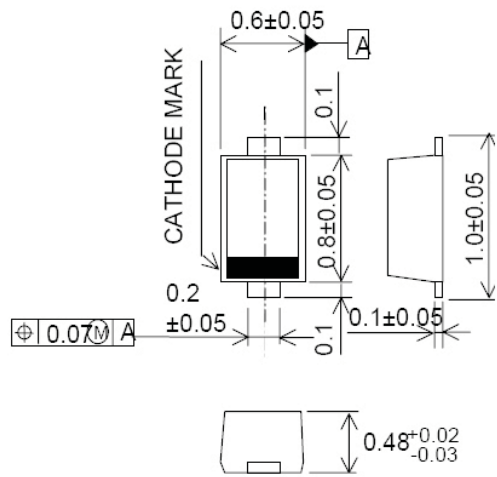
Pin	Name	Function
A1	LED1	High Side Current Source Output for Flash LED.
A2, B2	OUT	Step-Up DC/DC Converter Output.
A3, B3	SW	Drain Connection for Internal NMOS and Synchronous PMOS Switches.
A4, B4	GND	Ground
B1	LED2	High Side Current Source Output for Flash LED.
C1	LED1/NTC	LED Temperature Sensing .
C2	TX1/TORCH	Configurable as a RF Power Amplifier Synchronization Control Input or Hardware Torch Enable.
C3	STROBE	Active High Hardware Flash Enable. Drive STROBE high to turn on Flash pulse.
C4	IN	4.7µF ceramic capacitor.
D1	ENVM/TX2/GPIO	Synchronization Input.
D2	SDA	Serial Data Input/Output.
D3	SCL	Serial Clock Input.
D4	RESET /GPIO	Active Low Hardware Reset, or programmable general purpose logic input/output.

R2449, R2451, R2490 Resistor 0, Ohm +/-50m 63mW K0603 REP623001/0



V2200 Diode RKZ223911/1

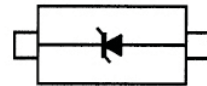
Unit in mm



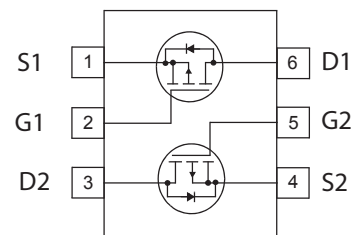
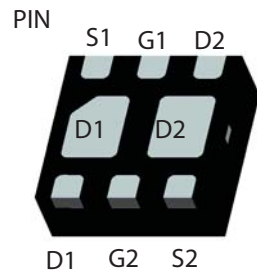
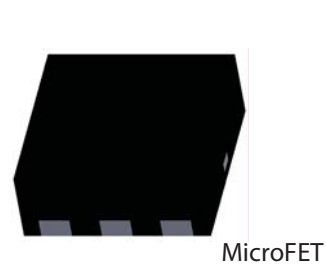
Marking



Equivalent Circuit (Top View)



V2202 Transistor 1200-0145

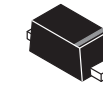


V2415-16 Diode 1201-8440

MARKING DIAGRAM



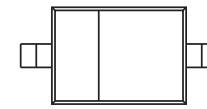
D = Specific Device Code
M = Date Code



SOD-923
CASE 514AB



V2417 Diode RKZ223905/2



Top view



MAM387

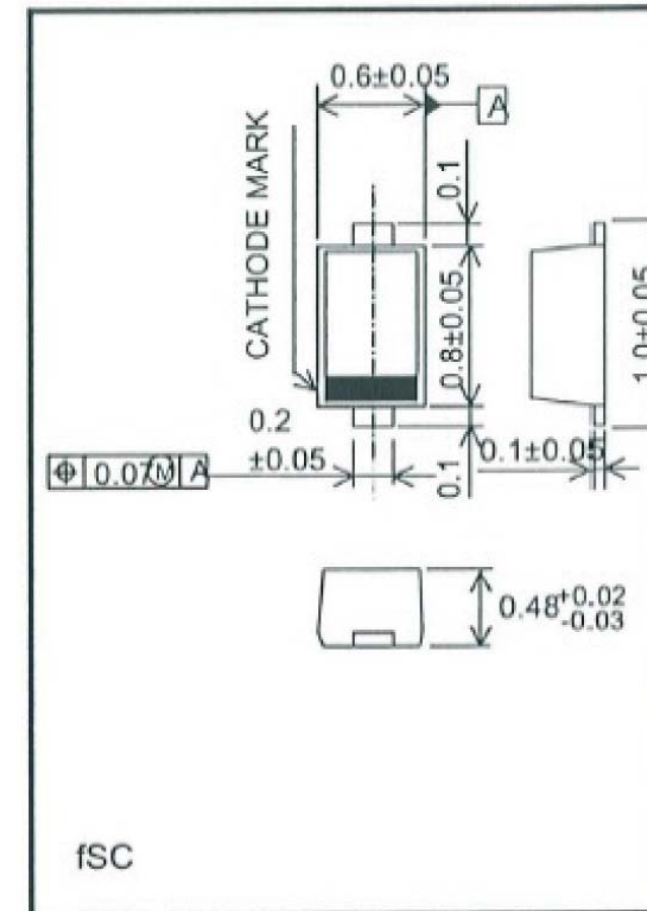
The marking bar indicates the cathode.

PINNING

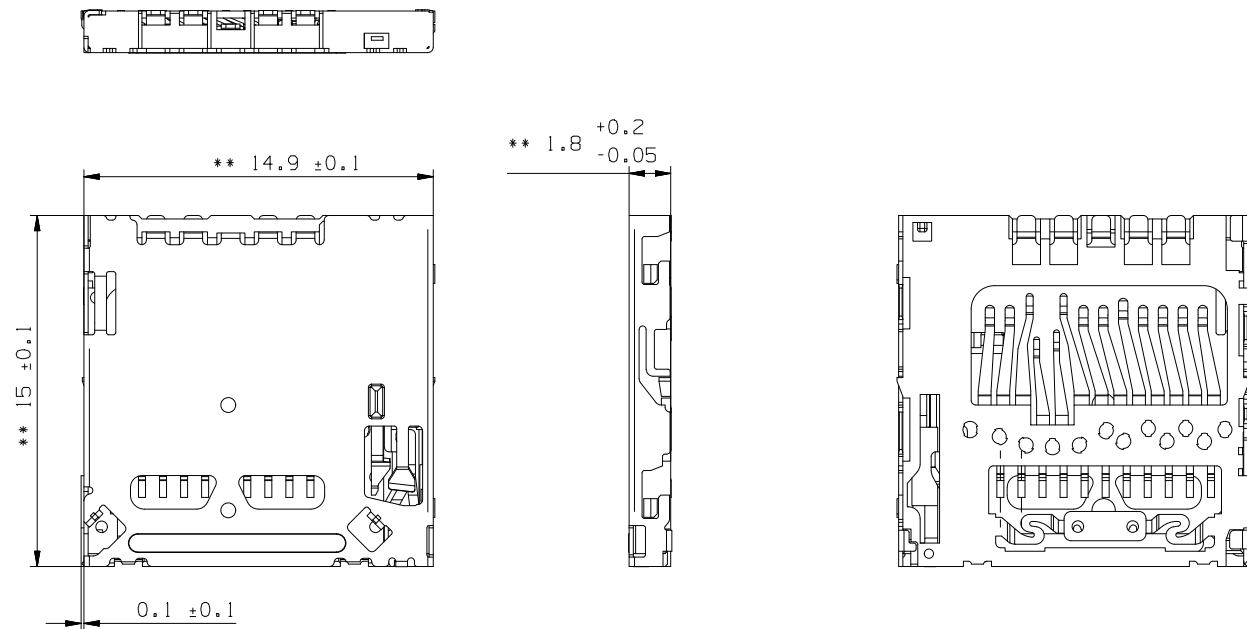
PIN	DESCRIPTION
1	cathode
2	anode

V3103 ZenerDiode, 5.6V, Pb-free RKZ223911/3

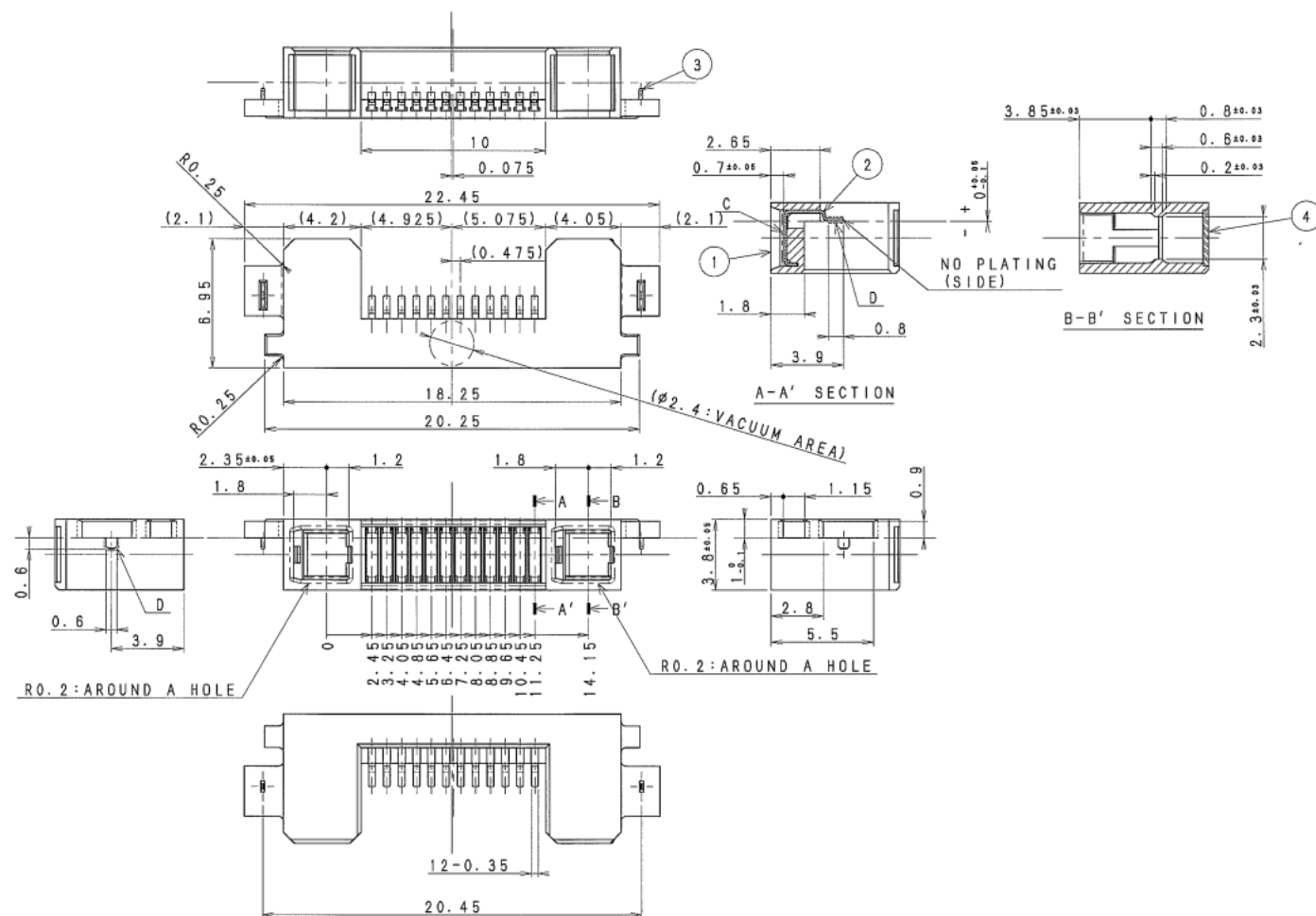
Unit in mm



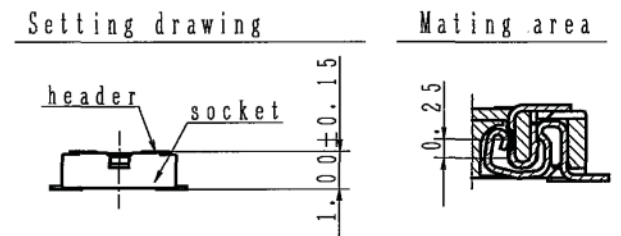
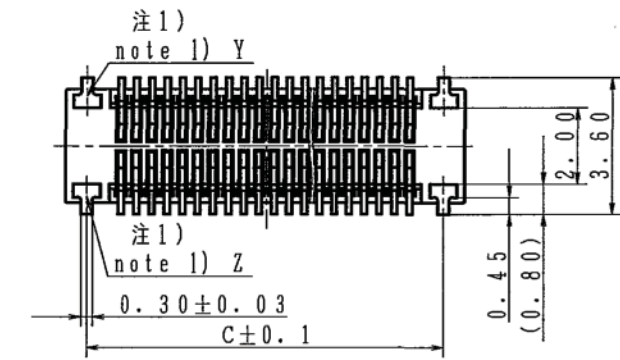
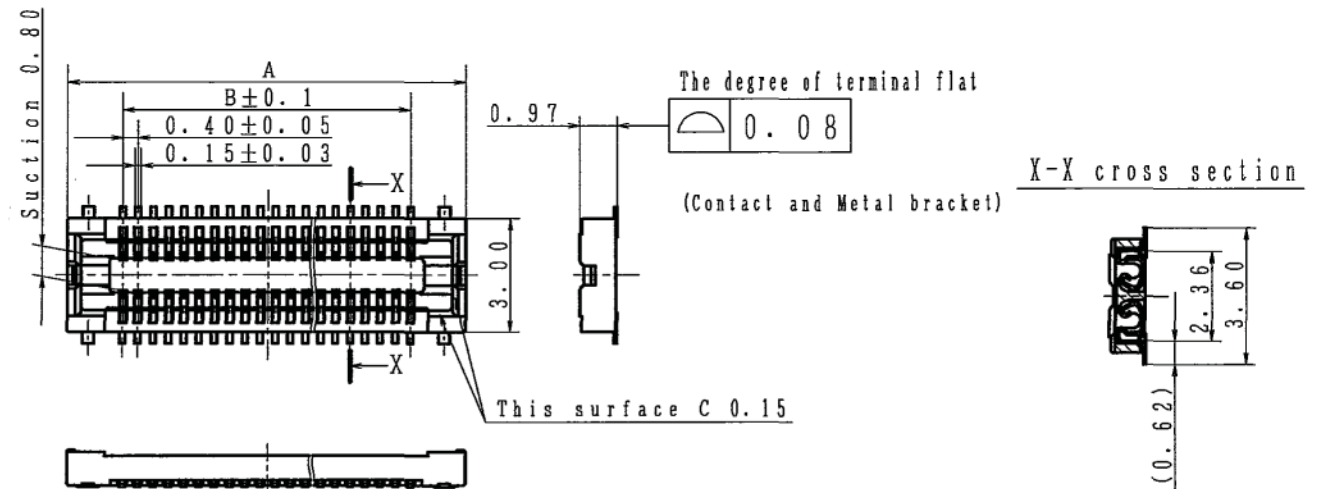
X2402 Memory Card Reader 1200-9764



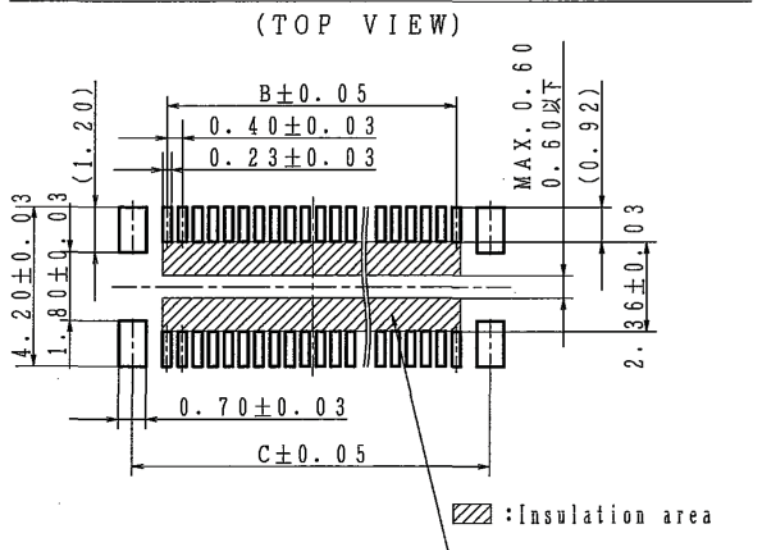
X2405 Connector 1210-0559



X2410 Conn BtB Receptacle 18p 1200-6752



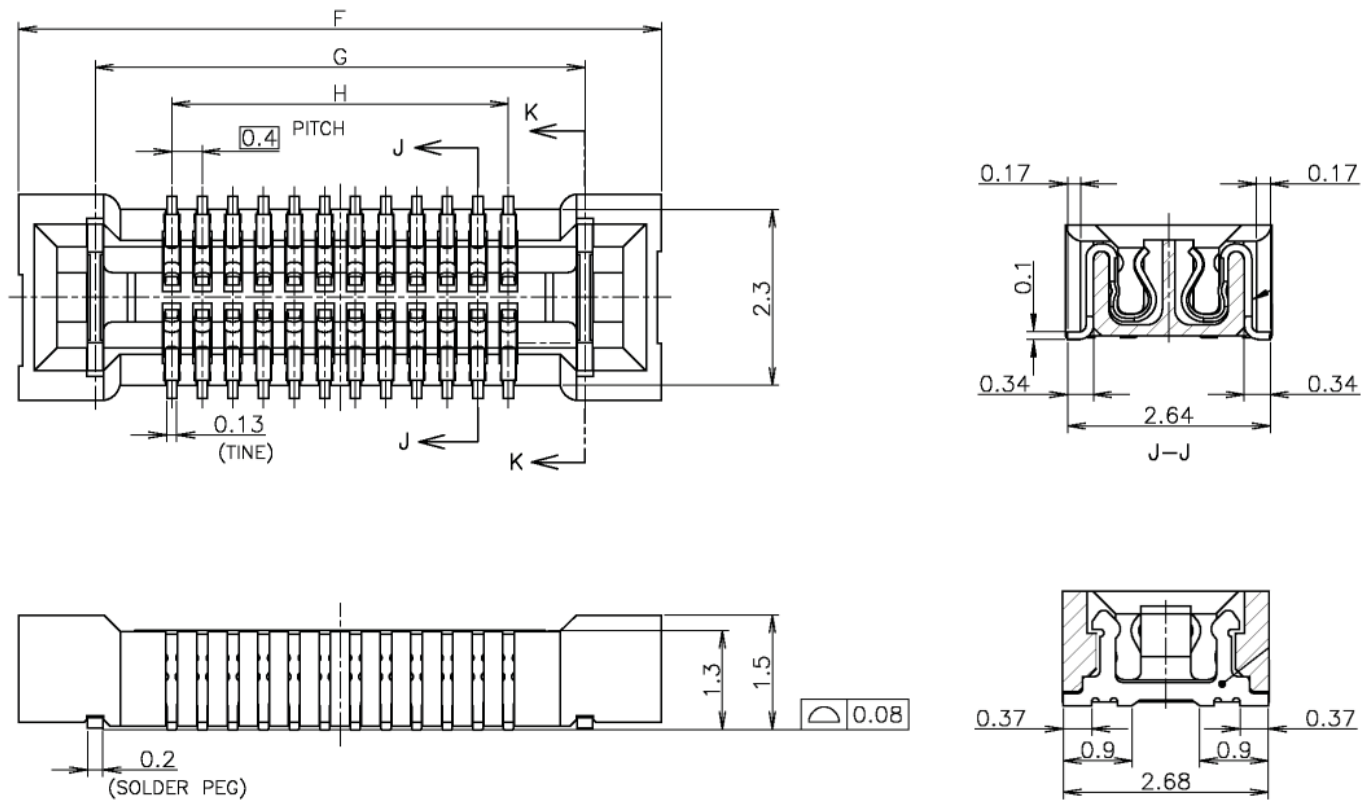
Recommended PC board pattern
(mounting pad layout)



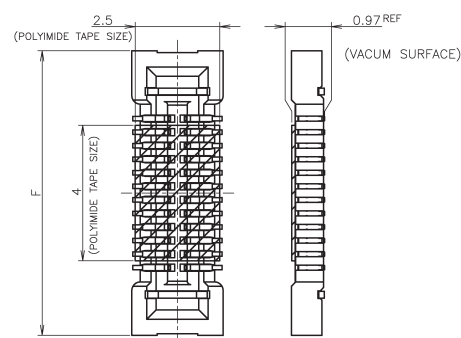
Dimension	A	B	C
No. of contacts			
10	4.5	1.6	3.4
12	4.9	2.0	3.8
16	5.7	2.8	4.6
18	6.1	3.2	5.0
20	6.5	3.6	5.4
22	6.9	4.0	5.8
24	7.3	4.4	6.2
26	7.7	4.8	6.6
28	8.1	5.2	7.0
30	8.5	5.6	7.4
32	8.9	6.0	7.8
34	9.3	6.4	8.2
36	9.7	6.8	8.6
38	10.1	7.2	9.0
40	10.5	7.6	9.4
42	10.9	8.0	9.8
44	11.3	8.4	10.2
46	11.7	8.8	10.6
48	12.1	9.2	11.0
50	12.5	9.6	11.4
54	13.3	10.4	12.2
60	14.5	11.6	13.4
64	15.3	12.4	14.2
70	16.5	13.6	15.4
80	18.5	15.6	17.4

Note 1) Because the metal bracket Y and Z are the unified structure, they are connected electrically.

X4300 Conn BtB Receptacle 70p 1206-2940

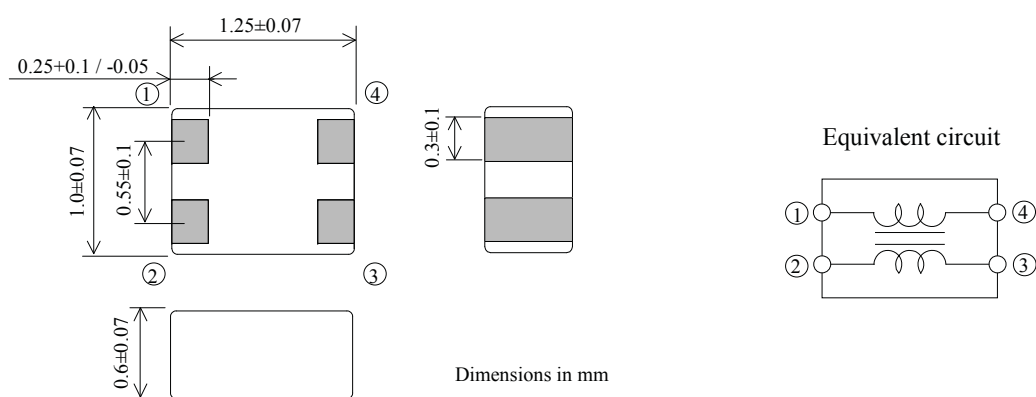


X4301 Conn BtB 30 pin 1200-1733

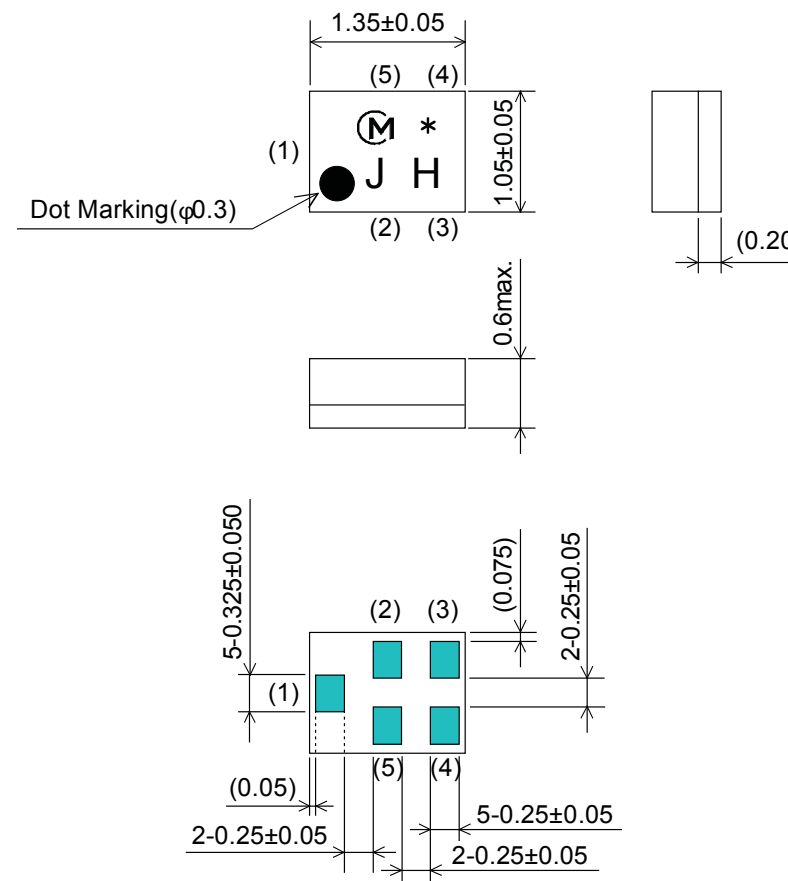


8-1747769-0	38.4	32.4	0.0606	15.6	17.2	19.6	19.9	16.9	14.2	28.4	32	8-2013134-0	80
7-1747769-0	30.4	24.4	0.0546	13.6	15.2	17.6	17.9	14.9	11.5	-	24	7-2013134-0	70
4-1747769-0	30.4	24.4	0.0366	7.6	9.2	11.6	11.9	8.9	11.5	-	24	4-2013134-0	40
3-1747769-0	30.4	24.4	0.0306	5.6	7.2	9.6	9.9	6.9	11.5	-	24	3-2013134-0	30
2-1747769-8	30.4	24.4	0.0294	5.2	6.8	9.2	9.5	6.5	7.5	-	16	2-2013134-8	28
2-1747769-4	22.4	16.4	0.0270	4.4	6.0	8.4	8.7	5.7	7.5	-	16	2-2013134-4	24
2-1747769-2	22.4	16.4	0.0258	4.0	5.6	8.0	8.3	5.3	7.5	-	16	2-2013134-2	22
2-1747769-0	22.4	16.4	0.0246	3.6	5.2	7.6	7.9	4.9	7.5	-	16	2-2013134-0	20
1-1747769-6	22.4	16.4	0.0222	3.6	4.4	6.8	7.1	4.1	7.5	-	16	1-2013134-6	16

Z2400 Filter 1201-6833



Z1400 Filter SAW 1.575 GHz 1211-5714



Marking : Laser Printing
 (M) : Manufacturer symbol
 * : EIAJ Code

Terminal (Surface) : Au
 thickness 0.5...1.0μm
 (Typ. 0.6μm)
 Terminal (Base) : Ni
 thickness 2.0...6.0μm
 (Typ. 4.0μm)

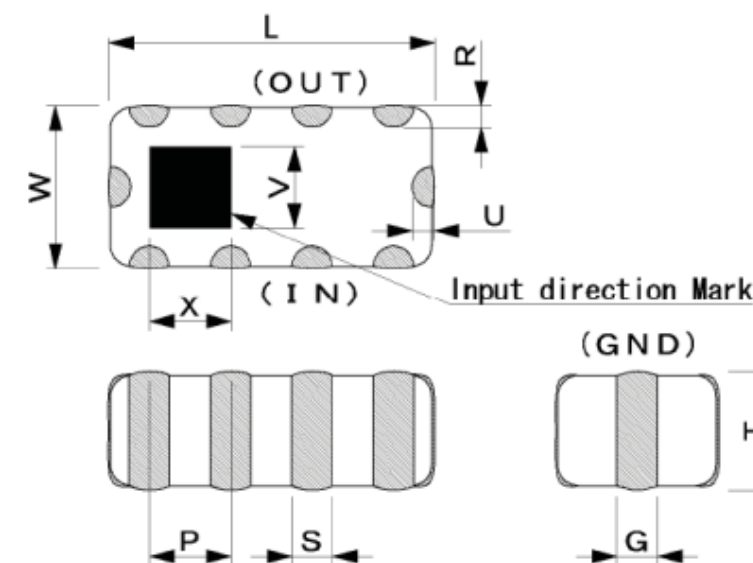
Terminal Number
 (1) : Unbalance Port
 (4) : Unbalance Port
 Others : Ground

Weight : 3.2±1.0mg

Coplanarity : 0.1mm max.

Unit : mm

Z4200-02 Filter 150.0 MHz 1221-4986



(Unit:mm)

Symbol	Dimmensions
L	1.60 +/- 0.08
W	0.80 +/- 0.08
T	0.50 +/- 0.10
P	0.40
S	0.20 +/- 0.075
G	0.20 +/- 0.075
R	0.01< ,(0.10 type)
U	0.01< ,(0.10 type)
V	0.40 type
X	0.40 type

NOTE ; Input direction mark of KNA16150C33MA is top side only.

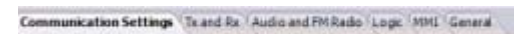
Troubleshooting Software Documentation

Introduction

Using this software you can control most parts and functions of all Sony Ericsson mobile phones. It is a GUI (**G**raphical **U**ser **I**nterface) for the commands implemented in the ITP (**I**ntegrated **T**est **P**rogram). The software communicates with the phone through standard serial communication over a USB/RS232 interface (SEPI).

Note: *The Troubleshooting Software application is to be used with the Troubleshooting Manual and the Troubleshooting fixture kit.*

The functions in the Troubleshooting Software application are divided into three main sections: **Communication Settings**, **Radio Control** and **Base Band Controls**. These main sections are presented under six different tabs.



All settings and functions are collected under these six main tabs.

Communication Settings

All settings for the communication between the Troubleshooting Software application and the phone are presented under the Communication Settings Tab.

Radio Controls

Note: *Some parts of Radio Control functions may not be implemented since they are not supported by the ITP SW.*

Note: *There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.*

All Radio Control Functions implemented in the Troubleshooting Software are presented under the **Tx and Rx** tab. The main radio functions of the mobile phone presented in this tab are:

- GSM radio part
- WCDMA radio part
- Bluetooth radio part

In the GSM and the WCDMA radio control part the following radio functions can be controlled: Transmitter (TX) and Receiver (RX)

In the Bluetooth radio control part only the Transmitter (TX) function is supported.

Base Band Controls

Note: *Some parts of Base Band Control functions may not be implemented since they are not supported by the ITP SW.*

Note: *There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available for all products.*

The functions for Base Band Control are presented under the following four different tabs:

Audio and FM Radio

Used for setting Audio Loop mode and test the functionality of the FM Radio.

Logic

Used to:

- Read out of the ADC channels
- Control or Test of SIM and Memory Stick Card
- Perform of Battery and Current Calibration
- Check Radio and Display temperature
- Etc.

GPIO Manager

Used to control GPIO ports at the Access and Application CPU.

Note: *It is very important to follow the GPIO activation sequence according to the Troubleshooting Guide instructions when the GPIO manager is used to avoid Hardware or SW function interruption.*

MMI

Used for:

- Main and VGA Camera Tests
- Camera Door Test
- Keyboard Scan Test
- Vibrator Test
- LED and Backlight Tests
- Xenon Flash Test
- Display Test
- Etc.

General

Used to:

- Read out Software and Product Data Information flashed into the phone
- Perform ASIC Revision test
- Perform available Self tests

Equipment Setup

Note: During calibration the accurate voltage from VBATT must be within ± 0.015 V. If this is not fulfilled it will cause a faulty calibration. For more information about recommended power supply units, see the Repair Tool Catalogue in CSPN under the Mechanical level. The Power Supply Channel 1 VBATT must allow reverse current.

Note: Before starting calibration test, the phone must be flashed with ITP Software.

Instructions for Customization of Power Supply Channel 2 DCIO/SEPI Cable

To perform Current Calibration the phone must be powered directly through the system connector. Customize the cable according to following instructions: Take the CST-75 battery charger and cut off the charger according to picture 1. **Length of the cable must be exact 1.3m.** Connect the CST-75 charger **Red** or **White** cable to the **Positive (+) Output** at Power Supply and the **Black** cable to the **Negative (GND) Output** at the Power Supply according to picture 2. Cut off isolation material from inside of the charger plug according to picture 3.

Picture 1



Picture 2



Picture 3



Power Supply Channel 2 DCIO/SEPI Cable Connection Setup

Note: The Power Supply Channel 1 (VBATT) must allow reverse current.

Note: The maximal cable length between the Power Supply Channel 1 VBATT and the dummy battery must not exceed 1m. The cable must have a capacity for at least 16A.

Picture 4



Correct DCIO and SEPI A1 Cable setup when the Troubleshooting Fixture is used.

Picture 5



Correct DCIO and SEPI A1 Cable setup when a Dummy Battery is used.

Picture 6



This setup between DCIO and SEPI A1 Cable is WRONG!

Note: Voltage and Current settings for the Power Supply Channel 1 VBATT and 2 DCIO/SEPI can be found in the Equipment List included in the Product Specific Troubleshooting Manual.

Note: Instructions about the Troubleshooting fixture connections with the External RF connector, Display, SIM Card, Memory Stick Card, Keyboard etc. can be found in Troubleshooting Fixture Connection Instruction included in the Product Specific Troubleshooting Manual.

System Requirements

Note: Before start using the Troubleshooting Software, the phone must be flashed with ITP SW.

The system requirements for running the application are:

- At least a Pentium III 500 MHz, with 128 MB of RAM
- Win2000 or Win XP
- One free USB connector
- USB Computer Cable
- At least 1024x768 display resolution. (1152x864 is recommended.)
- SEPI Drivers must be installed
- SEPI BOX
- SEPI A1 Cable
- Phone Specific Dummy Battery
- Phone Specific TRS Fixture
- CST-75 Charger cable
- One Dual or Two Single Channel Power Supplies

TX and RX - Tab

Communication Functions

Note: Some parts of the Communications functions may not be implemented since they are not supported by ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

GSM

GSM Mode Settings

Used for selecting of the GSM radio mode. The following Radio Modes are available:

- TX and RX Switched
- TX and RX Static

Note: In the TX Switched mode all parameters are available (Band, Channel and Power Level). In the TX Static mode the control of Power Level is hidden and the transmitter works with a predefined DAC value. This is done to protect the power amplifier against overheating.

GSM Radio Settings

Used for Channel and Power Level control of the selected GSM Band. The TX and RX frequency value for selected band and channel will be presented in the TX and RX frequency box.

1. Select the desired GSM band. Available options are **GSM 850** (Ch 128...251), **GSM 900** (Ch 1...124), **EGSM 900** (Ch 975...1023), **DCS 1800** (Ch 512...885) and **PCS 1900** (Ch 512...810).
2. Use default value or select desired channel.
3. Use default value or select desired power level.

Note: Any GSM band not used by the Mobile Phone will be unavailable in the GSM Radio Settings.

GSM RSSI measurements

This measurement is only possible to perform when RX Switched mode is selected. Use the Mobile Phone Tester instrument for feeding a signal to the mobile phone's receiver. For Instrument and Phone's settings go to Troubleshooting Manual – GSM Network problems.

1. Select RX Switched Mode.
2. Select desired GSM band and Channel.
3. Go to GSM RSSI Measurements and Start RSSI Test.

Note: The RSSI Test can be performed differently from product to product due to the limited ITP Software support.

WCDMA

Note: Unused WCDMA Bands will not be available in the WCDMA Radio Settings.

Note: For some products the TX and RX WCDMA Channels range can be reduced due to the limited product functionality or Test Instrument limitation. This is done to avoid wrong and incorrect measurement results.

Radio Settings

Used for TX and RX Channels control of the selected WCDMA Band. The TX and RX Channels frequency for selected band will be presented in the TX and RX frequency box.

1. Select the desired WCDMA band. Available options are **Band I** (TX Ch 9612...9888, RX Ch 10562...10838), **BAND II** (TX Ch 9262...9538, RX Ch 9662...9938), **BAND IV** (TX Ch 1312...1513, RX Ch 1537...1738), **BAND V** (TX Ch 4132...4233, RX Ch 4357...4458) and **BAND VIII** (TX Ch 2712...2863, RX Ch 2937...3088)
2. Use default value or select desired TX or RX channel.

Fast select channels

Set High Channel: The High Channel for selected WCDMA Band will be set by the Troubleshooting SW.

Set Mid Channel: The Mid Channel for selected WCDMA Band will be set by the Troubleshooting SW.

Set Low Channel: The Low Channel for selected WCDMA Band will be set by the Troubleshooting SW.

Modes

Max Pwr 23dBm set the Phone to transmit with maximum power at the selected Band and TX Channel. The limit is 23dBm.

Min Pwr Max -50dBm set the Phone to transmit with minimum power at the selected Band and TX Channel. The limit is -50dBm.

Read RSSI set the Phone in RX mode at the selected Band and RX Channel.

Out Pwr level x dBm set the Phone in TX mode at the desired power level value at the selected Band and TX Channel (Power level range to choose is: from -50dBm to 23dBm).

INP/OUT Pwr check set the Phone to transmit with maximum power and switch the receiver On at the selected Band and TX/RX Channel

Reset output set the Phone in WCDMA Off mode.

Rx on

Read measurement read the RSSI and report the result at Phone reported power. This function can only be used when the Receiver is On.

Note: *The RSSI Measurement can be performed differently from product to product due to the limited ITP Software support.*

VCO and VCXO Functions

Note: *These calibrations are only possible to perform when RX static mode is selected.*

Note: *These calibrations may not be possible to implement for all products due to limitations in ITP Software.*

VCO Calibration (TX)

Uses the default values in the TP to adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the TXVCO (measured with an ADC) is within the valid range and the optimal value is chosen. The optimal value is defined as: The CVCO value that gives loop voltages within the limits for both high and low channel and that has the lowest maximum loop voltage.

The optimum value is stored in GDFS.

VCXO Control

Used to fine tune the VCXO to **MCLK** frequency by calibrating the DAC that sets the VCXO control voltage. It is also used to verify the VCXO tuning range. When transmission is in Switched TX mode you are allowed to calibrate the VCXO oscillator controlling the DAC value on the AFC pin.

1. Switch the GSM tester to GSM900, Ch1.
2. Read the stored VCXO value from the GDFS by clicking the "**Read from GD**" button.
3. Start transmitting by clicking the "**TX Switched**" mode button.
4. To apply the VCXO DAC value you set, click the "**Set VCXO**" button.
5. Check your GSM tester.
6. Set the frequency error as close to 0 Hz as possible by using the up/down arrows and then click the "**Set VCXO**" button again.
7. The button "**Mean Value**" sets the value to 1024.
8. When the procedure is finished, click on "**Save VCXO**" button to store the calibrated value in GDFS.

VCO Calibration (RX)

Uses the default values in the TP to adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the RXVCO (measured with an ADC) is within the valid range, and the optimal value is chosen. The optimal value is defined as: The CVCO value that gives loop voltages within the limits for both high and low channel and that has the lowest maximum loop voltage.

The optimum value is stored in GDFS.

Audio and FM Radio - Tab

Audio & Radio Functions

Note: *Some parts of Audio and FM Radio may not be possible to implement for all products due to limitations in ITP Software.*

Note: *There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.*

Audio Loop Test

1. Select desired Audio Loop Test
2. Click "**Apply Audio Loop**" to start the test.
3. To switch off the loop, select **OFF** from **Audio Output** and click "**Apply Audio Loop**".

Audio input:

- **Mic1** is the internal microphone.
- **Aux1** is the input from the system connector.

Loop mode:

- **Analogue**, where the loop is set before and after the AD/DA conversions.
- **Digital/DSP** loop, where the DSP signal processing also affects to the audio signal.
- **CPU/PCM** loop, where the loop is set between the PCM audio signals.
- **Dictaphone** loop.

Audio output:

- **Earphone** is the internal Earpiece speaker of the unit.
- **AUX earphone** connected to the system connector.
- **Loudspeaker** is the internal loudspeaker of the unit.
- **OFF** is used to switch off the currently used Audio Loop.

Examples of different Audio Loop Test setups in Fault Trace SW.

Picture 9



K800 Project Setup

Picture 10



K850 Project Setup

Note: Audio output and input pins can be used by disconnecting the blue SEPI connector from the phone after the audio loop has been applied. Now the Portable Handsfree can be connected to the System Connector. After function test operation, disconnect the PHF or external audio device from the System Connector and connect the SEPI cable to proceed with other Audio Loop Tests.

FM Radio

- To activate the FM radio, click at the **Set FM Radio** button.
- To turn off the FM radio, click at the **Turn OFF FM Radio** button.

Audio output

Used for selecting Audio Output from the FM Radio. Most common Audio Outputs for all projects are AUX Stereo (Portable Handsfree, PHF) or Loudspeaker.

Frequency in MHz

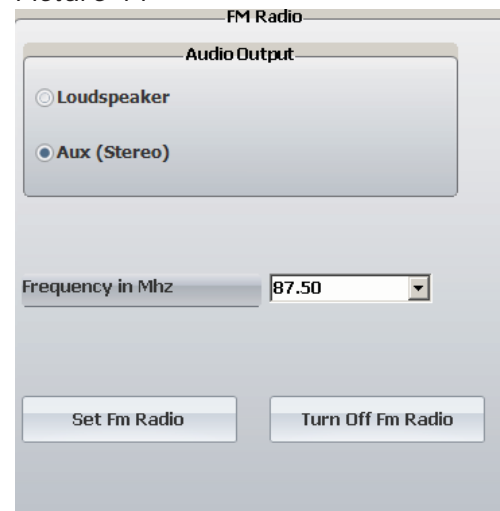
Frequency range box for the FM Radio. The frequency value can be selected in two different ways:

- The first one is with up/down spin buttons
- The second one is to type it directly into the Frequency field.

When typing directly into the Frequency field, the Frequency Span should be 100 KHz when changing from one frequency to another. The Frequency Range used in the Troubleshooting Software is from 87.50 MHz to 108.00 MHz.

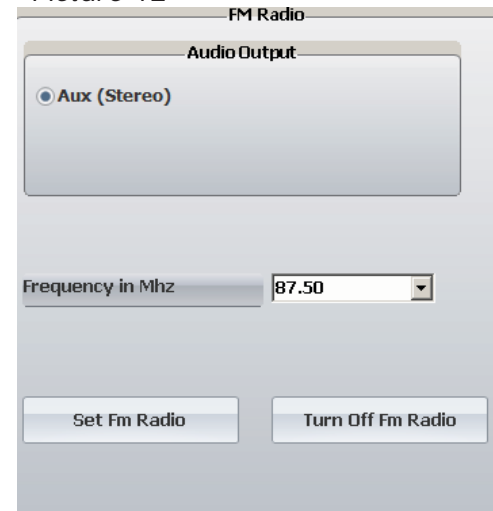
Examples of different FM Radio Test setups in the Troubleshooting Software

Picture 11



K850 Project FM Radio Setup

Picture 12



K800 Project FM Radio Setup

Logic – Tab

Logic Functions

Note: Some of the Logic functions may not be possible to implement for all products due to limitations in the ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

Battery Calibration

Note: To perform this test only Power Supply channel 1 is needed. Make sure that the correct voltage values are set for each test step, otherwise the test will fail.

The Battery Calibration test is similar to the Battery Calibration test performed in the factory environment.

1. Click **1. Battery Calibration.**
2. Click **SET VBATT to 3.2 Volt.**
3. Adjust Power Supply channel 1 (the dummy battery) to 3.2 V.
4. Click **VBAT1.**
5. Click **SET VBATT to 4.1 Volt.**
6. Adjust Power Supply channel 1 to 4.1 V and click **VBAT2.**
7. Adjust Power Supply channel 1 to 3.8 V and click **SET VBATT to 3.8 Volt.**
8. The test result (**Passed** or **Failed**) will now be displayed.

When the measured values are within the limits the calibration will be passed otherwise the test will be failed. The compensation factor will be calculated and stored in the GDFS.

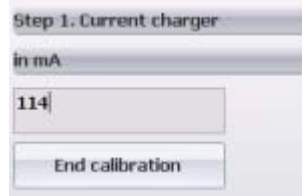
More information about the test limits can be found in the product specific Troubleshooting Manual and in the **Read Limits Table** in the **Battery and Current Calibration Test** document.

Current Calibration

The Current Calibration test is similar to the Current Test for the charging algorithm in the factory environment.

Note: For a correct and accurate result, perform the **Battery Calibration Test** before current calibration. To perform this test you will need both channel 1 and 2 from the Power Supply.

1. Click **2. Current Calibration**.
2. Adjust channel 1 (the dummy battery) to 3.8 V.
3. Click button **SET VBATT to 3.8 Volt**.
4. Note the measured current for channel 2 (the customized charger with SEPI).
5. Type in the measured current (in mA) in the text box.



In this example the current is measured to 114 mA.

6. Press **Enter**.
7. The phone will switch to charging with 800mA. Note the measured current value result at Power Supply Channel 2 DCIO/SEPI.
8. Type the new value in the text box.
9. Press **Enter**.
10. The test result (**Passed** or **Failed**) will now be displayed.

When the measured values are within the limits the calibration will be passed otherwise the test will be failed. The compensation factor will be calculated and stored in the GDFS.

More information about the test limits can be found in the product specific Troubleshooting Manual and in the **Read Limits Table** in the **Battery and Current Calibration Test** document.

ADC Values

1. Select the desired ADC Channel.
2. Click **Read ADC value**.

- The measured value will be presented in both hex and decimal info boxes.
- N/A means that the General Purpose port is not used by this phone or this port is not supported by ITP.
- If a port is missing in the Troubleshooting SW that port is not supported by the ITP SW.

SIM Card Control

This section controls the SIM interface in the phone.

SIM VCC: Voltage for the SIM Card will be activated.

SIM RESET, SIM DATA and **SIM CLOCK:** Activate the Reset, Data and Clock signals for the SIM Card.

SIM Com Test: Checks the communication with the SIM Card.

The test result (**Passed** or **Failed**) will be displayed in the info box.

Note: A SIM card must be inserted and a card reader connected to run this test.

Memory stick test checks the communication with the Memory stick card.

The test result (**Passed** or **Failed**) will be displayed in the info box.

Note: A Memory stick card must be inserted and a Memory card reader connected to run this test.

End Calibration

Ends the calibration and no data will be stored.

Go Idle for 2 sec

The unit will be set to IDLE mode for 2 seconds.

Reboot Phone

IPT command **KILL** will be send and the phone will restart.

Radio Temperature

The value of the Radio Temperature will be displayed in the info box.

Display Temperature

The value of the Display Temperature will be displayed in the info box.

GPIO Manager Functions

Set GPIO port at Access and/or Application CPU to High or Low and Read Out status of the port.

MMI – Tab

Functions

Note: Some parts of MMI functions may not be possible to implement for all products due to limitations in the ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

Display Pattern

Activate different test patterns on the display.

LED and Backlight

Activate/Deactivate LEDs and Backlights on the phone.

Misc

Activate/Deactivate tests such as:

- Main Camera Test
- VGA Camera Test

- Camera Door Test
- Vibrator Test
- Keyboard Scan Test
- Etc.

Note: *When one test has been deactivated the phone will be restarted.*

General – Tab

Functions

Note: *Some parts of General functions may not be possible to implement for all products due to limitations in ITP Software.*

Note: *There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.*

Software Information

This function is used to display the following information stored into the phone:

- ITP version
- IMEI number
- OTP number
- CID number
- PAF status
- Lock Status
- Etc.

Note: *The OTP number must match the IMEI number otherwise the IMEI has been changed.*

Note: *Some of these functions may not be available for all products due to security reasons.*

Product Data

This function displays production data stored in the phone, such as:

- First Identification (Serial Nr.)
- PBA Nr.
- PBA Rev.
- DPY Nr. (Sales Unit)
- Etc.

ASIC Revisions

This function displays the types and revisions of the different ASICs. To find out more information about which components are included in this test go to the **ASIC Revision Test** document **included in** the product specific **Troubleshooting Manual**.

Self Test

This function runs available self tests on the Phone.

1.

...timeout when reading

Check the following items:

- Connection between Power Supply Channel 2 (DCIO) and SEPI A1 cable (See picture 4, 5 and 6).
- If the SEPI BOX works properly (The Green LED at the SEPI BOX must be on).
- If the USB cable between SEPI BOX and PC is connected properly.
- If the phone has been flashed with the correct ITP version.
- If VBATT and DCIO Power Supply instruments are on.

2.

...timeout when writing ...timeout when reading

Check if the correct COM Port is selected in Troubleshooting Software - Communication Settings Tab

3.

...Port has not been successfully opened timeout

- Check if COM Port is connected
- Check if the correct Phone Project File is loaded
- Restart the Troubleshooting Software application and try again

4.

Command failed due to:

.... **Error_InvalidParameter, ERR**

or

CERR: Error_CommandDoesNotExist, ERR

- Check if the correct Phone Project File is loaded
- Check if the phone has been flashed with the correct ITP version.

Troubleshooting Fixture Setup Instructions

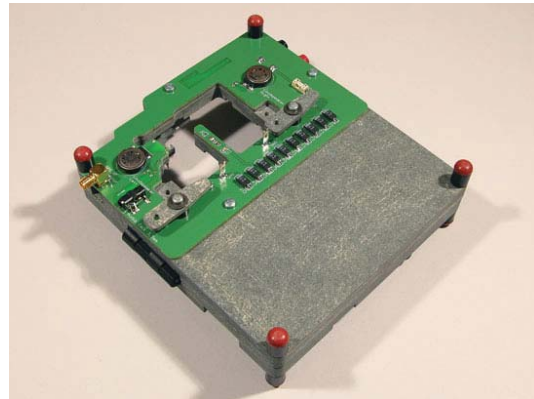
Top-part overview of the TRS Fixture, see picture 1.

Picture 1



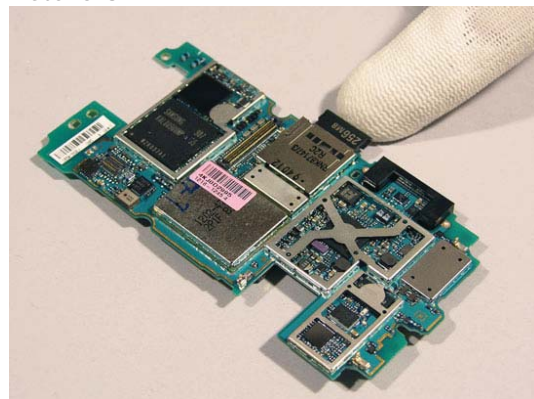
The Bottom-part overview of the TRS Fixture, see picture 2.

Picture 2



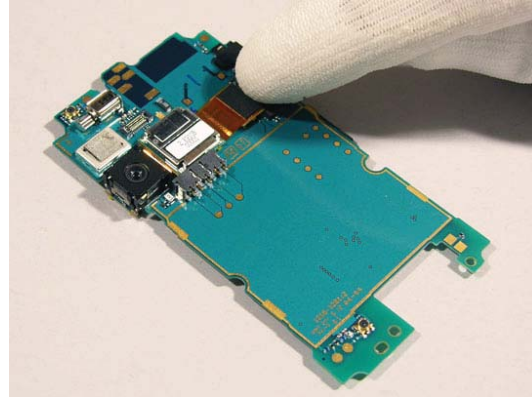
Insert Memory Card if needed according to picture 3.

Picture 3



When the Camera 8 MPixel CMOS is in use, connect it directly to the PBA according to picture 4.

Picture 4



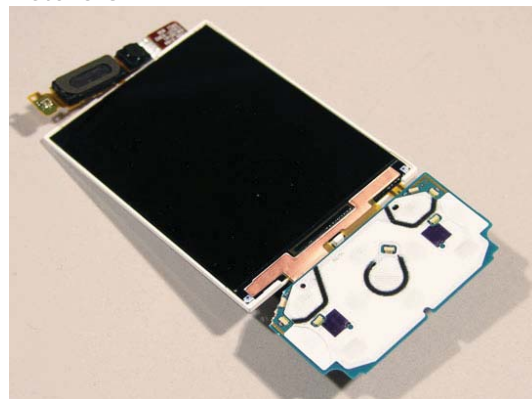
When the SIM Card is in use then connect the SIM Flex Assy directly to the PBA according to picture 5.

Picture 5

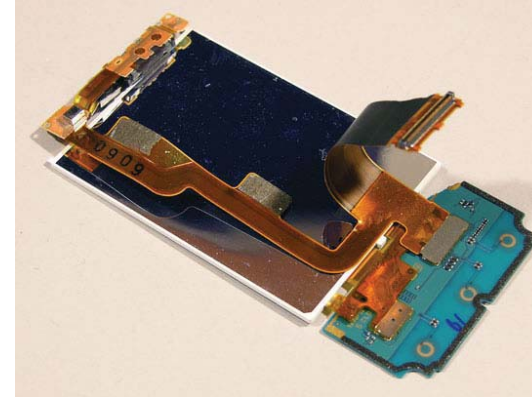


Connect Slider Flex Assy, PBA Navi Key, VGA/VTF Camera and the Display according to pictures 6 and 7.

Picture 6

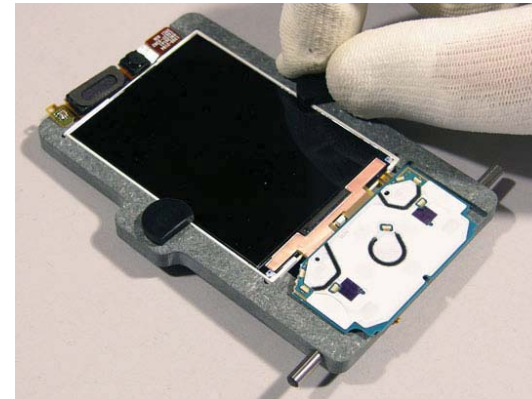


Picture 7

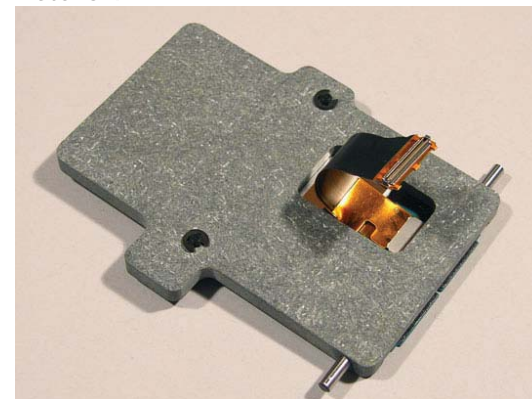


Place Slider Flex Assy, PBA Navi Key, VGA/VTF Camera and the Display into the TRS Fixture Display Holder and secure by using the locking screws, see pictures 8 and 9.

Picture 8

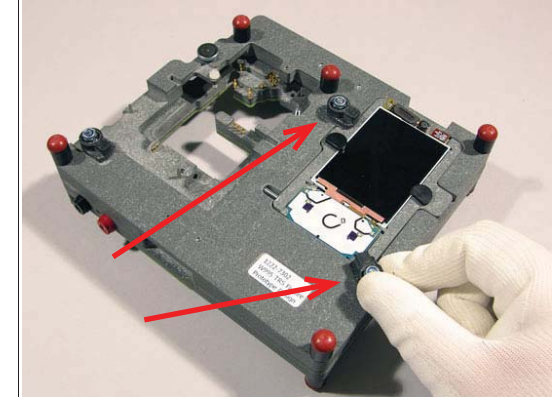


Picture 9



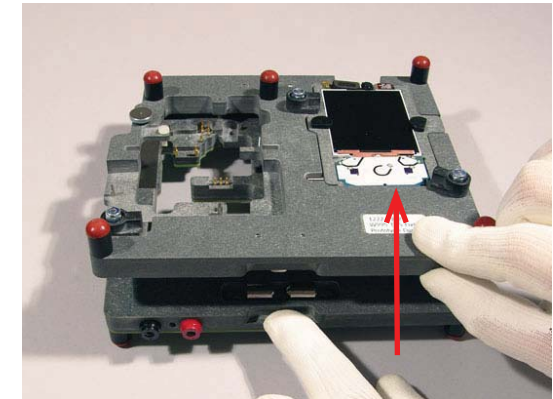
Place the TRS Fixture Display Holder into TRS Fixture and secure by using the locking screws according to picture 10.

Picture 10



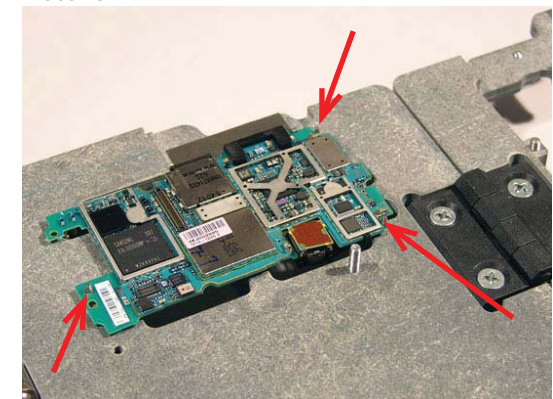
Open the TRS Fixture according to picture 11.

Picture 11



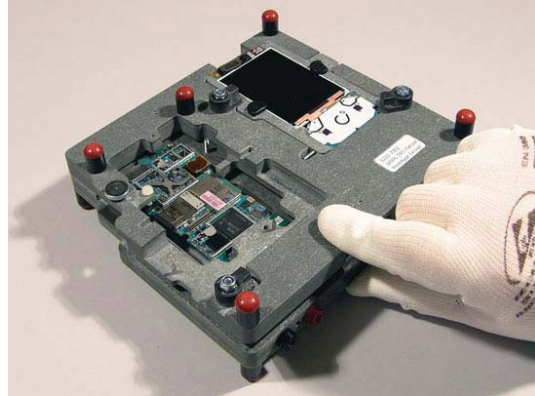
Place the PBA by using the Guide Pin mounted inside the TRS Fixture according to picture 12.

Picture 12



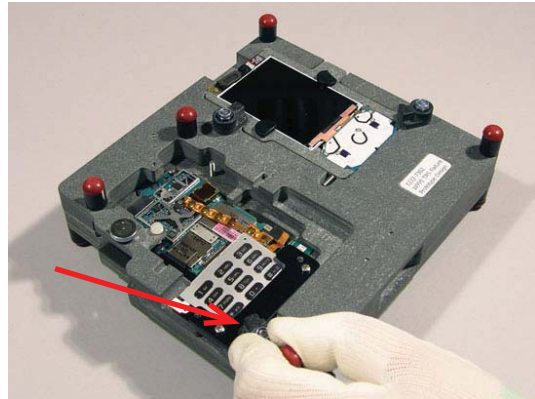
Close the TRS Fixture according to picture 13.

Picture 13

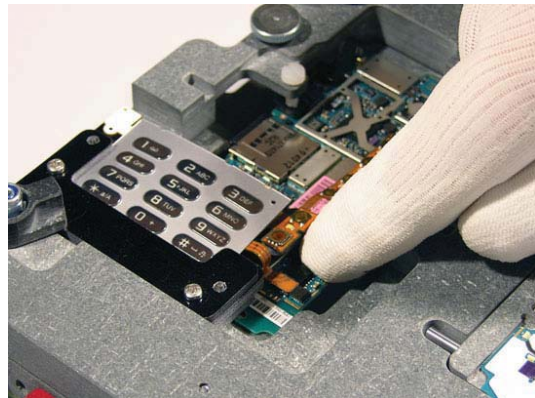


Connect the TRS Fixture Keyboard Holder with the Key Flex Assy directly to the PBA when the Keyboard is in use according to pictures 14 and 15.

Picture 14



Picture 15



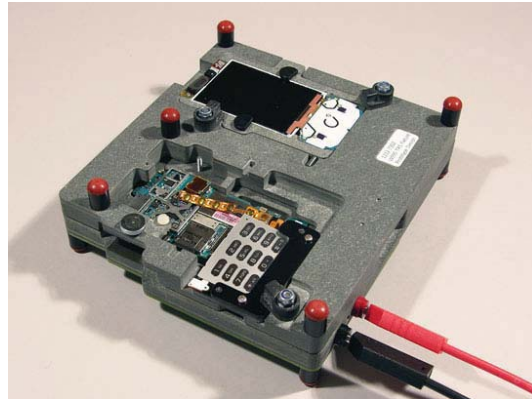
When using the Display, Navigation Keypad, Earphone, VGA-VTF Camera then use the TRS Fixture Display Holder and connect the Slider Flex Assy directly to the PBA see picture 16.

Picture 16



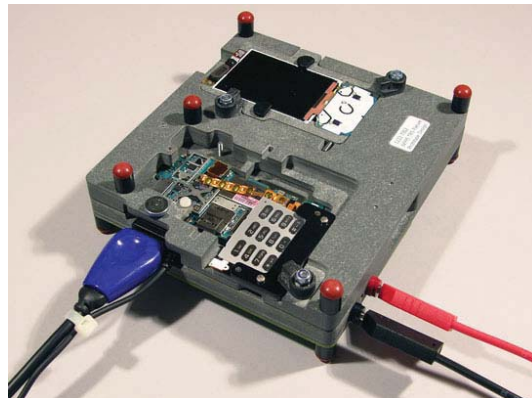
Connect Power Supply Channel 1 (VBATT) Black and Red Lab Plugs to the TRS Fixture according to picture 17.

Picture 17



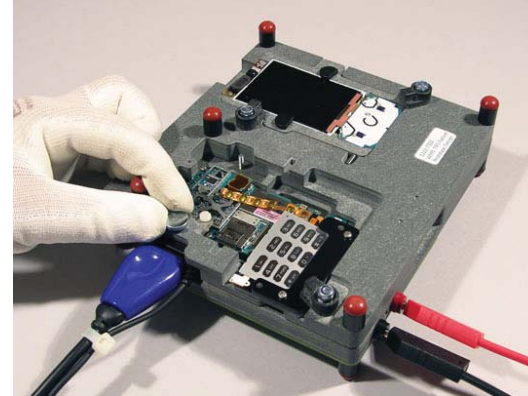
Connect the Power Supply Channel 2 Cable (DCIO/SEPI) according to picture 18.

Picture 18



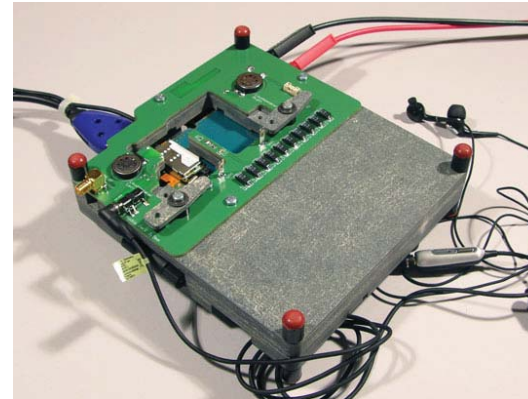
Secure the DCIO/SEPI Cable by using the locking screw according to picture 19.

Picture 19



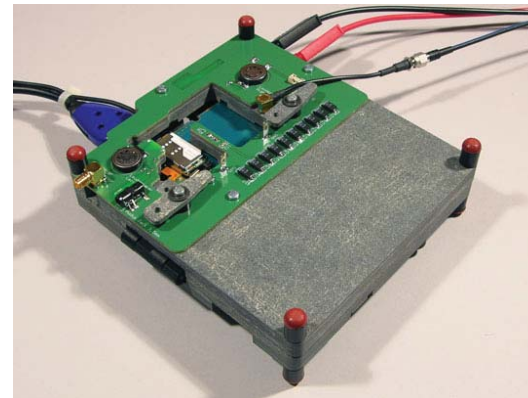
When the Audio Jack is in use then insert Hands-Free (PHF) Set with the 3.5mm Stereo Plug into the TRS Fixture 3.5mm Audio Jack according to picture 20.

Picture 20



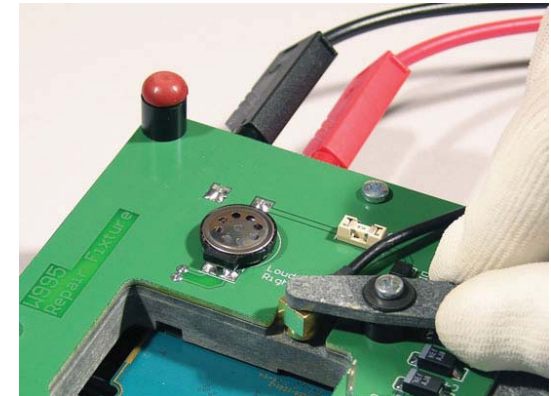
Connect the RF Cable Flexible with SMK RF Probe to the X1200 RF Switch according to picture 21.

Picture 21



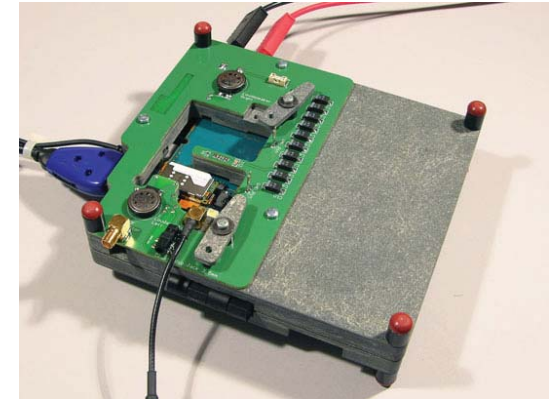
Secure the SMK RF Probe with the RF Probe locking device according to picture 22.

Picture 22



Connect the RF Cable Flexible with SMK RF Probe to the X1500 RF Switch according to picture 23.

Picture 23



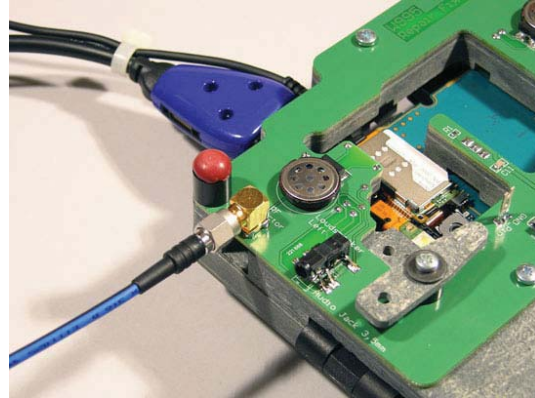
Secure the SMK RF Probe with the RF Probe locking device according to picture 24.

Picture 24



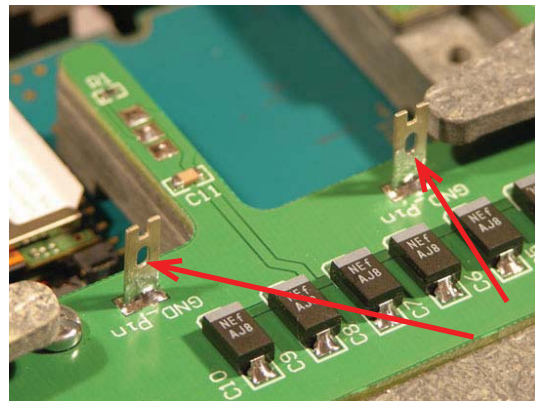
Connect the RF Cable Flexible to the GPS_RF Connector on the TRS Fixture according to picture 25.

Picture 25



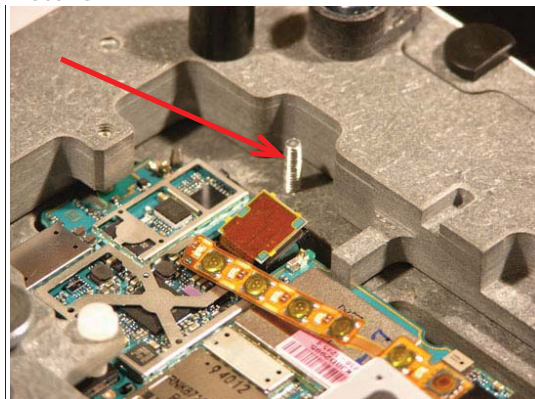
The PINs marked with GND text on the Bottom-part of the TRS Fixture can be used as an MP TRS Fixture GND or grounding for the oscilloscope probe, see picture 26

Picture 26



The PIN mounted inside TRS Fixture can be used as an MP TRS Fixture GND or grounding for the oscilloscope probe see picture 27.

Picture 27



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